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Microwave and Millimeter-Wave Communication Circuits in Silicon-Germanium BiCMOS Technologies

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Eric Christopher Wagner

Committee in charge:

Professor Gabriel Rebeiz, Chair
Professor Peter Asbeck
Professor Gert Cauwenberghs
Professor William Hodgkiss
Professor Daniel Sievenpiper

2019

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Chair

University of California San Diego

2019

EPIGRAPH

Only the paranoid survive.

-Andrew Grove

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Chapter 3, in full has been submitted for publication of the material as it may appear in *IEEE Trans. Microw. Theory Techn.*, E. Wagner and G. M. Rebeiz, “Packaging Effects on Stability in Millimeter-Wave Silicon Amplifiers”. The dissertation author was the primary investigator and author of this paper. The author would also like to thank Analog Devices for technical discussion and project funding, and Integrand Software for supplying licenses for EMX electromagnetic modeling software.

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E. Wagner and G. M. Rebeiz, “An 8-Way Combined E-Band Power Amplifier with 24 dBm Psat and 12% PAE in 0.12 μm SiGe,” in *Proc. 2018 IEEE MTT-S Int. Microw. Symp. (IMS)*, Philadelphia, PA, June 2018. pp. 1342-1344.

E. Wagner and G. M. Rebeiz, “A 9.4 - 11.7 GHz VCO in 0.12 μm SiGe BiCMOS with -123 dBc/Hz Phase Noise at 1 MHz Offset for 5G Systems,” in *Proc. 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Philadelphia, PA, June 2018. pp. 16-19

E. Wagner and G. M. Rebeiz, “Single and Power-Combined Linear E-Band Power Amplifiers in 0.12 μm SiGe With 19-dBm Average Power 1-GBaud 64-QAM Modulated Waveforms,” in *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 4, pp. 1531-1543, April 2019.

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ABSTRACT OF THE DISSERTATION

Microwave and Millimeter-Wave Communication Circuits in Silicon-Germanium BiCMOS Technologies

by

Eric Christopher Wagner

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2019

Professor Gabriel Rebeiz, Chair

The continued public demand for faster wireless data transfer, and the related expanding volume of mobile data traffic have led cellular network designers to envision new fifth-generation (5G) mobile networks which will leverage the large instantaneous bandwidths available within the microwave and millimeter-wave (mm-wave) frequency spectrums to achieve data-rates in the order of gigabits per second. The research presented in this dissertation will explore the design of two radio blocks which become especially challenging when moved to 5G bands: the power amplifier (PA) and frequency synthesizer. Using 0.12 μm SiGe BiCMOS technology, examples of both blocks were designed and demonstrate measured power and noise performance suitable for 5G systems. Practical challenges related to the stability and detuning of mm-wave amplifiers after packaging are also explored. Mitigation strategies are presented

and the proper assembly of the PA circuits onto a low-cost printed circuit-board (PCB) such that detuning and oscillations are avoided is demonstrated.

Chapter 1

Introduction

1.1 Background

Cellular communications have existed in the United States since at least 1983 when Bell Laboratories deployed its first cellular infrastructure in Chicago. This system, dubbed the "Advanced Mobile Phone System" (AMPS), was by today's standards exceptionally primitive. The system transmitted voice data through analog modulation schemes and relied on frequency-division multiple access (FDMA) to support concurrent users, making it comparable to AM radio which had already existed for decades before the advent of mobile telephony. Despite its initial limitations, cellular communications would prove popular and, in the 1990's second-generation (2G) cellular services would emerge in the US, Europe, and Asia. Enabled by the ever-improving capabilities of digital CMOS technology, 2G and all future systems would use entirely digital modulation schemes. 2G would also be the first to leverage time and code-division multiple access to improve spectral efficiency and allow more concurrent users per base-station.

With the success of 2G and the increasing demand among the general public for mobile data, it became clear that 2G would need to be replaced by a system that could support the growing trend in data usage. 3G was launched in the early 2000's and initially offered data rates ranging roughly between 2 and 0.2 Mbps, with phone operating frequencies between 0.9 and 3 GHz. During the reign of 3G the number worldwide mobile telephone subscriptions grew to the billions. Cellular phones and the instantaneous connectivity they afforded was now a fact of life for a huge (and still expanding) portion of the world's

population.

As the cellular market continued to grow, so too did its technology. The 2010's saw the launch of 4G which allowed further increases to mobile data rates through the use of new techniques such as multiple-input multiple-output (MIMO) antenna systems and orthogonal frequency-division multiplexing (OFDM). 4G, which is the current generation of cellular network as of the writing of this dissertation, has enabled the proliferation of smart-phones, a technology that has been profoundly influential in the daily lives of nearly everyone in the modernized world. Beyond phone calls, smart phones offer their users access to internet browsing, location tracking, gaming, music and video streaming, and financial transactions; and the proliferation of these devices has made practical new industries such as ride-sharing, which depends heavily on their location tracking, data, and voice transmission features.

The next generation of cellular infrastructure will be the fifth, and it will have the task of meeting the ever-rising public demand for faster and more reliable data transfer. In order to accomplish this task, plans are for 5G to move outside the traditional cellular frequency bands below 6 GHz and into the microwave and millimeter-wave (mm-wave) bands around 28, 39, and above 60 GHz (exact frequencies vary based on country, but all are near the mentioned bands). Moving to these frequencies will afford higher bandwidths, resulting in higher data rates and the possibility of gigabit per second wireless data transfer, however the challenges of designing higher frequency systems will come hand-in-hand with the benefits. Traditionally, communications at microwave and mm-wave frequencies has suffered from the scaling in the antenna's size which must be around one-quarter of a wavelength in order for the antenna to be an efficient radiator. Smaller antenna sizes, while beneficial for the beleaguered phone designer who must integrate multiple antennas into the small package of a phone, also lead to a reduced area for collecting desired signal power, leading to weaker transmission over a given distance when compared with a lower frequency system. To offset this effect, most proposed 5G architectures will leverage antenna arrays which effectively increase the gain and directivity of the radiating aperture. On the circuit side, the use of array antennas also offers challenges, requiring that a transmit/receive path with signal phase and amplitude control be integrated behind each antenna element, greatly increasing system complexity.

Despite the technical challenges, it has been clear for several years already that 5G will be realized, and soon. Indeed, Verizon wireless has already rolled out a trial 5G service in several US cities, including

Sacramento, Los Angeles, Houston, and Indianapolis. This trial 5G, unlike 4G, is a fixed point-to-point wireless service which beams internet directly into homes with speeds in the order of hundreds of Megabits per second, possibly replacing older wired infrastructure which costs more to build and maintain over time than a wireless solution. Whether 5G will succeed in offering the same speed to truly mobile users who may be riding in cars or trains is yet to be seen, however as 5G deployment continues technical challenges that surround it, and their solutions will continue to be a main focus of the engineers and researchers in the field of RF communications for years to come.

1.2 Motivation

Aside from the obvious system challenges associated with building microwave and mm-wave communication arrays, the circuit blocks of which they are comprised (low-noise amplifiers (LNA), power amplifiers (PA), phase shifters, mixers, frequency synthesizers, etc.) also face challenges as they are scaled to higher frequencies. For starters, the active devices (field-effect transistors (FET) and heterojunction bipolar transistors (HBT) in silicon technologies) suffer from limited available gain at high frequencies due to their inevitable parasitic capacitances which shunt current and power to undesired nodes. f_{max}, a commonly used metric of transistor performance which can be interpreted as the maximum frequency at which a transistor can produce power gain, is typically cited as around 380 GHz for the NFET device in Global-Foundries' 45 nm CMOS silicon-on-insulator (SOI) technology 'GF45SOI'. However, once the device is wired into the circuit the f_{max} will typically drop to between 200 - 250 GHz due to the considerable loss that occurs in the technology backend's lower metal layers which are on the order of only 0.1 μm in thickness. Systems designed to work at 28, 39, or 60 GHz and using GF45SOI are therefore working at a considerable fraction of their f_{max} and will be limited in total achievable gain per device.

While scaling devices in size may further enhance f_{max}, affording designers more gain at high frequency, it has a detrimental effect on power. As the device scales, the maximum voltage it can reliably handle between terminals also drops, exacerbating the issue of delivering power to the antenna. This means that while lower node length technologies make most other aspects of channel design easier, the design of high power amplifiers gets harder. Another critical component that suffers due to technology scaling is

the voltage-controlled oscillator (VCO) which is a critical block inside the frequency synthesizer and is necessary for frequency translation in the mixer. VCO noise performance is related to the power of the signal in the VCO core, and when signal swing is limited by low device breakdown voltages, this noise performance tends to suffer. Since noise from the local oscillator (LO) in a communication system adds directly to the error-vector magnitude (EVM) of the signal, a low-performance VCO can limit an entire system.

One solution to the issues faced by silicon is to move to III-V technologies such as Gallium-Arsenide (GaAs), Gallium-Nitride (GaN), or Indium-Phosphide (InP) where the tradeoff between device breakdown and operating frequency is less dramatic. Though tempting for their considerable power output over frequency, these technologies are disadvantaged by their fabrication costs, yield, and their compatibility with high speed digital CMOS circuitry. Somewhere between pure silicon and the III-V technologies lies Silicon-Germanium (SiGe) which allows the use of highly scaled CMOS for digital circuitry on the same wafer as high performance HBT devices which offer higher f_{max} and breakdown voltages than similarly scaled FETs. This thesis will focus on the use of SiGe technology to create high performance PAs and VCOs which seek to provide power and noise performance near the limits of their technology and which satisfy the needs of potential 5G systems. Focus on practical areas beyond IC design, such as the effects of the interface between chip and board on amplifier stability will be discussed in detail as well.

Finally, this dissertation will be written with the assumption that the reader is already familiar with basic concepts of radio-frequency (RF) integrated circuit (IC) design such as the basic operation of MOSFET and HBT devices, simple amplifier and phase-locked loop (PLL) designs, quality factor, and the concept of microwave network analysis. If the reader is not familiar with these concepts they are encouraged to review them before reading further.

1.3 Technology

The projects presented in this thesis all revolve around high performance SiGe ICs designed using Global-Foundries' 0.12 μm SiGe BiCMOS technology. In order to avoid unnecessary exposition time in

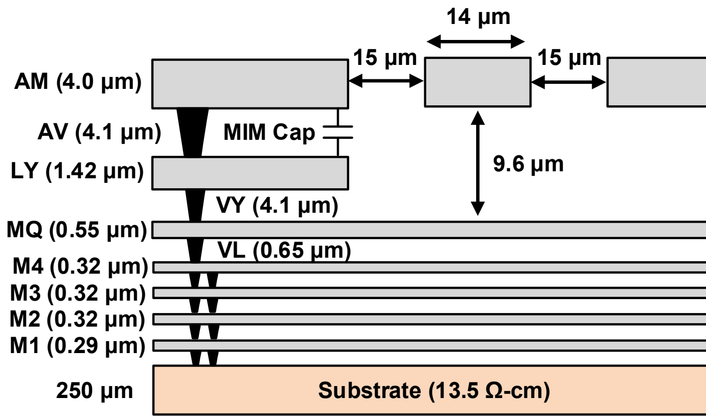


Figure 1.1: Global Foundries 8HP 0.12 μm SiGe BiCMOS process stackup.

future chapters the features of this technology will be outlined for the reader in this section.

GF8HPs seven metal layer stackup is shown in Fig. 4.7 and consists of 3 thick top metal layers (AM, LY, and MQ) which are useful for passive design and RF routing as well as 4 thin bottom metal layers used mostly for digital routing and biasing. Although GF8HP offers several different stackups, including 5 and 6 metal layer options, all works in this dissertation utilize the 7 metal layer option. Among the seven metals, all but AM are copper (AM is aluminum) resulting in lower routing loss/higher Q-factor passives due to copper's high electrical conductivity. The technology also offers high-density metal-insulator-metal (MIM) and dual-MIM capacitors between the AM and LY metals with capacitance densities of 0.79 and 1.82 fF/μm^2 respectively. Despite their high capacitance density, the Q-factor of the MIM and dual-MIM predicted by the process design kit (PDK) is quite low at high frequencies as a result of the single lossy via that connects the MIM top plate to AM. As a result, the works in this dissertation will favor custom designed metal-oxide-metal (MOM) capacitors over the PDK options.

In addition to the PDK capacitor options, GF8HP offers a deep-trench isolation (DTI) layer. Theoretically, at the boundary of a DTI layer substrate currents must be zero, therefore DTI is commonly placed underneath critical RF capacitors and inductors to mitigate losses due to unwanted currents induced in the substrate. DTI also allows for the creation of triple-well switches which can allow additional isolation over their non-triple-well counterparts.

Table 4.1 lists the active devices which are available in GF8HP alongside their f_{max} and recommended maximum supply voltages. The high f_t npn device is the highest frequency device offered and

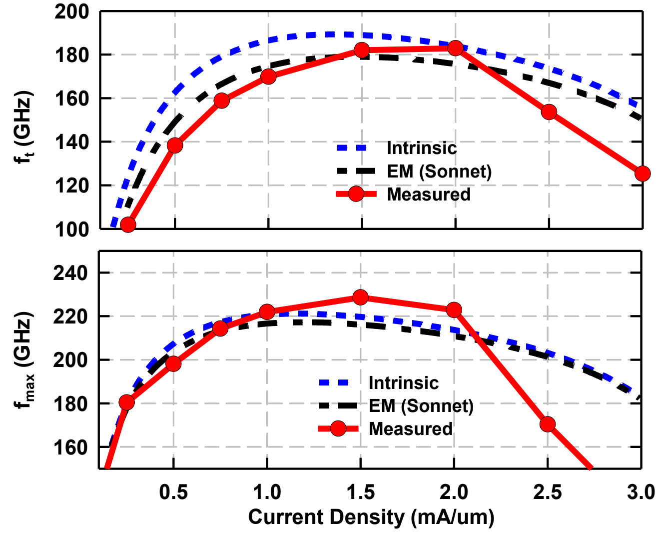


Figure 1.2: Simulated and measured f_t and f_{max} versus current density for 10 μm npn (single-ended layout).

Table 1.1: List of Devices Available in GF8HP

Device	f_{max} (GHz)	Vdd (V)
High f_t npn	220	1.8 (BVCEO)
High breakdown npn	60	3.5 (BVCEO)
NFET (thin oxide)	130	1.2
NFET (thick oxide)	95	2.5
PFET (thin oxide)	50	1.5
PFET (thick oxide)	30	2.5

has an f_{max} of 220 GHz, which unlike devices in highly scaled CMOS technologies, does not degrade significantly after the interconnects between top and bottom metal layers are added. Fig. 1.2 shows simulated and measured f_t and f_{max} versus current density for an npn device with 10 μm emitter length and 0.12 μm emitter width revealing an optimum current density of 1 - 2 mA/μm. Noteworthy is the steep drop in f_t and f_{max} at current densities beyond 2 mA/μm. This is likely due to the electro-migration limits of the metal interconnects between transistor and top metal which are not modeled in electromagnetic (EM) simulations of the interconnects.

Also to note are the NFET and PFET devices which come in thin oxide (0.12 μm minimum gate length) and thick oxide (0.24 μm minimum gate length) variants and have standard and triple-well options as well. Despite their low f_{max}, NFETs and PFETs are useful in the design of switches, when complementary structures are required, or in the implementation of digital logic, and find extensive use in

the design of the VCO and PLL in Chapter 4.

1.4 Thesis Overview

This thesis is comprised of 4 chapters which detail three separate projects. The projects focus on critical circuit blocks for potential 5G communication systems at 28, 39, and above 60 GHz including the design and measurement of high power amplifiers operating in the E-band and very low noise VCO design in the Ku-band.

Chapter 2 presents a set of wideband, fully-integrated E-band power amplifiers (PA) designed in GF8HP and working in the range of 60 - 75 GHz. The single-PA is based on common-emitter driver stages followed by a common-emitter output stage. A 3-stage and 4-stage version of the single-PA as well as 4 and 8-way combined variants of the 4-stage PA are measured and compared. The single, 4-way, and 8-way combined PAs achieve saturated output powers of 16, 19.5, and 24 dBm with peak power-added efficiencies (PAE) of 18, 11, and 12% respectively. Modulated waveforms are passed through each amplifier and data rates as high as 32 Gbps are demonstrated for all amplifiers when driven in the linear mode. Measurements of how error-vector magnitude (EVM) & PAE degrade versus output power are presented and it is demonstrated that the 8-way combined PA can deliver 17 - 20 dBm of average power in a 64-QAM, 1 Gbaud waveform (6 Gbps), with an EVM of -32 to -24 dB and a PAE of 3-5% without predistortion. To the author's knowledge the work presented in chapter 2 (which was also published in the *IEEE Transactions on Microwave Theory and Techniques* Journal in 2019 [1]) is the first paper reporting detailed measurements of PA EVM and PAE versus output power at frequencies exceeding 60 GHz.

Chapter 3 presents a theoretical analysis of how the stability and performance of packaged mm-wave amplifiers is negatively effected by the parasitic inductances of the electrical interfaces between the board and silicon chip such as bondwires, bondribbons, and bumps. The chapter details the causes of the stability issues and proposes several mitigation techniques and best practices. The variants of packaged E-band power amplifiers that were designed in chapter 2 are assembled onto low-cost PCBs using wirebond and flip-chip technology as a means of demonstrating proper assembly/packaging techniques of silicon amplifiers. The packaged amplifiers achieve saturated output power ranging from 15.0 to 20.3 dBm. the

author's knowledge, these amplifiers represent only the second published demonstration of *packaged* silicon power amplifiers using flip-chip and wirebond methods. The higher power PA variants achieve the highest reported saturated output power of any packaged E-band silicon amplifier to date. The work presented in this chapter was submitted for review to the *IEEE Transactions on Microwave Theory and Techniques* Journal in 2019 [2].

Chapter 4 presents a 9.9 - 12.45 GHz VCO designed in GF8HP with focus on achieving the lowest possible phase noise using only a single core and maintaining the recommended vdd of the technology. The oscillator consists of a cross-coupled design utilizing a transformer-coupled resonant tank which takes advantage of both harmonic tuning and the Q-enhancing properties of the transformer-coupled topology. An analysis is offered which justifies the use of the transformer, noting its importance in mitigating the practical limits imposed during layout on equivalent LC-tanks. An excellent phase noise of -122 dBc/Hz is measured at 1 MHz offset from the carrier resulting in a FoM and FoMT of -183 and -190, respectively. The VCO is incorporated into a type-II charge-pump based PLL with intent to be used as the LO generation in a potential 5G communication system. The work presented in this chapter was also submitted for review to the *IEEE Transactions on Microwave Theory and Techniques* Journal in 2019 [3].

Chapter 2

Design and Measurement of Single and Power-Combined Linear E-Band Power Amplifiers

2.1 Introduction

In recent years, silicon-based millimeter-wave (mm-wave) wireless systems in the E-band have become of increasing interest due to their applications in automotive radar [4–6], image sensing [7, 8], and short range high data rate wireless communication [9–13]. In order to enable the proliferation of these systems, it is desirable they be realized using low cost and high-yield technologies such as advanced CMOS or silicon-germanium (SiGe). Despite the push for integration, silicon technologies are limited in their ability to efficiently generate large output powers at mm-wave frequencies due to the natural tradeoff between breakdown voltage and transistor size and are often outperformed by III-V technologies such as GaAs [14–17], GaN [18–23], and InP [24].

To date, no single silicon-based power amplifier (PA) working above 60 GHz has been reported that can output higher than 27.3 dBm [25], and most authors report output powers between 17 and 24 dBm. Since the output power from a single silicon device is typically limited to $<$17 dBm, the use of power

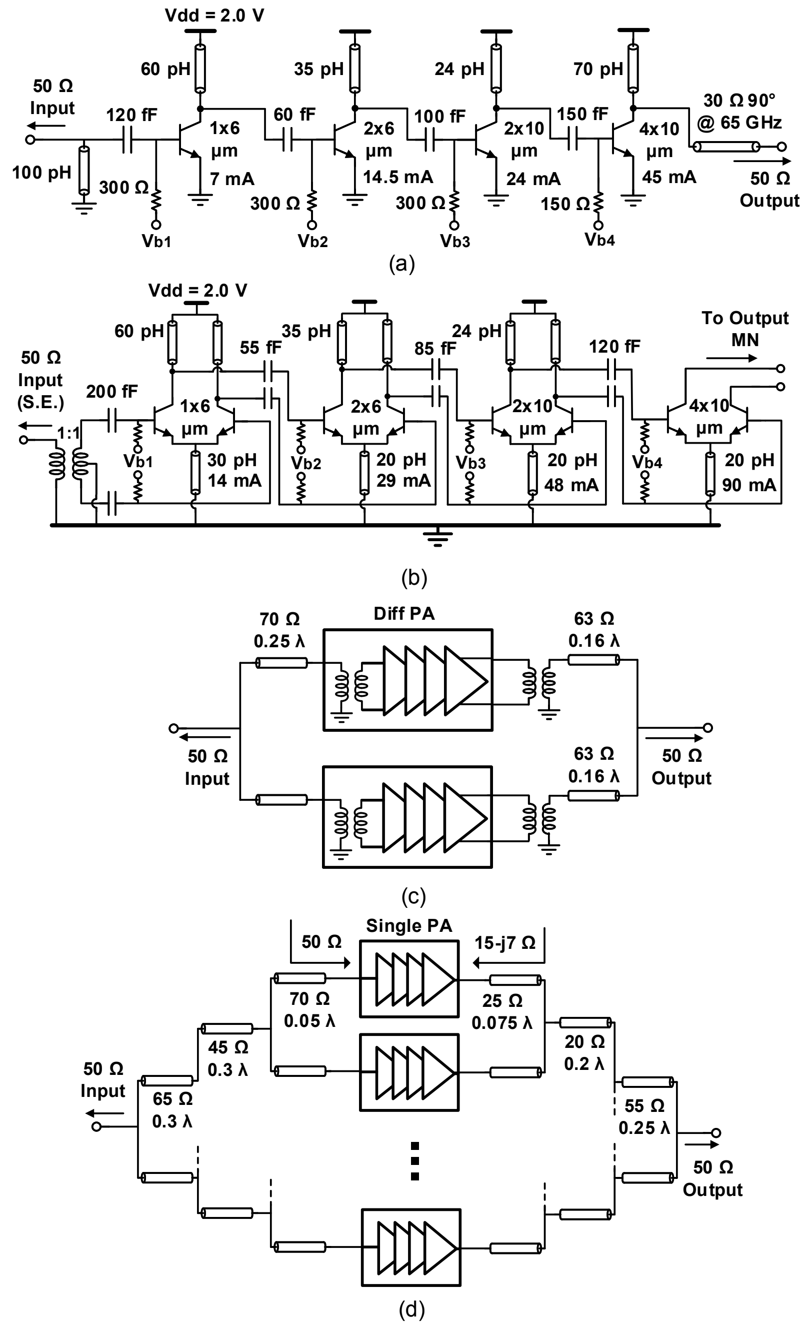


Figure 2.1: Circuit schematics of (a) single-ended 4-stage PA unit cell, (b) differential 4-stage PA unit cell, (c) 4-way combined PA, and (d) 8-way combined PA using 4-stage PA unit cells shown in (a).

combining methods including reactive [25–29], transformer-based [30–38], spacial [39–41], and device stacking [42–45] to produce higher output powers is common. Peak power-added efficiencies (PAE) are typically in the range of 10 - 20% due to the need to bias in class-A or class-AB regimes to achieve

reasonable gain.

This chapter expands on work originally presented in [46], by presenting, in addition to the 4-stage single-PA and 8-way combined PA (Fig. 3.12(a) and (d)) of the original work, a new 3-stage single-PA and a 4-way combined PA using transformer-combining techniques (Fig. 3.12(c)) also designed in 0.12 μm SiGe BiCMOS and working from 60 - 75 GHz. Modulation measurements with data rates up to 32 Gb/s are demonstrated for the PAs operating in the linear mode. The methodology of taking measurements involving modulated waveforms is expanded. The error-vector magnitude (EVM) response of each PA to 16 and 64-QAM modulation schemes versus output power are presented for various baud rates. Results show that the power amplifiers can pass 1-GBaud 64-QAM signals at 0 dB backoff with around -23 dB EVM and with a PAE as high as 8.5% for the single-PAs, 3.5% for the 4-way combined PA, and 6% for the 8-way combined PA. It is demonstrated that the 8-way combined PA can transmit a 7.7 dB peak-to-average power ratio (PAPR) 64-QAM signal with 50 - 100 mW average output power at -32 to -24 dB EVM and without significant non-linear compression. To the author's knowledge, this is the first work reporting detailed measurements of PA EVM and PAE versus output power at these frequencies.

2.2 Transistor Layout

The single-ended power amplifiers employ the device layout shown in Fig. 2.2(a) where the base and collector are extended length-wise through the M2 and M3/M4 layers respectively before connecting to via stacks leading to the top metal. The emitter finger, which carries the most current and is located in-between the base fingers, is connected directly to the MQ level using a large row of vias before fanning out to attach to the chip-wide MQ ground plane. In the single and 8-way combined PAs, four 10 μm transistors are layed out as individual cells and their base/collector nodes are attached on the top metal to create an output device with effective length of 40 μm without significantly impacting the transistor f_t and f_{max}.

In the differential PA unit cells, transistor interconnects are layed out differently so that the parasitic inductance from their emitters does not add in series as current travels to the virtual ground at the point of symmetry. The differential npn devices are lined up parallel to the point of symmetry as depicted in

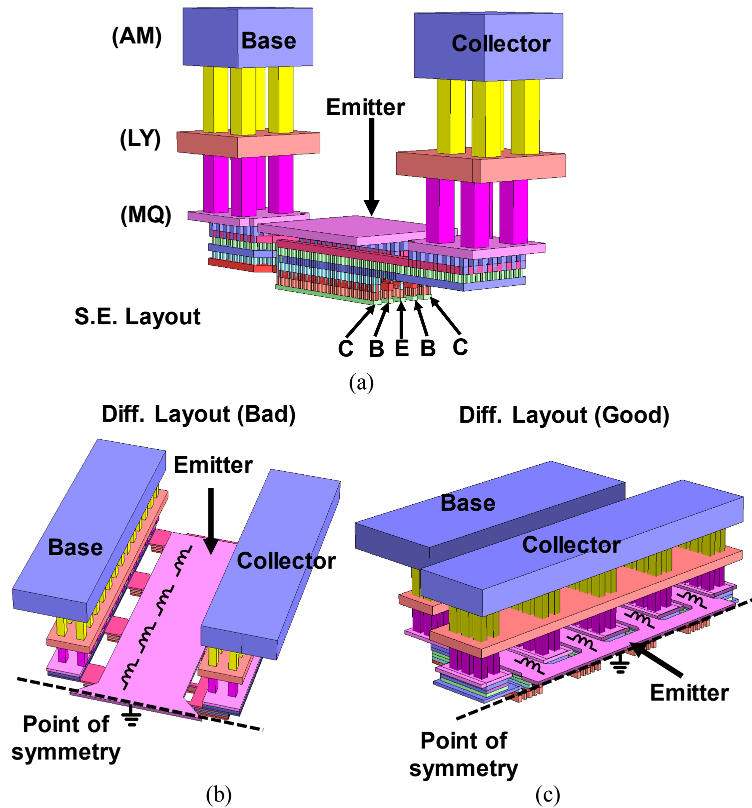


Figure 2.2: Sonnet EM models of (a) single 10-μm npn transistor with single-ended layout, (b) and (c) 4 x 10-μm transistor with proper and inproper differential layouts for mitigating emitter parasitic inductance. Note that only one side of the differential layouts are shown.

Fig. 2.2(c). Emitter fingers are widened on the MQ level to ensure that the device passes electro-migration rules as current flows length-wise down the emitter. The two collector fingers independently via upwards on the left and right sides of each device, not connecting together until they reach the top metals. Using this layout configuration, the unwanted parasitic emitter degeneration inductance is minimized and the differential transistors achieve an f_t and f_{max} which is nearly identical to that of the single-ended layout.

2.3 Design

2.3.1 Single Power Amplifier

The single power amplifier (Fig. 3.12(a)) uses a common-emitter (C.E.) topology with the output stage consisting of four 10 μm npn devices connected in parallel and biased at 1.1 mA/μm for peak f_t and

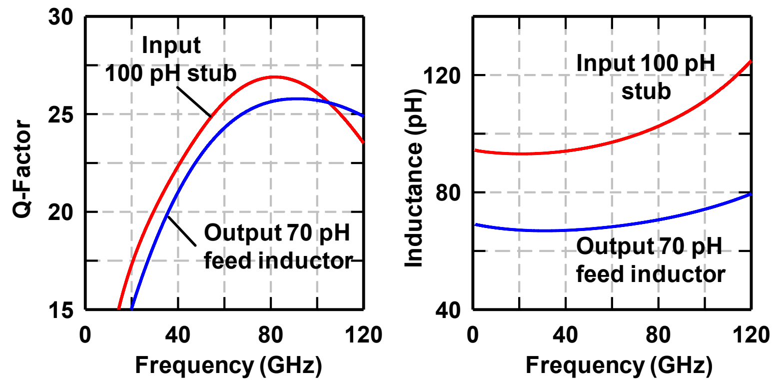


Figure 2.3: Simulated Q-factor and effective inductance of the 100 pH input matching microstrip stub and 70 pH output feed stub using Sonnet EM simulation tool.

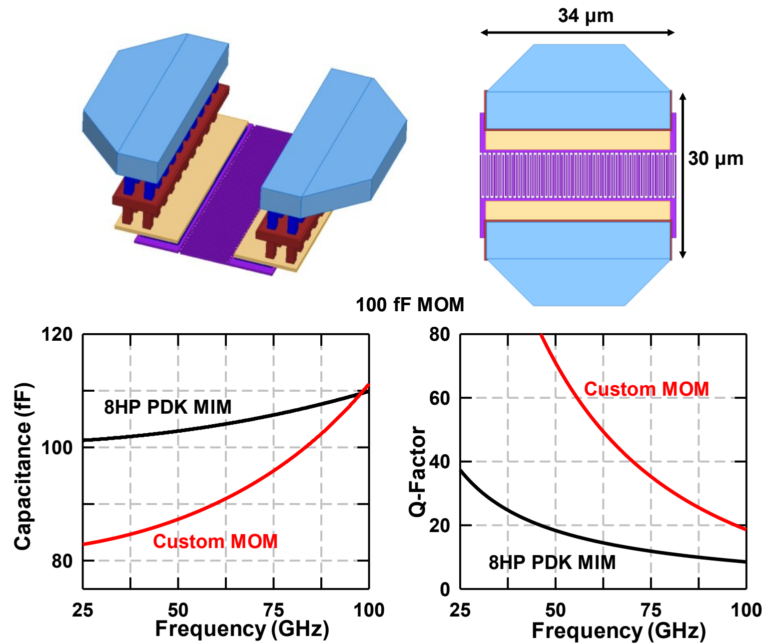


Figure 2.4: HFSS model of 100 custom interdigited MOM cap and simulated capacitance & Q-factor versus frequency of custom MOM cap and IBM PDK MIM cap.

f_{max}. Driver stages are each designed using a single feed inductor and series capacitor to provide conjugate interstage matching for maximum small signal gain and are sized to ensure that compression is limited by the output stage without sacrificing efficiency.

The passive components in the single PA are all custom designed using Sonnet, HFSS, and EMX electromagnetic simulation tools. Feed inductors are realized as high impedance (Zo = 50 - 77 Ω) microstrip transmission-line stubs using the top AM metal as signal and the MQ metal as ground. Care is

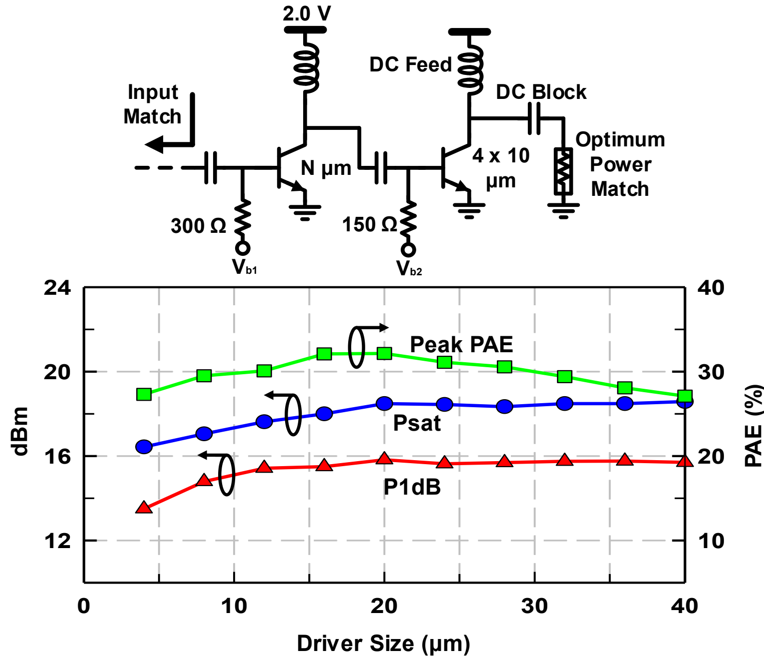


Figure 2.5: P1dB, Psat, and PAE vs. choice of driver stage for a two stage C.E. amplifier using a 4 x 10 μm output stage at 70 GHz. For each driver sizing choice the matching between the driver and output stage is retuned to provide optimum results.

taken in the design of the microstrip line widths, with wider lines being used for the later stages to meet electro-migration rules and thinner lines being used for earlier stages to reduce their length and therefore overall chip area. Fig. 2.3 shows simulated Q-factor and inductance for the input (w = 5 μm, Zo = 77 Ω) and output (w = 13 μm, Zo = 50 Ω) inductors. Both inductors achieve a Q-factor $>$ 25 at 70 GHz

GF8HP offers high density metal-insulator-metal (MIM) and dual-MIM capacitors with capacitance densities of 0.79 and 1.82 fF/μm^2 respectively. However due to high via resistance, the MIM capacitor Q-factor drops quickly at mm-wave frequencies, making them unsuitable as matching devices. Capacitors are realized instead using interdigited metal-oxide-metal (MOM) structures (Fig. 2.4) designed on the M4 metal layer. Deep-trench hashing is used underneath the MOM capacitor to prevent loss through the substrate. The interdigited capacitors are simulated using HFSS and EMX softwares which can accurately capture 3-D sidewall capacitances which are not well modeled by 2.5-D simulation tools. The custom MOM capacitors can achieve simulated Q-factors around 40 at 70 GHz but have a capacitance density which is roughly half that of the PDK MIMs.

The choice of driver size is a tradeoff between output power and efficiency. Fig. 2.5 shows the

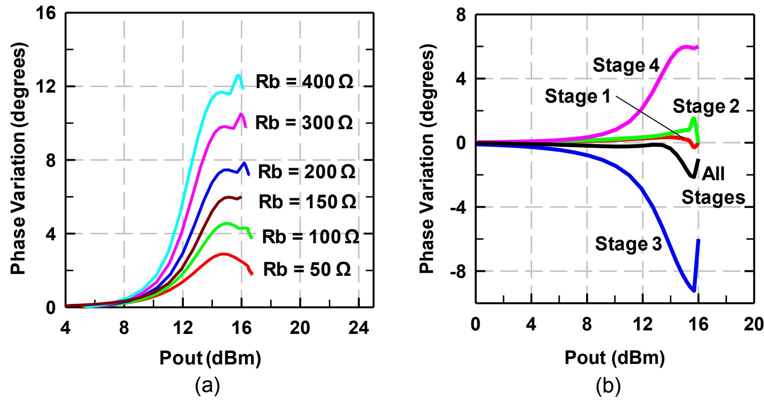


Figure 2.6: Simulated phase variation vs output power for (a) output stage for various values of Rb and (b) all stages in PA with nominal 150 Ω output stage bias resistor value.

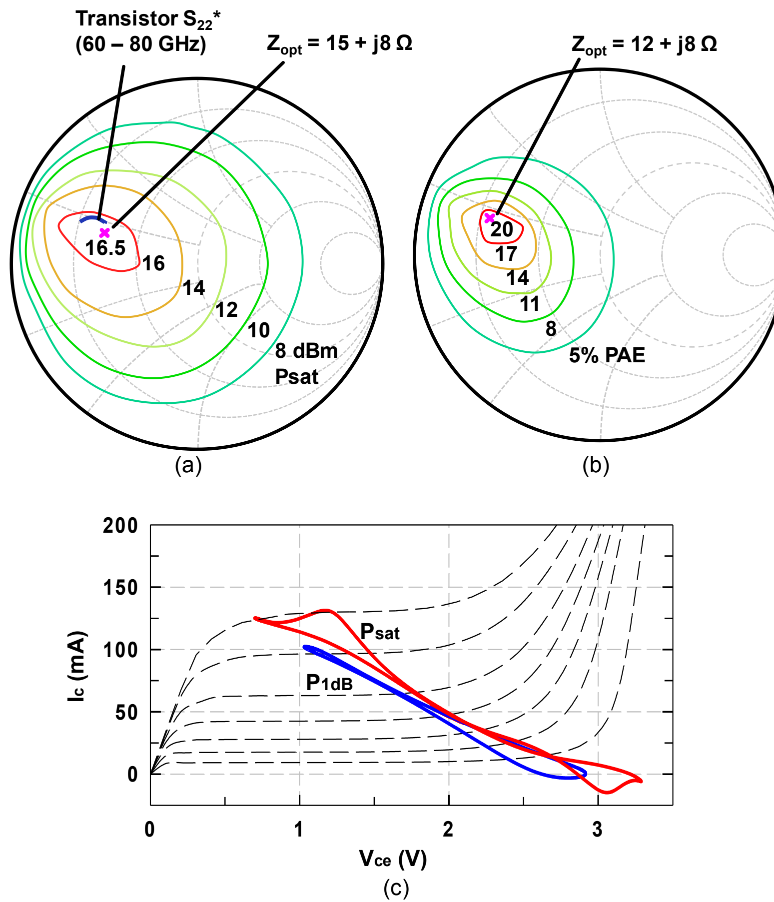


Figure 2.7: (a) Simulated output power loadpull contour, (b) simulated power added efficiency loadpull contours and (c) simulated loadline as seen at the output device transconductor (load capacitance tuned out) for the 4-stage single-PA.

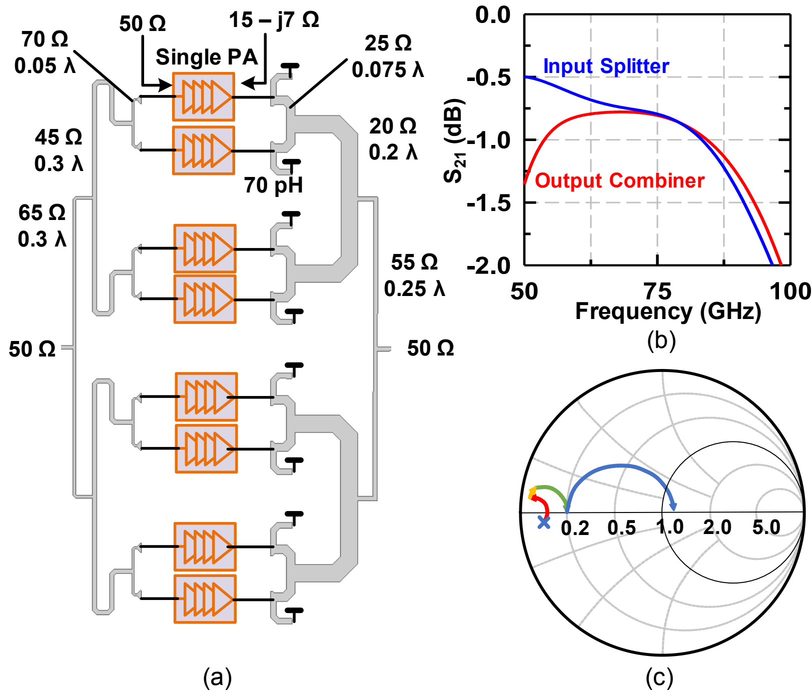


Figure 2.8: (a) Diagram of 8-way input splitter and output combiner with labeled transmission-line electrical lengths and impedances, (b) splitter and combiner S_{21} versus frequency, (c) smith chart visualization of matching between PA output impedance and 50 Ω load at 70 GHz.

simulated P1dB, Psat, and PAE of a two stage C.E. amplifier using the 4 x 10 μm output device versus driver size. In the testbench of Fig. 2.5 input and output matching is ideal and tuned to be optimum for each size of driver. Interstage matching is designed to be a conjugate match for maximum small signal gain and is modified to produce the best match for each driver size. Both driver and output device are biased at 1.1 mA/μm for peak f_t and f_{max}. Psat and P1dB both saturate when the driver is one half the size of the output device. Peak PAE is also maximum at this point because output power is maximized without wasting extra current in the driver device. The result of optimum driver to output stage sizing being 1:2 is not general and is typically determined by the driver gain, with drivers that have higher gain having smaller optimum sizes due to their superior ability to saturate the output stage.

Each stage of the single-PA is biased using a simple current mirror with beta helper and mirroring ratio of 8:1. The resistor used to isolate the base of the RF transistor from the bias network is chosen to be 150 Ω for the output stage so that the supply can be increased above the technology's 1.8 V BV_{ceo} to 2.0 V. Choosing a low bias resistor value is also important to prevent the IR drop through the bias resistor

from dropping the V_{be} of the output device when it self-biases at high output powers [25]. As shown in Fig. 2.6(a) the value of the bias resistor can also have a significant effect on the AM-PM distortion of a C.E. transistor. The bias resistor value can therefore be used as a tuning parameter to cancel the AM-PM distortion from the driver stages. Fig. 2.6(b) presents the total AM-PM distortion for the 4-stage S.E. PA as well as the individual contributions to the overall AM-PM from each stage. In common-emitter stages, the phase between the input and output typically flips polarity, therefore each subsequent stage contributes opposite polarity AM-PM distortion to the overall chain. Because of this feature, the AM-PM of the 3rd stage may be tuned to cancel the AM-PM of the final stage, resulting in an overall AM-PM distortion of less than 2° before output power saturates.

The optimum output impedance is determined by performing load-pull simulations (Fig. 2.7(a)) and the optimum power match is 15 + j8 Ω (nearly a conjugate match) at 70 GHz. The output matching network uses a 70 pH microstrip feed inductor (w = 13 μm, Q = 25) and a 30 Ω quarter-wave line (w = 40 μm, Q = 26) to match the output to 50 Ω.

Both three and four stage versions of the single-PA were fabricated. The 3-stage PA has identical component values to the four stage PA, but is missing the input stage. Results for both 3 and 4-stage single-PAs are similar with the 3-stage PA predictably having lower gain and slightly higher efficiency.

2.3.2 8-Way Combined Power Amplifier

The 8-way combined PA is designed using microstrip transmission-line segments to reactively match and power combine the 8 different 4-stage single-PA unit-cells. The layout details of the input splitter and output combiner are given in Fig. 2.8 (a). In order to minimize the output network loss, the 8-way combiner is designed to have the minimum possible length while providing a satisfactory output match to each unit PA. For this reason, the distance between each PA cell is made to be as small as possible while avoiding unwanted coupling between the unit-cell feed inductors. Once the distance is set, the minimum lengths of the output combiner segments can be obtained and the impedances of each transmission line chosen so as to match the unit-cells to 50 Ω. The input and output networks achieve roughly ∼0.75 dB of loss at 70 GHz. To avoid extra loss, a series capacitor is not used in the output network. because loss of the input network is less critical than loss of the output network, the input splitter lines are meandered and

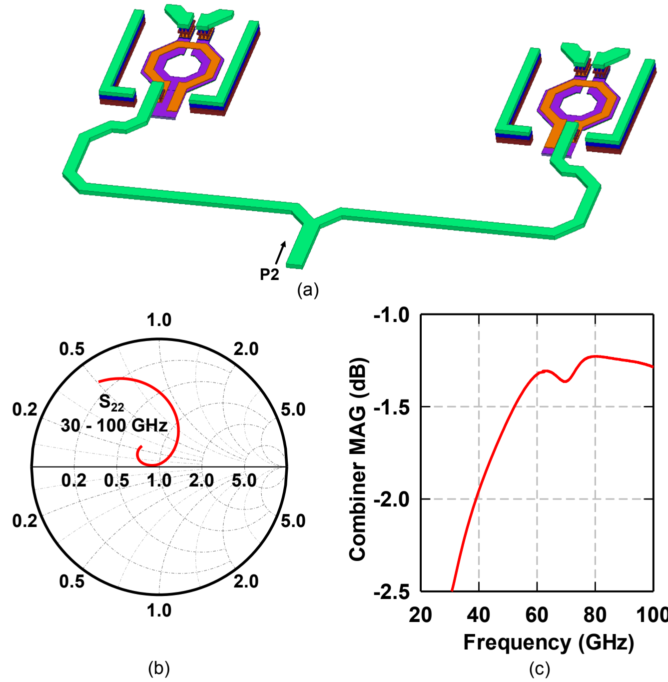


Figure 2.9: 4-way combined PA: (a) output combiner HFSS model, (b) combiner simulated S_{22}, (c) combiner simulated maximum available gain.

their lengths are used as an extra tuning parameter to achieve the widest bandwidth input match.

2.3.3 Differential Power Amplifier

The differential PA unit-cell uses a truly differential rather than a pseudo-differential topology, the difference being that the positive and negative RF signals are referenced to each other rather than to the ground plane, and a virtual ground exists at the plane of symmetry between the two differential signals. This can be exploited by adding inductive degeneration which rejects common-mode (CM) signals. The existence of this plane of symmetry in the layout, and the fact that the RF signal is not referenced to the on-chip dc ground can also have important implications for RF performance after packaging when the interfaces between chips and printed circuit boards (PCB) such as bumps, bondwires, and bondribbons typically create parasitic inductances which can separate the on-chip ground from PCB ground by several ohms, creating the potential for significant detuning of on-chip passives. Truly differential amplifiers, unlike their single-ended and pseudo-differential counterparts, are resistant to this type of detuning making them more suitable for packaging at these frequencies.

The differential PA is designed to use the same nominal component values as the single-ended 4-stage PA, but the transistor and inductor layouts are modified (see Section II) to increase symmetry and to reduce the area. A transformer balun is used at the input to transform the single-ended input into a differential signal. The transformer is designed using the thin M4 metal for the primary winding and thicker MQ metal for the secondary winding. This choice of metals is driven by the vertical proximity of the two metal layers which increases magnetic coupling in the transformer. The differential PA inductors are layed out to loop towards the center so that they shunt to the virtual ground at the point of symmetry thus upholding the true differential operation. This incurs a penalty in Q-factor (Q drops from 25 to $\sim$18) as well as introducing extra parasitic capacitance from the routing line that must cross under the inductor in order to connect to the next stage. In simulation the gain of the differential PA is dropped by 3 dB and the PAE by 2.5% compared to the S.E. PA due to the extra losses present in the differential matching networks and input balun.

To reduce to CM gain and to avoid CM oscillations, CM degeneration inductors are placed at the virtual ground between the transistor pairs. Ideally degeneration inductances should be large in order to reduce CM gain, but in practice are limited by electromigration rules which require degeneration inductors be made wide, and by the space between PA stages which should be kept small to prevent wasted chip area and unnecessary transmission-line loss between stages. The degeneration inductors were realized as microstrip transmission-lines with inductance values limited to between 20 and 30 pH by the spacing requirements described above. The rejection offered by these inductances at 70 GHz is enough to drop the common-mode gain of each stage to 0 dB.

2.3.4 4-Way Combined Power Amplifier

The 4-way combined PA is designed from two differential PA unit cells. The PA splits a single-ended 50 Ω input using meandered 70 Ω quarter-wave transformers so that each unit PA sees a 50 Ω impedance at its input. At the output, power is combined by first converting differential outputs to single-ended through a transformer-balun ($\sim$1.0 dB loss), then using 0.16 λ, 63 Ω microstrip transmission lines to reactively combine the common mode. The output transformer-balun is designed using M3 + M4 metals as the primary winding and MQ metal as the secondary and V_{dd} is distributed to the output stage through

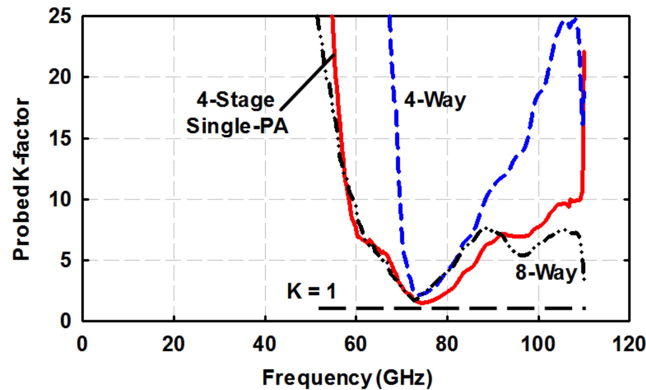


Figure 2.10: Measured (probed on chip) k-factor of the 4-stage S.E., 4-way, and 8-way combined PAs.

the center tap of the primary. As in the case of the input transformer, lower metals were used due to their close vertical proximity which increases the magnetic coupling between the windings.

The 3-D HFSS model of the output combiner is shown in Fig. 2.9(a). This topology has the added advantage of being truly symmetric, unlike alternative designs [33] which attempt to combine multiple differential signals by compensating asymmetric, multi-filament transformers so that they achieve balanced operation over a small bandwidth. The S_{22} seen from the output of the combiner is shown in Fig. 2.9(b) and the maximum available gain (MAG) of the combiner is shown in Fig. 2.9(c). A power combining loss of 1.25 dB is achieved from 60 to 100 GHz including the balun loss.

2.3.5 Stability

Probed K-factor measurements from dc to 110 GHz of the 4-stage single, 4-way, and 8-way combined PAs are shown in Fig. 2.10. The 3-stage single-PA K-factor is not shown but is nearly identical to that of the 4-stage PA. All power amplifiers demonstrate $K > 1$ over the entire frequency range suggesting that they will be stable when integrated onto a larger IC.

2.3.6 Performance versus Temperature

Fig. 2.11 shows the simulated performance of each power amplifier variant versus temperature at 70 GHz. The results show that as temperature is increased the gain and power-added efficiency of each PA variant drops due to the decrease in effective transistor transconductance in each stage. Although

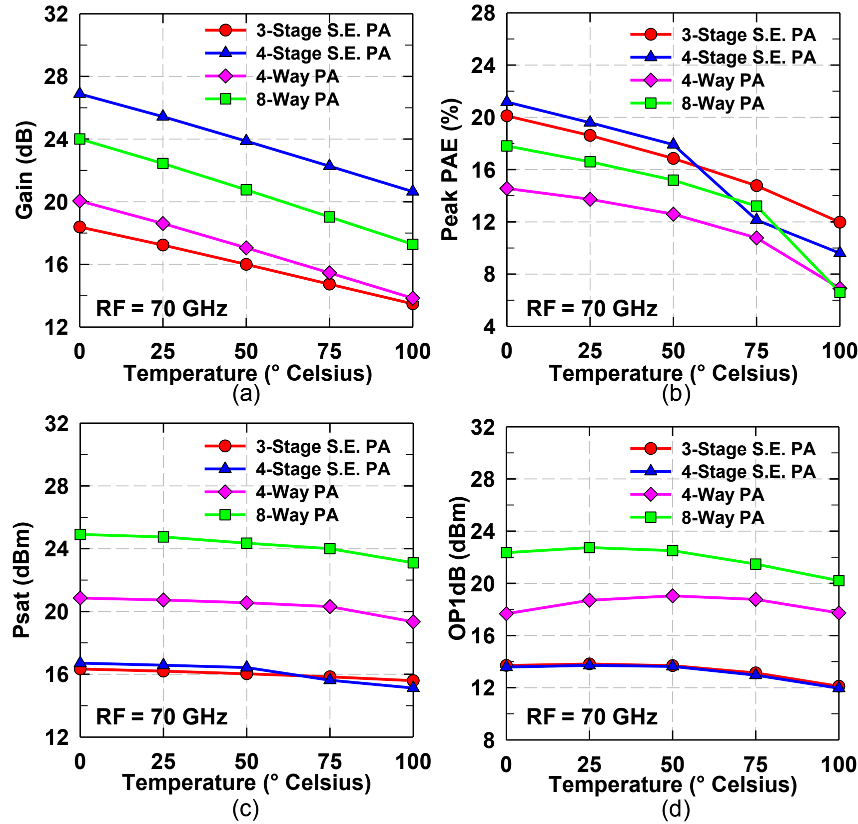


Figure 2.11: Simulated PA performance versus substrate temperature at 70 GHz: (a) gain, (b) power-added efficiency, (c) saturated output power, and (d) output 1-dB compression point.

saturated output power and 1 dB compression point stay relatively constant over temperature the decrease in efficiency suggests that the E-band PA variants should be cooled or operated near room temperature for best performance.

2.4 Measurements

2.4.1 Small Signal Measurements

Chip microphotographs of the 4-stage single-PA, the 4-way combined PA, and the 8-way combined PA are shown in Fig. 3.17. Small-signal measurements of the PAs were taken by probing directly onto the PA chips. For each chip explicit electrostatic-discharge (ESD) protection circuits are included on all DC pads. RF pads do not contain explicit ESD circuits, but are protected from high current ESD events by their shorted matching stubs which are part of the input matching networks. Measurements from

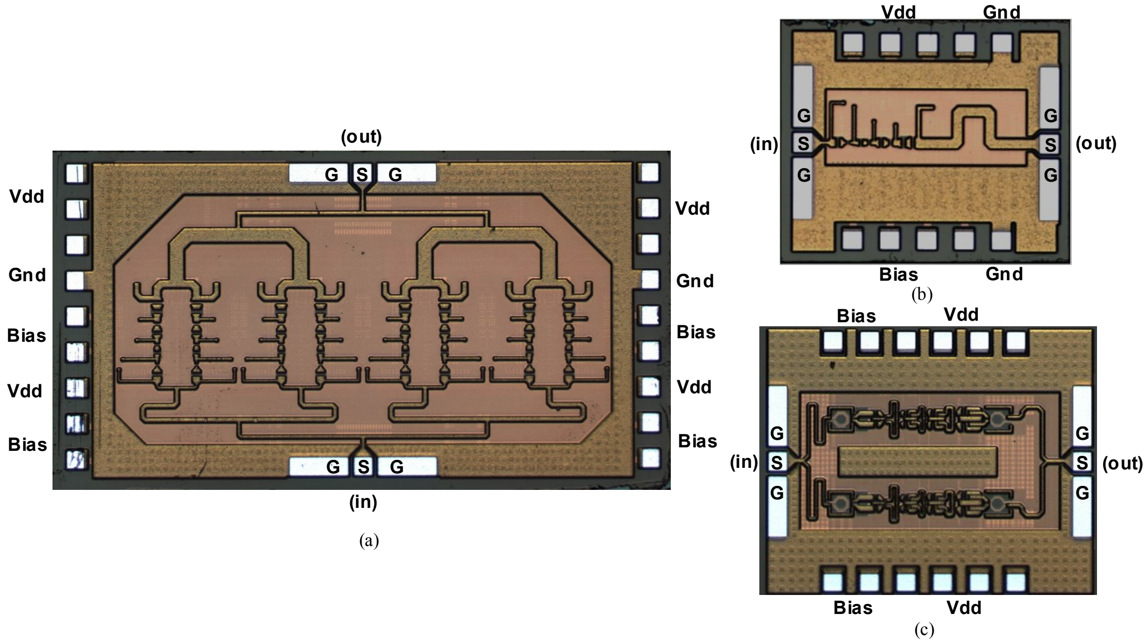


Figure 2.12: Chip microphotograph of (a) 8-way combined PA (2.5 x 1.35 mm including pads), (b) S.E. 4-stage PA breakout (0.9 x 1.1 mm including pads), and (c) 4-way combined PA (1.1 x 1.35 mm including pads).

dc - 70 GHz were taken using a Keysight N5247A (PNA-X). A Keysight 50 GHz VNA outfitted with Keysight mm-wave head controllers and VDI WR-10 waveguide extenders were used for measurements from 73 - 110 GHz. The gap in measured data between 70 - 73 GHz was filled with spline fitted data. Measured S-parameters of all PAs are shown in Fig. 2.13.

The 3-stage single-PA achieves a peak S_{21} of 18.5 dB centered at 67 GHz with a 3-dB bandwidth from 60 - 77 GHz. The 4-stage single-PA has peak S_{21} of 25.5 dB centered at 67 GHz with a 3-dB bandwidth from 60-73 GHz. For both designs there is no appreciable drop in gain between measurement and simulations, suggesting the PDK device models and the passive EM modeling is accurate.

The 4-way combined PA has a peak S_{21} of 18.5 dB at 72.5 GHz and a 3-dB bandwidth of 67 - 80 GHz. The 8-way combined PA achieves peak S_{21} of 22.5 dB centered at 67 GHz with a 3-dB bandwidth from 60 - 74 GHz. Again, in both cases, measurements and simulations fit tightly suggesting the accuracy of both the device models and passive EM modeling.

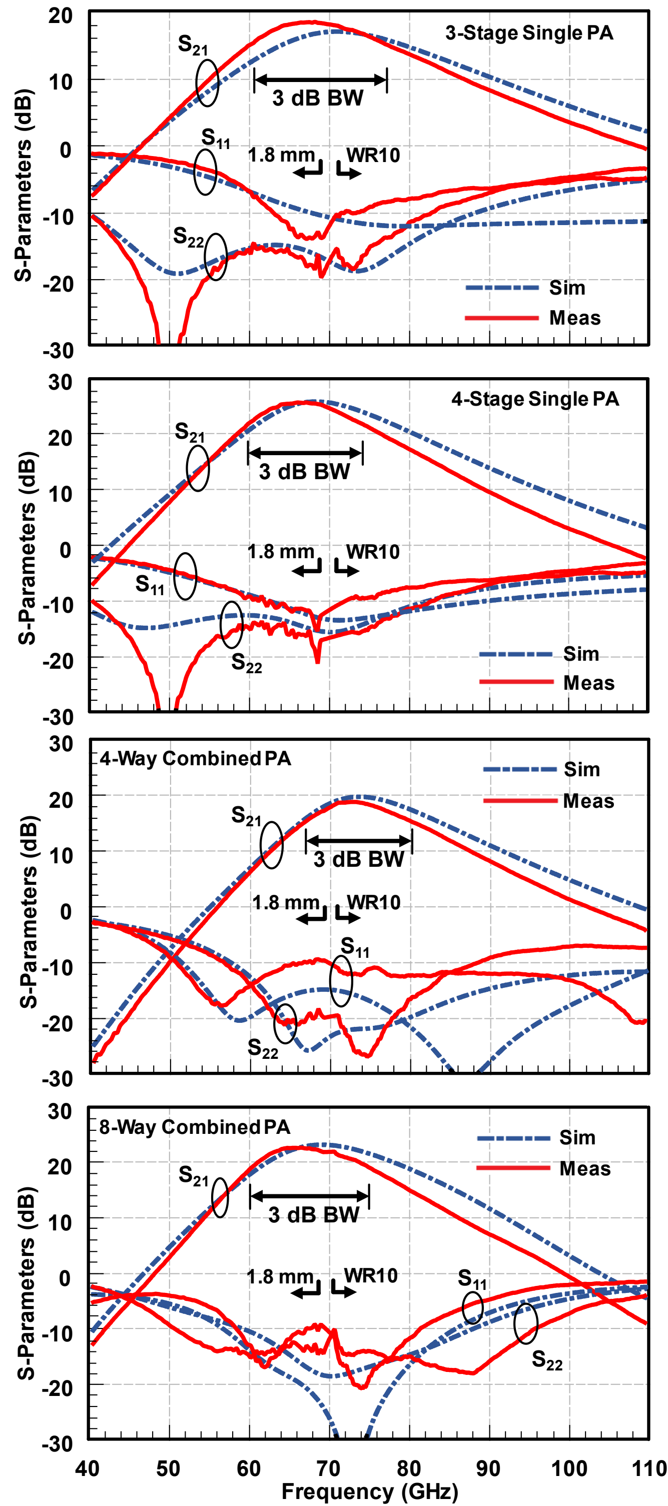


Figure 2.13: Measured and simulated S-parameters of the 3-stage single-PA, 4-stage single PA, 4-way combined PA and 4-stage 8-way combined PA.

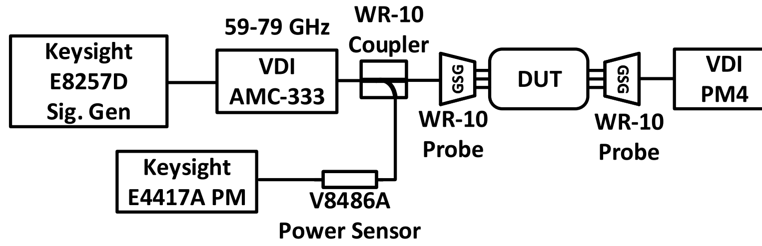


Figure 2.14: Large signal measurement setup.

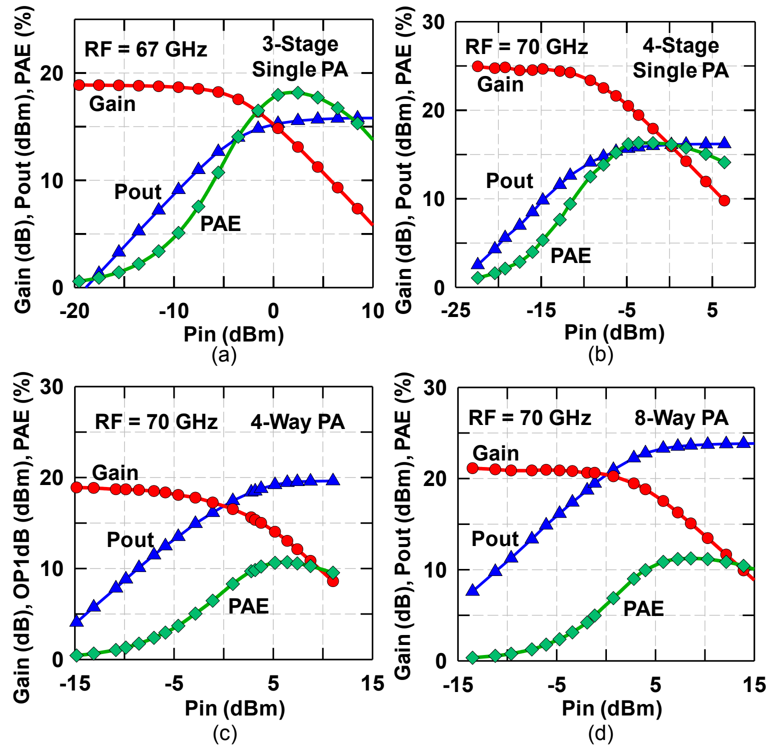


Figure 2.15: Measured gain, output power, and PAE versus input power for (a) 3-stage single-PA, (b) 4-stage single PA, (c) 4-stage 4-way combined PA, and (d) 4-stage 8-way combined PA.

2.4.2 Large-Signal Measurements

The setup for large signal measurements above 70 GHz is shown in Fig. 2.14. A Keysight signal generator is fed to a VDI-AMC 333 frequency multiplier to produce the input signal from 70 - 80 GHz. For below 70 GHz measurements, the input signal is generated directly from the Keysight E8257D signal generator. Probe losses are accounted for by measuring an on-chip thru which is used for calibrating out the losses of both the probes and GSG pads.

Large-signal measurements versus power are shown in Fig. 2.15 and versus frequency in Fig. 2.16.

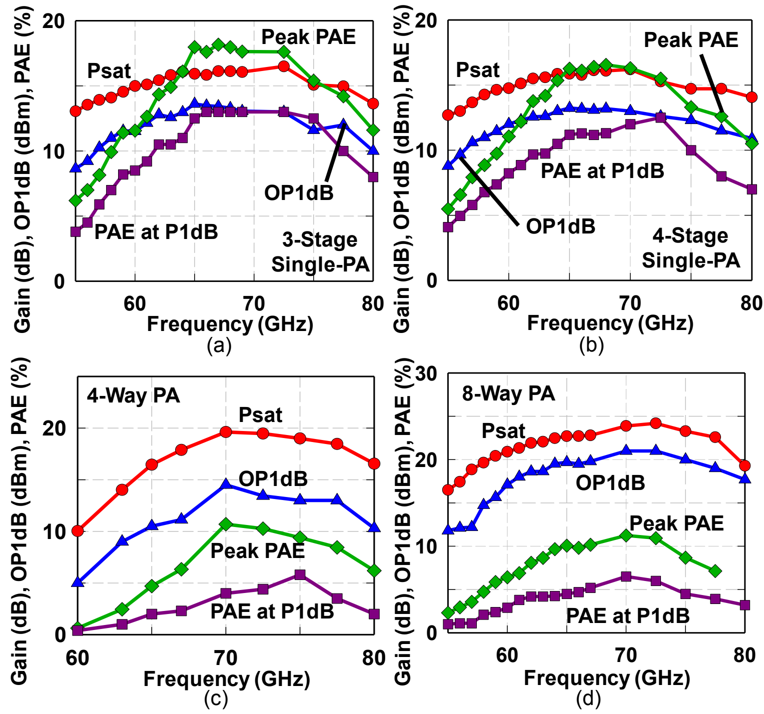


Figure 2.16: Measured Psat, OP1dB, and PAE versus frequency for (a) 3-stage single-PA, (b) 4-stage single PA, (c) 4-stage 4-way combined PA, and (d) 4-stage 8-way combined PA.

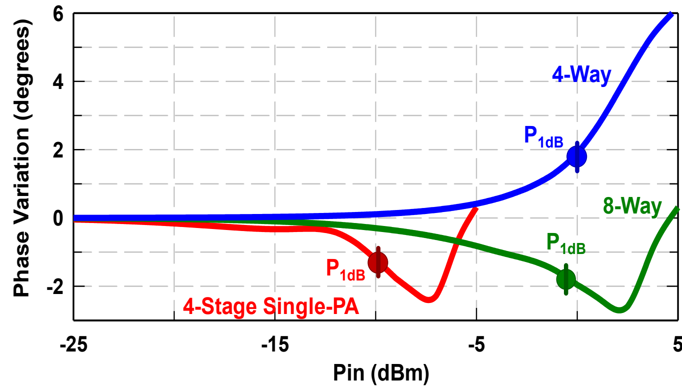


Figure 2.17: Simulated phase variation vs output power for the 4-stage single PA, 4-way combined differential PA, and 8-way combined PA. Results for the 3-stage single PA are omitted due to their similarity to the 4-stage single PA results.

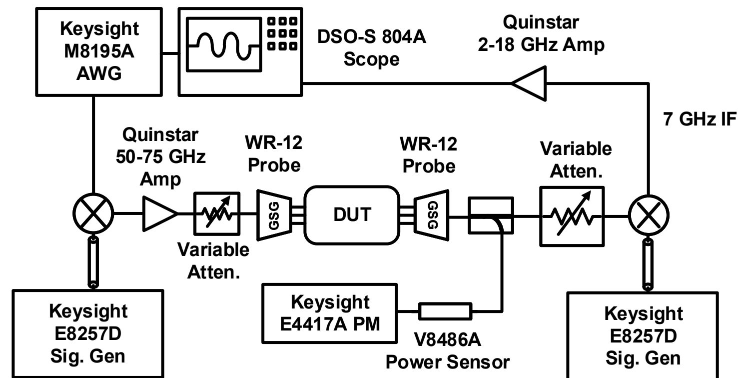
At 70 GHz, the 3-stage single-PA achieves a peak saturated output power of 15.8 dBm and a peak PAE of 18% (13% PAE at P1dB) at 67 GHz with an OP1dB $>$ 12 dBm from 61 - 77.5 GHz. The 4-stage single-PA achieves a peak saturated output power of 16.1 dBm and a peak PAE of 16.5% (12% PAE at P1dB) at 70 GHz with an OP1dB $>$ 12 dBm from 60 - 76 GHz. The 4-way combined PA achieves a

peak saturated output power of 19.6 dBm and a peak PAE of 11% (4% PAE at P1dB) at 70 GHz with an OP1dB$>$13 dBm from 70 - 77.5 GHz. The 8-way combined PA achieves a maximum output power of 24 dBm and a peak PAE of 11.5% (6.5% PAE at P1dB) at 70 GHz with an OP1dB $>$ 19 dBm from 64 - 77 GHz. Although AM-PM measurements were not taken, simulated results are shown in Fig. 2.17. For all PAs the simulated AM-PM distortion is less than 2° before P1dB and no PA variant reaches more than 6° of AM-PM distortion before reaching Psat. The single and 8-way combined PAs both show nearly identical AM-PM distortion characteristics due to their similar structures. The 4-way combined PA has a different AM-PM curve due to differences in degeneration and output matching between it and other designs.

2.4.3 Modulation Setup

Measurements with modulated waveforms at 70 GHz were conducted using the setup shown in Fig. 2.18. The waveforms are generated using a Keysight M8195A 65 GS/s arbitrary waveform generator (AWG) and upconverted using an external mixer. After passing through the PA, signals are downconverted through a second external mixer and passed to a Keysight DSO-S 804A 20 GS/s oscilloscope which applies equalization filtering and measures the error-vector magnitude. Here, the EVM is defined as the ratio of the root-mean-square (rms) error signal to the peak constellation symbol. In all measurements involving EVM in this work, equalization filtering has been applied to the received signal by the scope VSA 89601 software. Predistortion is not used.

In measurements of modulated waveforms, the AWG signal-to-noise ratio (SNR) is the maximum system measurable SNR, and this can be degraded at various points in the setup by system losses, noise and distortion from amplifiers/mixers, and LO phase noise. In this setup, the measured AWG wideband noise output is $\sim$-137 dBm/Hz at an IF of 6 GHz. For a 1-Gbaud 64-QAM waveform with square-root-raised cosine filtering and $\alpha = 0.35$, the noise in the 1.35 GHz of signal bandwidth is approximately -45 dBm. To avoid non-linear distortion from the upconversion mixer and compression from the RF amplifier, the AWG modulated signal is set to -11 dBm which results in an initial SNR of 34 dB. The loss of the upconversion mixer is 12 to 14 dB and attenuates the modulated signal to -23 to -25 dBm. This is necessary so that the signal is not compressed by the RF preamplifier with a gain of 30 dB and an OP1dB of 10 dBm. Since



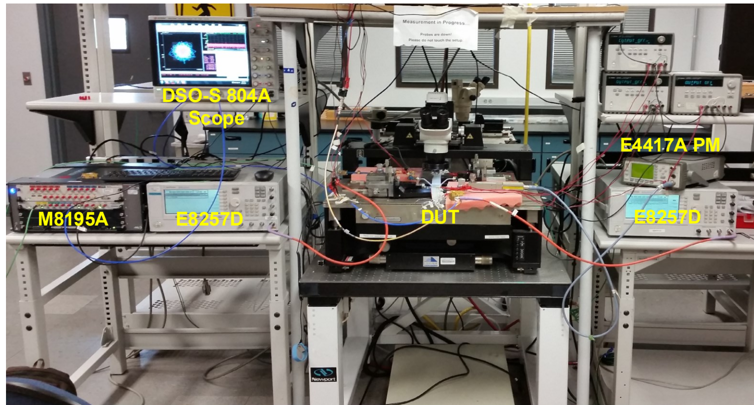


Figure 2.18: Modulated data measurement setup diagram and photo.

the wideband AWG noise is higher than thermal noise, the initial loss in the upconversion mixer does not significantly effect the system SNR, and the gain of the RF amplifiers (including the device under test (DUT)) mitigate any further SNR degradation. The image falls near 58 GHz and is rejected by the cutoff frequency of WR-10 waveguide components which connect the mixer to the amplifier. Power levels are always adjusted at the input and output of the DUT by variable attenuators rather than at the AWG in order to maintain a constant SNR for the modulated waveform.

For measurements that are corrupted only by noise, the EVM at the scope input can be calculated as: EVM $\approx$ -(SNR + PAPR) where all quantities are expressed in dB and PAPR is the peak-to-average power of the signal without square-root-raised cosine filtering (3.7 dB for 64-QAM [48]). Therefore the minimum EVM of a 1-Gbaud 64-QAM signal that is measurable with the E-band setup is -37.7 dB (and agrees well with measurements in Fig. 2.19 and 2.20).

A considerable source of EVM degradation is the phase noise introduced by the LO in the up

and down-conversion mixers. For this measurement, the LO signals were generated by Keysight E8257D signal generators which have a wideband LO phase noise floor of -135 dBc/Hz at 64 GHz [49] (which becomes -132 dBc/Hz after cable loss). To calculate the EVM contribution from the LO and determine the root-mean square (RMS) jitter, the phase noise should be integrated starting at the lower frequency bound set by the timeframe over which data is collected and up to the upper frequency (bandwidth) of the modulated signal. The RMS jitter contribution to the EVM degradation is calculated using: $EVM(\%) \approx RMSJitter(2\pi f_0)/100\%$. For example: if 1024 symbols are collected from a 100 Mbaud modulated waveform with square-root-raised cosine filtering and $\alpha = 0.35$, and a 64 GHz LO with a wideband phase noise floor of -132 dBc/Hz is used for up and down-conversion, and the close-in phase noise has reached the noise floor before 100 kHz offset: the RMS jitter should be calculated by integrating from 131 kHz (signal bandwidth / number of symbols) to 135 MHz resulting in an RMS jitter of 10 fs per LO. The equivalent RMS jitter for the two LOs is 14.1 fs. This results in an EVM degradation of 0.5% or -45 dB and sets the minimum measurable EVM of a 100 Mbaud signal.

The above example shows that although LO phase noise can add directly to EVM, several steps can be taken to mitigate its effects. For very wide bandwidth measurements, LO sources with low wideband noise floors should be used. If close-in phase noise is a problem, lowering the number of symbols sent can lessen the LO noise impact by increasing the low frequency integration bound in the jitter calculation. Still, a large enough sample of symbols should be used to obtain the EVM so that a fair measurement can be recorded. In this work, all EVM measurements are done from sets of 1024 transmitted symbols. For a more detailed analysis on the effects of white LO noise on wideband communications, the reader is referred to [47].

2.4.4 Modulation Measurements

Fig. 2.19 presents the EVM versus symbol rate measurements of 16, 64, 256, and 1024-QAM signals passed through each PA. The measurements are done in backoff to prevent distortion from clipping at high power constellation points. Results show that EVM monotonically increases with baud rate in all cases which is expected due to the increase in wideband noise with increasing symbol rates. Measurements where the PA is replaced by a thru are also included and match closely with the EVM measurements from

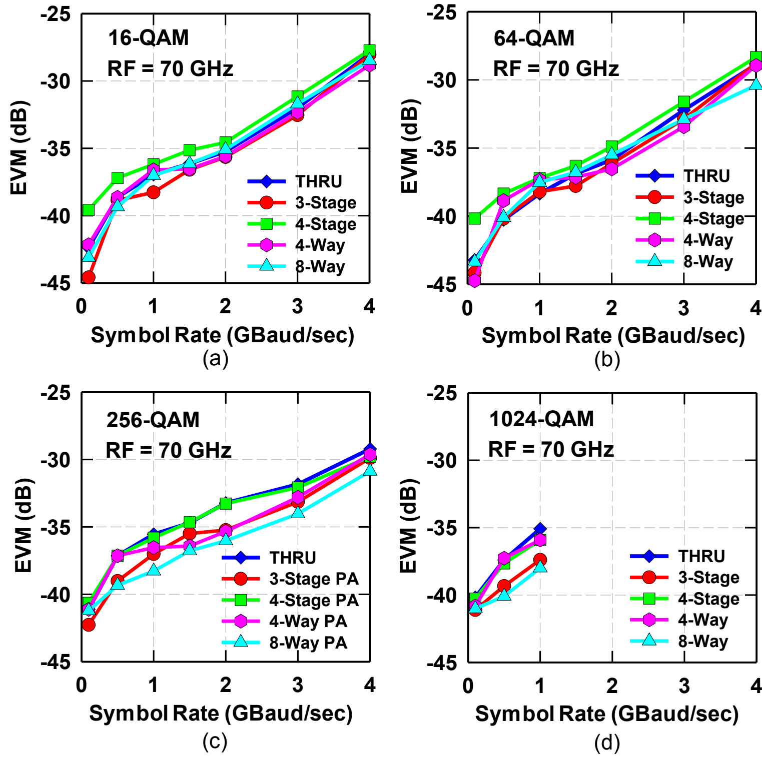


Figure 2.19: Modulated data measurements: (a) 16-QAM, (b) 64-QAM and (c) 256-QAM, and (d) 1024-QAM EVM versus symbol-rate for PAs operated in the linear mode and signals centered at 70 GHz (EVM is referenced to constellation peak).

the PAs. Note that the PA results are in some cases better than the thru due to the improved SNR arising from the amplifier gain.

Fig. 2.20 presents the measured EVM and PAE for each PA versus average output power of a 1-Gbaud 64-QAM signal (6 Gbps) with square-root-raised-cosine filtering with α of 0.35 (7.7 dB peak-to-average-power-ratio (PAPR)) centered at 70 GHz for each PA. The baseline EVM for each PA in far backoff is -35 dB and is caused by the measurement setup noise floor. The EVM and PAE are measured up to around 0 dB backoff (defined here as the point when the average output power is equal to P_{1dB}). At 0-dB backoff the 4-stage single-PA achieves -23 dB EVM and 8.5% PAE, the 4-way combined PA achieves -28 dB EVM and 2.5% PAE, and the 8-way combined PA achieves -24 dB EVM and 6% PAE. The lower efficiency of the 4-way combined PA at 0 dB backoff is partially due to its softer compression characteristic than the single and 8-way combined PAs. Notably the soft compression does not significantly increase the rate at which EVM rises with output power compared to the 8-way combined PA. The results show that for

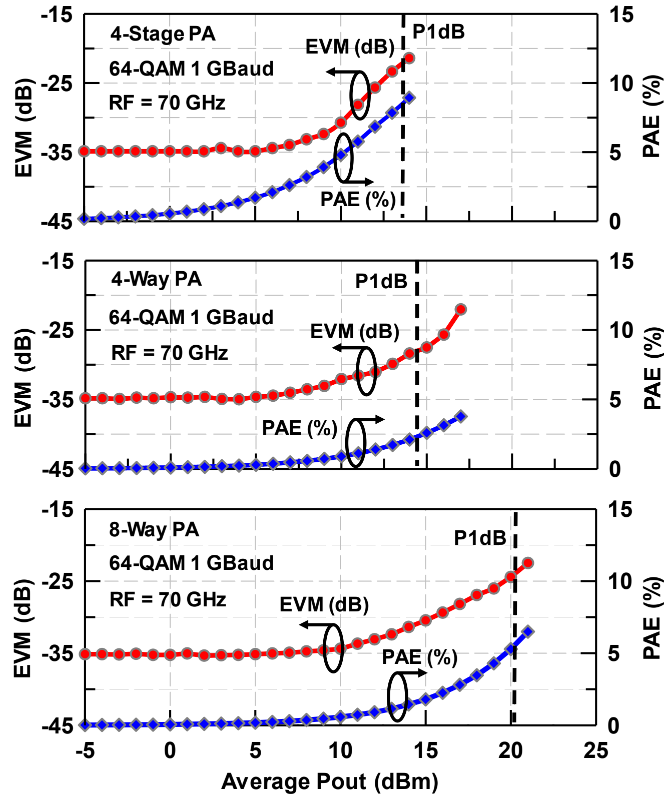


Figure 2.20: Measured EVM and PAE versus average output power for a 1-Gbaud 64-QAM modulated signal centered at 70 GHz with square-root-raised-cosine filtering (α = 0.35, PAPR = 7.7 dB) for (a) 4-stage single-PA, (b) 4-way combined PA, and (c) 8-way combined PA. (EVM is referenced to constellation peak in all plots), (3-stage single-PA is left out for brevity but achieves similar results to the 4-stage single-PA).

all PAs the EVM versus average output power of a modulated signal follows a nearly identical trend to the EVM versus average output power of a single tone.

Fig. 2.21 shows detailed EVM measurements versus average output power for all PAs for 16-QAM and 64-QAM signals with square-root-raised-cosine filtering with α = 0.35 (6.6 dB and 7.7 dB PAPR respectively [48]). The thermal and LO noise EVM is around -40 dB for 100 Mbaud waveforms and measurements clearly show the nonlinear distortion contribution at backoff levels higher than the waveform PAPR. The EVM results for 16 and 64-QAM signals show identical shapes but are offset by the difference between their PAPR (1.1 dB) on the x-axis.

The constellation and respective spectrum of the 1-GBaud 64-QAM signal passed through the 8-way combined PA with an average output power between 16 and 20 dBm are shown in Fig. 2.22. The measurements represent signal spectrums before equalization filtering. To the authors knowledge, this is

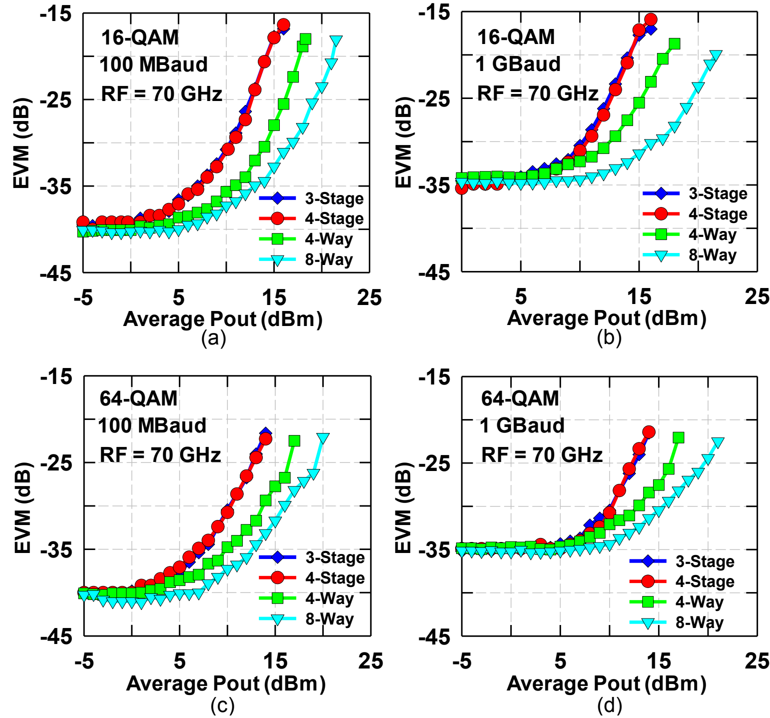


Figure 2.21: Measured EVM versus average output power of all PAs for 16 and 64-QAM with square-root-raised-cosine filtering with $\alpha = 0.35$ (6.6 dB and 7.7 dB PAPR for 16 and 64 QAM signals respectively) with various data rates (a) 16-QAM 100-Mbaud, (b) 16-QAM 1-Gbaud, (c) 64-QAM 100-Mbaud, (d) 64-QAM 1-Gbaud, (EVM is referenced to constellation peak in all plots).

the first time measurements have been presented which demonstrate an amplifier outputting modulated data in a linear mode and >50 - 100 mW average output power at these frequencies.

2.4.5 Comparison

As expected, the S.E. power amplifiers presented in this work showed higher efficiencies than the differential power amplifier due to the higher Q of its matching components and output network. Notably, the differential PA also showed a significantly softer compression curve than the S.E. amplifiers, with P1dB being separated from Psat by ∼5 dB. Soft compression may be due to unmodeled parasitic inductances on the emitters of the differential PA devices before the virtual ground point. In modulated data measurements, despite the softer compression characteristics of the differential PA, EVM did not increase considerably faster with power than for the single or 8-way combined S.E. PAs, suggesting that soft compression may not be a significant limiter of performance for the amplifier.

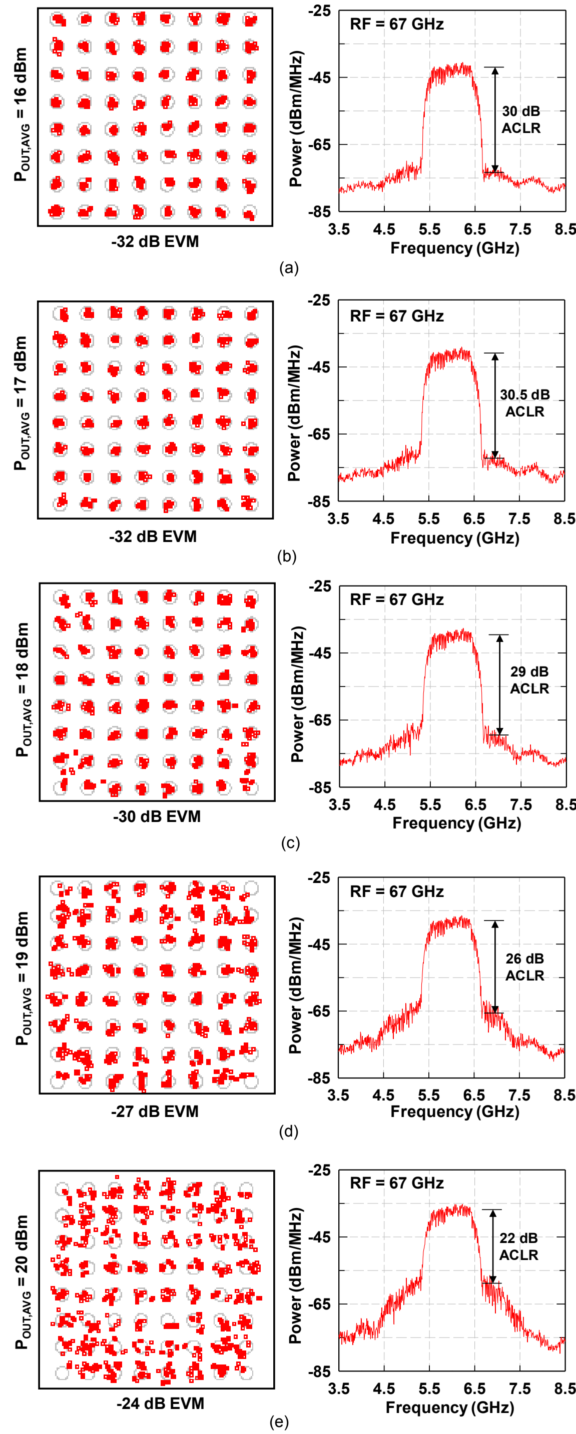


Figure 2.22: Measured constellations and spectrums of 64-QAM 1-Gbaud signals (α = 0.35, PAPR = 7.7 dB) centered at 67 GHz with various average output powers transmitted by the 8-way combined PA. Equalization filtering is used in constellation measurements but is not applied to the spectrum measurement.

Table 2.1: E-Band Power Amplifier Comparison to Previously Published Works

Freq (GHz)	Tech.	Circuit	Gain (dB)	Psat (dBm)	OP1dB (dBm)	PAE (%)	Vdd (V)	Area (mm^2)	Ref.
60-77	0.12 μm SiGe	3 & 4 Stage S.E. C.E.	18 & 25	15.8 & 16.1	13.6 & 13.2	18.1 & 16.5	2.0	0.93	This Work
67-80	0.12 μm SiGe	4-Way Diff. C.E.	18.5	19.5	14.5	11	2.0	1.46	This Work
60-75	0.12 μm SiGe	8-way S.E. C.E.	22	24.0	21	12	2.0	3.34	This Work
79-97	0.13 μm SiGe	Diff. C.E.	10.6	19.6	18	15.4	2.3	2.4	[50]
85-105	0.12 μm SiGe	4-Way Cascode	15	23.4	20.2	16.8	4	0.54	[28]
75-105	90 nm SiGe	Class E Cascode	17	22	-	19.1	4.4	1.425	[43]
68-91	90 nm SiGe	16-Way S.E. C.E.	19.3	27.3	22.3	12.4	1.8	6.48	[25]
51-67	55 nm SiGe	Single Stage C.E.	7	9	7	20	1.2	0.29	[51]
60-66	55 nm SiGe	4-Way Cascode	23.8	23.4	20	12.5	3.0	0.17	[52]
74-86	45 nm CMOS SOI	8-Way Cascode	10.1	21.1	-	5	2.0	1.0	[26]
70-95	45 nm CMOS SOI	Cascode	11	12.4	12.0	14.2	2.0	0.322	[45]
82-96	45 nm CMOS SOI	3-Stack FET	12.4	19.2	15	14	3.4	0.21	[44]
65-92	32 nm CMOS SOI	PMOS 3-Stack FET	11	18.7	16	24	3.6-4.5	0.12	[42]
60 - 75	40 nm CMOS	8-Way Xformer (Cascode)	19	21	19	13.6	1.5	0.187	[37]
59-67	40 nm CMOS	4-Way Xformer Push-Pull	22	16.4	13.9	23	1.8	0.09	[30, 31]
70-85	40 nm CMOS	4-Way Diff.	18.1	20.9	17.8	22.3	0.9	0.19	[38]
60	40 nm CMOS	4-Way Xformer	17.0	17.0	13.8	30	1	0.074	[35]
70-80	65 nm CMOS	4-Way Xformer	21	15.8	13	15.2	2	0.375	[36]
57-65	65 nm CMOS	8-Way Xformer	32.4	20.2	17.4	22.9	1.2	0.32	[34]
50-70	65 nm CMOS	32-Way	16.3	23.2	19.6	10	1.2	2.04	[27]

Table 2.1 compares this work to the current state of the art works. PAs from this work demonstrate some of the highest reported output powers and PAEs at these frequencies with the 8-way combined PA demonstrating the second highest output power within the frequency range of 60 - 80 GHz to date. The single-PAs also demonstrate PAE which is comparable to the best published results. Among works in comparable SiGe processes the PAs presented achieve some of the highest powers and efficiencies reported. Fig. 2.23 plots the saturated output power and peak PAE versus frequency of each PA alongside other published works.

2.5 Conclusion

This chapter presented a 3-stage single, 4-stage single, 4-way, and 8-way combined PA in 0.12 μm SiGe. The 4-stage single-PA achieved a saturated output power of 16.1 dBm and peak PAE of 16.5% while the 8-way combined PA achieved saturated output power of 24 dBm with peak PAE of 12%. Measurements

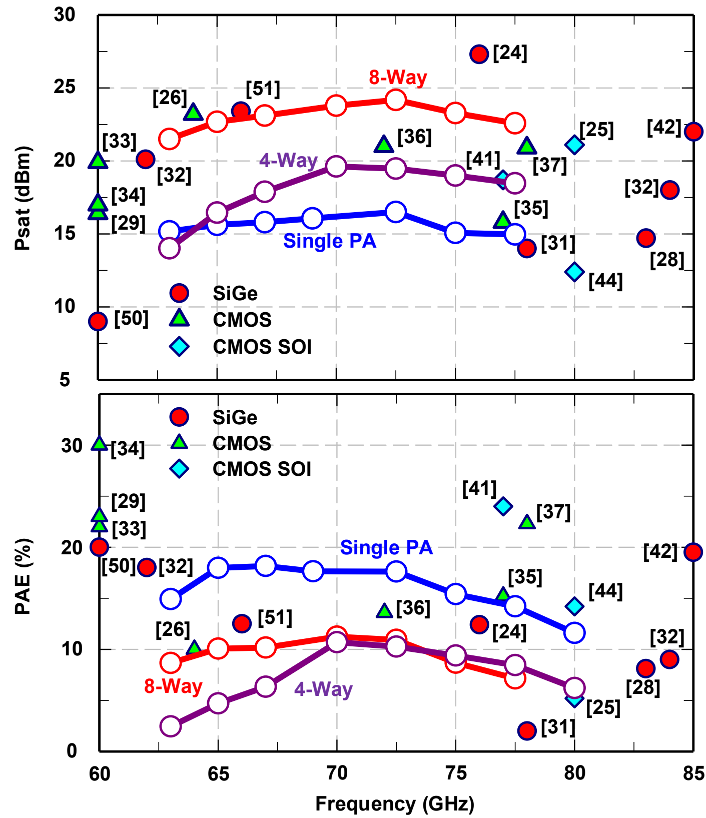


Figure 2.23: Comparison with previously published works.

of modulated data were presented. When operated in the linear mode all PAs could pass 32 Gbps 256-QAM signals and 24 Gb/s 64-QAM signals with ∼-30 dB EVM (referenced to constellation peak). Detailed measurements of EVM and PAE versus output power were presented which show how modulated signals degrade as a function of output power and efficiency. Results show that the 8-way combined PA is capable of passing a 1-GBaud 64-QAM signal in a linear mode with 50 - 100 mW average output power at 70 GHz.

Acknowledgment

Chapter 2, in full, is a reprint of the material in: E. Wagner and G. M. Rebeiz, "Single and Power-Combined Linear E-Band Power Amplifiers in 0.12 μm SiGe With 19-dBm Average Power 1-GBaud 64-QAM Modulated Waveforms," in *IEEE Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and author of this paper. The author would also like to thank Analog Devices for technical discussion and project funding, and Integrand Software for supplying

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Chapter 3

Packaging Effects on Stability in Millimeter-Wave Silicon Amplifiers

3.1 Introduction

Interest in silicon-based millimeter-wave (mm-wave) wireless systems has grown in recent years due to their applications in short range high data-rate communications [9–13], automotive radar [4–6], and imaging systems [7, 8]. Among the critical challenges facing widespread deployment of such systems are the problems related to packaging, and specifically the effects of the interfaces between an integrated circuit (IC) and the printed-circuit board (PCB) that it is assembled onto (e.g. bondwires, bondribbons or bumps). While at lower frequencies the effects of bondwires and bumps may be ignored, the parasitic inductances introduced by these interfaces are large enough to considerably effect the performance of both passive and active structures at microwave and mm-wave frequencies, and when proper design precautions are not taken, can lead to spurious oscillations and detuning.

This paper is organized as follows: Section II outlines the methods through which packaging parasitics contribute to instabilities in mm-wave amplifiers. A simple schematic model of packaging parasitic effects is offered and its limitations are analyzed through full-wave electromagnetic (EM) simulations. Section III offers a discussion of techniques and best-practices for mitigating packaging

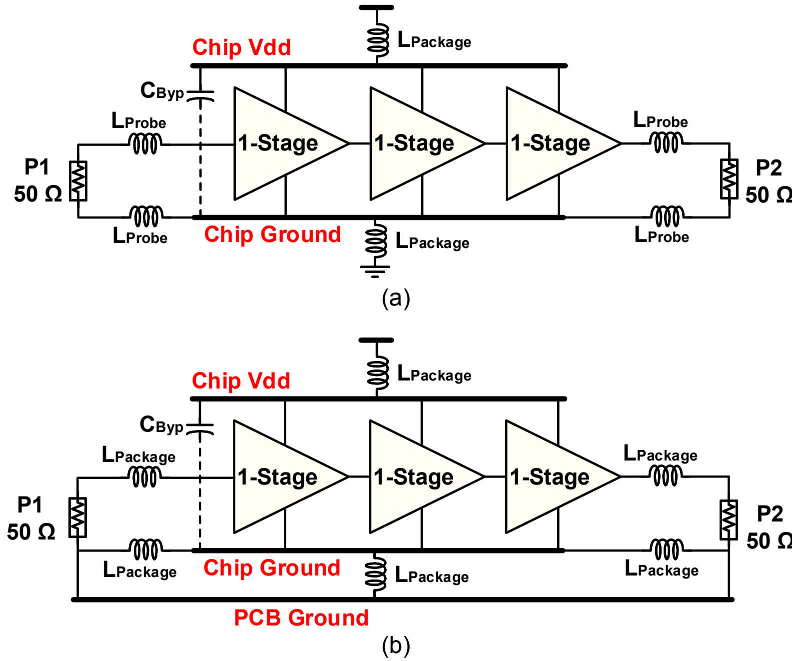


Figure 3.1: Schematic description of the difference between measurements of (a) probed and (b) packaged single-ended amplifier ICs.

instabilities. Effective and ineffective mitigation strategies are described and confirmed through EM simulations. Section IV presents the design and assembly of a set of silicon E-band power amplifiers (PAs), originally described in [1], on low-cost PCBs. Small and large-signal measurements of packaged amplifiers are presented in Section V, and confirm that, due to the precautions taken during the design phase, none of the PA variants experience spurious oscillations or detuning after assembly. Section VI offers a summary and conclusion.

3.2 Packaging Effects on Stability

The difference between probed-on-wafer and packaged measurements of a single-ended amplifier IC is described in Fig. 3.1. Fig. 3.1(a) presents a 3-stage amplifier IC which is receiving its dc bias (vdd and dc ground) either from wirebonds/bumps to a dc board or even using dc-probes, and is being tested using a set of RF probes placed at the input and output chip GSG pads. The parasitic inductances $L_{Package}$ on the vdd and ground nodes of Fig. 3.1(a) do not cause feedback between the chip's RF input and output ports and do not effect the RF performance so long as the bypass capacitance between the chip vdd and

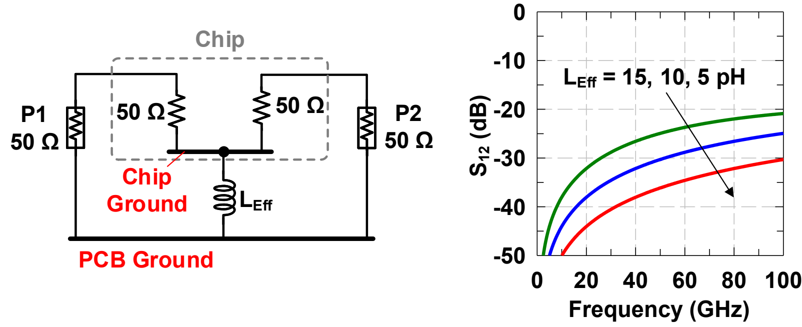


Figure 3.2: Schematic and simulated S_{12} of two-port chip with 50 Ω terminations and simplified packaging model.

ground nodes is sufficiently large.

Fig. 3.1(b) presents the same amplifier after it is packaged and assembled onto a PCB. Once packaged, the RF input and output signals propagate to and from the chip through transmission-lines printed on the PCB and are referenced to the PCB ground plane. Any impedance between the shared reference ('Board Ground' in Fig. 3.1(b)) and the chip reference node ('Chip Ground' in Fig. 3.1(b)) creates a voltage on the chip ground node which can detune passive structures and cause amplifier instabilities. Looked at another way, if the system reference is moved to the chip ground node, then the PCB ground node amounts to a direct feedback path between the amplifier input and output ports.

To provide the reader with intuition of how package parasitic-inductance affects the chip performance, Fig. 3.2(a) presents a simplified model of a two-port packaged IC containing nothing but 50 Ω terminations to ground at the chip input and output ports. In this model, the inductance separating the chip and PCB ground nodes (labeled 'L_{Eff}' in the figure) represents the parasitic inductance of the bumps or bondwires between the chip and PCB grounds. Fig. 3.2 also presents the simulated S_{12} of the chip for various values of L_{Eff}. Ideally, this chip configuration has perfect isolation between its two ports, however, as the value of L_{Eff} increases, a considerable frequency-dependent coupling is observed, which can be > -30 dB at mm-wave frequencies even for small values of L_{Eff}.

To provide further intuition, Fig. 3.3(a) presents the schematic of an active IC with packaging parasitics modeled as L_{Eff} between the chip and PCB grounds. The active IC, modeled as a three-stage amplifier where individual stages are g_m sources with a wideband input, a narrowband output impedance match, and infinite reverse isolation, still shows a considerable magnitude of S_{12} (Fig. 3.3(b)) for large

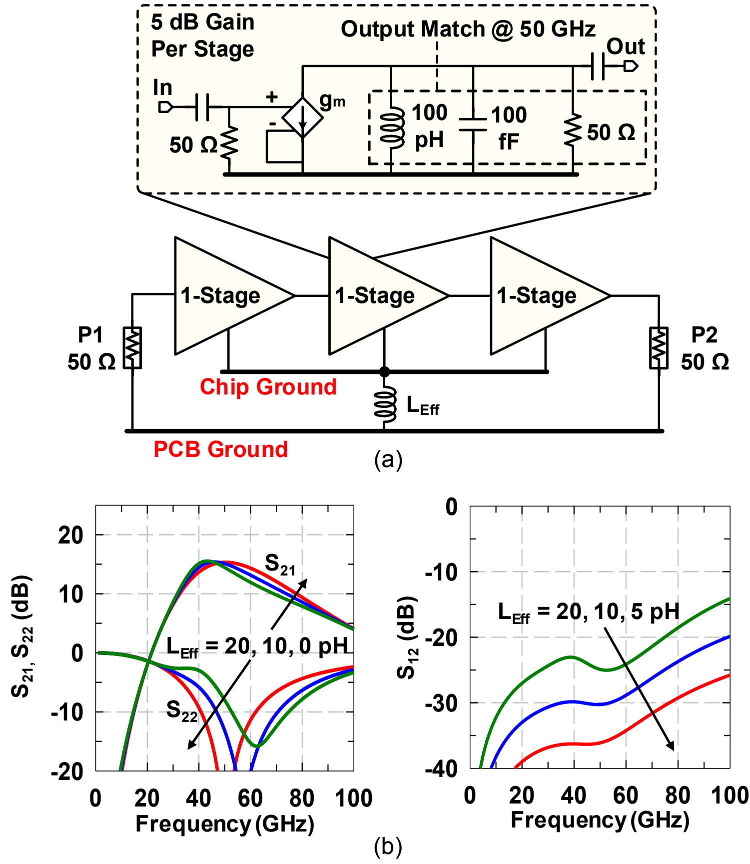


Figure 3.3: (a) Circuit schematic of a 3-stage 50 GHz amplifier with simplified packaging model, 50 Ω input and output match in each stage, and gain set by the value of g_m. (b) S_{21}, S_{22}, & S_{12} versus frequency for various values of L_{Eff}.

values of L_{Eff} despite the infinite reverse isolation in the amplifier stages, and has the potential to become unstable for high values of L_{Eff}. Additionally, even before the onset of instability, the amplifier's S_{21} and S_{22} experience significant detuning as L_{Eff} increases.

The reason why the circuits shown in Figs. 3.2 and 3.3 experience coupling and detuning despite their ideal on-chip reverse isolation is because L_{Eff} *creates a feedback path directly between chip input and output ports through the chip ground node.* The consequence is that even if a circuit is unconditionally stable before packaging, if the connection between the chip and PCB ground is not good enough (high L_{Eff}), the amplifier may oscillate or detune after packaging.

In practice, the simplified package parasitic model of Figs. 3.2 and 3.3 is only accurate over a limited frequency range due to the fact that the chip and PCB ground planes are actually distributed

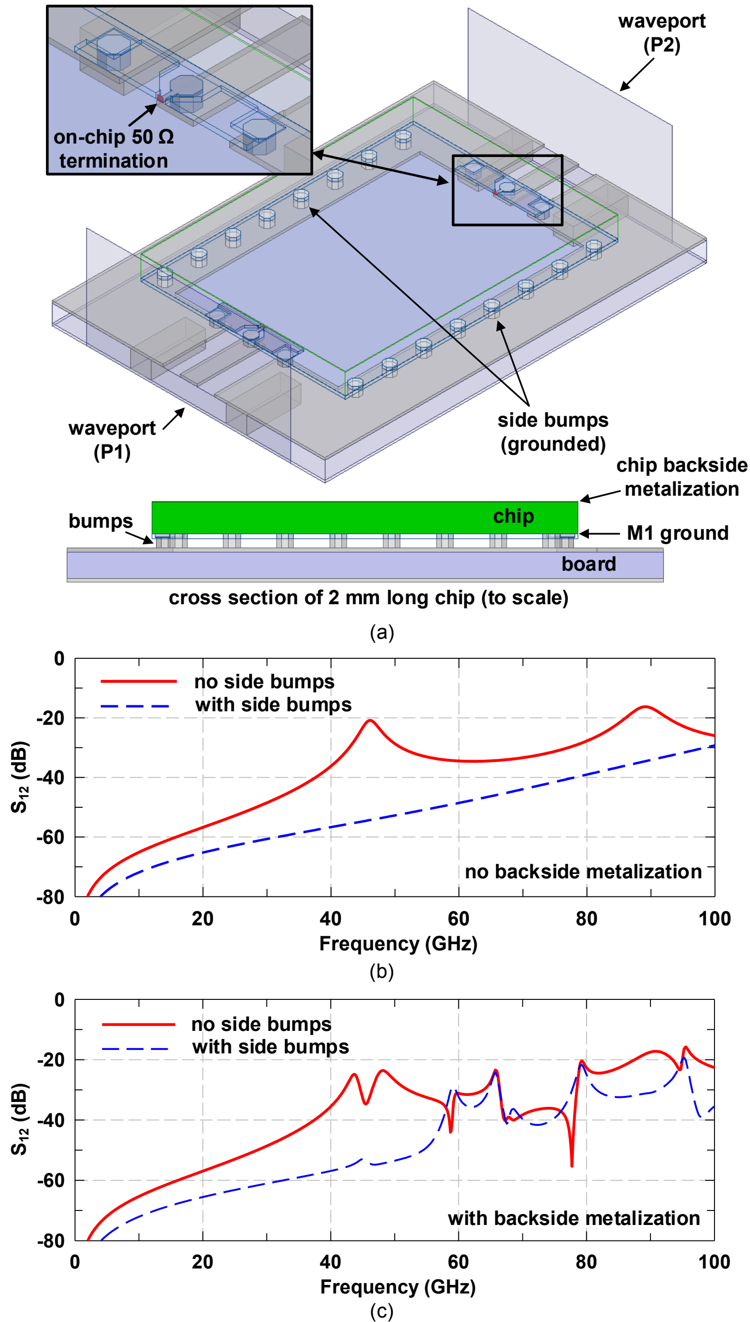


Figure 3.4: (a) HFSS model and (b) simulation results for 1.5 x 2.0 mm bumped silicon chip with different grounding configurations and chip backside metalizations. Signal is fed to circuit board through waveports and terminated on chip in 50 Ω lumped ports just after the GSG pads. Chips contain solid M1 ground plane that covers entire chip, side bumps are electrically connected to PCB ground, and all metals are perfect electric conductors.

structures where long physical (and electrical) distances may separate the chip-to-board interconnects. This leads to a resonant behavior at frequencies where these distances approach a fraction of a wavelength.

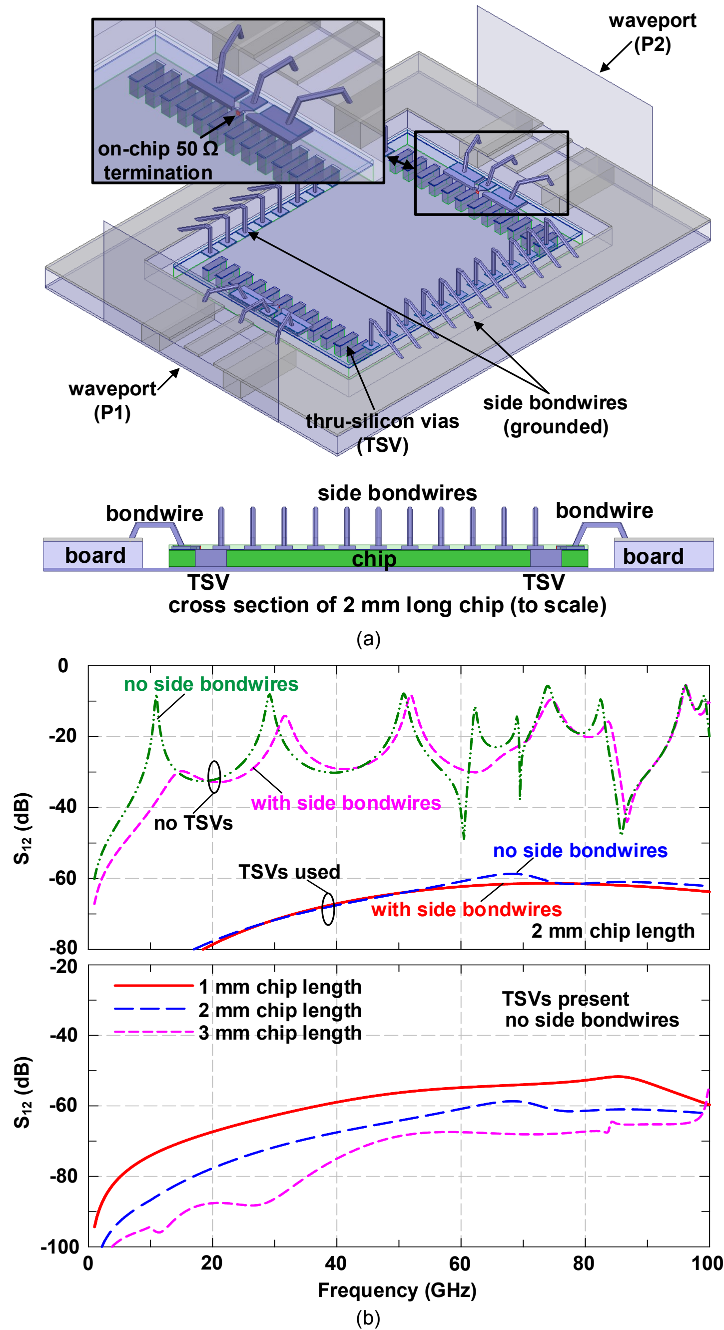


Figure 3.5: (a) HFSS model and (b) simulation results for wirebonded 1.5 mm wide silicon chip with different size and grounding configurations. Signal is fed to circuit board through waveports and terminated on chip in 50 Ω lumped ports just after the GSG pads. Chips contain solid M1 ground plane that covers entire chip, side bondwires are electrically connected to PCB ground, and all metals are perfect electric conductors.

This is exemplified in Fig. 3.4 where a small silicon chip assembled on a PCB using flip-chip packaging is modeled in Ansys HFSS [53]. In the model, the RF signal is fed to the PCB using waveports on

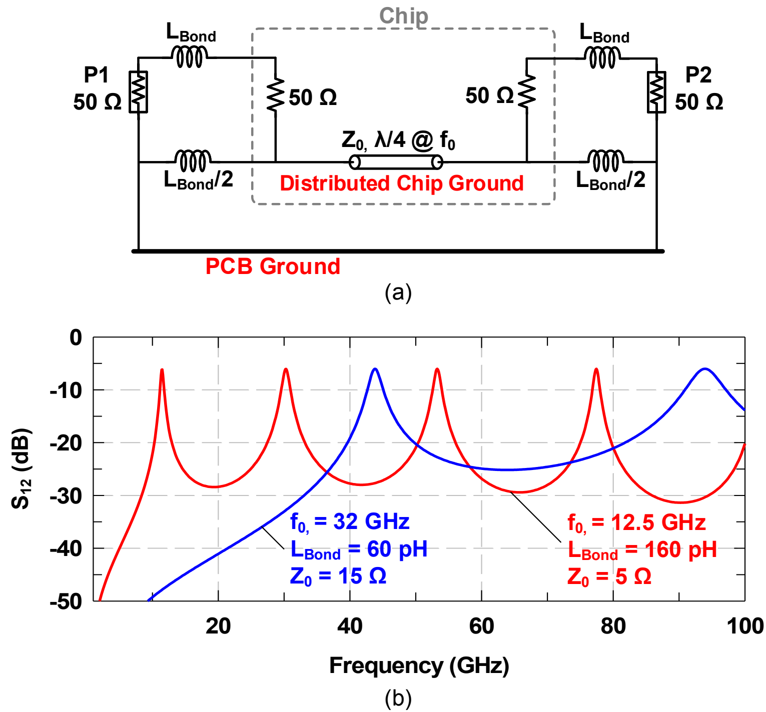


Figure 3.6: Schematic model and simulated S_{12} of chips from Figs. 3.4 and 3.5(a).

either side of the chip. The RF signal enters the chip through GSG bump pads with 250 μm pitch and is terminated using a lumped 50 Ω port with the ground being a chip-wide plane on the bottom (M1) metal layer, effectively mimicking the circuit schematic of Fig. 3.2. Grounded bumps with a spacing of 250 μm are also included along the chip sides to ensure a strong ground connection. Fig. 3.4(b) presents the simulated S_{12} with and without the side bumps. Simulations show that when side bumps are present, S_{12} is well-behaved and mimics the L_{Eff} model well. When the side bumps are not present, the port-to-port coupling experiences spikes at 45 and 90 GHz. At these frequencies, the ground plane is one quarter and one half wavelength respectively and is beginning to resonate and radiate as a microstrip patch. It is worth noting that the inclusion of side bumps does not completely eliminate resonances in S_{12} but rather pushes the resonances to a higher frequency determined by the spacing and number of bumps.

If the backside of the bumped chip is metalized, as is sometimes done for thermal reasons (e.g. for a heat-sink die attach), additional resonance issues may arise since the chip's M1 ground plane can form a parallel-plate waveguide with the metalized backside of the chip. This parallel-plate waveguide causes coupling between the chip input and output ports due to TEM modes that may be excited at

mm-wave frequencies (∼42.5 GHz in a 1.5 x 2.0 mm chip) and which depend on the geometry of the chip ground plane, and grounded bump locations. The simulated S_{21} with backside metalization shows chaotic resonances which are pushed higher in frequency, but not entirely eliminated by the inclusion of side bumps (Fig. 3.4(c)).

Fig. 3.5(a) presents results for a similar HFSS simulation where the chip is wirebonded and is placed inside a cut-out (cavity) in the PCB. The back of the chip is metalized and is connected to the PCB ground plane using eutectic die metal attach. Also, thru-silicon vias (TSVs) are placed at the chip input and output ports to connect the ground plane on the top layer (M1) to the chip ground on the back-side. Grounded bondwires are used with 150 μm pitch along the sides of the chip for additional grounding. The simulated S_{12} is shown for various configurations of TSV and grounded side bondwires (Fig. 3.5(b)). For both cases where TSVs are not used, resonances as high as -10 dB occur approximately every 20 GHz and are due to the resonating chip ground plane. The addition of extra grounding through the side bondwires does little to mitigate the high S_{12} coupling (especially above 30 GHz). This is because the side bondwires themselves are high impedance and therefore do not improve the grounding at mm-wave frequencies. When TSVs are present, S_{12} takes a well-behaved form, which is the result of a low effective inductance between the chip and PCB ground. As the length of a TSV chip is increased, S_{12} drops suggesting that magnetic coupling or radiation between input and output bondwires is the primary cause of output-to-input coupling, rather than parasitic inductive separation between the chip and PCB grounds.

To understand the resonances which occur in both the wirebond (no TSVs) and flip-chip designs when the chip sides are not grounded, a more complex schematic model which treats the chip ground plane as a transmission line with finite length and characteristic impedance (Z_0) can be used (Fig. 3.6(a)). This model is derived by recognizing that the chip ground plane forms a transmission-line with the ground trace of the PCB underneath the chip. The chip ground transmission-line length is approximately the geometric mean between the chip's width and length, and the characteristic impedance Z_0 can be calculated using the physical parameters of the chip (e.g. assuming the ground plane of the chip in Fig. 3.5 forms a microstrip line with the PCB ground with parameters ε_r = 11.7, H = 80 μm, W = 1.5 mm and L = 2.0 mm, the characteristic impedance is calculated as 5.2 Ω). Using the estimated values of the ground plane effective length, Z_0, and bump/bondwire impedance, it can be seen that the ground plane resonances of the chips of

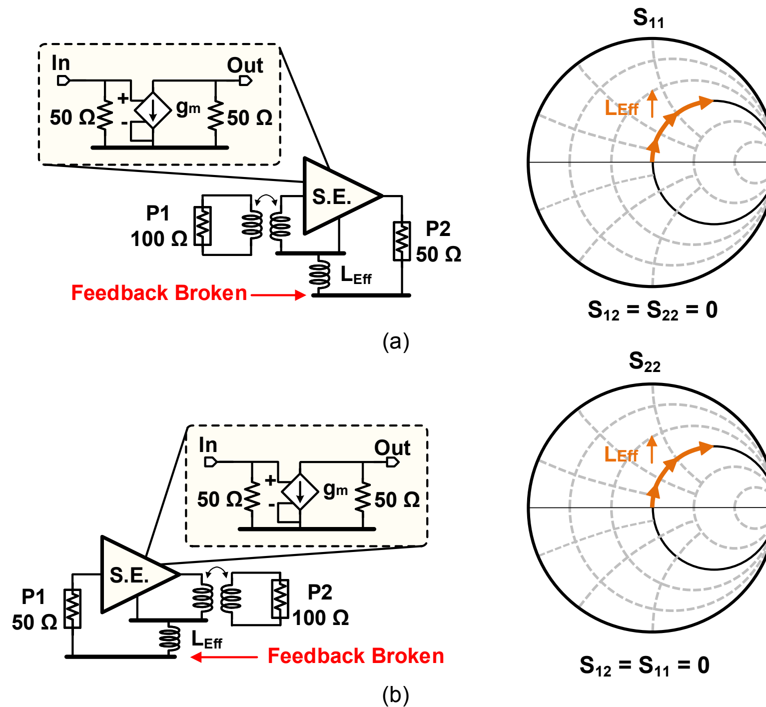


Figure 3.7: (a) Schematic and S_{11} of a single-ended (S.E.) amplifier which is stabilized in the presence of packaging parasitic inductances by using an ideal transformer balun on the input port and all S.E. active circuitry, (b) schematic and S_{22} of a S.E. amplifier which is stabilized using an ideal transformer balun on the output port and all S.E. active circuitry.

Figs. 3.4 and 3.5 can be estimated with good accuracy (Fig. 3.6(b)).

3.3 Mitigation Strategies

3.3.1 Minimizing Packaging Parasitics

The simplest mitigation strategy is to minimize the parasitic inductance between the chip and PCB grounds so that the effective impedance separating the chip ground from the PCB ground is near 0. As demonstrated in Fig. 3.5, this can be trivial in designs where thru-silicon vias are employed. However when flip-chip packaging or wirebond packaging (with no TSVs) is required, decreasing L_{Eff} can only be achieved by increasing the number of transitions between the chip and board grounds. Flip-chip packaging presents an obvious advantage in this regard since bump inductances (50-60 pH) are typically much lower than wirebond inductances ($\sim$1 nH per mm). The exact number of ground connections required to ensure

a design remains stable after packaging will be determined by the gain of the chip, and if proper grounding can not be ensured, chip gain can always be reduced during the design phase to guarantee stability after packaging.

If a design is expected to work at mm-wave frequencies, the resonances between the chip and PCB ground should also be carefully considered. For wirebond chips, the use of TSVs is necessary. For flip-chip designs, the maximum distance between individual ground bumps will have an effect on the lowest frequency at which the chip ground plane may resonate, and evenly spacing the ground bumps throughout a chip is a good practice for mitigating resonances. It is also recommended that the backside of bumped chips should not be metalized. If backside metalization is used, then additional EM simulations are recommended to ensure that the parallel-plate waveguide formed by the chip ground plane and the backside metalization is not excited within the intended frequency band.

3.3.2 Using Differential Structures

When reducing the chip gain or the impedance between the chip and PCB ground nodes is not possible, the feedback caused by package parasitic inductances can be removed with the use of differential input and/or output ports. Visualized in Fig. 3.7(a) and (b), this strategy works because one or both ports on the PCB are no longer referenced to the PCB ground node through which the feedback signal would otherwise flow[1]. Additionally, if an on-chip balun is used to convert between differential signaling at the PCB ports to single-ended signaling on the chip, L_{Eff} will appear in series between the single-ended chip port and ground, leading to detuning of the input match at the differential port. Conveniently, any single-ended circuitry that follows the balun will be properly referenced to chip ground and will not experience additional detuning. For this reason, whenever an on-chip balun is utilized in a chip with differential ports, foreknowledge of the chip assembly method is necessary so that the proper L_{Eff} can be accounted for and tuned out in the balun's matching network.

A full-wave EM simulation was performed using Ansys HFSS on a bumped chip similar to that of Fig. 3.4(a) but with a differential output port (Fig. 3.8). The simulated S_{12} confirms that when P2 is excited in the differential-mode, coupling is rejected by an additional $\sim$60 dB. However when P2 is

[1] Use of a differential input or output port works regardless of whether the chip's internal circuitry is single-ended or differential.

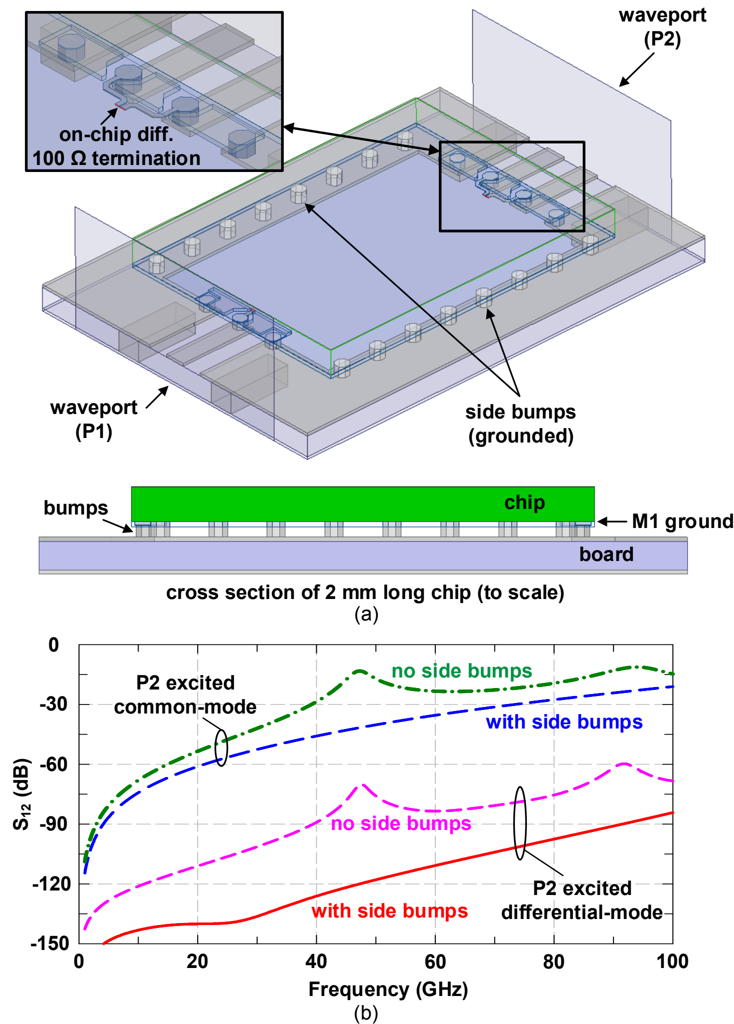


Figure 3.8: (a) HFSS model and (b) simulation results for 1.5 x 2 mm bumped silicon chip with single-ended input and differential output. Signal is fed to circuit board through waveports and terminated on chip in 50 Ω lumped ports just after the GSG pads. Chip contains solid M1 ground plane that covers entire chip, side bumps are electrically connected to PCB ground, and all metals are perfect electric conductors.

fed in common-mode, the S_{12} curve becomes nearly identical to that of the chip with single-ended ports. Therefore, when differential ports are utilized to mitigate package parasitics, the chip common-mode gain should be carefully designed so that problems do not arise due to the remaining common-mode PCB ground feedback path.

Fig. 3.9 presents a chip with differential active circuitry, but converts to single-ended signaling at the chip input and output ports. Use of this topology is tempting because differential lines and ports on a PCB are hard to build and are not compatible with microstrip or CPW lines. It may be intuited (correctly)

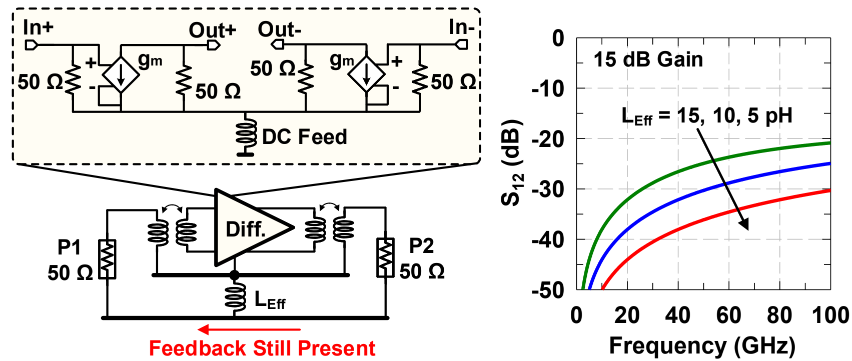


Figure 3.9: Schematic and S_{12} of a differential amplifier which is still vulnerable to packaging parasitic effects on S_{12} because its input and output ports are converted to S.E. before leaving the chip.

that detuning due to L_{Eff} will not be seen by the differential circuits since they are referenced to a 'virtual ground' (at the point of symmetry) and not the chip ground. This topology is, however, still vulnerable to feedback between the single-ended input and output ports. *This is because the direct connection between the reference nodes of ports 1 and 2 remains unbroken.* Using this topology, the simulated S_{12} still grows with L_{Eff} (Fig. 3.9), and the magnitude of the S_{12} coupling in the differential design is equal to that of an equivalent single-ended design.

3.3.3 Splitting PCB or Chip Ground Planes

Since the feedback caused by package parasitics is due to the continuous PCB or chip ground plane (depending on which is considered to be the system reference), a split in either ground plane can theoretically open-circuit the feedback path, therefore solving the issues of detuning and spurious oscillations. While this logic is sound in theory, in practice splitting ground planes will rarely work due to the non-zero capacitive coupling that is inevitable between the split ground planes. Additionally, it is virtually impossible to break the chip ground in an RF amplifier unless the ground plane is broken at a point where the signal is routed differentially, otherwise the RF signal will see an open circuit at the point of the break due to the cut in the signal return path.

The schematic model of Fig. 3.6(a) where the chip ground is treated as a distributed structure can also be used to analyze the effects of ground splits by breaking the ground plane transmission line into two sections of half-length and adding a capacitance C_{Coup} between them (Fig. 3.10(a)). Using the schematic

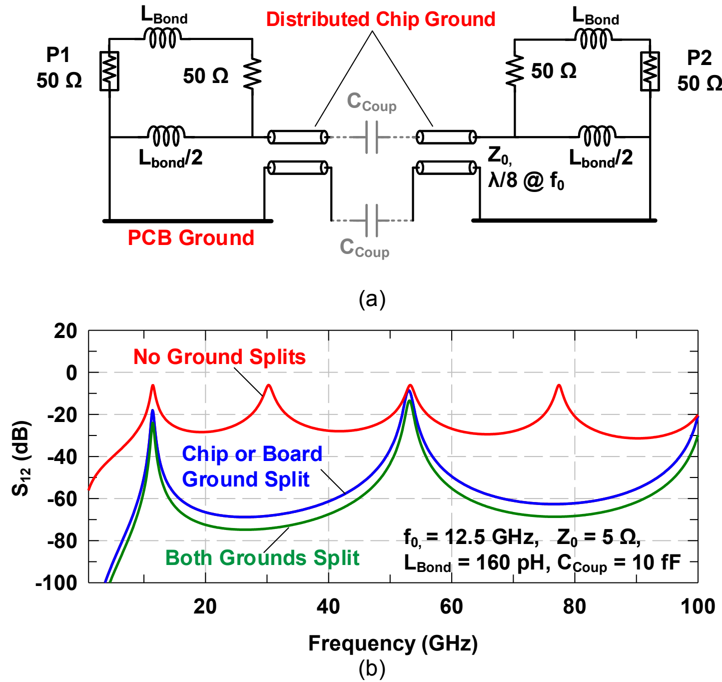


Figure 3.10: (a) Schematic model and (b) S_{12} of wirebonded 1.5 x 2.0 mm silicon chip with 50 Ω terminations at input and output for various configurations of chip and PCB ground plane splits.

component values of Fig. 3.5 and assuming a capacitive coupling between splits of only 10 fF, the simulated S_{12} shows considerable attenuation at frequencies far from resonance, however coupling at the resonant frequencies remains nearly unchanged. (Fig. 3.10(b)). This solution is therefore not recommended.

To confirm the validity of the schematic model of Fig. 3.10(a), full-wave EM simulations were performed in HFSS on a wirebonded chip containing 100 μm splits in both the chip and PCB ground planes (Fig. 3.11). The resulting simulated S_{12} follows the curves predicted by Fig. 3.10(b), confirming that splitting the chip and board grounds does not completely remove the resonant S_{12} behavior.

3.4 Packaged E-Band PA Design

To demonstrate the implementation of stable, packaged mm-wave amplifiers, several high-gain PAs implemented in Global-Foundries' 0.12 μm SiGe BiCMOS 'GF8HP' process working between 64 and 78 GHz were assembled and measured on low-cost printed-circuit boards. The PAs consist of wirebonded, single-ended single and 8-way combined PAs whose designs were previously reported in [1]

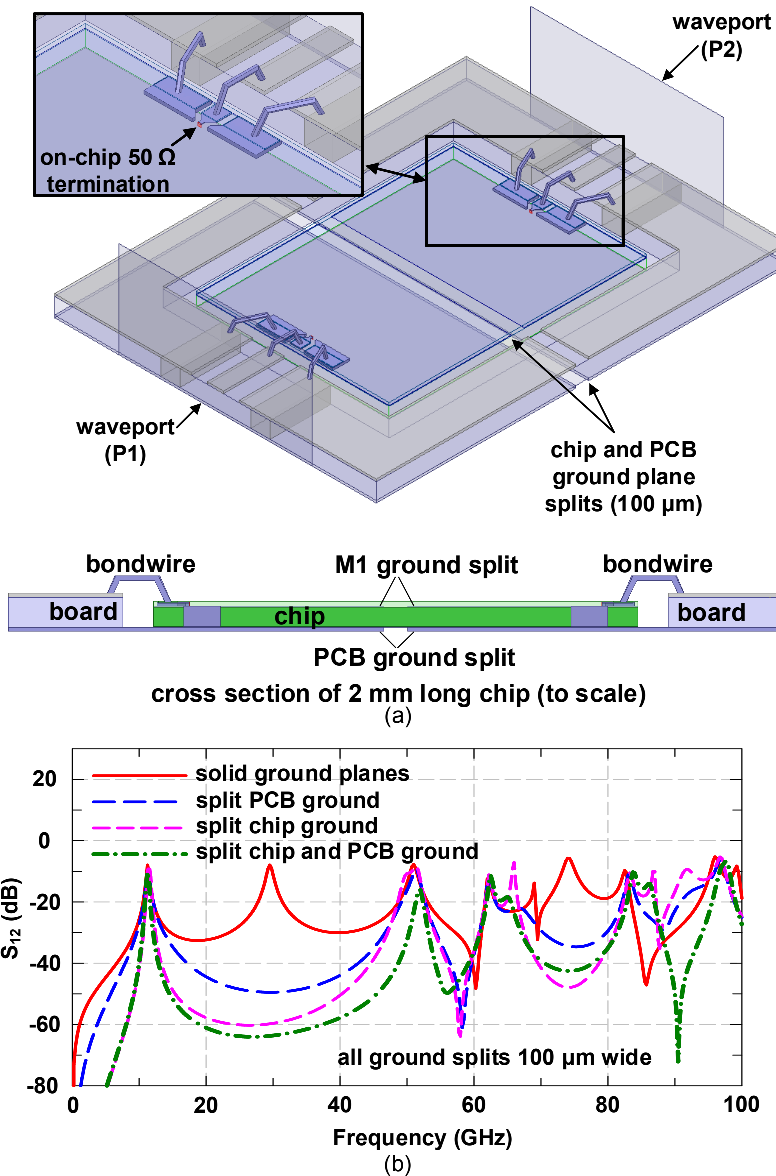


Figure 3.11: (a) HFSS model and (b) simulated S_{12} for wirebonded 1.5 x 2.0 mm silicon chip with 100 μm splits in the chip and PCB ground planes. Signal is fed to circuit board through waveports and terminated on chip in 50 Ω lumped ports just after the pads. Chips contain solid M1 ground plane that covers entire chip, side bondwires are electrically connected to PCB ground, and all metals are perfect electric conductors.

(Fig. 3.12(a) and (b)). Also, single and two-way combined PAs using a differential flip-chip unit PA are used (Fig. 3.12(c) and (d)). The wirebonded PA chips are both 4-stage common-emitter designs which utilize TSVs to minimize L_{Eff} and guarantee high-frequency stability. The differential flip-chip PA also uses a 4-stage common emitter design with identical component values to the single-ended PAs but with a modified, symmetric layout for true differential mode operation as well as common-mode degeneration

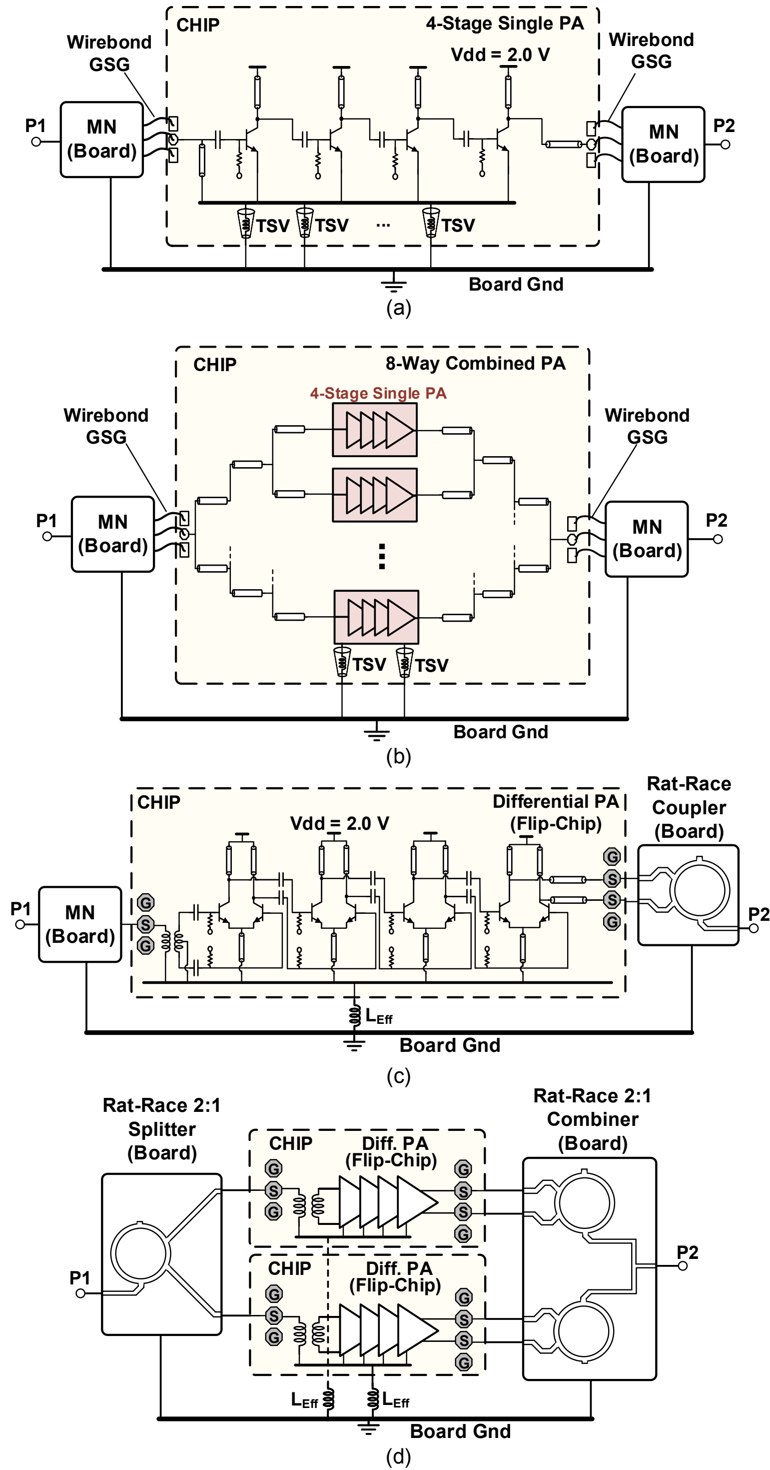


Figure 3.12: Schematics of assembled E-band power amplifiers. (a) Wirebond single-PA with thru-silicon vias, (b) wirebond 8-way combined PA with thru-silicon vias, (c) flip-chip differential PA, (d) flip-chip differential PAs with 2-way on-board combining.

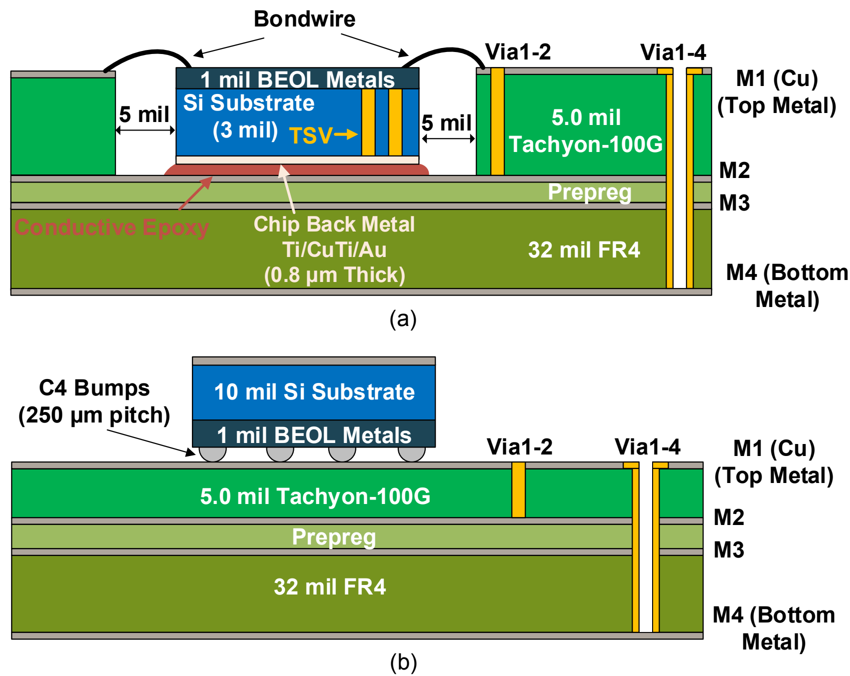


Figure 3.13: Diagram of board stackup used for assembled (a) wirebond and (b) flip-chip power amplifiers (drawing not to scale).

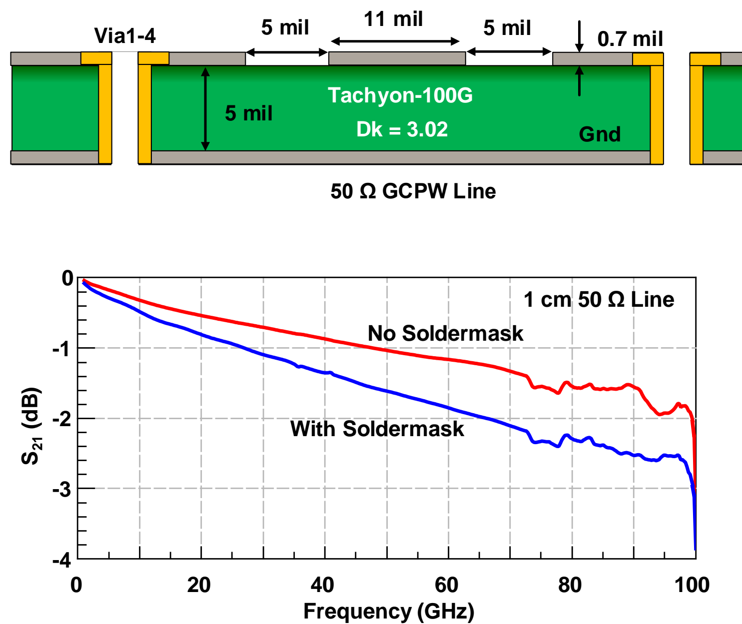


Figure 3.14: Measured line loss of a 1 cm 50 Ω GCPW line printed on a 5 mil Tachyon-100G substrate.

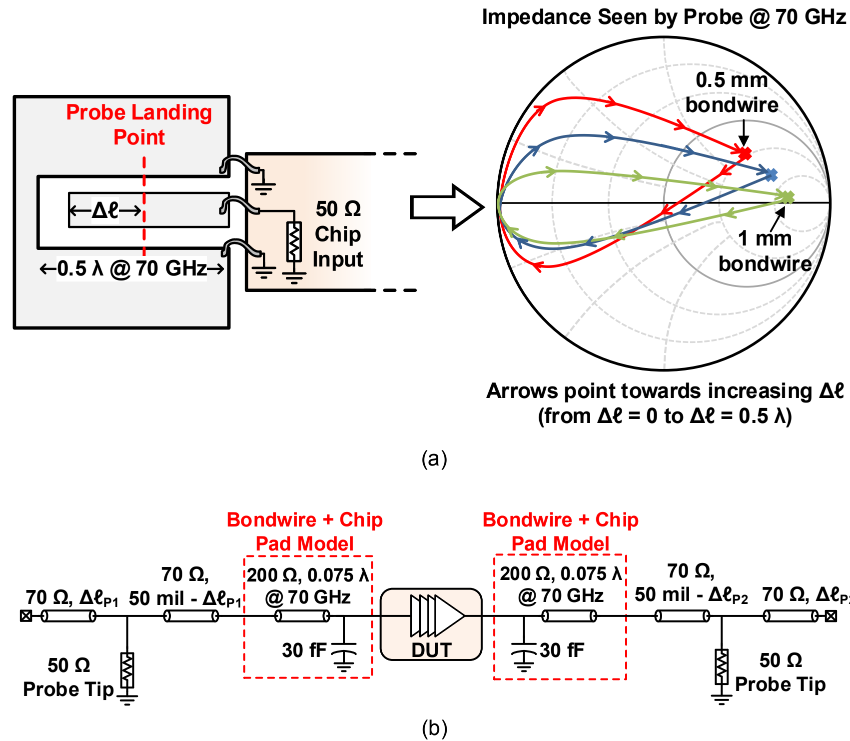


Figure 3.15: (a) Visualization of wirebond PA variable input matching network using probe landing point as tuning variable and (b) equivalent circuit diagram of chip input matching network.

inductors at the virtual ground nodes between differential transistors to kill common-mode gain. Note that the differential PAs cannot be tested using wafer probing due to the lack of availability of GSSG WR10 waveguide probes, and can only be tested after flip-chip assembly.

The PCB consists of a 5 mil Isola, Tachyon-100G substrate for low loss RF signal routing, attached to a 32 mil FR4 substrate for mechanical stability and to provide extra metal layers for dc routing (Fig. 3.13). Routing between the top 'M1' metal (RF signal) and the 'M2' metal (RF ground) is achieved using Via1-2 which is a filled, 8 mil diameter via. Routing between all other layers is achieved using Via1-4 which is an unfilled thru-board via of diameter 14 mil. Electroless nickel electroless palladium immersion gold (ENEPIG) finishing is used so that the board is compatible with both flip-chip and wirebond chip assemblies. For wirebond assembles, a cavity is laser-drilled in the Tachyon-100G substrate and the chips are placed into the cavity to reduce the total length of the GSG bondwires at chip input and outputs. The TSVs of the wirebonded chips are electrically connected to the M2 metal layer through a conductive epoxy (Epotek H20E) so that the TSVs may have the desired effect of reducing the effective inductance between

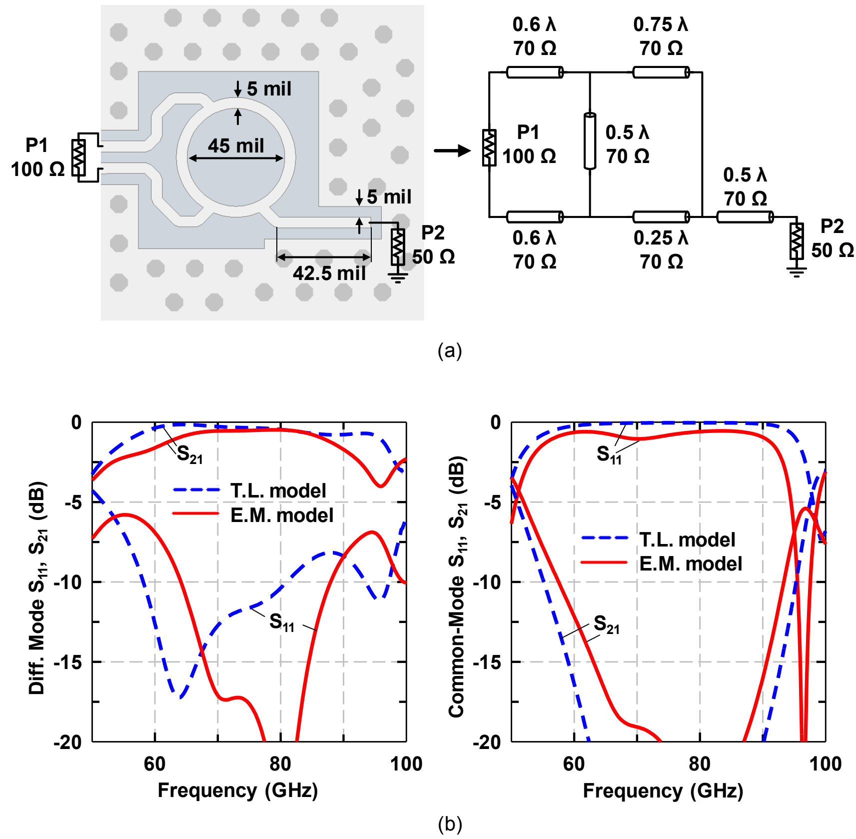


Figure 3.16: (a) Structure and equivalent schematic diagram of on-board rat-race coupler design. (b) Simulated S11 and S21 of rat-race coupler using differential 100 Ω and common-mode 25 Ω feed at input port.

chip and board.

The measured loss of a 50 Ω grounded coplanar waveguide (GCPW) printed on the Tachyon-100G boards at 70 GHz is less than < 1.5 dB/cm for lines without soldermask, and $\sim$2.1 dB/cm for lines with soldermask (Fig. 3.14). The measured line was printed using 0.7 mil thick copper with an ENEPIG finish.

Because the exact bondwire length and height was not known before the assembly of the wirebond PAs, it was necessary to design a variable matching network on the PCB to accommodate a range of potential bondwire inductances (Fig. 3.15). The matching network consists of an open λ/2 line at the input and output ports of the PA chip. The input match seen by the probe can be varied by changing the probe landing point along the line, which controls the length of the input transmission-line into the chip and the open transmission-line stub behind the probe. This is shown on the Smith chart in Fig. 3.15(a) and the schematic representation of the input and output matching network including a transmission-line based

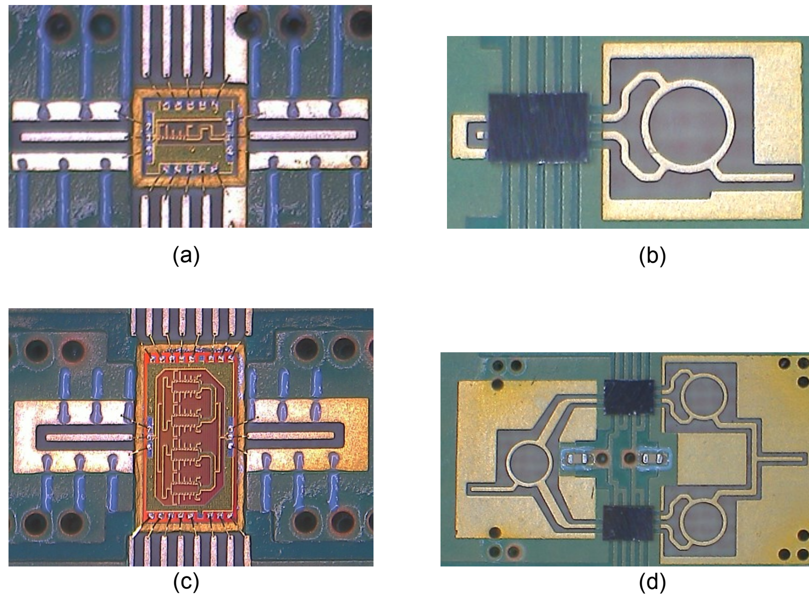


Figure 3.17: Microphotographs of assembled PA chips: (a) 4-stage S.E. wirebond PA, (b) 4-stage differential PA, (c) 8-way combined wirebond PA, and (d) 2-way combined differential PAs (on-board combining).

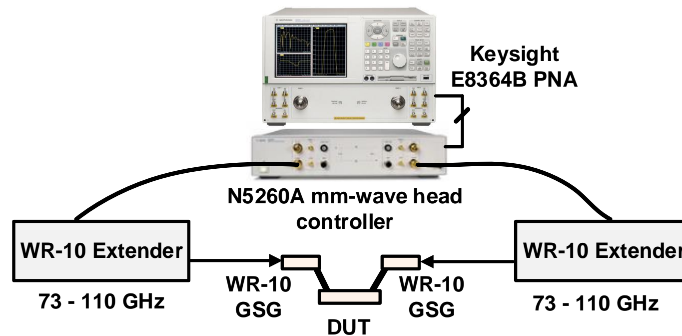
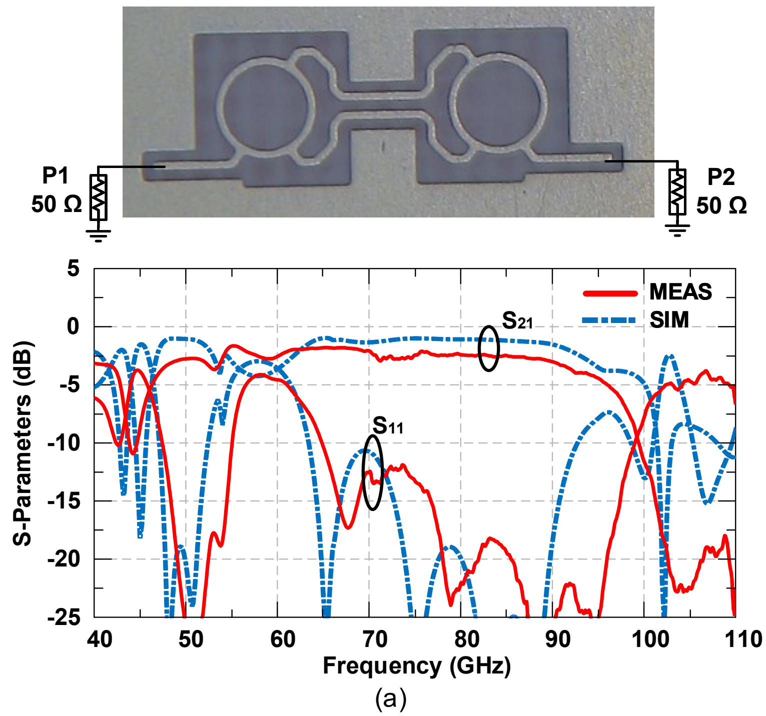


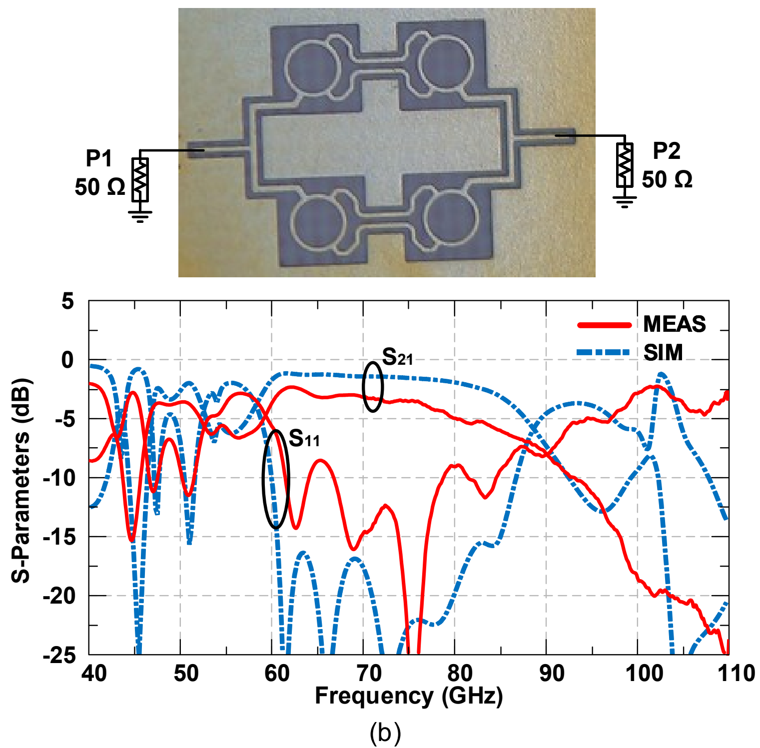
Figure 3.18: Small signal measurement setup for above 67 GHz measurements.

model of the GSG bondwires extracted from measurements is shown in Fig. 3.15(b).

The differential PAs utilize a single-ended input, differential output structure to avoid packaging related stability issues. In order to measure the output power of a single differential PA using a single-ended probe, a rat-race coupler (Fig. 3.16(a)) was designed using 70 Ω microstrip lines (5 mil width) on the M1 layer over an M2 ground layer. The rat-race is surrounded by Via1-2 on all sides to prevent signal from leaking to the parallel-plate waveguide between the M1 and M2 layers. Because bump impedances are typically small, the rat-race is not explicitly designed to tune out any series bump inductance between the



(a)



(b)

Figure 3.19: Measured S_{11} and S_{21} of back-to-back passive structures on Tachyon-100G substrate. (a) back-to-back rat-race coupler based combiner used at output of differential flip-chip PA. (b) back-to-back 2-way rat-race couplers used at output of 2-way combined differential flip-chip PA.

chip and the PCB. Fig. 3.16(b) shows the simulated common and differential mode coupler S_{11} and S_{21} for both the transmission-line model and the HFSS model of the coupler. In the differential mode, the S_{11} is < -10 dB and S_{21} is greater than -1 dB between 65 and 85 GHz. In the common-mode, since there is no explicit isolation port on the coupler, the S_{11} is not matched ($\sim$-2 dB). The common mode S_{21} is below -10 dB between 60 and 95 GHz.

For the two-way combined differential flip-chip PA variant, input signal splitting and output combining are achieved through passive on-PCB networks that are based on the same rat-race coupler of Fig. 3.16.

3.5 Measurements

3.5.1 Small Signal Measurements

Microphotographs of the assembled PAs are shown in Fig. 3.17. All measurements were conducted by landing probes directly on the metal traces of the boards. For the wirebond PAs, probes were landed at $\sim$10 mil from the end of the $\lambda/2$ line to produce a poor, yet wideband match for small signal measurements. Below 70 GHz, measurements were taken using a Keysight N5247A PNA-X, while above 70 GHz measurements were taken using a Keysight 8364B PNA connected to an N5260A mm-wave head controller with Virginia Diodes (VDI) WR-10 extenders (Fig. 3.18). All measured small signal results shown in this paper represent spliced data from the two separate setups.

The rat-race coupler of the single differential PA and the 2:1 combining rat-race couplers of the 2-way combined PA were fabricated in back-to-back configurations for loss measurements using single-ended probes (Fig. 3.19). The loss from the back-to-back 2:1 rat-race coupler is around 2.5 dB (1.25 dB per coupler) while the loss from the back-to-back 2:1 rat-race is around 3.5 dB (1.75 dB per coupler). Measurements and simulations show good agreement.

Measured S-parameters of all PA variants are presented in Fig. 3.20. De-embedding is performed up to the probe tips and the losses of the PCB transmission-lines are not removed in all measurements. For the wirebond PAs, S-parameters after assembly are compared against wafer-probed results with and without modeled GSG wirebonds. The assembled 4-stage PA achieves 17.5 dB of gain, a 7.5 dB drop

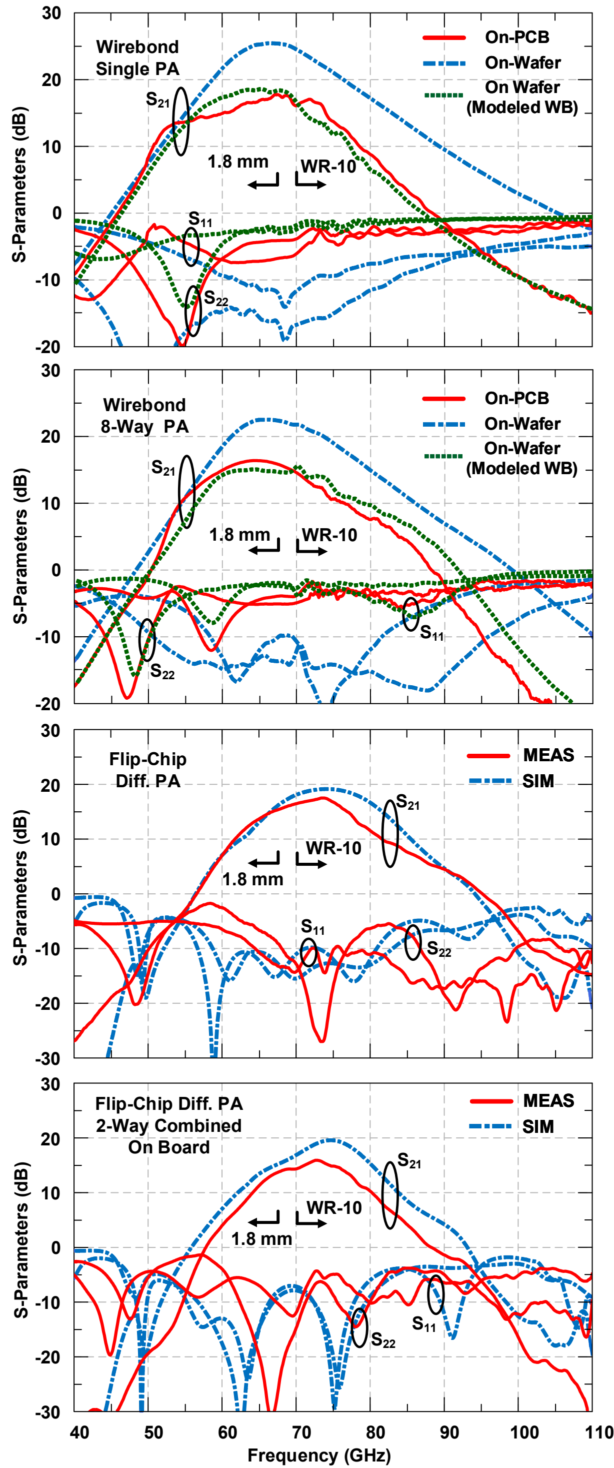


Figure 3.20: Measured S-parameters of assembled wirebond and flip-chip E-band PAs. Wirebond PAs are compared with probed-on-wafer measurements with and without modeled wirebonds. Flip-chip PAs are only compared with simulation due to their differential outputs which are incompatible with waveguide probing.

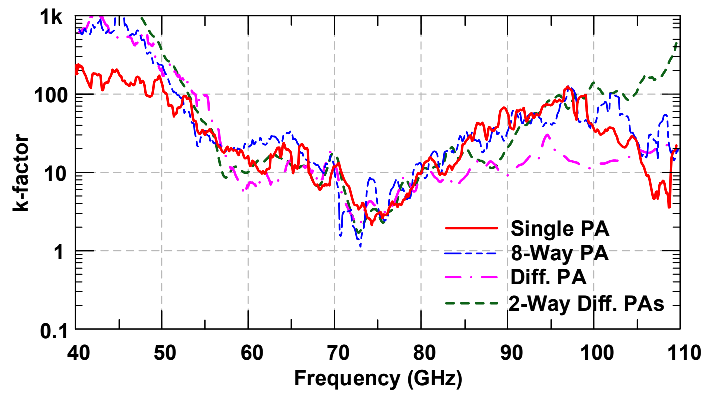


Figure 3.21: Measured k-factor versus frequency of all PA variants.

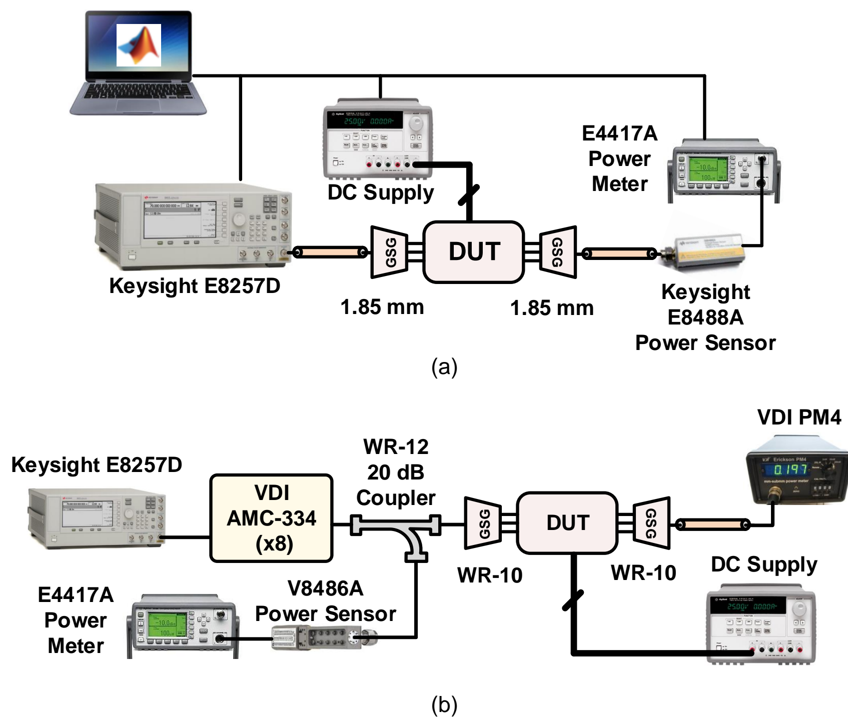


Figure 3.22: Large signal measurement setup for (a) below 70 GHz and (b) above 70 GHz measurements.

compared to wafer-probed measurements, and with a 3-dB bandwidth from 57 - 75 GHz. The assembled 8-way combined PA has a peak gain of 16.5 dB, a 6 dB drop compared to wafer-probed measurements, and with a 3-dB bandwidth from 58 - 71 GHz. Because the probe landing points are adjusted for widest bandwidth during small-signal measurements, the S_{11} and S_{22} of the wirebond PAs are around -3 dB, resulting in approximately 3 dB of return loss at the input and output nodes, which is predicted by the wafer-probed results with input and output bondwires modeled as in Fig. 3.15(b).

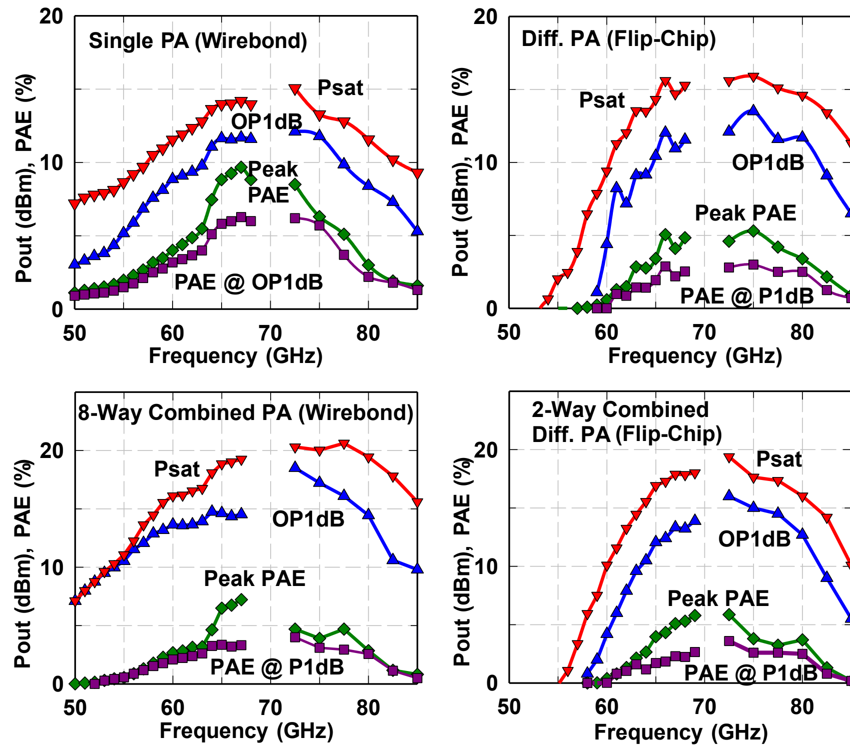


Figure 3.23: Measured large signal results of assembled amplifier variants versus frequency.

S-parameters of the assembled differential PAs are compared with simulated results and not with wafer-probed measurements due to the incompatibility of differential outputs with waveguide probes. The differential PA has a peak gain of 17.5 dB and a 3-dB bandwidth from 65 - 78 GHz. The two-way on board combined differential PAs show a peak gain of 16 dB with a 3-dB bandwidth from 66 - 78 GHz. Both differential PAs show better input and output matches than the wirebonded PAs despite not having any explicit matching networks for tuning out bump impedances, and is due to the considerably lower impedance of bumps when compared with bondwires at mm-wave frequencies. Measurements show that the k-factor remains above 1 for all variants across all measured frequencies (Fig. 3.21).

3.5.2 Large-Signal Measurements

Large-signal measurements were conducted using the measurement setup shown in Fig. 3.22(a) below 70 GHz and the setup shown in 3.22(b) above 70 GHz, and are shown in Fig. 3.23. Due to the limited output power of the E8257D signal generator near 70 GHz, the PAs could not be saturated in the range of

Table 3.1: Packaged E-Band Power Amplifier Comparison to Previously Published Works

Freq (GHz)	Tech.	Circuit	Gain (dB)	Psat (dBm)	OP1dB (dBm)	PAE (%)	Vdd (V)	Packaging	Ref.
64-75	**0.12 μm SiGe**	**4 Stage S.E. C.E.**	**17.5**	**15.0**	**12.1**	**9.6**	**2.0**	**Wirebond**	**This Work**
65-72.5	**0.12 μm SiGe**	**8-way S.E. C.E.**	**16.5**	**20.3**	**18.5**	**7.2**	**2.0**	**Wirebond**	**This Work**
65-78	**0.12 μm SiGe**	**Differential C.E.**	**17.5**	**15.9**	**13.5**	**5.2**	**2.0**	**Flip-Chip**	**This Work**
66-77	**0.12 μm SiGe**	**2-Way Combined on Board Diff. C.E.**	**16**	**19.4**	**16.0**	**5.8**	**2.0**	Flip-Chip	**This Work**
60-77	0.12 μm SiGe	4 Stage S.E. C.E.	25	16.1	13.2	16.5	2.0	NONE	[1,46]†
60-75	0.12 μm SiGe	8-way S.E. C.E.	22	24	21	12	2.0	NONE	[1,46]†
67-80	0.12 μm SiGe	4-Way Diff. C.E.	18.5	19.5	14.5	11	2.0	NONE	[1]
79-97	0.13 μm SiGe	Diff. C.E.	10.6	19.6	18	15.4	2.3	NONE	[50]
85-105	0.12 μm SiGe	4-Way Cascode	15	23.4	20.2	16.8	4	NONE	[28]
75-105	90 nm SiGe	Class E Cascode	17	22	-	19.1	4.4	NONE	[43]
68-91	90 nm SiGe	16-Way S.E. C.E.	19.3	27.3	22.3	12.4	1.8	NONE	[25]
51-67	55 nm BiCMOS	Single Stage C.E.	7	9	7	20	1.2	NONE	[51]
74-86	45 nm CMOS SOI	8-Way Cascode	10.1	21.1	-	5	2.0	NONE	[26]
70-95	45 nm CMOS SOI	Cascode	11	12.4	12.0	14.2	2.0	NONE	[45]
82-96	45 nm CMOS SOI	3-Stack FET	12.4	19.2	15	14	3.4	NONE	[44]
65-92	32 nm CMOS SOI	PMOS 3-Stack FET	11	18.7	16	24	3.6-4.5	NONE	[42]
60 - 75	40 nm CMOS	8-Way Xformer (Cascode)	19	21	19	13.6	1.5	NONE	[37]
59-67	40 nm CMOS	4-Way Xformer Push-Pull	22	16.4	13.9	23	1.8	NONE	[30, 31]
70-85	40 nm CMOS	4-Way Diff.	18.1	20.9	17.8	22.3	0.9	NONE	[38]†
70-85	40 nm CMOS	4-Way Diff.	11.7	16	-	18*	0.9	Wirebond	[55], [56]
70-85	40 nm CMOS	4-Way Diff.	14	17.6	-	-	0.9	Flip-Chip	[55], [56]
60	40 nm CMOS	4-Way Xformer	17.0	17.0	13.8	30	1	NONE	[35]
70-80	65 nm CMOS	4-Way Xformer	21	15.8	13	15.2	2	NONE	[36]
57-65	65 nm CMOS	8-Way Xformer	32.4	20.2	17.4	22.9	1.2	NONE	[34]
50-70	65 nm CMOS	32-Way	16.3	23.2	19.6	10	1.2	NONE	[27]

* Estimated from plotted data, † Unpackaged variant of a packaged work.

67 - 70 GHz. For the wirebond PAs, the landing locations of the RF probes were varied for measurements at different frequencies to produce the best possible input/output match for the given frequency.

The wirebond 4-stage single PA achieves a peak saturated output power (Psat) of 15 dBm at 72.5 GHz and a peak Power-added efficiency (PAE) of 9.6%, a drop of 1.1 dB and 6.5% respectively from

wafer-probed measurements [1]. Its 3-dB Psat bandwidth is 64 - 75 GHz. The wirebond 8-way combined PA achieves a Psat of 20.4 dBm at 77.5 GHz and peak PAE of 7.2% at 67 GHz, a drop of 3 - 3.5 dB and 5% respectively from on-wafer measurements. Its 3-dB Psat bandwidth is 65 - 81 GHz. Notably the 3-dB Psat bandwidths are offset from the 3-dB small-signal gain bandwidths for both wirebond PA variants. The large-signal performance drop between on-wafer and on-board measurements is much lower than in small-signal measurements due to the adjustments of probe landing location with frequency. The remaining performance losses are due to the still non-optimal power match at the chip output which is limited by the high bondwire impedances.

The flip-chip differential PA shows a measured peak saturated output power and peak PAE of 15.9 dBm and 5% respectively at 75 GHz with a 3-dB Psat bandwidth of 65 - 81 GHz. The two-way combined on-PCB flip-chip differential PA has a peak saturated output power and peak PAE of 19 dBm and 6.5% respectively at 75 GHz with a 3-dB Psat bandwidth of 66 - 77.5 GHz.

3.5.3 Comparison to Prior Works

Table I presents a comparison of this work with previously published E-band power amplifiers. To the best of the author's knowledge, the 8-way combined wirebond, and the 2-way combined flip-chip PAs presented in this work have the highest output power of any previously published packaged silicon power amplifier.

3.6 Conclusion

This paper presented an analysis of the effects of packaging on the stability of power amplifiers at mm-wave frequencies. The cause of instabilities was defined, and practical methods of mitigating instabilities were described. Four variants of an E-band common-emitter power amplifier previously reported in [1] were assembled onto low-cost PCBs using flip-chip and wirebond interfaces and measured using PCB probing. Results were compared with wafer-probed measurements and show that the wirebond amplifier performance degrades significantly after packaging. Overall flip-chip PA variants fared better than their wirebond counterparts in terms of small-signal gain and bandwidth drop after assembly. The

effective use of low loss, on-board reactive power combining networks was also demonstrated through the flip-chip PA variants. To the best of the author's knowledge, this work presented the highest saturated output powers measured from a fully packaged silicon PA at these frequencies to date.

Acknowledgment

Chapter 3, in full has been submitted for publication of the material as it may appear in *IEEE Trans. Microw. Theory Techn.*, E. Wagner and G. M. Rebeiz, "Packaging Effects on Stability in Millimeter-Wave Silicon Amplifiers". The dissertation author was the primary investigator and author of this paper. The author would also like to thank Analog Devices for technical discussion and project funding, and Integrand Software for supplying licenses for EMX electromagnetic modeling software.

Chapter 4

A Very Low Phase-Noise Transformer-Coupled Oscillator and PLL for 5G Communications

4.1 Introduction

Fifth-generation (5G) communications promise to meet consumer demands for multi-Gbps wireless speeds by utilizing silicon-based millimeter-wave (mm-wave) systems working at 28, 39, and above 60 GHz. One challenge facing such systems is the strict phase-noise requirements of the local oscillator (LO). The LO phase-noise adds directly to the received signal and results in degraded error-vector magnitude (EVM) and limited overall system performance [57]. To demonstrate the difficult specifications imposed upon the synthesizer, Fig. 4.1 presents the topology for a potential 5G transceiver which may be working at an RF of either 28 or 39 GHz with an IF of $4-6$ GHz. The synthesizer is based on a $10-12$ GHz voltage-controlled oscillator (VCO) which is frequency doubled or tripled to create a $20-24$ GHz or $30-36$ GHz LO signal, and allows a high image rejection using RF filtering before the PA and after the LNA. In order to guarantee minimum signal degradation, the contribution of LO phase-noise to EVM[1]

[1] In this chapter EVM is defined as the ratio of root-mean square (RMS) error signal to the RMS magnitude of the constellation symbols.

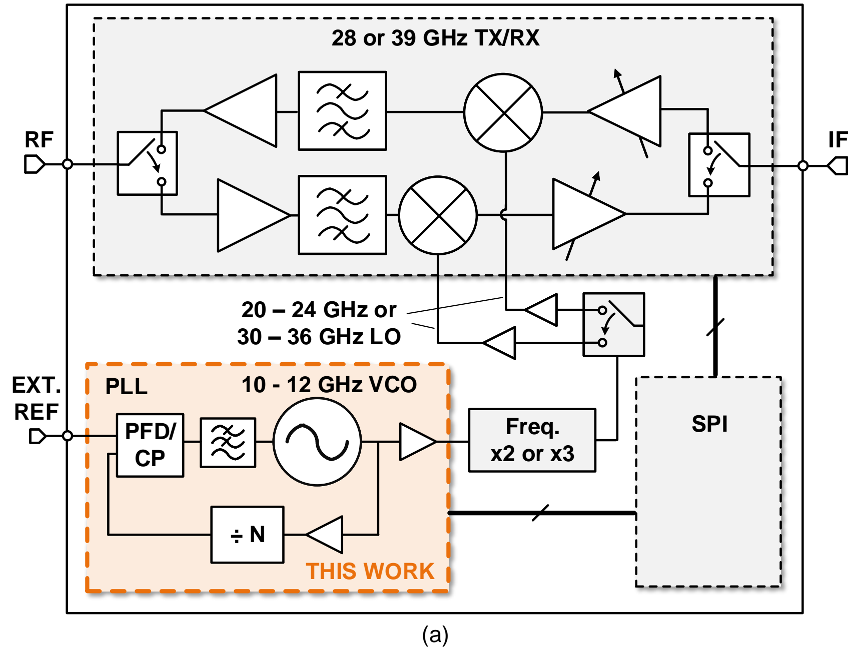
should be $< 2.5\%$ (-32 dB) (see Fig. 4.1(b) for a breakdown of system EVM contributors) for a 64-QAM waveform with 800 MHz channel bandwidth. If the LO phase-noise is assumed to degrade a signal's SNR in the same way as white noise (an approximation), then the EVM contribution from a mixer LO (or ADC clock) can be calculated as: EVM (%) $\approx$ 100%*(Double-Sideband Phase Error) [58]. The double-sideband (DSB) phase error has units of radians and is calculated as:

$$\text{DSB Phase Error} = \sqrt{2 \int L(f) df} \tag{4.1}$$

where L(f) is the phase-noise frequency response. The lower bound of integration is set by the communication waveform time-frame (generally 10 - 50 kHz), while the upper bound is set by the channel bandwidth. For a maximum EVM of 2.5%, the DSB phase error is 0.025 radians (1.43 degrees). DSB phase error can be converted to an RMS jitter value by dividing by $2\pi f_0$ which, for an LO at 24 GHz will lead to an RMS jitter of 166 fs.

The VCO specifications can be calculated from the desired RMS jitter. If it is assumed that the 12 GHz synthesizer has a -90 dBc/Hz in-loop noise, a 100 kHz loop filter bandwidth, and a noise floor of -150 dBc/Hz, then integrating the total phase-noise between 50 kHz and 800 MHz and accounting for the phase-noise degradation of 6 dB after frequency doubling, it is found that the VCO is required to have better than -120 dBc/Hz phase-noise at 1 MHz from the carrier to meet this requirement. For 39 GHz transceiver operation, the VCO performance will need to be even better to meet the same EVM requirement, and the PLL loop bandwidth may need to be decreased.

Recently, designers have leveraged cascaded [59], hybrid analog/digital [60], dual tuning [61], and other [62–64] synthesizer topologies in order to meet the strict noise requirements. This paper takes the opposite approach, by noting that state-of-the-art mm-wave communication systems are typically realized using phased arrays with 16 - 64 or more elements and with a power consumption of 85 - 300 mW on TX and 50 - 200 mW on RX per element [65–68], resulting in power consumption in the order of 10 - 20 W. Therefore, power consumption within the synthesizer is rarely a driver of the overall system efficiency, and simpler PLL designs centered around a single, high power, and very low noise VCO are of high value, and can save design time and complexity in practical systems. For a synthesizer which does not leverage



(a)

Component	EVM
EVM due to 31 dB SNR at RX path	3.0 %
EVM due to LO phase-noise jitter	2.5 %
EVM due to ADC quantization noise	1 %
EVM due to ADC clock jitter	<1 %
Total RX EVM	**4%**

(b)

Figure 4.1: (a) Schematic of a transceiver architecture for 5G systems which employs a 10 - 12 GHz synthesizer with a frequency multiplication of 2 or 3 to produce the LO for a 28 or 39 GHz RF path and 4 - 6 GHz IF, (b) breakdown of RX system noise contributions.

complexity, the optimum performance of the fundamental oscillator is critical, and must provide the lowest noise levels possible in the given technology to produce satisfactory performance.

This paper is an expanded version of [69], and presents the design and analysis of a $10-12$ GHz class-C transformer-coupled VCO, designed to achieve noise performance near the limits of its technology. The VCO achieves a measured phase-noise performance of -122 dBc/Hz at 1 MHz offset with a figure of merit[2] (FoM) of 183 dBc/Hz. The VCO is integrated into an integer-N PLL which achieves performance suitable for 5G communication systems.

[2]The figure of merit of a VCO is defined in this chapter as $FoM = -L(f_{off}) + 10log\left\{(\frac{f_0}{f_{off}})^2(\frac{1mW}{P_{DC}})\right\}$

4.2 Cross-Coupled VCO Analysis

4.2.1 Overview

The performance of cross-coupled VCOs has been extensively studied in the past, with publications often deeply focusing on singular aspects of the cross-coupled design. The purpose of this section is to expand upon several of the most important performance-enhancing techniques such as waveform shaping using 2nd & 3rd harmonic resonances, threshold voltage effects, and other effects which influence the VCO design presented in Section III.

4.2.2 Waveform Tuning Through Harmonic Resonant Loads

Among the most potent techniques for improving cross-coupled VCO performance is that of adding a common-mode 2nd harmonic resonance to the VCO tank. The existence of a common-mode 2nd harmonic resonance benefits VCO performance in three distinct ways: 1) the upconversion of device noise near dc is suppressed, 2) the oscillator's efficiency is improved by shaping current and voltage waveforms such that less dc power is consumed, and 3) waveform shaping also allows a larger magnitude fundamental oscillation without causing drain voltages to swing below 0. The dc noise suppression property of the common-mode 2nd harmonic resonance has been recognized since at least 1998 when [70] used Hajimiri and Lee's linear, time-variant oscillator noise model [71] to predict that waveforms with even symmetry should have a zero magnitude dc component of their impulse-sensitivity function (ISF) and therefore dc noise upconversion through the ISF should be suppressed. Designs successfully leveraging 2nd harmonic resonances to suppress flicker noise have been published as early as 2001 [72], and the technique has since been re-examined several times [73–75], and notably its relationship to the common-mode 2nd harmonic resonance by Shahmohammadi in [76, 77] and Murphy in [78].

Less well documented is the efficiency-enhancing properties of the common-mode 2nd harmonic resonance. For better understanding, it is necessary to inspect the time domain waveforms. Fig. 4.2 presents the calculated voltage and current waveforms of a voltage-biased cross-coupled oscillator in the presence of varying levels of 2nd and 3rd harmonics in the output voltage waveform. If the oscillator has no harmonics in its output voltage waveform then the voltage at the gate of the transistor will be a 180°

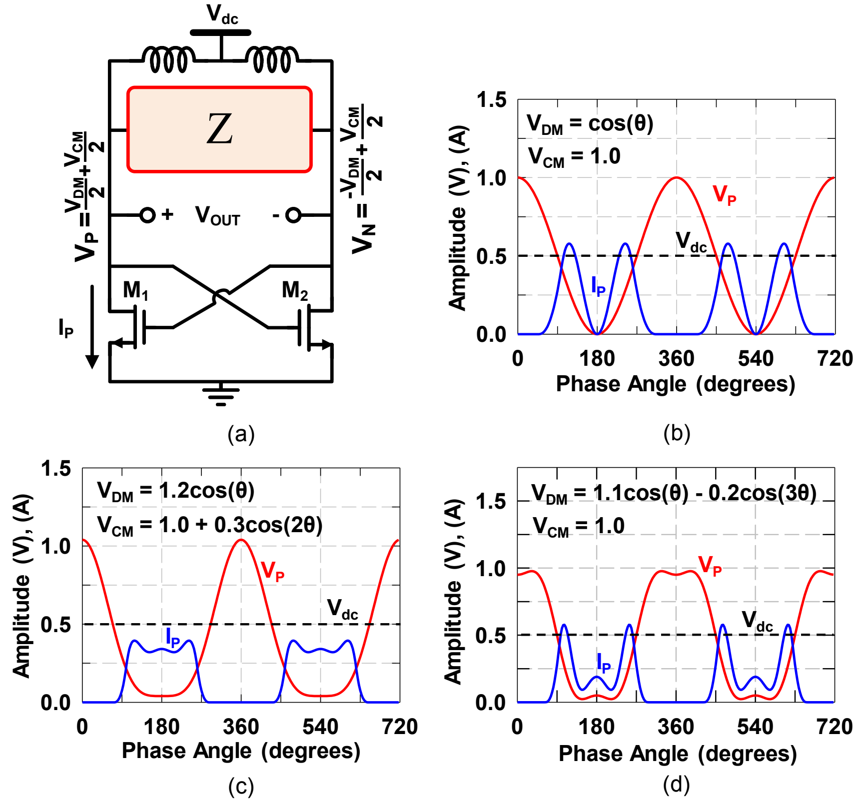


Figure 4.2: (a) schematic of voltage-biased cross-coupled VCO, and time-domain voltage and current waveforms at the drain of M1 for an output consisting of (b) no higher order harmonics, (c) a common-mode 2nd harmonic voltage with magnitude of 0.25 time the fundamental, and (d) a differential-mode 3rd harmonic voltage of 0.18 times the fundamental.

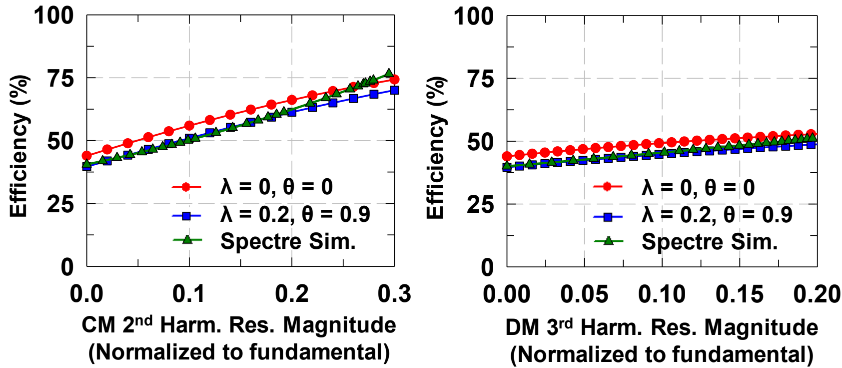


Figure 4.3: Calculated efficiency for a cross coupled oscillator using transistors with channel-length modulation factor λ, velocity saturation factor θ, and threshold voltage 0.17 V versus common-mode 2nd and differential-mode 3rd harmonic oscillation magnitude.

out-of-phase copy of the drain voltage and will result in the drain current displayed in Fig. 4.2(b). If a 2nd harmonic common-mode component is present in the output voltage, then the voltage and current

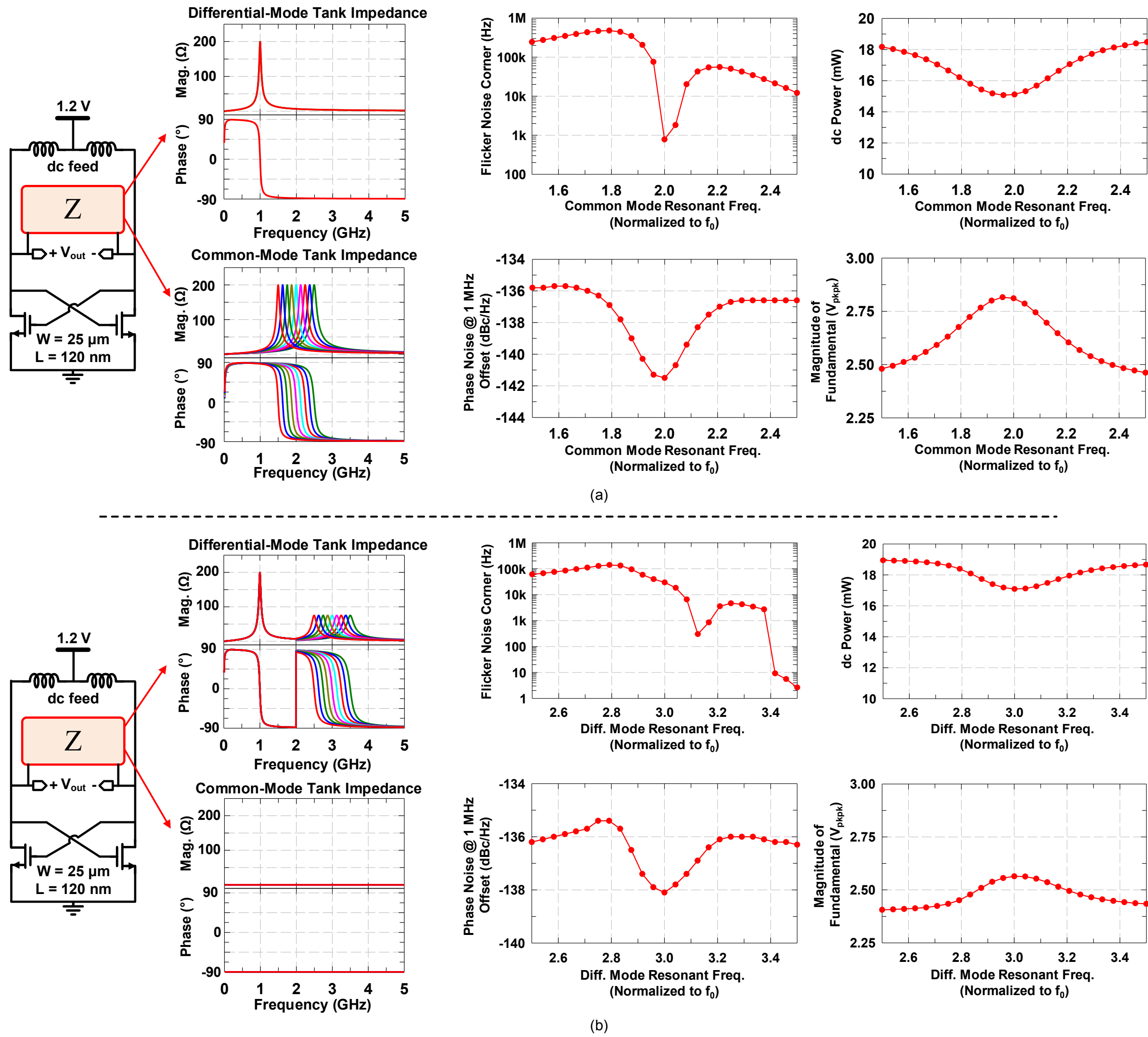


Figure 4.4: Simulated performance of voltage-biased cross-coupled VCOs with different harmonic loads. (a) Common-mode resonant load (Q = 20, $R_{parallel}$ = 200 Ω), (b) differential-mode resonant load (Q = 20, $R_{parallel}$ = 75 Ω) (simulated using spectre circuit simulation engine with GF8HP nfet models with parasitic shunt capacitances removed).

waveforms will be shaped similar to Fig. 4.2(c). It is noteworthy that due to the shaping effect of the 2nd harmonic the magnitude of the fundamental can be made larger than if the output purely sinusoidal without causing the drain voltage to drop below 0. The efficiency of this waveform is also enhanced beyond the sinusoidal case due to the increase in abruptness of the current and voltage transitions between high and low. Finally, If a 3rd harmonic differential-mode component is present in the output voltage, then the voltage and current waveforms will be shaped similar to Fig. 4.2(d). Like with the common-mode 2nd harmonic,

the addition of a differential-mode 3rd harmonic allows an increase in the fundamental magnitude and overall efficiency of the oscillator. Fig. 4.3 presents simulations of the efficiency enhancement due to common-mode and differential-mode harmonics. The calculated results are plotted for different values of active device channel-length modulation factor λ and velocity saturation factor θ and confirmed via simulations of Global Foundries' 8HP nfet models in the spectre circuit simulation engine.

Similarly to common-mode 2nd harmonic resonances, a differential mode resonance tuned to the 3rd harmonic may also improve a voltage-biased cross-coupled oscillator's efficiency and fundamental magnitude, although without providing the benefit of suppressing dc noise upconversion. The waveforms and theoretical efficiency enhancement of an oscillator with 3rd harmonic resonance are also presented in Fig. 4.2. The efficiency enhancement of a 3rd harmonic resonance is considerably smaller than that of the common-mode 2nd harmonic resonance, and a rigorous mathematical study of this resonance was conducted in [79]. Extra care must be taken when applying differential mode resonances to an oscillator, or else, the oscillator may begin to oscillate at the 3rd harmonic rather than the fundamental.

To demonstrate the performance gains that can be expected from the use of harmonically tuned loads, Fig. 4.4 presents the simulated performance of voltage-biased cross-coupled VCOs with high-order common-mode and differential-mode resonances as those resonances are swept in frequency. When the common-mode resonance is swept (Fig.4.4(a)), the dc power consumption, flicker noise corner, and phase-noise at 1 MHz offset frequency experience minimums and the magnitude of the fundamental oscillation experiences a maximum for the case when the resonance is at twice the fundamental frequency. With exception to the flicker noise corner, the same trends are seen when a differential-mode high-order resonance is swept (Fig.4.4(b)) and approaches three times the fundamental frequency, albeit with a notably lower performance enhancement. Though these results are simulated for a VCO with a fundamental frequency of 1 GHz, they can be generalized to oscillators working at any fundamental frequency.

Finally, it is worth noting that for common-mode resonances, adding an explicit common-mode resonant network to the load of a cross-coupled oscillator is not the only way to achieve the benefits of the common-mode oscillation. It has been noted in [76] and [78] that a common-mode resonant network applied to the source nodes of cross-coupled transistors will produce the same effect as one applied to the drain. The reason for this is that in a current biased cross-coupled design, when the reference is moved to

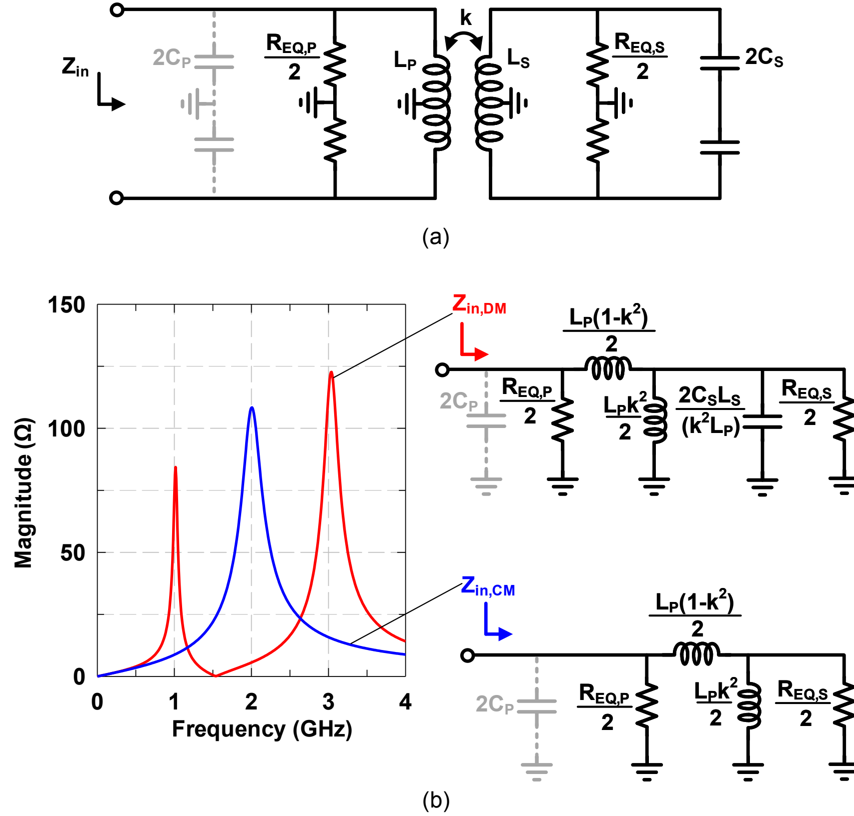


Figure 4.5: Simplified schematic model of transformer tank with 1st-order differential mode resonance of secondary side and 3rd and 2nd-order differential and common-mode resonances on primary side.

the transistor sources the equivalent circuit has the resonant network at the source appearing in series with the resonant network at device drains. Designs using resonant networks simultaneously at both the device source and drain have been proposed [80].

4.2.3 Harmonic Tuning with Transformer-Coupled Loads

While it is possible to design high-order common and differential-mode resonances into a VCO by including multiple independent resonant loads at either the drain or source nodes, this technique is expensive in terms of area since space must be allocated for multiple inductors, and they must be separated enough to avoid unwanted coupling. As noted in [76], a transformer-coupled resonant load can be designed such that its own parasitic inductance and capacitances create both common-mode 2nd and differential-mode 3rd harmonic resonances without the need for additional inductors.

Illustrated in Fig. 4.5(a), a transformer with an explicit resonant load may be formed by adding capacitance C_s in parallel with the secondary of a transformer. Assuming no parasitic capacitance is present on either side of the transformer and that the coupling k between primary and secondary is high, this circuit will experience a single parallel resonance at $\omega_0 \approx 1/\sqrt{L_s C_s}$ with Q-factor set only by the Q of the secondary-side components. If, however, parasitic shunt capacitance C_p is present on the primary side, the circuit can be broken down into the common and differential-mode half-circuits shown in Fig. 4.5(b), and both the primary and secondary side of the transformer will experience a differential-mode resonance with its respective parallel capacitance. The frequency of the differential-mode parallel resonances are derived in [81] as

$$\omega_{1,2}^2 = \frac{1 + \left(\frac{L_S C_S}{L_P C_P}\right) \pm \sqrt{1 + \left(\frac{L_S C_S}{L_P C_P}\right)^2 + \left(\frac{L_S C_S}{L_P C_P}\right)(4k^2 - 2)}}{2 L_S C_S (1 - k^2)} \tag{4.2}$$

where ω_1 can be approximated as

$$\omega_1^2 \approx \frac{1}{(L_P C_P + L_S C_S)} \tag{4.3}$$

when the value of k is close to 1. Because the parasitic capacitance on the primary side is grounded, the common-mode will also see a parallel resonance which will occur at

$$f_{0,CM} = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{4.4}$$

which is, notably, not affected by the coupling k or ratio of primary to secondary side inductances.

The phase-noise performance of a cross-coupled VCO using a transformer-coupled resonant tank is shown in Fig. 4.6 for swept values of primary side capacitance C_P and transformer coupling k. When C_P is swept, the frequency of the common-mode resonance is affected, and phase-noise shows a deep minimum at the value of C_P where the common-mode resonates at twice the fundamental. When the transformer coupling k is swept, the common-mode resonance remains unchanged while the higher order differential mode resonance moves in frequency. Here the trends are less distinct because the value of k controls the effective parallel resistance of the tank, the higher-order differential-mode resonance frequency, and the common-mode resonance frequency. In Fig. 4.6(b), C_P is chosen to set the common-mode resonance

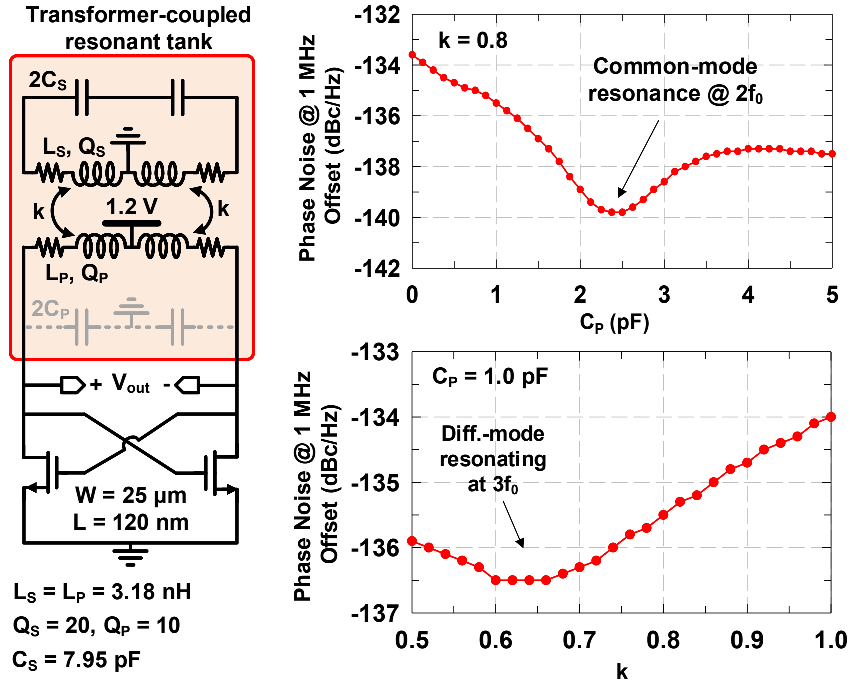


Figure 4.6: Phase-noise performance of cross-coupled VCO with transformer-coupled tank versus primary side parasitic capacitance C_p and coupling k. Simulated using Global-Foundries' 8HP nfet models with parasitic capacitances removed so that C_p may be controlled.

far from $2f_0$ and a dip is observed in the simulated phase-noise for the value of k that maximizes the differential-mode 3rd harmonic oscillation magnitude.

4.2.4 Additional Benefits of Transformer-Coupled Tank

According to Leeson's heuristic model, the phase-noise of an oscillator in the 20 dB per decade region is given by

$$L(\Delta\omega) = \frac{2FkT}{P_s} \cdot \left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \tag{4.5}$$

where F represents an excess noise supplied by the active devices, k and T are the Boltzmann constant and temperature respectively, Q is the Q-factor of the resonant load, and P_s is the power dissipated in the load [82]. While most of these parameters are fixed by the technology and thus outside of the designer's control, the power in the load can be manipulated by careful tuning of the tank inductance and capacitance. For lowest noise, ideally a small inductance and large capacitance should be used in the tank so that a smaller effective parallel resistance will be seen by the transistors and hence more current will be used for

an equivalent voltage swing.

This technique has two practical limits: the first being that as the equivalent parallel resistance of the tank falls, so too does the startup gain of the oscillator, requiring that larger devices be used. This leads to a trade-off as device parasitic capacitances will grow with device size limiting the tuning range of the oscillator. The second limit occurs as the physical size of the tank capacitances becomes large enough that the parasitic inductance of the capacitor interconnects begins to overtake that of the explicit tank inductor. The parasitic inductance of the interconnects forces a trade-off in oscillation frequency, and also in Q-factor, as the interconnects can rarely achieve the same Q as an explicit tank inductor.

While these limitations have been studied in the past [83], it is rarely acknowledged how the use of a transformer-coupled load can alleviate these limits in a parallel LC tank. In a transformer-coupled resonant circuit, such as the one depicted in Fig. 4.5, if the primary and secondary side have inductances L_p and L_s, respectively, and the inductance of the secondary resonates with the capacitance C_s at frequency ω_0 with Q-factor Q_s then the effective parallel resistance seen looking into the primary side is

$$R_{parallel} = Q_s \omega_0 L_p k^2 \tag{4.6}$$

This equation shows that the intrinsic resonator parallel resistance on the secondary side will be attenuated by both the ratio of the primary inductance to the secondary and the square of the coupling factor, k, which rarely has values greater than $\sim$0.8 in silicon technologies. The consequence is that a larger value of the secondary inductance L_s can be utilized for a given $R_{parallel}$ and resonant frequency, partially alleviating the physical limits of the LC-tank layout. For example: for a desired $R_{parallel}$ of 100 Ω and Q-factor of 20 at 10 GHz, the required values of L and C are 79.5 pH and 3.18 pF respectively for a standard LC-tank. Using a transformer-coupled resonator with a 1:1 ratio of primary to secondary side inductance and k = 0.75, the required value of L_p and L_s becomes 141 pH, and C_s becomes 1.79 pF leading to comparable performance without degrading the resonator Q-factor.

More interestingly, when shunt capacitance to ground is present on the transformer primary, the resonator Q-factor as a whole deviates from that of the secondary-side, and may receive a boost depending on individual component values. The effective Q-factor of the transformer-coupled resonator

was recognized first in [81] and derived as

$$Q_{Eff} = \frac{\left(1 + X^2 + 2kX\right)}{\left(\frac{X^2}{Q_p} + \frac{1}{Q_s}\right)} \tag{4.7}$$

where $X = \frac{L_p C_p}{L_s C_s}$ (the inverse of that derived in [81] due to the reversal of the primary and secondary sides in this work) and Q_s and Q_p are the Q-factors of the differential-mode secondary and primary side resonators, respectively. For a 1:1 transformer with realistic coupling of k = 0.75, the value of X for which the primary resonates at three times the fundamental frequency would be approximately 0.33, assuming both sides of the transformer have Q of 20, the effective Q-factor is then boosted by almost 50%. In practice, it is difficult to design a transformer with both high coupling and equal Q-factor on both primary and secondary due to the requirement of using lower metals with higher resistivity for one side of the transformer. For this reason, Q-factor in a practical design is rarely boosted by more than a few points in a transformer-coupled resonator.

4.3 Circuit Implementation

4.3.1 Technology

The VCO and PLL were fabricated in Global-Foundries' 0.12 μm SiGe BiCMOS 'GF8HP' process. The stackup used is shown in Fig. 4.7 and consists of seven metal layers including three thick top metal layers suitable for passive design and four thinner bottom metal layers for low-frequency or digital routing. The technology also offers high-density MIM and dual-MIM capacitors, and a deep-trench isolation layer to isolate passive and active devices from losses due to currents induced in the substrate. Table 4.1 lists the active devices which are available in GF8HP alongside their f_{max} and recommended maximum supply voltages.

4.3.2 VCO

The VCO is presented in Fig. 4.8 and utilizes a transformer-coupled resonant tank with thin-oxide PMOS active devices. The PMOS devices were chosen over their NMOS and HBT counterparts due to their

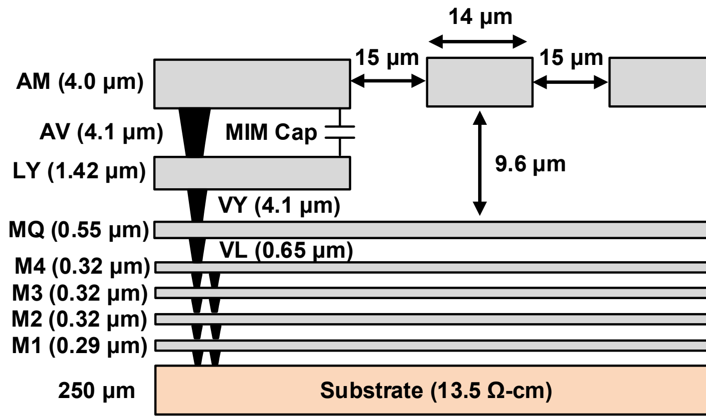


Figure 4.7: Global Foundries 8HP 0.12 μm SiGe BiCMOS process stackup.

Table 4.1: List of Devices Available in GF8HP

Device	f_{max} (GHz)	Vdd (V)
High f_t npn	220	1.8 (BVCEO)
High breakdown npn	60	3.5 (BVCEO)
NFET (thin oxide)	130	1.2
NFET (thick-oxide)	95	2.5
PFET (thin oxide)	50	1.5
PFET (thick-oxide)	30	2.5

superior noise performance. Ideally thick-oxide PMOS devices could be used to enhance the maximum tolerable voltage swing at the drains, however, the greater parasitic shunt capacitance of thick-oxide devices would have limited the oscillator tuning range and the enhanced voltage swing would have necessitated the use of lower Q-factor thick-oxide switches in the capacitor-bank, further limiting the performance.

The oscillator is biased in class-C with the gate nodes decoupled from the drains by large (500 fF) capacitors and a dc bias supplied through 400 Ω resistors. The gate resistors are optimized so that both the noise contributed and the loading at the FET gates is minimum. The dc bias current is set using a PMOS device from the supply which is biased in triode so that it acts as a resistor, rather than a current source, and its gate bias is controlled digitally so that its effective resistance value can be changed. The voltage drop across the current bias transistor also serves to protect the active devices from breakdown due to the 2.0 V supply.

The transformer-coupled tank is chosen to have a 1:1 windings ratio to allow a small tank effective parallel resistance while still benefiting from the Q-factor enhancing properties of the transformer resonator.

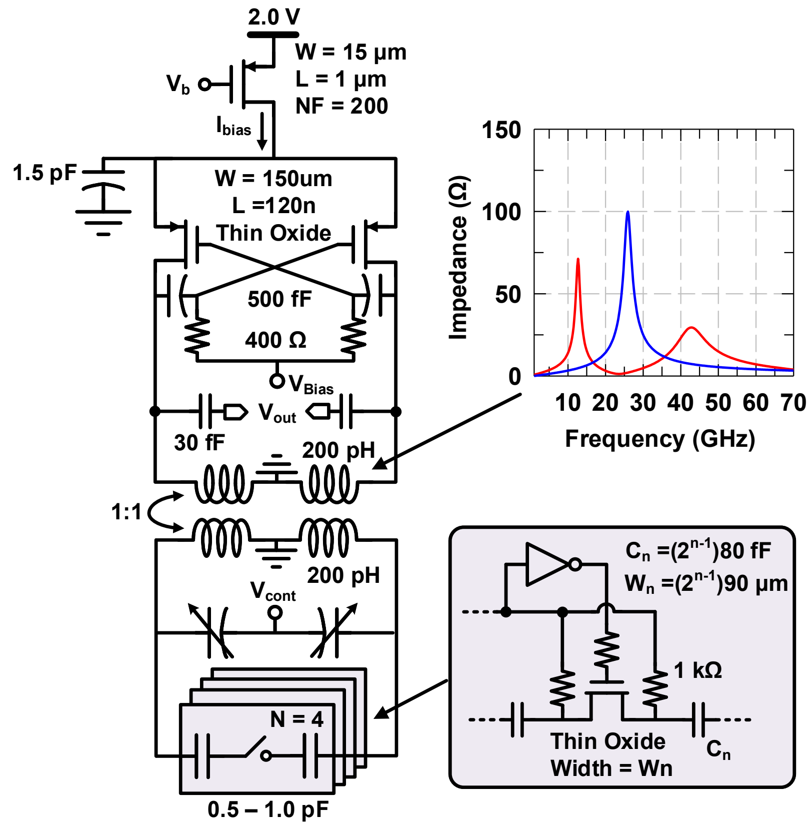


Figure 4.8: Schematic of 10 - 12 GHz PMOS voltage controlled oscillator.

The transformer is laid out using 64 μm wide, single-turn octagonal windings with 260 μm diameter (Fig. 4.9(a)). The inductor width is chosen so that the the primary side will have the proper parasitic shunt capacitance C_p which resonates with the primary to create the common-mode 2nd harmonic and differential-mode 3rd harmonic resonances. To ensure a high Q-factor of the fundamental resonance, the transformer secondary winding is implemented on the top metals (AM, LY and MQ), while the primary winding, which resonates at harmonic frequencies where Q-factor is less critical to performance, is implemented on the thinner bottom metals (M2, M3, and M4). This also serves to increase the coupling of the transformer, as the vertical distance between the technology's M4 and MQ metal is less than that between each of the top metals. The effective inductance of the primary and secondary is 200 pH and the Q-factor of the secondary peaks above 20 due to the extremely wide transformer coils (Fig. 4.9(b)).

The transformer secondary is connected to a four bit binary weighted capacitor-bank with an 80 fF interdigited MOM unit capacitance. The unit capacitor was implemented using the four bottom

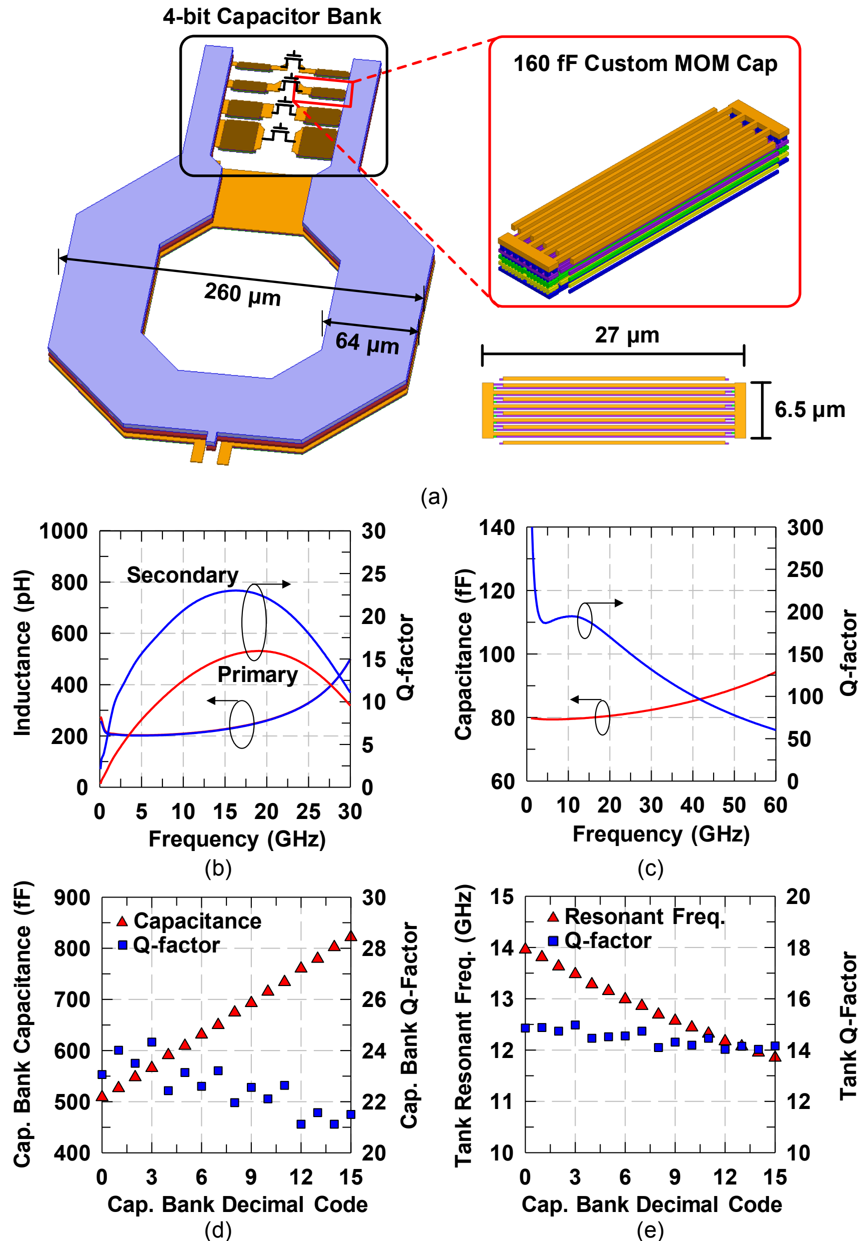


Figure 4.9: Performance of VCO resonant tank. (a) EM model of resonant tank, (b) simulated inductance and Q-factor of transformer primary and secondary excluding parasitic inductance of interconnects between transformer and capacitor-bank, (c) simulated capacitance and Q-factor of unit capacitor-bank 80 fF unit capacitor, (d) simulated capacitance and Q-factor versus frequency of full capacitor-bank, (e) simulated Q-factor and resonant frequency of complete VCO tank.

metal layers and has a Q-factor of nearly 200 at 10 GHz (capacitor-bank switch resistance not included) with capacitance density of 0.9 fF/μm^2 (Fig. 4.9(c)). Although the technology's process design kit (PDK) offers higher density dual-MIM (1.82 fF/μm^2) capacitors, they were not used due to their low Q-factor at

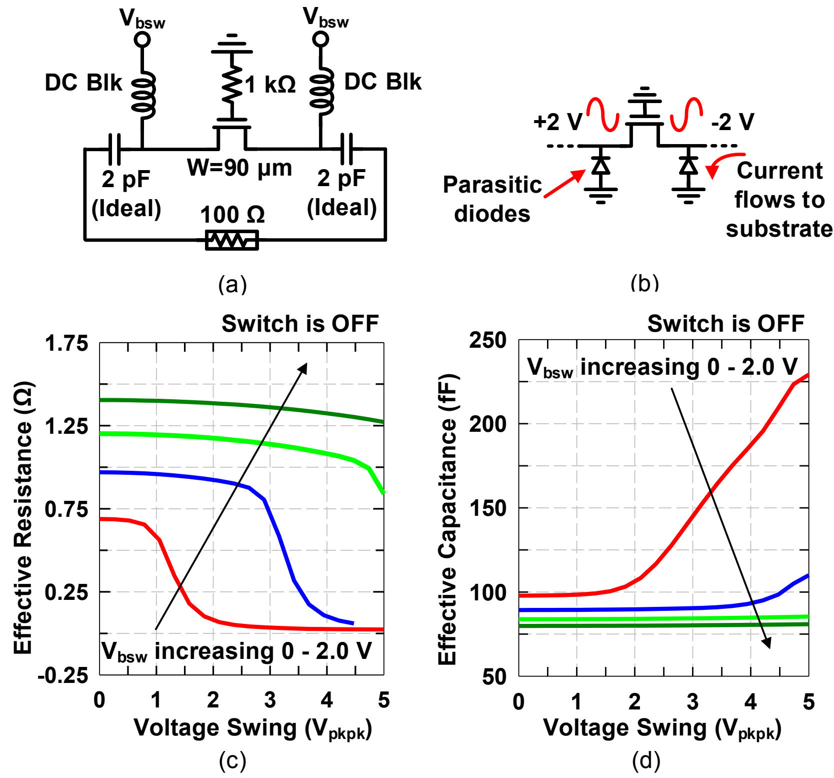


Figure 4.10: Simulated effective switch resistance and capacitance in the presence of large signal swings. (a) Simulation schematic, (b) switch performance degradation due to FET parasitic diodes (c) effective switch resistance vs. peak-to-peak voltage swing, (d) effective capacitance vs. peak-to-peak voltage swing.

10 - 12 GHz which is the result of the high series resistance of the vias between the AM and MIM top plate metal layers. The complete capacitor-bank is implemented using thin-oxide nfets as switches and can achieve capacitance values between 500 and 850 fF with a Q-factor between 24 and 21 (Fig. 4.9(d)). The capacitor-bank Q-factor is limited by the switch's ON resistance ($\sim$5 Ω per 100 μm switch) which trades with parasitic shunt capacitance when the switches are made wider. The switches are therefore designed to be as wide as possible without adding too much shunt parasitic capacitance which limits the capacitor-bank's tuning range. The complete tank including transformer and capacitor-bank resonates at 12 - 14 GHz with a Q-factor between 14 and 15 depending on the capacitor-bank's state (Fig. 4.9(e)). When the active devices are added, the resonant frequency is lowered to 10 - 12 GHz.

Due to the large (up to 4 V) peak-to-peak voltage swings seen by the capacitor-bank switches, switch biasing during the off-state is critical. When not properly biased, the parasitic diodes on the switch drain/source nodes can become forward biased near the negative peak of the voltage swing across the

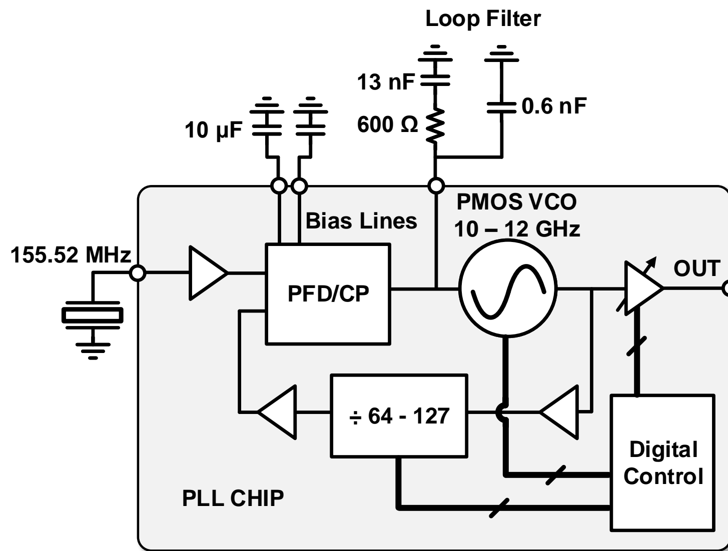


Figure 4.11: Schematic of the 10 - 12 GHz Integer-N PLL with off-chip loop filter and LDO (not shown).

switch, leading to a reduced effective off resistance and tank Q (Fig. 4.10). To prevent the switch diodes from becoming forward biased, a bias voltage of 1.2 V is applied to the source and drain nodes of the capacitor-bank switches when they are off.

4.3.3 PLL

The transformer-coupled VCO was integrated into the integer-N, type-II PLL shown in Fig. 4.11. The PLL's reference is supplied from an Abracon ABNM series 155.52 MHz crystal oscillator and the loop filter is realized using off-chip SMD components. The VCO is coupled to a variable gain amplifier (VGA) through small 30 fF series capacitors. The VGA is designed to deliver 0 − -15 dBm into a 50 Ω load.

The PLL's charge pump design (shown in Fig. 4.12) utilizes an error amplifier to reduce current sinking/sourcing mismatch, as well as bipolar devices in the current biasing network to minimize flicker noise and maximize output impedance of the bottom current biasing devices. To ensure that the PLL in-loop noise is as low as possible, further decoupling of the biasing lines is done using off-chip 10 μF capacitors. Due to the high division ratio of this PLL, passband phase-noise is dominated by the charge-pump and reference oscillator.

The PLL divider (Fig. 4.13) is a bipolar realization of the modular, synchronous divide-by-N

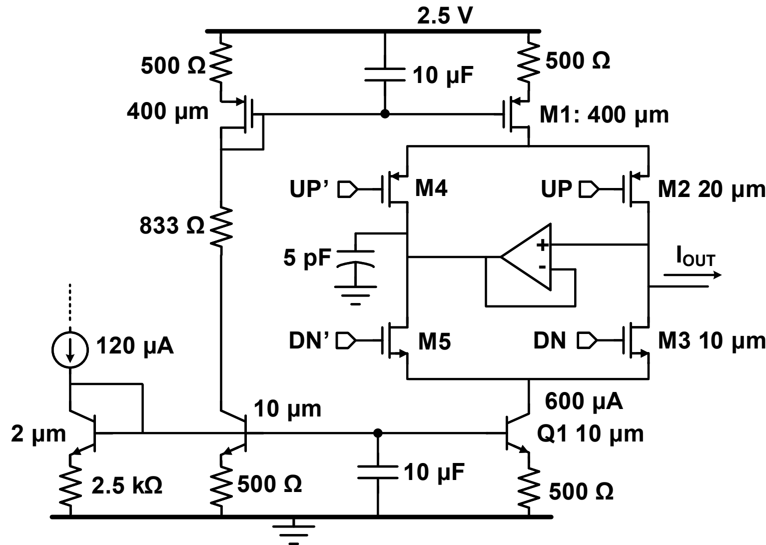


Figure 4.12: Schematic of charge pump used in the integer-N PLL.

scheme introduced in [84]. Six divide-by-2/3 stages are cascaded to produce a total integer division between 64 and 127 which can be set digitally, using SPI control. Aside from the biasing transistors, all npns in the design use the minimum emitter length allowed by the technology (0.62 μm) in order to reduce parasitic capacitance. Current usage is scaled lower in later divider stages to save power, with the first two stages consuming a 6 mW each, and all later stages consuming 3 mW. Additionally, the bias current of all divider stages can be digitally controlled, resulting in the range of dc power reported in Table 4.2. A high-speed re-timing flip-flop is included at the output of the divider’s last stage to reduce the dividerâĂŹs noise contribution.

In a 5G communication system working at 28 or 39 GHz, the PLL output would ideally be doubled or tripled in frequency before being used as an LO. However, if the LO signal is expected to be routed to multiple transceiver chips on a large phased array board, then it is more sensible to include frequency multiplication on the individual transceivers to avoid the considerable routing losses associated with 28 or 39 GHz transmission lines on the printed circuit boards. For this reason, no frequency multiplication is integrated onto the PLL chip.

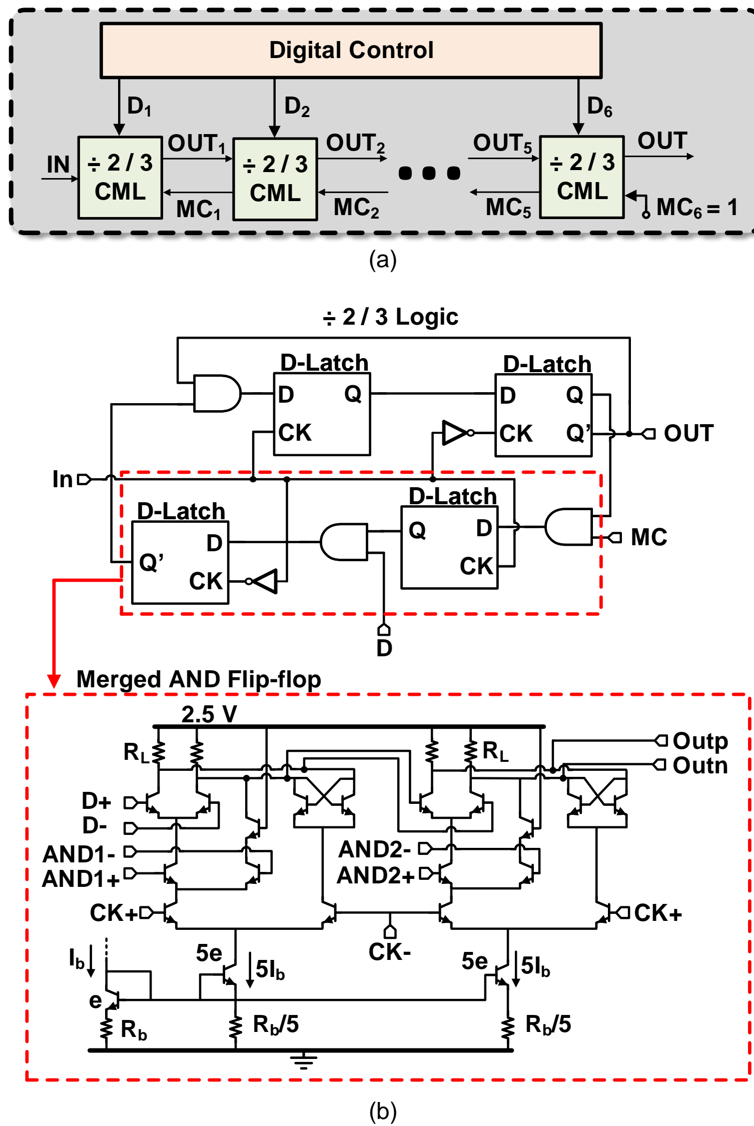


Figure 4.13: Schematic integer-N divider used in PLL. (a) Full block diagram of divider, (b) block diagram of single ÷2 or 3 stage with schematic of merged AND flip-flop cell.

4.4 Measurements

A microphotograph of the PLL chip is shown in Fig. 4.14. The chip's total area including flip-chip bumps is 1.115 x 1.105 mm^2 with an active area of 0.8 x 0.765 mm^2. The PLL chip was assembled onto a test board containing a 100 kHz loop filter, external filtering capacitors for the charge-pump, reference crystal oscillator, and two commercial ultra low-noise low-dropout regulators[3] (LDO) to provide adjustable,

[3]Commercial LDO used for testing was the ADM7151 from Analog Devices. Commercial reference oscillator was ABNM2-155.51MHz-C from Abracon.

Table 4.2: Power Consumption Breakdown in PLL

Block	Vdd (V)	P_{DC} (mW)
VCO	2.0 - 2.5	25 - 80
Output Buffer (VGA)	2.5	30
Divider	2.5	40
PFD + Charge Pump	2.5	8
Total:	-	**103 - 158**

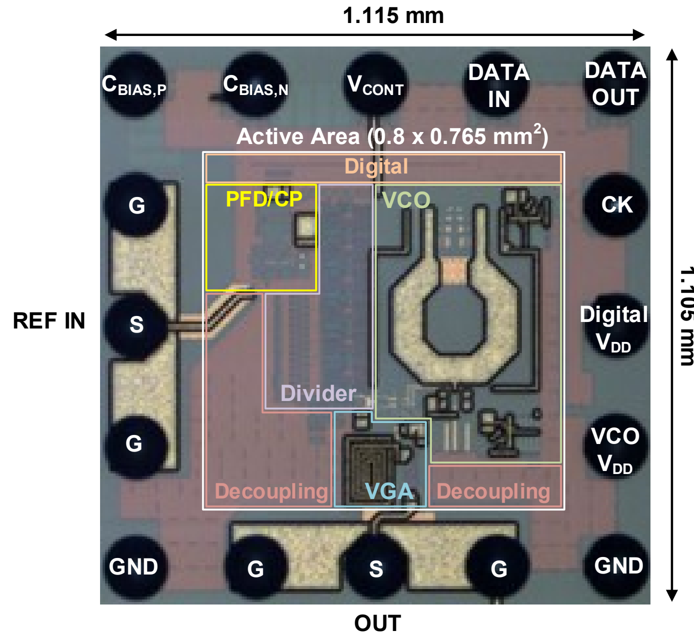


Figure 4.14: Chip microphotograph of PLL chip in 1.115 x 1.105 mm^2 including pads.

low noise dc supplies to the PLL power planes. Measurements of the VCO alone were made using a separate test chip on a similar board excluding reference crystal and loop filter and containing an extra LDO for setting the VCO tuning voltage.

The measurement setup is shown in Fig. 4.15. The signal from the PLL test board is amplified before being split by a Wilkinson divider so that it may be simultaneously analyzed by a Keysight UXA spectrum analyzer and a Keysight E5052B signal source analyzer. To accommodate the 7 GHz maximum frequency of the E5052B, the PLL signal is translated to an IF frequency using a wideband mixer and fed to the signal source analyzer.

Fig. 4.16 presents the measured results of the standalone PMOS VCO. The VCO's tuning range is from 9.94 – 12.4 GHz. The minimum measured phase-noise is -122 dBc/Hz in the minimum frequency

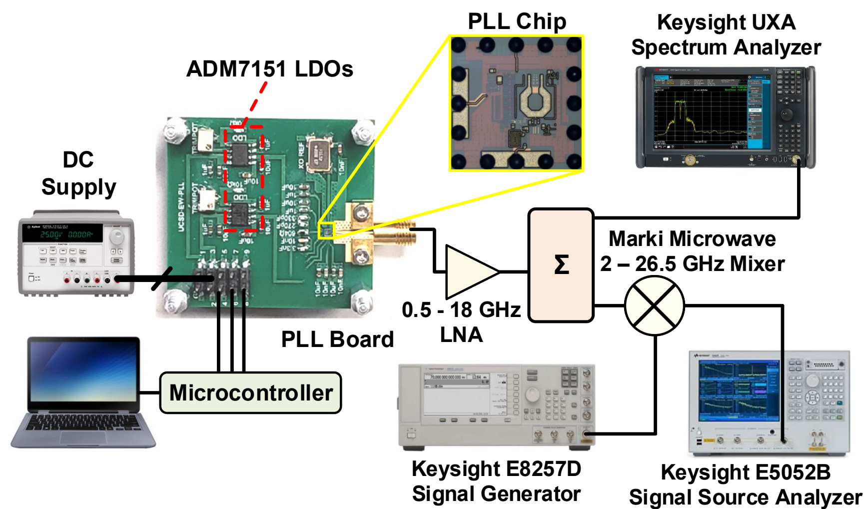


Figure 4.15: Measurement setup used for VCO and PLL characterization.

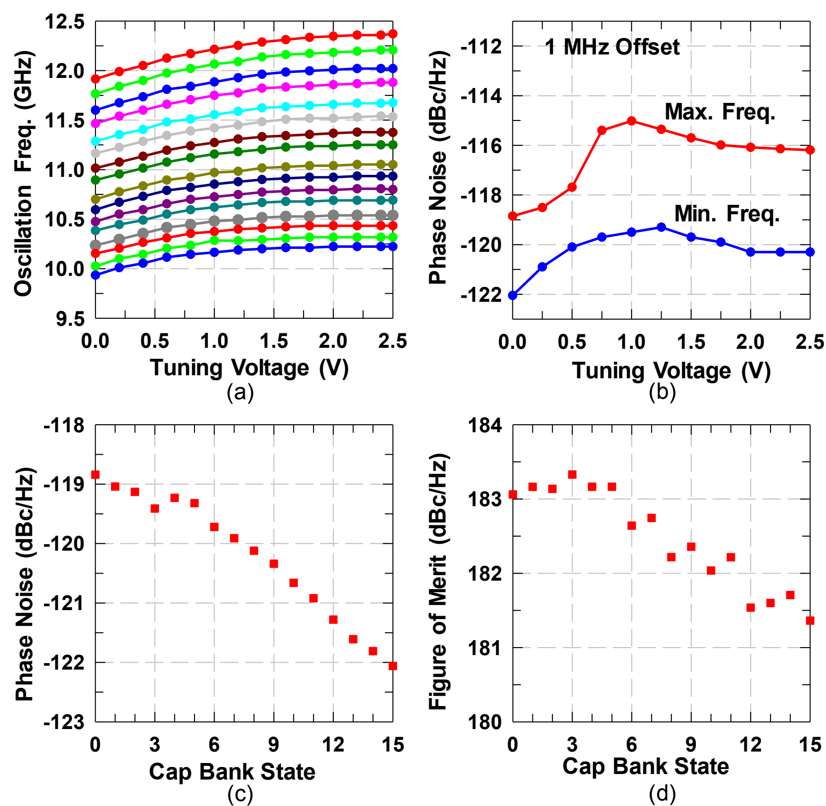


Figure 4.16: Measured frequency, phase-noise, and FoM of PMOS VCO. (a) Oscillation frequency versus tuning voltage, (b) phase-noise versus tuning voltage for minimum and maximum frequency states, (c) phase-noise versus capacitor-bank state when the tuning voltage is 0 V, (d) VCO figure of merit versus capacitor-bank state.

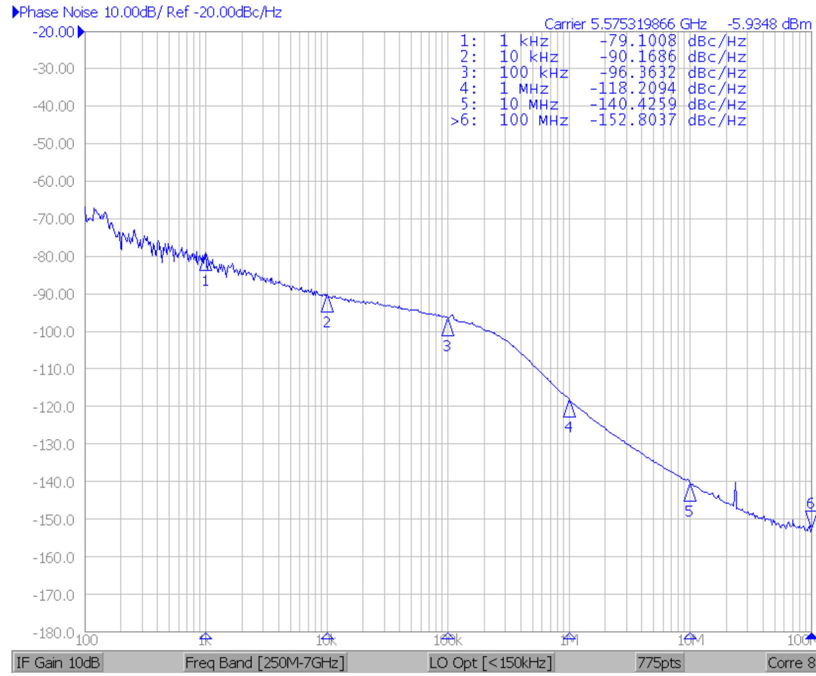


Figure 4.17: Screenshot on E5052B of measured PLL phase-noise at 10.575 GHz (LO frequency is 5 GHz).

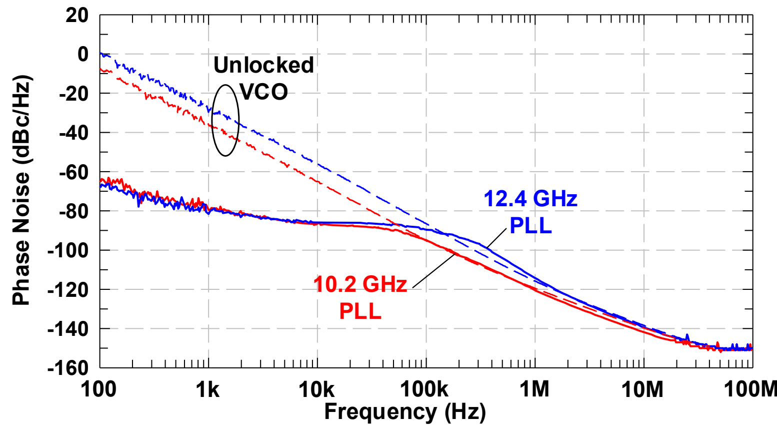


Figure 4.18: Plot of measured PLL and VCO phase-noise in highest and lowest frequency states.

state (maximum capacitance). Note that phase-noise tends to degrade with tuning voltage as the varactor is moved into the range with a lower Q-factor, and higher sensitivity to voltage variation. Fig. 4.16(c) and (d) present the VCO's phase-noise and FoM for a 0 V tuning voltage versus capacitor-bank state (where state 0 corresponds with the highest oscillation frequency and state 15 with the lowest frequency). For this measurement, the VCO supply voltage is adjusted between 2.0 and 2.5 V depending on the capacitor-bank

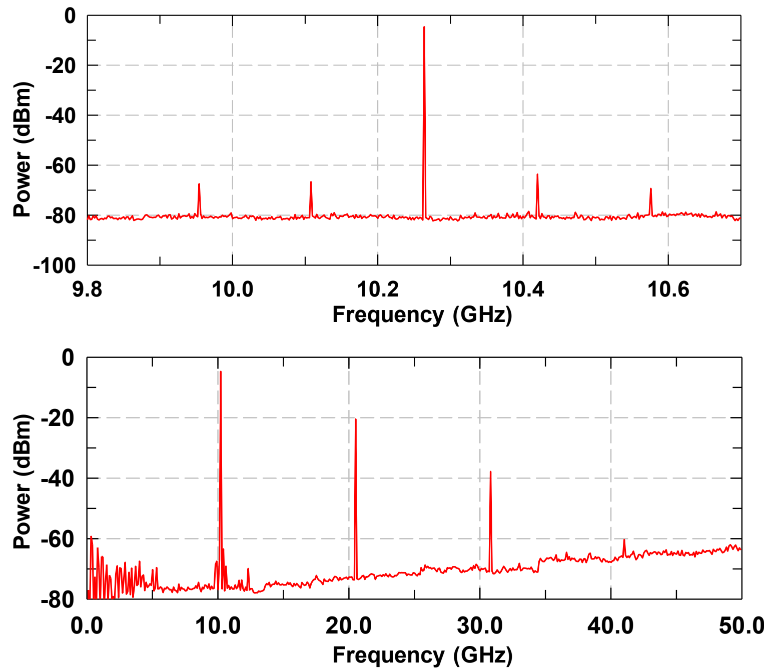


Figure 4.19: Measured close in and wideband spectrum of PLL output using Keysight UXA spectrum analyzer. Measurement is taken by connecting PLL output directly to spectrum analyzer without external amplification or de-embedding test board trace and connector losses.

Table 4.3: Integrated RMS Jitter and Estimated EVM Contribution for Various Integration Bounds and Frequency Multiplications

	Integration Bound (MHz)					
	0.001 - 10		**0.001 - 1000**		**0.05 - 1000**	
Mult.	**Jitter**	**EVM**	**Jitter**	**EVM**	**Jitter**	**EVM**
x1	198.6 fs	1.319%	199.2 fs	1.32%	144.8 fs	0.99%
x2		2.64%		2.65%		1.98%
x3		3.96%		3.97%		2.97%

state in order to achieve lowest phase-noise for a given state. The figure of merit of the VCO degrades versus capacitor-bank state despite the increase in phase-noise performance as a result of the raised supply voltage in these states.

A screenshot of the measured PLL phase-noise on the E5052B signal source analyzer is presented in Fig. 4.17, and is -118 dBc/Hz at 1 MHz offset. Fig. 4.18 presents the PLL and unlocked VCO phase-noise in the highest and lowest PLL locking states of 10.2 and 12.4 GHz. The close in and wideband PLL output spectrum is shown in Fig. 4.19. The specrums are measured by attaching the PLL test board output directly to the UXA spectrum analyzer with no line/connector loss de-embedded. Measured -70 dBc spurs

Table 4.4: VCO Comparison to Previously Published Works

Technology	Freq (GHz)	Tuning Range (%)	P_{DC} (mW)	Area (mm^2)	L(1 MHz) (dBc/Hz)	FoM @ 1 MHz	FoMT @ 1 MHz	Ref.
0.12 μm SiGe BiCMOS	**9.9 - 12.45**	**23**	**75**	**0.8†**	**-122**	**183**	**190**	**This Work**
SiGe BiCMOS	12 - 15.9	27	26.4	0.096	-117	186	190	[85]
0.18 μm SiGe BiCMOS	12.43 - 12.84	3	4.3	0.45†	-117	193.1	183.4	[86]
0.25 μm SiGe BiCMOS	12.43 - 13.08	5	93	0.25	-123	185	182	[87]
0.25 μm SiGe BiCMOS	13.5 - 14.8	9	231.5	0.87†	-121.4	180.4	179.4	[88]
65 nm CMOS	6.39 - 14	75	2.2 - 10.3	0.126	-117	186	194	[89]
90 nm CMOS	9.4 - 11.5	20	16	0.2	-117	185	188	[90]

$FoM = -L(f_{off}) + 10log\left\{(\frac{f_0}{f_{off}})^2(\frac{1mW}{P_{DC}})\right\}$, $FoMT = FoM + 20log(\frac{FTR}{10\%})$, † including pad area,

spaced at 155.52 MHz are observed in the close-in output spectrum and are likely caused by leakage of the reference signal to the supplies of the PLL chip. Due to the VCO harmonic loads, significant harmonics are observed in the wideband spectrum at the 2nd and 3rd harmonics of the fundamental output tone. In the larger system proposed in Fig. 4.1, these harmonics are easily filtered by a simple low-pass filter on the PCB and by the frequency response of the doubler or tripler stage in the transceiver chip.

The PLL's integrated RMS Jitter and its corresponding estimated EVM contribution to a system is summarized in Table 4.3. The RMS jitter integrated over the commonly reported bounds of 0.001 - 10 MHz is 198.6 fs, and corresponds to an estimated EVM contribution of 1.32% if the synthesizer is not followed by frequency multiplication. If the synthesizer is frequency multiplied by 2 for use in a 28 GHz system, or by 3 for use in a 39 GHz system, then the contributed EVM will double or triple, respectively. Due to the PLL's low (-150 dBc/Hz) noise floor after 10 MHz, the RMS jitter is negligibly affected if the integration bounds are extended to 0.001 - 1000 MHz. If the low-end integration bound is relaxed to 50 kHz to account for a realistic communication time-frame of 50 μs, the RMS jitter improves to just 144 fs and the associated EVM contribution is below 2% in a 28 GHz system and below 3% in a 39 GHz system.

Table 4.5: PLL Comparison to Previously Published Works

Technology	Type	Ref. Freq. (MHz)	Output Freq. (GHz)	Area (mm^2)	P_{DC} (mW)	L(1 MHz) (dBc/Hz)	Integrated Jitter (fs)	FoM*	Ref.
0.12 μm SiGe BiCMOS	**Integer**	**155.52**	**20.52 - 24.88**	**1.232†**	**150††**	**-116**	**199**	**-232.2**	**This Work**
65 nm CMOS	Fractional	230	26.2 - 32.4	0.28	26.9	-112.6	70.4	-249	[59]
65 nm CMOS	Fractional	40	27.5 - 29.6	1.2†	33	-95	510	-231	[91]
0.13 μm CMOS	Fractional	61 - 69	26.7 - 33.27	2.4†	143	-91	199	-232	[92]
28 nm CMOS	Fractional	40	9.2 - 12.7	1.035†	13	-104	230	-241	[63]
65 nm CMOS	Fractional	270	28.5 - 33.5	0.12	34.8	-	545	-230	[62]
65 nm CMOS	Integer	125	21 - 32	2.4†	87	-107	103.9	-235.5	[64]
45 nm CMOS	Integer	48	21.7 - 27.8	0.14	40	-93	306	-234	[93]
32 nm SOI	Fractional	28	13.1 - 28	0.24	31	-96	320	-235	[94]
32 nm SOI	Fractional	-	12 - 26	0.28	30	-90	-	-	[61]
32 nm SOI	Integer	-	23.8 - 30.2	0.22†	31	-93	199	-239	[60]
40 nm CMOS	Integer	390	21.4 - 25.1	0.1	64	-101	392	-230	[95]

* $FoM = 10log\{(Jitter/sec)^2(P_{DC}/1mW)\}$, † including pad area, ††buffer power (30 mW) included (P_{out} = 0 dBm). Multiplier not included as it is part of transceiver

4.4.1 Comparison to Prior Work

The performance of the VCO is compared to that of previously published works in Table 4.4, and shows one of the lowest reported phase-noises at 1 MHz offset frequency, and with higher tuning range than most comparable works. Table 4.5 presents the PLL comparison to other published works. So that the PLL may be compared with works intended for similar (28 GHz) systems the performance of the PLL is extrapolated assuming that it is followed by a frequency multiplication of 2 and its phase-noise is increased by 6 dB.

The PLL demonstrates the best phase noise at 1 MHz offset of any previous work, and with a moderate figure of merit. While references [59] and [64] achieve considerably lower integrated jitter performance than this work, [59] does so by using a highly complex cascaded topology where both a 7 and 28 GHz PLL are co-designed to produce a cascaded PLL with improved noise performance within a range of frequency offsets, and [64] reduces jitter by coupling three identical PLLs for a three-times improvement in noise performance. This work demonstrates that a simple, robust design emphasizing the performance of a single RF VCO, can produce results suitable for 5G communication systems.

4.5 Conclusion

This paper presented a simple, type-II charge-pump based PLL capable of achieving performance suitable for 5G communications at 28 or 39 GHz using a design emphasizing a single, high performance 10 - 12 GHz VCO. Analysis was presented showing that the tuning of VCO harmonic impedances can enhance VCO performance in terms of phase-noise, flicker corner, and dc power usage. The VCO achieved -122 dBc/Hz phase-noise at 1 MHz offset with an FoM and FoMT of 183 and 190, respectively. The PLL achieved an integrated jitter from 0.05 - 10 MHz of 144 fs at 10 - 12 GHz.

Acknowledgment

Chapter 4, in full has been submitted for publication of the material as it may appear in E. Wagner, O. Shana'a, and G. M. Rebeiz, "A Very Low Phase Noise Transformer-Coupled Oscillator and PLL for 5G

Communications in 0.12 μm SiGe BiCMOS," in *IEEE Trans. Microw. Theory Techn.*. The dissertation author was the primary investigator and author of this material. The author would also like to thank Intel for technical discussion and project funding, and Integrand Software for supplying licenses for EMX electromagnetic modeling software.

Although the work does not appear in the text of this chapter or in its corresponding publication, the author thanks Hyunchul Chung for his assistance providing the layout of a doubler that was originally intended to be integrated onto the PLL, and which was present in an early test version of this work.

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