Title

Engineering Wafer Bonded Heterojunction Interfaces for Wide Bandgap Semiconductors

Author

Huynh, Kenny

Publication Date

2023

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

Engineering Wafer Bonded Heterojunction Interfaces for Wide Bandgap Semiconductors

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy in

Materials Science and Engineering

by

Kenny Huynh

2023

ABSTRACT OF THE DISSERTATION

Engineering Wafer Bonded Heterojunction Interfaces for Wide Bandgap Semiconductors

by

Kenny Huynh

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2023

Professor Mark S. Goorsky, Chair

Heterogeneous integration of semiconductors necessitates the understanding of their interfaces. This dissertation focuses on understanding thermal transport across wafer bonded interfaces by beginning from a fundamental understanding of wafer bonded Si|Ge interfaces, then by increasing the complexity by integrating Si|GaN. Finally, the possibilities of bonding GaN, AlN, and β-Ga_2O_3 are explored.

First, we study the recovery of thermal conductivity in semiconductors that undergo amorphization due to ion implantation. Understanding this process is an important part of engineering wafer bonded interfaces that are subjected to ion bombardment to sputter off unwanted oxides prior to bonding. Depending on the implant energy and species, this ion

bombardment treatment may lead to the amorphization of some semiconductor surfaces in the order of nanometers. Bonding these amorphized surfaces will alter the interfacial transport properties at the bonded interface so understanding the recrystallization process and thermal conductivity can be recovered is an important step to post bonding interface engineering. We find full recrystallization of amorphized silicon after annealing at 700 °C for 30 min, and full recovery of the thermal conductivity.

Next, the Si-Ge system is used as a fundamental example of heterogeneous integration, which we can use to analyze the intricacies of interface engineering before introducing additional complexities when moving towards compound wide band gap semiconductors. Thermal boundary conductance (TBC) results show that the TBC of the as bonded sample is 47 ± 5 MW/(m^2·K). The TBC for the sample annealed at 600 °C for 48 hours is 95 ± 5 MW/(m^2·K), an improvement by a factor of two compared to the as-bonded interface. Recrystallization of the amorphous interface, interdiffusion, twist misorientation, and impurities at the interface all effect the thermal boundary conductance at bonded interfaces.

Then, the evolution of structural and thermal interfacial properties of direct wafer bonded (0001) GaN to (100) Si with annealing is investigated. Direct wafer bonded GaN on Si with high thermal boundary conductance of 140 MW/(m^2·K) is demonstrated in this work. Annealing at 450 °C for 7 hours and 700 °C for 24 hours was done to attempt to reconstruct the amorphous interface and to investigate the stability of the bonded interface at high temperatures. After annealing at 450 °C for 7 hours, a Ga-rich plane is observed across the interface near the surface of the Si in addition to SiN_x formation at the original bonded interface. Further high temperature annealing (700 °C 24 hours) resulted in the formation of Ga-rich pyramidal features that form across the bonded interface in the silicon along (111) Si planes. While recrystallization was

observed to have a beneficial impact in other bonded systems, the formation here of SiNx and Ga-rich pyramidal features in the Si have shown deleterious effects on thermal transport across the interface and a reduction in the measured TBC by a factor of two after annealing at 700 °C for 24 hours.

Moving forward towards technologically relevant wide band gap materials like GaN, AlN, and β-Ga_2O_3, successful integration must be achieved before interface engineering is possible. GaN|AlN direct wafer bonding has been successfully achieved and preliminary characterization is reported. A ~1.5 nm interfacial region is observed, which is suspected to be caused by reconfiguration of the interface after a total anneal of 350 °C 22 hours, 600 °C 1 hour, and 800 °C 1 hour. No thicker amorphous or oxide interfacial layer commonly found in other bonding methods (surface activated bonding, plasma treatment, or other interfacial layers) are observed in this study. The thermal boundary conductance in the as-bonded case is 250 $MW/(m^2 \cdot K)$

Lastly, the chemical reaction between Al and various orientations of β-Ga_2O_3 are studied as a precursor to heterogeneous integration of β-Ga_2O_3. A mechanism for increased interdiffusion between Al and β-Ga_2O_3 along (010) β-Ga_2O_3 in contrast to (001) and $(\bar{2}01)$ oriented substrates is proposed. Theoretical studies of Al incorporation in $(Al_xGa_{1-x})_2O_3$ alloys have predicted the preference of Al on octahedral sites in β-Ga_2O_3. A consecutive pathway of octahedral sites perpendicular to the interface presents itself in (010) β-Ga_2O_3 substrates that results in a thicker interfacial oxide layer. Under identical growth conditions, Al on (001) and $(\bar{2}01)$ β-Ga_2O_3 show thinner oxide layers that are sharper from the HRTEM. The rows of tetrahedral Ga sites act as barriers to interdiffusion of Al further into the β-Ga_2O_3 bulk.

The dissertation of Kenny Huynh is approved.

Dwight Christopher Streit

Suneel Kodambaka

Timothy S. Fisher

Mark S. Goorsky, Committee Chair

University of California, Los Angeles

2023

To my friends and family,

thank you for your endless love and support.

Table of Contents

List of Figures

pyramidal features observed in the HAADF STEM correspond to Ga. Additionally it can be seen that the original bonded interface (outlined in yellow), is deficient in Ga and Si and N are present in this region.

Figure 5.5: Integrated line scans of the EDX maps of (a) Sample_RT and (b) Sample_700.24. From the line scan of Sample_RT shown in (a), we can see evidence of a Ga-rich surface due to preferential sputtering of N during the Ar ion bombardment surface process. In (b), we observe clear evidence of Ga diffusion into the Si bulk as well as the presence of SiN_x formation at the original bonded interface (dotted in black).

Figure 6.1: The unit cell of β-Ga_2O_3 consists of two unique Ga sites and three unique oxygen sites: (gray) Ga_I on tetrahedral sites, (black) Ga_{II} on octahedral sites, (red) O_I shared between 1 tetrahedral and 2 octahedral, (green) O_{II} shared between 2 tetrahedral and 1 octahedral, and (blue) O_{III} shared between 1 tetrahedral and 3 octahedral.

Figure 6.2: High resolution transmission electron microscopy images at the interface of (a) Al | (010) β-Ga2O3, (b) Al | (001) β-Ga2O3, and (c) Al | $(2\bar{0}1)$ β-Ga2O3. The corresponding crystal models are shown below each respective TEM image.

Figure 6.3: EDX elemental mapping of Ga, O, and Al across the Al | β- β-Ga_2O_3 interfaces showing that Ga is segregated from the oxide and can be seen diffusing into the Al. The orientational dependence on the interface oxide layer thickness can be seen by comparing the (010) substrate interface with (001) and $(\bar{2}01)$ substrates.

Figure 6.4: Low magnification EDX mapping and STEM shows the presence of Ga diffusion from the interface and along grain boundaries within the Al film.

List of Tables

Acknowledgements

I would like to extend my deepest appreciation to Professor Mark Goorsky for his mentorship and guidance throughout my time in graduate school. He has taught me to be critical and meticulous of my work and to communicate clearly and concisely, skills that I will value for the rest of my career. I would also like to thank my committee members Professor Dwight Streit, Professor Suneel Kodambaka, and Professor Timothy Fisher for lending me their expertise and insight to further push the boundaries of my research. Thank you for all the time and effort that you have all dedicated to supporting me.

This work would not have been possible without the financial support from the Office of Naval Research under the Multidisciplinary University Research Initiatives (MURI) Program as well as from the National Science Foundation Graduate Research Fellowship Program. I was very fortunate to have collaborated with Professor Samuel Graham, Professor Patrick Hopkins, Professor Asif Khan, Professor Alan Doolittle, Professor Asegun Henry, Professor Tengfei Luo, and Dr. Jianguo Wen. Thank you all for the expertise and perspectives regarding thermal metrology, materials growth, computational materials science, and electron microscopy.

Next, I would like to thank all of labmates that I have had the pleasure working with over the years. To Dr. Michael Liao and Dr. Yekan Wang I could not have asked for better mentors, coworkers, and friends. Through the good times and bad times, we always supported each other and got the job done. To Dr. Ariella Machness, Dr. Tingyu Bai, Dr. Eva Rosker, Brandon Carson, Lezli Matto, Kaicheng Pan, Patricia Barron, Alexander Stafford, Eugene Kwon, Nishanth Ravi, Hrithik Agrawal, Dorian Luccioni and Ashwyn Yeo, it was a joy meeting and working with each and every one of you.

I would not be where I am today without the support and guidance that I received from the Santa Monica College Science and Research Initiative program as well as the UC Leadership Excellence through Advanced Degrees program. Dr. Rachel Kennison, Vanan Yahnian, and the late Dr. Oscar Stafsudd were integral in the early stages of community college that fostered the motivation for pursuing a graduate degree. Dr. Celina Mojica, Daniel Fabrega, Dr. Martha Mecartney, and Dr. Jaeho Lee gave me the opportunities to continue exploring my passion for research in materials science during my undergraduate studies.

Finally, I would like to thank my friends and family for their endless love and support. Specifically, to my mom and dad who emigrated from Vietnam and sacrificed so much to support my dreams and aspirations.

VITA

Education

2015	Santa Monica College Santa Monica, CA, USA
2018	Bachelors of Science in Materials Science and Engineering University of California, Irvine Irvine, CA, USA

Honors

2018	National Science Foundation Graduate Research Fellowship Program University of California, Los Angeles

Publications

Huynh, K, et al., (2023). Crack formation in strained β-$(Al_xGa_{1-x})_2O_3$ films grown on (010) β-Ga_2O_3 substrates. J. Vac. Sci. [submitted]

Huynh, K., et al., (2023). Improved Thermal Boundary Conductance in Annealed Direct Wafer Bonded Si-Ge. ACS Appl Mater Interfaces [submitted].

Huynh, K., et al., (2023). Stability of Interface Morphology and Thermal Boundary Conductance of Direct Wafer Bonded GaN|Si Heterojunction Interfaces Annealed at Growth and Annealing Temperatures. ACS Appl Mater Interfaces [submitted]

Huynh, K., et al., (2023). Dissolution of Mg-enriched Defects in Implanted GaN and Increased P-type Dopant Activation. Journal of Applied Physics [submitted]

Huynh, K., et al., (2023). Depth-dependent recovery of thermal conductivity after recrystallization of amorphous silicon. Journal of Applied Physics 133.13.

Huynh, K., et al., (2022). Surface reaction dependence of molecular beam epitaxy grown aluminum on various orientations of β-Ga_2O_3. APL Materials, 10(1), p.011110.

Liao, M.E., **Huynh, K.**, et al., (2023). Thermal transport and structural improvements due to annealing of wafer bonded β-Ga_2O_3| 4H-SiC. Journal of Vacuum Science & Technology A, 41(6).

Liao, M.E.,…**Huynh, K.**, et al., (2023). Origins of epitaxial macro-terraces and macro-steps on GaN substrates. Journal of Applied Physics, 133(18).

Liao, M.E., **Huynh, K.**, et al., (2023). Optimization of chemical mechanical polishing of (010) β-Ga_2O_3. Journal of Vacuum Science & Technology A, 41(1).

Hussain, K., **Huynh, K.**, et al., (2023). High figure of merit extreme bandgap $Al_{0.87}Ga_{0.13}N$ - $Al_{0.64}Ga_{0.36}N$ heterostructures over bulk AlN substrates. Applied Physics Express, 16(1), p.014005.

Pfeifer, T.W.,…**Huynh, K.**, et al., (2022). Measuring sub-surface spatially varying thermal conductivity of silicon implanted with krypton. Journal of Applied Physics, 132(7).

Wang, Y.,…**Huynh, K.**, et al., 2022. Investigation of the Reverse Leakage Behavior and Substrate Defects in Vertical GaN Schottky and PIN Diodes. ECS Journal of Solid State Science and Technology, 11(6), p.065006.

Koh, Y.R.,…**Huynh, K.**, et al., (2021). High thermal conductivity and thermal boundary conductance of homoepitaxially grown gallium nitride (GaN) thin films. Physical Review Materials, 5(10), p.104604.

Tan, S.,…**Huynh, K.**, et al., (2021). Surface reconstruction of halide perovskites during post-treatment. Journal of the American Chemical Society, 143(18), pp.6781-6786.

Hoque, M.S.B.,…**Huynh, K.**, et al., (2021). High in-plane thermal conductivity of aluminum nitride thin films. ACS nano, 15(6), pp.9588-9599.

Wang, Y.,…**Huynh, K.**, et al., (2021). Structural Characterization of Dot-Core GaN Substrates with Annealing Under Growth-Like Conditions Using Synchrotron Monochromatic X-ray Topography. ECS Journal of Solid State Science and Technology, 10(4), p.045010.

Lee, J.W.,…**Huynh, K.**, et al., (2020). Solid-phase hetero epitaxial growth of α-phase formamidinium perovskite. Nature communications, 11(1), p.5514.

Wang, Y., **Huynh, K.**, et al., (2020). Strain Recovery and Defect Characterization in Mg-Implanted Homoepitaxial GaN on High-Quality GaN Substrates. physica status solidi (b), 257(4), 1900705.

Cheng, Z.,…**Huynh, K.**, et al., (2020). Thermal Transport across Ion-Cut Monocrystalline β-Ga_2O_3 Thin Films and Bonded β-Ga_2O_3–SiC Interfaces.

Cheng, Z.,…**Huynh, K.**, ... & Graham, S. (2020). Experimental observation of high intrinsic thermal conductivity of AlN. Physical Review Materials, 4(4), 044602.

Liao, M.E., **Huynh, K.**, et al., (2020). Ion Species Dependence on the Interfacial Properties of Silicon Homojunctions Bonded Using an Ion Bombardment Treatment. ECS Transactions, 98(4), p.81.

Huynh, K., et al., (2018). Investigation of Elastic Modulus and Thermal Conductivity of Rough Silicon Nanowires. In 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) (pp. 214-217). IEEE.

Chapter 1: Introduction

1.1 Wide bandgap semiconductors

Advancements in silicon semiconductor devices are quickly approaching their performance limits and have shown limited high temperature capabilities. Self-heating of Si devices above 200 °C results in high junction temperatures and leads to high leakage currents.[1] In order to manage hot spots, cooling mechanisms may result in additional unwanted weight or size. Research in wide band gap (WBG) semiconductors has garnered popularity in an effort to reduce device size, increase efficiency, and allow device operation at higher temperatures. Since intrinsic carrier concentration of a semiconductor is inversely proportional to its bandgap, at higher temperatures intrinsic carrier concentrations may no longer be negligible in lightly doped regions, which lead to undesirable device characteristics. In silicon, this occurs around 150 to 200 °C. Additionally, WBG semiconductors (SiC, GaN, β-Ga2O3) have larger breakdown voltages (>2 MV/cm) compared to Si (~0.3 MV/cm), meaning that devices can be made much

Semiconductor	Si	GaN	4H-SiC	β-Ga_2O_3
Band Gap (eV)	1.1	3.4	3.3	4.8
Breakdown Electric Field (MV/cm)	0.3	3.3	2.5	8
Thermal Conductivity (W m^{-1} K^{-1})	120	200	270	10-27

Table 1.1: Comparison of the band gap, breakdown electric field, and thermal conductivity of wide band gap materials with Si.

thinner for the same power requirements. Improved switching speeds and higher operating temperatures would allow advancements in power electronics for applications such as electric motors, data centers, and aerospace to name a few.[2,3] Table 1.1 compares the relevant electrical and thermal properties of wide band gap semiconductors and Si.

1.2 Thermal management of power devices

Devices with faster switching speeds result in larger thermal gradients. New thermal management strategies are required to mitigate hot spots as a result of improved switching speeds for WBG semiconductors devices. Device architectures of top-side, bottom-side, and double-sided cooling schemes have been investigated for lateral and vertical WBG devices. Bottom-side cooling integrates high thermal conductivity substrates as a heat sink while top-side cooling strategies dissipate heat through the interconnect structure that includes the source, drain, and gate contacts, which are put in contact with a high thermal conductivity substrate. Not surprisingly, double sided cooling schemes that incorporate both top and bottom sided cooling result in the best thermal management in an idealized setting.[4-6] However, in complex device architectures thermal resistances increase with an increasing number of interfaces that are important to consider. Engineering these interfaces is a key aspect of making WBG semiconductor devices economically viable.

At the junction between two materials, interfacial resistance impedes thermal transport and causes a thermal gradient. Interfacial resistance is equal to heat flux over the change in temperature across that interface. When considering thermal transport across heterojunctions, engineer thermal boundary conductance is also important in addition to a high thermal conductivity substrate. Cheng et al., have simulated GaN and Ga_2O_3 two finger devices on several high thermal conductivity substrates and have shown the effect of thermal boundary

conductance on the maximum operating temperature.[7] The effect of thermal boundary conductance on maximum device temperature plateaus roughly around 100-150 MW/(m^2·K), after which substrate thermal conductivity plays a more dominant role.

1.3 Wafer bonding of semiconductors

Wafer bonding is a method of joining two materials systems via Van der Waals forces and is frequently used for applications in silicon-on-insulators (SOI), micro-electromechamical systems (MEMS), and 3D-integrated circuits. One of the biggest advantages over epitaxy is that wafer bonding is not restricted by lattice mismatch or orientation. This allows more flexibility in material choices for engineers during the design process. However, understanding of the underlying mechanisms is required to optimize properties of wafer bonded systems. Other concerns to consider during wafer bonding are the thermal stresses developed during annealing due to the differences in the coefficients of thermal expansion, which can lead to debonding or cracking. It is crucial to understand how to control the reconstruction of the interface because it has been shown to affect electrical, thermal, and mechanical properties of wafer bonded systems.[8-14]

The wafer bonding technique utilizes high surface energies that are a result of sub-nanometer rough surfaces to bond the surfaces that come into contact. In comparison to epitaxial growth, wafer bonding is not affected by lattice mismatch. So, there is more freedom in choosing the substrate. This allows for heterojunctions to be formed from separately grown, high quality substrates to limit dislocations that would otherwise thread through epitaxial layers during growth. Improving crystal quality and reducing dislocation density is crucial to limiting recombination sites that impede transport properties.[15]

Obtaining sub-nanometer roughness wafers is not always trivial. Oftentimes, this level of roughness can be obtained via chemical mechanical polishing (CMP).[16] During CMP a solution is used to chemically react with the surface and create an oxide or a softer material than the bulk wafer. Then the soft material is mechanically planarized with a polishing pad. The reason this level of roughness is important is because the decreased contact area between two rough wafers can lead to unbonded areas that form after wafer bonding is initiated.

To further enhance surface activation prior to bonding, surface preparation techniques are used to clean any unwanted oxides or surface contaminants. Low energy ion bombardment is one surface preparation method that has found popularity within this field. This involves a low energy, low angle ion implantation typically of an inert gas (ex. Ne, Ar, Kr). The resulting surface can sometimes be amorphized depending on the energy and the mass of the ion used. Careful characterization of this surface prior to bonding is important because the two surfaces will eventually bond to create the interface. Figure 1.1 shows a schematic of the ion bombardment process.

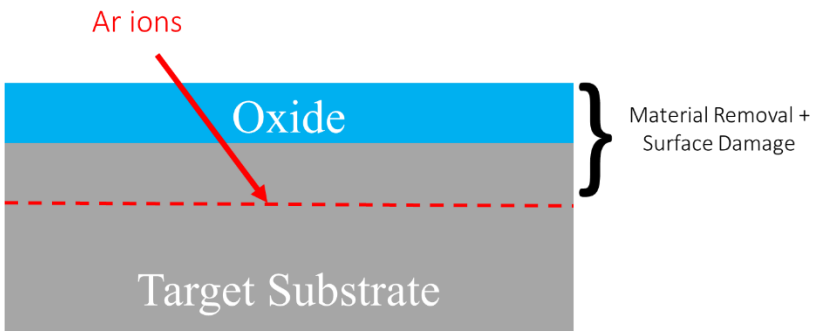

Figure 1.1: Schematic of surface activation via ion bombardment prior to wafer bonding. Depending on the energy and ion species used, this technique may induce an amorphous layer near the surface, which forms the interface when the wafer bonding procedure is done.

1.4 Dissertation outline

This dissertation focuses on understanding thermal transport across wafer bonded interfaces by beginning from a fundamental understanding of wafer bonded Si|Ge interfaces, then increases the complexity by integrating Si|GaN, and GaN|AlN. Finally, the Al|β-Ga_2O_3 interface as a function of β-Ga_2O_3 orientation is also investigated as a precursor to heterogeneous integration of β-Ga_2O_3.

1.5 References

[1]Neudeck, P.G., Okojie, R.S. and Chen, L.Y., 2002. High-temperature electronics-a role for wide bandgap semiconductors?. Proceedings of the IEEE, 90(6), pp.1065-1076.

[2]Kizilyalli, I.C., Carlson, E.P., Cunningham, D.W., Manser, J.S., Xu, Y.A. and Liu, A.Y., 2018. Wide Band-Gap Semiconductor Based Power Electronics for Energy Efficiency. USDOE Advanced Research Projects Agency-Energy (ARPA-E).

[3]Kizilyalli, I.C., Carlson, E.P. and Cunningham, D.W., 2020, March. Wide-Bandgap Semiconductor Power Electronics: Overcoming Barriers in Materials to Circuits for a more Electrified Future. In CIPS 2020; 11th International Conference on Integrated Power Electronics Systems (pp. 1-7). VDE.

[4]Liang, Z., 2015, September. Integrated double sided cooling packaging of planar SiC power modules. In 2015 IEEE Energy Conversion Congress and Exposition (ECCE) (pp. 4907-4912). IEEE.

[5]Montgomery, R.H., Zhang, Y., Yuan, C., Kim, S., Shi, J., Itoh, T., Mauze, A., Kumar, S., Speck, J. and Graham, S., 2021. Thermal management strategies for gallium oxide vertical trench-fin MOSFETs. Journal of Applied Physics, 129(8), p.085301.

[6]Yuan, C., Zhang, Y., Montgomery, R., Kim, S., Shi, J., Mauze, A., Itoh, T., Speck, J.S. and Graham, S., 2020. Modeling and analysis for thermal management in gallium oxide field-effect transistors. Journal of Applied Physics, 127(15), p.154502.

[7]Cheng, Z., Graham, S., Amano, H. and Cahill, D.G., *Applied Physics Letters*, *120*(3) (2022).

[8]Mu, F., et al., Journal of Alloys and Compounds, 905, p.164076 (2022).

[9]Mu, F., et al., ACS applied materials & interfaces, 11(36), pp.33428-33434 (2019).

[10]Tian, Z., et al., *Physical Review B*, *86*(23), p.235304 (2012).

[11]Cheng, Z., et al., *Nature communications*, *12*(1), p.6901 (2021).

[12]Liao, M., Tran, V., Yee, M., Seal, M. and Goorsky, M.S., 2018. The role of misorientation in direct wafer bonded III-V materials. ECS Transactions, 86(5), p.185.

[13]Kish, F.A., Vanderwater, D.A., Peanasky, M.J., Ludowise, M.J., Hummel, S.G. and Rosner, S.J., 1995. Low-resistance Ohmic conduction across compound semiconductor wafer-bonded interfaces. Applied physics letters, 67(14), pp.2060-2062.

[14]Okuno, Y., Uomi, K., Aoki, M. and Tsuchiya, T., 1997. Direct wafer bonding of III-V compound semiconductors for free-material and free-orientation integration. IEEE Journal of quantum electronics, 33(6), pp.959-969.

[15]Drozdov, N. A., et al. Recombination radiation on dislocations in silicon. Jetp Lett. 23(11), 597-599 (1976).

[16]Roelkens, G., et al. III-V/Si photonics by die-to-wafer bonding. Materials Today 10.7-8, 36-43 (2007)

Chapter 2: Materials Characterization

2.1 X-ray diffraction

X-ray diffraction is a non-destructive structural characterization technique that provides changes in interplanar spacing (also known as the d-spacing) between planes within the crystal. Analysis of the changes in d-spacing in single crystals can lead to information regarding crystal imperfections including (but not limited to) strain, tilt, and curvature in the sample. In this work, x-ray diffraction is primarily used to measure the strain, crystal quality, curvature, and in-plane orientation of samples that are to be bonded. The principle behind x-ray diffraction is that the wavelength of x-rays is on the same order as the d-spacing in crystals and so the x-rays interact with the lattice and diffract to form waves that constructively and destructively interact at certain angles of incidence. This gives rise to diffracted intensity that is a function of Bragg's law, where λ is the wavelength, d is the interplanar spacing and θ is incident angle of the wave.

$$\lambda = 2d \sin \theta \quad (1)$$

After x-rays are generated from the copper target, they pass through a graded mirror and a Si (220) channel cut monochromater to produce a parallel beam which strikes the sample. When Bragg conditions are met, the sample diffracts x-rays that are characteristic of the lattice planes (and changes in the lattice planes), which are then captured by a detector. The acceptance angle of the diffracted beams can be further narrowed by including a 3rd bounce where the diffracted x-rays from the sample pass through a (220) analyzer crystal. This allows for higher resolution x-ray diffraction measurements that are able to deconvolute effects of strain and tilt. A schematic of the triple axis diffraction set up is shown below in Figure 2.1.

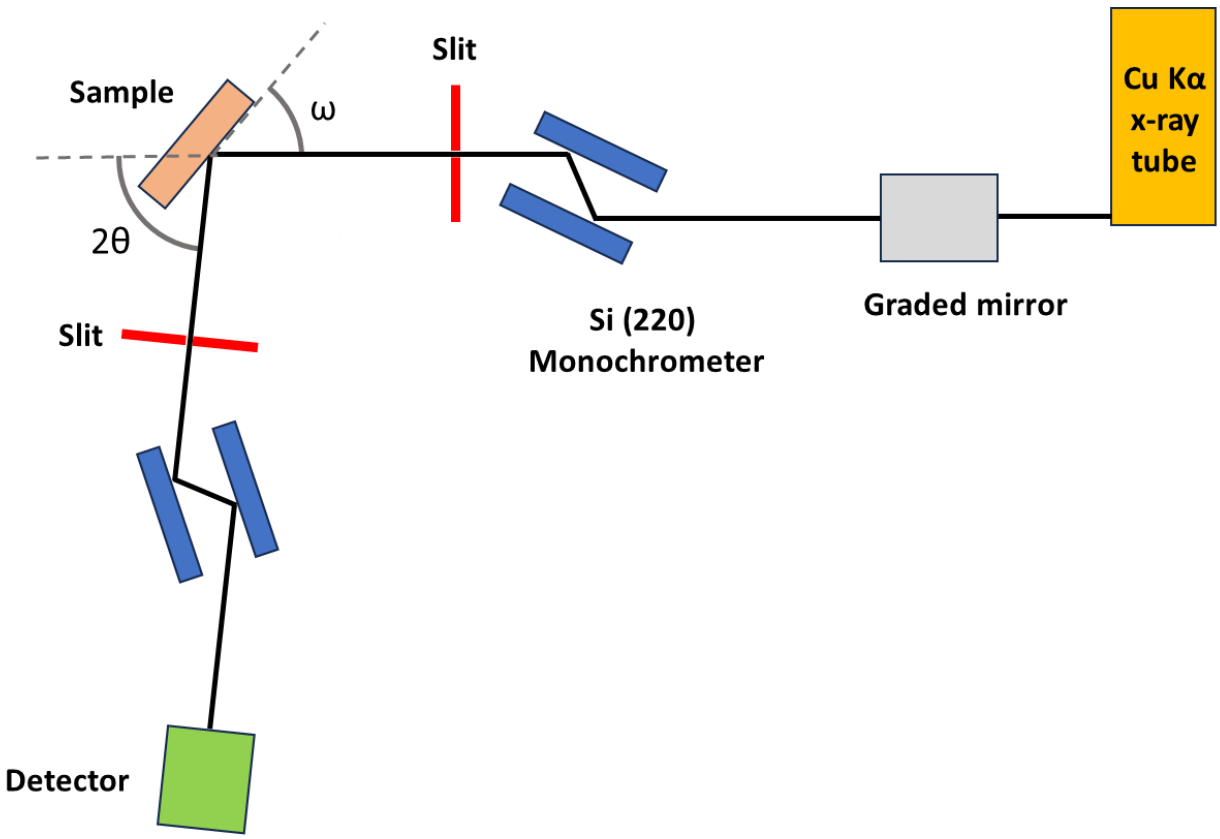

Figure 2.1: Schematic of triple axis x-ray diffraction used for strain, tilt, and in-plane misorientation measurements for wafer bonded samples.

2.2 Atomic force microscopy

Atomic force microscopy is a non-destructive surface characterization technique that provides topographical information of a sample surface. This is done by rastering the surface of a sample with a sharp probe at the end of a cantilever. The probe tip is controlled via a piezoelectric scanner that allows for movement in x, y and z dimensions. A laser is reflected off a mirror on the top side of the cantilever to a photodiode that records the position of the laser. As the probe is rastered across the surface, the force on the cantilever is kept constant through a feedback loop, such that as the probe encounters surface morphology, the piezoelectric scanner raises or lowers the probe to keep the force on the probe constant. This allows the probe to mimic the sample surface. The position of the probe is calibrated to the position of the reflected laser on the photodiode. As the cantilever is deflected, the position of the laser on the photodiode changes, and the position is recorded. See Figure 2.2 for a schematic of AFM in contact mode.

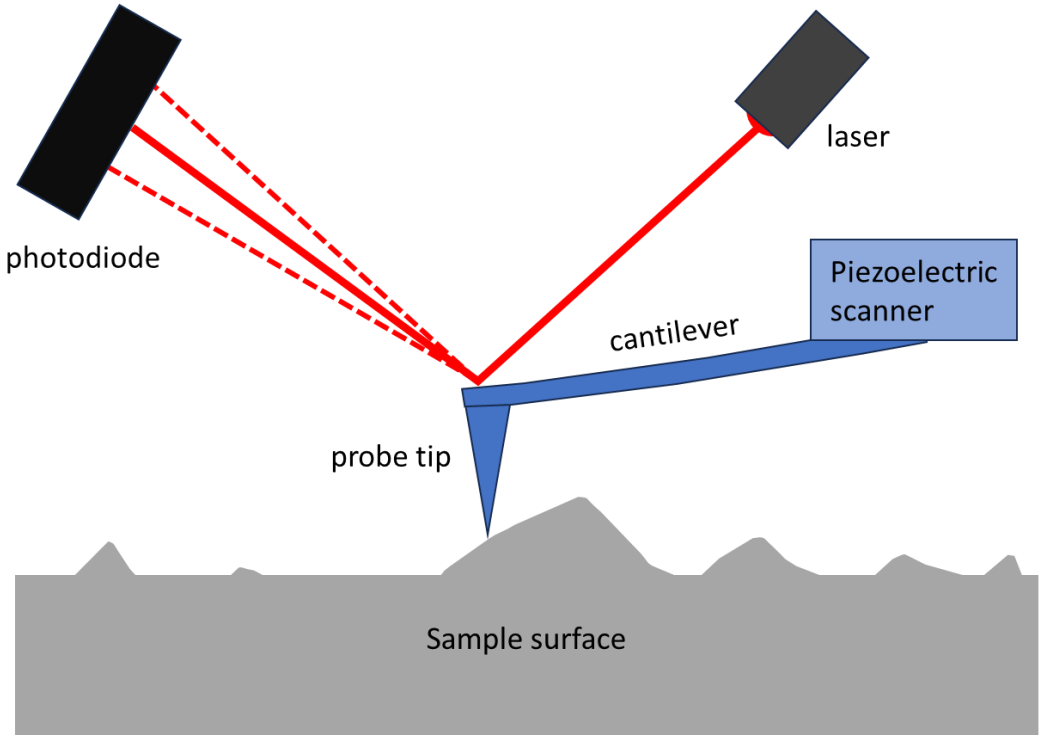

Figure 2.2: Schematic describing how atomic force microscopy measures changes in surface topography.

In this work, AFM is utilized to measure the surface roughness of semiconductor wafers prior to wafer bonding. Roughness is measured by the root-mean-square (RMS) of the peaks and valleys recorded by profiling the sample surface with the probe. This is preferred over the standard average of the peaks and valleys because RMS is more sensitive to outliers, which is important for more direct representation of the sample surface. Wafer bonding requires and RMS roughness of <1 nm.

2.3 Electron microscopy

To understand the structural characteristics of heterojunction interfaces, direct observation can be done through various electron microscopy techniques. This is made possible by accelerating a beam of electrons through an electromagnetic field and bombarding a sample, while collecting the signal from the various interactions that occur between the accelerated electrons and the sample electrons.

2.3.1 Sample preparation

To prepare a sample for transmission electron microscopy, in order to study changes at heterojunction interfaces, an electron transparent sample is required. This can be done by creating a very thin foil of the sample. The standard lift-out procedure is summarized below and show in Figure 2.3. First, a Pt protective layer is used to protect the sample surface. A gas-injection system releases a Pt precursor (Trimethyl(methylcylopentadienyl)Platinum(IV)), which dissociates due to collisions with secondary electrons near the surface of the sample. Local deposition of Pt is used as a protective layer to prevent unwanted milling of the surface when Ga^+ ions are used. Next, the ion beam is used to destructively mill away area revealing the cross-section of interest. A micromanipulator is maneuvered to the corner of the top surface of the sample and attached by platinum. The bottom of the cross-section is cut out by angling the FIB

beam with respect to the sample surface. The probe is then used to lift the sample out, where it is moved to a standard 4 post copper grid and attached with carbon. Lastly, the sample is milled down from both sides while lowering the ion beam current from 30kV to 10kV as the sample approaches its final thickness (~100 nm).

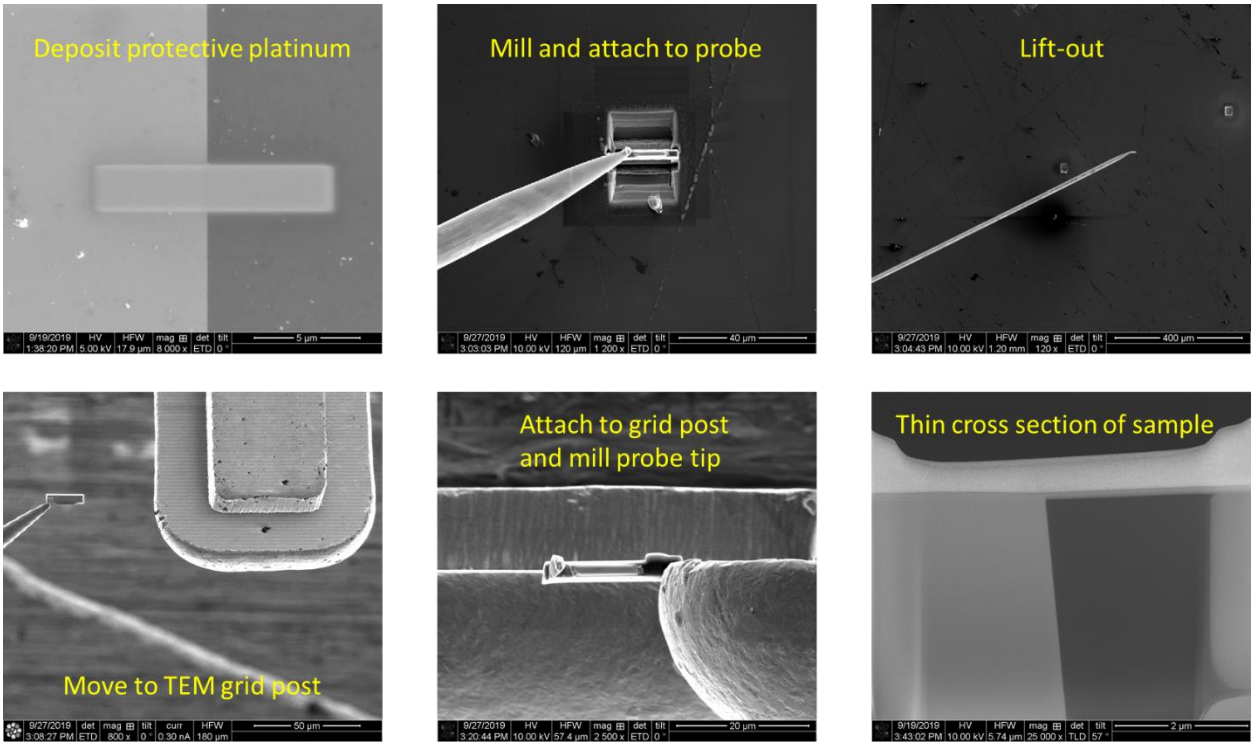

Figure 2.3: Step by step process showing how a TEM sample is fabricated for a wafer bonded sample.

2.3.2 Transmission electron microscopy

Transmission electron microscopy (TEM) is a technique that allows for direct observation of atomic sites, which is crucial for the study of heterojunction interfaces. A ~100 nm foil is loaded into a TEM sample holder that has access to two axes of rotation known as a double tilt stage. This stage is inserted into the TEM column and pumped down to ultra-high vacuum (10^{-7} to 10^{-8} torr). In a field emission electron source, a tungsten tip which is subject to high electric

fields (typical values ~3 x 10^7 V/m) extracts electrons from the tip and accelerates them with accelerating voltages from 80 – 300 kV. The electrons are then focused through a series of electromagnetic lenses and the final result is a parallel beam of electrons incident on the electron transparent sample as shown in Figure 2.4a. The resulting interactions with the sample as the electrons transmit through it are captured on a CCD camera.

There are several types of information that can be collected from TEM. Mass-density contrast is the difference in contrast in an image due to increased scattering of electrons due to differences in atomic number (Z) or the overall thickness of one region versus another. Diffraction contrast is contrast related to changes in crystallinity of a material, where defects may appear to change contrast based on satisfying Bragg's Law. Lastly, phase contrast is due to the interaction between transmitted and diffracted waves as they transmit through the sample. For a single crystal material, the interference pattern formed between transmitted waves and diffracted waves (due to the differences in the traveled path) gives rise to a periodic lattice that resembles the true lattice. Since sample thickness and microscope defocus change the distance that the waves travel, careful consideration of the defocus of the microscope and thickness of the sample are needed to accurately reveal the physical lattice.

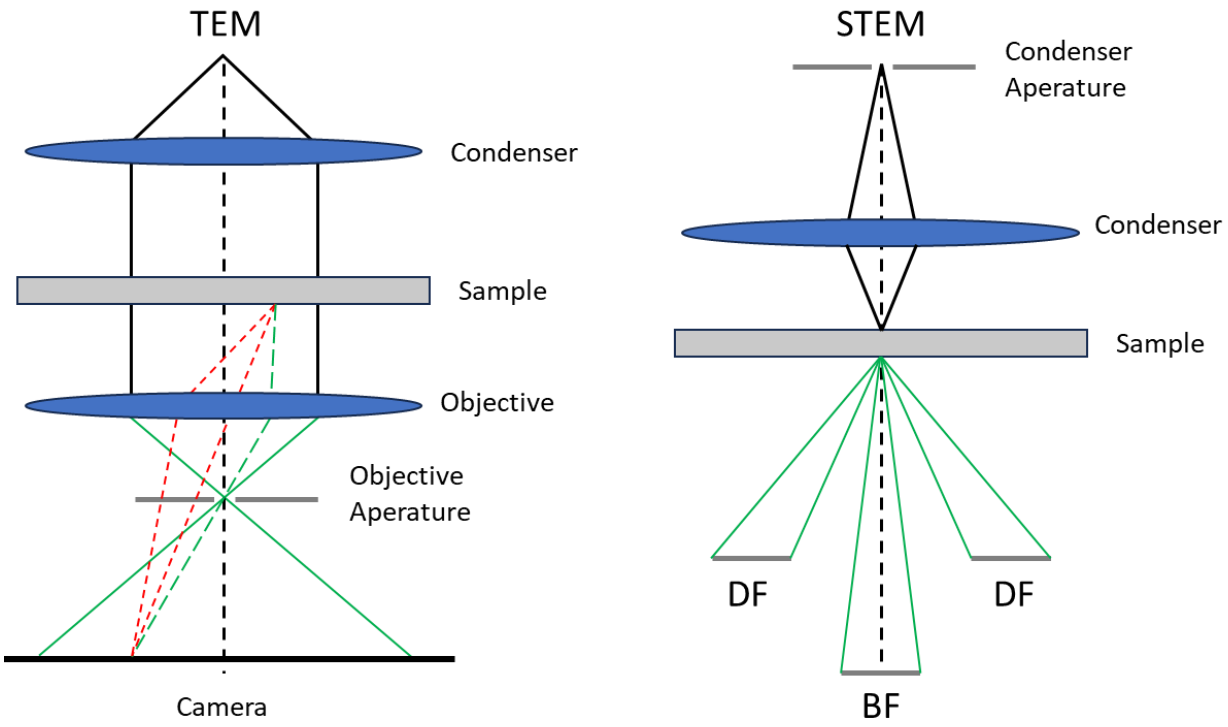

Figure 2.4: Schematic of TEM (left) and STEM (right)

2.3.3 Scanning transmission electron microscopy

Scanning transmission electron microscopy is another configuration of electron microscopy that focuses the beam to a point that is incident on the sample, instead of a parallel beam in conventional TEM. This point is rastered across the sample and the diffracted and transmitted beam are collected. In addition, the detectors are now separated by an angular range such that the undisturbed, transmitted beam is recorded by a bright field (BF) detector, while diffracted or scattered beams due to defects or z-contrast are collected by a dark field (DF) detector at a wider angular range. Adjusting the magnification of the exit beams, also known as the camera length, can allow the user to isolate certain diffracted intensities onto specific detectors for analysis.

2.4 Energy dispersive x-ray spectroscopy

Energy dispersive x-ray spectroscopy (EDX) is a method of chemical analysis achieved by electron bombardment in a sample. This technique can be done in scanning electron microscope as well as transmission electron microscopes. Due to the interaction volume of electrons a bulk materials, transmission of electrons through a thin foil in TEM allows for a smaller interaction volume. The smaller interaction volume results in higher resolution chemical analysis. Generation of characteristic x-rays of a material goes as such: 1) an electron beam displaces a core shell electron in a material, 2) a higher energy level electron relaxes into the vacated core shell energy level and emits an x-ray with discrete energy equal to the difference in energy levels, 3) the x-ray generated is a unique characteristic to each individual element and can be used to identify the material. See Figure 2.5 for a schematic of the principle of EDX.

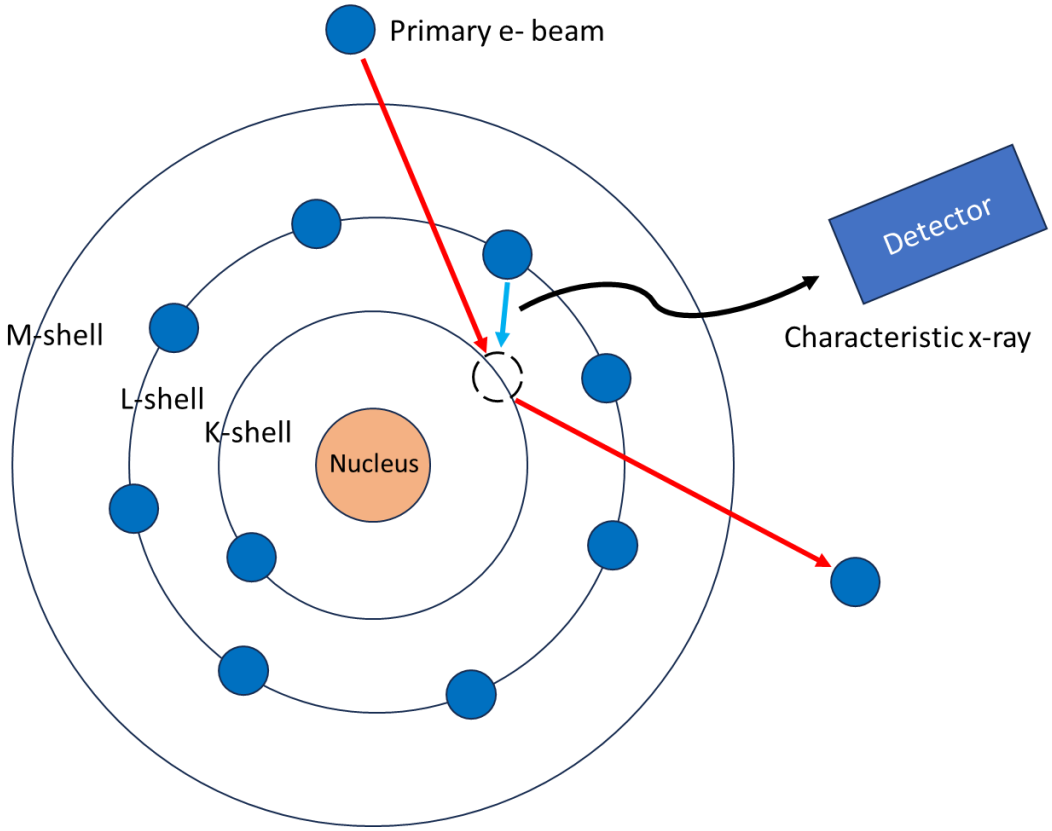

Figure 2.5: Schematic of the basic principle of EDX

Chapter 3: Recovery of thermal conductivity after recrystallization of amorphous silicon

3.1 Motivation

This chapter details a case study of the recovery of thermal conductivity in semiconductors that undergo amorphization due to ion implantation. Understanding this process is an important part of engineering wafer bonded interfaces that are subjected to ion bombardment to sputter off unwanted oxides prior to bonding. As mentioned in chapter 1, depending on the implant energy and species, this ion bombardment treatment may lead to the amorphization of some semiconductor surfaces on the order of nanometers. Bonding these amorphized surfaces will alter the interfacial transport properties at the bonded interface so understanding the recrystallization process and thermal conductivity can be recovered is an important step to post bonding interface engineering.

The effects of ion implantation on the microstructure of silicon[1-3] have been studied but relatively few publications bridged the connection between thermal transport in ion implanted silicon and its microstructure.[4-6] Those studies hypothesized that strain (regardless of defect type) has detrimental effects on thermal conductivity, while Scott et al. have suggested that the reduction in thermal conductivity can be tracked by the damage profile (displacements per atom) based on ion species, dose, implant energy.[7] Many earlier thermal studies of implanted silicon lacked detailed structural characterization to further support these hypotheses.

Ion implantation is known to cause distortions to the host lattice by introducing point defects, extended defects, and amorphization depending on the implant energy, temperature, dose, dose rate, and materials system. For heavier implanted species in silicon, it has been simulated[8,9] and experimentally observed[10-12] that small amorphous domains can form from single cascade events, creating a heterogeneous distribution of crystalline and amorphous domains near the implant projected range. This is unlike lighter implant species that have been shown to require multiple cascade events to eventually form a homogenous amorphous band of damage if the dose is sufficiently high.[13,14] From a thermal perspective, a mixture of amorphous domains and strained crystalline regions via ion implantation will add additional thermal resistance. We show that strain from point defects and the inclusion of the nanoscale amorphous pockets have detrimental effect on the thermal conductivity but can be fully recovered through annealing. For this study, silicon wafers implanted with Kr are investigated. Recovery of silicon thermal conductivity is achieved after recrystallization of partially amorphized silicon implanted with Kr ions and x-ray and electron microscopy characterization is performed to complement the thermal results.

The implant conditions used in this study generate an amorphous region in silicon with a non-uniform distribution of defects and a shallow implant range (~300 nm). This implanted structure has necessitated a finer assessment of thermal conductivity with depth in order to resolve the non-uniform distribution of defects. A mixture of nanocrystalline and amorphous regions exist in the damaged layer, which would not suggest homogeneous thermal conductivity within this region. In this study we utilize quantitative structural analysis to better understand how the thermal conductivity of silicon is modified with both strained and amorphous regions and how the thermal conductivity of these regions changes with subsequent annealing. In

particular, a novel, depth dependent thermal conductivity technique is used to better connect the distribution of defects with variations in thermal conductivity with finer depth resolution.

3.2 Experimental Methods

(001) silicon was implanted with 500 keV Kr ions at a dose of $1x10^{14}$ ions cm^{-2}. Bombardment was performed using a 3 MeV Pelletron implanter and performed at a few degrees from the surface normal. Sample #1 represents the as-implanted conditions. Sample #2 was annealed at 450 °C for 30 min in ambient air. Sample #3 was annealed at 700 °C for 30 min in ambient air. An FEI Nova 600 Nanolab Dual Beam SEM/FIB was used to prepare cross section TEM samples roughly 100 nm thick using a Ga source and transferred to a TEM grid using a standard lift out procedure. High resolution transmission electron microscopy (HRTEM) images were taken using an FEI Titan and double tilt stage at 300 kV to study the crystallinity and defect structure evolution at each annealing stage. Triple axis x-ray measurements used a Bruker D1 diffractometer with an incident beam mirror producing a parallel beam and a Si (220) channel cut collimator (Cu $k\alpha_1$ radiation). The scattered beam optics include a Si (220) channel cut crystal. Bruker RADS software[15] was used to fit and model experimental measurements to quantitatively analyze strain due to implantation. The Stopping Ranges of Ions in Matter (SRIM) software[16] was used to simulate and predict ion distributions and vacancy concentrations after implantation.

Thermal measurements were performed via Time Domain Thermoreflectance (TDTR). TDTR is an optical pump-probe technique wherein a pulsed laser is used to heat the sample surface (pump), and subsequently measure the changes in reflectivity (probe), which is indicative of the temperature rise. By changing the time delay between the arrival of pump and probe pulses, the temperature decay can be found, and an analytical thermal model is then used to fit for unknown thermal properties. This technique also requires the deposition of a thin metal film

which limits the optical penetration (heating) of the pump to the surface and provides an optically reflective surface for the probe. Our TDTR system is comprised of an 800 nm wavelength Ti:Sapphire laser pulsed at 80 MHz. The pump beam is modulated at frequencies between 2-8.4 MHz, which allows lock-in detection of the probe and sensitivity to thermal properties at varying depths based on frequency. We use an 80 nm aluminum transducer, deposited via e-beam evaporation following ion irradiation. The surface of the silicon is washed prior to aluminum deposition, using methanol, acetone, isopropyl alcohol, and O_2 plasma cleaned for 30 minutes, which ensures a strong bond between the aluminum and substrate is obtained.

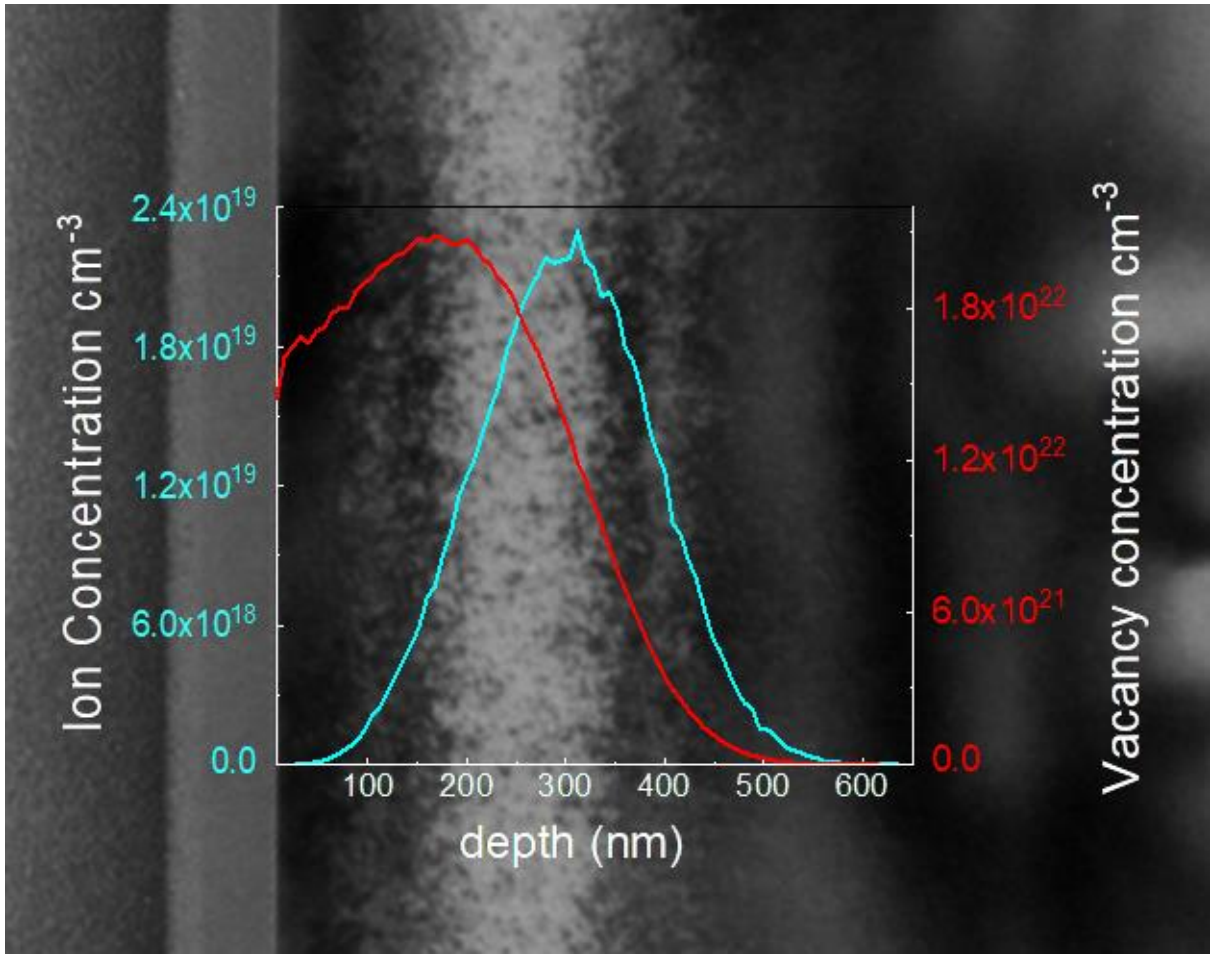

Figure 3.1: SRIM profiles simulating the ion and vacancy distributions, which are overlayed on to the as-implanted BFTEM image.

3.3 Results and Discussion

SRIM simulations predict a peak ion concentration of 4.5×10^{18} cm^{-3} at ~310 nm from the surface and a peak vacancy concentration due to displacements at a depth of 180 nm. This projected range compares well to TEM imaging in the as-implanted sample as seen in Figure 3.1. TEM of the as-implanted silicon sample reveals a structurally distorted band that begins roughly 150 nm below the surface and is 240 nm wide. Close inspection throughout the distorted region

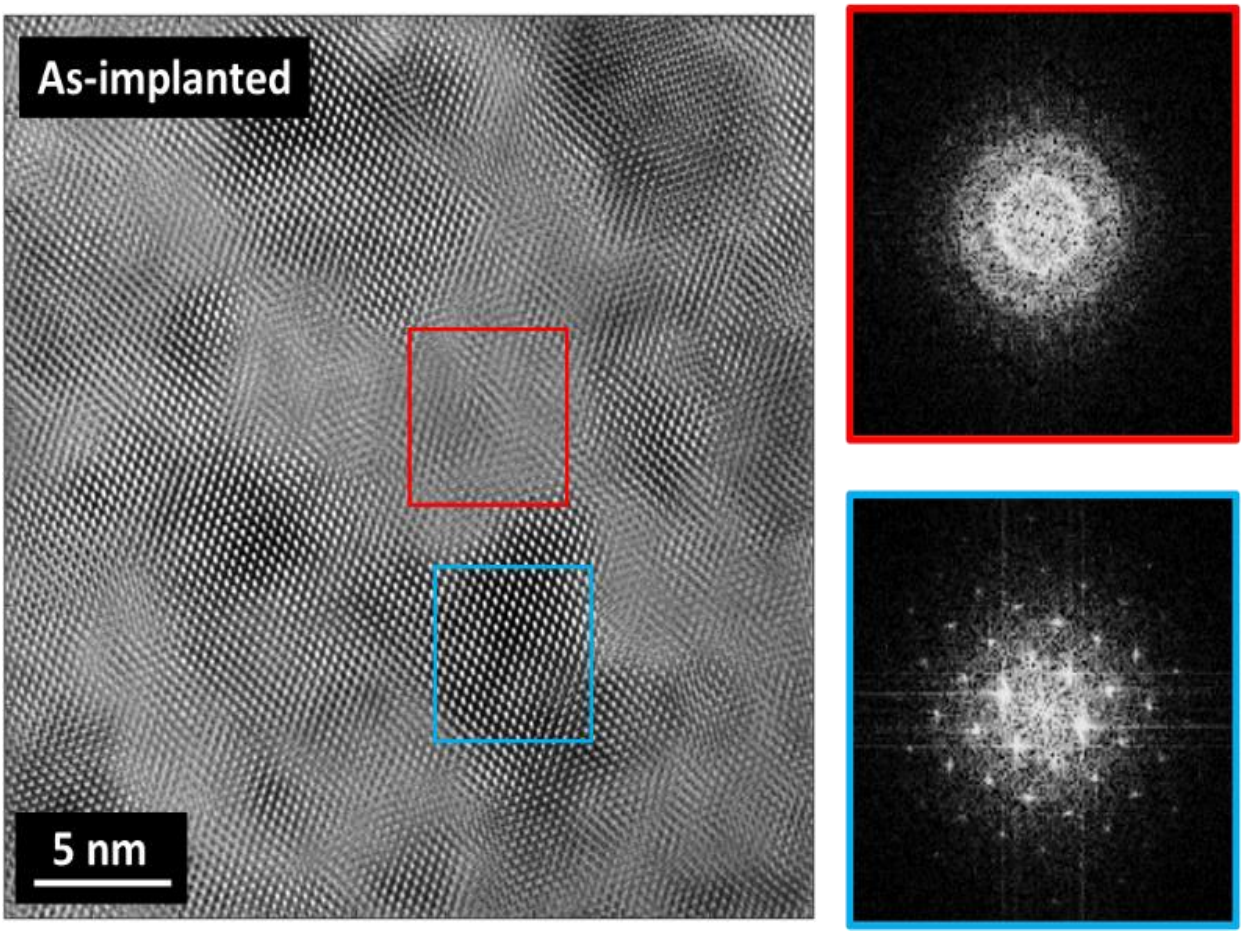

Figure 3.2: Filtered HRTEM image of the as-implanted sample near the peak of damage due to implantation. Nanoscale sized domains (5 – 10 nm in diameter) are distributed throughout the distorted band parallel to the surface of the sample. FFT's of these regions provide evidence of crystalline and amorphous structure.

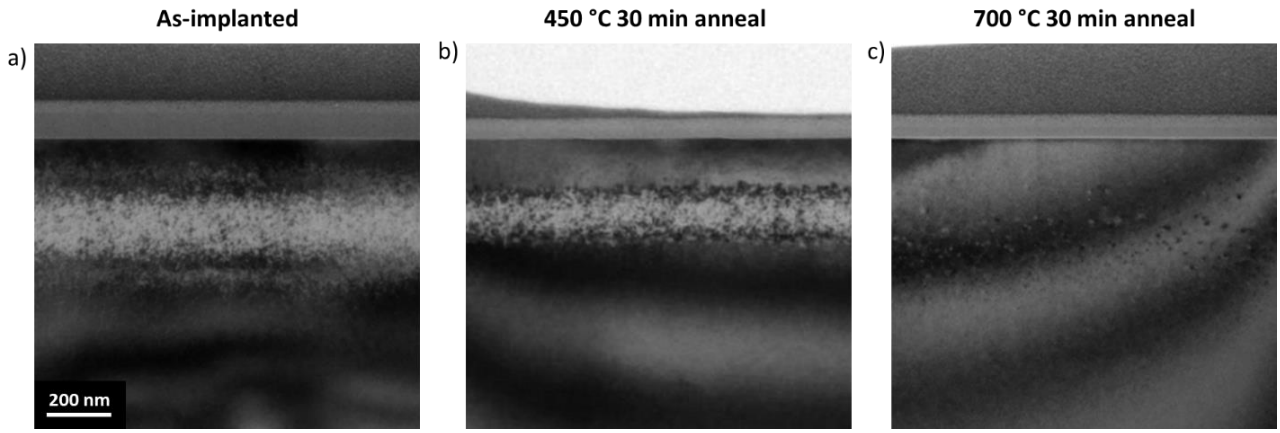

Figure 3.3: BFTEM image for the a) as-implanted b) 450 °C 30 min and c) 700 °C 30 min annealed samples. Comparison of a) and b) reveal the beginning of recrystallization as the thickness of the distorted region shrinks. After complete recrystallization seen in c) extended defects are left distributed near the projected range of implant.

shows pockets of amorphous silicon domains that range from 5 - 10 nm in diameter embedded in the crystalline silicon lattice. This observation is supported by localized Fast Fourier Transforms that reveal diffuse rings in the amorphous regions and well defined diffraction patterns in the crystalline regions shown in Figure 3.2. Amorphous domains in the as-implanted sample make up roughly 53% of the area in the distorted band as estimated from bright field TEM images, where amorphous regions do not strongly diffract the direct beam and therefore appear brighter than their crystalline counterparts.

After annealing at 450 °C for 30 mins, partial recrystallization is observed as the thickness of the distorted band shrinks roughly 60 nm (to ~180 nm thickness) from the bottom amorphous-crystalline interface. Recrystallization via solid phase epitaxy occurs at the crystalline boundary beyond the projected range rather than from both sides of the distorted band. This is comparing the distorted layer thickness in Figure 3.3a and Figure 3.3b.

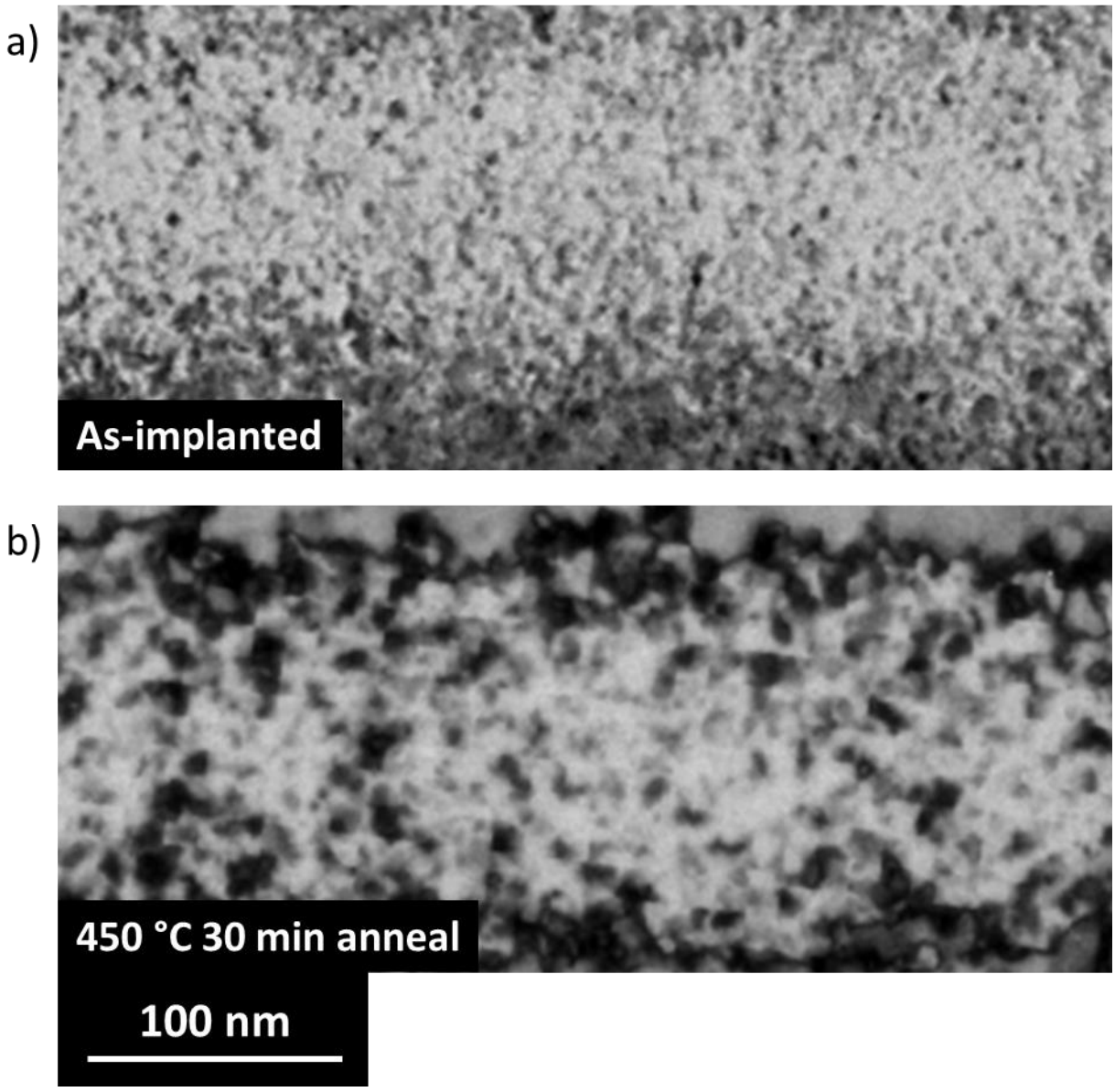

Figure 3.4: Higher magnification BFTEM of the a) as-implanted and b) 450 °C 30 min annealed sample. Comparison of the two show a decrease in the total fraction of amorphous regions from 53% to 34% after the first annealing step.

Additionally, recrystallization also occurs within the distorted band itself, and originates at the crystalline domains as solid phase epitaxy as well. This is evidenced by larger crystalline domains with diameters of 4.8 ± 1.5 nm (as implanted) and 12 ± 5.4 nm (450 °C) and a reduction

in the fraction of total amorphous area from 53% to 34% as shown in Figure 3.4. Complete recrystallization occurred after annealing at 700 °C for 30 min as shown by selective area diffraction measurements throughout the sample that revealed sharp diffraction spots. However, extended defects were present and concentrated near the projected range with a density of 6.25×10^{15} cm^{-3}.

Triple axis ω:2θ x-ray scans were taken to assess lattice strain after implantation and after each annealing step. Figure 3.5 compares the symmetric (004) Si ω:2θ line scans of the as-implanted, 450 °C 30 min, and 700 °C 30 min samples. In the as-implanted sample, well defined strain fringes towards lower angular values indicate out of plane tensile strain. After each

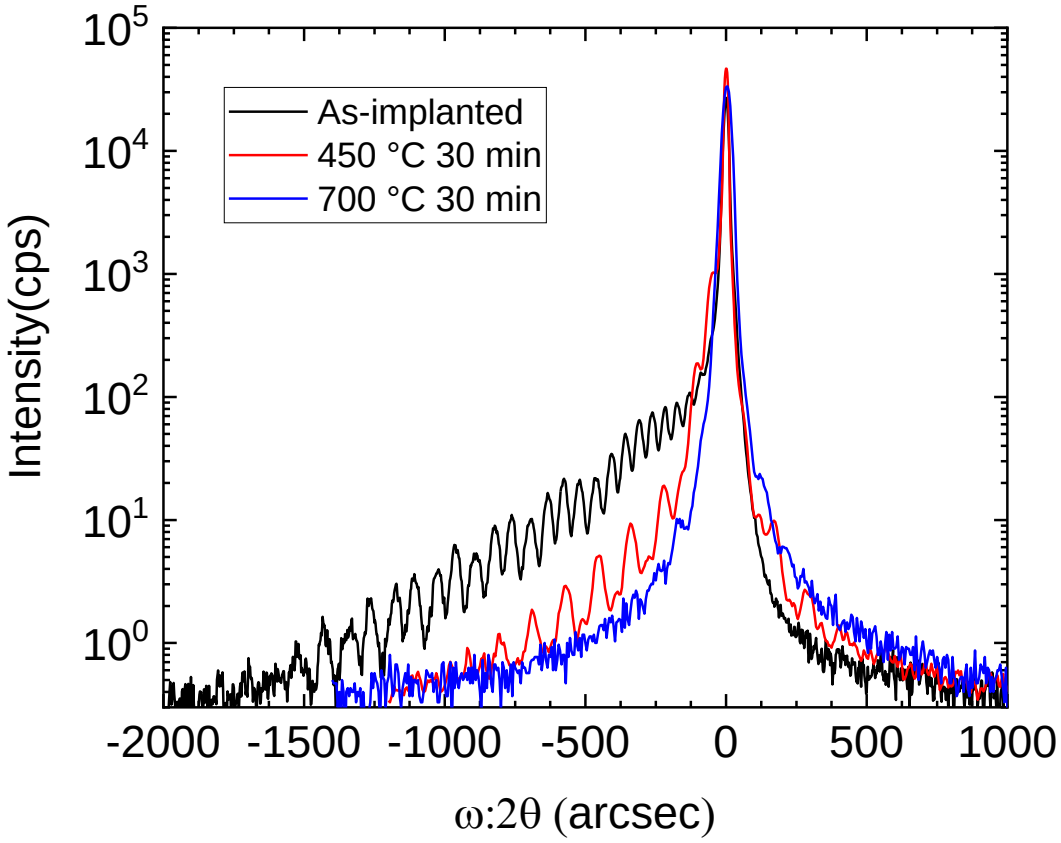

Figure 3.5: Triple axis diffraction ω:2θ (004) Si line scans show a reduction in strain fringes after each progressive annealing step.

progressive annealing condition, the shoulder recedes toward the main peak indicating strain reduction. For in-depth strain analysis, x-ray dynamical simulations using Bruker RADS software provide quantitative information about the strain-inducing implant species and the elastic deformation of the lattice after implantation. The simulation process is very similar to our earlier implantation studies.[17-24] However, in order to account for the presence of amorphous domains in the as-implanted sample and the 450 °C annealed sample, we created a quasi-Si structure by modifying the scattering factor for the amorphous regions. Because TEM showed complete recrystallization at 700 °C, a regular Si model is used in the fitting for that case. A strong fit between the simulated and the experimental ω:2θ scans were observed for all three samples, suggesting that the modified structures successfully mimic the lattice disorder in the real samples. Figure 3.6 shows the comparison between the simulated fits in each case. 60% of

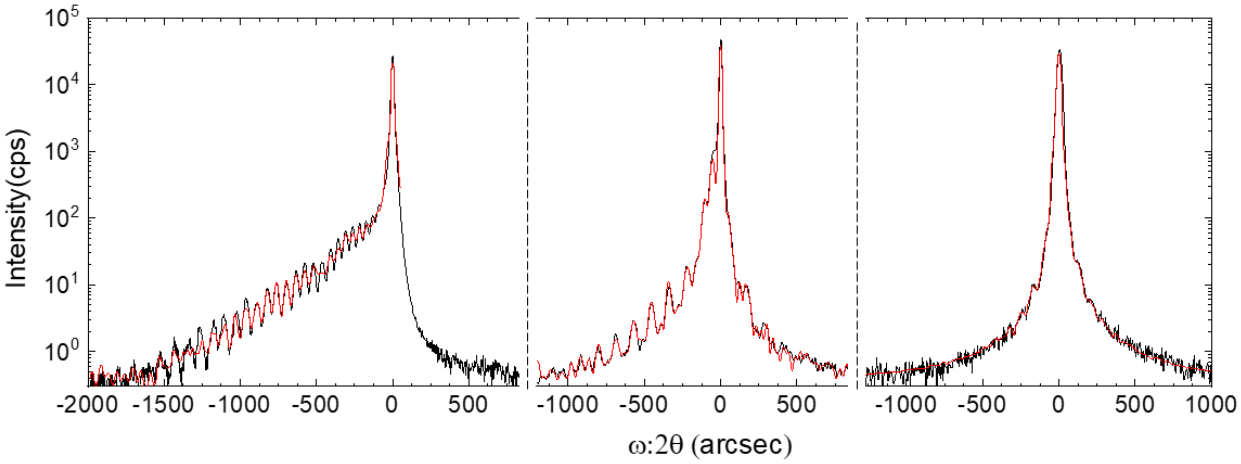

Figure 3.6: RADS fitting overlayed on experimental ω:2θ scans. To account for the presence of amorphous domains in the as-implanted sample and the 450 °C annealed sample, a quasi-Si structure was made by replacing part of the Si atoms on the lattice with H atoms. Since TEM showed complete recrystallization at 700 °C, a regular Si model is used in the fitting. Peak strain of the as-implanted (left), 450 °C (middle), and 700 °C (right) samples are 4300, 1700, and 110 ppm respectively.

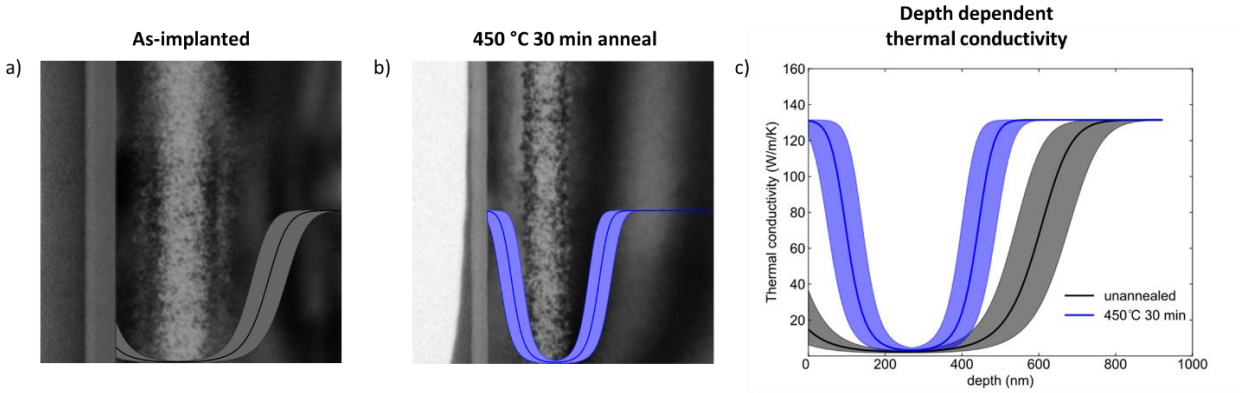

Figure 3.7. Depth dependent thermal conductivity measurements overlaid on the BFTEM images reveal how the thermal conductivity is recovered as the distorted band shrinks and as strain is relieved. The solid line represents the nominal best fit, and the shaded region represents the uncertainty corresponding to fitted functions yielding 2.5% residual.

the strain is recovered after annealing at 450 °C for 30 min and over 97% of the point-defect induced strain is recovered after annealing at 700 °C for 30 min.

In contrast to thermal metrology techniques that assume uniform material properties, modifications have been made to the Time Domain Thermal Reflectance analysis, which has allowed the measurement of thermal conductivity as a function of depth with non-uniform defect distribution. This is useful for understanding the effects of ion implantation where regions of amorphous and strained crystalline domains are observed as a function of depth in silicon. Spatially varying time domain thermoreflectance measurements as a function of depth shown in Figure 3.7 measure a minimum thermal conductivity of 2.5 ± 0.7 $W \cdot m^{-1}K^{-1}$ at 250 ± 20 nm in the as implanted sample, 3.2 ± 0.8 $W \cdot m^{-1}K^{-1}$ at 270 ± 20 nm in the sample annealed at 450 °C, and fully recovered thermal conductivity within error of bulk silicon (130 $W \cdot m^{-1}K^{-1}$) in the fully recrystallized sample annealed at 700 °C. In addition, the depth dependent thermal conductivity

mimics the structural changes seen in TEM, where the low thermal conductivity region shrinks alongside the decrease in the distorted region layer thickness after the annealing at 450 °C.

The critical dose of amorphization of silicon can be estimated as function of the ion beam energy, straggle (from SRIM), atomic density and displacement energy of Si.[29] For our system the critical dose is calculated to be ~6.5×10^{13} ions·cm^{-2}, slightly below the 10^{14} ions·cm^{-2} dose used in this experiment. For heavy ion implants, amorphous pockets have been observed to form from single cascade events, even below the critical dose.[8,10-14] The experimental parameters set here approach a regime where the amorphous pockets become so dense that they nearly form a homogenous amorphous layer. Instead, nanoscale domains of amorphous and crystalline material are distributed throughout the distorted band in the as-implanted sample. This phenomenon has been observed before when the implanted dose approached the estimated critical dose of amorphization.[30]

From a thermal perspective, previous studies showed that the strain caused by point defects was found to be the dominating contributor to the reduction in thermal conductivity in ion implanted semiconductors.[5,7] Our findings agree with these results, and we show that after annealing at 450 °C for 30 min the strain has sufficiently recovered near the edges of the distorted region and improvements in the thermal conductivity are observed. However, even after a 60% reduction in the peak strain, the minimum thermal conductivity measured remains the same as the as-implanted sample. To our knowledge no studies have recorded the evolution of strain and thermal conductivity with annealing, only the initial and final stages of pre-anneal and full recrystallization.[7] However, in a similar study, Scott et al. implanted Si with $^{28}Si^{+}$ at various incremental doses, which mimic gradually increasing strain states in silicon.[5] In their study, they observed a monotonically decreasing thermal conductivity from 110 W·m^{-1}K^{-1} to 40 W·m^{-1}K^{-1}

with increasing dose from 6.23×10^{13} to 6.24×10^{16} ions·cm^{-2} respectively. As seen in our 450 °C 30 min anneal case, there remains sufficient distortion in the crystal to maintain the low value of thermal conductivity in the distorted region but recovery of the thermal conductivity in the epitaxially regrown regions. Boundary scattering between amorphous and crystalline regions was hypothesized to be dominant in explaining the low thermal conductivity in the unannealed case, and this effect may also explain the similar maximum reduction in thermal conductivity in the 450 °C anneal case. After complete recrystallization when annealing at 700 °C for 30 min, the measured thermal conductivity is fully recovered and matches un-irradiated silicon within uncertainty. Dislocation loops do form near the projected range during the recrystallization process as a result of the agglomeration of point defects that reduces the strain, a process that has been systematically studied previously.[2] This matches well with our x-ray measurements and simulations that shows complete strain reduction in the layer and over 97% reduction in the region that had been most highly strained. The presence of the dislocation loops in these materials apparently does not have a measurable deleterious impact on the thermal conductivity as the conductivity is uniform as a function of depth in that case.

3.4 Conclusion

We have demonstrated complete recovery of thermal conductivity in partially amorphized Si implanted with 10^{14} Kr ions cm^{-2} at 500 keV. Quantitative structural analysis is performed for an as-implanted, 450 °C 30 min anneal, and 700 °C 30 min anneal, which shows strain reduction at each progressive annealing step. Comparison of the high resolution TEM of the as-implanted and 450 °C sample reveals progress towards recrystallization, where the area fraction of the amorphous domains is reduced from 53% to 34% within the distorted band. In addition, recrystallization occurs at bottom amorphous-crystalline interface where we observe shrinkage of

the distorted band. Depth dependent thermal conductivity measurements mimic these structural changes where the low thermal conductivity region shrinks as strain is relieved. Finally, when complete recrystallization occurs, in addition to point defects returning to lattice sites, extended defects are formed during the recovery process to reduce the overall strain in the crystal, as evidenced by our x-ray scattering measurements. After the 700 °C anneal, the thermal conductivity is fully recovered and is uniform throughout the depth of the layer. The 450 °C annealing condition prior to full recrystallization of the distorted region reveals that the thermal conductivity progressively recovers after the removal of the amorphous pockets and after reduction in the point-defect induced strain. While the peak strain is reduced by over 60%, the minimum thermal conductivity within the center of the distorted region remains unchanged. This suggests that that the nanoscale amorphous regions dominate the reduction in thermal conductivity prior to complete recovery and demonstrate the potential for the recently developed depth dependent thermal measurements.

3.5 References

[1]J. L. Benton, S. Libertino, P. Kringho/j, D. J. Eaglesham, J. M. Poate, and S. Coffa, Journal of applied physics 82(1), 120 (1997).

[2]K.S. Jones, S. Prussin, and E. R. Weber, Applied Physics A 45(1), 1 (1988).

[3]L. Pelaz, L. A. Marqués, J. Barbolla, Journal of Applied Physics 96(11), 5947 (2004).

[4]M. Khafizov, C. Yablinsky, T.R. Allen, and D. H. Hurley, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 325, 11 (2014).

[5]E. A. Scott, K. Hattar, C. M. Rost, J. T. Gaskins, M. Fazli, C. Ganski, C. Li, T. Bai, Y. Wang, K. Esfarjani, M. S. Goorsky, P. E. Hopkins, Physical Review Materials 2(9), 095001 (2018).

[6]E. A. Scott, K. Hattar, J. L. Braun, C. M. Rost, J. T. Gaskins, T. Bai, Y. Wang, C. Ganski, M. S. Goorsky, P. E. Hopkins, Carbon 157, 97 (2020).

[7]E. A. Scott, K. Hattar, E. J. Lang, K. Aryana, J. T. Gaskins, and P. E. Hopkins, Physical Review B 104(13), 134306 (2021).

[8]M.J. Caturla, T. D. de La Rubia, L. A. Marques, and G. H. Gilmer, Physical Review B 54(23), 16683 (1996).

[9]H. Hensel, and H. M. Urbassek. Physical Review B 57(8), 4756 (1998).

[10]M. O. Ruault, J. Chaumont, J. M. Penisson, and A. Bourret, Philosophical Magazine A 50(5), 667 (1984).

[11]L. M. Howe, and M. H. Rainville, Nuclear Instruments and Methods 182, 143 (1981).

[12]L. M. Howe, and M. H. Rainville, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms 19, 61 (1987).

[13]L. Pelaz, L. A. Marqués, and J. Barbolla, Journal of applied physics 96(11), 5947 (2004).

[14]F. Priolo, A. Battaglia, R. Nicotra, and E. Rimini, Applied physics letters 57(8), 768 (1990).

[15]RADS Software, Bruker Semiconductor, info.semi@bruker.com

[16]J. F. Ziegler and J. P. Biersack, The Stopping and Range of Ions in Matter (Springer US, Boston, MA, 1985), pp. 93–129.

[17]Y. Wang, T. Bai, C. Li, M. Tadjer, T. Anderson, J. Hite, M. Mastro, C. Eddy, K. Hobart, B. Feigelson, M. S. Goorsky, ECS Journal of Solid State Science and Technology 8, 70 (2019).

[18]Y. Wang, K. Huynh, M. E. Liao, H.-M. Yu, T. Bai, J. Tweedie, M. H. Breckenridge, R. Collazo, Z. Sitar, M. Bockowski, Y. Liu, and M. S. Goorsky, Phys. Status Solidi B 257, 1900705 (2020).

[19]C. Miclaus, and M. S. Goorsky, Journal of Physics D: Applied Physics 36(10A), A177 (2003).

[20]S. T. Horng, and M. S. Goorsky, Applied physics letters 68(11), 1537 (1996).

[21]S. T. Horng, M. S. Goorsky, J. H. Madok, and N. M. Haegel, Journal of applied physics 76(4), 2066 (1994).

[22]I.P. Ferain, K. Y. Byun, C. A. Colinge, S. Brightup, and M. S. Goorsky, Journal of Applied Physics 107(5), 054315 (2010).

[23]M. E. Liao, Y. Wang, T. Bai, and M. S. Goorsky, ECS Journal of Solid State Science and Technology 8.11, 673 (2019).

[24]S. Hayashi, R. Sandhu, and M. S. Goorsky, Journal of the Electrochemical Society 154.4, H293 (2007).

[25]D. G. Cahill, Review of scientific instruments 61(2), 802 (1990).

[26]D. G. Cahill, Review of scientific instruments 75(12), 5119 (2004).

[27]A. J. Schmidt, R. Cheaito, and M. Chiesa, Review of scientific instruments 80(9), 094901 (2009).

[28]J. L. Braun, D. H. Olson, J. T. Gaskins, and P. E. Hopkins, Review of Scientific Instruments, 90(2), 024905 (2019).

[29]S. K. Ghandhi, VLSI fabrication principles: silicon and gallium arsenide. John Wiley & Sons (2008).

[30]J. Narayan, and O. W. Holland, Journal of the Electrochemical Society 131(11), 2651 (1984).

Chapter 4: Interface engineering of wafer bonded Si-Ge

4.1 Motivation

In this chapter, we will discuss wafer bonding and interface engineering of silicon and germanium. The Si-Ge system is used as a fundamental example of heterogeneous integration, which we can use to analyze the intricacies of interface engineering before introducing additional complexities when moving towards compound wide band gap semiconductors. This chapter incorporates knowledge learned in previous chapters regarding surface activated bonding process and the recrystallization and recovery of thermal conductivity in silicon.

Heterogeneous integration of silicon and germanium is a well established and mature technology that we can leverage from. Epitaxial growth of Ge and $Si_{(1-x)}Ge_x$ films on silicon have been used as avalanche photodiodes, heterojunction bipolar transistors, and complementary metal-oxide semiconductors.[1,2] Additionally, wafer bonding is commonly used in fabrication of Si, Ge, and SiGe on insulator devices.[3-5] With epitaxial growth, due to the 4% lattice mismatch between Ge and Si, typical threading dislocation densities of Ge on Si are on the order of 10^6-10^7 cm^{-2}, where engineered buffer layers are used to impede misfit dislocation formation.[6] Direct wafer bonding of Si and Ge can bypass the 4% lattice mismatch between Si and Ge to provide higher quality films and interfaces by overcoming critical thickness constraints and thereby preventing misfit dislocation formation. In addition, since wafer bonding is not affected by lattice mismatch, any in-plane twist between the bonded samples is possible, opening up new heterojunction interfaces that were not possible with just epitaxy.

While wafer bonding presents many advantages for heterogeneous integration, there are many variables that can affect the interfacial properties of the bonded interface. Bond strength,

electrical interfacial resistance, and thermal boundary resistance can be engineered by prebonding surface treatments, wafer alignment, and subsequent post bonding annealing. Although a wide variety in-plane alignments are available when wafer bonding two dissimilar substrates, careful consideration of the effects of twist on the interfacial properties is crucial. The electrical interfacial resistance was found to heavily depend on twist between wafer bonded InP-InP,[7] GaP-InGaP,[8] and InP-GaAs,[9] where a deviation away from perfectly aligned cubic crystals (i.e. $[110]_{InP} \parallel [110]_{InP}$) lead to a minimum electrical interfacial resistance, and a cyclic trend of increasing and decreasing electrical interfacial resistance with increasing misorientation and realignment (as the lattices begin to rotate back to perfect alignment due to symmetry). Additionally, wafer bonded Si-Si homojunctions using the SAB method have shown improved electrical interfacial resistance[10] and thermal boundary conductance[11] when the amorphous interface is annealed and recrystallized.

The effect of twist on the thermal boundary conductance has also been studied but to a lesser extent. In wafer bonded Si-Si homojunctions, the interface was treated as one grain boundary, and twist induced during wafer bonding was associated change in the grain boundary energy.[12] Xu et al., found that the measured thermal boundary resistance seemed to correlate with the interfacial strain energy, and not the total grain boundary energy when twisting the Si-Si homojunction. This trend also showed similar cyclic behavior that was observed in the electrical interfacial resistance studies where twist angles of 0° and 90° minimized the thermal boundary resistance due to the symmetry of Si. However, dislocation strain energy is also found to be minimized at 45°, which has been suggested to be due to overlap in the strain fields of individual dislocations once the density becomes large enough.

Thermal boundary conductance of Si-Ge heterojunctions was found to be less sensitive to the effect of dislocation strain energy compared to the Si-Si homojunction system mentioned previously.[13] This is due to the additional scattering due to the acoustic mismatch in the phonon density of states between Si and Ge. Gurunathan et al., modeled that the strain energy component of the thermal boundary resistance amounted to about 50% of the contribution. So, the twist between heterojunctions still can significantly affect the boundary resistance but not as critically as seen in homojunctions. Additionally, when an amorphous ~3 nm interfacial layer is introduced, twist between the Si-Ge heterojunction was found to have negligible effects on the thermal boundary resistance and the resistance was speculated to be dominated by the amorphous interlayer.[14]

Modeling efforts have also predicted that the TBC at an amorphous Si (a-Si) to amorphous Ge (a-Ge) interface is higher than any of the other crystalline to crystalline or crystalline to amorphous Si and Ge interfaces (c-Si|c-Ge, c-Si|a-Ge, a-Si|c-Ge, and c-Si|c-Ge).[15] While this is a novel finding, experimental evidence is difficult to measure especially since device structures with an a-Si|a-Ge interface likely also involves the c-Si|a-Si and/or the a-Ge|c-Ge interface. While the a-Si|a-Ge TBC may be the highest, potentially adding a phonon bridge of a-Si|a-Ge between c-Si and c-Ge adds additional low thermal conductivity resistance in the form of the amorphous layers. So, in practice, the amorphous layers that create the a-Si|a-Ge interface need to be thin enough to not override the benefit of the increased TBC.

In this study we present a method of producing an a-Si|a-Ge interface between wafer bonded Si-Ge using the surface activated bonded technique. The evolution of the interface is studied by subsequent annealing and recrystallization of the interface and thermal boundary conductance is measured comparing as bonded and fully recrystallized interfaces.

4.2 Experimental Methods

(100) Germanium was bonded to (100) silicon using EVG® ComBond® equipment under high vacuum (~10^{-8} mtorr) and room temperature. This process is similar to other reported surface activated bonding (SAB) or in situ sputtering techniques, in which Ge and Si surfaces are sputtered with an Ar ion beam to remove unwanted native surface oxides prior to bonding.[0,**Error! Reference source not found.**] The post Ar-beam treated samples are placed face-to-face and pressure is applied to initiate the bond. After bonding the samples were cleaved into 1 x 1 cm^2 pieces and annealed at 600 °C for 2 hours and 600 °C for 48 hours in an N_2 ambient to investigate the stability and evolution of the interface. The samples are labeled as Sample_RT, Sample_600.2, and Sample_600.48 referring to the room temperature, 600 °C 2 hour, and 600 °C 48 hour annealing conditions.

Structural characterization was conducted electron microscopy techniques including high resolution scanning transmission electron microscopy (STEM) and energy dispersive x-ray spectroscopy (EDX). An FEI Nova 600 Nanolab Dual Beam SEM/FIB was used to prepare cross section TEM samples roughly 100 nm thick using a Ga source and transferred to a TEM grid using a standard lift out procedure. High resolution transmission electron microscopy (HRSTEM) and energy dispersive x-ray spectroscopy (EDX) of the interface were taken with a Cs-corrected JEOL GrandARM at 300 kV.

4.3 Results and Discussion

High angle annular dark field (HAADF) STEM images were taken to compare the interfacial changes of the bonded Si-Ge samples with annealing time. As observed in many other annealing studies of wafer bonded samples subjected to SAB bonding techniques, the amorphous layer thickness decreases with increasing annealing time.[10,11,16,17]Figure 4.1 shows the changes in

the amorphous layer thickness with annealing after 2 hours and 48 hours, where there is a 1.2 nm amorphous region in Sample_RT. The amorphous layer is reduced to 0.9 nm in Sample_600.2 and finally for Sample_600.48 we consider the <0.5 nm interface to be fully recrystallized. It can be seen that the atomic stacking of the Si compared to the Ge is clearly along a different orientation. We verify that the misorientation between the two wafers is ~45° twisted in-plane, based on orientation of the wafers when the bond was initiated. Figure 2 shows the FFT within the Si and Ge lattices that reveals the 45° twist between the $[110]_{Si}$ || $[100]_{Ge}$ zone axes. We will discuss the potential impacts of this misorientation on the thermal boundary conductance later in the chapter.

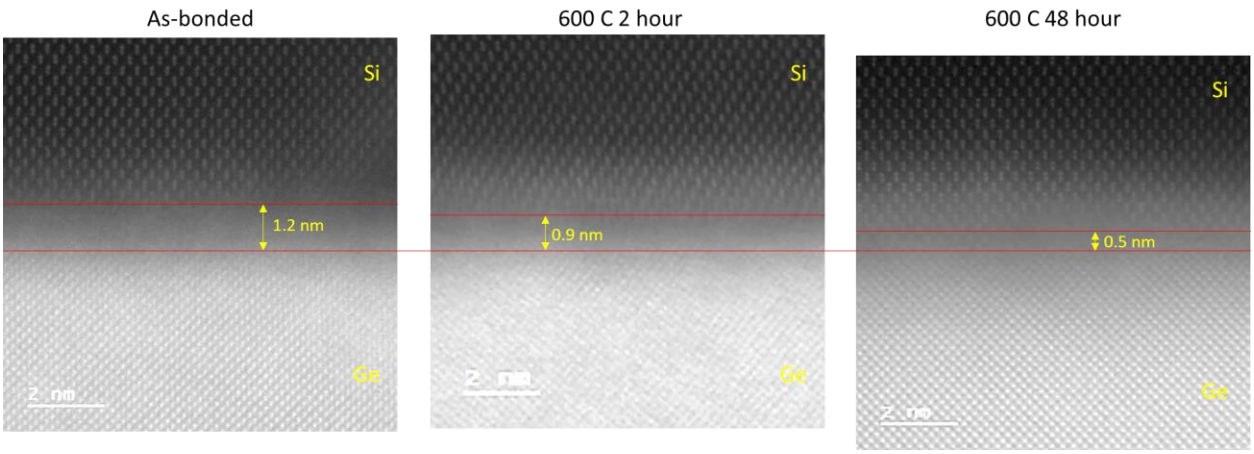

Figure 4.1: HRSTEM images comparing the amorphous interface after subsequent annealing at 600 C for 2 hours and 600 C for 48 hours.

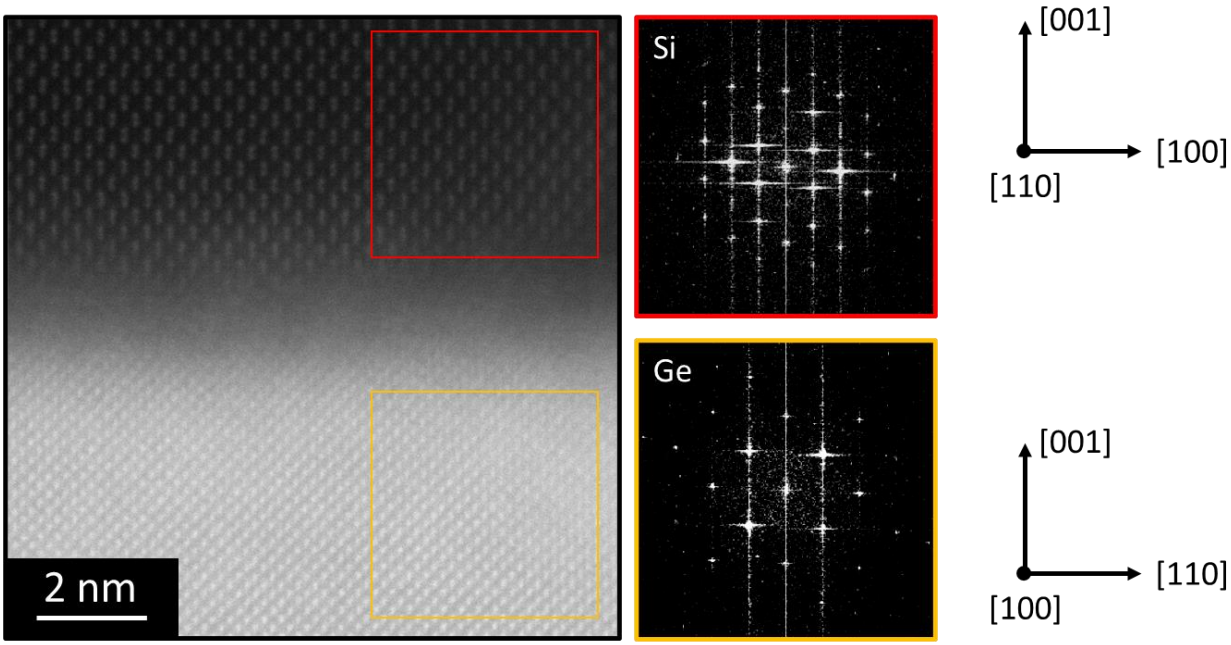

Figure 4.2: Fourier transform within the Si and Ge regions, which verify a 45° twist between the $[110]_{Si}$ || $[100]_{Ge}$ zone axes.

High resolution EDX maps were taken across the Si-Ge interface to measure the amount of interdiffusion caused by annealing, as a result of recrystallizing the interface. First we observe the Ar that is present at the bonded interface due to the Ar sputtering surface treatment used to clean the surface of the sample prior to initiating bonding. The Ar concentration at the interface is measured at 4 at% in Sample_RT, which is reduced to 3 at % in Sample_600.2, and finally 2 at% in Sample_600.48. The interdiffusion between Si and Ge can be more easily seen in Figure 4.4, which is a plot of the extracted EDX line scans. For our analysis and comparisons, the amount of intermixing is defined as the thickness from the interface where the Si/Ge concentrations are ~80/20. In theory, Sample_RT, which has not experienced any annealing, should show a sharp Si-Ge interface, and the curve that we measure is based on the 1 nm spot size limitations of the EDX measurement. Using the as-bonded line scans as a reference, we

observe a small but non-negligible increase in intermixing (~0.5 nm) that occurs after annealing at 600 °C for 2 hours, which increases to 1.7 nm for Sample_600.48.

Thermal boundary conductance at Si-Ge interfaces has been shown theoretically[#] and experimentally[#] to improve by introducing nanoscale amounts of intermixing at the interface. Modeling efforts have observed that TBC between two dissimilar materials can actually increase when intermixing is introduced in comparison to a sharp interface.[18] This work suggests that this

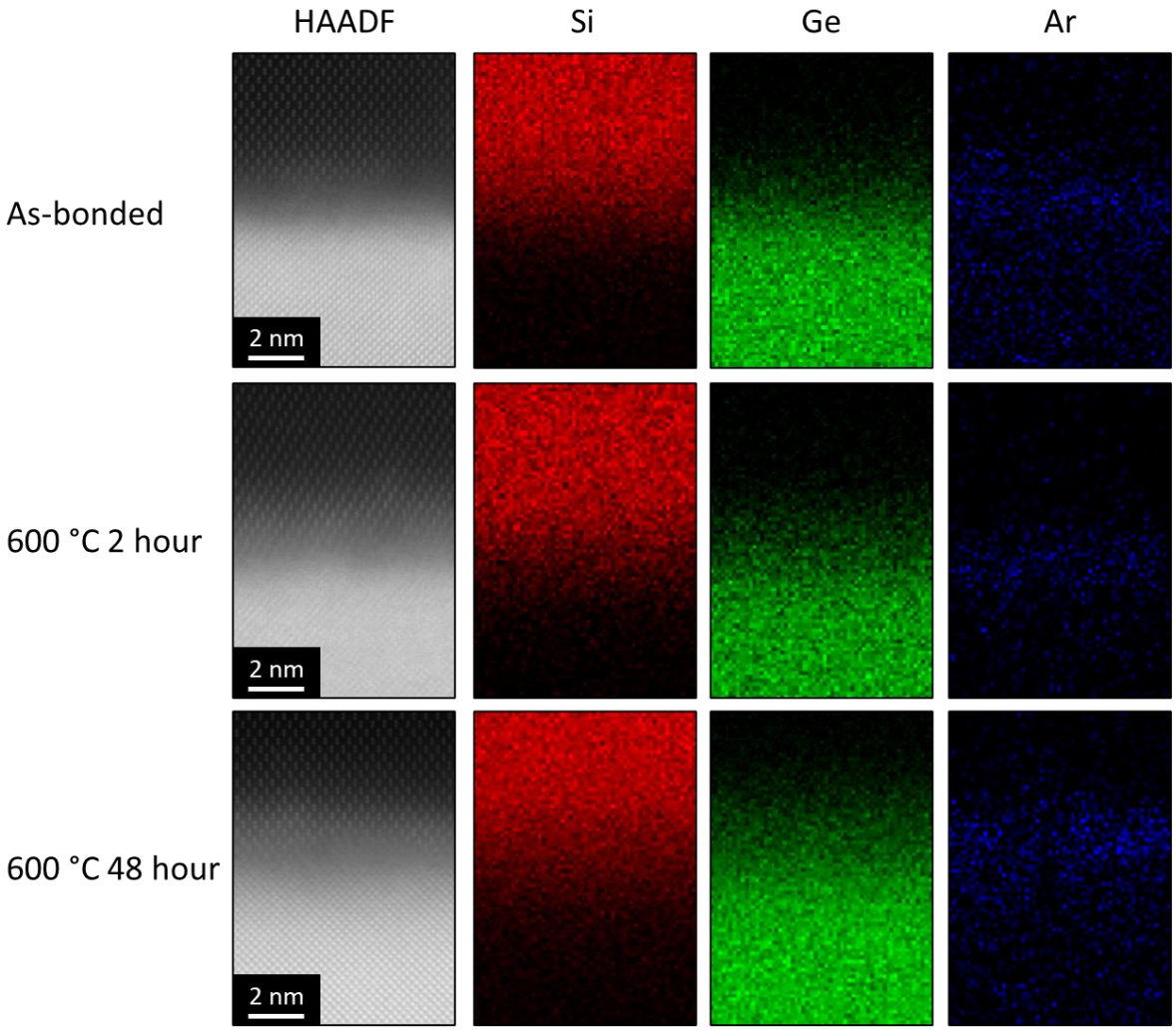

Figure 4.3: Energy dispersive x-ray spectroscopy at the bonded interface for the as bonded, 600 °C 2 hour, and 600 °C 48 hour annealed samples.

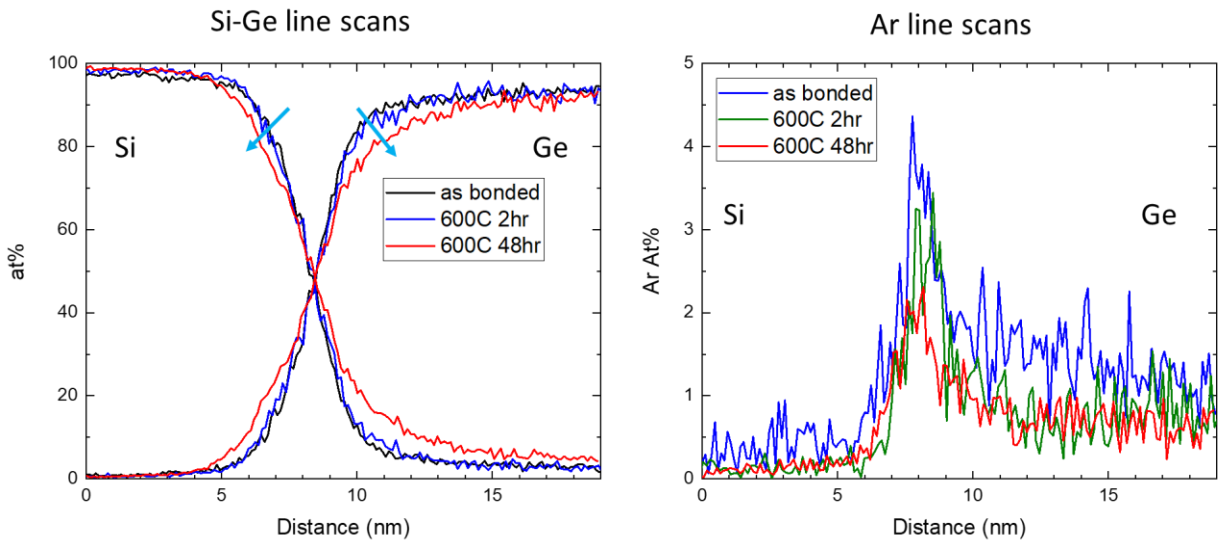

Figure 4.4: Energy dispersive x-ray spectroscopy line scans across the bonded interface for the as bonded, 600 °C 2 hour, and 600 °C 48 hour annealed samples.

phenomenon is more effective when the acoustic mismatch between the two materials is larger because additional scattering near the interface can soften the abrupt change at the interface. More recently, this effect was experimentally observed in epitaxially grown Si on Ge when ~0.7 nm of intermixing between Si and Ge increased TBC and resulted in additional phonon modes that were measured under vibrational EELS.[19] Figure 4.5 is a comparison between reported simulated and experimental TBC values of epitaxially grown Si-Ge compared to the TBC values measured in this study for wafer bonded Si-Ge (Sample_RT and Sample_600.48).

Immediately we observe that the overall TBC of both Sample_RT and Sample_600.48 are at least a factor of 2 lower than the epitaxial Si-Ge measurements. The TBC of Sample_RT was measured at 47 ± 5 MW/(m^2·K) and increased by a factor of two to 95 ± 5 MW/(m^2·K) after the 600 °C 48 hour anneal, in which the recrystallization of the interface was achieved. We speculate that there are several reasons that may explain the overall difference between the epi Si-Ge and

wafer bonded measurements, which include sample twist, intermixing, and the concentration of argon at the interface.

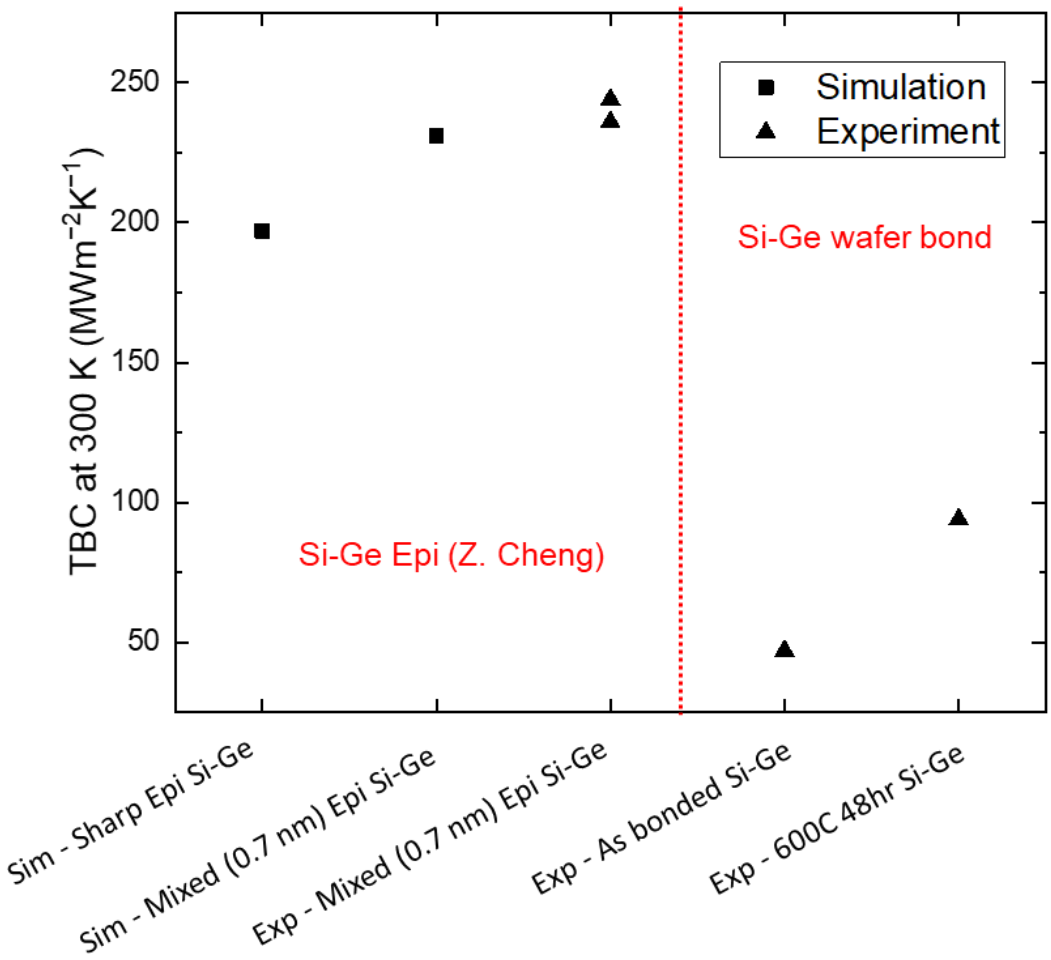

Figure 4.5: Thermal boundary conductance simulations (Sim) and experimental (Exp) measurements of epitaxially grown Si-Ge published in Cheng et al., compared to the wafer bonded Si-Ge with 45° in-plane twist in this work.

First we discuss the effect of intermixing and the presence of an amorphous interlayer on TBC. Increases in TBC due to intermixing in Si on Ge epitaxy had experimentally shown at most a 19% (47 MW/m^{2}K) increase in TBC when ~0.7 nm of interface mixing was introduced, which is coincidentally very close to the exact numerical increase in TBC between Sample_RT and

Sample.600.48 when 1.7 nm intermixing is introduced. However, there is also the fact that the amorphous interlayer is completely recrystallized. In a similar study of bonded Si-Ge (without Ar sputtering) with a 3 nm amorphous Si-Ge intermixed layer, Wang et al., reports a very low TBC of 3 MW/m^2K, which they attribute to the thick amorphous interlayer. On one hand, it has been theorized that the a-Si|a-Ge interface shows improved TBC over the other crystalline and amorphous interface combinations, but including an a-Si|a-Ge interface between c-Si and c-Ge additionally generates two more interfaces. So while we do see improvement in the TBC post anneal when removing the a-Si|a-Ge interface (which may contradict the theory), we acknowledge that the improvement observed from intermixing, removing the amorphous interlayer, and reducing the number of interfaces likely overshadows the possible increase in TBC from the a-Si|a-Ge interface.

Next we discuss the effect of twist on TBC. As mentioned previously, the wafer bonded samples studied here are subject to a 45° twist such that the [110]Si || [100]Ge. In modeling efforts, a wafer bonded interface is treated as a large grain boundary, where the grain boundary itself is described as an array of dislocations.[20] When introducing twist at a grain boundary, the total grain boundary energy γ_{GB} can be described as $\gamma_{core} + \gamma_{strain}$. γ_{core} describes the energy due to broken bonds while γ_{strain} is the elastic strain due to the dislocations. Xu et al. and Guranathan et al., both report that the effect of twist on TBC in Si-Si and Si-Ge is correlated to γ_{strain} and not the total grain boundary energy or γ_{core} of the interface. While the γ_{core} for a grain boundary between two cubic materials follows a cyclic trend minimized at 0° and 90° and maximized at 45° misorientation, the γ_{strain} of the boundary (which correlates to TBC), is actually minimized at 45°.[21] While the density of dislocations increases with increasing twist up to 45°, the γ_{strain} is

maximized between 10° - 15° (and again at 75° - 80° based on symmetry) but the overlapping strain fields minimize γ_{strain} at 45° twist. Additionally, when an amorphous Si-Ge interlayer (~3 nm) is present between Si and Ge, Wang et al. found that twist misorientation had negligible impact on the TBC.[14#] Their result may suggest that Sample_RT in this study is not influenced by the twist regardless, but for both of these reasons, it is speculated that the 45° twist involved in the wafer bonded samples is not the cause for the decrease in the TBC as compared to the Si-Ge epitaxially grown layers.

Lastly we discuss the presence of Ar ions at the interface and the potential effects on TBC. Like intermixing and twist misorientation, the effects on TBC are heavily dependent on the materials involved and their acoustic mismatch. For Si-Ge we have seen that intermixing can have beneficial impacts on TBC but the same concept showed negative impacts on TBC in the Cr-Si system.[22] Similarly, for ion irradiation at interfaces, there are reports of positive and negative effects on TBC for different materials systems. In an Al/native oxide/Si interface, TBC was improved through proton irradiation prior to Al deposition, while reduced TBC was observed in proton irradiated Al/Al_2O_3 interfaces. There are no studies regarding the use of Ar sputtering and the effect on TBC of wafer bonded interface. However, the TBC of wafer bonded GaN-SiC that has undergone similar Ar sputtering processes has been measured after full recrystallization of the amorphous interface.[16]Their results show that the TBC was improved after annealing from 170 to 230 MW/m^2 K, which matches TBC measurements done on GaN on SiC grown via MBE (230 MW/m^2 K).[23] However, both measured TBC values are significantly lower than predicted from simulation, which range from 400-800 MW/m^2 K (with no interface engineering). While the bonded GaN-SiC achieved TBC values that match current epitaxial GaN-SiC records, it is still difficult to say if the GaN-SiC interface in insensitive to the

remaining Ar. High dislocation densities of 8×10^9 cm^{-2} were observed in the MBE GaN-SiC measurements while low dislocation density substrates (10^4 - 10^6 cm^{-2}) were used in the wafer bonded case, which also may influence this comparison. So, it is still unclear what the presence of Ar at wafer bonded interfaces due to the SAB process has on TBC and if that is the cause of the significant decrease that is observed when comparing our wafer bonded Si-Ge and epitaxially grown Si-Ge.

4.4 Conclusion

In conclusion, the interface of wafer bonded Si-Ge was recrystallized by annealing and the TBC was measured and compared to epitaxially grown Si-Ge. We observe a significant reduction in TBC when compared to epi-grown samples, and the difference factors on interfacial thermal properties are explored (intermixing, amorphous interlayer, twist, Ar presence at interface). We find that our work supports the improvement in TBC through nanoscale intermixing and that the improvement is likely also attributed to recrystallization of the amorphous interface, which removes additional interface resistances. Based on modeling efforts from others regarding the effect of twist on TBC, we suspect that a 45° twist between our bonded sample is not the reason for a significant drop in TBC as compared to the epi-grown Si-Ge. Lastly, we note that a study of the effect of Ar presence at the wafer bonded interface on TBC would be of significant importance due to the recent success with the bonding method that has allowed fabrication of many different heterojunctions previously impossible.

4.5 References

[1]Kang, Y., Liu, H.D., Morse, M., Paniccia, M.J., Zadka, M., Litski, S., Sarid, G., Pauchard, A., Kuo, Y.H., Chen, H.W. and Zaoui, W.S., 2009. Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain–bandwidth product. *Nature photonics*, *3*(1), pp.59-63.

[2]Ye, H. and Yu, J., 2014. Germanium epitaxy on silicon. *Science and Technology of Advanced Materials*, *15*(2), p.024601.

[3]Höchbauer, T., Misra, A., Nastasi, M. and Mayer, J.W., 2001. Investigation of the cut location in hydrogen implantation induced silicon surface layer exfoliation. *Journal of Applied Physics*, *89*(11), pp.5980-5990.

[4]Hurley, R.E., Wadsworth, H., Montgomery, J.H. and Gamble, H.S., 2009. Surface blistering of low temperature annealed hydrogen and helium co-implanted germanium and its application to splitting of bonded wafer substrates. *Vacuum*, *83*, pp.S29-S32.

[5]Huang, L.J., Chu, J.O., Canaperi, D.F., D'emic, C.P., Anderson, R.M., Koester, S.J. and Wong, H.S.P., 2001. SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors. *Applied Physics Letters*, *78*(9), pp.1267-1269.

[6]Currie, M.T., Samavedam, S.B., Langdo, T.A., Leitz, C.W. and Fitzgerald, E.A., 1998. Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing. *Applied physics letters*, *72*(14), pp.1718-1720.

[7]Liao, M., Tran, V., Yee, M., Seal, M. and Goorsky, M.S., 2018. The role of misorientation in direct wafer bonded III-V materials. *ECS Transactions*, *86*(5), p.185.

[8]Kish, F.A., Vanderwater, D.A., Peanasky, M.J., Ludowise, M.J., Hummel, S.G. and Rosner, S.J., 1995. Low-resistance Ohmic conduction across compound semiconductor wafer-bonded interfaces. *Applied physics letters*, *67*(14), pp.2060-2062.

[9]Okuno, Y., Uomi, K., Aoki, M. and Tsuchiya, T., 1997. Direct wafer bonding of III-V compound semiconductors for free-material and free-orientation integration. *IEEE Journal of quantum electronics*, *33*(6), pp.959-969.

[10]Liao, M., Li, C., Flötgen, C. and Goorsky, M.S., 2018. Characterization of Wafer-Bonded Oxide-Free Silicon with Surfaces Treated with an Ion-Bombardment Procedure. ECS Transactions, 86(5), p.55

[11]Sakata, M., Oyake, T., Maire, J., Nomura, M., Higurashi, E. and Shiomi, J., 2015. Thermal conductance of silicon interfaces directly bonded by room-temperature surface activation. Applied Physics Letters, 106(8).

[12]Xu, D., Hanus, R., Xiao, Y., Wang, S., Snyder, G.J. and Hao, Q., 2018. Thermal boundary resistance correlated with strain energy in individual Si film-wafer twist boundaries. *Materials Today Physics*, *6*, pp.53-59.

[13]Gurunathan, R., Hanus, R., Graham, S., Garg, A. and Snyder, G.J., 2021. Thermal resistance at a twist boundary and a semicoherent heterointerface. *Physical Review B*, *103*(14), p.144302.

[14]Wang, S., Xu, D., Gurunathan, R., Snyder, G.J. and Hao, Q., 2020. Thermal studies of individual Si/Ge heterojunctions—The influence of the alloy layer on the heterojunction. Journal of Materiomics, 6(2), pp.248-255.

[15]Gordiz, K. and Henry, A., 2017. Phonon transport at interfaces between different phases of silicon and germanium. *Journal of Applied Physics*, *121*(2).

[16]Mu, F.; Cheng, Z.; Shi, J.; Shin, S.; Xu, B.; Shiomi, J.; Graham, S.; Suga, T. High Thermal Boundary Conductance across Bonded Heterogeneous GaN-SiC Interfaces. ACS Appl. Mater. Interfaces 2019, 11, 33428–33434.

[17]Xu, Y., Mu, F., Wang, Y., Chen, D., Ou, X. and Suga, T., 2019. Direct wafer bonding of Ga2O3–SiC at room temperature. *Ceramics International*, *45*(5), pp.6552-6555.

[18]Tian, Z., Esfarjani, K. and Chen, G., 2012. Enhancing phonon transmission across a Si/Ge interface by atomic roughness: First-principles study with the Green's function method. *Physical Review B*, *86*(23), p.235304.

[19]Cheng, Z., Li, R., Yan, X., Jernigan, G., Shi, J., Liao, M.E., Hines, N.J., Gadre, C.A., Idrobo, J.C., Lee, E. and Hobart, K.D., 2021. Experimental observation of localized interfacial phonon modes. *Nature communications*, *12*(1), p.6901.

[20]Read, W.T. and Shockley, W.J.P.R., 1950. Dislocation models of crystal grain boundaries. *Physical review*, *78*(3), p.275.

[21]Wolf, D., 2005. Structure and energy of grain boundaries. In *Handbook of Materials Modeling: Methods* (pp. 1953-1983). Dordrecht: Springer Netherlands.

[22]Hopkins, P.E., Norris, P.M., Stevens, R.J., Beechem, T.E. and Graham, S., 2008. Influence of interfacial mixing on thermal boundary conductance across a chromium/silicon interface.

[23]Ziade, E.; Yang, J.; Brummer, G.; Nothern, D.; Moustakas, T.; Schmidt, A. J. Thermal Transport through GaN−SiC Interfaces from 300 to 600 K. Appl. Phys. Lett. 2015, 107 (9), No. 091605.

Chapter 5: Interface stability of direct wafer bonded Gallium Nitride-Silicon heterojunction interfaces with annealing

5.1 Motivation

Heterogeneous integration of wide band gap semiconductors seeks to optimize the benefits and minimize the drawbacks of the properties associated with joining two (or more) materials but is often limited by crystal structure and lattice mismatch differences. One integration strategy is to leverage the mature Si infrastructure and integrate wide band gap materials like GaN with Si, to promote cost effectiveness and scalability. Another example is the integration of wide band gap materials with excellent electrical properties (GaN, bGO, SiC) merged together with high thermal conductivity substrates (AlN and diamond) as a thermal management strategy.[1-4] Heterogeneous integration of wide band gap semiconductors has garnered popularity in an effort to reduce device size, increase efficiency, and allow device operation at higher temperatures.

High quality epitaxial growth of GaN on Si is difficult due to the large in-plane lattice mismatch (17%) and CTE mismatch (54%) between (0001) GaN and (111) Si. When grown epitaxially, the large in-plane mismatch results in high dislocation densities that are reported in the range of 10^{10} cm^{-2} and as low as 10^{8} cm^{-2} when strain engineering using AlGaN buffer layers had been introduced.[5-6] For the integration of GaN in current Si-CMOS technologies, integration of GaN on (001) silicon is preferred based on the order of magnitude reduction in the density of interface states between Si and SiO_2 when comparing (001) and (111) oriented silicon[7] However, epitaxial growth of (0001) GaN on (100) Si presents an even greater challenge due to the difference

in symmetry between (0001) GaN (6-fold) and (001) Si (4-fold). The direct growth of (0001) GaN on (001) Si leads to rotational domains with 12-fold symmetry, but Feng et al., have reported single crystal growth of (0001) GaN on (001) Si with the use of a graphene and AlN buffer layer.[8] However, the dislocation density of the GaN film was not reported.

Direct wafer bonding allows for a greater range of materials combinations that are not limited by these restrictions. Bonding is commonly used in the fabrication of silicon-on-insulator wafers and has also been used to create a variety wide band gap semiconductor heterojunctions including GaN|Si,[9-11] GaN|SiC,[12] Ga_2O_3|Si,[13] Ga_2O_3|SiC,[14-17] and GaN|Diamond.[18] Matsumae et al., reported direct bonding of GaN|Si using plasma assisted bonding, in which they found that a coupled plasma treatment of oxygen and nitrogen (but not separately) led to successful bonding.[11] As a result of the bonding method, they observe oxide formation at the interface that is beneficial to bonding but is likely disadvantageous for interfacial transport properties. Mu et al., reports on the direct wafer bonding of GaN|Si using Ar sputtering surface activated bonding and compares the differences between Ga-face or N-face bonding with silicon at room temperature.[9] They observe a 5 nm amorphous interface in both Ga and N-faces bonded to Si and detect Ga diffusion into the amorphous interface at room temperature. They speculate that the Ga observed within the amorphous interface is due to the preferential Ar sputtering of N during the surface activation process, which leaves a Ga-rich surface that is local to the interface during bonding. Finally, they report close to bulk-like bond strengths, with the Ga-face bonded sample showing a small 13% improvement in bond strength on average over N-face bonded sample.

The Ar ion bombardment of the sample surfaces prior to bonding, while important for removing deleterious surface layers prior to bonding, is known to produce an amorphous or damaged region at the bonded interface that has been seen in many bonded systems that utilize the

ion bombardment method.[19-24] The effect of recrystallization of the amorphous interface has been shown to be beneficial in some bonded systems. For example, recrystallization of amorphous interfaces in Si-Si homojunctions bonded by Ar ion bombardment was shown to reduce electrical[20] and thermal[24] interface resistances after annealing at 450 °C and up to 700 °C respectively. For GaN-SiC heterojunctions, annealing at 1000 °C for 10 mins was reported to fully recrystallize the bonded interface and improve the TBC from 170 to 230 MW/(m^2·K).[12]

In this work, we investigate the evolution and stability of the amorphous interface after Ar sputtering between bonded GaN and Si and anneal at 450 °C and 700 °C to determine whether such annealing treatments would indeed recrystallize the interface or would lead to chemical interactions or morphological changes. We investigate the effects of annealing on the evolution of the heterojunction GaN-Si interface and report thermal boundary conductance measurements, which we correlate with morphological and chemical changes and interdiffusion at the interface.

5.2 Experimental Methods

(0001) GaN on sapphire templates were bonded to (100) silicon using EVG® ComBond® equipment under high vacuum (~10^{-8} mtorr) and room temperature. This process is similar to other reported surface activated bonding (SAB) or in situ sputtering techniques, in which GaN and Si surfaces are sputtered with an Ar ion beam to remove unwanted native surface oxides prior to bonding.[0,**Error! Reference source not found.**] The post Ar-beam treated samples are placed face-to-face and pressure is applied to initiate the bond. Removal of the sapphire substrate was done using Smart-Cut™ layer transfer technology, which resulted in a 2 μm GaN film bonded to Si. Further fabrication details can be found in our previous report.[00] After bonding and layer transfer, the samples were cleaved into 1 x 1 cm^2 pieces and annealed at 450 °C for 7 hours and 700 °C for 24

hours in ambient air to investigate the stability and evolution of the interface. The samples are labeled as Sample_RT, Sample_450.7, and Sample_700.24 referring to the room temperature, 450 °C 7 hour, and 700 °C 24 hour annealing conditions.

Structural characterization was conducted using various x-ray diffraction and electron microscopy techniques. In-plane and out-of-plane misorientation measurements between the bonded GaN and Si were done on a Bruker D1 diffractometer with an incident beam mirror producing a parallel beam and a Si (220) channel cut collimator (Cu kα1 radiation). The scattered beam optics include a Si (220) channel cut crystal. An FEI Nova 600 Nanolab Dual Beam SEM/FIB was used to prepare cross section TEM samples roughly 100 nm thick using a Ga source and transferred to a TEM grid using a standard lift out procedure. High resolution transmission electron microscopy (HRTEM) images of the bonded interface were taken using an FEI Titan at 300 kV. To study the chemical composition of the interface, high spatial resolution energy dispersive x-ray spectroscopy (EDX) was taken with Cs-corrected JEOL GrandARM at 300 kV.

5.3 Results and Discussion

The in-plane and out-of-plane orientation relationship between the GaN-Si bonded pair was analyzed using x-ray diffraction. To quantify the out-of-plane orientation between GaN and Si, a symmetric reciprocal space map (RSM) was taken that includes the (0004) GaN and (004) Si peaks. The RSM reveals a negligible <0.2° out-of-plane tilt between GaN and Si after bonding as seen in Figure 5.1a, which is likely due to the intrinsic miscut associated with both materials prior to bonding. To measure the in-plane orientation, x-ray phi scans of the (10$\underline{1}$1) GaN and (113) Si phi scans were taken sequentially without moving the sample and the scans were superimposed as shown in Figure 5.1b. The phi scans reveal that the bonding and alignment procedure results in

well aligned and controlled in-plane orientation where GaN [1010] || Si [110] with <1 degree misalignment.

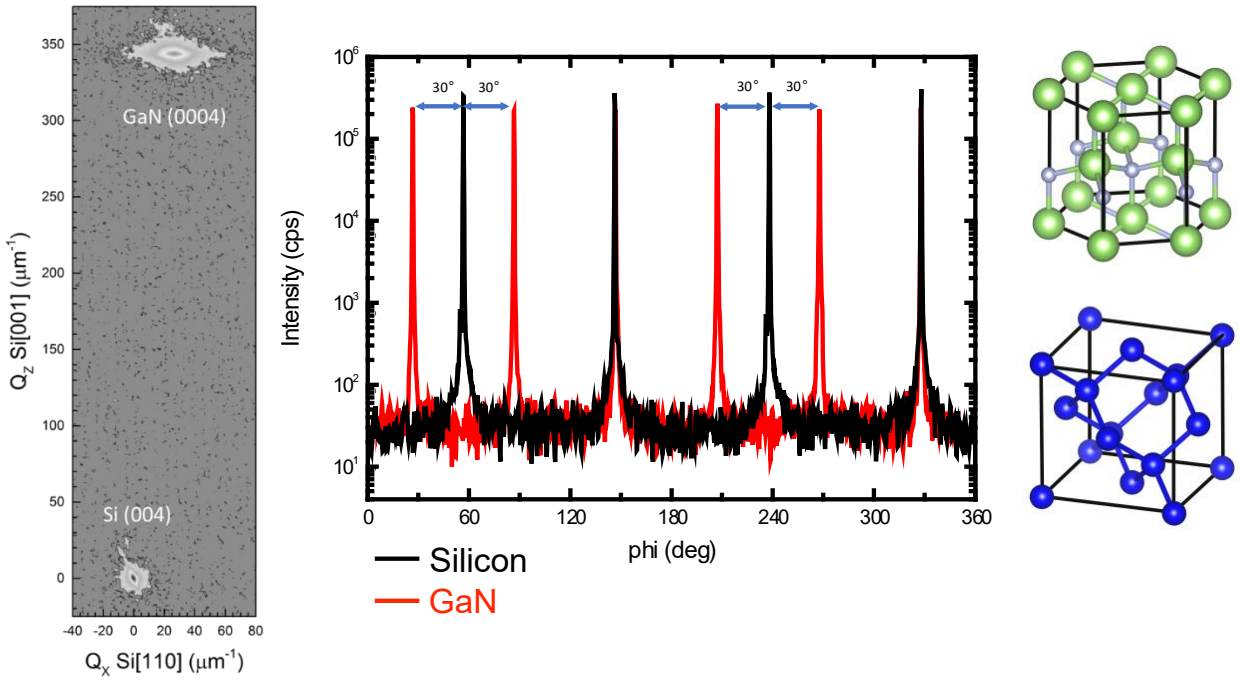

Figure 5.1: (a) Superimposed of phi scans of (10$\underline{1}$1) GaN and (113) Si taken in sequence without removal of the sample reveals alignment of the [10-10] GaN || [110] Si as seen in (b). (c) Reciprocal space map of Si (004) and GaN (0004) revealing ~0.2° tilt between the bonded layers.

The evolution and stability of the GaN|Si waferbonded interface can be seen in the HAADF STEM images of Sample_RT, Sample_450.7, and Sample_700.24 shown in Figure 5.2. In the as-bonded case (Figure 5.2a and 5.2d), an amorphous ~1.3 nm thick interlayer is present and atomic resolution of both the GaN and Si lattices are observed simultaneously, another indication of highly oriented zone axes. In comparison to Sample_RT, the amorphous interlayer thickness in Sample_450.7 (Figure 5.2b and 5.2e) is unchanged but a brightly contrasted feature borders the amorphous interlayer on the silicon side of the interface. Based on the HAADF imaging

conditions, bright contrast is associated with high z-contrast, suggesting excess Ga, which is supported by EDX below. In Sample_700.24 (Figure 5.2c and 5.2f), the Ga-rich plane observed in Sample_450.7, evolves into Ga-rich pyramidal shaped features that form 3 - 6 nm into the silicon with an average spacing of 10 nm. Figure 5.3 is a magnified HAADF image of one of these Ga-rich features, which shows that the edges of these pyramidal features follow the (111) planes of Si, as outlined in yellow dotted lines in Figure 5.3b.

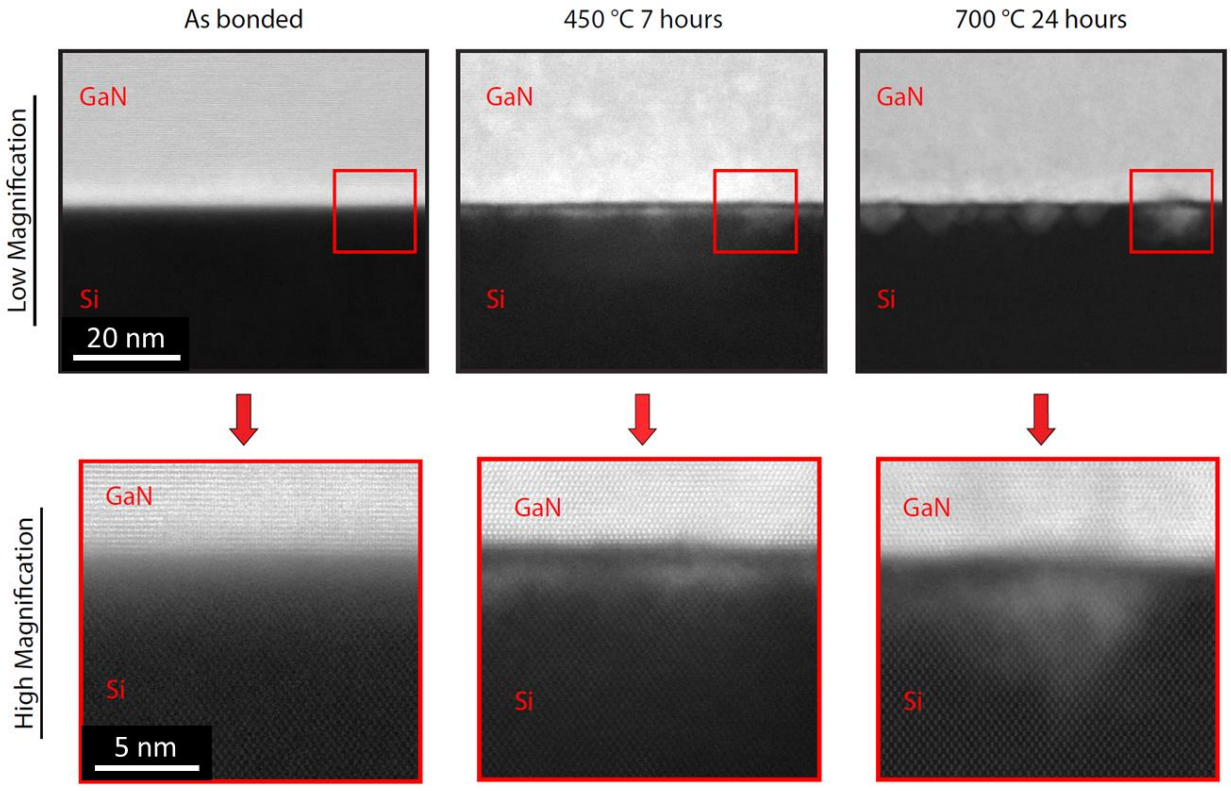

Figure 5.2: (a) Low and (d) high magnification STEM images of Sample_RT, which show a uniform ~1.3 nm amorphous interlayer between GaN and Si. (b) Low and (e) high magnification STEM images of Sample_450.7, which reveal a brightly contrasted Ga-rich region just below the original bonded interface on the Si side. (c) Low and (f) high magnification STEM images of Sample_700.24, which show the formation of Ga-rich pyramidal features that follow the (111) Si facets.

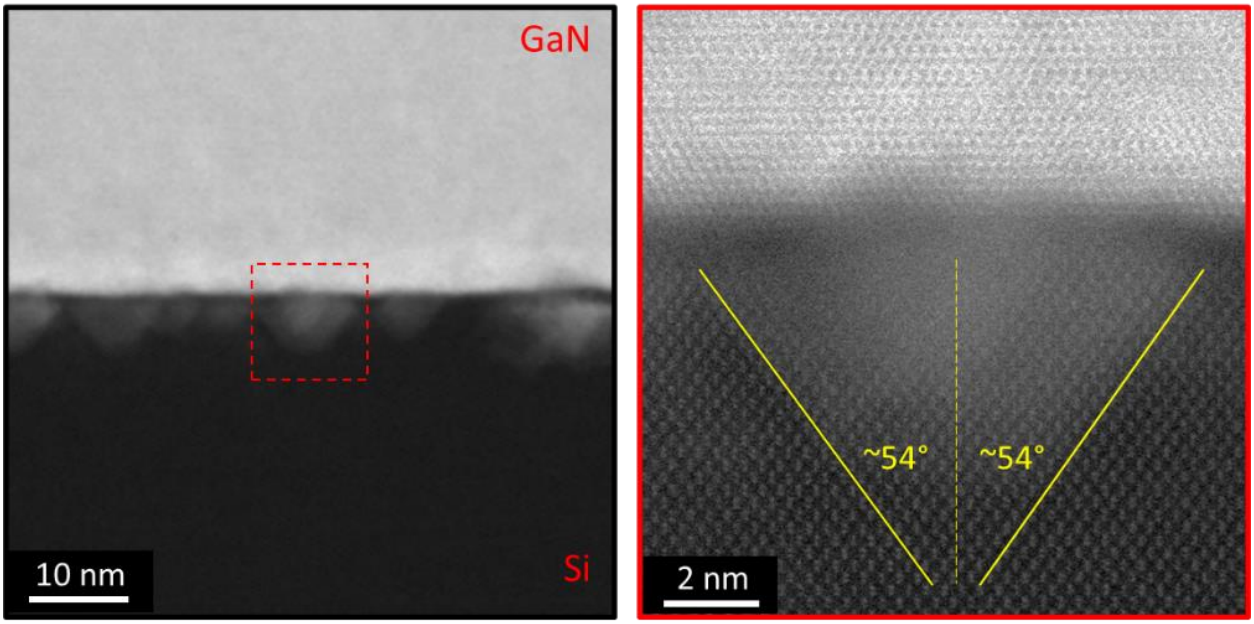

Figure 5.3: (a) HAADF STEM images of Sample_700.24, which show brightly contrasted Ga-rich pyramidal regions ~3-6 nm deep into the Si. (b) HRSTEM images of one pyramidal Ga-rich region that shows these features follow the (111) Si planes (outlined in yellow).

EDX maps of Ga, N, Si, and Ar are shown for Sample_RT and Sample_700.24 in Figure 5.4. For Sample_RT, comparison between STEM and EDX data show that the amorphous interlayer exists mainly on the Si side of the interface. In addition, Ar sputtering of GaN surfaces has been shown to induce a Ga-rich surface due to preferential sputtering of N atoms, which have been speculated as a consequence of the difference in atomic mass and surface binding energy between Ga and N.[25-29] We suspect that the 300 eV and 30° incident Ar sputtering parameters used in this study would lead to a Ga rich surface layer on the order of 1-2 nm based on MD simulations reported in previous works.[10-12] Integrated line scans of the EDX maps are shown on Figure 5.5. The line scan for Sample_RT is shown in Figure 5.5a, in which a slight increase in the Ga to N signal ratio is indeed observed which is evidence of an initially Ga-rich surface as indicated by the arrow on the plot.

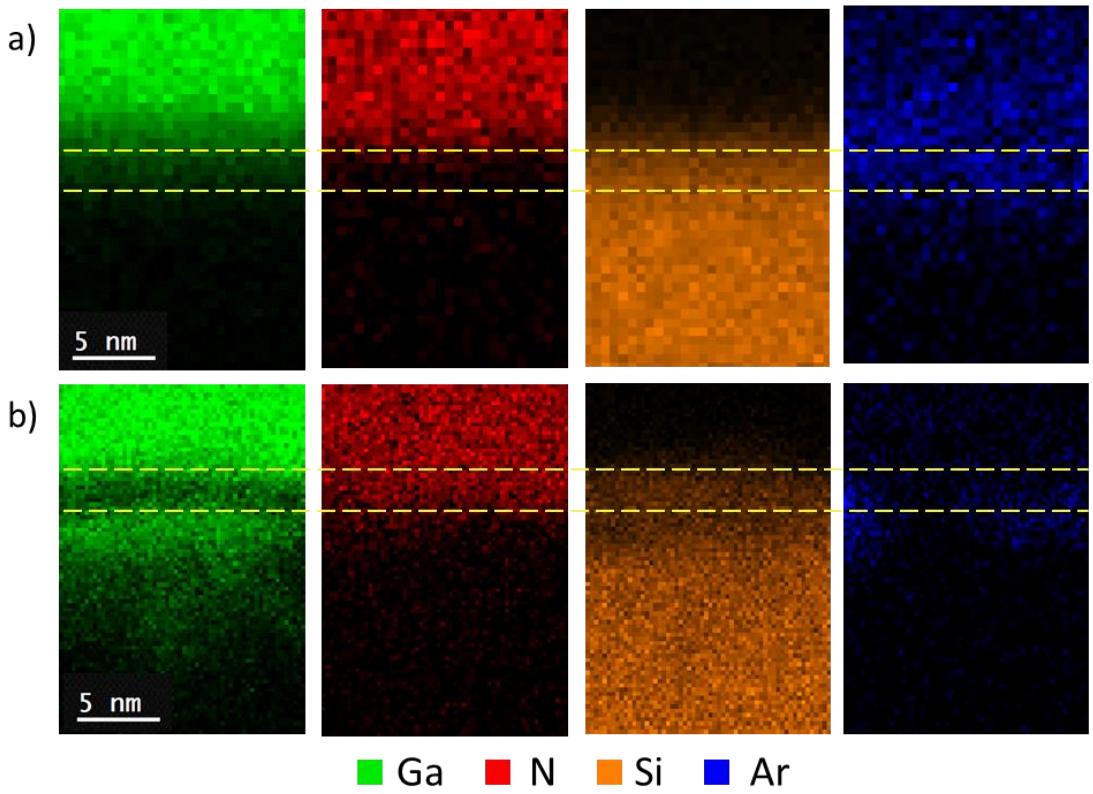

Figure 5.4: EDX maps (Ga, N, Si, Ar) (a) of Sample_RT and (b) Sample_700.24. EDX maps of Sample_RT reveal that the ~1.3 nm amorphous interface exists mainly on the Si side of the interface. The EDX maps of Sample_700.24 seen in (b) confirm that the brightly contrasted pyramidal features observed in the HAADF STEM correspond to Ga. Additionally it can be seen that the original bonded interface (outlined in yellow), is deficient in Ga and Si and N are present in this region.

For Sample_700.24, the EDX shown in Figure 5.4b shows evidence of the Ga-rich pyramidal regions that have formed into the Si substrate, which follow along the (111) planes as observed in the HAADF images. Additionally, it can also be seen that there is a Ga deficient region, which aligns with the original amorphous interface in the as-bonded case. The presence of Si and N within the Ga deficient region of the EDX map and line scans indicate that SiN_x is formed at the

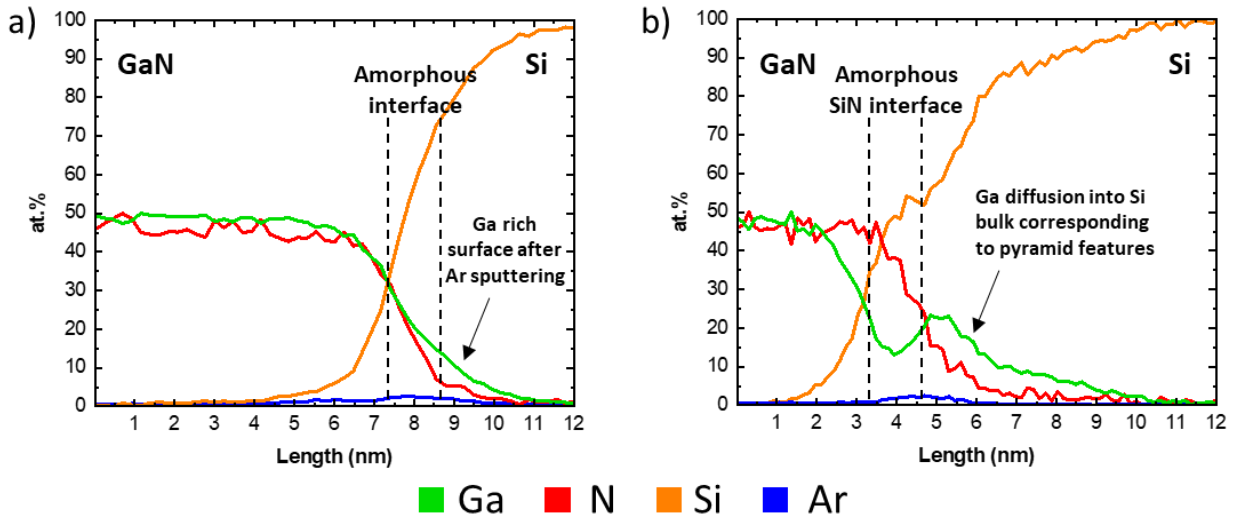

Figure 5.5: Integrated line scans of the EDX maps of (a) Sample_RT and (b) Sample_700.24. From the line scan of Sample_RT shown in (a), we can see evidence of a Ga-rich surface due to preferential sputtering of N during the Ar ion bombardment surface process. In (b), we observe clear evidence of Ga diffusion into the Si bulk as well as the presence of SiN_x formation at the original bonded interface (dotted in black).

interface. We speculate that the Ga rich surface layers diffuse into the Si and that the remaining N and amorphous silicon at the interface form SiN_x as observed in both Sample_450.7 and Sample_700.24.

Previous work has shown that recrystallization between Si|Si wafer bonded samples that had undergone Ar sputtering, occurred when annealed at 450 °C for 12 hours,[#] and at 700 °C for 3 hours.[20,24] The annealing conditions of 450 °C and 700 °C chosen here were based on our observations from the EDX of Sample_RT, that the 1.3 nm amorphous interlayer exists mainly within the Si. However, in the GaN-Si system, we found that the disordered interface did not recrystallize when annealed at these temperatures. Annealing at 450 °C up to 120 hours showed only initial stages of interdiffusion of Ga across the interface and the formation of SiN_x at the

interface. After annealing at 700 °C for 24 hours, an amorphous interface of similar thickness is still observed. With the formation of amorphous SiN_x, we suspect much higher annealing temperatures are required for the recrystallization of the GaN-Si bonded interface because amorphous silicon nitride is formed rather than the recrystallization of silicon. The recrystallization of amorphous SiN_x, however, has been reported to occur above 1200 °C[30] consistent with our observations that SiN_x forms at the expense of the recrystallization of silicon.

The Ga-Si phase diagram gives us insight on the formation of the Ga-rich pyramidal features in Si observed in Figure 5.3b.[31] The solid solubility of Ga in Si approaches 0.1% at 700 °C but is otherwise insoluble at 450 °C and at RT. As seen from the Ga-Si phase diagram, a two-phase region of Ga (L) + Si exists at the 450 °C and 700 °C annealing conditions. In Figure 5.2e, the Ga-rich planar feature at the surface of the silicon can be explained by the formation of liquid gallium from a Ga-rich surface (after the Ar ion bombardment treatment). At 700 °C, in which the solubility of Ga in Si is negligibly higher, we suspect that liquid gallium forms and some dissolves into Si and, when cooled to RT, solidifies onto lowest surface energy planes in Si, which are the close packed (111) planes.

Time domain thermal reflectance measurements were taken on Sample_RT and Sample_700.24 to measure the thermal boundary conductance in each case. The thermal boundary conductance (TBC) of Sample_RT is measured at 140 MW/(m^2·K), while the TBC for Sample_700.24 is degraded by a factor of two compared to the as-bonded interface. We speculate that the formation of a thermally insulating SiN_x layer and the formation of the Ga-rich pyramidal features, which create a chemically rough interface, both contribute to the degradation of the TBC after annealing. However, the TBC result of the GaN|Si interface as observed in Sample_RT reported here is higher than previously reported TBC values of epitaxially grown interfaces such

as GaN on Si, [32-34] GaN on SiC, [34,35] and GaN on diamond.[36,37] For epitaxially grown GaN on Si specifically, while the use of AlN or AlN/AlGaN superlattices has been used to reduce residual stresses in GaN, the addition of these buffer layers has been shown to drastically reduce the TBC.[33,34] These results demonstrate first that reconstruction of wafer bonded interfaces after a pre-bonding sputter-type in situ cleaning is highly dependent on the materials system. Second, room temperature bonding may be beneficial in creating a metastable interface with improved properties with no further annealing required.

5.4 Conclusion

In this study we investigate the stability and evolution of an amorphous interface in wafer bonded GaN-Si with annealing. As-bonded structures revealed abrupt interfaces with a ~1.3 nm amorphous interface due to Ar surface preparation techniques prior to bonding, while high temperature annealing (700 °C 24 hours) resulted in the formation amorphous SiN as well as Ga-rich pyramidal features that form across the bonded interface into the Si. These changes have deleterious effects on thermal transport across the interface and a reduction in the measured TBC by a factor of two. Finally, we show that high TBC can be achieved through wafer bonding of GaN and Si and that room temperature processing steps can create interfaces with improved interface properties that are stable at typical device operating temperatures (250 °C) and do not require further high temperature annealing processing steps.

5.5 References

[1]Yates, L., Anderson, J., Gu, X., Lee, C., Bai, T., Mecklenburg, M., Aoki, T., Goorsky, M.S., Kuball, M., Piner, E.L. and Graham, S., 2018. Low thermal boundary resistance interfaces for GaN-on-diamond devices. *ACS applied materials & interfaces*, *10*(28), pp.24302-24309.

[2]Tadjer, M.J., Anderson, T.J., Ancona, M.G., Raad, P.E., Komarov, P., Bai, T., Gallagher, J.C., Koehler, A.D., Goorsky, M.S., Francis, D.A. and Hobart, K.D., 2019. GaN-on-diamond HEMT technology with T AVG= 176 C at P DC, max= 56 W/mm measured by transient thermoreflectance imaging. *IEEE Electron Device Letters*, *40*(6), pp.881-884.

[3]Song, C., Kim, J. and Cho, J., 2020. The effect of GaN epilayer thickness on the near-junction thermal resistance of GaN-on-diamond devices. *International Journal of Heat and Mass Transfer*, *158*, p.119992.

[4]Montgomery, R.H., Zhang, Y., Yuan, C., Kim, S., Shi, J., Itoh, T., Mauze, A., Kumar, S., Speck, J. and Graham, S., 2021. Thermal management strategies for gallium oxide vertical trench-fin MOSFETs. *Journal of Applied Physics*, *129*(8).

[5]Dadgar, A., Poschenrieder, M., Bläsing, J., Contreras, O., Bertram, F., Riemann, T., Reiher, A., Kunze, M., Daumiller, I., Krtschil, A. and Diez, A., 2003. MOVPE growth of GaN on Si (1 1 1) substrates. *Journal of Crystal Growth*, *248*, pp.556-562.

[6]Fritze, S., Drechsel, P., Stauss, P., Rode, P., Markurt, T., Schulz, T., Albrecht, M., Bläsing, J., Dadgar, A. and Krost, A., 2012. Role of low-temperature AlGaN interlayers in thick GaN on silicon by metalorganic vapor phase epitaxy. *Journal of Applied Physics*, *111*(12).

[7]Balk, P., Burkhardt, P.J. and Gregor, L.V., 1965. Orientation dependence of built-in surface charge on thermally oxidized silicon. *Proceedings of the IEEE*, *53*(12), pp.2133-2134.

[8]Feng, Y., Yang, X., Zhang, Z., Kang, D., Zhang, J., Liu, K., Li, X., Shen, J., Liu, F., Wang, T. and Ji, P., 2019. Epitaxy of single-crystalline GaN film on CMOS-compatible Si (100) substrate buffered by graphene. *Advanced Functional Materials*, *29*(42), p.1905056.

[9]Mu, F., Morino, Y., Jerchel, K., Fujino, M. and Suga, T., 2017. GaN-Si direct wafer bonding at room temperature for thin GaN device transfer after epitaxial lift off. *Applied Surface Science*, *416*, pp.1007-1012.

[10]Dragoi, V., Razek, N., Guiot, E., Caulmilone, R., Liao, M., Wang, Y.S., Goorsky, M.S., Yates, L. and Graham, S., 2018. Direct wafer bonding of GaN for power devices applications. *ECS Transactions*, *86*(5), p.23.

[11]Matsumae, T., Fengwen, M., Fukumoto, S., Hayase, M., Kurashima, Y., Higurashi, E., Takagi, H. and Suga, T., 2021. Heterogeneous GaN-Si integration via plasma activation direct bonding. *Journal of Alloys and Compounds*, *852*, p.156933.

[12]Mu, F.; Cheng, Z.; Shi, J.; Shin, S.; Xu, B.; Shiomi, J.; Graham, S.; Suga, T. High Thermal Boundary Conductance across Bonded Heterogeneous GaN-SiC Interfaces. ACS Appl. Mater. Interfaces 2019, 11, 33428–33434.

[13]Xu, W., Wang, Y., You, T., Ou, X., Han, G., Hu, H., Zhang, S., Mu, F., Suga, T., Zhang, Y. and Hao, Y., 2019, December. First demonstration of waferscale heterogeneous integration of Ga_2O_3 MOSFETs on SiC and Si substrates by ion-cutting process. In 2019 IEEE International Electron Devices Meeting (IEDM) (pp. 12-5). IEEE.

[14]Xu, Y., Mu, F., Wang, Y., Chen, D., Ou, X. and Suga, T., 2019. Direct wafer bonding of Ga_2O_3–SiC at room temperature. Ceramics International, 45(5), pp.6552-6555.

[15]Cheng, Z., Mu, F., You, T., Xu, W., Shi, J., Liao, M.E., Wang, Y., Huynh, K., Suga, T., Goorsky, M.S. and Ou, X., 2020. Thermal transport across ion-cut monocrystalline β-Ga_2O_3 thin films and bonded β-Ga2O3–SiC interfaces. ACS Applied Materials & Interfaces, 12(40), pp.44943-44951.

[16]M. E. Liao, K. Huynh, Z. Cheng, J. Shi, S. Graham, and M. S. Goorsky, "Thermal Transport and Structural Improvements Due to Annealing of Wafer Bonded β-Ga2O3 | 4H-SiC," J. Vac. Sci. Technol. A, Accepted (2023).

[17]M. E. Liao, K. Huynh, B. Carson, L. Matto, K. Pan, J. S. Lundh, M. J. Tadjer, K. D. Hobart, and M. S. Goorsky, "Towards Controlled Transfer of (001) β-Ga_2O_3 to (0001) 4H-SiC Substrates," ECS Trans., Accepted (2023)

[18]Cheng, Z., Mu, F., Yates, L., Suga, T. and Graham, S., 2020. Interfacial thermal conductance across room-temperature-bonded GaN/diamond interfaces for GaN-on-diamond devices. ACS applied materials & interfaces, 12(7), pp.8376-8384.

[19]Flötgen, C., Razek, N., Dragoi, V. and Wimplinger, M., 2014. Novel surface preparation methods for covalent and conductive bonded interfaces fabrication. ECS Transactions, 64(5), p.103.

[20]Liao, M., Li, C., Flötgen, C. and Goorsky, M.S., 2018. Characterization of Wafer-Bonded Oxide-Free Silicon with Surfaces Treated with an Ion-Bombardment Procedure. ECS Transactions, 86(5), p.55.

[21]Xu, Y., Mu, F., Wang, Y., Chen, D., Ou, X. and Suga, T., 2019. Direct wafer bonding of Ga2O3–SiC at room temperature. Ceramics International, 45(5), pp.6552-6555.

[22]Jung, A., Zhang, Y., Arroyo Rojas Dasilva, Y., Isa, F. and von Känel, H., 2018. Electrical properties of Si-Si interfaces obtained by room temperature covalent wafer bonding. Journal of Applied Physics, 123(8).

[23]Takagi, H., Maeda, R. and Suga, T., 1999. Transmission electron microscope observations of Si/Si interface bonded at room temperature by Ar beam surface activation. Japanese journal of applied physics, 38(3R), p.1589.

[24]Sakata, M., Oyake, T., Maire, J., Nomura, M., Higurashi, E. and Shiomi, J., 2015. Thermal conductance of silicon interfaces directly bonded by room-temperature surface activation. Applied Physics Letters, 106(8).

[25]Lai, Y.H., Yeh, C.T., Hwang, J.M., Hwang, H.L., Chen, C.T. and Hung, W.H., 2001. Sputtering and etching of GaN surfaces. The Journal of Physical Chemistry B, 105(41), pp.10029-10036.

[26]Harafuji, K. and Kawamura, K., 2008. Sputtering yield as a function of incident ion energy and angle in wurtzite-type GaN crystal. Japanese journal of applied physics, 47(3R), p.1536.

[27]Despiau-Pujo, E. and Chabert, P., 2010. MD simulations of GaN sputtering by Ar+ ions: Ion-induced damage and near-surface modification under continuous bombardment. *Journal of Vacuum Science & Technology A*, *28*(5), pp.1105-1110.

[28]Despiau-Pujo, E. and Chabert, P., 2010. Low energy Ar+ bombardment of GaN surfaces: A statistical study of ion reflection and sputtering. *Journal of Vacuum Science & Technology A*, *28*(5), pp.1263-1268.

[29]Hattori, A.N., Endo, K., Hattori, K. and Daimon, H., 2010. Surface treatments toward obtaining clean GaN (0 0 0 1) from commercial hydride vapor phase epitaxy and metal-organic chemical vapor deposition substrates in ultrahigh vacuum. *Applied Surface Science*, *256*(14), pp.4745-4756.

[30]Riedel, R. and Seher, M., 1991. Crystallization behaviour of amorphous silicon nitride. Journal of the European Ceramic Society, 7(1), pp.21-25.

[31]Olesinski, R.W., Kanani, N. and Abbaschian, G.J., 1985. The Ga− Si (Gallium-Silicon) system. Bulletin of alloy phase diagrams, 6(4), pp.362-364.

[32]Yates, L., Bougher, T.L., Beechem, T., Cola, B.A. and Graham, S., 2015, July. The impact of interfacial layers on the thermal boundary resistance and residual stress in GaN on Si epitaxial layers. In International Electronic Packaging Technical Conference and Exhibition (Vol. 56901, p. V003T04A009). American Society of Mechanical Engineers.

[33]Pavlidis, G., Yates, L., Kendig, D., Lo, C.F., Marchand, H., Barabadi, B. and Graham, S., 2020. Thermal performance of GaN/Si HEMTs using near-bandgap thermoreflectance imaging. IEEE Transactions on Electron Devices, 67(3), pp.822-827.

[34]Kuzmik, J., Bychikhin, S., Pogany, D., Gaquière, C., Pichonat, E. and Morvan, E., 2007. Investigation of the thermal boundary resistance at the III-nitride/substrate interface using optical methods. Journal of Applied Physics, 101(5).J. Cho, et al., Phys. Rev. B., 89(11), 115301 (2014).

[35]Cho, J., Li, Y., Hoke, W.E., Altman, D.H., Asheghi, M. and Goodson, K.E., 2014. Phonon scattering in strained transition layers for GaN heteroepitaxy. Physical Review B, 89(11), p.115301.

[36]Pomeroy, J., Bernardoni, M., Sarua, A., Manoi, A., Dumka, D.C., Fanning, D.M. and Kuball, M., 2013, October. Achieving the best thermal performance for GaN-on-diamond. In 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) (pp. 1-4). IEEE.

[37]Sun, H., Simon, R.B., Pomeroy, J.W., Francis, D., Faili, F., Twitchen, D.J. and Kuball, M., 2015. Reducing GaN-on-diamond interfacial thermal resistance for high power transistor applications. Applied Physics Letters, 106(11).

Chapter 6: Surface reaction dependence of molecular beam epitaxy grown aluminum on various orientations of β-Ga_2O_3

6.1 Motivations

β-Ga_2O_3 is an emerging ultra-wide band gap semiconductor with promising electrical properties for high power electronics applications. With a band gap of 4.8 eV and theoretical breakdown voltage of 8 MV/cm, β-Ga_2O_3 can utilize thinner drift regions and provides lower on-resistance than SiC and GaN.[1,2] However, β-Ga_2O_3 suffers from low and anisotropic thermal conductivity (10-27 W/mK), an order of magnitude lower than GaN or SiC.[3] Development of thermal management strategies are important for successful implementation of β-Ga_2O_3 in high power devices. Device architectures of top-side, bottom-side, and double-sided cooling schemes have been investigated for lateral and vertical β-Ga_2O_3 devices.[4,5] Bottom-side cooling integrates high thermal conductivity substrates as a heat sink while top-side cooling strategies dissipate heat through the interconnect structure that includes the source, drain, and gate contacts, which are put in contact with a high thermal conductivity substrate.[5] Not surprisingly, double sided cooling schemes that incorporate both top and bottom sided cooling result in the best thermal management in an idealized setting. However, in complex device architectures thermal resistances increase with an increasing number of interfaces that are important to consider. Heterogeneous integration of Ga_2O_3 via wafer bonding introduces additional complexities due to its anisotropic properties.

The focus of this section is a closer inspection of the metal - β-Ga_2O_3 interface, which is an essential part of some wafer bonding techniques that utilize metals as an interfacial layer. Several metal on β-Ga_2O_3 interfaces have been investigated in the literature, such as Ti/β-Ga_2O_3,

Cr/β-Ga_2O_3, Ni/β-Ga_2O_3, Au/β-Ga_2O_3, and Al/β-Ga_2O_3.[6-8] Recent modeling studies have reported that thermal boundary conductance (TBC) across metal/β-Ga_2O_3 interfaces depends on the phonon cut off frequency of the metal, where a higher phonon cut off frequency is predicted to lead to higher TBC values.[7] However, a metal oxide interlayer was observed experimentally in some cases and the presence of the oxide was found to further suppress the TBC.[8] Formation of the oxide during metal deposition is observed if the energy of formation of the oxide is lower than β-Ga_2O_3 (in the case of Ti/β-Ga_2O_3, Cr/β-Ga_2O_3, and Al/β-Ga_2O_3), but not if the energy of formation is higher than β-Ga_2O_3 (in the case of Ni/β-Ga_2O_3). Experimentally reported TBC values of metal/β-Ga_2O_3 interfaces have not been consistent with each other.[7,8] An important consideration is that these studies utilized different orientations of β-Ga_2O_3 substrates. For example, reported TBC values of Ti on (010) β-Ga_2O_3 and Ti on $(\bar{2}01)$ β-Ga_2O_3 are 223 MW/(m^2·K) and 17 MW/(m^2·K) respectively.[7,8] β-Ga_2O_3 exhibits anisotropic properties as a result of its monoclinic crystal structure. Devices and structures have been produced on (010), $(\bar{2}01)$ and (001) oriented β-Ga_2O_3 and given the anisotropic nature of the material the relationship between orientation and processing steps (i.e. metallization) needs to be assessed.[9,10] The unit cell of β-Ga_2O_3 is shown in Figure 6.1. It contains two unique Ga sites, one that is octahedral (black) and the other that is tetrahedral (gray). This distinction is important and will be referred to in the discussion section. In this work we characterize the interface between Al and β-Ga_2O_3 and explore the influence of the β-Ga_2O_3 substrate orientation on the kinetics of the interlayer formed between Al and (010), (001), and $(\bar{2}01)$ β-Ga_2O_3 substrates.

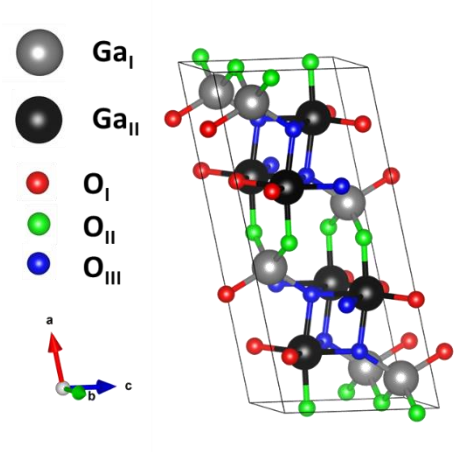

Figure 6.1: The unit cell of β-Ga_2O_3 consists of two unique Ga sites and three unique oxygen sites: (gray) Ga_I on tetrahedral sites, (black) Ga_{II} on octahedral sites, (red) O_I shared between 1 tetrahedral and 2 octahedral, (green) O_{II} shared between 2 tetrahedral and 1 octahedral, and (blue) O_{III} shared between 1 tetrahedral and 3 octahedral.

6.2 Experimental Methods

Aluminum was deposited on Sn doped β-Ga_2O_3 films grown on (010), (001), and ($\bar{2}$01) oriented β-Ga_2O_3 Novel Crystal Technology substrates simultaneously via molecular beam epitaxy (MBE). Prior to growth, Ga etching and O polishing were performed in the MBE environment at a substrate temperature of 800 °C, to reduce impurities on and polish the substrate. Growth of a ~170 nm Sn doped β-Ga_2O_3 at a growth temperature of 800 °C via metal oxide catalyzed epitaxy was performed with a Ga flux of $2.5*10^{-7}$ Torr, In flux of $4.0*10^{-7}$ Torr, and Sn cell temperature of 800 °C. Identical growth conditions for all three orientations were used and similar growth rates were achieved. Following growth, the substrates were cooled to 40 °C for Al deposition in the ultra-high vacuum environment within the same MBE chamber.

A Jordan Valley D1 X-ray diffractometer with parallel beam incident optics and Cu Kα radiation was used to perform pole figure measurements. The FEI Nova 600 Nanolab Dual Beam

SEM/FIB was used to prepare cross section TEM samples roughly 100 nm thick using a Ga source and transferred to a TEM grid using a standard lift out procedure. The sample was then further thinned using a gentle Ar^+ ion beam with 0.3kV energy to remove any Ga that may have been inadvertently deposited during the initial FIB process. High resolution transmission electron microscopy (HRTEM) images were taken using an FEI Titan at 300 kV. To study the chemical composition of the interface, high spatial resolution energy dispersive x-ray spectroscopy (EDX) was taken with Cs-corrected JEOL GrandARM at 300 kV.

6.3 Results and Discussion

HRTEM is used to investigate the structure and crystallinity of the Al/β-Ga_2O_3 interface. The thickness of the deposited aluminum film is 170 nm and an amorphous interfacial layer is observed between Al and β-Ga_2O_3 for all three samples. Aluminum oxide is formed at the interface as a result of a chemical reaction that reduces the Ga_2O_3 surface when aluminum is deposited. The formation of a metal oxide at the interface of Al and β-Ga_2O_3 is consistent with previous results and is attributed to Al_2O_3 having a lower energy of formation than β-Ga_2O_3, -1670 kJ/mol and -1070 kJ/mol respectively.[8] Figure 6.2 shows the HRTEM images of Al on (010), (001), and $(\bar{2}01)$ β-Ga_2O_3 substrates. Al grown on (010) β-Ga_2O_3 results in a 3.5 nm interfacial layer as compared to (001) and $(\bar{2}01)$ β-Ga_2O_3. Additionally, the interfaces for (001) and $(\bar{2}01)$ are sharp and distinct while the (010) interface shows evidence of nonuniform faceting. These results suggest that the β-Ga_2O_3 orientation plays a crucial role in the interfacial reaction that occurs between Al and β-Ga_2O_3. To confirm the chemical composition of the interface, EDX maps of 100 nm^2 areas were taken as shown in Figure 6.3. These maps confirm

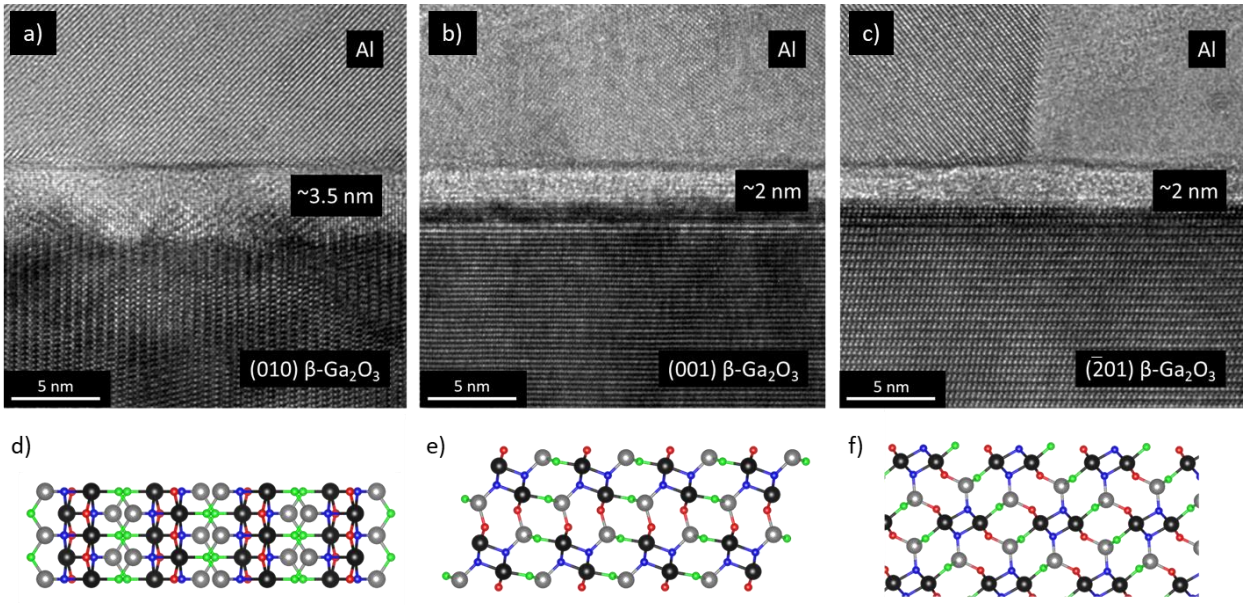

Figure 6.2: High resolution transmission electron microscopy images at the interface of (a) Al | (010) β-Ga_2O_3, (b) Al | (001) β-Ga_2O_3, and (c) Al | ($\bar{2}$01) β-Ga_2O_3. The corresponding crystal models are shown below each respective TEM image.

that the interfacial layer consists only of Al and O and is deficient of Ga. The absence of Ga in the interfacial layer suggests that Ga has been segregated and has diffused away from the original interface. This is supported by the increased Ga content that is observed above the interfacial layer at the Al-Al_2O_3 interface in Figure 6.3. In addition, lower magnification EDX reveals increased Ga content along grain boundaries within the Al film shown in Figure 7.4. Evidently, the Al reacts and reduces the β-Ga_2O_3 at the original Al/β-Ga_2O_3 interface and Ga ions then diffuse away from the oxide layer and along grain boundaries in the Al film. High gallium diffusion and segregation along Al grain boundaries is well known in studies of grain boundary embrittlement, so it is not surprising that this is observed.[11,12]

To understand the orientational dependence of the interfacial reaction, Figure 6.1 shows the β-Ga_2O_3 unit cell which consists of two unique Ga ions, one on a tetrahedral site (shown in

gray). The orientational dependence on the interface oxide layer thickness can be seen by comparing the (010) substrate interface with (001) and ($\bar{2}$01) substrates. and the other on an octahedral site (shown in black).[13] DFT calculations of $(Al_xGa_{1-x})_2O_3$ alloys have proposed that Al energetically favors octahedral Ga sites in β-Ga_2O_3 such that, thermodynamically, Al would prefer to occupy the octahedral sites before tetrahedral sites are filled. For example, for Al in $Al_{0.25}Ga_{0.75}O$ a tetrahedral site is 79 meV/cation higher in energy than an octahedral site.[15] To

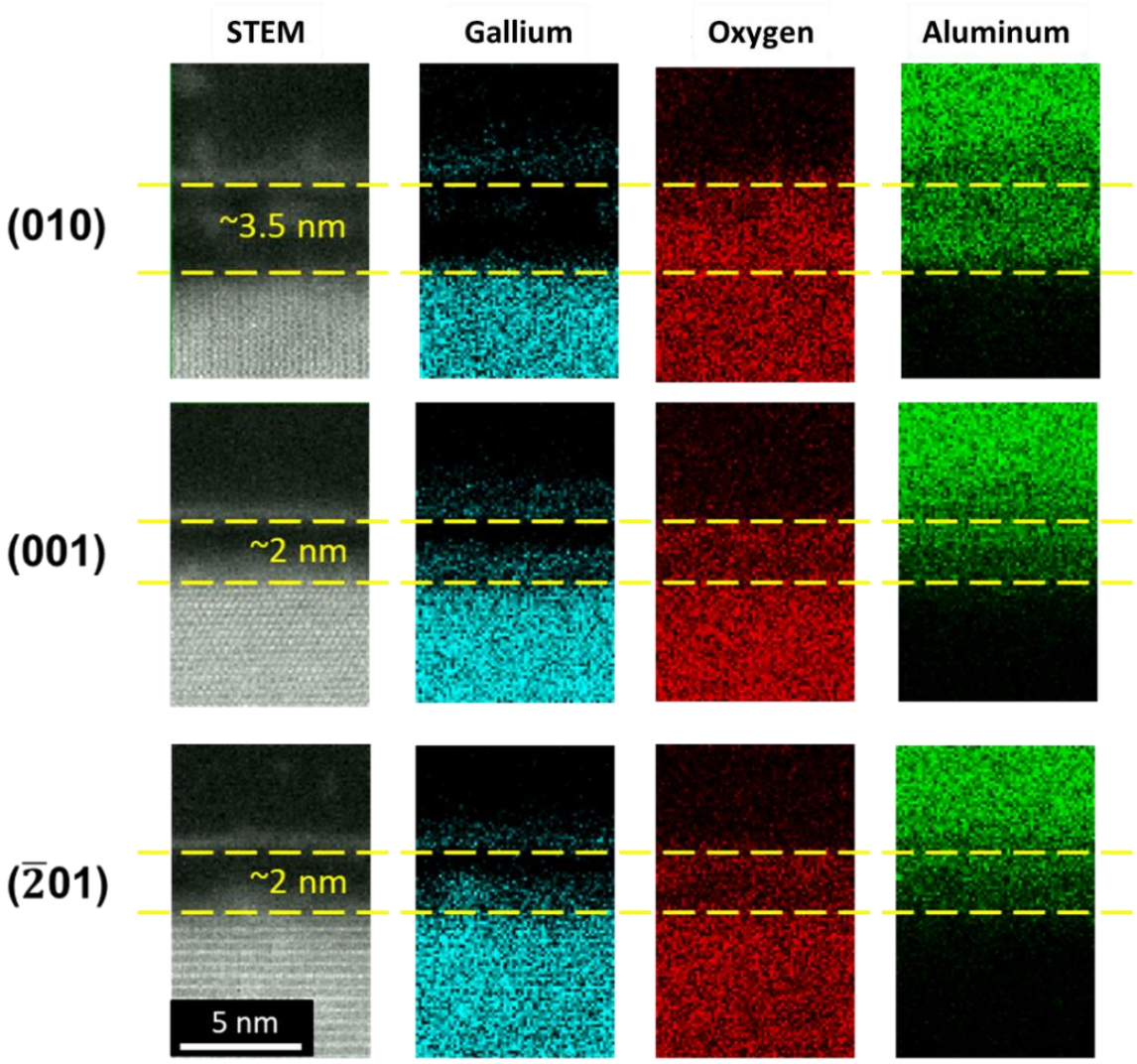

Figure 6.3: EDX elemental mapping of Ga, O, and Al across the Al | β- β-Ga_2O_3 interfaces showing that Ga is segregated from the oxide and can be seen diffusing into the Al.

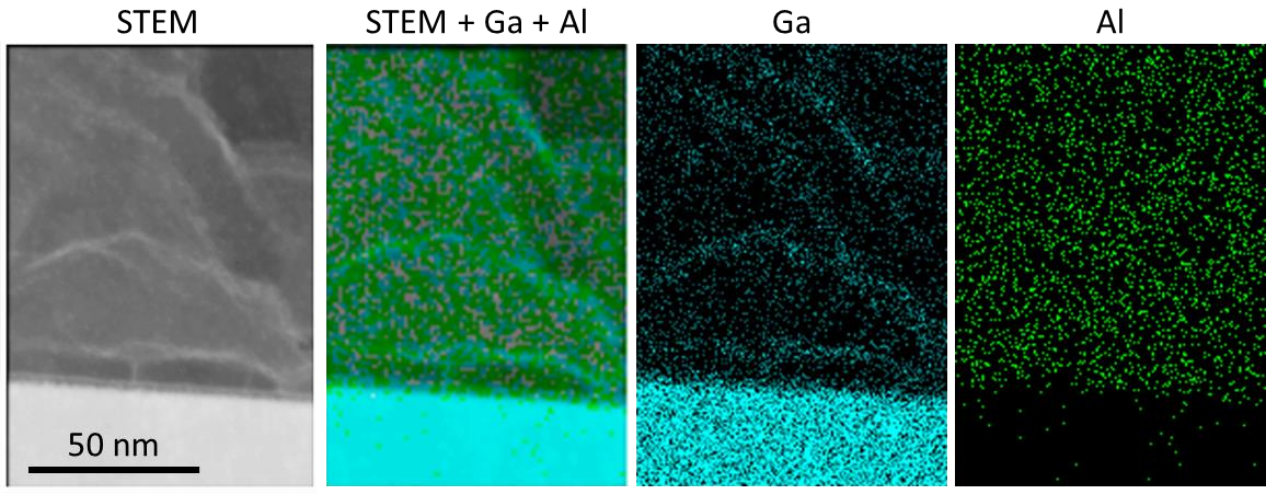

Figure 6.4: Low magnification EDX mapping and STEM shows the presence of Ga diffusion from the interface and along grain boundaries within the Al film.

understand why (010) β-Ga_2O_3 exhibits the thickest interfacial layer, atomic model cross sections along the various surface orientations of β-Ga_2O_3 studied are shown in Figure 6.3. For the (010) β-Ga_2O_3 sample, it can be seen that there are diffusional pathways of octahedral sites perpendicular to the interface that we propose allow for easier transport of Al through bulk β-Ga_2O_3 perpendicular to the interface. The alternating octahedral and tetrahedral columns perpendicular to the interface may also explain why the (010) β-Ga_2O_3 interface shows nonuniform faceting rather than a sharp interface. In contrast, (001) and $(\bar{2}01)$ orientations reveal alternating rows of octahedral and tetrahedral sites parallel to the interface, which may act as a barrier to diffusion of Al in β-Ga_2O_3 along these orientations. This correlates with the sharp and distinct interfaces seen in the HRTEM along (001) and $(\bar{2}01)$. This results in the thickest interfacial layer in the (010) oriented β-Ga_2O_3 sample and similar thinner layers for (001) and $(\bar{2}01)$ β-Ga_2O_3.

It is interesting to note that the interfacial reaction does not seem to correspond with the Al orientation. X-ray diffraction is used to determine the epitaxial relationship between Al and

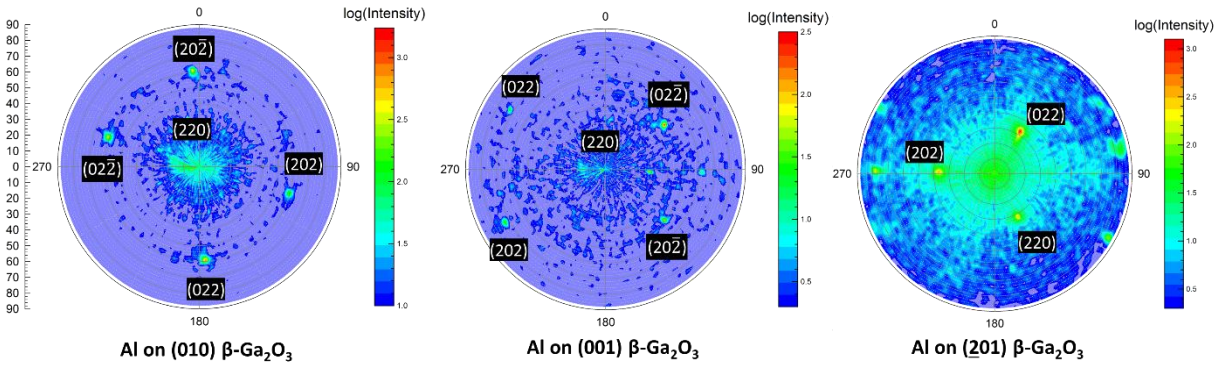

Figure 6.5: Pole figures of Al on (010), (001), and ($\bar{2}$01) β-Ga_2O_3 which identify the dominant orientation of the Al films with respect to the β-Ga_2O_3 substrate, which are (110) Al || (010) β-Ga_2O_3, (33-1) Al || (001) β-Ga_2O_3 (13.3 degrees from (110) Al), and (111) Al || ($\bar{2}$01) β-Ga_2O_3.

(010), (001), and ($\bar{2}$01) β-Ga_2O_3. Figure 6.5 shows pole figures which identify the dominant orientation of the Al films with respect to the β-Ga_2O_3 substrate, which are (110) Al || (010) β-Ga_2O_3, (33-1) Al || (001) β-Ga_2O_3, and (111) Al || ($\bar{2}$01) β-Ga_2O_3. As seen in Figure 6.3b and 6.3c, the (001) and ($\bar{2}$01) β-Ga_2O_3 have the same interlayer thickness but different dominant orientation. Additionally, in Figure 6.2c, an Al grain boundary is captured at the interface. The thickness of the interfacial layer does not seem to be affected by the Al orientation of these two grains and is uniform across the length of the image, further supporting the idea that the β-Ga_2O_3 orientation plays the main role in the interfacial layer thickness and thus is expected to be the dominant factor in electronic and thermal transport for metal - β-Ga_2O_3 interfaces.

6.4 Conclusion

In this section we propose a mechanism for increased interdiffusion between Al and β-Ga_2O_3 along (010) β-Ga_2O_3 in contrast to (001) and ($\bar{2}$01) oriented substrates. Theoretical studies of Al incorporation in $(Al_xGa_{1-x})_2O_3$ alloys have predicted the preference of Al on octahedral sites in β-Ga_2O_3. A consecutive pathway of octahedral sites perpendicular to the interface

presents itself in (010) β-Ga_2O_3 substrates that results in a thicker interfacial oxide layer. Under identical growth conditions, Al on (001) and $(\bar{2}01)$ β-Ga_2O_3 show thinner oxide layers that are sharper from the HRTEM. From the atomic model cross sections, alternating rows of octahedral and tetrahedral Ga sites exist parallel to the interface. The rows of tetrahedral Ga sites act as barriers to interdiffusion of Al further into the β-Ga_2O_3 bulk. EDX confirms that the oxide layer is deficient of Ga and that Ga can be observed diffusing away from the interface and along the grain boundaries of the Al film. Orientational dependence of metal-oxide interlayers in β-Ga_2O_3 will likely affect electrical and thermal characteristics for other metals that also possess oxides whose energies of formation are lower than β-Ga_2O_3.

6.5 References

[1] M. A. Mastro, A. Kuramata, J. Calkins, J. Kim, F. Ren, and S. J. Pearton, ECS Journal of Solid State Science and Technology 6, 356 (2017).

[2] B. Ozpineci and L.M. Tolbert, *Comparison of wide-bandgap semiconductors for power electronics applications*, U.S. Department of Energy, (2004).

[3] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, Applied Physics Letters 106, 111909 (2015).

[4] R.H. Montgomery, Y. Zhang, C. Yuan, S. Kim, J. Shi, T. Itoh, A. Mauze, S. Kumar, J. Speck, and S. Graham, Journal of Applied Physics 129, 085301 (2021).

[5] C. Yuan, Y. Zhang, R. Montgomery, S. Kim, J. Shi, A. Mauze, T. Itoh, J. S. Speck, and S. Graham, Journal of Applied Physics 127, 154502 (2020).

[6] M. H. Lee and R. L. Peterson, APL Materials 7, 022524 (2019).

[7] J. Shi, C. Yuan, H. L. Huang, J. Johnson, C. Chae, S. Wang, R. Hanus, S. Kim, Z. Cheng, J. Hwang, and S. Graham, ACS Applied Materials & Interfaces 13, 29083 (2021).

[8] H. T. Aller, X. Yu, A. Wise, R. S. Howell, A. J. Gellman, A. J. H. Mcgaughey, and J.A. Malen, Nano Letters 19, 8533 (2019).

[9] M. Higashiwaki, K. Konishi, K. Sasaki, K. Goto, K. Nomura, Q. T. Thieu, R. Togashi, H. Murakami, Y. Kumagai, B. Monemar, A. Koukitu, A. Kuramata, and S. Yamakoshi, Applied Physics Letters 108, 133503 (2016).

[10] S. J. Pearton, J. Yang, P. H. Cary IV, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, Applied Physics Reviews 5, 011301 (2018).

[11] S. Schmidt, W. Sigle, W. Gust, and M. Rühle, Zeitschrift Für Metallkunde 93, 428 (2002).

[12] E. Pereiro-López, W. Ludwig, D. Bellet, and J. Baruchel, Defect and Diffusion Forum 216-217, 241 (2003).

[13] S. Geller, The Journal of Chemical Physics 33, 676 (1960).

[14] H. Peelaers, J. B. Varley, J. S. Speck, and C. G. Van de Walle, Applied Physics Letters 112, 242101 (2018).

Chapter 7: Conclusion and Future Work

7.1 Conclusion

Engineering wafer bonded heterojunction interfaces for wide band gap semiconductors for improved transport properties is achieved in this work. First, the recovery of thermal conductivity is achieved in silicon after recrystallization of amorphized domains due to ion implantation. This study is necessary to understand how to engineer the Si|Ge wafer bonded system where the surface preparation process produces amorphized interfaces. The wafer bonded Si|Ge materials system is used as a fundamental study of engineering thermal boundary conductance at heterojunctions, which is observed to be affected by recrystallization of the interface, interdiffusion, twist misalignment, and impurities near the interface. Next, an additional complexity is added by bonding Si to a III/V, GaN. The Si|GaN system introduces an additional species to the materials system that can result in chemical reactions and interdiffusion anomalies. It is observed that the formation of SiN and non-uniform diffusion of Ga into the Si substrate introduces chemical roughness that reduces the thermal boundary conductance. Lastly, the effect of substrate orientation on chemical reactions between Al and β-Ga_2O_3 are reported as a precursor study to heterojunction interfaces involving β-Ga_2O_3. Due to is strongly anisotropic properties, substrate orientation will be another parameter when engineering interfacial properties.

7.2 Future Work

For the GaN|Si materials system, the effect of high temperature annealing was studied (700 °C), but the stability of the interface at relevant devices operating temperatures was not investigated. Future work may include a stability study of annealing at 200-250 °C (typical

power device operating temperatures) for long times, to see if the effects of diffusion are still prominent.

When moving forward towards more technologically relevant wide bandgap systems like GaN, AlN and β-Ga_2O_3, additional parameters will be involved in the bonding and subsequent processing for improved transport properties. Optimization of surface preparation and interfacial characterization of direct wafer bonded GaN to AlN have begun near the end of this work. In particular, the Ga face of the GaN wafer was bonded to the N face of the AlN wafer and characterized, but further engineering has not yet been done. The as received Ga-face of GaN substrates showed <1 nm roughness while the N-face AlN had a starting roughness of ~3 nm RMS. The N-face of the AlN was successfully polished to <1 nm RMS roughness suitable for direct wafer bonding using chemistry based on our previous work with GaN CMP [1]. For bonding, 2" GaN (Unipress) and 2" AlN (Hexatech) were bonded using standard cleaning and immersion in a $(NH_4)_2S$ solution. The samples were rinsed, dried and pressed Ga- to N-face (AlN) under moderate pressure (~50 kPa) and room temperature bonding was initiated. A significant fraction of the surfaces bonded, except for a couple of triangular regions associated with growth sector boundaries in the GaN. Subsequent annealing up to 800 C° was performed to strengthen the bond and to test the structure for high temperature stability. Similar coefficient of thermal expansion between GaN and AlN at high temperatures allows for high temperature annealing without debonding or cracking. The GaN substrate was then grinded and also subject to CMP to < 1um for transmission electron microscopy and time-domain thermal reflectance measurements of the bonded interface.

High resolution transmission electron microscopy shown in Figure 7.1 reveals complete crystallinity across the interface. However, only a ~1.5 nm interfacial region is observed, which

is suspected to be caused by reconfiguration of the interface after a total anneal of 350 °C 22 hours, 600 °C 1 hour, and 800 °C 1 hour. No thicker amorphous or oxide interfacial layer commonly found in other bonding methods (surface activated bonding, plasma treatment, or other interfacial layers) [2-5] are observed in this study. Preliminary thermal boundary conductance measurements via time domain thermal reflectance have measured a TBC of 250 MW/(m^2·K). This preliminary work demonstrates successful bonding and a baseline thermal boundary conductance that enables future studies in engineering transport properties across GaN|AlN.

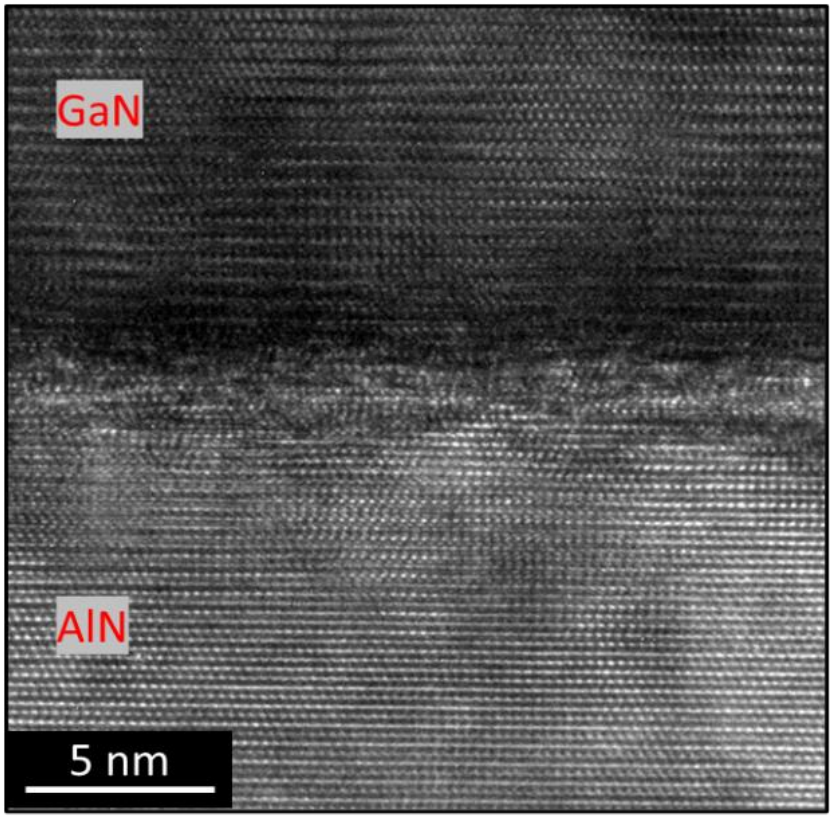

Figure 7.1 HRTEM of the wafer bonded GaN-AlN interface. ~1.5 nm interface can be observed due to reconfiguration of atoms after high temperature annealing.

7.3 References

[1] S. Hayashi, et al., J. Electrochem. Soc., 155(2), p.H113 (2007)

[2] M.E. Liao, et al., ECS Trans., 86(5), 55 (2018)

[3] V. Dragoi, et al., ECS Trans., 86(5), 23 (2018)

[4] Y. Xu, et al., Ceram. Int., 45, 6552 (2019).

[5] F. Mu, et al., Appl. Surf. Sci., 416, 1007 (2017)