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Wideband Transmit and Receive Phased-Array Integrated Circuits and Systems for Multi-Standard mm-Wave 5G Applications

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Wideband Transmit and Receive Phased-Array Integrated Circuits and Systems for Multi-Standard mm-Wave 5G Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Abdulrahman Alhamed

Committee in charge:

Professor Gabrie M. Rebeiz, Chair
Professor Gert Cauwenberghs
Professor Drew A. Hall
Professor Tzu-Chien Hsueh
Professor Brian Keating

2021

The Dissertation of Abdulrahman Alhamed is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2021

DEDICATION

To my family

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The material in this dissertation is based on the following papers which are either published, has been submitted for publication, or contains material that is currently being prepared for submission for publication.

Chapter 2, in full, is a reprint of the material as it appears in: A. Alhamed, and G. M. Rebeiz, "A 28–37 GHz Triple-Stage Transformer-Coupled SiGe LNA with 2.5 dB Minimum NF for Low Power Wideband Phased Array Receivers," *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2020, pp. 1-4.*. The dissertation author is the primary investigator and author of this paper.

Chapter 3, in full, has been accepted for publication of the material as it may appear in: A. Alhamed, O. Kazan, G. Gultepe and G. M. Rebeiz, "A Multi-Band/Multi-Standard 15-57 GHz Receive Phased-Array Module Based on 4 × 1 Beamformer IC and Supporting 5G NR FR2 Operation," *IEEE Transactions on Microwave Theory and Techniques*, accepted. The dissertation author is the primary investigator and author of this paper.

Chapter 4, in full, has been accepted for publication of the material as it may appear in: A. Alhamed, G. Gultepe and G. M. Rebeiz, "A Multi-Band 16-52 GHz Transmit Phased-Array Employing 4 × 1 Beamforming IC With 14-15.4 dBm Psat For 5G NR FR2 Operation," *IEEE Journal of Solid-State Circuits*, accepted. The dissertation author is the primary investigator and author of this paper.

Chapter 5, in full, has been submitted for publication of the material as it may appear in: A. Alhamed, G. Gultepe and G. M. Rebeiz, "64-Element 16-52 GHz Phased-Array Transmitter and Receiver Based on Slat-Array Architecture for Multiband 5G NR FR2 Operation," *IEEE Transactions on Microwave Theory and Techniques*, submitted. The dissertation author is the primary investigator and author of this paper.

Chapter 6, in part, will be submitted for publication of the material as it may appear in: A. Alhamed and G. M. Rebeiz, "15-52 GHz Multi-band Tx/Rx Beamformer IC and 16×1 Linear

Phased-Array for Wideband Multi-Gb/s 64-QAM Links," *IEEE Transactions on Microwave Theory and Techniques*, in preparation for submission. The dissertation author is the primary investigator and author of this paper.

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PUBLICATIONS

A. Alhamed, G. Gultepe and G. M. Rebeiz, "64-Element 16-52 GHz Transmit and Receive Phased Arrays for Multiband 5G-NR FR2 Operation," *IEEE Transactions on Microwave Theory and Techniques*, submitted.

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A. Alhamed and G. M. Rebeiz, "A Global Multi-Standard/Multi-Band 17.1-52.4 GHz Tx Phased Array Beamformer with 14.8 dBm OP1dB Supporting 5G NR FR2 Bands with Multi-Gb/s 64-QAM for Massive MIMO Arrays," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, Colorado.

A. Alhamed, O. Kazan, and G. M. Rebeiz, "A Multi-Standard 15-57 GHz 4-Channel Receive Beamformer with 4.8 dB Midband NF for 5G Applications," *2020 IEEE MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA.

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ABSTRACT OF THE DISSERTATION

Wideband Transmit and Receive Phased-Array Integrated Circuits and Systems for Multi-Standard mm-Wave 5G Applications

by

Abdulrahman Alhamed

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2021

Professor Gabrie M. Rebeiz, Chair

The inevitable growth of mobile users and the proliferation of data-intensive applications are creating unprecedented challenges and opportunities. Therefore, the deployment of the fifth generation (5G) networks worldwide is accelerating to meet the increasing data-rate demands. Several mm-wave bands have been standardized as part of the 5G new radio frequency range 2 (NR FR2) at 24.25-52.4 GHz. The dissertation addresses the challenges of designing mm-waves ultra-wideband circuits and phased-array systems capable of operating at this widespread spectrum in advanced SiGe technology. The major contributions are the design of receive (Rx), transmit (Tx), and Tx/Rx beamformer chips and the implementation of multi-band 8×1 linear

phased-array modules and large-scale 64-element phased-array systems.

The work in the 15-57 GHz Rx 4×1 beamformer culminated in the design and measurement of ultra-wide-band LNA, phase shifter, VGA, differential to single-ended stage and 4:1 on chip combining network with >40 GHz of bandwidth. Several circuit design techniques are introduced to break the gain-bandwidth (GBW) trade-offs in conventional beamformer designs. A peak electronic gain of 24-25 dB and a 4.7-6.2 dB noise figure is achieved with a 15-57 GHz record 3-dB bandwidth.

The mm-wave multi-band transmit phased-array contributions focus on the design of 16-52 GHz 4×1 transmit beamformer chip. The Tx IC has four differential RF beamforming channels each with an active balun, vector modulator based phase shiftier, VGA, and a 2-stage class-AB power amplifier (PA). Circuit techniques employed in this work are selected to fulfill the power and bandwidth requirements with compact area utilization. An 8-element phased-array Tx module is demonstrated achieving broadband performance with +/- 60^o scanning capability.

The work in the 64-element multi-band transmit and receive phased arrays employs the slat-array architecture using 16×1 linear arrays each has four 4×1 beamformer chips and end-fire tapered-slot antennas. Architecture and system analysis are presented to realize 16-52 GHz multi-standard operation. The 64-element Tx array achieves an EIRP of 50-51.7 dBm and 47.6-49 dBm at P_{sat} and P_{1dB}, respectively, at 24.5-48 GHz.

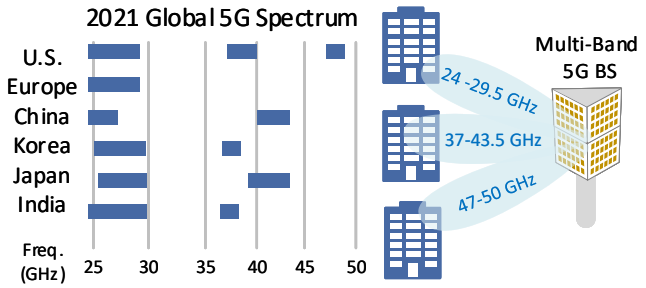
Chapter 1

Introduction

1.1 mm-Wave Phased-Arrays for 5G Communications

The deployment of 5G networks worldwide is accelerating to provide enhanced mobile broadband (eMBB), ultra reliable low latency communications (uRLLC), and massive machine type communications (mMTC). These use cases support several applications such as autonomous vehicles, remote surgery, and industry automation with targeted throughput up to 20 Gb/s in downlink and 10 Gb/s in uplink [1]. Therefore, multiple bands are allocated for 5G new radio frequency range 2 (NR FR2) which spans 24.25-52.5 GHz and with a channel bandwidth up to 400 MHz and can be aggregated to a maximum bandwidth of 800 MHz [1]. The 5G FR2 includes the n257 band (26.5-29.5 GHz), n258 band (24.25-27.50 GHz), n259 (39.5-43.5 GHz), n260 band (37-40 GHz), n261 band (27.5-28.35 GHz), and with expected bands to be allocated around 48 GHz (Fig. 1.1). Therefore, this widespread spectrum requires the design and implementation of a low-cost multi-band/multi-standard solution.

Due to the high free space path loss (FSPL) at mm-wave frequencies, directive communications using affordable phased-arrays is adopted for building mm-wave 5G-communication systems. These arrays are built using multi-channel beamformer chips fabricated in advanced SiGe and CMOS processes. The silicon-based technologies are selected rather than GaAs or InP based modules to reduce the cost, increase the yield, and achieve low power performance while providing unparalleled integration level and digital processing capabilities. Therefore,



(a)

NR Band	UL and DL Frequency Range (GHz)	Duplex mode
n257	26.5– 29.5	TDD
n258	24.25 – 27.5	
n259	39.5 – 43.5	
n260	37 – 40	
n261	27.5 – 28.35	

(b)

Figure 1.1. (a) Multi-band base-station and worldwide 5G spectrum snapshot in 2021. (b) 5G-NR FR2 operating bands.

silicon-based processes are the best candidates for mm-Wave 5G phased-array radios for base stations and user equipment [2–4].

To date, there have been several demonstrations of mm-wave phased-array systems [5–15]. Designs based on RF beamformeing [6, 16], LO beamforming [17], and digital/hybrid [18, 19] beamforming architectures have been proposed targeting narrow-band operation at the n257 (26.5–29.5), n258 (24.25–27.5) or n260 (37–40) 5G bands. These phased-arrays have fractional bandwidths $[(f_2 - f_1)/f_c]$ <10% limited by system and circuit design. Improvements to both system-level and circuit-level designs are essential in order to realize a solution capable of 5G FR2 multi-band operation.

Recently, multiple phased-arrays that can support dual or triple band operation are reported [18, 20–23]. Due to the challenge of wideband design, most of these systems are limited to an unpackaged beamformer IC implementation or a single channel front-end. Wideband phased arrays with full system implementation operating at 23.5-29.5 GHz and at 37-42 GHz are reported in [16, 24]. These arrays show excellent performance but still have relatively limited

bandwidth (<25%) and can not support all 5G bands at 24.25-52.6 GHz.

1.2 Thesis Overview

The thesis presents circuits, system architectures, phased-array design and measurement techniques to realize multiband 5G NR FR2 operation.

Chapter 2 presents a transformer-based three-stage SiGe low-noise amplifier (LNA) implemented in the Tower Semiconductor SBC18S5 process. The design realizes wideband input matching using a T-coil network, and wideband interstage matching using coupled transformers. The LNA exhibits 20 dB gain with a 3-dB bandwidth > 9 GHz and has a minimum noise figure (NF) of 2.5 dB with 13 mW of power consumption. The LNA can also operate at 6 mW power consumption with only a 0.3 dB increase in the NF, and achieves 3 dB of gain for 1 mW of DC power consumption at 33 GHz. To the author's knowledge, this work presents one of the highest figure-of-merit (FoM) of mm-wave amplifiers with a center frequency above 30 GHz.

Chapter 3 presents a 15-57 GHz multi-band/multi-standard phased array architecture for the 5G New Radio FR2 bands. An 8-element phased array receive module is demonstrated based on two 4-channel wideband beamformer chips designed in SiGe BiCMOS process and flipped on a low-cost printed-circuit board. The SiGe Rx chip employs RF beamforming and is designed to interface to a wideband differential Vivaldi antenna array. Each channel consists of a low-noise amplifier (LNA), active phase shiftier with 5-bit resolution, variable gain amplifier (VGA), and differential to single ended stage. The four channels are combined using a wideband 2-stage on chip Wilkinson network. The beamformer has a peak electronic gain of 24-25 dB and a 4.7-6.2 dB noise figure with a -29 to -24 dBm input P_{1dB} at 20-40 GHz. The 8-element phased array module also achieved ultra-wideband frequency response with flat gain and low system NF. The phased array scans +/- 55^o with <-12 dB sidelobes demonstrating multi-band operation. A 1.2 m OTA link measurement using the 8-element Rx module supports 400 MHz 256-QAM OFDMA modulation with <2.76% EVM at multiple 5G NR FR2 bands. To author's knowledge, this work

achieves the widest bandwidth phased array enabling the construction of multi-standard systems.

Chapter 4 introduces a mm-wave multi-band transmit phased-array design supporting the 5G New Radio frequency range 2 (NR FR2) bands. An 8-element phased-array module is presented employing two wideband 16-52 GHz 4×1 transmit beamformer ICs and tapered slot Vivaldi antenna array. The beamformer chips are designed in a SiGe BiCMOS process and flipped on a printed-circuit board (PCB). The IC has four differential RF beamforming channels each consists of an active balun, analog adder based phase shiftier (PS), variable gain amplifier (VGA), and a 2-stage class-AB power amplifier (PA). The RF input signal is distributed to the four channels using a compact Wilkinson network. The measured peak gain is 28.3 dB with 13.5-14.7 dBm output P_{1dB} and 14-15.4 dBm Psat at 20-50 GHz. Each channel dissipates 250 mW from 2 V and 3 V supplies at P_{1dB}. The beamformer chip is tested using 64-QAM waveforms and achieves a data-rate of 2.4 Gb/s at 5.2% EVM and 9.6 dBm average power. The 8-element phased array module shows a broadband performance with excellent patterns and +/- 60^o scanning capability and with a peak EIRP of 32-34 dBm at 19.5-51 GHz. At an EIRP of 21-22 dBm, 400 MHz 256-QAM 5G-NR compliant waveforms are transmitted with <2.98% EVM and demonstrating 5G NR FR2 operation. To the author's knowledge, this work achieves the highest bandwidth phased-array with a peak EIRP of 34 dBm enabling the construction of multi-standard/multi-band 5G phased-array systems.

Chapter 5 presents 16-52 GHz multi-band transmit and receive phased arrays designed to support multi-standard 5G communications. The 64-element arrays are built using 16×1 linear arrays each has four 4×1 beamformer chips on a 6-layer printed-circuit board (PCB) with a Wilkinson combiner/divider network and tapered-slot antennas. The wideband beamformer chips are designed in a SiGe BiCMOS process and employ the RF beamforming architecture. The arrays have +/- 60^o scanning capability in the azimuth-plane and +/- 30^o in the elevation-plane with low sidelobes. The 64-element Tx array achieves an EIRP of 50-51.7 dBm and 47.6-49 dBm at P_{sat} and P_{1dB}, respectively, at 24.5-48 GHz. 5G-NR compliant waveforms with 400 MHz and up to 256-QAM are transmitted with <2.98% EVM_{rms} and 34-36 dBm average EIRP. Single-

carrier (SC) 400 MHz 64-QAM waveforms are also transmitted achieving <3% EVM_{rms} with 39-40.3 dBm average EIRP and 2.4 Gb/s data rate. The 64-element Rx array achieves a system NF of 5.3-6.9 dB and a measured G/T of -19.3 to -14.4 dB (with $T_{ant} = 295K$) at 20-50 GHz, and <2.6% EVM performance when tested with 400 MHz 256-QAM 5G-NR complaint packets. To the author's knowledge, this work achieves the highest bandwidth Tx and Rx phased-array systems suitable for multi-band 5G operation.

Chapter 6 presents a transmit/receive (Tx/Rx) multi-band phased array 4×1 RFIC and a 16×1 phased-array module. Wideband system and chip architectures, circuit design and measurements are reported. The phased-array system integration and measurements are carried out including wideband pattern and effective isotropic radiated power (EIRP) measurements.

The thesis concludes with a summary of the presented work and suggestions for future research.

Chapter 2

A 28-37 GHz Triple-Stage Transformer-Coupled SiGe LNA with 2.5 dB Minimum NF for Low Power Ka-band Phased Array Receivers

2.1 Introduction

With recent interest in wideband mm-wave phased-arrays for high data rate applications and 5G communication systems, the design of a wideband low-noise amplifier (LNA) is key to achieve high system performance (Fig. 2.1). The LNA noise dominates the receiver overall noise figure (NF) and greatly affects the sensitivity. This critical front-end block is expected to provide a broadband input match with low-noise performance at low power consumption.

The advancement in silicon-based technologies such as CMOS, FD-SOI and SiGe BiCMOS enabled the design of broadband receivers at mm-wave frequencies with low NF. Previous work reported an LNA design with a gain of 18.2 dB and a minimum NF of 3.9 dB and 9.5 mW power consumption employing a common source (CS) design in 65 nm CMOS technology [25]. Other work showed a high gain LNA of 28 dB with 3.1 dB minimum NF but consumes 80 mW of power [26]. A two-stage CS LNA with source-gate feedback is presented in [27]. The LNA achieves a peak gain of 21.5 dB and 17.3 mW power consumption centered at 27 GHz.

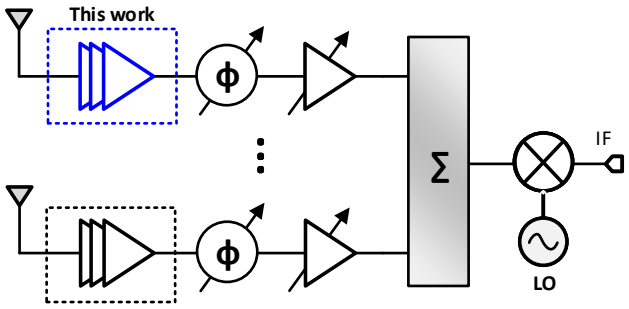


Figure 2.1. Wideband phased-array with the three-stage LNA.

This work presents a wideband low-power LNA design based on three cascode stages with transformer coupling for wideband interstage and output matching. A T-coil is employed at the input in order to realize the required wideband input and noise matching. This design avoids the use of resistors commonly used to achieve wideband operation, either in feedback or in inductive degeneration [28]. As a result of using only high-Q inductors, high gain and low NF are achieved across a wide bandwidth at low power consumption.

2.2 Technology

The wideband LNA is implemented in Tower Semiconductor 0.18μm SiGe BiCMOS technology (SBC18S5). The stack includes 7 Aluminum layers with metal-insulator-metal (MiM) capacitors. Fig. 2.2 presents the physical layout of a 3x4 μm transistor used in the first stage of the LNA. A multi-instance transistor is used to reduce the base resistance and minimize the parasitic capacitance as compared to a single 12 μm transistor. After extracting all parasitic capacitance and resistance up to M7, the simulated peak f_t and f_{max} are 270 GHz and 212 GHz, respectively, at a current density of 1.9 mA/μm. The simulated NF_{min} at 33 GHz is 1.15 dB at 0.25-0.3 mA/μm as shown in Fig. 2.2. The measured loss of a grounded coplanar waveguide (GCPW) 50-Ω transmission line implemented in this technology is 0.32 dB/mm at 30 GHz.

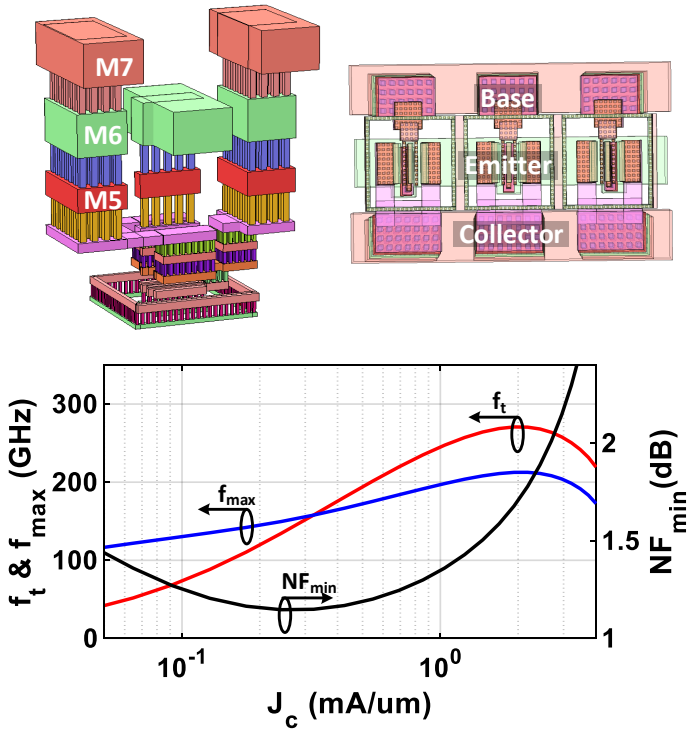


Figure 2.2. Physical layout of the first stage 3x4 μm transistor with the simulated f_t, f_{max} and NF_{min} (NF_{min} at 33 GHz) including parasitic extraction up to M7.

2.3 Wideband LNA Design

A significant part of the wideband LNA design is the input matching network. Different matching techniques can be applied to achieve the wideband performance shown in Fig. 2.3(a). A standard 2-section L-C network is usually used to achieve a wideband match to a 50 Ω source for design simplicity. However, the realization of the two shunt inductors of 420 pH and 400 pH with high Q results in large-area implementation. A resistive feedback technique can also be used for wideband compact designs, but degrades the LNA noise figure. A T-coil network consisting of two-coupled inductors achieves similar performance to the 2-section L-C network but with the use of smaller inductors and a compact area. The input return loss and NF performance comparison of the three design techniques applied to a single-stage cascode LNA is presented in Fig. 2.3(b). The feadback design achieved the widest bandwidth but with 0.35 dB higher NF compared to the other designs. The T-coil matching has best overall NF at 28-37 GHz and results

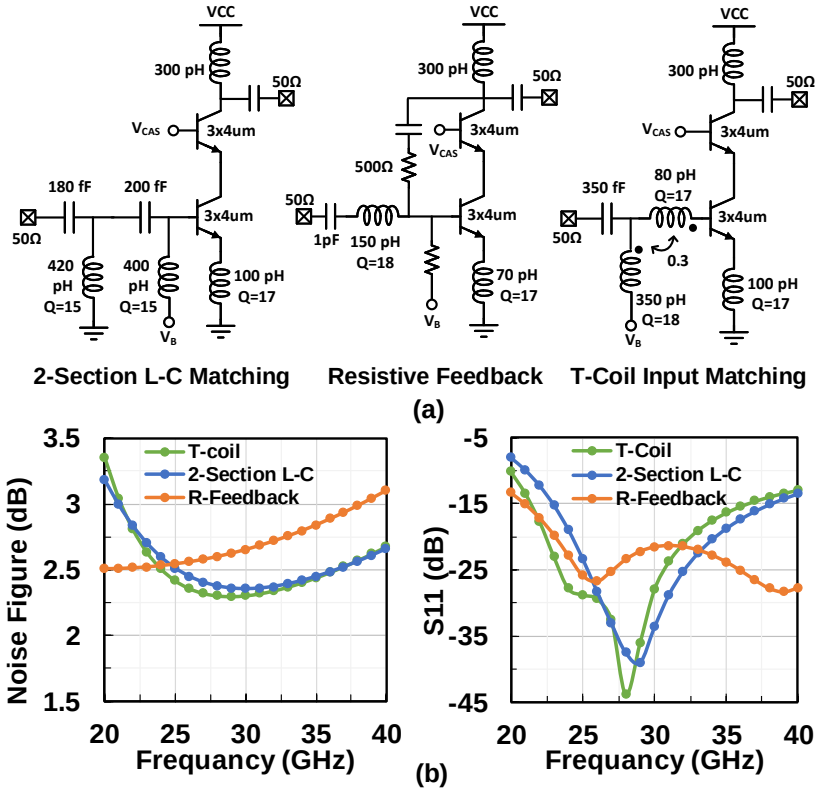


Figure 2.3. (a) Wideband input matching topologies, and (b) NF and input return loss comparison.

in wideband performance.

The LNA is based on three transformer-coupled stages with T-coil input matching network (Fig. 2.4). Transformers are employed between the LNA stages to achieve wideband interstage matching. For high gain and better isolation at 30 GHz, cascode topology is used for each stage instead of the common-emitter (CE) topology. In addition, the cascode design improves the noise and input matching but with small increase in noise contribution due to the cascode device. To cover wideband operation, the gain is staggered between the LNA stages with the last transformer designed to match to 50 Ω load.

The wideband input matching network consist of a degeneration inductor of 60 pH and an asymmetric T-coil network. The two coupled inductors ($L_1 = 55$ pH and $L_2 = 300$ pH with a Q of 20 and 17 at 30 GHz, respectively) result in a high-order matching network with a compact size and a small contribution to the LNA NF. The input impedance at the base of the transistor is

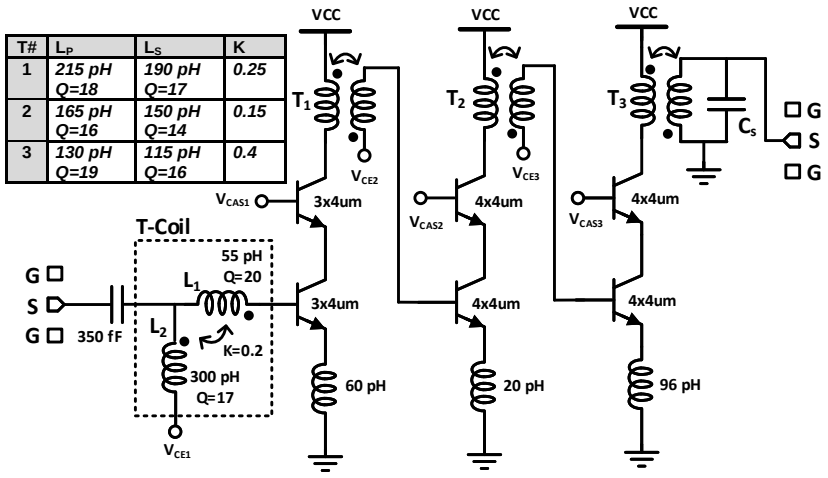


Figure 2.4. Schematic of the transformer-based 3-stage cascode LNA.

transferred to 50 Ω as shown in Fig. 2.5.

The transformers are constructed using transmission-line inductors (L_P and L_S) implemented in the top Aluminum layers (M7 and M6). The overlap between both windings controls the coupling coefficient k. Fig. 2.6(a) presents the layout of the first transformer between stage 1 and 2 in inverting and non-inverting configurations. The inverting configuration results in a wider bandwidth since it mitigates the effect of the feed-forward signal through the parasitic capacitance C_m shown in Fig. 2.6(b), and hence improves the coupled signal at the output port [29]. A T-section model shown in Fig. 2.6(c) is used to design the transformers where the mutual inductance M is defined as:

$$M = k \times \sqrt{L_P L_S} \tag{2.1}$$

By choosing L_P, L_S and the coupling coefficient k, the required impedance transformation is achieved between Z_1 and Z_2. The secondary coils of the interstage transformers are also used for biasing the common-emitter transistors.

The LNA first stage has a wideband gain response centered at 31 GHz with a peak gain of 8 dB to reduce noise contribution from the following stages. This stage is biased at a current density J_{c1} = 0.35 mA/μm which corresponds to the low NF bias point at 33 GHz. Stages 2

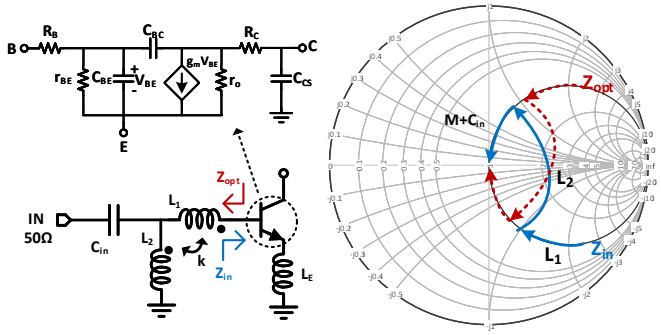


Figure 2.5. Wideband input matching using a T-coil network, and a degeneration inductor with the impedance transformation between Zopt and Zo.

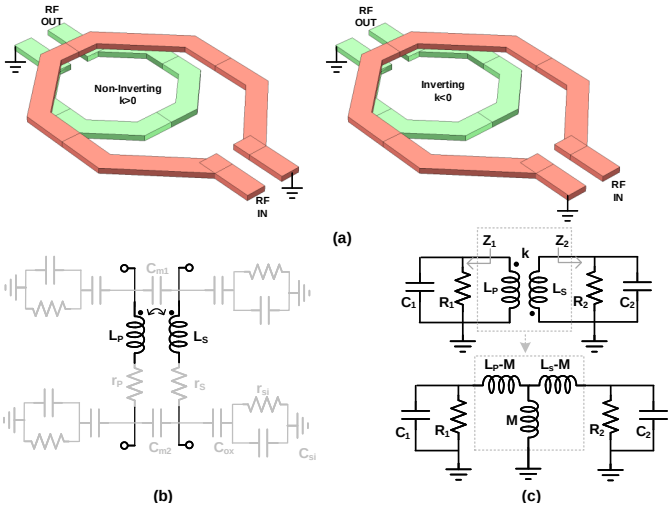


Figure 2.6. (a) Transformer 1 layout in inverting and non-inverting configurations. (b) Transformer lumped-element model. (c) Interstage wideband matching and T-section model.

and 3 also have a current density $J_{c2,c3} = 0.28$ mA/μm to keep a low power consumption. Their gain is staggered across the 3-dB bandwidth, with the second stage covering the high frequency side and the last stage covering the low frequency side to result in a wide flat low NF. In order to provide the gain staggering response, the transformers are designed with values of L_P, L_S and k shown in Fig. 2.4. Degeneration inductors in stages 2 and 3 are employed to provide real part impedance at the base of common-emitter transistors which contributes to enhancing the wideband matching between stages. For the common-base transistors in the cascode stages, the base is connected to the bias pad using a large resistor with a decoupling cap of 8 pF.

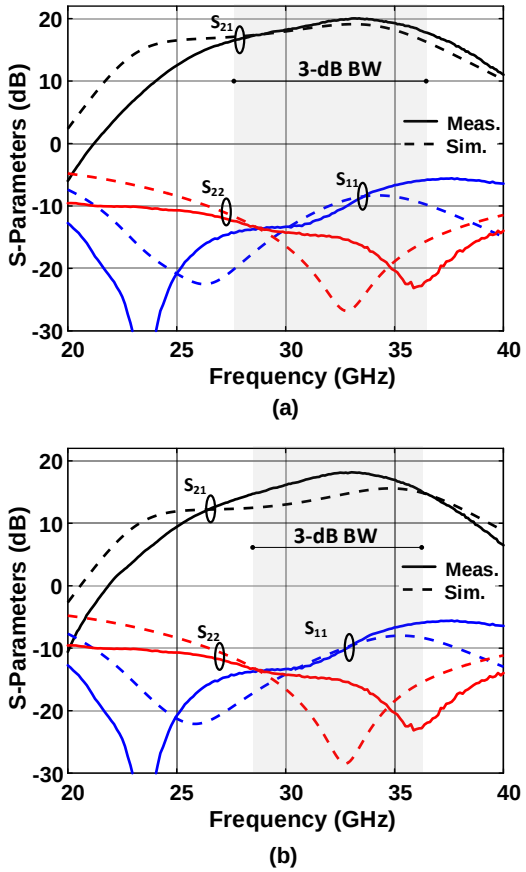


Figure 2.7. Measured and simulated S-parameters for (a) nominal operation (13 mW), and (b) low-power operation (6 mW).

2.4 Measurements

The chip measurements are done on a probe station using the Keysight PNA-X N5247B and calibration to the probe tip. The GSG pad transition and loss is therefore included in the measurements. The small-signal performance is presented in Fig. 2.7(a) for nominal operation with a supply voltage of 1 V. Wideband input matching is achieved at 20-34 GHz as a result of the input T-coil matching network. The small-signal gain (S_{21}) shows a 3-dB bandwidth of 28-37 GHz with a peak gain of 20 dB at 13 mW power consumption. The LNA gain is larger than 15 dB from 26.5 to 38 GHz covering nearly the entire Ka-band. The discrepancy between simulations and measured result is attributed to the transformers-coupling factor discrepancy

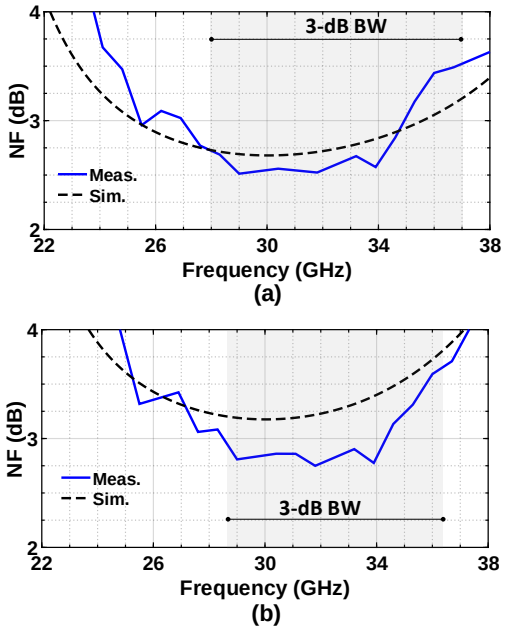


Figure 2.8. (a) NF for nominal-power operation (13 mW). (b) NF for low-power operation (6 mW).

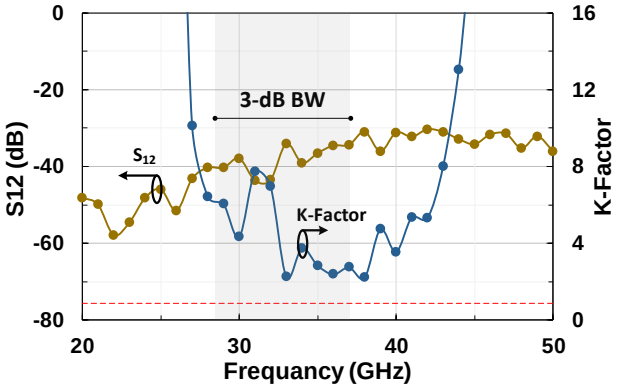


Figure 2.9. Reverse isolation and K-factor.

from EM simulations resulting in a small frequency response shift between the LNA staggered stages. The measured NF, using the PNA-X and calibrated to the probe tip, is 2.5-3.5 dB at 24-37 GHz for nominal operation and agrees with measurements (Fig. 2.8a). In particular, the LNA achieved a NF < 3 dB from 26-35 GHz.

For low-power operation, the supply voltage is reduced to 0.85 V. The LNA achieves a peak gain of 18 dB with a 3-dB bandwidth of 28.8-36.2 GHz and a power consumption of 6 mW

Table 2.1. Comparison with State-of-The-Arts Ka-Band LNAs

Design	This Work	[25] IMS'19	[26] RFIC'18	[30] RFIC'19
Technology	0.18um SiGe BiCMOS	65nm CMOS	0.25um SiGe	22nm CMOS FDSOI
f_c (GHz)	32.5	28	33	33.5
Peak Gain (dB)	20.1/18	18.2	28.5	23/18.2
Frequency (GHz)	28-37/ 28.8-36.2	22-34	29-37	24-43*
BW_{3dB} (GHz)	9/7.4	12	8	19*
In-band NF (dB)	2.5-3.6/ 2.75-3.8	3.9-4.1	3.1-4.1	3.1-3.7/ 3.4-4.3
P_{DC} (mW)	13/5.9	9.5	80	20.5/12.1
FoM (dB)	19/21.1	17	8	21.9/20.6*
Gain/P_{DC} (dB/mW)	1.55/3	1.9	0.36	1.12/1.5
IP_{1dB} (dBm) (at max gain)	-33 @32GHz	-15 @28GHz	-	-24 @30GHz

* 5-dB BW is used

$$FoM = 20log_{10}\Big(\frac{Gain[lin.] \times 3\text{-}dB\ BW[GHz]}{P_{DC}[mW] \times (Min.NF[lin.] - 1)}\Big)$$

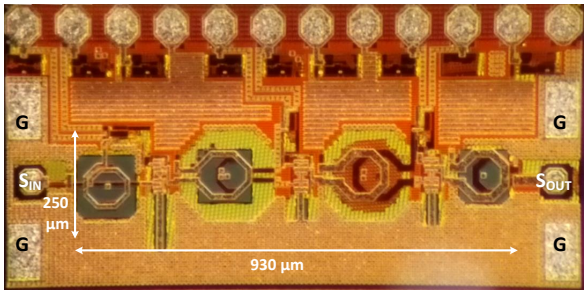


Figure 2.10. Die micrograph of the three-stage LNA (core area: 250 µm x 930 µm).

(Fig. 2.7b). The measured NF is 2.75-3.8 dB showing an increase of only 0.3 dB from nominal power operation (Fig. 2.8b). The NF is < 3 dB from 28.5-34.5 GHz with only 6 mW of power consumption.

The LNA reverse isolation, S_{12}, is lower than -35 dB across the entire 3-dB bandwidth with a k-factor >2 resulting in unconditional stability (Fig. 2.9). The measured input P_{1dB} is -33

dBm at 32 GHz due to the high LNA gain and low power consumption. The signal swing is limited at the output of the second stage as a result of using two high-gain cascode stages with a low-voltage supply prior to the LNA third stage.

Fig. 2.10 presents the die micrograph of the three-stage transformer-based LNA. The core area is 250 μm$\times$930 μm and with a total area 0.23 mm^2 .

A comparison with previous work is shown in Table 5.1. There are many LNA papers in the 22-29 GHz range with excellent performance but few with a center frequency above 30 GHz. The table compares this work with CMOS, SiGe and SOI LNAs above 30 GHz. The LNA achieves high gain at low power consumption with one of the highest FoM when compared with the state-of-the-art. In particular, this technology results in 3 dB of gain per 1 mW of DC power at 33 GHz, which is excellent for low power applications.

2.5 Conclusion

This work presented a three-stage Ka-band LNA utilizing T-coil input matching and transformers to achieve wideband operation and low NF. The SBC18S5 technology is particularly suited for low NF at low power, and such LNAs will reduce the overall system power consumption in large phased-arrays.

Acknowledgment

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Chapter 2, in full, is a reprint of the material as it appears in: A. Alhamed, and G. M.

Rebeiz, “A 28–37 GHz Triple-Stage Transformer-Coupled SiGe LNA with 2.5 dB Minimum NF for Low Power Wideband Phased Array Receivers,” *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2020, pp. 1-4.*. The dissertation author is the primary investigator and author of this paper.

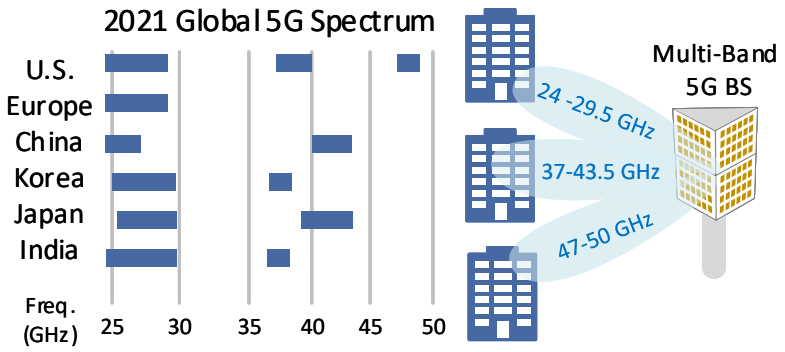
Chapter 3

A Multi-Band/Multi-Standard 15-57 GHz Receive Phased-Array Module Based on 4 × 1 Beamformer IC and Supporting 5G NR FR2 Operation

3.1 Introduction

The increasing demand for high data rate links is accelerating the deployment of mm-wave 5G networks worldwide. Fast wireless access points are being developed with the 5G new radio (NR) standards. As shown in Fig. 3.1(a), a large amount of spectrum at mm-wave frequencies has been assigned for 5G NR Frequency Range 2 (FR2). This raises the need for developing a multi-band/multi-standard solution capable of supporting cross network roaming, interband carrier aggregation, and agile frequency hopping features between different 5G FR2 bands.

Directive communications using affordable phased-arrays has been adopted as a key technology for building 5G-communication systems to overcome the large free space path loss (FSPL) at mm-wave frequencies. These arrays are enabled by narrowband multi-channel low-cost SiGe and CMOS beamformer chips supporting one or two bands in the 5G FR2 [5, 6, 8, 9, 11, 13–15, 17, 22, 23, 31–35]. However, to support multiple 5G bands, 2 or 3 separate beamforming chips are required to build a multi-band phased array system. Due to limited



(a)

NR Band	UL and DL Frequency Range (GHz)	Duplex mode
n257	26.5– 29.5	TDD
n258	24.25 – 27.5	
n259	39.5 – 43.5	
n260	37 – 40	
n261	27.5 – 28.35	

(b)

Figure 3.1. (a) Multi-band base-station and worldwide 5G spectrum snapshot in 2021. (b) 5G NR FR2 operating bands (TS 38.104) [1].

space on the phased array PCB, such an implementation becomes infeasible. Therefore, multiple narrow band phased arrays are employed for multi-band operation with the cost increasing as number of supported bands increases.

Some efforts recently have explored designs that can support dual or triple band operation [3, 18, 20, 21, 29, 36], but mostly limited to an unpackaged beamformer IC implementation or a single channel front-end design. In [29], a dual-band 28/37-GHz 4-element compact hybrid beamforming receiver is reported with low-power performance but relatively high NF. Also, a recent work presented in [3] demonstrated a 26/28/39-GHz low-power receive front-end using two separate receive channels for the 26/28 GHz band and the 39 GHz band and connected to two separate antennas. This approach allows optimizing the receiver performance compared with a wideband design approach but at the expense of increasing the aperture size and routing loss on the phased array PCB. Also, due to the very low-power operation, the reported front-end

has limited linearity performance at peak gain setting.

A wideband phased array with full system implementation supporting interband carrier aggregation and operating at 23.5-29.5 GHz is reported in [16]. Also, a 37-42 GHz phased array system achieving 30-Gb/s data rate is presented in [24]. However, these phased arrays have relatively narrow-band performance (< 25% fractional bandwidth) and can not support all 5G bands at 24.25 GHz to 52.6 GHz.

This work expands on [37] and introduces a low-cost, scalable, multi-band 15-57 GHz phased array module based on a 4-channel RF beamforming chip. System design and analysis of the 8-element phased-array are reported in section 2. The 4×1 Rx beamformer chip architecture and circuit design details are shown in section 3 including wideband matching techniques. Measurements of the packaged beamformer chip are presented in section 4 along with the 8-element module OTA link and phased array patterns measurements.

3.2 Multi-Band Receive Phased Array

3.2.1 Modular Phased Array Architecture

The multi-band system consists of stacked PCBs implemented as linear phased array modules. Each module can support 8 to 16 antenna elements using the 4-channel beamformer chips. For a 64 to 256-element phased array, 16 modules are stacked with their outputs combined using a summing PCB and downconverted to baseband [Fig. 3.2(a)]. Also, a hybrid beamforming system can be built using the stacked linear phased array modules [Fig. 3.2(b)]. The output of each PCB is individually downconverted to the digital domain enabling analog beamforming in one plane and digital beamforming in the other plane with multiple MIMO streams.

3.2.2 4-Channel RF Beamformer Chip

The RF beamforming architecture has been adopted for its low-complexity and ability to eliminate out of beam interference before the mixer, thus relaxing the receiver requirements

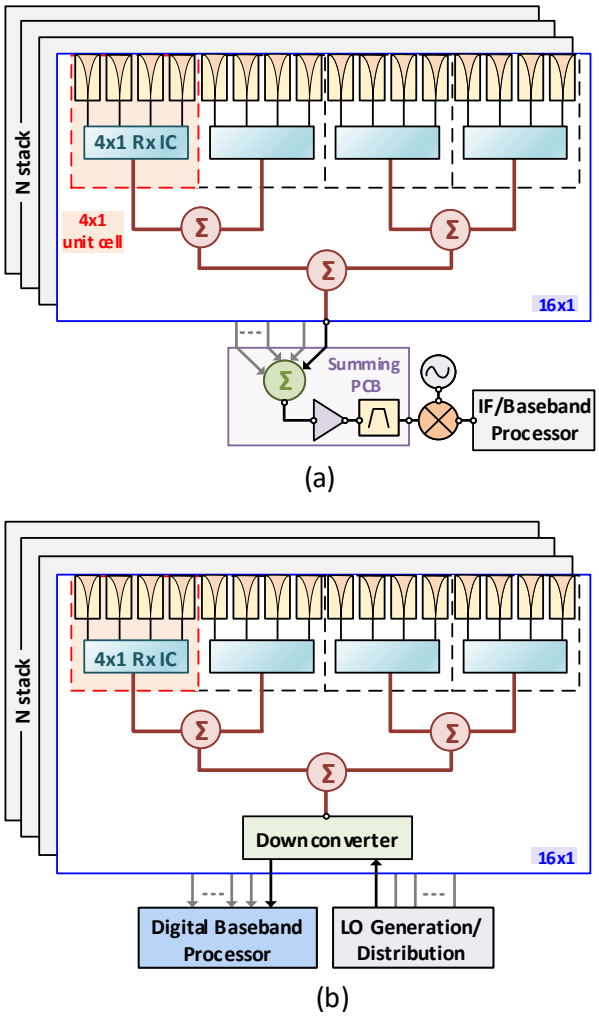


Figure 3.2. 64-elements wideband Rx phased array: (a) Analog beamforming, (b) hybrid beamforming architecture.

[6], [5]. The SiGe chip has 4 channels with differential input ports to connect to wideband differential antennas (Fig. 3.3). A differential channel design also preserves stability and reduces coupling between channels. The RF output signals are combined using a two-stage wideband Wilkinson network. Each channel consist of a three-stage cascode resistive-feedback low-noise amplifier (LNA), 5-bit vector modulator based active phase shifter (PS), 4-bit variable gain amplifier (VGA), and a differential to single ended active stage. This architecture is chosen to minimize the antenna routing length in a linear array, thus improving Rx dynamic range and minimizing calibration requirements.

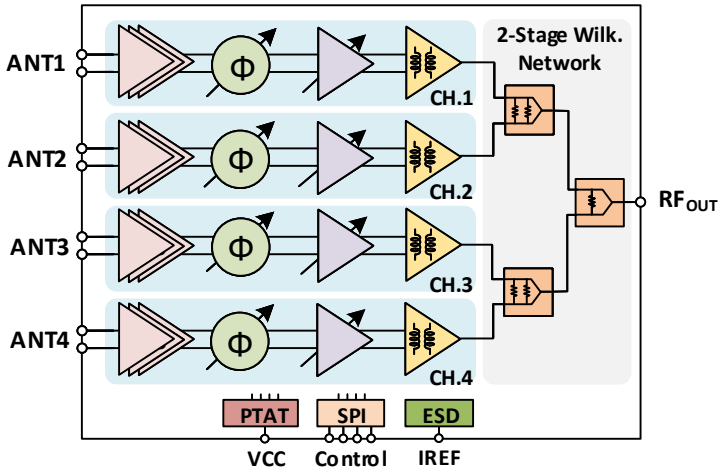


Figure 3.3. Block diagram of the wideband 15-57 GHz 4-channel Rx phased-array beamformer.

3.2.3 Wideband Phased Array Analysis

For N-element phased array ($N_x \times N_y$), the phased array antenna gain is calculated using:

$$G_{Array} = 10\ log_{10}(\frac{4\pi N_x N_y d_x d_y}{\lambda^2}) - L_{ANT} \tag{3.1}$$

Here d_x and d_y are the element-spacing in vertical and horizontal planes, respectively, λ is the wavelength, and L_{ANT} is the antenna and feedline ohmic losses ($L_{ANT} = 0.5$-1 dB). With 0.5λ element-spacing at 54 GHz (2.8 mm), a 64- and 256-element phased arrays achieve a gain of 22.1 and 28.1 dB at 54 GHz respectively [Fig. 3.4(a)]. The phased array 3-dB beamwidth is:

$$\theta_{3dB} = \frac{0.886\lambda}{L\ cos(\theta_s)} \tag{3.2}$$

Here L is the array length ($N_x \times d_x$) and θ_s is the scan angle. The 3-dB beamwidth grows inversely proportional to the frequency and an array of 64- and 256-element achieves a 3-dB beamwidth of $< 27^o$ and 6.8^o respectively at 24.25-52.6 GHz [Fig. 3.4(b)].

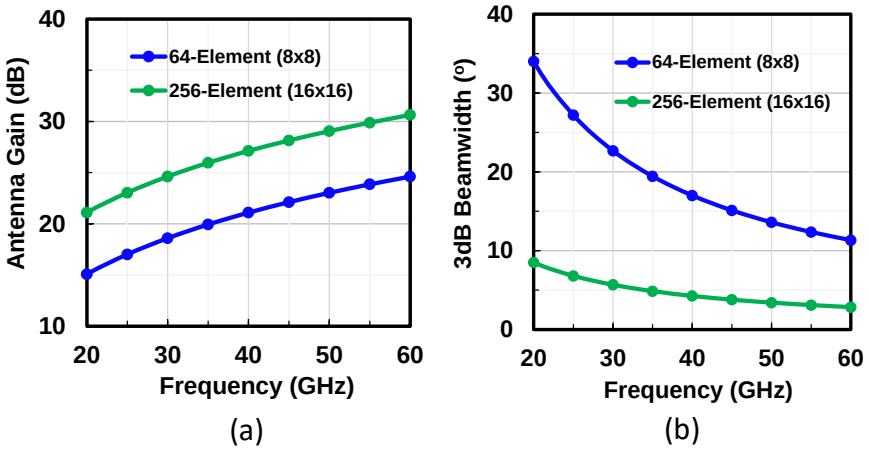


Figure 3.4. (a) Antenna gain and (b) 3-dB beamwidth for 64- and 256-element phased arrays on a $\lambda/2$ grid at 54 GHz (2.8 mm element-spacing).

3.2.4 Multi-band 5G System Consideration

Multi-band 5G mm-wave base stations are generally built utilizing large phased arrays. Table 1 presents the link budget for a 256-element Wideband Rx base station supporting 24-52 GHz frequency range operation with a 300 m line of sight (LOS). The user equipment (UE) is narrowband and three different users are transmitting to the base station at separate frequencies (28, 39, and 47 GHz), each with a linear EIRP of 31 dBm, a typical number in small user equipment. Table 1 shows that the wideband base station with a NF of 5-6.5 dB can receive the UE signals with a high SNR >27 at 300 m and can operate at 1.2 Gb/s using 64-QAM waveforms.

3.2.5 8-Element Module Design

The building block for an 8×8 (64-element) array is an 8×1 linear phased array module composed of two 4×1 beamformer chips [Fig. 3.5(a)]. The Rx electronic gain (G_{Rx}) of this module is defined from the antenna port to the common port and includes only the ohmic losses of the Wilkinson combiner network [38]. The beamformer chip has an electronic gain of 25 dB resulting in $G_{Rx} =$ 18.5-22 dB for the 8-element module at 20-50 GHz.

The NF of the Rx beamformer chip is 4.7-6.5 dB at 20-50 GHz. A single-sideband (SSB) high-linearity down-converter with 8-10 dB NF is typically used at the sum point of the

Table 3.1. Multi-band Micro Base Station and UEs Link Budget

Carrier Frequency (GHz)		28	39	47
Channel BW (MHz)		200		
Distance (m)		300 (LOS)		
FSPL (dB)		110.9	113.8	115.2
KTB (dBm)		-91		
Tx (UE)	Array size (N)	8-elements		
	$G_{Array\text{-}Tx}$ (dB)*	13.5		
	P_{out}/Element (dBm)	8		
	EIRP (dBm)**	30.5		
Rx (BS)	Array size	256-elements		
	$G_{Array\text{-}Rx}$ (dB)*	23	25.6	27.3
	Rx NF (dB)	5	6	6.5
SNR (dB)		28.6	27.3	27.1
		EIRP-FSPL+$G_{Array\text{-}Rx}$-NF-KTB		

* G_{Array} is calculated as shown in eq. 1 with $d = \lambda/2$ at center frequency for UEs

** EIRP= P_{out}+10log(N)+$G_{Array\text{-}Tx}$

phased-array [39–41]. The system NF is calculated to be 4.8-6.7 dB using the Friis equation where the first block is the beamformer chip followed by the combining network and the down-converter [Fig. 3.5(a)]. As the array size increases, the combining network ohmic loss and NF contribution is increased. Also, the gain preceding the down-converter drops resulting in a higher NF contribution from the down-converter. A beamformer with 24-26 dB gain is sufficient to maintain low-system NF when scaling the array size to 64- and 256-elements as shown in Fig. 3.5(b). This is with a total estimated ohmic loss due to the Wilkinson network, transmission lines, and RF connectors of 10 dB and 14 dB for the 64- and 256-elements phased arrays, respectively, at 30-40 GHz.

The power received by each channel is calculated as:

$$P_{ch} = EIRP + 10\ log_{10}(\frac{\lambda}{4\pi R})^2 + G_{ANT} \tag{3.3}$$

Here $EIRP$ is the effective isotropic radiated power by the transmitter, R is the link distance, and G_{ANT} is the antenna unit cell gain propotinal to $1/\lambda^2$ (G_{ANT} = -3 to 4 dB at 20-50 GHz including

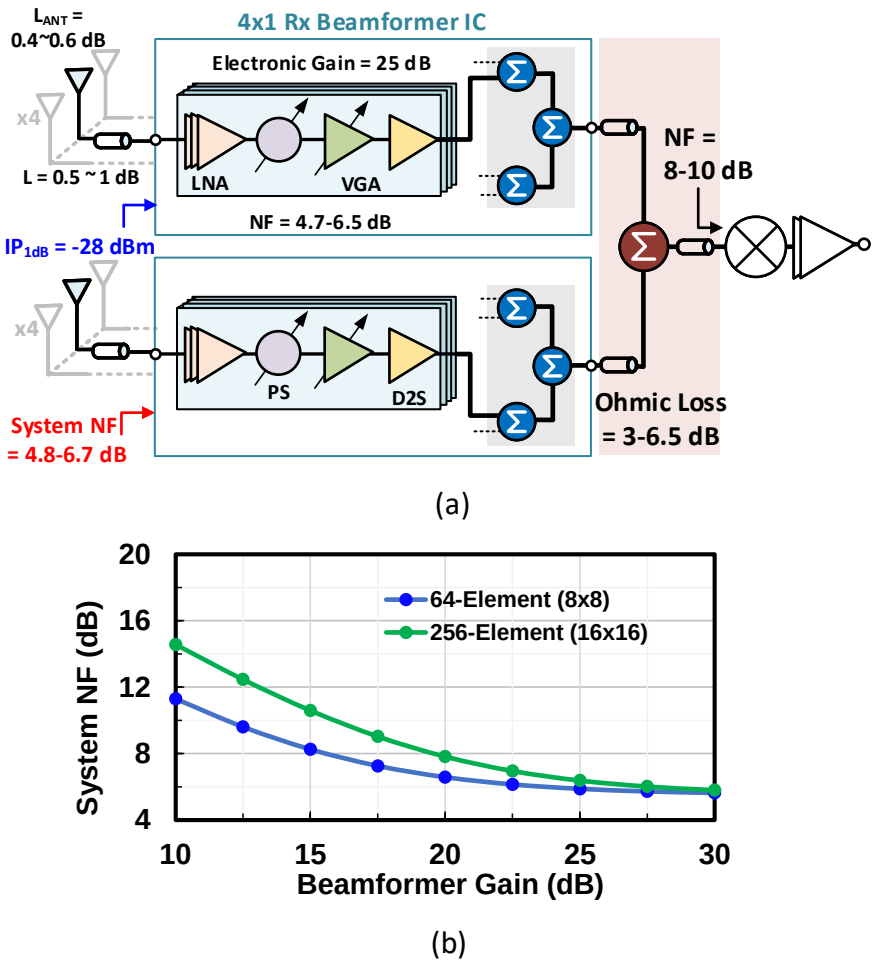


Figure 3.5. (a) System design of the 8-element phased array module based on two 4×1 receive beamformer chips (hybrid phased-array system assumed). (b) System NF versus Rx beamformer electronic gain.

the antenna and feedline ohmic loss). Using a base station EIRP of 55 dBm at R= 50-300 m, the received power by each element is -56 to -37 dBm. An input P_{1dB} of -26 dBm/ch. is sufficient to handle interferers from a nearby transmitters.

3.3 Circuit Design

The beamformer is designed using T-Semi SiGe BiCMOS 5th generation technology [2]. This process has 7 Aluminum layers, with a top metal layer thickness of 2.8 µm. A 3×4 µm SiGe HBT transistor has a simulated f_{max} and f_t of 305 and 272 GHz, respectively, at a current

density of 1.5-2 mA/μm with parasitic extraction to top metal layer. The simulated NF_{min} at 33 GHz is 1.1 dB at a current density of 0.25-0.28 mA/μm.

3.3.1 Low-Noise Amplifier

The differential LNA is designed using three cascode stages with a total gain of 18-20 dB which is sufficient to suppress the noise from the following blocks (Fig. 3.6). Each of the three stages is stagger-tuned to result in a wideband flat response [42], [43]. The first two stages are implemented with a current source at the emitter node for better common mode rejection. To avoid limiting the LNA linearity, the last stage is implemented as a pseudo-differential amplifier allowing for high voltage swing at the output node.

Resistive feedback and asymmetric T-coil bandwidth extension techniques are employed with a degeneration inductor to realize noise and power matching at the LNA input [Fig 6(a)]. The drawback of using resistive feedback at the input stage is an increase in the LNA NF. However, light resistive-feedback using a 700 Ω resistor achieves the required wideband matching with a 6.8% increase in NF [4].

The LNA devices (T1-T6) are sized at 3×4 μm with the first stage biased at 0.4 mA/μm for low noise operation and with a sufficient gain to suppress noise contribution from the following stages. The current source is designed to be controlled using a DAC circuit allowing for gain reduction to improve the Rx channel linearity and reduce the power consumption.

The inter-stage matching network is based on capacitively coupled resonators synthesizing a high-order band-pass filter [44]. A wideband performance is realized by separating the two complex poles of the matching network at the expense of increased in-band gain ripples. Feedback resistors are also employed in stages 2 and 3 to improve the response flatness and reduce the in-band ripples [Fig. 3.6(b)]. The three-stage resistive feedback LNA consumes 32.6 mA from a 2 V supply and has an input P_{1dB} of -18.5 dBm at 35 GHz.

The LNA S-parameters measurements are done on a test cell achieving a peak gain of 18 dB with a 3-dB bandwidth of 15.2-60 GHz. The simulated and measured S-parameters are

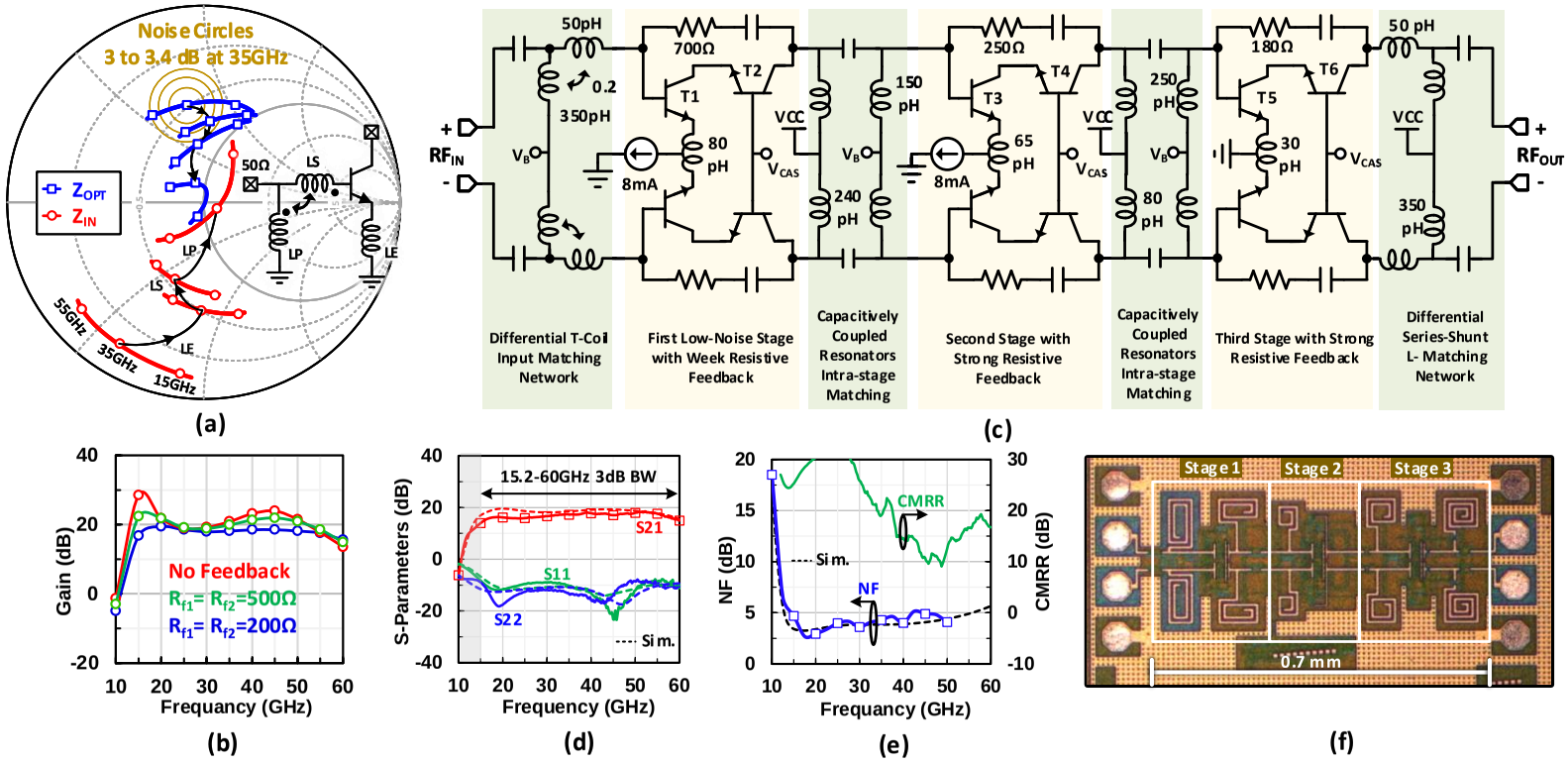


Figure 3.6. (a) Wideband noise and power matching network. (b) LNA gain response at different feedback resistor values. (c) Wideband 3-stage R-feedback LNA. (d) LNA S-parameters measurements and simulations. (e) LNA measured NF and CMRR. (f) Die micrograph.

presented in Fig 6(d) demonstrating a good agreement between measured and simulated gain (S_{21}) and return loss (S_{11} and S_{22}). The NF measurement is done in a single-ended (SE) mode with one port-terminated using 50 Ω. The difference in NF when the LNA is driven SE and when it is driven differentially is compensated based on Cadence simulation. The LNA achieves 2.95, 3.8, and 4.1 dB NF at 20, 30, and 50 GHz with a 4 dB mean NF at 15-50 GHz [Fig. 3.6(e)].

3.3.2 Wideband Phase Shifter

This block consists of a wideband differential quadrature all pass filter (QAF) network followed by a vector modulator [Fig. 3.7(a)]. An active phase shifter topology is selected for wideband response with small area and low insertion loss.

Among several I/Q generation circuits such as a passive poly phase filter [45], transformer-based poly-phase network [46], [47], the differential QAF is the most suitable for wideband I/Q generation in the RF path [Fig. 3.7(b)] [48]. The capacitive loading effect on the QAF network by the vector modulator is substantial especially at mm-wave frequencies. To overcome this issue, the QAF is designed with a relatively low characteristic impedance ($R = 50\ \Omega$) which increases the QAF capacitor (C), thus reducing the loading effect as it is proportional to C_{Load}/C [48]. Also, a series resistance ($R_s = 20\ \Omega$) is added to the QAF to reduce the network Q and its sensitivity to the loading capacitor C_{Load}. This increases the input impedance of the QAF network making it easier for the LNA stage to drive the PS block. Also, the series resistance increases the insertion loss by 3-4 dB and the phase shifter noise contribution, but results in I/Q signals with +/-3^o at 15-55 GHz. The simulated frequency response of the QAF network is presented in Fig. 3.7(d) and (e).

Series and degeneration inductors at the base and emitter of the I/Q VGAs ($L_S = 40$ pH and $L_E = 50$ pH) are used to enhance matching between the QAF network and the vector modulator. These inductors also work as a compensation network minimizing the I/Q amplitude errors over a wide bandwidth. The I/Q VGA transistors are 6 μm and biased with current sources I_I and I_Q = 6.5 mA. The differential I/Q weighted signals are combined at the output node and

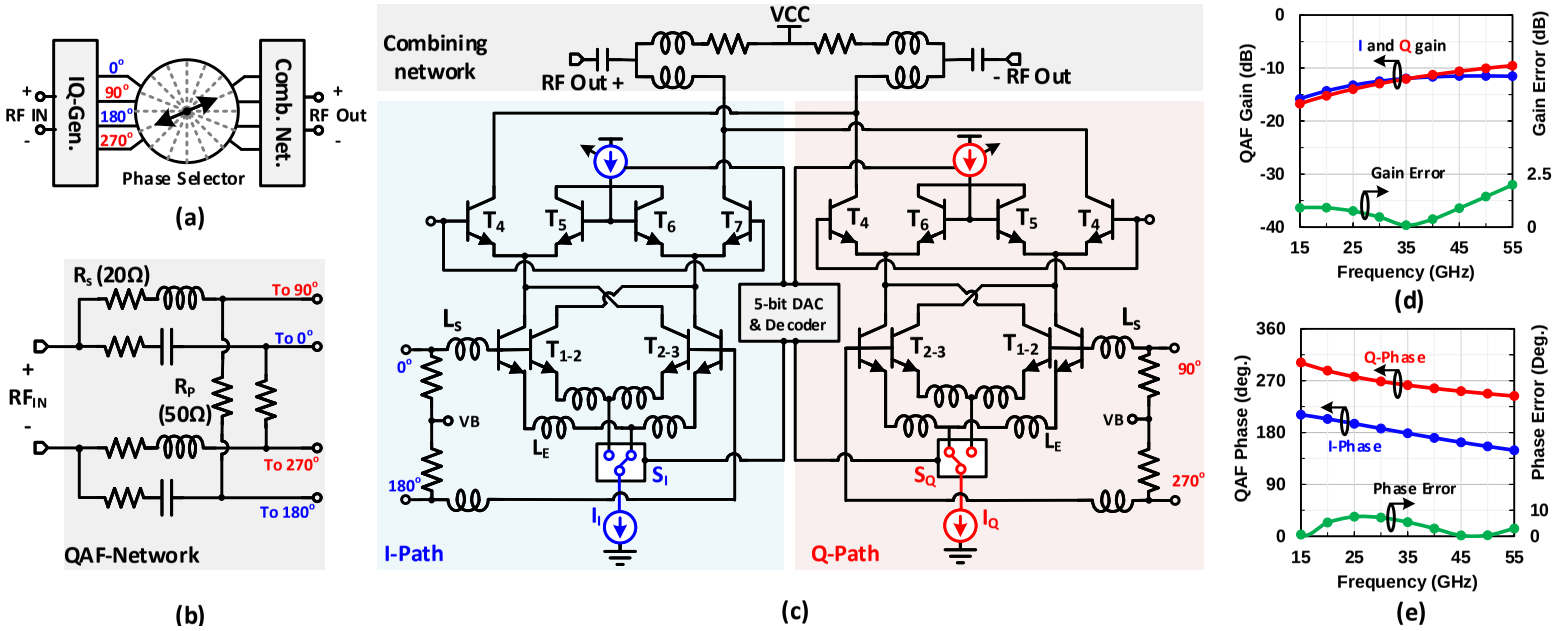


Figure 3.7. (a) Wideband phase generation, (b) QAF network, (c) wideband vector modulator circuit design. QAF network simulated (d) gain response and (e) phase response.

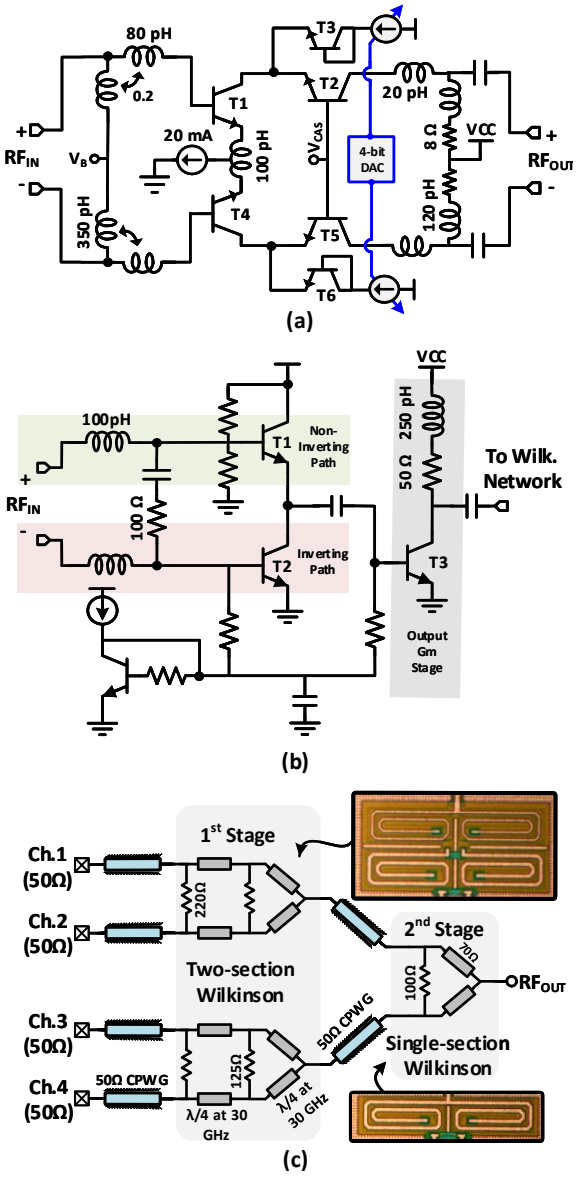


Figure 3.8. (a) 4-bit VGA with cascode current control, (b) active D2S stage, and (c) 2-stage Wilkinson network.

connected to a series-shunt peaking network synthesizing wideband gain response [Fig. 3.7(c)].

The simulated RMS phase error is <5.6^o with an RMS gain error < 1.5 dB at 17-50 GHz. The mean gain over the 32 states is -4.5 dB and is mostly attributed to the series resistor in the QAF network. The phase shifter input P_{1dB} is -1 dBm and consumes 26 mW from a 2 V supply. The NF is 16 dB at 35 GHz and the area utilization is 0.15 mm^2. High linearity performance after the 18 dB LNA gain is required to maintain -28 dBm system input P1dB.

3.3.3 Variable-Gain Amplifier

The VGA design is also based on current-steering topology presented in Fig. 3.8(a). An asymmetric T-coil input matching network is implemented to realize wideband matching to the phase shifter block. The current is steered from the cascode stage with a 4-bit DAC control circuit resulting in a phase change < 4^o with 10-dB gain control at 15-57 GHz. The low phase change is critical in order to calibrate any gain mismatch between phased array elements with a simple calibration algorithm. The VGA is biased using a 20 mA current source at the emitter node and has an input P_{1dB} of -6.5 dBm at the maximum gain state of 10 dB at 35 GHz.

3.3.4 Active Differential to Single-Ended Stage (D2S)

The VGA differential output signal is connected to an active in-phase combining stage to produce a single-ended output signal before the on-chip Wilkinson network. The D2S is based on a common-collector and common-emitter transistors for combining the differential signal in-phase at the common node [Fig. 3.8(b)] [49]. As the D2S is the last block in the Rx channel, it is designed to have high linearity with an input P_{1dB} of -1 dBm to achieve an overall high input P_{1dB} for the Rx channel. The output signal drives a common-emitter gain stage with inductive peaking network at the output node rendering a wideband match to a 50 Ω load.

3.3.5 Combining Network

The channels are combined using a wideband 2-stage Wilkinson network [Fig. 3.8(c)]. This network consists of a compact single-section Wilkinson combiner followed by a 2-section wideband Wilkinson. The λ/4 transmission lines (TL) are implemented using M7-layer for signal and M4/M5-layer for ground to synthesize the required characteristic impedance. The 100 Ω, 125 Ω, and 220 Ω are realized using Titanium Nitride (TiN) resistors available in the SBC18S5 technology. The 4:1 Wilkinson network results in a simulated isolation (S_{32}) of > 20 dB and insertion ohmic loss of 3-4 dB at 15-55 GHz including all connecting transmission lines.

The complete Rx path has a simulated gain of 26-27 dB with a 3-dB BW of 15-57

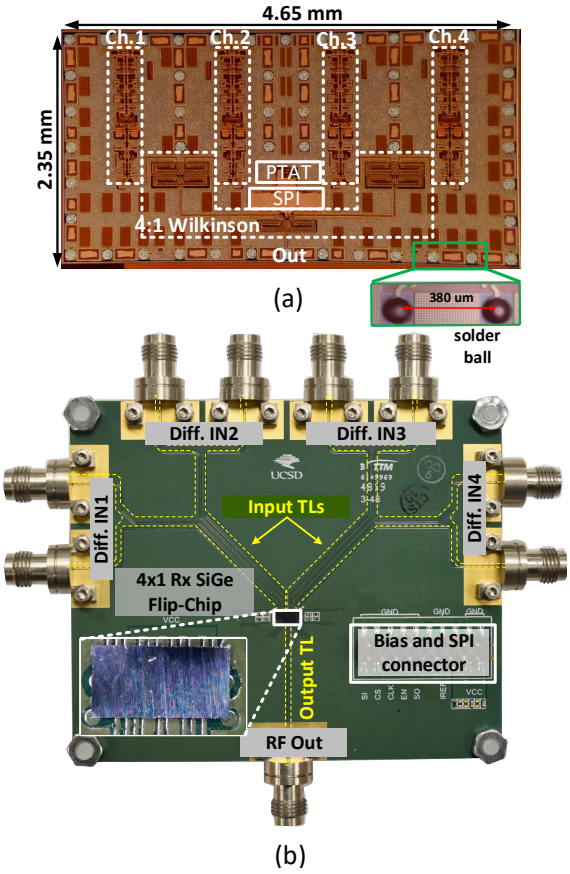


Figure 3.9. (a) 4-channel Rx wideband beamformer chip (4.65 mm × 2.35 mm) and (b) 4×1 flip-chip evaluation board.

GHz and a NF of 4-6.4 dB. The system simulated input P_{1dB} is -24 to -29 dBm with a power consumption of 242 mW from a 2 V supply. The relatively high power consumption is required to maintain linearity over a wide bandwidth. However, the DC power consumption can be reduced to 170-180 mW using current-bias control as shown in the next section.

3.3.6 4-Channel Beamformer Measurements

The single channel core size is 0.45 mm × 1.7 mm and the chip area is 11 mm^2 limited by the 380 µm-pitch bumps for wafer-level chip-scale packaging [50], [51]. The 4×1 Rx beamformer die micrograph is presented in Fig. 3.9(a).

The Rx beamformer chip is flipped on an evaluation PCB [Fig. 3.9(b)] and the packaged chip performance is measured using a Keysight PNA-X N5247A. The input and output trans-

mission lines losses up to the chip ports are de-embedded from measurements. All following results are referenced to the beamformer chip ports interfacing with the PCB with the bumps loss included in the measurements. The S-parameter measurements and electronic gain of each channel is presented in Fig. 3.10(a) showing a peak electronic gain of 25 dB and a 3-dB bandwidth of 15-57 GHz. The electronic gain of the chip is defined as the measured S_{21} between the output common port and a single input port plus 6 dB to compensate for the additional loss in the Wilkinson network as only one channel is energized. The measured reverse isolation is > 40 dB with a wideband input and output matching (S_{11} and S_{22}) <-10 dB at 10-60 GHz. The gain and phase difference between the beamformer channels across frequency normalized to channel 1 are shown in Fig. 3.10(b) and (c). The 4 channels track each other with a maximum of +/-1 dB gain and +/- 5^o phase variations at 15-57 GHz allowing for easy calibration.

3.4 Measurements

A gain control of 18-dB is measured and presented in Fig. 3.10(d). Fine resolution gain steps is achieved using the VGA and LNA gain control. The measured 5-bit phase response is shown in Fig. 3.10(e) and optimized at 35 GHz using an extra trim bit in the phase shifter. This trim bit can be also used to optimize the phase shifter performance at different frequencies. Therefore, the phase shifter operates in 20-25 GHz instantaneous bandwidth regions. The RMS phase error < 5.6^o in Fig. 3.10(e) is obtained when optimizing at 20 GHz (in green), 35 GHz (in blue) and 50 GHz (in red). The 5-bit phase response for the 20 and 50 GHz trim-bit settings are not shown for brevity.

The large-signal measurements of IP3 and P_{1dB} versus frequency are presented in Fig. 3.10(f). An input P_{1dB} of -30 to -23 dBm is measured at 20-50 GHz. The beamformer gain versus P_{in} is shown in Fig. 3.10(g) at 35 GHz. The Rx channel input P_{1dB} can be improved by lowering the LNA gain using current control and results in 3.5 dB improvement in input P_{1dB}. This also reduces the gain by 5 dB and the power consumption by 68 mW (to 172 mW per

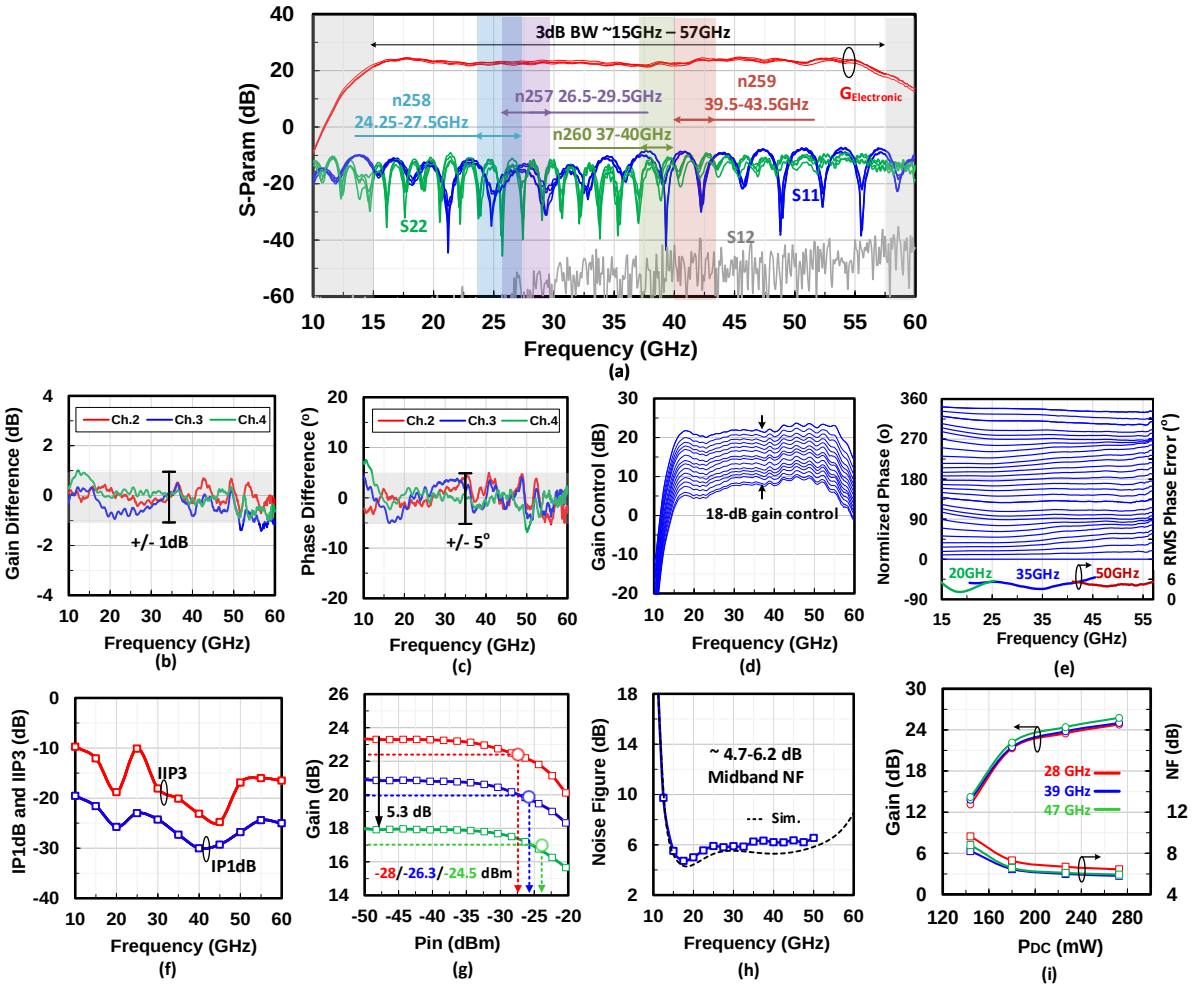


Figure 3.10. Measured (a) S-parameters for 4 channels, (b,c) gain and phase variations between channels normalized to ch. 1, (d) 18-dB gain control, (e) normalized 5-bit phase control, (f) IP1dB and IIP3, (g) gain versus Pin for different LNA gain states, (h) noise figure, and (i) gain and NF versus power consumption.

channel) with a 2 dB increase in the channel NF.

The measured chip NF is presented in Fig. 3.10(h). This measurement is done in SE mode and the difference in NF when the beamformer is driven SE and driven differentially is compensated based on Cadence simulation. The chip has a NF of 4.7-6.2 dB at 20-40 GHz with a mean NF of 5.9 dB at 15-50 GHz. Gain and NF are also measured versus current consumption level to assess the chip low-power performance [Fig. 3.10(i)]. Using chip bias current control, the power consumption per channel is reduced from 242 mW to 180 mW per channel to operate

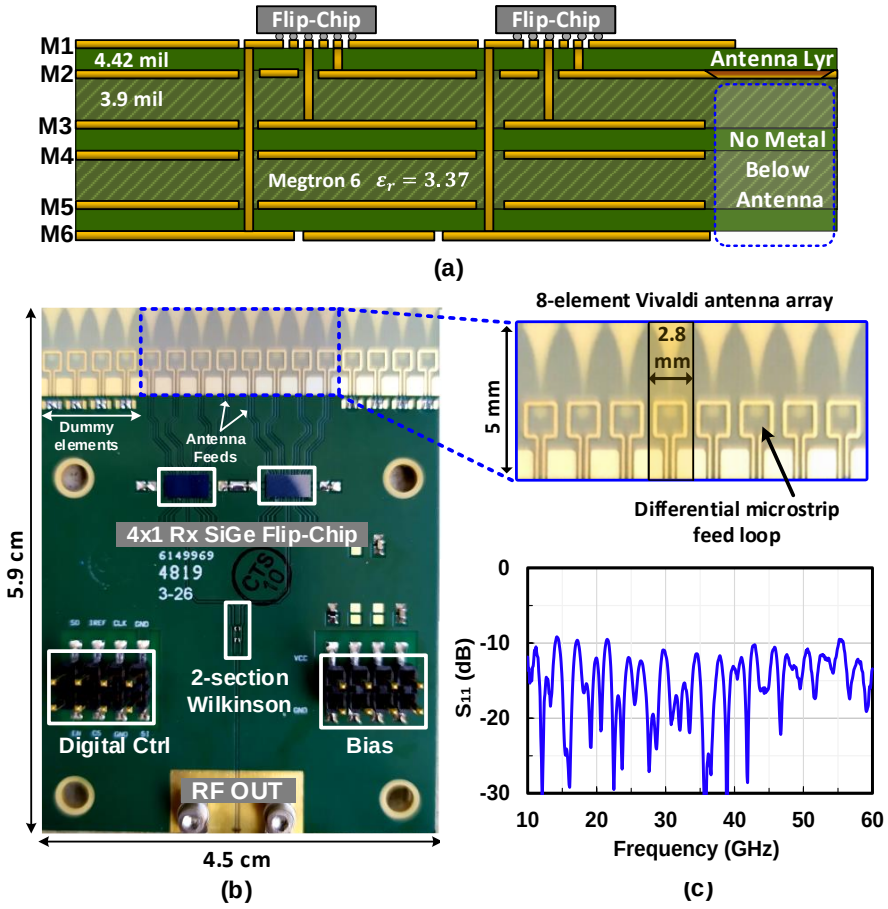


Figure 3.11. (a) PCB stackup for the 8-element Rx module, (b) top view of the array PCB with flip-chip beamformer ICs and PCB integrated Vivaldi antennas, (c) measured antenna return loss.

in low-power mode with a gain of 21.5 dB and a NF of 6.5 dB at 39 GHz.

3.4.1 8×1 Phased Array Measurements

To demonstrate a multi-band phased array, an 8-element module is built on a low-cost 6-layer Megtron-6 PCB (ε_r= 3.26 - 3.37). Two 4×1 beamformers chips are connected to a differential wideband Vivaldi antenna array [52–57] and the outputs are combined using a wideband 2-section Wilkinson network on the PCB (Fig. 3.11). The Vivaldi antenna feed is implemented using the M1 layer as a microstrip loop interfacing to a 100 Ω edge-coupled grounded coplanar waveguide transmission line. The antenna unit-cell aspect ratio is 2.8 mm × 8.1 mm including the microstrip feed loop and is shown in Fig. 3.11(b). The measured antenna

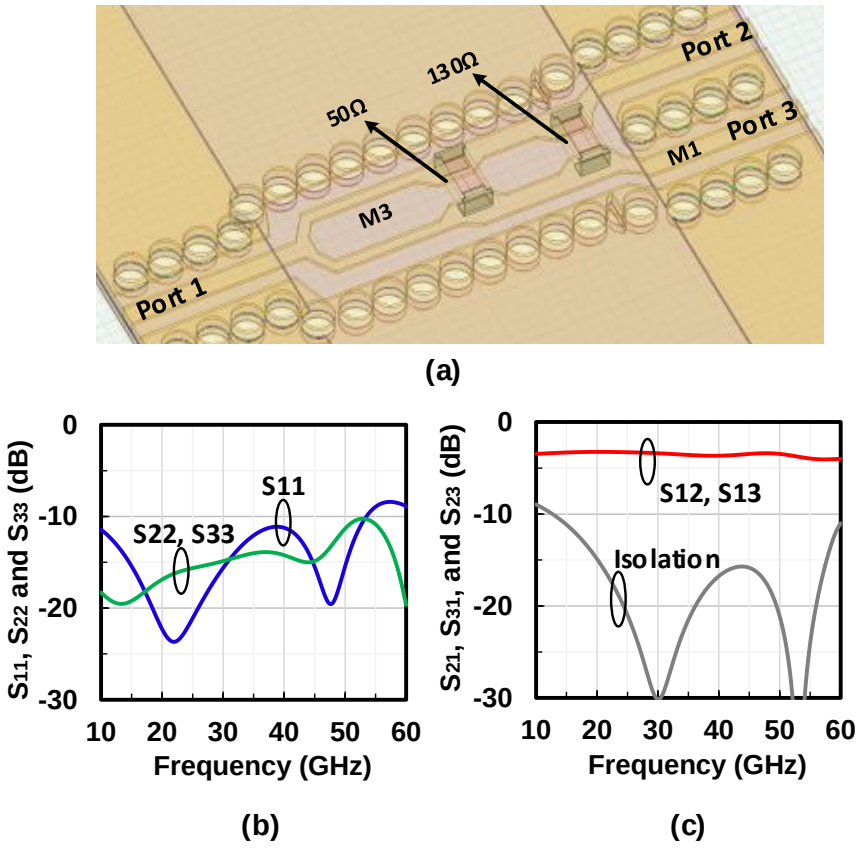


Figure 3.12. (a) 2-stage on PCB Wilkinson design, (b) simulated return loss, and (c) isolation and insertion loss.

input impedance using test PCB shows a wideband differential 100 Ω match at 10-60 GHz [Fig. 3.11(c)]. The simulated Vivaldi antenna unit cell has a gain of -4.2 to 3.9 dB at 15-55 GHz including the differential feed. The 8-element array can scan up to 60^o with $|S_{11}| < -10$ dB in E- and D-planes and < -7 dB in the H-plane at 15-55 GHz.

The PCB Wilkinson network built using M1 and M3 layers consist of 2 sections for broadband operation [Fig. 3.12(a)]. Surface mount resistors with values of 130 Ω and 50 Ω are used. The simulated Wilkinson insertion loss is 0.5-1.5 dB and the isolation is > 15 dB at 20-57 GHz. The simulated return loss is presented in Fig. 3.12(b) and the insertion loss (including the 3-dB Wilkinson loss) is shown in Fig. 3.12(c).

The Rx phased array is tested inside an ETS-5700 anechoic chamber at 1.2 m with a wideband horn that can operate up to 52 GHz [Fig. 3.13(a)]. The far-field S_{21} is measured

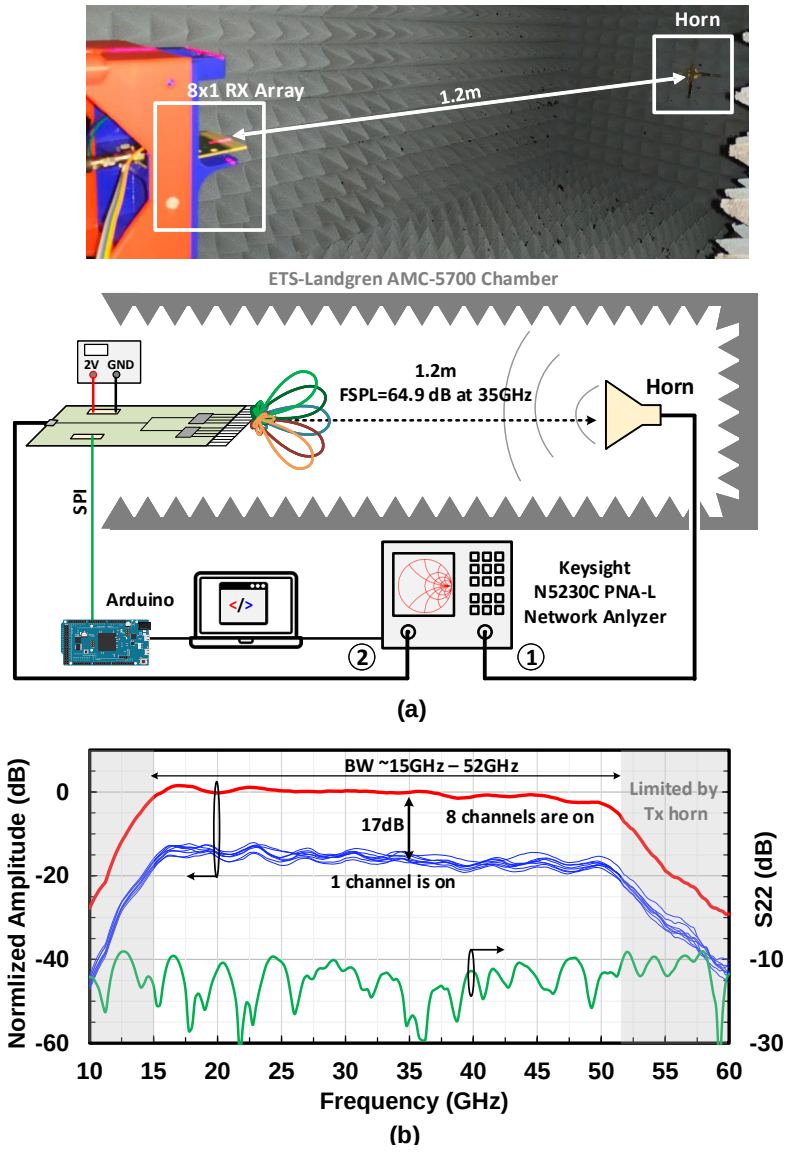


Figure 3.13. (a) Measurement setup and photo of the 8×1 Rx array, and (b) measured S-parameters when a single channel is turned on and when all 8 channels are on.

with one channel turned on at a time, and then when all channels are energized. Fig. 3.13(b) presents the array frequency response with an S_{21} 3-dB bandwidth of 15-52 GHz limited by the measurement setup. The antenna array gain has a positive slope versus frequency and adds up with ohmic losses in the PCB transmission lines, Wilkinson network, and RF connector resulting in an overall flat S_{21} array response. The gain ripples in the individual channels response are mainly due to antenna coupling as the antenna is designed to optimally operate when all channels

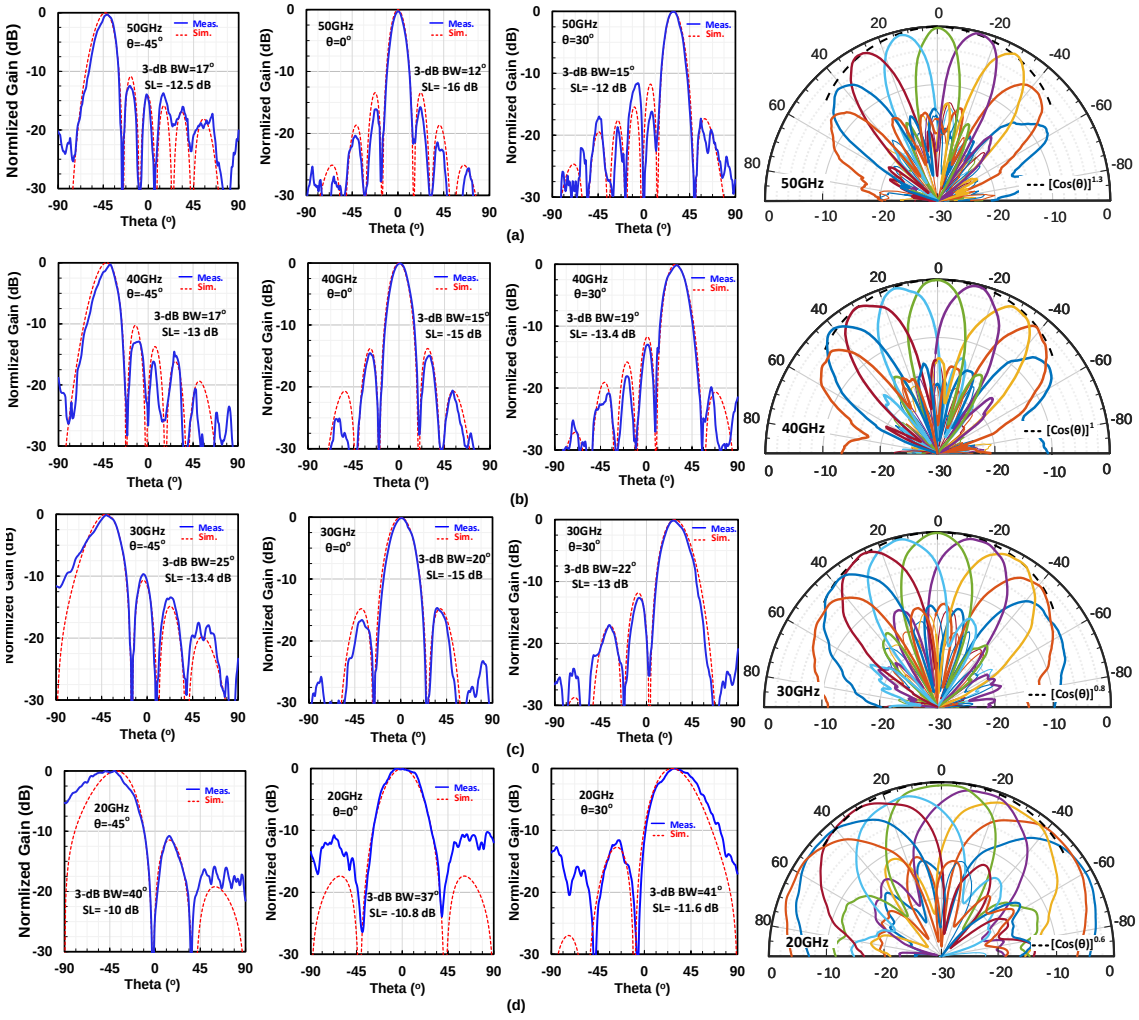


Figure 3.14. Measured patterns with -55^o to 55^o scan angles at: (a) 50 GHz, (b) 40 GHz, (c) 30 GHz, and (d) 20 GHz

are energized. An S_{21} increase of 17 dB is measured when all channels are energized. The 1 dB difference from the ideal 18 dB gain increase (20 *logN*) is due to the non-ideal Vivaldi antenna operation when only a single channel is turned on.

The 8-element phased array patterns are measured at 50, 40, 30, and 20 GHz (Fig. 3.14). The array is first calibrated at these frequencies by measuring the amplitude and phase response of every channel and compensating the difference using the channel phase shifter and VGA. Then the phase shift per element is set at each frequency for scanning purposes. The measured patterns match the simulated ideal patterns well at all frequencies and scan angles. The array

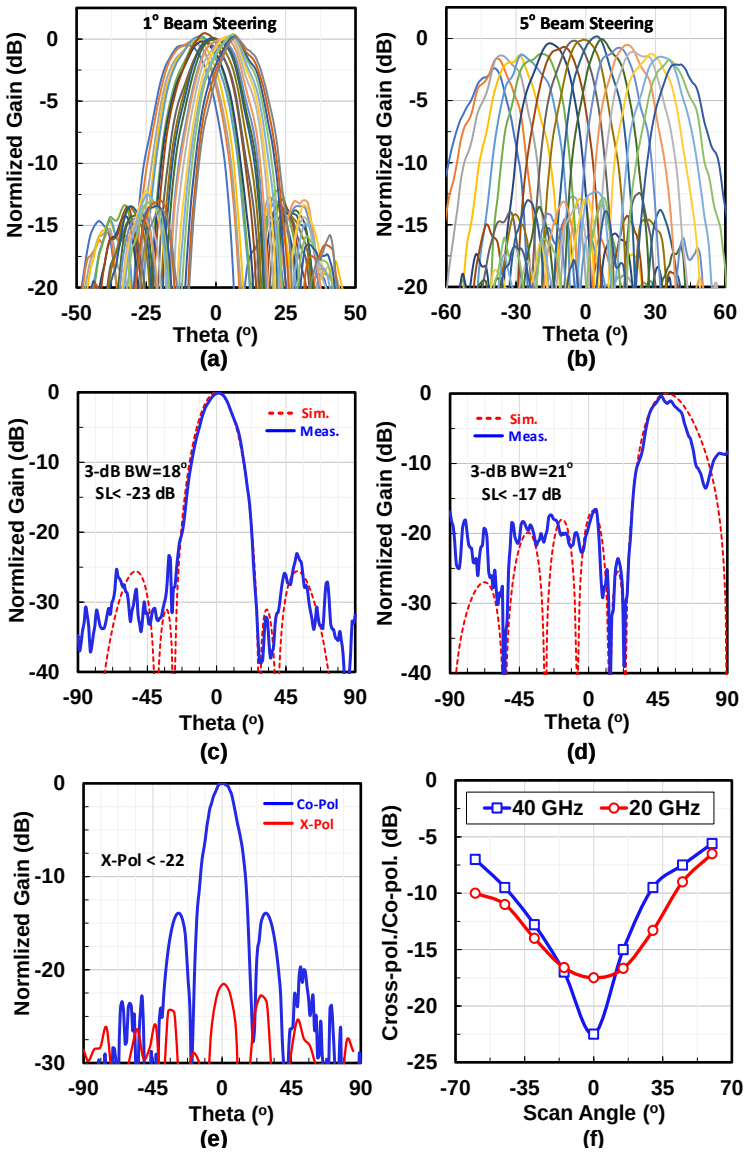


Figure 3.15. Fine resolution beam steering: (a) 1^o, and (b) 5^o. 8-dB raised-cosine taper: (c) at 0^o scan and (d) at 60^o scan. (e) measured co- and cross-pol. at 40 GHz in the E-plane (azimuth). (f) Cross-polarization level versus scan angle at 40 and 20 GHz.

patterns at 50 GHz follows the simulated element factor ($cos(\theta)^{1.3}$), and the array gain is 3.9 dB lower at +/- 45^o scan angle. The 3-dB beamwidth at boresight is 12^o and increases to 15^o at 30^o scan angle. The sidelobe levels are <-12 dB over all scan angles without taper.

The phased array module pattern is also measured at 40, 30, and 20 GHz to demonstrate multi-band performance capability [Fig. 3.14(b)-(d)]. The module is able to scan from -55^o to

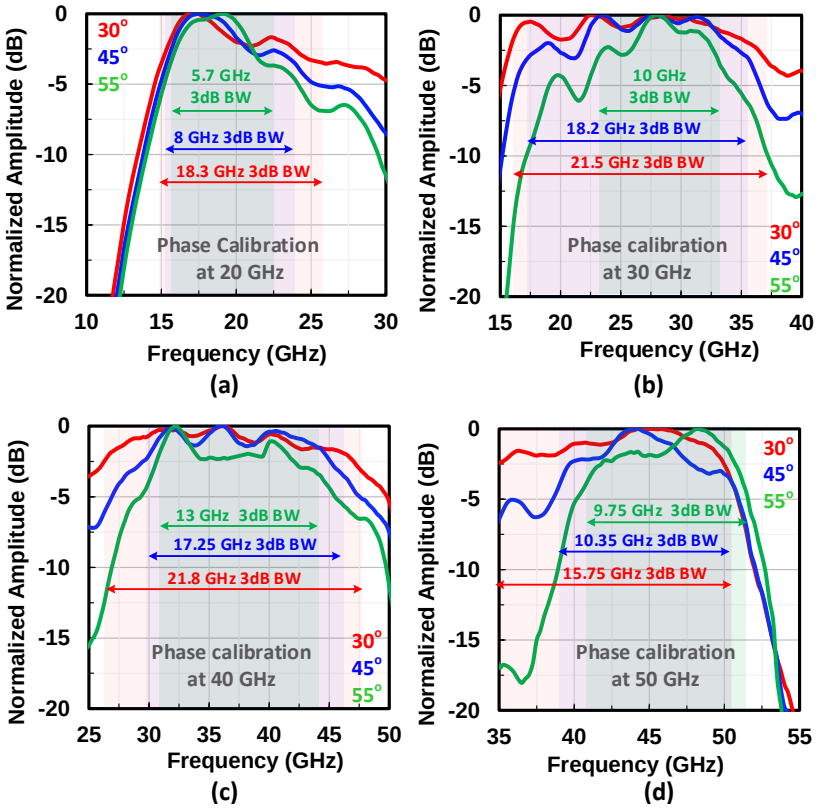
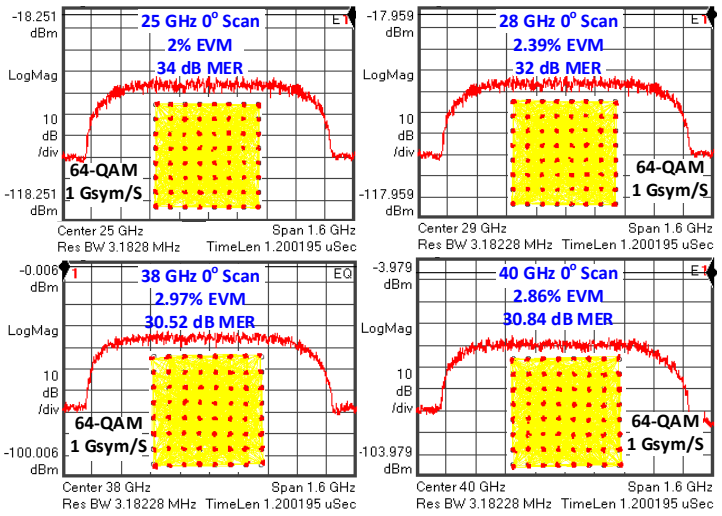


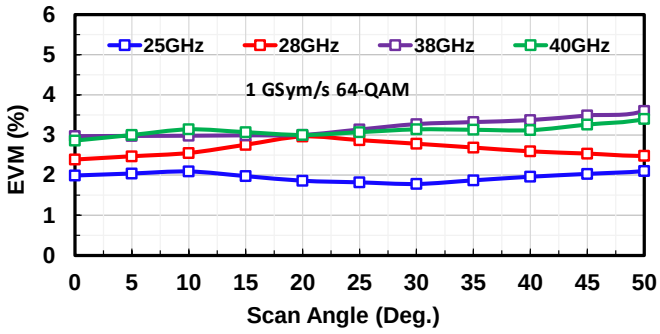
Figure 3.16. Measured frequency response with 30^o, 45^o, and 55^o scan at (a) 20 GHz, (b) 30 GHz, (c) 40 GHz, and (d) 50 GHz.

55^o with a slidelobe level < -12 dB at all scan angles, and with a 3-dB beamwidth of 15^o and 20^o at 40 and 30 GHz, respectively. The beam is also steered at 20 GHz with <-10 dB sidelobe level and 3dB beamwidth of 37^o. Note that the patterns at 20 GHz are much wider than 50 GHz. This is due to the antenna spacing of 0.5λ at 54 GHz, which results in an antenna spacing of only 0.19λ and an array size of 1.49λ at 20 GHz. This is a fundamental property of wideband arrays, and narrow beamwidths at the minimum frequency can only be achieved by building large arrays.

The phased-array beam can be steered in fine angular resolution as described in [58]. The beam is steered in 1^o and 5^o steps at 40 GHz [Fig. 3.15(a) and (b)]. To reduce the sidelobe levels, 8-dB raised cosine taper is applied to the array elements using VGA control. The measured tapered patterns at 40 GHz are presented in Fig. 3.15(c) and (d) at 0^o and 55^o scan angles,



(a)



(b)

Figure 3.17. (a) Measured constellation and EVM performance with 1 GSym/s 64QAM modulation at 25, 28, 38. 42 GHz. (b) EVM performance versus scan angle from 0-50^o.

respectively showing slidelobe level <-23 dB at boresight and <-17 dB at 55^o scan angle. The co- and cross-pol. patterns are measured at 40 GHz and at uniform illumination showing a cross-pol. level <-22 dB [Fig. 3.15(e)]. The cross-pol. level relative to the co-pol. is also plotted versus scan angle at 20 and 40 GHz [Fig. 3.15(f)]. The high cross-pol. level at wide scan angles in the E-plane is a normal characteristic of the Vivaldi antenna array [59–61].

The frequency response at 20, 30, 40, and 50 GHz and with scan angles of 30^o, 45^o, and 55^o is presented in Fig. 3.16(a)-(d). In each case, the phase was set at the center frequency and the array S_{21} was measured in the far field. A wide 3-dB instantaneous bandwidth of 15.75-21.8 GHz at 30^o scan, 8-18.2 GHz at 45^o scan, and 5.7-13 GHz at 55^o scan is attained at 20-50 GHz.

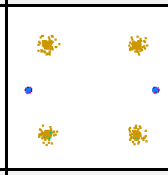
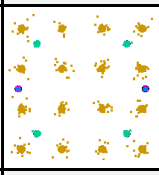
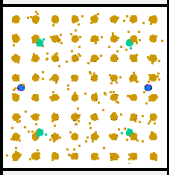
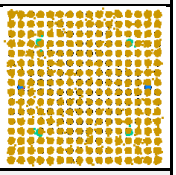
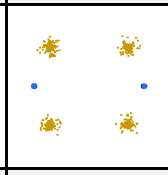
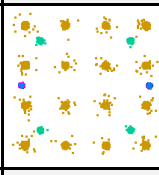
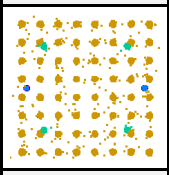
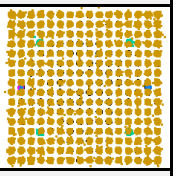
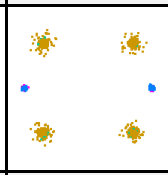
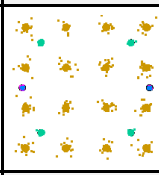
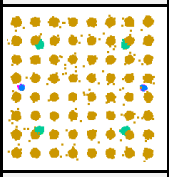
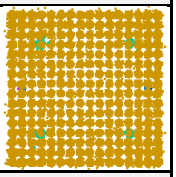
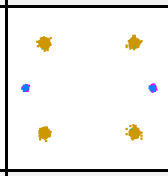
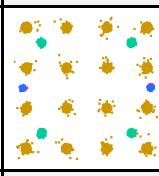
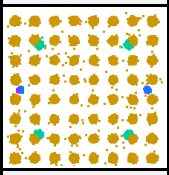
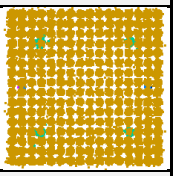
Modulation	QPSK	16-QAM	64-QAM	256-QAM
BW (MHz)	400	400	400	400
Constellation (25 GHz)				
EVM (%)	1.53	1.55	1.59	1.66
Constellation (28 GHz)				
EVM (%)	1.71	1.73	1.77	1.78
Constellation (38 GHz)				
EVM (%)	2.39	2.45	2.5	2.56
Constellation (42 GHz)				
EVM (%)	2.57	2.63	2.7	2.76

Figure 3.18. Measured 1.2 m OTA constellation and EVM performance using 8-element Rx phased array module and wideband horn antenna.

3.4.2 EVM Measurements

A 1.2 m link setup is used to measure the EVM performance of the 8-element phased array with 1 GSym/s single-carrier 64-QAM modulation (α= 0.35 and PAPR = 7.7 dB) at multiple-bands (25, 28, 38 and 40 GHz). A microwave signal generator (Keysight M9384B VXG) is used to generate the complex-modulated signals, and a 63-GHz real-time oscilloscope (Keysight DSOZ632A) with the VSA software is used to capture the signal and extracts the constellations and EVMs. The measured constellation and EVM at normal incidence is presented in Fig. 3.17(a) and shows a data rate of 6 Gb/s with < 3% EVM at all bands. Fig. 3.17(b) demonstrates the Rx EVM performance when scanning the beam up to 50 degrees. The measured EVM is < 3.6% at 25, 28, 38, and 40 GHz.

5G NR signals with 400-MHz channel bandwidth in QPSK, 16-QAM, 64-QAM, and 256-QAM are generated using Keysight M9384B VXG. At the Rx array common port, a Keysight UXA spectrum analyzer is used as the signal analyzer to evaluate the constellations and EVM. The measured constellations and EVMs at 25, 28, 38, and 42 GHz are summarized in Fig. 3.18. Data transmissions of up to 256-QAM is supported by this array. The measured EVMs are <1.66% at 25 GHz, <1.78% at 28 GHz, <2.56% at 38 GHz, and <2.76% at 42 GHz demonstrating excellent multi-band 5G NR FR2 operation.

A comparison with the state of the art 5G FR2 mm-wave phased arrays is presented in Table 2. This work achieves the widest bandwidth covering multiple bands from 15-57 GHz. The beamformer chip achieves a realized gain of 25 dB with 4.7-6.8 dB NF at midband and -30 to -23 dBm input P_{1dB}. The beamformer can operate at low-power mode with 180 mW/ch. and 21.5 dB gain with a NF of 5.1-7.4 dB. The 8-element phased array module is capable of scanning at -55^o to 55^o at 15-57 GHz.

3.5 Conclusion

This work presented a 4×1 beamformer chip with state-of-the-art performance. Compared with reported narrow-band 5G beamformers, the proposed design covers the entire 5G NR FR2 spectrum with a slightly higher NF and power consumption. An 8-element 15-57 GHz multi-band phased-array receive module is built using two 4×1 beamformers on a low-cost PCB. The scalable test module demonstrated an ultra-wideband performance with multi-band beam scanning capabilities. A single-carrier mode data rate of 6 Gb/s in 64-QAM modulation is demonstrated using the 8-element phased array module at 1.2 m distance. 5G NR standard compliant packets of up to 256-QAM are supported with 400-MHz channel bandwidth and <2.76% EVM at all 5G FR2 bands.

Table 3.2. Performance Comparison of mm-Wave Phased Arrays For 5G NR FR2

		Wideband/Dual-Band Beamformers					Narrow-Band Beamformers					
Design		This work		[16]	[29]		[24]	[8]	[14]	[6]	[15]	[17]
Technology		0.18 um SiGe BiCMOS		0.18 um SiGe BiCMOS	65-nm CMOS		0.18 um SiGe BiCMOS	65-nm CMOS	28-nm CMOS	0.18 um SiGe BiCMOS	65-nm CMOS	65-nm CMOS
Frequency (GHz)		15-57		23.5-29	27-29.75	35-38.75	37-42	39	37-40	28.4.4-29.4	28	28
Fractional BW (%)		117		22.6	9.7	10.2	12.6	-	7.8	3.46	-	
Architecture		4×1 Rx RF-PS		2×2 Tx/Rx RF-PS	4×1 Rx Hybrid		2×2 Tx/Rx RF-PS	2×2 Tx/Rx LO-PS	8×1 Tx/Rx RF-PS	2×2 Tx/Rx RF-PS	8×1 Tx/Rx RF-PS	8×1 Tx/Rx LO-PS
Integration/Chip		Beamformer		Beamformer	Full receiver		Beamformer	Full transceiver	Beamformer	Beamformer	Beamformer	Full transceiver
Phase Resolution (bit)		5		6	-	-	6	0.05°	5	6	0.4° RMS error	0.04° RMS error
Gain Control (dB)		18		26	-	-	25	-	10.2	14	-	-
Gain (dB)		25	21.5	19	33 (CG)	26.5 (CG)	26	3 (CG)	41.9	20	17	10 (CG)
Midband NF/ Path (dB)		4.7-6.2*	5.1-7.4*	5.5	5.7* (NF_{min})	8.5* (NF_{min})	5.5	7.7	6-7.6	4.6	4.2-5	4.1*
IP1dB (dBm)		-30 to -23		-19	-30	-23	-28	-22	-36 to -44	-22	-	-
P_{DC}/Ch. In Rx Mode (mW)		242	180	156	52.5		150	125	78.5	130	112.5	150
Chip Area (mm^2)		11		12.5	4.5		N/A	12	17.2	11.75	12	12
Phased Array Measurements												
Array size		8×1		8×8	4×1 (probe meas.)		8×8	16×4	4×4	8×4	4×16	8
Polarization		Single		Single	Single		Single	Single	Dual	Single	Dual	Single
5G Multi-Band Operation		Yes		Yes	Yes		-	-	-	-	-	-
OTA Distance (m)		1.2		1.38	-		1	1	-	5	1	5
Scan Range, Az (o)		+/- 55		+/- 60	+/- 60		+/- 60	+/- 40 (4×1 array)	+/- 45	+/- 45	+/- 50	+/- 50
SC. Meas.	**Constellation**	64-QAM		64-QAM	CW		64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM
	Data Rate	6 Gb/s		4.8 GB/s	CW		12 GB/s	2.4 GB/s	0.6 GB/s	3 Gb/s	2.4 Gb/s	4.8 Gb/s
	EVM (%)	1.7 at 25GHz and 3 at 38 GHz Rx EVM		3.5 Tx EVM	CW		3.3 Tx EVM	3.1 Tx-Rx EVM	3.2 Tx-Rx EVM (single Ch.)	4.46 Tx-Rx EVM	1.99 Tx-Rx EVM	1.78 Tx-Rx EVM
5G NR Evaluated		QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW		-	-		-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	64-QAM OFDM, 100MHz BW	-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW

* w/o TRx switch

Acknowledgment

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Chapter 4

A Multi-Band 16-52 GHz Transmit Phased-Array Employing 4 × 1 Beamforming IC With 14-15.4 dBm Psat For 5G NR FR2 Operation

4.1 Introduction

The pace of mm-wave communication systems development is accelerating and is motivated by the rapid deployment of 5G networks worldwide to meet the high data-rate demands. Several mm-wave bands have already been standardized as part of the 5G new radio frequency range 2 (NR FR2) including n257 band (26.5-29.5 GHz), n258 band (24.25-27.50 GHz), n259 (39.5-43.5 GHz), n260 band (37-40 GHz), and n261 band (27.5-28.35 GHz) [62]. Also, several regions globally started or planned auctions in FR2 for 26, 39, and 47 GHz bands. This widespread spectrum requires a multi-band/multi-standard solution capable of supporting current and future bands and enabling key features such as network roaming and interband carrier aggregation.

Compared to sub-6 GHz 5G operation, the 24.25-52.6 GHz bands suffer from higher free space path loss (FSPL). Therefore, directive communications based on affordable phased-arrays has been employed as a key technology for building mm-wave 5G-communication systems. Also, advanced SiGe and CMOS processes result in low cost, high yield, and low power while

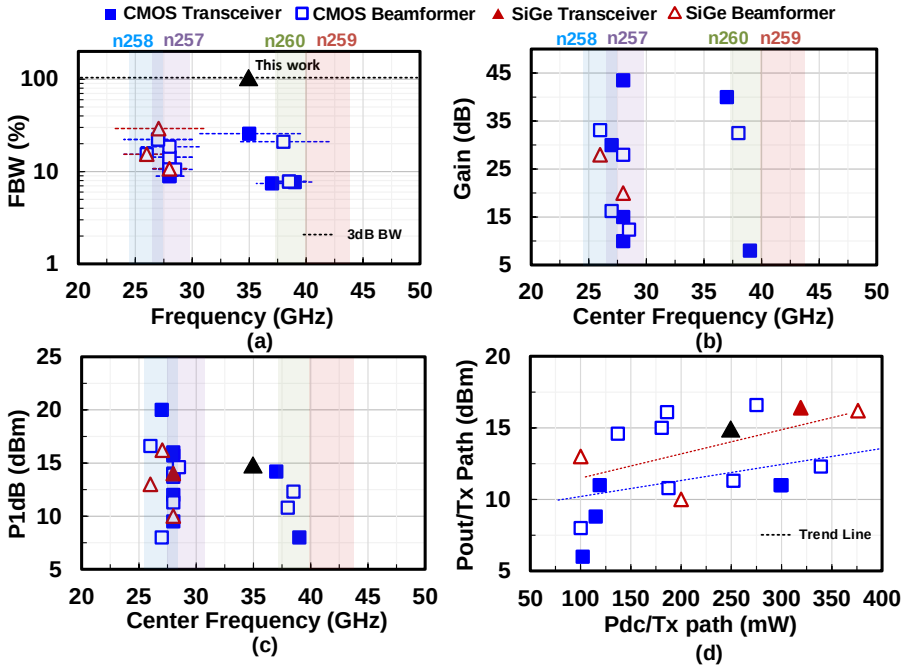


Figure 4.1. (a) Fractional bandwidth (b) gain/channel (c) P_{1dB}, and (d) Pout vs. Pdc of recently reported beamformers and phased array transceivers targeting 5G FR2 bands.

providing unparalleled integration level and digital processing capabilities. It is therefore a perfect candidate for 5G phased array radios for base stations and user equipment [63–65].

Multiple papers have demonstrated excellent phased-array systems targeting relatively narrow-band operation at the n257, n258 or n260 band (Fig. 4.1). The fractional bandwidth (FBW) defined as $(f_2 - f_1)/f_c$ is limited to $< 25\%$ by both the phased array system and beamformer circuit design. Therefore, enhancements to the architectural and circuit levels are required to realize a single wideband multi-octave phased array solution capable of 5G FR2 multi-band support.

This work is an expanded version of [66] and presents a transmit (Tx) multi-band phased array module based on a 4×1 beamformer chip. Wideband system and chip architectures are reported in section 2. An in-depth analysis of the power amplifier and key blocks is carried out in section 3. The packaged beamformer IC measured results are presented in section 4. Experiments using the 8-element phased array Tx module including wideband pattern and effective isotropic radiated power (EIRP) measurements are reported in section 5. The chapter concludes with a

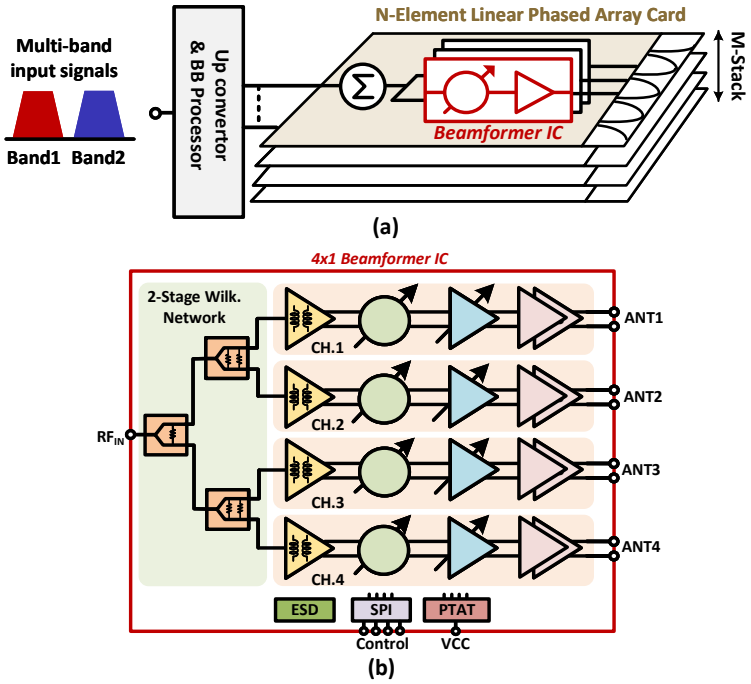


Figure 4.2. (a) $N \times M$ wideband phased array based on stacked linear phased array modules. (b) Block diagram of the wideband 4-channel Tx phased-array beamformer.

comparison with the state-of-the-art.

4.2 Multi-Band Phased-Array

4.2.1 System Considerations

The proposed design employs a slat array configuration utilizing linear phased array PCB modules [Fig. 4.2(a)]. This architecture is selected to enable the design of end-fire Vivaldi antenna arrays commonly used in ultra-wideband systems [67]. A two-dimensional $N \times M$ phased array can be implemented by stacking M modules with each having N number of linear antenna elements. The $N \times M$ selection is set by the EIRP, scanning, and beamwidth requirements. The EIRP for N-element phased array is:

$$EIRP = 10\ log_{10}(N) + G_{ANT} + P_{Ch} \tag{4.1}$$

Table 4.1. Multi-band base station and UEs link budgets

Link Budget Case		A: 64-element base station			B: 256-element base station		
Carrier Frequency (GHz)		28	39	47	28	39	47
Channel BW (MHz)		400			400		
Distance (m)		100 (LOS)			300 (LOS)		
FSPL (dB)		101.4	104.3	106.9	110.9	113.8	115.4
KTB (dBm)		-88			-88		
Narrowband Rx UEs	Array size (N)	8-elements			8-elements		
	$G_{ANT\text{-}RX}$ (dB)*	13.5			13.5		
	NF (dB)**	4.5	5.8	6.5	4.5	5.8	6.5
Wideband Tx Base Station	Array size (N)	64-elements			256-elements		
	$G_{ANT\text{-}TX}$ (dB)*	16.5	19.6	20.3	22.5	25.6	26.3
	P_{out}/Element (dBm)***	5			5		
	EIRP (dBm)****	39.6	42.7	43.4	51.6	54.7	55.4
SNR (dB)		35.2	34.1	31.5	37.7	36.6	35
		EIRP-FSPL+ $G_{ANT\text{-}RX}$ -NF-KTB					

* G_{ANT} is calculated as shown in eq. 2 for narrowband UEs with $d = \lambda/2$ at center frequency
** NF values are based on recent published data
*** Average output power **** Calculated as shown in eq.1

P_{Ch} is the output power per channel and G_{ANT} is the phased-array antenna gain. For N-element array ($N_x \times N_y$), the gain is defined as:

$$G_{ANT} = 10\, log_{10}(\frac{4\pi N_x N_y d_x d_y}{\lambda^2}) - L_{ANT} \tag{4.2}$$

Here d_x and d_y are the element-spacing in vertical and horizontal planes, respectively, λ is the wavelength, and L_{ANT} is the antenna and feedline ohmic losses ($L_{ANT} = 0.5$-1 dB). With 0.46λ element-spacing at 54 GHz (2.54 mm), a 64– and 256–element phased arrays achieve a gain of 21.3 and 27.3 dB at 54 GHz, respectively

For mm-wave 5G operation, the regulatory limits set a maximum EIRP of 75 dBm/100 MHz for fixed base stations, 55 dBm for transportable stations, and 45 dBm for mobile stations [68]. Base stations are based on 64- and 256-element phased arrays which will cover 100–300 m radius, and have a peak EIRP of 55–65 dBm [68]. This corresponds to a 14–16 dBm output power per channel. An example link budget between a multi-band base station and multiple narrowband user-equipment (UE) is shown in Table 1. For case A with a 64-element phased-array, an SNR > 32 dB can be realized with an average Pout of 5 dBm/ch. and 100 m line of sight (LOS). For

case B with a 256-element phased array, an SNR > 35.5 dB is achieved with the same average Pout/ch. and 300 m LOS. For an 8×8 (64-element) array, an 8×1 linear phased array module composed of two 4×1 beamformer chips is required. The design details and analysis of this module are presented in section 5.

4.2.2 Wideband Tx Beamformer Architecture

Multiple beamforming architectures such as digital beamforming [19], local oscillator (LO) beamforming [17], and radio frequency (RF) beamforming [9] have been demonstrated. For wideband operation at mm-wave frequencies, RF beamforming lends itself as the most suitable one due to its low complexity as discussed in [6].

The 4×1 Tx beamformer architecture is presented in Fig. 4.2(b). The RF input signal is divided using a wideband 1:4 Wilkinson network and distributed to 4 RF beamforming channels. Each channel consists of an active balun, 5-bit analog adder-based phase shifter, 4-bit variable gain amplifier (VGA), and a wideband two-stage power amplifier. A differential design is employed to preserve stability and reduce coupling between channels. The internal feedback caused by the package parasitic inductance is mitigated resulting in an improved input and output port isolation. This is due to the differential output port not being referenced to the PCB ground node.

4.3 Circuit Design

The beamformer is designed using Tower-Semi SiGe BiCMOS 5th generation technology (SBC18S5) [64]. This process has 7 Aluminum layers, with a top metal layer thickness of 2.8 µm. A 3×4 µm SiGe HBT transistor has a simulated f_{max} and f_t of 305 and 272 GHz, respectively, at a current density of 1.5-2 mA/µm with parasitic extraction to the top metal layer.

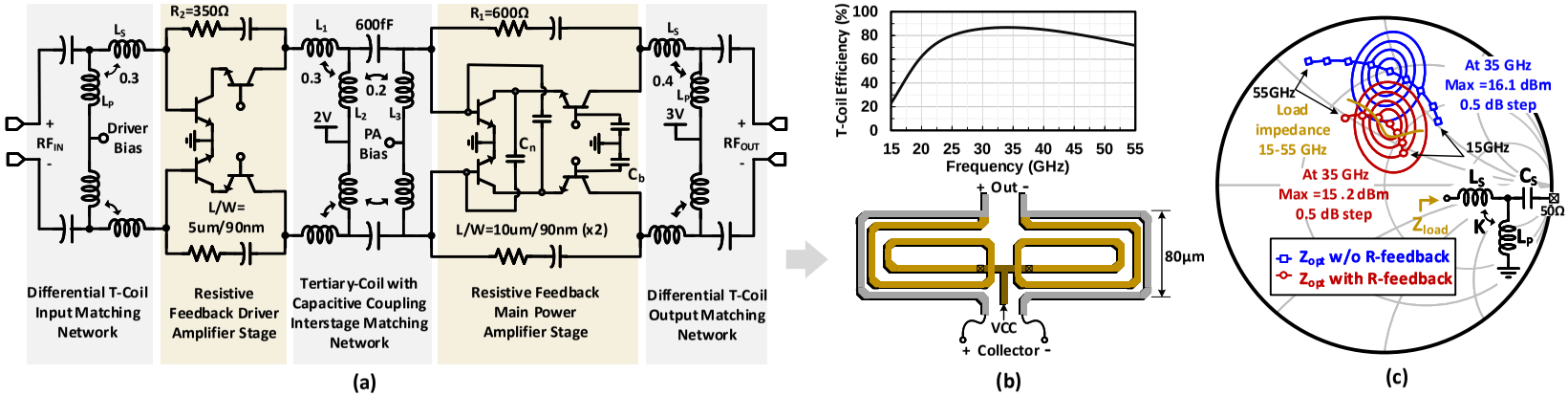


Figure 4.3. (a) Wideband 2-stage power amplifier. (b) Differential asymmetric T-coil network design and efficiency. (c) Simulated load-pull contours and impedance transformation.

4.3.1 Wideband Power Amplifier

The PA block has limited available area set by the small chip size due to reduced array pitch at mm-wave frequencies ($\sim\lambda/2$). Therefore, reported mm-wave PA architectures that require a large footprint for high power and wideband performance such as transformer-based power combining [69–72], balanced amplifiers with bulky 90^o hybrids [73–75], and distributed topologies [76–78] are not suitable for beamformers implementation. The techniques employed in this work are selected to fulfill the power and bandwidth requirements with compact area utilization.

The two stage class-AB power amplifier is designed with a combination of resistive feedback to enable broadband matching, transistor stacking for high output power, and low-loss wideband asymmetric T-coil ($L_p \neq L_s$) network [Fig. 4.3(a)]. A high R-feedback can facilitate wideband output match with some degradation in the PA efficiency, therefore, R_1 is limited to 600 Ω for wideband matching and results in <5-6% drop in efficiency. The optimum load required to generate the maximum output is shown in Fig. 4.3(c) with and without the feedback effect. An asymmetric T-coil network equivalent to a transformer is designed with negative coupling to realize the PA R_{opt} impedance transformation to 50 Ω. The feedback resistor also makes the PA input impedance predominantly resistive allowing for wideband impedance transformation in the interstage matching network

A cascode amplifier is used as a driver amplifier (DA). With the use of a tertiary-coil network employing capacitive and magnatic couplings, a broadband match between the PA Z_{in} and DA-stage Z_{opt} is realized. The DA also utilizes R-feedback of 350 Ω and a T-coil network for input matching.

A PA breakout cell is tested on a probe station and the measured results are presented in Fig. 4.4. A wide 3-dB bandwidth of 18-66.7 GHz is achieved with a peak gain of 22-23 dB. The output P_{1dB} is 11-14.8 dBm at 17.5-51.25 GHz with a peak Psat of 15.5 dBm. A PAE at P_{1dB} of 15-19.8% is achieved at 24-44 GHz. Power gain and Pout versus input power are shown in Fig.

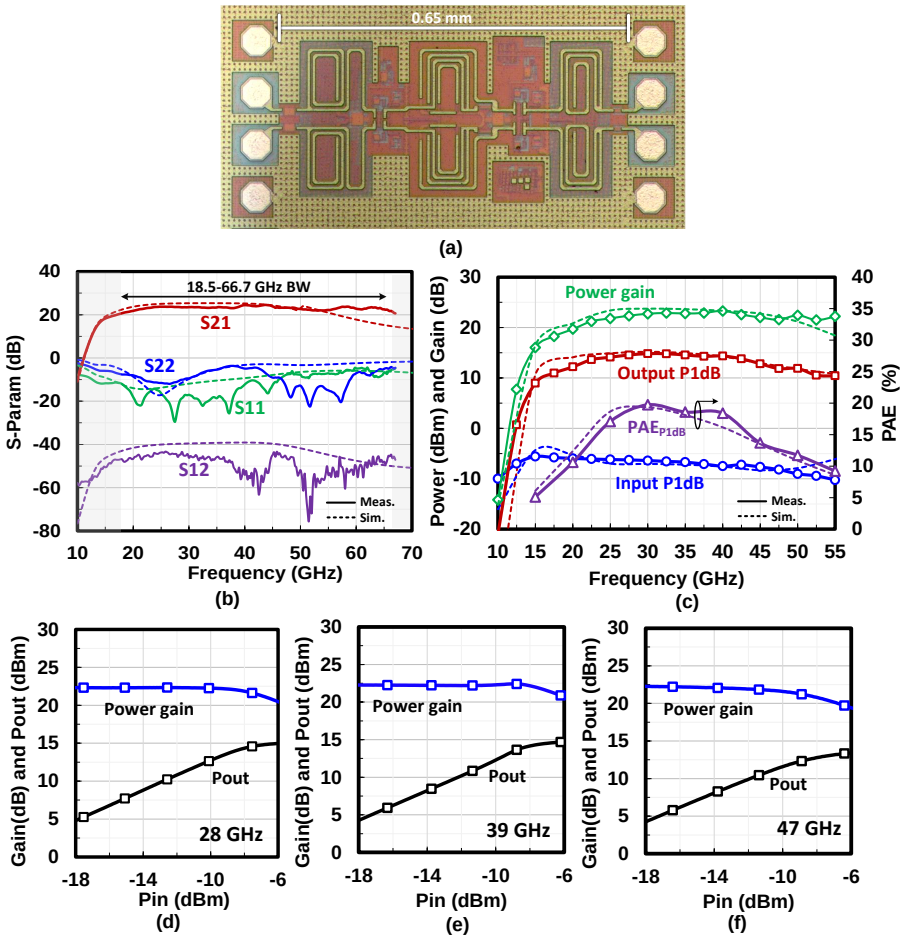


Figure 4.4. (a) Power amplifier chip micrograph, (b) measured and simulated S-parameters, (c) Large-signal measurement and simulation. Power gain and Pout versus input power at: (d) 28 GHz, (e) 39 GHz, and (f) 47 GHz.

4.4(d)–(f) at 28, 39, and 47 GHz, respectively. The two-stage PA occupies a compact area of 0.21 mm^2.

4.3.2 Broadband Power Divider and Active Balun Design

The broadband signal distribution to the four beamforming channels is realized using a 2-stage Wilkinson network. A single-section Wilkinson followed by a 2-section Wilkinson design is chosen to realize the wideband power division operation with lowest insertion loss over wide bandwidth. The $\lambda/4$ transmission lines are implemented using M7-layer for signal and M4/M5-layer for ground synthesizing the required characteristic impedance. The 100 Ω,

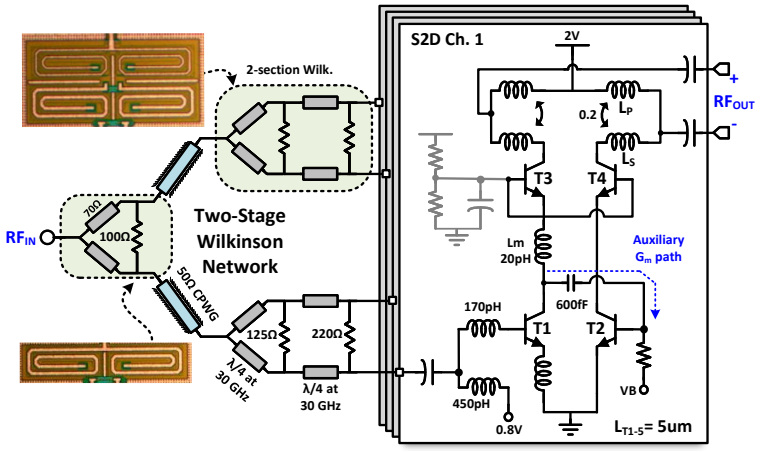


Figure 4.5. Wideband 1:4 Wilkinson divider network with active balun stage.

125 Ω, and 220 Ω are realized using Titanium Nitride (TiN) resistors. This design covers 15-57 GHz with a simulated isolation (S_{32}) of > 20 dB and insertion ohmic loss of 3-4 dB including all connecting transmission lines (Fig. 4.5).

The active balun consists of a main transconductance (Gm) stage T1 with a compensation path using an auxiliary Gm stage T2 to achieve gain and phase imbalance neutralization between the output nodes (Fig. 4.5). Cascode transistors (T3 and T4) are used to boost the balun gain and improve the reverse-isolation. A 20 pH is added in the main signal path as a line-based delay compensation to minimize the phase error at high frequencies. The 50 Ω input matching network is achieved using inductor based L-matching with 30 pH degeneration inductor at the emitter node. A compact T-coil network is used to realize a wideband match to the following phase shifter. This design results in a simulated common mode rejection ration (CMRR) > 15 dB and gain of 10 dB with a 3-dB BW from 15-55 GHz at 12 mW power consumption.

4.3.3 Wideband Phase Generation and Gain Control

The 5-bit phase control is realized as shown in Fig. 4.6(a). An active phase shifter design based on differential analog adder is employed for wideband operation and compact size. The differential quadrature signals are generated using a quadrature all pass filter (QAF) [Fig. 4.6(b)]. Compared with other I/Q generation circuits such as a passive poly phase filter [45],

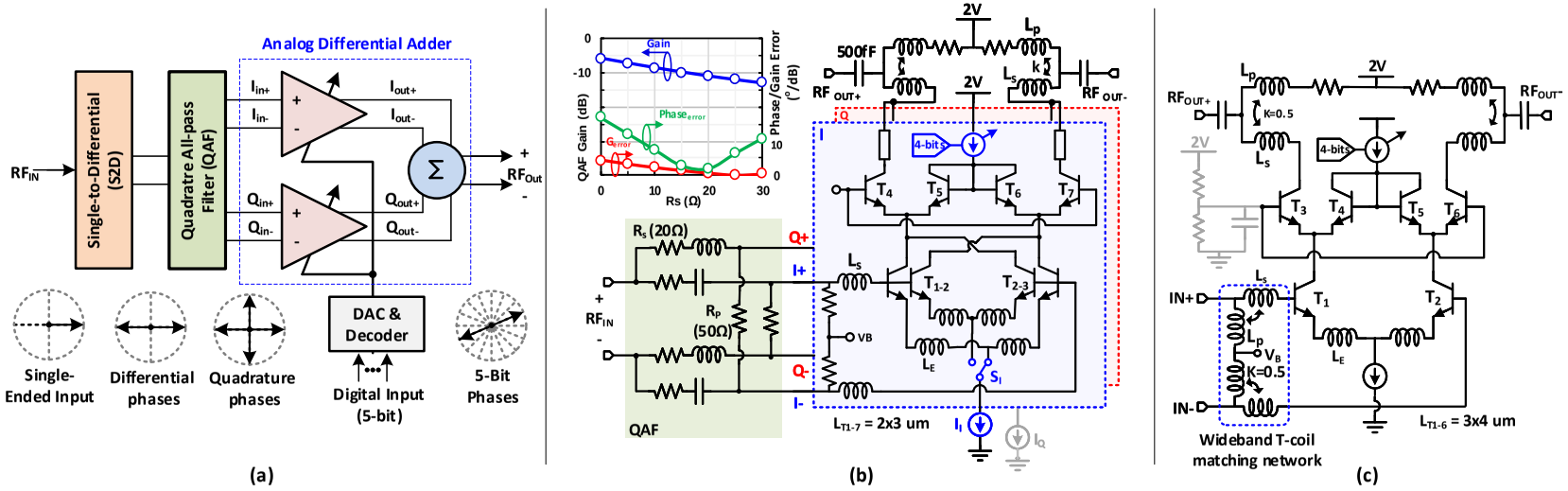


Figure 4.6. (a) Block diagram of the 5-bits phase generation, (b) active wideband phase shifter with QAF network, and (c) current-steering variable gain amplifier.

transformer-based poly-phase network [46, 47], the QAF is the most suitable for wideband I/Q generation in the RF path [Fig. 4.6(b)] [48]. The bandwidth is extended by pole-splitting technique described in [48] where the resistor (R) is increased from the ideal value of $\sqrt{L/C}$ with a small reduction of voltage gain.

The capacitive loading effect on the QAF network is mitigated using series resistance ($R_s = 20\ \Omega$) to reduce the network Q and its sensitivity to the loading capacitor C_{Load}. This also increases the input impedance of the QAF network making it easier to drive the PS block. The QAF maximum phase and gain errors versus R_s values are shown in Fig. 4.6(b).

The differential phase shifter employs two variable gain amplifiers (VGAs). The required magnitude is controlled by the current-mode DACs used to steer the current from cascode transistors (T4 and T7). Wideband gain response is realized by combining the differential I/Q weighted signals at the output node using a T-coil peaking network.

The simulated RMS phase error is < 5.6^o and the RMS gain error is < 1.7 dB at 16-52 GHz with a mean gain of -4.6 dB over the 32 states. The phase shifter input P_{1dB} is -1 dBm with a power consumption of 26 mW from a 2 V supply and area utilization of only 0.15 mm^2.

Gain control is achieved using current-steering topology to allow for 17 dB gain control [Fig. 4.6(c)]. The current is steered from the cascode stage with a 4-bit DAC control circuit resulting in a phase change < 4^o at 15-55 GHz. The low phase change is key in order to avoid a vicious cycle of phase-gain correction and simplify the calibration algorithm. The VGA is designed to have an output P_{1dB} of 1 dBm sufficient to drive the PA when operated at low-gain states. This design is biased at 20 mA and consumes 40 mW from a 2 V supply.

The Tx channel composed of the wideband blocks results in a simulated maximum gain of 36-37 dB and an output P_{1dB} of 14.9 dBm at midband frequency of 30-35 GHz. The simulated CMRR for the Tx channel is 25.2-33.8 at 17-52 GHz. This is achieved mainly by the VGA and phase shifter blocks prior to the power amplifier stage as they employ a fully-differential design with current sources at the emitter node. The 1:4 Wilkinson network adds 3-4 dB ohmic loss and 6 dB Wilkinson loss, resulting in a chip gain of 27-28 dB. The chip power consumption is 250

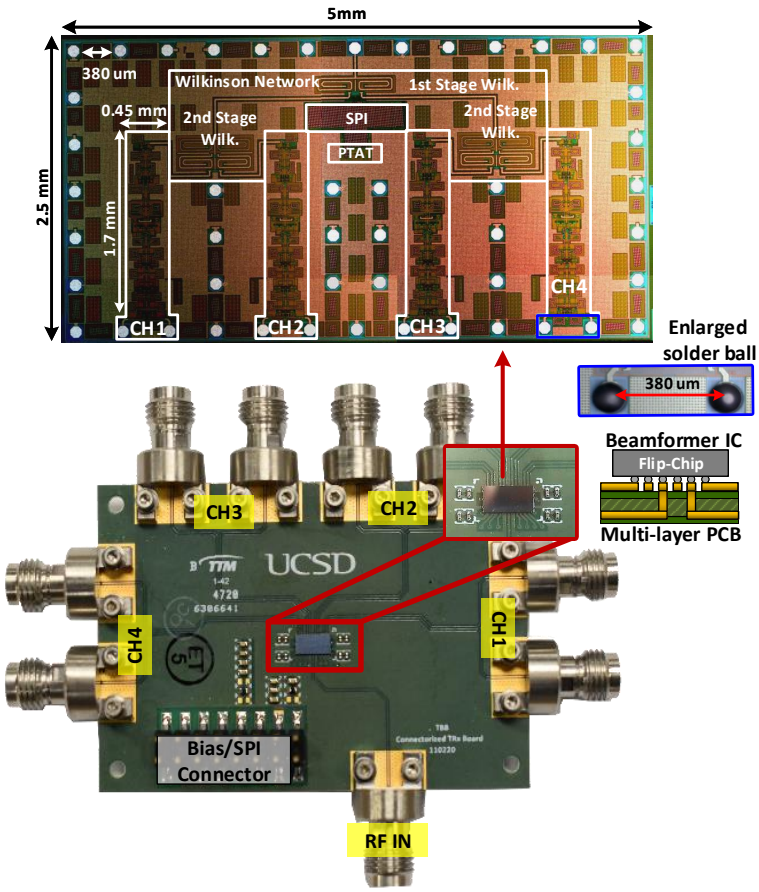


Figure 4.7. 4×1 packaged Tx wideband beamformer chip on a connectorized evaluation PCB.

mW/ch. at P_{1dB}.

4.4 4×1 Beamformer Measurements

An evaluation PCB is used to measure the Tx beamformer chip packaged with wafer-level chip-scale bumps at 380 μm pitch (Fig. 4.7). A Keysight 4-port PNA-X N5247A is used with the input and output PCB transmission lines de-embedded from measurements. The measured S-parameters of all 4 channels are presented in Fig. 4.8(a) with a peak gain of 28 dB and a 3-dB bandwidth of 16-52 GHz. The gain is defined as the measured S_{21} between the input common port and a single output port including the Wilkinson network ohmic and division losses. The measured reverse isolation is > 40 dB with a wideband input and output matching. The gain and

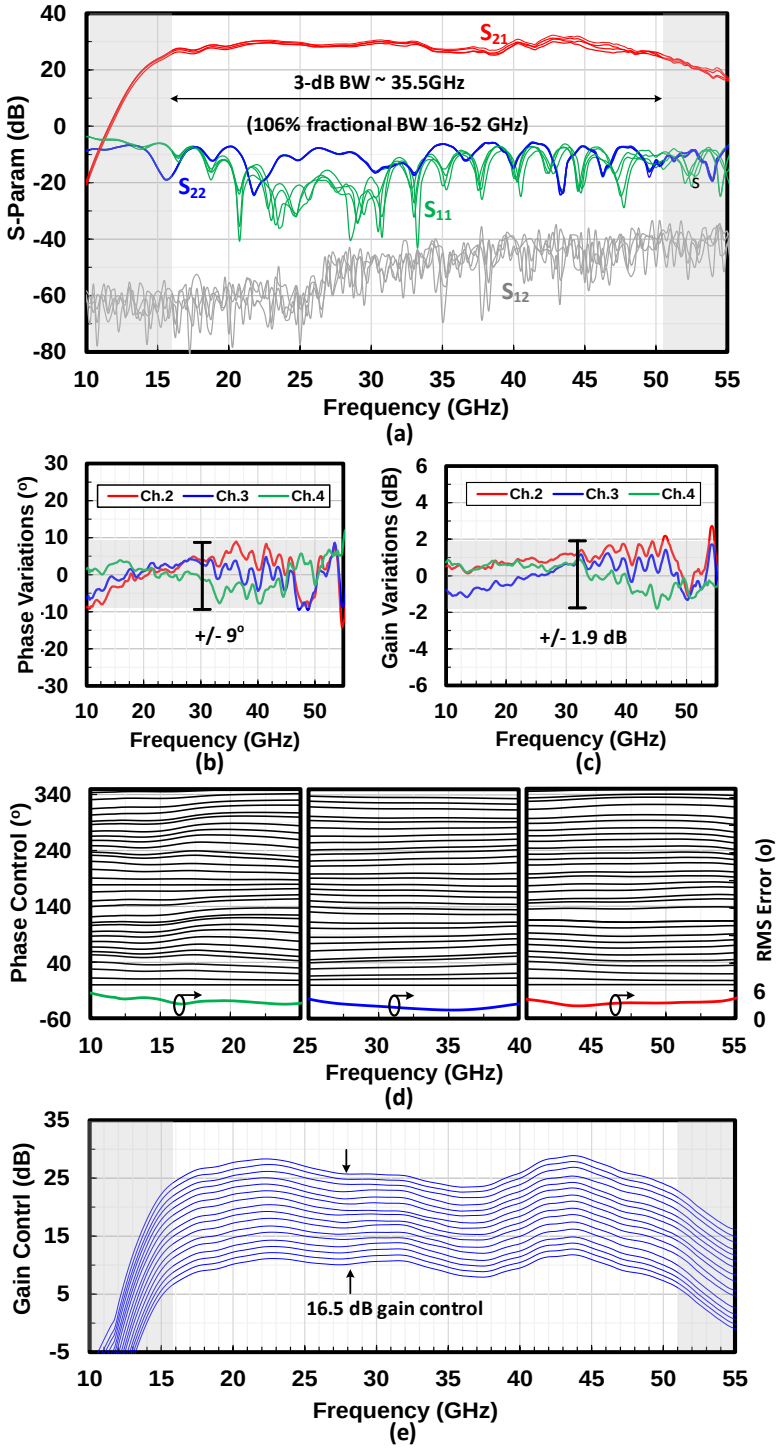


Figure 4.8. Measured (a) S-parameters for 4 channels, (b) phase variations and (c) gain variations normalized to channel 1. (d) Optimized 5-bit phase control at 20, 35, and 45 GHz, and (e) 16.5 dB gain control.

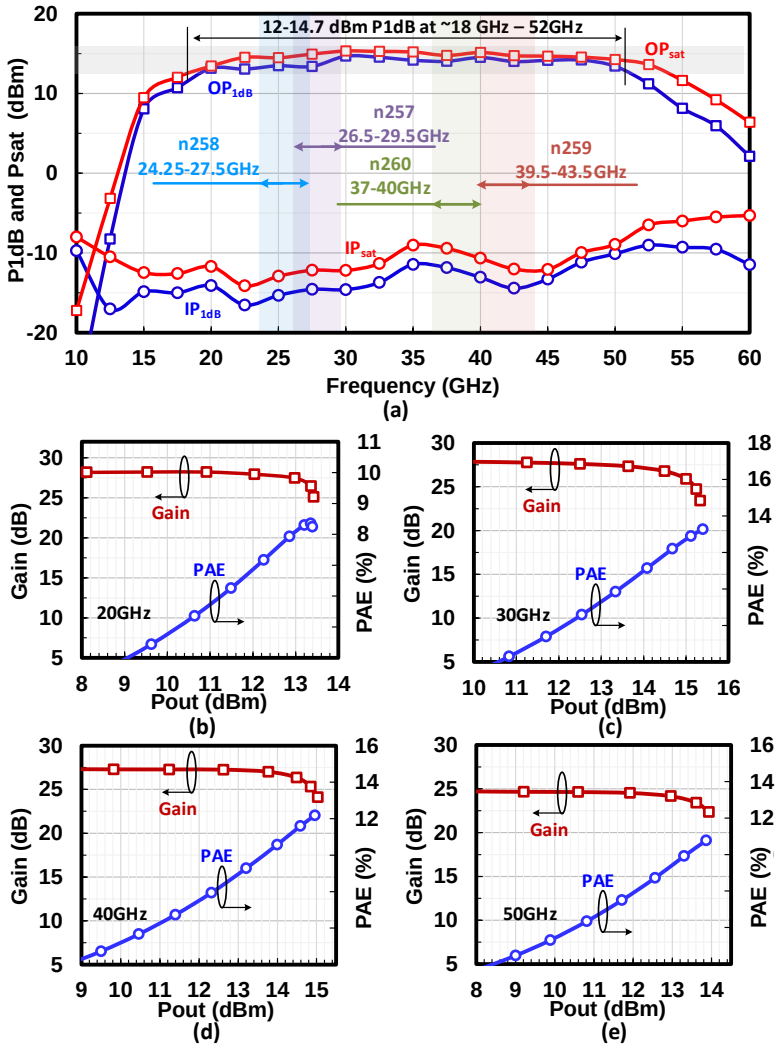


Figure 4.9. Large-signal measurements: (a) output and input power at P_{1dB} and Psat. Power gain and PAE versus Pout at (b) 20 GHz, (c) 30 GHz, (d) 40 GHz, and (e) 50 GHz.

phase difference between the beamformer channels normalized to channel 1 are shown in Fig. 4.8(b) and (c). The 4 channels have maximum of +/-1.9 dB gain and +/-9^o phase variations at 15-52 GHz allowing for easy calibration.

The beamformer measured phase response is shown in Fig. 4.8(d). Using an extra trim bit in the phase shifter, the phase response is optimized at three regions (20, 35, and 50 GHz). Therefore, the phase shifter operates in 20-25 GHz 5-bit instantaneous bandwidth regions. An RMS phase error of < 5.6^o is obtained at 15-25 GHz (green), 25-40 GHz (blue), and 40-50 GHz (red) as shown in Fig. 4.8(d). A gain control of 16.5-dB is measured with a gain step of ~1 dB

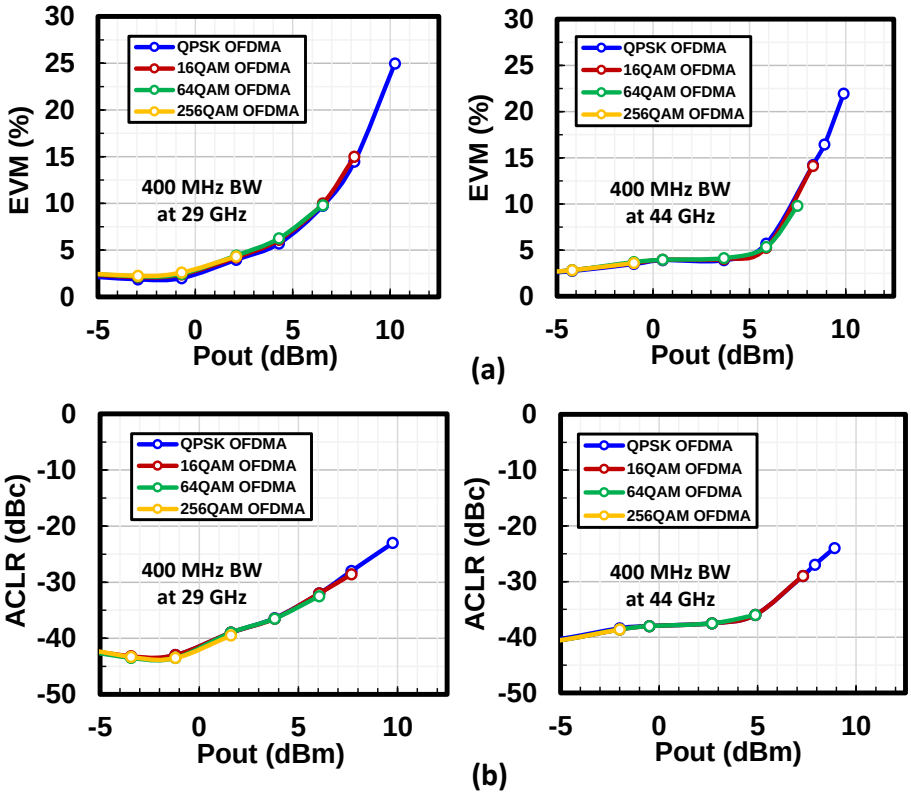


Figure 4.10. Measured OFDMA waveforms: (a) EVM levels versus Pout and (b) ACLR versus Pout at 29 GHz and 44 GHz with 400 MHz channel bandwidth.

using the VGA gain control [Fig. 4.8(e)].

Fig. 4.9(a) presents the large-signal measurements of the Tx 4×1 beamformer. The chip achieves an output P_{1dB} and Psat of 13.5-14.7 dBm and 14-15.4 dBm, respectively, at 20-50 GHz covering the entire 5G NR FR2 bands. The peak PAE is 13% at 30 GHz and > 10% at 24-50 GHz. The large-signal gain and output power are presented in Fig. 4.9(b)–(e) at 20, 30, 40, and 50 GHz. The Tx beamformer is also tested with 5G NR OFDMA packets with a center frequency at 29 and 44 GHz, and a channel bandwidth of 400 MHz. Fig. 4.10(a) demonstrates the measured EVMs in QPSK, 16-QAM, 64-QAM, and 256-QAM versus output power and Fig. 4.10(b) presents the measured adjacent channel leakage ratio (ACLR), at 29 and 44 GHz. Based on the 5G NR standard [62], the EVM level requirements are < 17.5%, 12.5%, 8.0%, and 3.5% for QPSK, 16-QAM, 64-QAM, and 256-QAM waveforms, respectively, with less than -28 dBc ACLR for base stations. This chip realizes a maximum output power compliant with the EVM

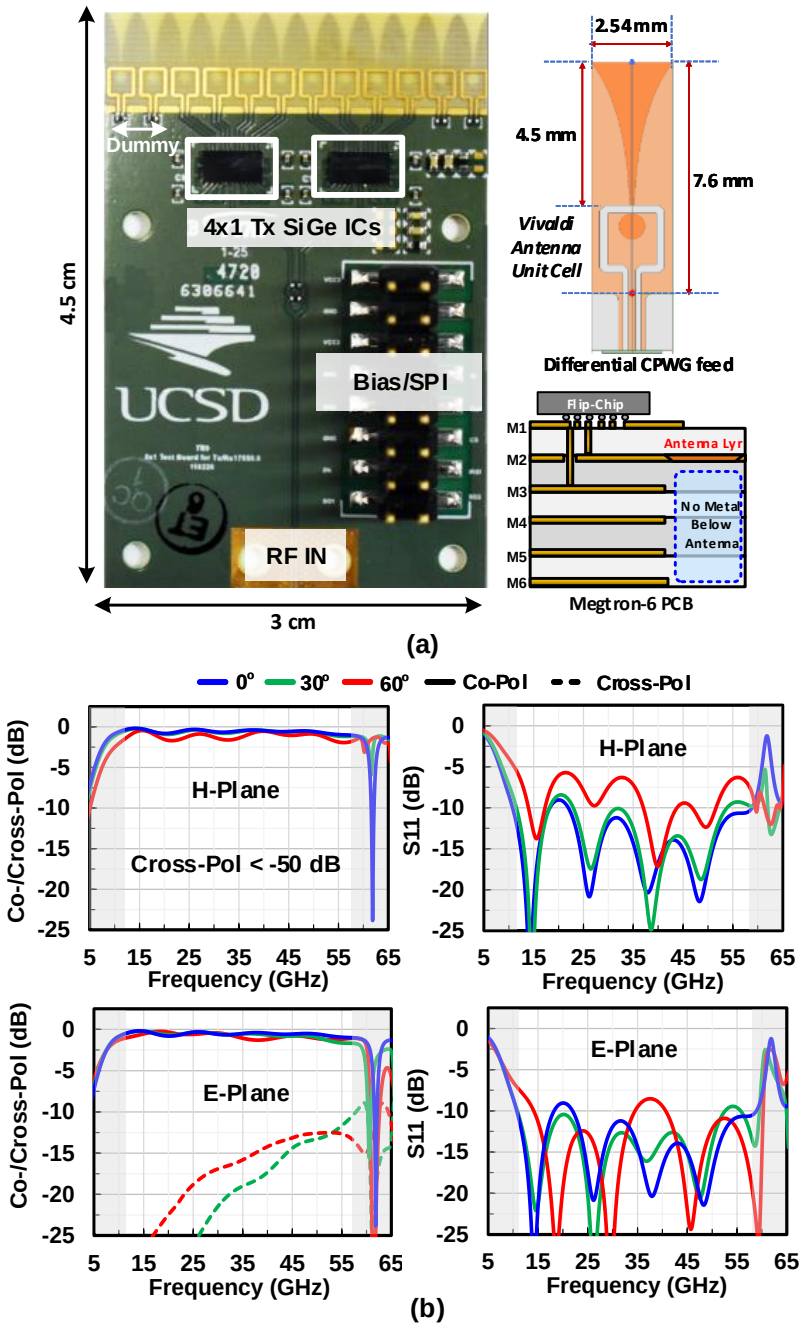


Figure 4.11. (a) Top view of the array PCB with SiGe beamformer ICs and PCB integrated Vivaldi antenna array. (b) Simulated Vivaldi antenna array performance in H- and E-planes.

level and ACLR requirements of 8.2, 7.4, 5.4, and 1.1 dBm for QPSK, 16-QAM, 64-QAM and 256-QAM modulation schemes, respectively, at 29 GHz. For the 44 GHz center frequency, the beamformer chip achieves a maximum output power of 8.6, 8, 6.8, and -0.9 dBm for QPSK,

16-QAM, 64-QAM and 256-QAM waveforms, respectively.

4.5 8×1 Phased Array Module

4.5.1 PCB and Antenna Design

Two 16-52 GHz beamformer chips are used to build a multi-band phased array module on a low-cost 6-layer Megtron-6 PCB (ε_r= 3.24). The ICs are closely placed to the differential wideband Vivaldi antenna array minimizing the feeding line loss [Fig. 4.11(a)]. The linear array spacing is 2.54 mm chosen to mitigate transverse-electric (TE1) parallel plate mode and allow for wideband operation up to 60 GHz. The antenna is simulated in Ansys HFSS, and Fig. 4.11(b) presents the co/cross pol and reflection coefficient in the E- and H-planes. The array can scan up to 60^o with $|S_{11}|$ < -10 dB in E-plane and < -7 dB in the H-plane at 15-55 GHz. The unit cell has a gain of -3.7 to 4.4 dB at 15-55 GHz including the differential feed ohmic loss.

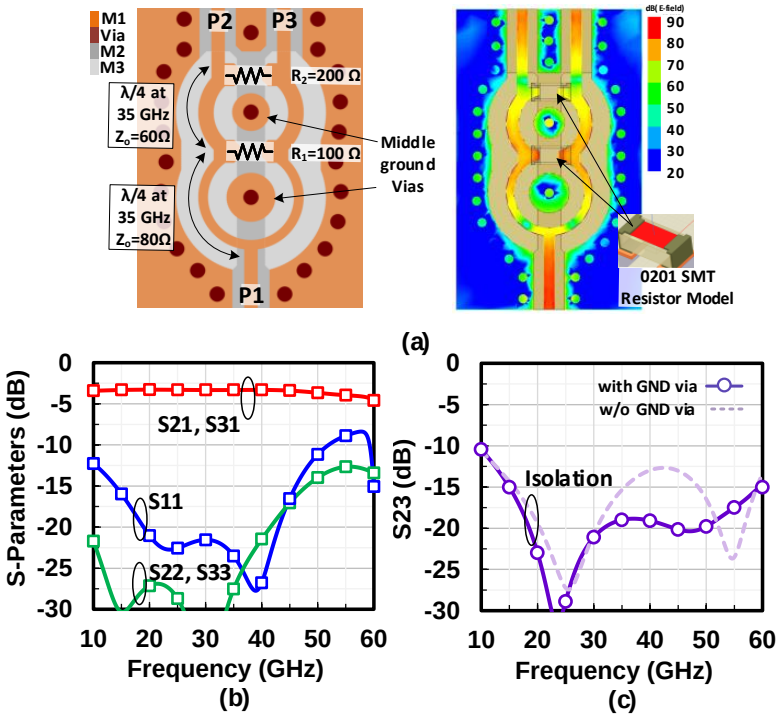


Figure 4.12. (a) 2-section PCB Wilkinson design, (b) simulated S-parameters, and (c) isolation between Wilkinson ports with and without middle ground vias.

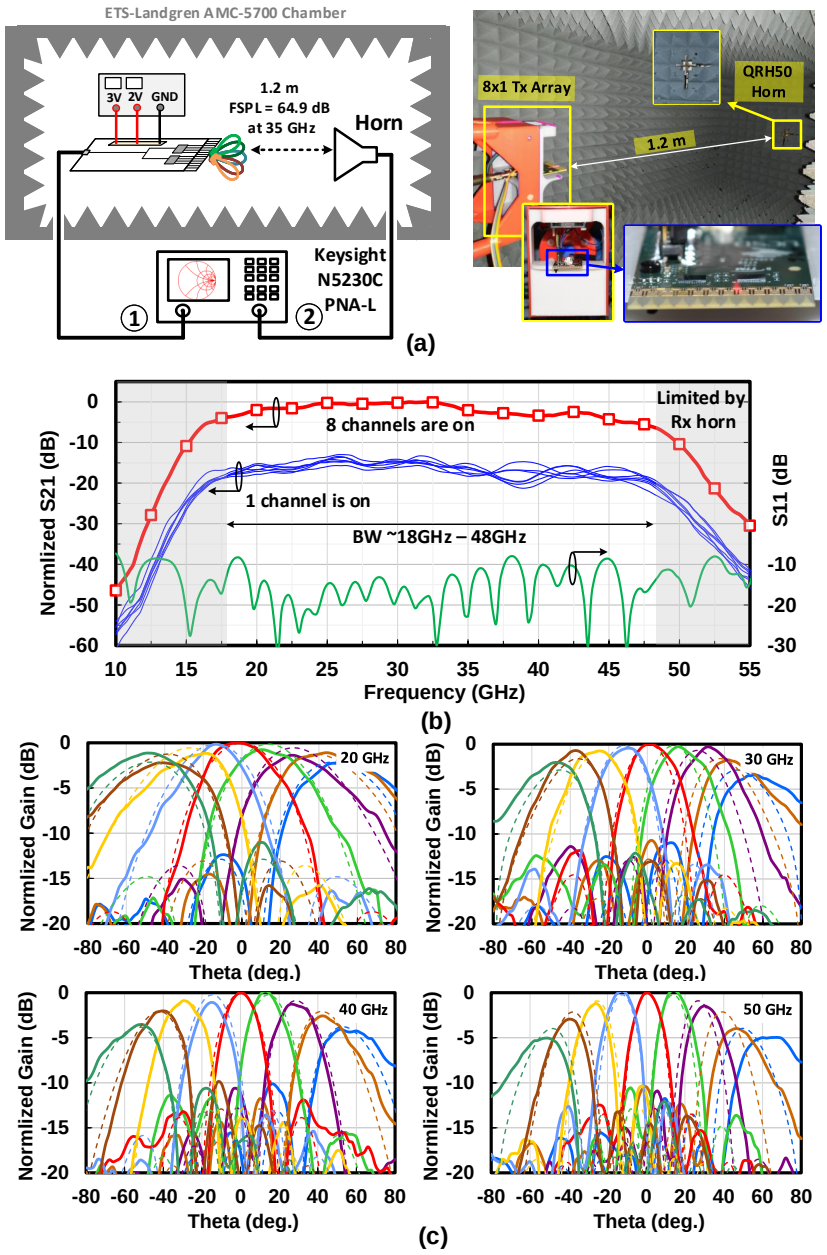


Figure 4.13. (a) Measurement setup and photo of the positioned 8×1 Tx array. (b) Measured S-parameters when a single channel is turned on and when all 8 channels are on. (c) Measured patterns with -60^o to 60^o scan angles at 20, 30, 40, and 50 GHz.

The input signal is distributed to the two beamformer chips using PCB Wilkinson power divider realized on M1 and M3 layers. The wideband performance is achieved by implementing a two section circular design as shown in Fig. 4.12(a). A 200 Ω and 100 Ω surface mount resistors are used for the Wilkinson resistors and a middle ground via is added in order to minimize the

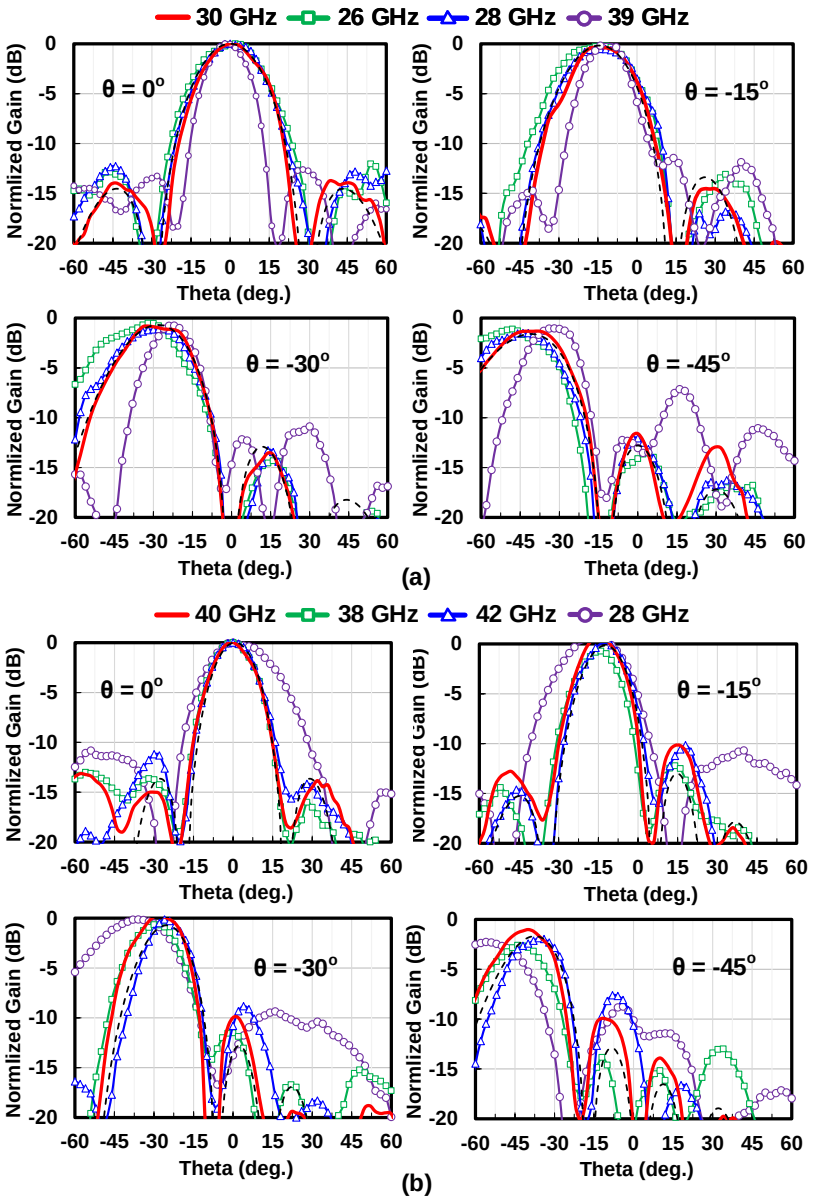


Figure 4.14. Pattern measurement: (a) at 26, 28, 30 and 39 GHz with calibration applied at 30 GHz and (b) at 28, 38, 40, and 42 GHz with calibration applied at 40 GHz.

coupling between the Wilkinson arms and improve the isolation (S_{23}). The simulated Wilkinson power divider insertion loss is < 0.6 dB and the isolation is > 20 dB at 16-50 GHz [Fig. 4.12(b) and (c)].

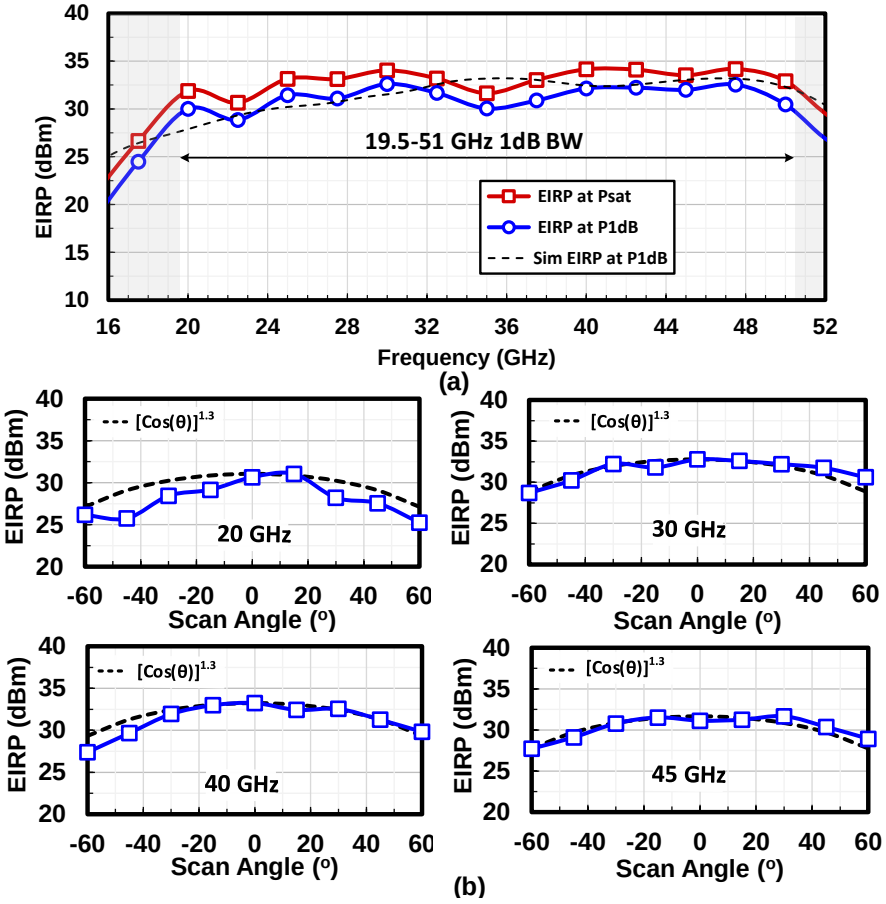


Figure 4.15. (a) Measured EIRP vs frequency at P_{1dB} and at Psat. (b) EIRP at P_{1dB} with -60^o to 60^o scan angles at 20, 30, 40, and 45 GHz.

4.5.2 Pattern and EIRP Measurements

The 8-element Tx phased array is tested inside an ETS-5700 anechoic chamber at 1.2 m distance with a wideband horn that can operate up to 50 GHz [Fig. 4.13(a)]. The far-field S_{21} is measured with one channel turned on at a time, and then when all channels are energized. Fig. 4.13(b) presents the array normalized frequency response. The gain ripples in the individual channels response are mainly due to antenna coupling as the antenna is designed to optimally operate when all channels are energized.

The 8-element patterns are measured at 20, 30, 40, and 50 GHz [Fig. 4.13(c)]. The array is first calibrated at each frequency by measuring the amplitude and phase response of every channel and compensating the difference using the channel's phase shifter and VGA. Then the

phase shift per element is set at each frequency for scanning purposes. The measured patterns match the simulated patterns well at all frequencies and scan angles.

The module is able to scan from -60^o to 60^o with a sidelobe level < -10 dB at all scan angles, and with a 3-dB beamwidth of 12^o, 15^o, 20^o and 37^o at 50, 40, 30, and 20 GHz, respectively. Due to the wideband phased-array performance, the frequency range where the calibration is valid is evaluated. The array is calibrated at 30 GHz and the pattern is measured at multiple frequencies [Fig. 4.14 (a)]. Beside the beam squinting effect, the measured patterns at 28 GHz and 26 GHz show excellent performance. At 39 GHz, the beam squinting effect is apparent and the sidelobe level increases significantly when scanning. Another measurement is done with the calibration applied at 40 GHz. Adjacent bands (38 and 42 GHz) have excellent patterns, but the 28 GHz band requires a re-calibration.

The measured EIRP is presented in Fig. 4.15. An EIRP at P_{1dB} >30 dBm is achieved at 20-50 GHz, with a peak EIRP of 34.5 dBm under Psat conditions. The EIRP versus scan angle is also measured at 20, 30, 40, and 45 GHz with +/- 60^o scan angle. The drop in EIRP follows $cos(\theta)^{1.3}$ element pattern and is expected from the Vivaldi antenna.

4.5.3 EVM Measurements

The 1.2 m link setup is also used to measure the EVM performance of the 8-element phased array with 400 MSym/s single-carrier 64-QAM waveform (α= 0.35 and PAPR = 7.7 dB) at multiple-bands (25, 29, 38 and 42 GHz). A microwave signal generator (Keysight M9384B VXG) is used to generate the complex-modulated signals, and a Keysight UXA spectrum analyzer is used with the 89600 VSA software to capture the signal and extract the constellations and EVMs. The measured constellation and EVM at normal incidence are presented in Fig. 4.16(a) and shows a data rate of 2.4 Gb/s with < 3.6% EVM at all bands. Also, EVM versus EIRP is measured and presented in Fig 16(b). An EVM < 5% is achieved at all bands with an EIRP level of 26-27 dBm. Fig. 4.16(c) demonstrates the EVM performance when scanning the beam to +/- 60^o and the measured EVM is < 4% at 25, 29, 38, and 42 GHz.

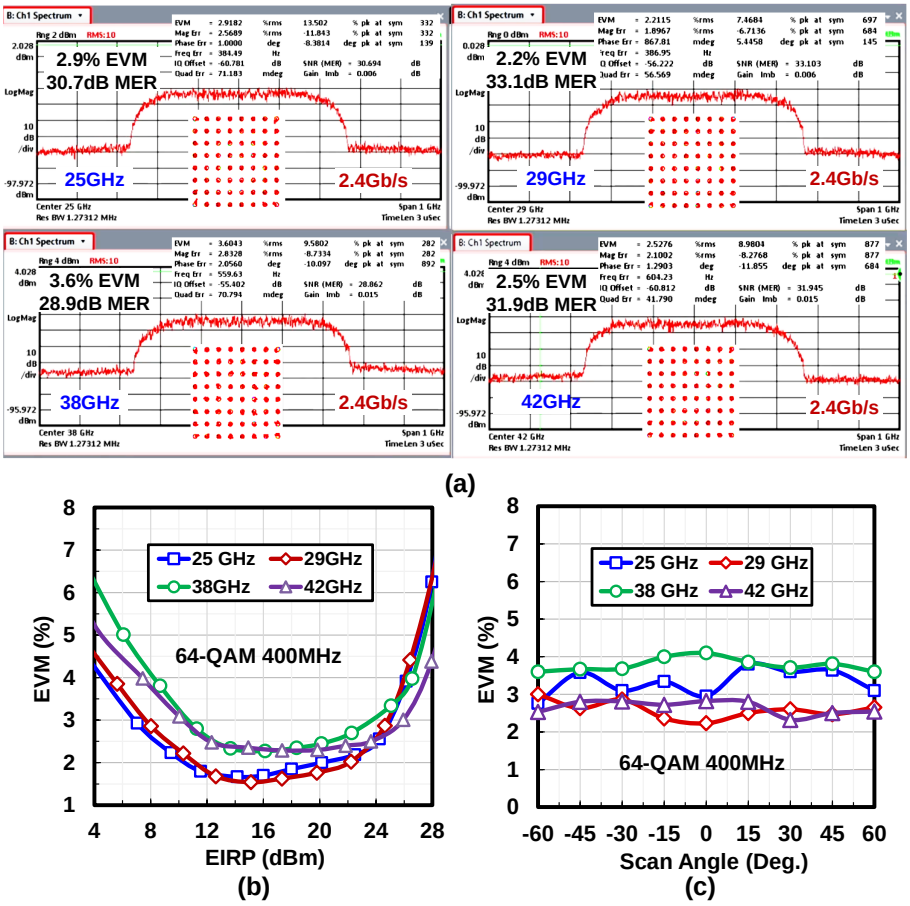


Figure 4.16. (a) Measured constellation and spectrum at 25, 29, 38, and 42 GHz center frequency and 24-25 dBm EIRP. (b) EVM performance versus EIRP at broadside. (c) EVM performance at 25-26 dBm EIRP versus scan angle. All measurements are done using single-carrier 400 MHz 64-QAM waveform (2.4 Gb/s).

5G NR waveforms with 400-MHz channel bandwidth in QPSK, 16-QAM, 64-QAM, and 256-QAM are also generated using the Keysight M9384B VXG (PAPR=11.72 dB for 64-QAM). The measured constellations and EVMs at 25, 29, 38, and 42 GHz are summarized in Fig. 4.17. Data transmissions of up to 256-QAM is supported by this array with EVM levels <2.98% and 20.8-22 dBm EIRP demonstrating excellent multi-band operation complaint with standard requirements for 5G OFDMA-mode mentioned previously.

A comparison with the state of the art 5G FR2 mm-wave phased arrays is presented in Table 2. This work achieves the widest bandwidth covering multiple bands from 16-52 GHz. The beamformer chip achieves a realized gain of 28.3 dB (34.3 dB/ch.) with 14.7 dBm output

Table 4.2. Performance Comparison of mm-Wave Phased Arrays For 5G NR FR2

Beamformer Measurements								
Design	This work	[13] TMTT'21	[14] RFIC'19	[24] TMTT'20	[8] JSSC'20	[16] TMTT'21	[6] JSSC'18	[15] JSSC'20
Technology	0.18 um SiGe BiCMOS	65-nm CMOS	28-nm CMOS	0.18 um SiGe BiCMOS	65-nm CMOS	0.18 um SiGe BiCMOS	0.18 um SiGe BiCMOS	65-nm CMOS
Frequency (GHz)	15.25-50.5	37.5-39.5	37-40	37-42	39	23.5-29	28.4.4-29.4	28
Fractional BW (%)	107.2	5.2	7.8	12.6	-	22.6	3.46	-
Architecture	4×1 Tx RF-PS	8×1 Tx RF-PS	8×1 Tx/Rx RF-PS	2×2 Tx/Rx RF-PS	2×2 Tx/Rx LO-PS	2×2 Tx/Rx RF-PS	2×2 Tx/Rx RF-PS	Two 4×1 Tx/Rx RF-PS
Integration/Chip	Beamformer	Beamformer	Beamformer	Beamformer	Full transceiver	Beamformer	Beamformer	Beamformer
Phase Resolution (bit)	5	4	5	6	0.05º	6	6	0.4º RMS error
Gain Control (dB)	16.2	20	10.2	25	-	26	14	-
Gain/Ch (dB)	34.3	32.3	45-48	25	3 (CG)	19	20	20
OP1dB (dBm)	13.5-14.7* (20-50 GHz)	10.8*	10.2-12.3	10-11	9	15-16	10.5	11.3
Psat (dBm)	14.4-15.3	-	-	12	15.5	-	12.5	15.1
P_{DC}/Ch. In Tx Mode (mW)	250 at P1dB	187.5	339 at P1dB	250 at P1dB	375 at P1dB	340 at P1dB	200 at P1dB	252 at P1dB
Chip Area (mm^2)	11	19.35	17.2	12.96	12	12.5	11.75	12
Phased Array Measurements								
Array size	8×1	8× 4	4×4	8×8	16×4	8×8	8×4	8×4
Polarization	Single	Single	Dual	Single	Single	Single	Single	Dual
Peak EIRP (dBm)	33-34	47.5	-	51	53	54.8	45	45.6
5G Multi-Band Operation	Yes	-	-	-	-	Yes	-	-
OTA Distance (m)	1.2	35	-	1	1	1.3	5	1
Scan Range, Az (o)	+/- 60	+/- 60	+/- 45	+/- 60	+/- 40 (4×1 array)	+/- 60	+/- 50	+/- 50
Constellation	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM MCS19	64-QAM	64-QAM	64-QAM
Data Rate	2.4 Gb/s	1.2 Gb/s	0.6 Gb/s	1.2 Gb/s	2.4 Gb/s	1.2 Gb/s	3 Gb/s	15 Gb/s
EVM (%)	2.5 25 dBm EIRP Tx EVM	4.57 Tx EVM	-	5 44 dBm EIRP Tx EVM	3 Tx -Rx EVM	5 47 dBm EIRP Tx EVM	4.46 Tx-Rx EVM	6.16 35.2 dBm EIRP Tx EVM
5G NR Evaluated	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	-	64-QAM OFDM, 100MHz BW	-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	-	-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW

* w/o TRx switch

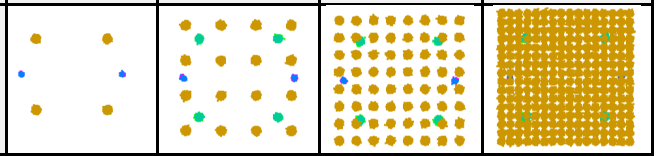
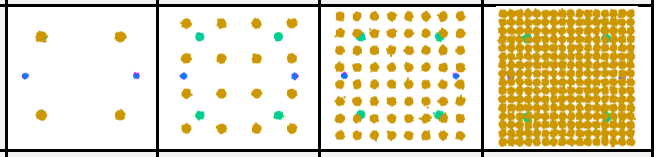
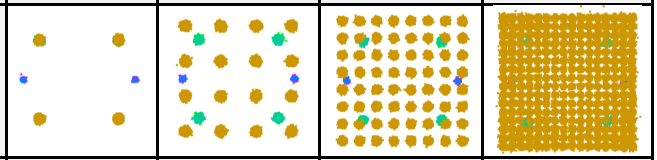
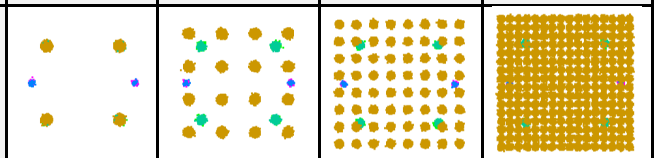
Modulation	QPSK	16-QAM	64-QAM	256-QAM
BW (MHz)	400	400	400	400
Constellation (25 GHz)				
EVM (%)	2.85	2.84	2.86	2.88
EIRP (dBm)	21.42	21.45	21.47	21.1
Constellation (29 GHz)				
EVM (%)	2.58	2.57	2.58	2.62
EIRP (dBm)	21.19	21.23	21.2	21
Constellation (38 GHz)				
EVM (%)	2.96	2.97	2.95	2.98
EIRP (dBm)	20.87	20.9	20.8	20.5
Constellation (42 GHz)				
EVM (%)	2.87	2.86	2.85	2.87
EIRP (dBm)	22.1	22.2	22.1	21.5

Figure 4.17. Measured over-the-air (OTA) 5G OFDMA-mode constellation, Tx EVM, and EIRP performance using the 8-element Tx phased array module at 25, 29, 38, and 42 GHz at broadside.

P_{1dB}. The 8-element phased array module is capable of scanning at -60^o to 60^o at 15.5-51 GHz and transmitting a peak EIRP of 34 dBm.

4.6 Conclusion

This work presented an ultra-wideband and high output power 4-channel SiGe beamformer chip. An 8-element 16-52 GHz multi-band phased-array module is built using two 4×1 beamformers on a low-cost PCB. The scalable test module demonstrated an ultra-wideband performance with multi-band beam scanning capabilities. A single-carrier mode data rate of 2.4 Gb/s in 64-QAM modulation is demonstrated using the 8-element phased array. 5G NR standard compliant packets of up to 256-QAM are supported with 400-MHz channel bandwidth and <

2.98% EVM at all 5G FR2 bands. Future work will concentrate on extending this design to a dual-polarized, dual-beam array for 5G FR2 2×2 MIMO systems.

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Chapter 5

64-Element 16-52 GHz Phased-Array Transmitter and Receiver Based on Slat-Array Architecture for Multiband 5G Operation

5.1 Introduction

High data rate demands are driving the development of mm-wave communication systems. 5G networks are being deployed worldwide to support ultra-reliable low-latency communications (uRLLC) serving applications such as autonomous vehicles, remote diagnosis and surgery, and virtual reality (VR). Therefore, regulatory bodies have auctioned multiple bands in the 5G new radio frequency range 2 (NR FR2) which spans 24.25-52.5 GHz. As a result, the development of mm-wave wideband communication systems is getting more attention to address the challenges of covering a widespread spectrum with a low-cost multi-band/multi-standard solution.

The 5G FR2 (24-52 GHz) encounter higher free space path loss (FSPL) when compared to sub-6 GHz operation. To address this challenge, directive communications using phased-arrays is employed as a key technology for mm-wave systems. To drive the development cost down, advanced SiGe and CMOS processes are used to design RF front-end modules for their attractive high yield, low power consumption, high integration level and digital processing capabilities. [64, 65].

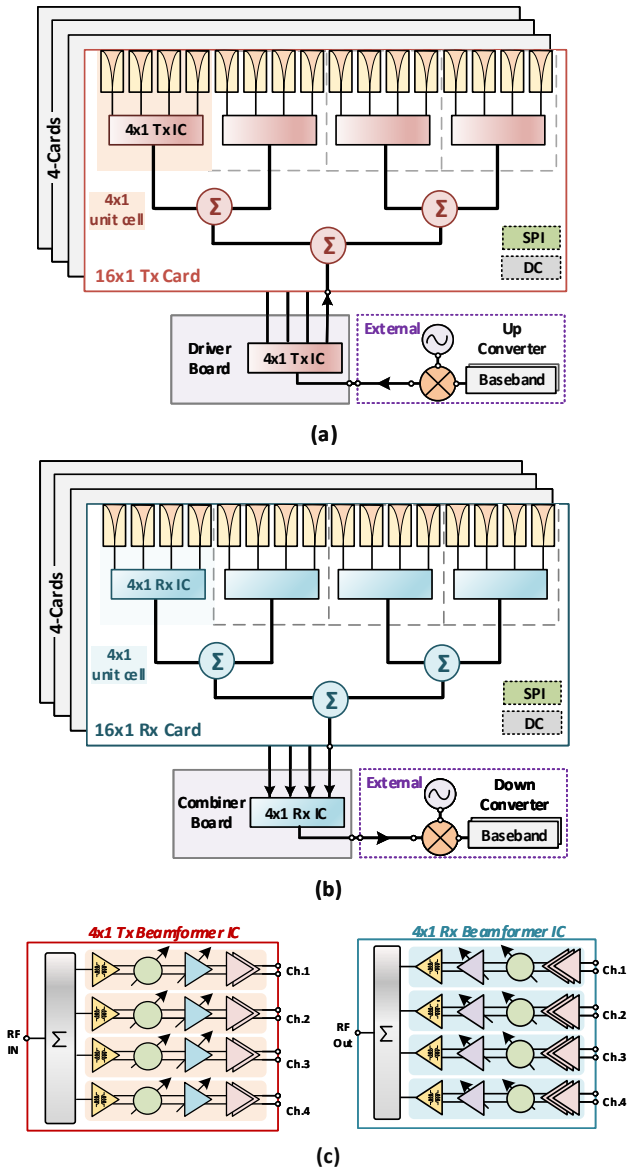


Figure 5.1. 64-element (a) Tx phased-array and (b) Rx phased-array based on brick array configuration. (c) Block diagram of the wideband 4-channel Tx and Rx beamformer chips.

To date, there have been several demonstrations of mm-wave phased-array systems [5–15, 17–19, 22, 23, 31, 32, 79–81] targeting narrow-band operation at the n257 (26.5–29.5), n258 (24.25–27.5) or n260 (37–40) 5G bands. These phased-arrays have fractional bandwidths $[(f_2 - f_1)/f_c]$ <10% limited by system and circuit designs. Improvements to both system-level and circuit-level designs are essential in order to realize a solution capable of 5G FR2 multi-band operation.

Recently, multiple phased-arrays that can support dual or triple band operation are reported [3, 20, 21, 29, 36]. Due to the challenge of wideband design, most of these systems are limited to an unpackaged beamformer IC implementation or a single channel front-end. Wideband phased arrays with full system implementation operating at 23.5-29.5 GHz and at 37-42 GHz are reported in [24], [16]. These arrays show excellent performance but still have relatively limited bandwidth (<25%) and can not support all 5G bands at 24.25-52.6 GHz.

This work presents transmit (Tx) and receive (Rx) multi-band phased-arrays based on 4×1 beamformers chips. Section II discusses the phased-array design, including the array architecture and beamformer chips. An in-depth system analysis for the 64-element Tx and Rx phased arrays and tapered slot antenna design is carried out in section III. Section IV presents the calibration, far-field response and pattern measurements. The effective isotropic radiated power (EIRP) for the Tx array, G/T for the Rx array, and EVM measurements for different waveforms are presented in section IV. Section V concludes this article.

5.2 Multi-Band 64-Element Phased-Arrays

5.2.1 Phased-Array Architecture

The tile-based phased-array architecture has been widely employed for 5G phased-arrays and results in the lowest cost implementation [4, 12]. However, for wideband systems at 16-52 GHz, the antennas become very challenging to build in a planar fashion, and the area allocated to the chip is drastically reduced due to the 0.5λ period at 52 GHz.

Another phased-array architecture is the slat-array configuration and is based on stacked slats oriented perpendicular to the face of the array. As multiple boards are stacked, a large area is available for attaching the beamformer chips and supporting electronic components (behind the antenna aperture). Also, the slat-architecture is compatible with wideband endfire antennas such as tapered-slot antennas, tapered-notch antennas, and angled dipoles. The challenge with this architecture is the large number of RF boards required for large arrays, and the required

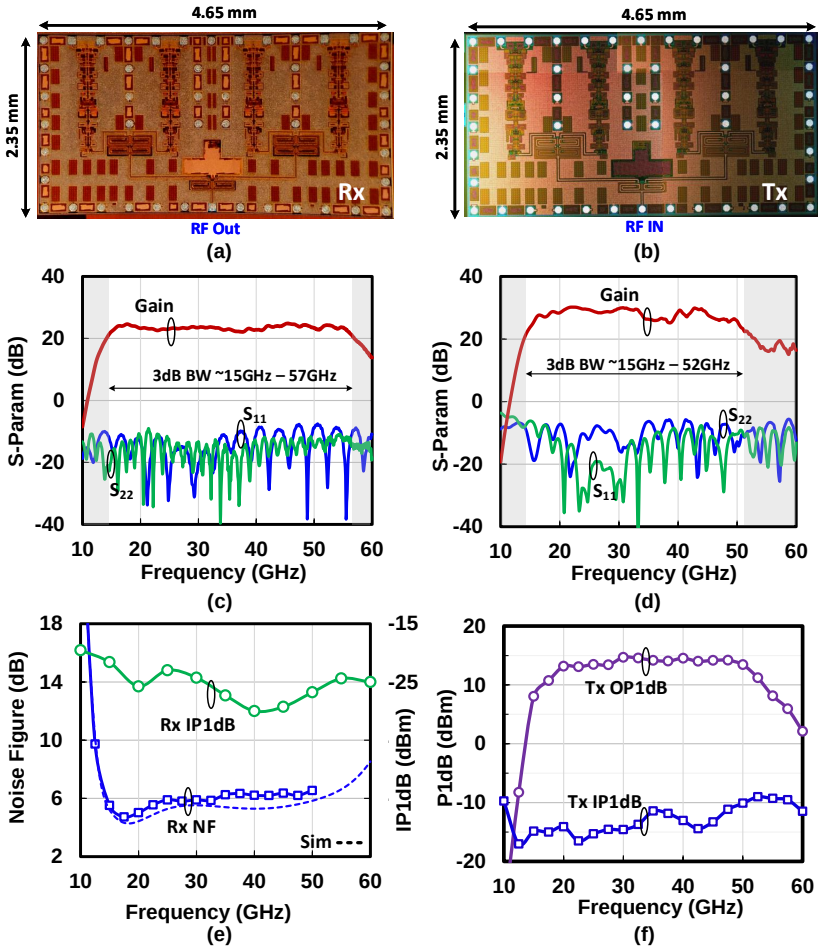


Figure 5.2. 4×1 (a) Tx and (b) Rx beamformer chips. Measured S-parameters of the (c) Rx beamformer and (d) Tx beamformer. (e) NF and input P1dB of the Rx beamformer and (f) output and input P1dB of the Tx beamformer.

cabling to route the RF, DC, and control signals. Fig. 5.1(a) and (b) present the system diagrams based on the slat-array configuration and Vivaldi endfire antennas for the 64-element arrays.

5.2.2 Wideband Beamformer Chips

Wideband Tx and Rx 4×1 beamformer chips are used to build the 64-element phased-arrays. The RF beamforming architecture is employed in the chips design to minimize the system complexity and power consumption. These chips have been presented before in [66] and [37].

The 4×1 Tx beamformer block diagram is shown in Fig. 5.1(c). The RF input signal is distributed to four the channels using a Wilkinson network. Each channel consists of an

Table 5.1. Measured 4×1 Tx and Rx Beamformers Performance

Parameter	Rx Beamformer	Tx Beamformer
Electronic Gain (dB)	23	34
3-dB Bandwidth (GHz)	15-57	15-52
Midband NF (dB)	5-6.2	-
IP_{1dB}/ch. (dBm)	-28 to -25	-21 to -18
OP_{1dB}/ch. (dBm)	-6 to -3	12 to 14.8
Phase resolution	5-bits	5-bits
RMS phase error (°)	<5.5	<5.5
Gain control (dB)	18	16.5
P_{DC}/ch. (mW)	200	250 at P_{1dB}

active balun, 5-bit phase shifter, 4-bit variable gain amplifier (VGA), and a wideband two-stage power amplifier [67]. The Rx beamformer chip also has four RF beamforming channels. Each channel consist of a three-stage low-noise amplifier (LNA), 5-bit phase shifter, 4-bit VGA, and a differential to single ended active stage. The RF output signals are combined using the on chip two-stage Wilkinson network. A 4×1 layout is adopted to place the chips with close proximity to the linear Vivaldi antenna array and minimize routing loss [37].

The beamformer chips are fabricated in the Tower-Semi 5^{th} generation SiGe BiCMOS process with an f_t/f_{max} of 272/305 GHz referenced to the top metal [4]. 380 μm pitch bumps are used so the beamformer chips can be directly flipped on a PCB without a multilayer laminate interposer [Fig. 5.2(a) and (b)]. The measured Tx and Rx chip performance is summarized in Table I. The Rx beamformer has 23 dB peak electronic gain with 5-bit phase control, 18 dB gain control, and a 15-57 GHz 3-dB bandwidth [Fig. 5.2(c)]. The midband NF is 4.9-6.2 dB with an input 1-dB compression point (IP_{1dB}) of -28 to -25 dBm and 200 mW/channel power consumption [Fig. 5.2(e)]. The Tx beamformer has a chip peak gain of 28 dB including the 6 dB division loss to the four channels, 5 bit phase control, 16.5 dB gain control, and 15-52 GHz 3-dB bandwidth [Fig. 5.2(d)]. The measured output P_{1dB} is 12–14.8 dBm at 16-52 GHz and the chip consumes 250 mW at P_{1dB} [Fig. 5.2(f)]. The chip gain in both Tx and Rx beamformers is defined from the antenna port to the common port and includes 2.7-3 dB on-chip transmission lines and Wilkinson ohmic loss.

The chips are controlled using a serial peripheral interface (SPI) for gain, phase, and bias current settings. The Rx beamformer chip operates from a 2 V supply and the Tx beamformer chip from a 3 V for the power amplifiers and 2 V for the rest of the chip.

5.3 System Analysis and Design

The (16×4) phased-array antenna directivity (D_{Ant}) is obtained using:

$$D_{Ant} = 10\ log_{10}(\frac{4\pi A}{\lambda^2}) \tag{5.1}$$

where A is the aperture area = $(N_x d_x) \times (N_y d_y)$, $N_x = 16$ and $N_y = 4$ are the number of elements in the horizontal and vertical directions, λ is the wavelength, $d_x = 2.54$ mm and $d_y = 2.5$ mm are the antenna elements spacing in the x and y directions. The phased-array antenna gain is:

$$G_{Ant} = D_{Ant} - L_{Ant} \tag{5.2}$$

where L_{Ant} is comprised of the antenna efficiency, feedline ohmic loss between the chip and the antenna input, and the mismatch loss (L_{Ant} =1.2-1.6 dB). With a grid of $0.49\lambda \times 0.48\lambda$ at 58 GHz, the 64-element array achieves a gain of 11.25-20 dB at 16-52 GHz. The 3-dB beamwidth with uniform illumination is given by:

$$BW_{3dB} = 50.76^o(\frac{\lambda}{N_x d_x}) \tag{5.3}$$

The array beamwidth is inversely proportional to the array linear dimension ($N_x d_x$). For the 16×4 array, the azimuth-plane beamwidth is 7.2^o, 9.86^o, 13.38^o at 52, 39, and 28 GHz respectively. A wide beam is expected in the elevation-plane since the linear dimension is only 10 mm ($0.67\text{-}1.67\lambda$ at 20-50 GHz). The Tx and Rx phased-arrays parameters and specifications are summarized in Table II.

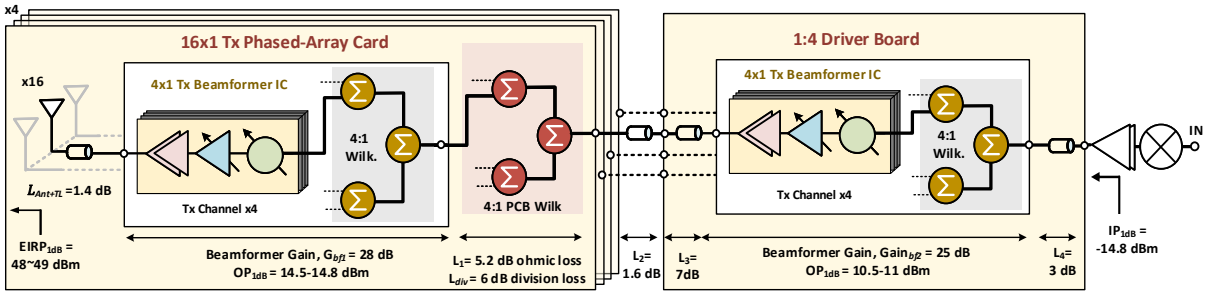


Figure 5.3. System diagram of the 64-element transmit phased-array based on the wideband 4×1 Tx beamformer chip. All values at midband (30-35 GHz).

5.3.1 64-Element (16×4) Tx Phased-Array

5G FR2 regulations limit the maximum EIRP to 75 dBm/100 MHz for fixed base stations, 55 dBm for transportable stations, and 45 dBm for mobile stations. With a 64-element phased-array base station, an area coverage of 100–300 m radius can be achieved with an EIRP of 50–55 dBm [68]. Fig. 5.3 presents the system view of the wideband 64-element Tx phased-array. The array EIRP is:

$$EIRP = 10\,log_{10}(N) + G_{Ant} + P_{ch} \tag{5.4}$$

where $N = 64$ is the total number of elements, P_{ch} is the channel output power, and G_{Ant} is the 64-element phased-array antenna gain (defined in eq. 2). The Tx array electronic gain (G_{Tx}) is defined as the output power per element divided by the input RF power ar the connector and is:

$$G_{Tx} = G_{bf_1} - L_{div} + G_{bf_2} - L_{ohmic} \tag{5.5}$$

where L_{div} = 6 dB is the division loss in the two-stage on PCB Wilkinson network. L_{ohmic} = 5.2 + 1.6 + 7 + 3 = 16.8 dB is the total ohmic losses of the transmission lines, Wilkinson network and RF cable interconnect. With G_{bf_1}=28 dB and G_{bf_2}=25 dB (driver chip is operated in single-ended mode), the Tx array electronic gain G_{Tx} is 30.2 dB at midband (35 GHz). The Tx array gain versus frequency is presented in Fig. 5.4(a).

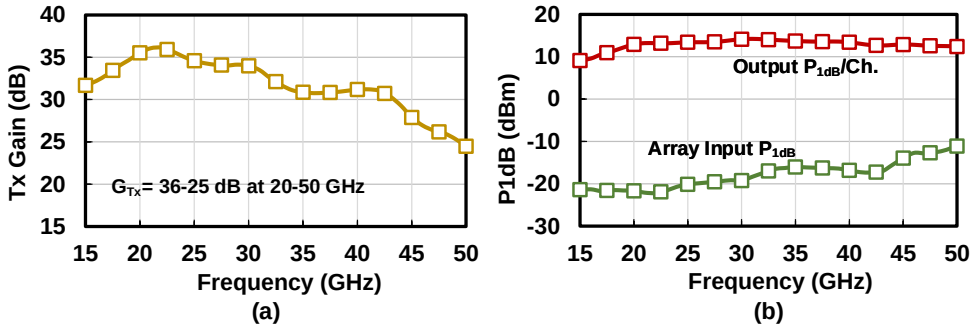


Figure 5.4. (a) 64-element Tx array electronic gain (G_{Tx}). (b) Tx phased-array input P_{1dB} and output P_{1dB}/channel.

The required input P_{1dB} at the RF port is:

$$IP_{1dB} = OP_{1dB} - (G_{Tx} - 1dB) \tag{5.6}$$

The array requires an input power of -21.6 to -11.2 dBm [Fig. 5.4(b)] and results in an output P_{1dB} of 12.9-14.8 dBm/element and an $EIRP_{1dB}$ of 44.7-50.2 dBm at 20-50 GHz.

5.3.2 64-Element (16×4) Rx Phased-Array

Fig. 5.5 presents the Rx array system. The output of the 4 phased-array cards are combined together using another beamformer chip operated in a single-ended mode. Employing the second beamformer chip as an active 4:1 combiner boosts the array electronic gain and improves the Rx system NF. With total ohmic losses in the array of 16.8 dB (L_{ohmic}= 16.8 dB), G_{bf_1}= 22.5 dB, and G_{bf_2}= 19.5 dB, the Rx array electronic gain (G_{Rx}) is 25.2 dB at midband (35 GHz). The electronic gain versus frequency is presented in Fig. 5.6(a).

The receive system noise figure (F_{Rx}) is calculated using the Friis equation:

$$F_{Rx} = F_{bf_1} + \frac{L_{ohmic}-1}{G_{bf_1}} + \frac{F_{bf_2}-1}{G_{bf_1}/L_{ohmic}} \tag{5.7}$$

The total ohmic losses after the beamformer due to the PCB 4:1 Wilkinson network, transmission lines and RF cable and connectors is L_{ohmic}= 5.2+1.6+7= 13.8 dB and the second

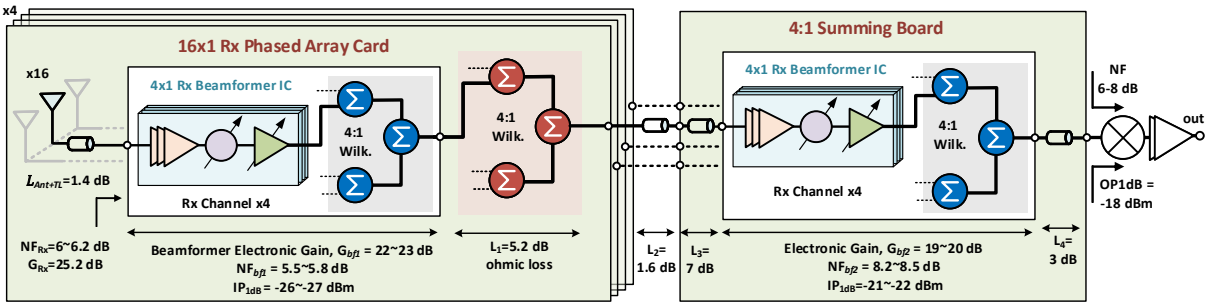


Figure 5.5. System diagram of the 64-element receive phased-array based on the wideband 4×1 Rx beamformer chip. All values at midband (30-35 GHz).

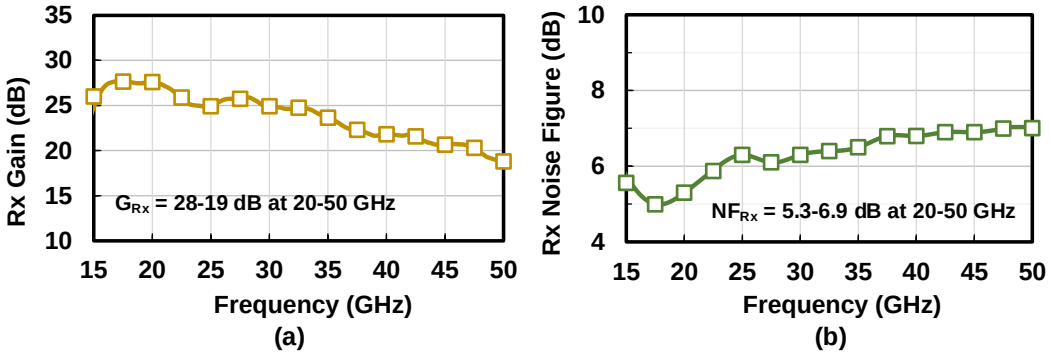


Figure 5.6. (a) 64-element Rx array electronic gain (G_{Rx}) and (b) system noise figure NF_{Rx} versus frequency.

beamformer chip has a NF of 8.25 dB when operated in single-ended mode. With 22.5 dB beamformer gain (G_{bf_1}), the system NF is degraded by 0.2-0.5 dB at 20-40 GHz. The noise contribution from the external downconverter is suppressed by the second beamformer gain and is negligible. The Rx system NF versus frequency is presented in Fig. 5.6(b).

The Rx system can also be characterized in terms of G/T (gain over temp). The system noise temperature is calculated using:

$$T_{sys} = T_{Rx} + T_{Ant'} \tag{5.8}$$

where T_{Rx} is the noise temperature at the beamformer input port. With T_o = 295 K, the T_{Rx} is calculated as:

$$T_{Rx} = T_o \times (F_{Rx} - 1) \tag{5.9}$$

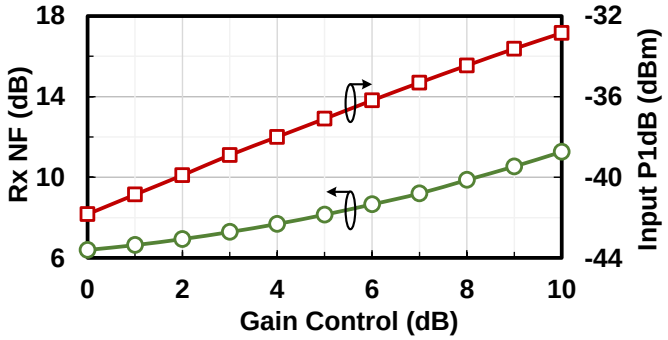


Figure 5.7. Rx phased-array input P_{1dB}/element and NF versus 10 dB gain control (lowering the beamformer gain from 22.5 to 12.5 dB at 30-35 GHz).

Table 5.2. Tx and Rx Arrays Parameters and System Calculations

Number of elements, N		64 (16x4)	
Frequency (GHz)		15-52	
Antenna spacing, d_x /d_y (mm)		2.54 / 2.5	
Antenna Gain, G_{ANT}(dB)		11.25-20	
Rx Array		**Tx Array**	
Rx system NF (dB)	5.8	Output P_{1dB}/ch. (dBm)	14.8
Antenna noise temp, $T_{ANT'}$ (K)	303	Array Input P_{1dB}	-15.4
G/T (dB/K)	-17.2	EIRP at P_{1dB} (dBm)	49

The antenna noise temperature $T_{Ant'}$ is calculated using:

$$T_{Ant'} = \eta \times T_{Ant} + T_o(1-\eta) \tag{5.10}$$

where $\eta = 10^{-L_{Ant}/10}$ and L_{Ant} = 1.2-1.6 dB. T_{Ant} is the antenna temperature and depends on the antenna environment. When the system is tested inside an anechoic chamber, T_{Ant}= 295 K and the gain to noise temperature (G/T) value is given as follows:

$$G/T = G_{Ant} - 10\,log_{10}(T_{sys}) \tag{5.11}$$

This results in a G/T of -18.7 to -14.1 dB/K at 20-50 GHz for the 64-element Rx array.

The Rx beamformer chip has an input P_{1dB} of -28 to -25 dBm at 20-50 GHz. The input P_{1dB}/element for the phased array is -40.6 to -43.5 dBm limited by the second beamformer chip (used as an active combiner) which has an input P_{1dB} of -20 to -23 dBm when operated in high

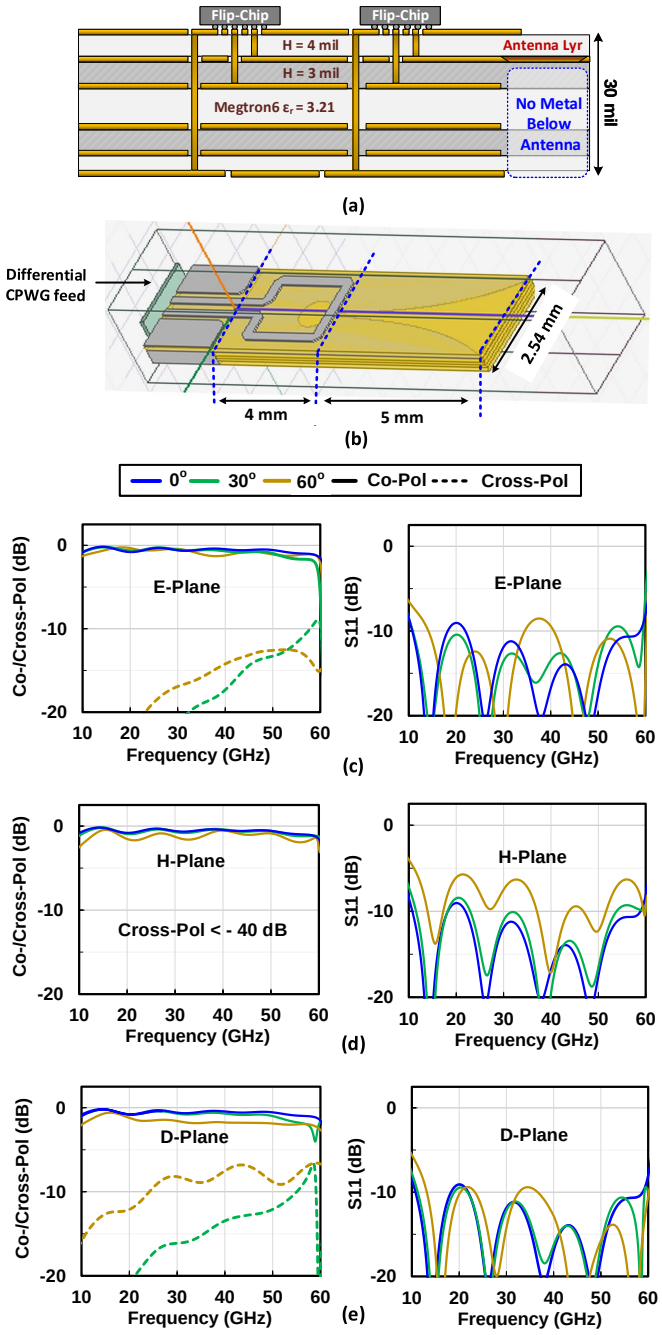


Figure 5.8. (a) 6-layer cost-efficient PCB stackup. (b) ANSYS HFSS simulated tapered-slot Vivaldi antenna. Simulated antenna impedance (S_{11}) and co/cross-pol. versus scan angle in (c) *E*-plane, (d) *H*-plane, and (e) *D*-plane.

linearity mode. A higher system input P_{1dB}/element of -32.8 dBm can be achieved by lowering the beamformer gain using the VGA at the expense of increasing the Rx system NF (Fig. 5.7).

5.3.3 Antenna Design

Fig. 5.8(a) presents the board stackup used to build the 64-element phased arrays. The beamformer ICs are placed on M1, interfacing with a 100 Ω differential coplanar waveguide transmission line (GSSG). The PCB thickness is 0.76 mm and this results in 1.74 mm air gap between different PCBs when placed together in a 2.5 mm (0.48λ at 58 GHz) vertical pitch. This air gap is sufficient to mount the beamformer chips and other supporting ICs.

The tapered-slot Vivaldi antenna is presented in Fig. 5.8(b). The M1 microstrip loop is used to feed the tapered-slot antenna on M2 with exponential growth slot-line. The antenna grid is selected as 2.54 mm×2.5 mm to mitigate transverse-electric (TE1) parallel plate mode between

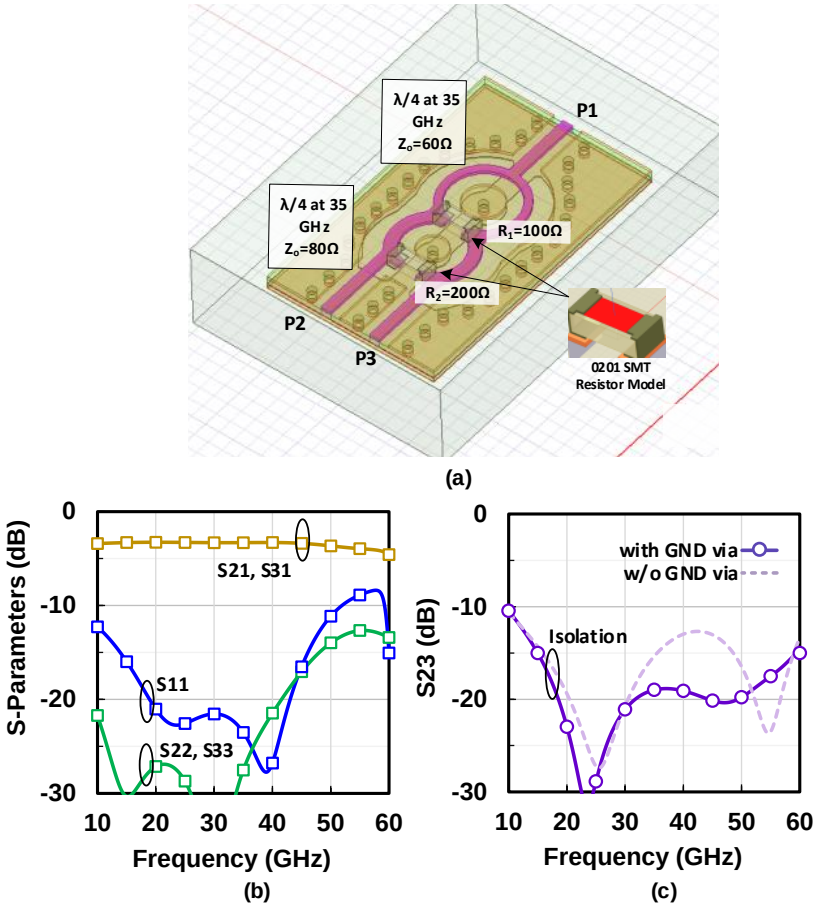


Figure 5.9. (a) PCB Wilkinson combiner/divider, (b) simulated S-parameters, and (c) isolation between the Wilkinson ports.

the phased array cards and suppress the higher order modes between the adjacent elements. The antenna is simulated using Ansys HFSS with master/slave boundary conditions [Fig. 5.8(c)-(e)]. The array has a very wide 3-dB bandwidth from 15-60 GHz and can scan up to +/- 60^o with $|S_{11}|$ < -10 dB in the E- and D-planes and < -7 dB in the H-plane at 15-55 GHz. The unit cell has a gain of -3.7 to 4.4 dB at 15-58 GHz including the differential feed ohmic loss. The antenna gain increases as f^2 which is standard in wideband arrays. Note that the cross-polarization component in the E-plane increases to -12.5 dB above 56 GHz.

5.3.4 Wilkinson Combiner/Divider Network

A wideband divider/combiner is achieved by implementing a two section circular design as shown in Fig 8(a). Middle ground vias are employed to minimize the coupling between the Wilkinson arms and enhance the ports isolation (S_{23}). The signal lines are implemented using M1 in stripline configuration with ground planes on M3 to synthesize the required characteristic impedance of 60 Ω and 80 Ω for the first and second section, respectively. A 200 Ω and 100 Ω surface mount resistors are used for the Wilkinson resistors. The Wilkinson network is simulated in HFSS and has an ohmic loss of < 0.6 dB (not including the 3 dB division loss) and an isolation > 20 dB at 17-50 GHz [Fig. 5.9(b) and (c)].

5.4 System Integration and Measurements

The front and back view of the 64-element (16×4) phased-arrays are shown in Fig. 5.10(a). The stacked arrays are connected to the combiner/driver board using phase-matched 1.85 mm cables and narrow-profile edge-launch connectors. The connector pad position is shifted for each card to allow for array stacking with 2.5 mm vertical pitch. Flat printed circuit (FPC) connectors with a height of 1.5 mm and cables are used to connect the phased-array cards with the bias/control board. The 4:1 Wilkinson network is laid out in a perfectly symmetrical design to have same length from the coaxial port to each of the 4 different chips. The 16×1 linear-array is surrounded with two dummy elements at both sides to improve the antenna performance at

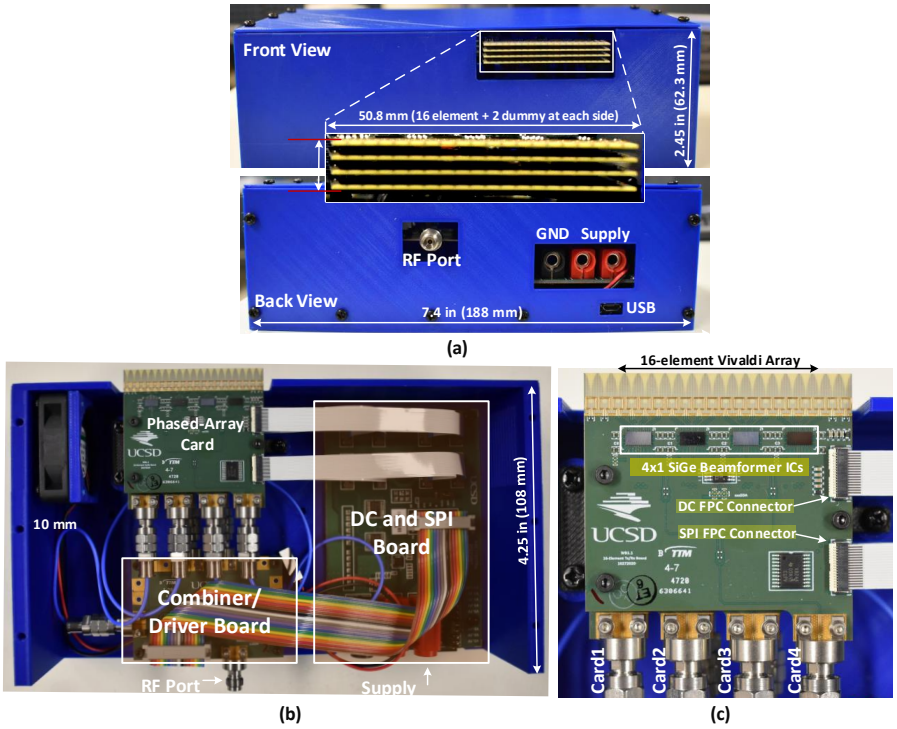


Figure 5.10. (a) Front and back view of the 16-52 GHz 64-element phased-array. (b) Top view of the system showing the 4-stack 16×1 phased-array cards and 4×1 combiner/driver board. (c) 16×1 linear phased-array with 4 SiGe beamformer chips.

large scan angles. Fig. 5.10(c) presents a top view of the 16×1 linear phased-arrays with 4 SiGe beamformer chips flipped on the PCB.

The array size is 50.8 mm×10 mm with a power consumption of 13.26 W in the Rx array and 17.6 W in the Tx array (at P_{1dB}). The power amplifiers in the Tx beamformer chips are designed in class AB mode, and the Tx array power dissipation decreases to 15.5 W at 7 dB backoff from P_{1dB}.

5.4.1 Array Calibration and S-Parameter Measurements

The 64-element Tx and Rx phased arrays are tested inside an ETS-5700 anechoic chamber at a range of 1.2 m using a vector network analyzer (VNA) [Fig. 5.11(a)]. A wideband horn with a gain of 8.2-12.9 dB at 15-50 GHz is used. To calibrate the 64-element phased arrays, each channel is turned-on individually and the far-field S_{21} is measured in the nominal gain and

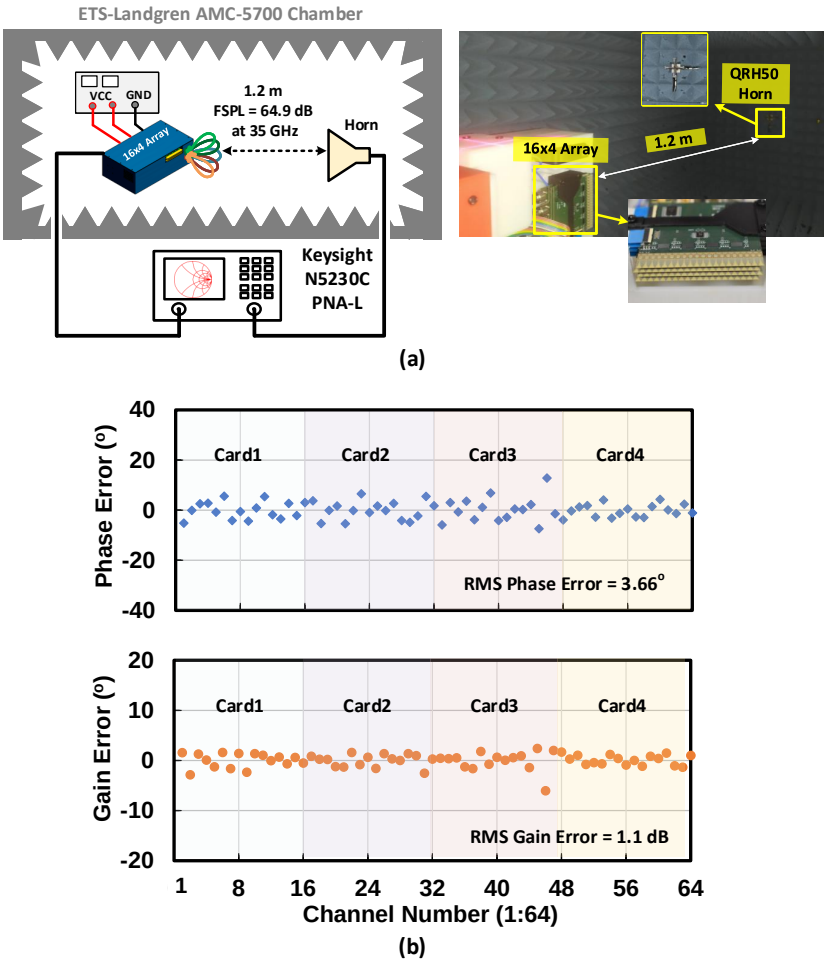


Figure 5.11. (a) Diagram and photograph of the measurement setup. (b) Residual phase error (3.6^o rms) and amplitude error (1.1 dB rms) for the 64-element Rx phased-array at 30 GHz.

phase state for each channel. After completing the 64 channels characterization, one channel is set as a reference and the gain and phase offsets are calibrated using the phase shifter and VGA control for each channel. The driver board is set at nominal gain and 0^o phase and is not used for calibration. The calibration is done at 20 GHz, 30 GHz, 40 GHz and 50 GHz, but could also be done every 5 GHz if needed.

To verify the calibration, the S_{21} for each channel is remeasured and the rms phase and gain errors are calculated after phase calibration. Fig. 5.11(b) presents the residual phase and gain errors for the 64-elements Rx array at 30 GHz after calibration showing an rms phase error <3.6^o and rms amplitude error <1.1 dB. The 64-element Tx array calibration follows the same

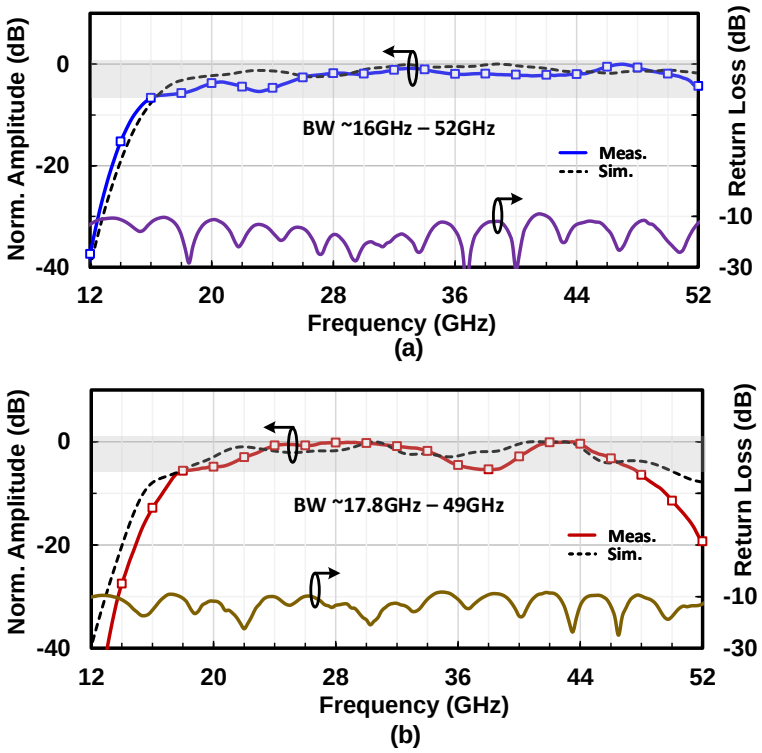


Figure 5.12. Measured and simulated co-polarized frequency response and return loss at broadside with uniform illumination for (a) 16×4 Rx phased-array and (b) 16×4 Tx phased-array.

method and has similar rms errors.

The far-field S-parameter measurements are conducted at broadside with the setup shown in Fig. 5.11(a). For the Rx array:

$$S_{21} = G_{Ant} + G_{Rx} - FSPL + G_{Horn} \tag{5.12}$$

The $FSPL = (\lambda/4\pi R)^2$ and horn gain are removed and the normalized Rx array frequency response ($G_{Ant} + G_{Rx}$) is presented in Fig. 5.12(a). Since G_{Ant} increases proportional to f^2 and G_{Rx} decreases by 6.1 dB from 25-50 GHz [Fig. 5.6(a)], the measured frequency response varies by +/- 1.8 dB at 25-50 GHz.

For the 64-element Tx array:

$$S_{21} = G_{Ant} + G_{Tx} + 10log(N) - FSPL + G_{Horn} \tag{5.13}$$

The normalized Tx array frequency response ($G_{Ant} + G_{Tx} + 18\ dB$) is presented in Fig. 5.12(b). As G_{Tx} drops by 10.13 dB from 25 to 50 GHz [see Fig. 5.4(a)] and G_{Ant} increases as f^2, the measured frequency response varies by +/- 2.5 dB at 25-48 GHz.

Both the Tx and Rx arrays show broadband performance and the operational bandwidth is mainly limited by the measurement setup at > 49 GHz. The Rx array shows a wider bandwidth since the Rx beamformer chips have a 3-dB bandwidth which goes up to 57 GHz as shown in Fig. 5.2. The Rx and Tx arrays have a wideband low return loss (< -10 dB) at 12-52 GHz.

5.4.2 Pattern Measurements

Fig. 5.13 presents the measured azimuth plane (E-plane) patterns for the Rx array at 20-50 GHz with uniform illumination. The measured patterns demonstrate good agreement with simulated patterns and with 3-dB beamwidths at boresight of 18.5^o, 12.6^o, 9^o, 7.2^o at 20, 30, 40, and 50 GHz, respectively [Fig. 5.13(a)-(d)]. The cross-pol. level is <-19 dB at 20-40 GHz at broadside and is <-16 dB at 60^o scan angle. The cross-pol. level reaches up to -12.6 dB at 50 GHz. This is expected from the Vivaldi antenna performance and agrees with simulations. The active patterns fit a $\cos(\theta)^{1.3}$ roll-off with a 3.9-dB drop at +/-60^o at 20-50 GHz.

For angular wide coverage and short-distance links, the phased-array can be excited to synthesize a flat-top pattern to serve multiple users at the same time. This is accomplished by placing a sinc function across the aperture with a width adjusted to determine the pattern beamwidth. The amplitude and phase of each element, $A(n)$, are determined using:

$$A(n) = sinc(\frac{r(n - \frac{N_x - 1}{2}))}{N_x - 1}) \tag{5.14}$$

where n is the element number, N_x = 16 is the number of elements in one row, and r is

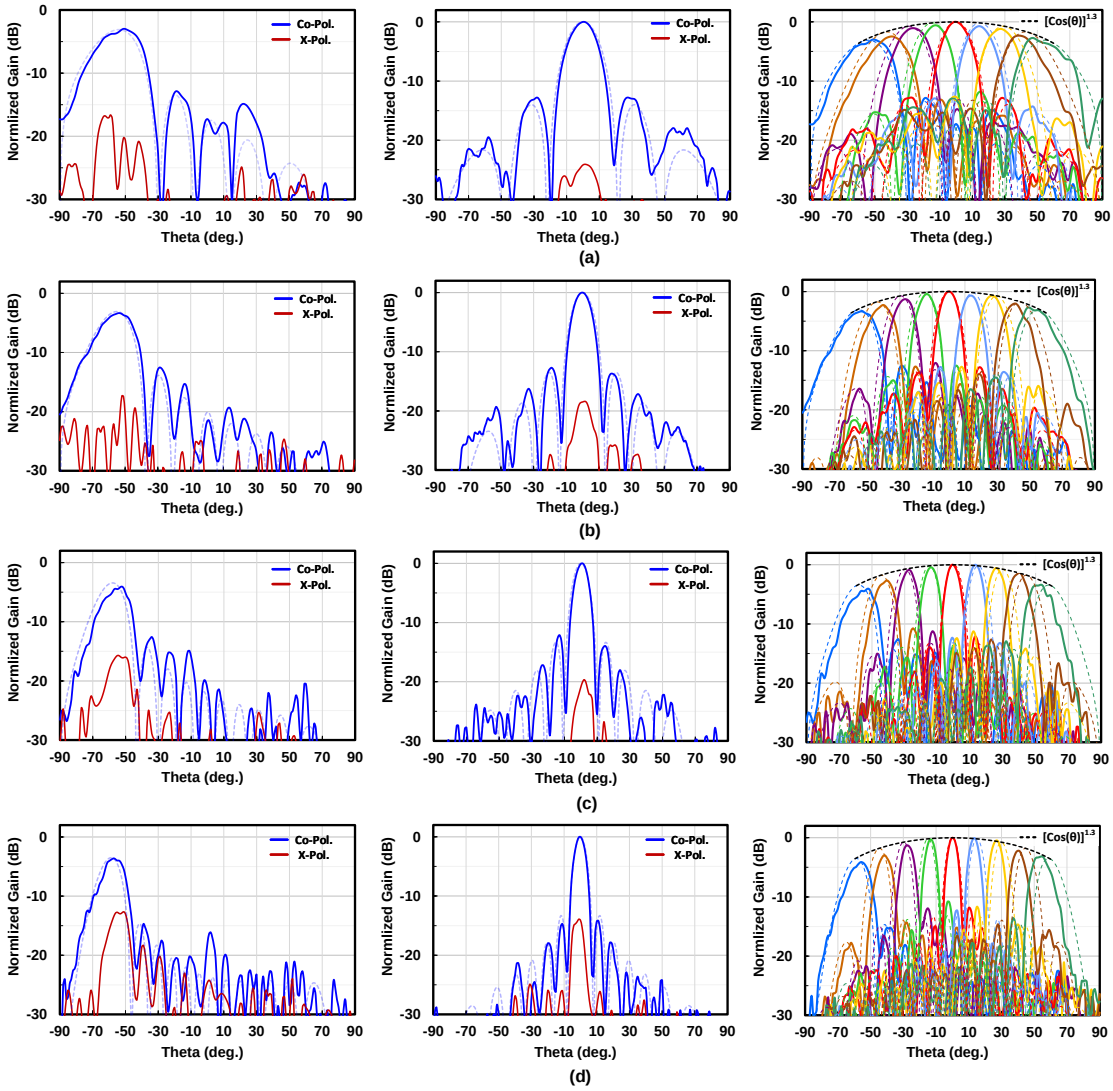


Figure 5.13. Measured azimuth-plane patterns at 0^o, -60^o, and -60^o to 60^o with uniform illumination at (a) 20 GHz, (b) 30 GHz, (c) 40 GHz, and (d) 50 GHz.

the pattern rate to result in flat-top patterns. Fig. 5.14 presents the measured flat-top patterns for r = 2, 3, and 4 at 30, 40 and 50 GHz.

The 64-element phased array can also be used for tracking applications using a difference (monopulse) pattern as demonstrated in [82]. This pattern is realized by setting the phases on the elements for a specific scan angle and then adding a 180^o phase shift to half of the array elements to result in a null at the scan angle. The measured monopulse patterns are presented in Fig. 5.15 at -30^o, 0^o, and 30^o at 30 GHz. The achieved null depth is -30 to -22 dB compared to

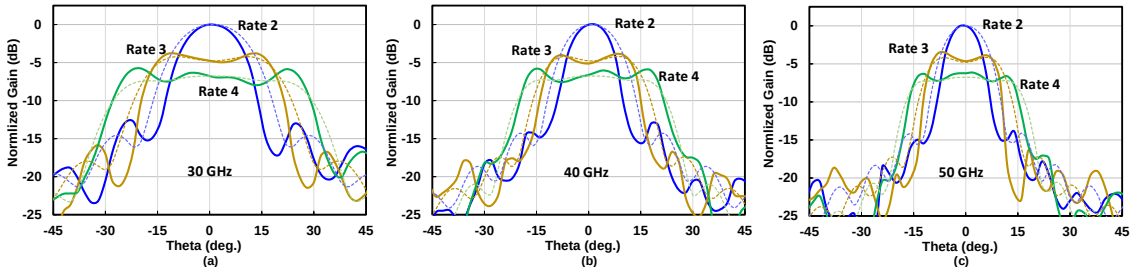


Figure 5.14. Measured azimuth-plane flat-top patterns for different rates at (a) 30 GHz, (b) 40 GHz, and (c) 50 GHz.

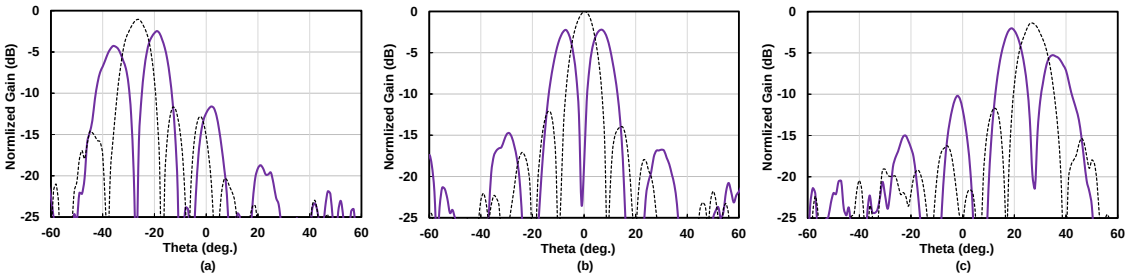


Figure 5.15. Measured monopulse patterns (solid) at (a) -30^o, (b) 0^o, and (c) 30^o in the azimuth-plane. Uniform illumination patterns are also shown (dashed). All patterns are normalized to the untapered 30-GHz pattern at boresight.

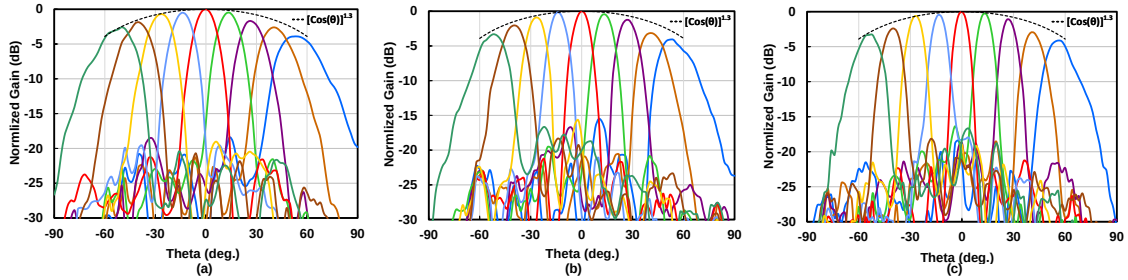


Figure 5.16. Measured azimuth-plane patterns at +/-60^o scan angles with 8-dB raised cosine taper illumination at (a) 30 GHz, (b) 40 GHz, and (c) 50 GHz.

uniform illumination.

The sidelobe levels can be reduced by applying an 8-dB raised-cosine taper illumination on the antenna aperture using the beamformers VGA gain control. For a raised-cosine taper, the elements normalized amplitude is set using:

$$A(n) = \alpha + (\alpha - 1) \times cos(\frac{2\pi(n-1)}{N_x - 1}) \tag{5.15}$$

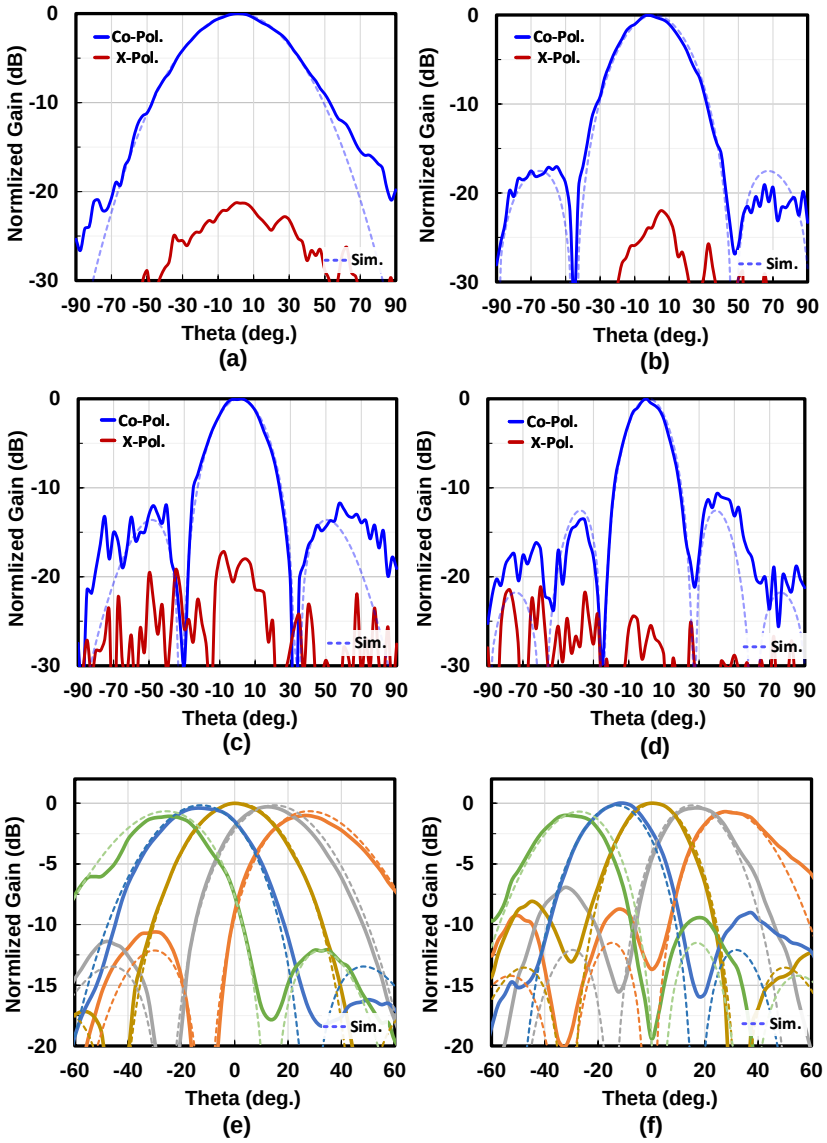


Figure 5.17. Measured boresight elevation-plane patterns at (a) 20 GHz, (b) 30 GHz, (c) 40 GHz, and (d) 50 GHz. Measured patterns with -30^o to 30^o scan settings at (e) 30 GHz and (f) 40 GHz.

where $\alpha = (1 + 10^{\frac{-L}{20}}/2)$ is the edge taper in dB ($L = 8$). The measured tapered patterns at 30, 40, and 50 GHz with scan angles of -60^o to 60^o are shown in Fig. 5.16. At broadside, the 3-dB beamwidths are 14.2^o, 11.5^o, and 9.7^o at 30, 40, 50 GHz, respectively, with slidelobes level < -21.7 dB. At +/-60^o scan angles, the sidelobes levels are <-17 dB.

The elevation plane (H-plane) broadside patterns are also measured at 20-50 GHz and

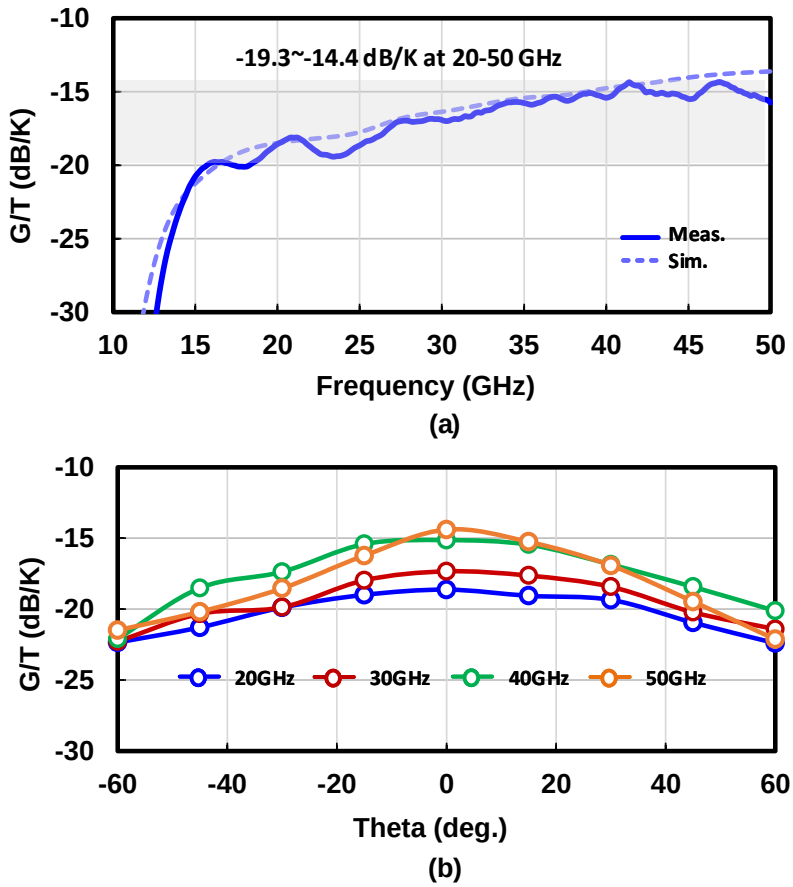
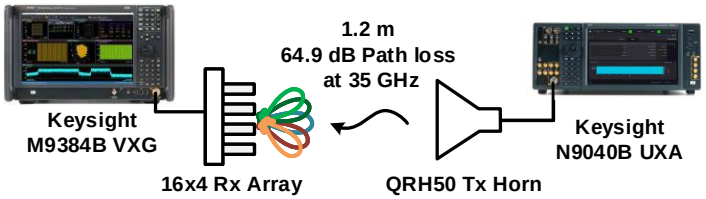


Figure 5.18. (a) Measured G/T versus frequency of the 64-element Rx phased-array at broadside and uniform illumination with T_{ant} = 295 K. (b) Measured G/T with -60^o to 60^o scan angles at 20, 30, 40, and 50 GHz.

agree well with simulations (Fig. 5.17). The cross-pol. level is <-20 dB at 20-50 GHz. Due to limited number of elements in elevation ($N_y = 4$), a wide 3-dB beamwidth of 22.5^o is measured at 50 GHz and the beams become much wider at 20 GHz. This is a result of an antenna spacing of only 0.17λ and an array size of 0.68λ at 20 GHz. The beam can be scanned from -30^o to 30^o in the elevation plane with slidelobe levels < -10 dB at 30 GHz. Also due to array size, the edge effects dominate and limit scan angles to $<30^o$ with low sidelobes.

The 64-element Tx array pattern measurements show similar performance to the Rx array and are not presented for brevity.



(a)

Modulation	QPSK	16-QAM	64-QAM	256-QAM
BW (MHz)	400	400	400	400
Constellation (25 GHz)				
Rx EVM (%)	1.97	1.96	1.97	1.97
Constellation (29 GHz)				
Rx EVM (%)	2.1	2.07	2.07	2.04
Constellation (38 GHz)				
Rx EVM (%)	2.6	2.6	2.59	2.57
Constellation (42 GHz)				
Rx EVM (%)	2.55	2.55	2.54	2.55

(b)

Figure 5.19. (a) 64-element (16×4) Rx array EVM measurement setup and (b) measured 1.2 m OTA constellation and EVM performance at 25, 29, 38, and 42 GHz with 5G-OFDMA waveforms.

5.4.3 Rx Array G/T and EVM Measurements

The measured G/T versus frequency at broadside with uniform illumination and $T_{Ant} =$ 295 K is presented in Fig. 5.18 (a). This is done using the Keysight N5245B PNA-X with noise figure option (S93029B), and according to the technique described in [83]. A -19.3 to -14.4 dB/K is measured at 20-50 GHz and agrees with simulations. Also, the G/T versus scan angle is measured at 20, 30, 40, and 50 GHz and the drop follows a $\cos(\theta)^{1.4}$ curve as expected from the

scan loss [Fig. 5.18(b)].

A 1.2 m link is conducted using the 64-element Rx array and a Tx horn. The array EVM performance is measured with 400 MSym/s 5G-OFDMA waveforms in QPSK, 16-QAM, 64-QAM, and 256-QAM modulation schemes at the mm-wave 5G FR2 key bands (25, 29, 38 and 42 GHz) and with >12 dB backoff from the array input P_{1dB}/element. A vector signal generator (Keysight M9384B VXG) is used to generate the complex-modulated signals, and a Keysight UXA spectrum analyzer is used with the 89600 VSA software to capture the signal and extract the constellations and EVMs [Fig. 5.19(a)]. The measured constellations and EVMs at normal incidence are summarized in Fig. 5.19(b). Data transmissions of up to 256-QAM (3.2 Gb/s) is

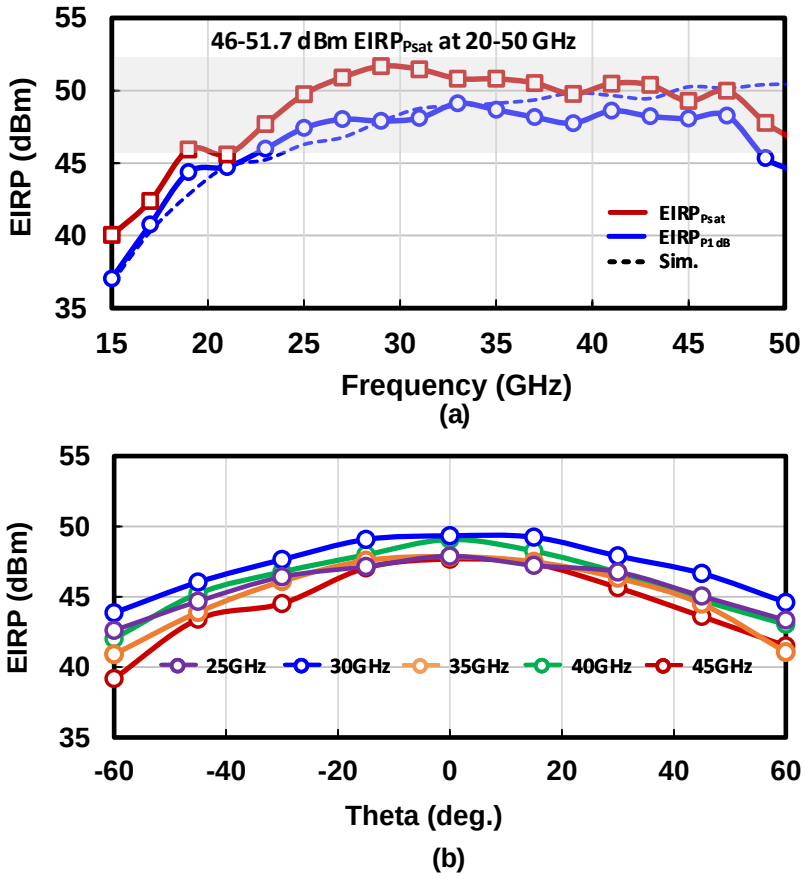


Figure 5.20. (a) Measured EIRP versus frequency of the 64-element Tx phased-array at broadside and uniform illumination with P_{1dB} and P_{sat} conditions. (b) Measured EIRP at P_{1dB} with -60^o to 60^o scan angles at 25, 30, 35, 40, and 45 GHz.

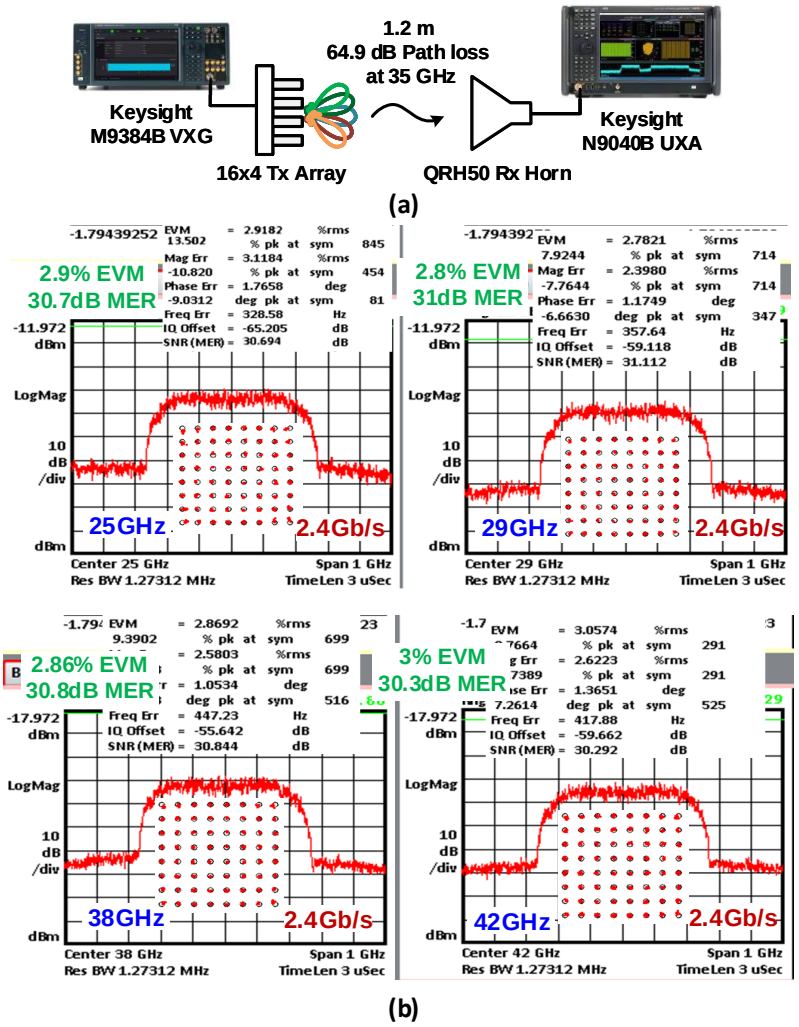


Figure 5.21. (a) 16×4-element Tx array EVM measurement setup. (b) Measured spectrum and constellation at 25, 29, 38, and 42 GHz center frequency and 38-39 dBm EIRP with single-carrier 400 MHz 64-QAM waveform (2.4 Gb/s).

supported by the array. The measured EVMs are <1.97% at 25 GHz, <2.07% at 29 GHz, <2.6% at 38 GHz, and <2.55% at 42 GHz demonstrating multi-band 5G NR FR2 operation.

5.4.4 Tx Array EIRP and EVM Measurements

The EIRP measurement is conducted for the 64-element (16×4) Tx phased-array inside the anechoic chamber using the Keysight E8257D signal generator and the Keysight 1913A power meter. An EIRP of 45-49 dBm at P_{1dB} operation is measured at 20-50 GHz with uniform

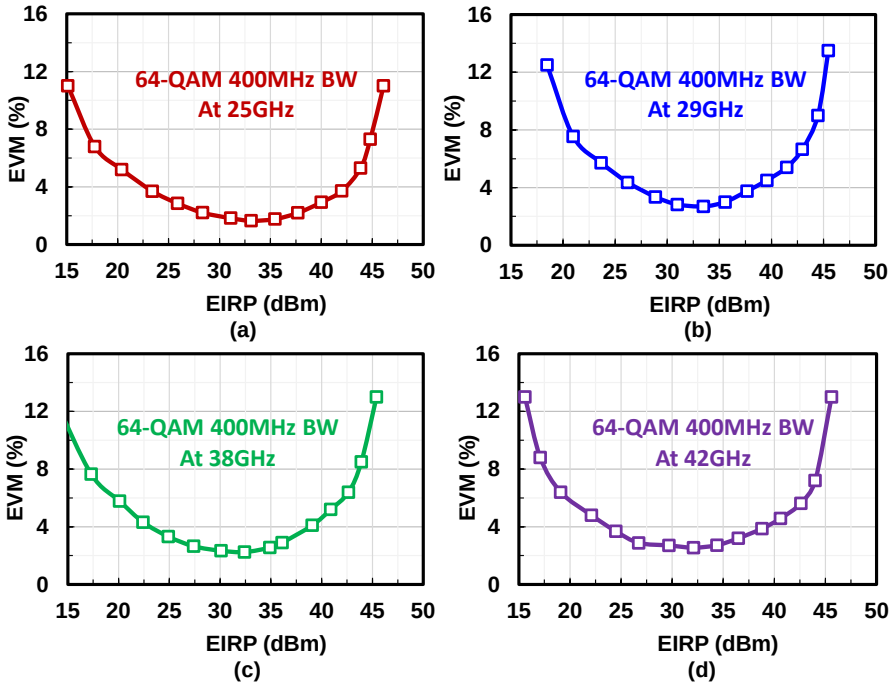


Figure 5.22. (a) Measured EVM versus EIRP with 64-QAM 400 MHz BW waveform at (a) 25 GHz, (b) 29 GHz, (c) 38 GHz, and (d) 42 GHz.

illumination and agrees with simulated EIRP at P_{1dB} [Fig. 5.20(a)]. The measured peak EIRP is 46-51.7 dBm with P_{sat} operation at 20-50 GHz. Also, the EIRP versus scan angle is measured at 25, 30, 35, 40, and 45 GHz with +/- 60^{o} scan angles and presented in Fig. 5.20(b).

The EVM performance of the 64-element Tx array is first evaluated with 400 MSym/s single-carrier 64-QAM waveform filtered with a root-raised cosine pulse shaping filter with a roll-off factor α= 0.35 and has a PAPR of 7.7 dB. This measurement is conducted for multiple-bands (25, 29, 38 and 42 GHz) at broadside and with uniform illumination. The measurement setup, measured spectrum, constellation, and EVM values are presented in Fig. 5.21. The EVM versus EIRP level is also measured to assess the array performance at different backoff levels and the results are presented in Fig. 5.22. All reported EVM values are rms values referenced to the constellation peak. An EVM value <5% with an EIRP of 41-43 dBm is achieved at 25-42 GHz.

5G NR waveforms with 400-MHz channel bandwidth in QPSK, 16-QAM, 64-QAM, and 256-QAM are used to evaluate the Tx array performance. The measured constellations and

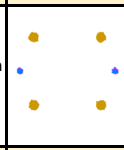
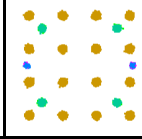
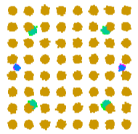
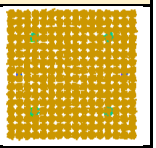
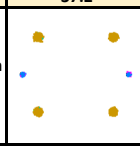
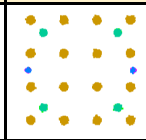
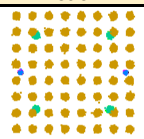
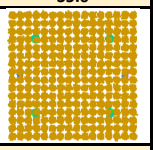
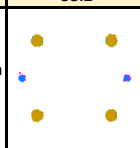
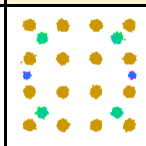
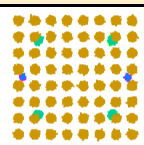
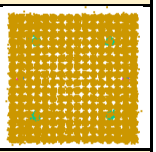
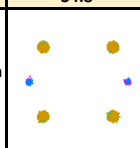
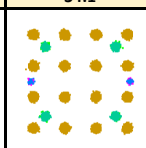
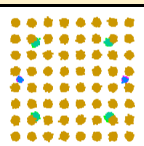
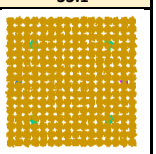
Modulation	QPSK	16-QAM	64-QAM	256-QAM
BW (MHz)	400	400	400	400
Constellation (25 GHz)				
EVM (%rms)	2.9	2.85	2.86	2.98
EIRP (dBm)	37.2	37.5	36.9	35.6
Constellation (29 GHz)				
EVM (%)	2.87	2.88	2.85	2.89
EIRP (dBm)	38.2	37.5	37.9	36.6
Constellation (38 GHz)				
EVM (%)	2.96	2.97	2.95	2.98
EIRP (dBm)	34.8	34.1	33.8	33.1
Constellation (42 GHz)				
EVM (%)	3.05	2.98	2.99	3.03
EIRP (dBm)	35.1	35.4	35.2	35.3

Figure 5.23. Measured 1.2 m OTA constellation and EVM performance using 64-element Tx phased array.

EVMs at 25, 29, 38, and 42 GHz are summarized in Fig. 5.23. Communication links with up to 256-QAM modulation are established with EVM levels <2.98% and 34-38 dBm EIRP at 25-42 GHz demonstrating state-of-the art multi-band performance.

A comparison with the recent 5G FR2 mm-wave phased-arrays is presented in Table III. This work achieves the widest coverage at 16-52 GHz.

5.5 Conclusion

This work presented 64-element (16×4) Tx and Rx phased-arrays based on the slat-array architecture with wideband Vivaldi antennas. The arrays are built using 16×1 linear arrays with 4×1 beamformer chips. The 64-element Rx phased-array demonstrates a system NF of 5.3-6.9 dB and a G/T performance >-16.9 dB/K at 30-50 GHz. The 64-element Tx phased-array achieves

Table 5.3. Performance Comparison of mm-Wave Phased Arrays For 5G NR FR2

Beamformer Chip Performance							
Design	This work	[14] RFIC'19	[24] TMTT'20	[8] JSSC'20	[16] TMTT'21	[6] JSSC'18	[15] JSSC'20
Technology	0.18 um SiGe BiCMOS	28-nm CMOS	0.18 um SiGe BiCMOS	65-nm CMOS	0.18 um SiGe BiCMOS	0.18 um SiGe BiCMOS	65-nm CMOS
Frequency (GHz)	Tx: 16-50.5 / Rx: 15-57	37-40	37-42	39	23.5-29	28.4.4-29.4	28
Fractional BW (%)	Tx: 106 / Rx: 117	7.8	12.6	-	22.6	3.46	-
Architecture	4×1 Tx / 4×1 Rx RF-PS	8×1 Tx/Rx RF-PS	2×2 Tx/Rx RF-PS	2×2 Tx/Rx LO-PS	2×2 Tx/Rx RF-PS	2×2 Tx/Rx RF-PS	Two 4×1 Tx/Rx RF-PS
Integration/Chip	Beamformer	Beamformer	Beamformer	Full transceiver	Beamformer	Beamformer	Beamformer
Phase Resolution (bit)	5	5	6	0.05°	6	6	0.4° RMS error
Gain Control (dB)	16.2/18	10.2	25	-	26	14	-
Tx Gain/Ch (dB)	34.3	45-48	25	3 (CG)	19	20	20
Tx OP1dB (dBm)	13.5-14.7* (20-50 GHz)	10.2-12.3	10-11	9	15-16	10.5	11.3
Tx Psat (dBm)	14.4-15.3	-	12	15.5	-	12.5	15.1
Tx P_{DC}/Ch. (mW)	250 at P1dB	339 at P1dB	250 at P1dB	375 at P1dB	340 at P1dB	200 at P1dB	252 at P1dB
Rx Gain (dB)	22	41.9	26	3 (CG)	19	20	17
Rx NF/ Path (dB)	4.7-6.2*	6-7.6	5.5	7.7	5.5	4.6	4.2-5
Rx IP1dB (dBm)	-28 to -25	-36 to -44	-28	-22	-19	-22	-
Rx P_{DC}/Ch. (mW)	200	78.5	150	125	156	130	112.5
Chip Area (mm2)	11	17.2	12.96	12	12.5	11.75	12
Phased-Array Performance							
Array size	16×4	4×4	8×8	16×4	8×8	8×4	8×4
Polarization	Single	Dual	Single	Single	Single	Single	Dual
Peak EIRP (dBm)	50-51.7	-	51	53	54.8	45	45.6
5G Multi-Band Operation	Yes	-	-	-	Yes	-	-
OTA Distance (m)	1.2	-	1	1	1.3	5	1
Scan Range, Az (o)	+/- 60	+/- 45	+/- 60	+/- 40 (4×1 array)	+/- 60	+/- 50	+/- 50
Constellation	64-QAM	64-QAM	64-QAM	64-QAM MCS19	64-QAM	64-QAM	64-QAM
Data Rate	2.4 Gb/s	0.6 Gb/s	1.2 Gb/s	2.4 Gb/s	1.2 Gb/s	3 Gb/s	15 Gb/s
EVM (%)	2.9 39 dBm EIRP Tx EVM	-	5 44 dBm EIRP Tx EVM	3 - Tx-Rx EVM	5 47 dBm EIRP Tx EVM	4.46 Tx-Rx EVM	6.16 35.2 dBm EIRP Tx EVM
5G NR Evaluated	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	64-QAM OFDM, 100MHz BW	-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW	-	-	QPSK, 16QAM, 64-QAM, 256-QAM OFDM, 400MHz BW

* w/o TRx switch

an EIRP of 45.9-51.7 dBm at 20-50 GHz. These arrays also demonstrated ultra-wideband performance with +/-60^o beam steering capabilities. 5G-NR standard compliant packets at 1.2 m link distance and up to 256-QAM are supported with 400-MHz channel bandwidth and <2.98% EVM at all 5G FR2 bands. Future work will include expanding this work to Tx/Rx functions in the same array and building dual-polarized/dual-beam versions to support MIMO links.

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Chapter 6

15-52 GHz Multi-band Tx/Rx Beamformer IC and 16×1 Linear Phased-Array for Wideband Multi-Gb/s 64-QAM Links

6.1 Introduction

As discussed in previous chapters, the mm-Wave 5G communications are advancing to accommodate the increasing data-rate demands. The current allocated bands in the 5G new radio frequency range 2 (NR FR2) include n257 band (26.5-29.5 GHz), n258 band (24.25-27.50 GHz), n259 (39.5-43.5 GHz), n260 band (37-40 GHz), and n261 band (27.5-28.35 GHz) [62]. Also, several regions globally started auctions in FR2 for 26, 39, and 47 GHz bands. The FR2 spectrum is vast and requires a multi-standard Tx/Rx communication system capable of supporting current and future bands. This system will reduce the development costs and enable operators to utilize key features such as network roaming and interband carrier aggregation.

The 24.25-52.6 GHz bands suffer from higher free space path loss (FSPL) compared with sub-6 GHz 5G operation. Therefore, directive communications based on affordable phased-arrays has been employed to build mm-wave 5G-communication systems based on advanced SiGe and CMOS processes. These silicon-based technologies result in low cost, high yield, and low power with unparalleled integration level and digital processing capabilities.

Prior art was mainly focused on targeting relatively narrow-band operation at the n257,

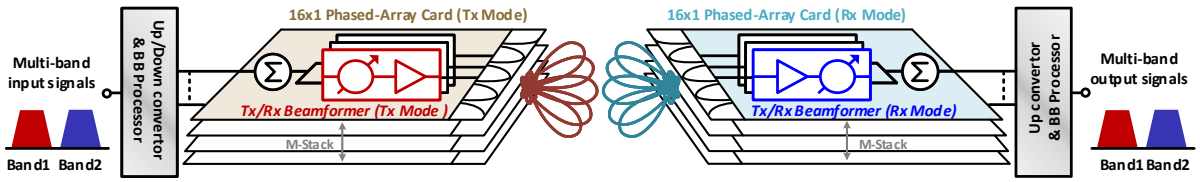


Figure 6.1. $16 \times M$ wideband Tx/Rx phased array based on stacked linear phased array modules.

n258 or n260 band. The fractional bandwidth (FBW) $(f_2 - f_1)/f_c$ is limited to $< 25\%$ by both the system and circuit design. Therefore, enhancements to the architectural and circuit levels are essential to realize multi-octave phased-array solution to support the multi-band 5G FR2.

This chapter presents a continuation of Chapters 3 and 4 and details the development of a transmit/receive (Tx/Rx) multi-band 4×1 beamformer IC and 16×1 phased-array module. An improved Rx channel with a lower power consumption and better LNA performance is implemented in this work. The Tx channel is also improved to support a wider band operation up to 54 GHz. Also, a wideband differential 16-55 GHz low-loss SPDT switch capable of power handling up to 17-18 dBm is designed and used on every channel. Wideband system and chip architectures, circuit design and measurements are reported in section 2. The phased-array system integration and measurements are carried out in section 3 including wideband pattern and effective isotropic radiated power (EIRP) measurements.

6.2 Multi-Band Tx/Rx Phased-Array

The phased-array design employs a brick-array architecture using linear phased-array modules (Fig. 6 .1). This architecture is selected to enable the design of end-fire Vivaldi antenna arrays commonly used in ultra-wideband systems [67]. A two-dimensional $N \times M$ phased array can be implemented by stacking M modules with each having N number of linear antenna elements.

All-RF beamforming architecture is adopted for 5G phased-arrays. This is because it has lower power consumption and complexity due to the elimination of the mixer and LO distribution

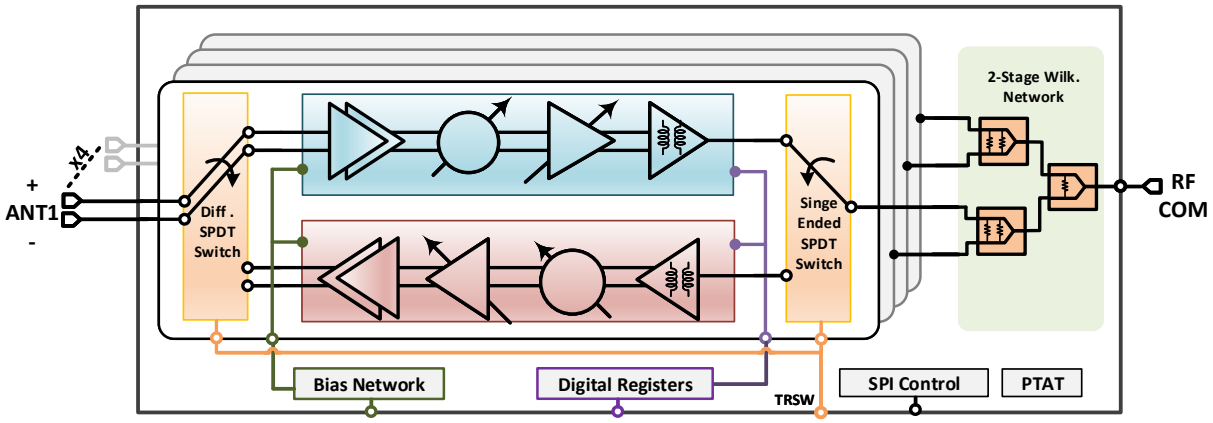


Figure 6.2. Block diagram of the wideband 4-channel Tx/Rx phased-array beamformer chip.

network required for other beamforming architectures [67], [37].

6.3 Wideband 4×1 Tx/Rx Beamformer Chip

The wideband Tx/Rx 4×1 beamformer chip architicture is presented in Fig. 6.2. Four RF Tx/Rx beamforming channels with Tx/Rx switches and 4:1 Wilkinson network are employed. In the Tx mode, the RF input signal is distributed to the channels using the Wilkinson network as 1:4 divider. Each channel consists of an active balun, 5-bit phase shifter, 4-bit variable gain amplifier (VGA), and a wideband two-stage power amplifier [67]. In the Rx mode, each channel consist of a three-stage low-noise amplifier (LNA), 5-bit phase shifter, 4-bit VGA, and a differential to single ended active stage. The RF output signals are combined using the two-stage Wilkinson network as a 4:1 combiner. A 4×1 layout is adopted to place the chips with close proximity to the linear Vivaldi antenna array and minimize routing loss [37]. A differential design is employed to preserve stability and reduce coupling between channels. The internal feedback caused by the package parasitic inductance is mitigated resulting in an improved input and output port isolation. This is due to the differential output port not being referenced to the PCB ground node.

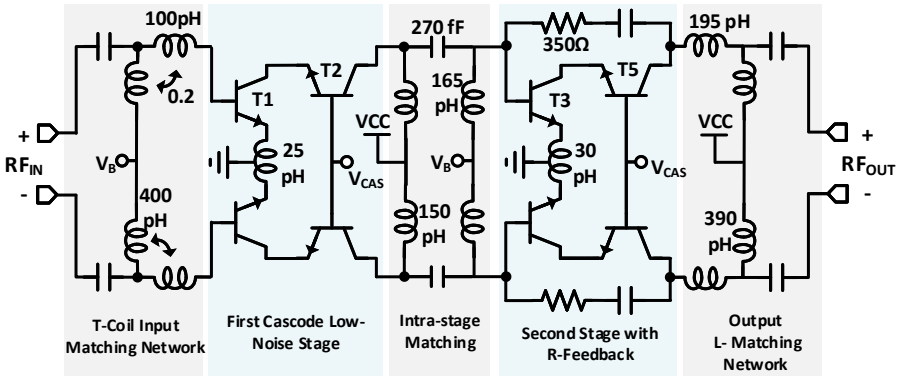


Figure 6.3. Two-stage 15-52 GHz low noise amplifier.

6.3.1 Circuit Design

The beamformer is designed using Tower-Semi SiGe BiCMOS 5th generation technology (SBC18S5) [64]. This process has 7 Aluminum layers, with a top metal layer thickness of 2.8 µm. A 3×4 µm SiGe HBT transistor has a simulated f_{max} and f_t of 305 and 272 GHz, respectively, at a current density of 1.5-2 mA/µm with parasitic extraction to the top metal layer.

The differential LNA design is based on two cascode stages with a total gain of 20-21 dB and a 3-dB BW of 15.3-52 GHz. The noise and power matching at the LNA input is realized by a differential asymmetric T-coil network with a degeneration inductor. The LNA devices are sized at 2×5 µm with the first stage biased at 0.45 mA/µm for low noise operation and with a sufficient gain to suppress noise contribution from the following blocks in the Rx channel. The inter-stage matching network is based on capacitively coupled resonators synthesizing a high-order band-pass filter [44] and resistive feedback to achieve wideband performance. In contrast with the LNA design in chapter 3, no resistive feedback is used at the input to avoid degrading the LNA NF. Also, as this design is targeted for lower power consumption and higher linearity performance, it employs only two cascode stages instead of three stages. The LNA has a simulated NF of 2.3-3.3 dB at 15.5-50 GHz (0.6-0.9 dB improvement from the design in Chapter 2). The LNA consumes 24 mA from a 2 V supply and has an input P_{1dB} of -12.8 dBm at 35 GHz. This LNA design is targeted to reduce the Rx channel power consumption and improve

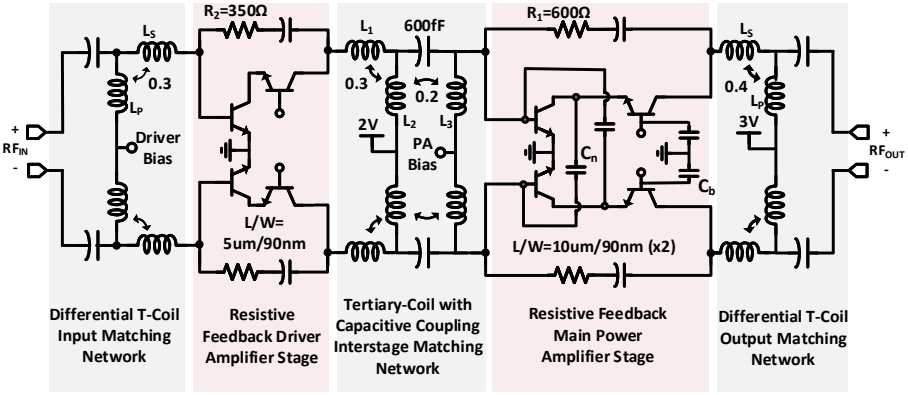


Figure 6.4. Wideband two-stage power amplifier with a 3 V supply for the main PA stage.

the linearity and NF performance at the expense of a narrower bandwidth and higher in-band ripples.

A class-AB power amplifier is employed to realize a wideband 14-15.5 dBm output power (Fig. 6.4). The broadband output power is realized using a combination of R-feedback, transistor stacking, and a low-loss asymmetric T-coil network. The T-coil network (equivalent to a transformer) is designed with negative coupling and transforms the PA R_{opt} impedance to 50 Ω. A cascode driver with a 2 V supply is used to drive the main PA stage. The wideband interstage matching is achieved using a tertiary-coil network with capacitive and magnatic couplings for a broadband matching. The main PA stage operates at 3 V separate voltage supply to achieve the required output power. The PA has a simulated 3-dB bandwidth of 17-52 GHz with a peak gain of 24 dB and an output P_{1dB} of 11-14.8 dBm at 17-51 GHz. The PA and Tx channel design is similar to the one presented in chapter 3 but with improved bandwidth to operate up to 54.5 GHz. In particular, the interstage matching between the Tx blocks is improved to boost the operational bandwidth to 54-55 GHz instead of 51-52 GHz in Chapter 3. Also, the Tx channel is co-optimized with the Tx/Rx switches for best performance.

The Tx/Rx single-pole double-throw (SPDT) switches are implemented using a series-shunt switch architecture. The shunt HBTs are operated in reverse saturation mode by connecting the emitter to the RF path and collector to the ground. This configuration enhances the switch

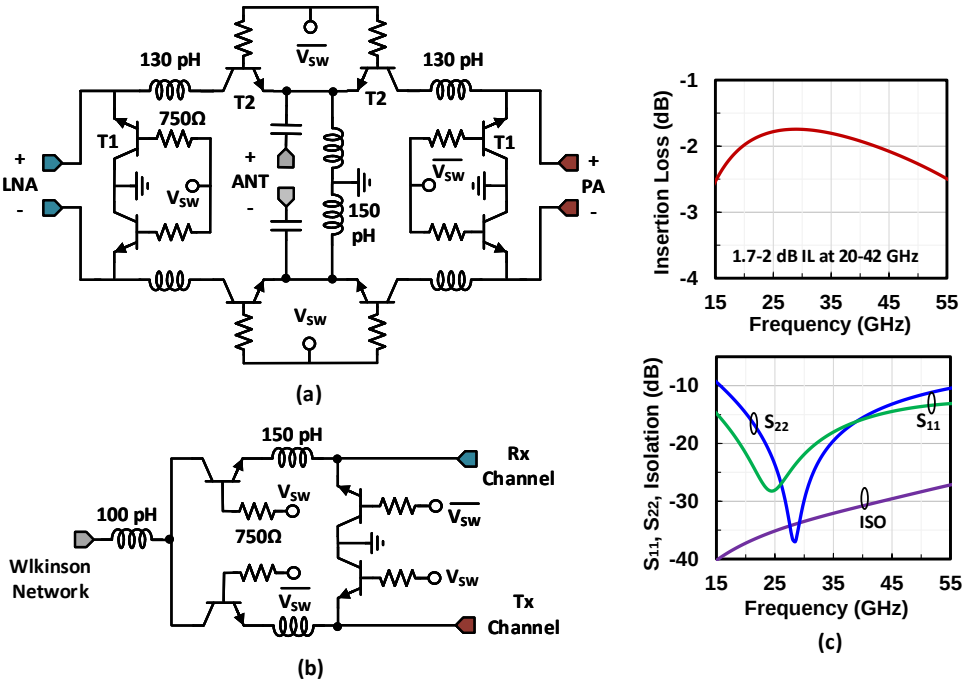


Figure 6.5. Wideband series-shunt Tx/Rx SPDT (a) differential switch and (b) single-ended switch. (c) Simulated insertion loss, return loss and isolation for the differential Tx/Rx switch.

RF performance due to physical isolation of the emitter from the conductive bulk silicon [84]. The Tx and Rx channels are connected to the antenna port using the differential SPDT switch presented in Fig. 6.5 (a). Series and shunt inductors at the switch ports are added to tune the devices parasitic capacitance and achieve wideband operation at 15-52 GHz. The simulated switch insertion loss is 1.7-2 dB at 20-42 GHz and the ports are well matched with a return loss <-10 dB at 15-55 GHz [Fig. 6.5 (c)]. The switch has a simulated input P_{1dB} of 17.3-18.4 dBm and with a port isolation > 30 dB. A single-ended SPDT switch is used to connect the Tx and Rx channels to the Wilkinson network [Fig. 6.5 (b)]. It has a similar performance to the differential switch with an insertion loss of 1.55-2.2 dB and a wideband match at 10-50 GHz.

6.3.2 4×1 Beamformer Measurements

An evaluation PCB is used to measure the Tx/Rx beamformer chip packaged with wafer-level chip-scale bumps at 380 μm pitch (Fig. 6.6). A Keysight 4-port PNA-X N5247A is

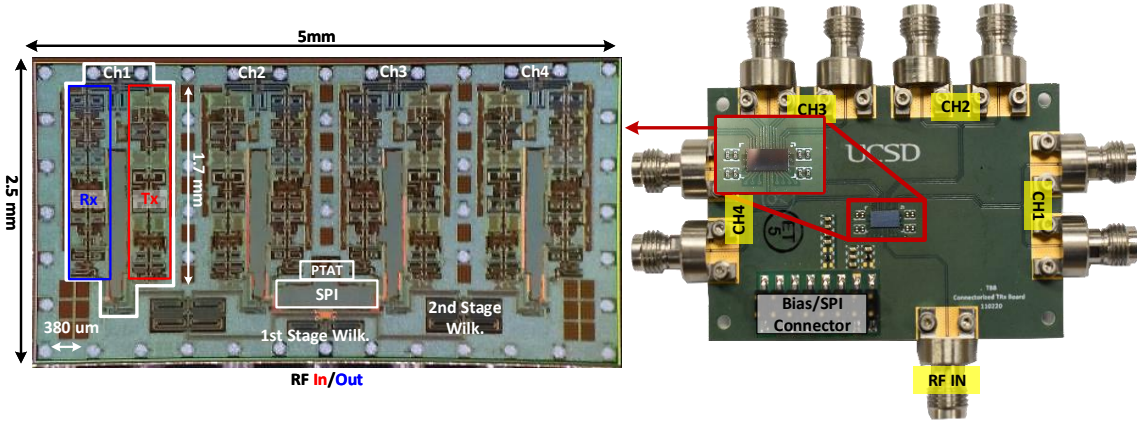


Figure 6.6. Packaged 4×1 Tx/Rx wideband beamformer chip on a connectorized evaluation PCB.

used with the input and output PCB transmission lines de-embedded from measurements. The measured S-parameters for the Rx and Tx modes are presented in Fig 6.7. The gain is defined as the measured S_{21} between the common port and a single antenna port including the Wilkinson network ohmic losses.

In the Rx mode operation, a peak electronic gain of 18-20 dB is measured with a bandwidth of 17-49 GHz and wideband input and output match (S_{11} and S_{22} <-10 at 17-55 GHz). The phase response is shown in Fig. 6.7(a) and is optimized at 30 GHz using an extra trim bit in the phase shifter. An RMS phase error of $< 5.6^{o}$ is obtained at 15-50 GHz by optimizing the phase shifter response at 20, 30, and 40 GHz. A gain control of 17-dB is measured with a gain step of ~1 dB using the VGA gain control

In the Tx mode, the beamformer has a peak gain of 21-24 dB (including the division loss) and with an operational bandwidth of 16.5-55 GHz. The 5-bit resolution phase control is shown in Fig. 6.7(b) for the Tx mode. A gain control of 14-dB is measured using the VGA Tx channel gain control.

Fig. 6.8(a) presents the measured NF for the Tx/Rx beamformer chip in the Rx mode. A midband NF of 5.7-6.5 dB is achieved at 28-42 GHz. The linearity measurements for the

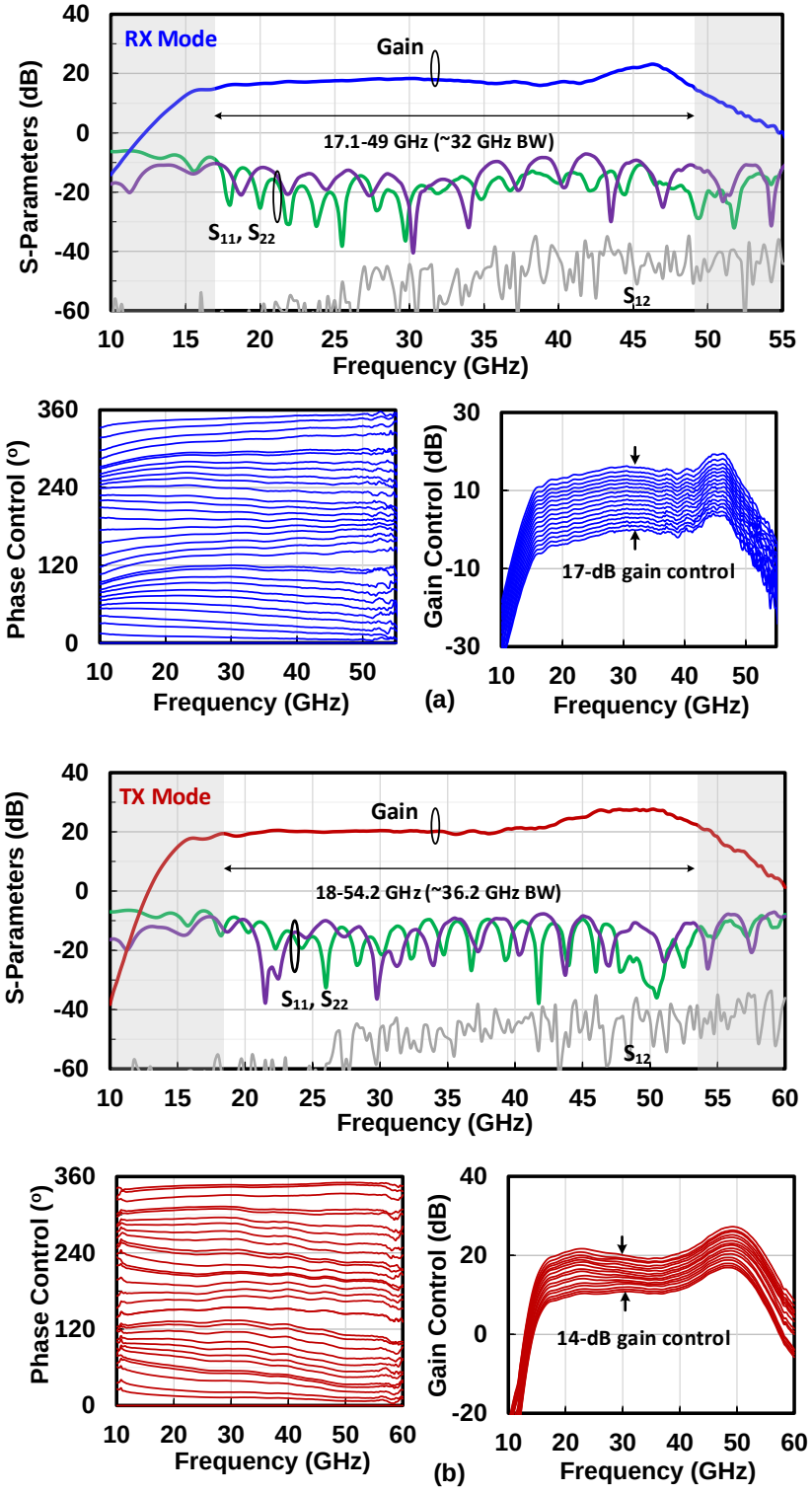


Figure 6.7. Measured S-parameters, phase and gain control in (a) Rx mode and (b) Tx mode.

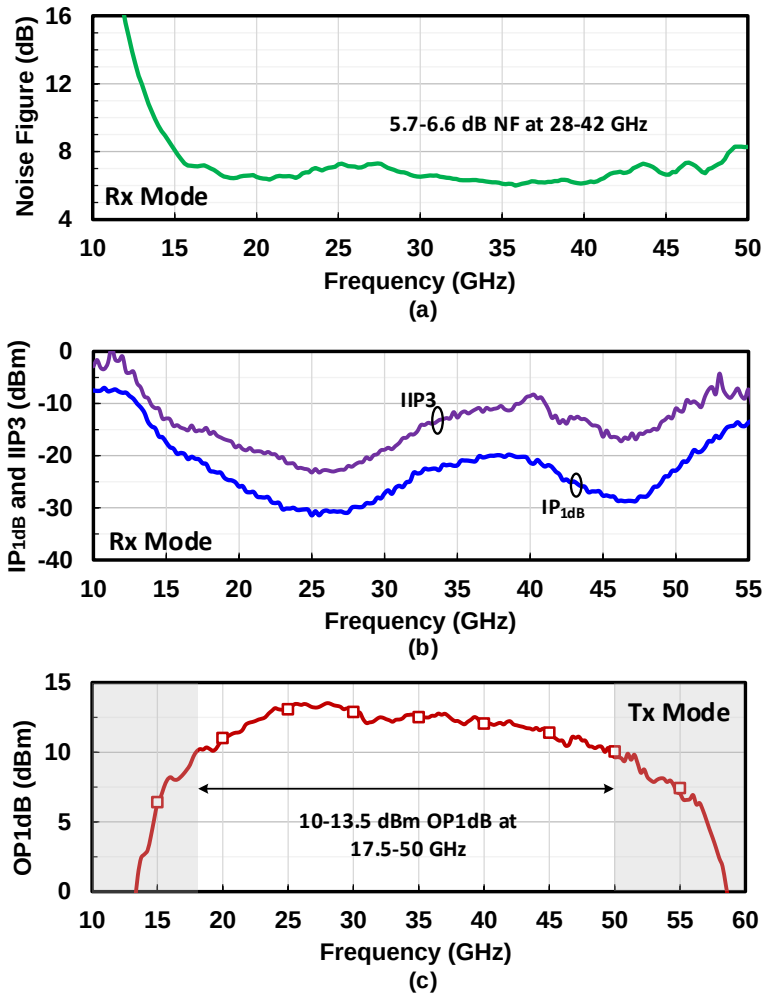


Figure 6.8. (a) Measured noise figure. (b) Input P_{1dB} and IIP3 in the Rx mode. (c) Output P_{1dB} in the Tx mode.

beamformer chip in the Rx mode is presented in Fig 6.8(b). The measured IP_{1dB} and IIP3 are -28.7 to -22 dBm and -20.1 to -12.3 at 28-50 GHz, respectively. In the Tx mode, the chip achieves a wideband output P_{1dB} of 10-13.5 dBm/channel at 17.5-50 GHz. The Tx/Rx beamformer power consumption is 185 mW/ch. in the Rx mode and 265 mW/ch. in the Tx mode (at P1dB).

6.4 System Integration and Measurements

Four 15-52 GHz Tx/Rx beamformer chips are used to build a multi-band 16×1 phased array module on a low-cost 6-layer Megtron-6 PCB (ε_r= 3.24). The ICs are closely placed to

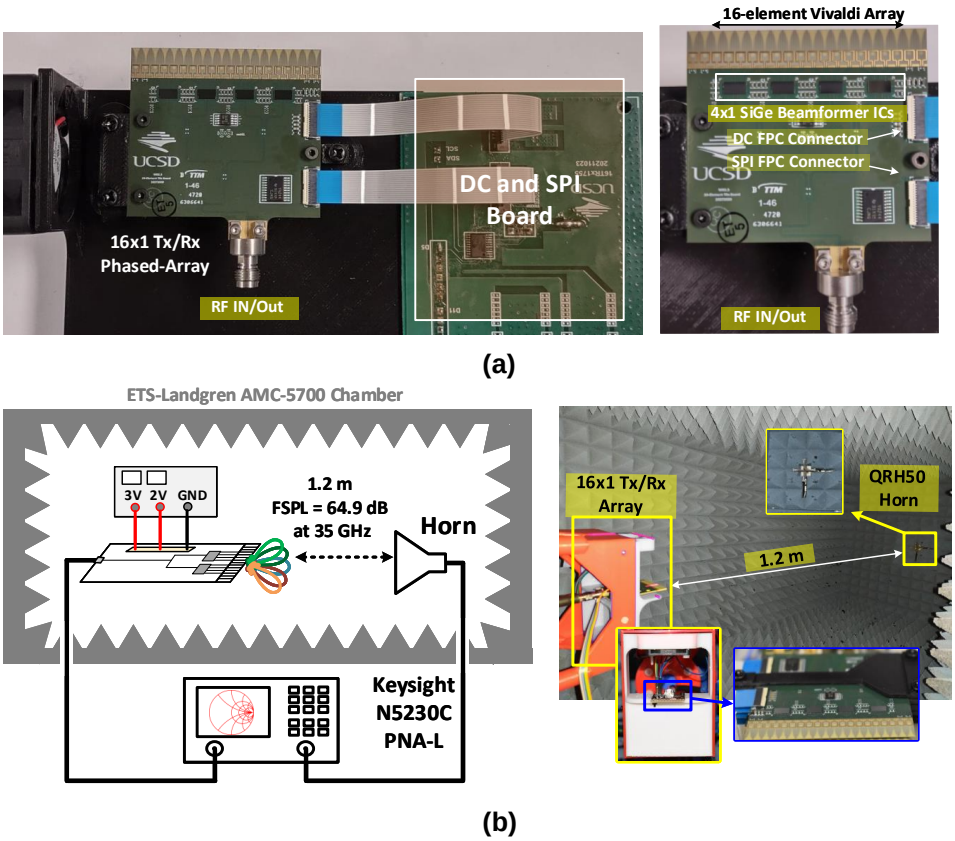


Figure 6.9. (a) Top view of the system showing 16×1 phased-array with 4 Tx/Rx SiGe beamformer chips. (b) Far-field measurement setup.

the differential wideband Vivaldi antenna array minimizing the feedline loss [Fig. 6.9(a)]. The linear array spacing is 2.54 mm selected to mitigate transverse-electric (TE1) parallel plate mode and allow for wideband operation up to 60 GHz. The antenna array can scan up to 60^o with $|S_{11}|$ < -10 dB in E-plane and < -7 dB in the H-plane at 15-55 GHz. The unit cell has a gain of -3.7 to 4.4 dB at 15-55 GHz including the differential feed ohmic loss. The input/output signals are distributed/combined using on PCB 4:1 Wilkinson network realized on M1 and M3 layers. The simulated Wilkinson power divider insertion loss is < 0.6 dB and the isolation is > 20 dB at 16-50 GHz.

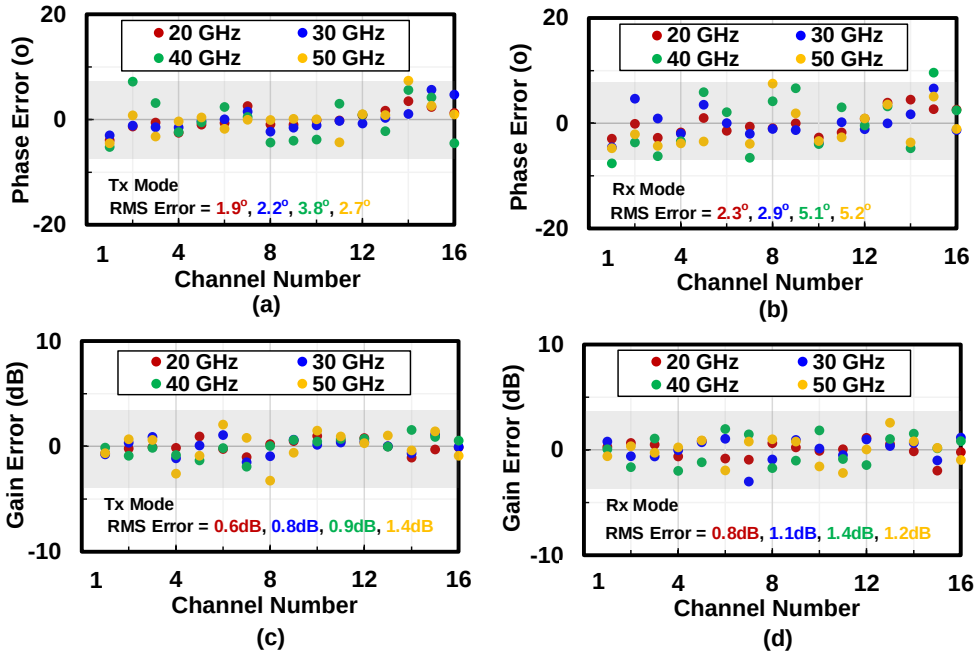


Figure 6.10. Residual phase error (<5.1^o rms) and amplitude error (<1.4 dB rms) at 20, 30, 40, and 50 GHz in Tx and Rx modes.

6.4.1 Array Calibration and Frequency Response

The 16-element Tx/Rx phased array is tested inside an ETS-5700 anechoic chamber at a range of 1.2 m using a vector network analyzer (VNA) [Fig. 6.9(b)]. A wideband horn with a gain of 8.2-12.9 dB at 15-50 GHz is used. To calibrate the 16-element phased array, each channel is turned-on individually and the far-field S_{21} is measured in the nominal gain and phase state for each channel. The gain and phase offsets are calibrated using the phase shifter and VGA control for each channel.

To verify the calibration, the S_{21} for each channel is remeasured and the rms phase and gain errors are calculated after phase calibration. Fig. 6.10 presents the residual phase and gain errors at 20-50 GHz after calibration in the Tx and Rx modes. The rms phase error is <5.1^o and rms amplitude error is <1.4 dB for both Tx and Rx modes at 20-50 GHz.

The far-field S-parameter measurements are conducted at broadside with the setup shown

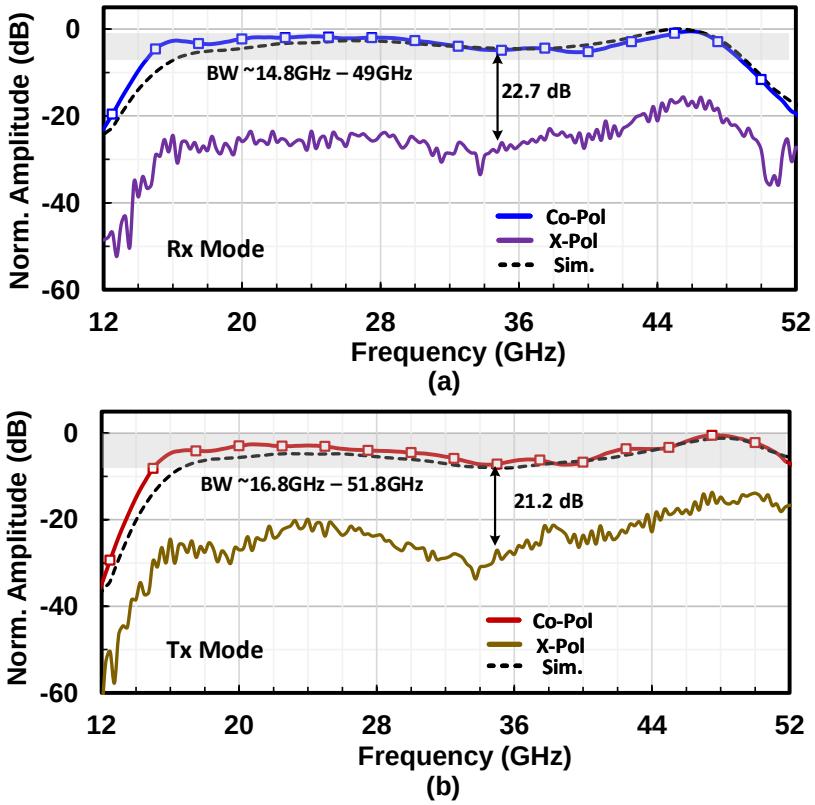


Figure 6.11. Measured co-and cross-polarized frequency response at broadside with uniform illumination for the 16×1 Tx/Rx phased-array.

in Fig. 6.9(b). In the Rx mode:

$$S_{21} = G_{Ant} + G_{Rx} - FSPL + G_{Horn} \tag{6.1}$$

The $FSPL = (\lambda/4\pi R)^2$ and horn gain (G_{Horn}) are removed and the normalized Rx array frequency response ($G_{Ant} + G_{Rx}$) is presented in Fig. 6.11(a). A wideband response at 14.8-49 GHz is measured with +/- 2.5 dB variations and the cross-polarization level is -22 to -18 dB at 20-40 GHz. In the Tx mode:

$$S_{21} = G_{Ant} + G_{Tx} + 10log(N) - FSPL + G_{Horn} \tag{6.2}$$

The normalized Tx mode frequency response ($G_{Ant} + G_{Tx} + 12\ dB$) is presented in Fig. 6.11(b).

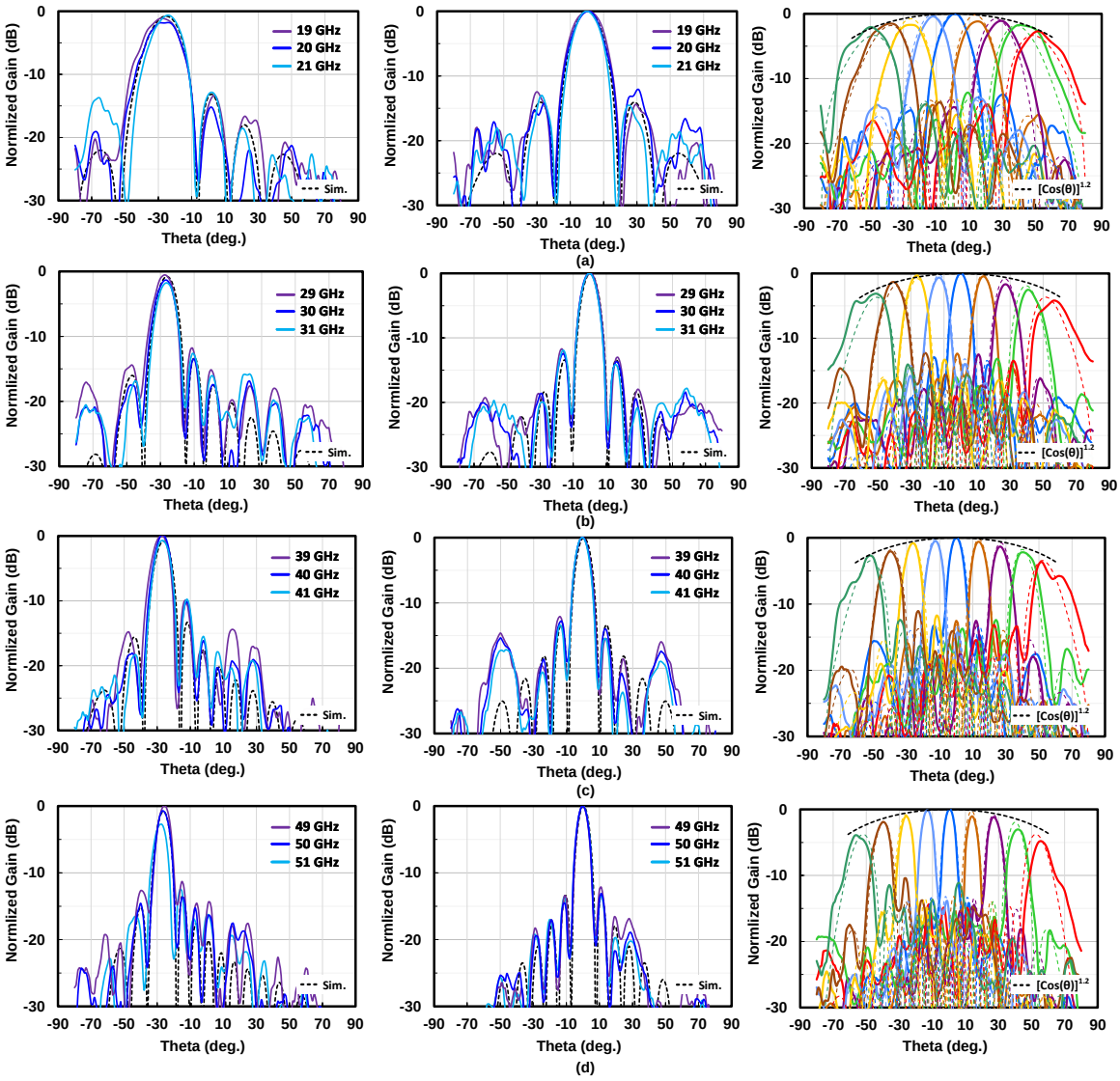


Figure 6.12. Measured azimuth-plane patterns at 0^o, -60^o, and -60^o to 60^o with uniform illumination at (a) 20 GHz, (b) 30 GHz, (c) 40 GHz, and (d) 50 GHz.

The measured Tx mode frequency response shows wideband operation at 17-52 GHz and varies by +/- 3.2 dB.

6.4.2 Pattern Measurements

Fig. 6.12 presents the measured azimuth plane (*E*-plane) patterns in the Tx mode at 20-50 GHz with uniform illumination. The measured patterns demonstrate good agreement with

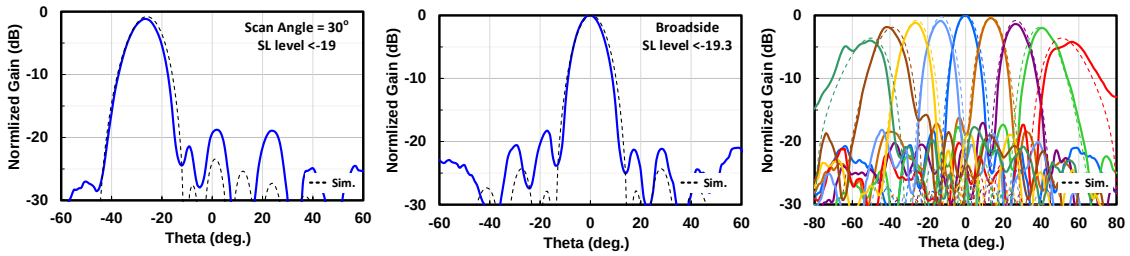


Figure 6.13. Measured azimuth-plane patterns at +/-60^o scan angles with 8-dB raised cosine taper illumination at 35 GHz.

simulated patterns and with 3-dB beamwidths at boresight of 18.5^o, 12.6^o, 9^o, 7.2^o at 20, 30, 40, and 50 GHz, respectively [Fig. 6.12(a)-(d)]. The patterns are also plotted with +/- 1 GHz from the calibration frequency, and the array demonstrates a 3-GHz wideband performance patterns with low sidelobe levels.

An 8-dB raised-cosine taper illumination is applied on the antenna aperture to reduce the sidelobe levels using the VGA gain control. The measured tapered patterns at 35 GHz with scan angles of -60^o to 60^o are shown in Fig. 6.13. At broadside, the 3-dB beamwidths are 14.2^o, 11.5^o, and 9.7^o at 30, 40, 50 GHz, respectively, with slidelobes level <-19 dB. At +/-60^o scan angles, the sidelobes levels are <-17 dB.

The Rx mode pattern measurements show similar performance to the Tx mode and are not presented for brevity.

6.4.3 EIRP and EVM Measurements

The EIRP measurement is conducted for the 16-element phased-array inside the anechoic chamber using the Keysight E8257D signal generator and the Keysight 1913A power meter. An EIRP of 34.3-39 dBm at P_{1dB} operation is measured at 25-50 GHz with uniform illumination and agrees with simulated EIRP at P_{1dB} [Fig. 6.14(a)]. The measured peak EIRP is 36.5-40 dBm with P_{sat} operation at 25-50 GHz [Fig. 6.14(b)]. Also, the EIRP versus scan angle is measured at 30, 35, 40, and 45 GHz with +/- 60^o scan angles and presented in Fig. 6.14(c).

The EVM performance of the 16-element array is first evaluated with 400 MSym/s single-

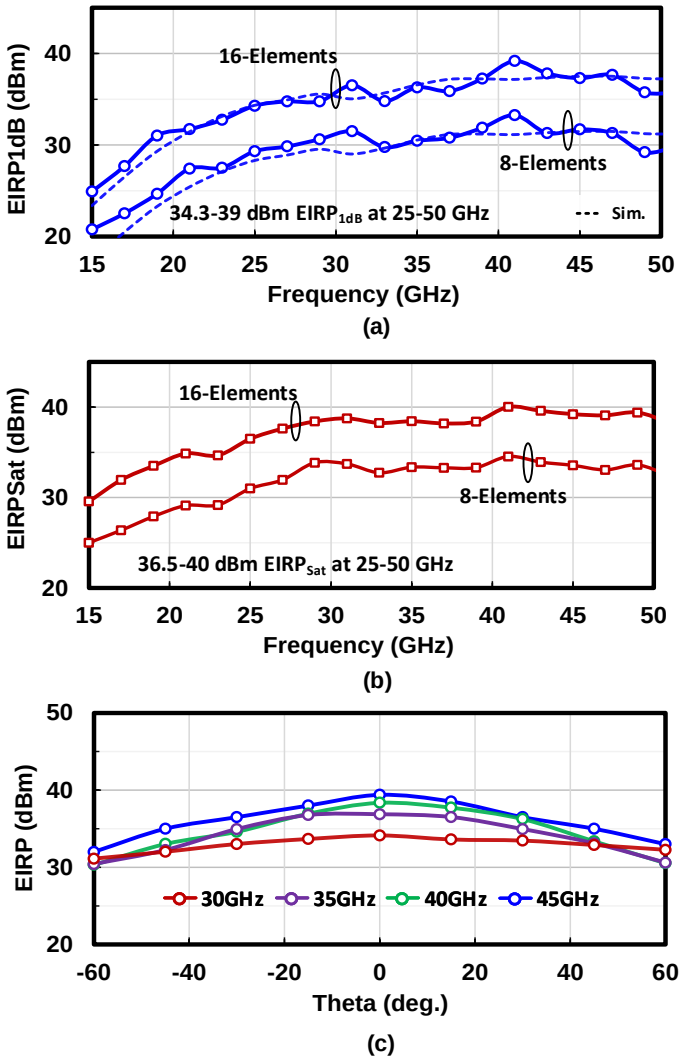


Figure 6.14. Measured EIRP versus frequency of the 16-element phased-array at broadside and uniform illumination with 8 and 16 elements on at (a) P_{1dB} and (b) P_{sat} conditions. (c) Measured EIRP at P_{1dB} with -60^o to 60^o scan angles at 30, 35, 40, and 45 GHz.

carrier 64-QAM waveform filtered with a root-raised cosine pulse shaping filter with a roll-off factor α= 0.35 and has a PAPR of 7.7 dB. This measurement is conducted for multiple-bands (25, 29, 38 and 42 GHz) at broadside and with uniform illumination. The measurement setup, measured spectrum, constellation, and EVM values are presented in Fig. 6.15. The EVM versus EIRP level is also measured to assess the array performance at different backoff levels and with 200 MHz and 800 MHz 64QAM waveforms (Fig. 6.16). All reported EVM values are rms

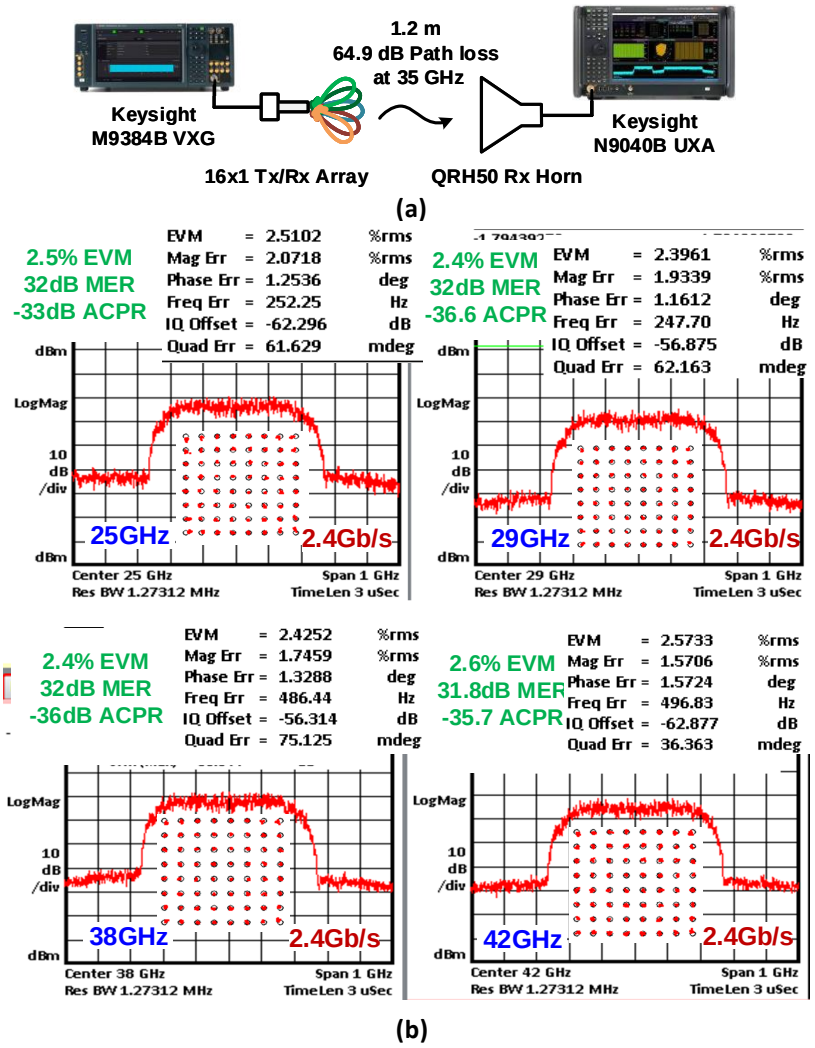


Figure 6.15. (a) 16×1-element Tx/Rx array EVM measurement setup. (b) Measured spectrum and constellation at 25, 29, 38, and 42 GHz center frequency and 38-39 dBm EIRP with single-carrier 400 MHz 64-QAM waveform (2.4 Gb/s).

values referenced to the constellation peak. An EVM value <5% with an EIRP of 30.5-34 dBm is achieved at 25-42 GHz.

5G NR waveforms with 400-MHz channel bandwidth in QPSK, 16-QAM, 64-QAM, and 256-QAM are used to evaluate the array performance. The measured constellations and EVMs at 25, 28, 38, and 42 GHz are summarized in Fig. 6.17. Communication links with up to 256-QAM modulation are established with EVM levels <2.98% and 24.5-26.7 dBm EIRP at 25-42 GHz demonstrating state-of-the art multi-band performance.

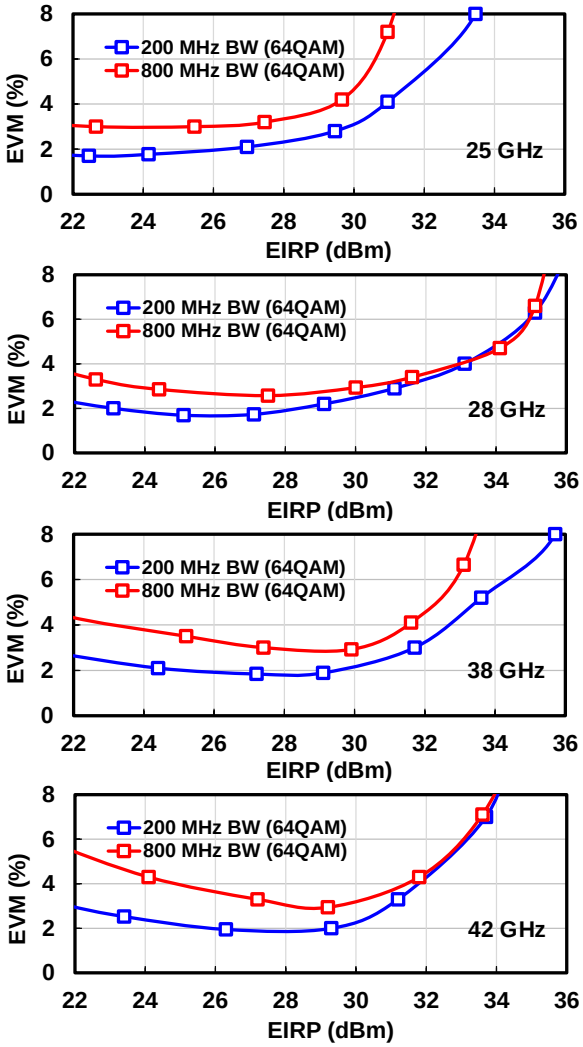


Figure 6.16. (a) Measured EVM versus EIRP with 64-QAM 200 and 800 MHz BW waveforms at (a) 25 GHz, (b) 28 GHz, (c) 38 GHz, and (d) 42 GHz.

6.5 Conclusion

This chapter presented a 16-element Tx/Rx phased-array built using wideband 4×1 Tx/Rx beamformer chips. The SiGe chip demonstrated a 16-52 GHz performance with a NF of 5.7-6.5 dB at 28-42 GHz in the Rx mode. In the Tx mode, the chip achieves a 10-13.5 dBm output P_{1dB} at 17-50 GHz. The 16-element phased-array achieves an EIRP of 36.5-40 dBm at 25-50 GHz with a multiband +/-60^o beam steering capabilities. 5G-NR standard compliant packets at 1.2 m link distance and up to 256-QAM are supported with 400-MHz channel bandwidth and

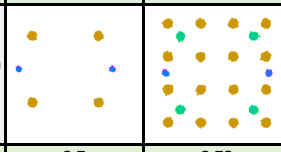
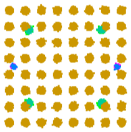
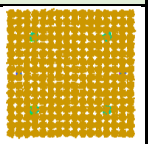
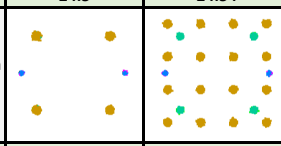
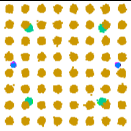
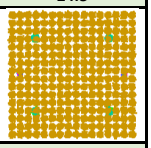
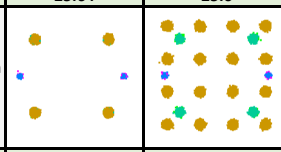
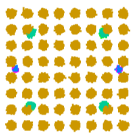
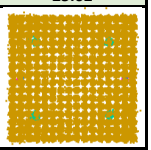
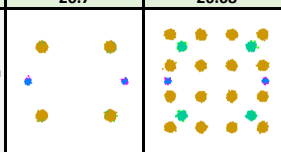
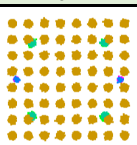
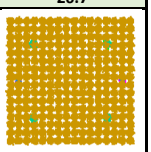
Modulation	QPSK	16-QAM	64-QAM	256-QAM
BW (MHz)	400	400	400	400
Constellation (25 GHz)				
EVM (%rms)	2.7	2.78	2.85	2.93
EIRP (dBm)	24.5	24.54	24.59	24.5
Constellation (28 GHz)				
EVM (%)	2.6	2.67	2.75	2.81
EIRP (dBm)	25.64	25.6	25.7	25.62
Constellation (38 GHz)				
EVM (%)	2.67	2.73	2.8	2.87
EIRP (dBm)	26.7	26.68	26.72	26.7
Constellation (42 GHz)				
EVM (%)	2.74	2.83	2.89	2.98
EIRP (dBm)	26.6	26.63	26.68	26.5

Figure 6.17. Measured 1.2 m OTA constellation and EVM performance using 16-element Tx/Rx phased array.

<2.98% EVM at all 5G FR2 bands.

Acknowledgment

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Chapter 6, in part, will be submitted for publication of the material as it may appear in: A. Alhamed and G. M. Rebeiz, "15-52 GHz Multi-band Tx/Rx Beamformer IC and 16×1 Linear Phased-Array for Wideband Multi-Gb/s 64-QAM Links," *IEEE Transactions on Microwave Theory and Techniques*, in preparation for submission. The dissertation author is the primary investigator and author of this paper.

Chapter 7

Conclusion

This thesis presented 17-55 GHz Tx, Rx and Tx/Rx beamformer chips and phased-array systems for multi Gb/s 5G communication links. A 4×1 Rx beamformer chip with state-of-the-art performance is presented. An 8-element 15-57 GHz multi-band phased-array receive module is built using two 4×1 beamformers on a low-cost PCB. The scalable test module demonstrated an ultra-wideband performance with multi-band beam scanning capabilities. A single-carrier mode data rate of 6 Gb/s in 64-QAM modulation is demonstrated using the 8-element phased array module at 1.2 m distance. 5G NR standard compliant packets of up to 256-QAM are supported with 400-MHz channel bandwidth and <2.76% EVM at all 5G FR2 bands.

An ultra-wideband and high output power 4-channel SiGe beamformer Tx chip is presented. An 8-element 16-52 GHz multi-band phased-array module is built using two 4×1 beamformers on a low-cost PCB. The scalable test module demonstrated an ultra-wideband performance with multi-band beam scanning capabilities. A single-carrier mode data rate of 2.4 Gb/s in 64-QAM modulation is demonstrated using the 8-element phased array. 5G NR standard compliant packets of up to 256-QAM are supported with 400-MHz channel bandwidth and < 2.98% EVM at all 5G FR2 bands. Future work will concentrate on extending this design to a dual-polarized, dual-beam array for 5G FR2 2×2 MIMO systems.

The build of 64-element 16-52 GHz Tx and Rx multi-band phased-arrays based on stacked linear Vivaldi arrays is presented in this thesis. The linear arrays are built using 4×1

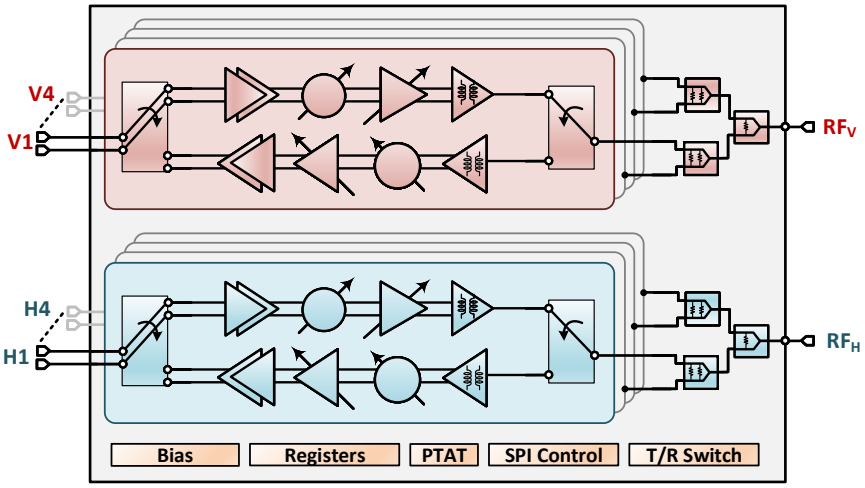

Figure 7.1. 2×4 Tx/Rx dual-beam quad beamformer chip.

beamformer chips on a low-cost PCB. The scalable array demonstrated an ultra-wideband performance with multi-band beam steering capabilities. 5G NR standard compliant packets at 1.2 m link distance and up to 256-QAM are supported with 400-MHz channel bandwidth and <2.98% EVM at all 5G FR2 bands.

A 16-element Tx/Rx phased-array module is built using wideband 4×1 Tx/Rx beamformer chips. The Tx/Rx SiGe chip demonstrated a 16-52 GHz performance with a NF of 5.7-6.5 dB at 28-42 GHz in the Rx mode. In the Tx mode, the chip achieves a 10-13.5 dBm output P_{1dB} at 17-50 GHz. The 16-element Tx/Rx phased-array achieves an EIRP of 36.5-40 dBm at 25-50 GHz with a multiband +/-60^o beam steering capabilities and a 4.8 Gb/s 64QAM links.

7.1 Future Work

The phased arrays demonstrated in this work are based on 4×1 beamformer chips combined with linear antenna array and Wilkinson networks integrated on low-cost PCBs. A wideband transceiver chip can be designed and incorporated in the driver/combiner PCB as well as frequency synthesizer block to demonstrate a complete transceiver system.

A hybrid phased-array can also be built using the stacked linear phased array modules.

The output of each PCB can be individually down/up converted to/from the digital domain enabling analog beamforming in one plane and digital beamforming in the other plane with multiple MIMO streams.

A large-scale phased-arrays (with 256-element) based on dual-polarized/dual-beam next generation chips can be built to demonstrate polarization-based MIMO links at 300-500 m link distance (Fig. 7.1). The link capacity can be boosted using the dual-polarized, dual-beam MIMO system which can be also used to simultaneously operate at two different bands.

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