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Advanced Microfabrication Technologies for Wearable Solar Energy Harvesting and Electrophysiology Monitoring Devices

A dissertation submitted in partial satisfaction of

the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

Yun Goo Ro

Committee in charge:

Professor Shadi A. Dayeh, Chair
Professor David P. Fenning
Professor Darren Lipomi
Professor Charles W. Tu
Professor Paul K. Yu

2020

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The Dissertation of Yun Goo Ro is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2020

DEDICATION

To my beloved parents and sister

EPIGRAPH

Where there is a will, there is a way.

If there is a chance in a million that you can do something, anything,

to keep what you want from ending, do it.

–Pauline Kael

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ACKNOWLEDGEMENTS

Ph. D. study was a long and tough journey which I would not have completed without enormous help from people around me. I would like to take this opportunity to thank all of them.

First, I would like to express the deepest appreciation to my advisor Prof. Shadi A. Dayeh for his warm guidance. His brilliant ideas inspired me every day and his ambitious and positive attitude towards research kept me moving forward. Thanks to his support, encouragement, and patient guidance, I was able to grow as a scientific researcher. Not only he provided fruitful advices but also, he is a great friend who sincerely cares about us. Among many memories with him, I will not forget the moment when he massaged my foot with his bare hands when I sprained my ankle.

In addition to my advisor, I would also like to extend my gratitude to the members of my thesis committee, Prof. Paul K. Yu, Prof. Charles W. Tu, Prof. David P. Fenning and Prof. Darren Lipomi for their guidance and advice. Special thanks should be given to Prof. S. S. Lau and Prof. Eric Halgren for their insightful suggestions.

I am very fortunate to have brilliant and nice lab mates in Integrated Electronics and Biointerfaces Laboratory (IEBL). I spent most of the time in San Diego with Dr. Atsunori Tanaka. Precious times we spent together surfing, watching baseball games at Petco Park, traveling, etc. will be unforgettable. Dr. Renjie Chen was always kindly willing to help me and I learned a lot from him when I first started my research in IEBL. He often encouraged me with his warm words when I was having a hard time. I got lots of help from my 5-year roommate Sang Heon Lee who is an expert in micro-fabrication, computer, and motorcycle. I will never forget his favor of taking me to the ER when I broke my collarbone. Dr. Ren Liu and Dr. Mehran Ganji are my good lab mates, colleagues and friends who went through tough times together. Dr. Keundong Lee always instilled me confidence and was willing to help me at no cost. Joyful moments inside and outside

the lab with Dr. Hongseok Oh, Po Chun Chen and Jihwan Lee kept me in positive spirits. I appreciate collaboration with Woojin Choi, Dr. Youngbin Tchoe in the wearable device and the laminar neural probe projects. Without them, both projects would not have been possible. I also had great pleasure of working with other IEBL members, Lorraine Hossain, Ritwik Vatsyayan, Andrew Bourhis, Samantha Russman, Tianhai Wu, not to mention the past IEBL members, Dr. Yoontae Hwang, Dr. Minh B Nguyen, Dr. Namseok Park, Dr. Siarhei Vishniakou, Dr. Supanee Sukrittanon, Farid Azzazy, Cory Heath, Michael Mullins-Jensen, Timothy Searcy, Dr. Joonseop Sim, Ahmed Taha El-Thakeb Youssef, Oscar Guerrero, Martin Magno, Adrian Luna, Valeria Gonzalez, Cheryle Wills, Prof. Chennupati Jagadish, Prof. Gyu-Chul Yi and late Dr. Phil Mages. Thank you all for being kind and friendly. I am proud to be an IEBL member and I see the bright future of this group.

I am also very grateful to my friends in UC San Diego, Dr. Lujian Yan, Dr. Weichuan Yao, Dr. Iftikhar Ahmed Niaz, Dr. Kangwei Wang, Dr. Alireza Kargar, Dr. Serdar Yavuz, Dr. Rui La, Dr. Chulmin Choi, Yue Gu, NamHeon Kim, Bo-kyeom Seo and my two lifetime friends in other part of U.S., Dr. Jaejun Lee and Kunho Baik, for their friendship.

Most of the fabrication part of this dissertation was done in Nano3 Cleanroom at Calit2. I very much appreciate Nano3 staff members, Dr. Bernd Fruhberger, Larry Grissom, Sean Parks, Dr. Xuekun Lu, Dr. John Tamelier, Patrick Driscoll, Hal Romans, Ahdam Ali and Ryan Anderson for their valuable technical supports and particularly for introducing a maskless aligner which profoundly advanced my research.

I have greatly benefited from many others, Dr. Jinkyoung Yoo in Los Alamos National Laboratory with his great help to the solar cell project, Dr. Daniel R. Cleary and Dr. Joel R. Martin with their help and advices in in vivo experiments, Dr. Angelique C. Paulk, Dr. Jimmy Yang and

Prof. Sydney S. Cash in Massachusetts General Hospital with collaboration work with our neural probe devices.

I would also like to acknowledge Prof. Takashi Fukui at Hokkaido University and Prof. Young Joon Hong at Sejong University for supporting me to achieve an opportunity to study in U.S.

Last but not the least, words are powerless to express my gratitude to my parents Dr. Man Tack Ro, Hae Suk Kim and my sister Joo Young Ro. Without their support and love, this dissertation would not have been possible. They prayed for me every single day and I consider myself to be very blessed. Thank you for being there for me.

The list is by no means exhaustive and I would like to acknowledge all other people who have helped me but are not mentioned above.

Chapter 2, in full, is a reprint of the material as it appears in *Advanced Energy Materials* 2018. Y. G. Ro, R. Chen, R. Liu, N. Li, T. Williamson, J. Yoo, S. Sim, R. P. Prasankumar, S. A. Dayeh. The dissertation author was the primary investigator and author of this paper.

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PUBLICATIONS

1. **Y. G. Ro**, R. Chen, R. Liu, N. Li, T. Williamson, J. Yoo, S. Sim, R. P. Prasankumar, S. A. Dayeh, "Surface Passivation and Carrier Collection in {110}, {100} and Circular Si Microwire Solar Cells", *Advanced Energy Materials* **2018**, 1802154.

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1. The 15th International Conference on Advanced Materials (IUMRS-ICAM 2017), “Mechanistic Studies for the Development of Thin Si Microwire Solar Cells for Wearable Electronics”, **Sep. 2017**, Kyoto, Japan.

2. 43rd Conference on the Physics and Chemistry of Surfaces and Interfaces (PCSI-43), “Mechanistic Studies for the Development of Thin Si Microwire Solar Cells for Wearable Electronics”, **Jan. 2016**, Palm Springs, CA.

3. 2015 Materials Research Society Fall Meeting (2015 MRS), “Flexible Nanowire Solar Cells for Wearable Electronics”, **Nov. 2015**, Boston, MA.

4. 2015 International Conference on Solid State Devices and Materials (SSDM 2015), “Surface Passivation Studies on Vertical Junction Silicon Microwire Solar Cells”, **Sep. 2015**, Sapporo, Japan.

5. 57th Electronics Materials Conference (EMC 2015), “Monolithic Integration of Self Powered Wearable Electronics”, **Jun. 2015**, Columbus, OH.

6. 57th Electronics Materials Conference (EMC 2015), “Surface Passivation Studies on Vertical Junction Silicon Microwire Solar Cells”, **Jun. 2015**, Columbus, OH.

7. TechConnect World Innovation Conference & Expo (TechConnect 2015), “Monolithic Integration of Self Powered Wearable Electronics”, **Jun. 2015**, Washington, D.C.

Poster Presentations

1. Research Expo at UCSD, "Passivation and collection in {100}, {110}, and cylindrical microwire solar cells", **Apr. 2018**, San Diego, CA.

2. UCSD-NSYSU Bilateral Symposium, “Microwire Solar Cells on Flex for Powering Wearable Devices”, **Nov. 2017**, San Diego, CA.

3. Research Expo at UCSD, “Surface Passivation Studies on Vertical Junction Silicon Microwire Solar Cells”, **Apr. 2015**, San Diego, CA.

ABSTRACT OF THE DISSERTATION

Advanced Microfabrication Technologies for Wearable Solar Energy Harvesting and Electrophysiology Monitoring Devices

by

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Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems)

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Internet of Things (IoT) is becoming pervasive in our daily lives. Wearable technologies will expand the connectivity of IoT and will increase the interaction between technology and human body. Micro Electro-Mechanical Systems (MEMS) microfabrication techniques that involve bulk Si micromachining and thin film processing have allowed us to develop electronic

systems that are based on Si and other advanced materials that are flexible, wearable, and implantable. Wearable and implantable electronics equipped with sensors enable us to perform real-time health monitoring from above and below the skin, respectively, and can replace conventional bulky electrophysiological monitoring devices and systems.

Research efforts in wearables and implantables have intensified in the last decade tackling several aspects of the sensor technology, embedded signal processing and conditioning, energy harvesting, connectorization, functionality, longevity and reliability. However, there are still technical challenges that impose restrictions for their widespread adoption. On top of these challenges is the power source for the wearable or implantable device. Energy harvesting is expected to replace conventional battery systems that power wearables and implantables. In this dissertation, we focus on solar energy as an energy source for self-powered electronics.

In Chapter 1, the motivation of the dissertation together with a brief survey of state of the art in flexible and wearable electronics with energy harvesting system and implantable medical devices are discussed.

In Chapter 2, we disclose our parametric studies on solar cells with different microwire surface and array morphologies to understand the effect of surface passivation, surface crystal orientation on surface recombination and carrier collection on SiMW solar cells with radial p-n junctions as well as their emitter series resistances with an overall goal of maximizing their power conversion efficiencies.

In Chapter 3, we present an approach for self-powered wearable electronics by means of the monolithic integration of SiMW solar cells with Si MOSFETs on a Silicon on Insulator (SOI) wafer that is subsequently transferred to flexible substrates. The fabrication details and its application to a voltage-controlled oscillator and electrophysiological monitoring are discussed.

In Chapter 4, we discuss the details of the novel fabrication processes for the development of a stylet guided depth/laminar probe and of a surface electrocorticography (ECoG) grid that is fabricated with bio-compatible polymers (Polyimide and Parylene C) including their electrochemical characterization and their use *in vivo* for electrophysiological recordings in rats.

Chapter 1

Introduction

1.1 Motivation

Advances of miniaturization of flexible electronics by microelectromechanical systems (MEMS) microfabrication techniques have brought realization of wearable devices integrated with multiplexed sensors. With rapid advances of the Internet of Things (IoT) and rise of 5G technology, a new era where flexible and wearable electronics are indispensable in our daily life is emerging. IoT integrated with wireless sensors network (WSN) will facilitate ubiquitous connectivity and will bring better life quality in various perspectives. On top of that, IoT application in healthcare has gained profound interests.

Flexible and wearable devices equipped with sensors, can make a conformal contact with epidermal interface or with cortex to detect human physiological status and provide instant feedback. Different type of biomedical signals can be recorded with electronic devices linked with the nervous system through neural interface, non-invasively, when the devices are above the skin (electromyogram (EMG), electroencephalogram (EEG) and electrocardiogram (ECG)), and when they are implanted below the skin and in some cases the skull as in the case of electrocorticography (ECoG) and stereoelectroencephalography (sEEG). For people who are suffering from neurological disorders, real-time healthcare monitoring is critical and wearable technologies enable more accessible and continuous monitoring of human health. Not only wearable and implantable medical devices allow us to do real-time monitoring but also, they are capable of long-

term monitoring to deal with chronic disorders. And if the medical devices are integrated with wireless modules, the collected data can be wirelessly transmitted to the patient to provide feedback.[1] Wearable and implantable medical devices also provides us information to identify electrophysiological biomarkers of brain disorders such as epilepsy,[2] Parkinson's disease[3] and Alzheimer,[4] which in addition to diagnosis are capable of curing and potentially preventing these disorders and their debilitating effects. With ability to detect physiological markers in real time, future physiological monitoring systems will heavily rely on wearable and implantable electronics.

Despite abovementioned potential of wearable electronics, there are still technical challenges that need to be overcome before cultivating the advantages of wearable electronics and their widespread use. One of the biggest challenges is the power source. The increasing demand for advanced wearable system on a chip (SoC) functionalities requires complex designs and processing algorithms, which in turn demand more power. Primary technical demands of wearable devices are primarily associated with their ultra-low power consumption[5] and the need for a compact and minimally invasive or minimally disruptive size. Wearables and implantables have been traditionally powered with batteries. However, Conventional batteries are bulky, rigid and require external charging and periodic replacement and are therefore not suitable for wearable and implantable applications. Energy harvesting, which scavenges and converts ambient energy to electrical energy, can prolong battery lifetime and moreover enables "battery-less" systems while simultaneously maintaining "always-on, always-sensing" systems. Thus, energy harvesting has gained much attention as an alternative power source of external battery to provide autonomous power supply with green and renewable energy.

1.2 Background of Self-powered Wearable Electronics

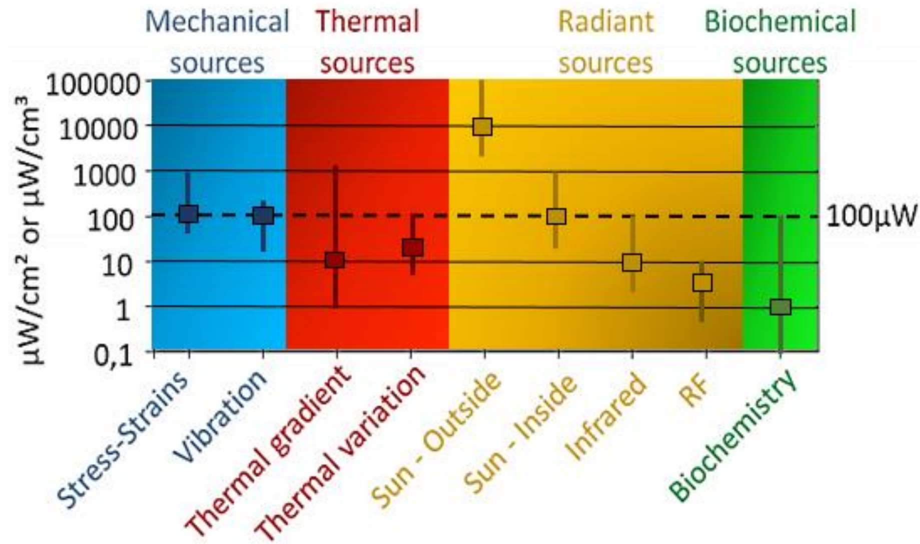

Figure 1.1 Power densities of common ambient sources. Reprinted with permission from Ref. 6. Copyright 2012, S. Boisseau, G. Despesse and B. Ahmed Seddik. Licensee IntechOpen.

Self-powered electronics by energy harvesting system can be categorized by the type of ambient energy sources such as mechanical energy, thermal energy, radiative energy, and biological energy. There are two factors that determine the decision of deploying energy harvesting technique within a particular technology. The first factor is the output power density. As shown in **Figure 1.1**, each energy source is associated with different power density making it best fit for a certain category of applications.[6] The second factor is the local environment of the target application. For example, indoor activities, where many of the ambient energy sources may not be present, naturally require different harvesting and design considerations than outdoor activities.

One of the most widely researched energy harvesting systems is sensors with nanogenerators which transduce the mechanical or thermal energy obtained from the human body or environment into the electrical energy. Piezoelectric nanogenerators (PENGs) make use of piezoelectric materials such as ZnO or $BaTiO_3$ to induce an electric potential resulting from the polarization of ions in the crystal due to strain.[7] Triboelectric nanogenerators (TENGs) use the

conjunction of triboelectrification and electrostatic induction which occur from separating or sliding two materials that have opposite tribo-polarity.[8] Pyroelectric nanogenerators (PyNGs) employ pyroelectricity defined by spontaneous polarization of certain anisotropic solids resulting from fluctuation in temperature.[9] PENGs and TENGs utilize motion energy sources varied from basic movements from daily life to physiological activities and PyNGs harvest energy from human temperature gradient in response to ambient temperature. These nanogenerators paved the way for sensors in diverse range of medical applications such as cardiovascular system,[10-12] respiratory,[13-15] sweat,[16,17] body temperature monitoring[18] and so on. Nevertheless, these nanogenerators count on mechanical and thermal energy of the human body. The amount of energy produced within the human body is relatively low compared to solar energy[19] and for certain applications, it might be appropriate to tap into the solar energy resource. Transducers that operate based on mechanical deformation suffer from degradation in performance over their lifetime, which remains to be a concern for these types of nanogenerators.[20,21]

1.3 Solar Energy Harvesting

Earth annually acquires about four million exajoules (1 EJ = 10^{18} J) of solar energy of which 5×10^4 EJ is known to be easily harvestable.[22] While the outdoor sunlight intensity is 100–1000 W/m^2 and it drops down to lower than 10 W/m^2 under indoor light conditions, solar cells are still capable of harvesting enough energy to power electronic devices including indoors.[23,24] The fundamental challenge of flexible solar energy harvesting systems are underscored by maintaining a high power conversion efficiency (PCE) at end-use in wearables, that is while integrated with other components such as actuators, sensors, transistors, or integrated circuits. Therefore, the two main requirements for flexible solar energy harvesting system are first the choice of an adequate material that is compatible with monolithic integration processes and second the end-use operational PCE at high rate on flexible substrates to increase the light harvesting efficiency.

Organic solar cells are considered as a promising platform for flexible and wearable applications owing to their flexibility, transparency, and light weight.[25] Hsieh et al. presented a Pt strain sensor powered by an organic solar cell that is connected in series on the same flexible substrate.[26] (**Figure 1.2 (a), (b)**) Under 1 and 0.02 sun, a PCE of 1.94% and 0.0091% was obtained respectively by the organic solar cell, providing sufficient power to the Pt strain sensor enabling human physiological signals monitoring under indoor light. Park et al. developed flexible organic electrochemical transistors powered by ultra-thin (3 μm) and flexible organic solar cell for self-powered cardiac sensor application.[27] (**Figure 1.2 (c), (d)**) Despite the fact that their organic solar cell exhibited PCE of 10.49%, superior to that of other flexible organic solar cells, and highest PCE of flexible solar cell reported up-to-date is 15.21%[28] yet it is relatively low compared to that of flexible perovskite (19.51%[29]) or flexible Si solar cells (19%[30]). The low PCE remains to be their major drawback.

Perovskite solar cells can be printed easily with roll-to-roll manufacturing[31] and due to their wide bandgap, perovskite solar cells are adequate candidates for indoor light harvesting applications.[32] Mathews et al. reported radio frequency identification (RFID) based sensors powered by serially-connected perovskite solar cells.[33] Perovskite solar cells fabricated on a glass substrate were assembled with RFID tag on a plastic substrate. Li et al. invented a flexible and wearable solar-powered on-skin physiological monitoring sensor composed of perovskite solar cells, photo-rechargeable lithium-ion capacitor, and graphene-based strain sensors.[34] In both reports, each component was fabricated individually and integrated externally, not monolithically. This arrangement occupies certain volume of the integrated device which affects the flexibility of the total structure and may not be appropriate for a scalable manufacturing solution.

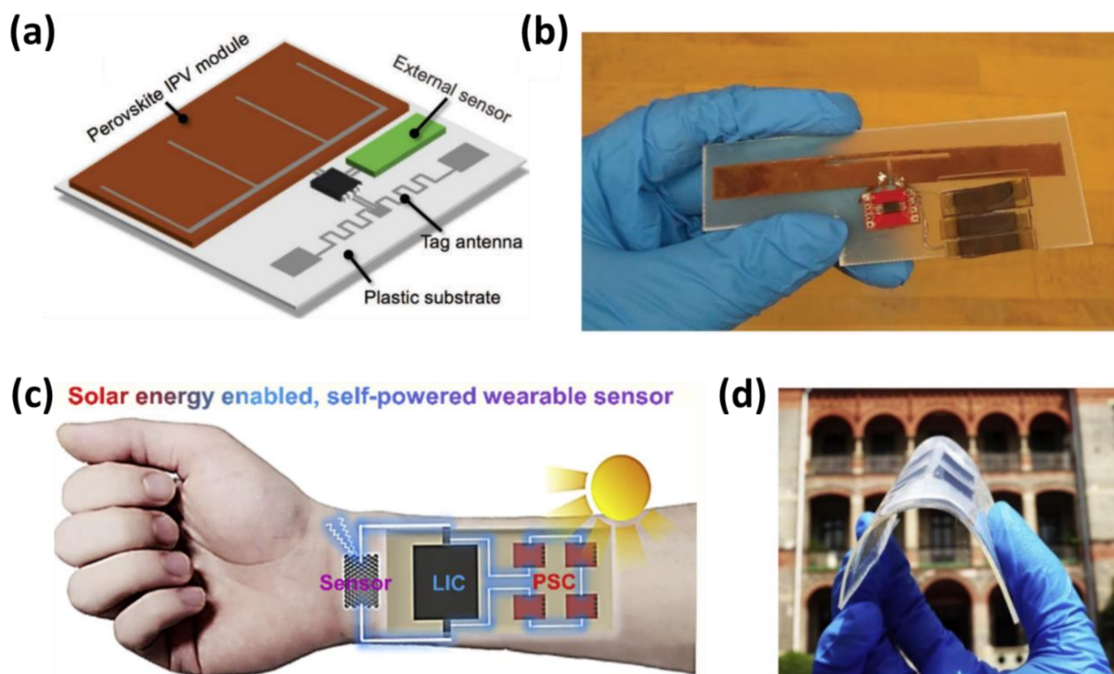

Figure 1.2 (a) A schematic diagram and (b) a photo of RFID temperature sensor powered by perovskite solar cells. Reproduced with permission from Ref. 33. Copyright 2019, John Wiley and Sons. (c) A schematic diagram and (d) a photo of flexible physiological monitoring senor powered by perovskite solar cells driven photo-rechargeable lithium-ion capacitor. Reproduced with permission from Ref. 34. Copyright 2019, Elsevier.

Si solar cells on the other hand possess a substantial potential to be monolithically integrated with sophisticated electronics as Si is the most widely used material for microelectronics. Endeavors of integration of Si solar cells with CMOS have been reported by few research groups using SOI wafers or by the direct deposition of Si solar cells backend on CMOS chips. Bellew et al. demonstrated the side-to-side fabrication process of Si solar cell and NMOS on an SOI wafer.[35] Chen et al. developed ring oscillators powered by solar cells integrated on the same SOI wafer.[36] Amorphous-silicon (a-Si) solar cell integrated with a CMOS chip by depositing passivation layer and a-Si:H n-i-p layer on top of a CMOS chip was attained by Lu et al.[37] However, to the best of our knowledge, monolithic integration of Si solar cell and transistors on a thin (<20 μm) or flexible substrate has not been reported or extensively studied mainly due to fabrication difficulties on thin and flexible substrates and due to the low device performance under mechanical deformation.

Decreasing the thickness of the Si wafer will improve the flexibility but degrades the Si solar cell performance on account of reduced light absorption.[38,39] Thus, maintaining PCE at high efficiency when transferring the device to a flexible substrate is a main obstacle for flexible solar cells. A number of research groups have adopted light trapping effect by introducing micro- or nanostructures to increase optical path length of light resulting in better light absorption while maintaining thin total substrate thickness.[40-43] Despite the effort of enhanced light absorption by light trapping effect, PCE of flexible Si solar cells have not reached 20% which is still far from ray-optics-based theoretical limit as a result of Auger, Shockley-Read-Hall, and surface recombination losses.[44,45]

1.4 Energy Harvesting and Wireless Power Transfer Systems for Electrophysiological Monitoring

Conventional electrophysiology recording systems require bulky and immobile equipment and recording can be performed only in limited spaces, such as clinical laboratories. When integrated with energy harvesting system and wireless transmission techniques, implantable medical devices will face a new paradigm shift with enormous advantages, such as reduced cost for both patients and clinics and readily accessible real-time monitoring.

Pacemaker can be self-powered if it is equipped with an energy harvester that converts vibrations from heartbeats to electrical energy. Hwang et al. investigated a self-powered pacemaker comprising a piezoelectric material (PMN-PT) that can generate 2.7 μJ of energy from each bending motion of the energy harvester, which is larger than the threshold energy to electrically stimulate the living heart of animals (1.1 μJ) (**Figure 1.3 (a)**).[46] Ouyang et al. implanted TENG in the chest of a pig as a pacemaker that can harvest 0.495 μJ from each cardiac motion cycle, which is higher than the pacing threshold energy of pigs and humans.[47]

EEG systems powered by thermo-electric generator and solar cells have been demonstrated by Torfs et al (**Figure 1.3 (b)**).[48] Thermo-electric generator in the form of head-band or head-phone produced 1.5-2.5 mW power where solar cells provided power of 45 mW under direct sunlight and 0.2 mW under indoor light. The harvested energy was stored in a capacitor to provide a stable supply voltage for EEG recording.

Ultrasound and electromagnetic energy exchange paradigms are commonly used for transcutaneous and wireless power transfer methods when energy harvesting is not applicable. Hinchet et al. used vibrating and implantable triboelectric generator to harvest the ultrasound mechanical energy *in vivo* and in liquids (**Figure 1.3 (c)**).[49] Their device at 1 cm under the porcine

tissue generated output power 98.6 μW by ultrasound energy transfer, which is high enough to recharge the batteries of small implants. Chang et al. implanted wireless and battery-less neural probe, powered by inductive coupled RF power, into the surface of a rat brain for ECoG recording (**Figure 1.3 (d)**).[50] A mainboard including RF power receiving coil is connected by wires to the headstage of the neural probe and RF power generated by a function generator is sent into a power amplifier, which is connected to power transmission coils located on the wall of the rat cage.

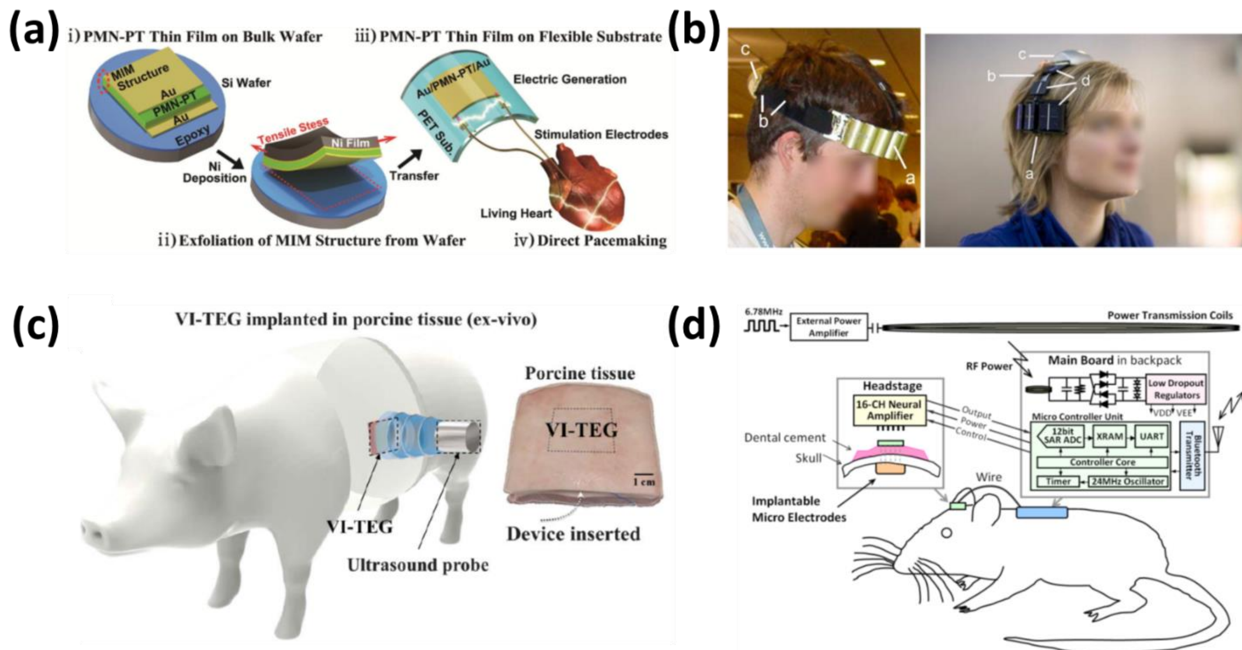

Figure 1.3 (a) Self-powered piezoelectric pacemaker. Reproduced with permission from Ref. 46. Copyright 2014, John Wiley and Sons. (b) EEG systems powered by thermo-electric generator and solar cells. Reproduced with permission from Ref. 48. Copyright 2008, IEEE. (c) Ultrasound energy harvesting by implantable triboelectric generator. Reproduced with permission from Ref. 49. Copyright 2019, The American Association for the Advancement of Science. (d) Electromagnetic power transfer for battery-less ECoG probes. Reproduced with permission from Ref. 50. Open Access.

Implantable solar cells have recently risen as potential energy harvester platforms for implantable medical devices. Lu et al. studied biodegradable Si solar cell integrated with SiO_2 back biofluid barrier, Mo electrodes/interconnections and poly(lactic-co-glycolic acid) (PLGA)

encapsulation layer which can produce 25 μW of power under 2 mm porcine skin and 2 mm fat, under 1 sun illumination.[51] The device is fully dissolved after 27 days under 1× PBS solution at 70 °C and after 4 months of implantation in infrascapular region of a rat, without any inflammatory responses in the surrounding tissues (**Figure 1.4 (a), (b)**). Song et al. implanted serially-connected GaInP/GaAs dual junction solar cells that were transfer-printed on flexible polyimide film and encapsulated with multiple layers of biocompatible polymers, under the skin of a hairless mouse and measured *in vivo* solar cell performance.[52] While the open circuit voltage and the fill factor remained constant, because of the reduced light under the skin, short-circuit current density dropped from 5.9 to 2.6 mA resulting in decrease of PCE from 21.7 % to 10 % after implantation. They showed that their solar cells can provide enough power (647 μW) under the mouse skin to operate a pacemaker and regulate the heart beats under the light, enabling a self-powered pacemaker (**Figure 1.4 (c)-(e)**).

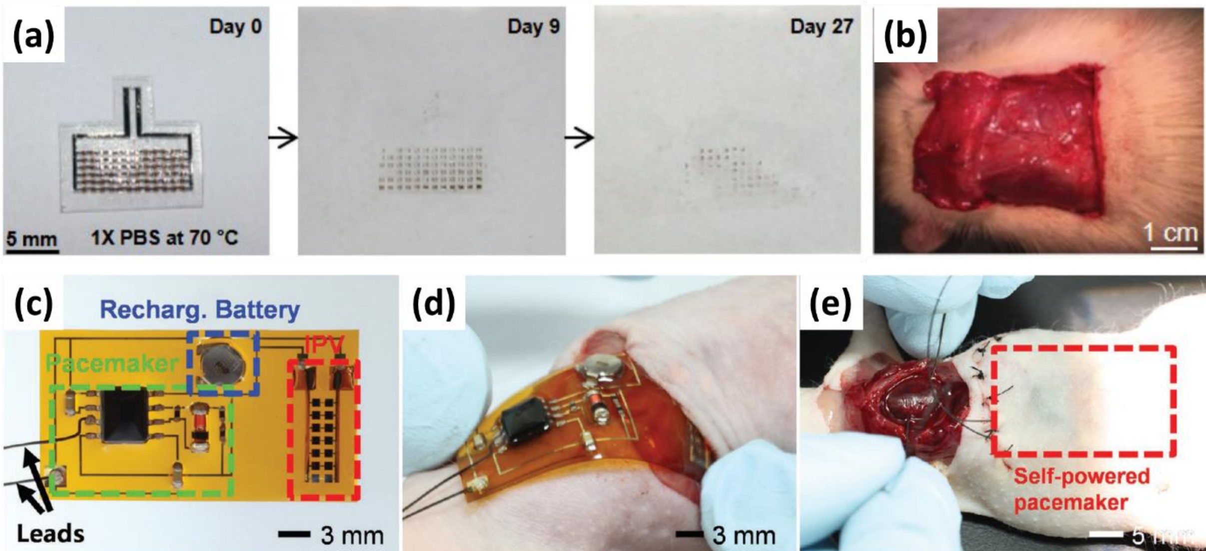

Figure 1.4 (a) Images accelerated dissolution of a bioresorbable Si solar cell array in 1 × PBS solution at 70 °C. (b) Optical image of the infrascapular region with Si solar cell array implanted for 4 months, showing that the device has fully dissolved. Reproduced with permission from Ref. 51. Copyright 2018, John Wiley and Sons. (c) Optical image of self-powered pacemaker integrated with solar cell arrays and a rechargeable battery. (d), (e) Optical images of subdermally implanted self-powered flexible pacemaker. Reproduced with permission from Ref. 52. Copyright 2016, John Wiley and Sons.

1.5 Overview of the Dissertation

The objectives of the work conducted for the preparation of this dissertation encompass understanding and demonstration of two inter-related areas, wearable solar energy harvesting system and electrophysiology monitoring by MEMS microfabrication technologies.

The organization of this dissertation is as follows. In chapter 2, we focus on Si microwire (SiMW) solar cells for flexible solar cell applications. To understand surface recombination which is a major bottleneck of realizing highly efficient micro/nano-structure solar cells and to provide general design principles for optimizing SiMW solar cell performance, parametric studies of the influence of SiMW surface-facet orientation (rectangular with flat-facets, {110}, {100} and circular), with a fixed height of 10 μm, diameter (D = 1.5–9.5 μm), and sidewall spacing (S = 2.5–8.5 μm), and mesh-grid density (1–16 mm^{-2}) on recombination and carrier collection in SiMW solar cells with radial p-n junctions are thoroughly investigated.

In chapter 3, we demonstrate fabrication of SiMW solar cell on an SOI wafer and transferring to a flexible substrate for self-powered wearable electronic application. Monolithic integration process of SiMW solar cell and MOSFETs on an SOI wafer and demonstration of voltage-controlled oscillator are addressed. We found that variation of doping concentration over SOI wafers affects the fabrication uniformity and at the time of writing of this dissertation, the control over the substrate doping concentration of SOI wafers and corresponding device performance remains to be a challenge such that further studies need to be conducted.

Chapter 4 explores flexible and scalable surface/depth neural probes for ECoG and intracortical recordings fabricated by MEMS microfabrication techniques. The fabrication details for the development of hollow structure on bio-compatible polymer substrates (Parylene C and Polyimide) for stylet guided depth probe are reported. A conductive polymer, poly(3,4-

ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS), was implemented on the neural probes to reduce electrochemical impedance in an effort to facilitate high signal-to-noise ratio recording. We present acute *in vivo* recordings from the cortex of the rat using the depth/surface neural probes.

This dissertation covers the development and fabrication of SiMW solar cells and neural probes to the characterization of device performances and analysis on data obtained from SiMW solar cells and neural probes.

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Chapter 2

Surface Passivation and Carrier Collection in {110}, {100} and Circular Si Microwire Solar Cells

2.1 Introduction

Micro/nanostructures provide promising building blocks for thin and flexible Si solar cells owing to their advantage of reduced volume with enhanced light trapping compared to conventional bulk crystalline Si.[1–7] In particular, radial p-n junctions in micro/nanowire solar cells allow lateral carrier separation, which leads to effective collection of photogenerated carriers over a short collection length.[8–10] However, the power conversion efficiency (η) of Si micro/nanowire solar cells is still low compared to conventional thick Si solar cells. Surface recombination is argued to be the dominant carrier collection loss mechanism in micro/nanostructure solar cells due to their large surface-area-to-volume ratio.[11–13] Severe surface recombination loss can compromise the benefits of improved optical absorption in micro/nanostructures and ultimately degrades η. One common strategy to suppress the surface recombination is to apply surface passivation layers that reduce the surface trap density and photogenerated minority carrier recombination at the surface.[14–17] The majority of previous studies on Si micro/nanowire solar cells utilized circular or cylindrical-shaped wires.[18–29] However, the sidewalls of circular or cylindrical Si microwires (SiMWs) contain high-index planes which are prone to more surface states than properly flat-faceted SiMWs.[23] Thus, controlling the micro/nanowire facets on crystal planes that are known to

have low interface state densities may help in reducing surface recombination and recovering the promised performance of micro/nanowire solar cells. Here, we devised a new approach toward SiMW solar cells by introducing SiMWs with well-defined sidewall facets known to result in low surface state densities. Solar cells were fabricated with square-shaped and flat-faceted SiMWs that have {110} and {100} sidewalls together with circular-shaped SiMW solar cells, and their electrical properties are compared to understand the effect of facet orientation on surface recombination. The SiMW solar cell performance is also influenced by the array geometrical design parameters (i.e., size, spacing, and height).[21,24,26,28–31] The surface area of SiMWs can be tuned by varying the size and spacing. In order to understand the correlation of design parameters on surface recombination and carrier collection, we carried out a comprehensive study of SiMW solar cell performance as a function of sidewall spacing (S) and diameter (D) for a fixed total surface area and optimized their cell performance. We observed that the SiMW surface facets with different crystal orientations have insignificant influence of solar cell performance compared to the SiMW height, spacing, and mesh electrode density. We decouple the influence of these design parameters on the optical and electrical characteristics of SiMW solar cells.

2.2 Experimental Detail

2.2.1 SiMW Etching

The morphology of SiMW obtained by top-down process is tunable by controlling the ICP-RIE gas flow rate (**Figure 2.1**, **Table 2.1**). F ions in sulfurhexafluoride (SF_6) etch-gas knock away Si ion or binds with Si to form a volatile SiF_4 which are pumped away while octafluorocyclobutane (C_4F_8) polymer-producing gas simultaneously passivates SiMW sidewall with polymer to ensure anisotropic etching with smooth surface.[32] As C_4F_8/SF_6 ratio is increased, SiMW showed a tapered sidewall profile due to thicker passivation layer. The tapered profile has advantage graded refractive index which enhances light absorption.[33] To correspond to the objective of our study, which is to investigate the surface recombination effect on different facets, we chose straight sidewall as possible to control the total surface area of SiMWs between different facets to be similar value.

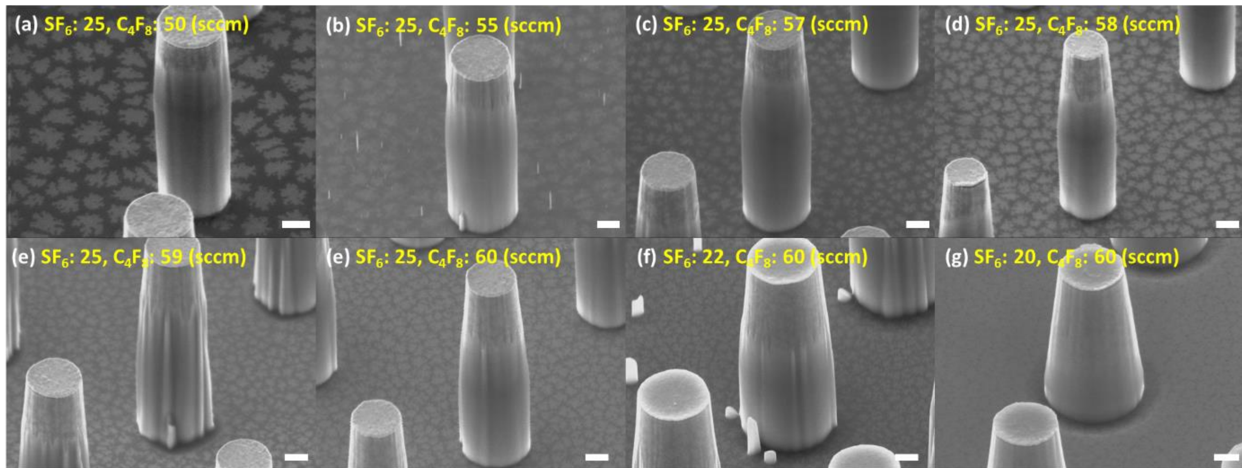

Figure 2.1 Scanning electron microscopy images (45-degree view) of SiMWs after ICP-RIE etching with different etch gas flow rate. Scale bars are 1 μm.

Table 2.1 Meausred sidewall angles of SiMWs etched with different gas flow rate.

SF_6 (sccm)	C_4F_8 (sccm)	C_4F_8/SF_6 ratio	Sidewall angle (°)
25	50	2.00	89
25	55	2.20	89
25	57	2.28	89
25	58	2.32	87
25	59	2.36	85
25	60	2.40	85
22	60	2.50	84
20	60	2.73	80

2.2.2 Fabrication of Verical SiMW Solar Cells with Radial p-n Junctions

200 nm thick Ni arrays were patterned as dry etch masks within an area of 1 × 1 mm^2 by photo or electron-beam lithography. 10 μm tall vertical SiMWs were etched by ICP-RIE with SF_6 and C_4F_8 gases. After Ni etch masks were removed by a commercial Ni etchant solution (Nickel Etchant TFB, Transene), oxygen plasma clean and Piranha cleaning (H_2SO_4:H_2O_2 = 3:1) were performed to remove organic residues from dry etching followed by the standard Radio Corporation of America (RCA) cleaning. Thermal oxidation at 1100 °C for 1.5 h (t_{SiO2} = 120 nm) and 6:1 BOE strip was applied to reduce the sidewall roughness induced by ICP-RIE etching.[20,25] Radial p-n junction was formed by spin-on-doping (SOD) method in rapid thermal annealing furnace. Prior to doping, SiMW arrays were prepared by the standard RCA cleaning to ensure clean surface. Phosphorus SOD source (P509, Filmtronics, Inc.) was spun-cast on a dummy Si wafer and cured at 200 °C for 15 min to evaporate excess solvent. Then the dummy wafer was placed on quartz spacers within 250 μm from SiMW arrays and annealed at 950 °C for 10 s in N_2 ambient followed by post-diffusion cleaning in 6:1 BOE to remove SOD residues. The surface of the formed p-n junctions was then passivated with a thin (<10 nm) thermally grown SiO_2 layer and a plasma-enhanced chemical vapor deposited (PECVD) SiN_X layer (80 nm); the SiN_X layer also served as an anti-reflective coating. The SiMW arrays were covered by photoresist and Si dry

etching of mesa structures for electrical isolation then followed after which the photoresist was stripped away. For the devices with passivation layers, SiO_2 and SiN_X were selectively removed for the area where top contact electrode will be deposited. Ti/Au (50/200 nm) was deposited on the n-doped layer as a top ohmic contact and 100 nm of Al was deposited at the backside of p-type substrate for a rear ohmic contact. It should be noted that each set of SiMWs that were used for performance comparison were fabricated on a single wafer where each wafer which also had a planar cell without SiMWs for a reference.

2.2.3 Doping Concentration of Base and Emitter

275 μm thick single crystalline p-type Si(100) wafers (boron doped, 0.2–0.4 Ω · cm) were used for this work. The optimal substrate doping density was calibrated in control SiMW cells (**Figure 2.2, Table 2.2**).

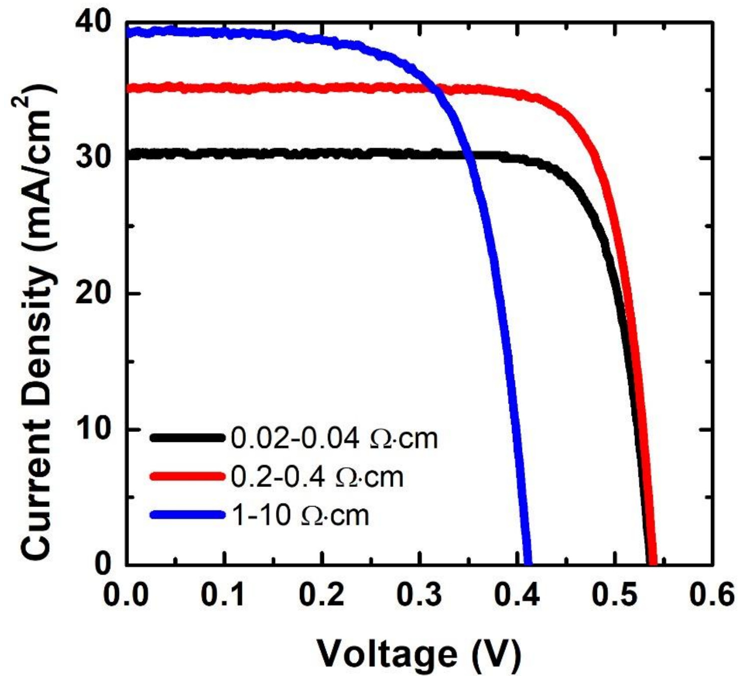

Figure 2.2 Measured light *J–V* characteristics of SiMW cells with different substrate resistivities.

Table 2.2 Measured solar cell performances of SiMW cells with different substrate resistivities.

Base Resistivity of *p*-Si substrate [Ω · cm]	Corresponding Carrier Concentration [atoms/cm^3]	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]
0.02 – 0.04	9.1x10^{17} – 2.7x10^{18}	30.4	0.537	79.2	12.9
0.2 – 0.4	4.1x10^{16} – 9.6x10^{16}	35.1	0.539	79.0	15.0
1 – 10	1.3x10^{15} – 1.5x10^{16}	39.4	0.411	68.7	11.1

Different annealing times and temperatures for different emitter doping layers were also calibrated for every new bottle of SOD dopant (**Table 2.3**) to optimize doping parameters that yield the best solar cell performance. Doping concentration and junction depth of emitter is determined by doping temperature and time where the increase in temperature leads to an increase in both surface doping concentration and junction depth while an increase in time results in increased junction depth but decreased surface doping concentration. We optimized the doping concentration and the thickness of the solar cell emitter by comparing performances of solar cells that were fabricated under different doping temperatures and times to obtain the optimal doping concentration and junction depth. From the results listed in **Table 2.3**, we concluded that the conditions of 950 ^{o}C, 10 s to be the optimized doping temperature and time, and these conditions were used as the fixed doping parameters for all cells that are reported here.

Table 2.3 Measured solar cell performances of Si planar cells under different doping parameters. Base resistivity of *p*-Si substrate is 0.2 – 0.4 Ω ·cm.

Doping Parameters (Temperature, Time)	Emitter Sheet Resistance [Ω/□]	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
925 °C, 10 s	160	33.7	0.541	75.7	13.8
950 °C, 10 s	120	33.7	0.555	77.0	14.4
950 °C, 15 s	101	31.8	0.546	73.8	12.8
950 °C, 20 s	88.5	32.7	0.537	75.6	13.3
975 °C, 10 s	93.1	32.6	0.531	68.3	11.8
975 °C, 20 s	64.6	34.0	0.545	74.6	13.8
1000 °C, 10 s	62.7	33.5	0.546	75.2	13.7
1000 °C, 20 s	47.9	32.6	0.541	66.3	11.7

2.2.4 Passivation and Anti-reflective Coating

The optimal thickness of the SiN_X anti-reflective coating layer was calculated to be 80 nm by 1) simulation of reflectance for ARC layers with different thickness using COMSOL Multiphysics (**Figure 2.3**) and MATLAB calculation of effective reflectance over wavelength (300 – 1100 nm) for different ARC layer thickness. The actual thicknesses of SiO_2 and SiN_X layer were measured by a spectrometer (F20, Filmetrics, Inc.) on planar cells. Annealing in Forming gas (H_2/N_2 5%/95%) at 400 °C was then performed for 30 min to terminate the dangling bonds at the interface between Si and the passivation layer and in the nitride passivation layer.[15]

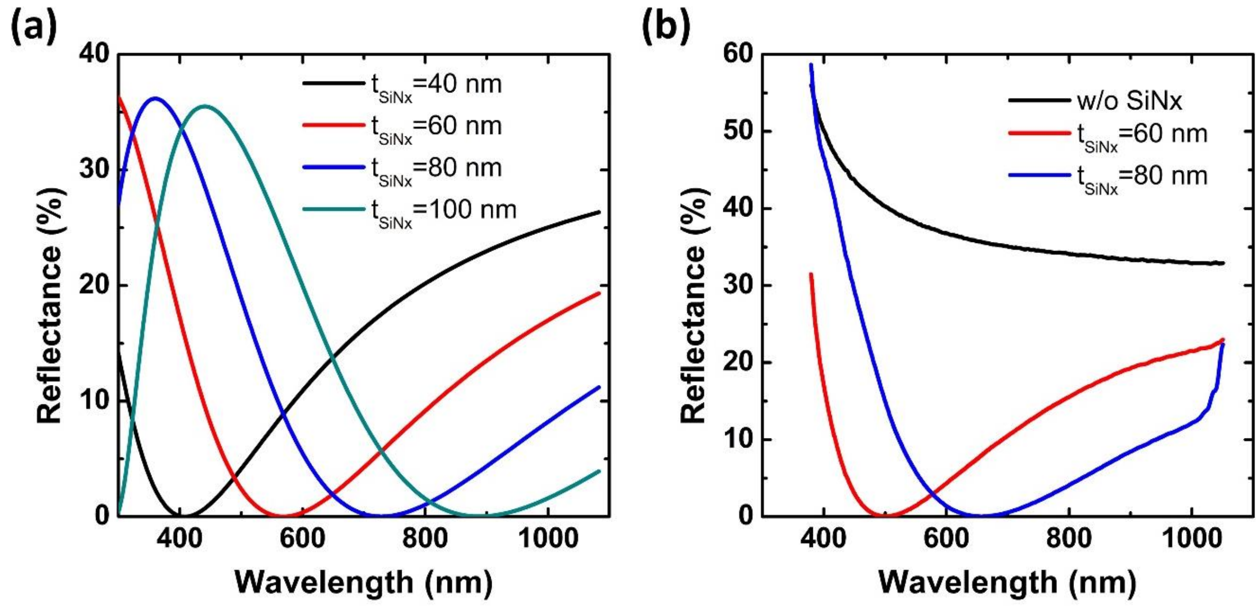

Figure 2.3 (a) Simulated and (b) measured reflectance of Si covered by SiO_2 (t_{SiO2}=10 nm) and SiN_x layer with different thicknesses. Simulation was conducted using COMSOL Multiphysics.

2.2.5 Characterization of SiMWs morphologies

The morphologies of SiMWs were characterized by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Thin slices of SiMW cross-sections were prepared by FEI Nova 600 Nanolab FIB tool. The TEM characterization was performed in FEI Titan 80-300 at 300 keV. The TEM studies were performed at the Center for Integrated Nanotechnologies at Los Alamos National Laboratory. The SIMS depth profiles of SiMW and planar cells were recorded by a CAMECA NanoSIMS 50L at Caltech Microanalysis Center. The carrier lifetime of the Si wafer was recorded by quasi-steady-state photoconductance lifetime measurement (WCT-120, Sinton Instruments) with iodine passivation. The minority carrier lifetime of SiMWs was measured by ultrafast pump probe measurement at the Center for Integrated Nanotechnologies at Los Alamos National Laboratory.

2.2.6 Device Characterization

The photovoltaic performances were measured under dark and light (AM 1.5G) conditions using a solar simulator (67005, Oriel) where 1 Sun (100 mW cm^{-2}) was calibrated using a National Renewable Energy Laboratory (NREL) calibrated reference photovoltaic cell (PV measurements, Inc.). The J–V characteristics were measured using a potentiostat (DY2300, Digi-Ivy, Inc.). For spectral photoresponse in 300–1100 nm wavelength range, a monochromator (Cornerstone 260, Oriel) equipped with a solar simulator was used and spectral reflectance measurement was carried out using a spectrometer (F40-UV, Filmetrics, Inc.).

2.3 Results and Discussion

2.3.1 Passivation and Crystal Orientation

The collection efficiency of nano and microstructured solar cells with higher surface-area-to-volume ratio than that of planar junction solar cells is degraded by surface recombination of photogenerated minority carriers. It is known that Si {100} surfaces have lower surface state densities compared to {110} and {111} surfaces, particularly when Si is passivated with its natural oxide, SiO_2.[34] By imaging carrier lifetimes on different surfaces, it has been reported that {100} planes passivated with thermal oxide exhibited lower surface recombination velocities compared to that of {111} planes.[35,36] This suggests that SiMW solar cells with crystalline flat facets with a low surface state density can potentially result in low surface recombination velocities and better minority carrier collection efficiencies. To investigate the facet orientation effects on surface recombination, we patterned our SiMW cell arrays to have three different facets on a single Si (100) substrate (p-type, 0.2–0.4 $\Omega \cdot$cm), {110}, {100} flat facets and circular without a well-defined facet for a reference. The alignment of the SiMW arrays in different facet orientations was determined by a substrate etching step using potassium hydroxide (KOH), which is the lowest at {111} planes and leads to pyramidal etch windows that are intercepted with ⟨110⟩ directions.[35] A PECVD SiN_x layer (200 nm) was used as a hard mask and was patterned by photolithography and reactive ion etching (RIE) of the SiN_x followed by Si anisotropic etching using 30 wt% KOH at 80 °C. After SiN_x mask removal, we aligned our SiMW arrays with {110} facets perpendicular to the exposed ⟨110⟩ directions during the KOH etch step. Arrays that are defined by 45° rotation in mask design with respect to the {110} ones will naturally form with {100} facets (**Figure 2.4**).[37] The fabrication steps of SiMW cells with radial p-n junctions are described in detail in the Experimental Section and are briefly summarized in **Figure 2.5 (a)–(f)**. **Figure 2.5 (g)–(i)** are

SEM images of {110}, {100} and circular-faceted SiMWs after inductively coupled plasma RIE (ICP-RIE) etching. A thermal oxidation step followed by stripping in buffered oxide etchant (BOE, 6:1) smoothed the rough sidewalls of SiMWs that were induced by the ICP-RIE etching (**Figure 2.6**).[20,25] This is important in reducing the surface defect density that traps photogenerated carriers.[38]

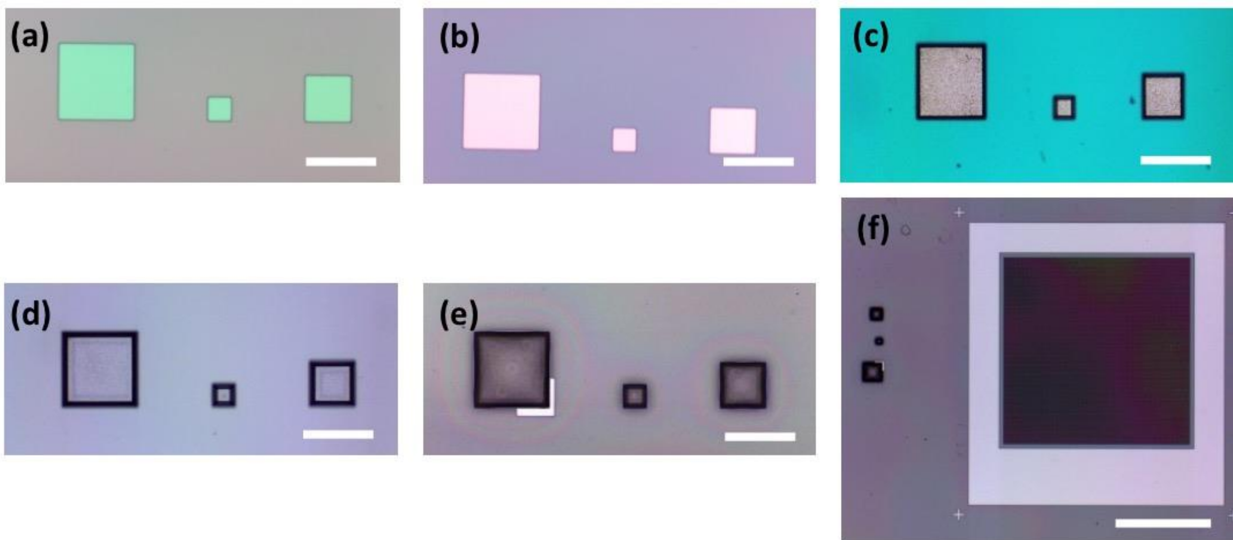

Figure 2.4 Optical microscopic images showing process flow of alignment of {110} flat-faceted Si microwire (SiMW) array by KOH etching. (a) Hard mask window patterning on SiN_x layer deposited on Si(100). (b) Hard mask window opening. (c) After KOH etching. (d) SiN_x mask removal. (e) Alignment mark patterning. (f) {110} flat-faceted SiMWs aligned in <110> direction. Scale bars are 100 µm for (a)-(e) and 500 µm for (f).

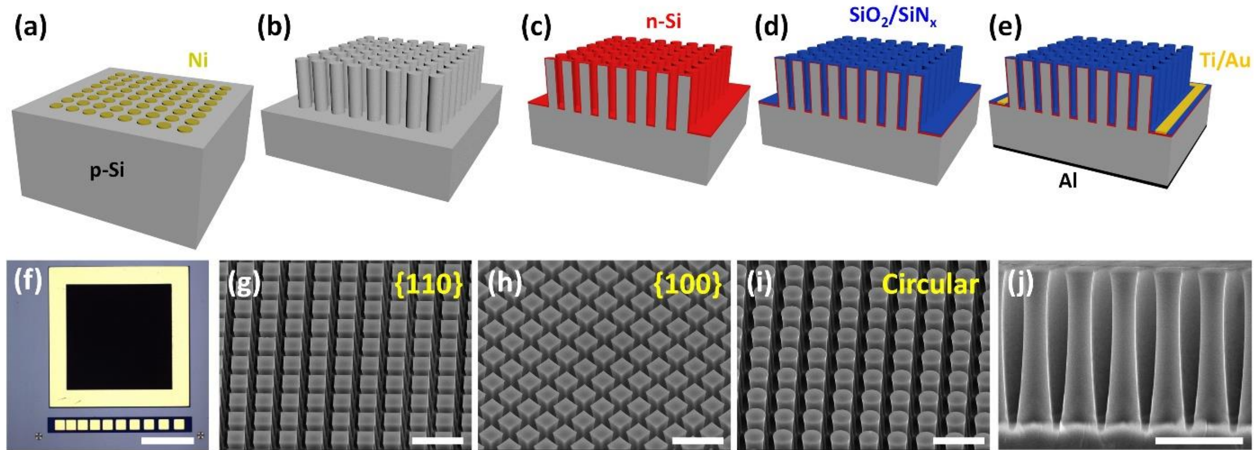

Figure 2.5 (a)-(e) Schematic illustration of the fabrication process (not to scale). (a) Ni dry-etch mask patterning. (b) ICP-RIE etching of SiMWs. (c) SOD phosphorus doping resulting in radial *p-n* junction. (d) Passivation of SiMW surface with SiO_2/SiN_x layer. (e) Mesa etching and patterned top metal electrode deposition; blanket bottom metal contact electrode deposition. (f) Top view optical microscopic image of a SiMW solar cell. Scale bar is 500 µm. (g)-(i) 45-degree view SEM images of 10 µm-tall SiMWs with different facets, {110} (width=1.5 µm, *S*=1 µm), {100} (width=1.5 µm, *S*=1 µm) and circular (*D*=1.5 µm, *S*=1 µm), respectively. Scale bars are 5 µm. (j) Cross-sectional SEM image of 10 µm-tall SiMWs. Scale bar is 5 µm.

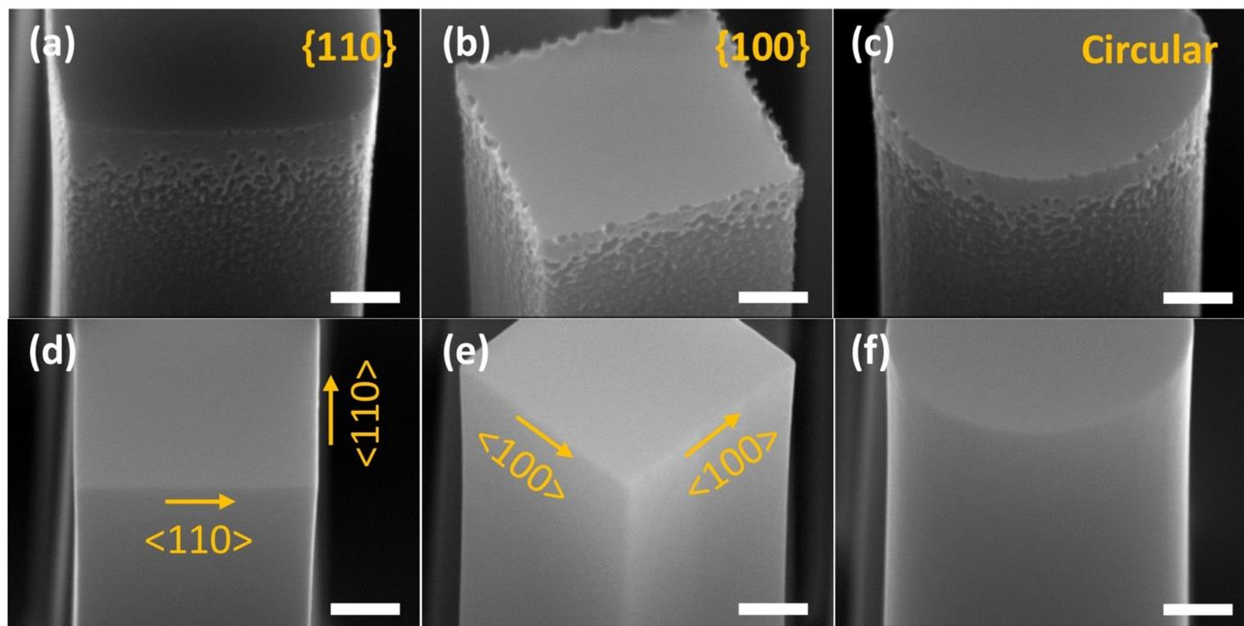

Figure 2.6 Magnified SEM images (45-degree view) of SiMWs with different facet orientations. (a)-(c) After ICP-RIE etching and Ni mask removal. (d)-(f) After thermal oxidation and strip. Scale bars are 500 nm.

2.3.1.1 Microwire Solar Cells versus Planar Solar Cells

The measured light and dark *J–V* characteristics for the devices displayed in **Figure 2.5** are shown in **Figure 2.7**. The widths (*W*) and *S* for {110} and {100} flat-faceted SiMWs were 1.5 μm and 1 μm, 1.5 μm and 1 μm, respectively. The diameter (*D*) and sidewall spacing (*S*) of circular SiMWs were 1.7 μm and 1 μm, respectively. The heights of SiMWs were fixed at 10 μm. In addition to different facet orientations, we compare the performances of solar cells without and with a passivation layer. A combination stack of thermally grown SiO_2 and PECVD SiN_x was chosen for the passivation layer because thermal SiO_2 forms a homogeneous layer with the Si surface with low interface state density while the SiN_x layer provides hydrogen passivation and acts as an antireflection coating (ARC).[15,39] The short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (*FF*), η, dark saturation current density (J_0), and ideality fill factor (*n*) are listed in **Table 2.4**. The J_0 and *n* were determined by linear extrapolation of the dark *J–V* curve at low forward bias in the range of $V = 0–0.3$ V. The *n* (1.52–1.73) for all studied cells are lower than 2, indicating the effectiveness of the passivation and the high quality of these SiMW solar cells to serve as a suitable platform to study the effect of surface recombination. For unpassivated devices, we found significant improvements (46–58%) in the J_{sc} of SiMW cells (24.2–26.1 mA cm^{-2}) compared to that of planar ones (16.5 mA cm^{-2}). Consequently, $V_{oc} = k_bT/q \times ln(J_l/J_0 + 1)$ is consistently larger by 4–5 mV in SiMW cells (0.539–0.540 V) validated through over 100 device runs. Here, k_b is Boltzmann's constant, *T* is the temperature, *q* is the fundamental charge constant, and J_l is the light-generated current density. This higher J_{sc} and V_{oc} for unpassivated SiMW cells compared to unpassivated planar cells is due to superior light absorption. This is deduced by comparing the external quantum efficiency (EQE) in **Figure 2.7 (c)** plots to the internal quantum efficiency (IQE) plot in **Figure 2.7 (d)**, where the overall EQE for unpassivated planar cells is

lower than that of unpassivated SiMW cells but the IQE of planar cells is higher than that for the SiMWs in the 400–600 nm wavelength regime. External quantum efficiency (EQE) was estimated using the following equation, $EQE = (R_\lambda/\lambda) \times (1240\ \mathrm{nmWA^{-1}})\ \times 100\%$ where R_λ is the photoresponsivity [$W^{-1}A$] at a given wavelength of incident light and λ is the wavelength [nm]. Internal quantum efficiency (IQE) was estimated using the following equation, $IQE = EQE(1 - R)$ where R is the reflectance. Here we assume that transmission through the substrate is negligible due to presence of the Al layer on the backside of the devices. This indicates poor collection efficiency for SiMW cells and that their enhanced absorption characteristics are the dominant contributor for the higher EQE and J_{sc}, and consequently V_{oc}. When the passivation layer is applied, both J_{sc} and V_{oc} increased due to reduction of surface recombination and increased light absorption assisted by the SiN_x ARC. The J_{sc} for the SiMW cells was ≈6–11% larger than that of planar cells. This difference is smaller than that for the unpassivated cells. Passivated planar cells exhibited 2% higher V_{oc} but 10.6% lower J_0, than passivated circular SiMW cells likely due to a higher residual surface recombination in the higher surface area SiMWs. This together with a lower ideality factor for the planar cells, that is, sharper forward J–V characteristics, lead to a higher FF for planar cells compared to passivated SiMW cells. It is worth noting that specific contact resistance for all samples was measured with the transmission line method and resulted in a $\rho_{c(un-passivated)} = 7.84 \times 10^{-5}\ \Omega \cdot \mathrm{cm}^2$ and $\rho_{c(passivated)} = 2.41 \times 10^{-5}\ \Omega \cdot \mathrm{cm}^2$. Secondary ion mass spectrometry (**Figure 2.11**) indicated lower phosphorus concentration near the surface for passivated cells compared to unpassivated cells. Therefore, we attribute the lower specific contact resistance for passivated cells due to a better contact/Si interface (lower interface contaminants) with thermally processed samples.

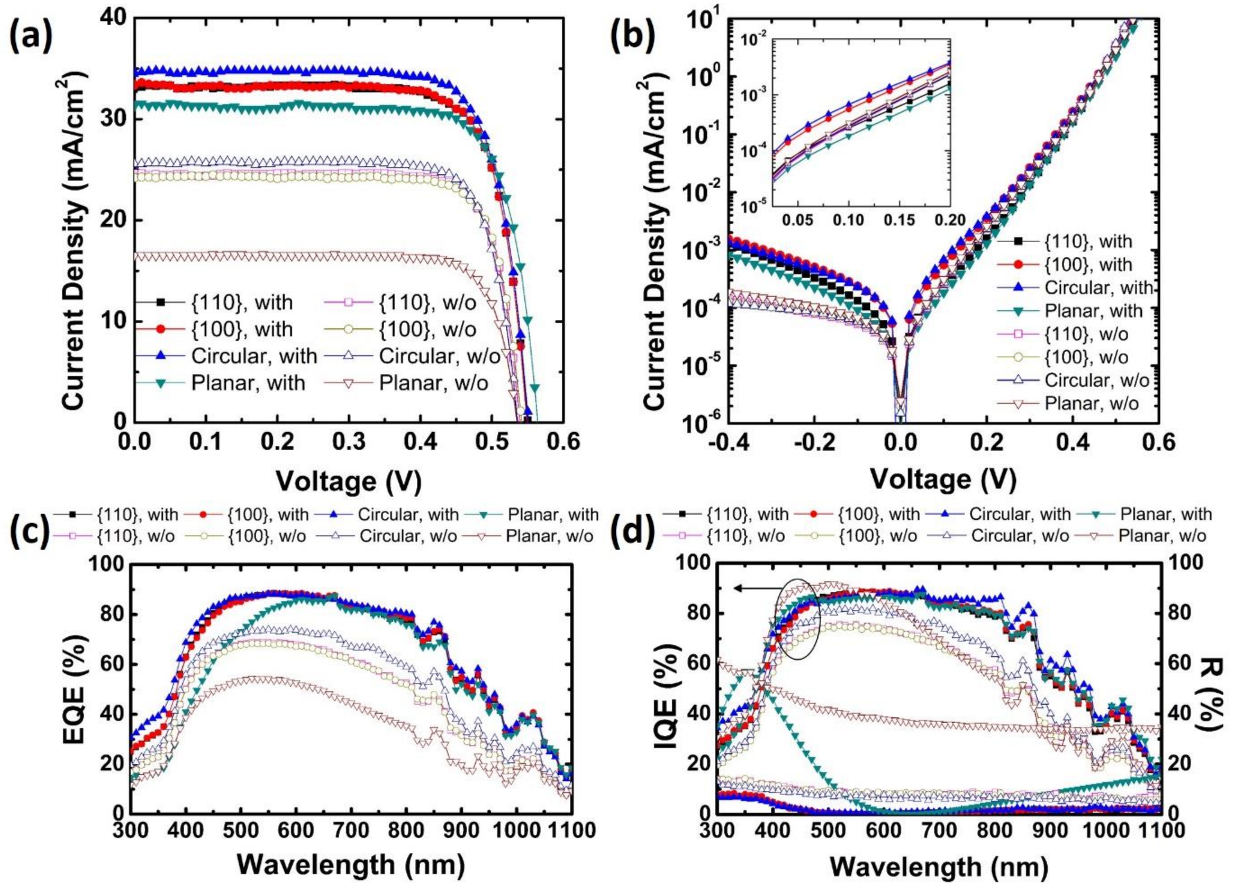

Figure 2.7 (a) Light and (b) dark *J–V* characteristics, (c) *EQE*, (d) *IQE* and Reflectance (*R*) of SiMW solar cell devices with different facet orientations and planar cells without and with a passivation layer (SiO_2/SiN_x, 5/80 nm) (See Figure 2.5 caption for details of cell topology).

Table 2.4 Measured solar cell performances of planar and SiMW solar cells with different facet orientations, without and with a surface passivation layer (See Figure 2.5 caption for details of cell topology).

Facet Orientation	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]	J_0 [nA/cm^2]	n
{110}, w/o	24.6	0.539	80.8	10.7	200	1.68
{110}, with	33.1	0.550	78.1	14.2	73	1.53
{100}, w/o	24.2	0.540	80.4	10.5	271	1.66
{100}, with	33.3	0.549	77.2	14.1	311	1.71
Circular, w/o	26.1	0.539	81.1	11.4	194	1.67
Circular, with	34.6	0.551	78.6	15.0	284	1.71
Planar, w/o	16.5	0.535	80.9	7.15	271	1.73
Planar, with	31.3	0.563	77.9	13.7	69	1.52

2.3.1.2 Microwires with and without Facets

To the best of our knowledge, the effect of facet orientation on the SiMW cell performance has not been studied or discussed before. To isolate the influence of surface recombination, we fixed the total surface area (≈7.8 × 10^5 μm^2) of the SiMW cells as well as the S of SiMWs (1 μm) for the {110},{100} and circular ones (**Table 2.5**). This deems the volume of the circular SiMWs to be greater than that of flat-faceted SiMWs. The results of this comparison are drawn from **Table 2.4**. With surface passivation, the J_{sc} and V_{oc} for {110} flat-faceted SiMW cells increased by 34 and 2%, respectively, and increased by 38 and 2%, respectively, for {100} flat-faceted SiMW cells. The {110} and {100} flat-faceted SiMW cells showed nearly identical performances in terms of J_{sc} and V_{oc} indicating similar surface recombination effects for both cells. With surface passivation for circular SiMW cells, the J_{sc} and V_{oc} increased by 33 and 2%, respectively. The circular SiMW cells exhibited 4% higher J_{sc} and 0.34% higher V_{oc} than {100} flat-faceted SiMW cells and an η = 15%, that is, 1% higher than that of the {100} flat-faceted SiMW cells (**Table 2.4**). The higher J_{sc} for circular SiMW cells is attributed to their better light absorption at short wavelengths (higher EQE in **Figure 2.7 (c)** and identical IQE in **Figure 2.7 (d)** compared to flat-faceted cells) and better collection efficiencies at long wavelengths from 750 to 1000 nm (identical EQE in **Figure 2.7 (c)** but higher IQE in **Figure 2.7 (d)** compared to flat-faceted cells) that is likely due to their larger cell volume (**Table 2.5**) as the total absorption volume increases with SiMWs volume which can efficiently absorb longer wavelength photons.[23,31] To evaluate the effectiveness of the surface passivation layer, we performed ultrafast pump-probe measurements on SiMWs with different facets with and without passivation and investigated their minority carrier lifetime (**Figure 2.8**).[40] For unpassivated SiMWs, the minority carrier lifetimes were longer (≈92 ps for {100} faceted SiMWs, followed by circular and {110} faceted SiMWs (≈61–67 ps). The passivated SiMWs

showed extremely slow dynamics with decay times that are well beyond our measurement capabilities (i.e., >1 ns), providing further evidence on the influence of the thermally grown SiO_2 and PECVD grown SiNx layers on surface passivation, which is consistent with previous results obtained by ours and other groups.[40,41] τ_d for un-passivated SiMWs shows the longest lifetimes for {100} faceted SiMWs (92.3 ps) which agrees to our expectation that the {100} facet will have the lowest surface recombination due to its low surface state density. This also explains the higher Voc measured for un-passivated {100} faceted SiMWs as compared to that of un-passivated {110} and circular SiMWs. When a passivation layer (SiO2/SiNx) is applied to SiMWs, the resulting time-resolved dynamics exhibited an extremely slow decay time that is beyond our measurement time range of ~300 ps, indicating that passivated SiMWs have a substantially longer minority carrier lifetime than un-passivated SiMWs, owing to reduced recombination from the passivated surface. Our ultrafast pump-probe microscopy setup[40] is based on a Ti:sapphire laser oscillator centered at 780 nm, the output of which is split into two arms. One arm is used as the probe and another arm is frequency-doubled in a BBO crystal to generate pump pulses at 390 nm. By using a 50X objective lens, the pump (2 μm spot size) and probe (1 μm spot size) beams are focused on an isolated single SiMW on a double-side-polished sapphire substrate. The polarization of both pump and probe beams are parallel to the SiMW axis. The initial carrier density generated by the pump is estimated to be $FA/E_{ph}d \sim 10^{18}$ cm^{-3}, where $F = 430$ μJ/cm^{-2} is the pump fluence, $A \sim 90\%$ is the absorbance of the SiMWs, $E_{ph} = 3.18$ eV is the pump photon energy and $d \sim 2$ μm is the SiMW diameter.

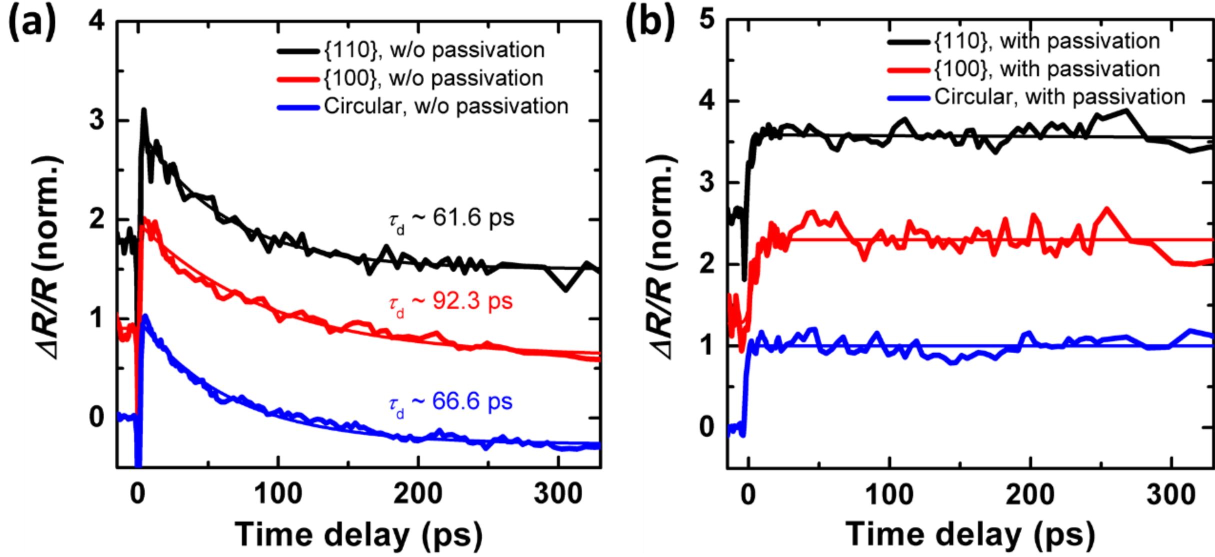

Figure 2.8 Ultrafast pump-probe measurements on (a) un-passivated and (b) passivated SiMWs with different facet orientations. Thick lines are measured normalized differential reflectivity ($\Delta R/R$) traces, offset for clarity. τ_{d} is the decay time constant, deduced from single-exponential fits (thin lines) to the traces.

Table 2.5 Geometric parameters of {110}, {100} and circular SiMW array solar cells.

Facet type	*W* or *D* [μm]	*S* [μm]	Number of SiMWs	Surface area of Device [μm^2]	Volume of SiMWs [μm^3]
{110}	1.5	1	1.12×10^5	7.76×10^5	2.53×10^6
{100}	1.5	1	1.12×10^5	7.76×10^5	2.53×10^6
Circular	1.7	1	1.27×10^5	7.79×10^5	2.88×10^6

While our results agree with earlier works that the SiMW cell performance is enhanced with surface passivation, we did not find that flat-faceted SiMW cells to be advantageous over nonflat SiMW cells. Since the passivated planar cells exhibited lower J_0 and higher V_{oc} than the SiMW cells, this seems to indicate that photogenerated carrier recombination prevails in SiMW cells even with the thermally grown surface oxide passivation. It is possible that this residual recombination blurs the benefits of using one surface facet versus the other or versus the nonflat circular SiMWs. Finally, it is important to note that the metrics presented in **Table 2.4** are reproducible from run to run. **Table 2.6** summarizes the results from three different runs in which

complete characterization for the different facets and planar reference devices with and without passivation is summarized.

Table 2.6 The average for measured solar cell performances from 3 runs for planar and SiMW solar cell devices with different facet orientations, without and with a surface passivation layer.

Facet Orientation	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]
{110}, w/o	28.5±3.31	0.521±0.019	75.5±6.48	11.1±1.02
{110}, with	34.8±3.36	0.540±0.008	77.3±0.58	13.5±1.08
{100}, w/o	28.4±3.64	0.525±0.014	74.6±5.00	11.0±0.56
{100}, with	34.2±2.81	0.539±0.007	78.6±0.72	13.8±0.75
Circular, w/o	29.2±2.69	0.524±0.016	74.9±5.49	11.4±0.50
Circular, with	34.7±2.34	0.538±0.008	77.8±0.38	14.0±0.81
Planar, w/o	19.1±3.69	0.523±0.016	78.0±4.10	7.75±0.85
Planar, with	27.0±1.37	0.555±0.006	76.4±0.79	11.4±0.56

We shall note however that there could exist many sources of nonuniformity in the processing of the devices. The most notable ones that we observed in our experiments include the uniformity of the proximity doping across individual samples that needed frequent calibration runs. Another source of nonuniformity includes small variations in the thermal oxide thickness, as further detailed below.

2.3.1.3 Metrology of Cell Structure and Analysis

To study the structural integrity of the SiMW cells and to understand the differences between SiMW and planar cells, we performed cross-sectional TEM analysis on all cell types studied here: {110}, {100} flat-faceted, nonflat circular SiMW cells and a planar cell with passivation (**Figure 2.9 (a)–(g)**) and a planar cell without passivation (**Figure 2.9 (h)**). First, the TEM images showed no noticeable defects in the SiMW and planar cells (**Figure 2.9.** and **Figure 2.10**). Second, despite small variation in the thickness of the thin thermally grown oxide layer at

850 °C between different samples (3–6 nm and nonuniform native oxide layer thickness for unpassivated planar sample), we observed a pronounced difference between the PECVD SiNx layer thicknesses. The thickness of the SiNx layer on the sidewalls of the SiMW cells was ≈40 nm whereas on the surface of the planar sample was ≈80 nm, in agreement with optical interferometry measurements (F20, Filmetrics, Inc.) performed on reference planar Si substrates. The shadowing effect of the SiMWs on the PECVD SiNx deposition in between tightly spaced wires, which is 1 μm for samples investigated with TEM, results in a thinner SiNx layer on the SiMW sidewalls compared to the non-shadowed planar surface. Thicker SiNx ARCs result in better absorption at short wavelengths (**Figure 2.3**) and while this effect has been optimized for the planar cells and the top surface of SiMWs, SiMW cells do not cultivate the same absorption benefits on their sidewalls. However, since light trapping effect of SiMWs enhances light absorption at their sidewalls, the optimized thickness of SiNx ARC at the top surface of SiMWs is more critical.[16] Third, the inset fast Fourier transform (FFT) pattern in **Figure 2.9 (a)–(c)** demonstrated alignment of the facets with the desired crystallographic directions resulting in {100} and {110} facets. For the radial SiMWs, the FFT pattern indicated that the resulting surface facets are of the {210} octahedral type. However, all of these facets are not atomically flat, as illustrated in the high-resolution TEM (HRTEM) images of **Figure 2.9 (i), (j)**. This, in addition to the graded diameter (tapering) across the SiMW length suggest imperfect facet orientations and therefore blurred effects on surface recombination and cell performance observed in **Figure 2.7** and **Table 2.4** above. The tapering leads to grading of effective refractive index that is known to enhance optical absorption in 1D nanowires.[33]

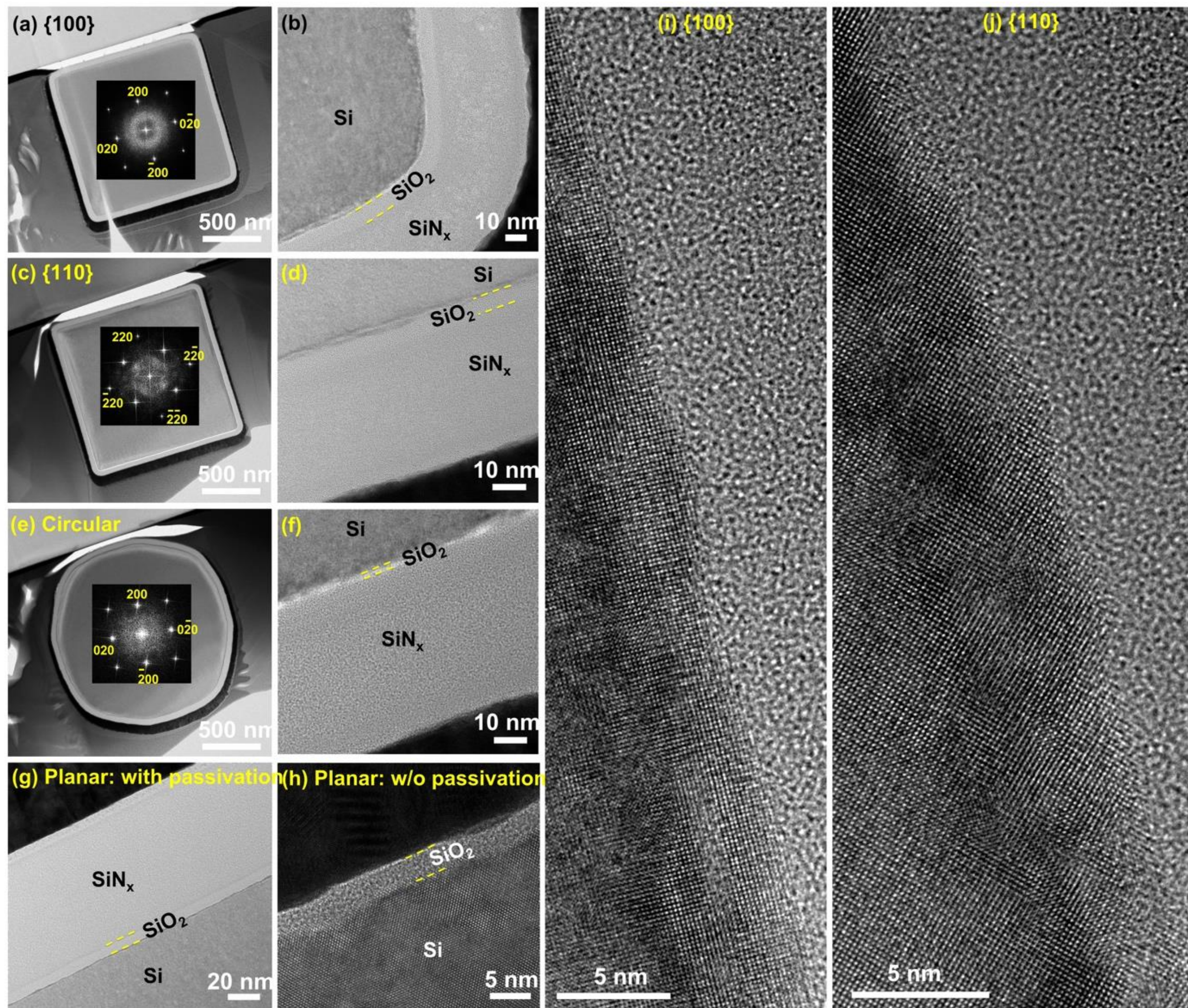

Figure 2.9 Cross-sectional TEM images. (a), (b) {100} flat-faceted, (c), (d) {110} flat-faceted, (e), (f) circular SiMWs. Surface passivation has been applied to all SiMW samples in (a)-(f). Insets to (a) – (e) are fast Fourier transforms of higher resolution TEM images taken from the same wires at a zone axis of 100. (g) Planar cell with a passivation layer. (h) Planar cell without a passivation layer. (i), (j) are HRTEM images at the side of the cross-sections (a) and (b), respectively.

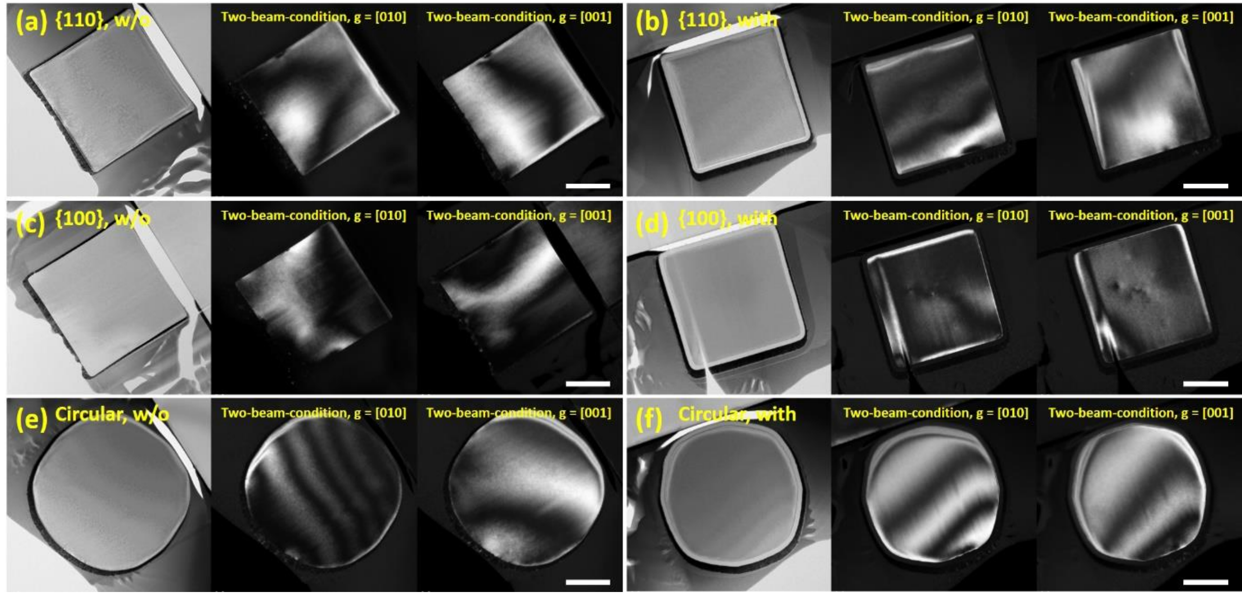

Figure 2.10 TEM images of SiMWs with different facets; bright field and dark field at two-beam conditions. Scale bars are 500 nm. Defects observed in the two-beam condition of (d) were induced during zone alignment.

To characterize the doping profile and junction depth on the planar and SiMW cells, we performed secondary ion mass spectrometry (SIMS) on planar cells with and without a passivation layer (**Figure 2.11 (a)**) and a single 1.5 μm wide, 10 μm tall {100} flat-faceted SiMW with and without a passivation layer (**Figure 2.11 (b)**). The junction depth (x_j) where the concentration of phosphorus determined from the SIMS profile, and background boron concentration—estimated by a four-point probe measurement prior to doping to be 5.3×10^{16} cm^{-3}—become equal, was estimated to be ≈450 nm for the unpassivated planar cell and ≈570 nm for the passivated planar cell. It should be noted that depth of SIMS profiles starts from the Si surface for the passivated cells and the Si/SiO_2 interface, beneath the SiO_2/SiN_x passivation layer for the passivated cells. The surface peak concentration of the unpassivated and the passivated planar cell was measured to be 9.7×10^{20} and 2.2×10^{20} cm^{-3}, respectively. The lower surface peak concentration and the broadening of x_j for the passivated planar cell are attributed to the redistribution of phosphorus

dopants during thermal oxidation where phosphorus atoms diffuse to deeper Si during thermal oxidation.[42] For the SiMWs, the SIMS was carried out on three different locations of a single SiMW sidewall: top (1 μm below the tip of SiMW), center (5 μm below the tip of SiMW), and bottom (1 μm above the base of SiMW) as shown in **Figure 2.11 (b)**. For SiMWs, we observed larger dopant concentration only at the top region of unpassivated SiMW surface, compared to passivated ones, similar to the planar cell case, while at the center and the bottom region, unpassivated SiMW has lower dopant concentration at the surface. The phosphorus concentration at the surface decreases from the top to the bottom portion of unpassivated SiMWs due to shadowing effects on phosphorus diffusion in between the SiMWs. In contrast to the unpassivated SiMW, the SIMS profiles of the passivated SiMW show nearly identical phosphorus concentration near the surface among three different locations. It is possible that during forming gas annealing at 400 °C, which we performed after passivation layer was applied, phosphorus atoms redistributed in the SiMWs which contributed to a more uniform doping profile.[43] The SIMS profiles at the top and the center region of SiMWs show no obvious p-n junction. This can be attributed to experimental errors induced by the inclination of the small diameter SiMW as it lays down on its side due to a larger base width than tip width and/or procedural errors. Cross-calibration with an ion-implanted reference sample with known dopant profiles and planar cells has been conducted to verify the SIMS results which we concluded to be due to experimental errors during SIMS measurements at the center and tip of the SiMWs. The results exhibited here serve as a qualitative analysis of the differences in the doping profiles within a single SiMW and between SiMW and planar cells. The bottom region of the SiMW exhibited a p-n junction with a shallow depth from the surface of ≈ 100 nm. To calculate the electric field and energy band-edge profiles for the different cells under consideration, we used Silvaco Atlas simulations to calculate the 1D Poisson's

solutions based on the experimentally measured phosphorus dopant profiles (**Figure 2.11 (c)–(f)**). Surface Fermi energy pinning was not accounted for in these simulations. These simulations assumed that all phosphorus dopants are electrically active even though this might not be the case for the very high concentration measured at the planar cells. The energy band diagram, particularly for the planar cells without passivation, resemble an n+-n-p structure with a highly doped surface that results in a strong electric field at the surface that serves as a front surface field layer and reduces surface recombination.[44] This explains higher IQE of planar cells compared to that of SiMW cells at the short wavelength regime for both without and with passivation (**Figure 2.7 (d)**) despite the fact that the junction depth and the maximum electric field for charge separation in the cell is closer to the surface for the SiMW cells ($x_j = 100$–125 nm) than the planar cells ($x_j = 450$–570 nm). Moreover, the stronger electric field at the surface of the unpassivated planar cell compared to the passivated planar cell explains the poorer blue spectral response of the passivated planar cell than that of the unpassivated one, which is not the usual case when surface recombination is suppressed by passivation layer.[15] On the contrary, for SiMWs, the electric field is stronger at the surface when SiMWs are passivated compared to that of unpassivated case, which together with reduced surface recombination results in higher IQE at the short wavelength regime of the passivated SiMWs than that of unpassivated SiMWs. Moreover, for high doping concentration (>10^{18} cm^{-3}), Auger recombination limits the photogenerated carrier collection not only at the short wavelength but also at the longer wavelength for the SiMW case because of their efficient absorption of longer wavelength photons.[12] Consequently, lower IQE for unpassivated SiMW cells at longer wavelength (>600 nm) was observed compared to passivated SiMW cells for which the SiN_x passivation layer effectively suppressed the Auger recombination.[15]

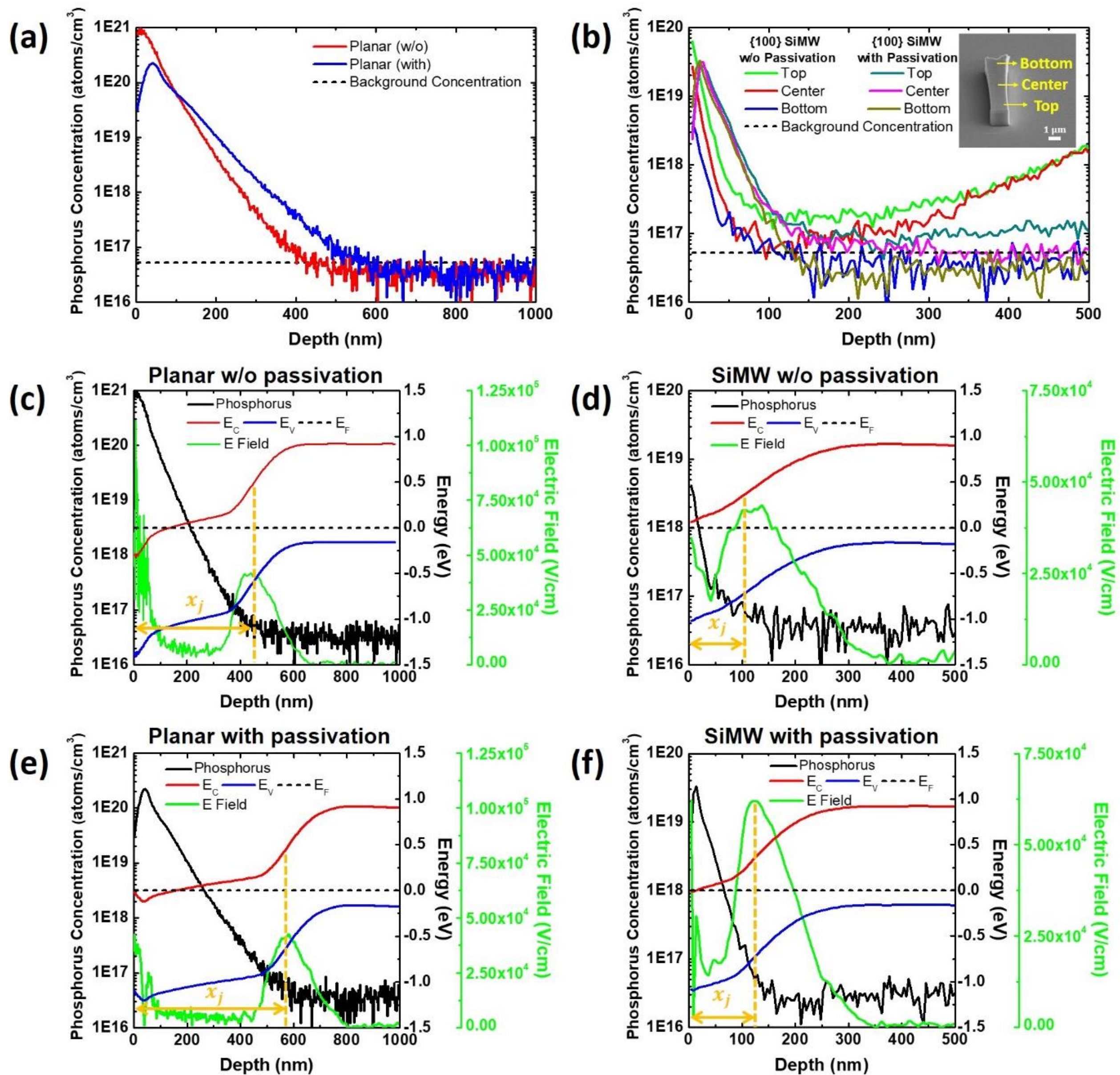

Figure 2.11 Measured SIMS profiles of (a) a planar cell without and with passivation. (b) Measured SIMS profiles of a {100} flat-faceted SiMW without and with passivation, measured at top, center, and bottom of the SiMW. Inset is the SEM image of a single {100} flat-faceted SiMW showing locations where the SIMS profiles were measured. Simulated energy band diagram and electric field of a (c) planar cell without passivation, (d) {100} flat-faceted SiMW (Bottom) with passivation, (e) planar cell with passivation, (f) {100} flat-faceted SiMW with passivation. x_j indicates junction depth for each cell.

2.3.2 Spacing and Diameter Dependence

To exploit the benefits observed here for absorption and photogenerated carrier collection in SiMW cells, we studied the influence of sidewall spacing (*S*) and diameter (*D*) of circular SiMWs in cell arrays that were fabricated side-to-side on the same Si sample. It is natural to expect that the effects of surface recombination will decrease with a lower surface-area-to-volume ratio in SiMW array cells. This can be accomplished by having sparse wire array or increasing the *D* of SiMWs but such geometries compromise light trapping effects of the SiMWs and the radial charge separation, respectively.[31] Therefore, it is important to find the optimized *D* and *S* to have balanced surface recombination, light absorption, and carrier separation that can yield high η for SiMW cells. For the SiMWs with different *S*, the *S* of the SiMWs after thermal oxidation and stripping were 2.5, 4.5, 6.5, and 8.5 μm where the *D* were kept the same as 1.5 μm. For the SiMWs with different *D*, the *D* after thermal oxidation and stripping were 1.5, 3.5, 5.5, 7.5 and 9.5 μm where the *S* were kept the same as 1 μm (**Figure 2.12**). The hole carrier lifetime measurement of the Si substrate (0.11 μs) confirmed that the *D*/2 is smaller than the minority carrier diffusion length (≈15 μm).[8] *S* and *D* were defined from the top surface of each SiMW. Circular SiMW arrays were used throughout these studies of the *S* and *D* dependence. The height of SiMWs was also fixed at 10 μm. Tighter S of SiMWs resulted in a higher geometrical fill factor over the active cell area (**Table 2.7**). On the other hand, the total surface area of the SiMW arrays increased with tighter *S* and can consequently result in higher surface recombination effects. Furthermore, the increase in surface area corresponds to larger junction area recombination.[14,28] Junction recombination yields increased J_0 which consequently leads to degradation of V_{oc}. This is evidenced by **Figure 2.13 (a), (b)** and **Table 2.7** which show that as the number of the SiMWs decreased with larger S, J_0 decreased and concomitantly V_{oc} increased. The V_{oc} for sparse arrays became similar to that of

planar devices (V_{oc} = 0.552 V). The SiMW cell with the tightest S (2.5 μm) exhibited the highest J_{sc} of 30.1 mA cm^{-2} and the best η of 12.7%. Results presented in **Table 2.8** measured on six different runs corroborate the above trends.

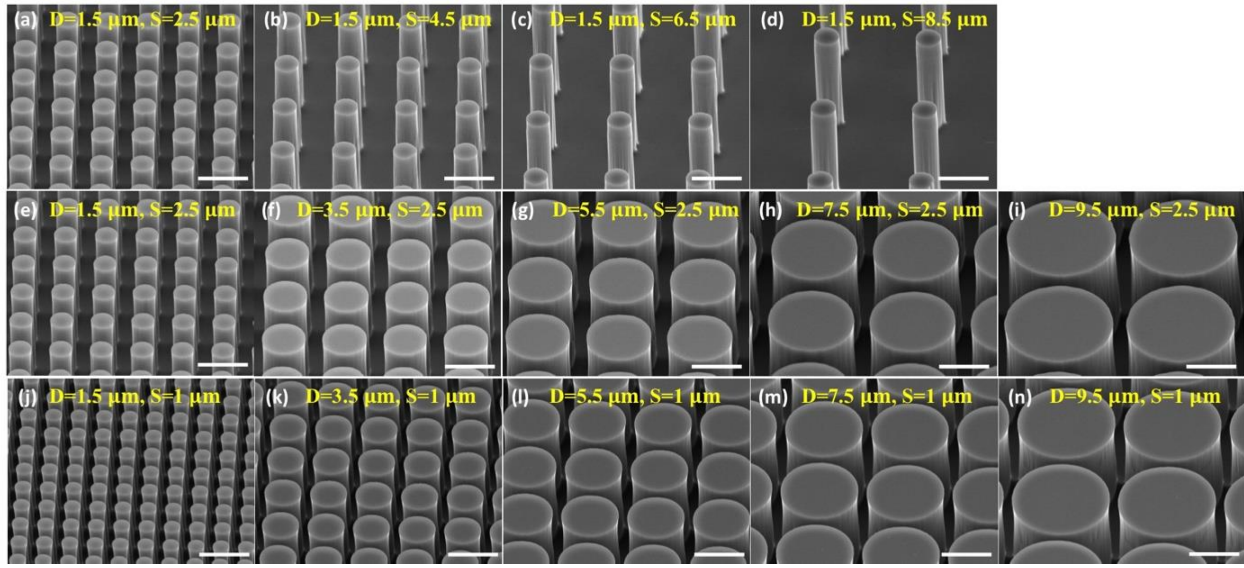

Figure 2.12 SEM images (45-degree view) of 10 μm-tall SiMWs with different *S* and *D*. Scale bars are 5 μm.

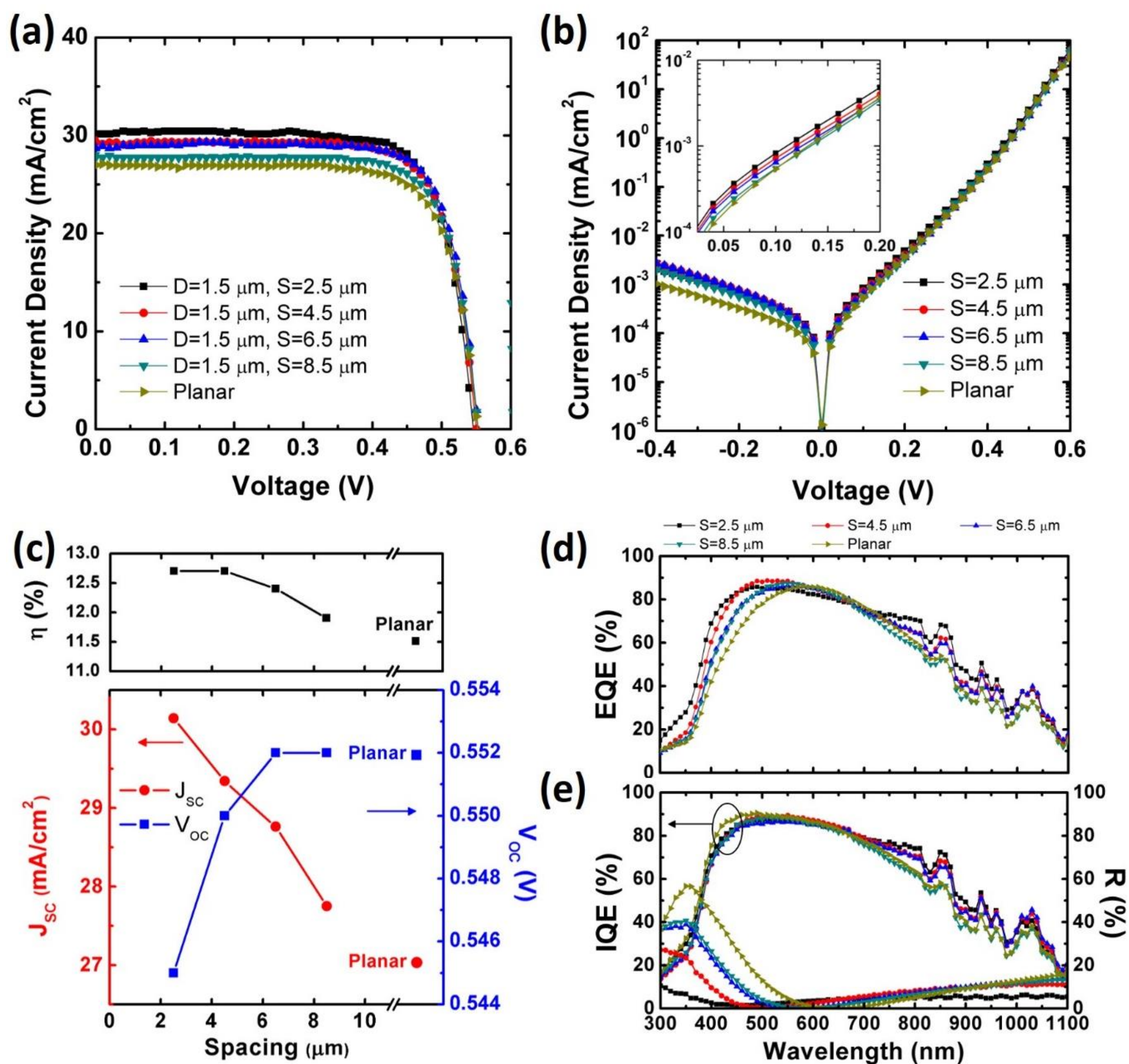

Figure 2.13 (a) Light and (b) dark *J–V* characteristics, (c) J_{sc}, V_{oc} and η dependence on *S*, (d) *EQE*, (e) *IQE* and *R* of SiMW solar cell devices with different *S* (*D*=1.5 μm).

Table 2.7 Measured solar cell performances of SiMW solar cells with different *S* (*D*=1.5 μm).

Device (*D*=1.5 μm)	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]	J_0 [nA/cm^2]	*n*	Relative Surface Area	Geometric Fill Factor [%]
S=2.5 μm	30.1	0.545	77.2	12.7	736	1.88	3.63	10.0
S=4.5 μm	29.3	0.550	78.5	12.7	615	1.89	2.22	4.5
S=6.5 μm	28.8	0.552	78.3	12.4	519	1.85	1.71	2.5
S=8.5 μm	27.7	0.552	77.7	11.9	433	1.76	1.44	1.6
Planar	27.0	0.552	77.2	11.5	590	1.89	1.00	-

Table 2.8 The average for measured SiMW solar cell performances from 6 different runs of cells with different *S* (*D*=1.5 μm).

Device (*D*=1.5 μm)	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
S=2.5 μm	30.9±1.98	0.540±0.005	77.8±1.02	12.8±1.00
S=4.5 μm	29.1±1.42	0.548±0.003	76.9±1.04	12.1±0.56
S=6.5 μm	28.4±1.05	0.547±0.007	76.2±0.69	11.5±0.67
S=8.5 μm	28.0±1.54	0.547±0.007	78.1±1.02	11.2±0.55
Planar	27.0±1.37	0.555±0.006	76.4±0.79	11.4±0.56

It is argued that SiMW cells have the advantage of enhancing light absorption through light trapping effects and of efficient carrier separation and collection over short radial distances. Thus, decrease in J_{sc} for sparse arrays (**Figure 2.13 (c)**) is attributed to lower number of SiMWs which is evidenced by EQE measurement (**Figure 2.13 (d)**). It should be noted that the planar region underneath SiMWs also contributes to J_{sc}. EQE at the short wavelength is largest for the smallest *S* and decreases as the S becomes larger and exhibit the lowest value for the planar cell. This is due to superior light absorption of SiMWs as evidenced in the reflectance measurement results (**Figure 2.13 (e)**). This shows the optical benefit of tighter spaced wires surpassed the disadvantage of surface recombination loss.[26] Planar cells exhibited the highest IQE at the short wavelength and interestingly, SiMWs with different S resulted in similar IQE spectra. This suggests that the surface recombination due to the large surface area was successfully suppressed by clean wire surface and

optimal surface passivation layer (SiO_2/SiN_x). We conclude that the increase in J_0 for arrays with a larger number of SiMWs is more likely due to junction recombination.[14] We next examined the effect of the D of SiMW on solar cell performance. As the D of SiMW increases, the total surface area of the SiMWs within the 1×1 mm^2 active cell area decreases and becomes close to that of planar cells (**Table 2.9**).

Table 2.9 Measured solar cell performances of SiMW solar cells with different D (S=1 μm).

Device (S=1 μm)	J_{sc-} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]	J_0 [nA/cm^2]	n	Relative Surface Area	Geometric Fill Factor [%]
D=1.5 μm	34.0	0.547	77.2	14.3	160	1.60	8.08	25.8
D=3.5 μm	33.2	0.551	78.0	14.3	107	1.60	6.11	43.4
D=5.5 μm	33.8	0.550	78.1	14.6	82	1.56	4.85	51.4
D=7.5 μm	34.2	0.553	78.4	14.8	77	1.55	4.05	55.4
D=9.5 μm	33.0	0.554	79.0	14.5	75	1.52	3.52	58.2
Planar	31.3	0.563	77.9	13.7	69	1.52	1.00	-

As described above, an increase in the total surface area can increase the possibility of both surface and junction recombination. This is evidenced by the increasing trend in V_{oc} with the D as shown in **Figure 2.14 (a), (c)**. The highest V_{oc} = 0.554 V is obtained from the SiMW cells with the largest D (9.5 μm). On the other hand, J_{sc} does not show a clear dependence on D with a fixed S. Ambiguous trend in J_{sc} is attributed to two conflicting factors that determine J_{sc}, light absorption and recombination loss. The SiMW cell with D = 7.5 μm and S = 1 μm exhibited the best η of 14.8% with J_{sc} = 34.2 mA cm^{-2}, V_{oc} = 0.553 V, and FF = 78.4%. To clarify the D dependence on photovoltaic performance, we evaluated their quantum efficiencies. At the short wavelength, EQE is the highest for the smallest D (1.5 μm) and decreased as the D increases; the largest D (9.5 μm) exhibited the lowest EQE among the SiMW cells with different D as shown in **Figure 2.14 (d)**. From the reflectance measurements shown in **Figure 2.14 (e)**, we found that the magnitude of the

reflectance at the short wavelength is proportional to the *D*. When the SiMWs have a large *D*, the area of the top flat surface of the SiMWs reflects the high-energy photons and lead to a reduced EQE at the short wavelength. For EQEs in the long wavelength range, there is an opposite behavior to the short wavelength region, with the highest EQE at the largest D (9.5 µm) and the lowest EQE at the smallest *D* (1.5 µm). From these results, we conclude that for the short wavelength, light absorption of SiMWs with smaller *D* is superior and SiMWs with larger *D* have better light trapping for long wavelengths. This *D* dependent spectral response suggests that if we combine SiMW arrays with two or more different *D*, we can expect an enhancement in J_{sc}.[45] The similarity in the IQE values at the short wavelength for different *D* indicate that the surface recombination can be suppressed by a surface passivation layer which is in agreement with our discussions above. Results presented in **Table 2.10** measured on four different runs corroborate the above trends.

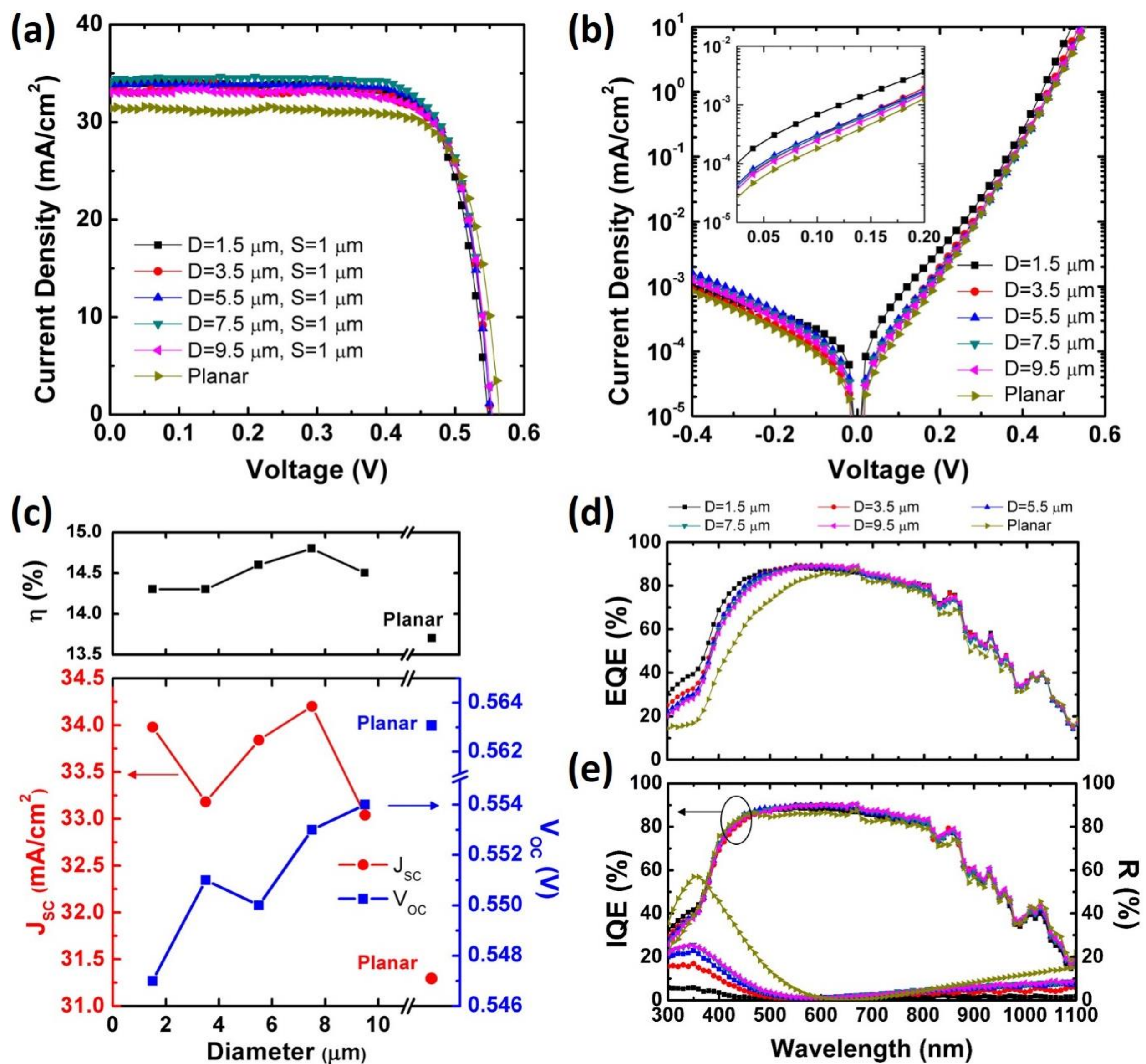

Figure 2.14 (a) Light and (b) dark *J–V* characteristics, (c) J_{SC}, V_{OC} and η dependence on *S*, (d), *EQE*, (e) *IQE* and *R* of SiMW solar cell devices with different *D* (*S*=1 μm).

Table 2.10 The average for measured SiMW solar cell performances from 4 different runs with different D (S=1 μm).

Device (S=1 μm)	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]
D=1.5 μm	29.7±1.92	0.533±0.012	76.1±1.99	12.1±1.10
D=3.5 μm	30.0±1.54	0.534±0.009	77.4±1.53	12.1±1.26
D=5.5 μm	29.5±1.43	0.538±0.010	75.8±1.04	12.1±0.82
D=7.5 μm	29.3±1.33	0.537±0.011	76.3±1.56	12.0±1.01
D=9.5 μm	28.8±1.72	0.537±0.012	77.1±0.61	12.1±1.22
Planar	26.4±3.53	0.547±0.010	77.4±1.48	11.2±1.42

2.3.3 Contact Design

Finally, our SiMW cell devices do not have a top transparent contact such as transparent conducting oxide over the SiMWs but rather an array-surrounding top contact such that photogenerated carriers need to drift in the thin heavily doped surface n-layer toward the contact. We chose an array surrounding top contact in order to avoid potential problems of transparent contacts such as their low transmittance at the visible light region[46] or the presence of interfacial defects between these contacts and Si.[47] To reduce the series resistance encountered in the n-layer of the cell, we applied mesh-type top contact electrodes with different spacings on SiMW cells as displayed in **Figure 2.15 (a)–(d)**. Mesh electrodes provide shorter carrier path length which helps in lowering the probability of carrier recombination and thus leads to efficient charge collection.[46,48] The mesh electrodes line width was 20 μm and the mesh side-to-side spacings were for a 2 × 2 mesh, 235 μm, a 3 × 3 mesh, 320 μm, and for a 4 × 4 mesh, 490 μm, where the side-to-side spacing and width of the single electrode without a mesh was 980 and 160 μm, respectively. Here, the D, S and height of the SiMWs were 1.5 μm, 1 μm and 10 μm, respectively, for all meshes. It is worth noting that the metal electrodes were deposited at the bottom part of the SiMWs as shown in **Figure 2.15 (e)** to minimize the carrier path length. The light J–V characteristics and J_{sc},

V_{oc}, and η dependence are displayed in **Figure 2.15 (f), (g)**. We found a clear increase in J_{sc}, V_{oc}, and FF when the spacing of mesh electrodes became tighter and correspondingly the η. The SiMW cell with the smallest electrode side-to-side spacing (235 μm) showed the highest J_{sc} of 35.2 mA cm^{-2}, V_{oc} of 0.550 V, and FF of 79.1%, resulting in the best η of 15.3% among the devices reported in this work. This mesh spacing dependence is also found in J_0, where J_0 decreased at the same time with spacing of mesh electrode (**Table 2.11**). These results indicate that a shorter carrier path length results in reduction of series resistance (**Table 2.11**) and assists in efficient carrier collection.[48] Higher IQEs for tighter electrode spacing in overall wavelength region (**Figure 2.15**) indicate that smaller spacing clearly diminished the carrier collection losses. It is notable that this enhancement in IQE at long wavelengths with a tighter electrode design is a manifestation of higher absorption in SiMWs at long wavelengths compared to planar cells where electrode spacing effects at long wavelengths are not significant. Results presented in **Table 2.12** measured on three different runs corroborate the above trends.

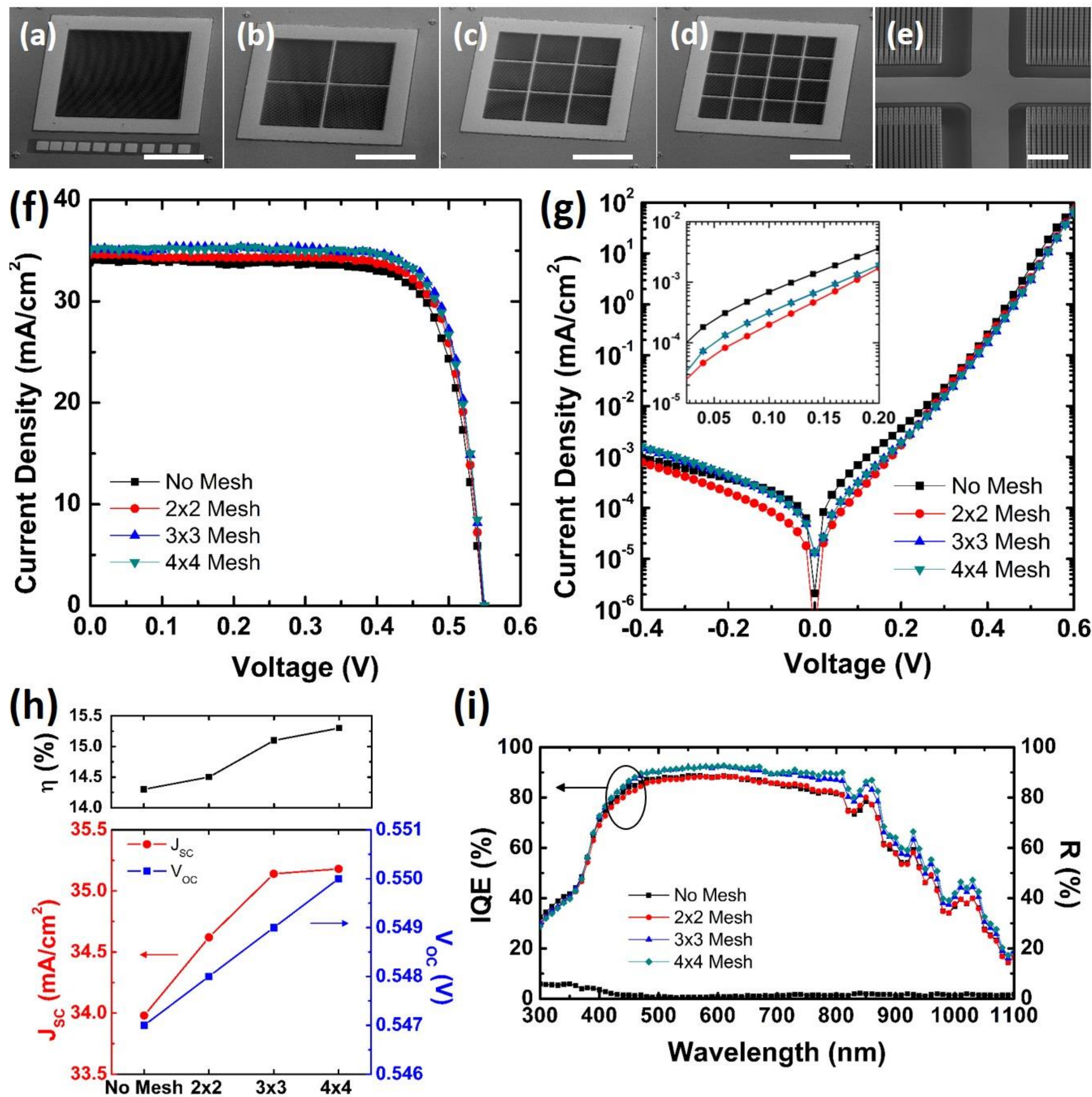

Figure 2.15. (a)-(d) Overview SEM images (45-degree view) of SiMW solar cell devices surrounded by Ti/Au contact pads. The *D* and *S* of SiMWs are 1.5 μm and 1 μm, respectively. The side-to-side spacing between adjacent electrodes is (a) No mesh: 980 μm (b) 2x2 Mesh: 490 μm (c) 3x3 Mesh: 320 μm (d) 4x4 Mesh: 235 μm. Scale bars are 500 μm. (e) A magnified SEM image (45-degree view) showing mesh-design top contact electrode and SiMWs. Scale bar is 20 μm. (f) Light and (g) dark *J*-*V* characteristics, (h) J_{sc}, V_{oc} and η dependence on spacing of electrodes, (i) *IQE* and *R* of SiMW solar cell devices with different top electrodes.

Table 2.11 Measured SiMW solar cell performance with different top contact designs (D=1.5 µm, S=1 µm).

Device	Spacing of Adjacent Electrodes [µm]	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]	J_0 [nA/cm^2]	n	R_S [Ω·cm^2]
No mesh	980	34.0	0.547	77.2	14.3	160	1.60	1.06
2x2	490	34.6	0.548	77.7	14.7	108	1.55	0.98
3x3	320	35.1	0.549	78.4	15.1	90	1.56	0.97
4x4	235	35.2	0.550	79.1	15.3	88	1.54	0.96

Table 2.12 The average for measured SiMW solar cell performances from 3 different runs with different top contact designs (D=1.5 µm, S=1 µm).

Device	Spacing of Adjacent Electrodes [µm]	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η [%]
No mesh	980	29.4±2.56	0.533±0.014	77.4±1.44	12.1±1.31
2x2	490	29.3±4.64	0.532±0.014	76.7±1.56	11.9±2.20
3x3	320	29.6±4.76	0.532±0.015	77.1±1.97	12.2±2.52
4x4	235	29.7±4.78	0.533±0.015	77.8±2.14	12.4±2.59

2.4 Conclusion

In summary, we performed an experimental parametric study on the effects of surface recombination and array geometry on the detailed performance of SiMW solar cells. Our results showed that with optimal surface passivation, surface recombination can be suppressed and have the advantage of enhanced light absorption from antireflective coating. SiMWs with different surface facets did not result in improved cell performance. Our results suggest that geometrical parameters of SiMWs strongly affect the device performances, especially in dark saturation current and light absorption. We found that for different *S* and *D* of SiMWs, the total surface area of SiMWs is reduced, there is an enhancement in V_{oc} which is compromised with lower light absorption. Moreover, carrier recombination loss can be reduced by applying mesh-type electrode that provides short carrier path length.

2.5 Acknowledgements

The chapter 2, in full, is a reprint of the material as it appears in *Advanced Energy Materials* in 2018 co-authored with Yun Goo Ro, Renjie Chen, Ren Liu, Nan Li, Theodore Williamson, Jinkyoung Yoo, Sangwan Sim, Rohit P. Prasankumar, and Shadi A. Dayeh. The authors thank Mr. Ahmed T. El Thakeb for the absorption calculations, Mr. Michael Jensen for initial calibration of SiMW etching, Mr. Jonathan Scharf for the lifetime measurements, and Dr. Yunbin Guan for the SIMS measurement. The authors also thank Prof. Yu-Hwa Lo, Prof. David P. Fenning, Dr. Yuchun Zhou, Dr. Yu-hsin Liu, and Dr. Alireza Kargar for the helpful discussions. The authors acknowledge Dr. Michael Williams and the UC San Diego Nano3 staff for technical assistance. The dissertation author designed all experiments, fabricated the devices, performed all analysis, and co-wrote the manuscript. Dr. Renjie Chen performed e-beam lithography. Dr. Renjie Chen, Dr. Ren Liu and Dr. Nan Li. performed the TEM analysis. Dr. Theodore Williamson and Dr. Jinkyoung Yoo contributed to the SIMS measurements. Dr. Sangwan Sim and Dr. Rohit P. Prasankumar performed pump-probe measurements and analysis. Prof. Shadi A. Dayeh led the project, designed the experiments, performed all analysis, and co-wrote the manuscript.

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Chapter 3

Solar Power Energy Harvesting through a Flexible Silicon CMOS-compatible Integrated Process for Physiological Monitoring in Wearable Devices

3. 1 Introduction

Flexible and wearable electronics integrated with human body to provide real time sensing and monitoring of health and activities became main components of internet of things (IoT) technology. A key driver to achieve breakthrough development for flexible and wearable electronics is replacing conventional bulky and rigid battery, which occupies large proportion of volume of electronics, to alternative power source that is lightweight and flexible. As discussed in chapter 1, energy harvesting, which scavenges energy from ambient energy sources is a fast-emerging solution to realizing battery-less wearable systems. In this work, the Si solar cell is suggested as an energy harvesting system to provide power to other Si circuit components on the same chip.

Si based electronics provide high performance as it is the mainstream platform of current semiconductor industry. However, owing to its brittle nature, Si possesses inherent difficulties for flexible and wearable electronics applications. Various approaches have been reported for realization of Si electronics on flexible platforms. The first approach is direct fabrication of Si devices on flexible substrates.[1,2] However, this approach is restricted to amorphous Si and not

feasible for monocrystalline Si which yields higher performance than amorphous Si. Second is the fabrication of electronics on conventional rigid Si wafers and transferring to flexible substrates. Transfer printing, where devices fabricated on a rigid surface are later printed to a flexible substrate using a polydimethylsiloxane (PDMS) stamp, is one of the most popularly used transferring method.[3,4] Chemical etching[5] or back grinding[6] have been also suggested as approaches to thin down the thick Si substrate.

Silicon on Insulator (SOI) wafers with a device layer as thin as few tens of micrometers to few hundred nanometers, are readily applicable for thin film electronics when the device layer is released from the thick bulk layer. Moreover, compared to conventional Si wafers, SOI wafers offer advantages of lower parasitic capacitance, resistance to latch up, and lower leakage current which leads to high electronic performance.[7] Here, SOI wafers were utilized as base/donor substrates to enable fabrication of self-powered flexible and wearable electronics.

This study aims to demonstrate the development of self-powered flexible and wearable electronics by solar energy harvesting where the Si solar cells are utilized to power up the Si metal-oxide-semiconductor field-effect transistor (MOSFET) circuits that are on the same Si layer. First, release of 10 μm thick Si membrane from an SOI wafer and transfer to flexible polymer substrates are investigated. Fabrication and characterization of Si solar cells and MOSFETs on both SOI wafers and after transferred to flexible substrates were performed. Side-to-side fabrication of Si solar cells and MOSFETs on the same Si layer is demonstrated to create self-powered flexible and wearable electronics. Finally, their application to a voltage-controlled oscillator composed of Si solar cells and MOSFETs is proposed.

3.2 Release of Si Membrane and Transferring to Flexible Substrates

SOI wafers consisted of a thin device layer (Si(100), p-type, boron doped, 0.01–0.02 Ω · cm, t_{Device}=10 μm), a buried oxide (BOX) layer (t_{BOX}=1 μm) and a handler layer (Si(100), p-type, boron doped, 1–10 Ω · cm, $t_{Handler}$=450 μm) were used. (**Figure 3.1**) The solar cells were fabricated on the device layer. Details of solar cell device fabrication are described in chapter 2.

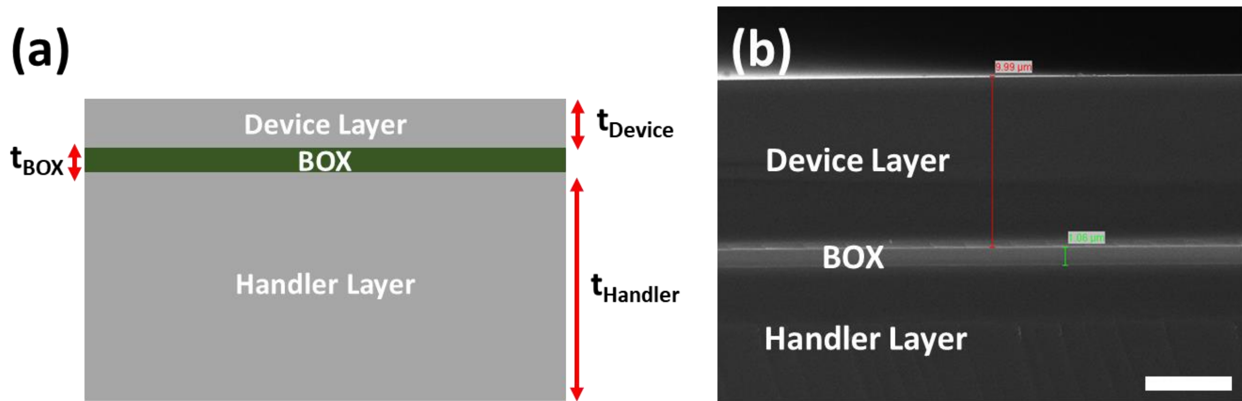


Figure 3.1 (a) A schematic illustration of cross-section view of an SOI wafer (not to scale). (b) A magnified cross-sectional SEM image of an SOI wafer. Scale bar is 5 μm.

Many researchers have demonstrated releasing thin Si membrane from SOI wafers by wet-chemical etching,[8] plasma etching,[9] gas phase etching[10] and chemical mechanical polishing.[11] In this work, chemical, plasma and gas phase etchings were investigated as methods for Si membrane release from an SOI wafer.

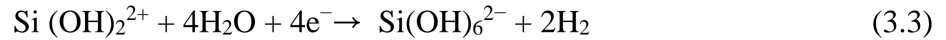
3.2.1 TMAH Si Etching

Potassium hydroxide (KOH) and Tetramethylammonium hydroxide (TMAH) are well known for Si anisotropic etching. After formation of free-standing structure of device layer by anisotropic etching of handler layer, device layer can be released by the removal of BOX[12] or

transfer printing method.[8] Here, TMAH was chosen over KOH owing to its low etch rate of SiO_2 and absence of alkali ions.[13] The reaction between TMAH and Si can be described by following steps,

$$(CH_3)_4NOH \rightarrow (CH_3)_4N^+ + OH^- \quad (3.1)$$

$$Si + 2OH- \rightarrow Si(OH)22+ + 4e^- \quad (3.2)$$



$$Si\,(OH)_2^{2+} + 4H_2O + 4e^- \rightarrow Si(OH)_6^{2-} + 2H_2 \quad (3.3)$$

where hydroxyl ions from TMAH react with Si atoms at the surface and form oxidized silicates.[13] Oxidized silicates then produce soluble silicic acid with hydrogen gas as a byproduct. Thermally grown wet-SiO_2 ($t_{SiO2,thermal}$=505 nm), plasma-enhanced chemical vapor deposited (PECVD) deposited SiO_2 ($t_{SiO2,PECVD}$=520 nm) and SiN_x (t_{SiNx}=510 nm) layers were tested as hard masks which protect the Si device layer being etched under TMAH Si anisotropic etching from the backside of the handler layer. Each hard mask was deposited on top of the SOI samples (1.5 cm×1.5 cm, $t_{Handler\ Si}$=450 µm) and backside of the SOI wafers were etched by plasma etching to ensure complete removal of oxide layers that were formed on the backside of the SOI wafers during thermal oxidation or PECVD deposition. The SOI wafers were immersed into 25 wt% TMAH at 90 ^{o}C. The thicknesses of each hard mask and etched Si from backside of the SOI wafers were measured by a surface profiler (Dektak 150, Veeco Instruments Inc) (**Table 3.1**). The etch rate of the hard mask was the slowest for the wet-thermal oxide layer, then PECVD SiN_x layer and PECVD SiO_2 layer was the fastest. However, the Si etched surface morphologies were found on all the hard masks, which can result in potential damage of the fabricated devices on top of SOI wafers (**Figure 3.2**).

Table 3.1 Thickness of wet-thermal SiO_2, PECVD deposited SiO_2 and SiN_x hard masks and etched Si under TMAH etching.

Total Etch Time (hr)	Wet-thermal SiO_2		PECVD SiO_2		PECVD SiN_x		Etched Si	
	Thickness (nm)	Etch Rate (nm/hr)	Thickness (nm)	Etch Rate (nm/hr)	Thickness (nm)	Etch Rate (nm/hr)	Thickness (µm)	Etch Rate (µm/hr)
0	505	-	520	-	510	-	-	-
1	487	18	455	65	473	37	55	55
2	472	15	410	45	433	40	99	44
3	462	10	373	37	420	13	128	29
5	446	8	322	25.5	361	29.5	220	46
6.5	427	8.4	265	38	313	32	280	40

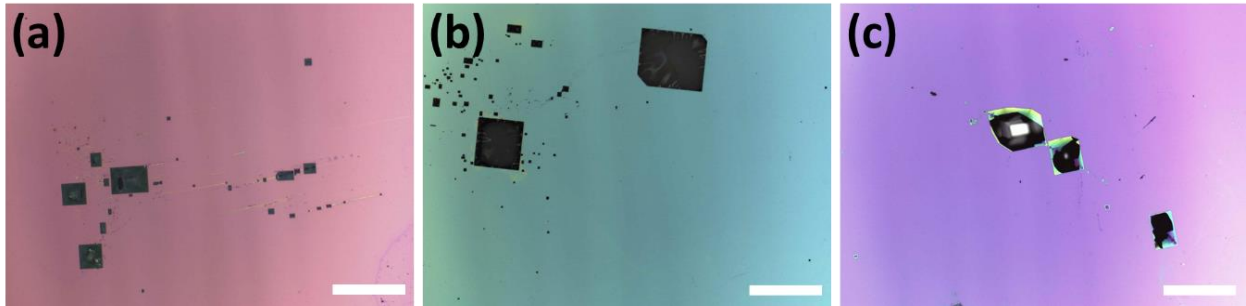


Figure 3.2 Top-view optical microscopic images of (a) wet-thermal SiO_2, (b) PECVD deposited SiO_2, and (c) PECVD deposited SiN_x hard masks on top of the SOI wafers after 5 hrs of TMAH etching. Scale bars are 500 µm.

Parylene C, known for its chemical inertness and stability in bases,[14] was also tested as a hard mask for TMAH Si etching. A parylene C layer ($t_{Parylene\ C}$=2 µm) was deposited conformally by chemical vapor deposition (PDS 2010, SCS coatings) on both top and bottom sides of the SOI wafer (1.5 cm×1.5 cm, $t_{Handler\ Si}$=450 µm) From the backside of the SOI wafer, the parylene C layer was removed by O_2 plasma etching to make an etch opening, expose the Si surface of the handler layer and enable TMAH etching from the backside. After 6 hrs of immersion of the SOI wafer in 25 wt% TMAH at 90 °C, no significant damage on the paryelene C was observed, but TMAH solution penetrated at the interface of the Si and parylene C and through the parylene C

layer (**Figure 3.3**). Improvement of adhesion of parylene C layer on Si wafer needs to be further investigated to avoid TMAH penetration and peeling off of parylene C layer.[14]

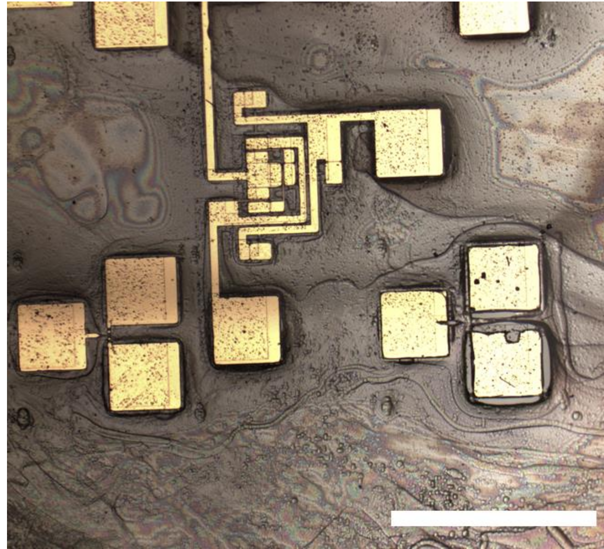


Figure 3.3 Top-view optical microscopic image of a top side of the SOI wafer covered by parylene C after 6 hrs of TMAH etching, showing TMAH penetration. Scale bar is 500 μm.

3.2.2 RIE Si Etching

As discussed in Chapter 2, SF_6 gas is used for anisotropic etch of Si when combined with C_4F_8 polymer-producing gas. On the other hand, SF_6 can etch Si isotropically in the absence of C_4F_8 gas.[15] For isotropic Si plasma etching, we used a mixture of SF_6 (80 ccm) and Ar (10 sccm) under RIE and ICP power of 200 W and 1500 W, respectively (Si etch rate = ~3 μm/min). Argon gas was added for stabilization of plasma as well as enhancement of etch rate caused by ion bombardment of the surface.[16] After the front contact formation of the SOI solar cell, polyimide (PI 2610, HD MicroSystems LLC) was spun-cast on the front side of the wafer and soft-baked at 170 ^oC for 5 min followed by curing at 300 ^oC for 30 min ($t_{Polyimide}$ = 2 μm). Then the whole SOI sample (1 cm×1 cm) was flipped and the surface of the polyimide layer was temporally bonded to

a 4-inch Si carrier wafer by a photoresist (NR9-1500PY, Futurrex) and soft-baked at 150 °C for 1 min. The 4-inch Si carrier wafer was loaded to the ICP-RIE system (Plasmalab 100, Oxford Instruments) and the thick handler layer ($t_{Handler}$=450 μm) of the SOI wafer was etched by ICP-RIE etching from the backside, where BOX (t_{BOX}=1 μm) acted as an etch-stop layer. After the handler layer is completely etched, the BOX layer was etched by buffered oxide etchant (BOE, 6:1) consequently to expose the p-Si layer of the device layer (t_{Device}=10 μm) of the SOI wafer. After an Al (100 nm) p-contact layer was deposited on the p-Si layer, another layer of polyimide was spun-cast on the backside of the SOI wafer and cured as a stress neutral plane. Partial openings were made on top of front- and back-contacts by etching polyimide with O_2 plasma etching to access probing for device characterization. As shown in **Figure 3.4**, the SOI solar cells embedded in polyimide layers were shown to conform to a curved surface and a human skin, exhibiting their potential for application to flexible and wearable electronics.

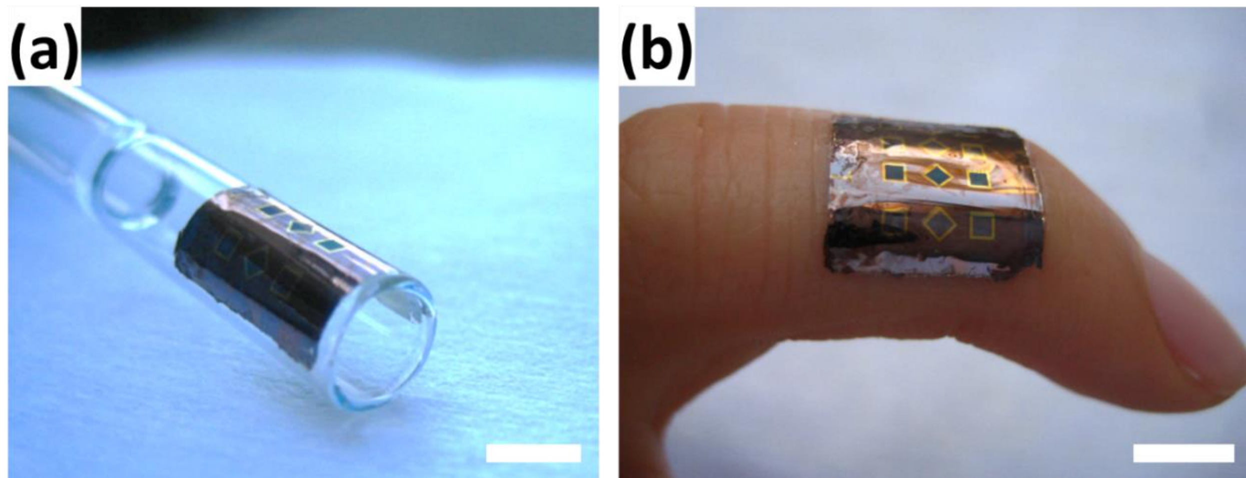


Figure 3.4 Photos of SOI solar cells embedded in polyimide layers making contacts on (a) a curved surface and (b) a human skin. Scare bars are 5 mm.

3.2.3 XeF_2 Si Etching

Xenon difluoride (XeF_2) Si etching undergoes following reaction,

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4 \quad (3.4)$$

where XeF_2, adsorbed at the Si surface, dissociates, and reacts with the Si surface to form SiF_4. Then both volatile SiF_4 and dissociated Xe are pumped away.[17] XeF_2 does not etch polymer or organic films, making parylene C a good hard mask for XeF_2 Si etching process.[18] A parylene C layer ($t_{Parylene\ C}$=2 μm) was deposited conformally by chemical vapor deposition (PDS 2010, SCS coatings) on both top and bottom sides of the SOI wafer (2 cm×2 cm, $t_{handler}$=450 μm). From the backside of the SOI wafer, part of the parylene C layer was removed by O_2 plasma etching to make an etch window, expose the Si surface of the handler layer and enable XeF_2 etching from the backside. The SOI wafer was loaded into the XeF_2 etcher (Xetch e1, Xactix, Inc.) with the backside of the SOI wafer facing upwards. Each etch cycle was for 15 s under XeF_2 pressure of 3.5 T. XeF_2 Si etch rate differs depending on the location of the wafer on the stage of the XeF_2 etcher, lowest at the center and highest at the edge of the stage.[17] Though XeF_2 Si etching has high etch selectivity against SiO_2, when exposed under long etch cycles, the BOX layer can be etched away as well. To avoid the BOX etch stop layer being fully etched, small etch window (0.65 cm×0.65 cm) was first opened (**Figure 3.5 (a)**). After 50 cycles of XeF_2 etching, additional etch window (1.45 cm×1.45 cm) was consequently opened. As shown in **Figure 3.4 (c)** and **(d)**, BOX starts to appear from each corner of the etch window. XeF_2 etch continues until BOX is fully exposed (**Figure 3.5 (e)**). BOX layer is then removed by BOE, exposing bottom surface of the device layer (**Figure 3.5 (f)**). On part of the device layer, the Al layer (100 nm) which acts as a p-contact layer of Si solar cell as well as a hard mask against XeF_2[17] is deposited by e-beam evaporation (**Figure 3.5 (g)**). The Al layer protects region of interest during additional XeF_2 etching to remove unwanted Si and expose

the top parylene C layer (**Figure 3.5 (h)**). The backside was coated with another layer of parylene C ($t_{Parylene\ C}$=2 μm) for a stress neutral plane. Finally, the Si membrane was released by cutting the paylene C layer that is anchoring the Si membrane to the handler layer by a razor blade (**Figure 3.5 (i)**).

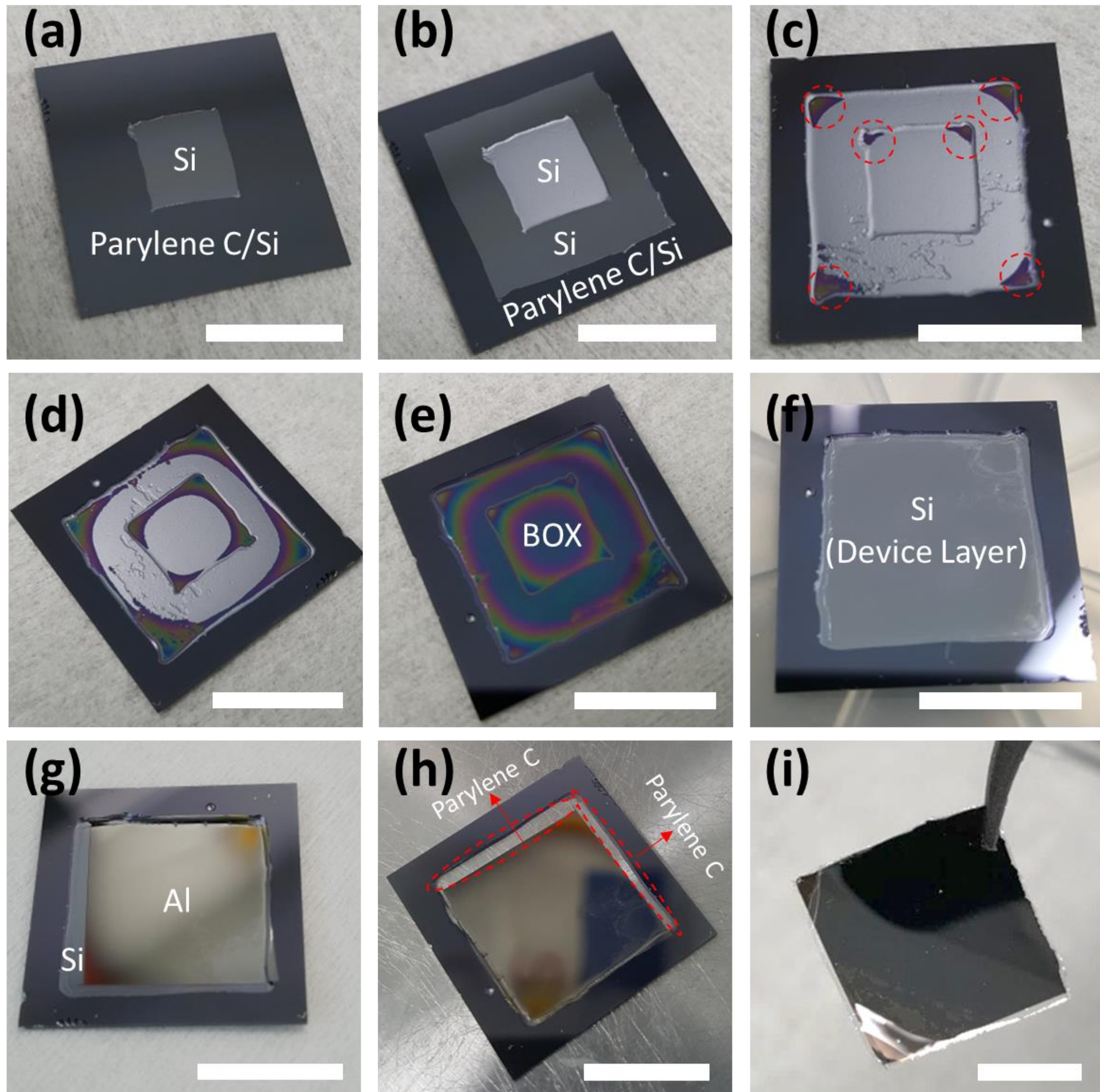


Figure 3.5 Photos of Si membrane release process from an SOI wafer. (a) Parylene C opening on the backside of the SOI. (b) After 50 cycles of XeF_2 etching followed by additional parylene C opening. (c) After 400 cycles of XeF_2 etching. Red dotted circles indicate exposed BOX layer. (d) After 450 cycles of XeF_2 etching. (e) After 500 cycles of XeF_2 etching showing full exposure of BOX layer. (f) After BOE etching of BOX layer, exposing Si device layer. (g) Al layer deposition on the part of the backside of the Si device layer. (h) After 5 cycles of XeF_2 etching. Red dotted circles indicate parylene C layer. (i) Front side view of released Si membrane. Scale bars are 1 cm.

3.3 Planar Si and Si Microwire Solar Cells on SOI Wafers

3.3.1 10 μm Thick Planar Si cell on an SOI Wafer

A planar solar cell was fabricated on an SOI wafer. The emitter n-Si layer was formed by SOD with phosphorus SOD source (P509, Filmtronics, Inc.). After removing SOD residues by BOE, a layer of SiN_x (t_{SiNx}=80 nm) was deposited by PECVD as a passivation layer and anti-reflective coating. Contact widow was opened by RIE etching of SiN_x followed by Ti/Au (50/100 nm) ohmic contact deposition. A parylene C layer ($t_{Parylene\ C}$=2 μm) was deposited on top of the device layer. Since parylene C layer is highly transparent, light absorption is merely affected even it is covering the active area of the solar cell.[19] The handler layer and the BOX layer underneath the planar cell were removed by XeF_2 and BOE etching, respectively, as described above, followed by deposition of an Al p-contact layer on the back side of the device layer (**Figure 3.6 (a)**). Another layer of parylene C ($t_{Parylene\ C}$=2 μm) was deposited on the backside of the device layer as a stress neutral plane. On top of each n-contact and p-contact, the parylene C was partially opened by O_2 plasma etching to create openings for probing. The Si membrane was released from the SOI handler layer resulting in a free-standing structure (**Figure 3.6 (b)**). To examine the effect of Si thickness on solar cell performance, a Si planar cell and a Si microwire (SiMW) cell were fabricated on a thick bulk Si (t_{Si}=525 μm) substrate with comparable base doping concentration (0.02–0.04 Ω · cm) and same solar cell configuration were compared with the planar cells on the SOI wafer (0.01–0.02 Ω · cm). The height, diameter, and side-to-side spacing of circular SiMWs on bulk Si were 10 μm, 1.5 μm, and 2.5 μm, respectively. **Figure 3.6 (c)** shows the structure of each cell. 8.02 % of power conversion efficiency (η) was obtained from the 10 μm thick SOI planar cell, yet 25.9% lower than that of the bulk Si planar cell, resulting from lower values on both J_{sc} and V_{oc} of the SOI planar cell. Lower V_{oc} for the SOI planar cell contradicts our expectation that

thin Si cell can exhibit higher V_{oc} as bulk recombination reduces with decreasing the Si thickness. We attribute low V_{oc} due to poor rear surface passivation of the SOI planar cell, as the rear surface recombination becomes more critical factor for limiting the efficiency for thin Si solar cells.[20] This can be improved by implementing local metal contacts with rear surface passivation.[20] Beside surface recombination loss, low J_{sc} for the 10 μm thick SOI planar cell is owed to lower light absorption of thinner Si thickness (**Table 3.2**). Due to low absorption coefficient of Si at long wavelength, reduction in absorption of long wavelength photons occurs with decreasing the Si thickness. When comparing bulk Si planar solar cell with SiMW on bulk Si cell, J_{sc} was increased by 37.6% due to increased light absorption from the light trapping effect of SiMWs. This implies light absorption of SOI cells can be improved by introducing micro- or nano-structures on the surface of SOI wafer.

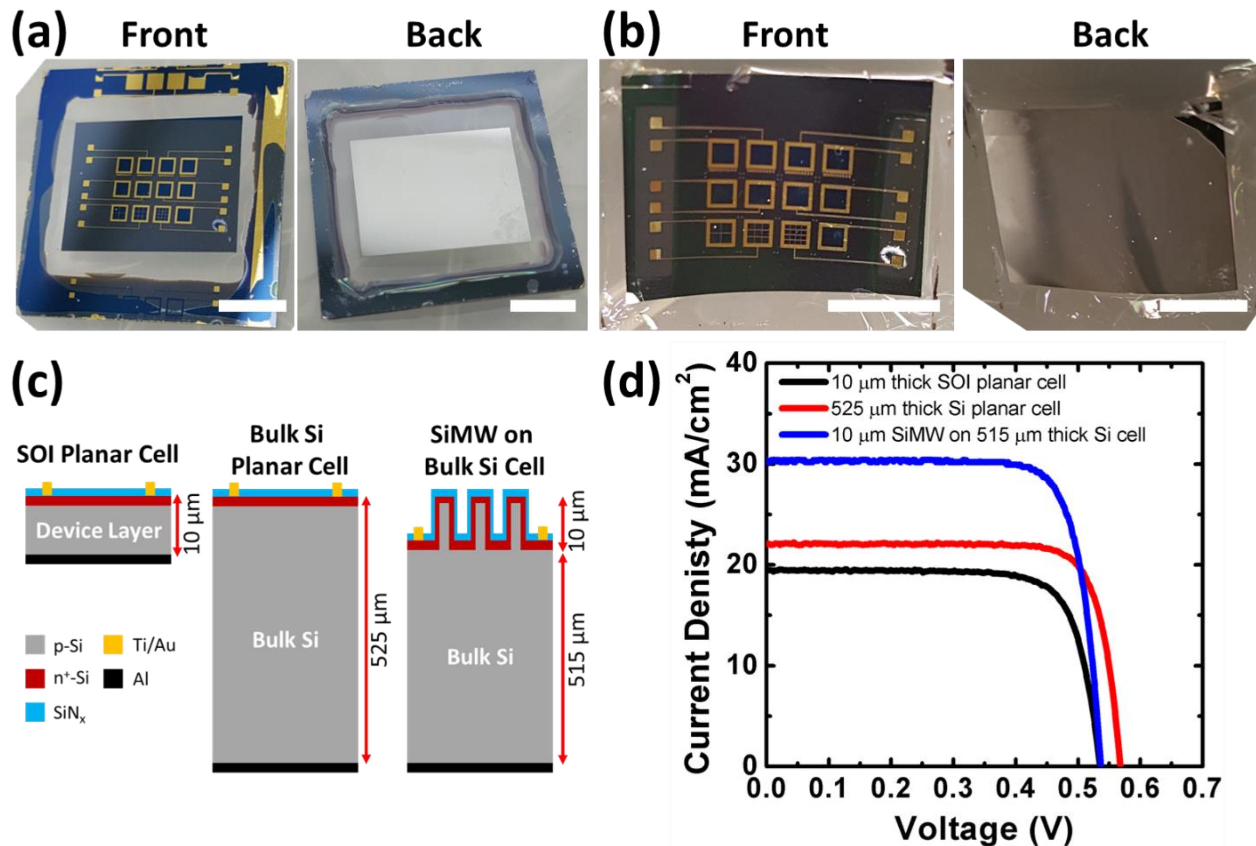


Figure 3.6 (a) Photos of 10 µm thick SOI planar cells anchored to the SOI handler layer. Scale bars are 5 mm. (b) Photos of free-standing 10 µm thick SOI planar cells. Scale bars are 5 mm. (c) Schematic illustration of 10 µm thick SOI planar cell, 525 um thick bulk Si planar cell, and 10 µm tall SiMW cell on a 515 µm thick bulk Si wafer (cross-section view, not to scale). (d) Light *J–V* characteristics of each cell depicted in (c).

Table 3.2 Measured solar cell performances of 10 µm thick SOI planar cell, 525 um thick bulk Si planar cell, and 10 µm tall SiMW cell on a 515 µm thick bulk Si wafer.

Device	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
10 µm thick SOI planar cell	19.4	0.535	77.1	8.02
525 µm thick bulk Si planar cell	22.1	0.567	80.7	10.1
10 µm SiMW cell on 515 µm thick bulk Si	30.4	0.537	79.2	12.9

3.3.2 All-Front-Contact SOI Planar and SiMW Cell

To improve the SOI solar cell performance, SOI wafers with moderate doping concentration ($\rho_{\text{Device Layer}}$ =0.5–0.75 $\Omega \cdot$cm, corresponding doping concentration=2.0x10^{16} – 3.2x10^{16} atoms/cm^3) was chosen as a starting substrate for SOI solar cells. Increasing the doping concentration lowers the saturation current but at the same time, the minority carrier diffusion length and minority carrier lifetime decreases. Thus, moderate doping concentration for the base of solar cell was found to be optimal for high solar cell performance as discussed in chapter 2. SOI wafers consisting of a thin device layer (Si(100), p-type, boron doped, 0.5–0.75 $\Omega \cdot$cm, t_{Device}=10 μm), a buried oxide (BOX) layer (t_{BOX}=250 nm) and a handler layer (Si(100), p-type, boron doped, 1–5 $\Omega \cdot$cm, $t_{Handler}$=400 μm) were used in this work. A planar cell and SiMW cell were fabricated on the device layer of SOI wafers (**Figure 3.7 (a)**). SiMWs were fabricated by RIE etching with Ni as dry etch mask. The height, diameter, and side-to-side spacing of circular SiMW were 9.5 μm, 1.5 μm, and 2.5 μm, respectively. To simplify fabrication process such as interconnection for connecting multiple solar cells and integration with MOSFETs, both ohmic contacts of p-Si and n-Si of solar cells were formed at the top side of the device layer. Due to thin thickness of the device layer (10 μm), carriers generated at the deeper regions of the Si have higher chance to be collected at the front contacts before they recombine. It is worth noting that the BOX layer (t_{BOX}=250 nm) underneath the device layer acts as a passivation layer suppressing surface recombination on the backside of the device layer. Light *J–V* characteristics were measured for each cell after fabrication (**Figure 3.7 (b)**). Interestingly, J_{sc} was reduced by 23.6% from the SOI planar cell to the SOI SiMW cell (**Table 3.3**), which contradicts our expectation that SOI cell with SiMW will have higher J_{sc} than that of SOI planar cell as a result of light trapping effect of SiMW. To elucidate the origin of the optical losses, external quantum efficiency (EQE) was measured and

compared for each cell (**Figure 3.7 (c)**). The SOI SiMW cell exhibits higher EQE values at shorter wavelength region (300–500 nm) due to superior light absorption of SiMWs at the surface. However, in the 500–900 nm range, EQE values of the SOI SiMW cell were drastically reduced compared to the SOI planar cell which indicates that the long wavelength was not efficiently trapped and absorbed by SiMWs. This explains the deteriorated J_{sc} for the SOI SiMW cell considering the fact that the long wavelength red light region contributes most to the solar cell efficiency.[21] Due to presence of gaps between SiMWs, total Si volume within the 1×1 mm^2 active cell area was reduced by 68.1% from the SOI planar cell to the SOI SiMW cell which leads to reduced number of absorbed photons. The optimal height, diameter and side-to-side spacing of SiMW that can increase absorption at short wavelength and at the same time effectively trap long wavelength light needs to be further studied. Introducing Si nanostructures on the surface with minimum decrement of the total volume of absorber can be also suggested as an alternative method.[22]

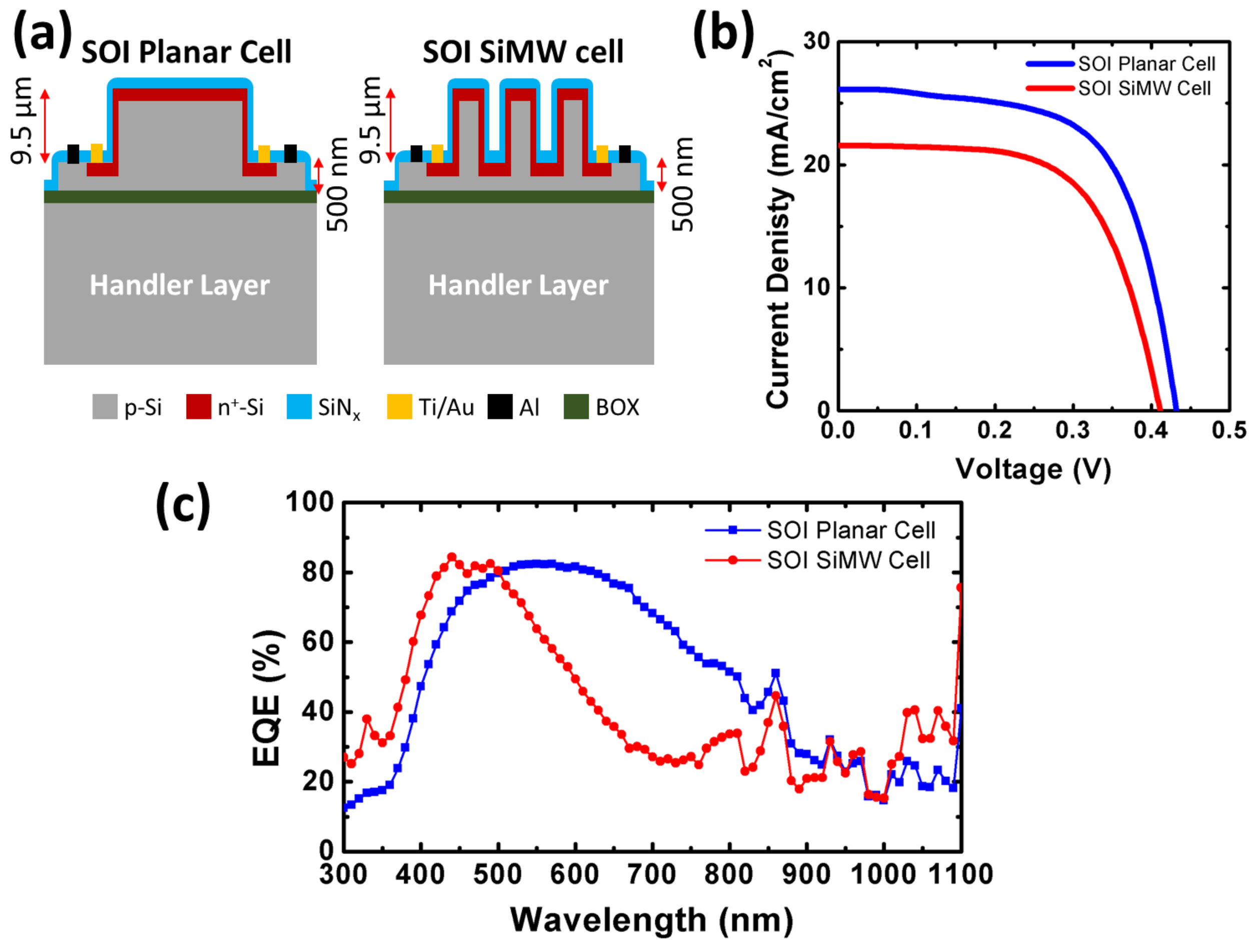


Figure 3.7 (a) Schematic illustration of an SOI planar cell and an SOI SiMW cell (cross-section view, not to scale). (b) Light *J–V* characteristics of each cell depicted in (a). (c) EQE of each cell depicted in (a).

Table 3.3 Measured solar cell performances of SOI planar cell and SOI SiMW cell.

Device	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
SOI planar cell	25.7	0.432	65.5	7.27
SOI SiMW cell	20.8	0.428	66.2	5.91

3.3.3 High Selective Doping Underneath the Metal Contact Region

As the thickness of the Si solar cell decreases, bulk recombination reduces and surface and contact recombination become the dominant recombination loss mechanism.[6,23] Surface recombination can be suppressed by applying SiN_x passivation layer on the front surface of the solar cell and with the presence of a BOX layer on the backside of the device layer. Heavy doping beneath the metal contacts can lower the contact resistance and mitigate contact recombination by repelling minority carriers away from the contact area. After formation of the n-layer in an SOI planar cell, the region below p-contact was selectively highly doped by boron SOD source (B155, Filmtronics, Inc.) to obtain a higher doping concentration. An SiO_2 mask (t_{SiO2}=500 nm) was deposited by PECVD as a diffusion mask layer against boron proximity doping which covers everywhere except the region under the p-contact. Boron doping parameters and corresponding sheet resistances after boron doping were tested on the same type of SOI wafers (p-type, 0.5–0.75 $\Omega \cdot$ cm) before solar cell fabrication and the results are summarized in **Table 3.4**. We chose 950 ^{o}C, 60 s as the boron doping tempeature and time to create a p^+-layer under the p-contact region of the Si solar cell. Solar cell perfomances of SOI planar cells with and without p^+-layer were measured and compared (**Figure 3.8 (b)**). We found a clear increase in J_{sc}, V_{oc}, and FF when the high p-doping layer was introduced underneath the p-contact region and correspondingly the power conversion efficiency, η, resulting in an η of 13.1% for 10 μm thick SOI planar cell with high p-doping layer (**Table 3.4**).

Table 3.4 Doping parameters and sheet resistance of p-Si before and after doping with B155.

Doping Parameters (Temperature, Time)	Sheet Resistance Before Doping [Ω/□]	Sheet Resistance After Doping [Ω/□]
950 °C, 60 s	953	302
975 °C, 60 s		249
1000 °C, 60 s		191
1100 °C, 60 s		37.7

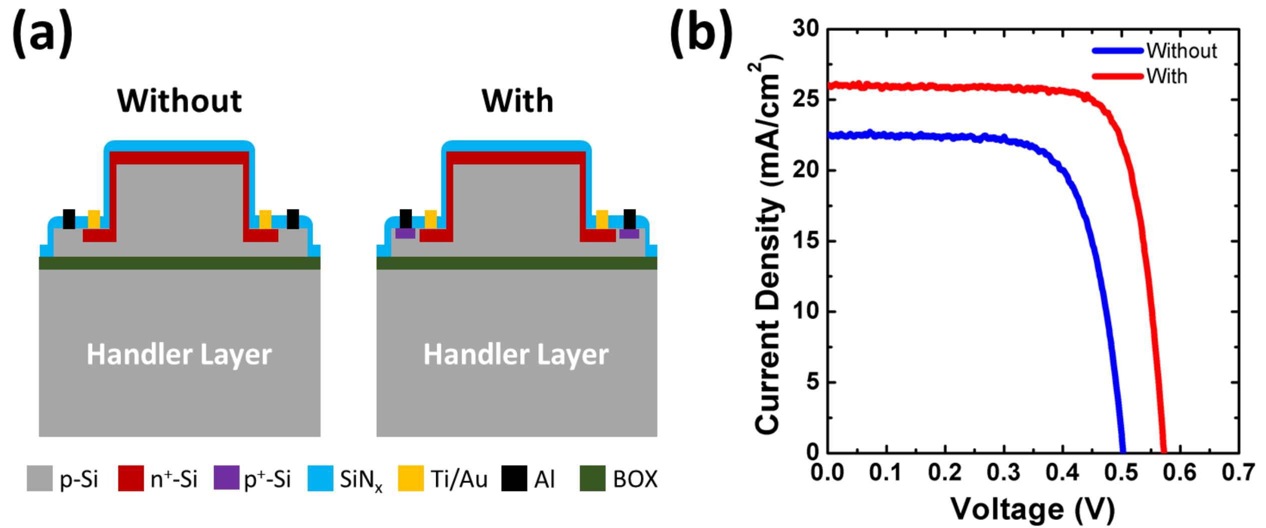


Figure 3.8 (a) Schematic illustration of an SOI planar cell with and without p^+-layer underneath the p-contacts (cross-section view, not to scale). (b) Light *J–V* characteristics of each cell depicted in (a).

Table 3.5 Measured solar cell performances of SOI planar cells with and without high doping underneath the p-contact.

Device	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
Without p^+-layer	22.5	0.503	70.9	8.03
With p^+-layer	30.3	0.573	75.4	13.1

3.3.4 Series-connection of Solar Cells on an SOI Wafer

Multiple SOI planar cells were connected in series to obtain high output voltage that can meet the circuit requirement for operation when integrated with other Si circuit components. For series-connection, minimizing leakage current in interconnection and mismatch losses is critical

for maximizing the power generated from solar cells. For the latter, a uniform doping of emitter over the wafer is the key. To avoid leakage current, applying an effective insulation layer is essential. We selected parylene C as the insulation layer. It is worth noting that the parylene C insulation layer also serves as a flexible substrate when the device layer is released from the handler layer of SOI wafer, as well as a protection layer against XeF_2 etching as discussed above. After fabrication of SOI planar cells, an insulating layer, a layer of parylene C ($t_{Parylene\ C}$=3 μm) was deposited on top of the device layer. Via openings were partially opened on top of the p-contact and n-contact by O_2 plasma etching. Ti/Au layer was deposited on top of the via openings and the parylene C layer by sputter to interconnect n-contact of one cell to p-contact of the other cell as shown in **Figure 3.9 (a), (b)**. **Table 3.6** summarizes solar cell performances performed on each cell before and after interconnection. V_{OC} of series-connected cells after interconnection was equivalent to sum of the V_{OC} of individual cells without any degradation, which indicates the parylene C insulation layer effectively passivated the sidewalls of device layer, not creating any unwanted leakage current paths. This result demonstrates that our fabrication method is scalable and can expand to configurations with larger number of cells and flexible to various circuit requirements.

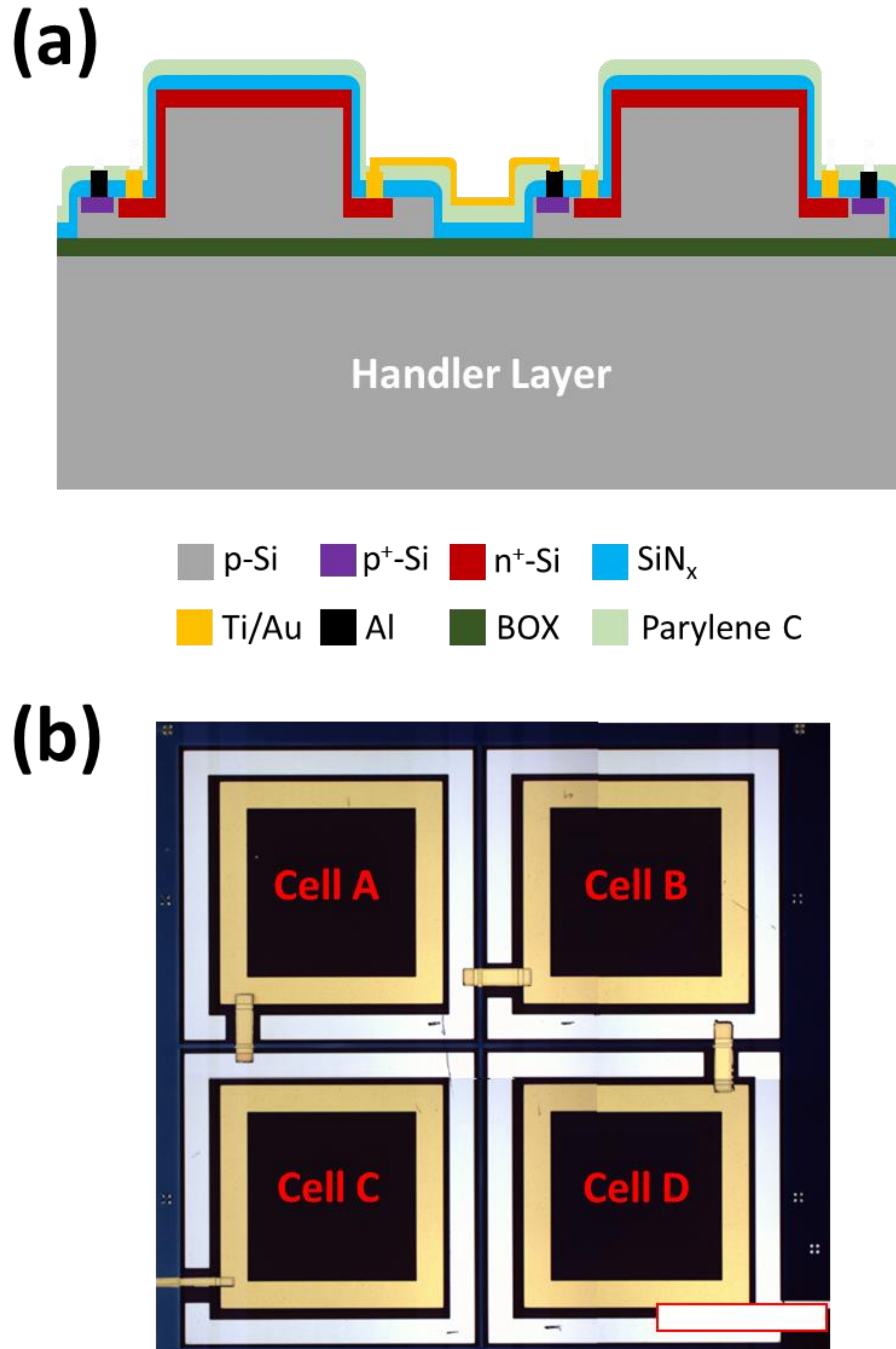


Figure 3.9 (a) Schematic illustration of two SOI planar cells connected in series (cross-section view, not to scale). (b) A top-view optical microscopic image of SOI planar cells connected in series. Scale bar is 1 mm.

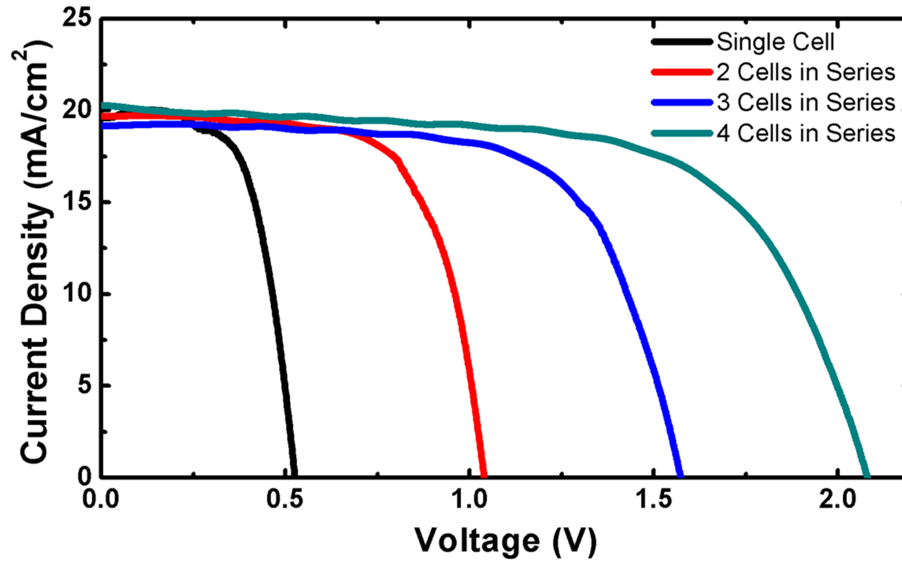


Figure 3.10 Light *J–V* characteristics of single and serially-connected planar SOI cells.

Table 3.6 Measured solar cell performances of a single SOI planar cell and multiple SOI planar cells connected in series.

Device	J_{sc} [mA/cm^2]	V_{oc} [V]	*FF* [%]	η [%]
Cell A	20.3	0.526	61.5	6.56
Cell B	19.9	0.508	58.1	5.88
Cell C	19.8	0.520	53.8	5.54
Cell D	20.4	0.528	58.5	6.31
Cell A, C connected in series	20.1	1.039	66.7	7.00
Cell A, C, D connected in series	19.3	1.573	67.1	6.77
Cell A, B, C, D connected in series	20.1	2.080	64.7	6.73

3.4 Monolithic Integration of Solar-Powered Oscillators

3.4.1 MOFETs on an SOI wafer

We fabricated n-channel MOSFETs on an SOI wafer with the same doping procedure for solar cells. After thinning down the device layer (t_{Device}=10 μm) of the SOI to 500 nm by RIE etching with photoresist as an etch mask, source and drain junctions were selectively formed by proximity doping with phosphorus SOD source (P509, Filmtronics, Inc.) using a SiO_2 layer (t_{SiO2} = 300 nm) as a diffusion mask. After removing SOD residues and the SiO_2 diffusion mask by BOE, a layer of SiN_x (t_{SiNx}=60 nm) was deposited by PECVD as a gate dielectric layer. We chose 60 nm thick SiN_x as a gate dielectric layer so that it can also be used as passivation and anti-reflective coatings for solar cells, as discussed above. After RIE etching of SiNx for contact window opening, Ti/Au (50/150 nm) was deposited on top of the n^+-Si as an ohmic contact layer. Finally, Ti/Au (50/150 nm) was deposited as a gate metal (**Figure 3.11 (a), (b)**). The gate length (L_G) and gate width (W_G) of the n-channel MOSFETs is 4 μm and 40 μm, respectively. After DC characteristics measurements (**Figure 3.12 (a)-(c)**), the device release from the handler layer was performed. After a parylene C layer ($t_{Parylene\ C}$=5 μm) was deposited on top of the device layer, the handler layer and the BOX were removed by XeF_2 and BOE etching, respectively, as described earlier. Another layer of parylene C layer ($t_{Parylene\ C}$=5 μm) was deposited on the back side of the device layer as a stress neutral plane (**Figure 3.11 (a), (c)**). On top of the source, drain, and gate metals, the parylene C was partially opened by O_2 plasma etching to make openings for probing. DC characteristics of n-channel MOSFETs were measured when the device is on the parylene C, after release from the SOI wafer (**Figure 3.12 (d)-(f)**). The measured parameters of MOSFET on the SOI and on the parylene C are summarized in **Table 3.7**. The subthreshold swing (S) was obtained from the I_D–V_G curve for the device before (373 mV/dec) and after release (427 mV/dec). The

relatively large S is due to large gate capacitance owing to the thick gate insulation layer (t_{SiNx}=60 nm). The effective mobility μ_{eff}, increased from 91.5 $cm^2/V \cdot s$ to 118 $cm^2/V \cdot s$ after the device is released and embedded in the parylene C. The increased mobility is due to compressively strained MOSFET channel when the device is embedded in the parylene C.[10] Due to the thermal mismatch between parylene C layer and Si, after parylene C layer deposition on Si, Si layer is subjected to compressive strain, [24] which was also found from our device as shown in **Figure 3.11 (c)** (convex surface). The strain on Si also affected threshold voltage (V_{th}), obtained from the I_D–V_G curve, showing a shift from −1 V to −1.5 V after the device was released.[25] The performance degradations such as increased S and decreased I_{max}/I_{min} after the device release are likely due to stress induced at the interface of SiN_x/Si which increased the gate leakage current. Further studies including examination of the device on a curved surface with different bending radii and attaching on a more rigid yet flexible matter such as PDMS to investigate whether the performance degradation is recoverable, can be suggested.

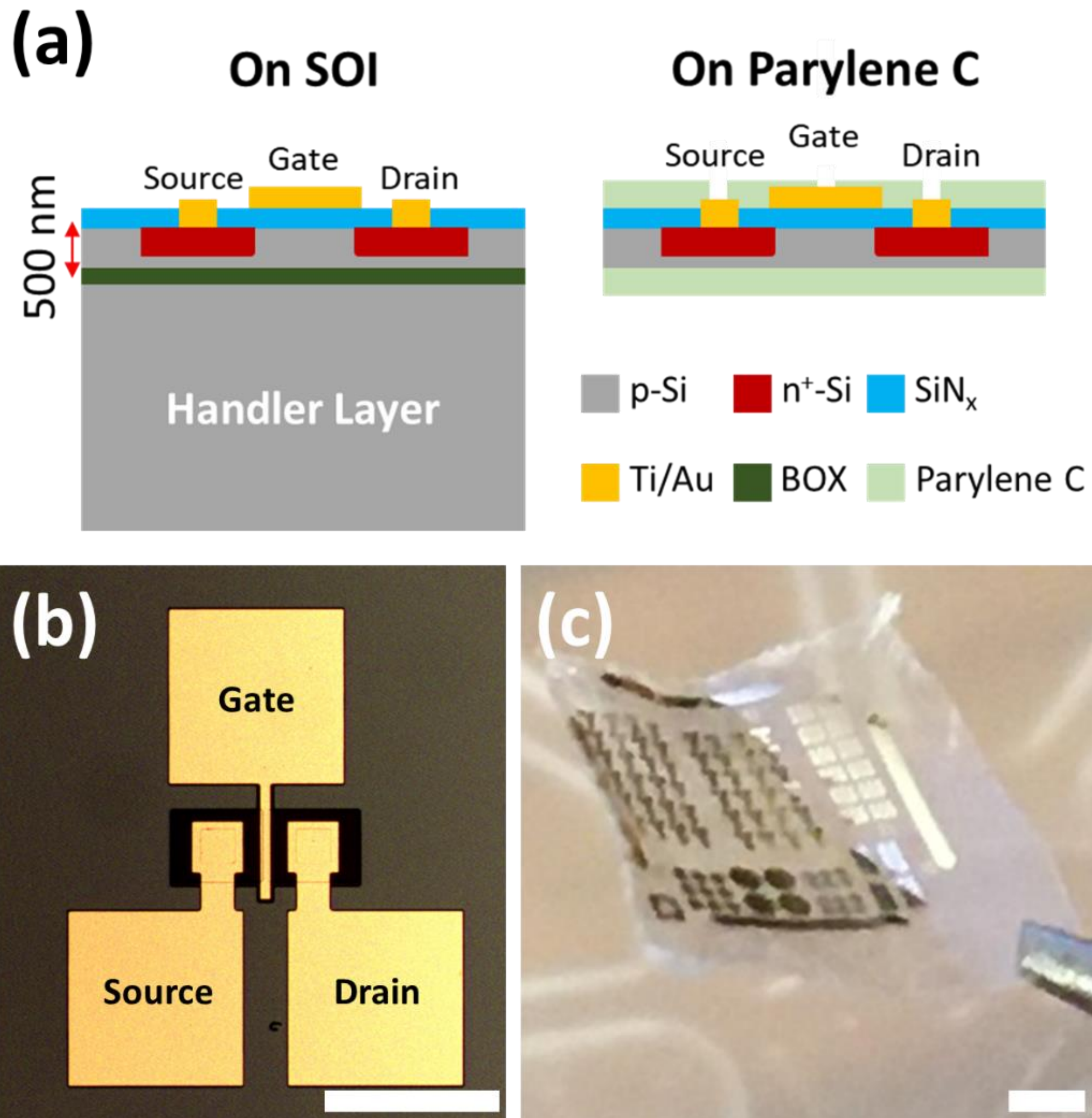


Figure 3.11 (a) Schematic illustration of MOSFET on an SOI wafer before release and after release, on parylene C (cross-section view, not to scale). (b) Top-view optical microscopic image of a MOSFET on an SOI wafer before release. Scale bar is 100 µm. (c) A photo of MOSFETs released from an SOI wafer and embedded in a parylene C layer. Scale bar is 1 mm.

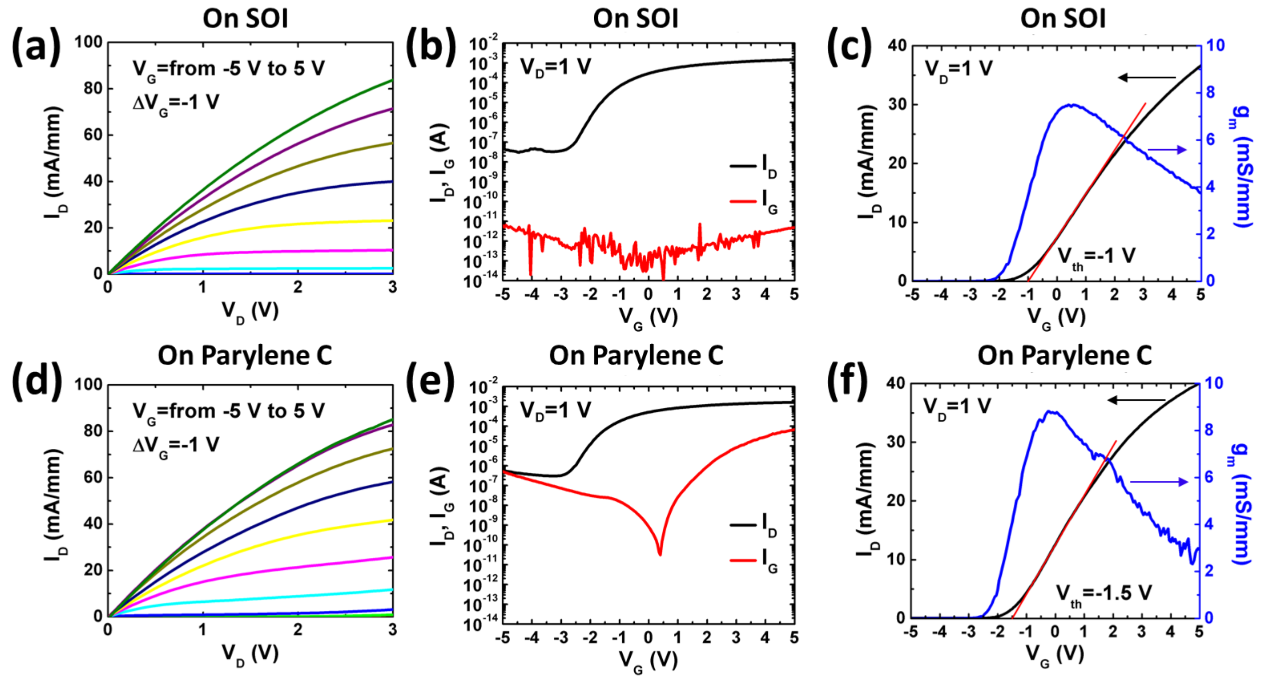


Figure 3.12 Measured DC characteristics of n-MOSFET on the SOI wafer ((a)-(c)) and on the parylene C layer ((d)-(f)). (a), (d) Output I_D–V_D characteristics at different gate voltages in steps of 1 V. (b), (e) Log-scale transfer characteristics (I_D–V_G) and gate leakage (I_G–V_G) at V_D = 1 V. (c), (f) Linear scale transfer characteristics (I_D–V_G) and transconductance as a function of gate bias (g_m–V_G) at V_D = 1 V.

Table 3.7 Measured device characteristics for n-channel MOSFETs on SOI and on parylene C.

Device	V_{th} [V]	S [mV/dec]	μ_{eff} [cm^2/V·s]	I_{max}/I_{min}
On SOI	−1	373	91.5	3.14×10^4
On Parylene C	−1.5	427	118	2.76×10^3

3.4.2 AC Characteristics of Si Solar Cell and Si MOSFET

The goal of our study is the monolithic integration of solar cells, Si CMOS circuits, and electromyography (EMG) or electroencephalography (EEG) sensors on a single platform that is flexible and conformal to the human skin. For this application, a solar powered voltage-controlled oscillator (VCO) that will transmit the solar harvested energy on an off-chip inductor was designed. The signal from the electrophysiological sensor will modulate the VCO resonance frequency and

to be decoded at the receiver end. We utilized CADENCE and PSPICE simulations to simulate and construct the VCO circuit. To do so, both the DC and AC characteristics of individual components must be characterized. First, to investigate the SOI MOSFET operation at high frequency, we fabricated MOSFETs with a layout that is compatible with 2-port S-parameter measurements along with the standard short, open, through, and load calibration structures, in order to de-embed the short-circuit current-gain (h21). A cut-off frequency (f_T) of 116.0 MHz was measured when the MOSFET was biased at $V_G = -1.2$ V, $V_D = 2.4$ V (**Figure 3.13**), illustrating the capability of these device to operate in the RF regime to transmit electrophysiological signals.

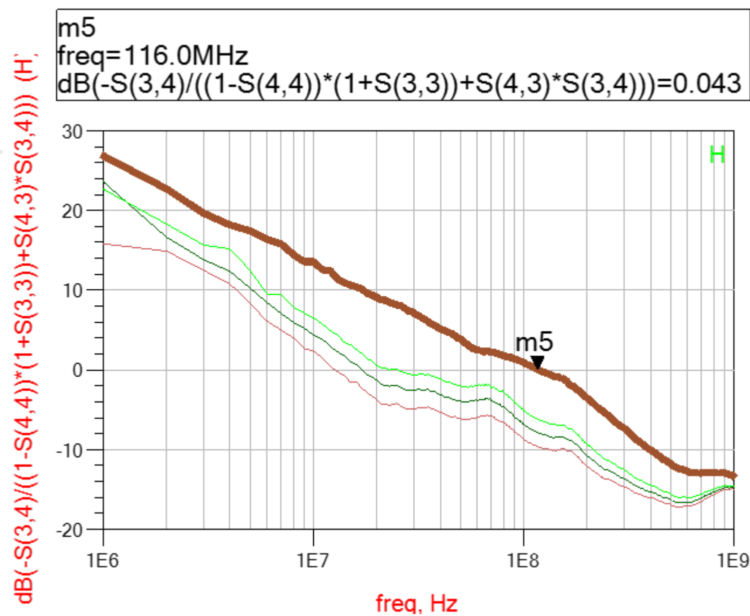


Figure 3.13 Short circuit current gains versus frequency determined from the full two-port S-parameter measurements on n-channel SOI MOSFETs.

The DC light characteristics and the AC characteristics of the Si solar cells were fitted to predict their capability in powering the VCO and to account for their capacitance components to operate in the RF regime. **Figure 3.14 (a)** shows the equivalent circuit model and the DC fit for

the DC light *J–V* characteristics of the Si solar cell. **Figure 3.14 (b)** shows the 1 MHz measured capacitance of the Si solar cell with fit by a conventional diffusion capacitance model.

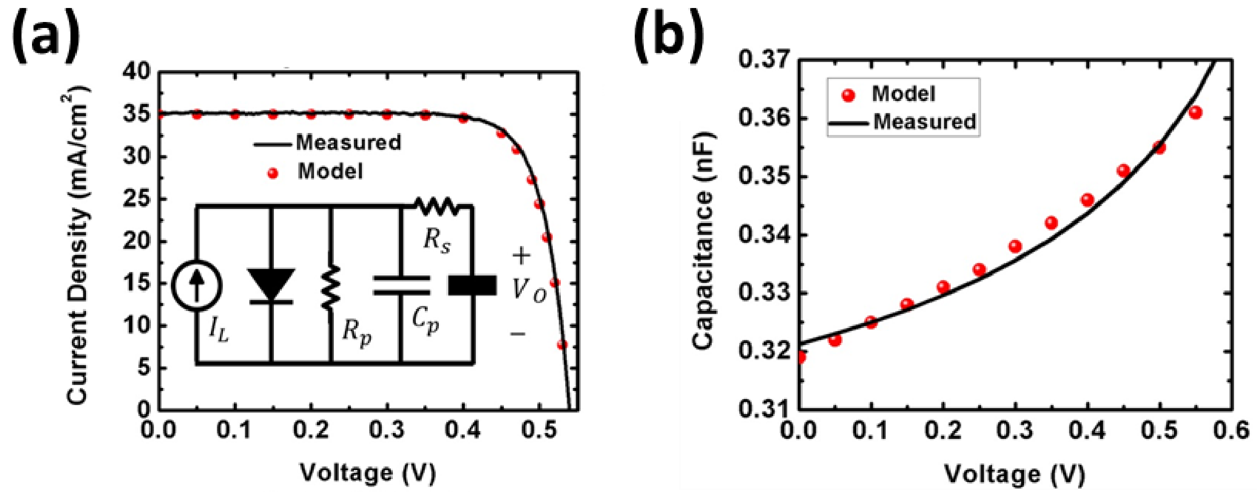


Figure 3.14 (a) Matching light *J–V* characteristics of Si solar cell with an electrical model. (b) Capacitance–Voltage measurement of Si solar cell at 1 MHz.

Figure 3.15 shows the simulated PSPICE structure of VCO based on the DC and AC characteristics of Si solar cell and Si MOSFETs.

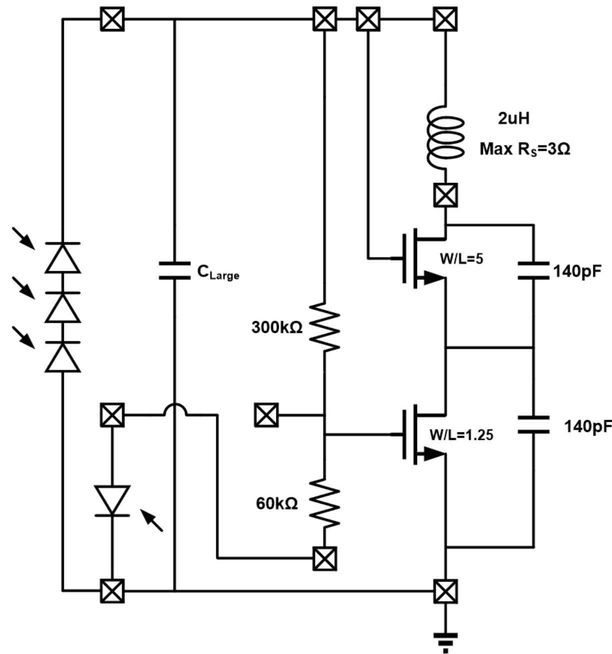


Figure 3.15 Circuit diagram showing simulated self-powered VCO using 4-stacked solar cells.

3.4.3 Side-to-side Monolithic Fabrication Process of Solar Cells and MOSFETs on an SOI Wafer

We demonstrate the side-to-side monolithic integration process that enable the fabrication of Si solar cells and Si MOSFETs on the same wafer. Since our solar cell fabrication process is Complementary Metal-Oxide Semiconductor (CMOS)-compatible, this offers a possible solution for the seamless integration of energy harvesting solar cells with Si MOSFET circuits on the same wafer. This is possible because first, the Si solar cell and the Si MOSFET fabrication share the same doping method (proximity doping) and second, the SiN_x layer was used as a passivation and anti-reflective coating for solar cells and a gate insulator for MOSFETs. Process detail of side-to-side fabrication of Si solar cell and n-channel MOSFET on a single SOI wafer is described in **Figure 3.16**. Based on this fabrication process, Si solar cells, MOSFETs, resistors and LC

oscillators were fabricated on an SOI wafer following the VCO structure we obtained from the simulation above (**Figure 3.17**).

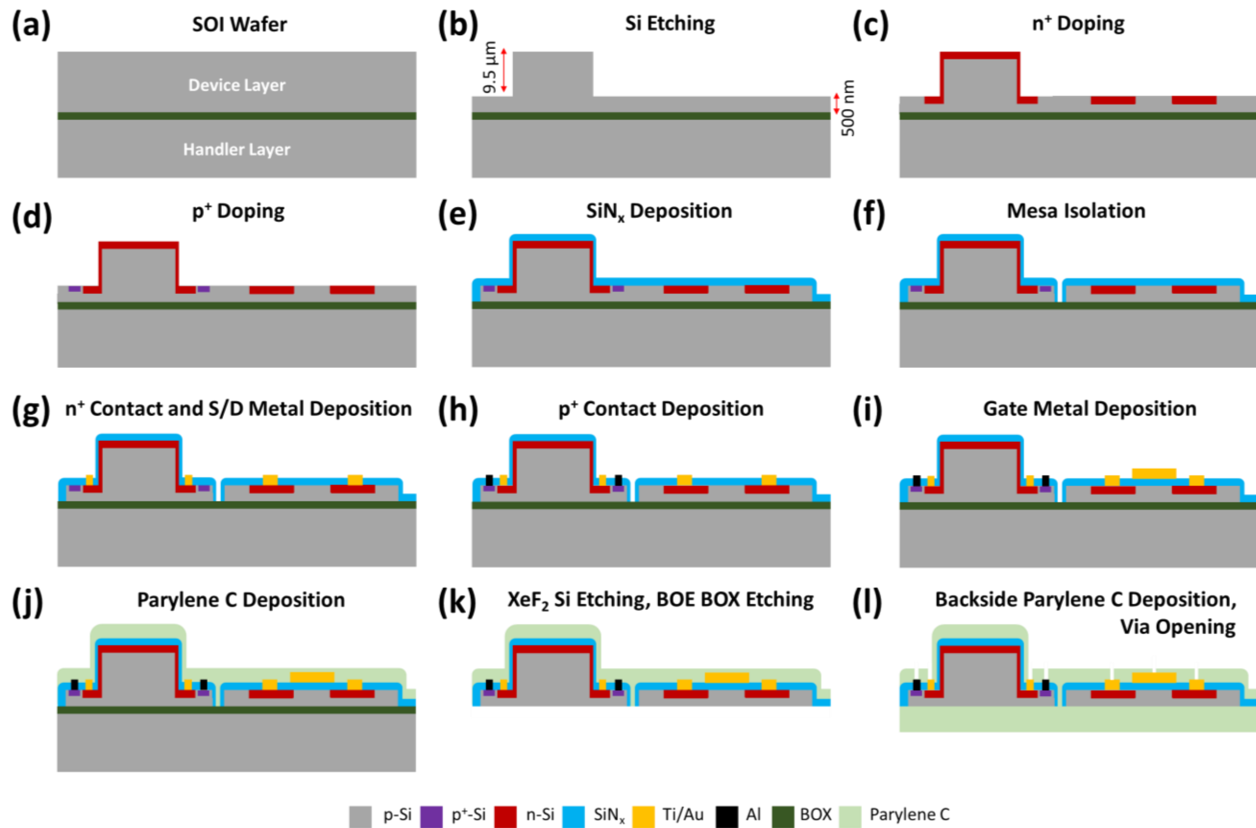


Figure 3.16 Schematic illustration of an SOI solar cell and an n-channel SOI MOSFET side-to-side fabrication on an SOI wafer (cross-section view, not to scale). (a) Starting SOI wafer. (b) Si RIE etching. (c) n^+ doping by phosphorus diffusion. (d) p^+ doping by boron diffusion. (e) SiN_x layer deposition by PECVD. (f) Mesa isolation by Si RIE etching. (g) Ti/Au n^+ contact and source/drain metal deposition. (h) Al p^+ contact deposition. (i) Ti/Au gate metal deposition. (j) A parylene C layer deposition. (k) Handler layer and BOX removal by XeF_2 and BOE etching. (l) Backside parylene C deposition and top side parylene C via opening.

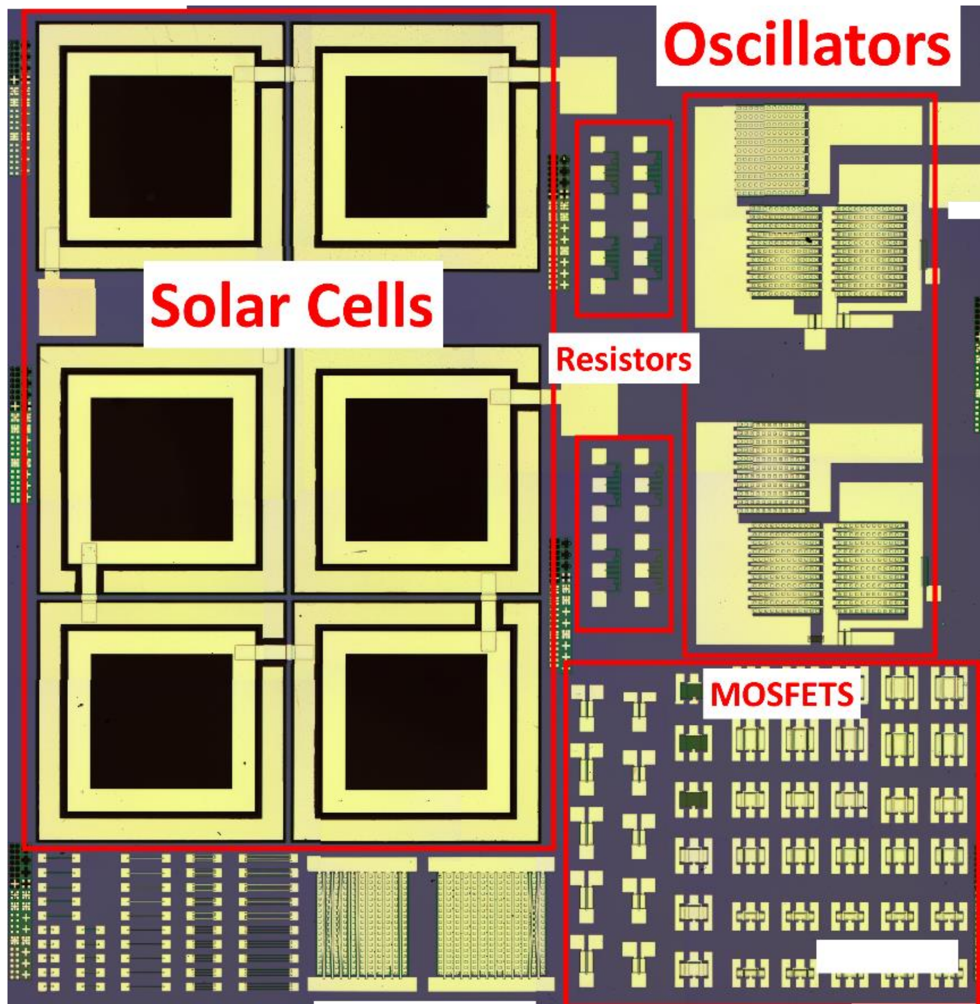


Figure 3.17 A top-view optical microscopic image of Si solar cells, MOSFETs, resistors and LC oscillators on an SOI wafer. Scale bar is 1 mm.

3.5 Conclusion

We presented the development of a novel fabrication process for the release of a Si membrane from an SOI wafer by XeF_2 etching and embedding in parylene C layers creating free-standing structures with thicknesses less than 15 μm in total. With this process, 10 μm thick free-standing SOI solar cells and free-standing SOI MOSFETs embedded in parylene C layers were fabricated and their performances were characterized demonstrating sufficient harvested solar power to operate voltage oscillators constructed from free-standing Si MOSFETs that are capable of RF operation. The CMOS compatible fabrication process of Si solar cells provides possible solutions for monolithic side-to-side fabrication of solar cells and MOSFETs on a single SOI wafer. We propose a solar-powered VCO composed of series-connected solar cells and MOSFETs that can be modulated by signals from electrophysiology sensors.

3.6 Acknowledgements

The dissertation author designed all experiments, fabricated the devices, performed all analysis, and co-wrote the chapter 3. The dissertation author thanks Mr. Woojin Choi and Dr. Namseok Park for the MOSFET fabrications/measurements and mask layout designs, Dr. Cooper Levy for S-parameter measurements and circuit modelling, Mr. Ahmed T. El Thakeb for solar cell modelling, Prof. James Buckwalter for the helpful discussions. Prof. Shadi A. Dayeh led the project, designed the experiments, performed all analysis, and co-wrote the chapter.

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Chapter 4

A Flexible and Scalable MEMS Based Surface and Laminar/Depth Electrode for Human Electrocortical and Intracortical Recording

4. 1 Introduction

The electrophysiological recording and stimulation of neuronal activity is the gold standard technique used for understanding the complex functionality of the brain and for treating brain disorders such as Parkinson's disease, tremor, and epilepsy. Among different electrophysiology recording methods, electrocorticography (ECoG) exhibits higher signal-to-ratio recordings in addition to higher spatial and temporal resolution compared to electroencephalography (EEG) or magnetoencephalography (MEG).[1] ECoG recordings are used in the clinic to delineate eloquent cortex and offer precise localization of epileptic foci.[2]

While ECoG recording occurs at the surface of the cerebral cortex, intracortical recording, where the depth recording electrodes are implanted inside the cerebral cortex, allow us to conduct recordings in the deeper regions of the brain and to obtain cellular level (single unit and multi-unit) activities and local field potentials (LFP). Intracortical depth electrodes can also facilitate deep brain stimulation (DBS) for the treatment of Parkinson's disease.[3,4]

Penetrating microelectrode arrays (MEAs), such as Utah[5] and Michigan[6] arrays have been extensively used for intracortical recordings. While MEAs provided excellent abilities for

extracellular recordings of action potentials, the high stuffiness of Si induces not only tissue damage during electrode insertion but also foreign body responses of the brain which limit their usage to acute studies.[7] Long-term neural recording in the brain over prolonged periods by chronically implanted intracortical depth probes can extend the range of neurobiology studies such as progression of disease states and development of neural networks.[8] The major challenges for long-term neural recording in the brain is the brain tissue response against the implanted probes. After the probe is implanted inside the brain, micromotion of the brain induces damage and inflammation owing to the mechanical mismatch between the brain and the implanted probes. The tissue damage leads to foreign body response, such as neuronal death and glial scar formation around the implanted electrode that consequently degrades the neural recording quality.[9]

Therefore, choosing materials with Young's modulus and bending stiffness that are close to that of the brain is essential for neural probes intended for chronic recordings to mitigate the adverse immune response. Flexible and bio-compatible materials such as polydimethylsiloxane (PDMS),[10] SU-8,[11] Parylene C[12] and Polyimide[13] are widely used for neural probes.

However, these flexible polymers are not stiff enough to penetrate the brain without undergoing probe deformation which can lead to loss of electrode channels or inaccuracy in placing the probe in the desired location. To avoid the polymer probe buckling issue, researchers have adopted rigid shuttles and carriers to aid polymer probes for precise insertion. One of the most popular methods to integrate shuttles or carriers with polymer probes is utilizing bio-dissolvable or degradable adhesives such as polyethylene glycol (PEG),[14,15] maltose[16] or sucrose gel[17] to temporarily adhere a rigid shuttle to a soft polymer electrode. After the electrodes are implanted, the adhesives are dissolved by body fluids or phosphate buffer saline (PBS) to extract

the shuttle after detaching from the probe and leaving only the flexible polymer probe inside the brain.

While this method has successfully enabled implantation of polymer probes, most of these devices are limited to recordings from superficial layers of the brain, mostly in animals due to their short device length (< 10 mm). For human neural recording, ultra-long probes are desirable as the size of the brain scales up from animal models to human models and to target deeper region of the brain such as thalamus and hippocampus, regions that can be as far as 10 cm from the surface of the brain.[18] Ultra-long probes require stronger structural stability than the temporal attachment. As an alternative method to incorporate shuttles or carriers with polymer probes, insertion of rigid shuttles inside the body of polymer electrodes have been suggested. This is accomplished by creating a hollow structure inside the polymer by dissolving a photoresist sacrificial layer in between two parylene C layers[19] or wrapping a polyimide electrode around the stainless-steel needle[20] or by conformal coating of parylene C on a hollow Si structure created by combination of reactive ion etching and XeF_2 etching.[21]

Here, we present flexible multi-channel, high-density, stylet-guided neural probes for intracortical recordings, realized by a Micro Electro-Mechanical Systems (MEMS) technique and *in vivo* recording results using the probes. Our fabrication process that is compatible with different types of polymers (Parylene C, polyimide) allows us to alter the design and the size of the device based on the target of interest for animal, non-human primate, and human use, for lengths extending from sub-tens to hundreds of millimeters.

4.2 Experimental Detail

4.2.1 Intracortical Laminar Probe

4.2.1.1 Fabrication Process

The fabrication method of intracortical laminar probe is based on the standard MEMS technology. First, a Ti/Al (10/200 nm) sacrificial layer was deposited on a 4" Si carrier wafer to enable the polyimide device release from the Si carrier wafer (**Figure 4.1 (a)**). A first polyimide layer (HD4104, HD MicroSystems LLC) was spun-coated on top of the Ti/Al sacrificial layer at 1500 rpm (7.5 μm) and cured at 300 °C in N_2 for 30 min (**Figure 4.1 (b)**). The curing temperature and time were designed to partially cure the polyimide layer.[16,22] A Ti/Au (50/100 nm) sacrificial layer was deposited on the first polyimide layer (**Figure 4.1 (c)**). Ti serves both as an adhesion layer for Au as well as an etch-stop layer to protect underlying polyimide layer during later part of via etching process. Au serves as a sacrificial layer to create a gap between the first and the second polyimide layer where a stylet will be inserted. On the periphery of the sacrificial layer, polyimide microholes were introduced to increase adhesion between the first and the second polyimide layer and avoid separation of polyimide to polyimide bonding during stylet insertion. Moreover, the shape of the sacrificial layer was designed to have tapered tip to STRESS avoid the separation. A photoresist (AZ1518) was used as an etch mask and polyimide microholes were etched by O_2 plasma. Both the diameter and the spacing of polyimide microholes are defined as 4 μm. The depth of polyimide microholes was 1.5 μm. The second polyimide layer was spin-coated at 3000 rpm (4 μm) and cured at 330 °C in N_2 for 45 min (**Figure 4.1 (d)**). A metal lead layer of Cr/Pt/Ti (20/100/100 nm) was deposited by sputter and patterned via lift-off process (**Figure 4.1 (e)**). Cr layer serves as an adhesion layer between Pt conduction layer and polyimide. The Ti layer was deposited to protect the underlying Pt layer during via dry-etching and Au sacrificial layer wet-

etching.[23] A third polyimide insulation layer was spun-coated at 3000 rpm (4 μm) and cured at 360 °C in N_2 for 60 min to complete the imidization of the polyimide and adhesion process (**Figure 4.1 (f)**). A Ti (100 nm) layer was deposited and patterned via lift-off process on the third polyimide layer as an etch hard mask against O_2 plasma etching. The Ti hard mask was patterned to define 1) via openings of Pt electrode sites and bonding pads, 2) an opening of entrance for stylet insertion, 3) via openings to etch the Au sacrificial layer and 4) shape of the device body (**Figure 4.1 (g)**). O_2 plasma etching was performed until polyimide layers are fully etched at the outside of the Ti hard mask (**Figure 4.1 (h)**). The Si carrier wafer was immersed in Au etchant (TFA, Transene Company, Inc.) to etch away the Au sacrificial layer between the first and the second polyimide layer. The Al sacrificial layer beneath the first polyimide layer was etched by Au etchant simultaneously to release the polyimide device from the carrier Si wafer (**Figure 4.1 (i)**). After the polyimide device was released and the Au sacrificial layer was etched away, the Ti hard mask and protection layer was removed by buffered oxide etchant (BOE) followed by DI water rinse, leaving fresh Pt surface on the electrode sites (**Figure 4.1 (j), (k)**). The bonding pad region (Cr/Pt) of the probe was bonded with anisotropic conductive films (ACF) with commercial off-the-shelf ribbon cables to connect the device to the external characterization circuitry. The diameter and pitch of electrode sites is 20 and 60 μm, respectively, and the probe consisted of 64 channels along 3.84 mm in a laminar manner. The dimension and the number of electrodes can be adjusted based on the target of merit.

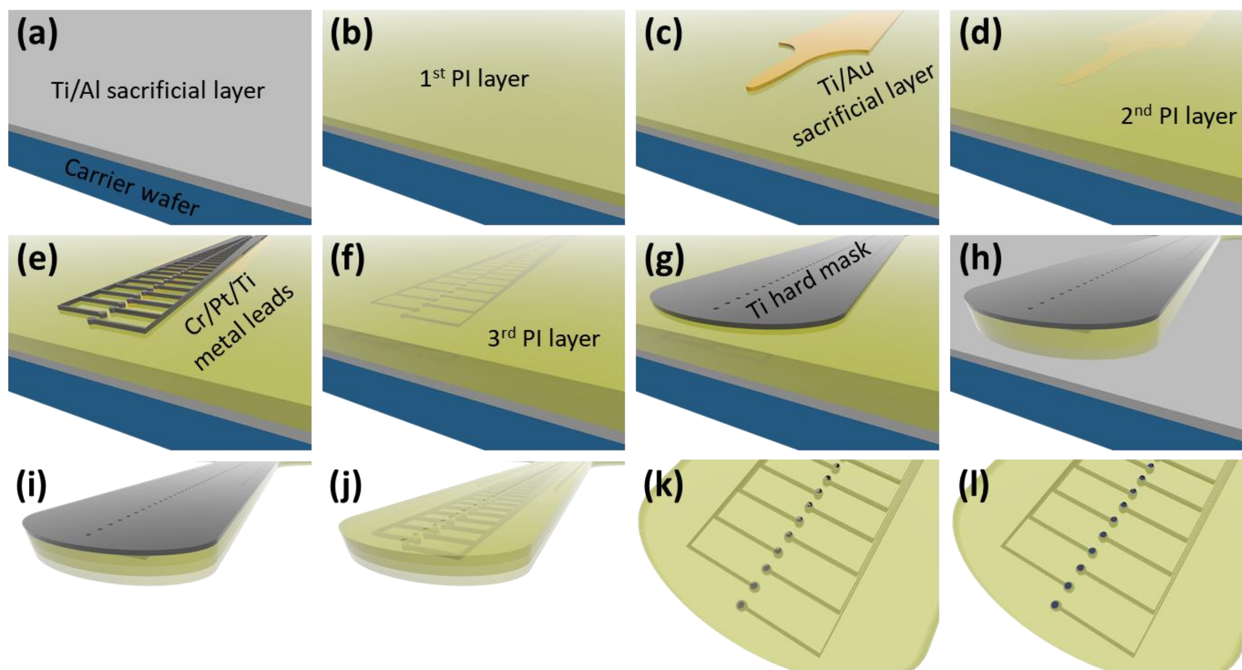


Figure 4.1 Schematic illustration of the laminar probe fabrication process. (a) Ti/Al sacrificial layer deposition. (b) The first polyimide layer deposition. (c) Ti/Au sacrificial layer deposition. (d) The second polyimide layer deposition. (e) Cr/Pt/Ti metal leads deposition. (f) The third polyimide layer deposition. (g) Ti hard mask deposition. (h) O_2 plasma etching. (i) Au etchant etching. (j), (k) Released laminar probe after Au etching. (l) Conductive polymer deposition on the electrode sites.

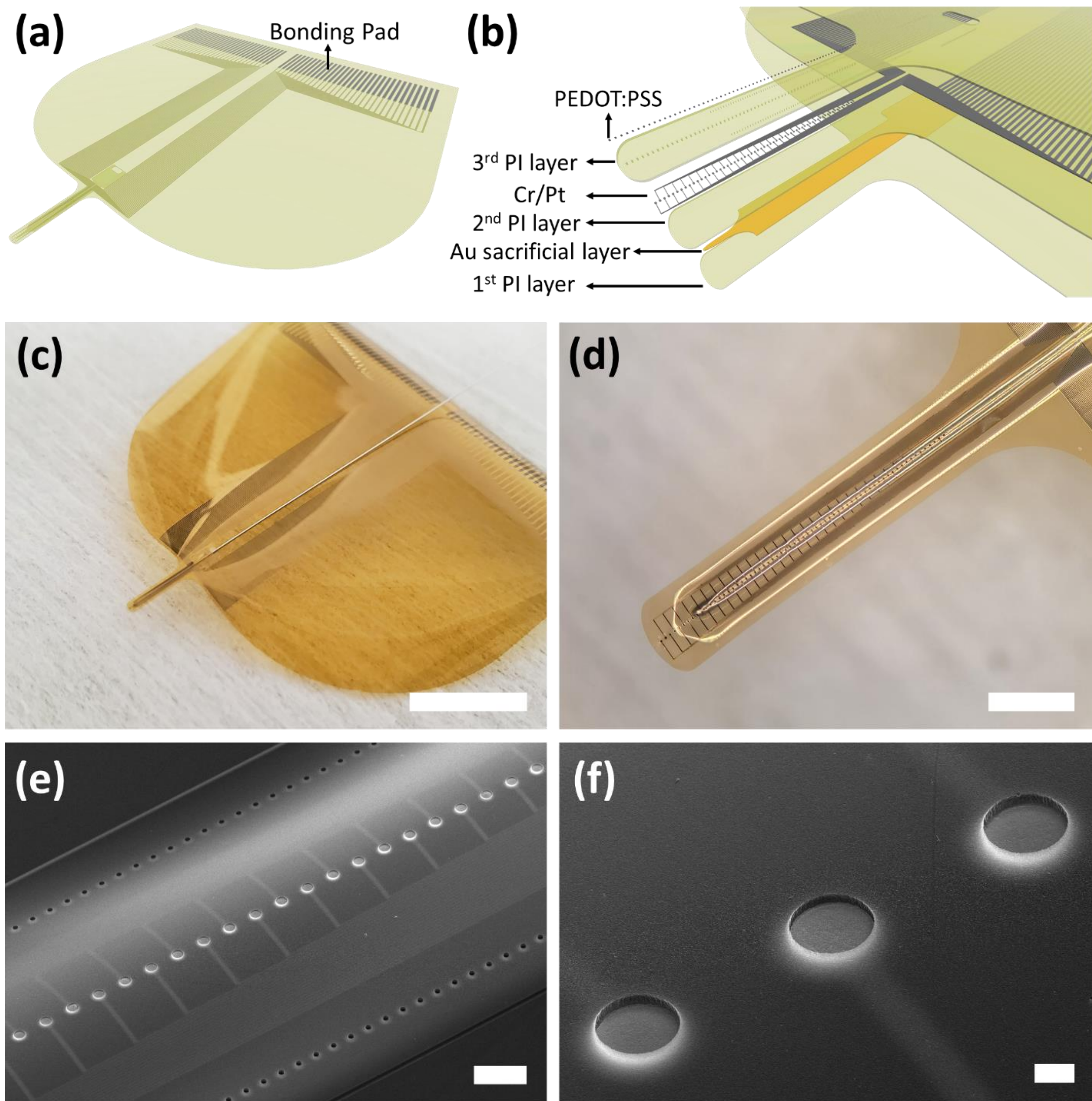


Figure 4.2 (a) A schematic illustration of laminar probe layout. (b) Exploded view of the layout at the electrode sites region. (c), (d) Optical images of laminar probe after stylet insertion. Scale bar is (c) 1 cm and (d) 1 mm. (e), (f) SEM image of laminar probe showing PEDOT:PSS on Cr/Pt after stylet insertion. Scale bar is (e) 100 µm and (f) 10 µm.

4.2.1.2 Microholes on Polyimide to Increase Adhesion

Due to low specific surface energy of polyimide,[24] polyimide to polyimide interface suffers from poor adhesion. This leads to the separation of polyimide during insertion of the stylet inside the hollow structure of polyimide. We introduced microhole structures on the first polyimide layer of the laminar probe by O_2 plasma etching to improve adhesion to the upper polyimide (**Figure 4.3**). O_2 plasma can cut the polymer chain on the surface of polyimide and change the surface from hydrophobic to hydrophilic.[24] Microholes increase polyimide surface area and roughness which affects the most in improving the adhesion strength.

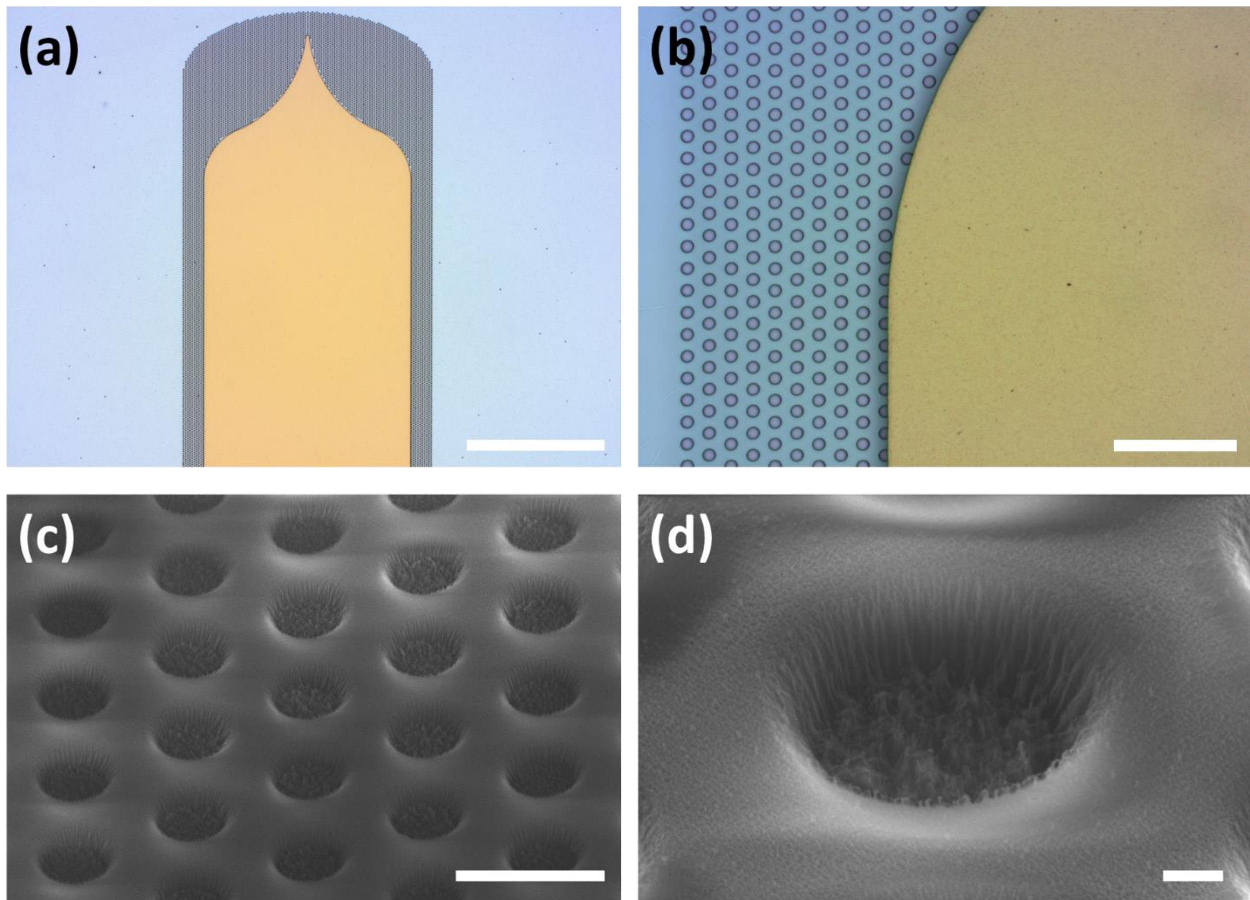


Figure 4.3 (a), (b) Top-view optical microscopic images of microholes on polyimide near periphery of Au sacrificial layer. Scale bar is (a) 500 μm and (b) 50 μm. (c), (d) SEM images (45-degree view) of polyimide microholes. Scale bar is (c) 10 μm and (d) 1 μm.

4.2.1.3 PEDOT:PSS Electrodeposition

Conductive polymers (CPs) such as PEDOT:PSS integrated on microelectrodes have substantially improved microelectrode recording with a high SNR recording ability, due to the high quality of their electrochemical interface and volumetric sensing that result in a low impedance. In addition, PEDOT:PSS electrodes provide safe and efficient stimulation to their high charge injection capacity.[25] We electrodeposited PEDOT:PSS on the surface of Pt contacts of the laminar probe to reduce the electrochemical impedance for improved signal quality over that attained with metal contacts. PEDOT:PSS was electrodeposited from 0.01 M 3,4-Ethylenedioxythiophene (EDOT) in 2.0 g per 100 mL Poly(sodium 4-styrenesulfonate) aqueous dispersion under galvanostatic conditions at a potential of 0.9 V versus Ag/AgCl in a three electrode setup, i.e., Ag/AgCl electrode as a reference electrode, a large Pt electrode as a counter electrode, and the Pt contacts on the probes as the working electrodes, at a constant temperature of 27 °C using a Gamry potentiostat (Gamry Interface 1000E; Gamry Instruments). Polymerization was driven for 20 s at current density of 5 mA/cm^2.

4.2.1.4 Stainless-steel Stylet Shuttle

Medical grade stainless steel 316 stylets (Ø 125 µm) were used as a shuttle after the tip was polished mechanically to have a tapered and smooth surface (**Figure 4.7**). The stainless-steel was chosen as a shuttle material over a tungsten rod or a silicon shuttle because of its hydrophilic surface, which helps to avoid adhesion between the hydrophobic polyimide surfaces.[10] These stainless steel shuttles are the standard stylets used for the implantation of clinical depth electrodes. After the PEDOT:PSS electrodeposition, the stylet was inserted through the openings on the polyimide layer along the hollow region between the first and the second polyimide layers where

the Au sacrificial layer is etched away. The retractable stylet provides rigidity to the polyimide probe tip and supports implantation to the cortex without probe deformation. **Figure 4.4** shows an optical microscopic and SEM images of mechanically polished stainless-steel stylet, showing smooth surface at its tip.

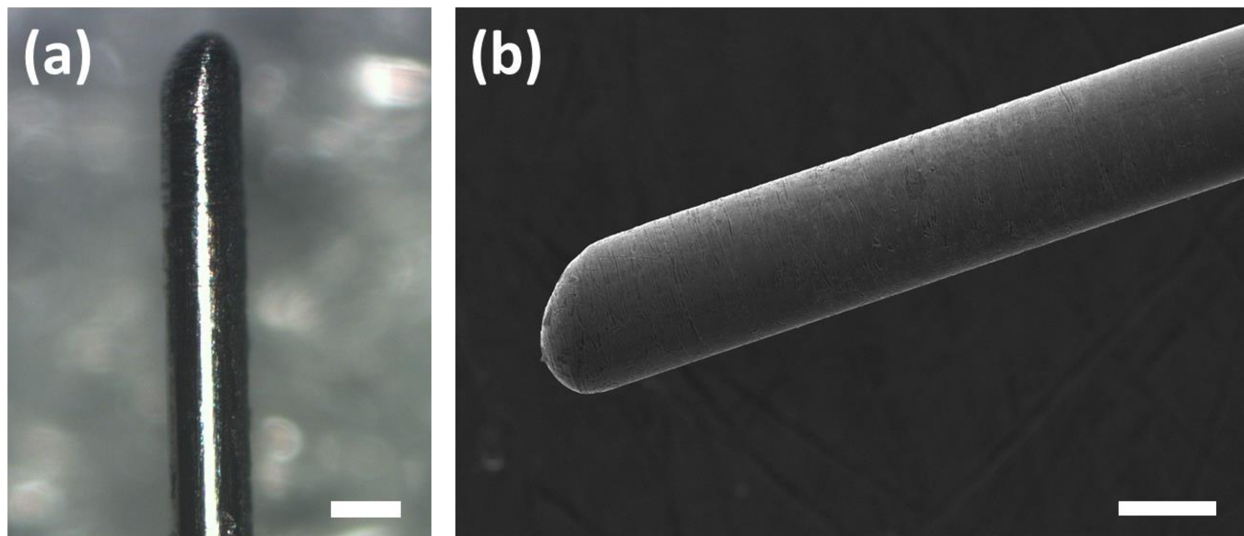


Figure 4.4 (a) A top-view optical microscopic image and (b) SEM image of a polished stainless-steel stylet. Scale bars are 100 μm.

4.2.2 ECoG Surface Electrode

Parylene C was chosen as the ECoG probe material because of its superior conformability and hydrophobic surface which makes stable electrical and mechanical contact with the surface of the cortex.[26] The fabrication process of parylene C ECoG surface probes was reported elsewhere.[25] First, an anti-adhesion layer, Mirco-90 (International Products Corporation) diluted with DI water (0.1 %) was spun-coated on a 4" Si carrier wafer to enable parylene C device release from the Si carrier wafer. A first parylene C layer (3 μm) was deposited on top of the anti-adhesion layer by chemical vapor deposition (PDS 2010, SCS coatings). A Cr/Au/Ti (10/100/50 nm) metal lead layer was evaporated and patterned via lift-off process. Cr layer serves as an adhesion layer between Au

conduction layer and parylene C. Ti layer was deposited to protect Au layer during later via dry-etching process. A second parylene C insulation layer (3 μm) was deposited. A Ti (50 nm) layer was deposited and patterned via lift-off process on the second parylene C layer as an etch hard mask against O_2 plasma etching. The Ti hard mask was patterned to define 1) via openings of the Au electrode sites and bonding pads, 2) shape of the device body and 3) perforations on parylene C layers. Perforations can help minimizing the excessive cerebrospinal fluid (CSF) around the electrode sites.[27] The Ti hard mask and protection layer was removed by BOE and rinsed with DI water, leaving fresh Au surface at the electrode sites. The parylene C device was released from the Si carrier wafer by removing Micro-90 with DI water. After the bonding pad region of the probe (Cr/Au) was bonded with ACF and commercial off-the-shelf ribbon cables, PEDOT:PSS was electrodeposited on the surface of Au electrode sites using the previously described technique. The surface probe consists of two column 32 channels along 3.1 mm in a laminar manner and the diameter and pitch of electrode sites is 20 and 100 μm, respectively.

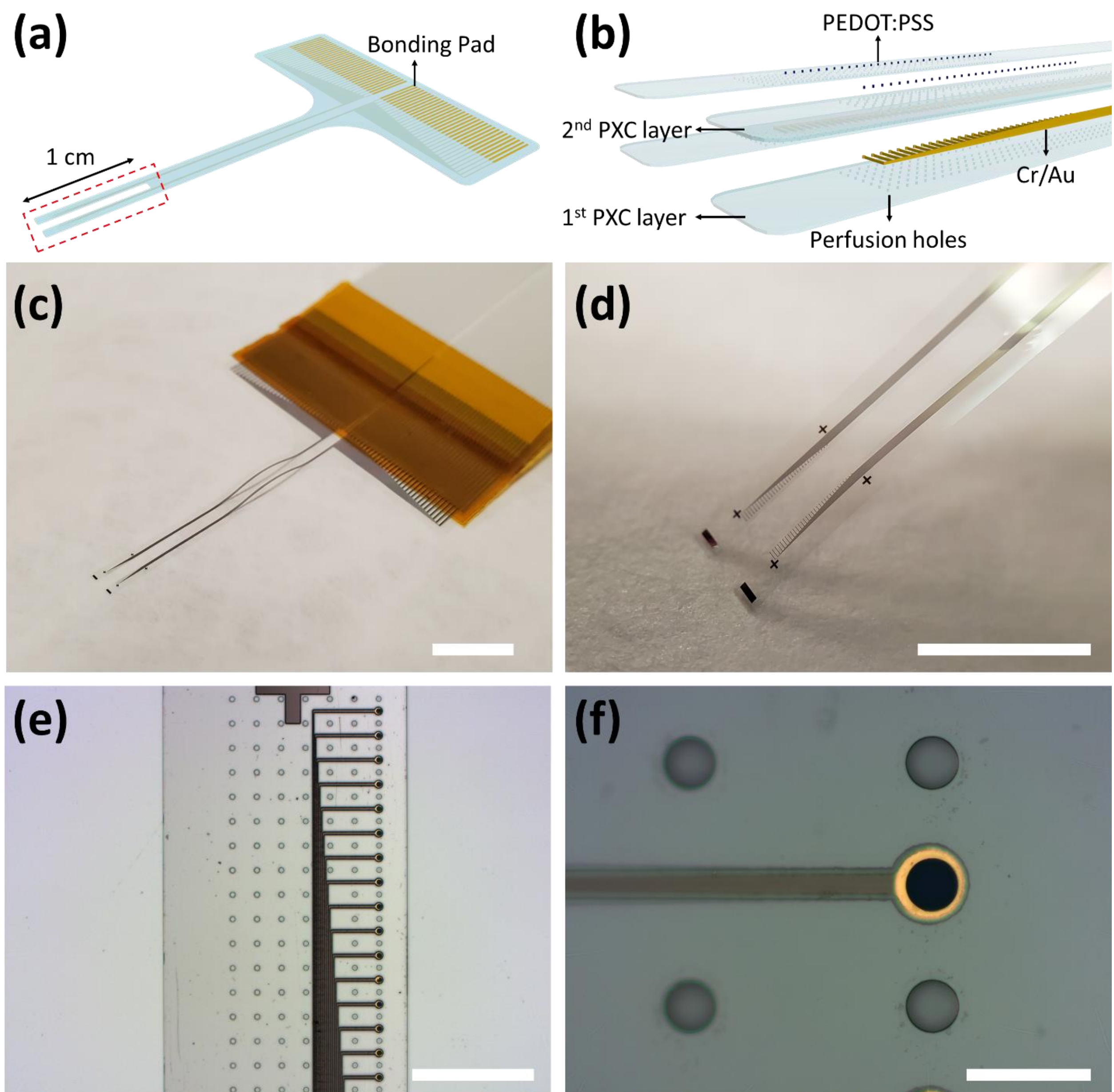


Figure 4.5 (a) A schematic illustration of ECoG surface probe layout. Red dotted square indicates electrode sites region. (b) Exploded view of the layout at the electrode sites region. (c), (d) Optical images of the ECoG surface probe. Scale bar is (c) 1 cm and (d) 5 mm. (e) Top-view optical microscopic image of the electrode sites region. Scale bar is 500 µm. (f) Magnified top-view optical microscopic image showing PEDOT:PSS on Cr/Au electrode sites and perforation holes. Scale bar is 50 µm.

4.2.3 Electrochemical Characterization

Electrochemical impedance spectroscopy (EIS) of the laminar probe was performed 1) before and 2) after the PEDOT:PSS electrodeposition and 3) after stylet insertion, in 1X phosphate buffer saline (PBS) solution (**Figure 4.6 (a)-(c)**). Three electrode configuration i.e., Pt or PEDOT:PSS electrodes as the working electrode, Ag/AgCl electrode as a reference electrode, a large platinum electrode as a counter electrode was used. 10 mV root mean square (RMS) sinusoidal signal with zero DC bias were applied and the frequency was swept from 1 Hz to 10 kHz using a Gamry potentiostat (Gamry Interface 1000E; Gamry Instruments). Electrochemical impedance at 1 kHz is commonly used as the benchmark for the characterization of neural electrodes, as this frequency corresponds to spiking activity.[28] The average impedance magnitude of Pt electrodes across 64 channels was 1039±179 kΩ which was reduced to 33.0±2.47 kΩ after the PEDOT:PSS electrodeposition on Pt electrodes. After stylet insertion, the average impedance magnitude maintained similar values of 35.0±3.67 kΩ on 64 channels (**Figure 4.6 (e), (f)**), indicating that the stylet was successfully inserted between the polyimide layers without any damage to the channel or PEDOT:PSS separation from Pt electrodes.

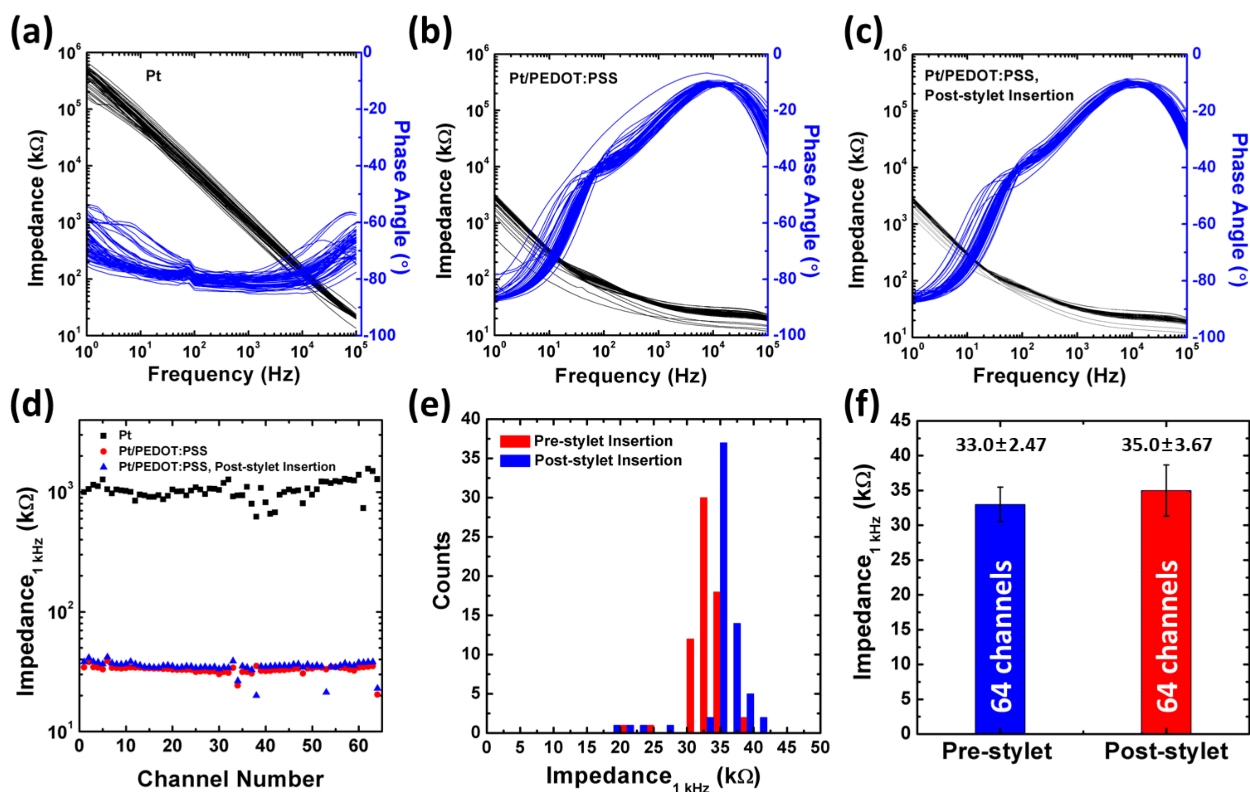


Figure 4.6 (a)-(c) The laminar probe electrochemical impedance spectra of (a) Pt, (b) Pt/PEDOT:PSS and (c) Pt/PEDOT:PSS after stylet insertion. (d) Electrochemical impedance magnitude at 1 kHz of each channel. (e) Electrochemical impedance magnitude at 1 kHz histogram of Pt/PEDOT:PSS before and after stylet insertion. (f) Electrochemical impedance magnitude at 1 kHz average and standard deviation before and after stylet insertion.

For the ECoG probe, electrochemical impedance at 1 kHz was measured using Intan RHD2000 USB interface board (Intan Technologies) in 1X phosphate buffer saline (PBS) solution with a stainless-steel needle as a reference electrode. The average impedance magnitude of Au electrodes was 739±85.4 kΩ, which was decreased to 33.6±3.21 kΩ after PEDOT:PSS electrodeposition on Au electrodes (**Figure 4.7**).

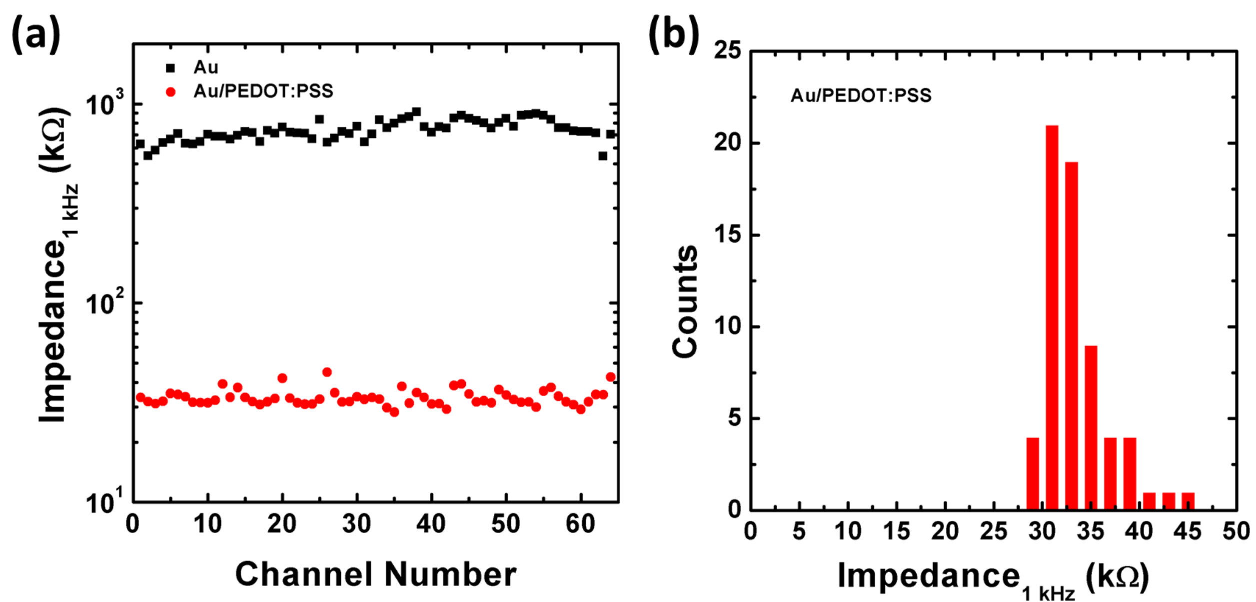


Figure 4.7 (a) Electrochemical impedance magnitude at 1 kHz of each channel of ECoG surface probe before and after PEDOT:PSS electrodeposition. (e) Electrochemical impedance magnitude at 1 kHz histogram of Au/PEDOT:PSS.

4.3 Laminar Probe Insertion Test on a Brain Model

Insertion of the laminar probe was tested on a phantom brain model. A transparent brain phantom gelatin model was prepared by mixing and dissolving a gelatin powder (Knox; Kraft Foods, Inc.) with weight concentration of 5.3 %. Knox gelatin with this concentration was reported to provide similar shear modulus to the mouse brain[29] and its transparency helps in visualization of the laminar probe movement in the gel. We designed and printed a custom-made 3D printed probe holder that can be attached to the stereotaxic micromanipulator while holding the laminar probe (**Figure 4.8 (a)**). The laminar probe, held by the 3D print holder, was slowly inserted into the gelatin using the z-axis control handle of the stereotaxic micromanipulator. After the laminar probe was inserted, the stainless-steel stylet was manually grasped by a tweezer and extracted from the laminar probe. The implantation of the laminar probe and displacement after stylet extraction were recorded using a camera with a macro lens. **Figure 4. (b)** shows the laminar probe in the gelatin model after implantation and after stylet extraction. The laminar probe was implanted without any deformation with help of the stylet. Also, the displacement of the laminar probe before and after stylet extraction was negligible.

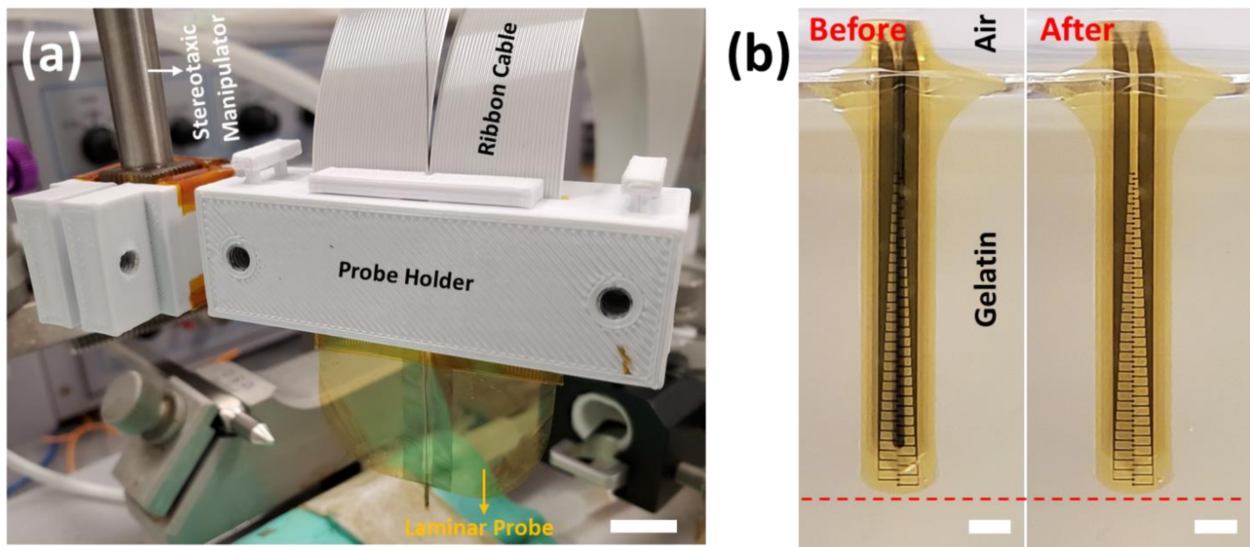


Figure 4.8 (a) An optical image of the 3D printed holder and the laminar probe attached to the stereotaxic manipulator. Scale bar is 1 cm. (b) An optical image of the laminar probe tip inserted in the gelatin model, before and after stylet extraction. Scale bar is 500 μm.

4.4 Acute *in vivo* Electrophysiological Recordings

4.4.1 Animal Preparation

Acute *in vivo* electrophysiological recordings were performed on the rat primary somatosensory "barrel" cortex (S1) with the ECoG surface probe and the laminar probe. All procedures were performed under a protocol approved by the Institutional Animal Care and Use Committee of the University of California, San Diego. Rats were anesthetized with mixture of ketamine/xylazine. The body temperature of the rat was maintained at 37 °C with a heating pad. Craniotomy and dura removal were performed over the right barrel and surrounding cortical region.

Figure 4.9 illustrates rat experiment set-up and placement of the probes. First, the ECoG surface probe was placed on the cortical surface. At the gap between two columns of the surface probe, the laminar probe was implanted, and the stylet was removed using the previously described technique (**Figure 4.10**).

Tactile stimulation was performed by delivering air puffs to the whisker pad. Air puff was pressure-injected through a glass micropipette using a PV830 pneumatic picopump (World Precision Instruments, Inc.) with 1 s pulses. The contralateral (left) whiskers with respect to the recording sites were deflected by air puff (±2 mm). First, the whole contralateral whiskers (multi-whisker) were stimulated. Then single whiskers (C1-3, D1-3, E1-4) were stimulated by placing the pipette as close as possible to each whisker to avoid deflection of the neighboring whiskers. Recording data were collected for 60 s for each whisker.

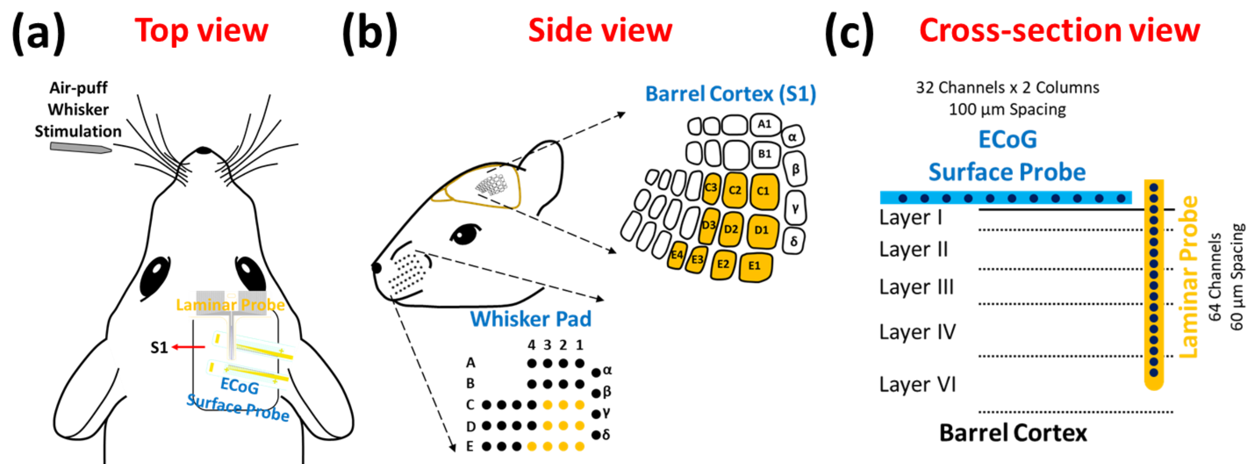


Figure 4.9 Schematic illustrations of rat experiment setup from (a) top, (b) side and (c) cross-section view.

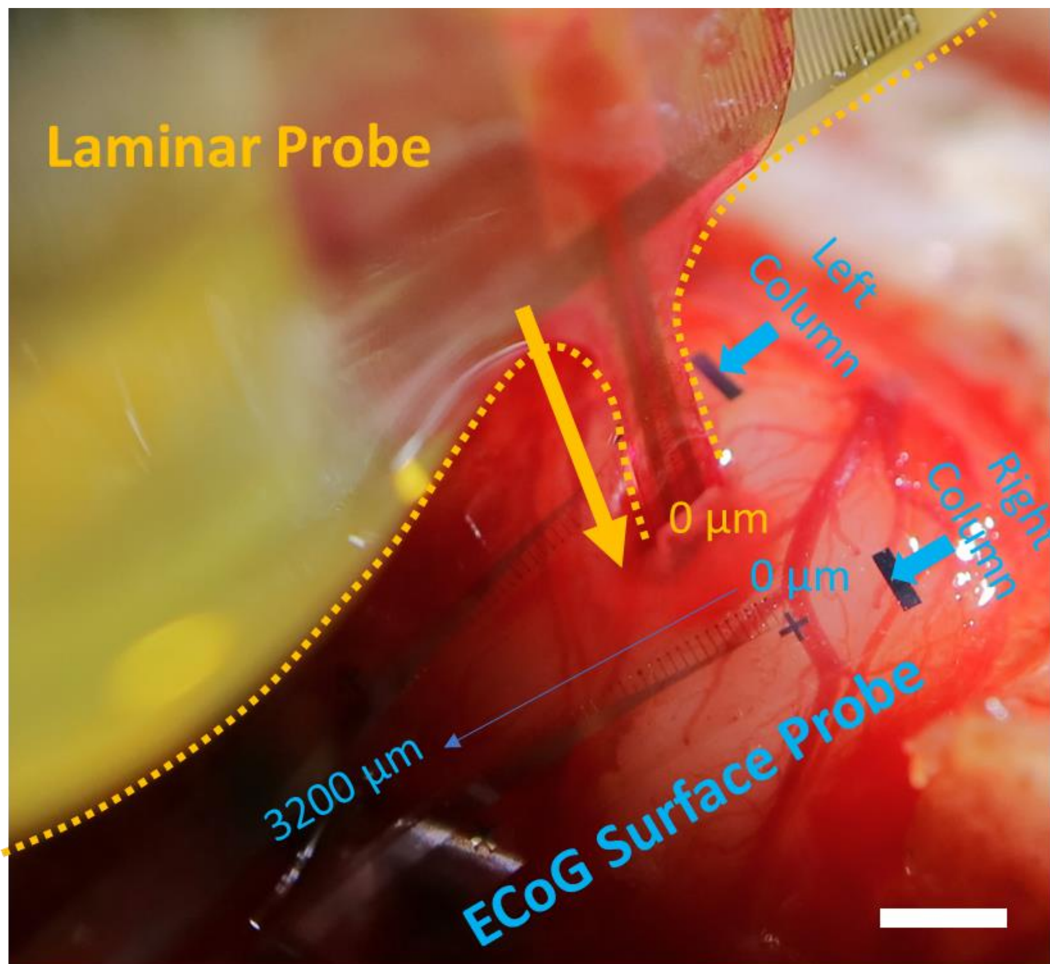


Figure 4.10 An optical image of the ECoG surface probe placed on the surface of the cortex and the laminar probe implanted in the cortex. Scale bar is 1 mm.

4.4.2 Data Acquisition

Electrophysiological recordings from both the laminar probe and the ECoG surface probe were performed simultaneously with the same data acquisition system, Intan RHS stim/recording controller (Intan Technologies) with sampling rate of 30 kHz. The Intan RHS stim/recording controller was connected to an RHS recording headstage that was connected to the laminar probe and a separate RHS recording headstage was connected to the surface probe. A pointed stainless-steel needle was inserted in the subcutaneous tissue near the craniotomy as a reference electrode. Electrochemical impedance at 1 kHz for both ECoG surface and laminar probe was measured after the device placement/implantation. Channels with high impedance magnitude (>500 kΩ) were assumed to be damaged channels and removed from further analysis. The depth probe channels that were not inserted in the cortex were also removed. The analog input of Intan RHS stim/recording controller was connected to the pneumatic picopump to record trigger stimulation pulses by air puff.

4.4.3 Histology

Prior to the insertion to the cortex, the back of the tip of the laminar probe was painted with a fluorescent dye, DiI (1,1′-Dioctadecyl-3,3,3′,3′-tetramethylindocarbocyanine perchlorate, 0.1% in ethanol; Invitrogen) to visualize the probe track in histopathological sections and verify the placement of the probe with respect to cortical depth. Following the electrophysiological recordings, rats were perfused with 4% PFA, and the brains post-fixed for 2 h in 4% PFA. Brains were transferred to a 30% sucrose solution, and then embedded in OCT matrix and stored at -80. Slices were sectioned on a cryostat at 50 µm. Free-floating sections were washed in PBS + 0.1% Triton for 10 min, and then incubated in 1:50 Neurotrace 500/525 (ThermoFisher) for 30 min.

Sections were washed in PBS + 0.1% Triton for 10 min, followed by PBS. Sections were mounted on slides and coverslipped using ProLong Gold (ThermoFisher). Slices were imaged using a Keyence BZX-700 at the UCSD Department of Neuroscience Microscopy Core (supported by NS047101). From the histology result (**Figure 4.11**), the tip of the probe was estimated to be 1750 µm deep in the cortex, reaching layer VI at the tip.

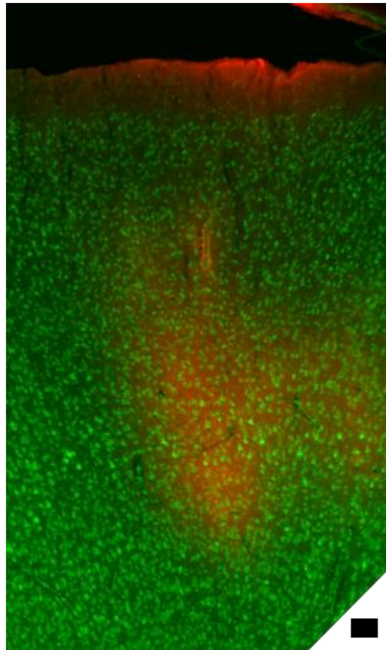


Figure 4.11 Nissl-stained coronal section of barrel cortex showing the track of the laminar probe in the cortex of the rat. Scale bar is 100 µm.

4.4.4 Data Analysis

All off-line data analysis including signal filtering and plotting were performed using MATLAB R2020a (MathWorks). The stimulus was delivered 39 times/trials and the recording data from each trial were averaged. To remove noise, the data were re-referenced by subtracting the average signal of the channels. Local field potentials (LFPs) and high gamma activity (HGA) evoked by tactile stimuli were investigated. The recordings were band-pass filtered for LFP (1–

300 Hz) and HGA (70–190 Hz) with fourth-order Butterworth bandpass filter. Among different stimulations, stimulations from C3, D3, E3, E4 whisker and multi-whisker were chosen for data analysis.

LFP response: Strong LFP responses were observed from whiskers C3 and D3, for both surface and laminar probes, which allows us to estimate the location of the probes to be near C3 and D3 barrel columns. For all kind of whisker stimulation, it is observed that LFP from the laminar probe is dominated by a single negative peak, whereas LFP from ECoG surface probe shows the opposite polarity.

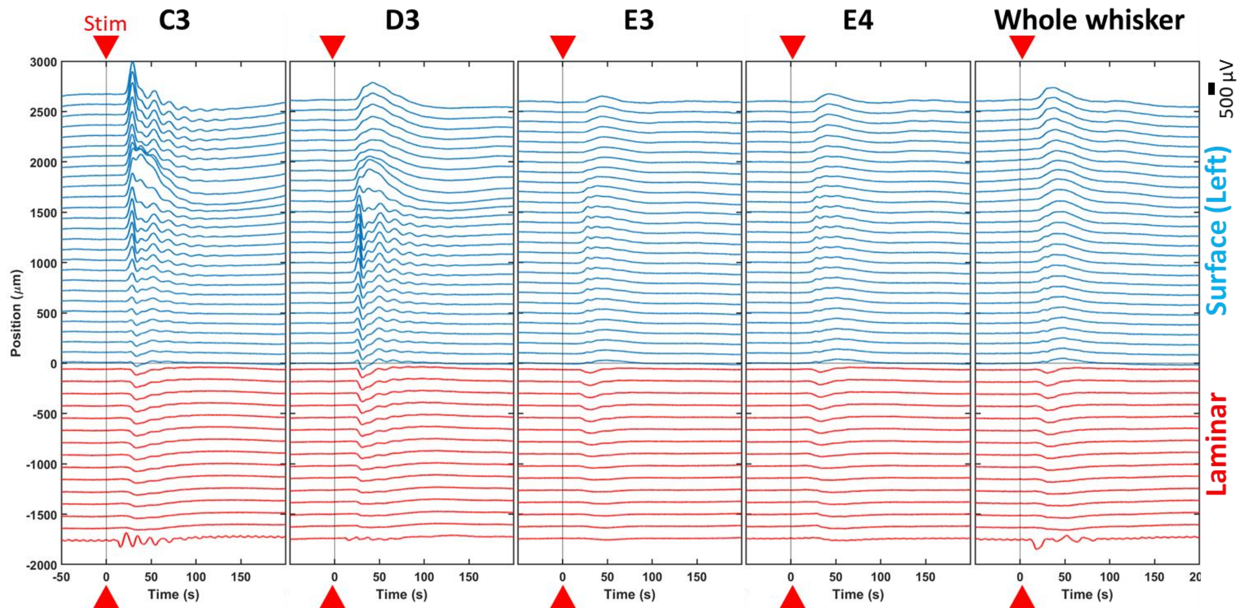


Figure 4.12 LFP profiles evoked by deflection of each whiskers. Blue and red LFP traces correspond to recordings from the surface probe and the laminar probe, respectively.

While LFP represents summation of excitatory and inhibitory synaptic activity, it has limitation of providing accurate spatiotemporal information of the synaptic activity.[30] On the other hand, current source density (CSD) provides information on the distribution of synaptic inputs for

the generators.[31] Here, CSD was calculated from LFP using the δ-source inverse CSD (iCSD) method, refined by Petterson et al.[32]:

$$C = F^{-1}\Phi \tag{4.1}$$

where C and Φ represents matrix for CSD and LFP, respectively. The transformation matrix F is described by

$$F_{ji} = \frac{h^2}{2\sigma}\left(\sqrt{(j-i)^2 + (R/h)^2} - |j-i|\right) \tag{4.2}$$

where h is the spacing between adjacent electrode, σ is the conductivity of the cortex and R is the radius of infinitely thin current-source discs. Here we set the σ and R as 0.3 S/m and 0.25 mm, respectively. Based on the calculated CSD, CSD heatmap was generated using the amplitude of CSD and overlaid with CSD plots (**Figure 4.13**). The negative values shown in red represents current sink and positive values shown in blue represents current source. Current sink is generated by excitatory synapse and to achieve electroneutrality, it is balanced by current source, which is opposing ionic flux from the intracellular to the extracellular space. It is important to note that the laminar probe was connected to two different ribbon cables which correspond to each column of two interdigitated columns of electrode channels of the laminar probe (32 channels, 2 columns). Because two ribbon cables are connected to two different recording headstages, the data obtained from the two headstages showed discrepancy from column to column. Since CSD is calculated from LFP data of adjacent electrodes, each column was separated for calculation of CSD and the column that included a greater number of low impedance (<500 kΩ) channels (31 out of 32) was selected for the CSD analysis. From the CSD profile it can be found for all kinds of stimulation, a large current sink is centered and shows the highest amplitude at layer IV. The current sink is extended to Layer II/III and Layer V. The current source appears near Layer I.

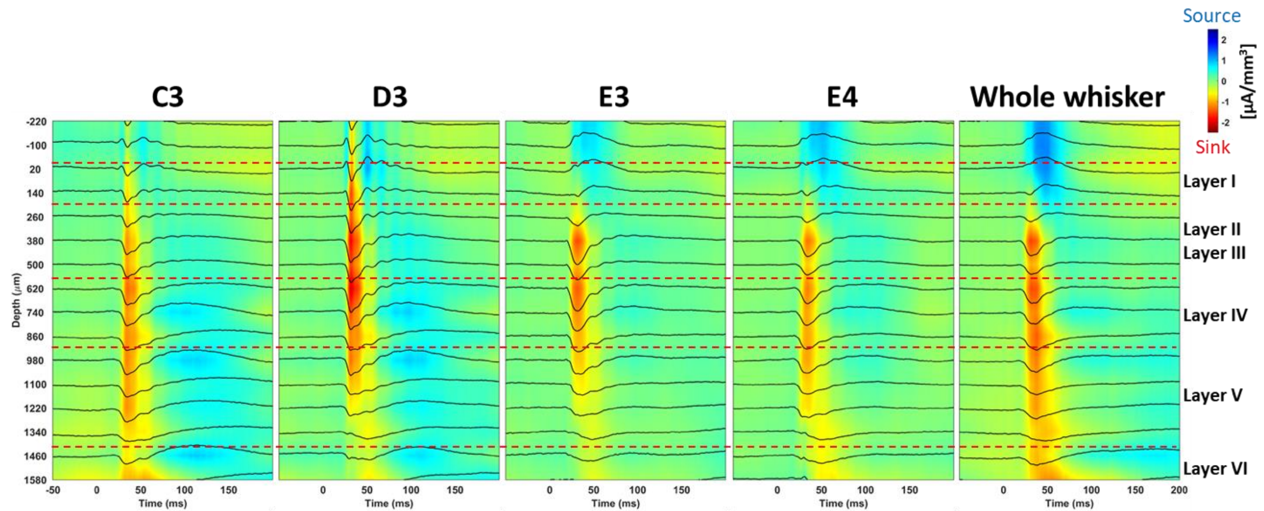


Figure 4.13 CSD profiles calculated from LFP obtained from the laminar probe along the depth of the cortex.

Additionally, HGA were investigated to see the propagation of the signal on the cortical surface (**Figure 14**). HGA amplitude from the surface was observed compared to that of the laminar probe while stimulation from C3 and D3 whiskers showed higher amplitude compared to other stimulated whiskers. To visualize the propagation of HGA on the surface probe, colormaps were generated based on the amplitude of the HGA (**Figure 15**). From the colormap, we can estimate the placement of the surface probe on the cortex. It is likely that the center of the surface probe left column is placed near D3 barrel column while from the region from the center to the edge covered areas near C3 barrel column. HGA from the right column of the surface probe was also estimated. For the right column, stimulation from E4 whiskers resulted in the highest amplitude, which indicates that the right column of the surface probe was placed near E4 barrel column.

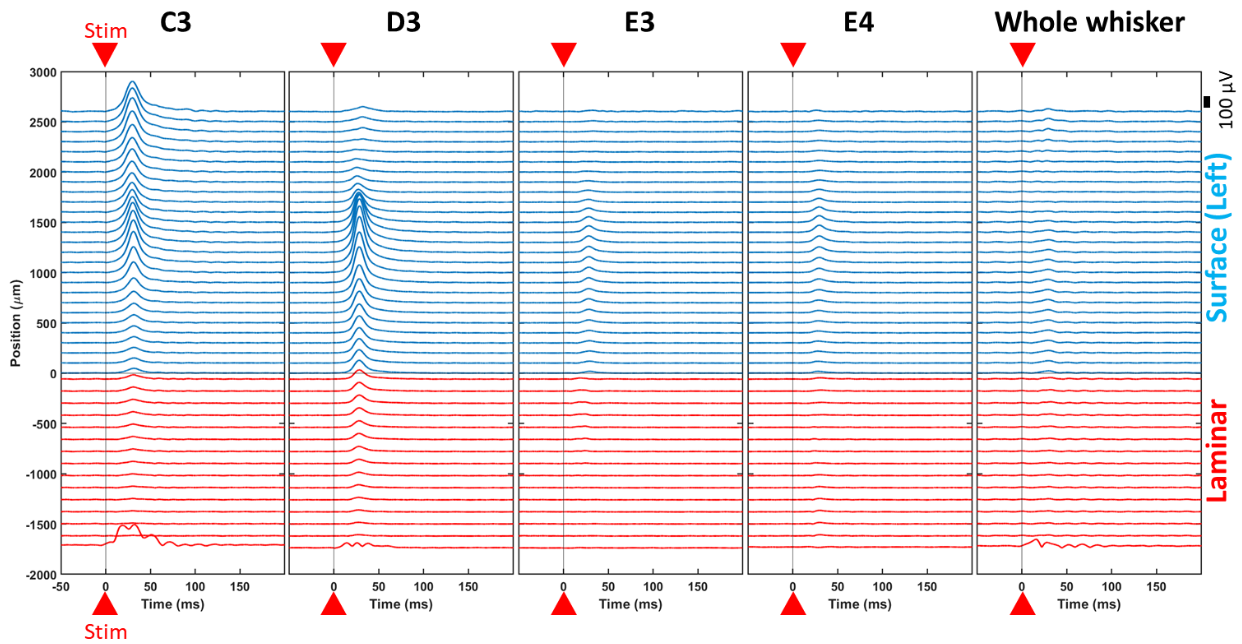
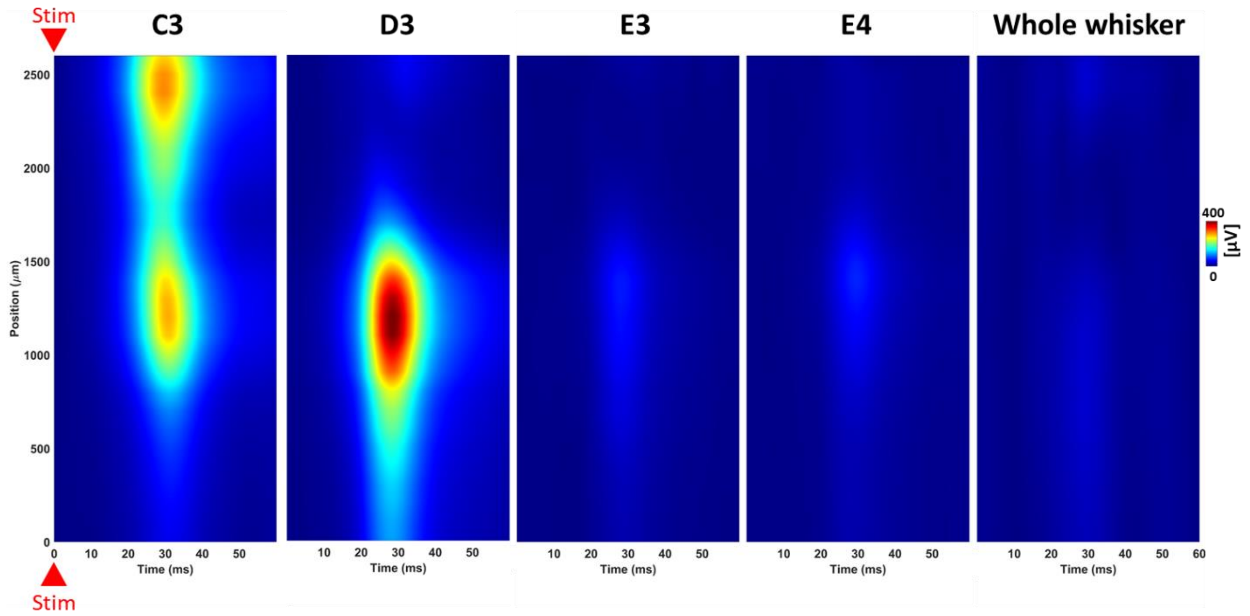


Figure 4.14 HGA profiles evoked by deflection of each whiskers. Blue and red LFP traces correspond to recordings from the surface probe and the laminar probe, respectively. Red triangles indicate the stimulation onset.



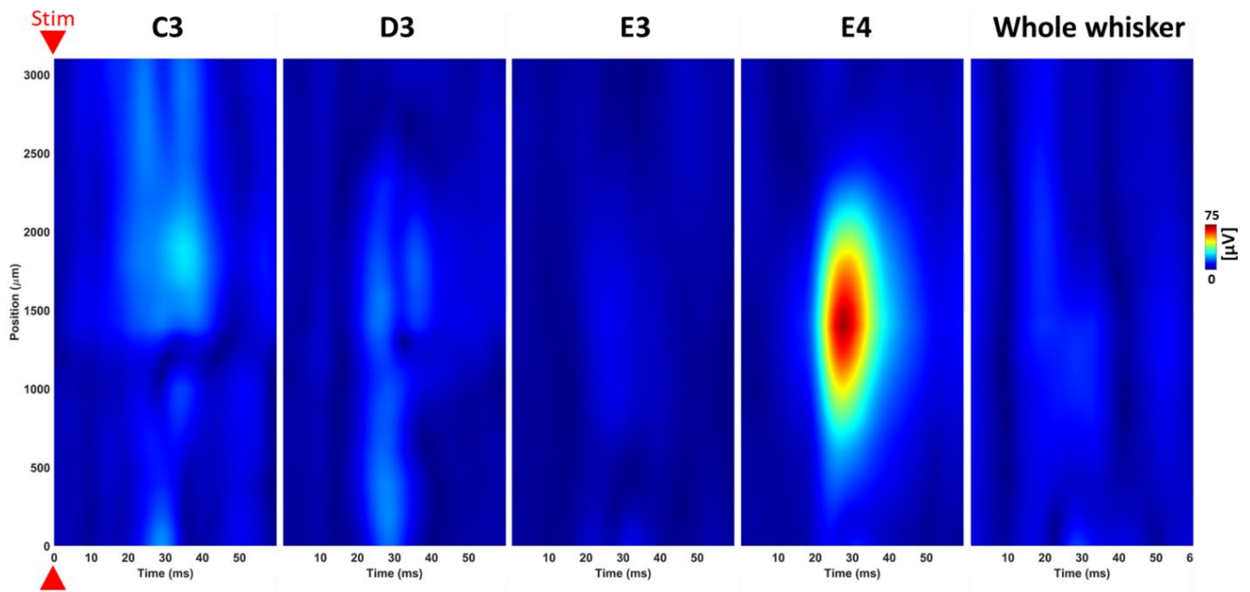


Figure 4.15 Colormap of HGA recorded by the surface probe. (a) Left Column. (b) Right Column. Red triangles indicate the stimulation onset.

4.5 Conclusion

We developed a novel stylet-guided intracortical neural probe with flexible polymer by MEMS based fabrication process. The retractable stylet assisted in insertion of the probe in the cortex without damaging the probe. *In vivo* recordings were performed on rat barrel cortex using a parylene C based ECoG surface probe and a polyimide based laminar probe. LFP, CSD and HGA were investigated for the propagation of evoked potentials by whisker deflection. The results demonstrate the potential for ECoG surface probe and laminar probe recordings can be used for mapping subcortical-cortical circuit connectorization in the brain. The MEMS based fabrication process allows flexibility in design and scalable process which is applicable to the fabrication of long intracortical probes for human recording.

4.6 Acknowledgements

The dissertation author designed all experiments, fabricated the devices, performed all analysis, and co-wrote the chapter 4. The dissertation author thanks Dr. Youngbin Tchoe for the assistance in the rat experiment set-up and the data analysis, Dr. Keundong Lee for assistance in the device fabrication, Dr. Daniel Cleary for assistance in the rat experiment set-up and surgery, Dr. Karen Tonsfeldt for the histology, and Prof. Eric Halgren, Dr. Angelique C. Paulk and Prof. Sydney S. Cash for the helpful discussions. Prof. Shadi A. Dayeh led the project, designed the experiments, performed all analysis, and co-wrote the chapter.

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