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Design of a 100+ meter 12Gb/s/Lane Copper Cable Link Based on Clock-Forwarding

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Design of a 100+ meter 12Gb/s/Lane Copper Cable Link Based on Clock-Forwarding

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical Engineering

by

Tamer A. Mohammed Ali

2012

Abstract of the Dissertation

Design of a 100+ meter 12Gb/s/Lane Copper Cable Link Based on Clock-Forwarding

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Tamer A. Mohammed Ali

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2012

Professor Chih-Kong Ken Yang, Chair

As data centers are expected to manage the increasing demands in bandwidth, processing power and storage requirements, connectivity issues between blades/racks present a whole new set of challenges in maintaining a stable infrastructure. While data centers may grow to occupy thousands of square feet, current passive copper interconnects pose a real limitation with a run length of 10 meters at 10Gbps per wire pair. Optical fiber can extend the interconnection length from 10 meters to 100 meters, but the large power requirements and expensive opto-electric modules prove to be too uneconomical for practical application. As a compromise, through the use of the Infiniband standard, a 12Gbps cable link can be achieved that would extend the range of copper interconnects beyond the 100 meter threshold. The proposed link leverages synchronous clock forwarding on one available data channel that improves jitter tracking, while greatly simplifying the design of the receiver and timing recovery circuits. Only a phase de-skewing is required at the receive side to retrieve the clock-data relationship. In the cable link architecture, the 12 Gbps data is repeated in 8 meter sections with clocking forwarding on a dedicated channel. Then the forwarded clock is dropped off every data repeating stage in order to be multiplied to half the data rate and be used to strobe the incoming data. The longer the quality of clock forwarding is maintained, the cleaner the data strobed at each repeater and the longer the cable can be extended. At each repeater, the clock resets the jitter accumulated from the

previous repeater, allowing for data transmission with as much jitter as in the strobing clock. Determining a fine balance in forward clock frequency is crucial in defining jitter performance of the cable link. Frequency beyond the cable bandwidth results in large attenuation of clock amplitude creating more noise and jitter accumulation along clock repeater. On the other hand, frequency well below the cable bandwidth will increase jitter accumulation time and will degrade jitter performance inside the clock multiplier. The trade-off between low frequency clock jitter accumulation in the Clock Multiplication Unit (CMU) and the high frequency jitter accumulation along the clock repeaters is one of the defining aspects of optimizing the active copper link. To further reduce the clock jitter accumulation across repeaters, phase interpolation between the input clock and the divided output of the CMU is used to generate the forward clock for the next repeater stage. The addition of the phase interpolator has negligible power/area cost, dramatically reduces jitter accumulation, and adds another degree of flexibility in choosing the forwarded clock to reduce the total accumulated jitter. With the proper choice of forward clock frequency, application of the FIR filtering technique and a high performance CMU, a total run length of 115 meters is achieved at 12Gbps data rate.

The dissertation of Tamer A. Mohammed Ali is approved.

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2012

To mom & my beloved wife Ghada ...

whose love, support and kindness

are what made this work come to light

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CHAPTER 1

Introduction

Data centers are managing increasing demands in data volume and processing power. High-performance connectivity between servers and storage within a rack and across multiples racks are necessary to provide sufficient data bandwidth. The type and length of the data connection depends on signaling technology and cost. Passive copper interconnects are the most viable approach of short distances up to 10∼12 meters at 10Gbps per wire pair. Fig. 1.1 shows a data center with an arrangement of racks, where the 12m shaded area shows the reach of passive copper cables. Beyond the 12m range, racks of switches need to be inserted to extend the connectivity, regenerate and repeat the data. This represents an overhead in power and cost to the data center designer. Active copper cables with embedded amplification circuitry can extend the passive copper cable reach, but are typically limited to less than 20m. For longer lengths of exceeding a kilometer, optical fibers are the only option that offers sufficient performance but at substantial cost. Lengths of <150 meters are an intermediate distance that can be particularly suitable for multiple 10Gbps lanes within a data center to connect across a row of racks to core switches at the end of a row.

This work explores an active cable approach based on a source synchronous architecture to extend the range for copper cables to >100 meters for per-pair data rate >10Gbps. Unlike 10GBASE-T signaling, the approach does not require complex symbols at a lower symbol rate across multiple signaling pairs and dissipates ∼4W per port. The proposed link uses low power and area repeaters powered through the cable that can potentially be embedded in the cable.

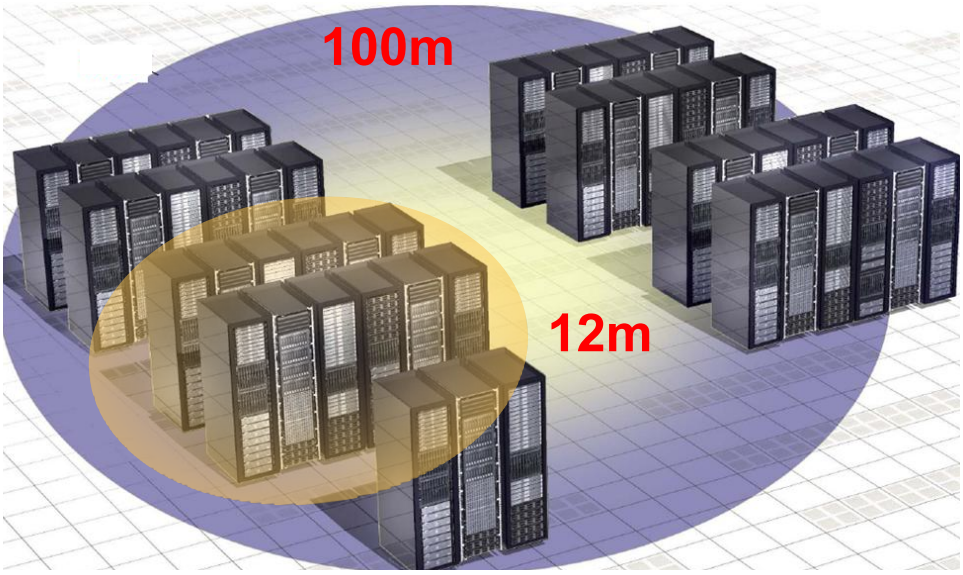


Figure 1.1: A data center showing arrangements of racks that span up to 100m

1.1 Motivation and proposed architecture

Source synchronous links have been proposed and used in server systems for multi-lane high-speed serial link applications such as connecting CPU to CPU, to memory, or to bridge chips due to their inherent tracking of correlated jitter [1–11]. A source synchronous receiver can track jitter in the received data by using a clock that is forwarded from the same transmitter that sends the data. The transmitted clock undergoes almost identical noisy environment as the transmitted data, particularly with similar supply and substrate noise. As a result, data jitter is transparent to the receiver by using the received clock to re-time it. Hence, only static and slowly varying phase offset need to be corrected for using slow phase compensation loops. This approach mitigates the need for fast and power hungry CDRs that are used traditionally in embedded clock link design. In addition, the power and hardware needed for the extra clock channel is usually simpler than the circuits for data transceivers and amortized by using multiple data lanes.

In practice, the correlation between the timing of the clock and the data is weakened when a delay difference between the clock and the data path is present [3]. Excessive delay

can cause correlated jitter in the clock path and data path to add instead of subtract and thus deteriorates the jitter tolerance. For that reason, delay mismatch between clock and data path are minimized. At the same time, uncorrelated noise need to be filtered especially for high frequencies near and above the data bandwidth. In literature, different clock forwarding techniques have been proposed to deal with the aforementioned problem. In [3] a clean-up PLL is used in the clock path at the receiver side. The PLL has sufficient bandwidth to track correlated jitter in the data path, and cut-off high frequency jitter. Another approach uses a DLL [4, 5]. The all-pass characteristic provides jitter correlation between clock and data paths, and jitter does not accumulate within the DLL. Delay has to be matched carefully between the clock and data paths to avoid jitter amplification. Similar to a DLL, an MDLL is used in [7] to multiply a lower frequency forwarded clock to one at half the data rate. As an alternative to an MDLL, an injection locked oscillator (ILO) is used to filter out uncorrelated jitter. Recently, the ILO has drawn more attention in source synchronous links because of its simplicity and wider bandwidth compared to a PLL which in turn enables it to track a wide range of correlated jitter [8–11].

Fig. 1.2 shows a block diagram of the proposed clock-forwarded cable-link architecture. The forwarded clock tracks the jitter of the data across a wide frequency range. At each repeater stage, the data signal is equalized, amplified, and retimed by the forwarded clock before being transmitted. Since, the relative jitter between the clock and the data is reset when the signal is retimed, the data repeating distance (or cable section) is defined mainly by the distance that can be easily transmitted with little power cost. Clock is transmitted on a separate channel without equalization. The clock frequency is a system variable that is determined using the model presented in the next section. A CMU multiplies the clock frequency from the forwarded frequency to half the data rate in each repeater. The clock and data repeating distance are not constrained to be the same. As seen from Fig. 1.2, clock can be tapped at each data repeating stage for frequency multiplication and retiming, and amplified/buffered at each clock repeating stage.

The critical challenge in a repeating a source-synchronous system is the accumulation

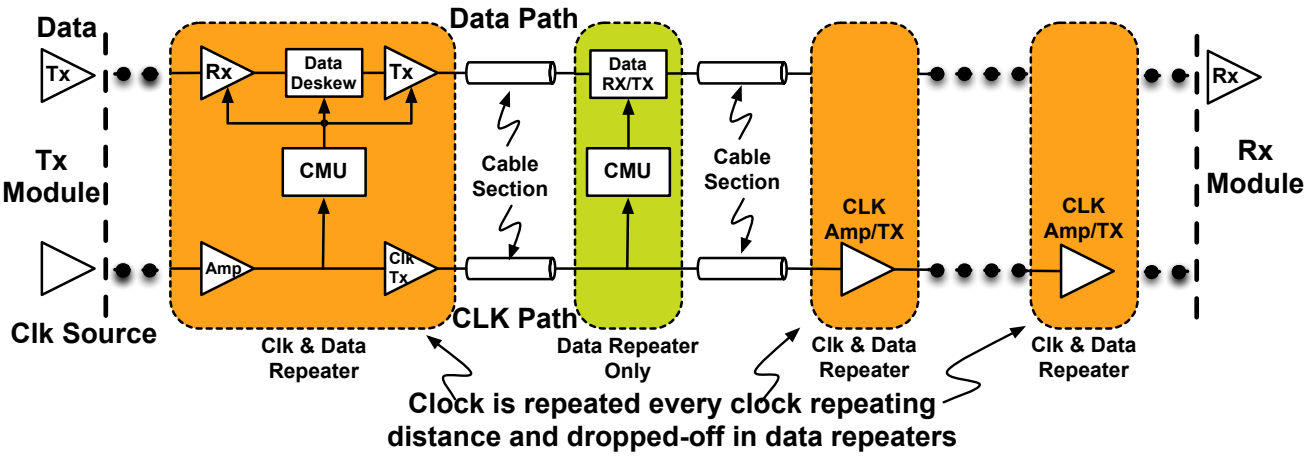


Figure 1.2: Synchronous repeater-based cable link architecture

of clock jitter. Hence, maintaining a clean clock is the focus of this thesis. Determining a fine balance in forward clock frequency is crucial in defining jitter performance of the cable link. Frequency beyond the cable bandwidth results in large attenuation of clock amplitude creating more noise and jitter accumulation along clock repeater. On the other hand, frequency well below the cable bandwidth will increase jitter accumulation time and will degrade jitter performance inside the clock multiplier. The trade-off between low frequency clock jitter accumulation in the Clock Multiplication Unit (CMU) and the high frequency jitter accumulation along the clock repeaters is one of the defining aspects of optimizing the active copper link. We propose an FIR jitter filtering technique that requires little area and power cost, but drastically reduces clock jitters accumulation. We also utilize a programmable PLL/MDLL clock multiplication unit (CMU) to verify and compare different clock configurations along the repeated link.

1.2 Organization

The dissertation is composed of seven chapters. Chapter 2 gives the necessary overview on the most common repeater designs used nowadays and common clock multiplication topolgoies. The chapter then presents background on most commonly used CMU architectures.

An overview on jitter metrics is also provided in this chapter, together with analysis of jitter on basic building blocks; an inverter and a differential pair. In Chapter 3, we propose a fast and accurate model for modeling clock forwarded repeater links. We use the model to evaluate link design space and different system parameters. In Chapter 4, system and implementation details are presented. We present a configurable and high speed clock multiplication PLL/MDLL in this chapter that is more than twice the speed of MDLLs published in literature. The experimental results are shown in Chapter 5. Chapter 6 concludes the work, list the contributions and offers some ideas for future work.

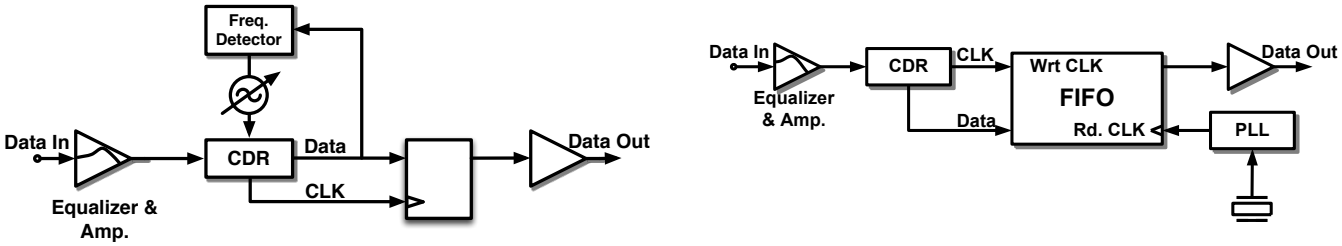
CHAPTER 2

Background

In this chapter a necessary background is covered to pave the way for the rest of the dissertation. The chapter starts with an overview on the most common repeater topologies that are used in the industry. It's then followed by background information on clock multiplication topologies used in high speed IO design. Timing jitter definition and metrics that will be used throughout this dissertation are explained in the third section. The chapter closes with jitter calculation in basic repeater building blocks.

2.1 Common Repeater Architectures

Two repeater architectures are commonly used: referenceless CDR-based repeater and fully-synchronized repeater. Fig. 2.1(a) shows a block diagram of a referenceless CDR, where phase acquisition occurs by connecting the VCO to a CDR loop where its frequency, and thus phase, is locked to the incoming data stream. The lock range is usually narrow and a frequency detector is often used to bring the VCO center frequency close to the data rate. This architecture poses the traditional trade-off between jitter filtering and the jitter tracking requirements by the CDR loop [12]. The CDR needs to have tight bandwidth in order to filter incoming data jitter. Nevertheless, it should have wide enough bandwidth so that recovered clock can tolerate and track data jitter to minimize bit error rate due to timing wander and low-frequency noise. Jitter peaking is another system parameter that presents challenge in the design of referenceless CDR repeater. Peaking in the transfer function of the CDR due to phase margin less than 60^0 causes jitter amplification at the peaking frequency. Cascading multiple repeaters can cause excessive jitter accumulation at



(a) Referenceless CDR repeater

(b) Full synchronizer with FIFO repeater

Figure 2.1: Most common repeaters architectures

the peaking frequency which deteriorates the overall system performance and its tolerance to jitter. In addition, design of a frequency detector that covers a very wide range requires additional specialized circuits [13–16]. An alternate architecture is the fully-synchronized repeater shown in Fig. 2.1(b). The architecture is similar except that a FIFO buffer is used to decouple the jitter filtering from the jitter tracking requirements. The CDR can thus have wide bandwidth for better tracking, and a clean oscillator/PLL is used at the output to read data from a FIFO buffer. The FIFO buffer handles any timing wander or frequency mismatch in the system. A driver, synchronized to the clean clock, transmits the data to the next repeater. This repeater is more robust but comes at the expense of more power and area due to the FIFO and clean oscillator/PLL.

2.2 Common Clock Multiplication Unit Architectures

Link designers use different schemes for multiplying reference clock frequency to data rate clocks. The most common are PLLs and MDLLs. In this section we will discuss the major differences between them, and introduce equations that model their behavior and transfer functions to help understand their response to different stimulus and noise sources.

2.2.1 Phase Locked Loops

PLLs are commonly used to provide accurate timing signals for both transmit and receive sides of a high-speed link. In its simplest form, a PLL is a 2nd order feedback system that

generates a clock signal whose output phase is aligned with respect to the phase of an input reference clock. Since phase is the integration of frequency, once the phases are aligned, both phase and frequency are locked. This alignment is achieved by comparing the phase of the output clock with the phase of the reference. Any resulting difference in phase, the phase error, feeds into a block that filters this error and generates a control signal, typically a voltage. A voltage-controlled oscillator, where the oscillation frequency changes as a function of the control voltage, then creates the output clock. Through negative feedback, the control signal forces the output clock phase to be aligned with the input clock phase, resulting in zero phase error.

Fig. 2.2 shows a 2^{nd} order PLL block diagram. It consists of a VCO (a ring based VCO is shown in the figure), a phase frequency detector (PFD), charge pump (CP), and a first order loop filter (The R and C in the diagram). The PLL can be modeled by a continuous time model if the closed-loop bandwidth is much smaller compared to the input reference clock frequency [17]. The closed loop phase transfer function from the reference input to VCO output is given by:

$$TF_{PLL}(s) = \frac{2s\xi\omega_n + \omega_n^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{2.1}$$

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi CM}}, \xi = \frac{R}{2}\sqrt{\frac{I_{CP}K_{VCO}C}{2\pi M}} \tag{2.2}$$

$$\omega_{-3dB} = \omega_n\sqrt{1 + 2\xi^2 + \sqrt{(1 + 2\xi^2)^2 + 1}} \tag{2.3}$$

Where I_{CP} is the charge pump current, and K_{VCO} is the gain of the VCO, which represents the change in oscillation frequency with respect to the control voltage (expressed in Hertz/V), ω_n is the natural frequency and ω_{-3dB} is the -3dB corner frequency of the transfer function. The transfer function is a second-order low-pass transfer function suggesting that if input phase varies rapidly due to high-frequency noise, then VCO output phase cannot track this variation. In other words, low-frequency jitter at the input propagates to the output unattenuated, but high-frequency jitter gets filtered out.

Another important transfer function is the VCO noise output transfer function $NTF_{VCO}(s)$

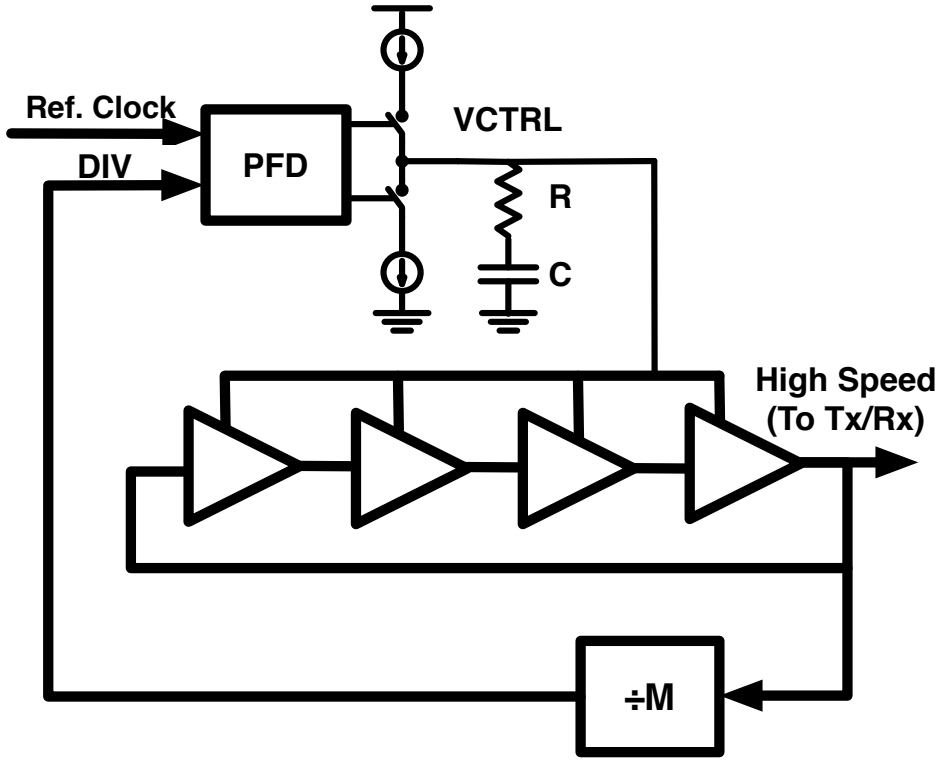


Figure 2.2: Block diagram of a ring oscillator based PLL

given by:

$$NTF_{VCO}(s) = \frac{s^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{2.4}$$

The PLL output noise transfer function has a high-pass characteristic. This indicates that low-frequency jitter components generated by the VCO are suppressed by the loop response, but high-frequency jitter components pass through the loop. This can be understood as follows. The PLL loop needs some time for the phase error generated at the VCO output to propagate thought the loop filter and to adjust the VCO frequency to correct this error. If the frequency content of the jitter is too high, the error produced by the PFD is mostly attenuated by the poles in the loop. This poses a tradeoff in PLL design. Systems dominated by noise on the reference clock benefit from a low-bandwidth PLL while systems dominated by noise at the output require high bandwidths to minimize jitter. Depending on applications and environments, one or both noise sources may be significant, requiring an optimum choice for the loop bandwidth.

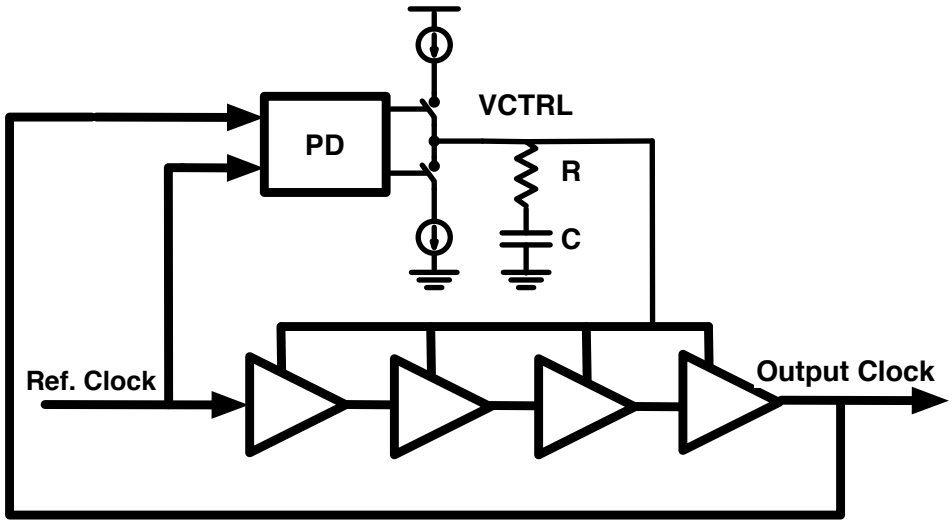


Figure 2.3: Block diagram of a DLL

2.2.2 Delay Locked Loops

Like the PLL, a DLL can also provide an accurate timing relationship between an input clock and output clock. Therefore, it is also a viable option for clock generation in a high-speed link. A DLL utilizes a voltage-controlled delay line (VCDL) to generate an output clock that is a delayed version of the input clock, where the delay through the VCDL is a fixed fraction (often 50% or 100%) of the input clock period. While there are several ways to implement a DLL, Fig. 2.3 presents a block diagram of a commonly-used charge pump based DLL topology. A phase detector (PD) measures the phase difference between coincident edges of the input and output clocks of the VCDL. The charge pump (CP) generates pulses of charge, proportional to the phase error, which is then integrated by the capacitor in the loop filter (LF). The resulting voltage out of the LF sets the magnitude of the control voltage (Vctrl) that determines the delay through the VCDL. Since the reference clock also feeds into the input of the VCDL, delay through the VCDL is fixed with respect to the period of reference through negative feedback.

A DLL is inherently simpler and easier to stabilize than a PLL [18]. The VCO in a PLL must change frequency in order to adjust its output phase, introducing an integrator. In

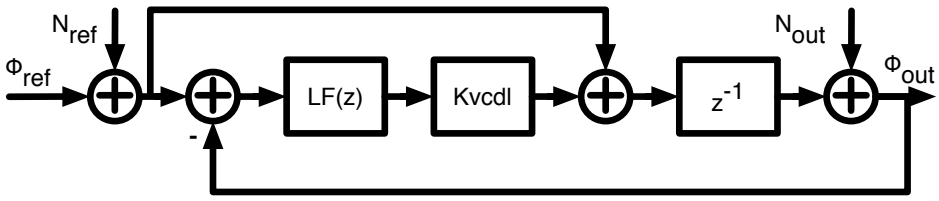


Figure 2.4: DLL discrete time z model

comparison, the phase of the clock edge out of the VCDL is directly controlled by Vctrl, which corresponds to a simple gain without integration. Hence, a DLL can be designed as a first-order loop and obviates adding proportional control to stabilize the loop. Moreover, frequency detection is not needed since the input and output clocks nominally have the same frequency.

DLL is better modeled by a discrete time z-domain because of the presence of a delay line that produces 1 clock cycle delay. A continuous time model can capture the delay effect but it ignores the impact of this delay on the sampling nature of the loop and its dynamics. Fig. 2.4 shows the z-domain model of the DLL. K_{vcdl} is the delay line gain in radians per cycle per volt. $LF(z)$ is the loop filter transfer function. After combining the phase correction term with the input reference clock phase, a one-cycle delay is applied. Supply noise modulates the delay of the VCDL and its effects are modeled by simply adding a noise term, N_{out}, before the output node.

Since a compensating zero is not required, the combined CP and LF transfer function is simplified with a single integrating capacitor. T_{ref} is the period of the input reference clock. the pole at the origin formed by the integrating capacitor in LF can be replaced by the factor $1/(1-z^{-1})$ in z-domain [19]. The z-domain transfer function from the input to the output is therefore given by:

$$TF_{DLL}(z) = \frac{(1+K_{VCDL}K_{CP})z-1}{z^2-z(1-K_{VCDL}K_{CP})}, K_{CP} = \frac{I_{CP}T_{ref}}{2\pi C} \tag{2.5}$$

The z-domain model can also be used to derive the DLL noise transfer function from

noise at the VCDL output to the DLL output. The expression is given by:

$$NTF_{VCDL}(z) = \frac{z-1}{z-(1-K_{VCDL}K_{CP})} \tag{2.6}$$

Similar to the PLL, the DLL output noise transfer function also has a high-pass characteristic, similar to that seen for a PLL. The high-pass corner frequency corresponds to the bandwidth of the loop. While the NTF responses of both the PLL and DLL are similar, there is an important distinction to point out. In a PLL, the output phase can only move by changing the VCO frequency, while in a DLL, the loop can directly move the output phase by adjusting the delay through the VCDL. This difference enables the DLL to respond much more quickly to noise injected at the output. Moreover, power supply noise is a dominant source of noise that must be dealt with in order to achieve low jitter. The VCDL used in a DLL has the added advantage of not accumulating the noise, as opposed to the VCO in a PLL. Therefore, power-supply noise that may couple into the VCDL only affects the output phase over a single clock period.

Fig. 2.5 shows the transfer functions of the PLL and the DLL for different bandwidth settings. As seen from the plot, the DLL transfer function is all-pass, peaking is observed in the transfer function with increase in bandwidth. The peaking can be reduced by increasing the DLL filter order [19]. The PLL is thus adequate when noise is dominated by clock input noise as the PLL low pass filters this noise, while the DLL is more adequate for systems that have clean input clocks and noisy supply and substrates because the DLL VCDL doesn't accumulate supply noise as the VCO inside the PLL does.

2.2.3 Realigned PLL and MDLL

Re-aligned PLL (RPLL) is another approach to clean up the accumulated VCO-induced jitter periodically [20,21]. The topology performs VCO phase realignment by injection locking the VCO to a strongly buffered version of the PLL reference clock at fixed intervals of the reference clock. Fig. 2.6 presents a block diagram of this topology. A buffered version of reference clock is injected into one of the delay cells in the VCO every reference cycle to pull

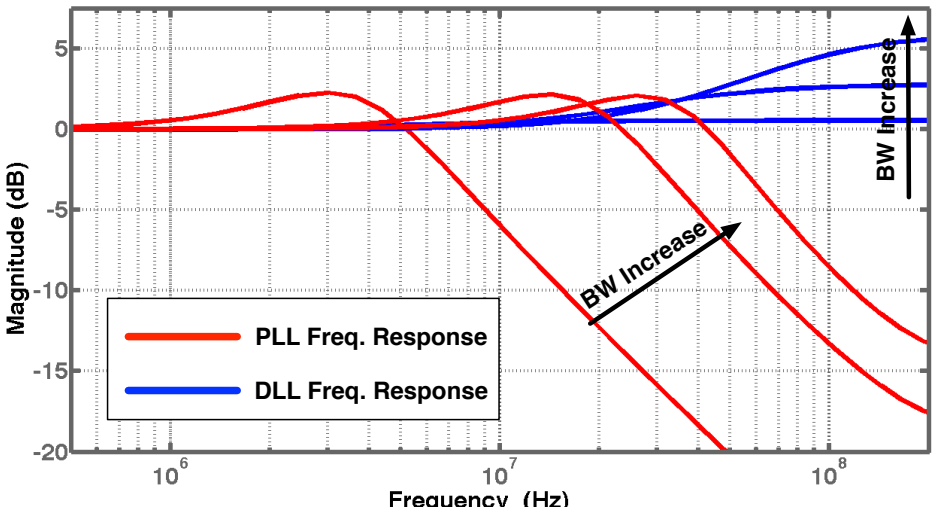


Figure 2.5: PLL and DLL transfer functions for bandwidth=1%,5%, and 10% of the reference frequency

the VCO internal clock edge toward the ideal position. If the amount of phase error correction is big enough to correct the phase difference between the buffered reference and the internal clock edge prior to the realignment, all the memory of the past errors at the VCO output clock can be completely suppressed. If the reference clock is clean, the accumulated noise in the VCO can be suppressed by resetting the accumulated phase error; thus, improving the supply noise rejection of the RPLL by realignment. The relative strength of the injection locking buffer to the delay cells in the VCO determines the amount of phase realignment performed. The injection operation is synchronized by a SEL pulse that is derived from the VCO output clock.

The main drawback in this topology stems when there is a difference in delay through the reference clock injecting buffer versus the VCO buffers the injection can create a phase mismatch between the reference clock edge and the output edge out of the VCO. This can lead to pattern jitter at the VCO output set by the periodicity of injection. This corresponds to a strong injection-induced spur when observing the spectrum of the output clock. A solution to resolve this problem will be proposed in chapter 4.

The topology can be extended to multiply the input clock by adding a divider in the

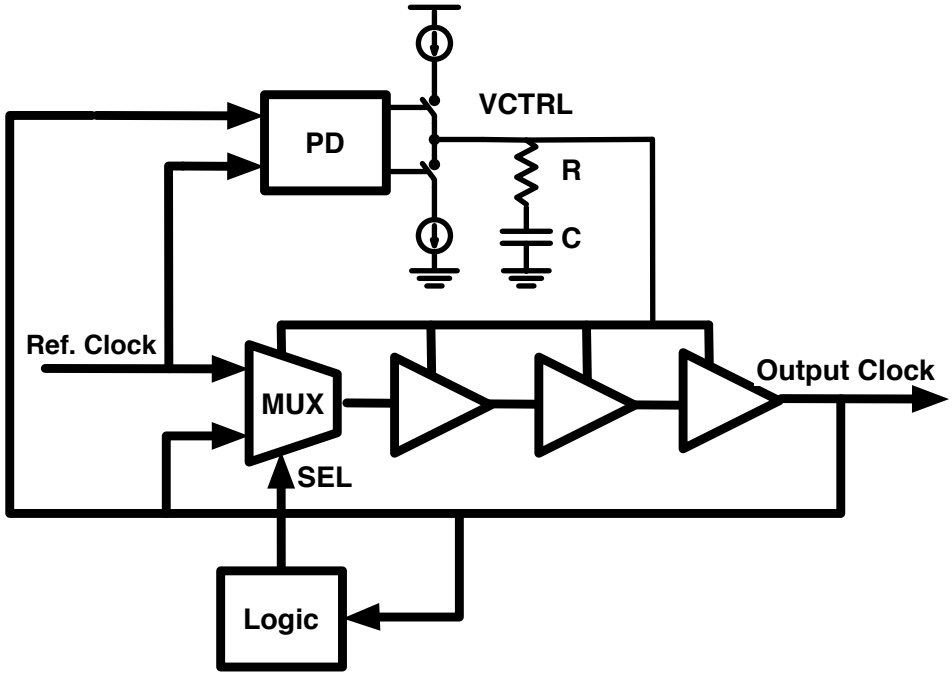


Figure 2.6: Realigned PLL block diagram

feedback path [22], which gives the circuit the name "Multiplying DLL" or (MDLL). The MDLL loop dynamics are similar to the DLL. This is because the injection happens at the reference frequency rate which makes the MDLL behaves as an DLL running at the reference frequency, while the VCO integration happens at the multiplied frequency in an open loop manner.

2.3 Timing Jitter and Its Metrics

Time (or phase) jitter is a key measurement in systems where the periodic behavior or exact event timing is crucial to system performance. The design process for high performance, low cost devices in today's communication systems requires comprehensive methods for modeling and analyzing both jitter and noise. Jitter measures undesired fluctuations in the timing of events; In oscillators and frequency synthesizers period jitter quantifies the time domain uncertainty of the output signal. In digital design period jitter describes the misalignment of the significant edges of a digital signal from their ideal position in time [23].

In communication systems, "jitter is an abrupt and unwanted variation of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles or the frequency or phase of successive cycles" [24].

Jitter can be considered as an undesired perturbation in time. A noisy signal can be represented as a noise-free signal $v_{ideal(t)}$ displaced in time with a stochastic process j(t). The noisy signal is modeled by:

$$v_n(t) = v_{ideal}(t + j(t)) \tag{2.7}$$

The voltage noise at the point where the threshold is crossed causes the time shift of the edge by way of the slew rate of the signal as shown Fig. 2.7, and as expressed in the following equation:

$$v_n(t_0) = v_{ideal}(t_0) + n(t_0) \tag{2.8}$$

$$\sigma_{j(t_0)} \cong \frac{\sigma_{n(t_0)}}{\frac{d}{dt} v_{ideal}(t_0)} \tag{2.9}$$

The $\sigma^2_{j(t_0)}$ is the expected value of the square of the deviations of a random signal from its mean value and t_0 is the time of the threshold crossing. Because the noise is assumed to be small enough that it does not affect the solution in any way that will significantly change the signal, we can approximate the actual signal slew rate with the slew rate you get from the ideal, jitter free, large signal model.

Various jitter metrics characterize the statistics of the observed sequence of events. When a periodic system has a reference time point, you can consider all other events in relation to that time point. For a driven system, such an event can occur when the periodic input signal crosses through a particular threshold value. The periodic output signal generates an ideal sequence of events in response to the input signal, separated by the period T of the system. Ideally the delay from the input edge to the output edge is a constant t_{delay}. This sequence of same direction threshold crossings by the output signal expects periodic threshold crossings

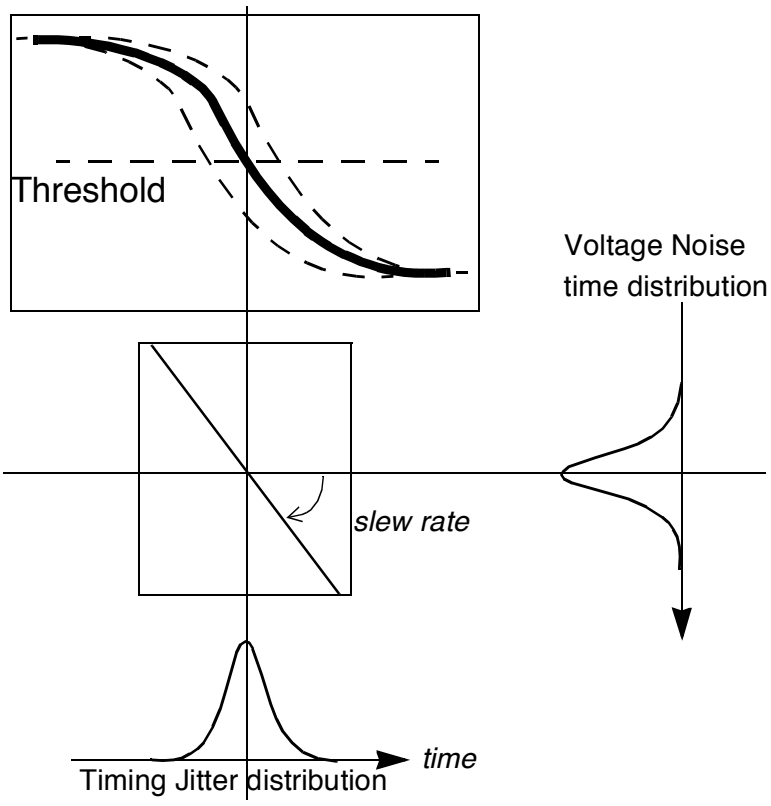


Figure 2.7: Noise to jitter conversion

at times $iT + t_{delay}$ where the events are indexed with i [23]. The uncertainty is represented by the sequence:

$$\delta t_i = t_i - (iT + t_{delay}) \tag{2.10}$$

This variation in the delay between a triggering event and a response event is the absolute jitter as shown in Fig. 2.8. It can be represented by:

$$\sigma^2_{abs} = \sqrt{E[t_i^2]} \tag{2.11}$$

Where $E[t_i^2]$ is the variance of zero crossing uncertainty defined in equation (2.10). Assuming wide-sense-stationary timing uncertainty, absolute jitter in equation (2.11) can also be represented by Weiner-Khinchin theorem:

$$\begin{aligned} \sigma^2_{abs} &= R(0) \\ &= (\frac{T}{2\pi})^2 \int_0^\infty S_\phi(f) df \end{aligned} \tag{2.12}$$

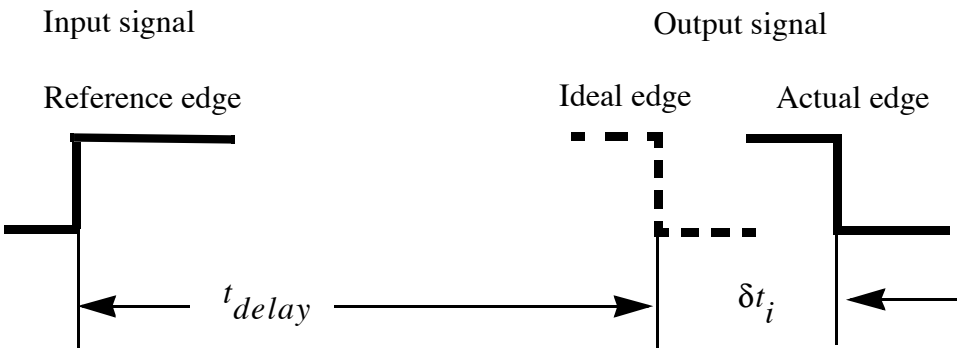


Figure 2.8: Absolute Jitter

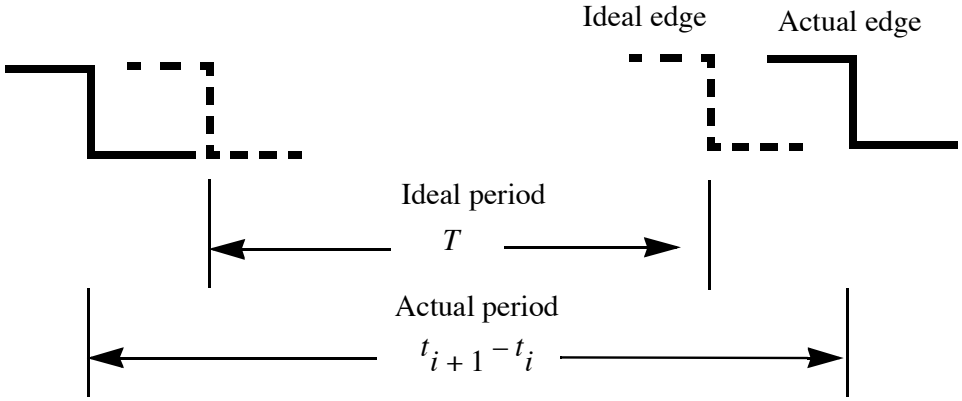


Figure 2.9: Cycle Jitter

Where $R(0)$ is the jitter auto-correlation function $R(t)$ for a time separation of $t = 0$, $S_\phi(f)$ is the single-sided phase noise power spectral density of absolute jitter.

The cycle or period between two similar output signal transitions is affected by the noise on both edges. The variation in the length of the period from the ideal value (as expressed in Equation (2.13)), is characterized by the standard deviation also known as the period jitter or cycle jitter, as shown in Fig. 2.9 and Equation (2.14).

$$J_c(i) = t_{i+1} - t_i - T \tag{2.13}$$

$$\sigma_{cycl} = \sqrt{E[(t_{i+1} - t_i)^2]} \tag{2.14}$$

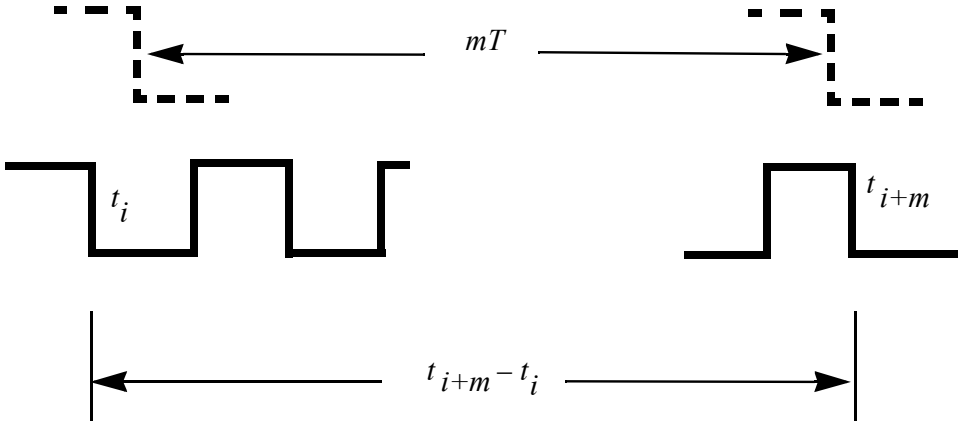


Figure 2.10: m Cycle Jitter

If two transitions are separated in time by m cycles or periods, as shown in Fig. 2.10, the standard deviation of the length of m cycles from nominal is computed using the following sequence:

$$J_c(mT) = t_{i+m} - t_i - mT \tag{2.15}$$

The standard deviation of the m cycle jitter is obtained by:

$$\sigma_{cycl}(mT) = \sqrt{E[(t_{i+m} - t_i)^2]} \tag{2.16}$$

The m cycle jitter can also be obtained in terms of the absolute jitter by:

$$\sigma^2_{cycl}(mT) = 2R(0) - 2R(mT) \tag{2.17}$$

Applying Weiner-Khinchin theorem and assuming wide sense stationary noise, the m cycle jitter can be found by:

$$\sigma^2_{cycl}(mT) = (\frac{T}{\pi})^2 \int_0^\infty S_\phi(f) sin^2(\pi f mT) df \tag{2.18}$$

In most practical systems, noise is limited to the system bandwidth f_h. For example, in a bandwidth limited system with a white noise power spectral density S_ϕ, m cycle jitter is

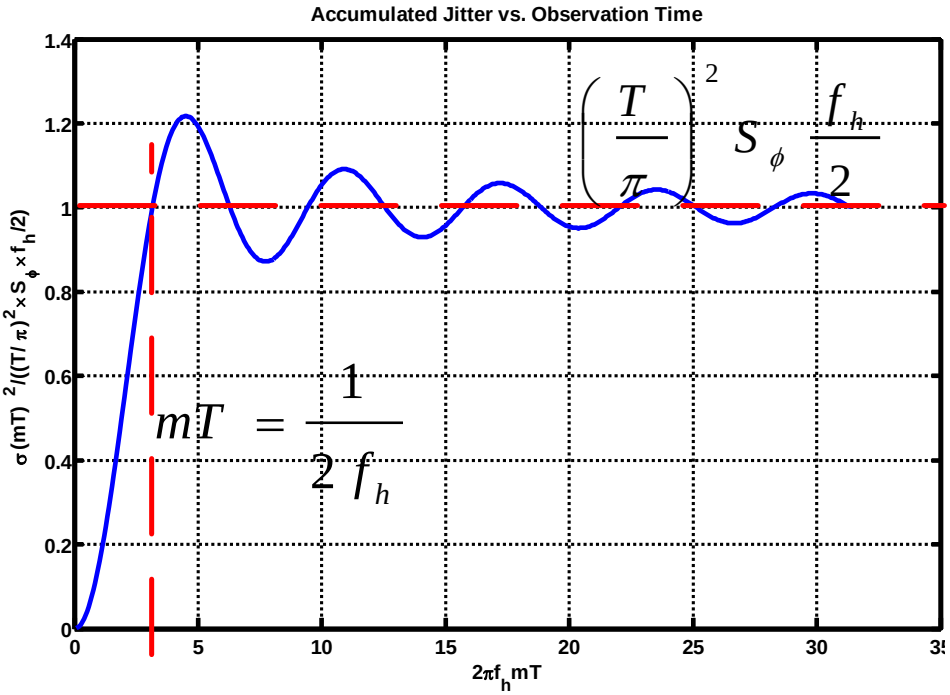


Figure 2.11: Jitter accumulation in bandwidth limited system with bandwidth f_h and PSD S_ϕ

given by:

$$\sigma^2_{cycl}(mT) = (\frac{T}{\pi})^2 S_\phi \int_0^{f_h} sin^2(\pi f mT) df \tag{2.19}$$
$$= (\frac{T}{\pi})^2 S_\phi \frac{f_h}{2} \left(1 - \frac{sin(2\pi f_h mT)}{2\pi f_h mT}\right)$$

Fig. 2.11 plots the jitter accumulation in a bandwidth limited system. Jitter accumulates to a long term value ($mT \to \infty$) that's equivalent to the square root of the absolute jitter. A result that can also be reached from Equation (2.17)

2.4 Noise and Jitter in Basic Circuits

Before discussing noise and jitter of clock repeater, we will provide a brief overview of jitter in the basic circuits comprising the clock repeater; namely inverter stage and differential pair

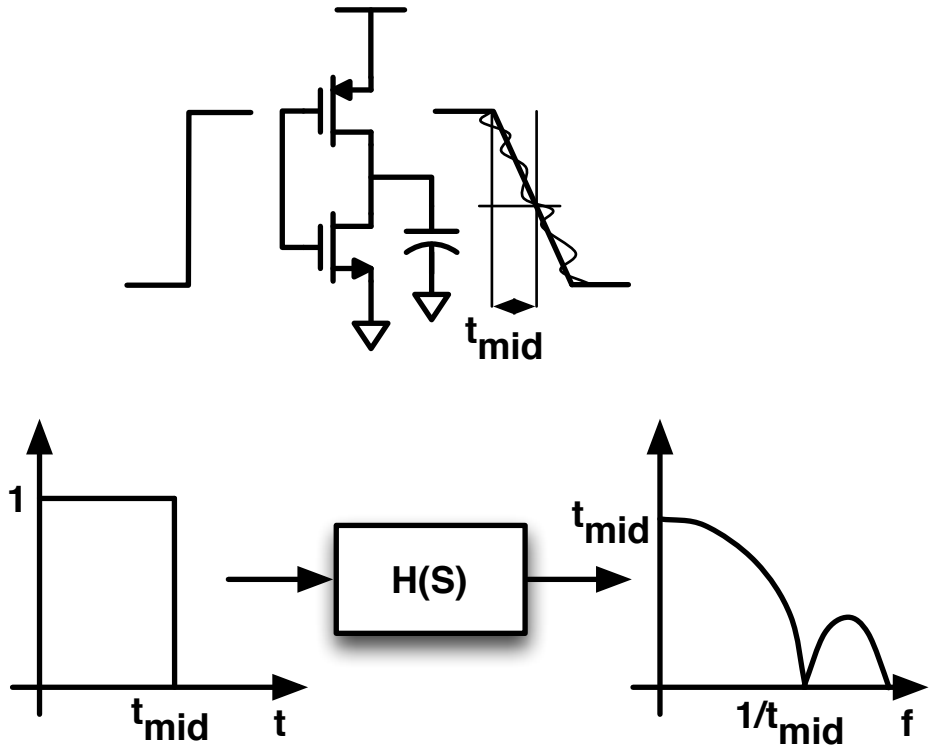
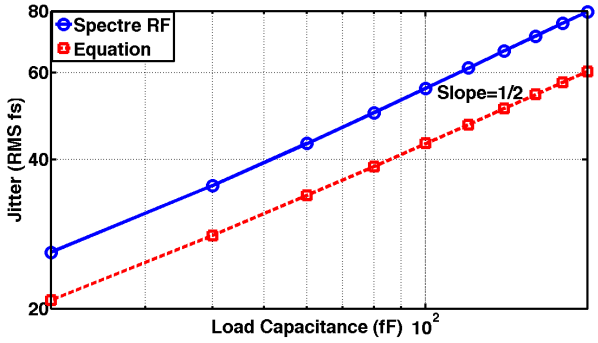


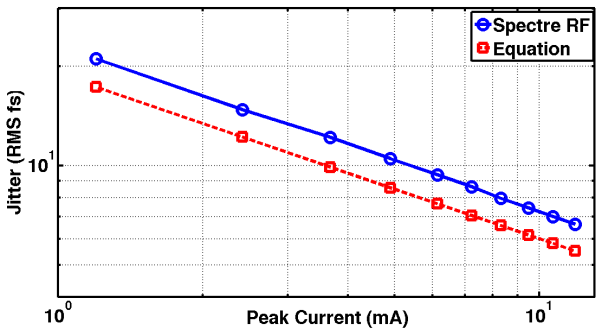
Figure 2.12: Noise in inverter stage

stage. Inverter jitter can be calculated by assuming the inverter input toggles momentarily. As a result, one of the inverter devices switches off and the other turns on immediately. The switched on device will start charging the load capacitance with the device on-current. During this time, the noise current will also start accumulating noise voltage on the load capacitance. This will continue until the voltage at the load capacitance reaches the tripping point for the next stage, e.g. time to reach mid supply t_{mid}. Thus, as shown in 2.12 inverter noise can be represented by:

$$\begin{aligned} v_n(t) &= \frac{1}{C}\int_0^{t_{mid}} i_n(t)\,\mathrm{d}t \\ &= \frac{1}{C}\int_{-\infty}^{\infty} i_n(t)h(t_{mid}-t)\,\mathrm{d}t \end{aligned} \tag{2.20}$$



(a) Inverter Jitter vs. C at constant I



(b) Inverter Jitter vs. I at constant fan-out, i.e. constant t_{mid}

Figure 2.13: Inverter jitter vs. load capacitance and current

By taking Fourier transform of the noise auto-correlation function, noise power spectral density (PSD) can be found to be:

$$S_{v_n} = \frac{1}{C^2} H^2(f) S_{i_n} \tag{2.21}$$

From which, jitter power spectral density S_{t_j} can be evaluated by dividing noise PSD by the square of the voltage slope $(\frac{I}{C})^2$:

$$S_{t_j} = \frac{1}{I^2} H^2(f) S_{i_n} \tag{2.22}$$

Jitter can be evaluated to be:

$$\begin{aligned} \sigma_{t_j}^2 &= \frac{1}{I^2} \int_0^\infty H^2(f) S_{i_n} \, \mathrm{d}f \\ &= \frac{t_{mid}}{\pi I^2} S_{i_n} \int_0^\infty \frac{sin(\pi f t_{mid})^2}{(\pi f t_{mid})^2} \, \mathrm{d}(\pi f t_{mid}) \\ &= \frac{4KT\gamma t_{mid}}{I(V_{DD} - V_t)} = \frac{2KT\gamma V_{DD} C}{I^2(V_{DD} - V_t)} \end{aligned} \tag{2.23}$$

Where I is the device saturation current, C is the load capacitance, and V_{DD} is the supply voltage. Fig. 2.13 shows the jitter of the inverter stage using (2.23) vs. jitter simulation performed by Spectre RF.

Similar analysis can be followed to obtain jitter for a differential pair, albeit differential pair can be operating in either a soft or hard switching mode. Soft switching occurs when

the amplitude of the input signal v_{in} doesn't cause steering of the amplifier total current, and it's amplified by gain A. Given g_m is the transconductance of the differential pair with a load resistance of R, capacitance of C, and a gain of A. Soft switching jitter can be found from:

$$\sigma^2_{tj,soft} = \frac{2KT\gamma g_m R}{C} \frac{1}{(A\frac{d(v_{in})}{dt})^2} \tag{2.24}$$

On the other hand, hard switching of the differential pair occurs when input signal is large enough, such that the tail current I is full steered in one direction. The output voltage thus slews towards its final value. Assuming a very short transition period where differential pair transistors are conducting simultaneously, jitter at the output solely depends on the tail current noise and its transconductance $g_{m,t}$. Jitter can be estimated by:

$$\sigma^2_{tj,Hard} = \frac{2KT\gamma g_{m,t} t_{mid}}{C^2(\frac{d(v_{out})}{dt})^2} \approxeq \frac{2KT\gamma g_{m,t} t_{mid}}{I^2} \tag{2.25}$$

The assumption here is that the load time constant RC is big enough such that the accumulated noise doesn't discharge considerably. Equation (2.25) of hard switching jitter of a differential pair is equivalent to inverter jitter in (2.23).

2.5 summary

In this chapter we shed the light on some necessary background to our work. We started with a brief on most common repeater architectures. Then we gave an overview on different CMU topologies; PLLs, DLLs and MDLLs. Transfer function of PLL shows that they are ideal for systems that have high reference clock jitter, but they suffer from supply noise accumulation inside the VCO. DLLs and MDLLs on the other hand are inadequate for systems that have noisy reference clock due to the all-pass nature of its transfer function. However, due to the use of the VCDL instead of a VCO, supply noise is not accumulated inside DLLs and MDLLs and it's more adequate for use in systems that have clean reference clock. The chapter then covers basic jitter definitions and metrics. Primarily, it distinguished between the definition of absolute jitter and period jitter. Those are important jitter metrics that will be used

in subsequent chapters. The chapter closes with derivations for the jitter in basic building blocks; the differential amplifier and the inverter.

CHAPTER 3

Modeling and Analysis of Repeater Based Source Synchronous System

This chapter deals with the modeling and analysis of the cable link; primarily the clock repeater which lies at the heart of the link. An overview on the clock repeater is given followed by a discussion on noise and jitter accumulation in the clock repeater. A semi-analytical model is then developed that allows us to predict the jitter accumulation across the link. This allows us to examine the design space for the proposed link and the power/jitter trade-offs. The chapter closes with a new simple and effective method for filtering clock jitter based on FIR filtering. The method is compared to PLLs and LC resonance filters.

3.1 Clock Repeater Overview

The clock path repeater is shown in Fig. 3.1. The clock is first amplified in a 100Ω terminated 3-stage differential receiver followed by a limiting amplifier that produces digital levels. The CMU input is fed from CMOS buffers. Output of the amplified clock and a divided version of the CMU are inputs to a phase interpolator. The role of this phase interpolator as a filter is discussed in subsequent sections. A clock driver sends the clock to the next cable section. This work uses a differential wire pair for sending the clock. The cost of the added wires can be amortized when using multiple data lanes. Alternatively, the clock can be sent embedded as the common-mode component of differential data lines [25].

Power for each data or clock repeater is provided through the cable. Many standards include wires for power with well-defined maximum voltage and current. Infiniband [26],

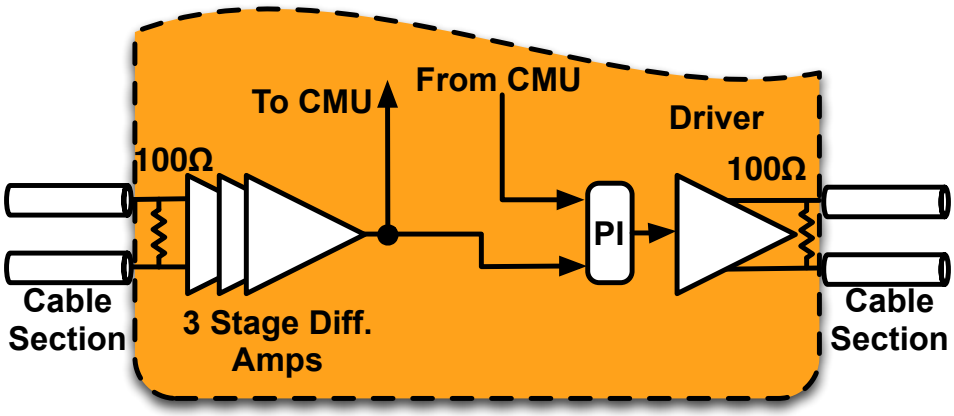


Figure 3.1: Block diagram of clock repeater

HDMI [27], and Thunderbolt [28] are a few examples of standards. The two wires for power can also be reduced by combining the clock and power wires by launching the power across signal lines as in Power over Ethernet (POE) [29] applications.

Clock doesn't need equalization and clock frequency can be chosen arbitrarily provided that we have a clock multiplication unit (CMU) in each repeater. Hence, clock repeating distance need not be the same as the data repeating distance. Practically, clock path needs less repeaters than data path. As seen from Fig. 1.2, clock is dropped-off at each data repeating stage for frequency multiplication, if needed, and retiming, while it's repeated only each clock repeating distance.

3.2 Noise and Jitter Discussion

3.2.1 Repeater Noise and Jitter

The incoming clock signal is amplified through the cascade of repeater gain stages. Depending on its amplitude, the clock amplitude saturates within few stages. The gain then drops to almost unity throughout the remain gain stages. For that reason, noise propagation inside the clock repeater can't be modeled with the traditional linear time invariant model, even though noise is still considered small signal. Instead, the problem needs to be solved using

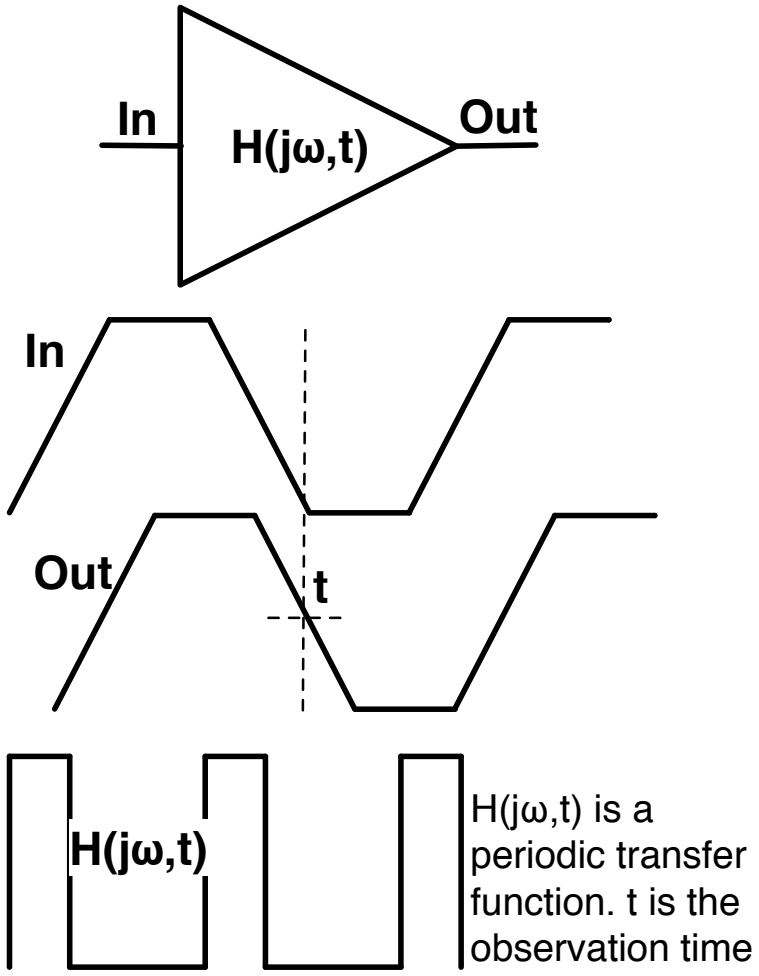


Figure 3.2: Input, output and transfer function $H(j\omega_o, t)$ waveforms for a gain stage driven with large signal

a time-variant linear model. Many modern circuit simulators (e.g ADS and SpectreRF) can simulate and solve circuits using this model. The periodic nature of the clock permits these tools to solve for a time varying DC operating point. At those time varying operating points, the circuit can be linearized and a time-variant transfer function $H(jw, t)$ can be obtained, where t is the observation time [30]. Fig. 3.2 exemplifies this case for a gain stage driven out of its linear operation with a strong input signal. The gain stage can still be linearized around its DC operating point. The resultant transfer function $H(j\omega, t)$ is a periodic transfer function that can be expanded to its Fourier coefficients:

$$H(j\omega, t) = \sum_{n=-\infty}^{\infty} H_n(j\omega) e^{jnw_o t} \tag{3.1}$$

Where w_o is the fundamental frequency of the large signal excitation, the clock signal in our case. n is the harmonic number of the fundamental frequency w_o. Steady state simulators usually solve for the Fourier expansion of the transfer function $H_n(jw, t)$, e.g. Spectre RF [31]. Noise spectral density at node k due to noise at node i can now be computed:

$$S_k(jw, t) = S_i(jw, t) \left| \sum_{n=-\infty}^{\infty} H_{n(k,j)}(jw) e^{jnw_o t} \right|^2 \tag{3.2}$$

$$S_k(jw) = \langle S_k(jw, t) \rangle_{avg} \tag{3.3}$$

Where $S_k(jw, t)$ and $S_i(jw, t)$ are the noise power spectral density (PSD) at nodes i and k, respectively. (3.3) is the time average PSD of node k from time t to $t + T$, where T is the clock period. The side bands of the transfer function $H(jw, t)$, obtained by the Fourier expansion above, cause noise to fold down from different sidebands, thus the cyclostationary nature of the noise inside the clock repeater. $S(jw, t)$ can be cyclostationary if noise sources gets modulated by the time varying operating point. If noise sidebands are filtered out, noise loses cyclostationary nature and becomes static.

The previous discussion suggests that the amplitude and slew rate of the clock signal affect the transfer function of the clock repeater and the noise. Fig. 3.3 plots total gain and noise accumulation inside the clock repeater for 2 cases; A small clock amplitude (50mV) and a large clock amplitude (500mV). Both clock signals result in the same amplitude and slew rate at the output of the repeater. The small clock amplitude undergoes high and linear gain at the first few stages. Gain eventually compresses. A linear time variant (LTV) analysis shows the time-averaged gain drops to one at the 4^{th} stage onward. Noise contribution from earlier stages dominates total noise. Noise contribution of last stages is minimal due

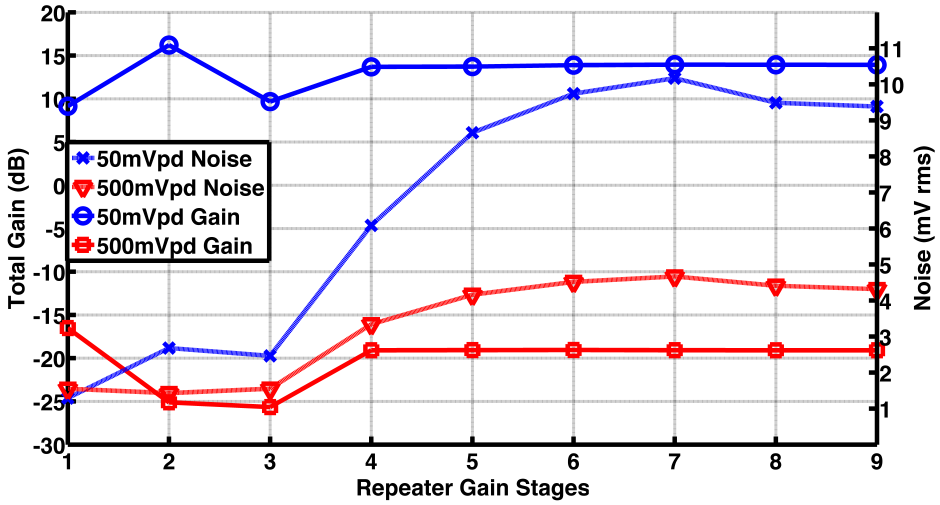


Figure 3.3: Total gain and integrated noise voltage as clock propagates through stages in the same repeater

to diminished gain and large clock slew rate. For the large clock amplitude, the average gain is even less than one early on the clock chain. Simply because the applied clock has much higher slew rate than the gain stages max slew rate during clock transition, while it's saturated elsewhere in the clock cycle. This results in less than unity time-averaged gain. Starting from the 4^{th} stage, the stage gain becomes unity. Noise growth is noticeably limited due to the reduced gain, and the result is that integrated noise of a small clock amplitude is twice as large as for large swing clock. It's to be noted also that the slight drop in integrated noise at stages 7 and 8 is attributed to reduction in noise bandwidth as we approach the end of the repeater.

Fig. 3.4 shows the impact of the slew rate on the total noise power of a 70mV clock amplitude. As input slew rate increases, stages saturate earlier, their gain drops and so does noise contribution. Overlaid in Fig. 3.4 is the noise power for 1^{st} and 2^{nd} repeater stages. They represent almost 80% of total repeater noise. Also overlaid on figure is noise power estimate based on LTV gain from equation (3.2) and noise sources calculated from devices in 1^{st} and 2^{nd} repeater stages.

To evaluate jitter at the output of the clock repeater. Noise needs to be evaluated at

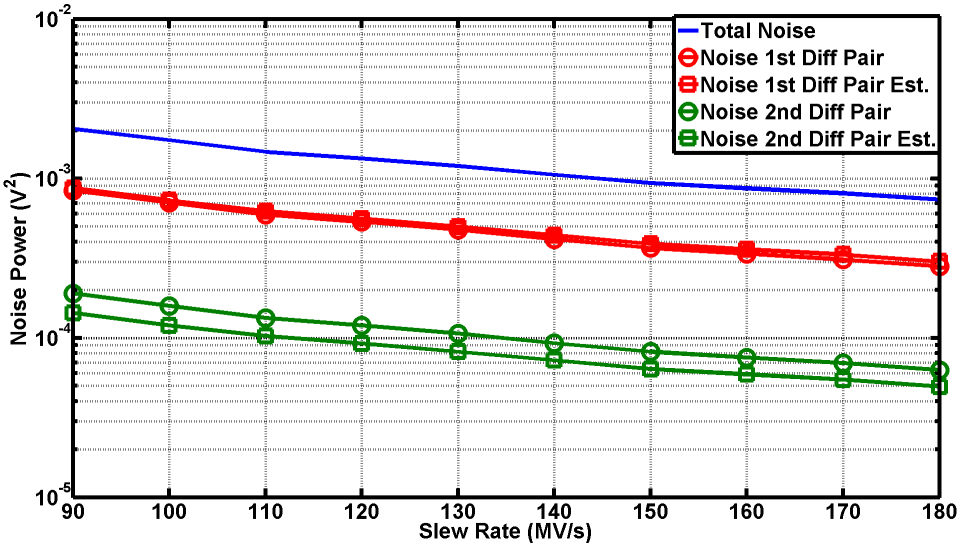


Figure 3.4: Clock repeater integrated noise power vs. slew rate for a 70mV

the zero crossing instance t_0. As we mentioned earlier, the LTV transfer function in (3.2) can be used to evaluate root mean square noise at the output of the repeater at different time points. Fig. 3.5 shows the clock repeater output noise and clock amplitude calculated with SpectreRF periodic steady state time domain noise (PSS tdnoise), Which uses (3.2) to evaluate noise at different time points. The graph shows the noise voltage at zero crossing point equals 12.5mVrms. It also shows that average noise voltage (evaluated by a normal PSS PNoise) is only 2mVrms. The repeater last stage exhibits large gain at the transition period that amplifies the stage internal noise sources as well as preceding stages noise. When transition completes, the gain drops and output noise also drops drastically. Thus the average noise is low compared to transition noise. Jitter at the output of the repeater is thus given by (3.4), where $V_{n,rms}(t_0)$ is the root mean square noise at t_0. Clock edges are sampling the noise every clock cycle, hence we only need to integrate noise from 0 to $f_clk/2$.

$$V_{n,rms}(t_0) = \sqrt{\int_0^{f_clk/2} S_{total}(jw, t_0)\,\mathrm{d}f}$$
$$\sigma_j(t_0) = \frac{V_{n,rms}(t_0)}{Slope(t_0)} \tag{3.4}$$

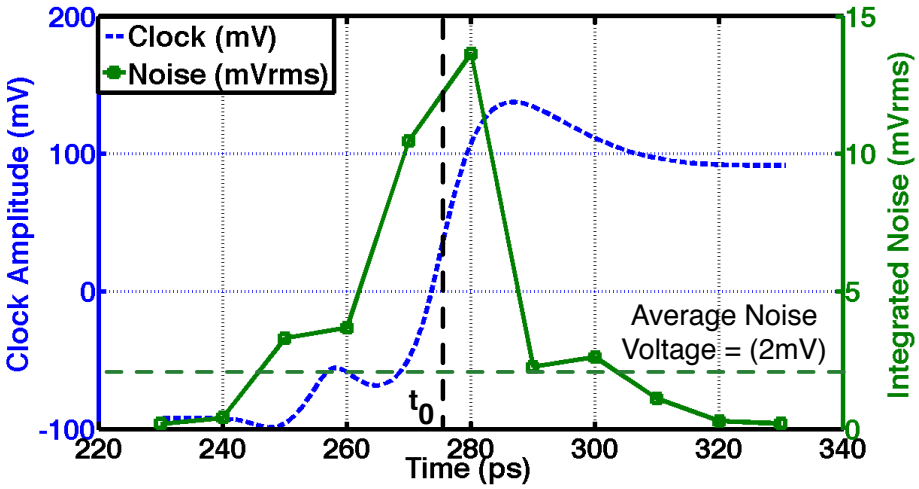


Figure 3.5: Clock repeater amplitude and time domain noise at the repeater output

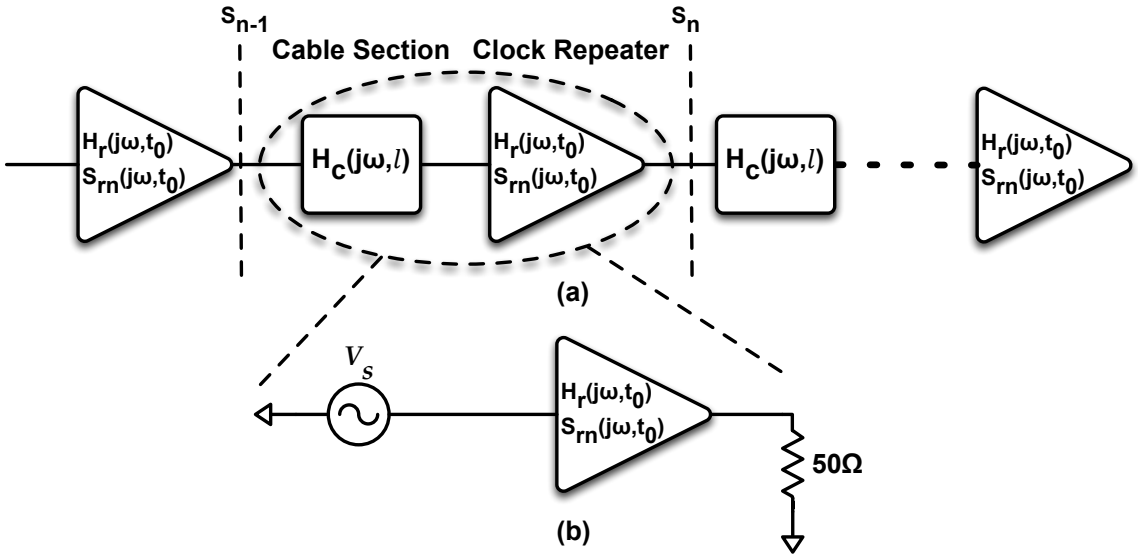


Figure 3.6: Cable link model (a) and an equivalent model for a cable section and a repeater (b)

3.3 Jitter Accumulation in Cable Link

Building a simulation model for the cable link shown in Fig.1.2 is a necessary step to estimate clock accumulation and jitter of the synchronous link, and thus predict its performance. The most accurate way to perform this simulation, given the strong non-linear and time variant

nature of the clock path is to use a transient noise analysis, where the different noise sources inside the SPICE model are internally replaced by a transient random sources that satisfy the power density and bandwidth of the original noise source. For a white noise source, this requires transient simulation step to be small enough to sample the highest frequency components of the noise source, and simulation time needs to be long enough to take at least one full cycle of lowest frequency components of noise. Those requirements are known obstructions for circuit designers and hinder practicality of transient noise simulation to cable links. On top of that, long simulation time needed to propagate the clock across the cable section. For instance, for CAT 7 cables, delay is almost 4ns/meter. For a 100 meter cable, this is a 400ns of simulation time that contains no information. Such simulations would typically take hours to a day. On the other hand, Steady state analysis could also be used for this purpose where noise analysis is solved as a small signal analysis on top of a linear time variant solution of the circuit, as we explained in the previous section. However, a circuit that contains cable model represented by S-Parameters is very tough to solve with state of the art steady state simulators, in particular when those models exhibit excessive delays as in the case with cable model.

Instead, we propose using a fast linear time variant model to estimate jitter accumulation and power of the clock forwarded cable link. Fig. 3.6(a) shows a block diagram of the clock forward link expressed in freq. domain transfer functions. The cable is a linear time variant element so it's expressed as $H_c(j\omega, l)$, where l is the cable section length. As explained in section 3.2.1 the clock repeater transfer function can be expressed in linear time variant model as $H_r(j\omega, t_0)$, and it's output noise power spectral density expressed by $S_{rn}(j\omega, t_0)$, where t_0 is the observation time set as the zero crossing point of the output clock. For most practical considerations we can assume that the clock driver output has a 50% duty cycle and fast edges compared to clock period. The Fourier expansion of such a clock contains only odd harmonics n scaled by $\frac{1}{2n+1}$. The harmonics are filtered by the cable transfer function before being applied to the next clock repeater. A single cable and repeater section can thus be expressed as shown Fig. 3.6(b) with a voltage source V_S representing the filtered clock

signal. The voltage source is given by:

$$V_S = \sum_{n=-\infty}^{\infty} A\frac{1}{2n+1}\left|H_c((2n+1)j\omega_0, l)\right| e^{(2n+1)j\omega_0 t} \tag{3.5}$$

Where A is the driver amplitude. In practice, only few tens of harmonics are needed to express the filtered clock signal, the remaining are filtered out by the cable.

3.3.1 Noise and Transfer Function Sidebands

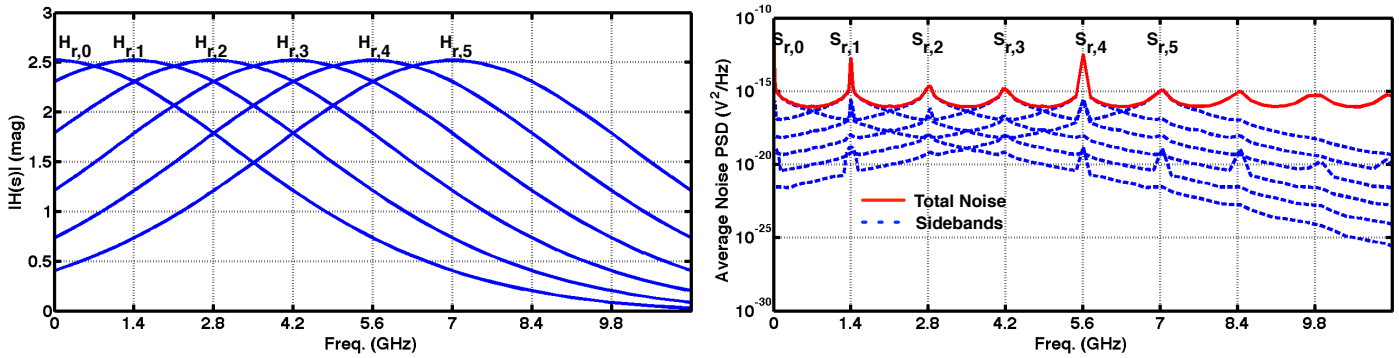
Because of the periodic nature of the clock signal, a linear time variant impulse response $h(t,\tau)$ can define the time domain relationship between the input $x(t)$ to the clock repeater and its output $y(t)$ as follows:

$$y(t) = \int_{-\infty}^{\infty} h(t,\tau)x(\tau)\,\mathrm{d}\tau \tag{3.6}$$

Where τ is the time instance when the impulse is applied, and t is observation time instance, e.g. zero-crossing time.

For most practical cases, the clock signal at the output of the clock repeater has fast rise and fall times i.e. negligible fraction of the clock cycle. It's at this window of rise and fall time where the repeater has non zero gain for noise and signal. The rest of the clock cycle, gain is almost zero. As a result, the linear time variant impulse response can be expressed as an almost ideal train of narrow impulses in the time domain. The frequency domain transfer function which can obtained by equation (3.1) consists of identical sidebands over a wide range of frequency much bigger than the repeater bandwidth.

Fig. 3.7(a) shows the frequency domain transfer function of the clock repeater, $H_r(j\omega)$, with 5 sidebands obtained by a Steady state simulation of the clock repeater. As can be seen from the figure the sidebands have the same magnitude and shifted by a frequency that's double the clock frequency. This is because the train of linear time variant impulses repeat for the rising and falling edges of the clock, i.e. The Fourier fundamental frequency is twice



(a) Clock Repeater Transfer Function $H_r(j\omega)$, 5 sidebands are shown

(b) Avg. Noise PSD at Repeater Output, 5 sidebands and total noise PSD are shown

Figure 3.7: Clock repeater transfer function and average output noise PSD

the clock frequency. The gain transfer can be expressed by:

$$H_r(j\omega) = \sum_{k=0}^{sdbnds} H_{r,0}(j\omega - 2k\omega_0) \tag{3.7}$$

Fig. 3.7(b) shows the average noise PSD at the output of the clock repeater, noise is also translated to the sidebands frequencies resulting in the cyclostationary nature of the repeater noise. The sidebands of the transfer function start to attenuate following a sync envelope when frequency approaches the inverse of the rise time duration.

3.3.2 Calculation of Total Noise Transfer Function

By taking into consideration the transfer function sidebands and cycloostationary nature of noise discussed in the previous section, we can now arrive at an expression of jitter accumulated after n repeaters. First, the average noise spectral density and average gain of the repeater (as in (3.3)) can be obtained by simple steady state analysis using the model shown in Fig. 3.6(b). V_S is obtained from (3.5) given the clock driver amplitude and the cable section magnitude response. The average noise at the n^{th} repeater output can thus be given by:

$$S_n(j\omega) = |H_r(j\omega)|^2 \left(\sum_{k=0}^{sdbnds} S_{n-1}(j\omega - 2k\omega_0) \right.$$

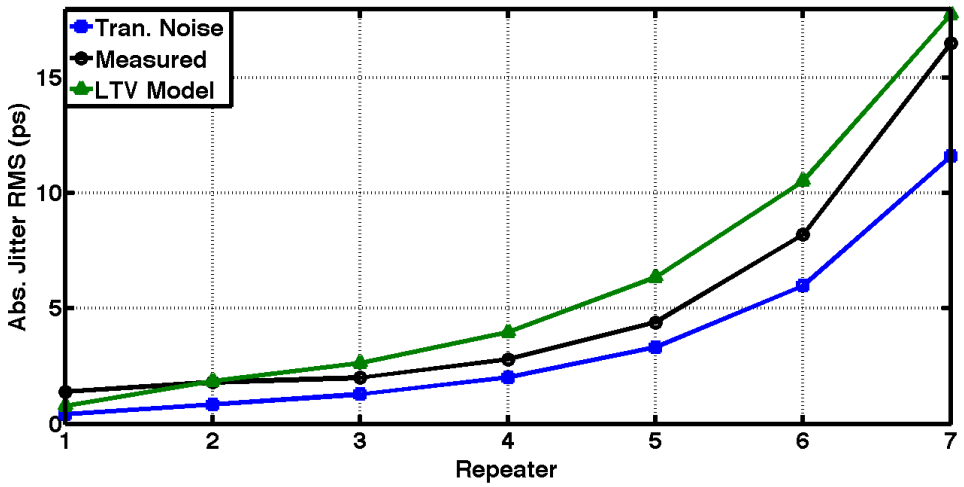


Figure 3.8: Jitter accumulation along 7 repeaters. Comparison between measurement, transient noise simulation and the proposed LTV model

$$\times |H_{c,l}(j\omega - 2k\omega_0)|^2 \Big) + S_{r,n}(j\omega) \tag{3.8}$$

Where $S_n(j\omega)$, and $S_{r,n}(j\omega)$ are the total average noise at the output of the n^{th} repeater and the repeater average output noise, respectively, as illustrated in Fig. 3.6(a).

Equation (3.8) describes the average noise accumulation across repeaters. To evaluate jitter at the repeater output we need to evaluate noise transfer and noise spectral density at the zero crossing point t_0 as follows:

$$S_n(j\omega, t_0) = |H_r(j\omega, t_0)|^2 \Bigg(\sum_{k=0}^{sdbnds} S_{n-1}(j\omega - 2k\omega_0) \times |H_{c,l}(j\omega - 2k\omega_0)|^2 \Bigg) + S_{r,n}(j\omega, t_0) \tag{3.9}$$

From which The RMS jitter at the output of the n^{th} repeater can be evaluated to be:

$$\sigma_n(t_0) = \frac{\sqrt{\int_0^\infty S_n(j\omega, t_0)\, \mathrm{d}f}}{\mathrm{d}(V_S(t_0))/dt} \tag{3.10}$$

Fig.3.8 shows jitter accumulation along 7 clock repeaters and comparison between measurement, transient noise simulation and the proposed LTV. The clock is at 750MHz, driver

amplitude is 625mVppd and cable section length is 16m. Transient noise simulation and the LTV model show fairly close jitter accumulation behavior with the measured result. Transient noise simulation predicts less accumulated jitter because minimum noise frequency is chosen relatively high to allow practical simulation time. Proposed LTV model shows only 10% accumulated jitter error with respect to measurement. Jitter result is overestimated because of the assumption that noise acts only as a small signal perturbation. In reality, this assumption breaks at large values of noise at the cable end which tends to alter the repeater DC operating point and reduce its gain, hence less noise and jitter at the cable end.

3.4 Exploration of Design Space

The aforementioned analysis proposes a fast and accurate model to estimate jitter accumulation in repeater based synchronous links. The cable used in the link design is a CAT7 cable with a channel response shown in Fig 3.9. The cable has a 2.2dB attenuation per meter at the Nyquist frequency of 12Gbps. Only a single repeater needs to be simulated to obtain LTV transfer function and output noise for a given driver amplitude and cable section length. Fig. 3.10 shows the jitter accumulation profile at the end of a 100m cable for a 500mV clock driver swing, for different cable length sections and clock frequencies. As frequency increases, loss of clock amplitude and slope inside the cable increase which results in SNR degradation. A smaller clock amplitude also implies that earlier stages inside the repeater possess more gain, as depicted in Fig. 3.3, which causes more noise contribution from those stages. Consequently, more degradation of SNR and jitter increases with the increase of clock frequency. A similar effect occurs with increasing cable section length. Fig.3.10 shows that 40ps RMS jitter is observed at end of 100m if we used 19m cable section length, and 800MHz Clock frequency. An amount of jitter that's practically intolerable by a receiver at the other end of the cable.

Increasing the clock amplitude increases the SNR and reduces jitter on the expense of total clocking power. Fig. 3.11 shows the total repeating clocking power, excluding clock

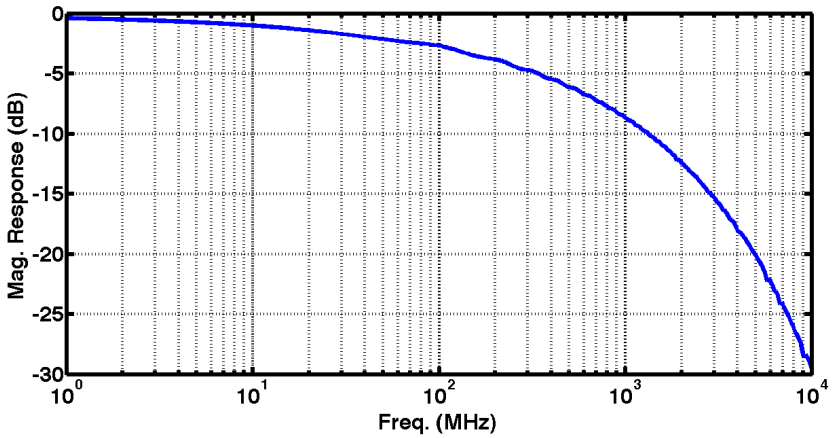


Figure 3.9: Channel response of a 10-m CAT7 cable

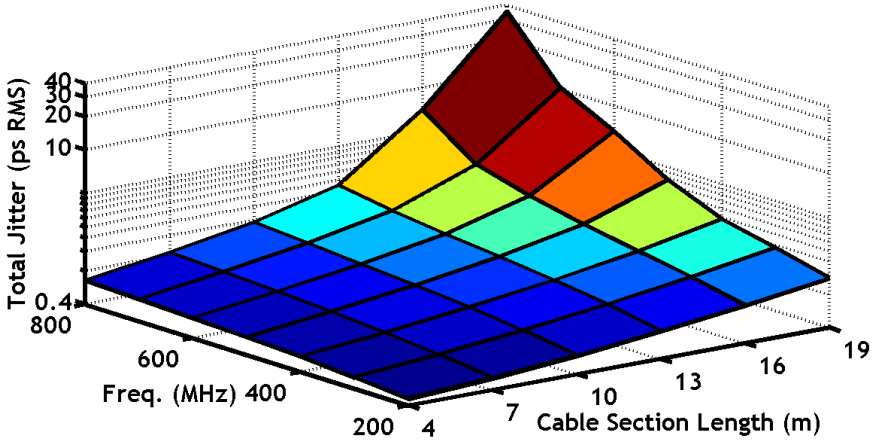


Figure 3.10: Jitter profile at the end of a 100m cable for different cable sections and clock frequencies, for a 500mV swing clock

multiplication, needed to meet a 4ps RMS jitter requirement at the end of the 100m cable. As expected, power increases when cable section length and clock frequency increase, to compensate for SNR loss and jitter accumulation.

Figures 3.10 and 3.11 suggest that a shorter cable section length and lower clock frequency are favorable for lower jitter accumulation along the entire cable. Shorter cable section means more number of sections needed to meet the required distance. Thus, more connectors are needed to connect cables to the repeaters which adds cost to the link and poses more

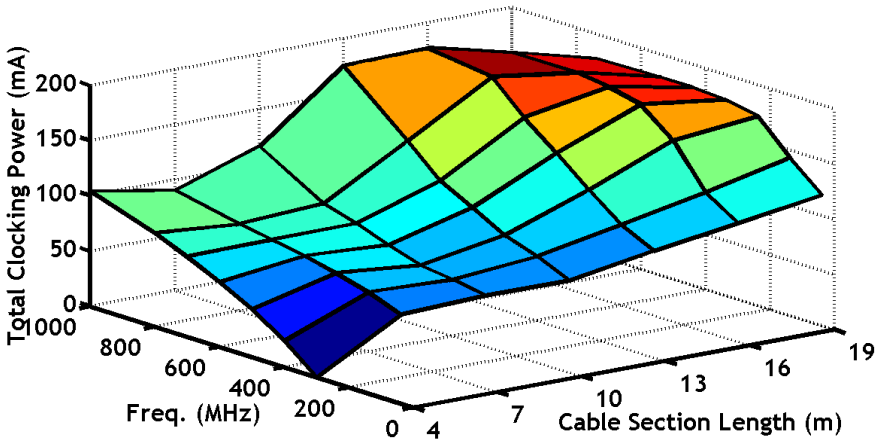


Figure 3.11: Total repeaters power for a 4ps RMS jitter at the end of the 100m cable. Cable section length and clock frequency are shown on the x and y axes, respectively

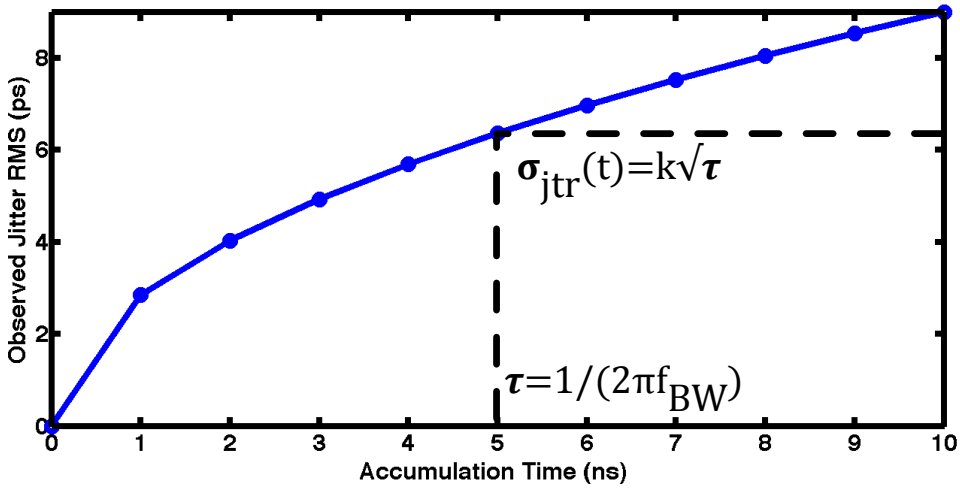


Figure 3.12: VCO open loop jitter observed at time t

mechanical week points. Detailed analysis of this issue is beyond the scope of this work, but generally less number of cable sections are needed to achieve the required length. On the other hand lowering the clock frequency reduces jitter accumulation because of less SNR degradation inside the cable but this doesn't come without a price. The lower the clock frequency, the larger the multiplication ratio needed inside the CMU in fig. 1.2 to multiply the clock up to the data rate. To understand the impact of large CMU multiplication ratio

on the performance of the link we need to have a closer look at jitter accumulation inside the CMU. Fig. 3.12 shows the RMS jitter observed as time elapses from some reference edge inside a typical ring oscillator. Jitter accumulates indefinitely inside an open loop oscillator with the square root of observation time. When the VCO is used inside a PLL CMU, the jitter accumulation plateaus at an observation time approximately equals to the CMU time constant [32]. For overdamped PLLs which are commonly used in repeater and jitter filtering applications, the PLL time constant is inversely proportional to the loop bandwidth. Knowing that the maximum PLL BW that doesn't undermine the loop stability is about one-tenth of the reference clock frequency [17], the PLL CMU jitter can thus be estimated by:

$$\sigma_{PLL} = \frac{1}{\sqrt{2}}\sigma_{VCO}(\tau) = \frac{k}{\sqrt{4\pi(f_{ref}/10)}} \tag{3.11}$$

Where k is the VCO jitter constant in $\sqrt{secs}$. The above equation doesn't take into account other noise sources inside the PLL (e.g. charge pump and dividers). In most practical ring based PLLs the VCO jitter is the most dominant contributor. This trade-off between CMU jitter accumulation and jitter accumulation inside the clock repeater is demonstrated in Fig. 3.13. The repeaters jitter accumulation graph in the figure corresponds to a link with 13m cable section and 250mV clock amplitude. The plot shows optimal clock frequency is somewhere between 500MHz and 700MHz. Thus, this trade-off puts a limitation on how low the clock frequency can go, whereas the Fig.3.11 poses an upper bound on how high clock frequency can go for a given jitter performance.

The optimum clock frequency can be pushed even lower by using a clean LC VCO inside the CMU instead of a ring oscillator. However, building a ring based CMU is advantageous because of the ring oscillator wide range of operating frequencies without simple tuning and calibration compared to LC oscillators. Therefore, the clock repeater can be realized in a small area and permits wide range of data rates.

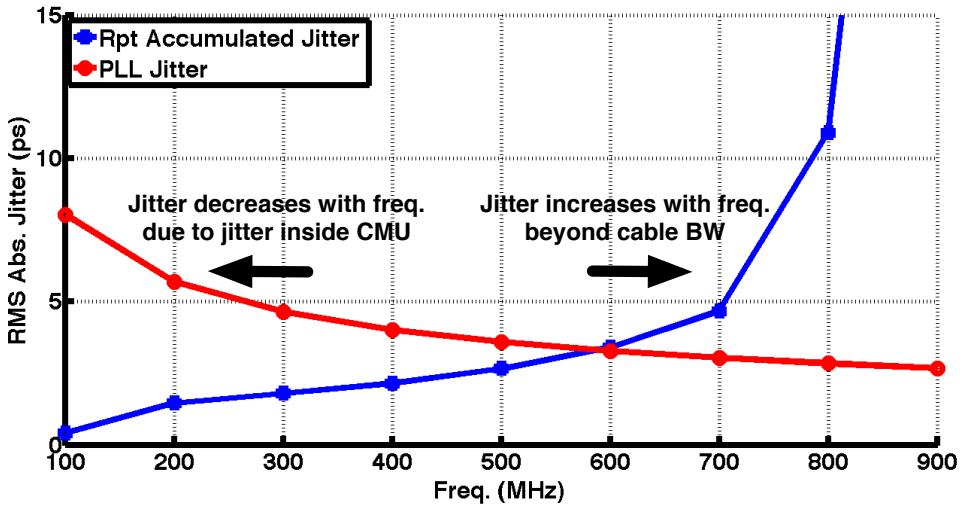


Figure 3.13: Trade-off between jitter accumulation inside CMU and jitter accumulation inside clock repeaters

3.5 Jitter Filtering

Jitter correlation between clock and data in source synchronous systems is crucial for the link to meet signal integrity and bit error rate requirements. This correlation is disrupted primarily due clock-to-data skew and the intrinsic delay inside the clock multiplication unit. The Fourier transform of the uncorrelated phase noise can be found by:

$$\phi_e(j\omega) = \phi_{data}(j\omega) - \phi_{clk}(j\omega) = \phi_{data}(j\omega)(1 - e^{-j\omega t_d}) \tag{3.12}$$

Where t_d is the clock-to-data delay, ϕ_{clk}, ϕ_{data}, ϕ_e are the clock phase noise, data phase noise and the uncorrelated phase noise, respectively. From which we can find the uncorrelated phase noise gain as:

$$|A_{uncorr}(j\omega)| = \left|\frac{\phi_e(j\omega)}{\phi_{data}(j\omega)}\right| = \sqrt{2(1 - \cos(\omega t_d))} \tag{3.13}$$

The above equation has a high pass characteristic suggesting that uncorrelated jitter amplification increases with frequency. Fig. 3.14 depicts the uncorrelated jitter amplification for a 12Gbps data pattern for clock skews ranging from 0.5UI to 5UI. For example, a 5UI clock-data skew (416.7ps) causes jitter beyond 400MHz to be amplified, cutting down from the

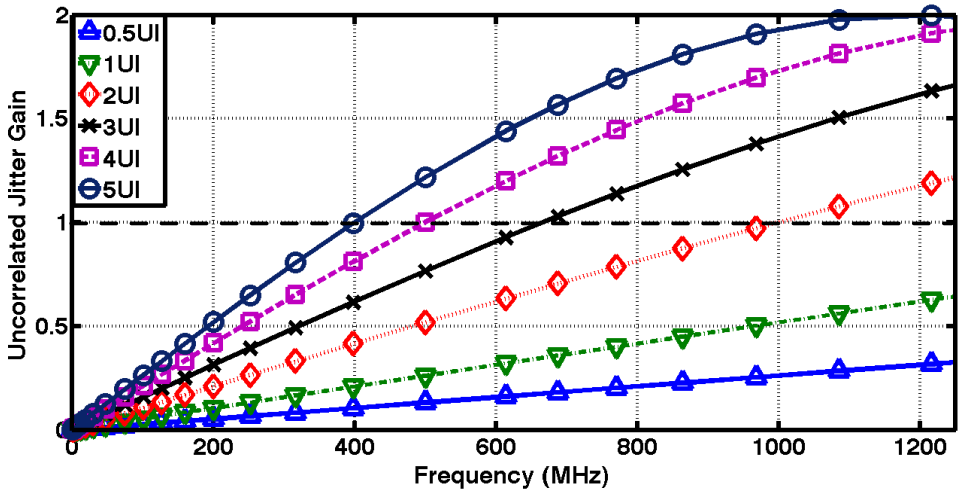


Figure 3.14: Differential jitter gain in source synchronous systems with different clock-data skews

total link jitter budget. Uncorrelated jitter is amplified at frequencies inversely proportional to clock-data delay. This suggests that filtering of high frequency jitter is advantageous in clock forwarded systems to mitigate uncorrelated jitter accumulation. Because the jitter filtering element is inserted only in the clock path, jitter filtering bandwidth should be controlled to track correlated jitter and pass it un-filtered, meanwhile it rejects uncorrelated high frequency jitter [3, 8–11].

There are several candidates for jitter filtering. For instance, a tuned clock buffer where a differential inductor is used at the clock amplifier filters the phase noise around the center frequency. While effective, the main disadvantage is the large silicon area for the inductor needed at propagated clock frequency. A 5nH differential inductor that resonates with 5pF cap at 1GHz can easily consume $300\times300\mu m^2$. Additionally, an LC-based filter does not accommodate a wide range of frequencies easily without needed large varactors that can compromise the filter performance. Another widely used jitter filtering circuit is a cleanup PLL with the appropriate bandwidth [3]. A PLL is already needed for the CMU and hence with proper design may serve both purposes. In the example above with a filter bandwidth of 75MHz, a cleanup PLL with similar bandwidth can be difficult to over-damp due to the delay within the loop. Furthermore, with a cascade of PLLs in the clock repeaters results

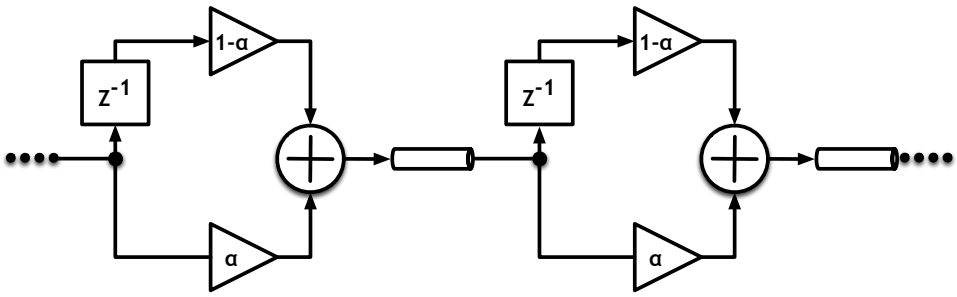
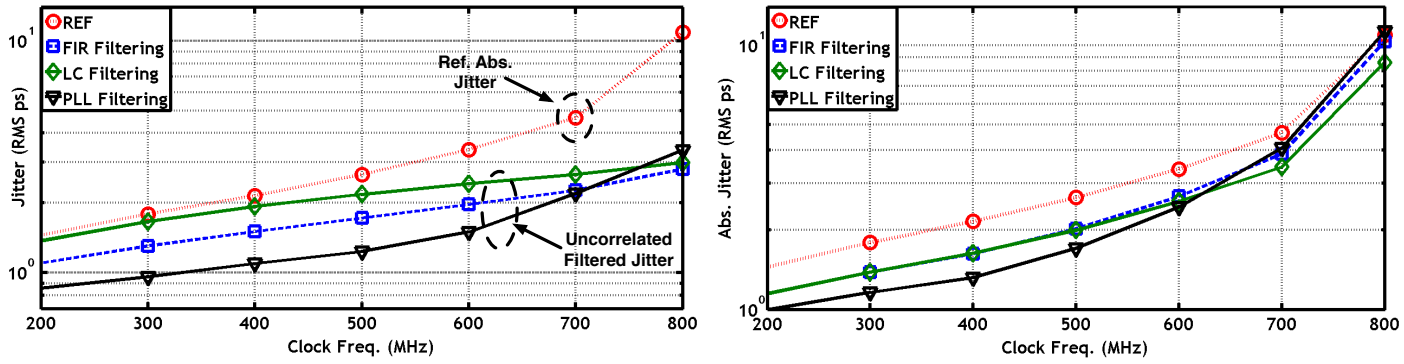


Figure 3.15: Illustration of a cascade of two repeaters. Each repeater contains a first-order FIR filter.

in accumulated peaking of the PLL transfer function. Sufficient damping of the transfer function is very challenging with wide tracking bandwidths and results in jitter amplification near the PLL bandwidth [12]. This work proposes a third option of using delay elements to implement a finite impulse response (FIR) phase filter to perform the high-frequency jitter filtering. As shown in Fig. 3.15, a first-order phase FIR needs a delay and summation. The summation can be implemented as a phase interpolator as described in the next section. The filter resembles phase averaging used in implementing a DLL in [33], where the phases of the delay cells are added to average timing mismatches.

Fig. 3.16 compares different filtering approaches for uncorrelated jitter (a) and absolute jitter (b). The analysis assumes a CAT7 cable link with 13m clock repeating distance, 250mV clock amplitude and observing jitter at the end of the 100m cable. The plot shows the impact of filtering with clock forwarding at clock frequencies ranging from 200MHz to 800MHz. The uncorrelated jitter is a filtered version of the absolute jitter. The reference is without any filtering and the decorrelation between clock and data stems from the 1 clock cycle delay inside the clock multiplication unit and noise from the clock repeaters. Additional filtering can reduce the high frequency noise but at the expense of further decorrelating the clocks and hence the filter is designed for high bandwidth. The LC-tuned amplifier design uses an inductor with quality factor of 4 at 1GHz. The PLL design assumes a bandwidth of 1/10 of the input frequency and 60^o phase margin. The FIR filter design is a $1+\alpha D$ first order filter at each repeater with the delay set at one clock cycle. The FIR zero falls at half the clock



(a) (b)

Figure 3.16: Comparison of the accumulated jitter for different filtering methods at the end of a 100-m cable as a function of different clock frequencies: (a) uncorrelated jitter and (b) absolute Jitter

frequency. As shown in both figures, a PLL has superior performance at lower frequencies due to a higher order of its filter but suffers at high frequencies due to the peaking in its transfer function. The FIR and LC filtering have very similar performance making the FIR an attractive option for a low-area implementation.

Fig. 3.17 compares FIR and PLL filtering with different noise sources. In mixed signal environments, supply noise from on-chip switching activity and external noise coupled to the chip can be a dominant component to the total output noise. This noise generally has a high-pass or band-pass characteristic due to high frequency capacitive and inductive coupling or behavior of the PLL. The FIR filter approach matches the PLL filtering performance at low frequency but outperforms the PLL at high frequency.

3.6 Summary

This chapters provides the necessary analysis foundation for the system implementation details. We introduce a simple and semi analytical model for estimating jitter accumulation in clock forwarded link. The analysis is used to understand the different trade-offs in design decisions. We also make a comparison between clock filtering schemes in the light of the

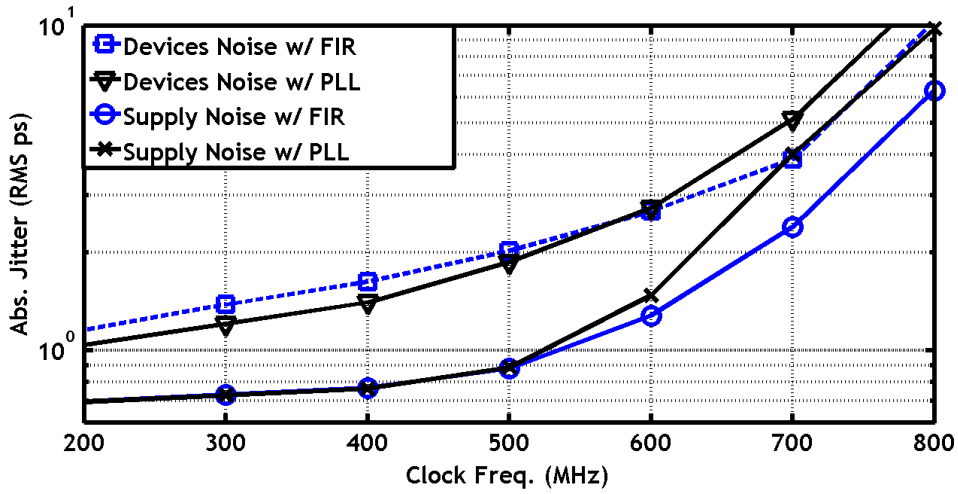


Figure 3.17: Comparison of output noise from using an FIR filter and PLL filter when accounting for noise from repeater devices and from supply noise.

analysis. A simple FIR filtering scheme is introduced and compared to PLL and LC filters in terms of absolute and period jitter performance.

CHAPTER 4

Implementation Details

In this chapter, the implementation details of the repeater is presented. We first describe the architecture of the FIR filter. The system is implemented so that we can configure the clock buffering to be without filtering or to be a PLL-based repeater for comparison. We then describe the detailed implementation of the clocking circuits followed by the data sampling and driving circuits.

4.1 FIR Filter Architecture

As shown in Fig. 3.15, a simple first order FIR has a delay of 1 clock cycle. We opportunistically observe that with the proper architecture the CMU for frequency multiplying and generating the sampling clock can produce this delay. The CMU is designed as a multiplying delay locked loop (MDLL) producing a 6GHz clock. By injecting the reference clock edge into the VCO, MDLLs [22, 34–37] do not accumulate jitter in comparison with VCO-based PLLs for data sampling. The divided output of the MDLL has an intrinsic delay of 1 clock cycle between the input and the feedback clocks and has an all-pass transfer function.

To implement the FIR, at the output of the MDLL, we insert a phase interpolator that takes as inputs the incoming reference clock and feedback clock of the CMU. Output of this phase interpolator is driven to the next repeater as depicted in Fig. 4.1(a). The interpolating between the two signals results in the summation of the FIR shown in Fig. 4.1(b). The phase interpolator weighting adjustment represents the FIR filter coefficient, and the transfer function is given by $H(z) = \alpha + (1 - \alpha)z^{-1}$. The added phase interpolator has very little

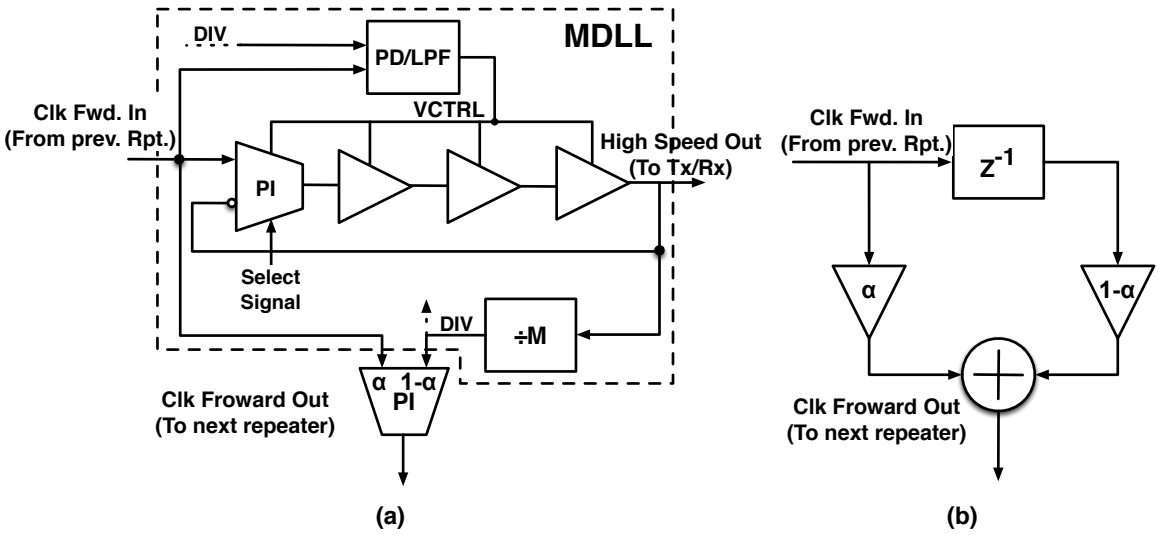


Figure 4.1: Simplified schematic of the CMU (a) with interpolator at the output. The equivalent phase-FIR filter (b).

power and area cost and allows programmable α.

With a programmable interpolator, the filter function can be adjusted. An α of zero passes the MDLL divided clock to the output, and an α of one forwards the reference clock like a simple buffer. Tuning the phase interpolator setting, α, changes the -3dB bandwidth. Fig. 3.15 shows the cascade of two clock repeaters with FIR filtering for the output clock. The phase noise side-band spectrum of two cascaded clock repeaters with 40% FIR interpolation coefficient is shown in Fig. 4.2. Jitter is reduced with each stage of the filtering. Since each stage can have the filtering coefficient independently adjusted, Fig. 4.3 illustrates the impact of varying α for each of 4 cascaded clock repeaters. The best combination for least jitter is found to be an α of 40% for the first 3 repeaters and an α of 0.6 in the fourth repeater. Proper choice can reduces jitter by up to 50% in a repeater stage. In our system where more repeaters are used, additional stages of FIR filtering do not reduce jitter significantly due the sharp roll-off of filtering beyond a fourth-order filter.

MDLL input mux is implemented as a configurable phase interpolator, shown in Fig. 4.4, to change the relative injection strengths of the reference edge and the VCO feedback edge [38]. It can be configured from 0 to 100% injection strength with 20% steps. Where 0%

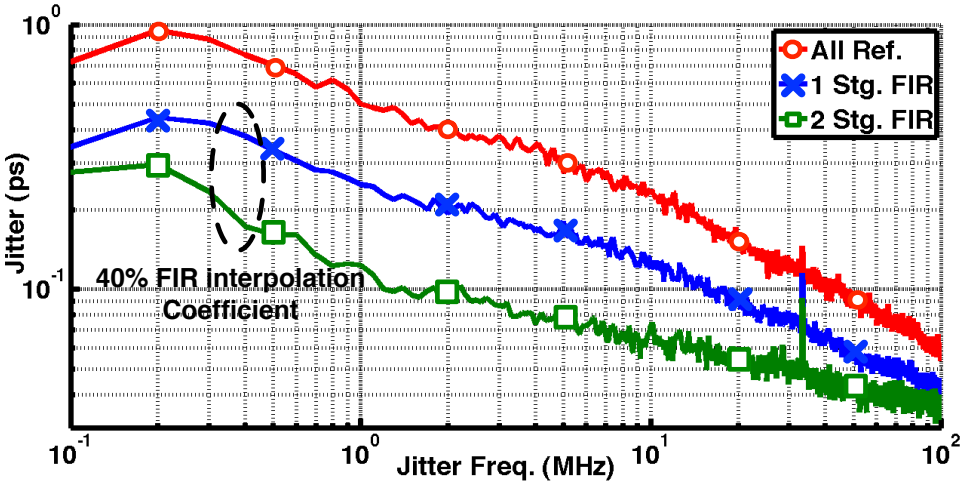


Figure 4.2: Jitter spectrum and impact of the FIR filtering

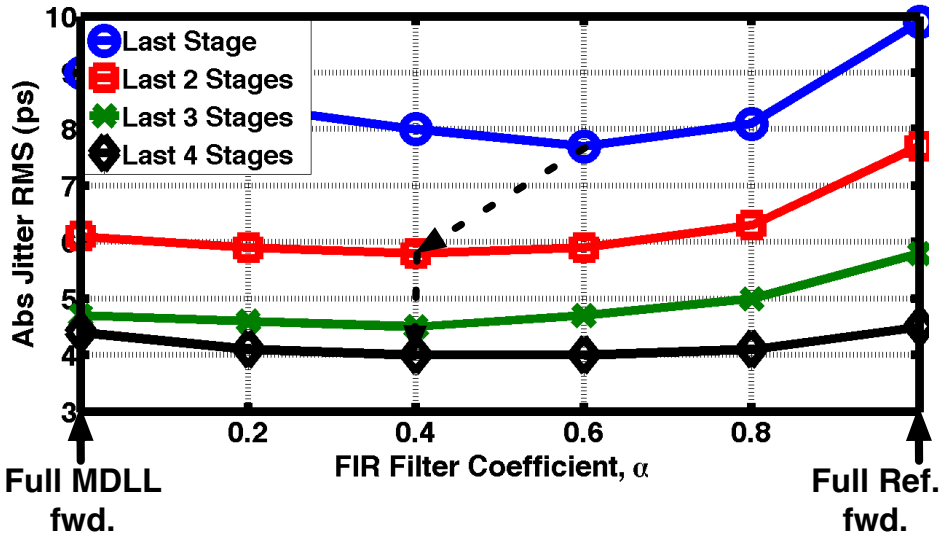


Figure 4.3: Absolute jitter (RMS) as a function of the FIR filter coefficient measured at the output of the 4 cascaded clock repeaters.

setting denotes the mux is configured to operate as a normal delay cell in the VCO, thus the CMU is configured as a PLL. A 100% setting permits full injection of reference edge, thus CMU is configured as an MDLL. Intermediate settings interpolate between reference and VCO edges, and the CMU operates as a semi-PLL/MDLL. At the output of the CMU we are adding a second mux/phase interpolator structure that takes the incoming reference clock

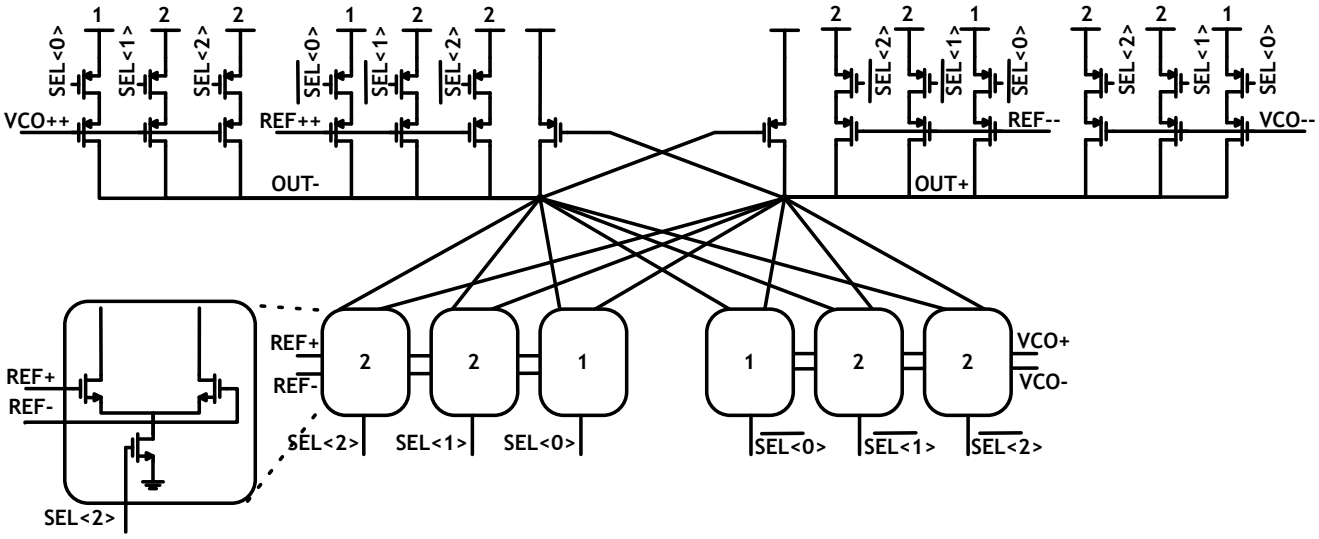
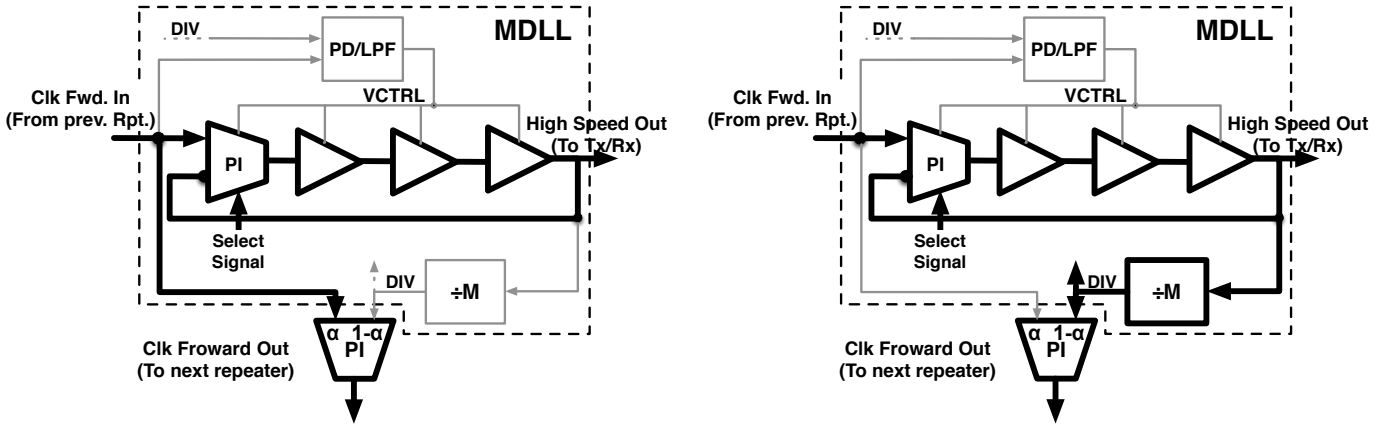


Figure 4.4: Design of the configurable multiplexer at the input of the MDLL

and a divided version of the CMU as inputs. Output of this phase interpolator goes directly to the clock driver, as depicted in Fig. 4.1(a). With such configurability, jitter accumulation across the different repeaters can be kept low. depending on its location on the cable. Early on in the link, when forward clock is still clean and didn't suffer jitter accumulation, the CMU is configured in a MDLL mode to reset VCO jitter accumulation. We also set the PI to forward the incoming clock to the next stage, as depicted in Fig. 4.5(a). Similarly, later on the link, when clock has undergone significant jitter accumulation, we tune the CMU in a PLL mode to filter incoming clock jitter. We also set the PI to forward a divided version of the filtered PLL clock, Fig. 4.5(b). Intermediate settings can be used in the middle of the cable link.

4.2 Clock Multiplication Unit

Multiplying DLLs have gained much interest in recent publications [22,34–37] because of their inherent ability to reset jitter accumulation inside the VCOs compared to MPLLs. This is attributed to the fact that reference clock edges are injected into the VCO each reference cycle and thus remove the jitter accumulation memory of the VCO. This can be interpreted as



(a) Early on the link, MDLL configuration

(b) Later on the link, PLL configuration

Figure 4.5: CMU configurations depending on its location in the link

designing an MPLL that has a bandwidth equivalent to the reference frequency bandwidth, compared to traditional MPLLs where bandwidth can't be greater than one tenth of the reference frequency. One challenging aspect in the design of MDLLs is the alignment of the injected reference edge to the VCO feedback signal. As shown in Fig. 4.6(a), the select logic is responsible for generating an aperture that allows the reference edge inside the loop and blocks the VCO feedback signal. As shown in Fig. 4.6(b), any delay mismatch between the reference edge and the VCO feedback edge, or a mismatch in the charge pump would cause the pulse following the injected edge different than the remaining VCO pulses, an effect that would manifest itself as period jitter or reference spur in the frequency domain, which limits the minimum jitter attained by the MDLL. Solutions are provided to this problem in literature. In [34] a slave oscillator is injected with the MDLL master oscillator. The slave oscillator acts as a LPF for the period jitter. In [35] an auxiliary calibration loop is used to measure the duty cycle error of the output. This error is then used to unbalance the charge pump current to absorb this mismatch. In [36] digital duty cycle measurements are correlated between consecutive samples. The error is then used to steer the control voltage of the VCO. This alleviates the need of PFD and charge pump altogether. While in [37] a phase detector that is based on chopping and correlated double sampling is used to minimize mismatches.

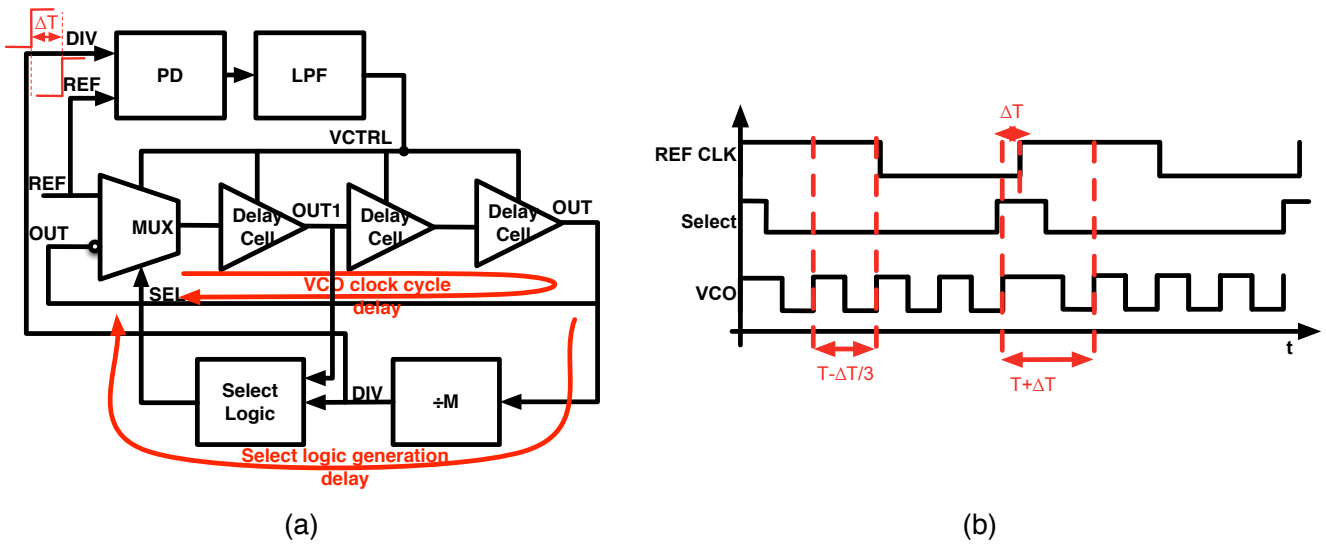


Figure 4.6: Schematic of (a) typical MDLL and (b) timing diagram showing impact of the REF and SEL pulses mismatches on the output period jitter

In all of the published techniques, a select logic block generates the SEL pulse that opens the aperture for reference injection. These prior works assumed that the SEL pulse could be generated quickly enough to select the next reference edge. Moreover the position of the SEL pulse with respect to the Ref edge was overlooked as a possible factor to affect the pattern jitter. As can be seen from Fig. 4.6(b) the SEL pulse is asserted when the DIV signal goes high and then OUT1 signal, one of the VCO phases, goes high. The delay for generating the SEL signal from the time the VCO signal OUT1 goes high is thus equal to the delay of the CMOS level restoration buffer after OUT1, not shown in Fig. 4.6(a), plus 3 or 4 gate delays inside the select logic. This has to be shorter than half a clock cycle of the VCO frequency. This delay is also function of process, voltage and temperature variations. A simulation that shows the impact of the SEL pulse phase shift is illustrated in Fig. 4.7. When the SEL pulses arrives early with respect to the VCO and reference edges, a hold violation inside the select multiplexer causes significant period jitter in the VCO output. Similarly, a SEL pulse arriving late would cause a VCO setup violation inside the multiplexer and also a period jitter increase. This constraint made the design of MDLLs for multi-gigahertz applications quite a challenging task. In fact, none of the published MDLLs, as far as we know, exceeded

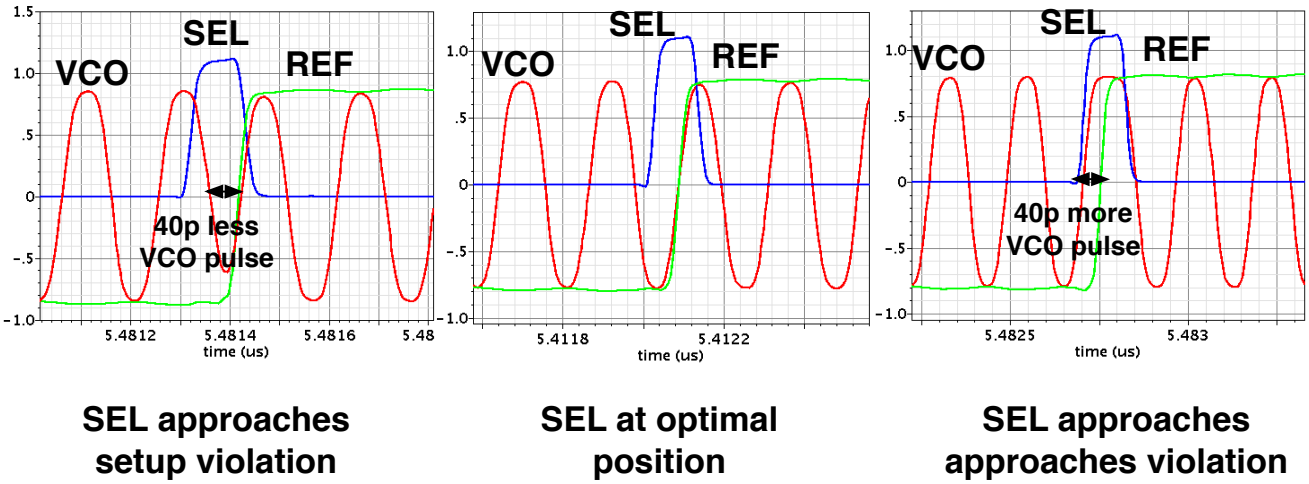


Figure 4.7: Impact of misalignment of SEL pulse with respect to VCO and reference edge. Left and right plots show early and late SEL pulses respectively while middle plot shows the ideal position

2GHz operation.

Figure 4.8 shows the schematic of the MDLL with the proposed modification. A 360^o phase rotator uses the quadrature phases of the VCO to vary delay of the SEL pulse by 1 complete clock cycle. This can compensate for any amount of latency in the select logic generation and precisely positions the SEL pulse with respect to the ref edge to minimize the period jitter. The VCO comprises 4 delay stages. The MUX stage is configured as a delay cell and used as the third stage of the VCO to maintain the quadrature nature between the two halves of the VCO. By doing this we can have constant phase steps for the SEL pulse tuning. The output of the phase rotators is then connected to the divider and the select logic to generate the required SEL signal. A calibration loop based on a search algorithm reads the duty cycle error of the VCO output (similar to [36]) and uses this reading as a measure of period jitter. The loop then advances the phase rotator setting and searches for the minimum value for the duty cycle error. This represents the optimal aperture position.

Design of the phase rotator is shown in the inset of Fig. 4.8. The interpolator comprises a bank of capacitors, connected from one terminal together to form the interpolation node,

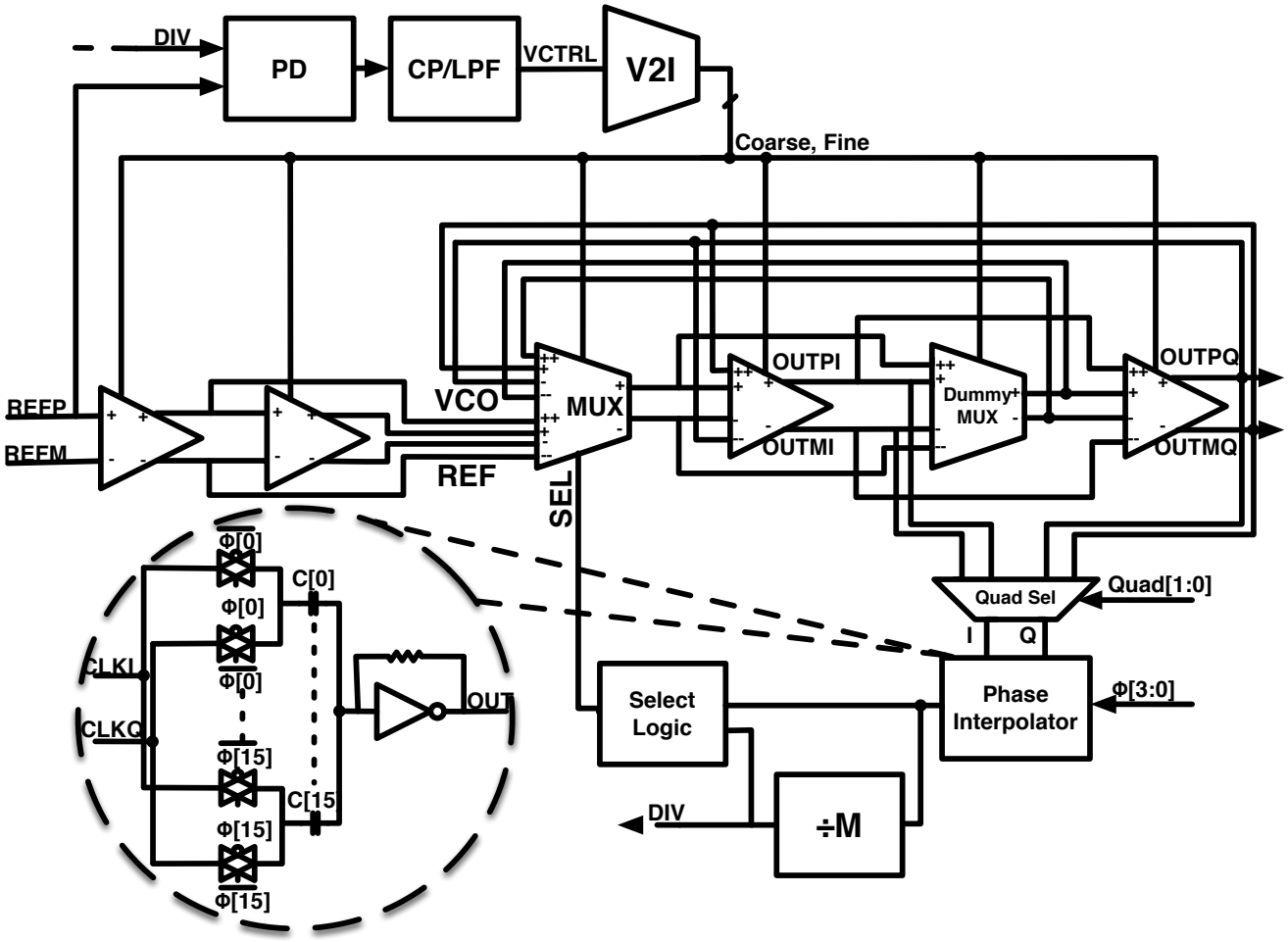


Figure 4.8: Schematic of the multiplying delay-locked loop. The capacitive-based phase interpolator is shown in the inset.

and from the other terminal each capacitor is connected to a pair of digitally controlled pass gates. Each pass gate is connected to one of the clock inputs CLKI and CLKQ. Interpolation takes place at the common terminal of the capacitors bank as a weighted sum of input clock voltages. Because summation takes place with passive components, this implementation provides better linearity performance than the conventional current-source based phase interpolator. Conventional phase interpolators suffer from nonlinearity due to finite output impedance of current sources and clock feedthrough from input to output. A 4fF/unit capacitor is used to achieve the 4-bit matching requirement for the phase interpolator.

Charge pump is a critical component of this design. Any mismatches in the charge pump

will be interpreted as phase mismatches between reference and divided edge. Unlike PLLs, phase mismatches in MDLL are manifested as period jitter. The charge pump used in this design minimizes static and dynamic mismatches to less than 0.5%, which was satisfactory for our application. Fig. 4.9 shows the charge pump design. Static mismatch is corrected by Transistors M1-M4, which form a singled ended replica of the charge pump. Amplifier 1 forces the output node of the replica to be equal to the control voltage by changing the down current. This guarantees that the DC up and down currents of the charge pump are equal (limited by the loop gain which is 50dB). It also guarantees that the down current is tracking the up current with different control voltages. This means that the charge pump can be used with wider control voltage ranges and therefore lower VCO gain. Using a voltage follower amplifier connected between VCTRL and VCTRL1 is used traditionally to minimize dynamic mismatch. Keeping VCTRL1 equals to VCTRL reduces charge sharing caused by switching currents between these 2 nodes. In our design, dynamic mismatch is corrected by another replica charge pump M5-M10. This replica guarantees that current is always flowing through the charge pump branch formed by M13-M14. This branch now is identical to the single ended replica and node VCTRL1 remains equal to VCTRL. Current consumed by this replica is tens of microamperes.

To minimize area, the MDLL loop filter capacitor is implemented using core thin-oxide devices rather than thick oxide devices. This reduces loop filter area by 63%. Due to the high gate leakage of these devices, an additional compensation technique similar to [39] is used. Amplifier 2, M17 and a replica of the loop filter capacitor (one tenth) are connected in a negative feedback configuration as shown in Fig. 4.9. The loop sets M17 current to be equal to the replica capacitor leakage. Consequently, the leakage current in the loop filter is provided by M18 instead of leaking the charge on the loop filter capacitor.

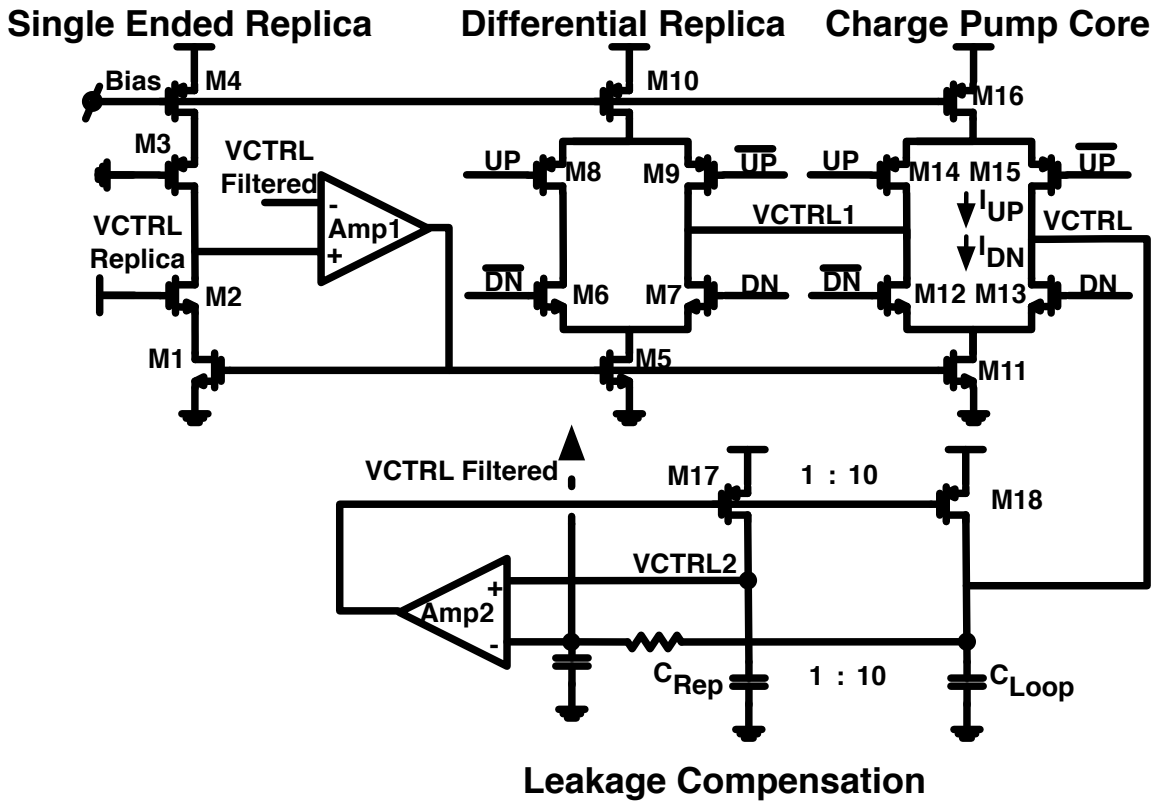


Figure 4.9: Schematic of the charge pump, which includes static and dynamic mismatch compensation circuit, and leakage correction circuit

4.3 Data Path Design

The noise analysis in chapter 3 and section 4.1 ensures the clock propagates across the entire cable length with sufficiently low noise. For data transmission, the distance between data repeaters is essentially a point-to-point link. The primary constraint is to minimize the power/meter for the targeted data rate. Longer repeat distances reduce power/meter by amortizing the repeater circuit's power. However, with more channel attenuation, more power is needed for equalization. For this study, CAT7 cable is used which has approximately 2.2-dB loss per meter at the data Nyquist frequency of 6GHz. This power trade-off with distance is analyzed and illustrated in Fig. 4.10. Total energy per bit for repeated data transmission across 100 meters is shown versus section repeat distance. Short distances require no equalization but pays the power penalty of terminating the cable for a given

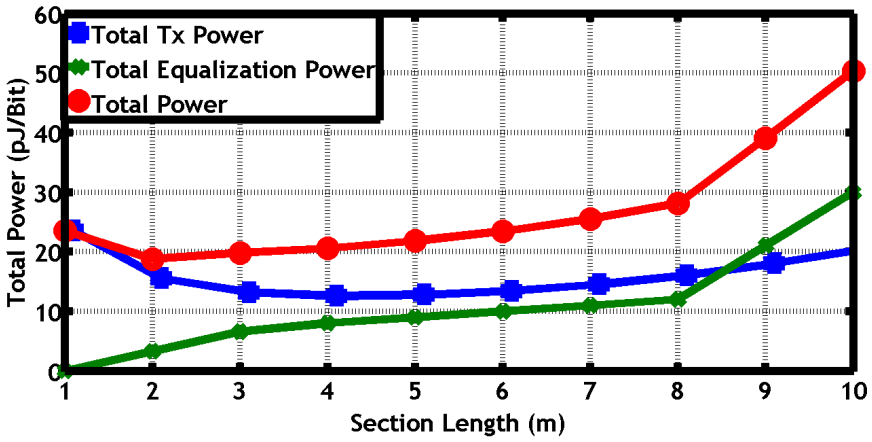
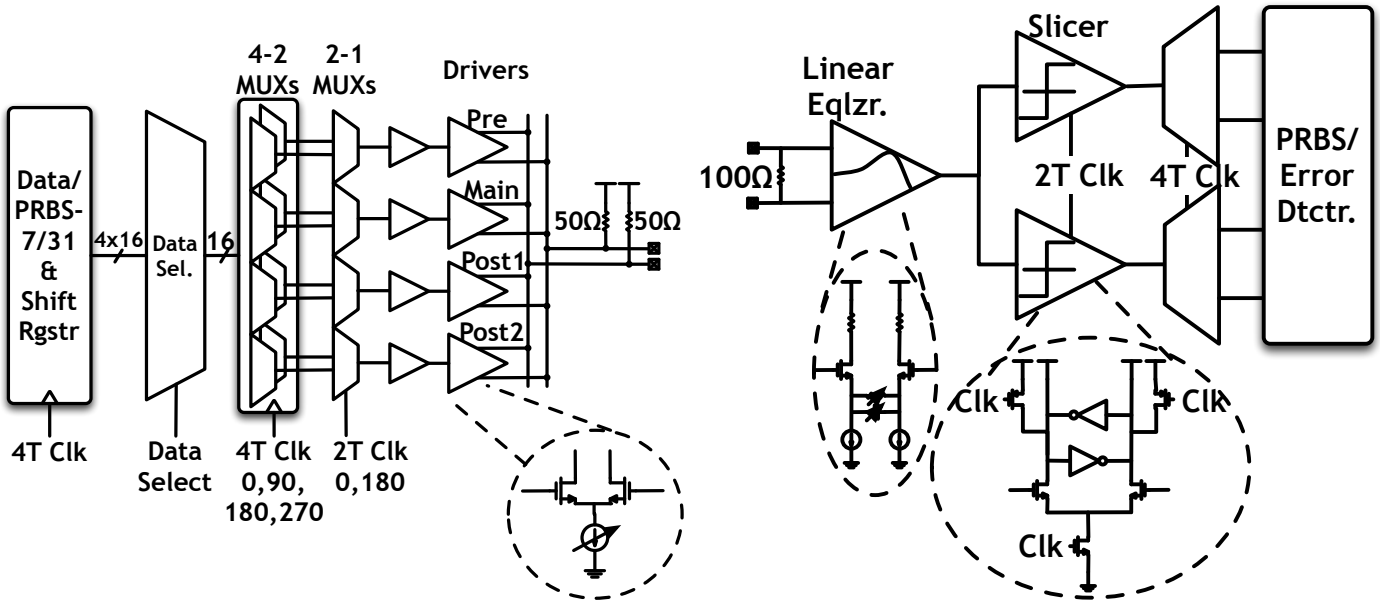


Figure 4.10: Total drivers and equalization power for data path as a function of the repeat distance

minimum receiver sensitivity. Modest equalization power is possible if data repeat distance is kept below 20dB channel loss, which is equivalent to 9m of CAT7 cable [40–44]. Channel loss beyond this requires added filtering which increases the power per repeater. This analysis uses realistic circuit simulations and includes varying the driver power for higher signal swing to compensate for cable loss. A shallow optimum exists between 4 and 8 meters. An 8-m data repeating distance is chosen to minimize the cost of inserting a large number of repeaters.

Figure 4.11 shows the transceiver block diagram of each repeater. The transmitter uses a half-rate architecture and comprises a 16-1 data serializer. The delay for the pre-emphasis FIR is performed in the low frequency digital section to save power. The CML driver has 1 precursor and 2 post-cursor pre-emphasis taps to achieve 9 dB of equalization. The pattern generator and the serializer are used to generate data at each repeater for signal quality and BER characterization. The receiver comprises a continuous time linear equalizer with 6 dB of equalization, and half rate slicers. 2-4 data deserializer and BERT are also needed to measure BER and characterize data quality. Quadrature outputs of the CMU are applied to a phase interpolator to set the clock phases for timing recovery at receiver.



(a) (b)

Figure 4.11: Schematic of the (a) transmitter and (b) receiver used in the data path

4.4 Summary

The chapter provides the different circuit details of the link. We introduce the high frequency MDLL and a calibration scheme to center the select aperture around the reference edge and therefore be able to push the MDLL frequency up to 6GHz. The fastest introduced in literature to the authors knowledge. We also introduce a capacitive coupled phase interpolator that's suitable for use in high frequency applications and has low power. We also introduce a low mismatch charge pump circuit with a loop filter leakage compensation scheme. Finally, we explain the transceiver implementation and choice of the data repeating distance.

CHAPTER 5

Measurement and Experimental Results

This chapter presents the link experimental and measurement results. The repeater prototype repeater is implemented in a 65-nm CMOS technology. The chapter is divided into two main sections. The first section covers the configurable PLL/MDLL measurement results including the low mismatch charge pump design. The second section presents the link measurement performance. It shows the jitter accumulation along the clock path and compares different clocking schemes including the proposed FIR filtering scheme. It also shows the data path results including the BER measurements and eye diagrams.

5.1 CMU Measurement Results

The CMU is separately characterized using a dedicated test chip built in a 90-nm CMOS technology and operates up to 4.6GHz. The design integrated into the repeater is built in 65-nm CMOS technology has an improved operating frequency of >6GHz. The test setup uses a real-time oscilloscope with a 15GHz bandwidth (TDS6154C). The scope can be configured to calculate fast Fourier transforms of the high-speed clock. By adjusting the captured frame size of the scope, the FFT bins can be placed on the MDLL reference spurs and thus spur performance of the MDLL can be accurately measured. Peak-to-peak periodic jitter (PJ) can be estimated from the reference spur measurement using the following equation:

$$PJ_{pp} \approx \frac{2}{\pi} T_{period} \times 10^{(\frac{dBc}{20})} \tag{5.1}$$

Overlaid onto Fig. 5.1 are the measurement results for the period jitter versus SEL aperture position using the 90-nm CMOS test chip . Period jitter drops to 0.7ps at the optimal setting,

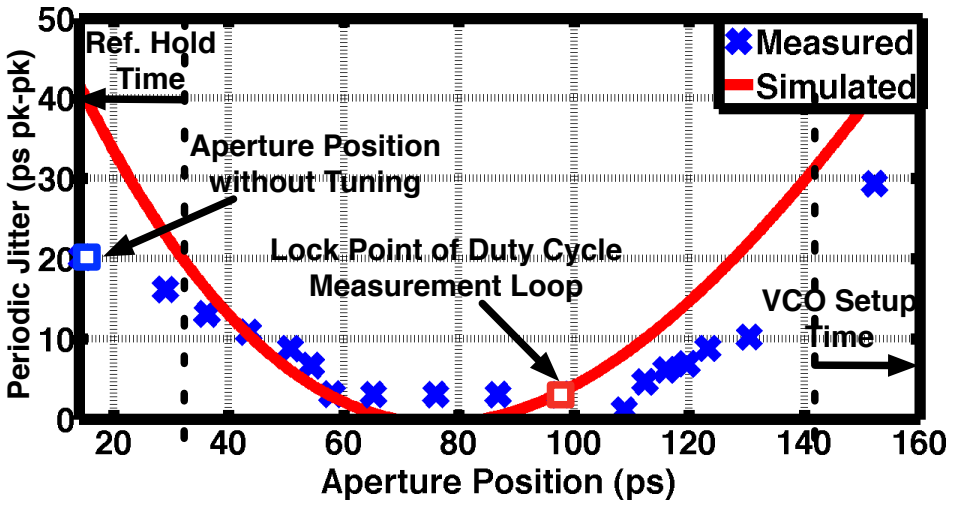


Figure 5.1: Measured tuning characteristic of the aperture circuit with simulation results overlaid. Aperture position without tuning is also shown.

the equivalence of -46dBc spur. By sliding the aperture to the right, period jitter increases slightly until the setup time of the mux with respect to the VCO edge, after which the period jitter increases sharply and the loop eventually loses lock. Similarly, sliding the aperture to the left approaches the hold time of the mux. Note that the period jitter sensitivity is shallow near the optimum and can absorb residual mismatch in the loop. The graph indicates the aperture position with and without the aperture calibration. After enabling the calibration loop by measuring the duty cycle, the period jitter reduces from 20ps to 0.7ps. Impact of charge pump mismatch reduction circuit is shown in Fig. 5.2. The reference spur is compared with and without activating the charge pump dynamic mismatch reduction circuit. When using the repeater test chip in 65-nm CMOS, 13dB spur reduction is measured when the CMU is configured as MDLL at 6GHz, while 9 dB is observed when configured as a PLL.

Random jitter of the MDLL is characterized using the scope time interval error measurement (TIE). The readout shows in Fig. 5.3 2ps RMS of random jitter. Because the reference source has 1.5ps RMS jitter and the scope has a 0.86ps RMS jitter floor and trigger error, a 1ps RMS random jitter is estimated. Table 5.1 summarizes the performance of the two implemented MDLLs at 4.6GHz & 6GHz and comparing them to previous publications.

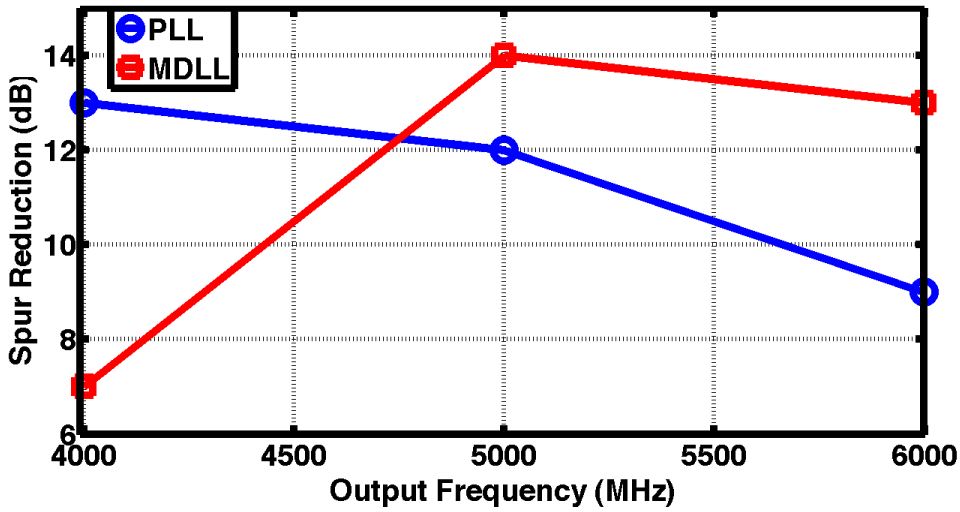


Figure 5.2: Measured reference spur reduction by turning on the charge pump dynamic mismatch correction circuit

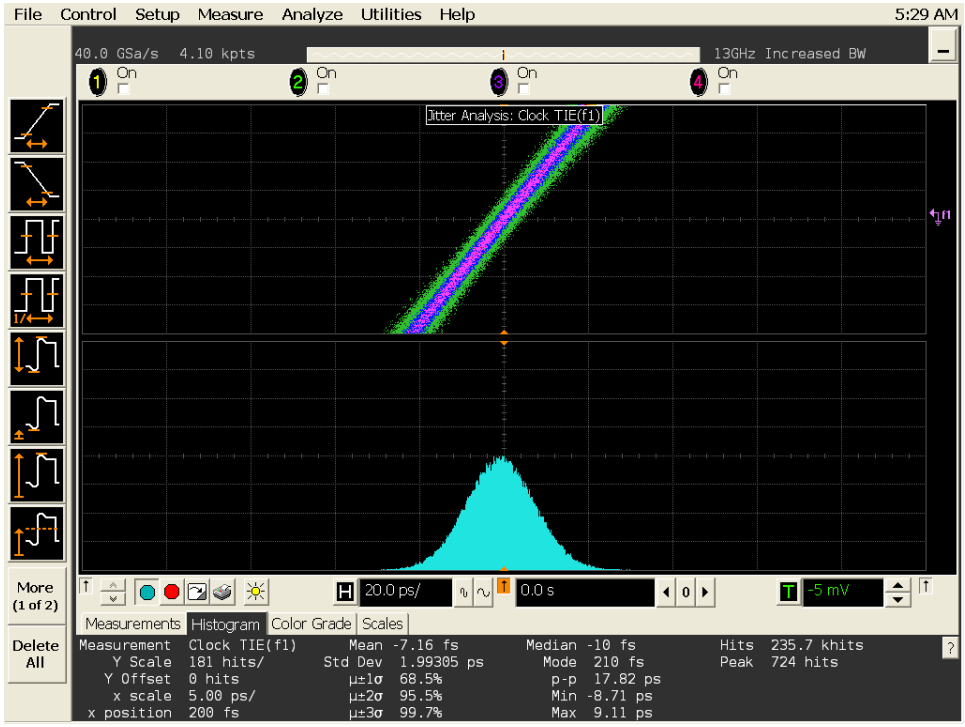


Figure 5.3: Time interval error measurement of the high speed MDLL output using real time scope

Table 5.1: MDLL Comparison with Previous Work

	[22]	[35]	[36]	MDLL in 90nm	MDL in 65nm
Freq. (GHz)	2	1.2	1.6	4.6	6
Ref. Freq. (MHz)	250	64	50	570	750
Spur (dBc)	-37	-46.5	-58.3	-46	-42
PJ (ps pk-pk)	4.5	2.5	0.48	0.7	0.84
RJ (ps rms)	-	-	0.68	1	1.1
Tech.	0.18μm	0.18μm	0.13μm	90nm	65nm
Power (mW)	12	19.8	8.2	6.8	9.6

5.2 Cable Link Measurements and Results

To achieve low jitter accumulation and total link power, we chose a clock repeating distance of 16m and a clock frequency of 750MHz similar to the results of the previous analysis. CAT7 cable segments are repeated 8 times to reach 115m. The test setup is shown in Fig. 5.4. A clock source launches a 500mV sinusoid clock at the input of the first clock repeater. A 5V supply powers the repeaters through one of the cable wire pairs. Each repeater board drops the supply to 1V/1.2V supplies by a linear regulator. The CAT 7 cable has $\sim 7\Omega$ of DC resistance per 100 meters (R_{100m}). The IR drop observed at the last repeater N, given repeater current of I_{rptr}, can be found by the arithmetic series:

$$IR = \frac{I_{rptr} R_{115m}}{2}(1 + N) \tag{5.2}$$

With about 50 mA of total repeater current, the IR drop of 8 repeaters is $\sim$2V. Voltage drop can be reduced by supplying power from both sides of the cable. Switching regulators can also be used to improve the efficiency of power distribution.

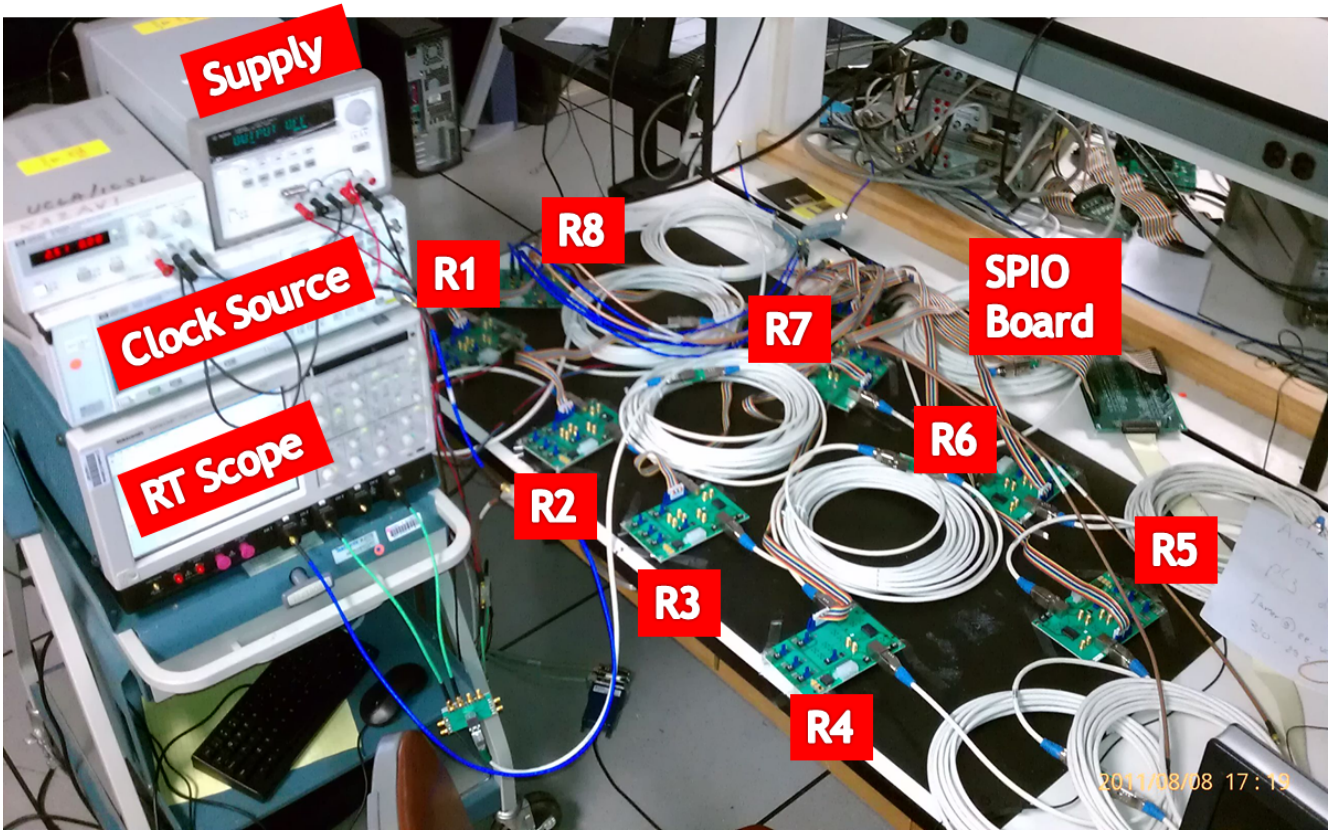


Figure 5.4: Test setup for a link using 115 meters of cable. The picture shows power supply, clock source, real time scope, and 8 clock repeaters

Absolute Jitter is measured at each clock repeater output using the real-time oscilloscope TDS6154C TIE measurement. Different clock forwarding configurations are examined. Namely, all-reference, all-PLL, MDLL with FIR, and configurable PLL/MDLL clock forwarding. The results are depicted in Fig. 5.5. The plot shows absolute jitter accumulation from one clock repeater to the next across the link. As obvious from the plot, reference clock forwarding and PLL clock forwarding results in 16.5ps and 6.6ps of RMS jitter at the link output, respectively. Those are excessive amounts of jitter that cannot be tracked by a practical receiver at the end of the link. Although all-PLL forwarding shows less jitter accumulation than all-reference forwarding, yet the clock exhibits excessive jitter peaking due to cascaded stages of PLLs and high ring oscillator jitter. The 4^{th} repeater in the all-PLL forwarding also has excessive jitter transfer peaking due to process variation. The other

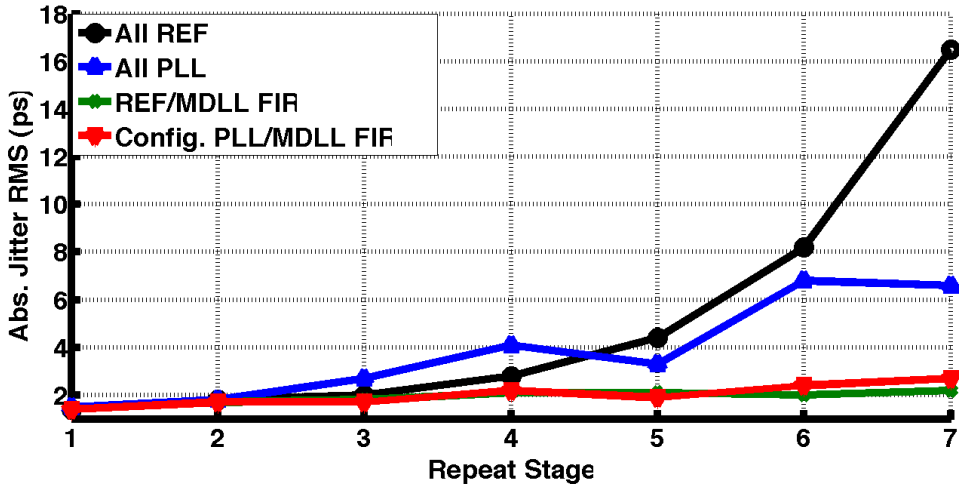


Figure 5.5: Jitter accumulation inside the clock repeaters for 4 different clocking configurations

lines in the graph show the benefit of CMU configurability and FIR technique in lowering the link jitter. The FIR filtering technique with MDLL divided output results in 2.2ps RMS jitter. The configurable PLL/MDLL yields 2.7ps RMS jitter. Note that with an FIR a PLL setting is not needed since the input noise is kept low. The settings for the FIR coefficients and the CMU input mux are overlaid in the figure. As discussed in section 3.5, all-MDLL and mostly-MDLL ($\alpha = 100\%, 80\%$) setting is needed early on the link to favor forwarding of the clean clock. Later on the link, PLL or semi-PLL ($\alpha = 0\%, 20\%$) setting is used to benefit from PLL filtering. Also repeater 4 CMU shows excessive jitter in PLL mode and is bypassed altogether from clock forwarding by setting ($\alpha = 100\%$).

While absolute jitter is a crucial metric for asynchronous data reception by a CDR module at the end of the cable, uncorrelated jitter is important for synchronously clocked systems to determine tracking between the data and clock paths. Fig. 5.6 portrays the untracked jitter accumulation across the link for a delay of 1 forward clock period. For an All-PLL system, the untracked jitter is 3.4ps rms at the output of the under-damped 4th repeater, and 2.8ps rms at the last repeater. The jitter tracking for the FIR filtered technique outperforms the all-PLL design. It shows 31% reduction in untracked jitter with respect to the all-PLL at the 4th repeater, and 18% reduction at the last repeater. The result suggests the link can

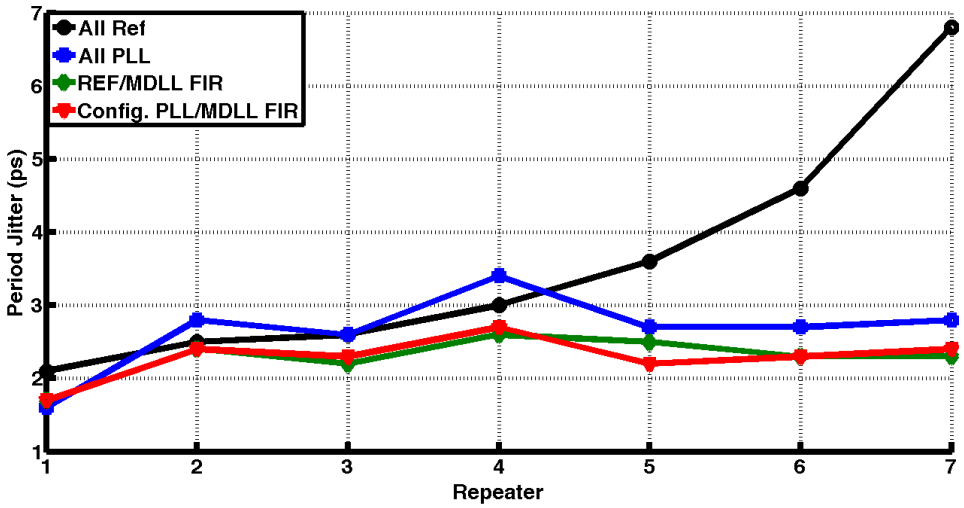


Figure 5.6: Uncorrelated jitter accumulation inside the clock repeaters for 4 different clocking configurations

be extended even further with good jitter tracking capability. The plot also shows the all-reference forwarding has excessive untracked jitter across one period that renders it unusable for clock forwarding.

Data path characterization is performed at the last 2 repeaters where clock jitter is the maximum. Fig. 5.7 shows the bathtub curves for the link at 12Gbps. At the Tx output, the bathtub plot is obtained by sweeping the clean source clock phase with respect to the data. The Tx eye is completely closed for all-reference and all-PLL clocking forwarding. For the configuration using the MDLL with FIR filtering, 0.55UI open eye is measured at the Tx output. At the receiver input the eye opening is 0.27UI at BER of 10^{-12} for a PRBS31 pattern.

Data eye diagrams are shown in Fig. 5.8. The eye diagram is completely closed in case of all-reference forwarding whether it's triggered by an asynchronous clean clock as in Fig. 5.8(a), or triggered by the same forward clock as in Fig. 5.8(b). In case of all-PLL forwarding, eye is completely closed with asynchronous triggering in Fig. 5.8(c), which suggests inoperability of an asynchronous CDR at the Rx side. However, all-PLL clock forwarding shows good tracking with data, Fig. 5.8(d), and 4.9ps RMS jitter. On the other

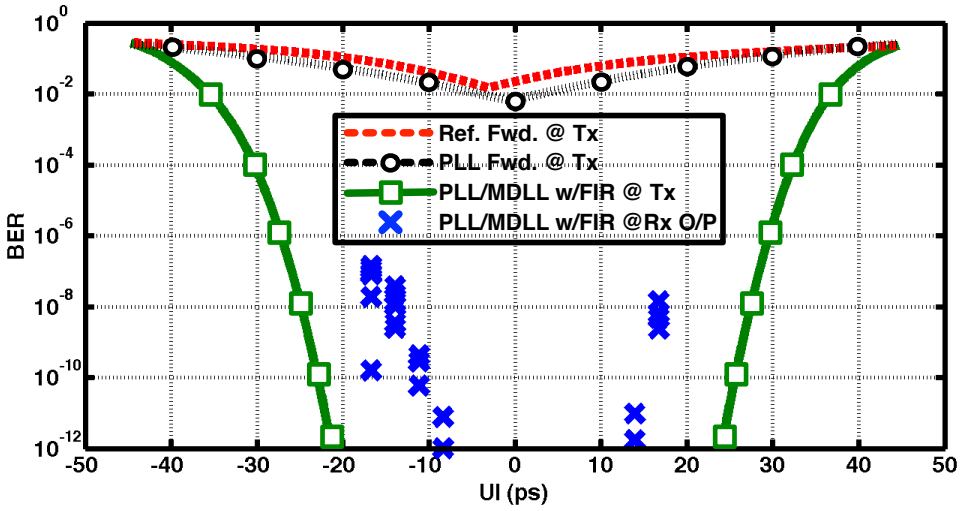
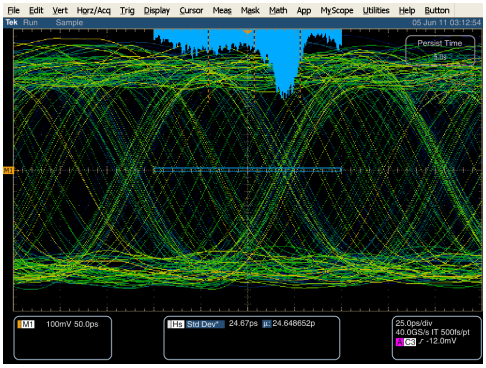


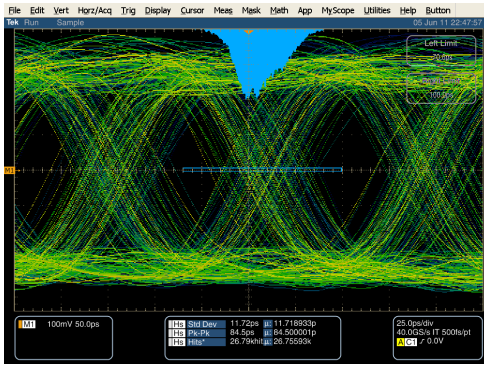
Figure 5.7: Bath-tub curve of the received data eye at the end of the 115-m link for different CMU configurations

hand, MDLL and FIR filtering outperforms all-PLL clock forwarding whether it is triggered asynchronously or synchronously. In Fig. 5.8(e) and (f), the eyes show 4.4ps and 3.9 RMS jitter at the end of the link with asynchronous and synchronous triggering, respectively. The pattern used is PRBS-31 pattern.

Table 5.2 summarizes the link performance. The CMU section consumes a total of 9.6mW. The transmitter driver and pre-driver dissipate the majority of power at 24.4mA due to the voltage swing and the pre-emphasis. The receiver front end consumes 1.2mA. The clock driver consumes 5mA. Total chip power is 48mW including high-speed pattern generators and error detectors. Reliable reception is demonstrated at the end of a 115m CAT7 cable at 12Gbps. Total repeater chip area is 1mm^2. With such a small area and power, it is feasible to embed such a repeater within a cable for extending the reach of copper cables. The chip micrograph in Fig. 5.9 shows the design with each building block marked individually.



(a)



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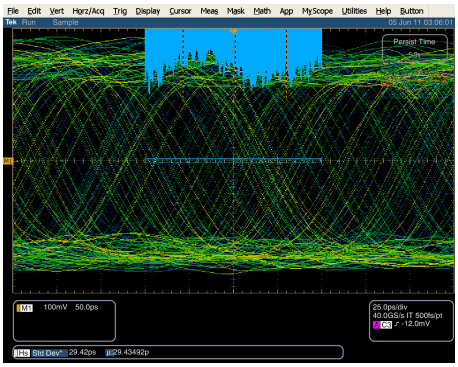

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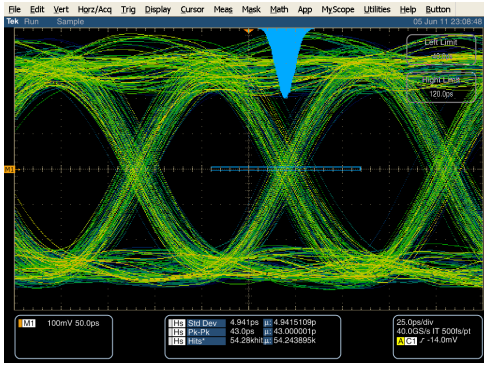

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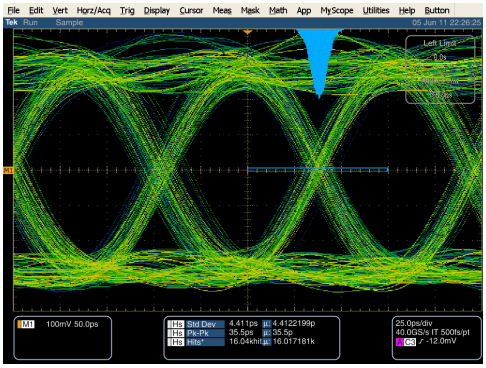
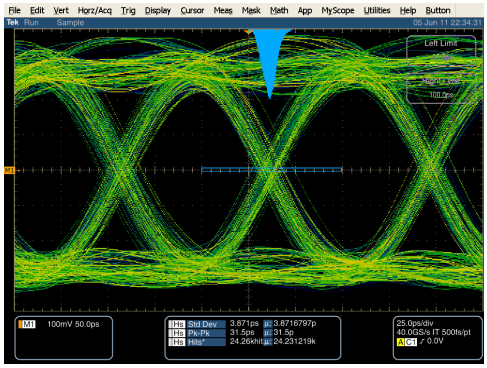


(e)



(f)

Figure 5.8: Eye diagrams (a) All reference-forwarding with source trigger (b) with fwd. clock trigger (c) All-PLL with source trigger (d) with fwd. clock trigger (e) FIR filtering with source trigger (f) with fwd. clock trigger

5.3 Summary

This chapter provides the measurement and experimental results of the link. It starts with the MDLL measurement results and shows a low jitter performance of 0.84ps peak-to-peak

Table 5.2: Link Performance Summary

Power	CMU	9.6mW	1,1.2V Supply
	PI for FIR	1mA	1V Supply
	Pre-Driver & Driver	24.4mA	
	Rx Front End	1.2mA	
	Clock Driver	5mA	
	Total Power/Rpt.	48mW	
Fwd. Clock Freq.		750MHz	
Data Rate		12Gbps	
Clk Jitter at Cable End		2.2ps RMS	
Jitter at Tx Eye (PRBS31)		4.4ps RMS	
Total Cable Distance		115m/CAT7	
Repeater Chip Area		$1mm^2$	
Technology		65nm CMOS	

of period jitter, and 1.1ps RMS random jitter at 6GHz. The chapter then provides the link measurement results. It compares the jitter performance of the proposed FIR filtering scheme, a PLL/MDLL configurable scheme with all-PLL and all-reference forwarding. The results show that the FIR filtering and the PLL/MDLL configurability have superior performance compared to all-PLL and all-reference forwarding. It also shows that FIR filtering outperforms PLL/MDLL configurable approach in absolute jitter. A 2.2ps RMS jitter is observed for the former versus 2.7ps RMS jitter for the later. The chapter then presents link data transmission results. This includes the bath-tub curves and eye diagrams. The data link has a 4.4ps RMS jitter at the output of the last repeater transmitter. The eye

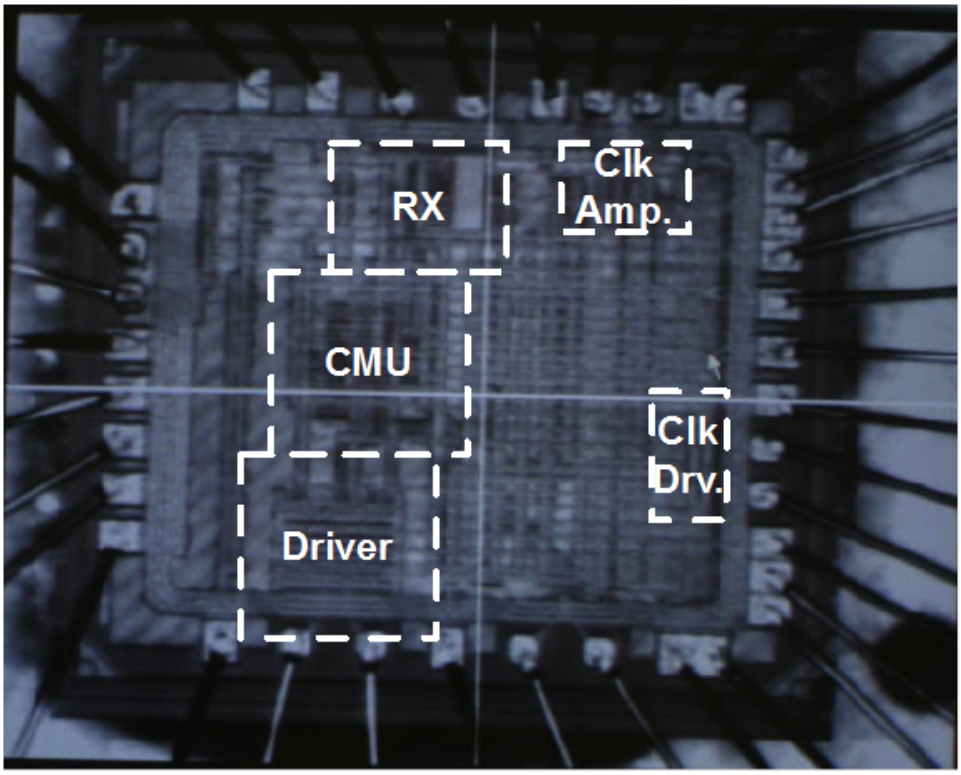


Figure 5.9: Chip micrograph

opening at the receiver input is 0.27UI at 12Gbps. Measurement results show reliable link transmission which validate the proposed link feasibility.

CHAPTER 6

Conclusion and Future Work

This work demonstrates the potential use of source synchronous repeaters as means of extending multi-Gbps cable links for distances exceeding 100 meters. A 115 meter CAT7 cable is used to demonstrate reliable data transmission at 12Gbps. Longer reach can potentially be achieved since the total jitter at the end of the cable is only 4.4ps RMS. The work describes and validates an area-efficient phase filtering technique using a phase-based FIR to filter jitter across cascaded repeaters. To achieve both the clock multiplication and the phase delay of the FIR, an MDLL is used that can produce a 6GHz clock output. While challenges such as mechanical attachment, robustness to strain, tracking of environmental variations, etc., clearly exist for a repeater based copper link that embeds the repeater within the cable, this work indicates that the power and area requirements for the electronic circuits is feasible.

The work also provides a fast semi-analytical method for modeling linear time variant noise accumulation across clock forwarded repeaters. The analysis provides accurate correlation with transient noise analysis and measured accumulated jitter for low and moderate levels of jitter accumulation. Because the analysis is based on a linear noise analysis, it tends to overestimate jitter when noise level increases and perturbs the DC operating point of the repeater.

The work also demonstrates the fastest multiplying delay locked loop implemented in literature. We were able to push the MDLL operation up to 6GHz by accurately placing the select aperture with respect to reference and VCO pulses. This MDLL exists at the core of the our clocking and filtering scheme. Its inputs can be configured to select the lowest of the input clock and the VCO clock for clock multiplication. Thus, it prevents jitter accumulation

along the link. Outputs are also mixed to provide an effective FIR phase filter to filter the output clock.

In the implemented prototype, a dedicated clock channel is used to forward the clock. In future work, the dedicated channel can be eliminated altogether and clock forwarding occurs on the common mode of the data channels [25] or the power lines [29]. Along that same line, a referenceless CDR could also be a viable alternative that needs to be investigated for repeater based copper cables.

Finally, to complete the experiment, multiple data channels could be added and the effect of cross talk on the entire link should be examined.

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