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Authors

Zhu, Yicheng
Zou, Jiarui
Pilawa-Podgurski, Robert

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Y. Zhu
J. Zou
R. C. N. Pilawa-Podgurski

A 1500-A/48-V-to-1-V Switching Bus Converter for Next-Generation Ultra-High-Power Microprocessors

Yicheng Zhu, Jiarui Zou, and Robert C. N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Email: {yczhu, jiarui.zou, pilawa}@berkeley.edu

***Abstract*—This paper presents a switching bus converter, an ultra-high-current hybrid switched-capacitor (SC) voltage regulator for single-stage 48-V-to-1-V vertical power delivery, for next-generation ultra-high-power microprocessors (e.g., GPUs, CPUs, ASICs, etc.). The proposed switching bus converter consists of two 2-to-1 SC front-ends and four 10-branch series-capacitor-buck (SCB) modules, merged together through four switching buses. Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. Through a topological comparison, this paper reveals that the proposed topology achieves the lowest normalized switch stress and the smallest normalized passive component volume compared with existing 48-V-to-1-V hybrid SC demonstrations, showing great potential for both higher efficiency and higher power density than prior solutions. A hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards to validate the functionality and performance of the proposed switching bus converter. It was tested up to 1500-A output current and achieved 92.7% peak system efficiency, 85.7% full-load efficiency (including gate drive loss), and 759 W/in^3 power density (by box volume), pushing the performance limit of the state-of-the-art 48-V-to-1-V works in previous literature.**

I. Introduction

High-performance microprocessors (e.g., GPUs, CPUs, ASICs, etc.) serve as the engine of data center computing platforms and the foundation for technical progress in areas such as artificial intelligence, deep learning, autonomous vehicles, and countless other applications. In recent years, the electric power consumption of microprocessors has increased dramatically and is approaching 1000 W due to the fast-growing demand for greater computational power. For example, as shown in Fig. 1, the thermal design power (TDP) of one NVIDIA GPU platform has grown by 10 times in the past decade, from 106 W to 1000 W. And just in the past three years alone, the TDP has more than doubled.

As power levels increase, the 48-V bus architecture is gradually replacing the legacy 12-V bus in modern data centers since the power distribution losses (i^2R losses) decrease by sixteen-fold with the quadrupling of the bus voltage. This makes the design of the voltage regulation modules (VRMs) responsible for the 48 V to Point-of-Load (PoL) power conversion more challenging with a quadrupled voltage conversion burden. To address these challenges, multiple regulated hybrid switched-capacitor (SC) topologies have been proposed in previous literature for 48-V-to-PoL conversion in data centers [1]–[12].

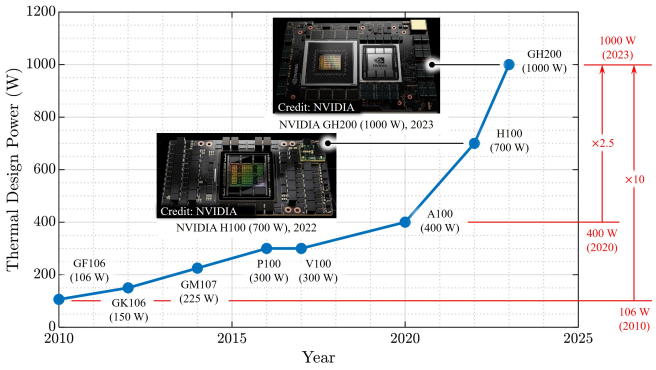

Fig. 1: Rapid growth in thermal design power of NVIDIA data center GPUs.

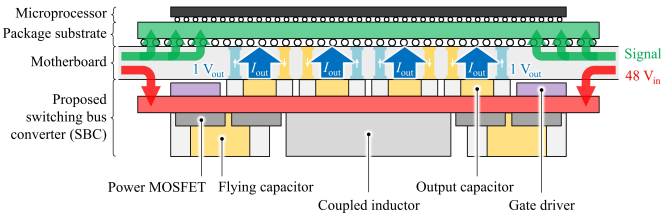

Fig. 2: Single-stage 48-V-to-1-V vertical power delivery (VPD) for next-generation ultra-high-power microprocessors with the proposed switching bus converter (SBC).

As an emerging family of topologies, hybrid SC converters can leverage both the greatly superior energy density of capacitors compared to magnetic components [13], [14] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [15].

With operating currents beyond 1000 A, the high power distribution network (PDN) resistance of the current lateral power delivery (LPD) solution can lead to a dramatic voltage drop and unacceptable power distribution losses, which significantly limits processor performance, reduces system energy efficiency, and hinders data center decarbonization. Moreover, the resulting low efficiency necessitates a larger size of the thermal management solution, which is presently a bottleneck of system densification.

This work presents a high-performance 48-V-to-1-V switching bus converter (SBC) to address the above challenges through vertical power delivery (VPD), as illustrated in Fig. 2. With the sufficiently high power density enabled by the switching-bus-based architecture, the proposed switching bus

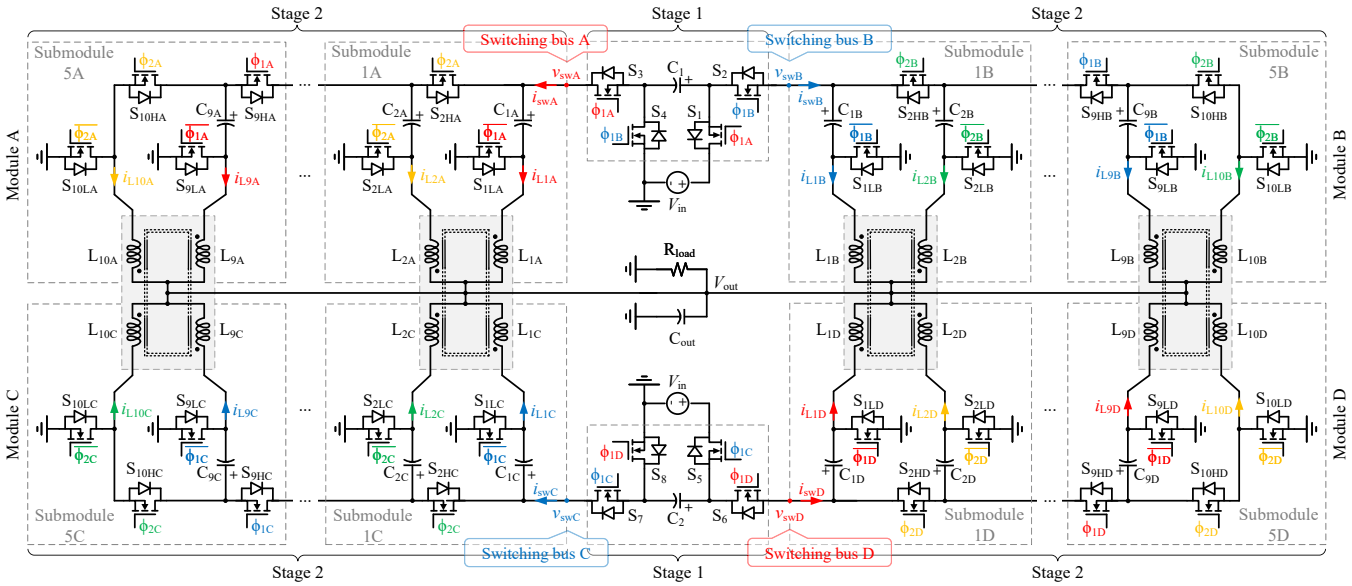

Fig. 3: Schematic drawing of the proposed switching bus converter (SBC).

converter can be placed on the bottom side of the motherboard directly underneath the processor and vertically deliver the high output current to the processor on the top side through the vias on the motherboard, which can greatly reduce the PDN loss and save the valuable topside area on the motherboard for high-speed communication and memories. Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

II. Switching Bus Converter

A. Proposed Topology and Operating Principles

Fig. 3 shows the schematic drawing of the proposed switching bus converter. In the proposed topology, two 2-to-1 SC front-ends (i.e., Stage 1) are merged with four 10-branch series-capacitor-buck (SCB) modules (i.e., Modules A-D in Stage 2) through four intermediate buses (i.e., Switching buses A-D). Since the intermediate bus voltages v_{swA}-v_{swD} always switch between two voltage levels rather than being DC, this type of intermediate bus is referred to as a *switching bus*. The concept of a switching bus was first introduced in [10].

Each SCB module consists of five submodules and operates in a two-phase fashion with a 180° phase shift between neighboring branches. The control signals of Modules C and D are 90° phase shifted with respect to those of Modules A and B to enable the use of four-phase coupled inductors illustrated in the grey rectangles.

B. Advantages of the Switching-Bus-Based Architecture

The most straightforward approach to combining two (or multiple) conversion stages is to link them with an intermediate DC bus, as illustrated in Fig. 4(a). This DC-bus-based architecture typically requires a large and bulky bus capacitor ($\mathrm{C_{bus}}$) to maintain a stiff DC bus voltage (V_{DC}), which hinders converter miniaturization.

Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture shown in Fig. 4(b) has three advantages that promise higher performance:

- It does not require bus capacitors to maintain a stiff DC bus voltage.
- One redundant switch can be removed on each switching bus while two stages are merged.
- It ensures complete soft-charging operation.

Fig. 5 illustrates the two-stage merging process based on the switching bus architecture. First, open the output node of the 2-to-1 SC converter in Stage 1 as shown in Fig. 5(a), leaving two floating nodes v_{swA} and v_{swB}. Second, as illustrated in Fig. 5(b), connect a series-capacitor buck (SCB) module to each of these floating nodes through a switching bus. After this combination, we can see that the highest high-side switch $\mathrm{S_{1HA}}$ in Module A is connected in series with $\mathrm{S_3}$ and $\mathrm{S_{1HB}}$ in Module B is in series with $\mathrm{S_2}$. Since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, compared to the DC-bus-based architecture, the switching-bus-based architecture enables a reduction in the number of switches.

C. Topological Comparison

To compare the theoretical potential of the proposed topology to that of existing 48-V-to-1-V hybrid SC topologies, this paper uses two metrics for topological comparison [16].

The first metric is the normalized switch stress M_{S}, defined as the total switch volt-ampere (VA) stress normalized to the output power

$$M_{\mathrm{S}} = \frac{\sum\limits_{\text{switches}} V_{\mathrm{ds},i} I_{\mathrm{d(rms)},i}}{V_{\mathrm{out}} I_{\mathrm{out}}}, \tag{1}$$

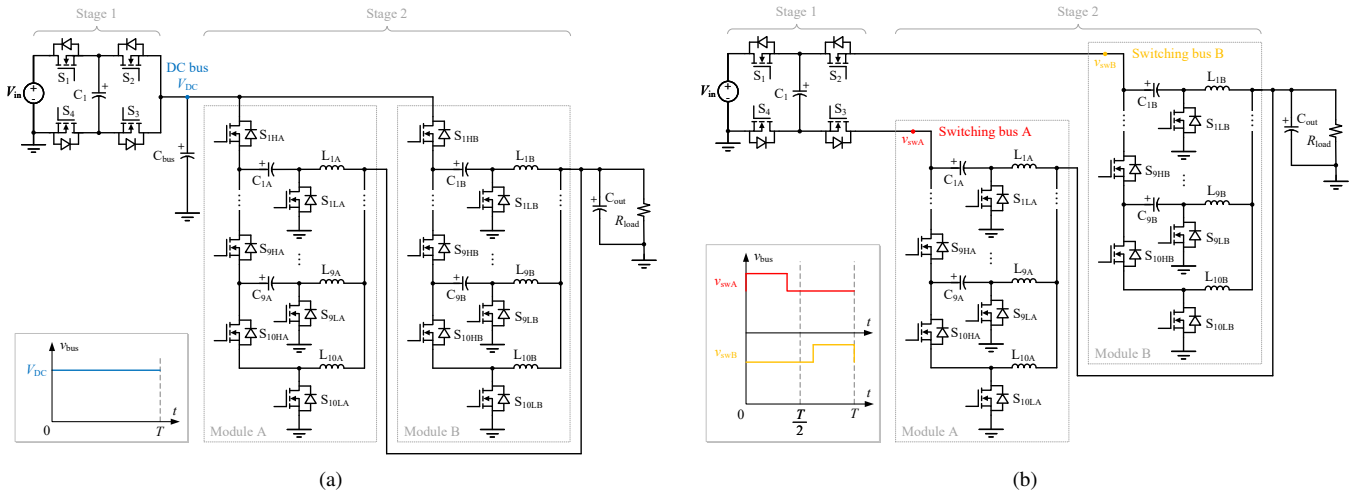

Fig. 4: Comparison between the existing DC-bus-based architecture and the proposed switching-bus-based architecture. (a) DC-bus-based architecture. (b) Switching-bus-based architecture. Compared to the DC-bus-based architecture, the switching-bus-based architecture does not require bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

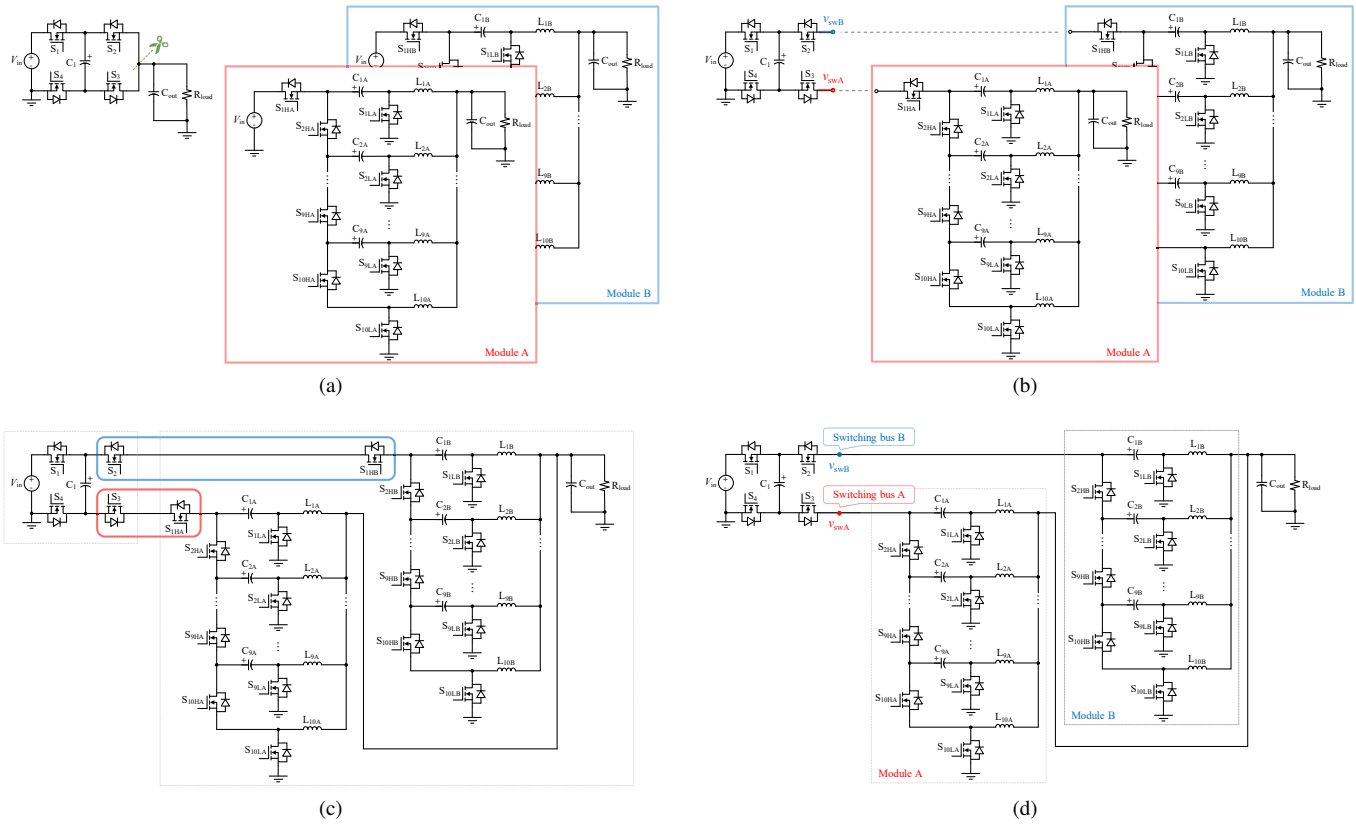

Fig. 5: Illustration of the two-stage merging process based on the switching bus architecture. (a) First, open the output node of the 2-to-1 SC converter in Stage 1, leaving two floating nodes v_{swA} and v_{swB}. (b) Second, connect a series-capacitor buck (SCB) module to each of the floating nodes through a switching bus. (c) Third, since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, switches $\mathrm{S_{1HA}}$ and $\mathrm{S_{1HB}}$ are removed. (d) Finally, obtain the topology of one switching bus converter.

where $V_{\mathrm{ds},i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{\mathrm{d(rms)},i}$ is the RMS value of the current through switch i when assuming no inductor current ripple. The normalized switch stress M_{S} indicates how much VA stress the switches in a topology experience when transferring one per-unit watt of power from the input to the output. A lower M_{S} is desirable, as it indicates lower switching losses and lower conduction losses and thus

TABLE I: Topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations

Year	Reference	SC Stage Conversion Ratio	Buck Stage Conversion Ratio	Buck Stage Duty Ratio	Normalized Switch Stress	Normalized Passive Component Volume
2020	Crossed-coupled QSD buck [1]	4:1	12:1	0.083	24.2	2.08
2020	DIH [2]	6:1	8:1	0.125	14.7	2.40
2021	CaSP [3]	6:1	8:1	0.125	23.5	2.02
2022 2023	LEGO [4] Mini-LEGO [5]	6:1	8:1	0.125	17.6	2.41
2023	SDIH [6]	6:1	8:1	0.125	14.7	2.40
2022	MLB [7]	8:1	6:1	0.167	23.7	2.03
2022	VIB [8]	8:1	6:1	0.167	14.3	2.07
2023	MSC [9]	8:1	6:1	0.167	15.1	1.95
2022	Dickson^2 [10]	9:1	5.33:1	0.188	14.8	1.90
2023	16-to-1 SBC [11]	16:1	3:1	0.333	10.2	1.69
2023	This work (20-to-1 SBC [12])	20:1	2.4:1	0.417	8.99	1.56

TABLE II: Component list of the hardware prototype

Component (X = A, B, C, D)	Part number	Parameters
MOSFET S_{1-8}	Infineon IQE013N04LM6CGSC	40 V, 1.35 mΩ, dual-side cooling
MOSFET $S_{2HX-10HX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
MOSFET $S_{1LX-10LX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
	Infineon IQE004NE1LM6	15 V, 0.45 mΩ
Flying capacitor $C_{1,2}$	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μF*×20 (in parallel)
Flying capacitor C_{1X-6X}	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μF*×6 (in parallel)
Flying capacitor C_{7X-9X}	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×6 (in parallel)
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μF*×14 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μF*×248 (in parallel)
Gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
Low-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink
High-side gate driver in Stage 2	Texas Instruments LM27222	3-A peak source, 4.55-A peak sink

* The capacitance listed in this table is the nominal value before DC derating.

higher efficiency. A lower M_{S} also indicates a smaller switch size, which is favorable to higher power density.

The second metric is the normalized passive component volume M_{P}, which can be assessed with an energy-based approach by analyzing the peak energy stored in each passive component [14], [17]. The normalized passive component volume M_{P} indicates the total passive component volume needed to meet the given ripple requirements on the inductor currents and flying capacitor voltages when transferring one per-unit watt of power from the input to the output. A smaller normalized passive component volume is desirable, as it indicates higher power density.

Table I compares the two metrics of this work and those of existing 48-V-to-1-V hybrid SC demonstrations. Detailed derivations and analyses of these two metrics can be found in [16]. As can be seen in Table I, the proposed topology achieves the largest SC stage conversion ratio with the lowest normalized switch stress and the smallest normalized passive component volume, showing great potential for both higher efficiency and higher power density than prior solutions.

III. Hardware Implementation

A 48-V-to-1-V hardware prototype was designed and built to verify the functionality and performance of the proposed converter. Fig. 6 shows the annotated photograph of the prototype, with the top view showing the power stage and the bottom view showing the gate drive circuitry. The main circuit components are listed in Table II. The power board has 6 layers, with 6-oz copper on the two outer layers and 2-oz copper on the four inner layers.

To achieve high performance, we customized the magnetics and gate drive circuitry for this prototype, as shown in Fig. 7. Each group of inductors highlighted in the grey rectangles in Fig. 3 was implemented as the custom four-phase coupled inductor presented in Fig. 7(a). This coupled inductor consists of two pieces of Mn-Zn ferrite cores and four pieces of one-turn windings. One practical challenge of the hardware implementation is the gate drive circuitry for the high-side switches in the second stage (i.e., $S_{2HA-10HA}$ and $S_{2HB-10HB}$) since the conventional cascaded bootstrap circuit suffers from accumulative voltage drops across the bootstrap

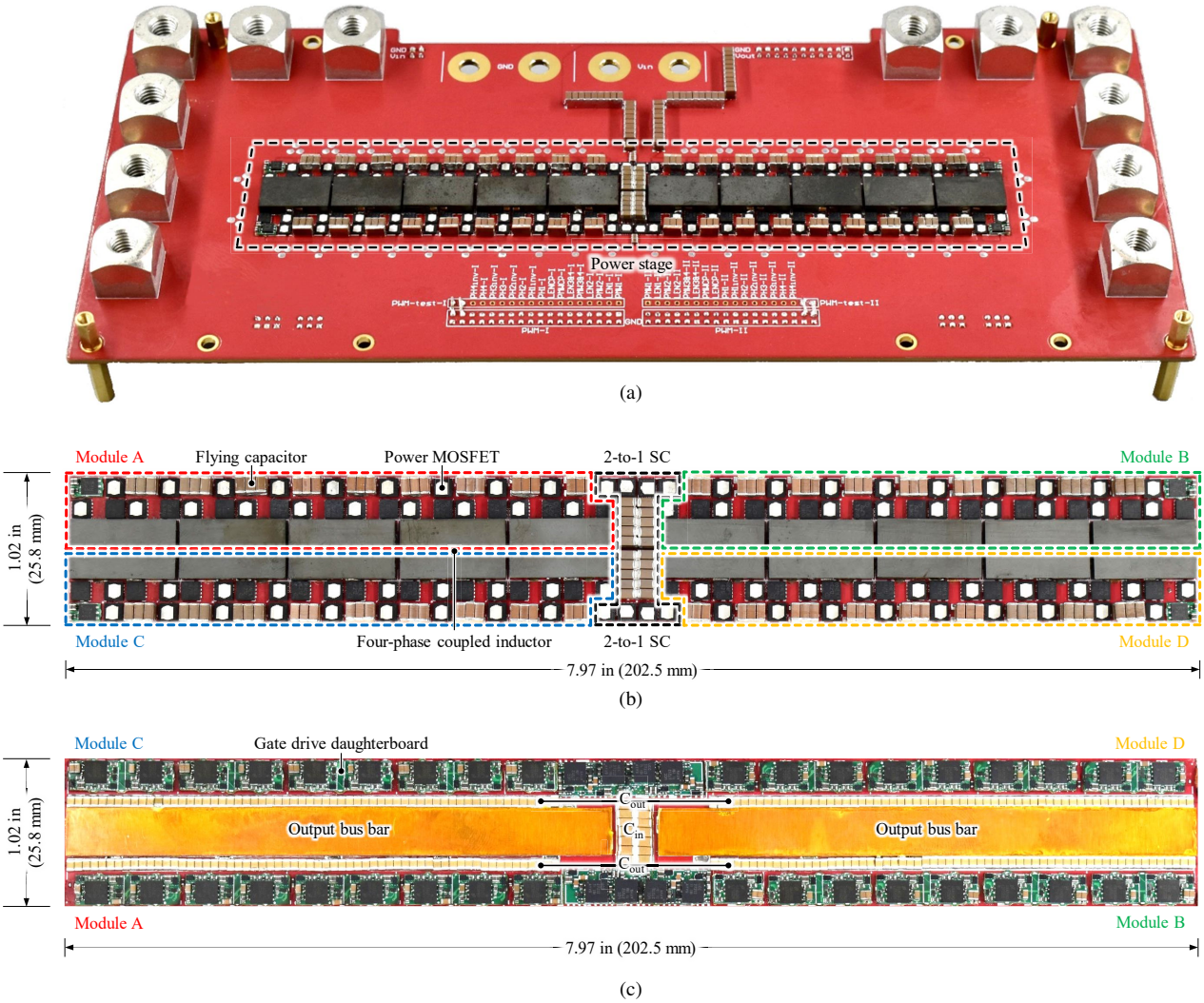

Fig. 6: Photograph of the hardware prototype. Converter dimensions: $7.97 \times 1.02 \times 0.244$ in^3 ($202.5 \times 25.8 \times 6.2$ mm^3). (a) Complete view. (b) Top view showing the power stage. (c) Bottom view showing the gate drive circuitry.

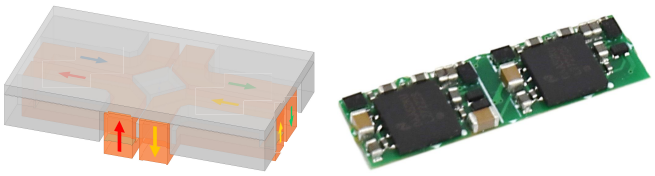

Fig. 7: Custom components for high-performance implementation of the proposed switching bus converter. (a) 3D rendering of the custom four-phase coupled inductor with current paths annotated. Dimensions: $18.5 \times 10.5 \times 3.2$ mm^3. (b) Photograph of the custom gate drive daughterboard. Dimensions: $18.5 \times 5.5 \times 1.0$ mm^3.

TABLE III: Key parameters and test conditions of the hardware prototype

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Maximum tested output current	1500 A (37.5 A/phase)
Switching frequency	220 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	6.5 V
Low-side gate drive voltage of Stage 2	5.3 V
Prototype box volume*	1.98 in^3
Power density by box volume	759 W/in^3

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.

diodes [18]. To tackle this challenge, this work adopts a hybrid gate drive circuitry [12] composed of gate-driven charge pump circuits and cascaded bootstrap circuits that were implemented as the green daughterboards shown in Fig. 7(b) that were mounted on the bottom side of the PCB, as presented in Fig. 6(c).

IV. Experimental Results and Performance Comparison

A. Experimental Results

To validate the performance of the proposed switching bus converter, the hardware prototype was tested up to 1500-

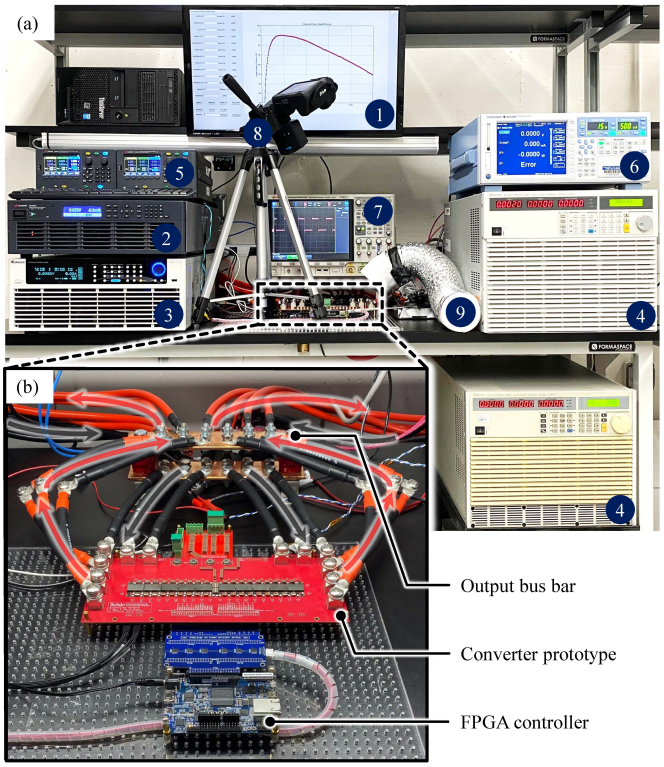

Fig. 8: Experimental setup for automated efficiency measurement with remote control of equipment. (a) Bench setup. (b) Prototype under test. List of equipment: ① Monitor for displaying measurement results. ② Keysight RP7962A regenerative power system (500 V/±40 A). ③ Chroma 63206A-60-1000 DC electronic load (60 V/1000 A). ④ Chroma 63203 DC electronic load (80 V/600 A) ×2. ⑤ Keysight E36312A triple output programmable DC power supply used to power the control and gate drive circuitry. ⑥ Yokogawa WT3000E precision power analyzer used to measure the input voltage, input current, and output voltage. ⑦ Keysight oscilloscope. ⑧ FLIR thermal camera. ⑨ Air inlet of the air cooling system.

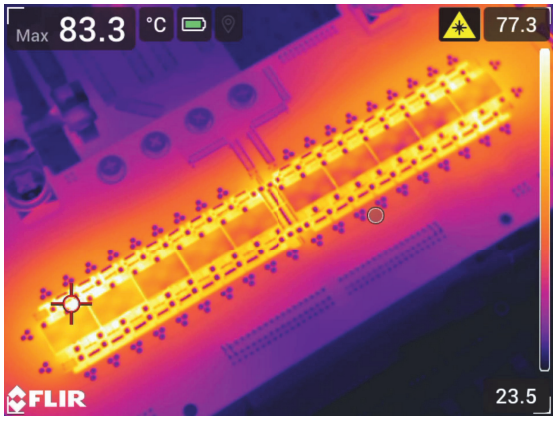

Fig. 9: Thermal image at equilibrium with air cooling only ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 1300$ A).

A output current at 220-kHz switching frequency with 48-V input voltage and 1-V output voltage. Table III lists the key parameters and test conditions of the hardware prototype. Fig. 8 shows the experimental setup for automated efficiency measurement with remote control of equipment. A 1000-A Chroma 63206A-60-1000 DC electronic load and two 600-

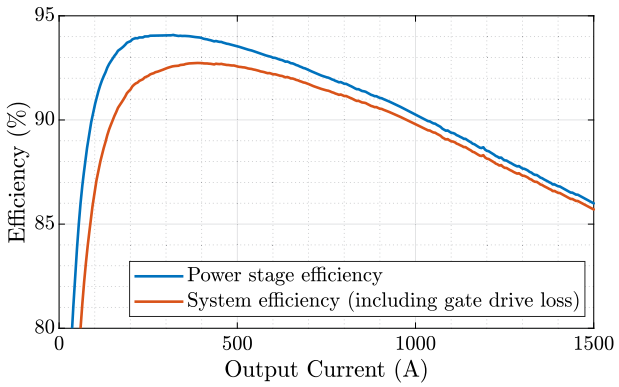

Fig. 10: Measured 48-V-to-1-V efficiency. Peak efficiency: 94.1% at $I_{\text{out}} = 320$ A (92.7% at $I_{\text{out}} = 395$ A including gate drive loss). Full-load efficiency: 86.0% (85.7% including gate drive loss) at $I_{\text{out}} = 1500$ A.

A Chroma 63203 DC electronic loads were used to sink the ultra-high output current of the converter. The input voltage, input current, and output voltage were measured with a high-precision Yokogawa WT3000E power analyzer. The output current was measured by the DC electronic loads. A FLIR thermal camera was used to monitor the surface temperature of the prototype.

At 1500-A output current, the prototype achieved a power density of 759 W/in^3 by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry). Fig. 9 shows the thermal image of the prototype running continuously at 1300-A output current with air cooling only. It should be noted that the current hardware prototype does not incorporate any heat sink, heat spreader, or any other type of thermal management system. For continuous operation above 1300 A and converter temperature below 85°C, either improved heat-sinking in air-cooled systems, or incorporation of liquid-cooling technology is needed. For example, a custom cold plate can be designed for the prototype utilizing the space above the switches between the flying capacitors and coupled inductors and leveraging the dual-side cooling package of the power MOSFETs.

Fig. 10 presents the measured efficiency of the hardware prototype. It achieved 94.1% peak power stage efficiency at 320-A output current and 86.0% full-load power stage efficiency at 1500-A output current. With the gate drive loss included, it achieved 92.7% peak system efficiency at 395-A output current and 85.7% full-load system efficiency.

B. Performance Comparison

Table IV compares the performance of this work with that of the state-of-the-art 48-V-to-1-V works presented in previous literature, with the system performance of each work at the peak system efficiency point and the full-load point plotted in Fig. 11. As evident from Table IV and Fig. 11, this work achieved the highest output current and demonstrated outstanding efficiency and power density, pushing the performance limit toward the top-right corner of Fig. 11 which represents higher overall performance.

TABLE IV: Performance comparison between this work and the state-of-the-art 48-V-to-1-V works

Year	Reference	Output Current	Power Density†	Power Stage Efficiency	System Efficiency‡
2023	This work (20-to-1 SBC [12])	1500 A (37.5 A/phase)	759 W/in^3 (by box volume)	Peak efficiency: 94.1% Full-load efficiency: 86.0%	92.7% 85.7%
2023	16-to-1 SBC [11]	500 A (31.3 A/phase)	464 W/in^3 (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	MSC [9]	450 A (28.1 A/phase)	621 W/in^3 (by box volume)	Peak efficiency: 93.1% Full-load efficiency: 86.2%	91.7% 85.8%
2023	Mini-LEGO [5]	240 A (20 A/phase)	1390 W/in^3 (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2022	Dickson^2 [10]	270 A (30 A/phase)	360 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [8]	450 A (28.1 A/phase)	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [7]	60 A (30 A/phase)	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	SDIH [6]	105 A (52.5 A/phase)	598 W/in^3 (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	LEGO [4]	450 A (37.5 A/phase)	294 W/in^3 (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [1]	40 A (20 A/phase)	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%* Full-load efficiency: 92.7%*	N/A N/A
2020	Sigma [19]	80 A	420 W/in^3 (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

† The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.
‡ Gate drive loss is included in the calculation of system efficiency. *According to direct correspondence with the author.

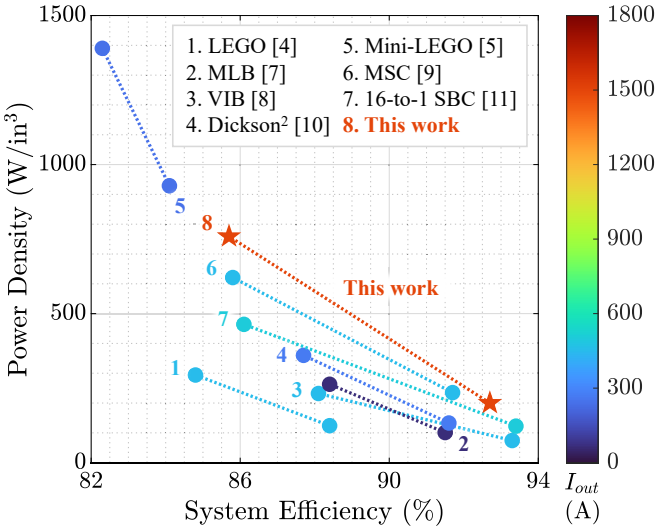

Fig. 11: Performance comparison between this work and the state-of-the-art 48-V-to-1-V works.

V. Conclusion

This paper presents a switching bus converter for next-generation ultra-high-power microprocessors (e.g., GPUs, CPUs, ASICs, etc.) with single-stage 48-V-to-1-V vertical power delivery. In the proposed topology, two 2-to-1 SC front-ends are merged with four 10-branch SCB modules through four switching buses, achieving a very large SC stage conversion ratio of 20-to-1. Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. With a topological comparison using the normalized switch stress and the normalized passive component volume as two metrics, this paper demonstrates that the proposed topology shows great potential for both higher efficiency and higher power density than prior solutions. To validate the functionality and performance of the proposed switching bus converter, a hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards. It was tested up to 1500-A output current and achieved 92.7% peak system efficiency, 85.7% full-load efficiency (including gate drive loss), and 759 W/in^3 power density (by box volume), pushing the performance limit of the state-of-the-art 48-V-to-1-V works in previous literature.

VI. Acknowledgements

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