UNIVERSITY OF CALIFORNIA
SANTA CRUZ

ISOLATED MVDC POWER CONVERTERS USING WIDE BANDGAP TECHNOLOGY

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL AND COMPUTER ENGINEERING

by

Amin Ashraf Gandomi

June 2024

The Dissertation of Amin Ashraf Gandomi
is approved:

_____
Professor Leila Parsa, Chair

_____
Professor Keith Corzine

_____
Professor Yu Zhang

_____
Peter F. Biehl
Vice Provost and Dean of Graduate Studies

Table of Contents

List of Figures

List of Tables

Abstract

Isolated Mvdc Power Converters Using Wide Bandgap Technology

by

Amin Ashraf Gandomi

In this thesis, bidirectional isolated dc–dc converters are analyzed for MVDC applications. Medium voltage dc (MVDC) is an attractive architecture for some power systems including all-electric ship systems based on numerous advantages including increased efficiency and reduced cost. The US Navy is investing in MVDC technology for future shipboard power systems. In this dissertation, an active 5-level T-type converter is used on the primary and secondary sides of a high-frequency transformer. The modified T-type converter features higher efficiency, fault tolerant capability, and smaller filter size compared to the common dual-active bridge dc–dc converters. The operation of the proposed converter is optimized based on minimizing power losses. For the optimization, the transformer core loss, reactive power, and rms current are considered. Wide bandgap devices are used for the minimization of semiconductor switching losses. A control method based on the Fourier series and decomposition theorem is proposed. A fault-tolerant analysis is carried out for this converter and post-fault switching methods are proposed for each faulty condition. To reduce voltage overshoot, a laminated dc-link is designed, and

a two-level turn-off method is used for operating frequencies around 75 kHz. The steady state and dynamic operations of the proposed structure are verified through experiments. In addition, a neural network-based fault diagnostic model is developed. By applying feature selection methods, the model achieves an accuracy of over 95%. The developed model is implemented in real-time to detect and locate open-circuit failures of the switches. The detection duration for various types of single and double failures ranges from 10 to 60 cycles.

Acknowledgments

I would like to express my deepest gratitude to my beloved parents, Naser and Shamsi, for their unwavering love, encouragement, and prayers. Your steadfast support has given me the courage to overcome any challenges and difficulties. I am also profoundly thankful to my dearest brother, Yasser, my first and best mentor, who has always been there to assist me whenever I needed him. My heartfelt thanks go to my fiancé, Sama, for understanding the challenges I faced and helping me complete this journey.

I am immensely grateful to my research advisor, Dr. Leila Parsa, for selecting me for this work. Being part of her research team has been an invaluable learning experience, and I appreciate her patience and support throughout this project. I must acknowledge Dr. Keith Corzine for his assistance with every problem I encountered. His shared knowledge and experience have been incredibly instructive. I extend my thanks to Dr. Yu Zhang for his patience and guidance as a member of my dissertation reading committee.

Last but not least, I am very grateful to all my friends in Santa Cruz and Tabriz for helping me stay focused and providing much-needed relief when I needed it most.

Chapter 1

1 Introduction

1.1 Medium voltage direct current (MVDC) systems overview

Medium Voltage Direct Current (MVDC) systems represent a variant of electrical power transmission and distribution technology functioning within the medium voltage spectrum, typically spanning from 1kV to 150kV. Unlike traditional alternating current (AC) systems, MVDC systems utilize direct current (DC) for the transmission and distribution of electrical power. Operating within medium voltage levels, which bridge the gap between low voltage (LV) and high voltage (HV) systems, the specific voltage level varies according to the system's unique application and requirements. To ensure efficient power transmission and distribution, MVDC systems necessitate specialized cables and substations. For long-distance transmission, HVDC cables with insulation suitable for medium voltage levels are employed, while MVDC substations facilitate the connection and conversion of power between different voltage levels. Power electronic converters play a pivotal role in MVDC systems, enabling the conversion between AC and DC

voltage levels and regulating power flow within the system. These converters encompass various types, including ac-dc rectifiers for converting AC power into DC power, dc-ac inverters for converting DC power back into AC power, and dc-dc isolated or non-isolated converters for adjusting DC power levels. Additionally, MVDC systems leverage different converter technologies tailored to specific application requirements, such as line-commutated converters (LCCs) and voltage source converters (VSCs). LCCs, relying on thyristor-based technology, are prevalent in HVDC applications due to their high power handling capabilities, ideal for long-distance transmission. Conversely, VSCs, employing insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs), boast fast response times and precise voltage and frequency control, making them suitable for MVDC applications. These systems incorporate advanced protection and control mechanisms, including protective relays, circuit breakers, and monitoring devices, to ensure safe and reliable operation by detecting and addressing faults, overloads, and abnormal conditions within the system. [1]-[14].

MVDC systems present numerous advantages over conventional AC systems, encompassing heightened efficiency, particularly evident in long-distance transmission lines due to minimized losses, improved controllability, and stability which facilitate precise regulation of voltage and frequency, as well as space and cost savings achieved through the utilization of smaller conductors and reduced

insulation material. MVDC systems are applied across a broad spectrum of industries and sectors, serving various purposes, including: 1- Renewable energy integration: MVDC systems streamline the integration of renewable energy sources, such as solar and wind power, into the grid by facilitating the transmission and distribution of DC power; 2- Electric vehicle charging infrastructure: MVDC technology supports the establishment of rapid-charging stations for electric vehicles, thereby reducing charging durations and enabling bidirectional power flow for vehicle-to-grid (V2G) applications; 3- Data centers: MVDC architectures present energy-efficient solutions for power distribution in data centers, thereby enhancing power quality and diminishing distribution losses; 4- Marine and offshore applications: MVDC systems are employed in marine propulsion systems and offshore platforms to ensure efficient power transmission and distribution, particularly in environments where space is limited. MVDC power electronics play a pivotal role in modernizing naval and shipboard power systems, offering advantages such as [15], [16], [17] firstly, in terms of power conversion and distribution, MVDC power electronics play a pivotal role in naval applications by converting ac power generated by onboard generators or supplied from external sources into dc power for distribution throughout the vessel. This conversion process typically involves rectification using solid-state devices like diodes or thyristors to transform ac to dc. Secondly, regarding efficiency and the reduction of losses, MVDC power electronics offer superior efficiency compared to ac systems,

particularly over long transmission distances. By mitigating losses during power conversion and distribution, MVDC systems optimize energy utilization and minimize fuel consumption, resulting in cost savings and increased mission endurance for naval vessels. Thirdly, with respect to modular and scalable design, MVDC power electronics are crafted to be modular and scalable, enabling flexible integration and expansion of power generation, distribution, and consumption modules as operational requirements evolve. This modular design streamlines maintenance, troubleshooting, and upgrades, reducing downtime and enhancing system reliability and availability. Fourthly, concerning advanced control and protection, MVDC power electronics incorporate sophisticated control algorithms and protection schemes to ensure safe and reliable operation in challenging maritime environments. These control systems facilitate precise regulation of voltage and frequency, alongside supporting various operating modes such as grid-forming and grid-following operation. Additionally, advanced fault detection and isolation mechanisms help mitigate the impact of electrical faults and disturbances, ensuring continuous power supply to critical onboard systems and equipment. Fifthly, in terms of integration with energy storage systems, MVDC power electronics facilitate the integration of energy storage systems (ESS) such as batteries and supercapacitors to enhance system resilience and efficiency. Leveraging MVDC technology enables naval vessels to optimize the use of renewable energy sources, store excess energy during low-demand periods, and provide backup power during

emergencies or combat situations. Lastly, regarding the electrification of ship systems, MVDC power electronics enable the electrification of various ship systems including propulsion, auxiliary power, heating, ventilation, and air conditioning, and weapon systems. Electrifying onboard systems reduces reliance on mechanical and hydraulic systems, simplifies maintenance and logistics, and improves overall system efficiency and performance [15]-[17]. In addition, alignment with international standards: MVDC power electronics conform to established international standards and guidelines, guaranteeing interoperability and compatibility with systems and equipment from diverse manufacturers and vendors. Noteworthy standards like IEEE 2030.10 and IEC 80005 offer comprehensive directives for the design, implementation, and operation of MVDC systems in naval and shipboard applications. Emphasizing safety, reliability, and efficiency, these standards play a pivotal role in promoting uniformity and best practices within the industry.

The US Navy is investing in MVDC technology for future shipboard power systems [20], [21]. According to IEEE standard 1709, MVDC architectures for shipboard applications can improve reliability, survivability and power quality [22]. In these applications, efficiency, power density and safety are important factors [23], [24] that can be improved by specific power electronic topologies and devices. Galvanic isolation is important in these topologies to mitigate electromagnetic

compatibility concerns and transform from MVDC to lower voltage levels. MVDC systems in shipboard applications rely heavily on isolated dc-dc converters. These converters should have fault tolerant capability to enhance the system reliability and survivability. Figure 1.1 shows a general MVDC system in a shipboard zonal application. The isolated dc-dc converter stages should have bidirectional power flow capability.

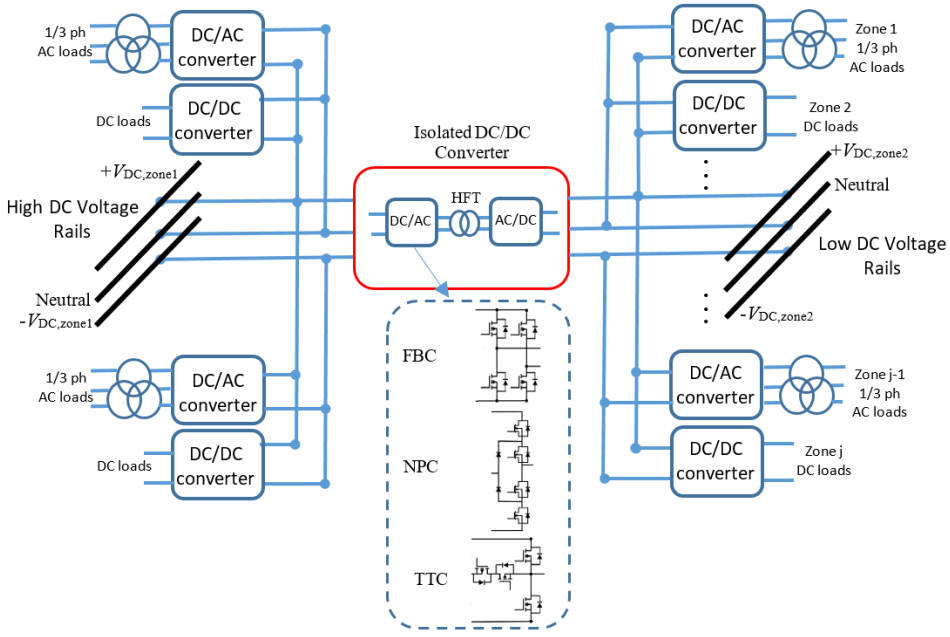


Figure 1.1 General MVDC system in shipboard zonal application.

1.2 Dc-dc converters overview in MVDC applications

Hereafter, dc-dc converters for medium voltage applications are going to be reviewed. There are two general categories for dc-dc converters including non-

isolated and isolated structures. In [25], a non-isolated non-coupled inductor modular structure for high voltage applications based on multi-input dc–dc converter is presented. The presented topology benefits from continuous input current. In [3] a bi-directional modular non-isolated dc–dc converter is presented. This structure consists of a boost converter fed from the high-voltage (HV) side. At the boost converter (BC) output stage, a certain number of half bridge submodules (HBSMs) are connected across the BC switch. In the non-isolated converters, there is no galvanic isolation between input and output and so these converters may have lower weight, volume and power loss due to absence of transformers, while may have problems of safety and fault tolerance.

In isolated dc-dc converters, high-frequency transformers provide galvanic isolation which can eliminate ground faults and circuitous currents. Due to the reduced component ratings and fault tolerant capabilities, modular structures are gaining popularity in high power medium voltage applications. Much research in the literature on isolated dc/dc converters relies on the dual-active bridge (DAB) structure. At the same time, modular multilevel converters (MMCs) have become significantly popular for medium-voltage applications in recent years. Also, there are some other different types of converters based on MMCs and DABs in the literature which have different properties in comparison to previous ones.

In [26], [27], single-phase half bridge-based isolated dc-dc converters are proposed for medium voltage applications. The presented converter in [27] used 15kV 10A SiC MOSFEETs in its structure. The switching frequency is 40 kHz with 2 μs deadtime. This structure is shown in Figure 1.2. The efficiency of this structure is 97% in this 6 kV prototype. Since this converter contains a single stage for 6 kV applications, the voltage ranges of the switches need to be compatible. In [26], the converter is based on two single phase half-bridge inverters in every side. By considering the power flow in both sides with a voltage-clamping circuit or extra switching devices and resonant components, unified zero-voltage switching was achieved. Also, a prototype of 1.6-kW has been tested under full power in this work.

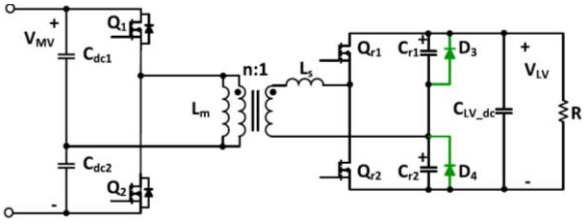


Figure 1.2 Presented structure in [27]

In [28], [29], a bidirectional dual-active bridge DC-DC converters based on full-bridge inverter are presented shown in Figure 1.3.

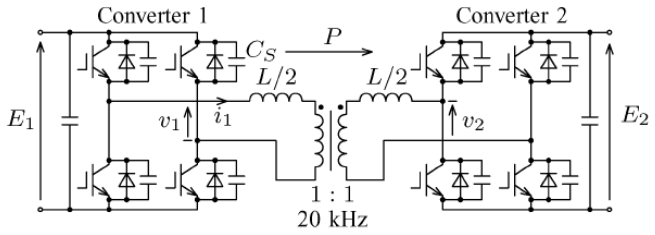


Figure 1.3 Presented structure in [28], [29]

This structure is a bidirectional isolated dc–dc converter including two single-phase full-bridge converters and a 20 kHz transformer for medium voltage applications. In this structure, power switching devices based on silicon carbide (SiC) and/or gallium nitride can be considered. In [28], a 350 V and 10 kW dc–dc converter is tested with the overall efficiency of input-output dc terminals as high as 97%. The common topology to use in each side of the isolated dc-dc converter is full-bridge converter (FBC). This topology has straightforward dc bus implementation and control method [30]. All power electronic switches in this topology should withstand the full dc-link voltage. This converter can produce a 3-level voltage at the primary and secondary sides of the high-frequency transformer with the maximum level of full dc-link voltage. In a single-phase dual-active bridge converter to balance losses of conduction, switching, and magnetic under light, medium, and heavy loading, a switching sequence is presented in [31]. Applying the switching sequence causes to improve overall efficiency in this structure by enabling

soft switching. Also, this method can adjust the frequency to match the minimum RMS transformer current in the full operating range.

Analytical analysis of the general multiphase isolated dc-dc topologies based on half/full bridge inverters is done in [32]. This structure is shown in Figure 1.4. The multiphase single active bridge, dual-active bridge and series resonant converters have been analyzed in this paper. Three-phase structures have been resulted as an interesting option in comparison to all the analyzed topologies regarding the number of phases for high power applications.

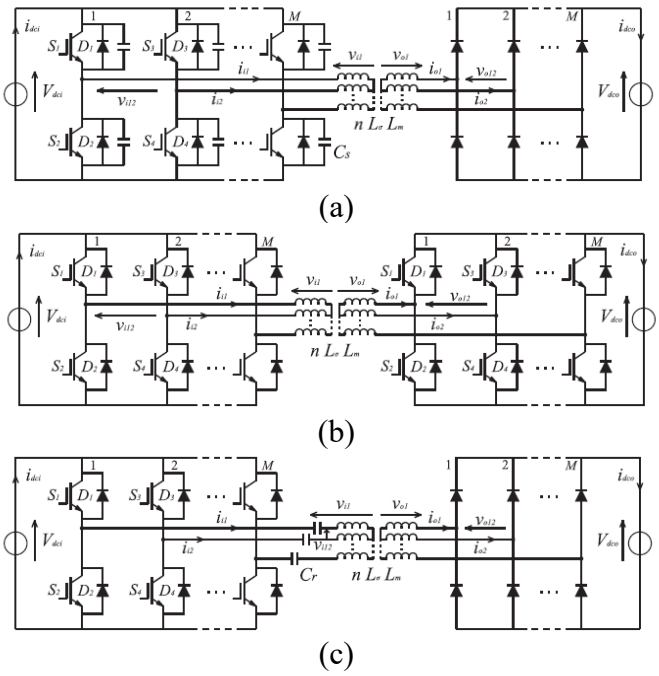


Figure 1.4 Presented structure in [32]

In [33], a multi winding high-frequency transformer for modular cascaded multilevel converter based on full-bridge inverter is presented for medium and high voltage applications. Cascaded full-bridge inverters are used on both sides of the transformer. In this structure that shown in Figure 1.5, by using the multi winding transformer, voltage stress on the power electronic devises is decreased.

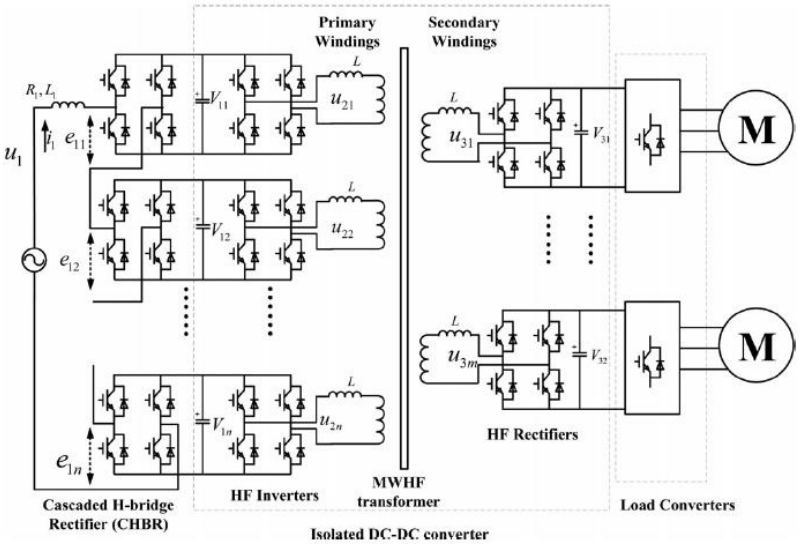


Figure 1.5 Presented structure in [33]

Figure 1.6 shows the input-series output-parallel high-frequency isolated bidirectional DC-DC converter based on dual-active bridge inverter that is presented in [34].

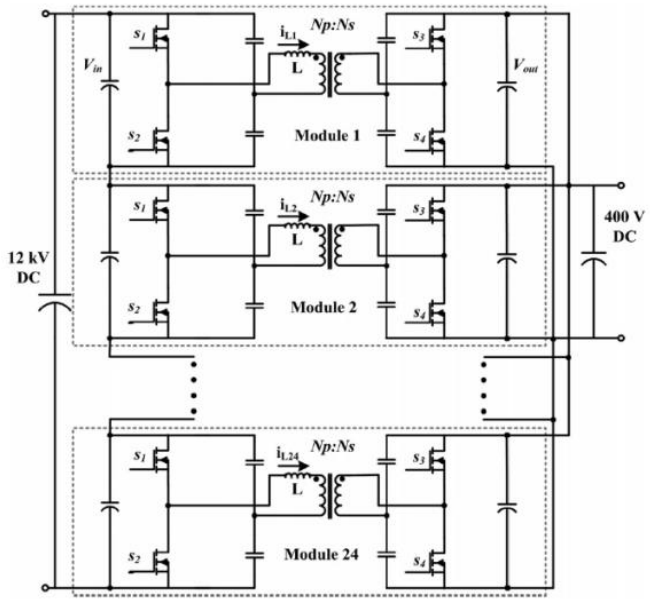


Figure 1.6 Presented modular converter in [34].

This paper presents the structure of isolated bidirectional dc-dc converter based on dual-active half-bridge inverter connected in series-input paralleled-output for 20 kVA-solid state transformer. It is possible to use low-voltage metal-oxide-semiconductor field-effect transistors (MOSFETs) with low on-state resistance in this structure that resulted conduction losses. The merits of this structure are bidirectional power flow, having high-frequency galvanic isolation, zero voltage switching (ZVS) capability of all switching devices, and low switching losses even with high-frequency operation. In this paper, 1kW converter modules with 50 kHz switching are presented as experimental setup.

Other options for the converter stages in isolated dc-dc converters include 3-level topologies such as the neutral point clamped converter (NPC) and T-type

converter (TTC) shown in Figure 1.1. In [35], authors presented a three-phase DAB converter based on the diode-clamped converter which uses 10 kV SiC MOSFETs. The efficiency of this structure, consisting of lower voltage 1.2 kV SiC MOSFETs, is near 98.33%. A dual-active structure based on neutral point clamped inverter shown in Figure 1.7, is presented in [36]. 15-kV SiC insulated-gate bipolar transistors are used in this structure. In the left side of the transformer, three phase neutral point clamped inverter is used, while in the right side, three leg half bridge inverters are utilized.

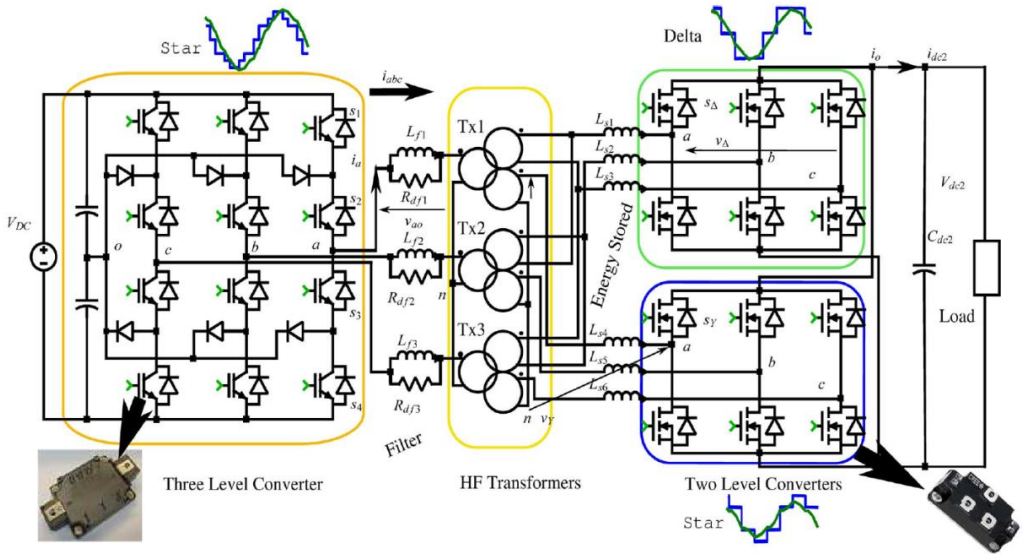


Figure 1.7 Presented three phase DAB structure in [36].

In [35] and [37], isolated dc-dc converters based on the NPC and TTC have been presented. The voltage stress on the switches in the NPC is half of the full dc-link voltage. In the TTC, voltage stress on the switches in main leg is equal to full

dc-link, while a middle bidirectional switch has voltage stress of half of the dc-link voltage. The NPC and TTC in Figure 1.1 are half-bridge structures. Therefore, these converters could not utilize the full dc-link voltage. In addition, the implementation of the dc-link in the NPCs and TTCs are slightly more difficult than the FBCs [38]. The TTCs are becoming popular in applications that require high reliability due to their improved performance and fault-tolerant capabilities [39], [40], [41]. Also, they have some other advantages including better electromagnetic compatibility (EMC) and high efficiency [42], [43].

An isolated dc-dc modular multilevel converter (MMC) is shown in Figure 1.8 [44]. The control method to balance of the internal power storage components in this topology is complicated. A MMC based structure is presented in [5] which uses a lower number of switches for producing a set number of output voltage levels. The [45] presents the control of isolated dc–dc modular multilevel converter. To obtain the steady-state and small-signal models, the fundamental period averaging method is applied. It is shown that the presented method can preserve the information of model about the MMC structure.

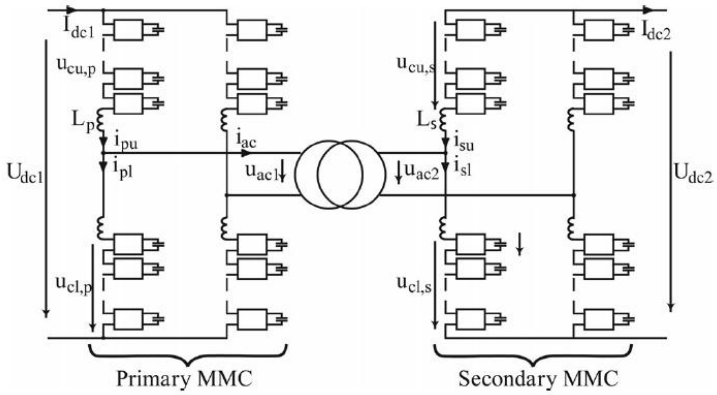


Figure 1.8 Presented structure in [44]

An isolated dc-dc dual-active modular multilevel converter for MV application is investigated in [46]. This converter has several characteristics including soft switching, small passive components and breaker-less MVDC system. A lab scaled 40kHz, 3kW prototype was built in this work. In MMCs, different types of control methods are presented to produce desired output voltage and regulate the voltage of the capacitors. The control methods used mostly in MMCs are phase shifted pulse width modulation (PSPWM) and phase disposition PWM (PDPWM).

The paper in [47] presents a hybrid isolated dual-active dc–dc converter that is shown in Figure 1.9. In this structure, three leg half bridge inverter is combined with modular multilevel converter that has bidirectional and soft switching capability. In this paper, a 50 kV/400 kV, 400 MW converter is simulated to evaluate semiconductor losses.

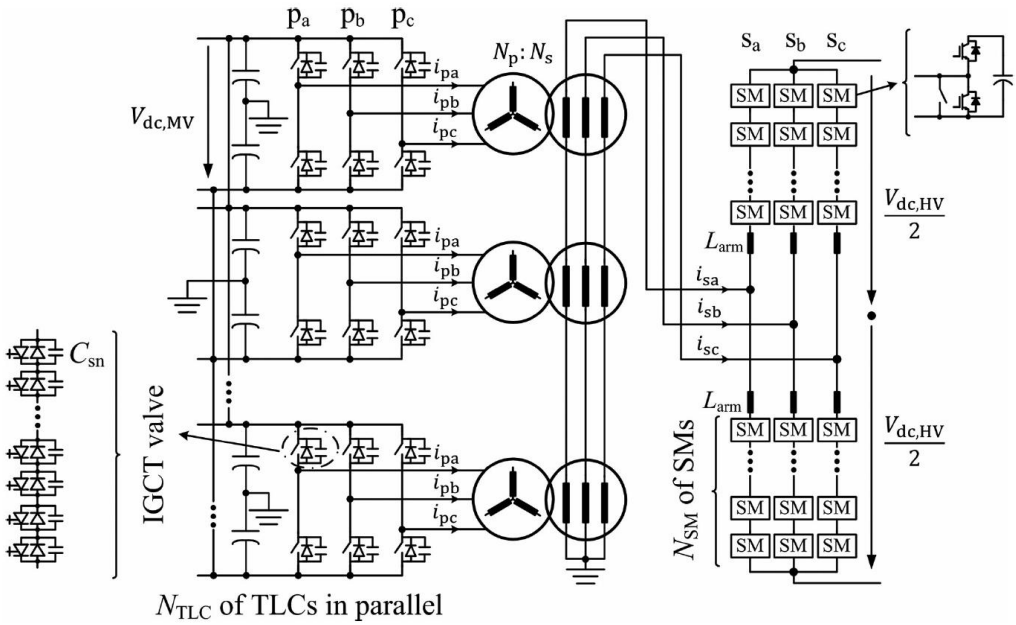


Figure 1.9 Presented structure in [47]

The [48] presents a hybrid isolated dc-dc modular multilevel converter based on resonant mode for medium voltage applications. Figure 1.10 shows the structure of the presented converter. Two other topologies based on main structure are presented for balancing the voltage and current between the blocks. The voltage balancing of the capacitors complicates the control method in this structure.

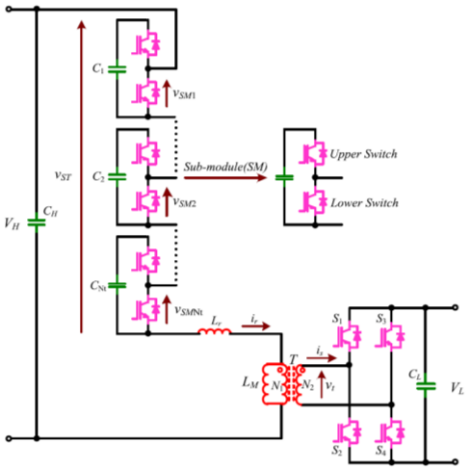


Figure 1.10 Presented structure in [48].

A breaker-less shipboard medium-voltage dc (MVDC) system is gaining more attention recently due to its advantage in dealing with a dc fault by using switched-mode power modules and disconnectors. The most used structures in the medium voltage applications are dual-active bridge converters and modular multilevel converters that are shown in Figure 1.11 [49]. The structure shown in this figure is investigated from the viewpoint of fault management. In this paper, fault protection strategy of presented control algorithms have been developed.

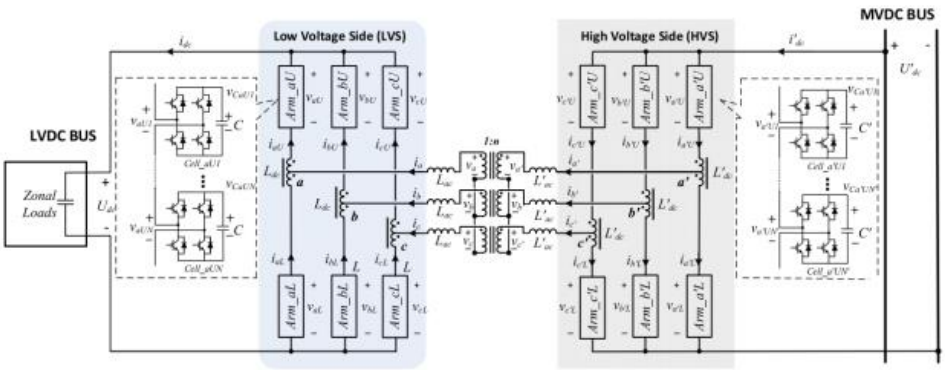


Figure 1.11 Hybrid modular multilevel converter in [49].

The application of the multilevel converters results in some unique features such as the operation in high power and medium-voltage ranges, the generation of the high-quality output voltage with low total harmonic distortion (THD) and lower static voltage on switches [50]. These superior properties have increased the application of multilevel converters in isolated dc-dc converters.

Chapter 2

2 Isolated T-type Dc-Dc Converter

In this chapter, several T-type based dc-dc converters are proposed. The proposed structures are investigated in detail as follows:

2.1 Single-phase T-type inverter

A single-phase T-type inverter is shown in Fig. 2.1. This inverter has some advantages of having higher efficiency and better EMI behavior in comparison to full-bridge and neutral point clamped inverters [7]. Therefore, it will be used as a main leg in the proposed converter.

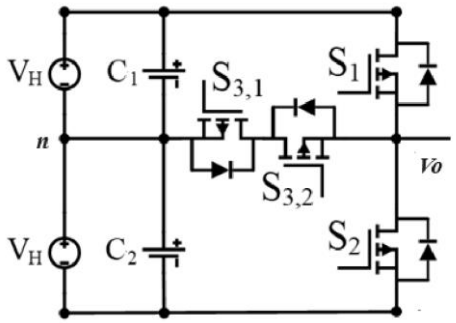


Figure 2.1 The single-phase T-type inverter.

This inverter can generate 3-level voltage with half of the dc-link in output in comparison to the neutral point of the dc-link. Table 2.1 shows the switching pattern for this inverter.

Table 2.1 Switching states in single-phase T-type inverter.

Output voltage level	**S_1**	**S_2**	**$S_{3,1}$**	**$S_{3,2}$**
V_H	1	0	0	1
0	0	0	1	1
$-V_H$	0	1	1	0

2.2 Single-phase modified T-type converter

In this section, a novel isolated dual-active dc-dc converter is proposed. The proposed structure is symmetrical. Each primary and secondary converter is a 5-level modified T-type converter. Using a 5-level converter on the higher voltage side helps to decrease the *dv/dt* of the switches. Also, it helps to improve the quality of voltages in the primary and secondary sides of transformer which leads to decrease the size of filters. Also, by having these voltages with lower amount of total harmonic distortion (THD), the better sinusoidal current can be achieved to pass through transformer. In addition, using T-type converter helps to have fault tolerance capability that helps to increase reliability of the system. Two primary and secondary converters are connected through a high-frequency transformer that provides

galvanic isolation. Power can transfer between these two converters by helping leakage inductances of the transformer. In this application, based on availability of neutral point of the dc-link as well as positive and negative rails in both primary and secondary sides, the balancing issues of dc-links capacitors no longer exist. The proposed dc-dc converter is shown in Figure 2.2.

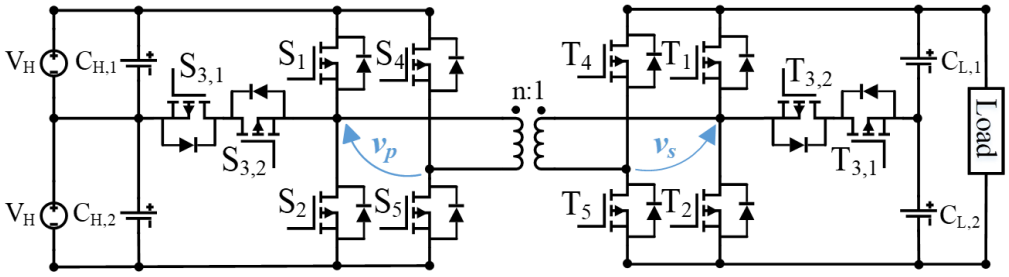


Figure 2.2 The proposed symmetrical 5-level dual-active dc-dc converter.

As seen in Figure 2.2, each primary and secondary converters comprises 3-level T-type and a half bridge module. By adding a half bridge module to the 3-level T-type converter, better dc-link utilization is achieved. This structure is completely symmetrical and bidirectional. In transferring power from the primary to secondary sides, the primary converter operates as a 5-level inverter and the secondary converter operates as a full bridge rectifier. In the reverse power transferring from the secondary to primary side, the secondary converter operates as a 5-level inverter and the primary converter operates as a full bridge rectifier. Therefore, based on the symmetrical operation of the proposed converter, it is only analyzed when the power is transferred from the primary side to the secondary side.

2.2.1 Modulation strategies

The switching pattern of the proposed converter to produce 5-level voltage at the primary side of transformer and 3-level at the secondary side of transformer is shown in Table 2.2. In the primary converter, first, by turning on switches S_1 and S_5, the primary converter produces voltage of $2V_H$ at the primary side of transformer. Second, switches $S_{3,1}$, $S_{3,2}$ and S_5 are on and the voltage at the primary side of transformer is V_H. Third, switches S_2 and S_5 are on, the primary voltage is zero. In the secondary converter, by turning on switches T_1 and T_5, the secondary converter produces voltage of V_o at the secondary side of transformer. It also produces zero voltage at the secondary side of transformer by using switches T_2 and T_5. The same pattern can be considered in the negative half cycle. Based on Table 2.2, there is a redundant switching states to generate zero voltage at primary and secondary sides that are useful for decreasing switching losses. Therefore, switches S_4 and S_5 operate at fundamental frequency, while S_1, S_2, $S_{3,1}$ and $S_{3,2}$ operate at switching frequency under healthy operation of the converter.

Table 2.2 The switching state of the proposed dc-dc converter.

Primary voltage	**Switches**												**Secondary voltage**
	Primary converter						**Secondary converter**						
	S_1	S_2	$S_{3,1}$	$S_{3,2}$	S_4	S_5	T_1	T_2	$T_{3,1}$	$T_{3,2}$	T_4	T_5	
$2V_H$	1	0	0	1	0	1	-	-	-	-	-	-	-
V_H	0	0	1	1	0	1	1	0	-	-	0	1	V_o
0	0	1	1	0	0	1	0	1	-	-	0	1	0
	1	0	0	1	1	0	1	0	-	-	1	0	
$-V_H$	0	0	1	1	1	0	0	1	-	-	1	0	$-V_o$
$-2V_H$	0	1	1	0	1	0	-	-	-	-	-	-	-

In this work, different modulation methods are analyzed for the proposed dc-dc converter that are described in detail as follows:

2.2.1.1 PWM modulation method

In this method, phase disposition pulse width modulation (PDPWM) is applied for primary converter and sine PWM (SPWM) is applied for the secondary converter. It is supposed that the load voltage is constant. The carriers and the reference waveforms in the normal operation of the proposed converter are shown in Figure 2.3. For the primary converter, there are two carriers with the same frequency and same phase (C_1 and C_2) where C_1 is from 0.5 to 1, while C_2 is from 0 to 0.5. Also, there is a level-shifted sinusoidal reference R_H. When the R_H is larger than C_1, S_1 is on and when the R_H is larger than C_2, $S_{3,2}$ is on. Switches $S_{3,1}$ and S_2 operate in complementary of S_1 and $S_{3,2}$, respectively. Also, switch S_4 is on in the

negative half cycle, while switch S_5 operates in the positive half cycle. For the secondary converter, there is a carrier C_3 with the amplitude of -1 to 1. Also, there are two sinusoidal references $R_{L,1}$ and $R_{L,2}$ with the same amplitude and same frequency for each legs of (T_1,T_2) and (T_4,T_5) respectively, where $R_{L,2}$ is 180 degree phase-shifted with respect to $R_{L,1}$. When $R_{L,1}$ is larger than C_3, T_1 is on and when $R_{L,2}$ is larger than C_3, T_4 is on. Switches T_2 and T_5 operate in complementary of T_1 and T_4, respectively. Also switches $T_{3,1}$ and $T_{3,2}$ are off in the normal operation of converter that transfers power from primary side to secondary side.

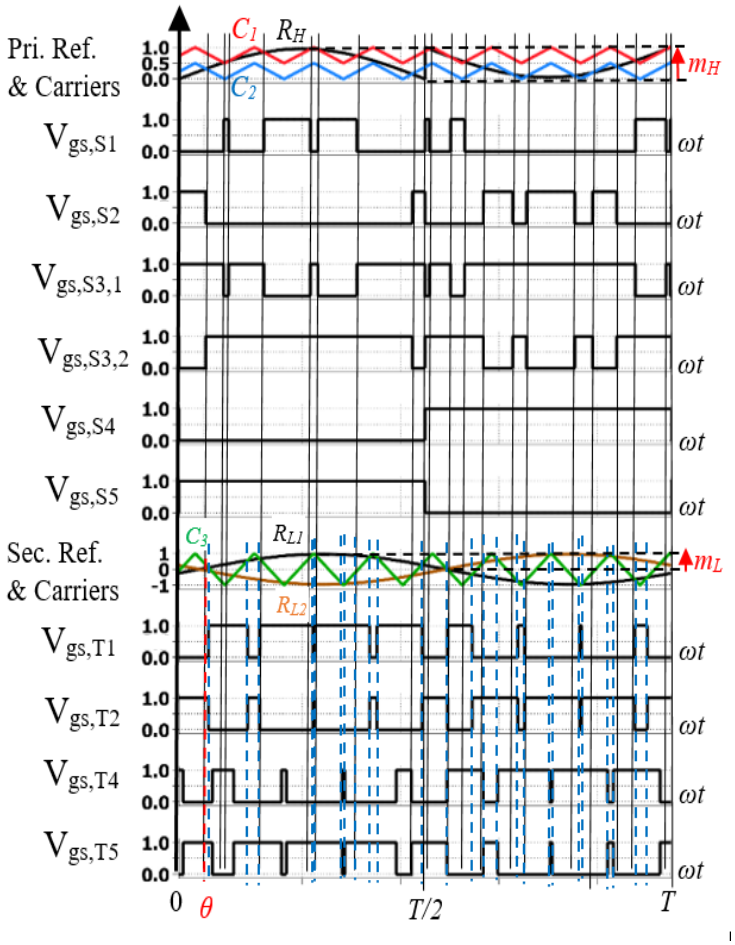


Figure 2.3 The PWM modulation method in the proposed dc-dc converter.

The control analysis of the converter using PWM method for both primary and secondary converters is described as follows:

The equivalent circuit of an isolated dc-dc converter can be considered as Figure 2.4. It is worth noticing that a simple equivalent model for transformer is supposed. In this figure, v_p, v_s' and L_s are the primary voltage, secondary voltage

reflected to the primary side and equivalent inductance between two primary and secondary converters including leakage inductances of the transformer.

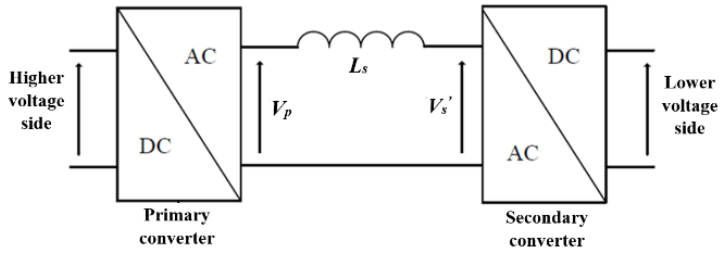


Figure 2.4 The equivalent circuit of DAB converter.

The fundamental value of primary voltage (v_p) and secondary voltage reflected to primary side (v_s') are calculated as follows.

$$v_p(t) = 2m_H V_H \sin(\omega t) \tag{2-1}$$

$$v_s'(t) = nm_L V_o \sin(\omega t - \theta) \tag{2-2}$$

where, V_H, V_o, θ and n are each higher dc-links, regulated output voltage, phase shift between the reference waveform of first leg of secondary side (R_{L1}) and reference waveform of primary side (R_H) and turn ratio of transformer, respectively. The current passes through transformer from primary to secondary is calculated as bellow.

$$i(t) - i(0) = \int_0^t \frac{v_p(t) - v_s'(t)}{L} dt \tag{2-3}$$

By considering symmetry of converter operation in one switching cycle and the average current of the equivalent inductor over one switching period should be zero in steady state, (2-4) is resulted.

$$i\left(\frac{\pi}{\omega}\right) = -i(0) \tag{2-4}$$

where ω is angular frequency equal to $2\pi f_c$. Here, f_c is base frequency. Therefore, current can be derived as follows:

$$i_1(t) = A\sin(\omega t + \lambda_1) \tag{2-5}$$

$$\begin{cases} A = \sqrt{(\frac{2V_H m_H}{n})^2 + (\frac{V_o m_L}{2})^2 + \frac{2V_H m_H V_o m_L}{n}\cos(\theta)} \\ \lambda = \tan^{-1}\frac{\frac{2V_H m_H}{n} + \frac{V_o m_L}{2}\cos(\theta)}{\frac{V_o m_L}{2}\sin(\theta)} \end{cases} \tag{2-6}$$

The average power during one switching period transfers from primary side to secondary side, can be considered as follow:

$$P = \frac{1}{T}\int_0^T v_p(t) i(t) dt \tag{2-7}$$

where $T = \frac{1}{f_c}$ is one fundamental period. Therefore, power is resulted as follows.

$$P = m_H V_H \cos(\lambda) \sqrt{(\frac{2V_H m_H}{n})^2 + (\frac{V_o m_L}{2})^2 + \frac{2V_H m_H V_o m_L}{n} \cos(\theta)} \quad (2\text{-}8)$$

Therefore, the control parameters are modulation index of primary reference (m_H), modulation index of secondary references (m_L) and phase shift of R_H and R_{L1} (θ).

Therefore, the modulation indices m_H and m_L as well as angles θ are controlled such that minimum amount of total harmonic distortions (THD) are obtained in the generated 5-level voltage at the primary side of transformer, 3-level voltage of secondary side of transformer as well as producing desired output voltage and maximizing the amount of transferred power.

2.2.1.2 Phase-shifted modulation method

In this method, quad phase-shifted modulation is applied to the proposed converter. The primary voltage is 5-level voltage and the secondary voltage is 3-level voltage. The load voltage is supposed to be constant in this analysis. Also, it is supposed to have symmetrical voltages at the primary and secondary sides of transformer. Therefore, there are two rising edges at the primary and one rising edge at the secondary voltages. Moreover, fundamental voltages of the primary and secondary voltages have θ degree phase shift regarding to each other. Then, there

are four degrees of freedom in this method. Figure 2.5 shows the primary voltage and secondary voltage reflected to the primary, primary current and pulses of the switches in this method. Based on this figure, the angles α_1 and α_2 which are related to the primary voltage, are controlled such that minimum amount of total harmonic distortion (THD) is obtained in the generated 5-level voltage at the primary side of transformer. To obtain the lower amount of THD in primary current of transformer, the rising edge of the secondary converter (α_3) is calculated. Also, θ is calculated based on the amount of transferring power.

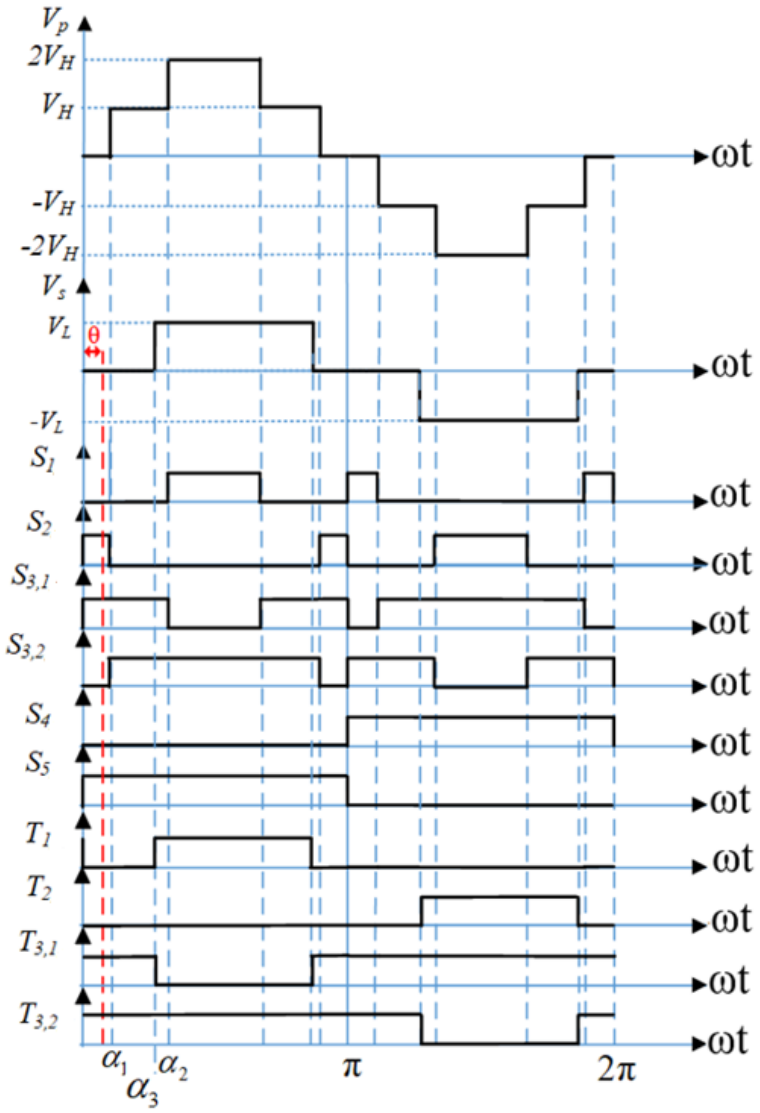


Figure 2.5 The phase-shifted modulation method in the proposed dc-dc converter.

The control goals are setting output dc voltage at the desired value as well as minimizing the total harmonic distortion (THD) of the primary voltage of the transformer. Two control parameters are the angles α_1 and α_2 of the primary voltage. The Fourier series of the primary voltage waveform can be written as (2-9).

$$V_p(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_H}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2))\sin(n\omega t) \tag{2-9}$$

The fundamental and harmonics of voltage can be written as (2-10) and (2-11), respectively.

$$V_{p,1}(\omega t) = \frac{4V_H}{\pi}(\cos(\alpha_1) + \cos(\alpha_2))\sin(\omega t) \tag{2-10}$$

$$V_p(\omega t) - V_{p,1}(\omega t) = \sum_{n=3,5,7,\dots}^{\infty} \frac{4V_H}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2))\sin(n\omega t) \tag{2-11}$$

Therefore, the THD of the primary voltage is calculated as follows:

$$THD_{V_P} = \frac{\sqrt{\sum_{n=3,5,7,\dots}^{\infty} (\frac{1}{n}(\cos(n\alpha_1) + \cos(n\alpha_2)))^2}}{\cos(\alpha_1) + \cos(\alpha_2)} \tag{2-12}$$

The angles α_1 and α_2 are controlled such that minimum amount of THD is obtained in the generated 5-level voltage at the primary side of the transformer. The fundamental component voltage of secondary three-level voltage reflected to the primary side is calculated as follows:

$$V_{s,1}'(\omega t) = \frac{4nV_L}{\pi}\cos(\alpha_3)\sin(wt) \tag{2-13}$$

For optimal performance of the dc-dc converter, the fundamental values of primary and reflected secondary voltages should be the same, therefore the angle α_3 is calculated from (2-14).

$$\alpha_3 = \cos^{-1}\left(\frac{V_H}{nV_L^*}(\cos(\alpha_1) + \cos(\alpha_2))\right) \tag{2-14}$$

Where, V_L^* is the desired output voltage. θ is controlled based on desired active power that needs to transfer from primary to secondary sides calculated from (2-15).

$$P_o = \frac{V_H^2}{2\pi^2 f_s L_s}|\theta|(\pi - \theta) \tag{2-15}$$

where, P_o, f_s and L_s are the output power, fundamental frequency, and equivalent inductance between primary and secondary side converters.

2.2.1.3 Hybrid modulation method

In this method, PDPWM is applied to the primary converter and dual phase-shifted modulation is applied to the secondary converter that is shown in Figure 2.6. For the primary converter, there are two carriers with the same frequency and same phase (C_1 and C_2) where C_1 is from 0.5 to 1, while C_2 is from 0 to 0.5. Also, there is a level-shifted sinusoidal reference R_H. When the R_H is larger than C_1, S_1 is on and when the R_H is larger than C_2, $S_{3,2}$ is on. Switches $S_{3,1}$ and S_2 operate in

complementary of S_1 and $S_{3,2}$, respectively. Also switch S_4 is on in the negative half cycle, while switch S_5 operates in the positive half cycle. Dual phase-shifted modulation control method is applied to the secondary converter and this converter operates as a controlled full-bridge rectifier. In other words, square-wave control method with the 50% duty cycle is applied for secondary converter. The rising edge of the first leg includes T_1 and T_2 has $\theta - \frac{\alpha}{2}$ degree phase shift regarding to R_H. The switches T_4 and T_5 in the second leg operate in the complementary of T_1 and T_2, with the phase shift of α, respectively. Therefore, the control parameters in this method are modulation index (m), phase shift of primary and secondary fundamental voltages (θ) and phase shift between the two legs of secondary converter (α).

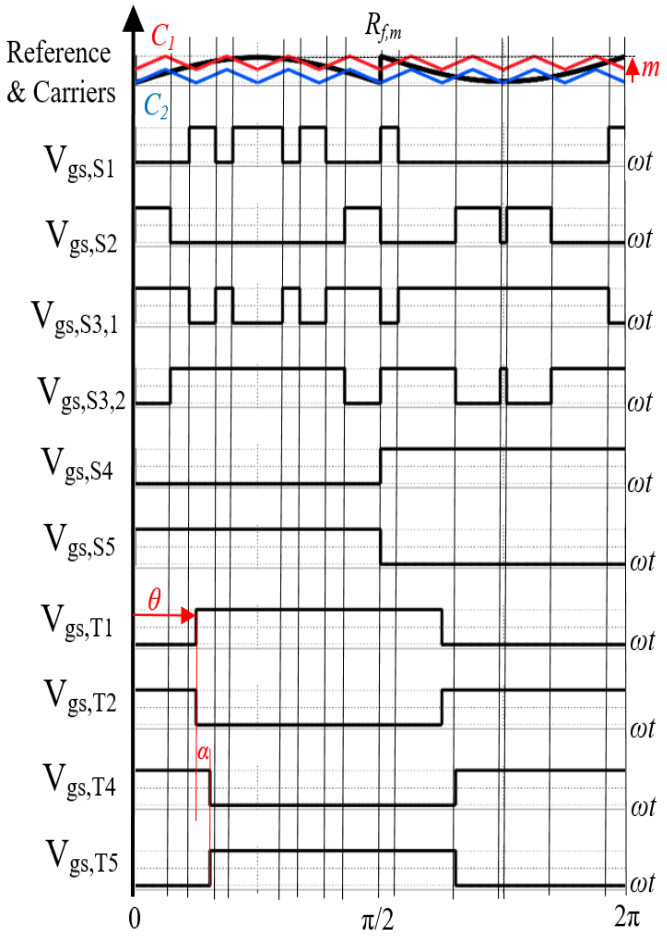


Figure 2.6 The hybrid modulation method in the proposed dc-dc converter.

Based on Figure 2.6, the peak values of primary voltage (V_p) and secondary voltage referred to the primary side (V_s') are calculated as (2-16) and (2-17), respectively.

$$V_p = 2mV_H \tag{2-16}$$

$$V_s' = \frac{4nV_o^*}{\pi}\cos(\alpha) \tag{2-17}$$

where V_H, V_o^* and n are the upper (lower) dc-link voltage, load desired voltage and turns ratio of the transformer. In this analysis, it is supposed that the load voltage is constant. The active and reactive powers transfer from primary converter to secondary converter are calculated as follows:

$$P = \frac{V_p V_s'}{2\pi f_c L_s} \sin(\theta) \tag{2-18}$$

$$Q = \frac{V_p V_s'}{2\pi f_c L_s} \cos(\theta) - \frac{V_p^2}{2\pi f_c L_s} \tag{2-19}$$

where f_c and L_s are the fundamental frequency and equivalent series inductances between both converters, respectively. The goal of the control method is maximizing the active power as well as minimizing the absolute value of reactive power. Therefore, the cost function can be considered as follows:

$$P = \frac{V_p V_s'}{2\pi f_c L_s} \sin(\theta) \tag{2-20}$$

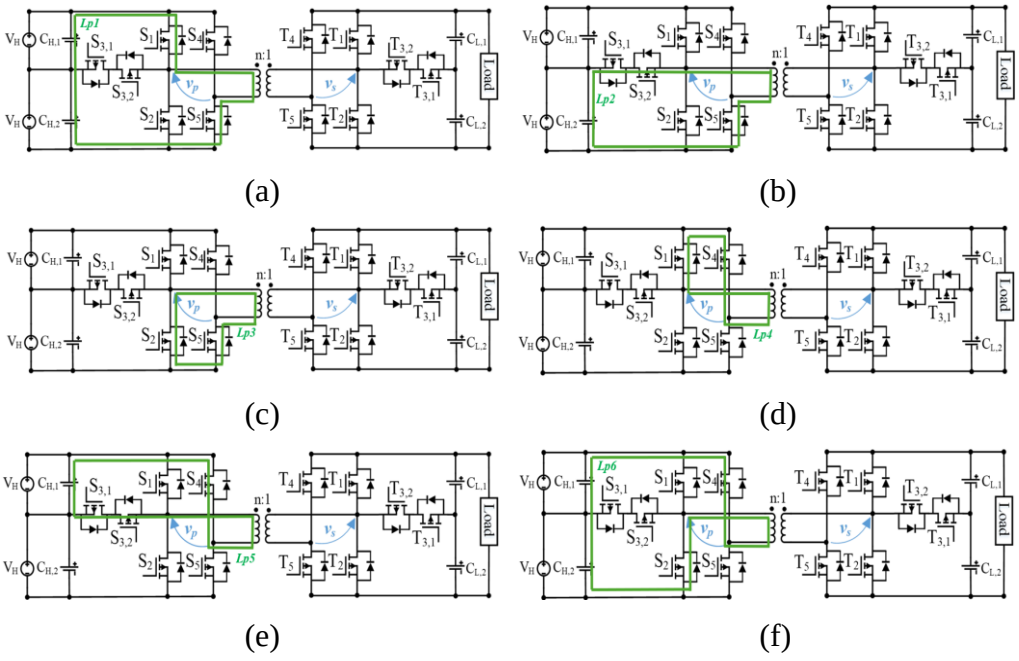
Therefore:

$$\text{Min} \left(\left|\frac{4mnV_H V_o^* \cos(\alpha)}{\pi^2 f_c L_T}\cos(\theta) - \frac{2m^2 V_H^2}{\pi f_c L_T}\right| - \frac{4mnV_H V_o^* \cos(\alpha)}{\pi^2 f_c L_T}\sin(\theta)\right) \quad (2\text{-}21)$$

$$S.to \begin{cases} 0 < m < 1 \\ 0 < \alpha < \frac{\pi}{2} \\ 0 < \theta < \frac{\pi}{2} \end{cases}$$

2.2.2 Proposed control method

The proposed 5-level modified T-type converter with available operating scenarios is shown in Figure 2.7.



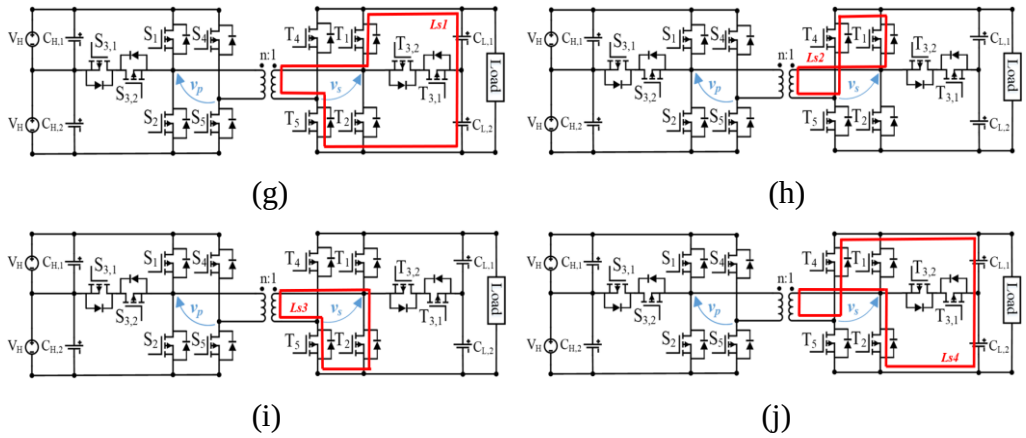


Figure 2.7 Proposed converter with different operating scenarios.

In the normal operation (mode 1) when the power transfers from primary to secondary side, the primary converter produces 5-level voltage by using six different switching states, while the secondary converter produces 3-level voltage by using four different switching states. By turning on switches S_1 and S_5, the primary converter produces voltage of $2V_H$ at the primary side of the transformer (L_{p1}). Next, switches $S_{3,1}$, $S_{3,2}$ and S_5 are on and the voltage at the primary side of transformer is V_H (L_{p2}). When switches S_2 and S_5 are on, the produced voltage is zero (L_{p3}). A similar pattern is considered in the negative half cycle (L_{p4}- L_{p6}). A redundant switching state to generate zero voltage is useful for decreasing switching loss. Therefore, the primary voltage can generate 5-level voltage of $+2V_H$, $+V_H$, 0, $-V_H$ and $-2V_H$ at the output. In the secondary converter, by turning on switches T_1 and T_5, the voltage of V_o is produced at the secondary side of the transformer (L_{s1}). When switches T_1 and T_4 are on, the produced voltage is zero (L_{s2}). A similar pattern is considered in the negative half cycle (L_{s3}- L_{s4}). In normal operation, the switches

(S_1, $S_{3,1}$), (S_2, $S_{3,2}$), (S_4, S_5), (T_1, T_2) and (T_4, T_5) have complementary operations. The switching concept in normal operation is shown in Figure 2.8. The waveforms in this figure from top to bottom are the sawtooth carrier and control signals, the primary voltage of the transformer (v_p), secondary voltage of the transformer (v_s) and pulses of the switches (S_1, $S_{3,1}$), (S_2, $S_{3,2}$), (S_4, S_5), (T_1, T_2) and (T_4, T_5). Also, α_1- α_8 are the edges of the primary voltage, β_1- β_4 are the edges of the secondary voltage and θ is the phase shift of secondary voltage. To avoid having even harmonics and dc values in the primary and secondary voltages, the angles in Figure 2.8 should be calculated as follows:

$$\alpha_5 = \pi + \alpha_1;\ \alpha_6 = \pi + \alpha_2;\ \alpha_7 = \pi + \alpha_3; \alpha_8 = \pi + \alpha_4 \tag{2-22}$$

$$\beta_3 = \pi + \beta_1;\ \beta_4 = \beta_2 - \pi \tag{2-23}$$

In Figure 2.8, D is the amplitude of the carrier and d_1- d_6 are the control signals to produce the pulses of switches and can be obtained as:

$$\begin{aligned} &d_1 = \alpha_1 \frac{D}{2\pi};\ d_2 = (\beta_1 + \theta)\frac{D}{2\pi};\ d_3 = \alpha_2 \frac{D}{2\pi}; \\ &d_4 = \alpha_3 \frac{D}{2\pi};\ d_5 = \alpha_4 \frac{D}{2\pi};\ d_6 = (\beta_2 + \theta)\frac{D}{2\pi} \end{aligned} \tag{2-24}$$

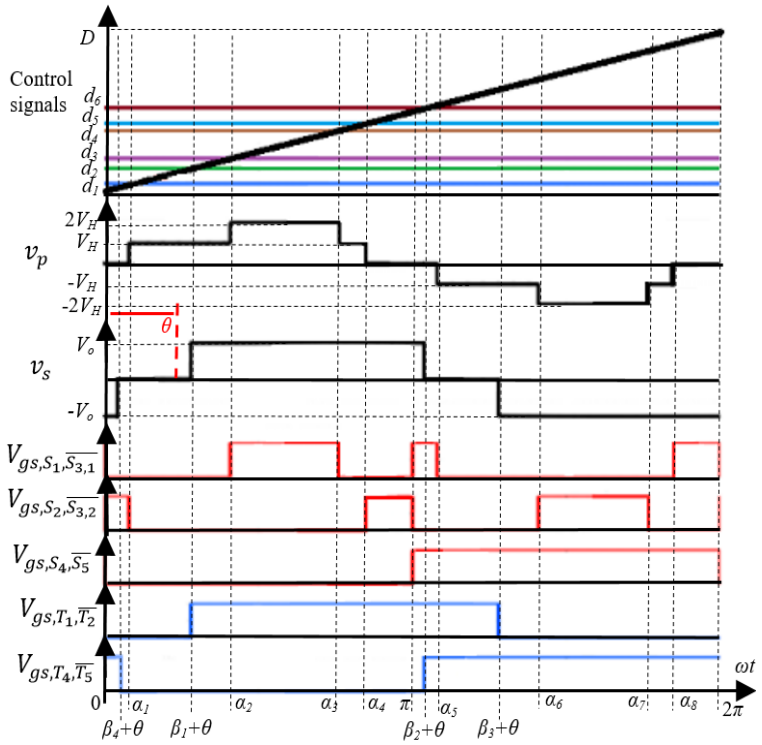


Figure 2.8 The switching strategy of the proposed converter in healthy condition.

2.2.2.1 Fundamental analysis

In the normal operation, the fundamental value of periodic square voltages of primary and secondary sides of transformer are calculated as follows:

$$v_p(\omega t) = \frac{2V_H \sin(\omega t)}{\pi}(\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3) - \cos(\alpha_4)) \quad (2\text{-}25)$$

$$v_s'(\omega t) = \frac{2nV_o \sin(\omega t - \theta)}{\pi}(\cos(\beta_1) - \cos(\beta_2)) \quad (2\text{-}26)$$

$$\omega = 2\pi f_c \quad (2\text{-}27)$$

where, v_p and v_s' are the primary square voltage and secondary square voltage referred to the primary side, respectively. Also, V_H, V_o, n, ω and f_c are half of the total dc-link, regulated output voltage, turn ratio of transformer, angular frequency and fundamental frequency, respectively.

Generally, the primary current flowing from primary to secondary sides is calculated as follows:

$$i(\omega t) - i(0) = \int_0^{\omega t} \frac{v_p(\omega t) - v_s'(\omega t)}{\omega L_s} d\omega t \quad (2\text{-}28)$$

where L_s is the leakage inductances of the transformer. Based on this fact that average current of the inductor should be zero in one fundamental period (T), then:

$$i(\pi) = -i(0) \quad (2\text{-}29)$$

The average amount of the active power transferred from the primary to secondary in one fundamental period of T is calculated as follows.

$$P_{avg} = \frac{1}{2\pi}\int_0^{2\pi} v_p(\omega t) i(\omega t)\, d\omega t \tag{2-30}$$

Therefore, the resulting transformer current and the transferred active and reactive powers in normal condition are resulted as follows.

$$\begin{aligned} i(\omega t) = \frac{2}{\omega \pi L_s}\big(& nV_o \cos(\omega t - \theta)(\cos(\beta_1) - \cos(\beta_2)) \\ & - V_H \cos(\omega t)(\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3) \\ & - \cos(\alpha_4))\big) \end{aligned} \tag{2-31}$$

$$P = \frac{4nV_H V_o(\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3) - \cos(\alpha_4))(\cos(\beta_1) - \cos(\beta_2))}{\omega \pi^2 L_s}\sin(\theta) \tag{2-32}$$

$$Q = \frac{4nV_H V_o(\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3) - \cos(\alpha_4))(\cos(\beta_1) - \cos(\beta_2))}{\omega \pi^2 L_s}\cos(\theta) - \frac{4(V_H(\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3) - \cos(\alpha_4)))^2}{\omega \pi^2 L_s} \tag{2-33}$$

For obtaining the higher efficiency, the losses of the converter should be minimized. The losses in an isolated dc-dc converter include switching and conduction losses of the switches in the primary side, core and winding losses of the transformer and switching and conduction losses of the switches in the secondary side. The Steinmetz equation is used to calculate the time-average core loss of the

transformer per unit volume (P_c) as follows [32]. Here, B_{ac} is the peak flux amplitude.

$$P_c = \sum_{x=1}^{\infty} K.f_c^{\alpha}.B_{ac}V_p^{\beta} \tag{2-34}$$

K, α and β are the material parameters obtained from manufacture's datasheet or curve fitting ($\alpha, \beta > 1$). In high-frequency operation, the core losses will be higher. Therefore, by decreasing the values of harmonics in primary voltage of the transformer, the core loss is decreased.

The winding loss of the transformer (P_w) and conduction loss of the MOSFETs (P_{MOS}) and diodes (P_{Diode}) can be calculated as follows:

$$P_w = (R_{w1} + R_{w2}.n^2).i_{rms}^2 \tag{2-35}$$

$$P_{MOS} = R_{DS_{ON}}.i_{DS}^2 \tag{2-36}$$

$$P_{Diode} = R_F.i_F^2 \tag{2-37}$$

where, R_{w1}, R_{w2}, R_{DS_ON} and R_F are the primary winding resistance, the secondary winding resistance, the resistance of MOSFET when it is conducting and the resistance of diode when it enters conduction mode. Also, i_{rms}, i_{DS} and i_F are the

root mean square (RMS) current of primary winding, each MOSFET and each diode. Since i_{DS} and i_F are directly related to i_{rms}, by decreasing the RMS values of transformer current, the winding and conduction losses are decreased. Therefore, the weighted cost function to calculate the control parameters to have higher efficiency is considered as (2-38).

$$\begin{cases} \text{Min } (K_I i + K_Q Q + K_V THD_V - K_P P) \\ V_o = V_o^* \\ 0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \pi; \\ 0 < \beta_1 < \beta_2 < \pi;\ 0 < \theta < \frac{\pi}{2} \end{cases} \tag{2-38}$$

where, V_o^* is the regulated output voltage. Also, the K_I, K_Q, K_V and K_P are the constant values to normalize the cost function. THD_{Vp} is calculated as follows:

$$THD_{Vp} = \frac{\sqrt{{V_{p,3}}^2 + {V_{p,5}}^2 + {V_{p,7}}^2}}{V_{p,1}} \tag{2-39}$$

2.2.2.2 Comprehensive analysis

The equivalent circuit of the proposed converter is depicted in Figure 2.9, where v_p, v_s' and L_s are the primary square voltage, secondary square voltage referred to the primary side and the equivalent series and leakage inductances of the transformer, respectively. Under normal operation, the primary voltage is 5-level,

and the secondary voltage is 3-level. Each periodic square sources of v_p and v_s' can be considered as the summation of infinite sinusoidal ac sources ($v_{p,x}$ and $v_{s,y}$') with a Fourier series as follows:

$$v_p(\omega t) = \sum_{x=1,3,5}^{\infty} v_{p,x} = \sum_{x=1,3,5}^{\infty} V_{p,x}\sin(x\omega t) \tag{2-40}$$

$$v_s'(\omega t) = \sum_{y=1,3,5}^{\infty} v_{s,y}' = \sum_{y=1,3,5}^{\infty} V_{s,y}'\sin(y(\omega t - \theta)) \tag{2-41}$$

where, θ is the phase shift of the secondary voltage. The coefficients $V_{p,x}$ and $V_{s,y}'$ are the peak values of each order in primary and secondary voltages that are calculated as follows:

$$V_{p,x} = \frac{2V_H}{x\pi}(\cos(x\alpha_1) + \cos(x\alpha_2) - \cos(x\alpha_3) - \cos(x\alpha_4)), \quad x = 1,3,\ldots \tag{2-42}$$

$$V_{s,y}' = \frac{2nV_o}{y\pi}(\cos(y\beta_1) - \cos(y\beta_2)), \quad y = 1,3,\ldots \tag{2-43}$$

where V_H and V_o are the half of the total dc-link and regulated output voltage, respectively. α_1 and α_2 are the rising edges and α_3 and α_4 are the falling edges of the positive half cycle of the primary voltage and β_1 and β_2 are the rising

and falling edges of the positive half cycle of the secondary voltage, respectively. As depicted in Figure 2.9, the current can flow between each two sources in primary and secondary sides (i_{xy}) and subsequently active and reactive powers (P_{xy} and Q_{xy}) can transfer between them.

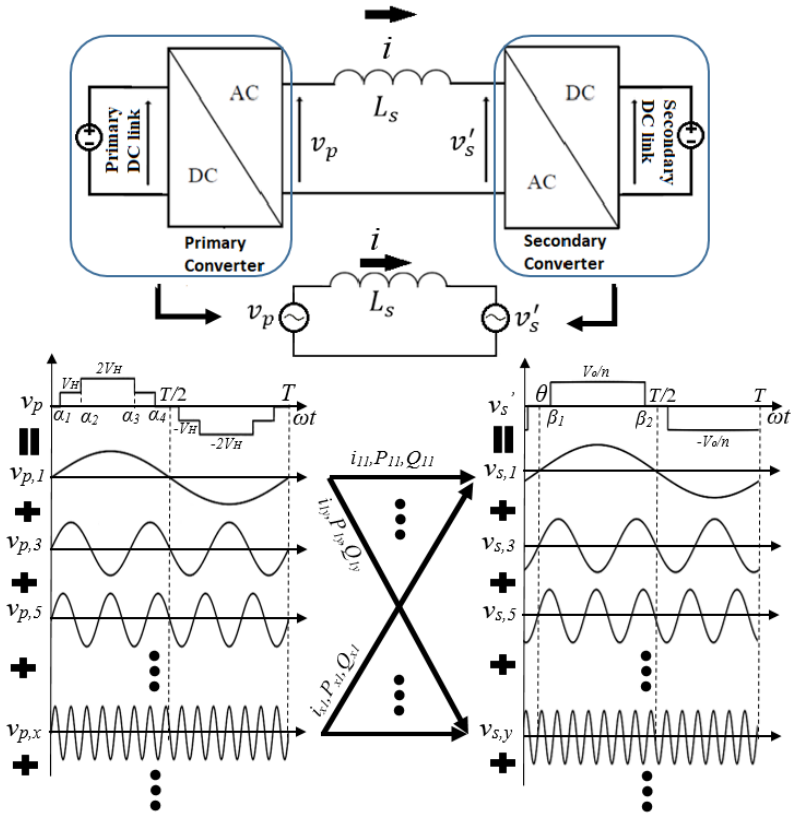


Figure 2.9 The equivalent circuit of the proposed converter and analysis principle.

The primary current is calculated as (2-44).

$$i_{xy}(\omega t) = \frac{1}{L_s \omega}\left(\frac{-V_{p,x}}{x}\cos(x\omega t) + \frac{V_{s,y}}{y}\cos(y(\omega t - \theta))\right) \tag{2-44}$$

In the case of $x = y$, the current can be considered as

$$i_{xx}(\omega t) = \sum_{x=1,3,5}^{\infty} \mathrm{A}\cos(x\omega t + \tan^{-1}(B)) \tag{2-45}$$

$$A = \frac{\sqrt{(V_{p,x})^2 + (V_{s,x})^2 - 2V_{p,x}V_{s,x}\cos(x\theta)}}{xL_s\omega} \tag{2-46}$$

$$B = \frac{V_{s,x}\sin(x\theta)}{V_{s,x}\cos(x\theta) - V_{p,x}} \tag{2-47}$$

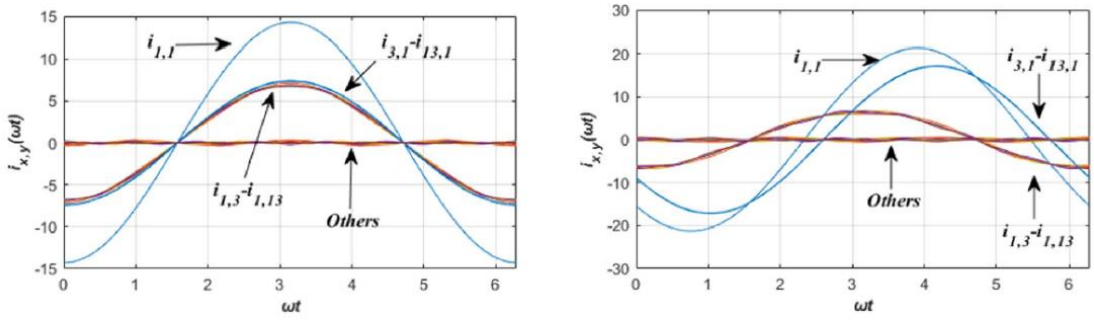
In the case of $x \neq y$, no active power transfers. If $x = y$, the transferred active and reactive powers are calculated as (2-48) and (2-49), respectively.

$$P_{xx} = \frac{V_{p,x}V'_{s,x}}{2xL_s\omega}\sin(x\theta), \quad x = 1,3,\ldots \tag{2-48}$$

$$Q_{xx} = \frac{V_{p,x}V'_{s,x}}{2xL_s\omega}\cos(x\theta) - \frac{(V_{p,x})^2}{2xL_s\omega}, \quad x = 1,3,\ldots \tag{2-49}$$

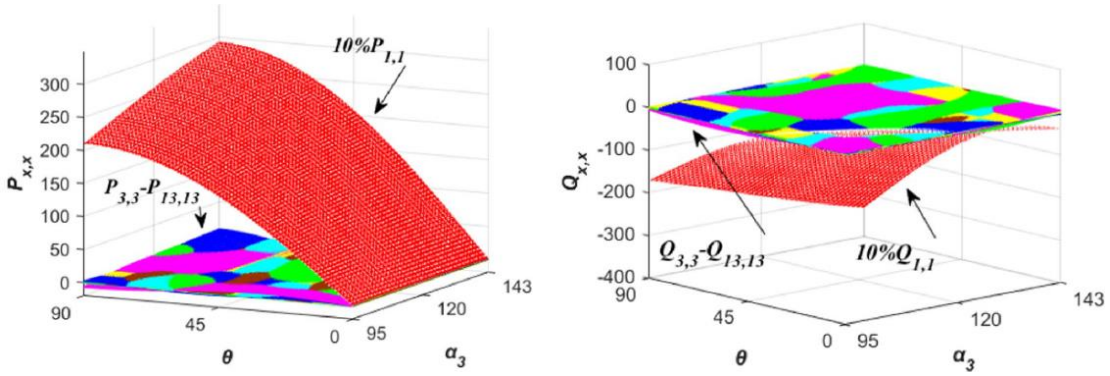
Let's assume V_H, V_o, f_c, L, n, α_1, α_2, α_3, α_4 and β_2 are 500V, 500V, 48kHz, 100μH, 1, 10°, 45°, 130°, 160° and 140°, respectively. Figure 2.10(a) and (b) show the current waveform when β_1 is 40° and θ equals to 15° and 75°. It is shown that in the case of θ equal to 15°, the first order (i_{11}) has the highest value. When the

harmonic order y is equal to 1 and x differs from 3 to 13 (i_{31} to $i_{13,1}$), the current values are almost the same and have second highest value. When the harmonic order x is equal to 1 and y differs from 3 to 13 (i_{13} to $i_{1,13}$), the current values are about the same and have third highest value. The others can be ignored. The same applies when θ is 75°, the currents of i_{31} to $i_{13,1}$ have the same and highest value, the i_{11} has the second highest value and currents of i_{13} to $i_{1,13}$ have the same and third highest value. Figure 2.11(a) and (b) show the active (P_{xx}) and reactive (Q_{xx}) powers when x varies from 1 to 13. In these figures, β_1 and θ vary from 0 to 140 and 0 to 90, respectively. Based on Figure 2.11, the fundamental values of active and reactive powers are much more than other components, therefore only fundamental component is considered.



(a) (b)

Figure 2.10 The current waveforms in the cases of θ equal to (a) 15° and (b) 75°.



(a) (b)

Figure 2.11 (a) Active power (P_{xx}), (b) reactive power (Q_{xx}); when x varies from 1 to 13.

The desired power in the isolated dc-dc converter is active power, while the reactive power increases the losses. For utilizing the maximum possible capacity of the converter, the amount of active power should be maximized while the reactive power should be minimal. In addition, based on the loss analysis the RMS values of the transformer's current and THD of the primary voltage should be minimized to obtain higher efficiency. There are seven control parameters of α_1- α_4, β_1- β_2 and θ in the normal operation of the proposed converter. The weighted cost function to calculate the control parameters is considered as (2-50).

$$\begin{cases} \text{Min } K_I(i_{11}+i_{13}+i_{31}) + K_Q|Q_{11}| + K_{Vp}THD_{Vp} - K_P P_{11} \\ V_o = V_o^* \\ 0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \pi; \\ 0 < \beta_1 < \beta_2 < \pi;\ 0 < \theta < \dfrac{\pi}{2} \end{cases} \tag{2-50}$$

where

$$i_{11} = \frac{\sqrt{(V_{p,1})^2 + (V_{s,1})^2 - 2V_{p,1}V_{s,1}\cos(\theta)}}{\sqrt{2}L_s\omega} \tag{2-51}$$

$$Q_{11} = \frac{V_{p,1}V'_{s,1}}{2L_s\omega}\cos\theta - \frac{(V_{p,1})^2}{2L_s\omega} \tag{2-52}$$

$$p_{11} = \frac{V_{p,1}V'_{s,1}}{2L_s\omega}\sin(\theta) \tag{2-53}$$

$$THD_{Vp} = \frac{\sqrt{{V_{p,3}}^2 + {V_{p,5}}^2 + {V_{p,7}}^2}}{V_{p,1}} \tag{2-54}$$

In (2-50), V_o^* is the regulated output voltage. Also, the K_I, K_Q, K_{VP} and K_P are constant values to normalize the cost function. The current waveforms of i_{13} and i_{31} are not sinusoidal waveform, but can be approximated as:

$$i_{13} \cong \frac{-V_{p,1}}{L_s\omega} \tag{2-55}$$

$$i_{31} \cong \frac{V_{s,1}}{L_s\omega} \tag{2-56}$$

It is worth noting that in (2-50), $-\pi/2 < \theta < 0$ is for transferring power from secondary to primary. For the operating point of V_H, V_o, f_c, L and n equal to 500V, 500V, 48kHz, 100μH and 1, for different values of V_o between 100V to 1kV, the optimization results are shown in Figure 2.12.

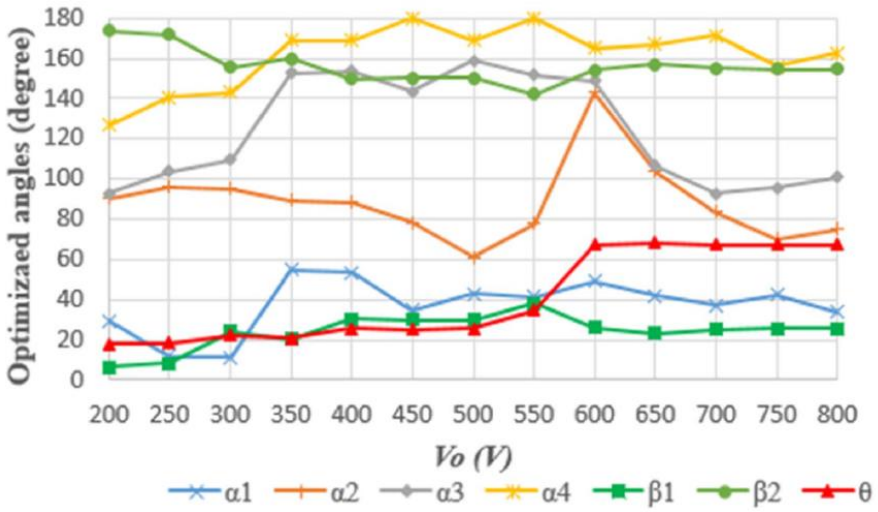


Figure 2.12 The optimization results for different values of V_o.

2.2.3 DC-bus design

Figure 2.13 shows the current commutation loops (CCLs) in the proposed converter.

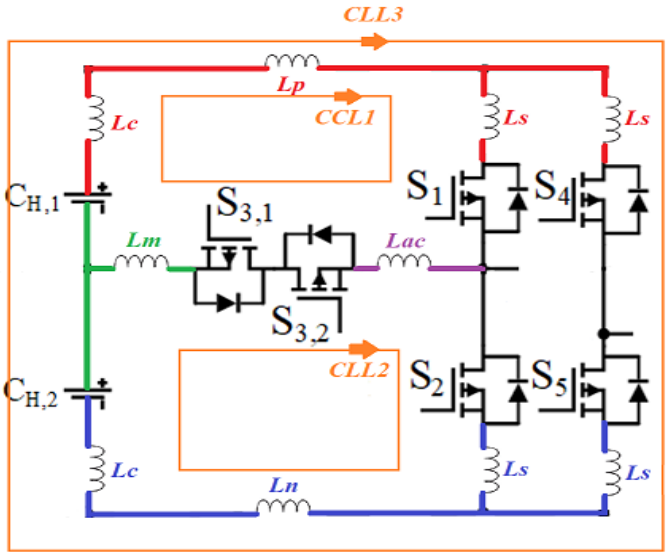


Figure 2.13 The current commutation loops in the proposed converter.

As shown in Figure 2.13, there are three CCLs as *CCL1* and *CCL2* in the inner loops and *CCL3* in the outer loop. *Lc* is the inductance of dc-link capacitors, *Lp*, *Ln* and *Lm* are the connection's inductance, *Ls* is the switches inductance and *Lac* is the connection's inductance in the ac part. *Lc* and *Ls* can be minimized by selecting proper capacitors and switches with the lower internal inductances. For minimizing the *Lp*, *Ln*, *Lm* and *Lac*, a dc-link should be designed. In this work, a dc-link is designed and simulated in Ansys Q3D that is shown in Figure 2.14. In this figure, the bottom layer is a positive layer, the middle layer is negative, and the upper layer is neutral layer.

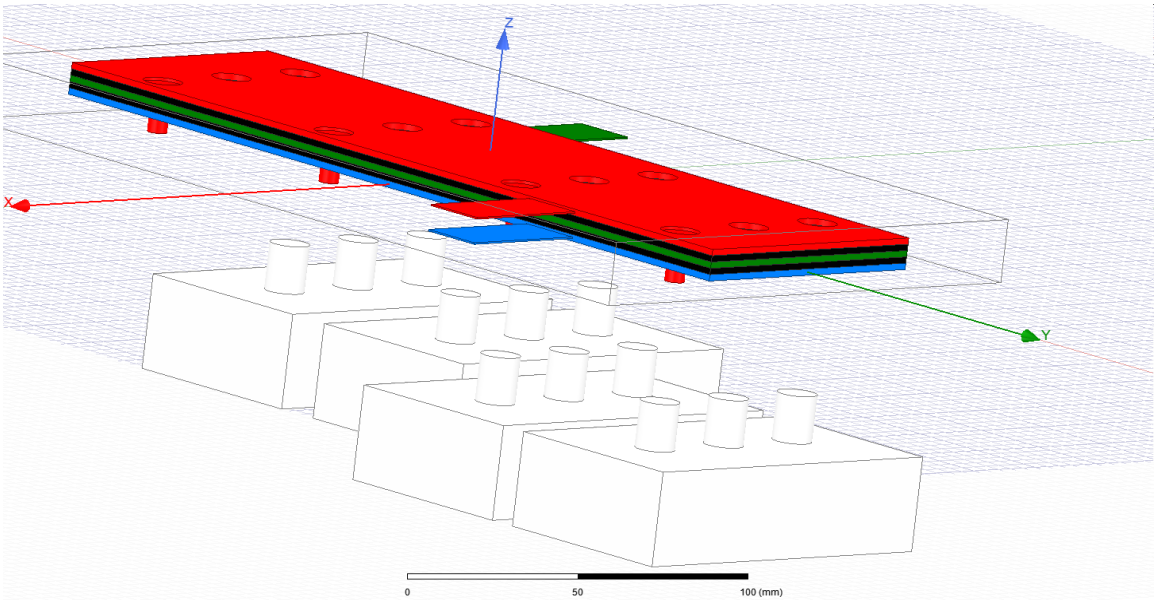
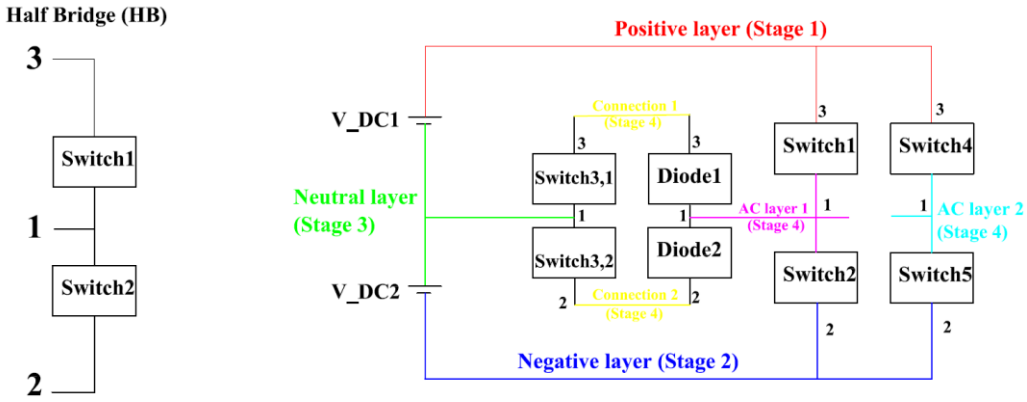
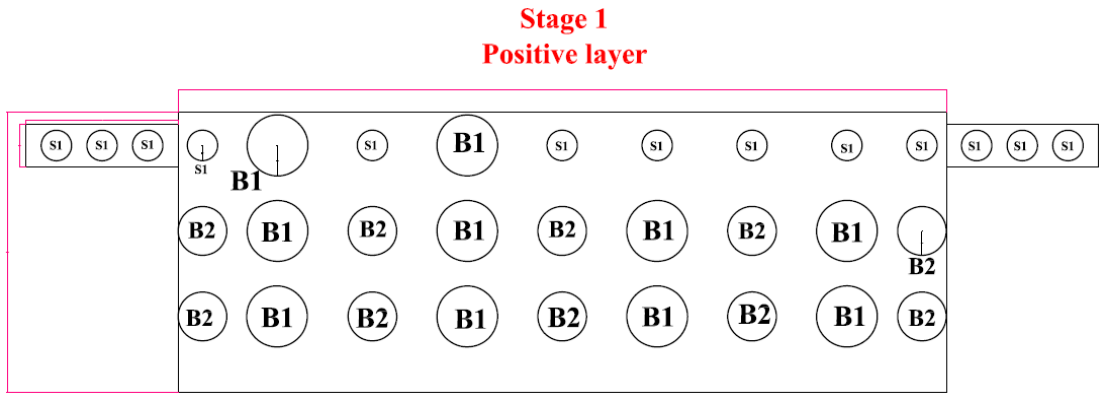


Figure 2.14 The designed dc-link in Ansys Q3D.

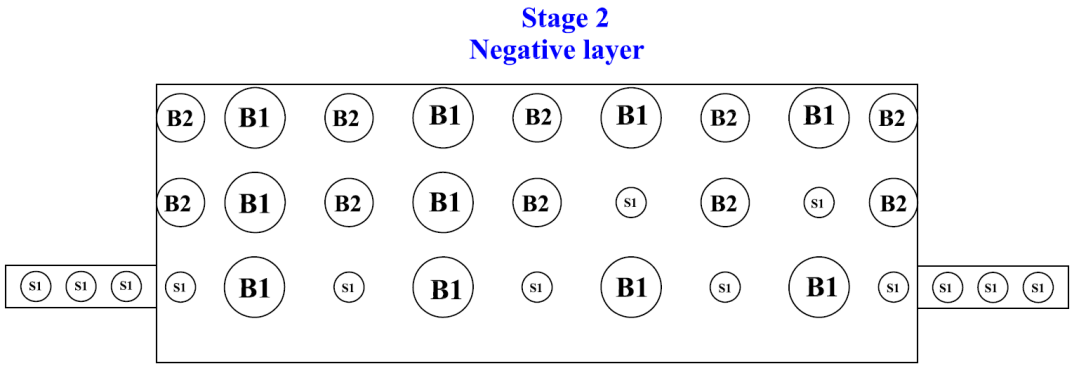
Figure 2.15 shows the detailed CAD designed of the proposed dc-link.



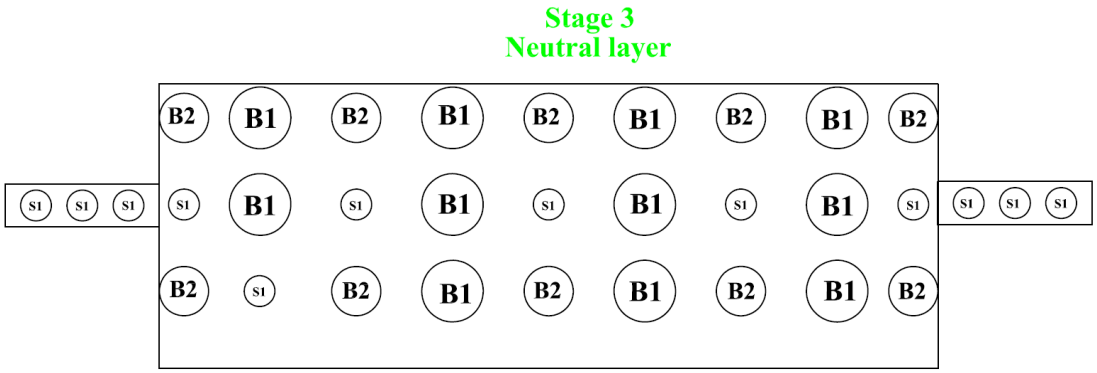
(a)


Stage 1
Positive layer
S1
B1
B2

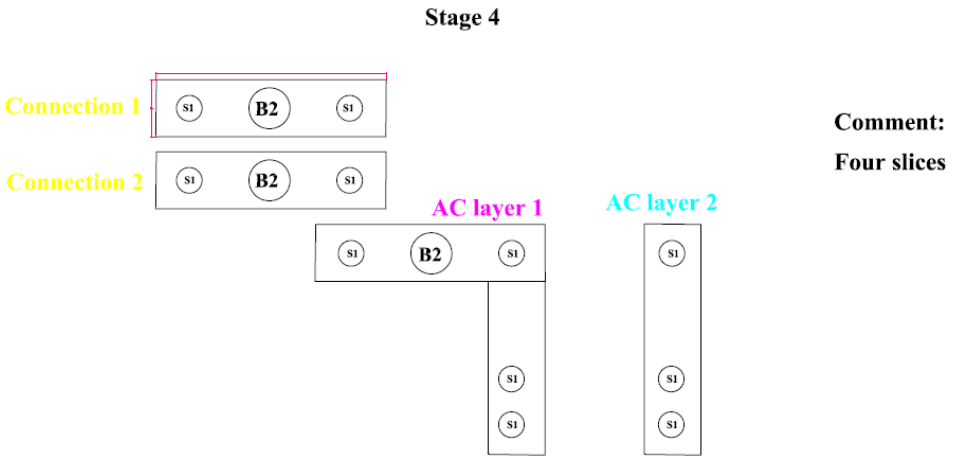
(b)


Stage 2
Negative layer
B2
B1
S1

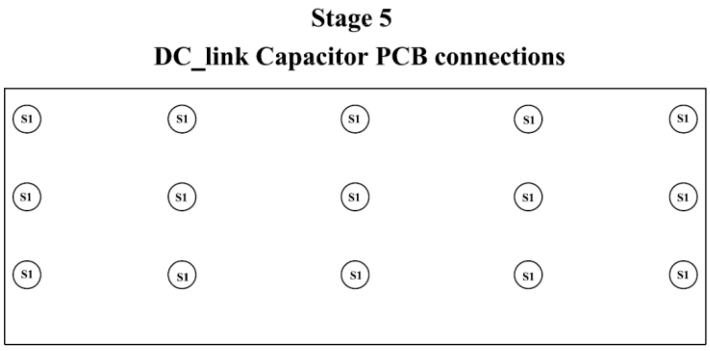
(c)


Stage 3
Neutral layer
B2
B1
S1

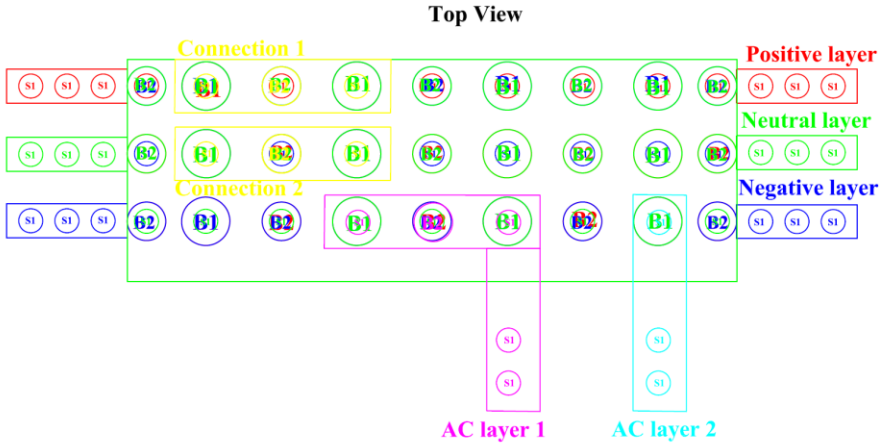
(d)


Stage 4
Connection 1
Connection 2
S1
B2
AC layer 1
AC layer 2
Comment:
Four slices

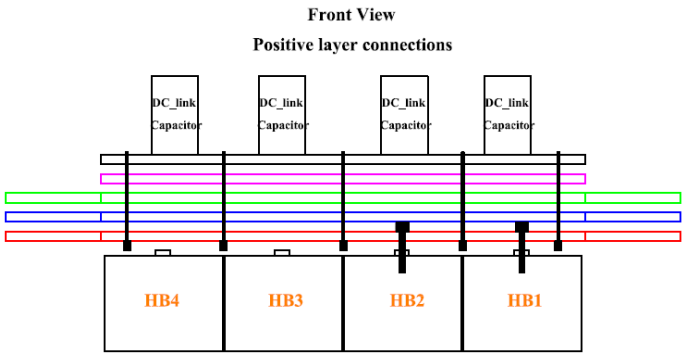
(e)


Stage 5
DC_link Capacitor PCB connections
S1

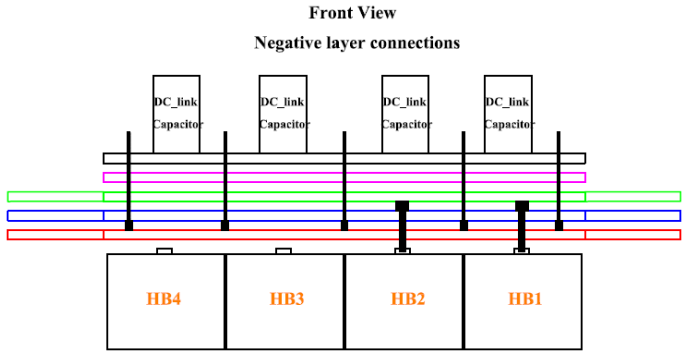
(f)


Top View
Connection 1
Connection 2
Positive layer
Neutral layer
Negative layer
B1
B2
S1
AC layer 1
AC layer 2

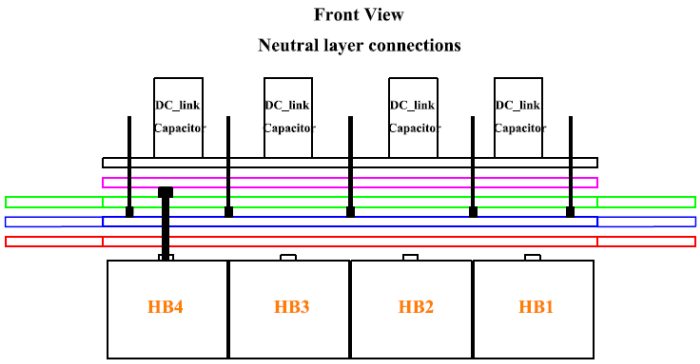
(g)


Front View
Positive layer connections
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
HB4
HB3
HB2
HB1

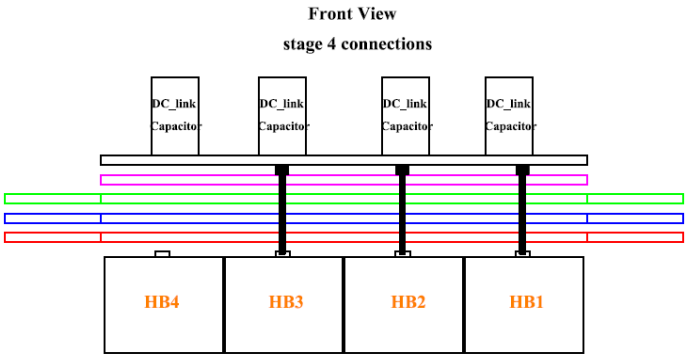
(h)


Front View
Negative layer connections
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
HB4
HB3
HB2
HB1

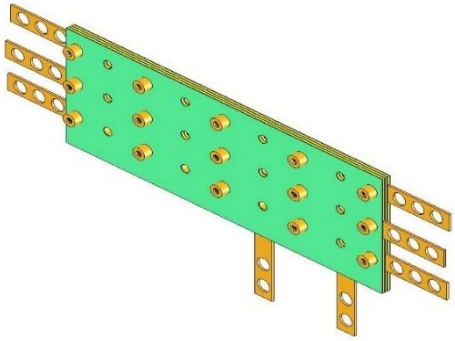
(i)


Front View
Neutral layer connections
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
DC_link Capacitor
HB4
HB3
HB2
HB1

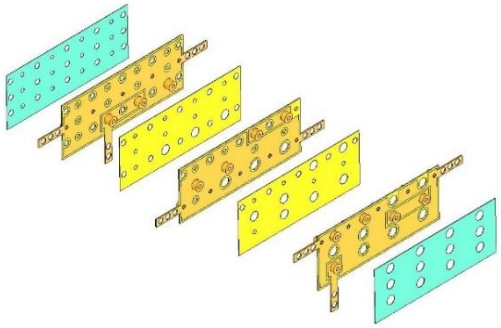
(j)



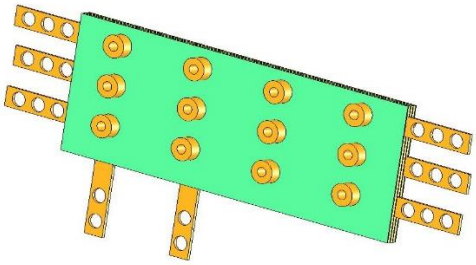
(l)



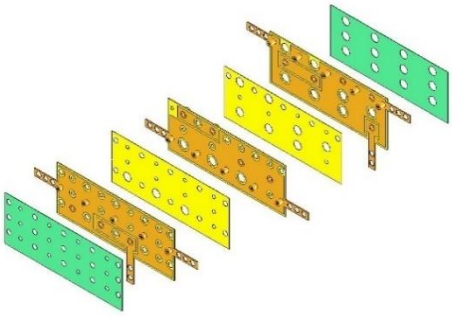
(m)



(n)



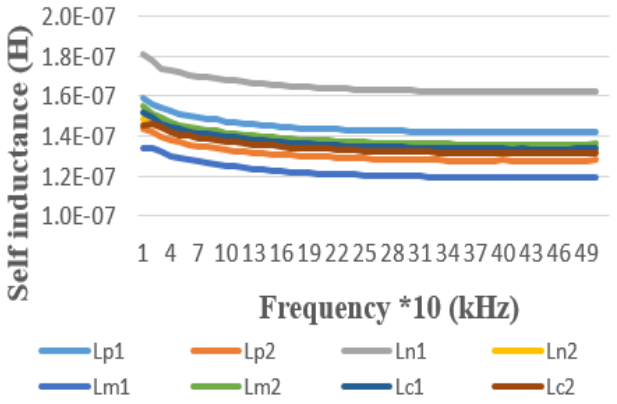
(o)



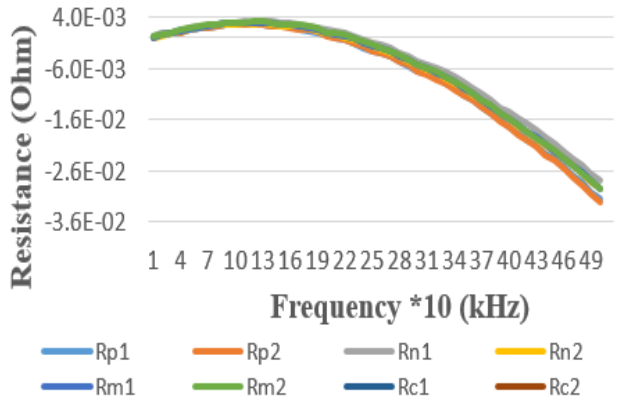
(p)

Figure 2.15 Detailed CAD designed of the proposed dc-link.

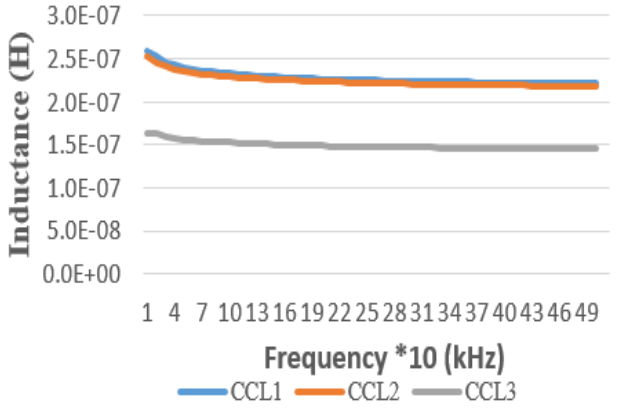
The resistances and inductances in each layer are shown in Figure 2.16.


Self inductance (H)
2.0E-07
1.8E-07
1.6E-07
1.4E-07
1.2E-07
1.0E-07
1 4 7 10 13 16 19 22 25 28 31 34 37 40 43 46 49
Frequency *10 (kHz)
Lp1
Lp2
Ln1
Ln2
Lm1
Lm2
Lc1
Lc2

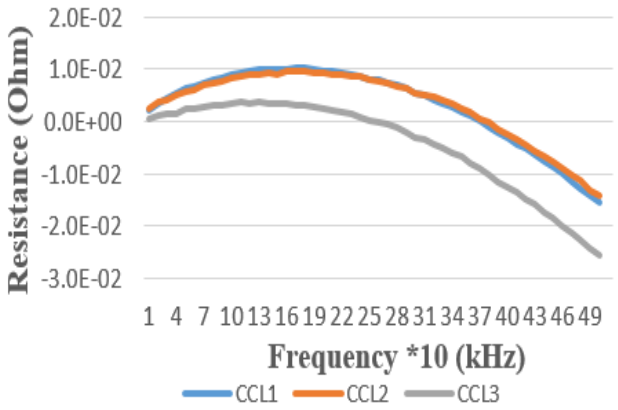
(a)


Resistance (Ohm)
4.0E-03
-6.0E-03
-1.6E-02
-2.6E-02
-3.6E-02
1 4 7 10 13 16 19 22 25 28 31 34 37 40 43 46 49
Frequency *10 (kHz)
Rp1
Rp2
Rn1
Rn2
Rm1
Rm2
Rc1
Rc2

(b)


Inductance (H)
3.0E-07
2.5E-07
2.0E-07
1.5E-07
1.0E-07
5.0E-08
0.0E+00
1 4 7 10 13 16 19 22 25 28 31 34 37 40 43 46 49
Frequency *10 (kHz)
CCL1
CCL2
CCL3

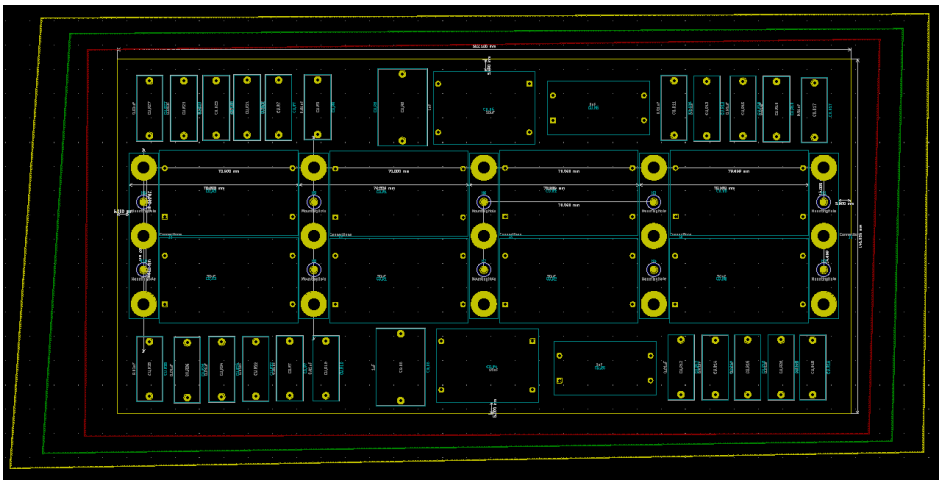
(c)



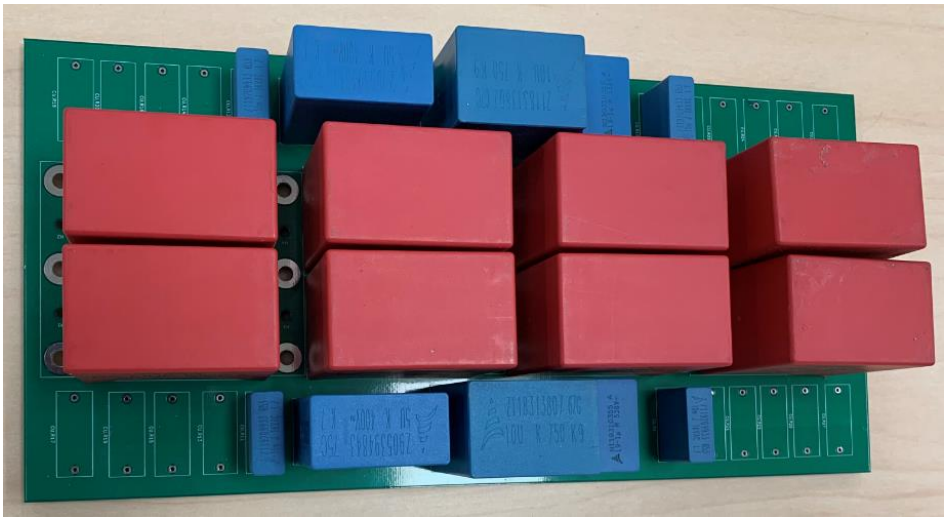
(d)

Figure 2.16 (a) and (b) Self-inductances and their resistances (c) and (d) inductances and resistances of CCLs; in the primary side of the converter.

Figure 2.17 shows the designed printed circuit board (PCB) for the dc-link capacitors.



(a)



(b)

Figure 2.17 PCB for the dc-link capacitors.

2.2.4 Heatsink design

A heatsink is designed based on the switches' losses. For each device, an acceptable maximum limit of the heatsink temperatures is resulted as (2-57) [28].

$$T_{j-i} = Q_{c-i} \times (R_1 + R_2) + T_h \leq T_{limit} \tag{2-57}$$

where $Q_{c\text{-}i}$, R_1, R_2, $T_{j\text{-}i}$, T_h, and T_{limit} are the power loss generated by the i^{th} device, thermal resistance from junction to case, thermal resistance of the interface between the case and the heatsink, temperature of the i^{th} device junction, temperature of the heatsink and upper limit for the operating junction temperature for that device. The required thermal resistance for the heatsink R_3 is given in (2-58). Here, T_0 is the ambient temperature.

$$R_3 = \frac{T_h - T_0}{Q_{c-i}} \tag{2-58}$$

The thermal characteristics of the active switches in this work were modeled in the PLECS software package and based on that, the proposed converter is simulated. The loss of 10 kW primary converter is 180 W for three modules. Here, R_2 is zero. By considering the worst case of 0.125 ˚C/W for R_1, T_0 of 25 ˚C, and maximum junction temperature of 150 ˚C, R_3 is resulted as 1.83 ˚C/W.

2.2.5 Fault tolerance analysis

In dual-active full bridge dc-dc converter, if one of the switches in the primary or the secondary sides has open-circuit failure, this structure can't continue its operation and should completely shut down. The proposed converter in this work has fault tolerant capability on the open-circuit failure of switches S_1, S_2, $S_{3,1}$ and $S_{3,2}$ from the primary side and switches T_1, T_2, $T_{3,1}$ and $T_{3,2}$ from the secondary side without any change in the blocking voltages of the remaining operating switches.

2.2.5.1 Fault tolerant analysis in PWM modulation

The proposed converter has fault tolerance capability in the case of open circuit failure of switches S_1, S_2, $S_{3,1}$ and $S_{3,2}$ from primary converter and T_1 and T_2 from secondary converter. This capability is analyzed in this section when PWM

modulation is applied. For the other two modulations, the analysis is similar. In the normal operation of the proposed structure, S_1, S_2, $S_{3,1}$ and $S_{3,2}$ switches from primary side are high-frequency switches, while S_4 and S_5 are low frequency switches. In the proposed methodology, fault signals of F_{S1} and F_{S2} are one when the fault is on switches S_1 and S_2, respectively. Also, the fault signal of F_{S3} is one for fault on switches $S_{3,1}$ or $S_{3,2}$. Moreover, in the secondary converter, F_{S4} and F_{S5} are used for open circuit failures of switches T_1 and T_2, respectively. When one of the fault signals is one, the fault tolerant control methods are applied that investigated in detail as follows:

In normal operation, there are six different switching states in the primary converter and four different switching states in the secondary converter. The primary and secondary voltages are 5-level and 3-level PWM voltages that can transfer power by using series leakage inductors of high-frequency transformer. Output voltage is regulated by using two series output capacitors C_{L1} and C_{L2}. It is supposed to have resistive load in this analysis.

In the first step (F_{s1}=1), it is supposed that an open-circuit fault happens on switch S_1. The available switching states in primary side will be three, while the secondary side has its four normal switching states. The primary converter can generate 3-level PWM voltages of $-V_H$, 0 and V_H by using the switches S_2, $S_{3,2}$, S_4 and S_5. In the modulation method of this step, two rectified (R_{H1}) and normal (R_{H2})

sinusoidal are used as reference waveforms. There are two carriers C_1 and C_2 with the amplitudes between 0.5 to 1 and 0 to 0.5 respectively, that C_2 is 180 degrees out of phase in respect to C_1. When R_{H1} is larger than carrier C_1, $S_{3,2}$ is on and S_2 operates in the complementary of $S_{3,2}$. Also, when R_{H2} is larger than carrier C_2, S_4 is on and S_5 operates in the complementary of S_4. Switch $S_{3,1}$ is on. The secondary converter has its normal operation.

In the second step (F_{s2}=1), it is supposed that an open circuit fault happens on switch S_2. The available switching states in primary side will be three, while the secondary side has its four normal switching states. The primary converter can generate 3-level PWM voltage of $-V_H$, 0 and V_H by using the switches S_1, $S_{3,1}$, S_4 and S_5. The concept of the modulation method is like the first step. When R_{H1} is larger than carrier C_1, $S_{3,1}$ is on and S_1 operates in the complementary of $S_{3,1}$. Also, when R_{H2} is larger than carrier C_2, S_5 is on and S_4 operates in complementary of S_5. Switch $S_{3,2}$ is on. The secondary converter has its normal operation.

In the third step (F_{s3}=1), it is supposed that an open circuit fault happens on switch $S_{3,1}$ or $S_{3,2}$. The available switching states in primary side will be four, while secondary side has its four normal switching states. The primary converter can generate 3-level PWM voltage of $-2V_H$, 0 and $2V_H$ by using the switches S_1, S_2, S_4 and S_5. In the modulation method of the primary converter, there are two sinusoidal references, R_{H1} and R_{H2} that have 180 degrees phase-shifted regarding to

each other. There is a carrier C_1 with the amplitude -1 to 1. When R_{H1} is larger than carrier C_1, S_1 is on and when R_{H2} is larger than carrier C_2, S_4 is on. Switches S_2 and S_5 operate in complementary of S_1 and S_4 respectively. The secondary converter has its normal operation.

In the fourth step (F_{s4}=1), it is supposed that an open-circuit fault happens on switch T_1. The available switching states in secondary side will be three, while the primary side has its six normal switching states. The primary converter can generate 5-level PWM voltages of $-2V_H$, 0 and $2V_H$. In the modulation method of the secondary converter, there are two rectified (R_{L1}) and normal (R_{L2}) sinusoidal references. Also, two carriers C_3 and C_4 with the amplitudes between 0.5 to 1 and 0 to 0.5 are used respectively, that C_4 is 180 degrees out of phase in respect to C_3. When R_{L1} is larger than carrier C_3, $T_{3,2}$ is on and T_2 operates in complementary of $T_{3,2}$. Also, when R_{L2} is larger than C_4, T_4 is on and T_5 operates in complementary of T_4. Switch $T_{3,1}$ is on.

Finally in the fifth step (F_{s5}=1), it is supposed that an open-circuit fault happens on switch T_2. The available switching states and produced voltages are similar to step four. When R_{L1} is larger than carrier C_3, $T_{3,1}$ is on and T_1 operates in complementary of $T_{3,1}$. Also, when R_{L2} is larger than C_4, T_5 is on and T_4 operates in complementary of T_5. Switch $T_{3,2}$ is on. The time constant of charging capacitors $C_{L,1}$ and $C_{L,2}$ depend on the switches' resistance, while their discharging time

constant depends on the load resistance which is much higher than switches' resistance. Therefore, the proposed converter can operate properly. Therefore, by adjusting the modulation method in the faulty condition, the proposed converter has compatibility to transfer power to the load. The complete modulation algorithm is shown in Figure 2.18.

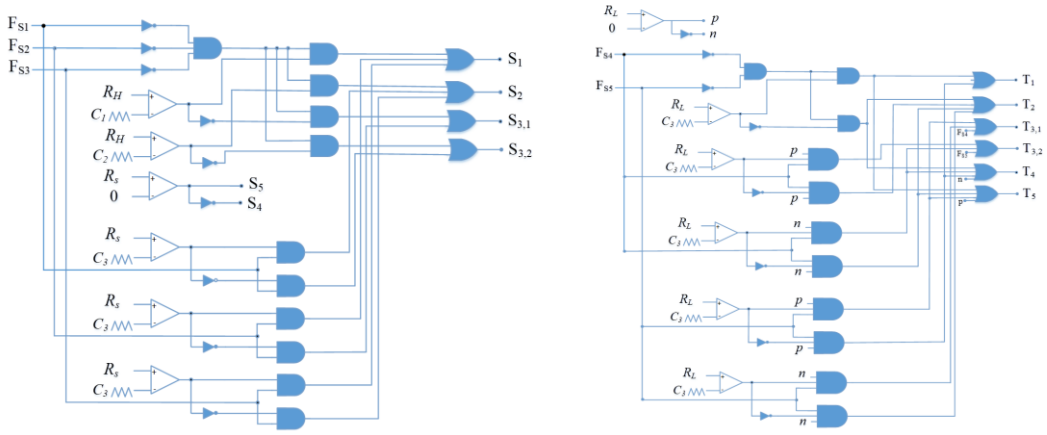
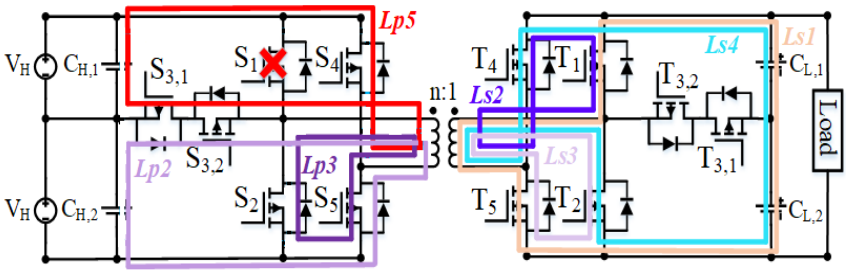


Figure 2.18 Fault tolerance operation of the proposed converter in PWM modulation method.

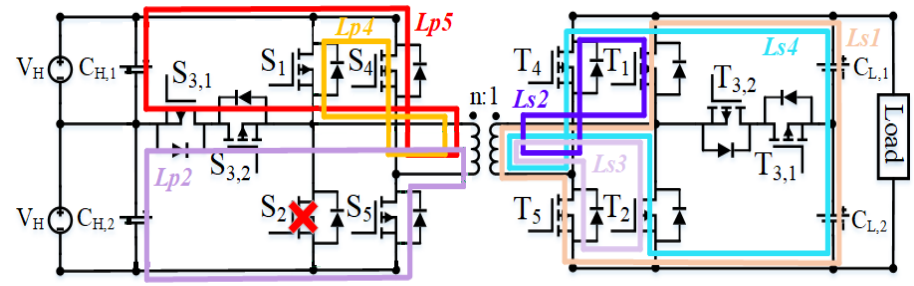
2.2.6 Fault tolerant analysis in square-wave modulation

First, let's assume an open-circuit fault occurs on switch S_1 or S_2 (mode 2). The primary converter has three switching states and produces 3-level voltage of $+V_H$, 0 and $-V_H$ at the primary side of the transformer by using switches S_2, $S_{3,1}$, $S_{3,2}$, S_4, S_5 (fault on S_1) or S_1, $S_{3,1}$, $S_{3,2}$, S_4 and S_5 (fault on S_2). They are shown in

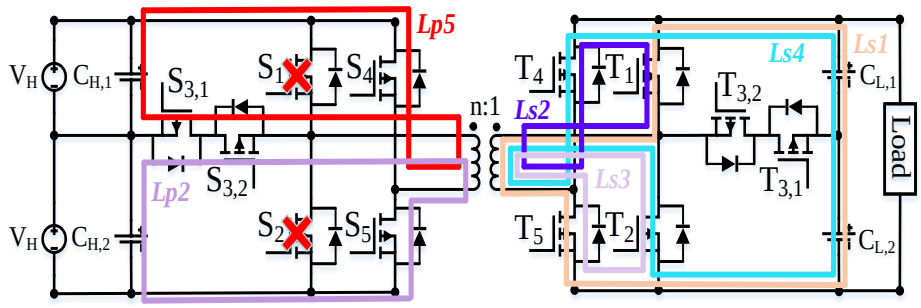
Figure 2.19(a) and (b). In mode 3, it is assumed that open-circuit faults are on both switches S_1 and S_2 simultaneously. The primary converter has two switching states and produces 2-level voltage of $+V_H$ and $-V_H$ by using switches $S_{3,1}$, $S_{3,2}$, S_4 and S_5 (Figure 2.19(c)). In mode 4, the open circuit fault is on switch $S_{3,1}$ or $S_{3,2}$ or both. The primary converter operates as full bridge inverter and produces 3-level voltage of $+2V_H$, 0 and $-2V_H$ by using switches S_1, S_2, S_4 and S_5 (Figure 2.19(d)). In these modes, the secondary converter has its four switching states as normal operation. In mode 5, assuming an open circuit fault on switch T_1 or T_2, the secondary converter has three switching states and produces 3-level voltage of $+V_o$, 0 and $-V_o$ at the secondary side of the transformer by using switches T_2, $T_{3,1}$, $T_{3,2}$, T_4, T_5 (fault on T_1) or T_1, $T_{3,1}$, $T_{3,2}$, T_4, T_5 (fault on T_2). They are shown in Figure 2.19(e) and (f). Finally, in mode 6, in the case of open circuit failure on switches T_1 and T_2, the secondary converter has two switching states and produces 2-level voltage of $+V_H$ and $-V_H$ by using switches $T_{3,1}$, $T_{3,2}$, T_4 and T_5 (Figure 2.19(g)). In modes 5 and 6, the primary converter has its normal operation.



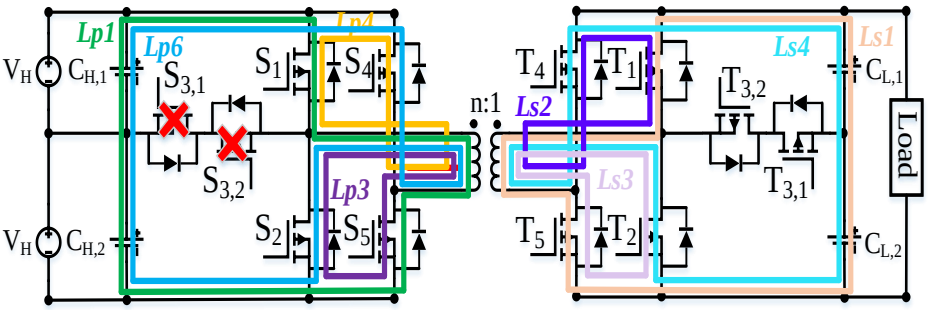
(a)


Lp4
Lp5
VH
CH,1
S3,1
S1
S4
n:1
Ls2
T4
T1
Ls4
Ls1
CL,1
T3,2
Load
Lp2
S3,2
Ls3
T3,1
VH
CH,2
S2
S5
T5
T2
CL,2

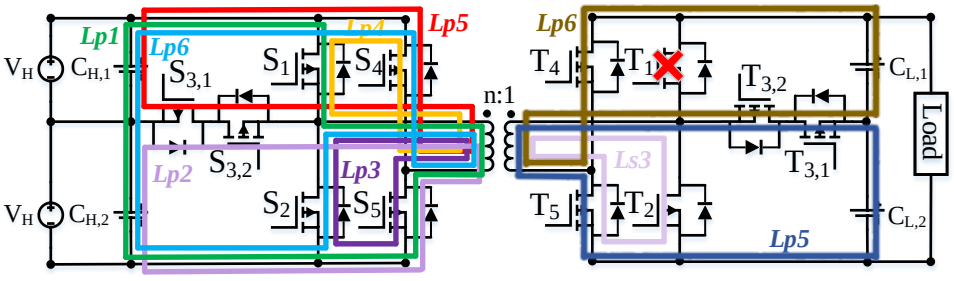
(b)


Lp5
VH
CH,1
S3,1
S1
S4
n:1
Ls2
T4
T1
Ls4
Ls1
CL,1
T3,2
Load
Lp2
S3,2
Ls3
T3,1
VH
CH,2
S2
S5
T5
T2
CL,2

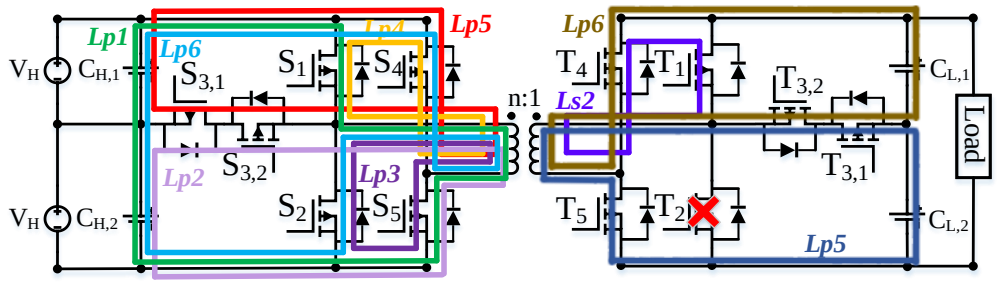
(c)


Lp1
Lp6
Lp4
VH
CH,1
S3,1
S1
S4
n:1
Ls2
T4
T1
Ls4
Ls1
CL,1
T3,2
Load
S3,2
Lp3
Ls3
T3,1
VH
CH,2
S2
S5
T5
T2
CL,2

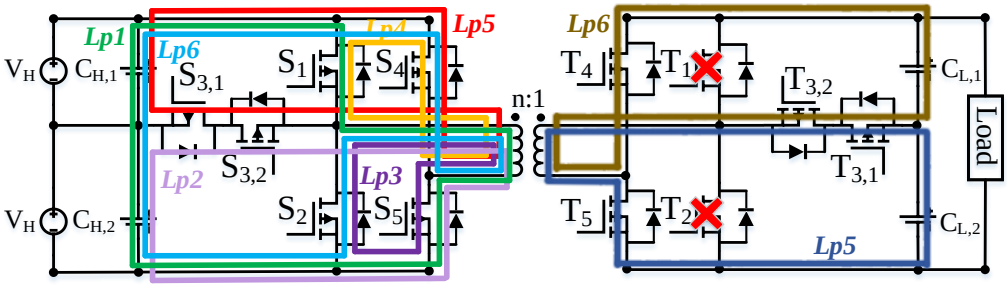
(d)


Lp1
Lp6
Lp4
Lp5
VH
CH,1
S3,1
S1
S4
n:1
Lp6
T4
T1
T3,2
CL,1
Load
Lp2
S3,2
Lp3
Ls3
T3,1
VH
CH,2
S2
S5
T5
T2
Lp5
CL,2

(e)



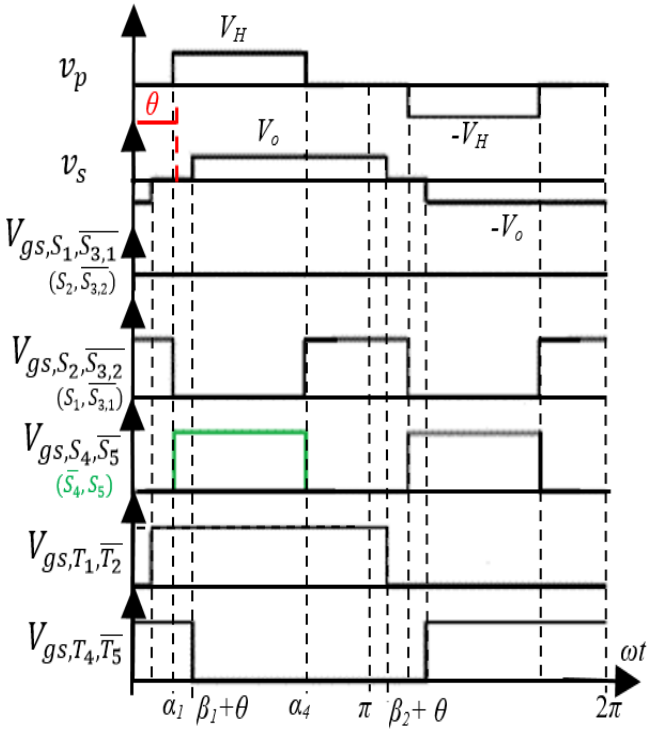
(f)



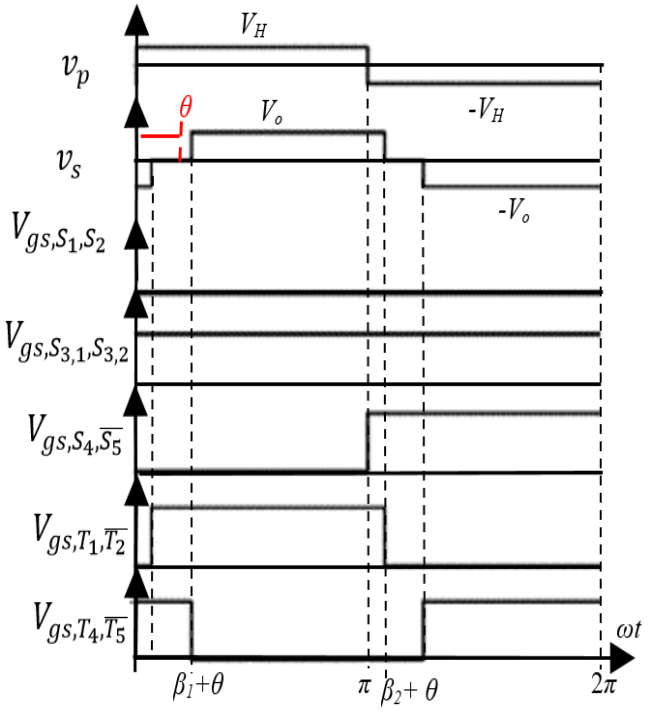
(g)

Figure 2.19 Available operating scenarios of the proposed converter in the open circuit fault on (a) switch S_1, (b) switch S_2, (c) switches S_1 and S_2, (d) switches $S_{3,1}$ and $S_{3,2}$; (e) switch T_1, (f) switch T_2 and (g) switches T_1 and T_2.

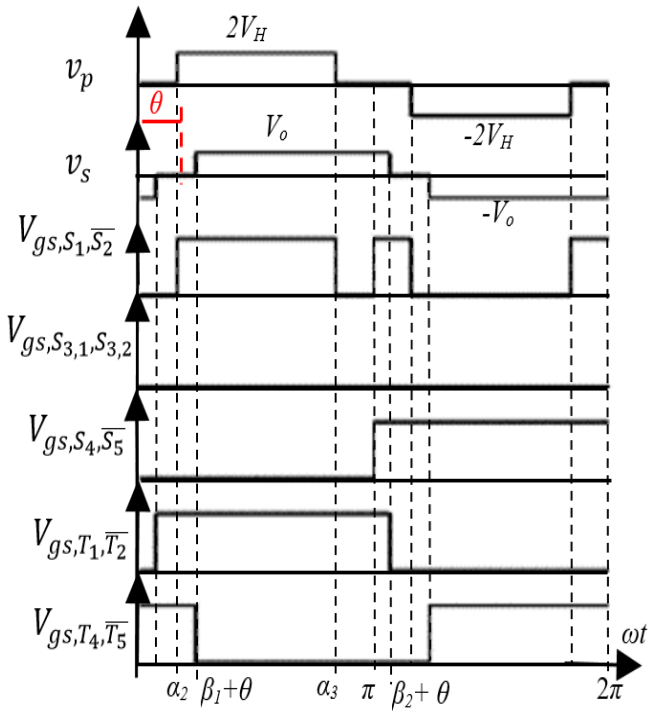
The switching concept in each mode of faulty conditions is also shown in Figure 2.20.


V_H
v_p
θ
V_o
$-V_H$
v_s
$-V_o$
$V_{gs,S_1,\overline{S_{3,1}}}$
$(S_2,\overline{S_{3,2}})$
$V_{gs,S_2,\overline{S_{3,2}}}$
$(S_1,\overline{S_{3,1}})$
$V_{gs,S_4,\overline{S_5}}$
$(\overline{S_4},S_5)$
$V_{gs,T_1,\overline{T_2}}$
$V_{gs,T_4,\overline{T_5}}$
ωt
α_1 $\beta_1+\theta$ α_4 π $\beta_2+\theta$ 2π

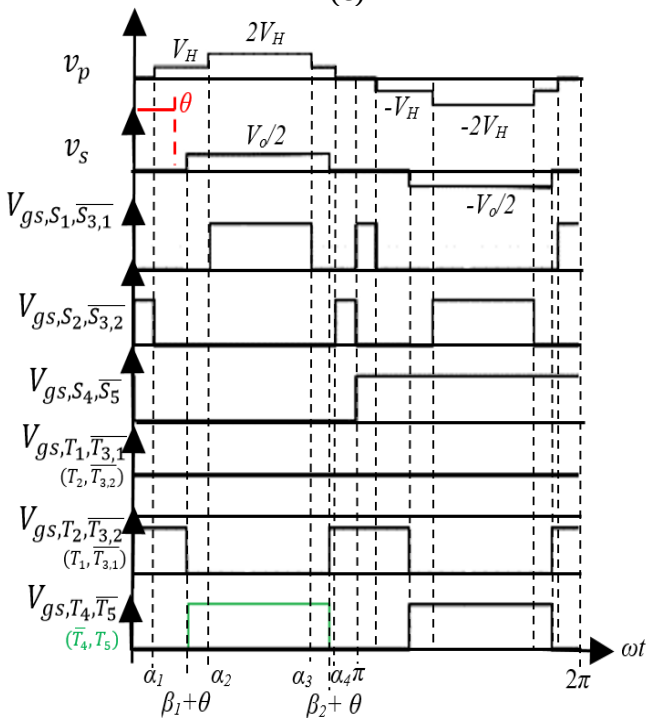
(a)


V_H
v_p
θ
V_o
$-V_H$
v_s
$-V_o$
V_{gs,S_1,S_2}
$V_{gs,S_{3,1},S_{3,2}}$
$V_{gs,S_4,\overline{S_5}}$
$V_{gs,T_1,\overline{T_2}}$
$V_{gs,T_4,\overline{T_5}}$
ωt
$\beta_1+\theta$ π $\beta_2+\theta$ 2π

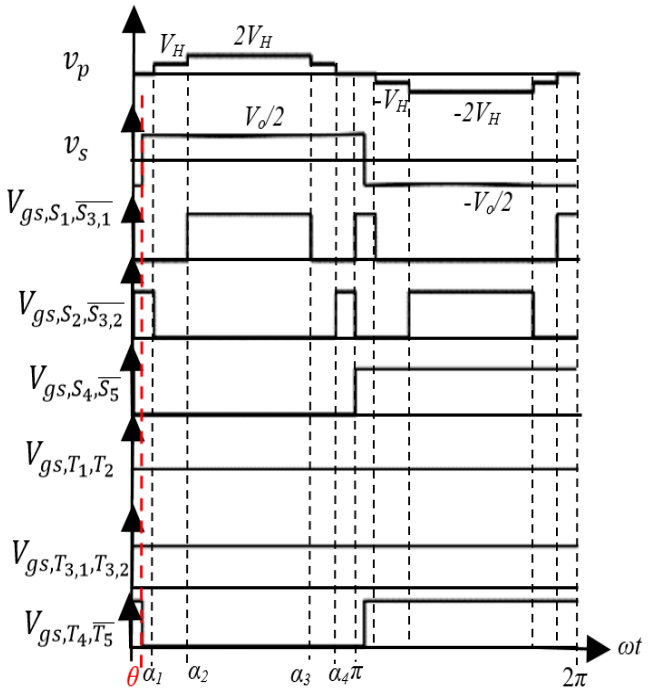
(b)


$2V_H$
v_p
θ
V_o
$-2V_H$
v_s
$-V_o$
$V_{gs,S_1,\overline{S_2}}$
$V_{gs,S_{3,1},S_{3,2}}$
$V_{gs,S_4,\overline{S_5}}$
$V_{gs,T_1,\overline{T_2}}$
$V_{gs,T_4,\overline{T_5}}$
ωt
α_2 $\beta_1+\theta$ α_3 π $\beta_2+\theta$ 2π

(c)


V_H
$2V_H$
v_p
θ
$-V_H$
$-2V_H$
$V_o/2$
v_s
$-V_o/2$
$V_{gs,S_1,\overline{S_{3,1}}}$
$V_{gs,S_2,\overline{S_{3,2}}}$
$V_{gs,S_4,\overline{S_5}}$
$V_{gs,T_1,\overline{T_{3,1}}}$
$(T_2,\overline{T_{3,2}})$
$V_{gs,T_2,\overline{T_{3,2}}}$
$(T_1,\overline{T_{3,1}})$
$V_{gs,T_4,\overline{T_5}}$
$(\overline{T_4},T_5)$
ωt
α_1 α_2 α_3 α_4 π 2π
$\beta_1+\theta$ $\beta_2+\theta$

(d)



(e)

Figure 2.20 Switching strategy of the proposed converter in open circuit faults of (a) S_1 or S_2 (b) S_1 and S_2 (c) $S_{3,1}$ or/and $S_{3,2}$ (d) T_1 or T_2 (e) T_1 and T_2

Table 2.3 shows the transferred active and reactive powers in the faulty operations of the proposed converter. The desired power in the isolated dc-dc converter is active power, while the reactive power increases the losses. For utilizing the maximum possible capacity of the converter, the amount of reactive power should be minimal. In addition, based on the loss analysis, the RMS values of the transformer's current and THD of the primary voltage should be minimized to obtain higher efficiency. There are seven control angles of $\alpha_1 - \alpha_4$, β_1, β_2, and θ in the normal operation of the proposed converter. The weighted cost function to calculate the control angles is considered as (2-59). Here, V_o^* is the desired output voltage and

P^* as a nonlinear constraint is the converter's power. The K_I, K_Q, and K_{VP} are constant values to normalize the cost function.

$$\begin{cases} \text{Min } (K_I I^2 + K_Q Q^2 + K_{Vp} H_{VP}^2) \\ \quad V_o = V_o^*, \quad P = P^* \\ 0 \le \alpha_1 \le \alpha_2 \le \alpha_3 \le \alpha_4 \le \pi; \\ 0 \le \beta_1 \le \beta_2 \le \pi;\ 0 < \theta < \dfrac{\pi}{2} \end{cases} \tag{2-59}$$

In (2-59), I is the peak value of the primary current of the transformer. Also, H_{VP} is the THD of the primary voltage that three dominant harmonics are considered.

$$I = \frac{\sqrt{(V_p)^2 + (V_s')^2 - 2V_p V_s' \cos(\theta)}}{\sqrt{2} L_s \omega} \tag{2-60}$$

$$H_{Vp} = \frac{\sqrt{{V_{p,3}}^2 + {V_{p,5}}^2 + {V_{p,7}}^2}}{V_p} \tag{2-61}$$

V_s' is the peak amount of voltage in (2-60). Also, $V_{p,i}$ for i equal to 3, 5, 7 are calculated as:

$$V_{p,i} = \frac{2V_H}{i\pi} \begin{bmatrix} \cos(i\alpha_1) + \cos(i\alpha_2) \\ -\cos(i\alpha_3) - \cos(i\alpha_4) \end{bmatrix}, \quad i = 3,5,7 \tag{2-62}$$

Table 2.3 Formulas of transferred active and reactive powers in the faulty conditions.

Operation	**Active power (P) and reactive power (Q)**
Scenario 1	$P = \frac{4nV_HV_o(\cos(\alpha_1)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\sin(\theta)$ $Q = \frac{4nV_HV_o(\cos(\alpha_1)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\cos(\theta) - \frac{4(V_H(\cos(\alpha_1)-\cos(\alpha_4)))^2}{\omega\pi^2L_s}$
Scenario 2	$P = \frac{8nV_HV_o(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\sin(\theta)$ $Q = \frac{8nV_HV_o(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\cos(\theta) - \frac{16{V_H}^2}{\omega\pi^2L_s}$
Scenario 3	$P = \frac{8nV_HV_o(\cos(\alpha_1)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\sin(\theta)$ $Q = \frac{8nV_HV_o(\cos(\alpha_1)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\cos(\theta) - \frac{16{V_H}^2}{\omega\pi^2L_s}$
Scenario 4	$P = \frac{2nV_HV_o(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\sin(\theta)$ $Q = \frac{2nV_HV_o(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4))(\cos(\beta_1)-\cos(\beta_2))}{\omega\pi^2L_s}\cos(\theta) - \frac{4(V_H(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4)))^2}{\omega\pi^2L_s}$
Scenario 5	$P = \frac{4nV_HV_o(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4))}{\omega\pi^2L_s}\sin(\theta)$ $Q = \frac{4nV_HV_o(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4))}{\omega\pi^2L_s}\cos(\theta) - \frac{4(V_H(\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4)))^2}{\omega\pi^2L_s}$

To obtain the formulas of current, active and reactive powers, and cost function in each faulty conditions, the control angles can be considered as Table 2.4. Based on this table, Table 2.3 is updated and active and reactive powers' formulas are resulted in the faulty conditions.

Table 2.4 Control angles in faulty conditions.

Operation	Control angles	Conditions
Scenario 1	$\alpha_1, \alpha_4, \beta_1, \beta_2, \theta$	$\alpha_2 = \alpha_3$
Scenario 2	β_1, β_2, θ	$\alpha_1 = 0$ $\alpha_2 = \alpha_3$ $\alpha_4 = \pi$
Scenario 3	$\alpha_2, \alpha_3, \beta_1, \beta_2, \theta$	$\alpha_1 = \alpha_2$ $\alpha_3 = \alpha_4$
Scenario 4	$\alpha_1 - \alpha_4, \beta_1, \beta_2, \theta$	-
Scenario 5	$\alpha_1 - \alpha_4, \theta$	$\beta_1 = 0$ $\beta_2 = \pi$

2.2.1 Comparison

The most common isolated dc-dc converter is dual-active bridge (DAB) converter [28] and is chosen to compare with the proposed converter. It is important to note that the DAB converter is a 3L-3L converter, while the proposed converter in normal operation is 5L-3L. A 3-level voltage waveform in the primary side of the converter has higher THD compared to a 5-level voltage resulting in increased core and winding losses of the transformer as well as conduction losses of the switches and diodes. The other advantage of the proposed converter in comparison to the DAB converter is fault-tolerance capability. In the DAB converter, if one of the switches on the primary or secondary sides has an open-circuit failure (OCF), the converter cannot continue operation. However, the proposed converter has fault-

tolerant capability under the OCF of switches S1, S2, S3,1, S3,2 from the primary side and switches T1, T2, T3,1, T3,2 from the secondary side without any changes to the blocking voltages of the remaining operating switches. The fault-tolerant capability of the proposed converter increases the reliability of the system. In high-frequency applications, high-frequency radiated and conducted emissions can lead to unacceptable responses. Fast switching generates the transient current (di/dt) and transient voltage (dv/dt) which is known as EMI. The main sources of the conducted EMI include the nonlinear behavior of semiconductor devices in power converters, parasitic elements and nonlinear control components that results in interference with other electronic systems [52]. Based on the electromagnetic compatibility (EMC) standards, an EMI filter is necessary to filter these noises, particularly in the case of using wide band gap devices with high conducted and radiated EMI emissions at high frequencies. Due to better estimate the EMI filter performance, Fast Fourier Transformation (FFT) technique is applied on the primary voltage to convert the time-domain waveform to frequency domain spectrum. Based on the FFT results of the primary voltage waveforms for the proposed and DAB converters, the THD of primary voltage in the proposed converter is lower. Hence, the proposed converter can have the smaller EMI filter. Table 2.5 summarizes this comparison.

Table 2.5 Comparison of the proposed converter and DAB.

Converter	THD of primary voltage	Core loss	Winding and conduction losses	EMI filter	Fault tolerant
DAB	Higher	Higher	Higher	Larger	No
Proposed	Lower	Lower	Lower	Smaller	Yes

Table 2.6 shows the comparison between the proposed converter and other high efficiency isolated dc-dc converters in the literature [27], [28], [53]-[60]. As is shown in this table, the efficiency of the proposed converter with the hard switching is comparable with other topologies with soft switching modulation.

Table 2.6 Comparison of the proposed converter and [27], [28], [53]-[60]

Topology	Voltage ratio	Efficiency (W/%)	Switches	Freq. (kHz)
Flyback [9]	300/300	750/96.4	Reverse-blocking	22.4
Resonant [34]	400/48	580/94	Si MOSFET	100
Resonant [35]	400/48	480/96	Si MOSFET	~ 100
Half bridge [36]	48/48	500/97	Si MOSFET	200
Half bridge [37]	380/24	600/96.6	Si MOSFET	-
Hybrid half bridge [38]	6k/400	10k/97	SiC MOSFET	40
Full bridge/T-type [39]	36/340	280/~94	Si MOSFET	32
Full bridge [8]	350	10k/96.8	Si IGBT	20
Triple Full bridge [40]	380/228/48	1.2k/~96.5	SiC MOSFET	50
Z-source full bridge [41]	140/300	550/95.9	Si MOSFET	20
Proposed	100/100	1k/96.2	SiC MOSFET	37.5

2.2.2 Simulation results

2.2.2.1 Normal operation

The proposed converter is simulated in PLECS software package based on circuit shown in Figure 2.2. 1. The simulation parameters are shown in Table 2.7. 1.2kV SiC carbide MOSFETs are used and thermal characteristics of them are modelled.

Table 2.7 Simulation parameters.

Parameters	Definition	Values
V_H	Each Dc-link of primary side	500 V
f_c	Fundamental frequency	5 kHz[1]
f_s	Switching frequency	41 kHz
C_H	Input DC-links capacitors	10 uF
C_L	Output filter capacitor	20 uF[1]
L_s	Series inductance	1 mH[1]
m	Modulation index	0.95
n	Transformer winding ratio	1
R_o	Output load	100 Ω

[1]For 41kHz square wave, these values are 41kHz, 2uF and 0.1mH, respectively.

2.2.2.2 Applying PWM modulation

In this simulation, θ is 54°. The operation of the proposed converter is shown in Figure 2.21. The voltage of the first leg to negative rail (Vp1) is a 3-level voltage with the maximum level of 1 kV and the produced voltage by the second leg to negative rail (Vp2) is 2-level voltage with the maximum level of 1 kV. Therefore, the 5-level voltage with the maximum level of 1 kV is produced at the primary side

of the transformer (Vp). Also, the 3-level voltage with the maximum level of 1285.88 V is produced at the secondary side of transformer. The primary current (Ip) with the maximum amount of 34.52 A is produced at the primary side of the transformer. The input and output voltages and currents of the proposed converter are shown in Figure 2.22. Based on this figure, the average input currents are 16.58 A and 16.58 A with the dc-link of 500 V each and the average current and voltage of the output are 12.86 A and 1285.88 V, respectively. Therefore, the input and output powers are 16581 W and 16535 W, respectively. The efficiency is 99.72%. The gate pulses of switches' S_1, S_2, $S_{3,1}$, $S_{3,2}$, S_4, S_5, T_1, T_2, T_4 and T_5 are shown in Figure 2.23. It is shown that switches S_4 and S_5 are low frequency switches, while others are high-frequency switches.

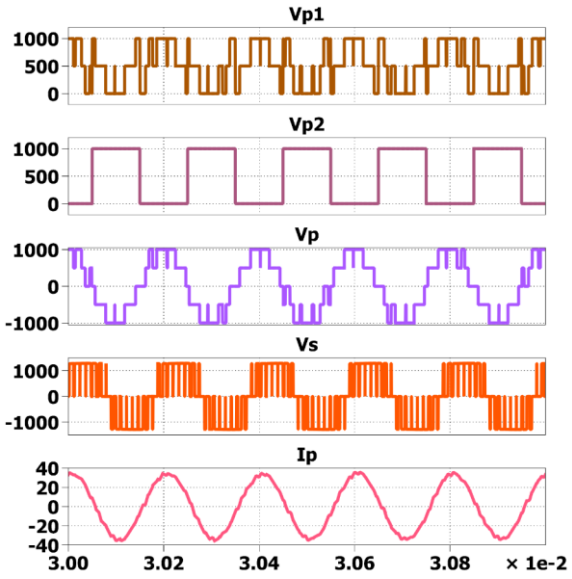
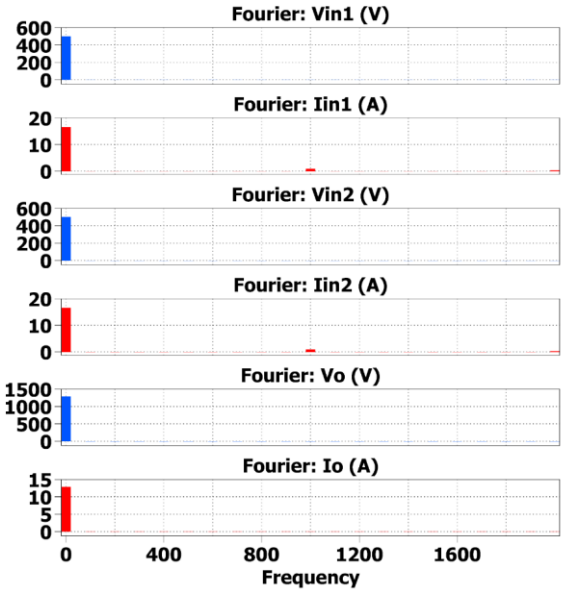


Figure 2.21 Operation of the proposed converter in PWM modulation.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	100	200	300	400	500
Fourier: Vin1 (V)						
v_in1	500	6.56443e-12	1.8946e-12	2.79782e-12	1.92378e-12	3.11695e-12
Fourier: Iin1 (A)						
i_H1	16.5809	0.00167856	0.00087047	0.000586138	0.000442889	0.000357399
Fourier: Vin2 (V)						
v_in2	500	6.56443e-12	1.8946e-12	2.79782e-12	1.92378e-12	3.11695e-12
Fourier: Iin2 (A)						
i_H2	16.5815	0.00153918	0.000796244	0.000532654	0.000398289	0.000316385
Fourier: Vo (V)						
v_o	1285.89	0.124174	0.0643192	0.0431731	0.0324579	0.0259953
Fourier: Io (A)						
i_o	12.8589	0.00124174	0.000643192	0.000431731	0.000324579	0.000259953

(b)

Figure 2.22 Analysis of the input and output voltages and currents in PWM modulation.

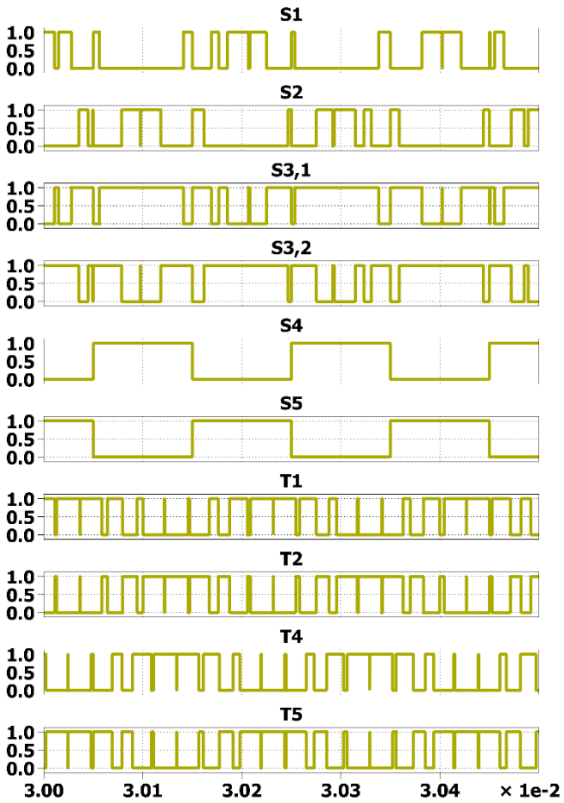


Figure 2.23 Gate pulses in PWM modulation.

2.2.2.3 Applying phase-shifted modulation

In the first step, it is supposed that fundamental frequency is 5 kHz. The degrees of α_1, α_2, α_3 and θ are 13.2°, 41°, 0° and 35°. The operation of the proposed converter is shown in Figure 2.24. The voltage of the first leg to negative rail (Vp1) is a 3-level voltage with the maximum level of 1 kV and the produced voltage by the second leg to negative rail (Vp2) is 2-level voltage with the maximum level of 1 kV. Therefore, the 5-level voltage with the maximum level of 1 kV is produced at the primary side of the transformer (Vp). Also, the 3-level voltage with the

maximum level of 1303.53 V is produced at the secondary side of transformer. The primary current (Ip) with the maximum amount of 31.96 A is produced at the primary side of the transformer. The input and output voltages and currents of the proposed converter are shown in Figure 2.25. Based on this figure, the average input currents are 17.03 A and 17.04 A with the dc-link of 500 V each and the average current and voltage of the output are 13.04 A and 1303.53 V, respectively. Therefore, the input and output powers are 17036.7 W and 16992 W, respectively. The efficiency is 99.74%. The gate pulses of switches' S_1, S_2, $S_{3,1}$, $S_{3,2}$, S_4, S_5, T_1, T_2, T_4 and T_5 are shown in Figure 2.26. It is shown that switches S_4 and S_5 are low frequency switches, while others are high-frequency switches.

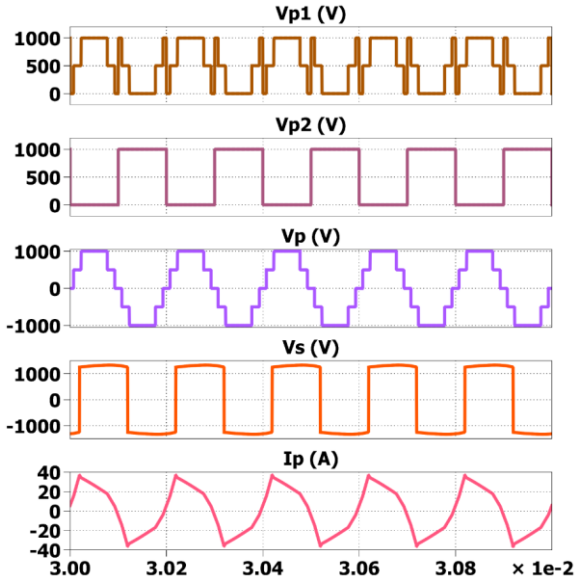
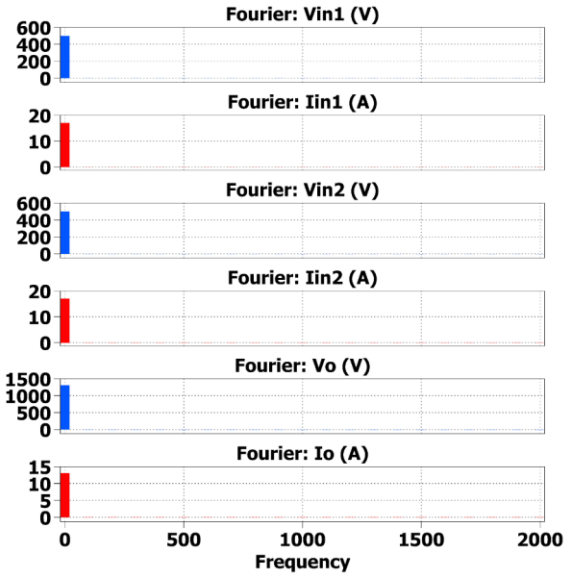


Figure 2.24 Operation of the proposed converter in 5 kHz phase-shifted modulation.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	100	200	300	400	500
Fourier: Vin1 (V)						
v_H1	500	2.69571e-12	3.10012e-12	5.4981e-12	1.82375e-12	1.62605e-12
Fourier: Iin1 (A)						
i_H1	17.0293	0.00331538	0.00170625	0.00115862	0.000887878	0.000729131
Fourier: Vin2 (V)						
v_H2	500	2.69571e-12	3.10012e-12	5.4981e-12	1.82375e-12	1.62605e-12
Fourier: Iin2 (A)						
i_H2	17.0442	0.0035208	0.00184694	0.00129112	0.00102533	0.000875446
Fourier: Vo (V)						
v_o	1303.53	0.00176281	0.00176507	0.00176886	0.00177418	0.00178108
Fourier: Io (A)						
i_o	13.0353	1.76281e-5	1.76507e-5	1.76886e-5	1.77418e-5	1.78108e-5

(b)

Figure 2.25 Analysis of the input and output voltages and currents in 5 kHz phase-shifted modulation.

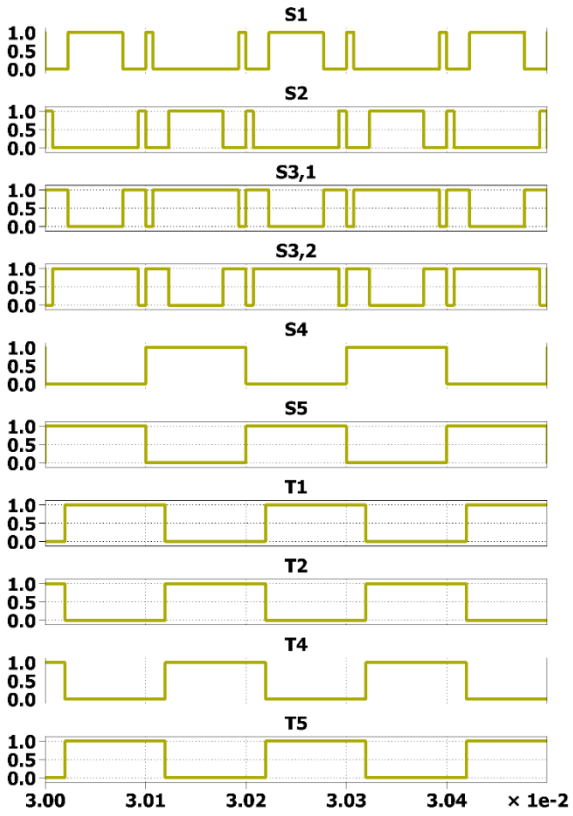


Figure 2.26 Gate pulses in 5 kHz phase-shifted modulation.

In the second step, it is supposed that fundamental frequency is 41 kHz. The degrees of α_1, α_2, α_3 and θ are 13.2°, 41°, 0° and 27°. The operation of the proposed converter is shown in Figure 2.27. The voltage of the first leg to negative rail (Vp1) is a 3-level voltage with the maximum level of 1 kV and the produced voltage by the second leg to negative rail (Vp2) is 2-level voltage with the maximum level of 1 kV. Therefore, the 5-level voltage with the maximum level of 1 kV is produced at the primary side of the transformer (Vp). Also, the 3-level voltage with the maximum level of 1269.03 V is produced at the secondary side of transformer.

The primary current (Ip) with the maximum amount of 32.20 A is produced at the primary side of the transformer. The input and output voltages and currents of the proposed converter are shown in Figure 2.28. Based on this figure, the average input currents are 16.15 A and 16.15 A with the dc-link of 500V each and the average current and voltage of the output are 12.69 A and 1269.03 V, respectively. Therefore, the input and output powers are 16153 W and 16104 W, respectively. The efficiency is 99.7%. The gate pulses of switches' S_1, S_2, $S_{3,1}$, $S_{3,2}$, S_4, S_5, T_1, T_2, T_4 and T_5 are shown in Figure 2.29. It is shown that switches S_4 and S_5 are low frequency switches, while others are high-frequency switches.

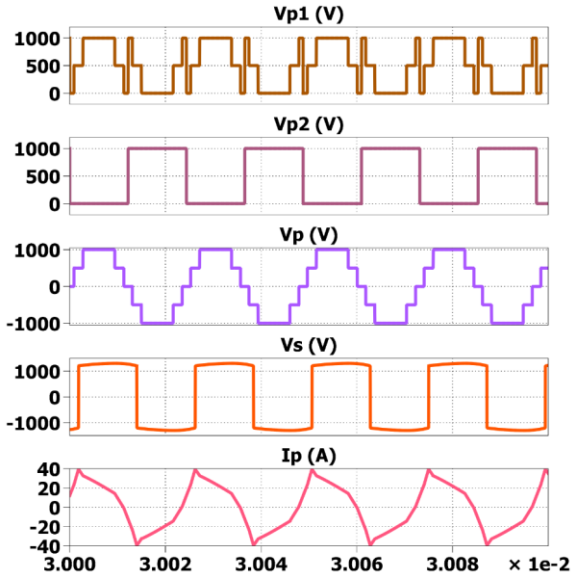
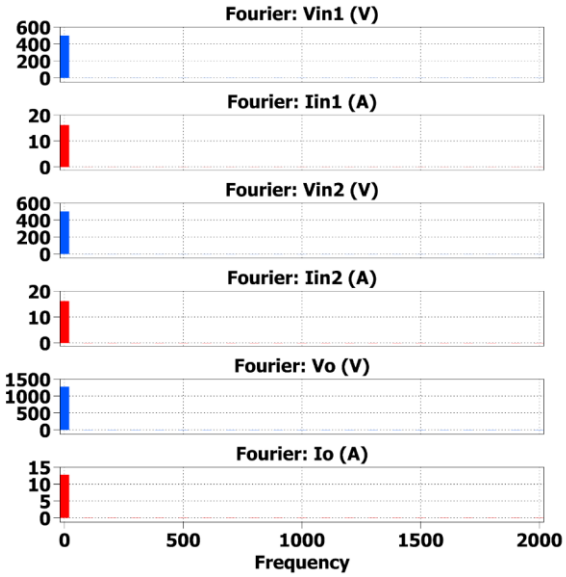


Figure 2.27 Operation of the proposed converter in 41 kHz phase-shifted modulation.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	100	200	300	400	500
Fourier: Vin1 (V)						
v_H1	500	3.28316e-12	5.51371e-12	1.30977e-12	3.32335e-12	1.32657e-12
Fourier: Iin1 (A)						
i_H1	16.1531	2.82145e-9	1.44275e-9	4.69743e-10	9.77675e-10	2.07665e-10
Fourier: Vin2 (V)						
v_H2	500	3.28316e-12	5.51371e-12	1.30977e-12	3.32335e-12	1.32657e-12
Fourier: Iin2 (A)						
i_H2	16.1531	6.69312e-10	9.09055e-10	5.15447e-10	1.06238e-9	4.24475e-10
Fourier: Vo (V)						
v_o	1269.03	2.27144e-9	2.7047e-9	2.32494e-9	4.53747e-9	3.49299e-10
Fourier: Io (A)						
i_o	12.6903	2.27509e-11	2.71331e-11	2.3239e-11	4.52997e-11	3.32085e-12

(b)

Figure 2.28 Analysis of the input and output voltages and currents in 41 kHz phase-shifted modulation.

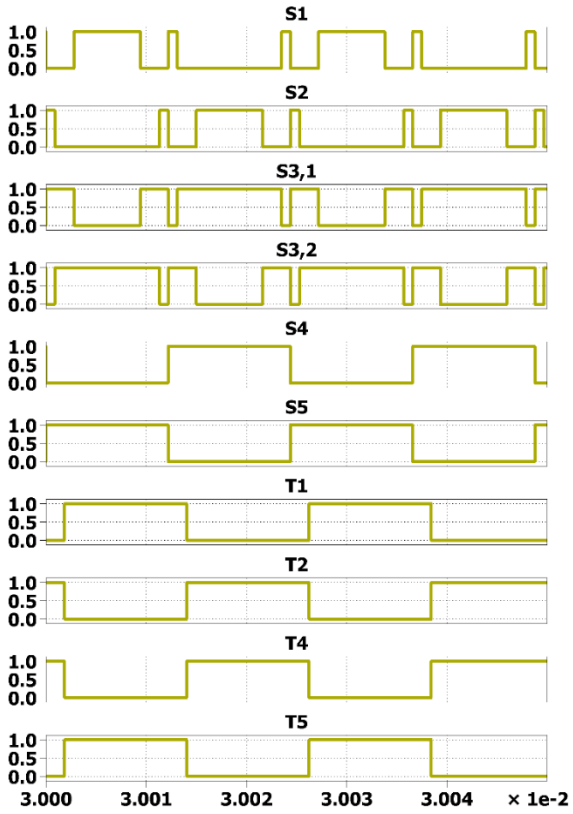


Figure 2.29 The gate pulses in 41 kHz phase-shifted modulation.

2.2.2.4 Applying hybrid modulation

In this simulation, θ and α are 55° and 0°. The operation of the proposed converter is shown in Figure 2.30. The voltage of the first leg to negative rail (Vp1) is a 3-level voltage with the maximum level of 1 kV and the produced voltage by the second leg to negative rail (Vp2) is 2-level voltage with the maximum level of 1 kV. Therefore, the 5-level voltage with the maximum level of 1 kV is produced at the primary side of the transformer (Vp). Also, the 3-level voltage with the maximum level of 1260.12 V is produced at the secondary side of transformer. The

primary current (Ip) with the maximum amount of 4.039 A is produced at the primary side of the transformer. The input and output voltages and currents of the proposed converter are shown in Figure 2.31. Based on this figure, the average input currents are 1.69 A and 1.69 A with the dc-link of 500 V each and the average current and voltage of the output are 1.26 A and 1260.12 V, respectively. Therefore, the input and output powers are 1686.14 W and 1587.8 W, respectively. The efficiency is 94.16%. The gate pulses of switches' S_1, S_2, $S_{3,1}$, $S_{3,2}$, S_4, S_5, T_1, T_2, T_4 and T_5 are shown in Figure 2.32. It is shown that switches S_4 and S_5 are low frequency switches, while others are high-frequency switches.

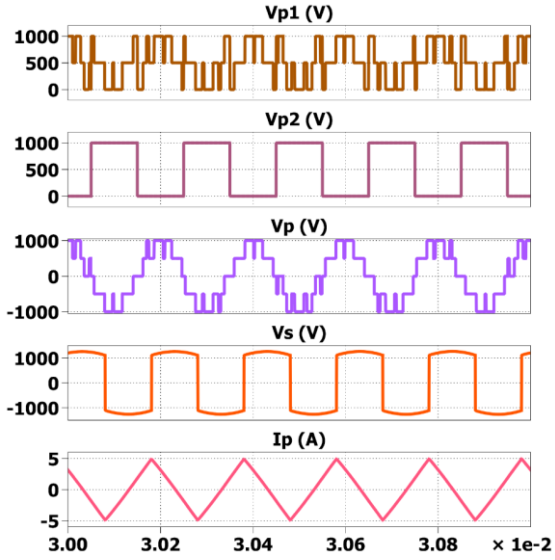
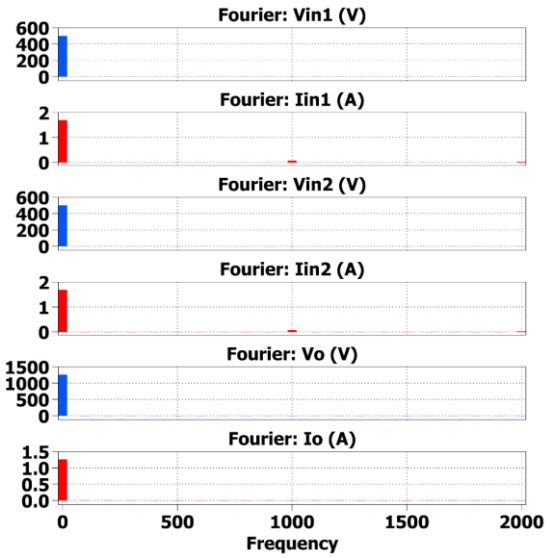


Figure 2.30 Operation of the proposed converter in the hybrid modulation.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	100	200	300	400	500
Fourier: Vin1 (V)						
v_H1	500	2.57709e-12	5.87034e-12	3.99999e-12	1.16185e-12	1.21499e-12
Fourier: Iin1 (A)						
i_H1	1.68614	0.00722545	0.00364781	0.00244	0.00183593	0.00147507
Fourier: Vin2 (V)						
v_H2	500	2.57709e-12	5.87034e-12	3.99999e-12	1.16185e-12	1.21499e-12
Fourier: Iin2 (A)						
i_H2	1.68634	0.00718955	0.0036235	0.00241616	0.0018089	0.00144203
Fourier: Vo (V)						
v_o	1260.12	5.38263	2.71488	1.81286	1.36041	1.08861
Fourier: Io (A)						
i_o	1.26012	0.00538263	0.00271488	0.00181286	0.00136041	0.00108861

(b)

Figure 2.31 Analysis of the input and output voltages and currents in the hybrid modulation.

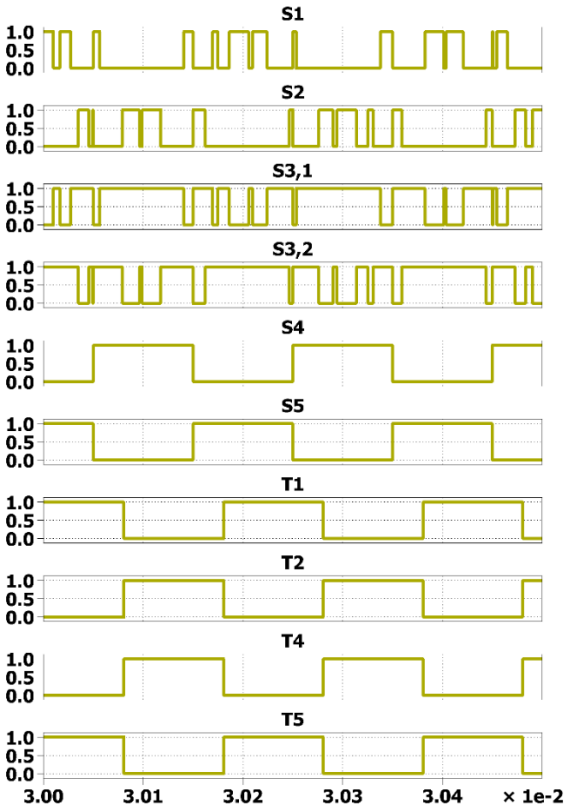


Figure 2.32 Gate pulses in the hybrid modulation.

Table 2.8 summarizes the simulation results for the three proposed modulation methods.

Table 2.8 Summarized characteristics of proposed three modulation methods.

Method	Switching freq.	Fund. freq.	Input1	Input 2	Output	Effi. %
PWM	41kHz	5kHz	V_{in1}=500V I_{in1}=16.59A P_{in1}=8290.4W	V_{in2}=500V I_{in2}=16.58A P_{in2}=8290.6W	V_o=1285.88V I_o=12.86A P_o=16535W	99.72
Phase-shifted	-	5kHz	V_{in1}=500V I_{in1}=17.03A P_{in1}=8514.6W	V_{in2}=500V I_{in2}=17.04A P_{in2}=8522.1W	V_o=1303.53V I_o=13.04A P_o=16992W	99.74
	-	41kHz	V_{in1}=500V I_{in1}=16.15A P_{in1}=8076.5W	V_{in2}=500V I_{in2}=16.15A P_{in2}=8076.5W	V_o=1269.03V I_o=12.69A P_o=16104W	99.7
Hybrid	41kHz	5kHz	V_{in1}=500V I_{in1}=1.69A P_{in1}=843.07W	V_{in2}=500V I_{in2}=1.69A P_{in2}=843.07W	V_o=1260.12V I_o=1.26A P_o=1587.8W	94.1

2.2.2.5 Fault tolerance operation

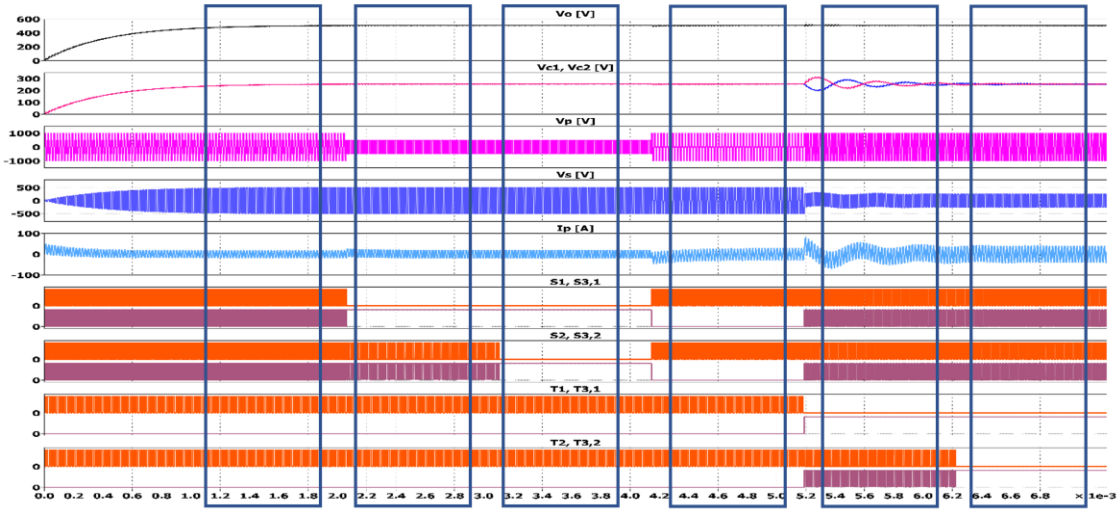
1.2kV SiC MOSFET power modules from Wolfspeed are used and their thermal characteristics have been modelled in PLECS. Each input dc-links (V_H), fundamental frequency, transformer turn ratio and output load are 500 V, 48 kHz, 1 and 50 Ω, respectively. The operation of the proposed converter is shown in Figure 2.33(a). In this figure, the waveforms from top to bottom are output voltage, output capacitors' voltages, primary voltage, secondary voltage, primary current, pulses of S_1 and $S_{3,1}$, pulses of S_2 and $S_{3,2}$, pulses of T_1 and $T_{3,1}$, and pulses of T_2 and $T_{3,2}$. This figure includes sections A-F for different operations of the proposed converter. The section A (mode 1) shows the normal operation of the converter that is zoomed in Figure 2.33(b). The primary converter produces 5-level voltage with the maximum level of 1 kV. For calculating the optimized angles, it is considered that output voltage is regulated at 500 V. So, the secondary converter has a 3-level voltage

waveform with the maximum level of 500 V. Sections B, C, D, E and F show the operation of the converter under open-circuit faults on switches S_1 (mode 2), both S_1 and S_2 (mode 3), both $S_{3,1}$ and $S_{3,2}$ (mode 4), T_1 (mode 5) and both T_1 and T_2 (mode 6), respectively, that the circuit of each is shown in Figure 2.34. The open-circuit fault on S_2 is the same as S_1, so it hasn't been shown in this figure. These sections are zoomed in Figure 2.33(c)-(g), respectively. In section B and C, both the primary and secondary are close to 2-level voltages with the maximum level of 500 V. In section D, the primary voltage is 3-level and secondary is 2-level.

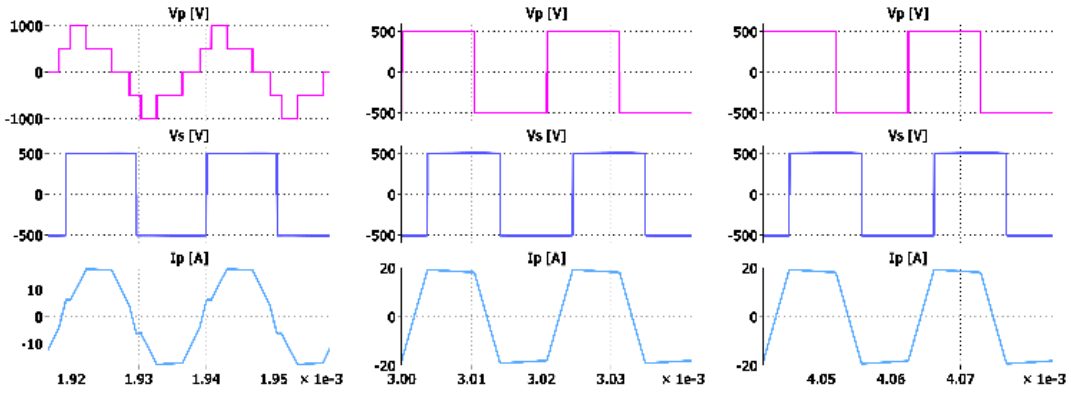
In sections E and F, the primary voltage is 5-level and secondary is 2-level. The important point in this figure is that this converter can properly regulate the output voltage at 500 V in normal operation and each faulty condition. The calculated optimized angles in these sections are listed in Table 2.9.

Table 2.9 Calculated optimized angles.

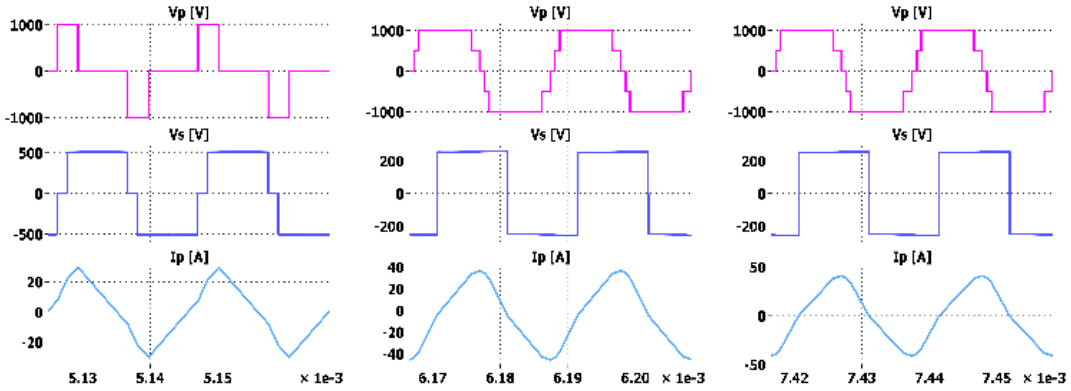
Section	**Optimized angles (degree)**						
	α_1	α_2	α_3	α_4	β_1	β_2	θ
A	10	42	96	178	0.5	179.5	45
B	0.375	90	90	179.96	0.03	179.97	90
C	0	90	90	180	0.21	179.79	90
D	21.56	21.56	75	75	10	170	44.96
E	10.99	22.5	157.5	178	0.07	179.78	90
F	10.99	22.5	157.5	178	0	180	90


Vo [V]
Vc1, Vc2 [V]
Vp [V]
Vs [V]
Ip [A]
S1, S3,1
S2, S3,2
T1, T3,1
T2, T3,2
× 1e-3

(a)

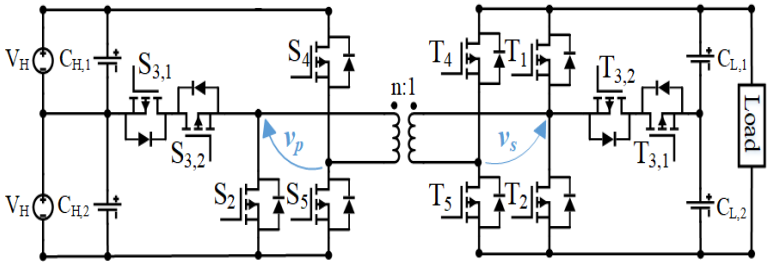

Vp [V]
Vs [V]
Ip [A]
× 1e-3

(b) (c) (d)

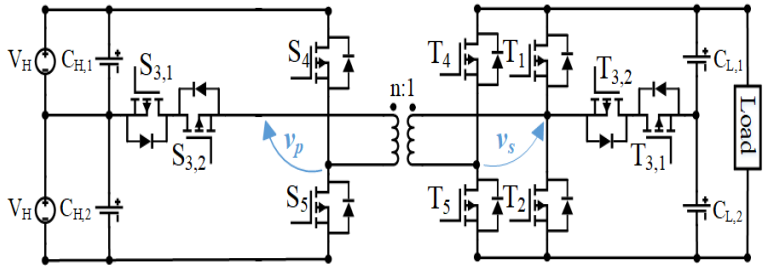


(e) (f) (g)

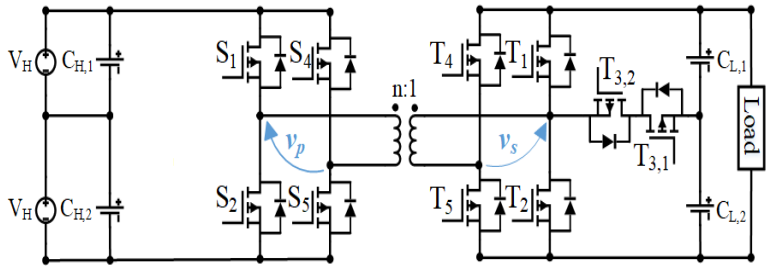
Figure 2.33 (a) Operation of the proposed converter (b) normal operation; open circuit fault on (c) switch S_1 (d) switches S_1 and S_2 (e) switches $S_{3,1}$ and $S_{3,2}$ (f) switch T_1 (g) switches T_1 and T_2.



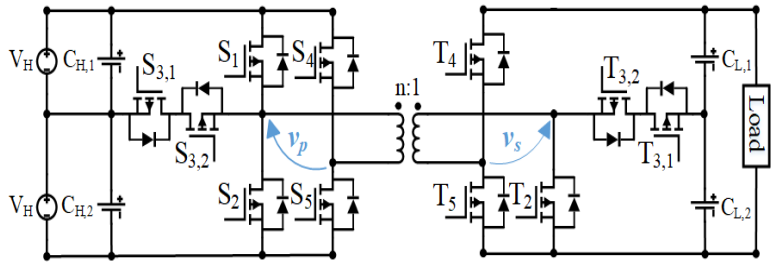
(a)



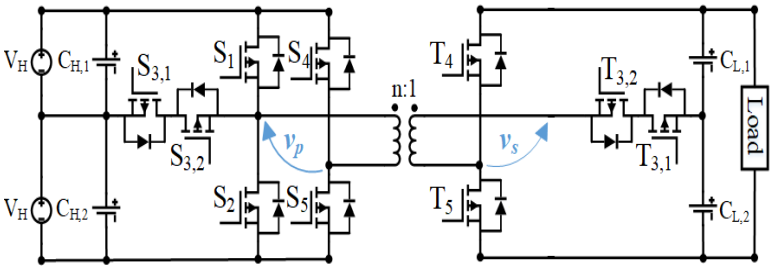
(b)



(c)



(d)



(e)

Figure 2.34 Schematic of the proposed converter in (a) section B (mode 2) (b) section C (mode 3) (c) section D (mode 4) (d) section E (mode 5) (e) section F (mode 6).

2.2.3 Experimental results

2.2.3.1 Normal operation

A scaled down prototype of the proposed converter has been built (Figure 2.35) to obtain the experimental results. The TMS320F28335 digital signal

processor (DSP) is used to produce the gate pulses for switches. A high-frequency transformer with the core of AMCC-50 of Powerlite series from Metglas has been built and used for this converter. The fundamental frequency is 37.5 kHz, however the switches S_1, S_2, $S_{3,1}$, and $S_{3,2}$ are operating at approximately twice this frequency (75 kHz). In the switching method shown in Figure 2.8(c), in zero and π, all six switches in the primary side are switching creating higher rings in the primary voltage in these two points. To avoid that, the sequence of switching is changed in the experiments. In the revised switching method, the zero voltage of primary in interval $\alpha_4 - \alpha_5$ is generated by turning on S_2, $S_{3,1}$, S_5, while in intervals $0 - \alpha_1$and $\alpha_8 - 2\pi$, it is generated by S_1, $S_{3,2}$, S_4. This revised switching method as well as generated primary voltage is shown in Figure 2.36(a). In this figure, the waveforms from top to bottom are the primary voltage and pulses of S_1, $S_{3,1}$, S_2, $S_{3,2}$, S_4, and S_5, respectively. The total dead time is 450 ns. An interface board is designed to convert the DSP pulses of 0 V and 3.3 V to -4 V and 20 V, to turn off and fire the MOSFETs, respectively. There is a trade-off between switching losses and switching rings. In this work, a two-level turn off method for SiC MOSFETs are used to control the voltage's rings of dc-link. During turn off, the gate voltage first drops from 20 V to 6 V in 150 ns and remains there for duration of 250 ns and after that, it drops to -4 V in 50 ns. It is shown in Figure 2.36(b).

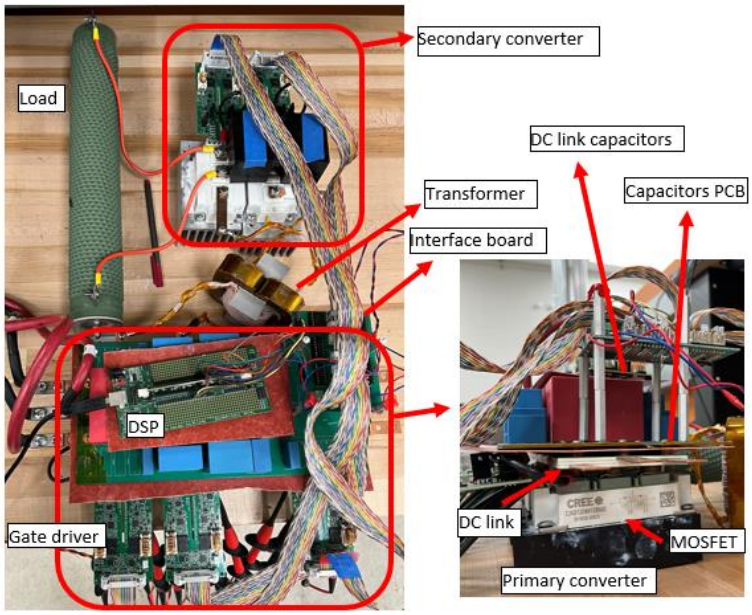
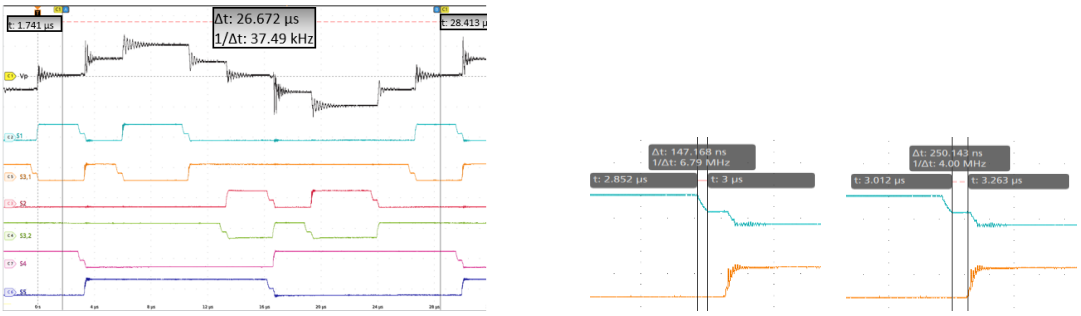


Figure 2.35 Experimental prototype.



(a) (b)

Figure 2.36 (a) Revised switching strategy (b) two-level turning off method.

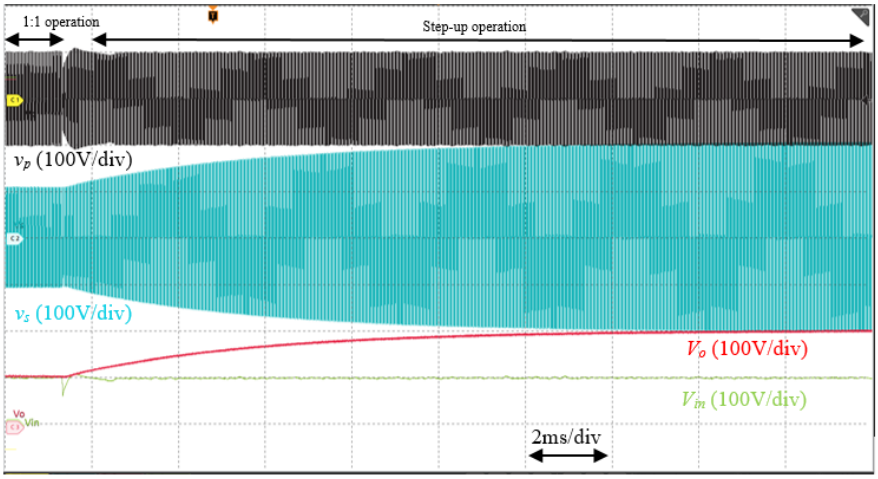
The operation of the proposed converter is shown in Figure 2.37. Table 2.10 shows the component values used in the experimental.

Table 2.10 Components values used in the experimental.

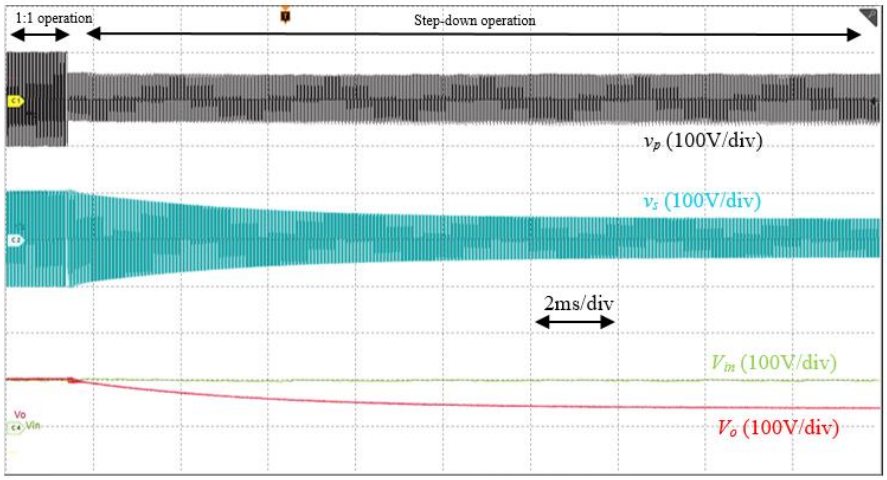
Parameter	Definition	Value
$2V_H$	Full dc-link	100 V
Load	Output load	47 Ω
L_s	Leakage inductance of transformer	10 µH
f_c	Fundamental frequency	37.5kHz
n	Turn ratio of transformer	1
C_H	Input capacitors	50 µF
S_i & T_i,	Switches	CAS120M12BM2
Heatsink	Aavid Thermalloy (extrusion profile 74765)	

Figure 2.37(a) shows the dynamic step-up operation of the proposed converter. First, this converter produces regulated 100 V at the output (referred to herein as 1:1 mode). In this mode, the primary voltage v_p is the 5-level voltage with the maximum level of 100 V and the secondary voltage v_s is the 3-level voltage with the maximum level of 100 V. The steady-state of 1:1 mode is shown in Figure 2.38(a). The control angles of α_1, α_2, α_3, α_4, β_1, β_2, and θ are 18˚, 45˚, 135˚, 162˚, 18˚, 162˚, and 27˚, respectively. The converter efficiency is 96.2%. As shown in Figure 2.37(a), the operation of the proposed converter is changed from 1:1 mode to step-up mode. In the step-up mode, the primary voltage is the 3-level voltage with the maximum level of 100 V and the secondary voltage is the 3-level voltage with the maximum level of 200 V. The output voltage is regulated at 200 V. The steady state operation of the converter in step-up mode is shown in Figure 2.38(b). The control angles of α_1, α_4, β_1, β_2, and θ are 27˚, 153˚, 27˚, 153˚, and 45˚, respectively.

In this mode, α_2 and α_3 are equal to α_1 and α_4, respectively. The efficiency is 95.1%. Figure 2.37(b) shows the dynamic step-down operation of the proposed converter. Again, at the beginning, it is in 1:1 mode. Then, the operation is changed to step-down mode. In the step-down mode, the primary and secondary voltages are the 3-level voltages with the maximum level of 50 V. The output voltage is regulated at 50 V. The steady-state operation of the converter in step-down mode is shown in Figure 2.38(c). The control angles of α_1, α_4, β_1, β_2, and θ are 45˚, 135˚, 22.5˚, 157.5˚, and 31.5˚, respectively. In this mode, α_2 and α_3 are equal and cancel out each other. The efficiency is 95.5%. Therefore, the proposed converter could be able to operate at step-up and step-down modes by generating 5-level and 3-level voltages at the primary side of the transformer. Table 2.11 summarizes the experimental results of Figure 2.38.

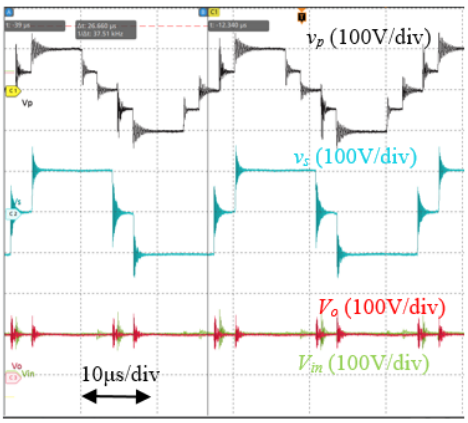


(a)

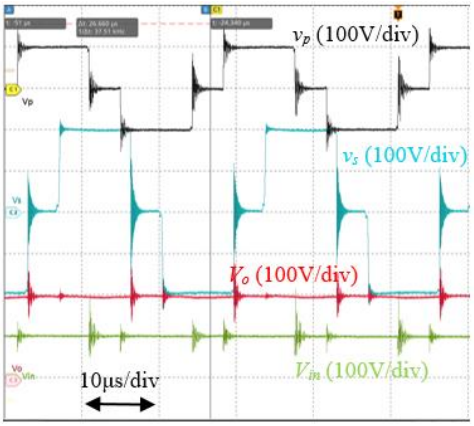


(b)

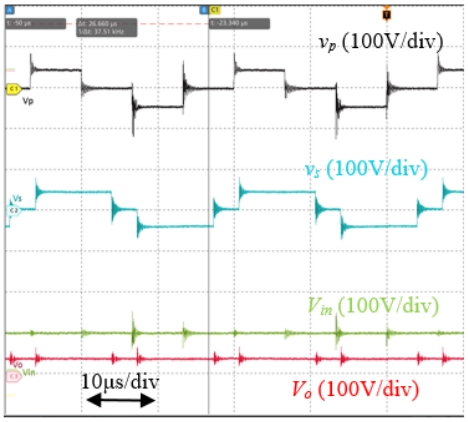
Figure 2.37 Dynamic experimental results of the proposed converter in (a) 1:1 mode to step-up mode (b) 1:1 mode to step-down mode; from top to bottom: the primary voltage (v_p), the secondary voltage (v_s), total dc-link (V_{in}), and output voltage (V_o).



(a)



(b)



(c)

Figure 2.38 Steady state experimental results of the proposed converter in (a) 1:1 operation, (b) step-up operation, and (c) step-down operation.

Table 2.11 Details of Figure 2.38.

Figure	v_p	v_s	V_o	$\alpha_1, \alpha_2, \alpha_3, \alpha_4, \beta_1, \beta_2, \theta$	**Eff. (%)**
Figure 2.38(a)	5-level ML*:100V	3-level ML:100V	100V	18º, 45º, 135º, 162º, 18º, 162º, 27º	96.2
Figure 2.38(b)	3-level ML:100V	3-level ML:200V	200V	27º, 27º, 153º, 153º, 27º, 153º, 45º	95.1
Figure 2.38(c)	3-level ML:50V	3-level ML:50V	50V	45º, 90º, 90º, 135º, 22.5º, 157.5º, 31.5º	95.5

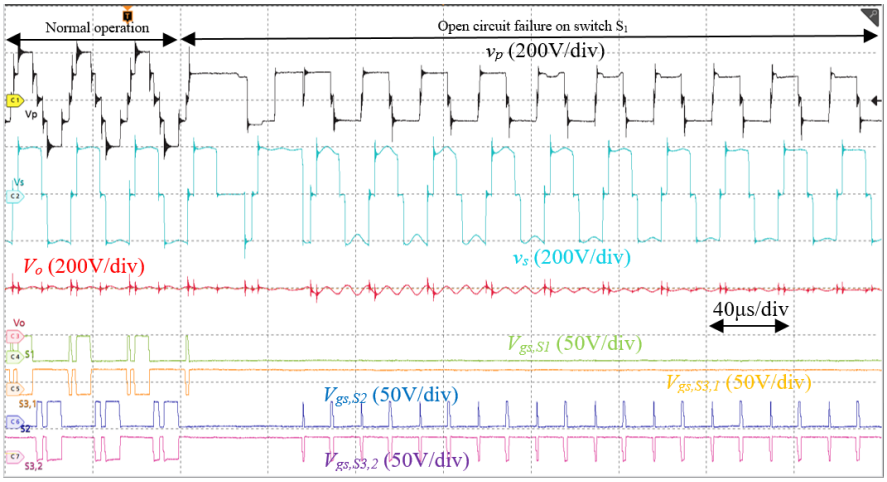
* Maximum level

2.2.3.2 Fault tolerance operation

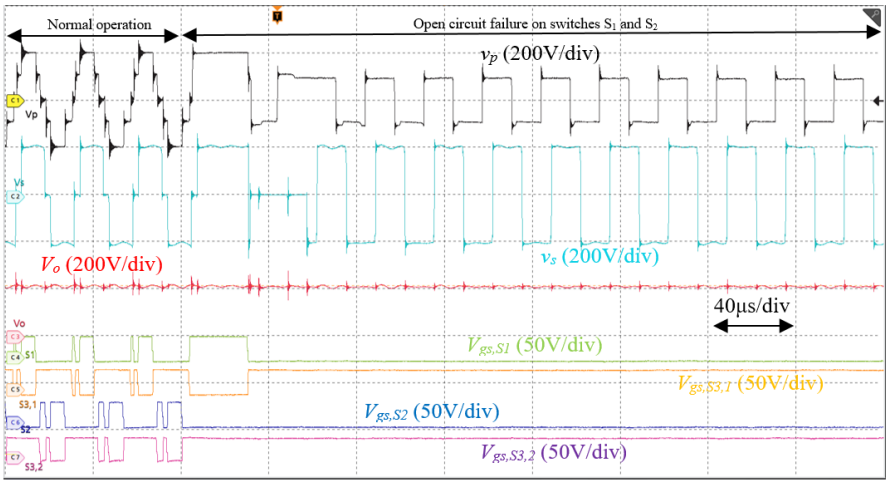
The dynamic operation of the proposed fault-tolrent converter is shown in Figure 2.39. The total dc-link and output load are 200 V and 47 Ω, respectively. Figure 2.39(a) shows the dynamic operation of the proposed converter when an open-circuit failure (OCF) happens on switch S_1. In the normal operation (first three cycles), the 5-level voltage with the maximum level of 200 V is generated at the primary side of the

transformer (v_p). The secondary voltage is 3-level voltage with the maximum level of 200 V (v_s). The regulated output voltage is 200 V (V_o). The steady-state of normal operation is shown in Figure 2.40(a). The normal switching method is applied in this step and the control angles of α_1, α_2, α_3, α_4, β_1, β_2, θ are 18˚, 45˚, 135˚, 162˚, 18˚, 162˚, 27˚, respectively. The converter efficiency is 96.11%. As it is shown in Figure 2.39(a), at the end of cycle third, the gate pulse of S_1 is changed to zero to analyze the operation of the converter in the case of OCF of this switch. By applying the post-fault switching method of scenario 1, the primary voltage is the 3-level voltage with the maximum level of 100 V and the secondary voltage is the 3-level voltage with the maximum level of 200 V. The output regulated voltage remains at 200 V. The steady-state operation of the converter in the OCF of S_1 is shown in Figure 2.40(b). The control angles of α_1, α_4, β_1, β_2, θ are 9˚, 171˚, 18˚, 162˚, 63˚, respectively. The efficiency is 95.32%. The operation of the converter in the case of OCF of S_2 is similar to S_1, so it hasn't been shown here. Figure 2.39(b) shows the dynamic operation of the proposed converter when an OCF happens on both switches S_1 and S_2. The normal operation is same. Again, at the end of cycle third, the gate pulse of both S_1 and S_2 are changed to zero. The post-fault switching method of scenario 2 is applied and then, the primary voltage is the 2-level voltage with the maximum level of 100 V and the secondary voltage is the 3-level voltage with the maximum level of 200 V. The output regulated voltage remains at 200 V. The steady-state operation of the converter in this faulty condition is shown in Figure 2.40(c). The control angles of β_1, β_2, θ are 0˚, 180˚, 63˚,

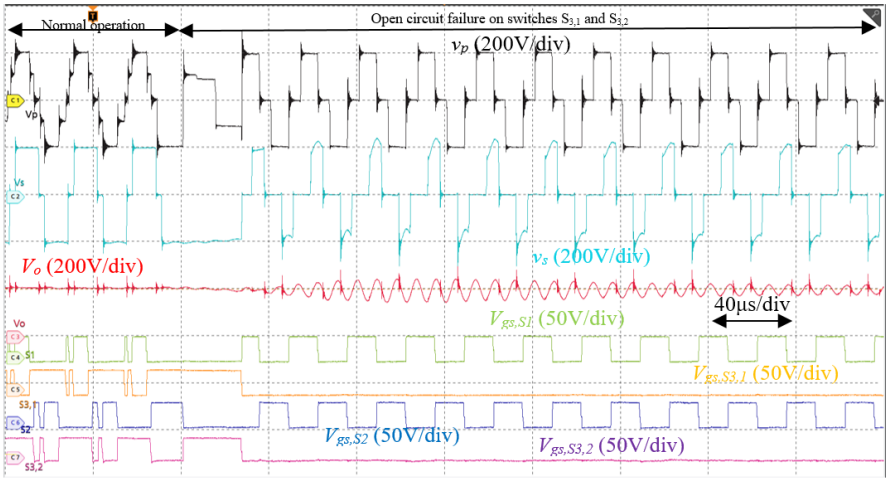
respectively. The efficiency is 95.62%. Finally, the dynamic operation of the proposed converter when an OCFs happens on both switches $S_{3,1}$ and $S_{3,2}$, is shown in Figure 2.39(c). The normal operation is same. At the end of cycle third, the gate pulse of both $S_{3,1}$ and $S_{3,2}$ are changed to zero. By applying the post-fault switching method of scenario 3, this converter can produce 3-level voltage with the maxmimum level of 200 V at primary and secondary sides. Again, the output regulated voltage remains at 200 V. The steady-state operation of the converter in this faulty condition is shown in Figure 2.40(d). The control angles of α_2, α_3, β_1, β_2, θ are 108˚, 180˚, 54˚, 126˚, 9˚, respectively. The efficiency is 95.9%. The operation of the converter in the case of OCF of secondary is similar to primary side. Therefore, the proposed converter could be able to keep the output voltage unchanged in any mentioned faulty conditions by applying the post-fault switching methods and modifying the control angles.



(a)



(b)



(c)

Figure 2.39 Experimental results of the dynamic operations of the proposed converter in OCFs of (a) switch S_1 (b) switches S_1 and S_2 (c) switches $S_{3,1}$ and $S_{3,2}$; from top to bottom, primary voltage, secondary voltage, regulated output voltage, gate pulses of S_1, $S_{3,1}$, S_2, and $S_{3,2}$, respectively.

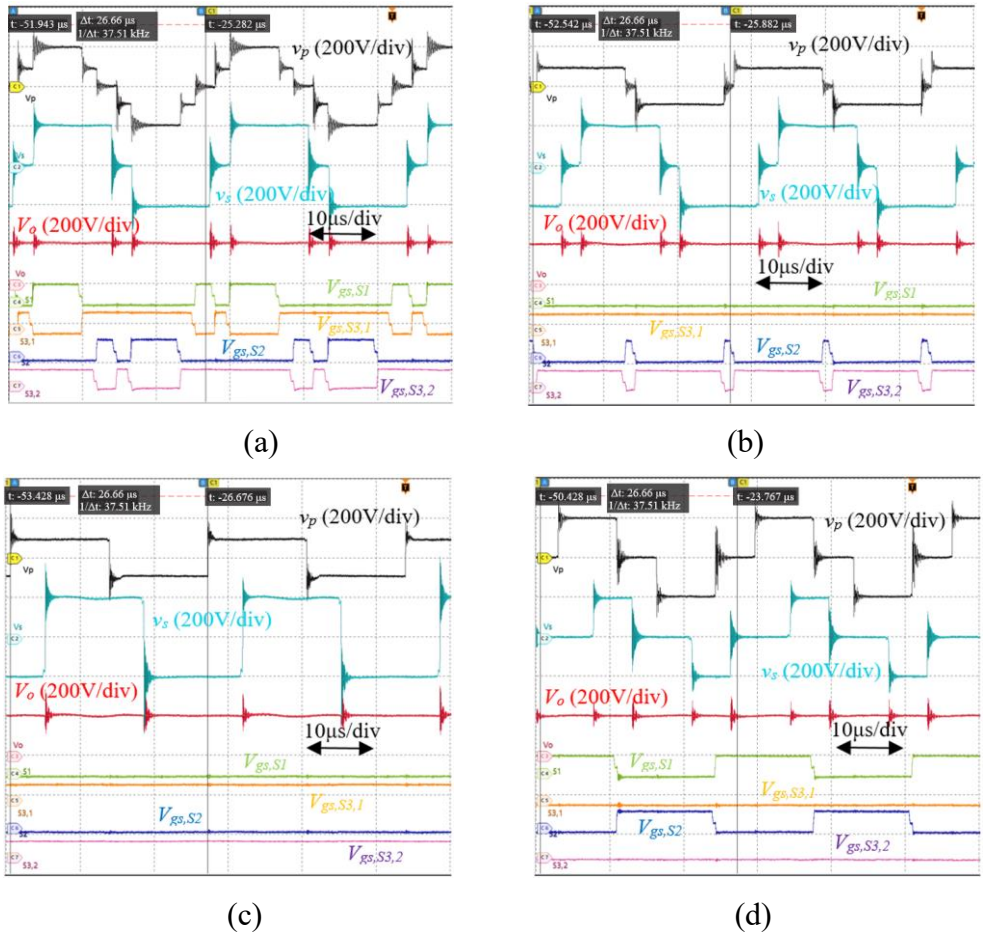


Figure 2.40 Experimental results of the steady-state operations of the proposed converter in (a) normal operation and OCF of (b) switch S_1 (c) switches S_1 and S_2 (d) switches $S_{3,1}$ and $S_{3,2}$; from top to bottom, primary voltage, secondary voltage, regulated output voltage, gate pulses of S_1, $S_{3,1}$, S_2, and $S_{3,2}$, respectively.

Table 2.12 summarizes the experimental results of Figure 2.40. It is worth noting that due to the dramatically lower parasitic capacitances in wide band gap devices, high frequency switching leads to high *di/dt* or *dv/dt* and induces voltage and current oscillations.

Table 2.12 Details of the experimental results

Figure	v_p	v_s	V_o	Input/output powers (W)	Eff. (%)
Figure 2.40(a)	5-level ML*:200V	3-level ML*:200V	200V	885/851	96.16
Figure 2.40(b)	3-level ML*:100V	3-level ML*:200V	200V	892.8/851	95.32
Figure 2.40(c)	2-level ML*:100V	3-level ML*:200V	200V	890/851	95.62
Figure 2.40(d)	3-level ML*:200V	3-level ML*:200V	200V	887/851	95.9

* Maximum level

2.3 Three-phase modified T-type converter

In this section, a three-phase isolated dc-dc converter based on the proposed 5-level T-type converter is proposed. This structure includes three single-phase transformers that primary sides are parallel and secondary sides are Y-connected. The unidirectional and bidirectional types of the proposed three-phase converter are described in detailed as follows:

2.3.1 Three-phase unidirectional modified T-type converter

The proposed three-phase isolated unidirectional dc-dc converter is shown in Figure 2.41. For each phase, the primary converter is a 5-level T-type converter and the secondary converter is a three-leg uncontrolled rectifier. The phase-shifted modulation is applied for this converter. The other two modulation methods can be applied as well.

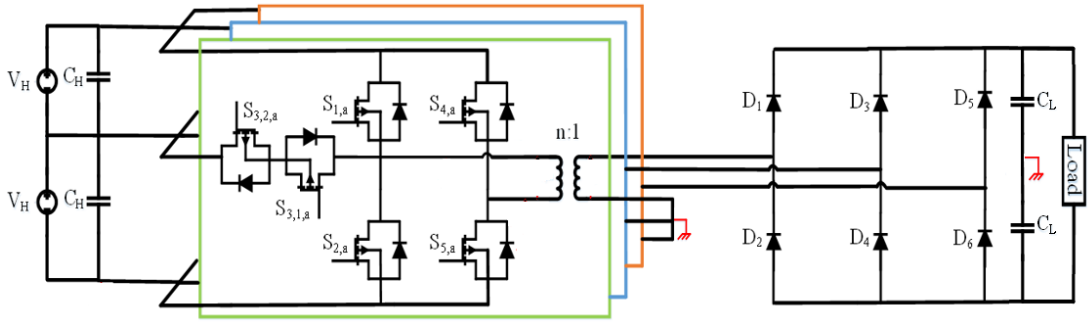


Figure 2.41 Proposed unidirectional 3-phase isolated DC-DC converter.

The operation modes for the *a*-phase are as follows:

First, by turning on switches $S_{1,a}$ and $S_{5,a}$, the primary converter produces voltage of $2V_H$ at the primary side of transformer. Second, switches $S_{3,1,a}$, $S_{3,2,a}$ and $S_{5,a}$ are on and the voltage at the primary side of transformer is V_H. Third, switches $S_{2,a}$, $S_{5,a}$ are on, the primary and secondary voltages are zero. The same patterns are considered in the negative half cycle. The *b* and *c*-phases operate in a similar way with phase shift of 120 and 240 with respect to *a*-phase, respectively.

2.3.2 Three-phase bidirectional modified T-type converter

The proposed three-phase isolated bidirectional dc-dc converter is shown in Figure 2.42. For each phase, the primary converter is a 5-level T-type converter. Because the range of voltage at the secondary side is low, the three-level T-type converter is used as the secondary converter. The phase-shifted modulation is applied for this converter. The other two modulation methods can be applied as well.

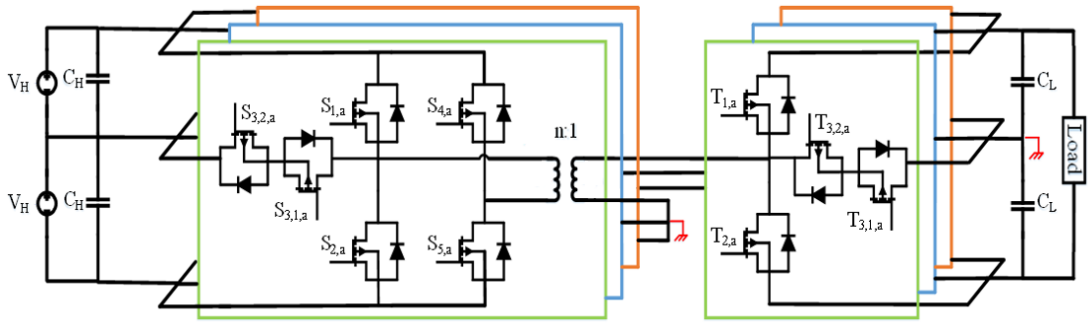


Figure 2.42 Proposed bidirectional 3-phase isolated DC-DC converter.

The operation modes of *a*-phase in the proposed structure are as following:

The primary converter operates the same as the previous one. In the secondary converter, the voltage of V_L is produced by turning on switch $T_{1,a}$. This converter produces zero voltage at the secondary side of transformer by using switches $T_{3,1,a}$ and $T_{3,2,a}$. The same patterns can be considered in the negative half cycle. The *b* and *c*-phases operate in a similar way but with phase shifts of 120 and 240 degrees with respect to *a*-phase.

2.3.3 Switching and control strategy

Figure 2.43 shows the switching strategy of the unidirectional converter. The control goals are setting output dc voltage at the desired value as well as minimizing the total harmonic distortion (THD) of the primary voltage of the transformer. The two control parameters are the angles α_1 and α_2. The Fourier series of the primary voltage waveform shown in Figure 2.43 (V_P) can be written as (2-63).

$$V_p(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_H}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2))\sin(n\omega t) \tag{2-63}$$

The fundamental and harmonics of voltage can be written as (2-64) and (2-65), respectively.

$$V_{p,1}(\omega t) = \frac{4V_H}{\pi}(\cos(\alpha_1) + \cos(\alpha_2))\sin(\omega t) \tag{2-64}$$

$$V_p(\omega t) - V_{p,1}(\omega t) = \sum_{n=3,5,7,\dots}^{\infty} \frac{4V_H}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2))\sin(n\omega t) \tag{2-65}$$

Therefore, the THD of the primary voltage is calculated as follows:

$$THD_{V_P} = \frac{\sqrt{\sum_{n=3,5,7,\dots}^{\infty} (\frac{1}{n}(\cos(n\alpha_1) + \cos(n\alpha_2)))^2}}{\cos(\alpha_1) + \cos(\alpha_2)} \tag{2-66}$$

The dc values of the output voltage (V_o) is calculated as (2-67).

$$V_{o,dc} = \frac{2V_H}{n\pi}(\pi - \alpha_1 - \alpha_2) \tag{2-67}$$

Therefore, the cost function can be written as follow.

$$\min \frac{\sqrt{\sum_{n=3,5,7,\ldots}^{\infty} \left(\frac{1}{n}(\cos(n\alpha_1)+\cos(n\alpha_2))\right)^2}}{\cos(\alpha_1)+\cos(\alpha_2)} \quad s.to \begin{cases} \alpha_1+\alpha_2 = \pi - \dfrac{n\pi V_{o,dc}^*}{2V_H} \\ 0 \prec \alpha_1 \prec \alpha_2 \prec \dfrac{\pi}{2} \end{cases} \tag{2-68}$$

In (2-68), $V_{o,dc}^*$ is the desired output voltage. By solving (2-68), the optimum switching angles that generate primary 5-level voltage with the minimum THD and desired output voltage are calculated. The switching strategy in the bidirectional dc-dc converter is shown in Figure 2.43(b). As mentioned earlier, the fundamental voltage of the primary five-level voltage is calculated from (2-66). The angles α_1 and α_2 are controlled such that minimum amount of THD is obtained in the generated 5-level voltage at the primary side of the transformer. The fundamental component voltage of secondary three-level voltage reflected to the primary side is calculated as follows:

$$V_{s,1}'(\omega t) = \frac{4nV_L}{\pi}\cos(\alpha_3)\sin(wt) \tag{2-69}$$

For optimal performance of the converter, the fundamental values of primary and reflected secondary voltages should be the same, therefore the angle α_3 is calculated from (2-70).

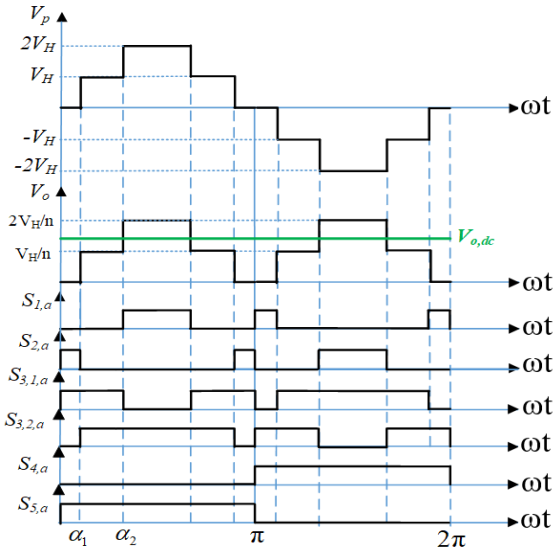
$$\alpha_3 = \cos^{-1}\left(\frac{V_H}{nV_L^*}(\cos(\alpha_1)+\cos(\alpha_2))\right) \tag{2-70}$$

Where, V_L^* is the desired output voltage.

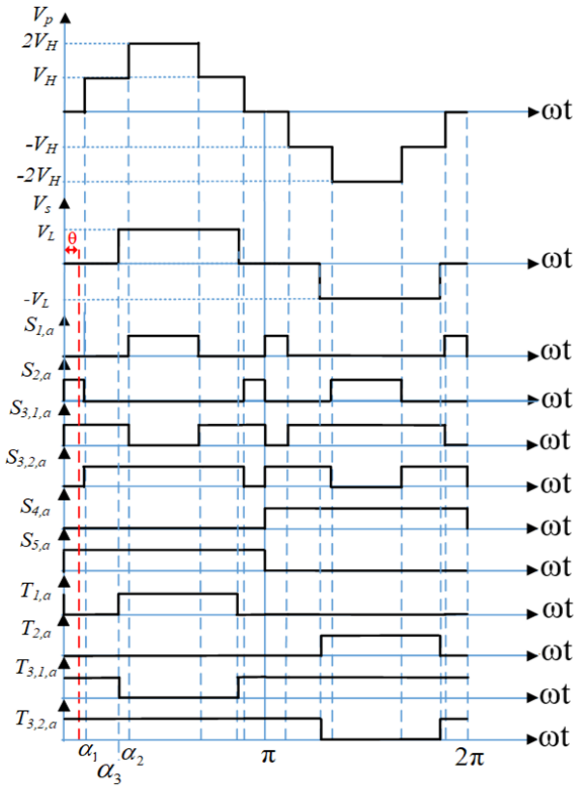
In Figure 2.43(b), θ is the phase shift between the fundamental values of the primary 5-level and secondary 3-level reflected voltages which is controlled based on desired active power that needs to transfer from primary to secondary sides calculated from (2-71).

$$P_o = \frac{V_H^2}{2\pi^2 f_s L_s} |\theta|(\pi - \theta) \tag{2-71}$$

where, P_o, f_s and L_s are the output power, fundamental frequency, and equivalent inductance between primary and secondary side converters.



(a)



(b)

Figure 2.43 Switching states as well as primary and secondary voltages in (a) unidirectional (b) bidirectional topologies.

2.3.4 Simulation results

The proposed three-phase isolated dc-dc topology is simulated in this section based on circuit shown in Figure 2.41 and Figure 2.42. The simulation parameters are based on Table 2.7. It is important to note that in this simulation, the turn ratio of transformer is 4:1. The operation of the proposed unidirectional converter is shown in Figure 2.44 includes the primary and secondary voltages and primary currents of *a*-phase to *c*-phase. The 5-level voltage with the maximum level

of 1 kV is produced at the primary side of the transformer. The maximum amount of primary current is 1.2 A. The input and output voltages and currents are shown in Figure 2.45. Based on this figure, input currents are 1.23958 A for each dc-link of 500 V. The output voltage and current are 350.239 V and 3.50239 A. The input and output powers are 1239.6 W and 1226.7 W. The efficiency is 98.96%.

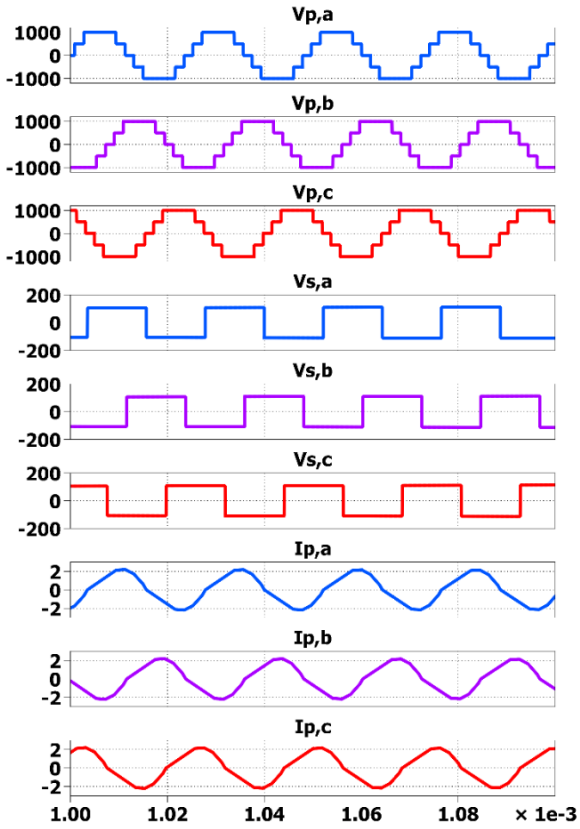
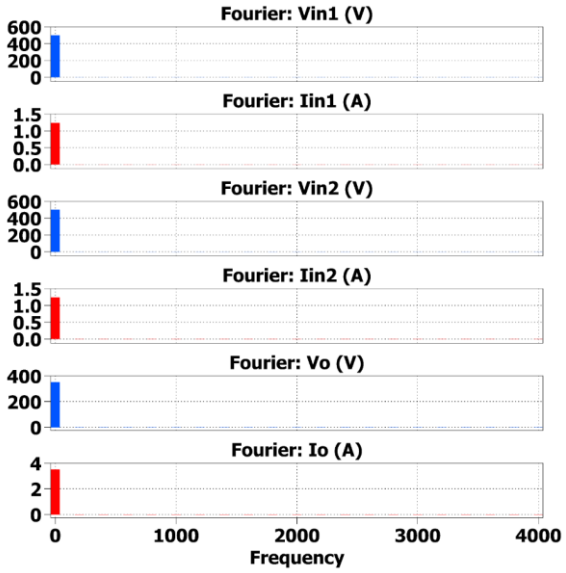


Figure 2.44 Operation of the proposed unidirectional 3-phase converter.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	200	400	600	800	1000
Fourier: Vin1 (V)						
v_H1	500	3.00828e-12	5.48662e-12	3.42667e-12	1.63356e-12	5.67881e-12
Fourier: Iin1 (A)						
i_H1	1.23958	5.76341e-8	3.50342e-8	2.43512e-8	1.86803e-8	1.46592e-8
Fourier: Vin2 (V)						
v_H2	500	3.00828e-12	5.48662e-12	3.42667e-12	1.63356e-12	5.67881e-12
Fourier: Iin2 (A)						
i_H2	1.23958	5.7588e-8	3.50071e-8	2.42964e-8	1.86706e-8	1.46392e-8
Fourier: Vo (V)						
v_o	350.239	6.64022e-6	4.04922e-6	2.83059e-6	2.16098e-6	1.74335e-6
Fourier: Io (A)						
i_o	3.50239	6.64021e-8	4.04922e-8	2.83059e-8	2.16098e-8	1.74335e-8

(b)

Figure 2.45 Analysis of the input and output voltages and currents of the proposed unidirectional 3-phase converter.

The operation of the proposed bidirectional converter is shown in Figure 2.46 includes the primary and secondary voltages and primary currents of *a*-phase to *c*-phase. The 5-level voltage with the maximum level of 1 kV is produced at the primary side of the transformer. The 3-level voltage with the maximum level of 465.425 kV is produced at the primary side of the transformer. The maximum amount of primary current is 1.2 A. The input and output voltages and currents are

shown in Figure 2.47. Based on this figure, input currents are 2.16837 A for each dc-link of 500V. The output voltage and current are 465.425 V and 4.65425 A. The input and output powers are 2168.4 W and 2144.5 W. The efficiency is 98.9%.

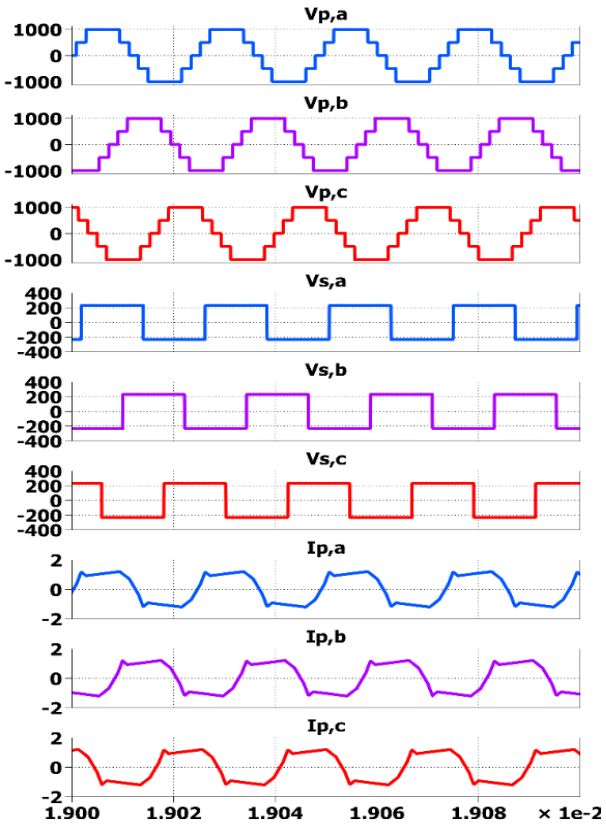
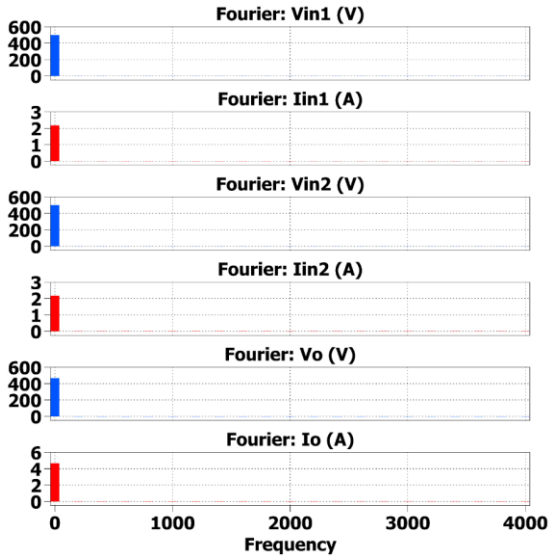


Figure 2.46 Operation of the proposed bidirectional 3-phase converter.



(a)

Data

Name	0	1	2	3	4	5
Frequency	0	200	400	600	800	1000
Fourier: Vin1 (V)						
V_H1	500	8.02338e-12	1.54073e-12	1.38919e-12	2.33964e-12	5.68572e-12
Fourier: Iin1 (A)						
i_H5	2.16837	2.31219e-6	2.43162e-6	2.53564e-6	2.66365e-6	2.82604e-6
Fourier: Vin2 (V)						
V_H2	500	8.02338e-12	1.54073e-12	1.38919e-12	2.33964e-12	5.68572e-12
Fourier: Iin2 (A)						
i_H6	2.16837	9.61143e-6	9.57885e-6	9.62876e-6	9.72237e-6	9.85401e-6
Fourier: Vo (V)						
v_o1	465.425	3.9561e-5	2.34864e-5	1.63116e-5	1.24418e-5	1.00518e-5
Fourier: Io (A)						
i_H12	4.65425	3.95611e-7	2.34864e-7	1.63116e-7	1.24418e-7	1.00518e-7

(b)

Figure 2.47 Analysis of the input and output voltages and currents of the proposed bidirectional 3-phase converter.

Chapter 3

3 Real-time Fault Diagnostic

3.1 Introduction

The commonly mentioned 3-level isolated dc-dc converters do not have fault-tolerant capability via alternate switching states. The reliability of the system using power electronic devices should be considered due to the fact that fast-switching power semiconductors are the most fragile component of the power conversion apparatus. To ensure reliability of the power conversion system, a fault-tolerant topology should be investigated, and detection, location, isolation, and post-fault control methods must be suitably embedded in the control system. Different methods based on the inverter's model and machine learning have been analyzed in the literature to detect and locate an open-circuit fault [61], [62], [63]. Since dual-active dc-dc converters are the crucial parts of the power conversion in zonal shipboard applications, different fault detections methods of the literature in dc-ac inverter part are briefly reviewing here. It is important to note that mostly open-circuited faults of switches are considered, since other types of faults, including

short-circuited damage of switches and an input supply line to ground faults, are expected to actuate the protection mechanisms to safely stop the system [64]. Generally, open circuit fault detection of semiconductor devices is analyzing based on inverter's model or machine learning methods. [64], [65] are analyzing the fault detection in matrix converter based on the model of the converter. In these methods, more current or voltage sensors are needed. They need to know the switching pattern. In multilevel (cascaded H-bridge) converters, model predictive control has been used to fault detection. This method is based on the variables states and need more voltage or current sensors to measure the values of parameters [61], [66], [67], [68]. Also another downside of this method is that it is completely developed for the specific topology. In [69], [70], [71], [72], fault detection methods are analyzed on multicell modular converters (MMCs). The method used in [50] is not based on the state values of the converter and it is robust to system parameters. They can detect the fault in 10-40 ms. The methods used in [51], [52], [53] are based on the state variables of the analyzed converter and need to measure them. A fault detection based on sliding mode observer is introduced in [73]. It has shown that it is effective in locating the faulty switch and very robust against both parameter uncertainty and measurement error. However, in all of the mentioned methods for MMCs, a higher number of voltage sensors are needed to measure the voltages of each cells. In the fault detection method analyzed on flying capacitor converter [74], it is needed to measure the terminal voltage and direction of current. Based on this method, 24 and

25us are needed to detect the fault and 808 and 352 us is needed to localize the fault. Also in [75], the current based fault detection method is applied on back-back NPC converter that needs more current sensors. Overall, in all mentioned methods, more voltage or current sensors are needed. Besides, they are not general methods and only can apply on specific topologies. Also detecting the fault in those methods mostly takes longer time. The machine learning based fault detection methods are analyzed on multilevel converter [76] and MMC converter [77], [78]. Based on the chosen signal to analyze the feature, more voltage and current sensors are needed. Multiphase multilevel NPC using active semi-supervised fuzzy clustering algorithm with Pairwise Constraints is analyzed in [79]. It is based on a model of the converter that can detect the fault in 500 ms. In the other work of same authors using similar method based on gate signals and actual motor currents, the fault is detecting in less than 1 ms [80]. 3-phase ANPC grid-tied converter is analyzed in [63] regarding the fault detection method. The method used in this work is based on three phase currents. The trained neural network displayed a high average detection accuracy of 99.6% for multi-level current open switch faults within an average time of 1.027 ms. In [62], [81], [82], other machine learning methods have been applied. In [43] that is applied on MMC, the authors claimed that the presented method has perfect accuracy on fault detection and identification (100%), robustness against variations of MMC parameters, real-time monitoring and low time delay for fault detection and identification (<0.1 s). In [62] that is applied on multilevel (cascaded H-bridge)

converter, to improve fault diagnosis accuracy and efficiency of a cascaded H-bridge multilevel inverter system (CHMLIS), a fault diagnosis strategy based on the principal component analysis and the multiclass relevance vector machine (PCA-mRVM), was presented.

3.2 Data acquisition

In a real system, the transient between normal and post-fault operations is very important. The system needs to detect and locate the fault in a very short time to have higher safety and reliability. In this section, the focus is on the primary side 5-level T-type converter. In the case of normal operation and open-circuit failure (OCF) of switches S_1, S_2, both S_1 & S_2, $S_{3,1}$, $S_{3,2}$, and both $S_{3,1}$ & $S_{3,2}$, the output voltage (vo), output current (io), and input currents will get affected. By investigating these signals, in each faulty condition, the symmetrical primary voltage is changed to a non-symmetrical waveform that increases the THD of the primary voltage. It causes higher core loss in high-frequency transformer as well as increasing the thermal stress of it. Also, the waveform of the current is changed to a higher THD waveform that increases the transformer and switches conduction losses. Most importantly, in each faulty condition, the output voltage in isolated dual-active bridge converter is regulated at different values with higher amount of ripple that is not acceptable in this application. Therefore, having a fault detection system to detect and locate the fault in limited time and apply the post-fault

switching method is urgent. In machine-based methods, the first step is feature extraction. Fourier transform-based methods have been extensively used for this purpose due to their effectiveness in transforming signals into the frequency domain. Here, time-frequency features are extracted from the discrete-time primary voltage waveform, providing valuable information about the signal's frequency components over time. To achieve fast detection, a recursive discrete Fourier transform (rDFT) is used to extract these features. The recursive form of short-time Fourier transform (STFT) allows for efficient computation of the Fourier transform over sliding windows of the signal, making it particularly suitable for real-time applications. The recursive form of short-time Fourier transform is as follows:

$$X_n[k] = e^{\frac{j2\pi k}{N}}(X_{n-1}[k] - x[n-N] + x[n]) \tag{3-1}$$

where $x[n]$ and N are the primary voltage waveform at time sample n and the number of data samples in the window, respectively. A complex array X_n of length N is produced by applying the short-time Fourier transform at time n wherein $X_n[k]$ is proportional to the power in the frequency component $k \times F\_S/N$. Here, F_S is the sampling frequency for discretization of the primary voltage waveform. The extracted feature vector contains the magnitude of $X_n[k]$ for k=1, 2, 3…N/2.

Based on the total number of faulty conditions as well as normal operation, there are 7 classes shown in Table 3.1. In each class, by applying the mentioned

feature extraction method, 21 first harmonics including DC value, fundamental and orders 2 to 20 have been used in this work as features of each class. These harmonics are crucial for characterizing different operational states and faults in the system. The extracted features, specifically the harmonics, provide a detailed spectral representation of the signal. Each harmonic represents a specific frequency component of the signal, and changes in these components can indicate different types of faults or operational conditions.

Table 3.1 Numbers of classes

Normal	**OCF on S_1**	**OCF on S_2**	**OCF on S_1 & S_2**	**OCF on $S_{3,1}$**	**OCF on $S_{3,2}$**	**OCF on $S_{3,1}$&$S_{3,2}$**
Class 1	Class 2	Class 3	Class 4	Class 5	Class 6	Class 7

3.3 Deep learning-based fault diagnosis method

In this section, a fault diagnosis method including a preprocessing module and deep learning (DL) model is proposed that its architecture is shown in Figure 3.1. In the following, each component and its functionalities are explained in detail.

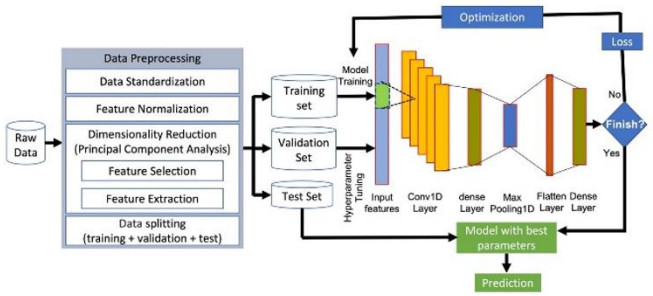


Figure 3.1 Proposed system design for the deep learning model

3.4 Data preprocessing

Generally, in all machine learning (ML) or DL methods, it is necessary to prepare the input data in the right format for the designed model to ensure or enhance its performance. It is a data mining technique that transforms raw data (real world data) into an appropriate format so the DL model can fully learn the existing patterns. Raw data is always incomplete, due to existing noise or possible errors in the data collection phase, and that data cannot be sent through the model. Data preprocessing transforms the data into a format that is more easily and effectively interpreted and processed in the ML or DL part. Data preprocessing techniques used in this work are explained in the following:

3.4.1 Data standardization

In most real-world cases, dataset features are not on the same scale. Some features often have very big values, and others have small values. If such data is not transformed into a standard scale, features with tremendous values dominate those with small values, and the DL model treats those with small values as if they don't exist. To ensure this is not the case, it is needed to scale the features on the same range. Data standardization (also called Z-Score normalization) is the process of transforming data to a standard format that is more easily and effectively processed in data mining, ML, and other data science tasks. Standardization entails scaling data to fit a standard normal distribution, which is defined as a distribution with the mean and standard deviation of the data in question. The formula used to derive standardized values is as follows:

$$\hat{X} = \frac{X - \mu}{\sigma} \tag{3-2}$$

where X is the input data, μ is the mean, and σ is the standard deviation. Standardization transforms values based on the mean and the standard deviation of the data in question. After this step, all the features are centered around 0 with a standard deviation of 1.

3.4.2 Feature normalization

Like the previous step, normalization also transforms data into a specific format, which makes training less sensitive to the scale of features, so we can better solve for coefficients. The following is the formula for normalizing the values of a data set:

$$X_{norm} = \frac{X - \min(X)}{\max(X) - \min(X)} \tag{3-3}$$

Normalizing will ensure that a convergence problem does not have a massive variance, making optimization feasible. In this paper, both standardization and normalizations methods have been used separately to see if they can improve the results. For implementing both standardization and normalization steps, the standard Scikit-learn preprocessing package is used, which provides several common utility functions and transformer classes to change raw feature vectors into a representation that is more suitable for the downstream estimators.

3.4.3 Dimensionality reduction

The presented deep learning model takes the harmonics of the primary voltage as the input vector. The number of features in the vector (input dimensions) can range from a couple of features to tens or even hundreds. When dealing with

high dimensional data, making a predictive modeling task becomes more challenging to the DL model, which is more generally referred to as the curse of dimensionality. The curse of dimensionality can have adverse effects on the performance of the system from latency of the training process to the accuracy of the model, throughput, the rate of learning, size of the model, energy efficiency, and so on. To tackle this problem, a group of dimensionality reduction techniques are used. Dimensionality reduction refers to techniques that reduce the number of input dimensions in a dataset. The way that techniques work is to project the data to a lower dimensional subspace which captures the "essence" of the data. There are many techniques that can be used for dimensionality reduction such as Feature Selection Methods, Matrix Factorization, Principal Component Analysis (PCA), Linear Discriminant Analysis (LDA), and Generalized Discriminant Analysis (GDA). To tackle the curse of dimensionality problem, PCA on the datasets is used reducing the number of dimensions before training the model. Although PCA is applicable to all datasets, it is especially useful for the ones with a very large number of features. Projecting data to a lower dimensional subspace is very common in different areas such as meteorology, image processing, storage and database systems, and genomics analysis, especially before clustering algorithms [83], [84]. The main basis of PCA-based dimension reduction is to keep only the principal components which explain the most variance in the original data [64]. Figure 3.2 shows the PCA variance ratio according to the number of principal components for

input data, which has 20 numerical input features. This test is conducted using the standard Scikit-learn preprocessing package. As shown in Figure 3.2, keeping only the first five components is enough to represent 95% of the variance in the data. This variance rises to 99% in the case of keeping the first 10 components. We only keep the first 10 principal components because they are enough to represent more than 99% of the variance in the data.

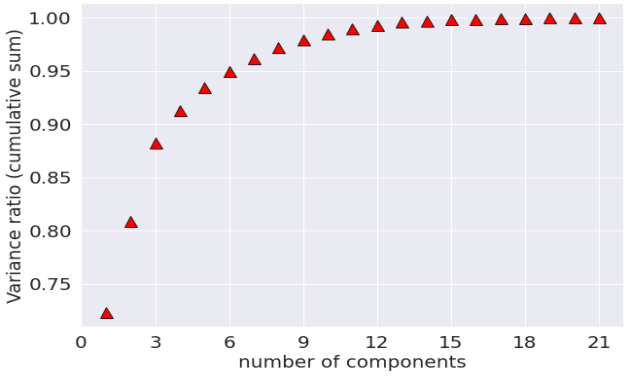


Figure 3.2 PCA variance ratio according to the number of principal components.

3.4.4 Data splitting

After finishing the first steps of the feature engineering process, which includes importing necessary libraries, reading the data input into the pandas.DataFrame, checking for missing values, checking for categorical data, standardizing and normalizing the data, and finally applying PCA transformation, it is needed to start training the model using the available data. So, the first decision to make is how to utilize the existing data. One common technique that is used in

DL realm is to split the data into three groups typically referred to as the training, validation, and testing sets. The training and validation sets are used for developing models, estimating parameters, comparing models, and all the activities required to reach a final model. When the model is trained and the one with the best parameters is saved, the training test set is used to determine the final, unbiased assessment of the model's performance. The reason of keeping this test data set separated from the training and validation sets is that looking at the test sets results outcomes to be biased since the testing data will have become part of the model development process.

3.5 Implemented deep learning model

Figure 3.3 shows the architecture of the proposed deep learning model. As it is clear, this model is a sequential model with only 5 hidden layers including one Conv1D layer, two dense layers, one maxpooling1D layer, and one flatten layer. The total number of parameters is 2392, which makes this model a very lightweight and simple one. Here, Adam optimizer with the learning rate of 0.001 is used.

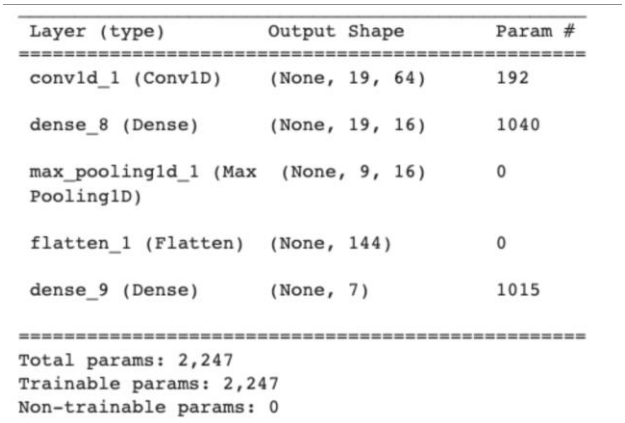


Figure 3.3 Architecture of the proposed deep learning model.

Therefore, when the raw data is received, it is saved into the pandas.DataFrame, and starts the preprocessing phase. In this phase, several techniques are applied to the raw data to transform it into the appropriate format so it can be fed into our model. Then, the transformed data is split into the training, validation, and testing data sets. The next step is to create a deep learning model, adjust its hyperparameters, and finally compile it. When the model is compiles, the training phase is started, which includes setting some hyperparameters such as the number of epochs, batch size, and finally, feeding the data to the model. In this process, after each epoch, the model tries to classify the available data in the validation set. This process results in a loss value, which is produced by the loss function. Using this loss value, the optimizer comes back to the model and adjusts the weights in the layers in a way that reduces the loss. This process continues until either it gets to the last epoch, or the early stopping mechanism stops model training. In the last step, the model with the best parameters (highest accuracy) is saved. The

performance of the model in terms of accuracy or loss can be seen by applying the test set to the model. Based on the predictions and the real labels, the performance of the system is calculated. In the following section, the case study specifications and testing results are discussed in detail.

3.6 Case study

In this section, the behavior of the model is evaluated experimentally. Below is the detailed analysis to understand the different characterizations of the model.

3.6.1 Methodology

As an evaluation platform, the experiments are executed on two different machines: (1) In the first configuration, the tests are run on an Intel Core i7 processor running at 2.2 GHz with 2 cores (4 logical cores), each of which has 256KB L2 Cache and 4MB L3 Cache using 8 GB of RAM, running macOS Monterey (version 12.6.1 (21G217)). The reason that the tests are run on a local computer without any GPU support is to get a sense of how the methods work on an ordinary system without any unique capabilities. (2) In the second configuration, the tests are run on Google's Colab with GPU support (NVIDIA 1xTesla K80, compute 3.7, having 2496 CUDA cores, and 12GB GDDR5 VRAM. The performance of the proposed method is evaluated using different metrics such as accuracy, precision, recall, F1-

score, and so on. As far as the data set is concerned, we collected 336 samples (48 samples from each 7 class), from which 269 (80% of the total) samples are separated as the training and validation sets and 67 samples for the testing set.

3.6.2 Results

Understanding how the features in the dataset interact with each other is crucial to keep the important features and remove the irrelevant ones. Although dimensionality reduction techniques such as PCA are used to reduce the number of features, having knowledge of the data at hand, and finding its feature relations can help to improve the performance of the model. There are many ways to construct an effective and accurate model. One of the ways to strengthen a model is to identify and reduce the features in the dataset that are highly correlated. Correlated features can easily add noise and inaccuracy to a model, which in turn will make it harder to achieve the desired outcome. Figure 3.4 shows the correlated features in the data set as the relational heatmap. As this figure shows each harmonic orders from 0 to 20 is listed on both axes, and their relationships with other variables are displayed using color. As the color becomes darker in either direction (red or blue), it means that those variables are more highly correlated and should not be paired together in the same model. This can help us to choose the best features before feeding them to the model or even decide to collect more samples.

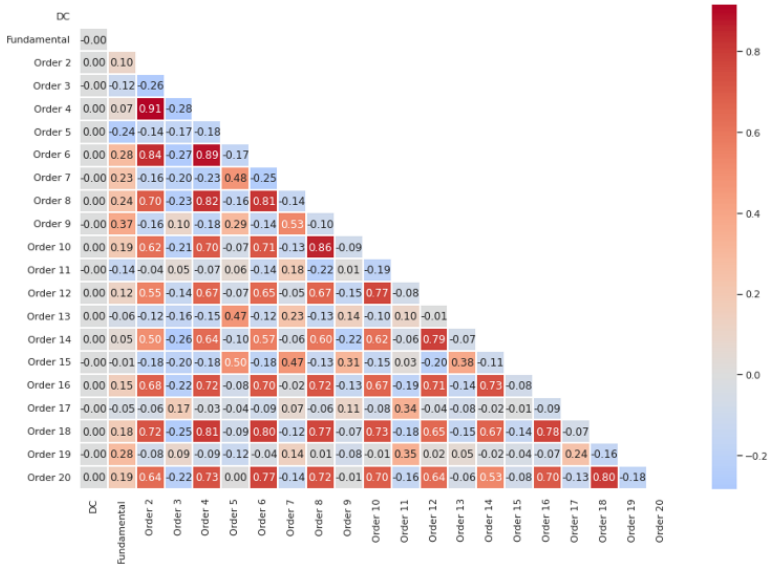


Figure 3.4 Correlation matrix of the data set used in this work

In the next test, an experiment is conducted to see the importance of the features. To this aim, the variable-importance measure for random forest is used. In this method, the model's performance change is measured by removing the effect of a selected explanatory variable, or of a group of variables using perturbations or permutation of the values of the variable. To quantify the goodness-of-fit of the model, the area under the Receiver Operating Characteristic (ROC) curve (AUC) is used as the model-performance measure. This is useful for the evaluation of the importance of an explanatory variable. Using this method can simplify the data set further to variables that do not influence the model's predictions. Also, the ordering of variables in the function of their importance is helpful in deciding in which order should we perform further model exploration. Figure 3.5 shows the Single-permutation-based variable-importance measures for the explanatory variables

included in the random forest model for the data set using 1-AUC as the loss function (to quantify the performance of the model). In other words, we fit a random forest model to predict the classes, and then measure the error increase by 1-AUC (1 minus the area under the ROC curve). For example, based on the figure, the feature with the highest importance is DC associated with an error increase of 0.193766 after permutation.

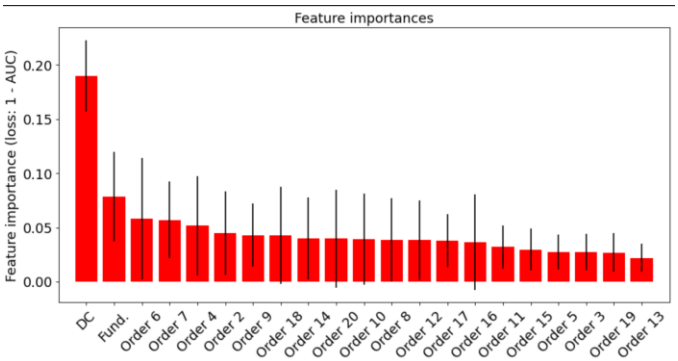
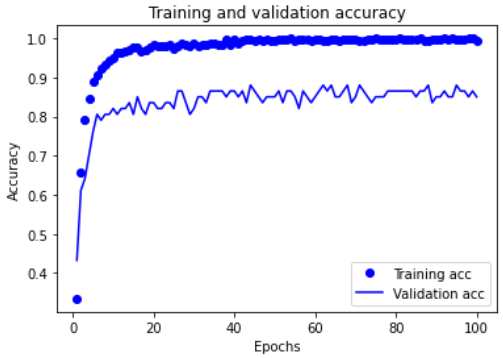


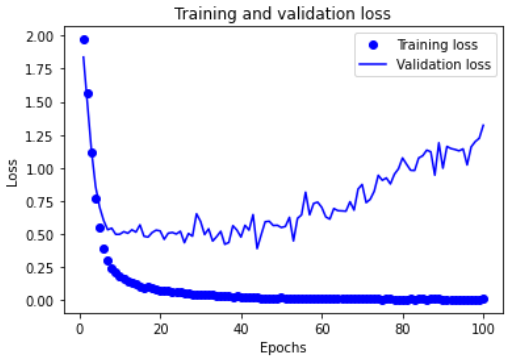
Figure 3.5 Single-permutation-based variable-importance measures for the explanatory variables included in the random forest model for our data set using 1-AUC as the loss function.

The plot in Figure 3.5 suggests that the most important variable in the model is DC value that was predictable due to have asymmetric primary voltage waveforms in the faulty conditions. This agrees with the conclusions drawn in the exploratory analysis presented in the previous section. The next three important variables are Fundamental, Order 6, and Order 4. Using these recent tests, we can not only boost the performance of our deep learning-based system in terms of accuracy and loss but also save a huge amount of time in model training and data

collection. To see the performance characteristics of the proposed deep learning-based model, three scenarios are conducted. In the first scenario, any feature selection or feature extraction method is not used. Figure 3.6 shows that results as the learning curves. As it is shown in this figure, when there is no feature selection and feature extraction, the model cannot use its full potential and find the patterns hidden in the data set due to the reasons that are mentioned in the preprocessing section. Keeping irrelevant and low-importance features along with the small number of available training data samples results in overfitting the model after the first couple of epochs, which further decreases the accuracy of the model.



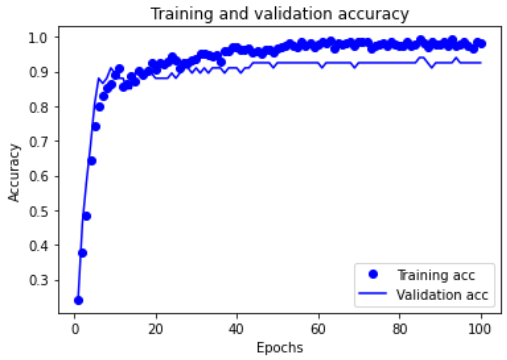
(a)



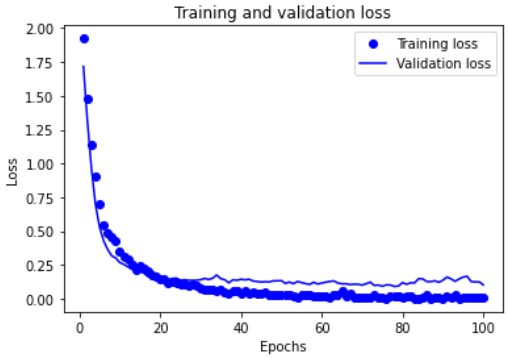
(b)

Figure 3.6 Training and validation (a) accuracy; and (b) loss; for feature extraction for the data set without feature selection and PCA.

Unlike the previous test, in the next one, the correlation matrix and feature importance is used to extract features without using any dimensionality reduction techniques. For this scenario, 10 most important features are selected that do not have very strong correlation based on the results from Figure 3.4 and Figure 3.5. Figure 3.7 illustrates the results for this scenario. As it is clear in the figure, not only does the model's accuracy and loss improve, but also it does not overfit anymore. Finally, Figure 3.8 shows the last scenario, which is conducted by applying both feature importance and selection and dimensionality reduction. In this test, one of the most common dimensionality reduction techniques called PCA is applied. As it is clear in this figure, by collecting more information from the data set and exploring its features and their relations, the model's performance significantly can be improved.

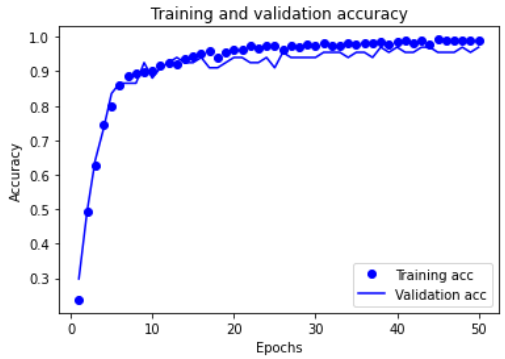


(a)

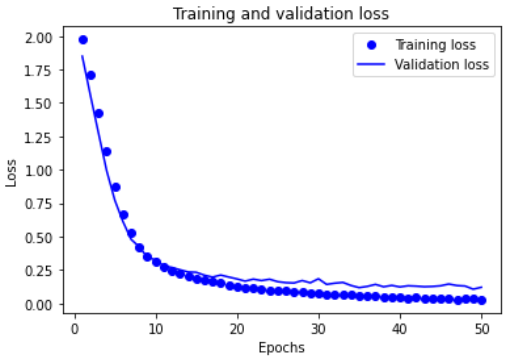


(b)

Figure 3.7 Training and validation accuracy and loss for feature extraction for the data set with feature selection but not PCA.



(a)



(b)

Figure 3.8 Training and validation accuracy and loss for feature extraction for the data set with both feature selection and PCA.

Classification accuracy alone can be misleading if a system has imbalanced observations in each class or if you have more than two classes in your dataset. To measure the performance of the deep learning-based method more accurately, confusion matrix is used. A confusion matrix is a summary of prediction results on a classification problem, where the number of correct and incorrect predictions are summarized with count values and broken down by each class. Figure 3.9 shows the confusion matrix for this problem as a heatmap. As it can be seen in this figure, although there are some misclassifications, the proposed deep learning model has succeeded in predicting/classifying the available samples with high accuracy (see the numbers on the diagonal of the heatmap) for all the classes. It is worth noting that this simple deep learning model has achieved this accuracy with being trained on only 269 samples. This means that the accuracy of the model can be increased by either collecting more real samples or generating synthetic ones using generative

models. In Table 3.2, metrics derived from a confusion matrix are calculated and makes them directly accessible from a pandas.DataFrame. The detailed metrics shows the robustness of the method. For example, the precision for each class is about how precise/accurate the proposed model is out of those predicted positive, which is calculated as follows:

$$\text{Precision} = \frac{True\ Positive}{True\ Positive + False\ Positive} \tag{3-4}$$

To explore the behavior of the model more precisely, there is another metric called recall, which is calculated as follows:

$$\text{Recall} = \frac{True\ Positive}{True\ Positive + False\ Negative} \tag{3-5}$$

While precision is the ability of a classification model to identify only the relevant data points, recall is the ability of a model to find all the relevant cases within a data set. Not only are these metrics necessary in calculating a model's actual performance, but they can also be valuable in finding the classes with lower performance. Using this information, for instance, we can spot those classes with lower performance and collect more data samples related to that class, improving the system's performance.

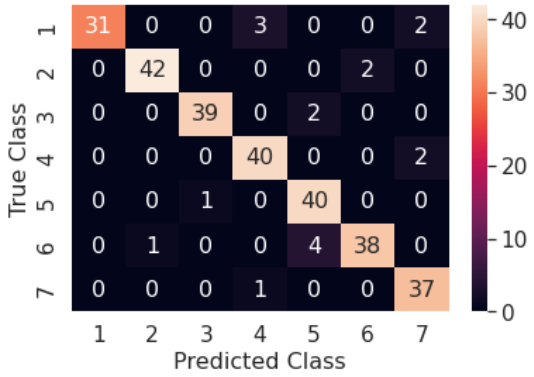


Figure 3.9 Confusion matrix for Figure 3.8

Table 3.2 Accuracy, precision, and recall of the proposed model.

Classes	**Precision**	**Recall**	**Accuracy**
1	1	0.861111	0.982456
2	0.976744	0.954545	0.989474
3	0.975	0.951220	0.989474
4	0.909091	0.952381	0.978947
5	0.869565	0.975610	0.975439
6	0.95	0.883721	0.975439
7	0.902439	0.972684	0.982456
Average	0.936842	0.936842	0.981955

In the last experiment, the latency overhead of the proposed model is calculated in the two different mentioned hardware configurations and shown in Table 3.3. In these tests, the number of components/features in the data set is set to 5, 10, 15, and 20, and the model on both hardware equipped is trained with CPU and GPU. After the training is done, predictions on the testing data are performed using the saved model. Based on the tests, the following important results are observed: (1) Despite the number of features, our lightweight DL model can predict the class

of each faulty conditions or normal operation in a couple of microseconds, which makes the proposed model extremely fast either on a regular hardware with no GPU or on a hardware that is equipped with GPU. (2) The training latency is also very low, which resulted in training every epoch in less than 2 milliseconds for the data set. (3) The third observation is that if we have access to better hardware with GPU, it can cut the latency in half, which is useful especially when latency is of great importance for us. (4) The last observation is that if we decrease the number of features either using dimensionality reduction techniques such as PCA or selecting features manually, we can improve systems' latency. However, by decreasing the number of features we also decrease the accuracy of the system.

Table 3.3 Training and testing latency per sample in the proposed deep learning model for different number of features on CPU and GPU.

Hardware	**# of components**	**Latency (µs)**		**Accuracy (%)**
		Training	**Testing**	
CPU	5	75.2	2.25	75.83
	10	79.64	2.64	98.25
	15	85.26	2.8	98.89
	20	101.3	3.1	99.05
GPU	5	32.76	1.3	75.83
	10	39.86	1.64	98.25
	15	55.26	1.79	98.89
	20	75.3	2	99.05

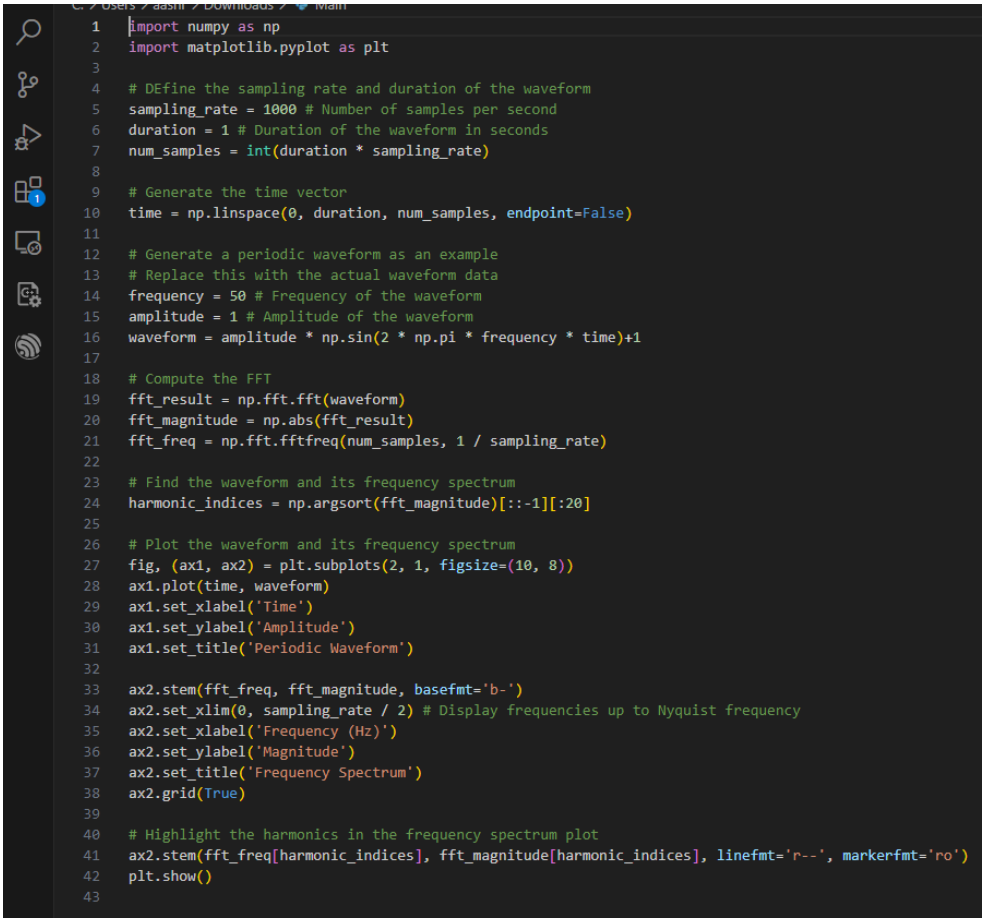
3.7 Real time implementation

To implement the neural network in the hardware phase, the main steps involve using the ADC module of the controller with enough sampling frequency to capture real-time data, applying the mentioned post-processing techniques on the captured data, taking the FFT from the resulting data, and implementing the model using the output of the FFT. For this purpose, the Raspberry Pi 3B+ has been chosen initially, utilizing Python programming. The ADS1115 external ADC module with I2C protocol is used for data acquisition, and Thonny IDE is used to implement the FFT and the neural network model. The ADS1115 is an external ADC module chosen for its high resolution (16-bit) and its ability to interface with the Raspberry Pi using the I2C protocol. This module provides a sufficient sampling rate to capture high-frequency signals accurately. It's crucial to select a sampling frequency that is at least twice the highest frequency component in the signal, according to the Nyquist theorem. For most electrical signals, a sampling frequency in the range of 10 kHz to 100 kHz is typically sufficient. NumPy library is used to perform FFT efficiently in Python. The Thonny IDE, a Python development environment, provides a user-friendly interface for implementing and testing the FFT code. The neural network model, trained and validated in a software environment, is deployed on the Raspberry Pi. This involves converting the trained model into a TensorFlow Lite format suitable for execution on the Raspberry Pi. The output of the FFT serves

as the input to the neural network model. The Raspberry Pi processes this data in real-time, performing inference to classify the signal into one of the predefined fault classes or normal operation. The Raspberry Pi 3B+ features a 1.4 GHz 64-bit quad-core ARM Cortex-A53 CPU, providing sufficient computational power for real-time signal processing and neural network inference. The general purpose Input/Output (GPIO) pins on the Raspberry Pi facilitate connection with the ADS1115 ADC module via the I2C protocol, enabling efficient data acquisition. The I2C interface allows for easy integration with the Raspberry Pi, providing a simple and reliable method for transferring high-resolution analog-to-digital conversion data. The 16-bit resolution of the ADS1115 ensures precise measurement of the signal, capturing even small variations which are crucial for accurate fault detection. Python is chosen for its extensive libraries and ease of use. However, this experiment showed that Raspberry pi with the Python IDE is not fast enough for the real-time implementation because it needs an interpreter to be converted to the machine code. Below shows the Python codes for ADC reading and FFT implementation.

```python
import time
import board
import busio
import adafruit_ads1x15.ads1015 as ADS
from adafruit_ads1x15.analog_in import AnalogIn


ADS1115_ADDRESS = 0x48

# Define the ADC channel to read from (0-3)
#ADC_CHANNEL = 0
# Create the I2C bus
i2c = busio.I2C(board.SCL, board.SDA)

# Create the ADC object using the I2C bus
ads = ADS.ADS1015(i2c)

# Create single-ended input on channel 0
chan = AnalogIn(ads, ADS.P0)

csv_file = open('i2c_log.csv', 'w')

# Write the header row to the CSV file
csv_file.write('SamplingTime, Time, ADC Count, ADC Value\n')

# Create differential input between channel 0 and 1
# chan = AnalogIn(ads, ADS.P0, ADS.P1)

#initial_timestamp = int(time.time()*1)
initial_time = time.time()*1
#print("{:>5}\t{:>5}".format("raw", "v"))

while True:

            # Read the ADC value
        # Get the current timestamp
    timestamp = time.strftime('%Y-%m-%d %H:%M:%S')
    #Current_timestamp = int(time.time()*1)
    Current_time = time.time()*1
    SamplingTime = Current_time - initial_time

    print("{:>5}\t{:>5}\t{:>5.3f}".format(SamplingTime, chan.value, chan.voltage))
        # Write the timestamp and ADC value to the CSV file
    csv_file.write(f'{SamplingTime},{time.time()},{chan.value},{chan.voltage}\n')

        # Flush the file buffer to ensure the data is written immediately
    csv_file.flush()

    time.sleep(1/1000000)
```

(a)



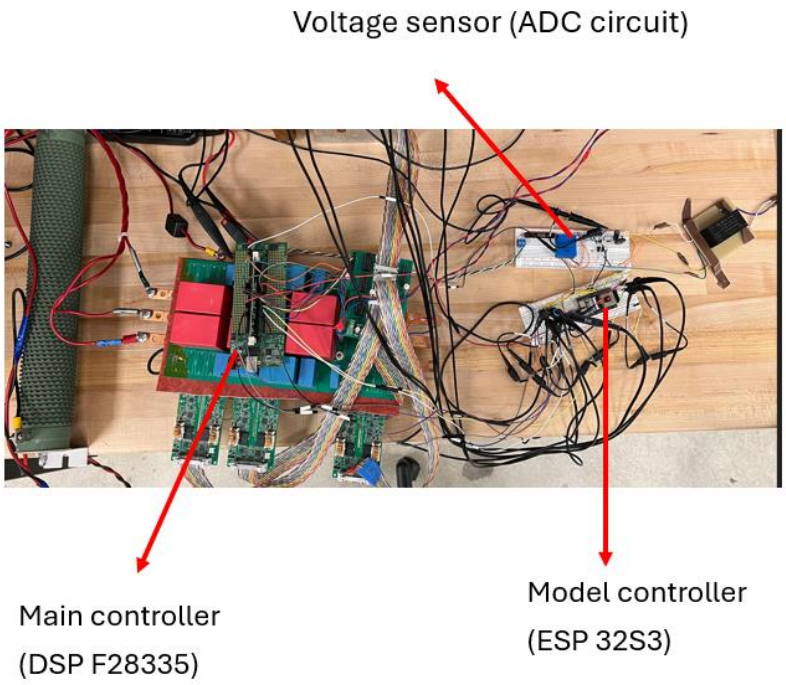
```python
import numpy as np
import matplotlib.pyplot as plt

# DEfine the sampling rate and duration of the waveform
sampling_rate = 1000 # Number of samples per second
duration = 1 # Duration of the waveform in seconds
num_samples = int(duration * sampling_rate)

# Generate the time vector
time = np.linspace(0, duration, num_samples, endpoint=False)

# Generate a periodic waveform as an example
# Replace this with the actual waveform data
frequency = 50 # Frequency of the waveform
amplitude = 1 # Amplitude of the waveform
waveform = amplitude * np.sin(2 * np.pi * frequency * time)+1

# Compute the FFT
fft_result = np.fft.fft(waveform)
fft_magnitude = np.abs(fft_result)
fft_freq = np.fft.fftfreq(num_samples, 1 / sampling_rate)

# Find the waveform and its frequency spectrum
harmonic_indices = np.argsort(fft_magnitude)[::-1][:20]

# Plot the waveform and its frequency spectrum
fig, (ax1, ax2) = plt.subplots(2, 1, figsize=(10, 8))
ax1.plot(time, waveform)
ax1.set_xlabel('Time')
ax1.set_ylabel('Amplitude')
ax1.set_title('Periodic Waveform')

ax2.stem(fft_freq, fft_magnitude, basefmt='b-')
ax2.set_xlim(0, sampling_rate / 2) # Display frequencies up to Nyquist frequency
ax2.set_xlabel('Frequency (Hz)')
ax2.set_ylabel('Magnitude')
ax2.set_title('Frequency Spectrum')
ax2.grid(True)

# Highlight the harmonics in the frequency spectrum plot
ax2.stem(fft_freq[harmonic_indices], fft_magnitude[harmonic_indices], linefmt='r--', markerfmt='ro')
plt.show()

```

(b)

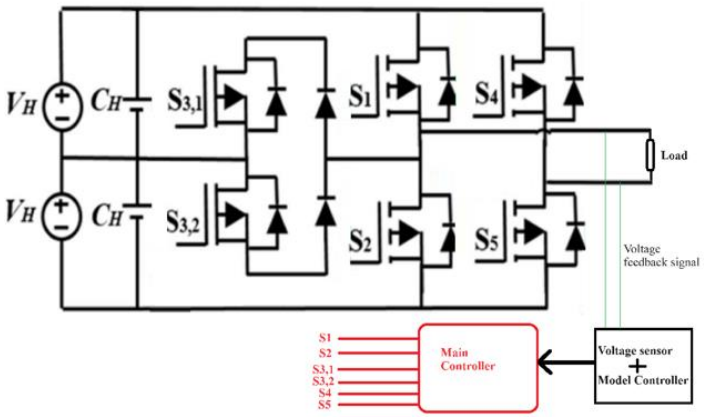
Figure 3.10 Python codes for ADC reading and FFT implementation.

In the second and third steps, DSPs of F28335 and F28379D have been used with C programming. These experiments were also not successful because the model size was larger than the DSPs' stack size. Below, we delve deeper into these steps, exploring the challenges faced and potential solutions. Digital Signal Processors (DSPs), specifically the Texas Instruments TMS320F28335 and

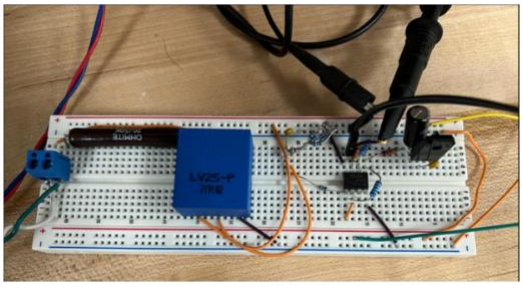
TMS320F28379D, were chosen for their high-performance capabilities in real-time signal processing. These DSPs are well-suited for applications requiring fast and efficient data processing. However, the implementation encountered significant challenges. In TMS320F28335 includes 32-bit floating-point CPU with 150 MHz clock speed, 256 KB flash memory, and 34 KB SRAM. On the other hand, TMS320F28379D includes dual 32-bit floating-point CPUs with 200 MHz clock speed, 1 MB flash memory, and 204 KB SRAM. Both F28335 and F28379D faced issues with memory allocation. The trained neural network model exceeded the stack and heap size available on the DSPs. The memory limitations hindered the direct deployment of the model. Given the memory constraints of the DSPs, alternative approaches were considered to achieve the desired fault diagnosis performance. Exploring other microcontrollers or DSPs with larger built-in memory could mitigate memory constraints. Therefore, ESP32-S3 is chosen for this purpose due to having higher stack size. Figure 3.11 shows the prototype image and corresponding schematic on it. Here, the voltage transducer LV 25 is used in the ADC circuit as a voltage sensor. The built circuit is shown in Figure 3.11(c). Here, 1.5V voltage regulator of TO220FP-3 and NJM5532 operational amplifier are used.


Voltage sensor (ADC circuit)
Main controller
(DSP F28335)
Model controller
(ESP 32S3)

(a)


VH
CH
S3,1
S1
S4
Load
VH
CH
S3,2
S2
S5
Voltage feedback signal
S1
S2
S3,1
S3,2
S4
S5
Main Controller
Voltage sensor + Model Controller

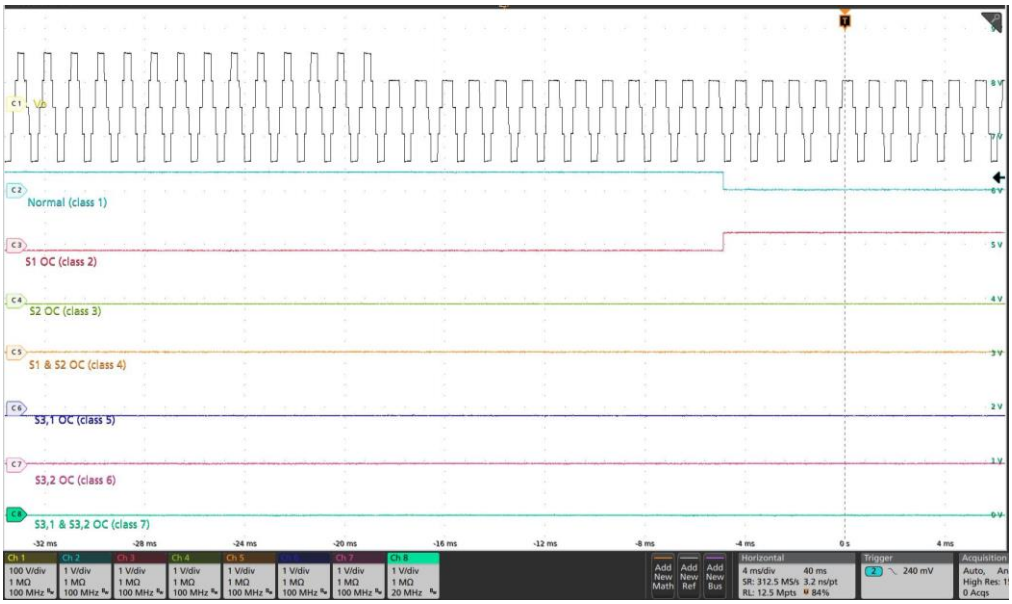
(b)



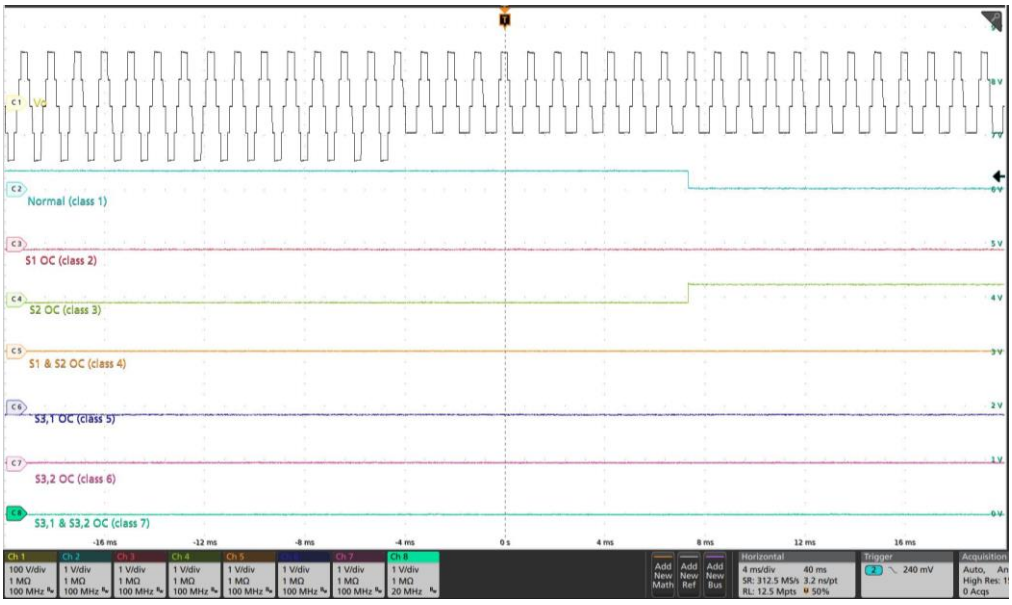
(c)

Figure 3.11 Real-time fault detection prototype details.

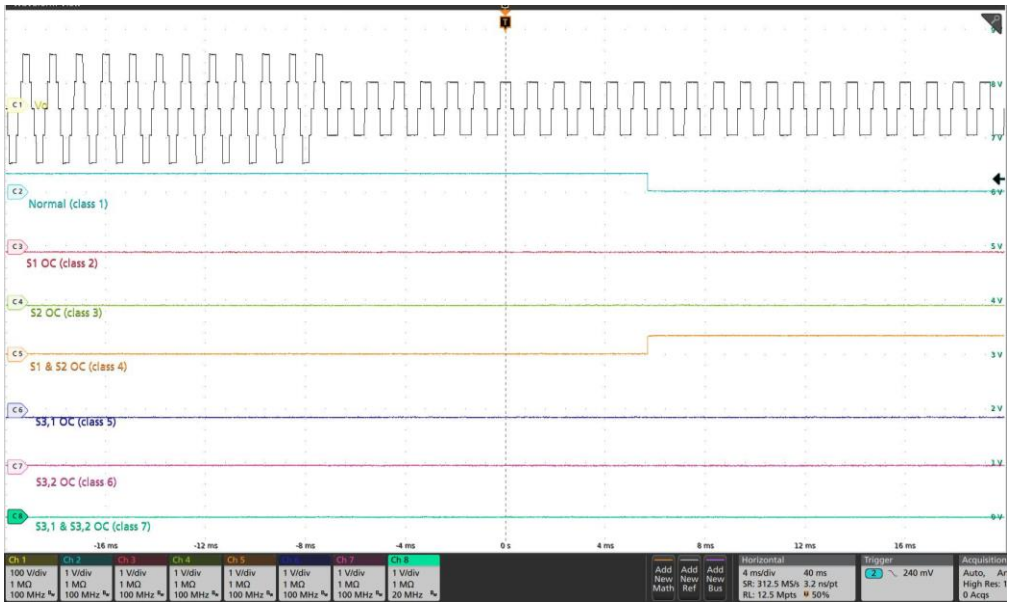
The input power supplies have set to 50 V and the fundamental frequency is 1 kHz. Figure 3.12(a) shows the behavior of the inverter when an open circuit failure happens on switch S_1. As can be seen, first, the inverter was in the normal condition with symmetrical 5-level output voltage. Then by having an open circuit failure on S_1, the output voltage became a non-symmetrical 4-level voltage. Eventually, the open-circuit failure is detected by the controller in 11.76 ms. Figure 3.12(b)-(f) shows the behavior of the inverter when an open circuit happens on S_2, both S_1 and S_2, $S_{3,1}$, $S_{3,2}$, and both $S_{3,1}$ and $S_{3,2}$. As can be seen, in all cases, the inverter started in the normal operation and after seeing an open circuit failure, the model is able to detect and locate the type of failure successfully. It is important to note that the open circuit failure is modeled by sending the zero pulse instead of the actual pulse to the corresponding switch.


Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)

(a)


Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)

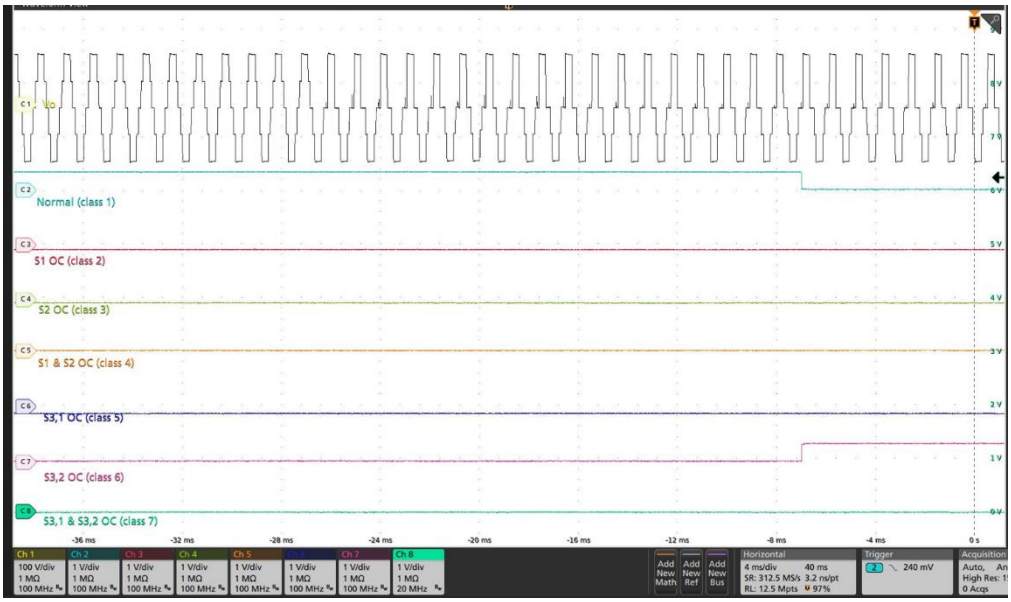
(b)


Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)

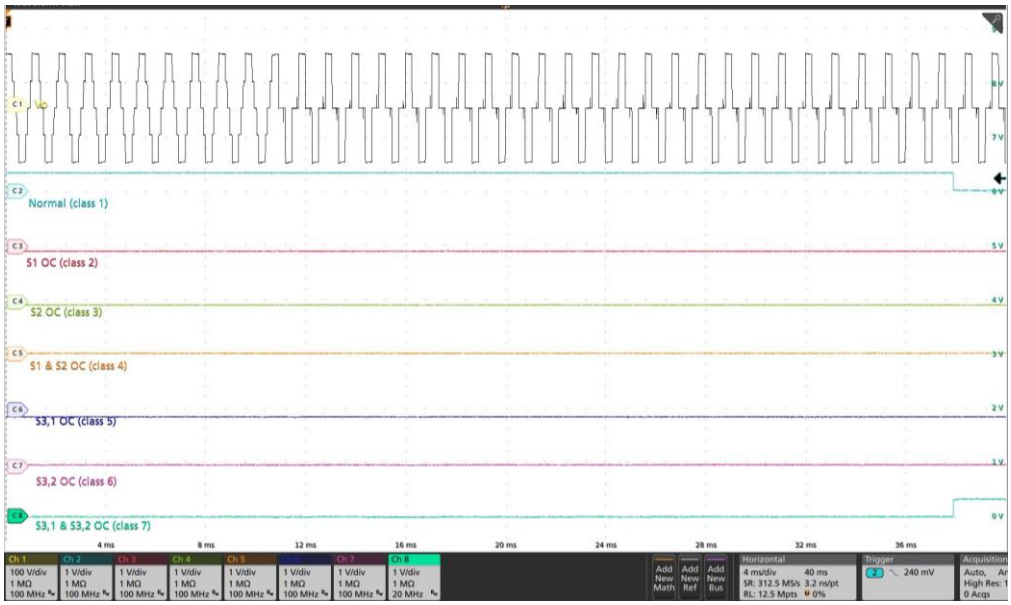
(c)


Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)

(d)



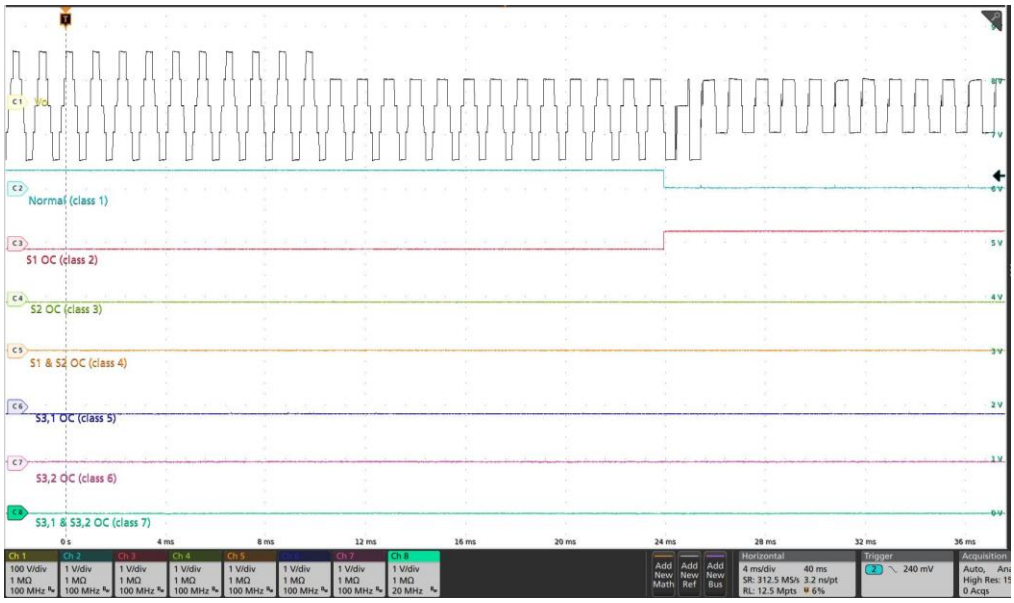
(e)



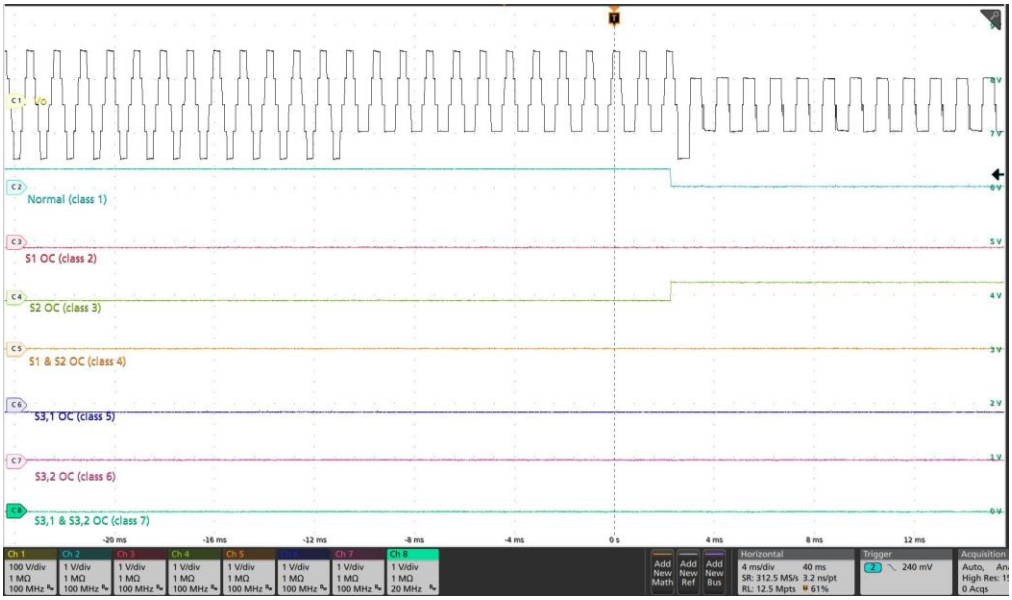
(f)

Figure 3.12 Fault detection and location behavior of the proposed inverter in the case of open circuit failure of (a) switch S_1 with the reaction of 11.76 ms (b) switch S_2 with the reaction of 10.979 ms (c) switches S_1 & S_2 with the reaction of 9.563 ms (d) switch $S_{3,1}$ with the reaction of 23.246 ms (e) switch $S_{3,2}$ with the reaction of 21.566 ms (f) switch $S_{3,1}$ & $S_{3,2}$ with the reaction of 17.976 ms.

In the next step, based on the analyzed post fault switching methods, reconfiguration of the switching scheme of the inverter based on the fault detection result is analyzed. Therefore, two used controllers including DSP F28335 as a main controller and ESP32 as a fault detector are connected to each other and based on the detected result of the model, the proper post fault switching method is applied. Figure 3.13 shows the reconfiguration results.



(a)


C1 Vo
Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)
-20 ms
-16 ms
-12 ms
-8 ms
-4 ms
0 s
4 ms
8 ms
12 ms
Horizontal
4 ms/div 40 ms
SR: 312.5 MS/s 3.2 ns/pt
RL: 12.5 Mpts 61%
Trigger
240 mV
Acquisition

(b)

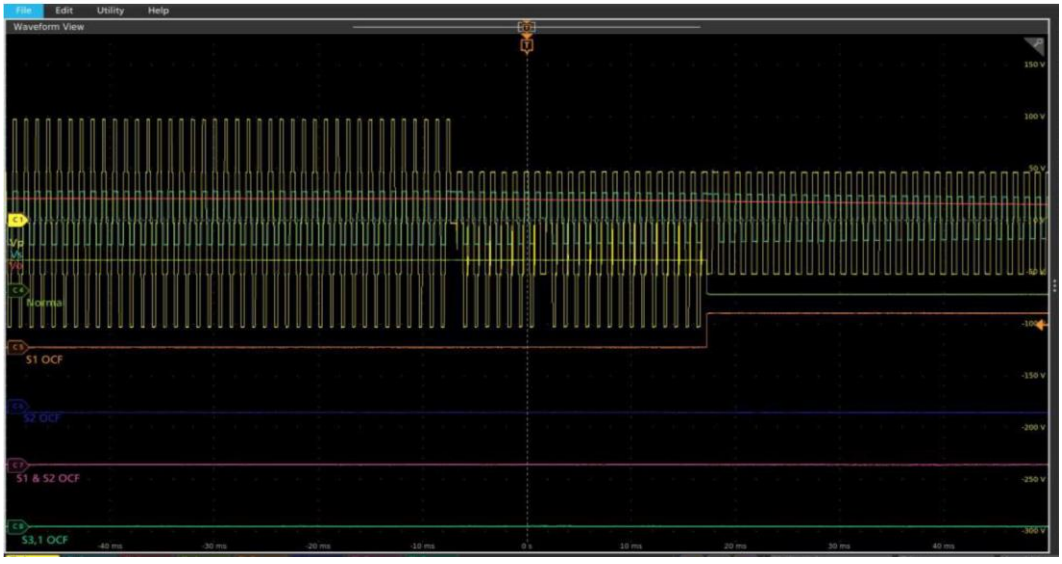

C1 Vo
Normal (class 1)
S1 OC (class 2)
S2 OC (class 3)
S1 & S2 OC (class 4)
S3,1 OC (class 5)
S3,2 OC (class 6)
S3,1 & S3,2 OC (class 7)
0 s
4 ms
8 ms
12 ms
16 ms
20 ms
24 ms
28 ms
32 ms
36 ms
Horizontal
4 ms/div 40 ms
SR: 312.5 MS/s 3.2 ns/pt
RL: 12.5 Mpts 7%
Trigger
240 mV
Acquisition

(c)

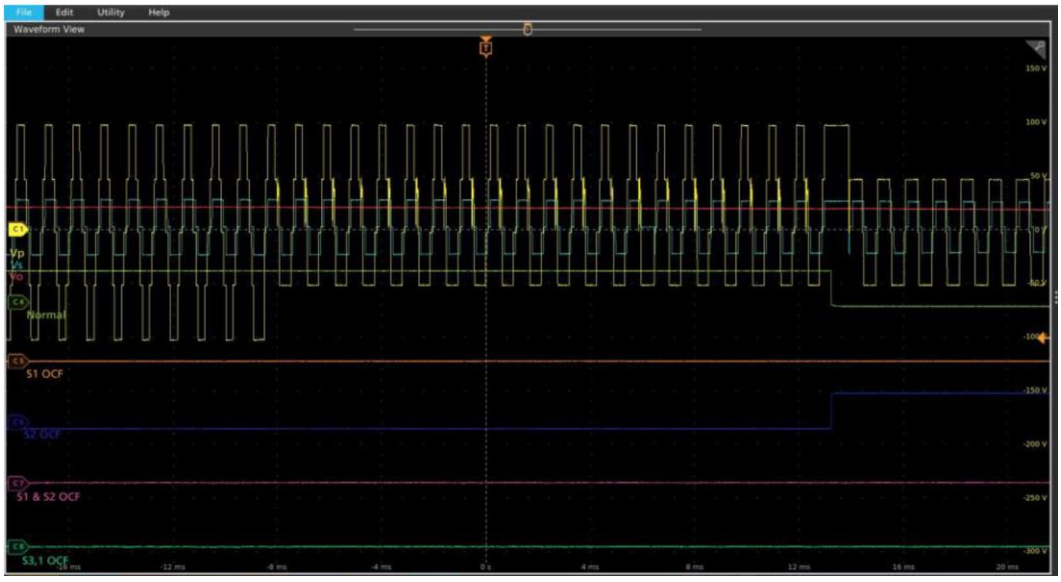
(d)

Figure 3.13 Reconfiguration behavior of the proposed inverter in the case of open circuit failure of (a) switch S_1 (b) switch S_2 (c) switch $S_{3,1}$ (d) switch $S_{3,2}$.

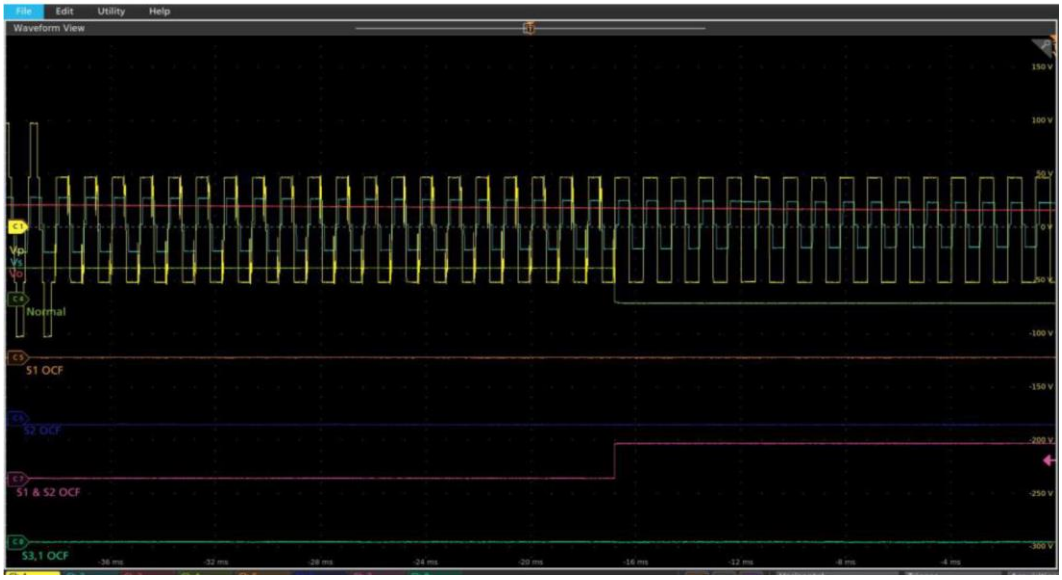
In the last step, real-time fault detection and reconfiguration is applied on the dual-active modified T-type converter and the results are shown in Figure 3.14.



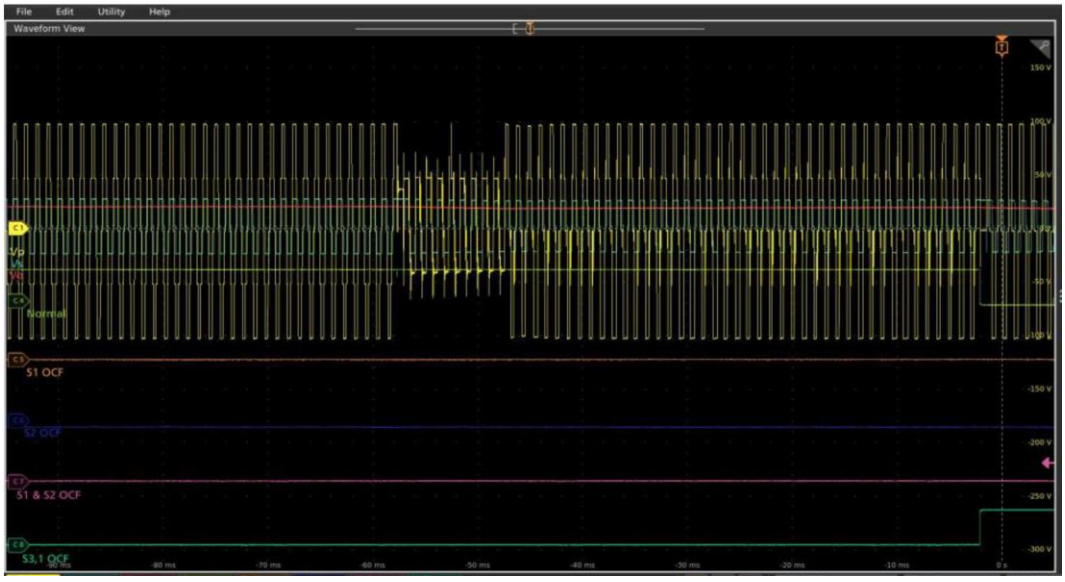
(a)


File
Edit
Utility
Help
Waveform View
150 V
100 V
50 V
0 V
-50 V
-100 V
-150 V
-200 V
-250 V
-300 V
C1
Vp
Vs
C4
Normal
C5
S1 OCF
C6
S2 OCF
C7
S1 & S2 OCF
C8
S3,1 OCF

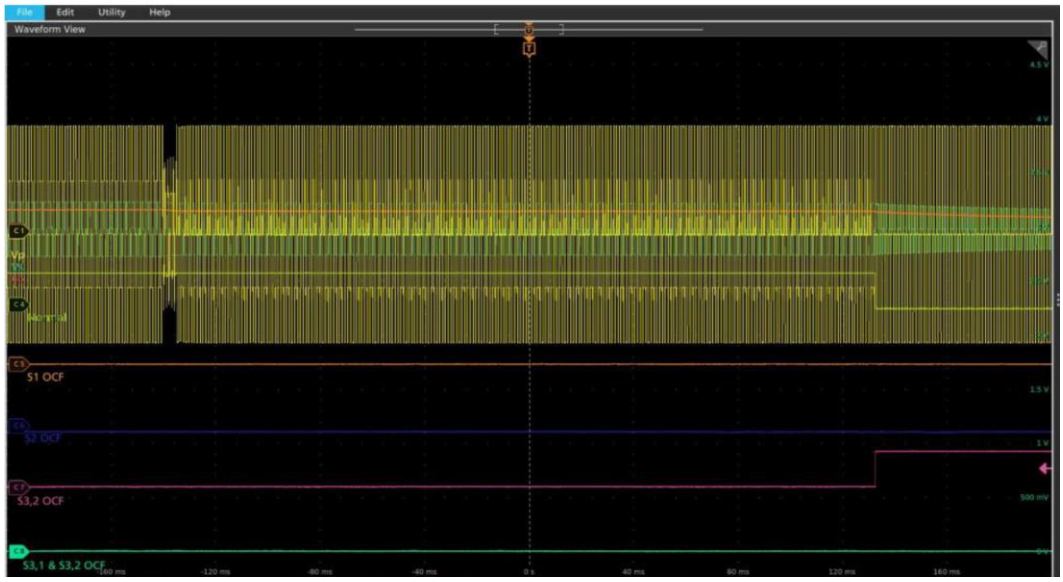
(b)


File
Edit
Utility
Help
Waveform View
150 V
100 V
50 V
0 V
-100 V
-150 V
-200 V
-250 V
-300 V
C1
Vp
Vs
C4
Normal
C5
S1 OCF
C6
S2 OCF
C7
S1 & S2 OCF
C8
S3,1 OCF

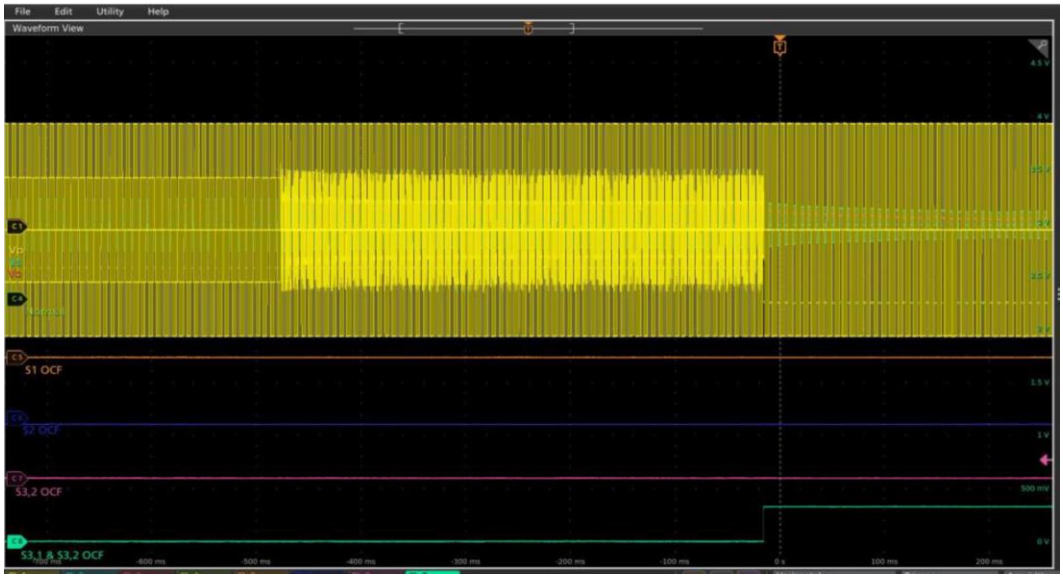
(c)


File
Edit
Utility
Help
Waveform View
S1 OCF
S2 OCF
S1 & S2 OCF
S3,1 OCF

(d)


File
Edit
Utility
Help
Waveform View
S1 OCF
S2 OCF
S3,2 OCF
S3,1 & S3,2 OCF

(e)



(f)

Figure 3.14 Reconfiguration behavior of the proposed dc-dc converter in the case of open circuit failure of (a) switch S_1 (b) switch S_2 (c) switches S_1 and S_2 (d) switch $S_{3,1}$ (e) switch $S_{3,2}$, and (f) switches $S_{3,1}$ and $S_{3,2}$

Chapter 4

4 Conclusion and Future Works

In this work, a bidirectional dc–dc converter using SiC MOSFETs was proposed that can produce a 5-level voltage at the primary side of the high-frequency transformer. Fundamental and complete control methods based on the Fourier analysis were proposed for the proposed bidirectional dc-dc converter. The proposed structure has the merit of higher efficiency, fault-tolerant capability, and smaller filter size in comparison to the common dual-active FBCs. The switching strategies for optimal operation of the proposed converter considering core loss of the high-frequency transformer and transferred reactive power was analyzed. Optimal switching angles were determined for minimizing rms current and reactive power leading to higher efficiency. For the construction of the laboratory prototype, a laminated dc-link was designed. Laboratory experiments were carried out for step-down and step-up operation to verify the operation of the proposed converter. In addition, post-fault switching strategies were investigated in detail. Prototype experiments were carried out to show and verify the operation of the proposed converter in faulty conditions. Three open-circuit fault cases were studied. In each

case, the alternate switching pattern can continue supplying the load, though with a reduced number of voltage levels. Dynamic measurements showed the converter switching from healthy to faulty operation. A deep-learning based fault detection method has been proposed for dual-active 5-level dc-dc converter to detect and locate the open-circuit failures of each power electronic switch. To verify the effectiveness of the proposed model a deep neural network was implemented, which contains five hidden layers including one Conv1D layer, two dense layers, one maxpooling1D layer, and one flatten layer. The total number of parameters is 2247, which makes this model a very lightweight and simple one. Using this architecture more than 98.25% accuracy was achieved and about 2.64 μs and 1.64 μs latencies arose using CPU and GPU, respectively. Furthermore, the proposed model does not need complex hyper-parameter adjusting process to obtain results. Real-time implementation of the proposed model is developed and successfully confirmed the functionality of the model. Finally, reconfigurations in the hardware level using the proposed switching methods in normal and faulty conditions along with the proposed detection and location method have been applied. The developed model was able to detect and locate single and double open-circuit failures in real-time experiments within 10-60 cycles.

For future works on this dissertation, the developed neural network-based fault diagnostic model could be optimized. Implementing the model at high

frequencies requires addressing radiated noise in the built circuit. Additionally, a modular topology of the proposed converter could be investigated for higher voltage applications.

Bibliography

[1] P. L. Métayer, Q. Loeuillet, F. Wallart, C. Buttay, D. Dujic, and P. Dworakowski, "Phase-Shifted Full Bridge DC–DC Converter for Photovoltaic MVDC Power Collection Networks," *IEEE Access*, vol. 11, pp. 19039–19048, 2023, doi: 10.1109/ACCESS.2023.3247952.

[2] P. García-Triviño, L. De Oliveira-Assís, E. P. P. Soares-Ramos, R. Sarrias-Mena, C. A. García-Vázquez, and L. M. Fernández-Ramírez, "Supervisory Control System for a Grid-Connected MVDC Microgrid Based on Z-Source Converters With PV, Battery Storage, Green Hydrogen System and Charging Station of Electric Vehicles," *IEEE Trans. Ind. Appl.*, vol. 59, no. 2, pp. 2650–2660, Mar. 2023, doi: 10.1109/TIA.2022.3233556.

[3] M. Yang, X. Cai, A. Wusiman, J. Zhang, and J. Lyu, "Distributed-Diode-Rectifiers-Based Offshore Wind Power MVDC Direct-Transmission System," *IEEE Trans. Energy Convers.*, vol. 37, no. 1, pp. 643–653, Mar. 2022, doi: 10.1109/TEC.2021.3110525.

[4] L. Zheng, R. P. Kandula, and D. Divan, "Current-Source Solid-State DC Transformer Integrating LVDC Microgrid, Energy Storage, and Renewable Energy Into MVDC Grid," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 1044–1058, Jan. 2022, doi: 10.1109/TPEL.2021.3101482.

[5] M. Abbasi, R. Emamalipour, M. A. M. Cheema, and J. Lam, "A Constant-Frequency High-Voltage Gain Resonant Converter Module With Semiactive Phase-Shifted Voltage Multiplier for MVdc Distribution," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 4, pp. 3603–3616, Aug. 2022, doi: 10.1109/JESTPE.2021.3088120.

[6] J. Fabre *et al.*, “Characterization and Implementation of Resonant Isolated DC/DC Converters for Future MVdc Railway Electrification Systems,” *IEEE Trans. Transp. Electrification*, vol. 7, no. 2, pp. 854–869, Jun. 2021, doi: 10.1109/TTE.2020.3033659.

[7] A. R. Sadat and H. S. Krishnamoorthy, “Fault-Tolerant ISOSP Solid-State Transformer for MVdc Distribution,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 6, pp. 6985–6996, Dec. 2021, doi: 10.1109/JESTPE.2020.3032832.

[8] W. Chen, T. Liang, and V. Dinavahi, “Comprehensive Real-Time Hardware-In-the-Loop Transient Emulation of MVDC Power Distribution System on Nuclear Submarine,” *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 326–339, 2020, doi: 10.1109/OJIES.2020.3036731.

[9] M. Abbasi and J. Lam, “A Bridgeless AC/DC High Voltage Gain Converter With Three-Phase Modular Series-Output Connected Configuration for MVDC Grid Applications,” *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10323–10337, Oct. 2020, doi: 10.1109/TPEL.2020.2977912.

[10] L. Zhou *et al.*, “Virtual Positive-Damping Reshaped Impedance Stability Control Method for the Offshore MVDC System,” *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4951–4966, May 2019, doi: 10.1109/TPEL.2018.2865446.

[11] U. Javaid, F. D. Freijedo, D. Dujic, and W. Van Der Merwe, “Dynamic Assessment of Source–Load Interactions in Marine MVDC Distribution,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4372–4381, Jun. 2017, doi: 10.1109/TIE.2017.2674597.

[12] G. Yang, F. Xiao, X. Fan, R. Wang, and J. Liu, “Three-Phase Three-Level Phase-Shifted PWM DC–DC Converter for Electric Ship MVDC Application,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 162–170, Mar. 2017, doi: 10.1109/JESTPE.2016.2620282.

[13] J. Siegers, S. Arrua, and E. Santi, “Stabilizing Controller Design for Multibus MVdc Distribution Systems Using a Passivity-Based Stability Criterion and Positive Feedforward Control,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 14–27, Mar. 2017, doi: 10.1109/JESTPE.2016.2618382.

[14] M. T. Daniel, H. S. Krishnamoorthy, and P. N. Enjeti, “A New Wind Turbine Interface to MVdc Collection Grid With High-Frequency Isolation and Input Current Shaping,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 4, pp. 967–976, Dec. 2015, doi: 10.1109/JESTPE.2015.2443843.

[15] A. H. Wijenayake *et al.*, “Next-generation MVDC architecture based on 6.5 kV / 200 A, 12.5 mΩ SiC H-bridge and 10 kV / 240 A, 20 mΩ SiC dual power modules,” in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, Arlington, VA, USA: IEEE, Aug. 2017, pp. 598–604. doi: 10.1109/ESTS.2017.8069343.

[16] S. Das and P. Swarnkar, “Fuzzy Logic Control of DC-DC converters for Navy shipboard Medium Voltage DC Distribution System,” in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, India: IEEE, Jul. 2016, pp. 1–5. doi: 10.1109/ICPEICES.2016.7853416.

[17] P. Kankanala, S. C. Srivastava, A. K. Srivastava, and N. N. Schulz, “Optimal Control of Voltage and Power in a Multi-Zonal MVDC Shipboard Power System,” *IEEE Trans. Power Syst.*, vol. 27, no. 2, pp. 642–650, May 2012, doi: 10.1109/TPWRS.2011.2178274.

[18] Y. Chen, Z. Li, S. Zhao, X. Wei, and Y. Kang, “Design and Implementation of a Modular Multilevel Converter With Hierarchical Redundancy Ability for Electric Ship MVDC System,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 189–202, Mar. 2017, doi: 10.1109/JESTPE.2016.2632858.

[19] C.-L. Su, K.-L. Lin, and C.-J. Chen, "Power Flow and Generator-Converter Schemes Studies in Ship MVDC Distribution Systems," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 50–59, Jan. 2016, doi: 10.1109/TIA.2015.2463795.

[20] H. Alafnan *et al.*, "Stability Improvement of DC Power Systems in an All-Electric Ship Using Hybrid SMES/Battery," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 3, pp. 1–6, Apr. 2018, doi: 10.1109/TASC.2018.2794472.

[21] C. N. Doerry, "Next Generation Integrated Power Systems (NGIPS) for the Future Fleet," p. 21, 2009.

[22] "IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships," *IEEE Std 1709-2010*, pp. 1–54, Nov. 2010, doi: 10.1109/IEEESTD.2010.5623440.

[23] F. Wang, Z. Zhang, T. Ericsen, R. Raju, R. Burgos, and D. Boroyevich, "Advances in Power Conversion and Drives for Shipboard Systems," *Proc. IEEE*, vol. 103, no. 12, pp. 2285–2311, Dec. 2015, doi: 10.1109/JPROC.2015.2495331.

[24] H. V. M., C. Kumar, and M. Liserre, "An MVDC-Based Meshed Hybrid Microgrid Enabled Using Smart Transformers," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3722–3731, Apr. 2022, doi: 10.1109/TIE.2021.3071683.

[25] K. Varesi, S. H. Hosseini, M. Sabahi, and E. Babaei, "Modular non-isolated multi-input high step-up dc–dc converter with reduced normalised voltage stress and component count," *IET Power Electron.*, vol. 11, no. 6, pp. 1092–1100, 2018, doi: 10.1049/iet-pel.2017.0483.

[26] Hui Li, Fang Zheng Peng, and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 525–535, Mar. 2003, doi: 10.1109/TIA.2003.808965.

[27] L. Wang, Q. Zhu, W. Yu, and A. Q. Huang, “A Medium-Voltage Medium-Frequency Isolated DC–DC Converter Based on 15-kV SiC MOSFETs,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 100–109, Mar. 2017, doi: 10.1109/JESTPE.2016.2639381.

[28] S. Inoue and H. Akagi, “A Bidirectional Isolated DC–DC Converter as a Core Circuit of the Next-Generation Medium-Voltage Power Conversion System,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 535–542, Mar. 2007, doi: 10.1109/TPEL.2006.889939.

[29] H. Akagi and R. Kitada, “Control and Design of a Modular Multilevel Cascade BTB System Using Bidirectional Isolated DC/DC Converters,” *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2457–2464, Sep. 2011, doi: 10.1109/TPEL.2011.2107752.

[30] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich, “Busbar design for SiC-based H-bridge PEBB using 1.7 kV, 400 a SiC MOSFETs operating at 100 kHz,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–7. doi: 10.1109/ECCE.2016.7854903.

[31] G. G. Oggier and M. Ordonez, “High-Efficiency DAB Converter Using Switching Sequences and Burst Mode,” *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2069–2082, Mar. 2016, doi: 10.1109/TPEL.2015.2440753.

[32] A. Garcia-Bediaga, I. Villar, A. Rujas, I. Etxeberria-Otadui, and A. Rufer, “Analytical Models of Multiphase Isolated Medium-Frequency DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2508–2520, Apr. 2017, doi: 10.1109/TPEL.2016.2570941.

[33] Z. Zheng, Z. Gao, C. Gu, L. Xu, K. Wang, and Y. Li, “Stability and Voltage Balance Control of a Modular Converter With Multiwinding High-Frequency Transformer,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4183–4194, Aug. 2014, doi: 10.1109/TPEL.2013.2290019.

[34] H. Fan and H. Li, "High-Frequency Transformer Isolated Bidirectional DC–DC Converter Modules With High Efficiency Over Wide Load Range for 20 kVA Solid-State Transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3599–3608, Dec. 2011, doi: 10.1109/TPEL.2011.2160652.

[35] S. Madhusoodhanan *et al.*, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3343–3360, Jul. 2015, doi: 10.1109/TIA.2015.2412096.

[36] A. K. Tripathi *et al.*, "Design Considerations of a 15-kVSiCIGBT-Based Medium-Voltage High-Frequency Isolated DC–DC Converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3284–3294, Jul. 2015, doi: 10.1109/TIA.2015.2394294.

[37] R. M. Burkart and J. W. Kolar, "Comparative η– ρ– σ Pareto Optimization of Si and SiC Multilevel Dual-Active-Bridge Topologies With Wide Input Voltage Range," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5258–5270, Jul. 2017, doi: 10.1109/TPEL.2016.2614139.

[38] A. Deshpande and F. Luo, "Multilayer busbar design for a Si IGBT and SiC MOSFET hybrid switch based 100 kW three-level T-type PEBB," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2017, pp. 20–24. doi: 10.1109/WiPDA.2017.8170496.

[39] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013, doi: 10.1109/TPEL.2012.2203151.

[40] J. He, N. A. O. Demerdash, N. Weise, and R. Katebi, "A Fast On-Line Diagnostic Method for Open-Circuit Switch Faults in SiC-MOSFET-Based T-Type Multilevel Inverters," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2948–2958, May 2017, doi: 10.1109/TIA.2016.2647720.

[41] A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen, and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 407–416, Mar. 2020, doi: 10.1109/JESTPE.2019.2952367.

[42] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013, doi: 10.1109/TIE.2012.2233698.

[43] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 855–865, May 2005, doi: 10.1109/TIA.2005.847285.

[44] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated DC/DC Structure Based on Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015, doi: 10.1109/TPEL.2014.2305976.

[45] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and Control of the Isolated DC–DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017, doi: 10.1109/JESTPE.2016.2615071.

[46] Y. Shi and H. Li, "Isolated Modular Multilevel DC–DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2145–2161, Mar. 2018, doi: 10.1109/TPEL.2017.2695575.

[47] S. Cui, N. Soltau, and R. W. De Doncker, “A High Step-Up Ratio Soft-Switching DC–DC Converter for Interconnection of MVDC and HVDC Grids,” *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018, doi: 10.1109/TPEL.2017.2702207.

[48] X. Xiang, X. Zhang, G. P. Chaffey, and T. C. Green, “An Isolated Resonant Mode Modular Converter With Flexible Modulation and Variety of Configurations for MVDC Application,” *IEEE Trans. Power Deliv.*, vol. 33, no. 1, pp. 508–519, Feb. 2018, doi: 10.1109/TPWRD.2017.2735634.

[49] R. Xie and H. Li, “Fault Performance Comparison Study of a Dual Active Bridge (DAB) Converter and an Isolated Modular Multilevel DC/DC (iM2DC) Converter for Power Conversion Module Application in a Breaker-Less Shipboard MVDC System,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5444–5455, Sep. 2018, doi: 10.1109/TIA.2018.2794355.

[50] T. Zheng *et al.*, “A Novel High-Voltage DC Transformer Based on Diode-Clamped Modular Multilevel Converters With Voltage Self-Balancing Capability,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10304–10314, Dec. 2020, doi: 10.1109/TIE.2019.2962486.

[51] S. Guo, P. Liu, L. Zhang, and A. Q. Huang, “Design and optimization of the high frequency transformer for a 800V/1.2MHz SiC LLC resonant converter,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 5317–5323. doi: 10.1109/ECCE.2017.8096892.

[52] N. Keshmiri, M. I. Hassan, R. Rodriguez, and A. Emadi, “Comparison of Isolated Bidirectional DC/DC Converters Using WBG Devices for More Electric Aircraft,” *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 184–198, 2021, doi: 10.1109/OJIES.2021.3058196.

[53] H. Keyhani and H. A. Toliyat, “Partial-Resonant Buck–Boost and Flyback DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4357–4365, Aug. 2014, doi: 10.1109/TPEL.2014.2301094.

[54] R.-L. Lin and C.-W. Lin, “Design criteria for resonant tank of LLC DC-DC resonant converter,” in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Nov. 2010, pp. 427–432. doi: 10.1109/IECON.2010.5674988.

[55] W. Chen, P. Rong, and Z. Lu, “Snubberless Bidirectional DC–DC Converter With New CLLC Resonant Tank Featuring Minimized Switching Loss,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010, doi: 10.1109/TIE.2009.2037099.

[56] S. Inoue, M. Ishigaki, A. Takahashi, and T. Sugiyama, “Design of an Isolated Bidirectional DC–DC Converter With Built-in Filters for High Power Density,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 739–750, Jan. 2021, doi: 10.1109/TPEL.2020.3003618.

[57] M. Schulz and S. Ditze, “Analysis and Experimental Verification of an Isolated Half-Bridge Bidirectional DC−DC Converter,” *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5089–5106, May 2022, doi: 10.1109/TPEL.2021.3127125.

[58] H. Higa, S. Takuma, K. Orikawa, and J. Itoh, “Dual active bridge DC-DC converter using both full and half bridge topologies to achieve high efficiency for wide load,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 6344–6351. doi: 10.1109/ECCE.2015.7310549.

[59] J. Li, Q. Luo, T. Luo, D. Mou, and M. Liserre, “Efficiency Optimization Scheme for Isolated Triple Active Bridge DC–DC Converter With Full Soft-Switching and Minimized RMS Current,” *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9114–9128, Aug. 2022, doi: 10.1109/TPEL.2022.3157443.

[60] E. S. Oluwasogo and H. Cha, "A Quadratic Quasi-Z-Source Full-Bridge Isolated DC–DC Converter With High Reliability for Wide Input Applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10090–10100, Oct. 2022, doi: 10.1109/TIE.2022.3159955.

[61] M. Chai, N. B. Y. Gorla, and S. K. Panda, "Fault Detection and Localization for Cascaded H-Bridge Multilevel Converter With Model Predictive Control," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10109–10120, Oct. 2020, doi: 10.1109/TPEL.2020.2978670.

[62] S. Ye, J. Jiang, Z. Zhou, C. Liu, and Y. Liu, "A Fast and Intelligent Open-Circuit Fault Diagnosis Method for a Five-Level NNPP Converter Based on an Improved Feature Extraction and Selection Model," *IEEE Access*, vol. 8, pp. 52852–52862, 2020, doi: 10.1109/ACCESS.2020.2981247.

[63] S.-H. Kim, D.-Y. Yoo, S.-W. An, Y.-S. Park, J.-W. Lee, and K.-B. Lee, "Fault Detection Method Using a Convolution Neural Network for Hybrid Active Neutral-Point Clamped Inverters," *IEEE Access*, vol. 8, pp. 140632–140642, 2020, doi: 10.1109/ACCESS.2020.3011730.

[64] S. Kwak, "Fault-Tolerant Structure and Modulation Strategies With Fault Detection Method for Matrix Converters," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1201–1210, May 2010, doi: 10.1109/TPEL.2009.2040001.

[65] S. Khwan-on, L. de Lillo, L. Empringham, and P. Wheeler, "Fault-Tolerant Matrix Converter Motor Drives With Fault Detection of Open Switch Faults," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 257–268, Jan. 2012, doi: 10.1109/TIE.2011.2162711.

[66] M. Shahbazi, P. Poure, S. Saadate, and M. R. Zolghadri, "FPGA-Based Fast Detection With Reduced Sensor Count for a Fault-Tolerant Three-Phase Converter," *IEEE Trans. Ind. Inform.*, vol. 9, no. 3, pp. 1343–1350, Aug. 2013, doi: 10.1109/TII.2012.2209665.

[67] A. Yazdani, H. Sepahvand, M. L. Crow, and M. Ferdowsi, "Fault Detection and Mitigation in Multilevel Converter STATCOMs," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1307–1315, Apr. 2011, doi: 10.1109/TIE.2010.2050415.

[68] J. Lamb and B. Mirafzal, "Open-Circuit IGBT Fault Detection and Location Isolation for Cascaded Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4846–4856, Jun. 2017, doi: 10.1109/TIE.2017.2674629.

[69] W. Zhou, J. Sheng, H. Luo, W. Li, and X. He, "Detection and Localization of Submodule Open-Circuit Failures for Modular Multilevel Converters With Single Ring Theorem," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3729–3739, Apr. 2019, doi: 10.1109/TPEL.2018.2849441.

[70] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721–2732, May 2015, doi: 10.1109/TPEL.2014.2348194.

[71] Q. Yang, J. Qin, and M. Saeedifard, "Analysis, Detection, and Location of Open-Switch Submodule Failures in a Modular Multilevel Converter," *IEEE Trans. Power Deliv.*, vol. 31, no. 1, pp. 155–164, Feb. 2016, doi: 10.1109/TPWRD.2015.2477476.

[72] D. Zhou, S. Yang, and Y. Tang, "A Voltage-Based Open-Circuit Fault Detection and Isolation Approach for Modular Multilevel Converters With Model-Predictive Control," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9866–9874, Nov. 2018, doi: 10.1109/TPEL.2018.2796584.

[73] S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson, "Fault Detection for Modular Multilevel Converters Based on Sliding Mode Observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013, doi: 10.1109/TPEL.2013.2242093.

[74] P. Hekmati, I. P. Brown, and Z. J. Shen, “Open Circuit Switch Fault Detection in Flying Capacitor and Cascaded H-Bridge Multilevel Converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12332–12341, Nov. 2021, doi: 10.1109/TPEL.2021.3078158.

[75] J.-S. Lee, K.-B. Lee, and F. Blaabjerg, “Open-Switch Fault Detection Method of a Back-to-Back Converter Using NPC Topology for Wind Turbine Systems,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 325–335, Jan. 2015, doi: 10.1109/TIA.2014.2327151.

[76] P. Achintya and L. Kumar Sahu, “Open Circuit Switch Fault Detection in Multilevel Inverter Topology using Machine Learning Techniques,” in *2020 IEEE 9th Power India International Conference (PIICON)*, Feb. 2020, pp. 1–6. doi: 10.1109/PIICON49524.2020.9112870.

[77] W. Xing *et al.*, “An Open-circuit Fault Detection and Location Strategy for MMC with Feature Extraction and Random Forest,” in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 1111–1116. doi: 10.1109/APEC42165.2021.9487126.

[78] W. Xing, H. Yang, J. Sheng, X. Chang, W. Li, and X. He, “Open-circuit Fault Detection and Location in MMCs with Multivariate Gaussian Distribution,” in *2020 4th International Conference on HVDC (HVDC)*, Nov. 2020, pp. 555–559. doi: 10.1109/HVDC50696.2020.9292753.

[79] N. Torabi, F. Naghavi, and H. A. Toliyat, “Real-time fault isolation in multiphase multilevel NPC converters using active semi-supervised fuzzy clustering algorithm with pairwise constraints,” in *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, May 2017, pp. 1–7. doi: 10.1109/IEMDC.2017.8002409.

[80] N. Torabi, V. M. Sundaram, and H. A. Toliyat, “On-line fault diagnosis of multi-phase drives using self-recurrent wavelet neural networks with adaptive learning rates,” in *2017 IEEE*

Applied Power Electronics Conference and Exposition (APEC), Mar. 2017, pp. 570–577. doi: 10.1109/APEC.2017.7930751.

[81] S. Kiranyaz, A. Gastli, L. Ben-Brahim, N. Al-Emadi, and M. Gabbouj, "Real-Time Fault Detection and Identification for MMC Using 1-D Convolutional Neural Networks," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8760–8771, Nov. 2019, doi: 10.1109/TIE.2018.2833045.

[82] T. Wang, H. Xu, J. Han, E. Elbouchikhi, and M. E. H. Benbouzid, "Cascaded H-Bridge Multilevel Inverter System Fault Diagnosis Using a PCA and Multiclass Relevance Vector Machine Approach," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7006–7018, Dec. 2015, doi: 10.1109/TPEL.2015.2393373.

[83] S. Kargar, H. Litz, and F. Nawab, "Predict and Write: Using K-Means Clustering to Extend the Lifetime of NVM Storage," in *2021 IEEE 37th International Conference on Data Engineering (ICDE)*, Chania, Greece: IEEE, Apr. 2021, pp. 768–779. doi: 10.1109/ICDE51399.2021.00072.

[84] "Principal component analysis: a review and recent developments." Accessed: Feb. 18, 2024. [Online]. Available: https://royalsocietypublishing.org/doi/epdf/10.1098/rsta.2015.0202