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New Techniques for Future RF and Millimeter Wave Radios

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New Techniques for Future RF and Millimeter Wave Radios

A dissertation submitted in partial satisfaction

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Doctor of Philosophy in Electrical and Computer Engineering

by

Seyyed Hossein Razavi

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ABSTRACT OF THE DISSERTATION

New Techniques for Future
RF and Millimeter Wave Radios

by

Seyyed Hossein Razavi
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2021
Professor Behzad Razavi, Chair

This dissertation consists of two parts. In the first part, a broadband universal receiver is proposed with channel selection and blocker rejection that achieves a low noise figure and high linearity through an innovative use of feedback techniques. It also demonstrates ample harmonic rejection owing to its newly proposed harmonic trap method with no calibration required. Realized in 28-nm CMOS technology, the receiver exhibits a noise figure of 2.1 dB and a third and fifth harmonic rejection of more than 60.8 dB up to 2 GHz while consuming 49 mW.

In the second part, we introduce a a new linear, time-variant model that provides a general framework for understanding and modeling of injection locking in oscillators and frequency dividers. Application of the proposed model to direct injection locked frequency dividers (DILFDs) results in new insights and design optimization criteria which highly improves the divider lock range and power consumption. Two DILFD prototypes have been fabricated: A 1.88-mW single DILFD that operates from 26 GHz to 63 GHz and a 4.76-mW coupled DILFD that operates from 24 GHz to 73 GHz with no need for tuning or adjustments.

The dissertation of Seyyed Hossein Razavi is approved.

Chee Wei Wong

Gregory J. Pottie

Danijela Cabric

Behzad Razavi, Committee Chair

University of California, Los Angeles

2021

To my parents . . .

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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CHAPTER 1

Introduction

This dissertation includes two separate parts. The first part deals with developing a universal receiver for wireless applications in the RF range. The second part introduces a new frame work for the analysis of injection locking and develops millimeter wave frequency dividers with unprecedented lock range.

Today's mobile devices must support more than 15 cellular and WiFi bands. Radios serving in such an environment require many off-chip front-end filters, occupy a large chip area, and pose severe difficulties in generation and distribution of the local oscillator (LO) signals. Hence, an RF universal receiver, capable of receiving at various standards over different frequency bands is of high demand. Such a receiver, however, needs to overcome numerous challenges, specifically, wideband low noise performance with sufficient input matching, sufficient in-band and out-of-band linearity with no prior filtering of the blockers and adequate rejection of the blockers located at the harmonics of the LO all within a limited power budget. Chapter 2 describes the steps toward developing such a receiver. Section 2.1 explains the challenges of designing a universal receiver. Section 2.2 provides the background for this work, and section 2.3 deals with the performance requirements. Section 2.4 presents the receiver front-end design and section 2.5 describes our proposed harmonic rejection technique. Section 2.6 explains clock generation circuits and section 2.7 summarizes the experimental results followed by the conclusion of the universal receiver design in section 2.8.

As the wireless and wireline systems push for higher frequencies, millimeter wave frequency synthesis is becoming a critical challenge. As an essential block inside any frequency synthe-

sizer, the frequency dividers should also be revisited and improved to be able to deliver required performance at millimeter wave frequencies. Chapter 3 introduces a new analysis framework for injection locking and its applications to direct injection locked frequency dividers (DILFDs). Section 3.1 explains the challenges in understanding and analyzing the injection locking phenomenon. Section 3.2 presents our proposed injection locking model for oscillators. Section 3.3 extends the method to DILFDs. Section 3.4 discusses the idea of quadrature coupling and its design considerations. Section 3.5 deals with the circuit implementation and section 3.6 summarizes the experimental results. Finally this chapter is concluded in section 3.7.

CHAPTER 2

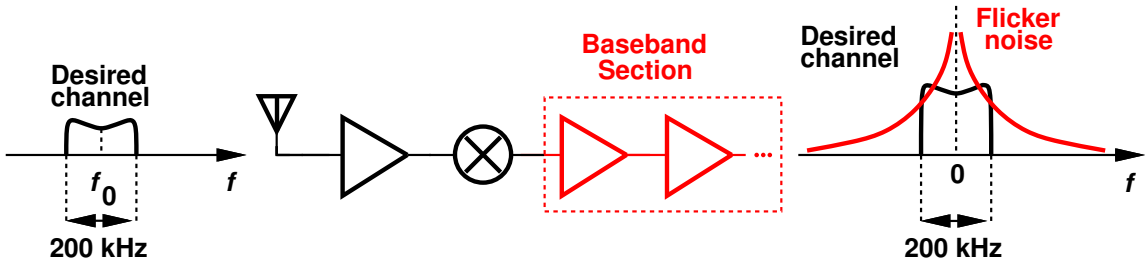
A Universal Receiver for Sub-6 GHz Wireless Applications

2.1 Problem Statement

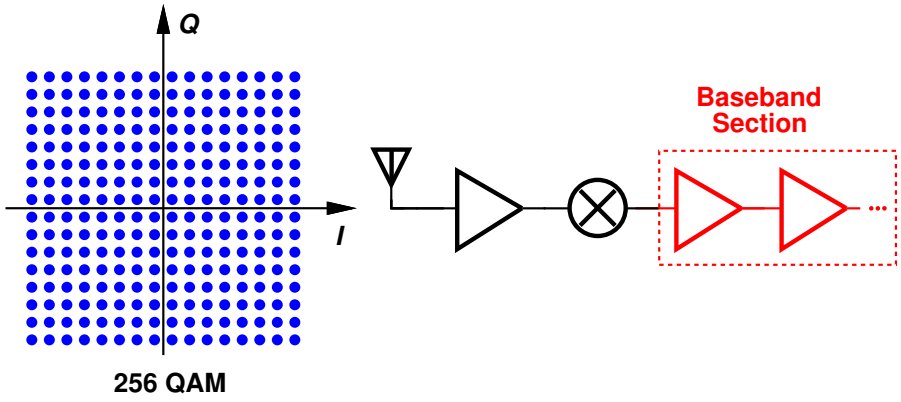
The idea of Having a wideband receiver, capable of receiving signals at various standard has long been a fascinating objective for RF designers. However, there have been several obstacles in realizing such a system. 1) The receiver must be able to maintain good noise performance, input matching and sufficient gain over a wide RF bandwidth and for different channel bandwidths based on the standard. 2) The baseband section must be able to support signal processing up to wide channel bandwidths of the new WiFi 6 standard with sufficient gain and acceptable power consumption. 3) It must be able to maintain required linearity measures. To this end, it needs to select a band and reject large out-of-band blockers and in-band interferers. 4) Since in many cases, harmonics of the desired signal fall inside the receiver bandwidth, the system must be able to reject the harmonics and prevent them from being folded back on the desired signal.

In order to have a clear vision of the mentioned problems we start with the problem of flicker noise. As depicted in Fig.2.1a in any RF receiver, the signal is eventually downconveted to the baseband. Now the flicker noise presented by the MOS devices in the baseband section becomes critical, especially for the narrow channel band width of cellular standards such as GSM. If we decide to use larger transistors to overcome this problem, the bandwidth will be limited and the receiver will not be able to receive 160 MHz channel of WiFi 6. And if more RF gain is implemented before the downconversion, linearity degrades and the receiver chain will compress in the presence of blockers.

Second challenge is about receiving wide band channels of WiFi 6. The baseband processing section must be able to receive high modulation index signals with a wide bandwidth (Fig.2.1b) such as 256-QAM, 160 MHz WiFi 6 signal . Therefore the baseband section must be wideband and linear enough to avoid signal corruption and at the same time we prefer to provide this wide bandwidth without a power consumption compromise.



(a)



(b)

Figure 2.1. (a) The problem of flicker noise in CMOS receivers and (b) an example of a 256-QAM wideband WiFi signal to be received the receiver.

Third challenge as depicted in Fig.2.2a, is that the input signal could be accompanied by a large out-of-band blocker. Since we are developing an ultra-wideband receiver, the out-of-band blocker is not attenuated by an off-chip filter. Hence, it is important to provide sufficient rejection for the blocker signal in the receiver chain. The resurrection of translational circuits ([1] and [2]) in the form of N-path filters ([3]) helped to alleviate this problem, although as mentioned in the

next section, it took an extensive effort to make the idea closer to practice.

Finally, we discuss the problem of harmonic rejection. In an ultra-wideband receiver, the blockers present at the higher harmonics of the desired signal will enter the receiver without any prior filtering (Fig.2.2b). This blockers will then get downconverted and fall on top of the desired signal and corrupt it. Therefore, it is important to avoid this undesirable problem by attenuating higher harmonics. This issue has recently been subject to an extensive research, however, the assumptions made and results obtained still do not meet the practical requirements as will be discussed in the next section.

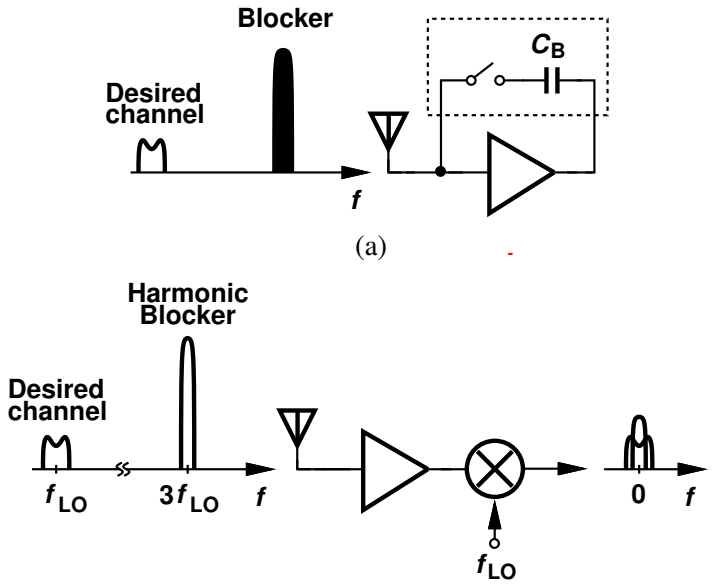


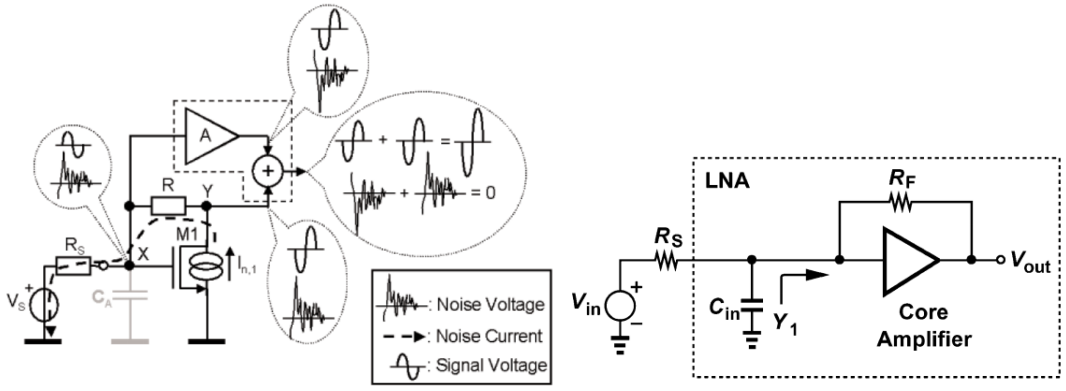
Figure 2.2. (a) The problem of large out-of-band blockers and (b) harmonic blockers in the radio receivers.

This paper introduces a new approach to receiver design that brings together low noise, sufficient linearity and wide band input matching over a wide frequency range while improving harmonic rejection considerably. These features make the proposed receiver architecture a good candidate for future radios. Implemented in 28-nm CMOS technology, the design exhibits a noise figure of 1.6-2.1 dB over the frequency range of 0.4-6 GHz, while supporting channel Bandwidths

From 200 kHz to 160 MHz. Additionally, It is able to tolerate 0-dBm out-of-band blockers and reject third and fifth harmonic blockers by more than 60.8 dB up to 2 GHz.

2.2 Background

Wideband low noise amplifiers with promising performances have been proposed in the papers for years ([4] and [5]). Fig.2.3a depicts a noise cancelling LNA ([4]) which cancel the noise of the input device using a feed-forward scheme. Fig.2.3b on the other hand, shows the concept of reactance cancelling LNA proposed by[5] which reduces the effect of the input noise device by cancelling half of its noise due to the global feedback used for input matching. A major obstacle in the way of wideband LNAs way to be used in a practical wideband receiver structure, is the problem of large interferers. In the absence of a passive filter preceding the LNA, large interferers reach the LNA without any attenuation and compress the receiver.

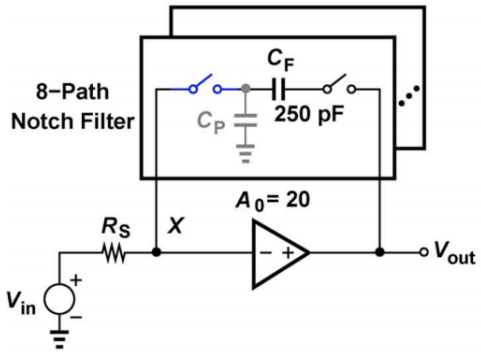


(a) (b)

Figure 2.3. (a) Noise cancelling LNA proposed in [4] and (b) reactance cancelling LNA proposed in [5].

To address this problem, a key element is a tunable bandpass filter that can sweep its center frequency across the entire receiver bandwidth. This demand was the reason for the resurgence of interest in frequency translational circuits and their most popular form which is N-path filter. N-path filters translate a baseband impedance to a desirable RF frequency by switching N replicas of

the baseband impedance with a set of N non-overlapping clocks. Despite the amazing property of frequency translation which made it possible to have band-pass filter with tunable center frequency, the original N-path structures suffered from several practical issues, resolving which was the subject of extensive study and research in recent years. First problem arises from the on-resistance of the N-path filter switches. The on-resistance of the switches limits the out of band rejection of the filter. This problem manifests itself in the presence of a large out-of-band blocker for which insufficient rejection leads to severe non-linearity in the receiver. Employing large switches to reject the out of band blockers is an approach taken by several papers ([6] and [7]), however it requires a large power consumption in the clock path to drive the switches. Moreover, it limits the RF bandwidth due to large parasitic capacitance of the switches on the RF side. On the other hand, [8] proposes utilizing the Miller effect by leveraging gain of an amplification stage which makes the switches smaller, hence consuming less power and supporting larger RF bandwidth (Fig. 2.4). However, The out-of-band blocker rejection is still limited and needs to be further improved.



(a)

Figure 2.4. Placing the N-path filter around a gain stage to benefit from the Miller multiplication proposed in [8].

Second major issue was the problem of center frequency shift in which the parasitic capacitance connected to the RF node, shifts the center frequency of the bandpass filter to the left side of LO frequency. This effect becomes more problematic as the desired RF frequency increases; hence the impedance of the parasitic capacitance becomes smaller and comparable with resistive load at the

RF node. There are two approaches to tackle the problem.

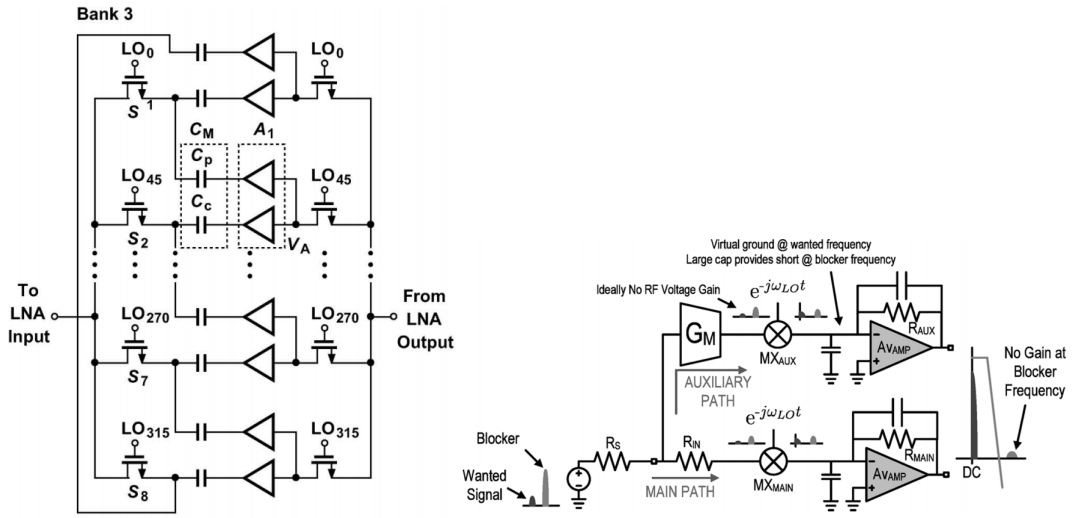


Figure 2.5. (a) Polyphase filtering proposed in [8] and (b) introducing low resistance using a translational feedback loop proposed in [7].

First approach is to utilize poly-phase operation in the N-path filter as in [8] and [9](Fig. 2.5a). Although able to solve the problem, this method has a major shortcoming, especially in the context of wideband receivers. Polyphase operation is only suitable for a specific frequency, so in order to receive the same channel bandwidth at different RF frequencies, different sets of polyphase capacitors are required. In other words, it is not a versatile solution. Second approach which has more interesting properties is basically avoiding this problem by exhibiting a low impedance to the RF node using a feedback in the baseband section([7] and [10]) as shown in Fig. 2.5b. By applying this idea, the impedance of the parasitic capacitance would be much larger than the small equivalent impedance connected to the RF node. In this method once the input voltage signal is converted to current in the RF amplifier, it will only be converted back to voltage in the baseband section, thus it does not need to deal with the parasitic capacitance of the RF node. This method has two more interesting properties: 1) Since it avoids voltage amplification until the baseband section and its amplification happens in the same stage as channel selection in baseband, it does not need to do any filtering on the close-in weak interferers on the RF side. In contrast architectures with RF

filtering need to perform channel selection at RF to filter the in-band interferers. 2) In the baseband section it is possible to afford for large resistors because of long channels of baseband transistors, therefore, smaller capacitors are required, hence the occupied area will be reduced. In contrast, in the case of RF filtering large resistors are not affordable and designs have to make advantage of the Miller effect to shrink the capacitor size.

Last issue to be addressed is not specific to N-path filters and applies to every N-phase mixer. It is the problem of harmonic rejection. For any N-phase mixing system, harmonics of number $kN \pm 1 (k \in \mathbb{Z})$ will inevitably be folded back on the first harmonic signal. But the fold-back of other harmonics can be avoided through the use of harmonic rejection combining after the mixer. The original idea proposed in [11] (Fig. 2.6) was presented on a 3-path mixer with three clock phases spaced 45° away from each other. Same concept was then used in 8-path structures ([8], [7] and [12]). This method, in essence, reconstructs the sine and cosine waveforms by adding eight phases of square waves spaced equally with proper weighting.

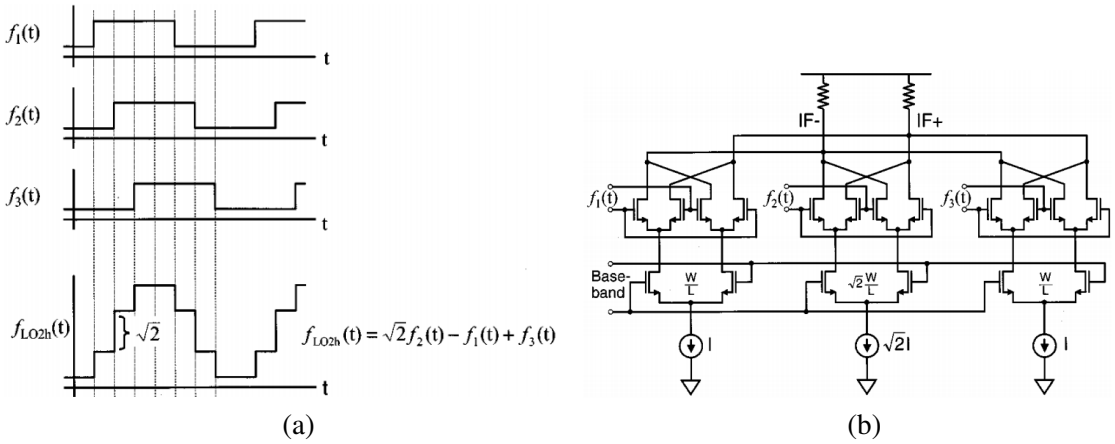
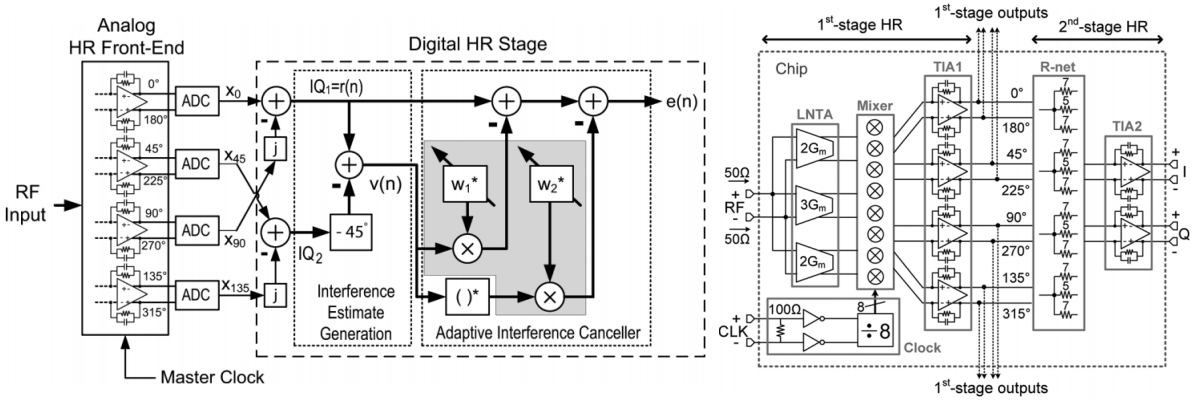


Figure 2.6. (a) The idea of harmonic mixing proposed in [11] and (b) its implementation.

While working perfect in theory, this method has its own limits. Systematic mismatches in the layout and mismatches due to process variation will affect both phase accuracy of the LO signals and gain accuracy of the weighting circuit, resulting in limited harmonic rejection. Most common architectures of harmonic combining use 8-phase clocks which makes the fold-back of seventh and ninth harmonic inevitable. Among the harmonics between second and sixth, even harmonics

are of less interest since their rejection depends only on the accuracy of differential clocks and amplifiers, therefore, they experience sufficient levels of rejection. Third and fifth harmonics, however, do not get attenuated adequately and have been subject to extensive research recently. In the recent literature, two approaches have been taken to alleviate this issue.



(a) (b)

Figure 2.7. (a) Using an equalization technique to reject a single harmonic blocker proposed in [13] and (b) the idea of two stage harmonic rejection proposed in [13].

First, is to use an equalization technique to cancel the folded harmonic in the baseband after conversion to baseband ([13], [14], and [15]). Fig. 2.7a depict the equalization method proposed by [13]. However, this method can only equalize for a specific harmonic at a time and needs calibration. [16] proposes a 32-phase mixing solution which puts the desired signal on a higher harmonic of LO and makes it possible to reject more than one harmonic simultaneously using the equalization technique, however, using a sub-harmonic LO is not desirable. Suppose the desired signal is on the $k^{th}, (k \in \mathbb{Z})$ harmonic of the LO. Then the number of mixing spurs is multiplied by a factor of k which the proposed receiver is not capable of handling. Second approach, first introduced in [13] (Fig. 2.7b) and then utilized in other papers such as [10] and [17], is calibration free and can reject third and fifth harmonics at the same time. It is based on dividing the weighting operation of harmonic combining to two cascaded stages, one in baseband and one in RF, hence, making the harmonic rejection a product of two independent mismatches which reduces the effect of gain mismatch by $\sim$46 dB. However, this method has has several deficiencies. First, it is lim-

ited by phase mismatch far before it can realize the 46-dB improvement. Second, it is suitable for differential RF inputs which calls for an off-chip balun that directly increases the noise figure by at least 1 dB at the input. Third, it does not lend itself to wideband low noise designs easily. Finally, the proposed prototype in [13] relies on $8f_{LO}$ input clock and a power hungry clock generation circuit to obtain small clock phase mismatch. [10] is an attempt to fit this idea to a frequency translational noise cancelling (FTNC) receiver and provides a single ended prototype too. However, it ended up in a complex architecture and eventually the single-ended prototype harmonic rejection was not promising.

2.3 Performance Requirements

Before presenting the proposed receiver, it is important to review the design specifications and requirements. We start with RF bandwidth. The newest WiFi 6 release based on 802.11ax standard, operates up to 5GHz band similar to its predecessor 802.11ac. Considering our objective to have a universal receiver that supports all the previous standards in the sub-6 GHz band as well as newly defined standards, we seek a receiver whose RF bandwidth covers 400MHz to 6 GHz.

In terms of channel bandwidth, the proposed receiver must be able to cover all defined channel bandwidths for the standards defined in the sub-6 GHz band. To show its performance at extreme cases, it should be able to support 200 kHz bandwidth of GSM as well as 160 MHz bandwidth required by 802.11ax.

In other words, our receiver must provide required gain, noise figure and input matching over the entire 6 GHz bandwidth and it should be able to maintain these specifications over the channel bandwidth of interest at each standard while performing the channel selection filtering. Regarding the noise performance, we aim to provide a noise figure of less than 2 dB over the entire RF bandwidth. Finally, the receiver should be able to provide an S_{11} <-10 dB over the entire channel bandwidth while maintaining its performance over the 6 GHz RF range.

It is also important to mention the stringent blocker requirements of GSM standard which

we will be addressing as the most extreme case of blocker tolerance. According to the GSM requirement, the receiver must be able to tolerate a 0 dBm blocker as close as 23 MHz from the desired channel.

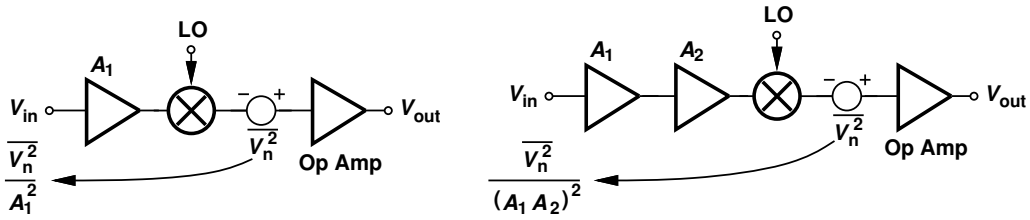
Another important specification to consider is harmonic rejection. Since the proposed receiver must cover a bandwidth of 400 MHz – 6 GHz, third and fifth harmonics of the desired channel fall inside the receive band and will be translated to the first harmonic due to phase and gain mismatches in the mixer and N-path filters. Considering maximum RF frequency of 6 GHz, our goal is to provide more than 60 dB rejection for the third and fifth harmonic up to 2 GHz. To summarize our receiver specifications, we aim to build a receiver that provides S_{11} <-10 dB and NF<2 dB from 400 MHz to 6 GHz, supporting channel bandwidths of 200 kHz-160 MHz. It should be capable of tolerating large out-of-band blockers, specifically 0 dBm blocker at 23 MHz offset while receiving GSM signals and providing sufficient in-band linearity. Additionally, this receiver must provide more than 60 dB rejection for third and fifth harmonics up to 2 GHz.

2.4 Receiver Front-End Design

2.4.1 Multi-Loop Architecture

According to the specifications defined in the previous section, we first recognize the noise figure requirement. Providing such a low noise figure over the anticipated wide RF bandwidth requires using a wideband low noise architecture. As mentioned in section 2.2, two major approaches have been introduced in the prior art. First approach is noise cancelling architecture first introduced in [4] and then fitted into an N-path version in [7]. Despite showing promising results, this method needs calibration and its calibration parameter might change at very high RF frequencies due to phase mismatch between main and auxiliary path. Second approach is to use a resistor in feedback around a high gain LNA, first introduced as reactance cancelling architecture [5] and then utilized in an N-path channel selection architecture [8] and in frequency translational feedback architectures ([18],[19] and [20]). In all of the previous utilizations of this method in receivers

with translational loops and N-path filters, they either fail to maintain S_{11} <-10 dB over the entire channel bandwidth or meet it marginally. This is a topic that we will discuss and resolve later in this section. For now, we will focus on another interesting problem arising from the fact that our receiver should be able to support 200 kHz channel bandwidth of cellular standards as well as 160 MHz of WiFi 6 which are different by a factor of 800. To support 200 kHz bandwidth with the noise figure of $\sim$2 dB we should make sure that our first baseband stage has large enough transistors whose flicker noise do not dominate the noise figure at 100 kHz (or even less) offset. In a regular receiver, first baseband stage (op amp) will be preceded by an RF gain stage - of gain A_1 – as shown in Fig. 2.8a to relax the noise requirements by reducing the noise of baseband transistors in the first baseband stage by a factor of A_1^2. In the case of our receiver, however, using this method does not suffice because even with a single RF gain stage , in order to keep noise figure in the required range, the transistors in the first baseband stage must be chosen so large that their parasitic capacitance does not allow receiving 160 MHz channel bandwidth. As will be discussed later in this section, we choose 40 nm channel length for our RF gain stages and we will use inverter architecture to reuse the current and maximize the gain which results in a gain of $\sim$19 dB. The idea is to add another gain stage – of gain A_2 – in cascade with the first gain stage as shown in Fig. 2.8b. This will boost the RF gain by a factor of $A_2 \approx 10$, which in turn improves the input referred flicker noise by a factor of 100. From another perspective, it would be possible to maintain the same noise performance with baseband transistors shrunk by a factor of 100, making it possible to receive 160 MHz channels.



(a) (b)

Figure 2.8. (a) one and (b) two RF gain stages preceding the baseband stage (op amp).

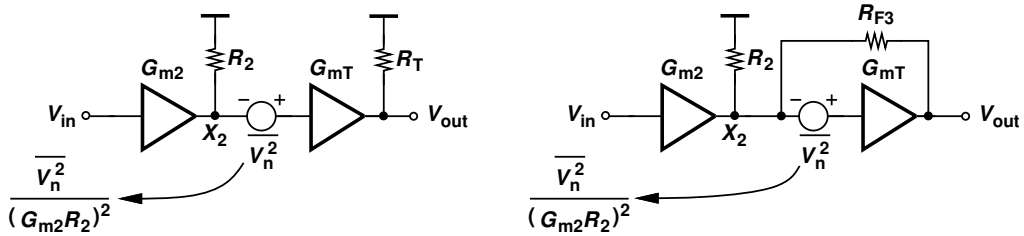
In spite of solving the conflict between flicker noise and 160 MHz channel reception, the idea

of preceding the baseband stage with a large RF gain has its own shortcomings. While the out-of-band blockers will be handled in the RF gain stages using N-path filters and will be discussed later, close-in interferers at the input of the LNA can cause large swings at the output of first and second RF gain stages which results in receiver non-linearity. To overcome this problem, we start with an observation. Suppose in the circuit of Fig. 2.8a we replace the A_2 and the op amp stage with their transistor small signal equivalents as in Fig. 2.9a. We have also removed the mixers and are analyzing the baseband equivalent of the transnational circuit. Now we can write the input referred noise of the op amp stages as:

$$V_{n,input}^2 = \frac{V_n^2}{(G_{m2}R_2)^2} \tag{2.1}$$

And the gain of the RF stage as:

$$\frac{V_{X_2}}{V_{in}} = -G_{m2}R_2 \tag{2.2}$$



(a) (b)

Figure 2.9. Baseband equivalent of an RF gain stage preceding the op amp (a) without feedback and (b) with feedback.

Now we add a feedback around the baseband stage as in Fig. 2.9b. We assume switch resistance of R_{sw} for the mixer and that the feedback resistor. Also, we assume that R_{F3} is much smaller than the output resistance of the op amp, R_T, and that $R_{F3} >> R_2$ which both are valid in this design. The input resistance looking at node X_2 is equal to $R_{X_2} = R_{sw} + 1/G_{mT}$. The RF gain from input to node X_2 could the be written as:

$$\frac{V_{X_2}}{V_{in}} = -G_{m2}(R_2||R_{X_2}) = -\frac{G_{m2}R_2}{1 + \frac{G_{mT}R_2}{1+G_{mT}R_{sw}}} \tag{2.3}$$

For the sake of simplicity we assume that $R_{X_2} << R_2$. This assumption will help simplifying the analysis of input referred noise. A more detailed analysis with more general assumptions is

presented in appendix I. the overall gain could be expressed as $V_{out}/V_{in} = G_{m2}R_{F3}$ and the output noise as $V_{n,out} = -[(R_{F3} + R_{sw} + R_2)/(R_{sw} + R_2)]V_n \approx -(R_{F3}/R_2)V_n$ which leads to an input referred noise of:

$$V^2_{n,input,CL} = \frac{V^2_{n,out}}{(\frac{V_{out}}{V_{in}})^2} = \frac{V^2_n}{(G_{m2}R_2)^2} \tag{2.4}$$

As evident from equations (2.1)-(2.4), the feedback method results in a reduced RF gain by a factor of $[1 + (G_{mT}R_2)/(1 + R_{sw}G_{mT})]^2$ while maintaining same noise performance as the open-loop configuration.

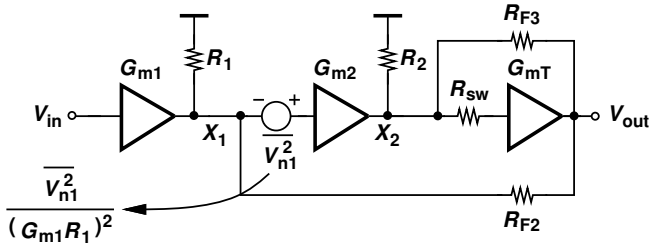


Figure 2.10. Baseband equivalent of two RF gain stages preceding the op amp with nested feedback.

Based on our observation, we now repeat this technique once more in the cascaded RF architecture of Fig. 2.9b that results in the circuit shown in Fig. 2.10. With V_{n1} being the input referred noise of the op amp with respect to the second RF stage and $R_{F2} >> R_1$. We should point out that the eight op amps are in fact implemented as four differential op amps and in order to maintain the negative polarity of the feedback, R_{F2} and R_{F3} are connected to the opposite outputs of each differential op amp, however for the sake of simplicity it has not been depicted in Fig. 2.10. It is worthy to note that in this second loop, the mixer switch is in the feedback path in series with R_{F2}, hence can be absorbed in R_{F2} without the loss of generality. Another important point to mention is that the op amp has a high gain, hence X_1 and X_2 could be considered as ground compared to the output node,V_{out}. Therefore, the current generated in op amp will be divided between R_{F2} and R_{F3} in inverse proportion to their resistance. First outcome of this observation is that the input resistance of node X_2 will be $R_{X_2} = R_{sw} + (R_{F2} + R_{F3})/(R_{F2}G_{mT})$, hence the gain of the second

stage can be written as

$$\frac{V_{X_2}}{V_{X_1}} = -G_{m2}(R_2||R_{X_2}) = -\frac{G_{m2}R_2}{1+\frac{G_{mT}R_2R_{F2}}{G_{mT}R_{sw}R_{F2}+R_{F2}+R_{F3}}} \tag{2.5}$$

Now we will calculate the gain of the first gain stage. We start with the input resistance at X_1. We fairly assume $R_{X_2} << R_2$, hence the current generated by G_{m2} will be directed to R_{F3} make it necessary for a current of $G_{m2}(R_{F3}/R_{F2})$ to flow in R_{F2}, hence the input resistance of X_1 would be $R_{X_1} = R_{F2}/(R_{F3}g_{m2})$, resulting in the gain of:

$$\frac{V_{X_1}}{V_{in}} = -G_{m1}(R_1||R_{X_1}) = -\frac{G_{m1}R_1}{1+\frac{G_{m2}R_1R_{F3}}{R_{F2}}} \tag{2.6}$$

So the overall gain of the first two stages from the input to node X_2 is:

$$\frac{V_{X_2}}{V_{in}} = \frac{G_{m1}R_1G_{m2}R_2}{(1+\frac{G_{m2}R_1R_{F3}}{R_{F2}})(1+\frac{G_{mT}R_2R_{F2}}{G_{mT}R_{sw}R_{F2}+R_{F2}+R_{F3}})} \tag{2.7}$$

We assume $R_{X_1} << R_1$, hence the overall gain of this circuit would be $V_{out}/V_{in} = -G_{m1}R_{F2}$ and the output noise could be written as $V_{n,out} = -[(R_{F2}+R_1)/(R_1)]V_{n1} \approx -(R_{F2}/R_1)V_{n1}$ which leads to an input referred noise of:

$$V^2_{n,input,CL} = \frac{V^2_{n,out}}{(\frac{V_{out}}{V_{in}})^2} = \frac{V^2_{n1}}{(G_{m1}R_1)^2} = \frac{V^2_n}{(G_{m1}R_1G_{m2}R_2)^2} \tag{2.8}$$

Equations (2.7)-(2.8) show that we are able to maintain open-loop noise performance while reducing the RF gain by a factor of $(1+\frac{g_{m2}R_1R_{F3}}{R_{F2}})(1+\frac{g_{mT}R_2R_{F2}}{g_{mT}R_{sw}R_{F2}+R_{F2}+R_{F3}})$. Fig. 2.11 shows the effectiveness of this method in reducing the input referred noise of the four differential op amps used in this design. It shows that a single loop structure reduces the noise by a factor of $\sim$40 while the dual loop structure leverages two gain stages, hence reducing the input referred noise by a factor of $\sim$ 1500. The dotted horizontal line in this plot, indicates the thermal noise level of a 50 Ω resistor to give us an idea of the magnitude of the input-referred noise in each scenario. Using this method we are able to solve the flicker noise and channel bandwidth trade-off without increasing RF voltage gain, hence keeping the receiver linearity within the required limits. Fig. 2.12 depicts the input-output characteristic curve of the three stage receiver with

and without feedback suggesting a 10 dB improvement of the 1-dB compression point after using the feedback technique. Moreover, since the RF nodes are loaded by a small impedance, their parasitic capacitance imposes much less impact on the gain and phase response of the LNA at higher frequencies which makes it more suitable for wideband applications.

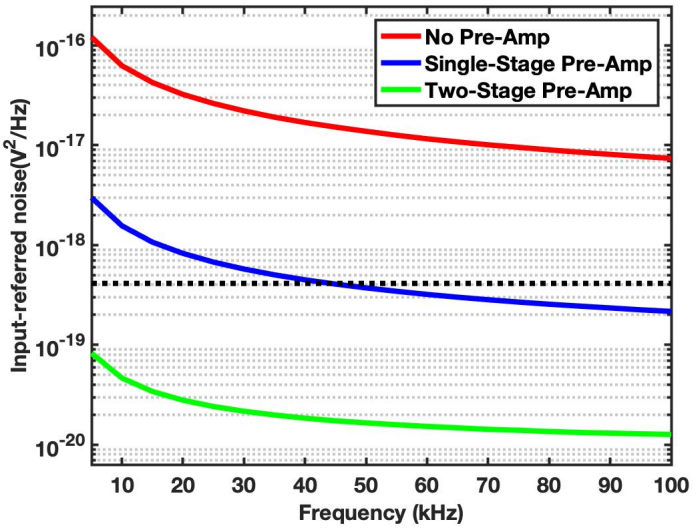
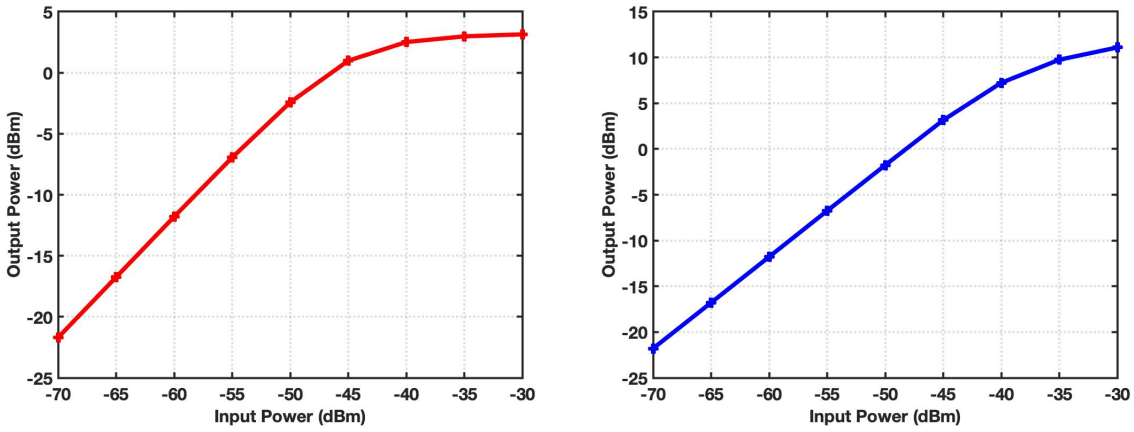


Figure 2.11. Input referred noise of the four differential op amps with and without RF gain stages in feedback.

Now we will focus on input matching. We aim to provide input matching through a global feedback around the whole dual-loop structure as depicted in Fig. 2.13, making it a multi-loop design. Once more, we mention that the current at the output of the op amps, will be divided between the feedback resistors in an inverse proportion to the resistors values. We know that the current flowing through R_{F2} is equal to $V_{in}(G_{m1}R_1)/(R_1 + R_{X_1})$, hence, the current returning to the input node will be $V_{in}[(G_{m1}R_1)/(R_1 + R_{X_1})](R_{F2}/R_{F1})$ which results in an input impedance equal to

$$R_{in} = \frac{(R_1 + R_{X_1})R_{F1}}{G_{m1}R_1R_{F2}} \tag{2.9}$$

It is worthy to note that input impedance in this case depends on ratio of R_{F1}/R_{F2} rather than



(a) (b)

Figure 2.12. Input-output characteristic of (a) the three-stage open-loop and (b) the three-stage closed-loop architectures.

their absolute values which is much more robust to process variations knowing that both R_{F1} and R_{F2} are implemented as poly resistors with large process variation in their absolute value. In this design we choose $R_{F1}/R_{F2} = 3$ that provides sufficient input matching over the entire RF bandwidth, noting that at higher frequencies parasitic capacitors will result in an increase in the magnitude of input impedance and also add a positive reactive component to it which will partially cancel the input node parasitic capacitance.

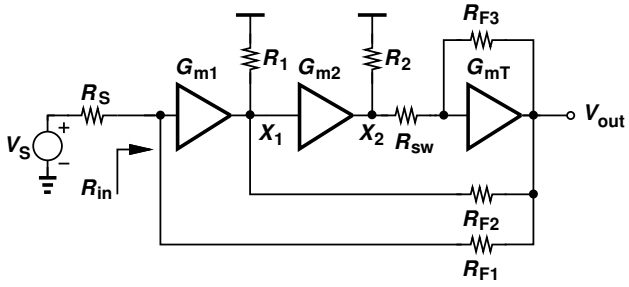


Figure 2.13. Addition of the global feedback for matching.

Finally, it is worthy to note that the actual circuit with mixer switches consists of eight switches in each feedback path, driven with non-overlapping clocks and four differential op amps, depicted as eight single-ended op amps in Fig.2.14. The noise figure and 1-dB compression point are

depicted in Fig.2.15 across the entire RF bandwidth, showing the effectiveness of the proposed multi-loop architecture.

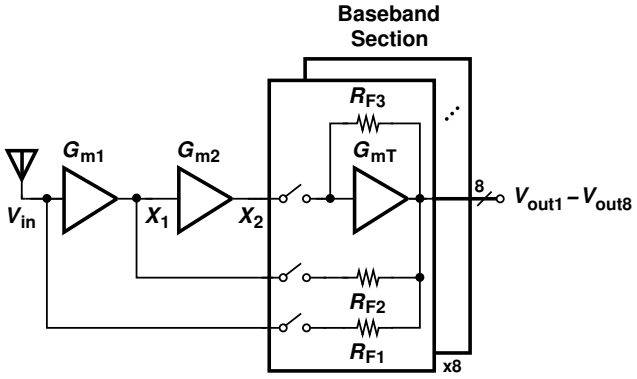
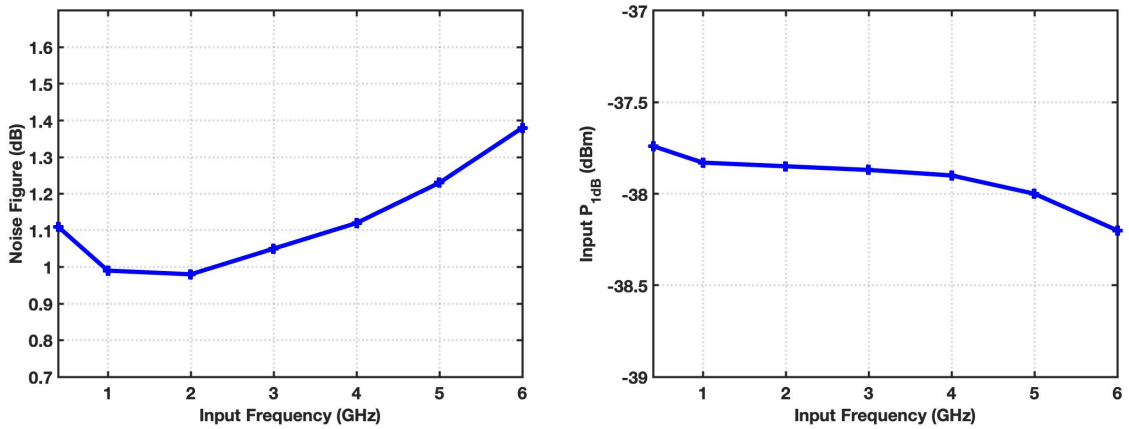


Figure 2.14. Multi-loop translational feedback.



(a) (b)

Figure 2.15. (a) Noise figure and (b) 1-dB compression point of the proposed multi-loop architecture across the RF range.

2.4.2 Baseband G_m Boosting

As depicted in Fig.2.14, We are using 3 different feedback paths from the output of the baseband amplifier to the three RF nodes, i.e. V_{in}, X_1 and X_2. In order to guarantee the linearity improvement, we have to make sure that the voltage swing at the RF nodes is small. To this end, the input

resistance provided by the feedback paths to each of the RF nodes must be small. In order to simplify the problem, let's take the circuit of Fig.2.16a in which a single RF gain stage is followed by a set of eight mixer switches driven by 12.5 $\%$ clocks and a set of eight baseband amplifiers. We seek to find the input resistance of looking through the feedback network. At each point of time, one of the switches is turned on and the equivalent Miller impedance presented to node V_{in} is:

$$Z_{in} = \frac{R_F}{1 + A_1 A_2} \tag{2.10}$$

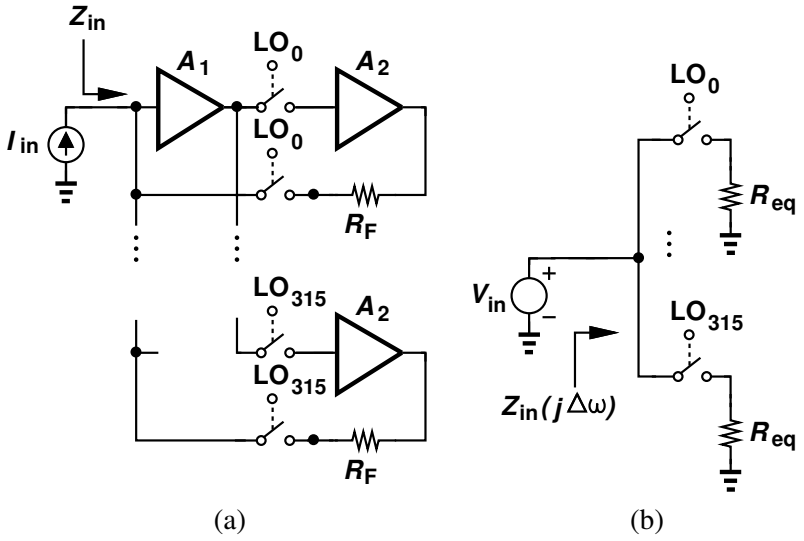


Figure 2.16. (a) A translational feedback loop and (b) its equivalent model from the input impedance perspective.

Although, the $1+A_1A_2$ factor is large, in order to reduce Z_{in} we have to take a value for R_F that will heavily load the output of the baseband amplifier and reduce its gain. Therefore just reducing R_F does not help. If we want the baseband amplifier to be able to drive a small R_F, we inevitably need to increase its power consumption which is not desirable. To tackle this problem we start with a simplified model of the circuit in Fig.2.16a. On the right side of the mixer switches connected to V_{in} we technically have an equivalent resistor equal to $R_{eq} = R_F/(1 + A_0A_1)$. At each point of time, one of these equivalent resistors is connected to the V_{in}, therefore showing an equivalent RF impedance of $Z_{in} = R_F/(1+A_0A_1)$. The equivalent circuit is depicted in Fig.2.16b. Interestingly,

it could be proved that if we add a capacitor in parallel to each resistor as in Fig.2.17a - so that to change it to a low-pass impedance that drops to very small values at ω_{LO} and its harmonics- the equivalent impedance at V_{in} would be equal to:

$$Z_{in} = \frac{R_{eq}}{8(1 + R_{eq}C_H\Delta\omega)} \tag{2.11}$$

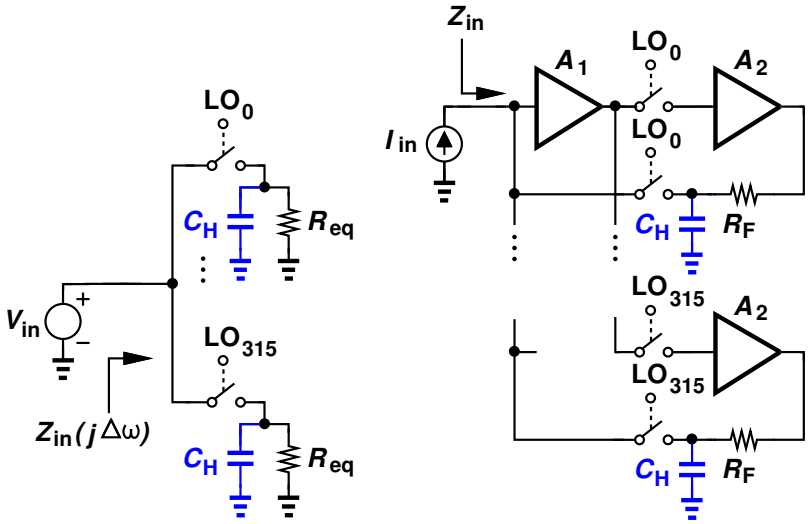


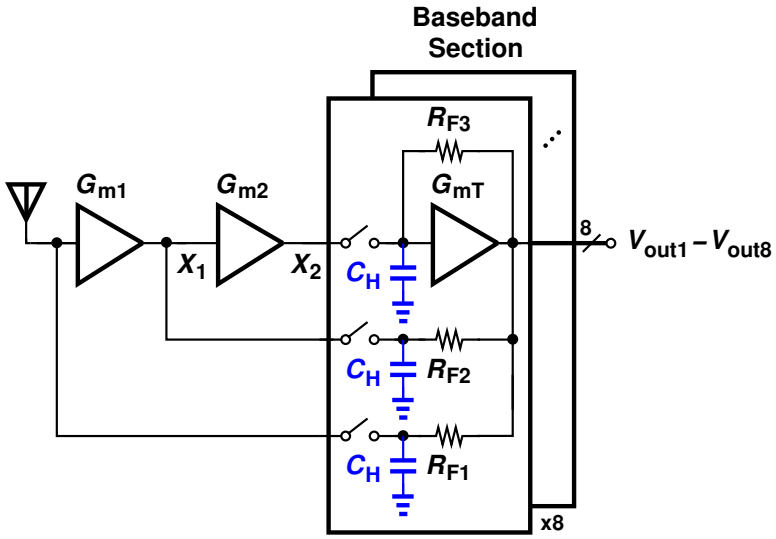
Figure 2.17. (a) Boosting the input impedance by means of baseband hold capacitors and (b) implementation of this idea in a translational feedback loop.

where $\Delta\omega$ is the frequency offset from ω_{LO}. If we assume that the channel bandwidth (CBW) of interest is much smaller than $(R_{eq}C_H)^{-1}$, the equivalent input impedance would be:

$$Z_{in} = \frac{R_{eq}}{8} \tag{2.12}$$

This shows that by choosing a value of C_H such that $CBW << (R_{eq}C_H)^{-1} << \omega_{LO}$ we can reduce the input impedance by a factor of eight. Now we implement this idea in the circuit of Fig.2.16a which results in the circuit depicted in Fig.2.17b. By employing this technique, for a desired input impedance, we can use eight times larger R_F which can be drive by eight times smaller G_m in the baseband amplifier that consumes eight times less power. The mathematical

explanation of the equivalent impedance of an N-path filter with low-pass load is presented in appendix II. As a simple explanation for this improvement, we can look at a single branch of



(a)

Figure 2.18. Multi-loop receiver architecture after the addition of hold capacitors.

Fig.2.17b. without the capacitor, the feedback resistor only draws current when the switch is on and when the switch is off, the current in the baseband amplifier is wasted. When we add the capacitor to each branch, even when the switch is off - for $7/8$ of the time -, the baseband amplifier draws current through the R_F and stores charge on the top plate of the capacitor which we call "hold capacitor". When the switch turns on - for $1/8$ of the time -, not only the R_F draws current, but also the charge stored on the C_H will flow through the switch as a current - which is seven times the current drawn by R_F -, hence, the overall current drawn from V_{in} is eight times larger compared to the previous case. Using this method, we add hold capacitors to all of the three feedback paths of Fig.2.14 to benefit from the G_m boosting property of this technique at all of the three RF nodes.(Fig.2.18)

2.4.3 Proportional Capacitor Allocation

We now need to explain the filtering method used in this architecture to select the desired channel. We need to filter the signal at the first point that we have a high voltage gain which in the case of our receiver, is the output of the op amps. To this end, we add capacitors in parallel with the feedback resistors as show in Fig. 2.19. The key point here is that in order to avoid any impact on the RF gain of the first and second stages as well as any change in the input impedance of the receiver, the three RF nodes should not "feel" any changes in their load impedance due to channel selection. This means that the current generated by the op amps, should be divided between the three feedback branches with the same proportion regardless of baseband frequency. This condition translates to addition of capacitors in parallel with the feedback resistors whose values are inversely proportional to the value of the resistors. This technique not only prevents RF channel selection, hence, avoiding center frequency shift, but also maintains input matching within the required limit over the desired channel bandwidth and beyond, which was a problem in previously reported receivers with translational feedback loop.

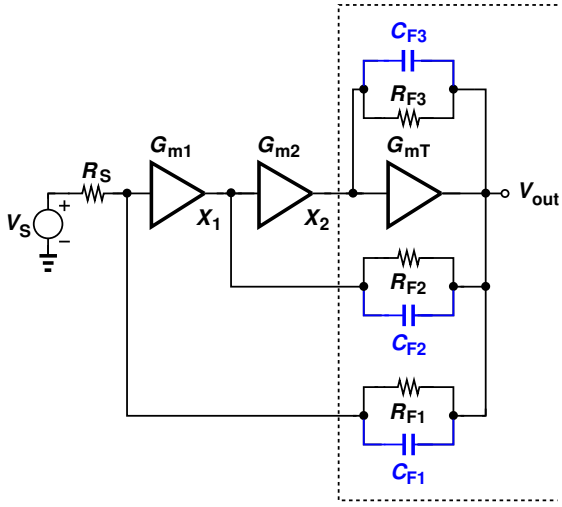


Figure 2.19. Proportional capacitor allocation.

It is beneficial to have a closer look at what causes input impedance matching problem in the presence of channel selection and our solution for that from another more general perspective.

Suppose we have added the channel-select capacitors to the two inner feedback loops, but the outer loop consists only of a resistor (Fig. 2.20a). As shown in Fig. 2.20b, we can model the whole three stages of the receiver performing channel selection with an amplifier having a transfer function of $A(j\Delta\omega) = A_0/(1 + j\Delta\omega/p_{ch})$ where $\Delta\omega = \omega - \omega_{LO}$ is the frequency offset from the LO frequency and p_{BB} represents the baseband pole. This transfer function results in an equivalent input admittance of $Y_{in}(j\Delta\omega) = (1 + A(j\Delta\omega))/R_{F1} \approx A(j\Delta\omega)/R_{F1} = A_0G_{F1}/(1 + j\Delta\omega/p_{ch})$, with $G_{F1} = 1/R_{F1}$. Assuming that for proper matching at the center frequency, R_{F1} is chosen such that $A_0G_{F1} = G_S = 1/R_S$, at the edge of the desired channel where $\Delta\omega = \pm p_{ch}$, we will have $Y_{in}(j\omega) = G_S/2(1 \pm j)$. Hence, at the edge of the channel we will have the following S_{11}:

$$S_{11} = 10log[\frac{(0.5G_S)^2 + (0.5G_s)^2}{(1.5G_S)^2 + (0.5G_S)^2}] = -7dB \tag{2.13}$$

That exceeds the allowable -10 dB threshold. This is the reason for S_{11} degradation in the prior art. Here, it is worthy to note two additional drawbacks of using only resistors in the outer feedback loop. First, we calculate the overall gain of the system from input source to the output. Assuming $A_0 >> 1$ and $R_{F1}/A_0 = R_S$ for proper matching, we can write the input impedance as $Z_{in} = (R_{F1}/A_0)(1 + j\Delta\omega/p_{ch}) \approx R_S(1 + j\Delta\omega/p_{ch})$. Now we can write the overall gain as:

$$\frac{V_{out}}{V_S} = \frac{Z_{in}}{Z_{in} + R_S}A(j\Delta\omega) = -\frac{A_0}{2[1 + j\Delta\omega/(2p_{ch})]} \tag{2.14}$$

Which implies that using only resistors in the feedback for matching will double the baseband bandwidth of the overall system, which requires to double the baseband capacitors in parallel to R_{F3} and R_{F2} in order to maintain the desired bandwidth that is a huge area penalty. Second, We assume a parasitic capacitance at the input node, C_{par}, which introduces a positive imaginary admittance at the input, $jC_{par}\omega_{LO}$. On the other hand, the input admittance presented due to the feedback will be:

$$Y_{in}(j\Delta\omega) = 1/Z_{in}(\Delta\omega) = \frac{1 - j\Delta\omega/p_{ch}}{R_S(1 + \Delta\omega^2/p_{ch}^2)} \tag{2.15}$$

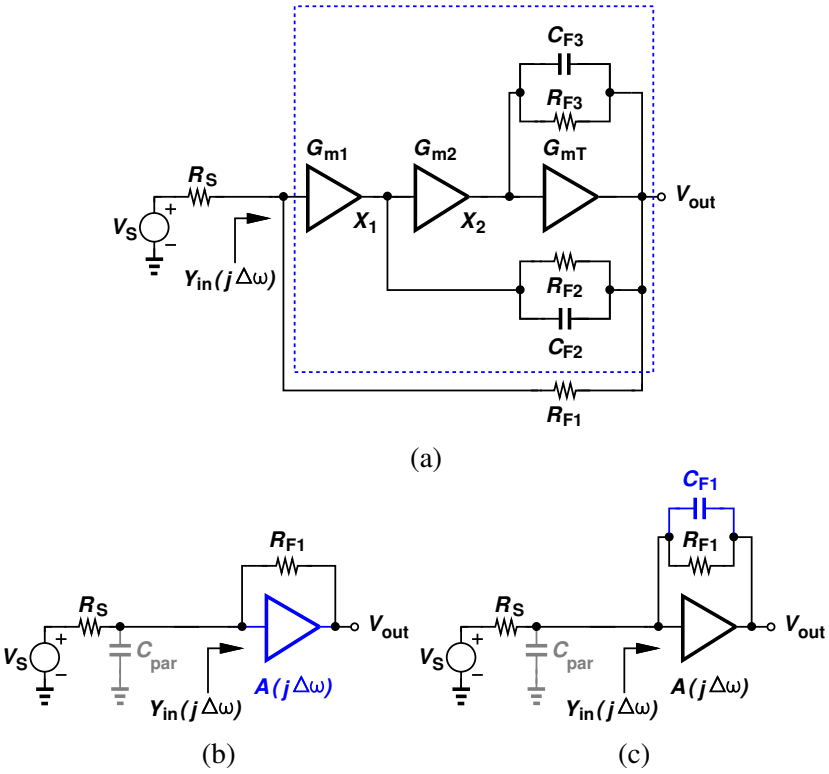
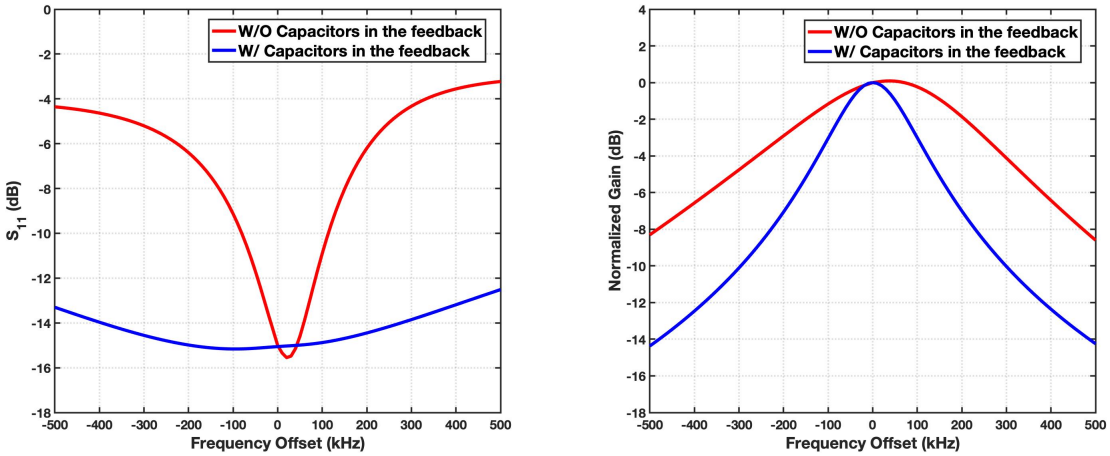


Figure 2.20. (a) Using only resistive feedback in the outer loop while the inner feedback loops include channel-select capacitors, (b) its simplified equivalent and (c) addition of the feedback capacitor to the outer loop.

Which shows that the real part of the input admittance decreases as the input frequency departs from ω_{LO} in either direction. However, the imaginary part of the input admittance becomes negative as the input frequency takes values greater than ω_{LO}, hence partially cancelling the positive imaginary admittance of C_{par} and increases the gain, while taking positive values as the input frequency becomes less than ω_{LO}, hence adding up with the admittance due to C_{par} and reducing the gain. This phenomenon results in an asymmetric frequency response with the center frequency shifted to the right of ω_{LO}. Interestingly, there is a systematic solution for this problem. If we add a zero to $Y_{in}(j\Delta\omega)$ equal to its pole, we can make its value constant, regardless of baseband frequency offset and solve all of the forgoing issues. To this end we add a baseband zero to Y_{F1} and change it to $Y_{F1}(j\Delta\omega) = (1/R_{F1})(1 + j\Delta\omega/p_{ch})$ and implement it by adding a capacitor C_{F1}

in parallel with R_{F1} (Fig. 2.20c) such that $p_{BB} = 1/(R_{F1}C_{F1})$. This result explains the logic behind proportional capacitor allocation from another perspective.

In order to have a better evaluation of the effect of adding capacitors in the matching feedback network, Fig. 2.21a depicts the input matching with and without capacitors in the feedback path which clearly shows how adding the capacitors extends the input matching far beyond the channel bandwidth. Also Fig. 2.21b illustrates how adding the feedback capacitors helps keeping the channel bandwidth from being doubled and shifted to the right. Both plots in Fig.2.21 are for a 200 KHz channel bandwidth configuration at 1 GHz LO frequency.



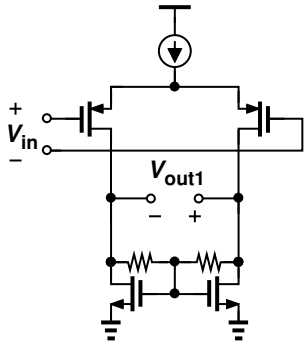
(a) (b)

Figure 2.21. (a) Input Matching and (b) Frequency response of the receiver with and without capacitors in the feedback.

2.4.4 Low-Power, Wideband Op Amp Topology

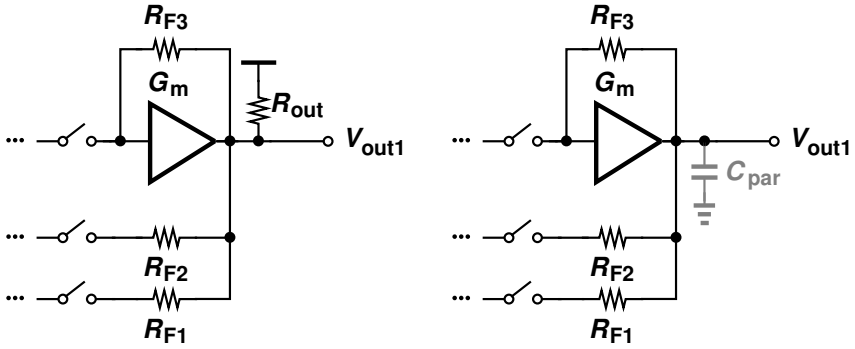
In this section we will discuss the op amp used as the first baseband section. We start with the simple differential pair topology shown in Fig.2.22. Four of these op amps are to be used in the 8-path multi-loop feedback architecture. To each output of the op amp three feedback resistors are connected that steer the current produced in the op-amp to the three RF nodes of the receiver. As mentioned earlier we seek to reduce the equivalent resistor at the RF nodes as much as possible

which means we prefer to steer as much of the current generated in the op amp as possible to the feedback paths.



(a)

Figure 2.22. A differential pair as a one stage op amp.



(a) (b)

Figure 2.23. (a) A simplified model of the op amp in feedback and (b) accounting for the parasitic capacitance at the output of the op amp.

Now since we cannot use large transistors with long channels, the channel resistance of the transistors in the differential pair together with the common-mode feedback resistors will be comparable to the feedback resistors and absorb part of the op amp current which is not desirable. Therefore, we seek to increase the op amp output resistance as much as possible. Increasing the op amp output resistance is also important from another perspective. Suppose that we have added the channel-select capacitors to the feedback paths and that the op amp output resistance is comparable to the feedback resistors as conceptually depicted in Fig.2.23a. At frequencies much less than the

channel bandwidth, the op amp output current is divided between the $R_{F1} - R_{F3}$ and R_{out}. As we get closer to the channel bandwidth and the capacitors impedance becomes comparable to that of the resistors, the op amp current prefers to go to the feedback paths more than it prefers to go to R_{out}. Therefore, the RF nodes will "feel" the channel selection and the undesirable asymmetric frequency response shift will occur as discussed in the previous section. One solution would be to add a capacitor from the output of the op amp to the ground to follow the rule of proportional capacitor allocation which is not desirable due to its area penalty especially for narrow bandwidth standards such as GSM. The other option is to add a negative capacitance to negate the op amp output resistance. To this end, we add a tiny cross-coupled pair to the output of the op amp whose negative resistance cancels out with R_{out}. This modification is show in Fig.2.24a.

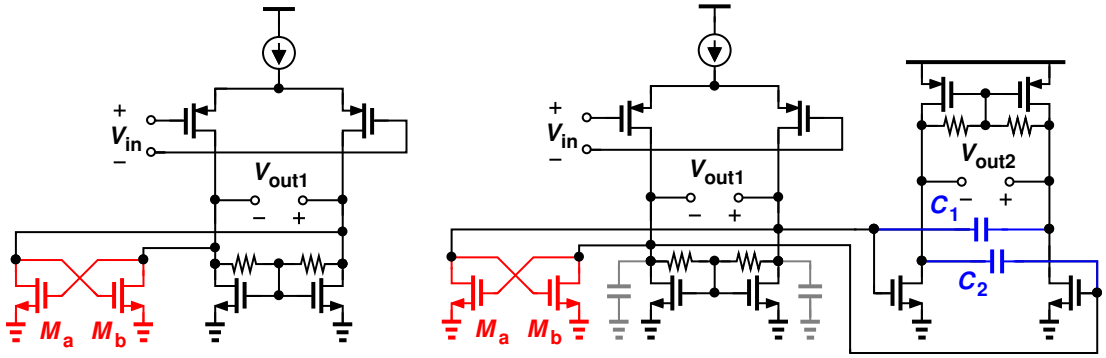
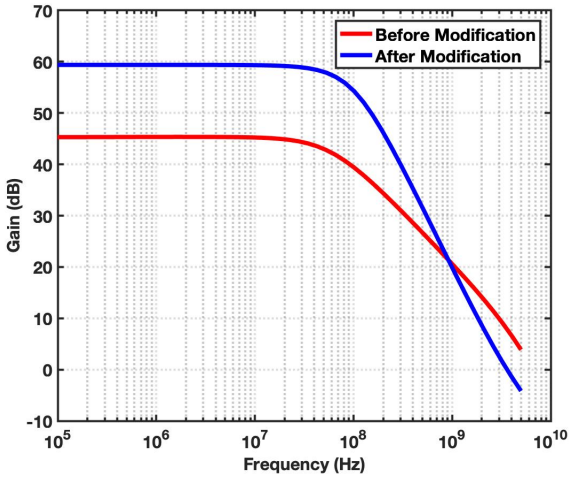


Figure 2.24. (a) Negative resistance added to the op amp in the form of a cross-coupled pair and (b) negative Miller capacitance added to the output of the op amp.

Now that we have removed the op amp output resistance, we focus on another problem. the transistors used in the op amp and its subsequent stage introduce parasitic capacitance(Fig.2.23b). This parasitic capacitance will be comparable to the feedback channel-select capacitors of the wideband channel configurations such as 160 MHz channel bandwidth of WiFi 6. Let us have another thought experiment. Suppose we start from small baseband frequencies where the op amp current is divided between the three feedback paths in an inverse proportion to their resistor values. As we get closer to the frequencies comparable to the channel bandwidth, the capacitors begin to take over and indicate the the current division factor. Now C_{par} will also draw a portion of the

op amp current which means that less current will go to the RF nodes through the feedback paths, RF nodes will ”feel” the channel selection and the frequency response gets asymmetric. To solve this problem we introduce a negative capacitance at the output of the op amp using the gain of subsequent baseband amplifier and the Miller effect as shown in Fig.2.24b.



(a)

Figure 2.25. Frequency response of the two stage amplifier with and without the proposed techniques.

Using these two techniques, i.e. cross-coupled negative resistance and Miller negative capacitance, we have introduced a high gain, wideband op amp which consumes only 1.5 mW. The frequency response of the op amp before and after the modifications is depicted in Fig.2.25 showing the effectiveness of the proposed techniques in increasing the gain without any sacrifice in the bandwidth.

2.4.5 Blocker Rejection N-Path Filter

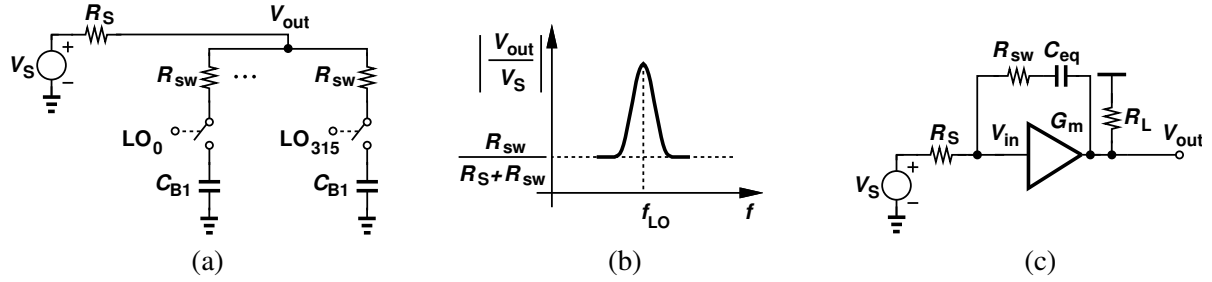
Although the multi-loop architecture maintains the RF gain low enough for the desired signal and close-in interferers to avoid non-linearity, the RF gain is not low enough to prevent large out-of-band blockers from compressing the receiver. In order to address this problem, we need to have frequency selective filtering at the first and second stages that attenuates out of band signals while

amplifying the desired band. This feature calls for an N-path filter to be added to the input and output of the first and second stage of the LNA. However as depicted in Fig.2.26b, the out-of-band rejection of a N-path filter (Fig.2.26a) is limited by the resistance of the switches. Therefore, we place the N-path filter around a gain stage to benefit from the Miller effect, hence reduce the size of the N-path switches and capacitors. However as we will see in this section, this technique has more interesting properties.

Fig. 2.26c shows the baseband equivalent of an N-path filter placed around a gain stage. Writing KCL at nodes V_{in} and V_{out} will lead to the following relationships for the transfer function from V_S to V_{in} and V_{out}:

$$\frac{V_{in}}{V_S} = \frac{1 + j(R_{sw} + R_L)C_{eq}\Delta\omega}{1 + j(R_{sw} + R_L + R_S(1 + G_m R_L))C_{eq}\Delta\omega} \tag{2.16}$$

$$\frac{V_{out}}{V_S} = -g_m R_L \frac{1 + j(R_{sw} - \frac{1}{G_m})C_{eq}\Delta\omega}{1 + j(R_{sw} + R_L + R_S(1 + G_m R_L))C_{eq}\Delta\omega} \tag{2.17}$$



(a) (b) (c)

Figure 2.26. (a) An N-path filter, (b) its frequency response and (c) baseband equivalent of an N-path filter placed around a gain stage.

The above relationships show that both V_{in} and V_{out} have the same pole in their transfer function which clearly shows the Miller effect. But what is more important than the pole is the zeros that we have in the two transfer functions. Zero is an undesirable part in both transfer functions as it limits the out of band rejection. While we cannot eliminate the zero or push it to higher frequencies at the input of the gain stage, we can do this about the zero at the output transfer function and the output transfer function is the most important one as the amplification takes place at the output. As evident from (2.17), if we choose R_{sw} to be equal to $1/G_m$, we can eliminate the zero and enjoy

unlimited out of band rejection. It is important to note that as (2.17) suggests, it is not a good idea just to reduce R_{sw} as much as possible. There is an exact optimum for its value. To have better understanding of how the output transfer function changes with the value of R_{sw}, the normalized transfer function of the circuit shown in Fig. 10(a) is depicted in Fig. 2.27 for different values of R_{sw}.

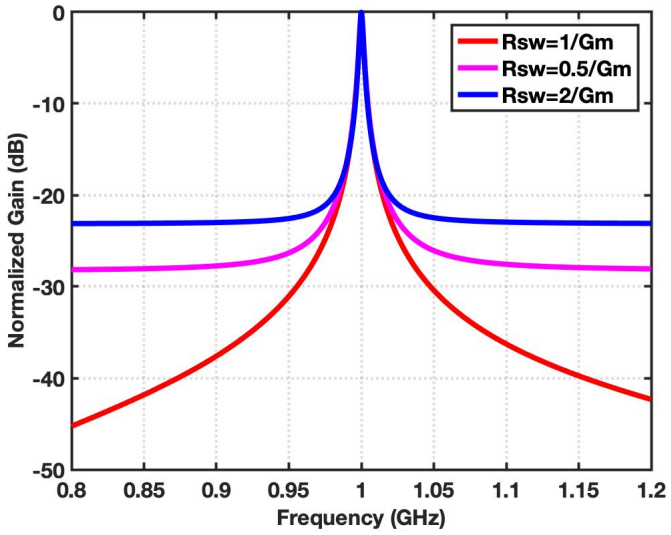


Figure 2.27. Frequncy response of the circuit shown in Fig. 2.26c

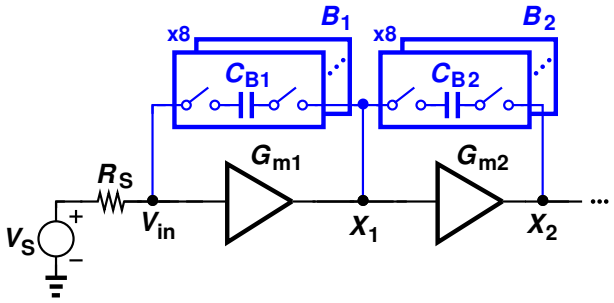
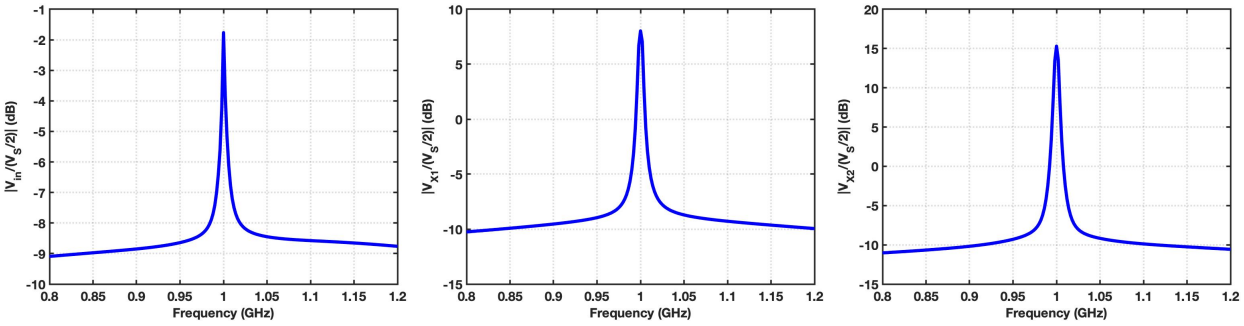


Figure 2.28. Addition of blocker rejection banks to the receiver.

Fig. 2.27 clearly shows that the optimum value for R_{sw} is $1/G_m$ and reducing it more will limit the out-of-band rejection. Choosing $R_{sw} = 1/G_m$ is the best choice for receivers with lower maximum frequencies, almost up to 3.5 GHz or the ones with 4-path structures that have a smaller

number of switches. In our case, however, we have eight paths in order to reject harmonic blockers up to the sixth harmonic. This number of paths requires higher clock power consumption and also adds more parasitic capacitance to the RF nodes, hence reducing the gain and increasing noise figure at high RF frequencies. Both of the above-mentioned issues lead us to choose $R_{sw} \approx 3/G_m$ for the total switch resistance of the two N-path filters placed around the first and second stages of the LNA (Fig.2.28). These two banks are on only for the low band standards that have stringent blocker rejection requirements. Fig.2.29 shows the frequency response at the three RF nodes of the proposed receiver which show that these two 8-path filters provide a $\sim$27 dB out of band rejection at node X_2 which serves an important role in keeping the receiver linear.



(a) (b) (c)

Figure 2.29. Frequency response of the receiver over the desired and out-of-band frequency range at (a) the input node, (b) node X_1 and (c) node X_2.

2.4.6 Frequency Response Correction Bank

Another phenomenon that manifests itself as we increase the channel bandwidth is that other base-band nodes also add poles to the transfer function that will skew the shape of frequency response, make it fall steeper on the left side of the center frequency and gentler on the right side of it. Recall from section 2.4.2 that we have added the hold capacitors in all of the three feedback paths to add memory and boost the transconductance. The simplified resistor and capacitor equivalent model of the 8-path feedback routes used in the receiver is depicted in Fig. 2.30.

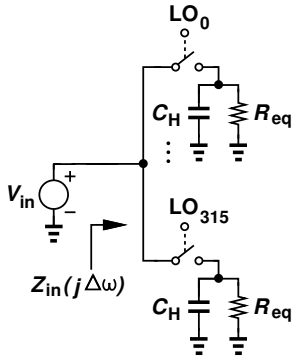


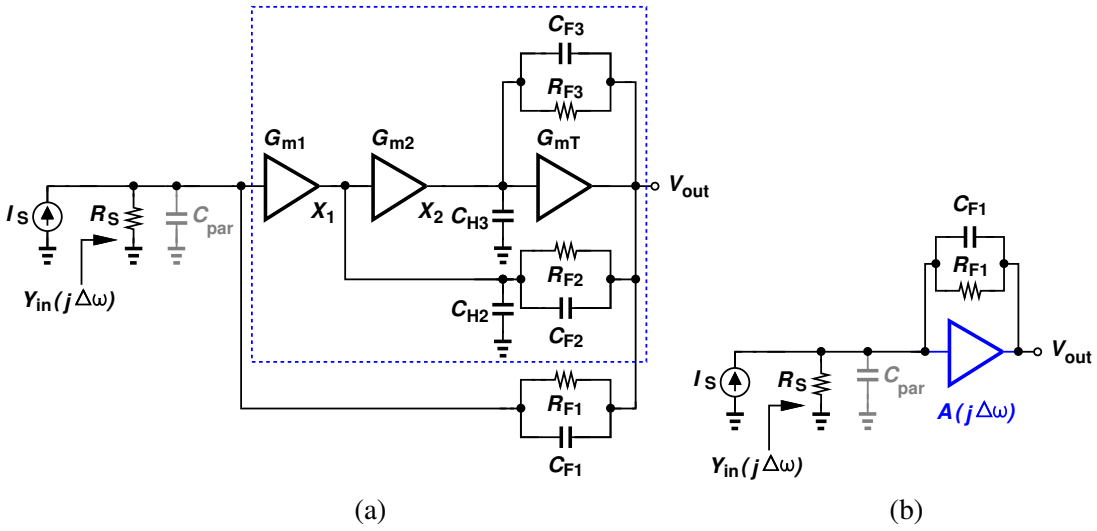
Figure 2.30. An 8-path structure with resistors and capacitors as baseband impedance.

Although our goal is to have an impedance of $R_{BB}/8$ at the input, we should keep in mind that over a frequency range wider than our channel bandwidth of interest, the hold capacitor becomes comparable to R_{BB} and the input impedance would be represented as $Z_{in} = R_{sw} + [R_{BB}||1/(jC_H\Delta\omega)]/8$ that introduces a pole much larger than the desired channel bandwidth. Same argument applies to the three channel selection banks that we have in our receiver. As we go from the lowest frequency standard supported which is at 400 MHz with 200 KHz channel bandwidth to the highest frequency one which is at 6 GHz with 160 MHz channel bandwidth, carrier frequency scales up by a factor of 15 which allows us to use 15 times smaller hold capacitors. Meanwhile, channel bandwidth scales up by a factor of 800. This means that at 6 GHz with 160 MHz channel bandwidth, The unwanted added poles are a factor of $\sim$53 closer to the channel bandwidth.

We now seek to analyze the effect of the added poles on the overall frequency response of the receiver. For the sake of simplicity, let us assume that only the two inner loops incorporate hold capacitors ad add extra poles to the system (Fig. 2.31a). The simplified equivalent of the circuit in the blue dashed box is shown in Fig. 2.31b. Now let us take a look at the input admittance of this circuit. The parasitic capacitance of the input node is depicted in gray to emphasize that it is considered to be in the RF domain, hence should be treated as a constant imaginary admittance in our analysis. Looking through the input node, we aim to calculate the input admittance including the source admittance. According to this design, both baseband nodes X_1 and X_2 add an extra pole

of almost same frequency p_0 to the V_{out}/V_{in} transfer function. In the frequency range of our interest which is smaller than p_0 we can approximate the two poles at p_0 with one pole at $p_{ex} = p_0/2$. In practice,the two mentioned baseband nodes will add a pair of complex poles at $p_0 = p_r \pm jp_i$ due to the inner feedback loops, but still we can approximate those poles with a single pole at $p_{ex} = (p_r^2 + p_i^2)/(2p_r)$ inside our frequency range of interest. Thus, the approximated transfer function would be:

$$A(j\Delta\omega) = -\frac{A_0}{(1 + j\Delta\omega/p_{ch})(1 + j\Delta\omega/p_{ex})} \tag{2.18}$$



(a) (b)

Figure 2.31. (a) Base band equivalent of the Multi-loop structures and (b) its simplified model.

With $\Delta\omega = \omega - \omega_{LO}$ and p_{ch} being the baseband channel bandwidth. Also, please note that this transfer function is symmetric around $\Delta\omega = 0$. Now assuming that $A(j\Delta\omega) >> 1$ in our frequency range of interest, which is a valid assumption, the input admittance including the source resistance can be written as:

$$Y_{in}(j\Delta\omega) = G_S + jC_{par}\omega_{LO} + \frac{(G_{F1} + jC_{F1}\Delta\omega)A_0}{(1 + j\Delta\omega/p_{ch})(1 + j\Delta\omega/p_{ex})} \tag{2.19}$$

Where $G_S = 1/R_S$ and $G_{F1} = 1/R_{F1}$. From section 2.4.3 we know that $(G_{F1}+jC_{F1}\Delta\omega)A_0/(1+ j\Delta\omega/p_{ch}) = G_s$, therefore, we can simplify (2.19) as:

$$Y_{in}(j\Delta\omega) = G_S + jC_{par}\omega_{LO} + \frac{G_S}{1 + j\Delta\omega/p_{ex}} \tag{2.20}$$

The overall transfer function from I_{in} to V_{out} is $H_{tot}(j\Delta\omega) = A(j\Delta\omega)/Y_{in}(j\Delta\omega)$. Knowing that $A(j\Delta\omega)$ is symmetric around 0, For the overall transfer function to be symmetric, $Y_{in}(j\Delta\omega)$ must be symmetric too. However, from (2.20) we can see that because of the parasitic capacitance and the frequency dependent feedback component, the symmetry cannot be maintained. As a simplified explanation, we can say that the feedback part of Y_{in} which is $G_s/(1 + j\Delta\omega/p_{ex})$, shows an inductive imaginary part for $\Delta\omega > 0$ which partially cancels $jC_{par}\omega_{LO}$, hence decreasing overall Y_{in} which results in an increase in $H_{tot}(j\Delta\omega)$. On the other hand, for $\Delta\omega < 0$, $G_S/(1+j\Delta\omega/p_{ex})$ shows a capacitive imaginary part which adds up to $jC_{par}\omega_{LO}$, increasing overall Y_{in} which makes $H_{tot}(j\Delta\omega)$ smaller. As a result, the overall transfer function falls with a steeper slope on the left side of ω_{LO} compared to the right side. To address this problem, we need to examine (2.20) more carefully. In order to solve the problem of asymmetry, we either need to eliminate $jC_{par}\omega_{LO}$ from the expression or remove dependency of the feedback admittance, i.e. $G_s/(1 + j\Delta\omega/p_{ex})$ to $\Delta\omega$. Eliminating $jC_{par}\omega_{LO}$ is not a feasible since it needs either an inductor which will work only at a certain frequency range or a negative capacitor which is not practical at 6 GHz. To remove the dependency of $G_S/(1 + j\Delta\omega/p)$ to $\Delta\omega$, we need to add a zero to it which is equal to its pole. Therefore, the feedback admittance should be modified as in (2.21):

$$Y_{in}(j\Delta\omega) = \frac{G_S(1 + j\Delta\omega/p_{ex})}{1 + j\Delta\omega/p_{ex}} = \frac{G_S}{1 + j\Delta\omega/p_{ex}} + \frac{1}{\frac{1}{G_S} + \frac{p_{ex}}{jG_S\Delta\omega}} \tag{2.21}$$

In other words, we need to add an element with impedance of $1/(G_S + p_{ex}/(jG_S\Delta\omega)$ in parallel to the admittance looking through the feedback network. Surprisingly, this element is an 8-path structure with switch resistance of $1/G_S$ and a $G_S/(8p_{ex})$ capacitor (C_{B3}) in each path as shown in Fig. 2.32a. We can go a step further and place this 8-path structure around the first stage, hence reducing required switch and capacitor (Fig. 2.32b). One might wonder why we did not assume parasitic capacitance at RF outputs of the first and second stages of the LNA (nodes X_1 and X_2). The answer is that we have parasitic capacitance at those two nodes too, but the ratio of capacitive load to resistive load is smaller at these two nodes compared to the input node as a result of stronger feedback. Secondly, node X_1 faces a similar issue with much less severity because it only sees a single extra pole at p_0 rather than a two-pole system. Thirdly, node X_2 does not experience

this problem, in fact, it experiences the opposite as it sees the load of $[(R_{F1}R_{F2} + R_{F1}R_{F3} + R_{F2}R_{F3})/(R_{F1}R_{F2}G_{mT})||1/(jC_{H3}\Delta\omega))]/8$ whose imaginary part is capacitive for $\Delta\omega > 0$ and inductive for $\Delta\omega < 0$ which causes an asymmetry in an opposite direction compared to node X_1. This property partially compensates for the asymmetry caused at node X_1. Finally, placing the added 8-path filter around the first stage, lets the added 8-path filter to help correct the asymmetry at node X_1 in addition to the input node.

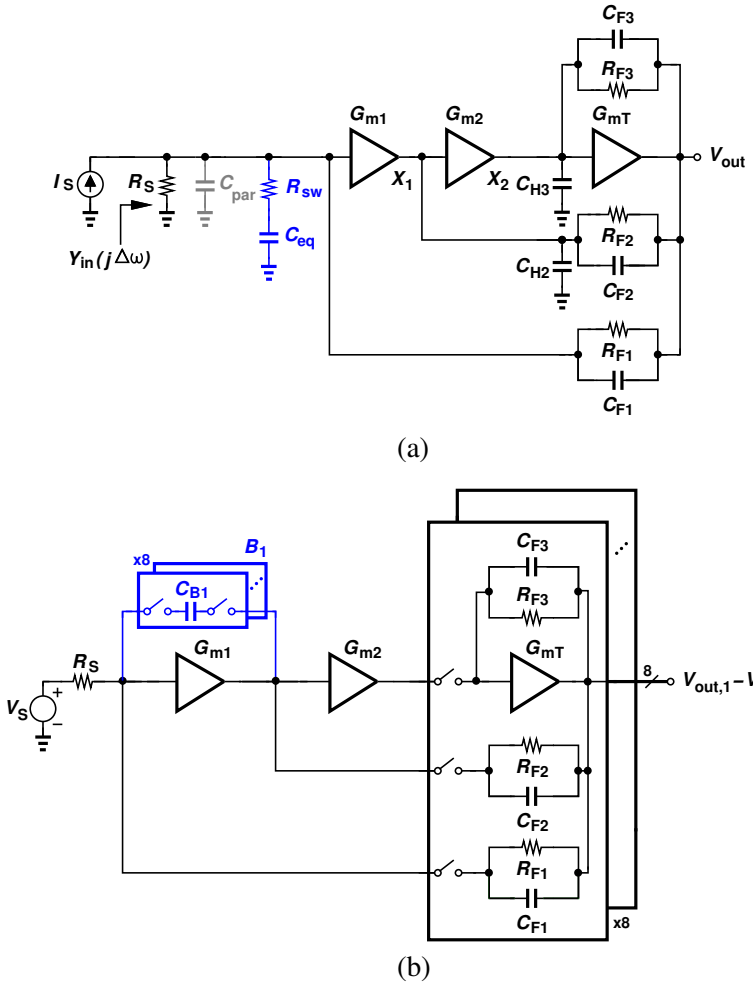


Figure 2.32. (a) Addition of the frequency correction element and (b) addition of frequency correction bank to the receiver.

It is worthy to note that approximating the two added poles with one pole holds for small frequency offsets. As the baseband frequency becomes comparable to the added unwanted poles,

the receiver will behave like a 3-pole system that can shift the phase of the gain by more than 180°- hence the input impedance by more than 90 °- which results in an input impedance with negative real part that can cause gain peaking in an undesired frequency offset or instability in the worst case. Adding the frequency response correction bank guarantees the stability of the feedback system and the elimination of the gain peaking. Fig. 2.33 illustrates the frequency response of the receiver with 160 MHz channel bandwidth at 6 GHz LO frequency with and without the frequency response correction bank. It clearly shows how adding this bank will assure frequency response symmetry in the desired channel bandwidth and solves the problem of gain peaking at large frequency offsets.

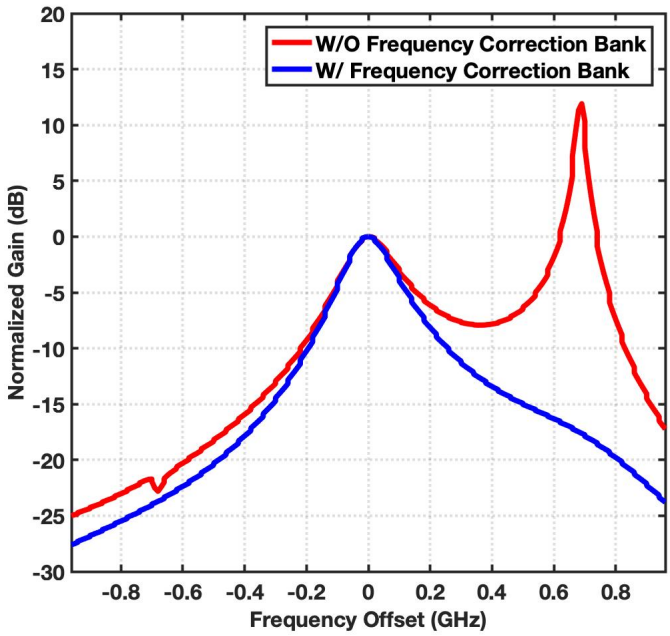


Figure 2.33. Frequency Response of the receiver at 160 MHz channel bandwidth with and without the the frequency response correction bank.

2.4.7 Multi-Loop Receiver Implementation

Now that we have developed our multi-loop receiver solution, we continue to explain its implementation. As shown in Fig. 2.34 it comprises two RF gain stages and four differential baseband op amps. The eight outputs of the op amps are connected to the three RF nodes in the sigal path, i.e. V_{in}, X_1 and X_2 via three sets of 8-phase mixers driven by non-overlapping clocks. We have put eight capacitors between the the baseband side of mixer switches and ground to add memory to the baseband impedance and boost the transconductance of the baseband op amps.

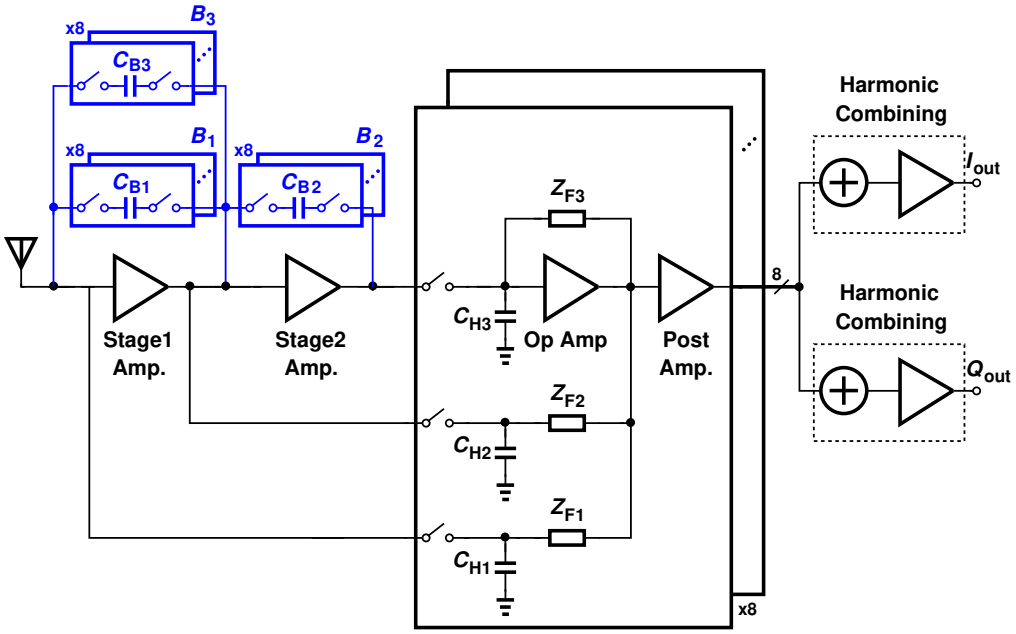
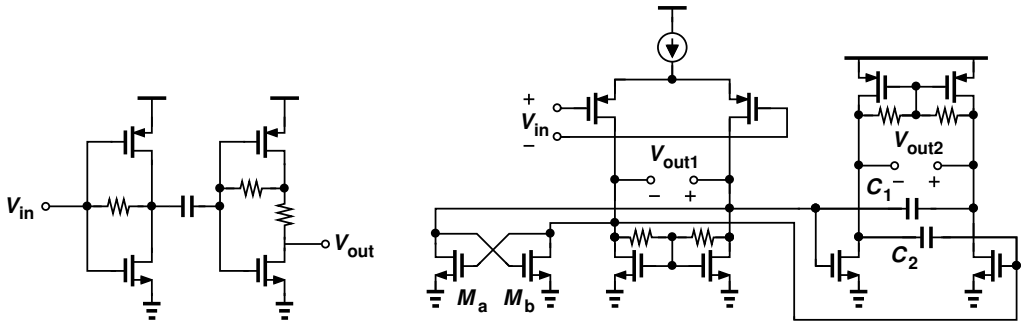


Figure 2.34. Proposed receiver architecture.

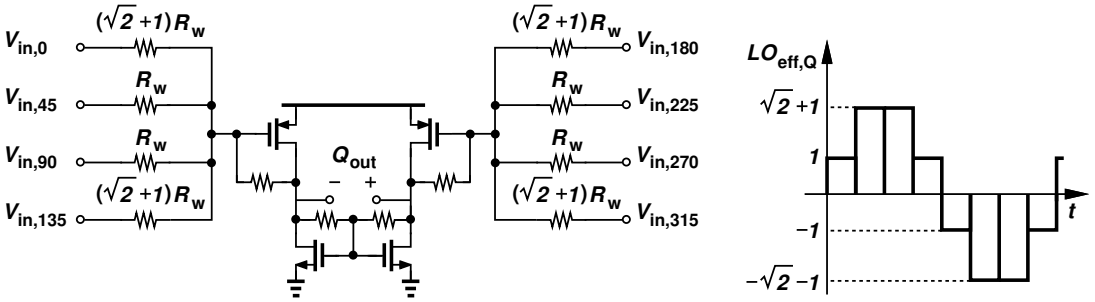
First two RF stages are implemented as self-biased inverters to create most possible transconductance for a specific current consumption (Fig. 2.35a). In the second stage, width of the transistors are chosen to be a factor of 2.35 smaller than the first stage. First and second stages are separated by a 600 fF AC coupling capacitor in order to allow second stage to be self-biased. Also, since the equivalent resistance looking through the mixers is small; it requires a large AC coupling capacitor between second stage and mixers whose parasitic capacitor to substrate limits RF bandwidth. To avoid this problem we add a small resistor between the PMOS and NMOS

at the output of second stage to shift the DC level and make it suitable for the op amp's PMOS differential pair bias. This resistor is small compared to the output resistance of NMOS and PMOS transistors, thus has a small impact on the gain of the second stage.



(a) (b)

Figure 2.35. Circuit implementation of (a) the two RF gain stages and (b) op amp and post amplifier.



(a) (b)

Figure 2.36. (a) Circuit implementation of the baseband harmonic combiner and (b) Reconstruction of a sine waveform using eight non-overlapping LOs.

Op amp architecture has been discussed in section 2.4.4 and is depicted in Fig. 2.35b. The outputs of the post-amplifiers are then applied to two baseband harmonic combiners to derive I and Q signals. each of the combiners are implemented as a pseudo-differential amplifier with a feedback resistor and eight inputs that are connected to eight weighted resistors (Fig.2.36a). The resistors are weighted such that they can resemble the sine wave from eight non-overlapping clocks as shown in Fig.2.36b. For the I output, we simply change the order of the inputs to resemble

a cosine wave. It is worthy to note that this design brings very good accuracy in terms of the harmonic combiner gain matching since the weighting accuracy depends on the relative value of the polysilicon resistors which can be realized with sufficient accuracy.

2.5 Harmonic Rejection Technique

2.5.1 The Effect of LO Phase Mismatch on Harmonic Rejection

As an ultra-wideband receiver with 6 GHz bandwidth, The harmonics of the desired signal will inevitably fall inside the pass-band of the receiver if the desired signal is in the lower range of the 6 GHz spectrum. As will be explained later in this section, our goal is to reject third and fifth harmonics. Considering the 6 GHz bandwidth of the receiver, we have to propose a technique that is capable of harmonic rejection for the signals up to 2 GHz. While harmonic mixing was proposed in [11], its performance is severely limited by the phase mismatches between the mixer LOs and the gain mismatches of the combining circuit. Fig.2.37 shows the reconstruction of a sine waveform using eight non-overlapping clocks and its block-level implementation. [13] proposes using a cascaded combining scheme that reduces the effect of gain mismatch by ∼46 dB. However, its performance is highly limited by the LO phase mismatch that completely shadows the 46 dB gain mismatch advantage. As suggested in [13] for an 8-phase mixer, the relationship between phase and gain mismatch and third and fifth harmonic rejection could be expressed as:

$$HR3 = \frac{sin^2(\pi/8)}{9sin^2(3\pi/8)[(\sigma_A/12)^2 + (\sigma_\phi/4)^2]} \tag{2.22}$$

$$HR5 = \frac{sin^2(\pi/8)}{9sin^2(5\pi/8)[(\sigma_A/20)^2 + (\sigma_\phi/4)^2]} \tag{2.23}$$

in Which HR3 and HR5 are the 3σ values of the harmonic rejection and σ_A and σ_ϕ are rms gain and LO phase mismatch (in radians) respectively. In order to gain a better understanding of the relationship between harmonic rejection and LO phase mismatch, Fig. 2.38 illustrates how HR3 and HR5 change with the combiner gain mismatch and LO phase mismatch. These plots show

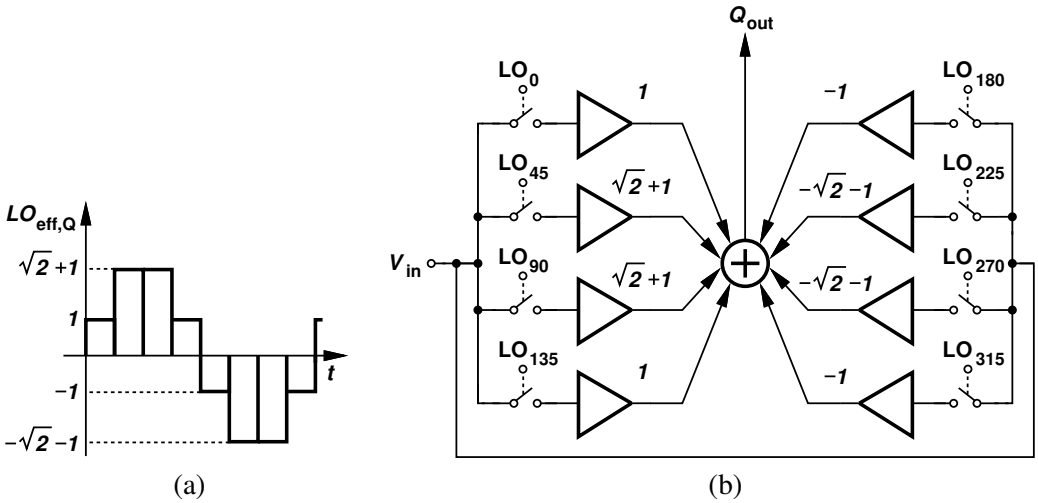
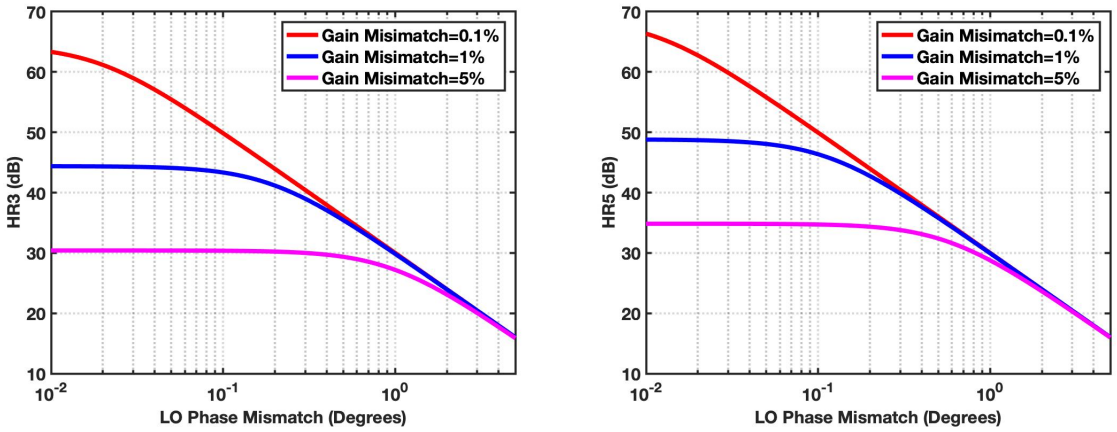


Figure 2.37. (a) Reconstruction of a sine waveform using eight non-overlapping LOs and (b) its implementation.

that to have a HR3 and HR5 of 60 dB, the LO phase mismatch should be $\leq$0.03°. This LO phase mismatch translates to 42 fs delay mismatch at 2 GHz which is extremely challenging. In order to reach this LO phase mismatch, [Ru] uses 8f$_{LO}$ input clock to re-time all the 12.5% clocks which is not a practical solution specially for LO frequencies up to 2 GHz. [13] also suggests using only 1 buffer stage between the clock generation circuit and mixer switches which results in high power consumption in the clock generation module.

Before we explain our harmonic rejection technique, we want to point out that our focus is on third and fifth harmonics of LO since the even harmonics experience a sufficient level of rejection due to differential design of the baseband circuitry and due to the fact that their rejection only depends on the phase matching between LO pairs with 180° phase difference which is much easier to provide using a 4f$_{LO}$ input clock as a re-timer. Also, seventh and ninth harmonics are much farther from the desired signal and their fold-back on the desired signal at first harmonic is inevitable in an 8-phase mixer.



(a) (b)

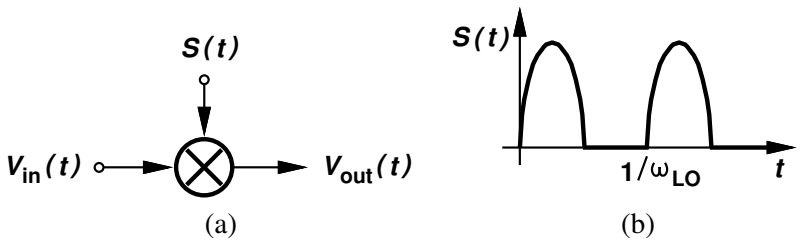
Figure 2.38. Effect of gain and phase mismatch on (a) third harmonic rejection and (b) fifth harmonic rejection

2.5.2 Half-Sine Mixer

We begin our discussion on the proposed harmonic rejection technique with an observation. What if instead of mixing the input with a sine wave, we mix it with a half-sine wave, as shown in Fig. 2.39 ? The harmonic contents of the half-sine could be represented as:

$$S(t) = 0.5sin(\omega t) + \sum_{n=1}^{\infty} \frac{cos[2(n-1)\omega t] - cos[2(n+1)\omega t]}{(2n-1)\pi} \tag{2.24}$$

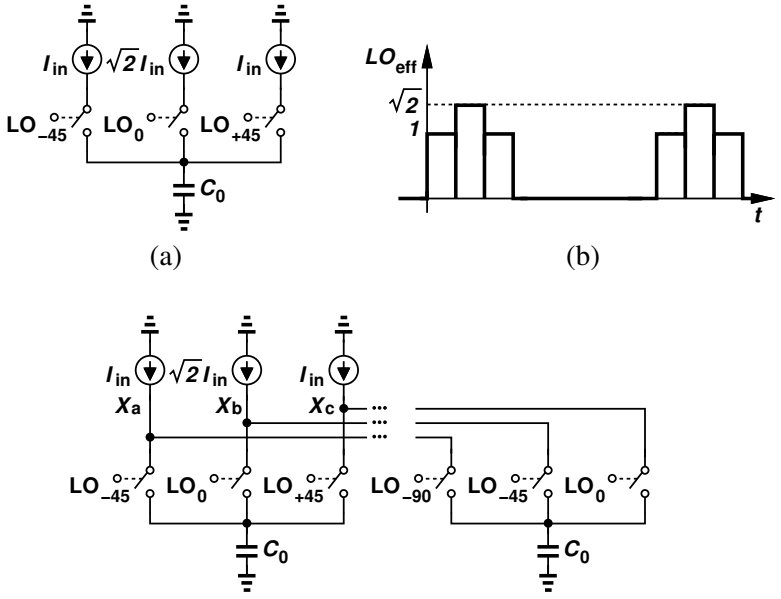
which shows that the half-sine only converts first harmonic and even harmonics to baseband and rejects all the odd harmonics. Therefore, to reject the odd harmonics a half-sine mixer is enough. This helps a lot in the implementation stage, since it does not need negative coefficients, hence no need for differential input.



(a) (b)

Figure 2.39. (a) Half-sine mixer and (b) half-sine wave LO waveform.

In order to implement the idea of half-sine mixer, we can use the circuit shown in Fig. 2.40a which approximates the half-sine wave as shown in Fig. 2.40b.



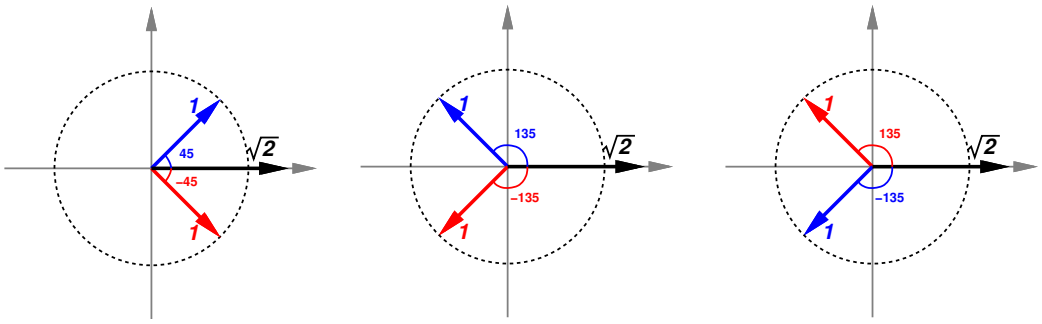
(a) (b)

(c)

Figure 2.40. (a) Implementation of a half-sine mixer, (b) Reconstruction of half-sine wave and (c) 8-path version of the half-sine mixer.

Fig. 2.41 shows the phasor diagram of the three currents that are accumulated on the base-band capacitor in Fig. 2.40a. It shows that while the first harmonic components are being added constructively, third and fifth harmonic components cancel each other. In order to transfer this harmonic rejection property to the RF, we now need to use a 8-path version of the half-sine mixer as shown in Fig. 2.40c and call it a ”harmonic-reject” 8-path filter. Third and fifth harmonics

are rejected as predicted by our previous analysis. seventh and ninth harmonics, however, are not rejected in the 8-phase reconstruction of the half-sine.



(a) (b) (c)

Figure 2.41. Phasor diagram of (a) first, (b) third, (c) fifth harmonic.

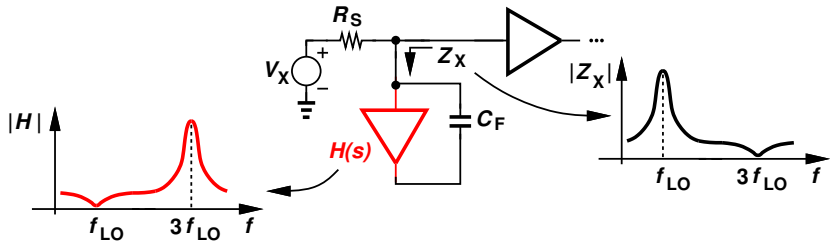
Next question is how to use this 8-path half-sine mixer in the signal path to attenuate third and fifth harmonics. Here, we need to make an important distinction. The fact that the half-sine mixer rejects third and fifth harmonics only implies that: 1) The third and fifth harmonics will be attenuated at the RF nodes of this mixer which helps keeping the mixer linear in the presence of large harmonic blockers. 2) The third and fifth harmonics will be attenuated largely after they are converted to baseband. However, LO phase mismatch occurs in the conversion process. Take the third harmonic as an example. The LO phase mismatch manifests itself before the harmonic blockers are converted to baseband by shifting the phase of the baseband components associated with the third harmonic, such that a small part of the baseband components coming from the third harmonic mimics the phase difference properties of a baseband component that is coming from the first harmonic and does not get attenuated. Then because the phase order of these baseband components on the eight paths is similar to the phase order of a signal that has been downconverted from the first harmonic, it will be upconverted to the first harmonic at the RF node. We call this effect ”harmonic fold-back”. It is important to note that this phenomenon can also occur in a regular 8-path filter. According to our study thus far, we can say that using the harmonic-reject 8-path filter in the main mixers of the receiver reduces the effect of gain mismatch in the harmonic combiner because of its harmonic rejection property, but will not help with the problem

of harmonic fold-back from third and fifth harmonics to the first harmonic caused by LO phase mismatch which is our main target in this work. This distinction between attenuating a higher harmonic - i.e. rejecting it - and folding it back on the first harmonic is important and will be studied in our proposed harmonic rejection method.

2.5.3 Harmonic Trap

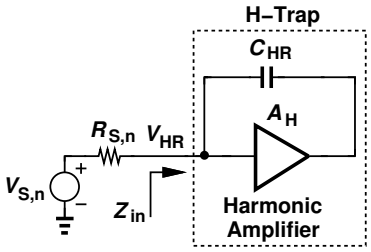
Our harmonic rejection method not only should reduce the level of third and fifth harmonics which reduces the effect of gain mismatch, but also must reduce the harmonic fold-back due to LO phase mismatch. Fig. 2.42 depicts our solution for harmonic rejection. It comprises of a harmonic amplifier and a feedback capacitor to take advantage of the Miller multiplication at higher harmonics. The overall circuit is called a harmonic trap (H-Trap). The harmonic amplifier rejects signals in the vicinity of first harmonic of the LO but amplifies higher harmonics by a gain of A_H(Fig. 2.43). $V_{S,n}$ represents the nth harmonic component of the input source and $R_{S,n}$ represent the equivalent source resistance at the nth harmonic. The reason that we do not assume the same source resistance for all harmonics is that in all of the RF nodes in the signal path, i.e. nodes V_{in}, X_1 and X_2, a major part of the total resistance comes from the feedback network. For example, at the input node at the first harmonic frequency we have the equivalent resistance of $R_{S,1} = (50\Omega||50\Omega) = 25\Omega$ from which 50 Ω comes from antenna and 50 Ω comes from the feedback matching network. At higher harmonics, however, the feedback is much weaker due to smaller conversion factor of the mixers, which results in the feedback portion of the equivalent resistance being much larger than the antenna resistance, hence for higher harmonics, $R_{S,n} \approx 50\Omega$ at node V_{in}. Therefore, for $n > 1$ we have $R_{S,n}/R_{S,1} \approx 2$. We start by analyzing the harmonic rejection property of the circuit of Fig. 2.43. The input impedance of the harmonic amplifier with capacitive feedback C_{HR}, could be written as:

$$Z_{in}(n\omega_{LO}) = \begin{cases} \frac{1}{jC_{HR}\omega_{LO}} & ; n = 1 \\ \frac{1}{j(A_H+1)nC_{HR}\omega_{LO}} & ; n > 1 \end{cases} \tag{2.25}$$



(a)

Figure 2.42. The idea of harmonic trap (H-Trap).



(a)

Figure 2.43. A harmonic trap driven with a voltage source.

Which suggests that the input impedance at the nth harmonic is smaller than its value at first harmonic by a factor of $n(A_H + 1)$ that can provide a harmonic selective filtering at node V$_{HR}$:

$$V_{HR,n} = \begin{cases} \frac{V_{S,1}}{1+jR_{S,1}C_{HR}\omega_{LO}} & ;n = 1 \\ \frac{V_{S,n}}{1+j(A_H+1)nR_{S,n}C_{HR}\omega_{LO}} & ;n > 1 \end{cases} \tag{2.26}$$

This shows the harmonic rejection property of the circuit of Fig. 2.43. As we will explain later in this section, we will exploit half-sine mixers in the implementation of the harmonic amplifier. Therefore, we aim to compare the H-Trap harmonic fold-back property caused by LO phase mismatch with that of a half-sine mixer. We start with the simple half-sine mixer of Fig. 2.40c and assume that the source has a first harmonic component equal to $V_{S,1}$ and an nth harmonic component of $V_{S,n}$. Also assume that due to LO phase mismatch, a portion of of the nth harmonic will fold back on the first harmonic at each of the RF nodes, X_a,X_b and X_c with a fold-back factor of K_n. The ratio of this fold back component, $V_{X,n,FB}$ that is created due to $V_{S,n}$,to the main first

harmonic component, $V_{X,1}$ -due to $V_{S,1}$-, i.e. the normalized fold-back component, is important for us which we call α_n for later references.

$$\alpha_n = \frac{V_{X,n,FB}}{V_{X,1}} = \frac{K_n V_{S,n}}{V_{S,1}} \tag{2.27}$$

Now we assume that the fold-back factor of the harmonic selective circuit inside the harmonic amplifier is also equal to that of a simple half-sine mixer which is proved in appendix III. Also, we assume that the fold-back happens at the output of the harmonic amplifier after the input nth harmonic has experienced a gain of A_H which is justified in appendix III as well. Since the gain of the harmonic amplifier is $\sim$0 at the first harmonic, the feedback loop is technically open for the signals at first harmonic and what ever fold-back component that is generated at the output of the harmonic amplifier, would simply experience a voltage division between the C_{HR} and $R_{S,1}$. Thus, the magnitude of the fold-back component from the nth harmonic to the first harmonic at node V_{HR} could be expressed with:

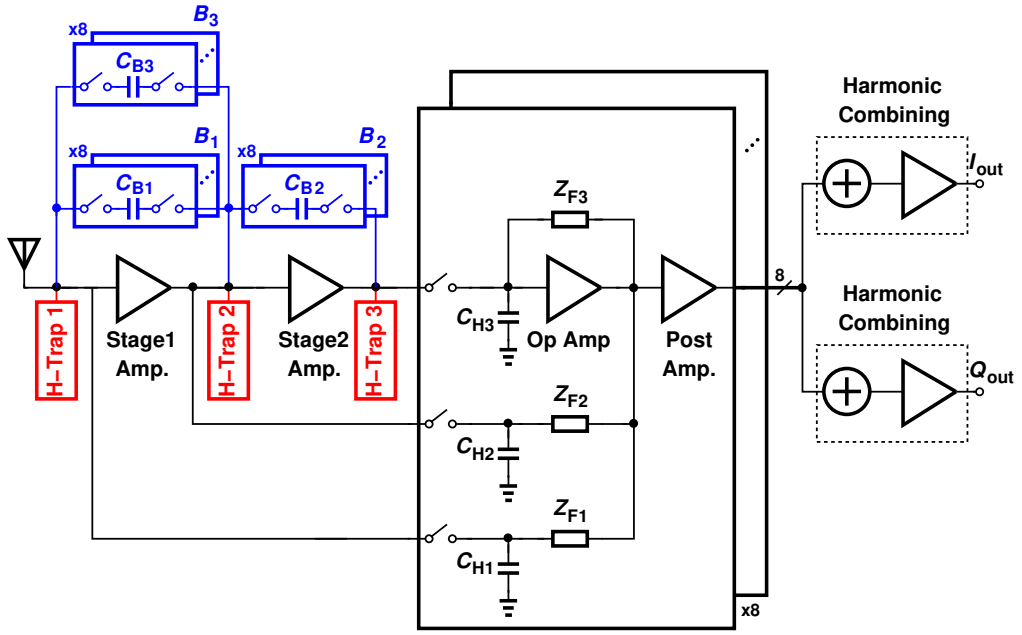
$$\begin{aligned} V_{HR,n,FB} &= -V_{HR,n} A_H K_n \frac{jR_{S,1}C_{HR}\omega_{LO}}{1 + jR_{S,1}C_{HR}\omega_{LO}} \\ &= -\frac{jA_H R_{S,1}C_{HR}\omega_{LO}K_n}{(1 + j(A_H+1)nR_{S,n}C_{HR}\omega_{LO})(1 + jR_{S,1}C_{HR}\omega_{LO})} V_{S,n} \end{aligned} \tag{2.28}$$

Hence, the normalized value of the fold-back component with respect to the main first harmonic component can be written as:

$$\beta_n = \frac{V_{HR,n,FB}}{V_{HR,1}} = -\frac{jA_H R_{S,1}C_{HR}\omega_{LO}K_n}{1 + j(A_H+1)nR_{S,n}C_{HR}\omega_{LO}} \left(\frac{K_n V_{S,n}}{V_{S,1}}\right) \tag{2.29}$$

which implies that the normalized fold-back factor of the H-Trap, β_n, compared to that of the simple half-sine mixer, α_n, is greatly improved. In fact, it is reduced by a factor of $(A_H R_{S,1} C_H R \omega_{LO})/\sqrt{1 + [(A_H+1)nR_{S,n}C_{HR}\omega_{LO}]^2}$. In the case of input node of the LNA with $R_{S,n}/R_{S,1} = 2$, this improvement is greater than 2n which is a factor of 6 for third harmonic and 10 for fifth harmonic. With the values of $R_{S,n}$, A_H and C_{HR} in this design, the improvement factor of third and fifth harmonic are 7.2 and 12 which translate to 17.1 dB and 21.5 dB respectively which indicates the upper bound on the harmonic rejection improvement in the presence of phase mismatch. Another

important factor that indicates the level of harmonic rejection improvement is how much does the H-Trap reject third and fifth harmonics before they enter the regular 8-path filters in the signal path (i.e. B1-B3 and and the 8-feedback paths that connect the outputs of the op amps to each RF node), and fold back onto the first harmonic. In practice we will instantiate three of these H-Traps at the three RF nodes in the signal path (Fig. 2.44) which highly reduces the effect of gain mismatches in the baseband harmonic combiner. The harmonic rejection is then limited by LO phase mismatch in B1 as the harmonics has been attenuated only by H-Trap1 before they enter B1. It depends on how much the harmonic traps in nodes V_{in} and X_1 are able to prevent the harmonic current from flowing through B1. In other words, H-Trap1 attenuates the harmonics right at the input while H-Trap2 reduces the RF gain of the first stage at harmonic frequencies, hence increasing the equivalent Miller impedance of B1 at those harmonics which prevents the harmonic currents from flowing through B1. Monte Carlo simulations suggest that this technique, is able to enhance third and fifth harmonic rejection of the whole receiver by a factor of $\sim$17 dB.

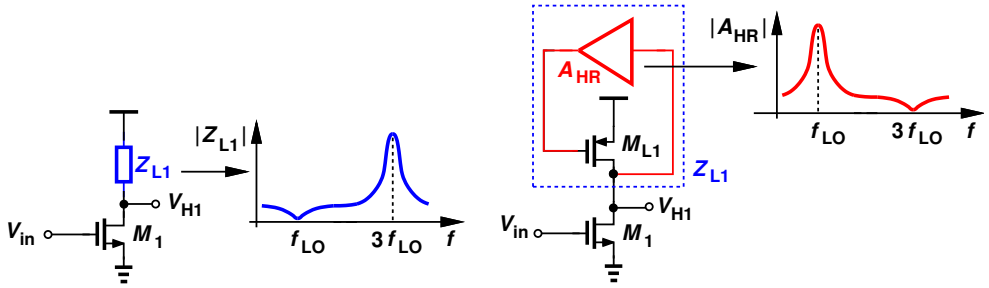


(a)

Figure 2.44. Complete proposed receiver architecture with H-Traps added.

2.5.4 Implementation of the Harmonic Amplifier

Now we will discuss the implementation of the harmonic amplifier. We start with a common source stage with a load Z_{L1} (Fig. 2.45a) which assumes a small magnitude at first harmonic and a large magnitude at higher harmonics, therefore presenting a harmonic enhancing impedance. To implement such impedance, we can take V_{H1}, pass it through a harmonic-reject amplifier and feed it back to the gate of a PMOS transistor (Fig. 2.45b). In order to implement the harmonic-reject amplifier, we exploit the concept of half-sine 8-path structure (Fig 2.40c) and transform it to Fig. 2.46 which benefits from the Miller effect of the second stage of amplifiers to better reject the higher harmonics. To sum the harmonic rejected outputs (Z_a-Z_c) we apply them to the gate of three PFETs whose drain is connected to V_{H1}.

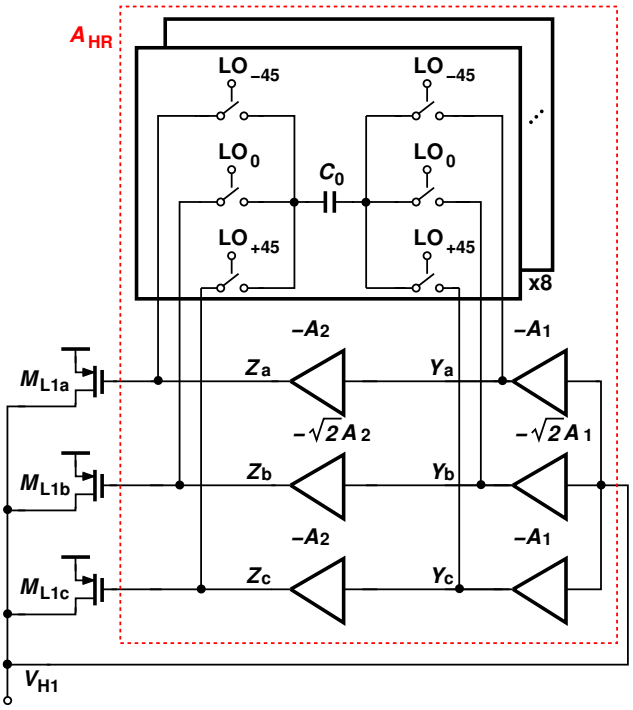


(a) (b)

Figure 2.45. (a) Conceptual implementation of the first stage of the harmonic amplifier and (b) conceptual implementation of Z_{L1}.

To further reject the first harmonic, we use a second stage implemented as a source follower (Fig. 2.47a) in which Z_{L2} is conceptually implemented as in Fig. 2.47b and shown in more details in Fig. 2.48. Please note that Z_{L2} is operating as a DC current source and a harmonic-enhancing load simultaneously.

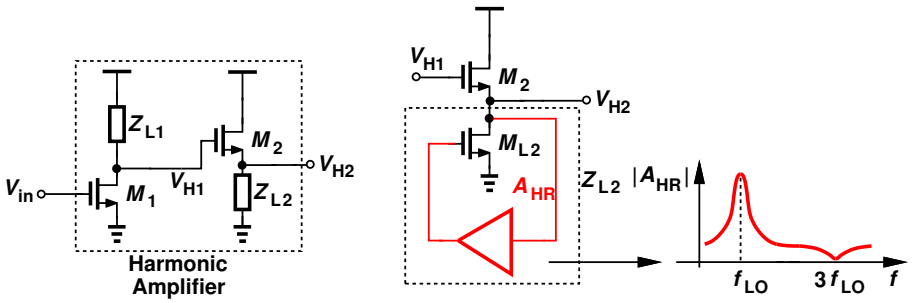
The frequency response of the harmonic amplifier is plotted in Fig. 2.49a for a 1 GHz LO. Fig. 2.49b depicts the frequency response of the harmonic trap of Fig. 2.43 with a $R_{S,n} = 50\Omega$ and $C_{HR} = 600fF$ at 1 GHz LO which clearly shows the effectiveness of this approach in rejecting harmonics. The peaking on the right of the first harmonic is due to the N-path operation and



(a)

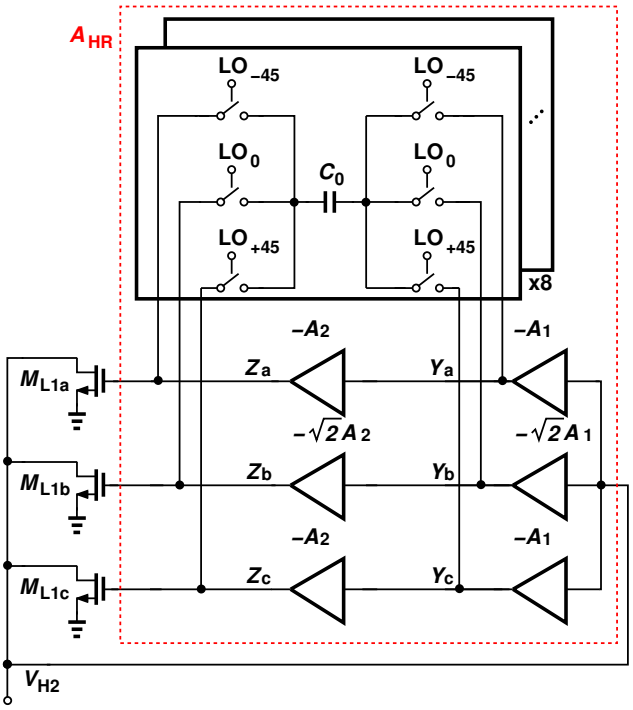
Figure 2.46. Implementation of the harmonic-reject amplifier.

parasitic capacitance which is negligible since signals in the vicinity of the peak frequency are being largely attenuated by B1 and B2 in Fig. 2.44. Also notice that in the receiver $R_{S,1} = 25\Omega$, hence less attenuation at the first harmonic.



(a) (b)

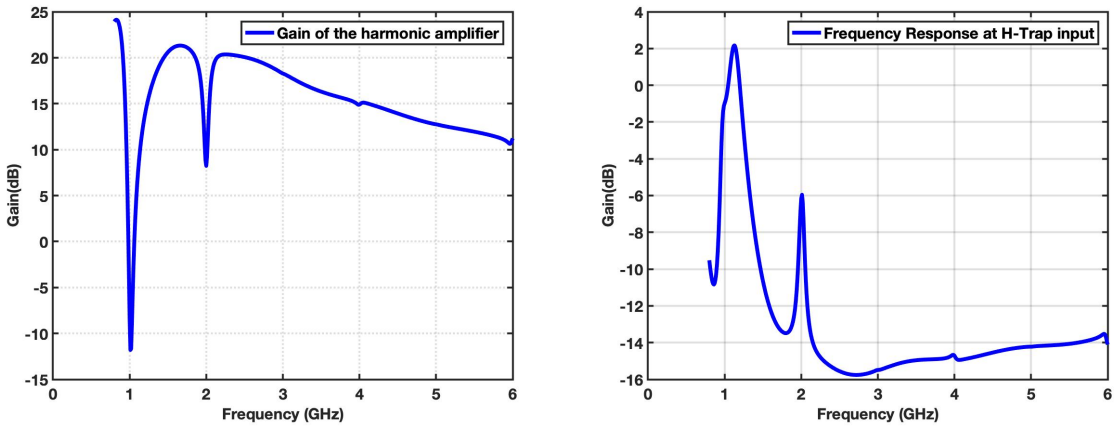
Figure 2.47. (a) Conceptual implementation of the two-stage harmonic amplifier and (b) conceptual implementation of Z_{L2}.



(a)

Figure 2.48. Implementation of the harmonic-reject amplifier for the source follower stage.

Now we discuss the effect of using the three harmonic traps in the receiver focusing on the level of harmonic rejection at the baseband output. Monte Carlo simulations on 50 samples at 1 GHz LO frequency in the schematic mode suggest that with H-Traps off, HR3 and HR5 have an average value of 56.5 dB and 61.4 dB respectively while turning the H-Traps on increases them to 74.3 and 74.8 dB which suggests an enhancement of $>$17 dB for HR3 and $>$13 dB for HR5. It is worthy to note that this enhancement is in the presence of both phase and gain mismatches. Simulations suggest that if we consider only gain mismatches, H-Traps will enhance HR3 and HR5 by more than 26 dB. In practice the layout asymmetry of the eight clock paths driving the 8-path structure adds up to the random phase mismatch modeled by Monte Carlo Simulations.



(a) (b)

Figure 2.49. (a) Harmonic Amplifier Gain and (b) H-Trap Frequency Response.

2.6 Clock Generation

Clock generation is a critical part of any receiver design, specifically in the case of the receivers with 8-path mixers, they need to have non-overlapping 12.5 $\%$ clocks at f_{LO}. Conventionally, these clocks are generated using an input clock at $4f_{LO}$ and divider stages. While a viable solution for frequencies up to 4 GHz, this approach is less favorable at higher LO frequencies as $4f_{LO}$ synthesizer design proves challenging. Therefore, in this design we use a hybrid clock generation circuit that works with a $4f_{LO}$ input clock for LO frequencies up to 4 GHz using divider-based clock generation. For LO frequencies above 4 GHz, it uses a delay-locked loop (DLL) to generate the eight phases of the LO generation with its input clock at f_{LO}. First, we discuss the clock generation circuit based on the frequency division. In this approach a $4f_{LO}$ input clock is fed into two cascaded frequency divider stages as shown in Fig. 2.50a and gets divided by 4. The topology of the latches used in the dividers is C^2MOS as shown in Fig. 2.50b. Then the input clock as well as the outputs of the first and second dividers are fed into an array of eight NOR gates which provide 12.5$\%$ clocks and then goes through four buffer stages before it drives the mixer switches (Fig. 2.51a). The phase order of $4f_{LO}$, $2f_{LO}$ and f_{LO} signals are chosen so as to ensure that the $2f_{LO}$ input 0-state will be completely contained inside the f_{LO} input 0-state and the $4f_{LO}$ input 0-state

is completely contained inside the $2f_{LO}$ input 0-state considering the delay of the divider stages. Waveforms assuming reasonable delays for each divider stage as well as the NOR gate is depicted in Fig. 2.51b. It is important to note that at the NOR gates, each 12.5 $\%$ clock rising and falling edge is being adjusted by one of the $4f_{LO}$ differential inputs, hence, reducing the phase mismatch of the clocks which is important to the harmonic rejection required of the received signals up to 2 GHz.

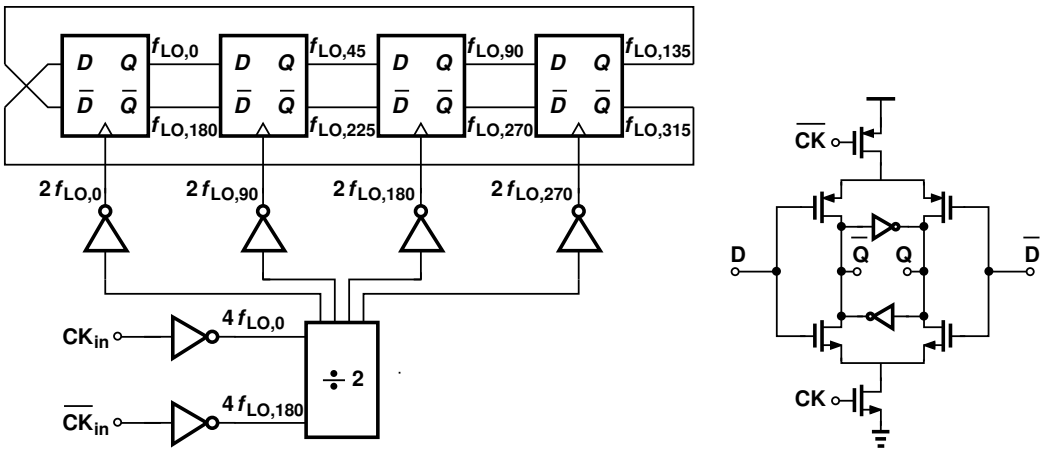


Figure 2.50. (a) 8-phase clock generation based on frequency division and (b) Latch implementation.

For the LO frequencies above 4 GHz, we use an input clock of f_{LO} and generate eight phases using a DLL. As depicted in Fig. 2.52, the input clock is fed into a delay line as well as a phase detector. The delay line consists of four differential delay elements. Each delay element is a pseudo-differential inverter loaded with a varactor (Fig. 2.53) whose value is controlled by the charge-pump output following the phase detector. Also, since the DLL is designed to operate over a wide range, each delay element has a 4-bit binary control capacitor bank which allows it to work from 3 to 7 GHz in order to guarantee its performance at the desired 4-6 GHz frequency range.

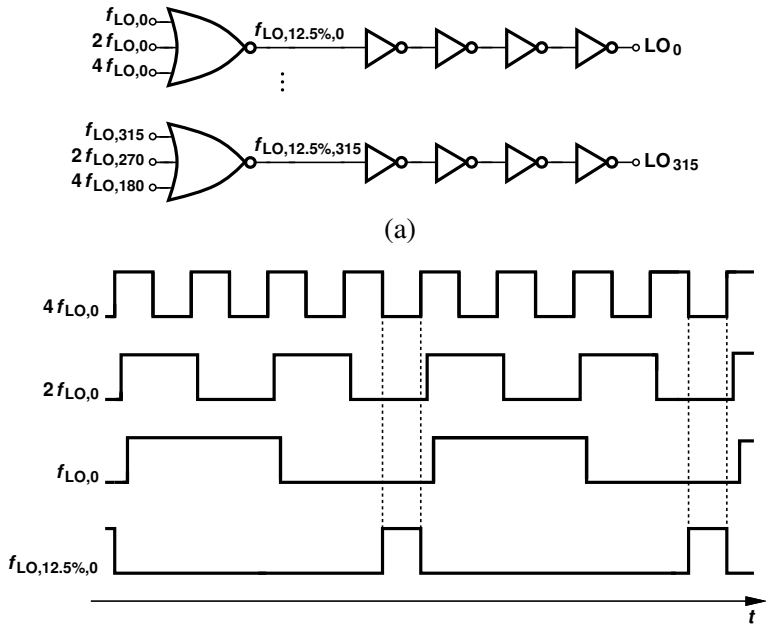


Figure 2.51. (a) 12.5 % clock generation circuit based on dividers outputs and (b) its corresponding clock waveforms.

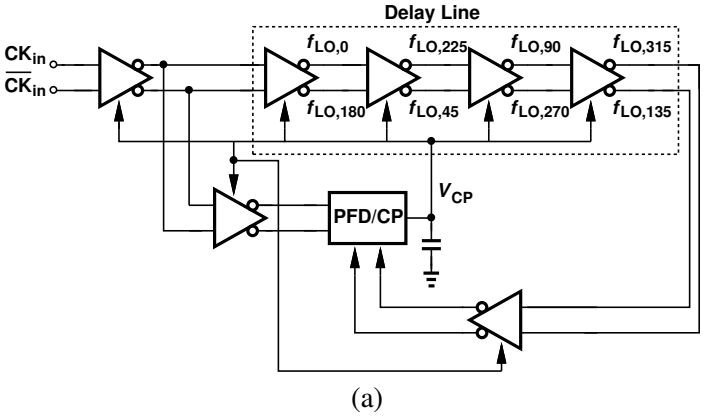
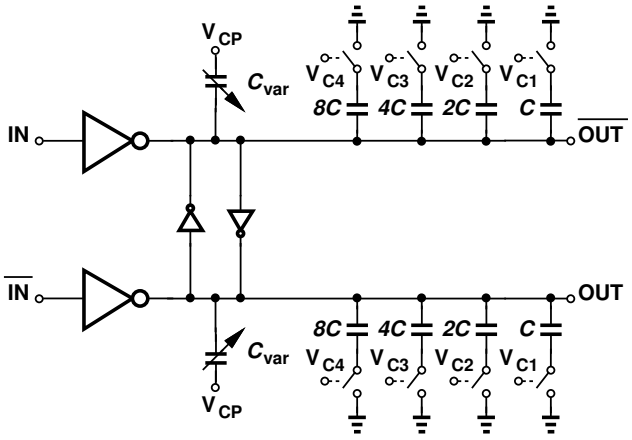
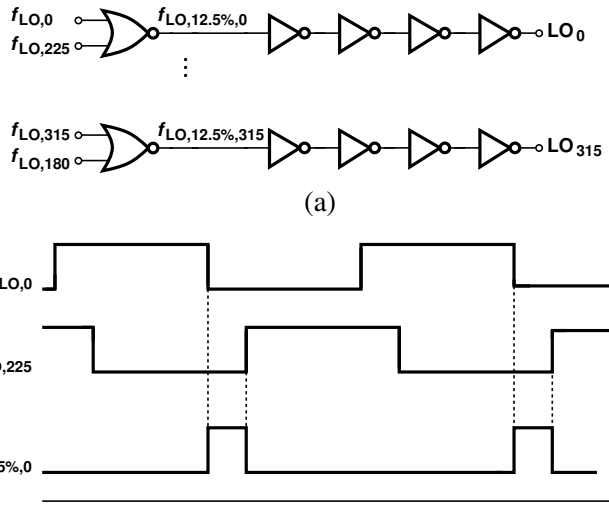


Figure 2.52. 8-phase clock generation based on DLL.



(a)

Figure 2.53. Delay Element implementation.



(a)

(b)

Figure 2.54. (a) 12.5 % clock generation circuit based on DLL outputs and (b) its corresponding clock waveforms.

The eight phases generated in the DLL are then fed into eight NOR gates with the phase order depicted in Fig. 2.54a in order to generate 12.5 % clocks. The 12.5 % clocks are then delivered to the 8-path mixer switches through a four stage buffer line. The buffer stages are common between the clock divider path and the DLL path and are switched to each of them depending on

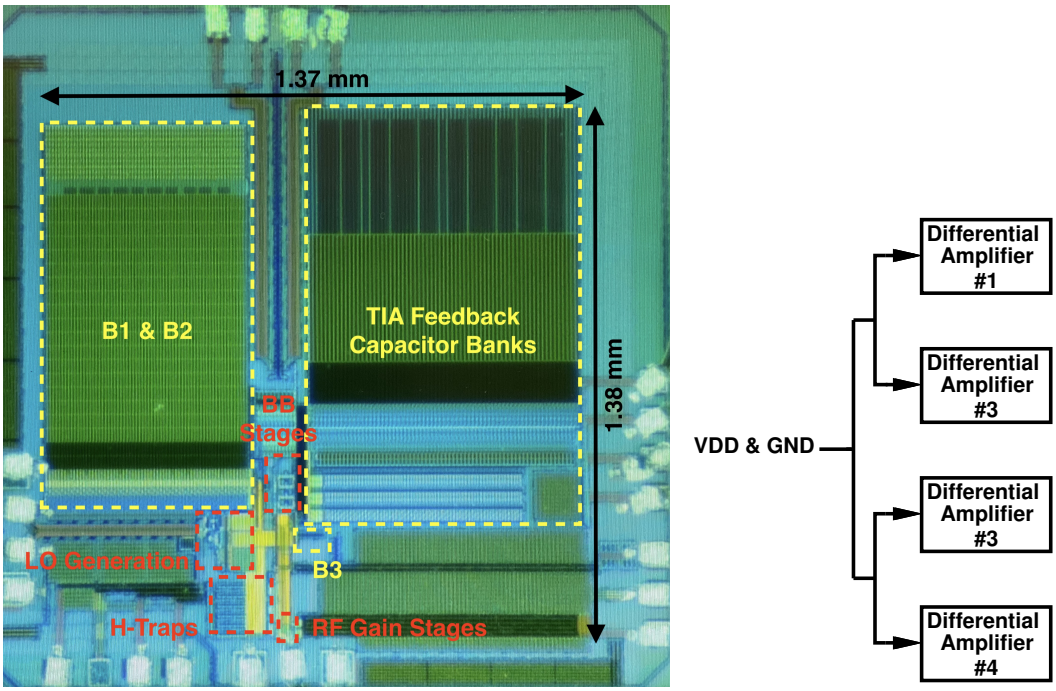
the operating frequency of the receiver. The clock waveforms at the inputs and outputs of the NOR gates are depicted in Fig. 2.54b.

2.7 Experimental Results

The proposed receiver has been fabricated in TSMC's 28-nm CMOS technology. Shown in Fig. 2.55a, the die occupies an active area of 1.9 mm^2. With a 1 V supply, the RF amplifiers draw 9.5 mW, The baseband op amps, post amplifiers and combiners consume 6.4 mW, H-Traps draw 10.5 mW and clock generation circuitry consumes 7.4-28.8 mW depending on the receiver configuration which results in the overall power consumption of 23.3-49.2 mW. Capacitors in B1 and B2 as well as all feedback capacitors from op amp outputs are programmable through an on-chip serial bus so as to support different configurations. It is worthy to mention that in the layout of the baseband section, supply routing of the four differential op amps and post amplifiers play a crucial role in harmonic rejection since any major asymmetry in the supply routing between the baseband amplifier will result in asymmetric DC bias currents and large gain mismatch which results in poor harmonic rejection. Hence, supply routing of the four differential op amps and post amplifiers use a binary tree scheme as shown in Fig. 2.55b which balances the voltage drop over the supply lines, hence, making the DC currents equal. Also all capacitors are implemented as MOM fringe capacitors with ample linearity.

2.7.1 Gain, Noise Figure, Out of Band Blocker Test and Input matching

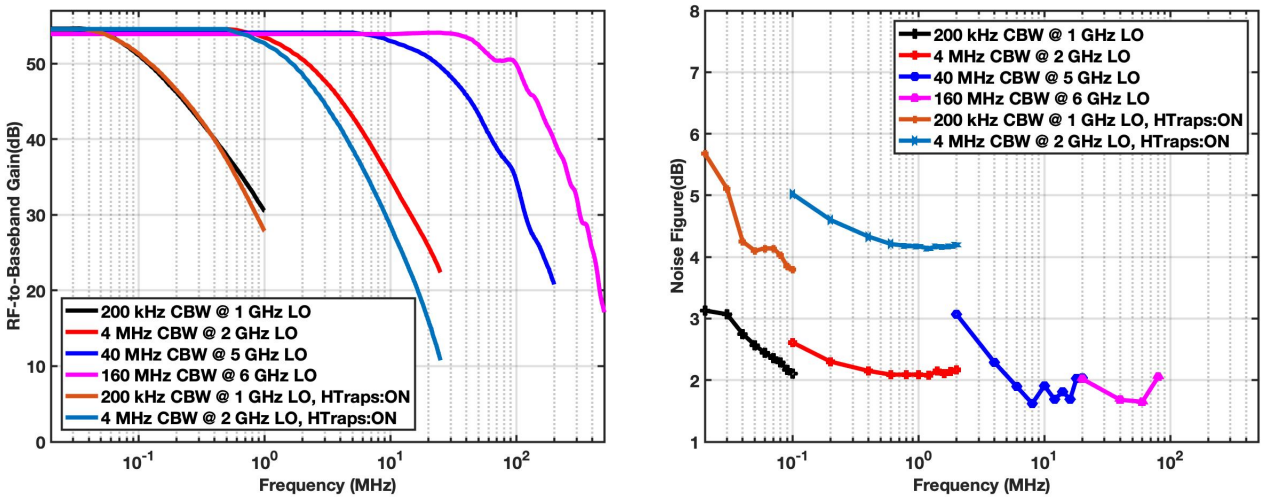
Fig. 2.56a shows the measured RF-to-baseband gain of the receiver for 6 different configurations: 200 kHz bandwidth at 1 GHz with and without H-Traps on, 4 MHz bandwidth at 2 GHz with and without H-Traps on, 40 MHz bandwidth at 5 GHz and 160 MHz bandwidth at 6 GHz. The configurations are chosen to demonstrate a variety of channel bandwidths as well as carrier frequencies. Fig. 2.56b shows the noise figure measurements for the same configurations. First point to notice is that the receiver is capable of maintaining its noise performance across the RF bandwidth. Also,



(a) (b)

Figure 2.55. (a) Die photograph and (b) binary tree layout scheme of supply lines used for the baseband amplifiers.

as the black curve suggests, the receiver shows a noise figure of only 2.1 dB at 100 kHz baseband offset with only 1 dB degradation at 20 kHz offset. Also, when H-Traps are turned on, the noise figure increases by 1.6-2.1 dB depending on the RF frequency. As the next test, we measure the out-of-band blocker tolerance of the receiver. We choose the GSM blocker test with a 0-dBm blocker at 20 MHz offset as the most stringent blocker test to show the superior performance of our proposed receiver in the presence of large blockers. Fig. 2.57 shows the noise figure vs. blocker power for the 200 kHz channel bandwidth at 1 GHz RF frequency. The plots show that at the presence of the 0-dBm blocker, the receiver demonstrates a noise figure of 5.2 dB and 7.4 dB with H-Traps off and H-Traps on respectively. Since a typical RF generator's noise floor at 1 GHz is -152 dBc/Hz, the 0 dBm blocker phase noise at 20 MHz offset, where the desired signal resides, will heavily dominate the noise figure. To overcome this problem, we use a 1 GHz crystal oscillator with the noise floor of -170 dBc/Hz and apply its output to the input of the receiver through



(a) (b)

Figure 2.56. (a) Gain and (b) noise Figure vs frequency offset for different receiver configurations.

a printed circuit notch filter comprising of a microstrip loaded by 7 LC traps that are separated by $\lambda/4$ which provides 11 dB rejection at 20 MHz offset and choose the input signal to be on 980 MHz.

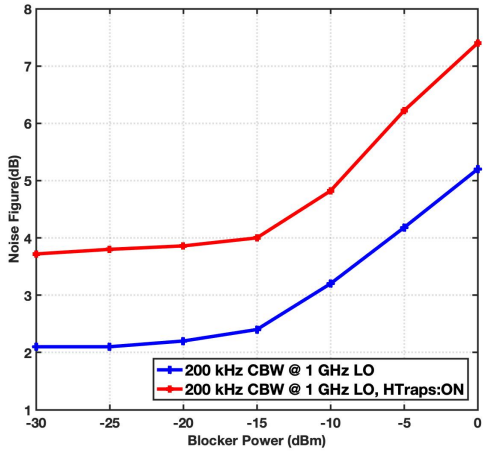


Figure 2.57. Noise figure vs. Blocker power at 20 MHz offset.

Finally, we study the input matching of the receiver. In order to show its performance, we have plotted S_{11} for different channel bandwidths and frequency bands in Fig. 2.58. The plots clearly

show that S_{11} remains below -10 dB well above the required channel bandwidth in all cases. We also should mention that eventually it is B1 - B3 banks that limit the S_{11} due to their band-select properties.

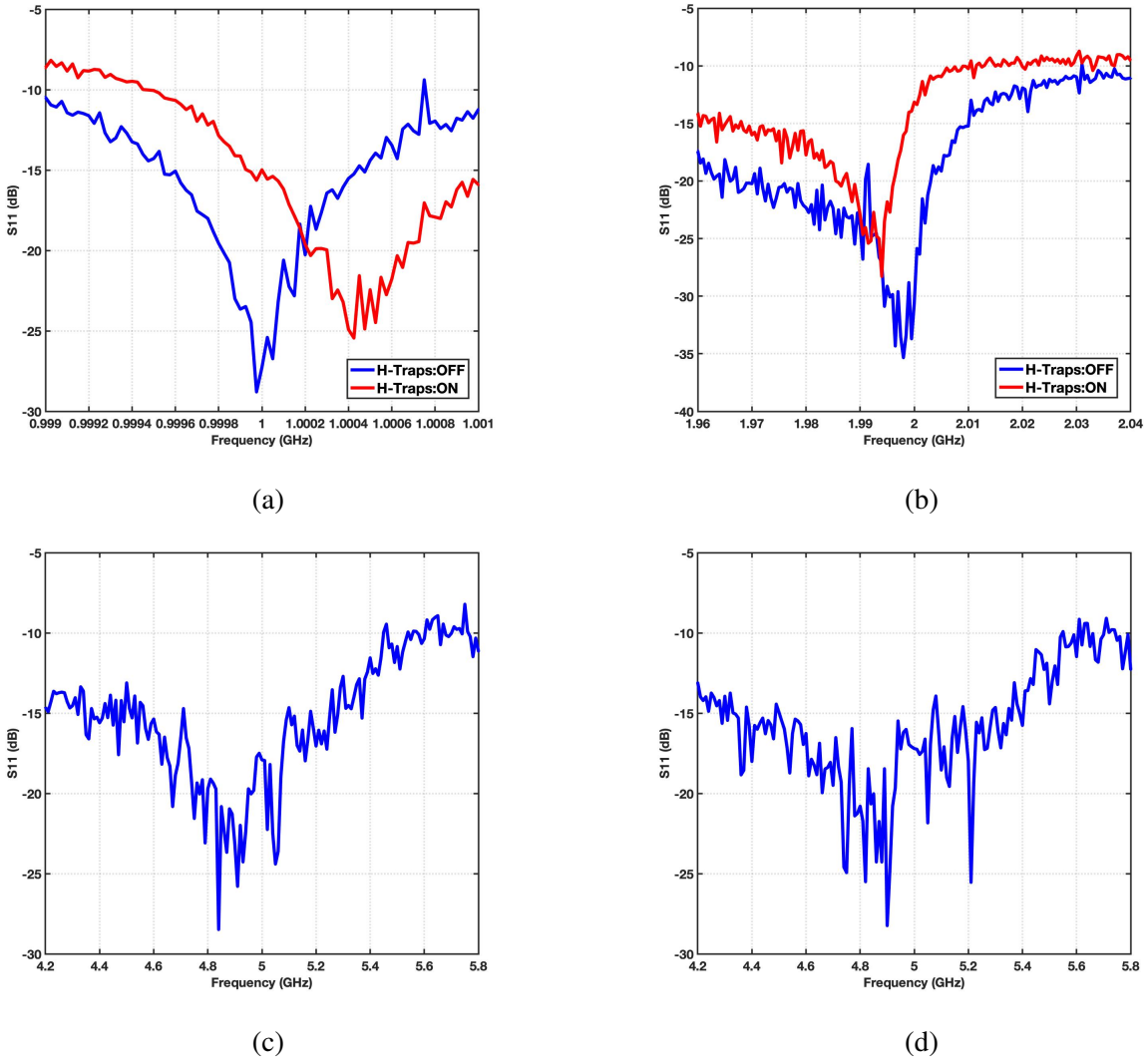


Figure 2.58. Input Matching for (a) 200 kHz CBW at 1 GHz, (b) 4 MHz CBW at 2 GHz, (c) 40 MHz CBW at 5 GHz and (d) 160 MHz CBW at 5 GHz.

2.7.2 Linearity Tests

Now we will check the linearity of the proposed receiver. Fig. 2.59 shows IIP3 and IIP2 for four channel bandwidth configurations at different frequency bands. First we focus on IIP3. As shown in Fig. 2.59 it meets the linearity requirements required of the corresponding frequency offsets.

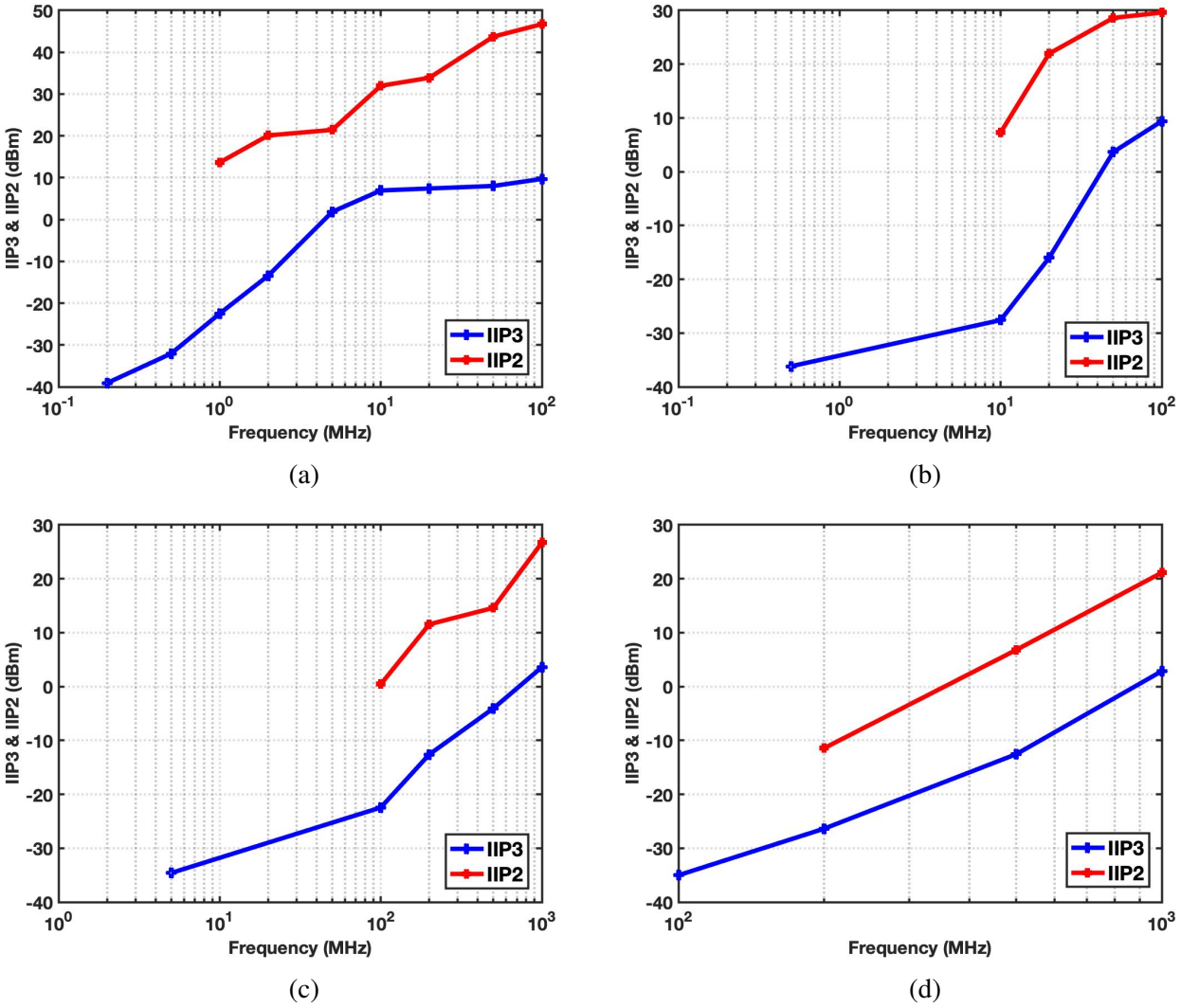


Figure 2.59. IIP3 and IIP2 curves for (a) 200 kHz CBW at 1 GHz, (b) 4 MHz CBW at 2 GHz, (c) 40 MHz CBW at 5 GHz and (d) 160 MHz CBW at 5 GHz.

For IIP3 tests two tones have been applied to the input, one at f_{os} and one at $f_{os} + \Delta f$. Δf

has been chosen to be 20 kHz for 200 kHz channel band width, 500 kHz for 4 MHz Channel bandwidth and 5 MHz for 40 MHz and 160 MHz channel bandwidths. At frequency offsets close to the channel bandwidth the IIP3 is $\sim$ -35 dBm which is highly limited by the open drain NMOS transistors at the output of the receiver chain that are used for measurement purposes and are not a part of the receiver chain. Simulations suggest that IIP3 of the receiver without the output open-drain NMOS transistors is $\sim$ 10 dB higher. However, as discussed in section 2.4.1, since we engineer the voltage gain, such that the first large voltage gain takes place at the output of the op amps, where channel selection is applied, at the frequency offsets where in-band blockers reside, the IIP3 is above -12 dBm which satisfies the requirements, yet limited by the output open-drain NMOS transistors. In the case of 200 kHz and 4 MHz channel bandwidth where out-of-band blocker rejection banks (B1 and B2) are on, they will take over the frequency response for large frequency offsets and further attenuate the signals and improve the linearity until IIP3 reaches its maximum of 9.8 dBm. It is important to note that since IIP3 reaches a plateau at this level, it could be inferred that it is dominated by the RF gain stages, mixer switches and op amps. If it was dominated by the latter stages it should have kept improving due to higher rejection provided by channel selection banks. We can also see this phenomenon as we compare the out-of-band IIP3 (OB-IIP3) of the 200 kHz and 4 MHz where both show $\sim$10 dBm IIP3 at 100 MHz while the level of out-of-band rejection due to channel selection is far more in the case of 200 kHz offset. In the case of 40 MHz and 160 MHz, the OB-IIP3 is limited to 3 dBm due to smaller switches used in B3 compared to B1 and B2 as a results of less sever blocker requirements, which needs less out-of-band blocker rejection.

For IIP2 tests two tones have been applied to the input, one at f_{os} and one at $1.8f_{os}$ to make sure that the second order inter-modulation (IM2) product falls near the two main tones ($0.8f_{os}$) and experiences a similar gain in the receiver chain. Since IIP2 is less restricted due to the differential and pseudo-differential topology of the baseband stages, the IIP2 measurements start at farther frequency offsets to show the performance of the circuit at higher frequency offsets with stronger blockers. It is important to note that in a receiver chain with differential and pseudo-differential

baseband stages, the IM2 components produced in the prior stages get highly rejected by the common mode rejection ratio of the latter differential and pseudo-differential stages. As we go towards the end of the receiver chain, the level of this rejection reduces and reaches its minimum at the last stage which in the case of our proposed receiver are the open-drain NMOS transistors. Eventually the IM2 component which is a common mode signal will be sensed at the output due to the asymmetry of the output wirebonds, transmission lines and, the differential to single-ended balun. The fact that most of the IM2 component comes from the last baseband stages manifests itself in the comparison of the IIP2 between different channel bandwidths at the same frequency offset. As an example comparing the IIP2 at 100 MHz offset in 200 kHz, 40 MHz and 160 MHz channel bandwidths shows that IIP2 decreases as the channel bandwidth increases, hence less rejection before the latter baseband stages.

2.7.3 Harmonic Rejection Tests

The harmonic rejection tests have been conducted over a range of frequencies from 0.4 to 2 GHz as the frequencies for which third and fifth harmonic rejection are important. Fig. 2.60 shows the third and fifth harmonic rejection tested on a single chip across the above-mentioned frequency range with and without H-Traps. The results show an average of $\sim$ 17 dB improvement in harmonic rejection with H-Traps on. Both with and without H-Traps, clock phase mismatch is the bottleneck. We should remark that both HR3 and HR5 stay above 60.8 dB across the entire targeted frequency range.

2.7.4 EVM Tests

Finally we test the receiver with real modulated signals for two popular standards, i.e. LTE and WiFi 6. Fig. 2.61 shows the constellation and EVM numbers for two tests. First test is for a 64-QAM LTE signal with 20 MHz channel bandwidth at 2 GHz, showing an EVM of -22.15 dB at -74 dBm input power. Second test is for a 256-QAM 802.11 ax signal with 80 MHz channel bandwidth

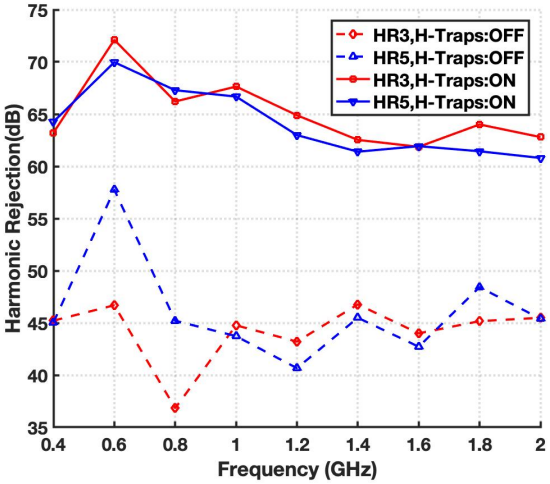
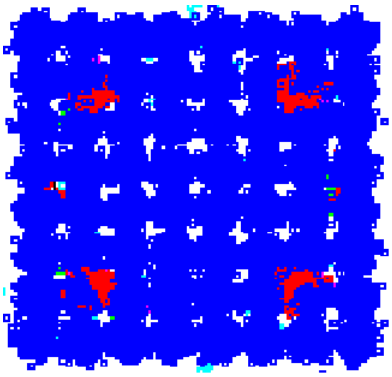


Figure 2.60. Harmonic rejection vs. Input frequency.

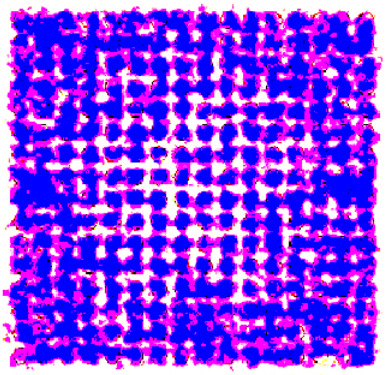
at 5 GHz that demonstrates an EVM of -25.21 dB at -57 dBm input power. The modulated RF signals were generated using Keysight N5182b MXG vector signal generator and the baseband outputs were analyzed by Keysight N9030A PXA signal analyzer. Unfortunately, we were not able to test 160 MHz bandwidth due to the limited analysis bandwidth of the baseband inputs on the N9030A. Table I summarizes the performance of our receiver and several state-of-the art designs.

2.8 Conclusion

The idea of multi-loop feedback highly relaxes the linearity and noise figure requirements of the receiver, breaking the trade-off between the flicker noise and the supported channel bandwidth in the baseband stages. We have boosted the baseband transconductance by a factor of 8 by adding memory to the baseband side of the mixers through the use of hold capacitors. Proportional capacitor allocation guarantees input matching far above the channel bandwidth and symmetric frequency response. The proposed op amp topology provides high gain and wide bandwidth with a low power consumption. Additional blocker rejection banks, help satisfy out-of-band blocker requirements while a frequency response correction bank guaranties symmetric frequency response and stability.



Standard	LTE
Modulation Scheme	64-QAM
Carrier Frequency [GHZ]	2
Channel Bandwidth [MHz]	20
Input Power [dBm]	-74
EVM [dB]	-22.15



Standard	802.11 ax
Modulation Scheme	256-QAM
Carrier Frequency [GHZ]	5
Channel Bandwidth [MHz]	80
Input Power [dBm]	-57
EVM [dB]	-25.21

Figure 2.61. EVM test for LTE and 802.11ax.

Finally, the harmonic trap concept has been introduced to reject the harmonic blockers beyond the limits of baseband harmonic combiners and alleviate the problem of clock phase mismatch.

Appendix I: An Analysis on Multi-Loop Feedback Receiver Noise Performance

In this section we provide a more accurate and general analysis for noise and gain performance of multi-loop feedback structure by writing the KCL at each node and deriving the minimum requirements that will satisfy both input-referred noise reduction and RF gain reduction. We start from a single feedback loop as depicted in Fig. 2.9b. Writing the KCL equations at nodes X_2 and

Table 2.1. Receiver performance summary and comparison

	[8]	[12]	[14]	[10]	[16]	This work
RF Input	Single-ended	Single-ended	Differential	Single-ended	Single-ended	Single-ended
Input Frequency [MHz]	80-2700	0.2-2000	400~6000	600~3000	500-3000	400-6000
Channel Bandwidth [MHz]	0.35-20	N/A	1-100	0.4-6	40-98	0.2-160
Gain [dB]	38	40	70/58[1]	N/A	38-46	54
NF [dB]	2.9	2.1-2.5	2.4[2,6]/3.1[4,6]	1.8[2]/3[3]	2.5-5	2.1[2]/4.2[3]
0-dBm OB-Blocker NF [dB]	5.1	6.7	10[5,6]/14[4,6]	9[2]/13[3]	9 (@ -5 dBm)	5.2[2]/7.4[3]
OB-IIP3 [dBm]	10	+14	8[5]/3[4]	10	+4	9.8/2.8[7]
Harmonic Rejection (HR) [dB] $3f_{LO}/5f_{LO}$	35/45	N/A	70/75	52/54	80	63/64 (62/60.8)[8]
EVM (dB)	N/A	N/A	N/A	N/A	N/A	-22.1[9]/-25.2[10]
HR Calibration	N/A	N/A	Yes	No	Yes	No
Power Consumption [mW]	20	68-95	40	38.8-70	28-31	23-49
CMOS Technology	65 nm	45 nm SOI	28 nm	28 nm	28 nm	28 nm

[1]Above 3 GHz [2]Low noise mode [3]Harmonic rejection mode [4]Standard operation [5]LNA optimized [6]Balun loss not included [7]With B1 and B2 turned off and B3 turned on for channel bandwidths more than 4 MHz with less stringent blocker requirements [8]Up to 2 GHz [9]LTE [9]WiFi 6

V_{out} will result in the following equation for the gain at node X_2:

$$\frac{V_{X_2}}{V_{in}} = -G_{m2}(R_2||R_{X2}) = -\frac{G_{m2}R_2}{1+\frac{G_{mT}R_2R_{F2}}{G_{mT}R_{sw}R_{F2}+R_{F2}+R_{F3}}} \tag{2.30}$$

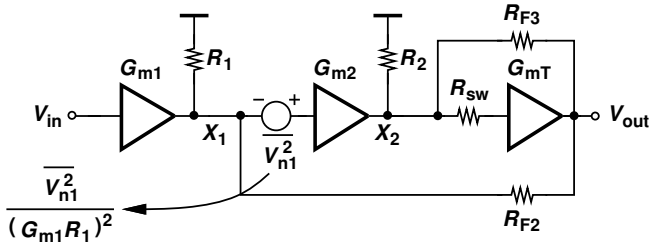
In order to calculate the input referred noise, we first calculate output noise and the overall gain by writing the KCL equations at nodes X_1 and V_{out}. Our assumptions are $R_{F3} >> R_2 + R_{sw}$ and $G_{mT}R_{F3} >> 1$ which are all valid in this design. We also reasonably assume that R_{F3} is much larger than the output resistance of the op amp, hence, all of the op amp current will be steered to R_{F3}.

$$\frac{V_{out}}{V_{in}} = G_{m2}R_{F3}\frac{G_{mT}R_2}{G_{mT}(R_2+R_{sw})+1} \tag{2.31}$$

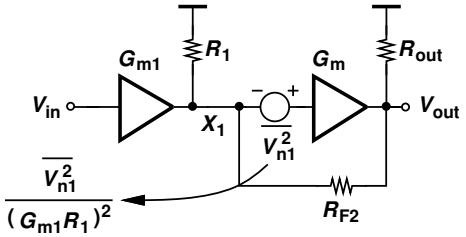
$$V_{n,out} = -\frac{G_{mT}R_{F3}}{G_{mT}(R_2+R_{sw})+1}V_n \tag{2.32}$$

Hence, the input referred noise would be:

$$V^2_{n,input,CL} = \frac{V_n^2}{(G_{m2}R_2)^2} \tag{2.33}$$



(a)



(b)

Figure 2.62. (a) Baseband equivalent of two RF gain stage preceding the op amp with nested feedback and (b) its equivalent model by replacing the inner loop with its Norton equivalent.

It is important to note that this result does not require the simplifying assumption of $R_{X2} << R_2$ which we assumed in our previous analysis. Now, we continue our analysis to the dual-loop feedback of Fig. 2.62a. We can now model the inner loop as a trans-conductance in parallel with an output resistance as shown in Fig. 2.62b, where $G_m = G_{m2}G_{mT}R_2$ and $R_{out} = R_{F3}/(1 + G_{mT}(R_{sw} + R_2))$. Our assumptions are $R_{F2} >> R_1$, $R_{F2} >> R_{out}$ and $G_m R_{out} >> 1$ which are all valid in our design. The gain of the first stage will then be calculated as:

$$\frac{V_{X_1}}{V_{in}} = -\frac{G_{m1}R_1}{1 + \frac{G_m R_{out} R_1}{R_{F2}}} \tag{2.34}$$

In order to calculate the input referred noise we first calculate the overall gain and output noise, noting that $V_{n1} = -V_n/(G_{m2}R_2)$.

$$\frac{V_{out}}{V_{in}} = G_{m1}[R_{F2}||(G_m R_{out} R_1)] \tag{2.35}$$

$$V_{n,out} = -\frac{R_{F2}||(G_m R_{out} R_1)}{R_1} V_{n1} \tag{2.36}$$

Therefore, the input referred noise could be derived as:

$$V_{n,input,CL}^2 = \frac{V_{n1}^2}{(G_{m1}R_1)^2} = \frac{V_n^2}{(G_{m1}R_1G_{m2}R_2)^2} \tag{2.37}$$

Appendix II: An Analysis on the Input Impedance of An N-Path Filter With Low-Pass Load

In this appendix we study the input impedance looking at an N-path filter loaded with low-pass impedance, $Z_{BB}(j\omega)$ as shown in Fig. 2.63a. Our approach is similar to that used in [21]. In the time domain we show the parameters with small letters and the corresponding parameters in the frequency domain are represented with capital letters. We begin our analysis in the time domain. The input current, $i_{in}(t)$ is chopped by $s_i(t)$ in each branch and then applied to the low-pass impedance. This means that the voltage created on the low-pass impedance in the ith path is equal to:

$$v_{BB,i}(t) = [i_{in}(t)s_i(t)] * z_{BB}(t) \tag{2.38}$$

Then the voltage on each path is sampled by $s_i(t)$ and summed at V_{in}. Hence, we can write $v_{in}(t)$ as:

$$v_{in}(t) = \sum_{i=1}^{8}\{[i_{in}(t)s_i(t)] * z_{BB}(t)\}s_i(t) \tag{2.39}$$

Now, we convert this result to the frequency domain:

$$V_{in}(j\omega) = \sum_{i=1}^{8}\{[I_{in}(j\omega) * S_i(j\omega)]Z_{BB}(i\omega)\} * S_i(j\omega) \tag{2.40}$$

at this point we need to have the Fourier transform of $s_i(t)$ which is a 12.5$\%$ clock with a frequency of ω_{LO} and its rising edges at $[k + (i-1)/N]T_{LO}, (k \in \mathbb{Z})$ as shown in Fig. 2.63b. The Fourier

transform of this waveform would be:

$$S_i(j\omega) = \sum_{n=-\infty}^{+\infty} a_n e^{-j(i-1)n\frac{2\pi}{N}} \delta(\omega - n\omega_{LO})$$
$$a_n = \frac{sin(\frac{n\pi}{N})}{n\pi} e^{-jn\frac{2\pi}{N}} \tag{2.41}$$

Thus, (2.40) could be written as:

$$V_{in}(j\omega) = \sum_{i=1}^{8} \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} a_n a_m I_{in}\{j[\omega - (n+m)\omega_{LO}]\} Z_{BB}(\omega - m\omega_{LO}) e^{-j(i-1)n\frac{2\pi}{N}}$$
$$= \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} a_n a_m I_{in}\{j[\omega - (n+m)\omega_{LO}]\} Z_{BB}(\omega - m\omega_{LO}) [\sum_{i=1}^{8} e^{-j(i-1)(n+m)\frac{2\pi}{N}}] \tag{2.42}$$

The term $\sum_{i=1}^{8} e^{-j(i-1)(n+m)\frac{2\pi}{N}}$ in (2.42) is equal to N for $m + n = kN, (k \in \mathbb{Z})$ and zero otherwise. Therefore, (2.42) could be simplified to:

$$V_{in}(j\omega) = N \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} a_n a_m I_{in}\{j[\omega - (n+m)\omega_{LO}]\} Z_{BB}(\omega - m\omega_{LO})$$
$$(m + n = kN, k \in \mathbb{Z}) \tag{2.43}$$

We assume $I_{in}(j\omega)$ to be close to the LO frequency. In order to define the input impedance, we are only interested in the part of $V_{in}(j\omega)$ that is close to the LO frequency, Therefore (2.45) will be further simplified to:

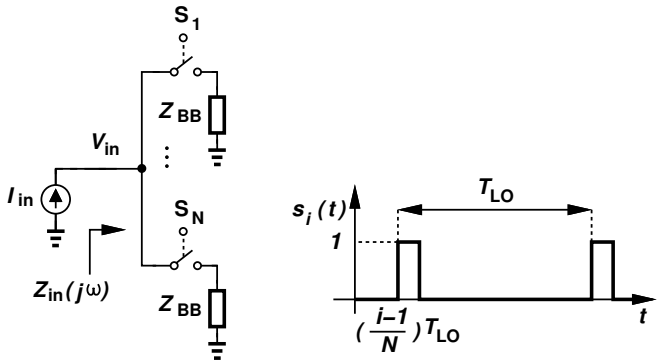
$$V_{in}(j\omega) = N \sum_{n=-\infty}^{+\infty} a_n a_{-n} I_{in}(j\omega) Z_{BB}(\omega + n\omega_{LO})$$
$$= N \sum_{n=-\infty}^{+\infty} [\frac{sin(\frac{n\pi}{N})}{n\pi}]^2 I_{in}(j\omega) Z_{BB}(\omega + n\omega_{LO}) \tag{2.44}$$

Now, since $Z_{BB}(j\omega)$ is a low-pass impedance that has negligible values at frequencies around ω_{LO} and its harmonics, only $n = -1$ will be considered in (2.44) when the desired ω is in the vicinity

of ω_{LO}. Then the input impedance could be written as:

$$Z_{in}(j\omega) = N[\frac{sin(\frac{n\pi}{N})}{n\pi}]^2 Z_{BB}(\omega - \omega_{LO}) \approx \frac{Z_{BB}}{N} \tag{2.45}$$

Which proves that in the case of a low-pass load impedance in an N-path filter, the equivalent RF impedance is equal to the baseband impedance divided by N.



(a) (b)

Figure 2.63. (a) An N-path filter with a low-pass load (b) Waveform of $s_i(t)$.

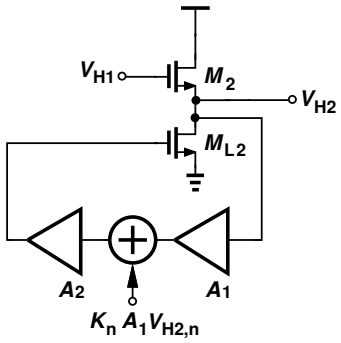
Appendix III: An Analysis on The Harmonic Fold-Back Behavior of The Harmonic Amplifier

In this appendix we aim to show that if the fold-back factor of a simple half-sine filter (Fig. 2.40c) from the nth harmonic to the first harmonic is K_n, then the fold-back factor at the output of the harmonic amplifier is also almost equal to K_n. It is important to note that in the two stage harmonic amplifier of Fig. 2.47a the main fold-back component comes from the second stage because the fold-back component produced in the first stage gets heavily attenuated in the second stage by Z_{H2} since it resides at the first harmonic. Second, we can model the second stage as shown in Fig. 2.64 in which the equivalent model of Z_{H2} is valid for the first harmonic. The $A_1 K_n V_{out,n}$ component added after the first stage is to model the fold-back component from the nth harmonic to the first harmonic produced by the half-sine mixer at the output of A_1. Assuming that the the

gain produced by the trans-conductance of M_{L2} at the output node is A_3, we derive the equivalent fold-back component of the harmonic amplifier at the output node to be:

$$V_{H2,FB,n} = -\frac{A_1 A_2 A_3}{A_1 A_2 A_3 + 1} K_n V_{H2,n} \approx -K_n V_{H2,n} \tag{2.46}$$

Which holds the assumption of $A_1 A_2 A_3 >> 1$ that is valid in this design. As (2.46) suggests, the fold-back factor of the harmonic amplifier is equal to that of a simple half-sine 8-path structure.



(a)

Figure 2.64. Equivalent model of the second stage of the harmonic amplifier at the first harmonic.

CHAPTER 3

Study of Injection Locking in Oscillators and Frequency Dividers

3.1 Problem Statement

Injection locking has always been an interesting and intractable phenomenon in the clock generation circuit design. Injection locking, injection pulling and phase noise are the three main phenomena that happen in the context of oscillation and all are from one root: Power injection to the oscillator at a different frequency from the oscillator's natural resonance frequency. If the injected power shows a low power noise spectrum, it results in phase noise. If it is a tone with slightly higher power and at a frequency sufficiently far from the oscillator's natural resonance it causes pulling. Eventually, if it is a strong enough tone at a close enough frequency, it results in injection locking.

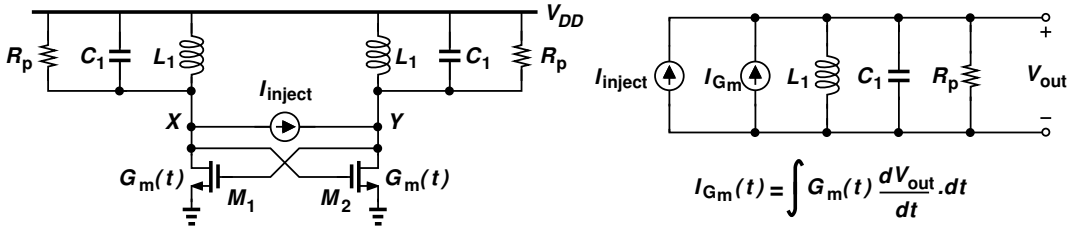
While phase noise and injection pulling are unwanted phenomena and most of the theoretical frame works developed to understand them are meant to provide remedies to reduce them, injection locking could be a desirable phenomenon and finds application in frequency generation circuits such as quadrature oscillators and frequency dividers. Therefore, the models developed for injection locking must be able to provide insights on how to optimize the design parameters to increase the performance in circuits utilizing injection locking.

Prior models developed for injection locking ([22]-[25]) are based on geometrical phasor analysis which makes the models somewhat descriptive. In addition, some of them are developed under simplifying assumptions such as low power injection ([22],[23]) or hard-limiting operation of the

cross-coupled pair ([25]). In this work we develop a theoretical frame work based on the oscillator linear time-variant model ([26]) which results in two closed form equations that governs the injection locking with no need to a descriptive phasor analysis. In the next step, we extend this technique to direct injection locked frequency dividers (DILFDs) which results in new insights into the operation of the DILFDs and defines criteria for optimized performance of them. Eventually we propose the use of quadrature coupling in the DILFDs - which further increases the lock range - and provide the optimum coupling criteria using the same framework. These improvements results in unprecedented wide lock rage that obviates the need for heavy frequency tuning of the frequency dividers ([27],[28]].

3.2 Oscillator Linear Time-Variant Injection Model

We start with a a cross-coupled oscillator that has an injection current at its output as depicted in Fig. 3.1a. The equivalent half-circuit model to be used in our analysis is illustrated in Fig. 3.1b. Before we start the analysis, we have to state our assumptions. First, we assume that the LC tank is capable of filtering the higher order harmonics and the DC component of its input current sufficiently, such that we can assume a pure sine wave at the output, i.e. $V_{out}(t) = V_0 cos(\omega t + \phi)$ where ϕ denotes the phase difference between the output voltage and the injected current, $I_{inject}(t) = I_{inj}\, cos(\omega t)$. Second, Similar to [26], we assume that the cross coupled transistors current exhibits a memory-less odd-order non-linear dependency to V_{out}, i.e.:



(a) (b)

Figure 3.1. (a) A cross-coupled oscillator under injection and (b) its half-circuit equivalent model.

$$I_{G_m} = I_{DC} + \alpha_1 V_{out} + \alpha_3 V_{out}^3 + \alpha_5 V_{out}^5 + ... \tag{3.1}$$

Then the definition of transconductance i.e. $G_m = dI_{Gm}/dV_{out}$ together with our first and second assumption lead to a time variant transconductance expressed in (3.2).

$$G_m(t) = G_{m_0} + 2\sum_{n=1}^{\infty} G_{m_{2n}}\, cos(2n\omega t + 2n\phi) \tag{3.2}$$

Now that we have set the ground for the analysis, we start our analysis with writing a KCL at the output:

$$I_{Tank} = I_{G_m} + I_{inject} \tag{3.3}$$

We start from I_{Tank} and write it as (3.4):

$$I_{Tank} = \frac{V_0}{R_p}\, cos(\omega t + \phi) + \frac{V_0}{L_1\omega}\, sin(\omega t + \phi) - V_0 C_1 \omega\, sin(\omega t) \tag{3.4}$$

Then we rewrite the injection current as (3.5):

$$I_{inject} = I_{inj}\, cos(\phi)\, cos(\omega t + \phi) + I_{inj}\, sin(\phi)\, sin(\omega t + \phi) \tag{3.5}$$

Finally we write the cross-coupled pair current

$$I_{G_m} = I_{DC} + \int_0^t G_m(t)\frac{dV_{out}}{d\tau}.d\tau = I_{DC} - V_0\omega \int_0^t G_m(t)\, sin(\omega t + \phi).d\tau \tag{3.6}$$

We should note that the the lower bound of the integration in (3.6) is not important as it only results in a DC term which gets absorbed in I_{DC}. We are only looking for the first harmonic component of the current as we have previously assumed that DC component and higher harmonics are filtered by the LC tank. Now we substitute (3.2) in (3.6) and only take the first harmonic components which results in (3.7):

$$I_{G_m} = (G_{m0} - G_{m2})V_0\, cos(\omega t + \phi) \tag{3.7}$$

Now we substitute (3.4),(3.5) and (3.7) in (3.3) and decompose the resulting equation into two independent equations based on the orthogonality of $sin(\omega t + \phi)$ and $cos(\omega t + \phi)$ which results in the following two equations:

$$\frac{1}{R_p} = G_{m_0} - G_{m_2} + \frac{I_{inj}}{V_0}\, cos(\phi) \tag{3.8}$$

$$\Delta\omega C_1(\frac{\omega + \omega_0}{\omega}) = -\frac{I_{inj}}{V_0}\, sin(\phi) \tag{3.9}$$

With ω defined as the injection (and oscillation) frequency, ω_0 the resonance frequency of the LC tank and $\Delta\omega = \omega - \omega_0$. Equations (3.8) and (3.9) are the fundamental equations governing the oscillation under injection (Interestingly, (3.8) can be obtained also by using the law of conservation of energy in the oscillator which is presented in appendix I). As the injection frequency (ω) or magnitude (I_{inj}) changes, the system regulates V_0 and ϕ such that both (3.8) and (3.9) are satisfied. note that as V_0 changes, so does $G_{m_0} - G_{m_2}$. In order to further simplify the two fundamental equations, we begin with the $(\omega + \omega_0)/\omega$ term in (3.9). If we start from $\omega = 0.5\omega_0$ and gradually increase its value to ω_0 and even further to $2\omega_0$, we observe that the value of $(\omega + \omega_0)/\omega$ changes from 3 to 2 and eventually reaches 1.5. Therefore assuming $(\omega + \omega_0)/\omega = 2$ is an acceptable approximation for a feasible range of ω. Second, as in [24], we assume that the cross-coupled pair current is defined by a tail current and is equal to $I_{osc}\, cos(\omega t + \phi)$. Then from (3.7) we can write:

$$G_{m0} - G_{m2} = \frac{I_{osc}}{V_0} \tag{3.10}$$

The two simplifying assumptions transform (3.8) and (3.9) into the following equations:

$$\frac{1}{R_p} = \frac{I_{osc}}{V_0} + \frac{I_{inj}}{V_0}\, cos(\phi) \tag{3.11}$$

$$2\Delta\omega C_1 = -\frac{I_{inj}}{V_0}\, sin(\phi) \tag{3.12}$$

Removing V_0 from the above two equations and replacing C_1 with $Q/(R_p\omega_0)$ -where Q is the quality factor of the tank- will result in the following relationship:

$$|\Delta\omega| = \frac{\omega_0}{2Q}\frac{I_{inj}sin(\phi)}{I_{osc} + I_{inj}cos(\phi)} \tag{3.13}$$

For a given injection level, we seek to find the maximum $\Delta\omega$ that the circuit can still lock to the injection frequency. Hence we take the derivative of (3.13) with respect to ϕ which results in the following optimum phase difference and lock range:

$$\phi_{opt} = cos^{-1}(\frac{I_{inj}}{I_{osc}}) \tag{3.14}$$

$$|\Delta\omega|_{max} = \frac{\omega_0}{2Q}\frac{1}{\sqrt{(\frac{I_{osc}}{I_{inj}})^2 - 1}} \tag{3.15}$$

Which is in line with the result obtained in [24]. We wish to discuss two especial cases: 1) The case which the injection frequency is equal to the tank resonance frequency, i.e. $\Delta\omega = 0$ which results in $\phi = 0$ and maximum V_0. In other words in the middle of lock range, the injection current and oscillator current are in phase which results in maximum output voltage swing. 2) The case which injection level is much smaller than the oscillator current. According to (3.14) the optimum value of phase difference is $\sim \pm 90^\circ$ which suggests that maximum lock range occurs when the injection's peaks occur at the zero-crossings of the output voltage.

3.3 Injection Locking in DILFDs

Analysis of direct injection locked frequency dividers has always been challenging. Most of the prior work on DILFDs ([29]-[31]) try to reorder the previous derivations of injection locking in oscillators ([22] and [24]) to fit it to the operation criteria of a frequency divider. While this approach could be a reasonable approximation for a conventional ILFD as depicted in Fig. 3.2a, It is neither accurate nor insightful for the DILFDs (Fig. 3.2b). In our analysis we will show that modeling the input injection transistor as a switch that turns on and off periodically - hence exhibiting a time-variant conductance - provides a much more accurate model of the DILFD operation and results in clear-cut optimization criteria that boosts the performance and devises a straight-forward design procedure.

We start our analysis with the equivalent half circuit model of the DILFD (Fig. 3.2b) as depicted in Fig. 3.2c where the injection transistor is modeled as a switch with an on resistance $R_{sw}/2$ in the

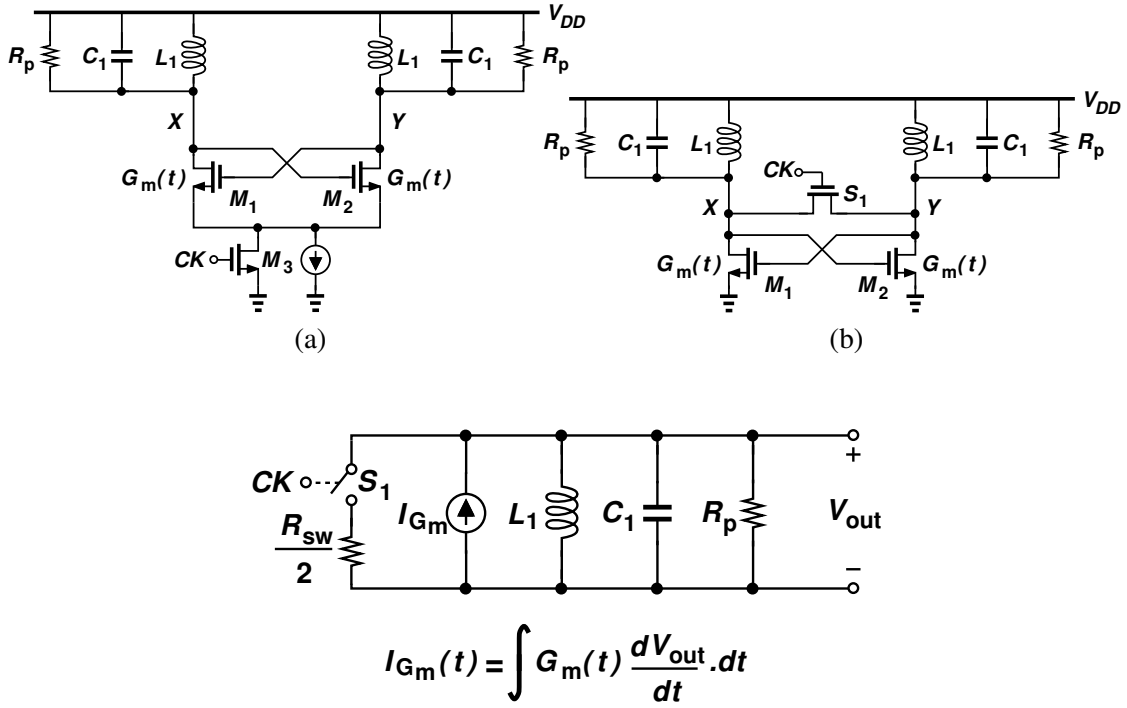


Figure 3.2. (a) Conventional injection-locked frequency divider, (b) direct injection-locked frequency divider and (c) its half-circuit equivalent model.

half circuit. The switch in Fig 3.2b turns on and off with a clock, hence its conductance changes with time as shown in Fig. 3.3a. Please note that here $G_0 = 1/R_{sw}$ is the effective conductance of the switch in the on-state. In other words, the clock in fact is a sine wave, rather than a square wave, hence the G_0 is equal to $(2/\pi)G_{max}$ in the case of a switch driven by a moderate level sine wave (Fig. 3.3b). In the case of a large input, the square wave approximation is more realistic, therefore we take the square-wave assumption for the switch conductance which is more general and could be adjusted to a sine wave conductance by multiplying a factor of $2/\pi$. Also please note that in the half-circuit model, half of the switch resistance is present, so its conductance would be twice as large as that of the input switch as illustrated in Fig 3.3c. We can then represent this conductance as:

$$G_{sw/2}(t) = G_0[1 + \frac{4}{\pi}\sum_{n=1}^{\infty} sin(2n\omega t)] \tag{3.16}$$

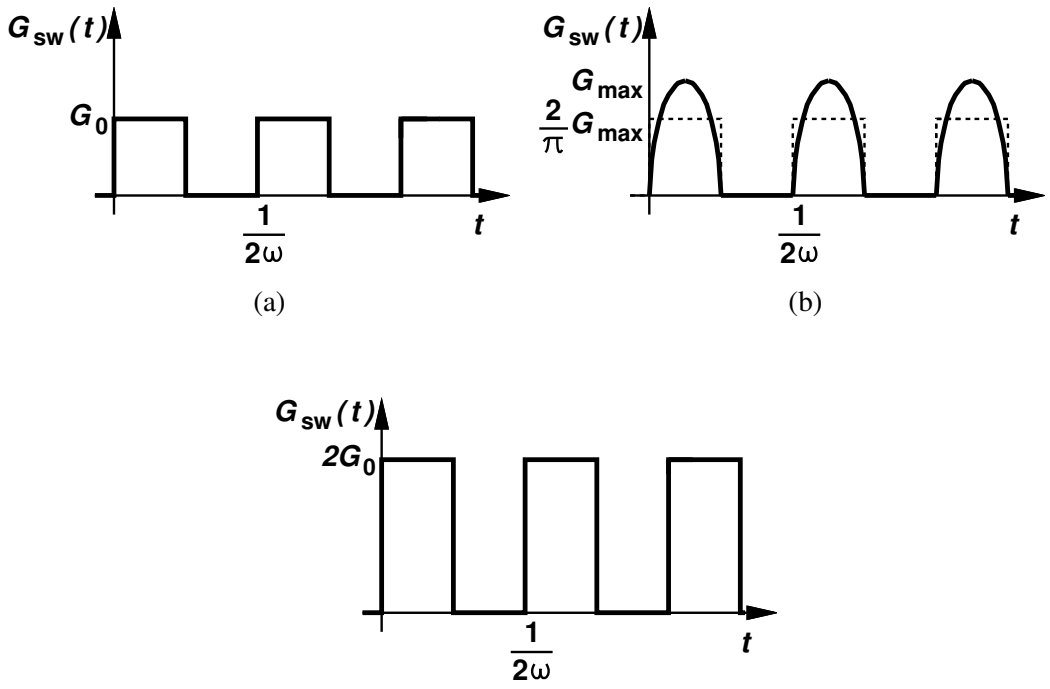


Figure 3.3. (a) Equivalent square wave switch response, (b) equivalent sine wave switch response and (c) half-circuit equivalent switch response.

Now we take a similar approach to that in the oscillator injection analysis. The tank current and cross-coupled pair current are the same as the oscillator analysis. Now, we need to calculate the injection current. We, therefore multiply V_{out} by $G_{sw/2}$ and only take the first harmonic component. Also we add a negative sign to the final product to comply with the KCL in (3.3):

$$I_{inject} = -G_0[1 - \frac{2}{\pi}sin(\phi)]V_0\, cos(\omega t + \phi) - G_0\frac{2}{\pi}V_0\, sin(\omega t + \phi) \tag{3.17}$$

Now using the KCL equation in (3.3) and decomposing the resultant equation into two equations due to the orthogonality of $sin(\omega t+\phi)$ and $cos(\omega t+\phi)$ results in the following key equations:

$$\frac{1}{R_p} = G_{m_0} - G_{m_2} - G_0[1 - \frac{2}{\pi}\, sin(2\phi)] \tag{3.18}$$

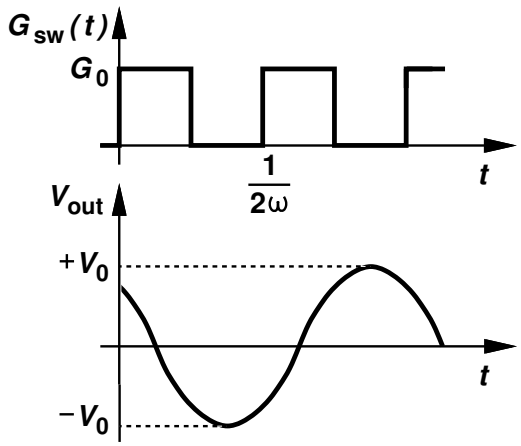
$$2\Delta\omega C_1 = \frac{2}{\pi}G_0\, cos(2\phi) \tag{3.19}$$

Where $(\omega + \omega_0)/\omega$ is approximated by 2 on the left side of (3.19). We want to discuss the implications of the above equations governing the DILFD operation and compare it with those of the oscillator. Firstly, we discuss the operation in the middle of the lock range, i.e. $\Delta\omega = 0$. Equations (3.18) and (3.19) suggest that $\phi = 45^\circ$ which is in contrast with that of the oscillator where $\phi = 0^\circ$. In other words, the zero crossings of the output waveform must be surrounded by the input edges (Fig.3.4). Secondly, at the edge of lock, oscillator model with weak injection suggests that the phase difference is $\sim \pm 90^\circ$ while the divider model does not suggest so. In fact, at the edge of lock, the value of ϕ depends very much on the value of G_0 because the values chosen for G_0 and ϕ must satisfy both (3.18) and (3.19). Finally, (3.19) devises that the larger the parasitic capacitance, the smaller the lock range. This means that as we go to more advanced CMOS technologies with shorter channel length, the lock range would increase. But this result also shows a limitation in the lock range. As the transistors size shrinks in newer technologies, inductor and routing parasitic capacitance which does not scale becomes more dominant and limits the benefit of using newer technology nodes, Hence, the need for more accurate models for maximum optimization and new techniques to break the trade-offs. In this section we will show how our proposed model gives an optimization criteria for the DILFDs and in the next section we propose a new technique to extend the lock range above the limit defined by (3.18) and (3.19). Our objective is to find the optimum value of G_0 at which the lock range is maximum. To this end we eliminate ϕ from (3.18) and (3.19) which results in the following equation:

$$\Delta\omega = \pm\frac{1}{\pi C_1} G_0 \sqrt{1 - \frac{\pi^2}{4}\left[\frac{G_{m_0} - G_{m_2} - \frac{1}{R_p}}{G_0} - 1\right]^2} \tag{3.20}$$

We also reasonably assume that at the edge of lock, the output amplitude is small enough to approximate the effective transconductance of the cross-coupled pair, i.e. $G_{m_0} - G_{m_2}$ with the small signal transconductance at the equilibrium ($V_X = V_Y$ in Fig. 3.2b) , i.e. g_m. Hence, taking the derivative of (3.20) with respect to G_0 results in the following optimum value for G_0 and maximum lock range:

$$G_{0,opt} = \frac{\pi^2}{\pi^2 - 4}\left(g_m - \frac{1}{R_p}\right) \tag{3.21}$$



(a)

Figure 3.4. Input and output waveforms at the center of lock range ($\omega = \omega_0$).

$$\Delta\omega_{max} = \frac{\omega_0}{\sqrt{\pi^2 - 4}}(\frac{g_m R_p - 1}{Q}) \tag{3.22}$$

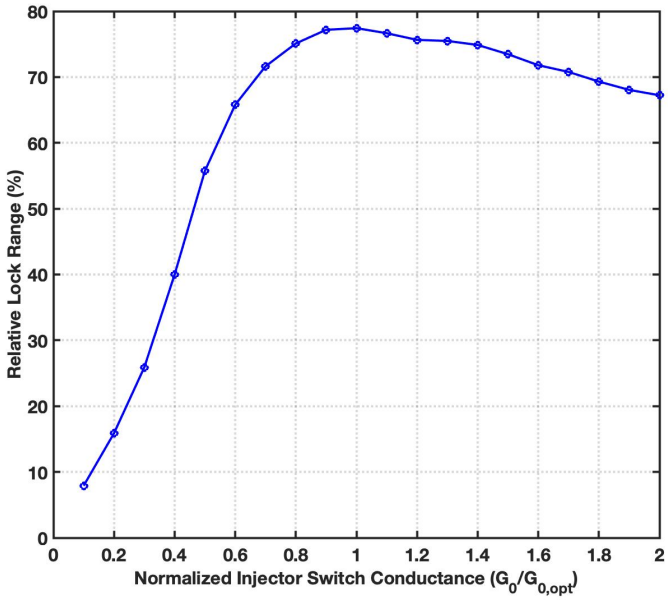
Where $Q = R_p C_1 \omega_0$. We wish to remark several important points. To the authors' knowledge, this is the first analysis that is capable of prescribing an optimum condition for the injector transistor which is obtained due to the novel time-variant modeling of the injector as a switch rather than inaccurate approximation of the injector as a current or voltage source.

Fig. 3.5 shows the simulated relative lock range ($(\omega_{max} - \omega_{min})/\omega_0$, where ω_{max} and ω_{min} are the maximum and minimum frequencies at which the divider locks) versus $G_0/G_{0,opt}$ which confirms the analysis results. Secondly, We should also mention that as we increase the injector switch size, we are increasing C_1 in (3.20) which decreases the lock range. But the output capacitance is still dominated by the inductor and routing parasitics and the cross-coupled pair parasitics and as simulation results suggest, the effect of G_0 optimization dominates the capacitance increase and the optimum point does not change. Finally we simplify (3.22) by assuming $g_m R_p >> 1$:

$$\Delta\omega_{max} = \frac{\omega_0}{\sqrt{\pi^2 - 4}}(\frac{g_m R_p}{Q}) \tag{3.23}$$

Same assumption in a Miller divider leads to the following lock range ([32]):

$$\Delta\omega_{max} = \frac{\omega_0}{\pi}(\frac{g_m R_p}{Q}) \tag{3.24}$$



(a)

Figure 3.5. Relative lock range vs. Normalized injector switch conductance ($G_0/G_{0,opt}$).

Comparing (3.23) with (3.24) shows that DILFDs have fundamental advantage over Miller dividers. In fact, the ratio of their lock range is $\pi/\sqrt{\pi^2-4} \approx 1.3$, which implies that the lock range of the DILFD is 30% higher than the Miller divider. Considering the more complicated circuit of the Miller divider which entails more parasitic capacitance in the signal loop would give the DILFD side even more advantage. An application of our analysis method to the Miller dividers is presented in appendix II.

3.4 Quadrature Coupling

In this section we discuss how adding a quadrature injection to the DILFD will change its lock range. Assume a current with quadrature phase compared to the output voltage of the DILFD is injected to its output as depicted in Fig. 3.6a where $I_Q = I_{inj}sin(\omega t + \phi)$. If we rewrite the KCL that resulted (3.18) and (3.19), we see that only the second equation changes. In fact the resultant

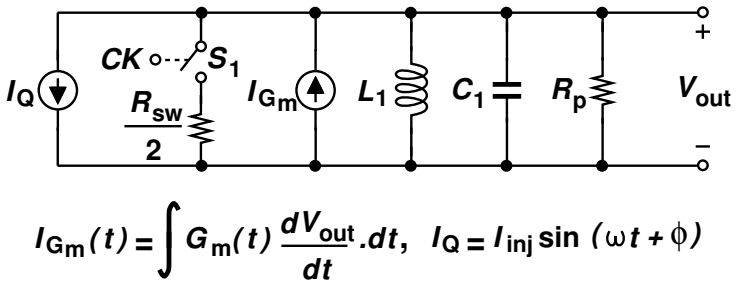
key equations are as follows:

$$\frac{1}{R_p} = G_{m_0} - G_{m_2} - G_0[1 - \frac{2}{\pi}\, sin(2\phi)] \tag{3.25}$$

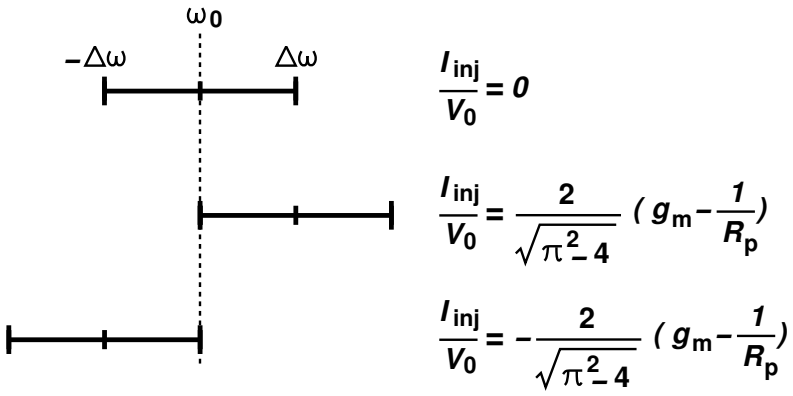
$$2\Delta\omega C_1 = \frac{2}{\pi} G_0\, cos(2\phi) + \frac{I_{inj}}{V_0} \tag{3.26}$$

Notably, (3.25) prescribes the bounds for ϕ whereas (3.26) suggests that $\Delta\omega$ will be shifted up or down by the term I_{inj}/V_0. In fact, we can shift the $\Delta\omega$ completely above the resonance frequency, ω_0, by selecting:

$$(\frac{I_{inj}}{V_0})_{opt} = \frac{2}{\sqrt{\pi^2 - 4}}(g_m - \frac{1}{R_p}) \tag{3.27}$$



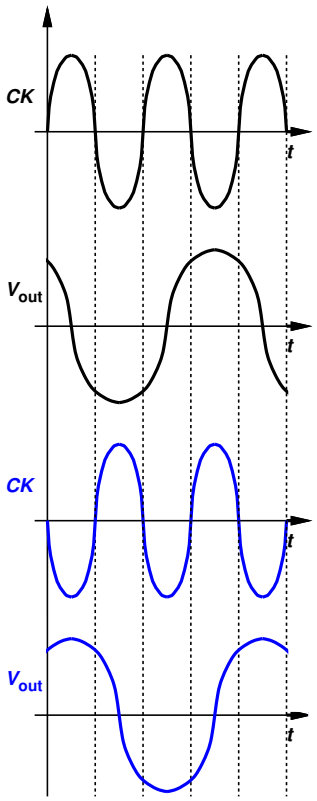
(a)



(b)

Figure 3.6. (a) Quadrature current injection and (b) change of lock range with coupling factor.

Similarly, we can fully shift $\Delta\omega$ below ω_0 if we simply change the sign of I_{inj} (Fig. 3.6b). The foregoing thoughts suggest the need for either $I_{inj}sin(\omega t + \phi)$ or $-I_{inj}sin(\omega t + \phi)$ depending on



(a)

Figure 3.7. Input and output waveforms for two inputs with 180° phase difference

whether the circuit must operate at very high frequencies or very low frequencies. Surprisingly, if we drive two identical frequency dividers with two input clocks that are 180° out of phase, the divider outputs will be quadrature. As shown in Fig. 3.7, a 180° phase shift in the input clock will shift every change in the waveforms by $T_{CLK,in}/2$ which is $T_{CLK,out}/4$ or in other words as 90° phase shift in the output. Of course, It is not possible to decide which of the two identical and independent differential dividers would be 90° ahead and which one would be 90° behind. But when we couple the two dividers there would be only one feasible solution at each frequency. In other words, coupling two identical dividers, driven by differential input clocks as shown in Fig. 3.8a, not only provides the required quadrature current, but also will force the dividers to a specific phase order depending on the frequency of operation. For example in Fig. 3.8a, if we choose the value of coupling transconductance stage, g_{mC}, as prescribed by (3.27), i.e.

$g_{mC,opt} = (2/\sqrt{\pi^2 - 4})(g_m - 1/R_p)$, we will have the maximum lock range as shown in Fig. 3.8b. For $\omega > \omega_0$, $V_{out,Q}$ is 90° behind $V_{out,I}$ while for $\omega < \omega_0$ it is 90° ahead.

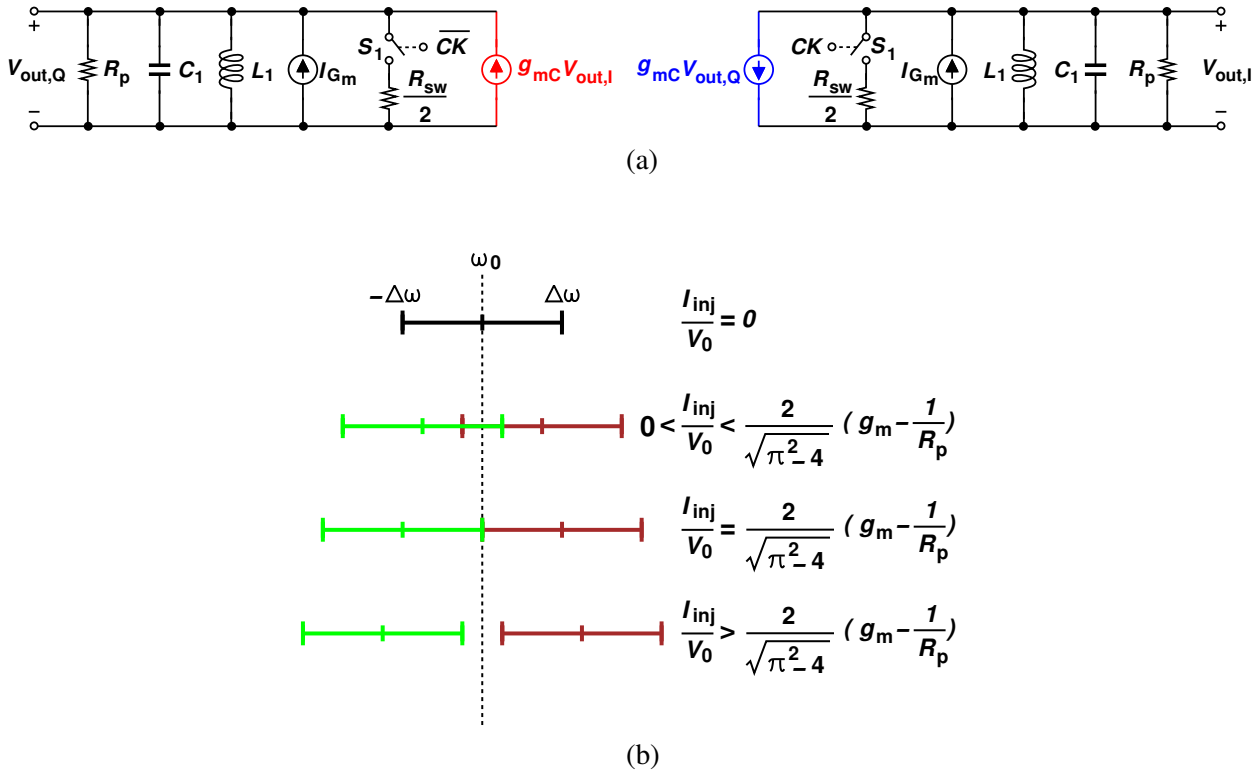
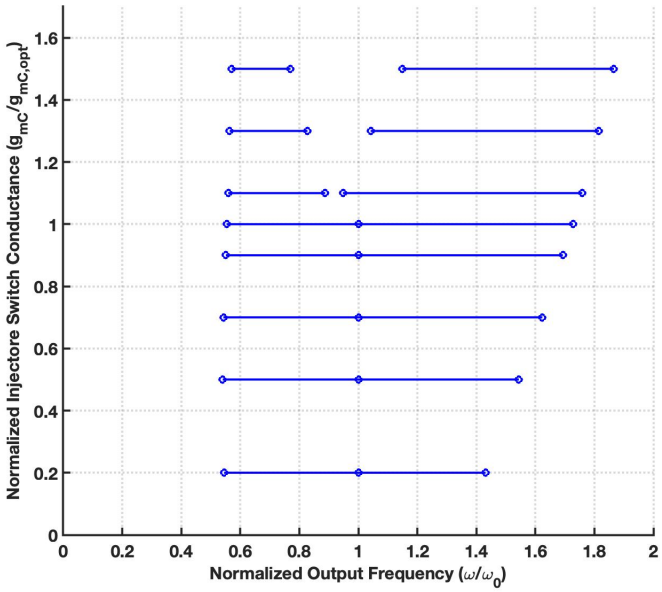


Figure 3.8. (a) Quadrature coupling of two dividers and (b) change of lock range with coupling factor.

Fig. 3.9 plots the relative lock range for different values of relative coupling, $g_{mC,opt}/g_m$, which complies with the theoretical derivation in (3.27). Here we wish to mention three points. 1) As can be examined in Fig 3.9, the lock range extends more on the frequencies above ω_0 than the frequencies below it. This is due to the $(\omega + \omega_0)/\omega$ factor that we approximated with 2 in (3.19). In fact for $\omega > \omega_0$, the $(\omega + \omega_0)/\omega$ factor is smaller compared to that for $\omega < \omega_0$ which increases the magnitude of $\Delta\omega$ for $\Delta\omega > 0$ as compared to $\Delta\omega < 0$. 2) It is good to mention that as can be examined in Fig 3.9 the lower edge of the lock range does not go below $\sim 0.6\omega_0$. This is because in our analysis we have assumed a pure sine wave at the output. As we go to smaller frequencies, the third harmonic of the output current begins to see larger gain provided by the tank impedance. In

fact at $\omega = 0.58\omega_0$, the tank impedance at the third harmonic is equal to that of the first harmonic. If the third harmonic does not get attenuated sufficiently it will affect the zero crossings of the output and prevent proper frequency division operation. 3) As we make the coupling stages stronger, we are increasing the output capacitance which will decrease the lock range, but as Fig.3.9 suggests, the lock range increase due to the lock range shift on both sides of ω_0, strongly outweighs the lock range reduction due to capacitance increase and increases the overall lock range. Finally, We note the similarity between this topology and that in [33] but remark the novelty expressed by (3.27), which allows to substantially increase the lock range.



(a)

Figure 3.9. Simulated lock range for different normalized coupling factor values.

3.5 Circuit Implementation

Two prototypes have been implemented. First one is a single DILFD with optimized switch width to show the efficacy of the optimization provided by our analysis. The circuit schematic is shown

in Fig. 3.10a. We have utilized both NMOS and PMOS transistors to reuse the current and double the g_m, hence increasing the lock range. We must note that If we use both NFET and PFET, the parasitic capacitance at the output, C_1, also increases which according to (3.19) will decrease the lock range. However, while the g_m is doubled, C_1 is not doubled because it does not consist only of the cross-coupled parasitic capacitance. The routing and inductor capacitance and the injector switch capacitance are also contributing to C_1. Hence, using both NMOS and PMOS transistors will help with the lock range.

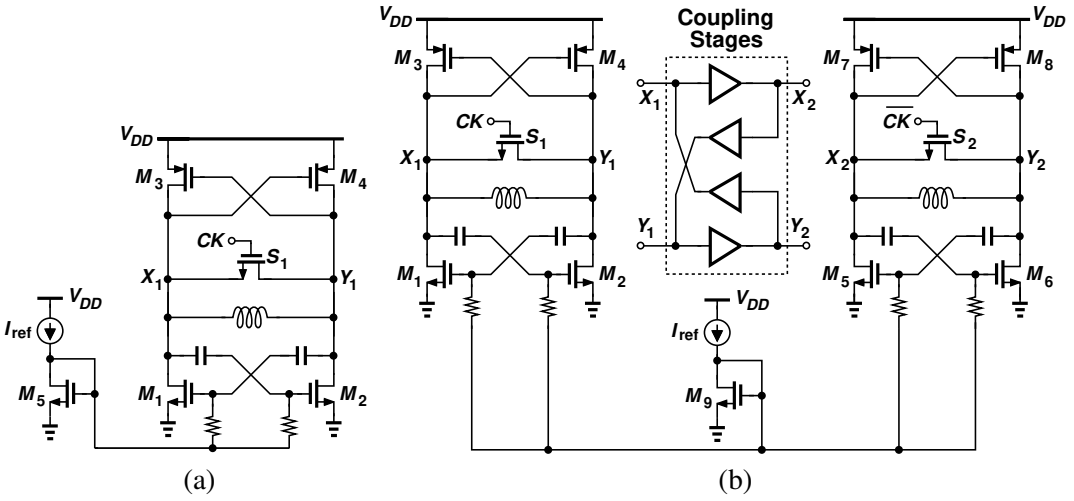
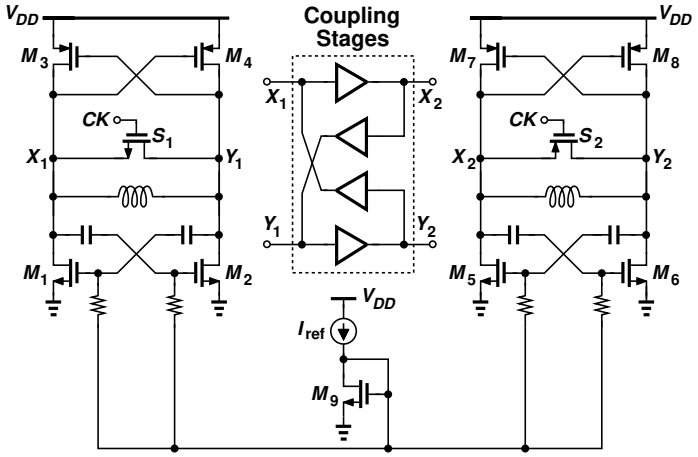


Figure 3.10. Circuit implementation of (a) the single DILFD and (b) the coupled DILFD.

For the quadrature coupled divider we duplicate the single divider in Fig. 3.10a and use inverter-based coupling stages with a relative strength of 0.6 compared to the main cross-coupled pair (Fig. 3.10b). The PFET of the inverter is connected to the output, while the NFET is connected to the gate of the corresponding NFET of the main cross-coupled pair to have proper biasing. This implementation is the best for a divider driven by an on-chip oscillator as it is fully symmetric with respect to the differential input clocks. However, in an standalone measurement with external clock, it is not feasible to bring a differential clock on the chip, therefore, we use a PFET as an injector switch in one of the dividers that works with the same clock signal as the NFET injector switch in the other divider but turns on and off with 180° phase shift. The final implementation is illustrated in Fig. 3.11. The size of the NMOS and PMOS injector switches are chosen to be

the same to make the two tanks have identical resonance frequencies. The biasing of the NMOS and PMOS injectors are chosen so as to provide same lock range in each individual divider before coupling. Finally, the divider outputs are connected to four open-drain PFETs, one of which is connected to the output pad to sense the output.



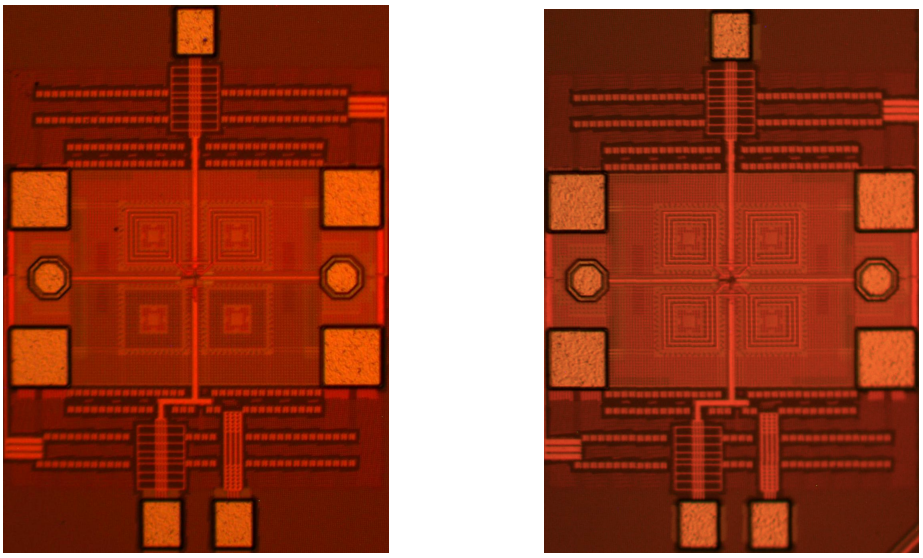
(a)

Figure 3.11. Modified coupled DILFD Circuit.

3.6 Experimental Results

The two prototypes have been fabricated in 28-nm CMOS technology. the die photographs are shown in Fig. 3.12. The inductors used in each divider are implemented as two separate spiral inductors connected in series as depicted in Fig. 3.13a in contrast two a single compact inductor (Fig. 3.13b) to reduce the mutual capacitance of the inductor traces that appear between the differential outputs of the divider an reduce the lock range. We have used minimum channel length in all transistors and a width of 3.2 μm for the main cross-coupled pair and 2 μm for the coupling transistors. The injector FETs have a width of 11.2 μm and the open drain buffers' PFETs have a width of $4\mu m$.

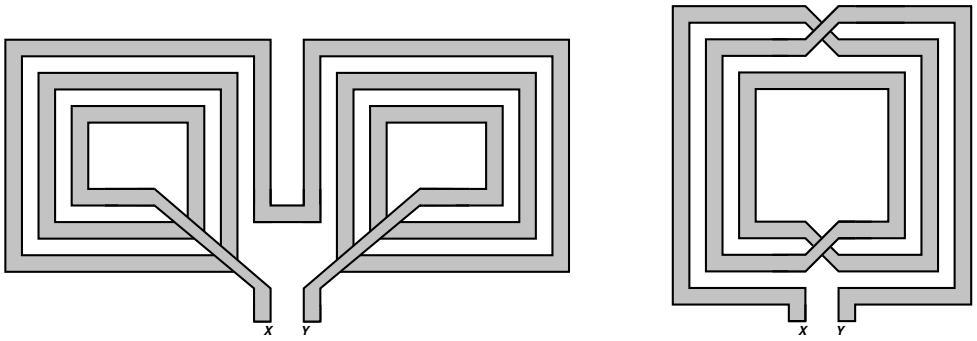
The prototypes have been characterized with both 1 V and 1.1 V supplies. They show slightly less lock range with 1 V supply compared to the 1.1 V case. With 1V supply, the single divider



(a) (b)

Figure 3.12. Die photograph of (a) the single DILFD and (b) the coupled DILFD.

prototype exhibits a lock range of 27-61.5 GHz while consuming 1.42 mW. With 1.1 V supply its lock range increases to 26-63 GHz while consuming 1.88 mW. The quadrature coupled divider exhibits a lock range of 25.2 GHz-72.2 GHz while consuming 3.6 mW with 1 V supply. With 1.1 V supply the lock range extends to 24-73 GHz while consuming 4.76 mW. The input sensitivity of the two prototypes are plotted in Fig. 3.14 which summarizes the performance for both 1 V and 1.1 V supplies.



(a) (b)

Figure 3.13. Inductor layout as (a) two separate spirals and (b) one compact inductor.

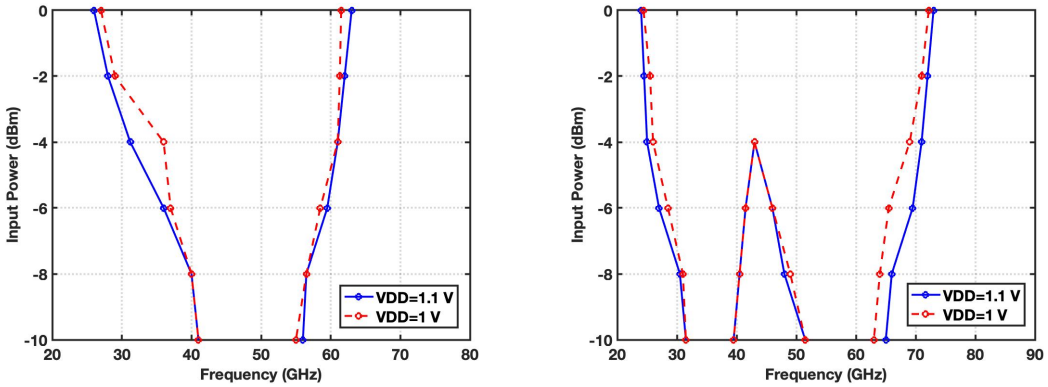


Figure 3.14. Input sensitivity of (a) the single DILFD and (b) the coupled DILFD.

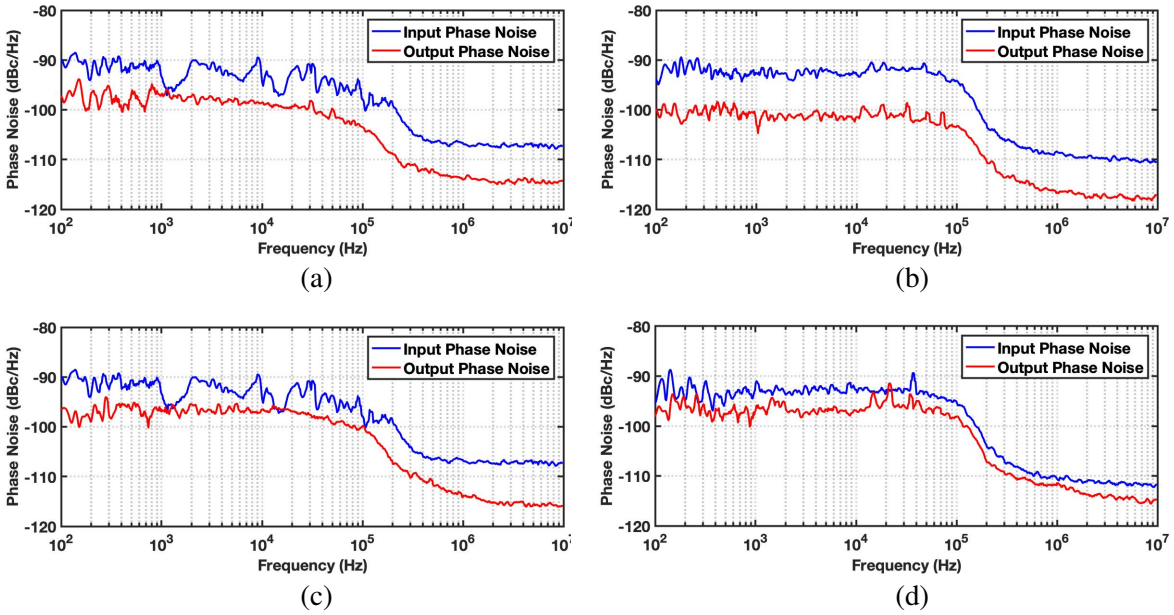
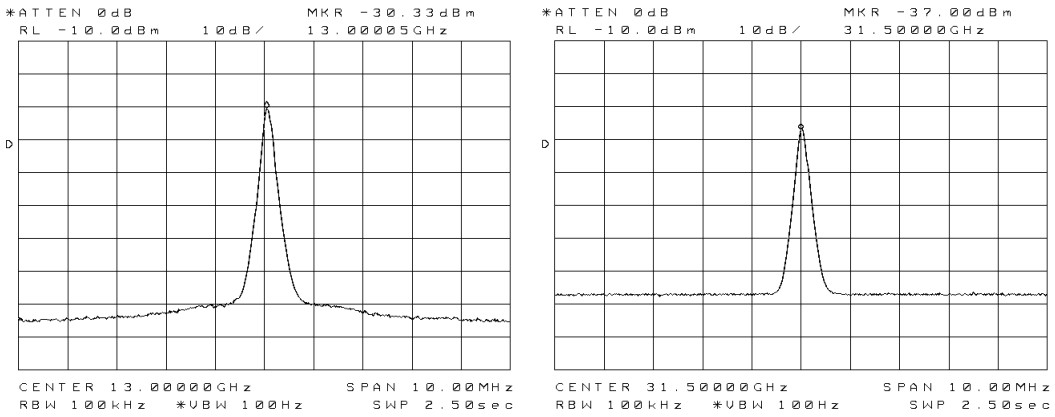


Figure 3.15. Phase noise plots of the input and output for (a) the single DILFD at 45 GHz input, (b) the single DILFD at 63 GHz input, (c) the coupled DILFD at 45 GHz input and (d) the coupled DILFD at 73 GHz input.

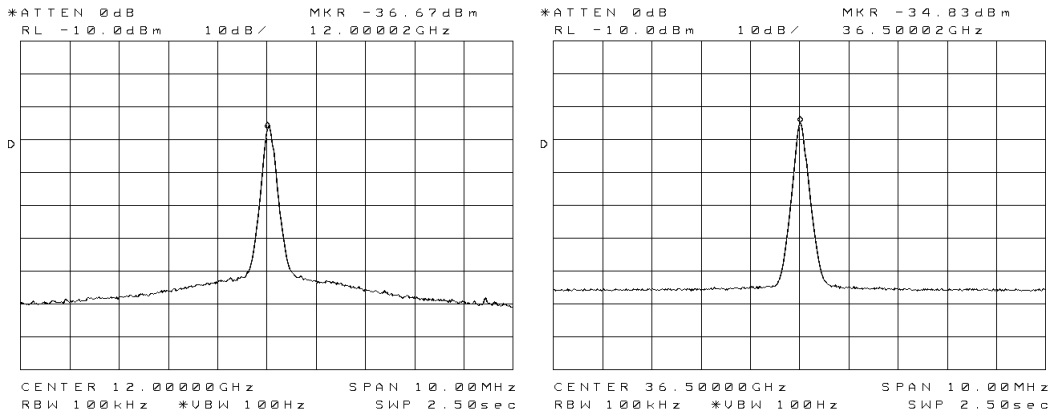
Plots in Fig. 3.15 illustrate the phase noise of the output and input for both prototypes at the middle and upper edge of the lock range when driven by 1.1 V supply. They clearly show the

6 dB noise reduction after frequency division and the phase noise is limited by the signal source performance. The divider intrinsic phase noise as indicated by simulations is -138 dBc/Hz at 10 MHz offset.



(a) (b)

Figure 3.16. Output spectrum for the single DILFD (a) at 26 GHz input and (d) at 63 GHz input.



(a) (b)

Figure 3.17. Output spectrum for the coupled DILFD (a) at 24 GHz input and (d) at 73 GHz input.

Finally, the output spectrum for the upper edge and lower edge of the lock range, measured with 1.1 V supply, are plotted in Fig. 3.16 and Fig. 3.17 for the single DILFD and coupled DILFD respectively.

The performance of both single divider and quadrature coupled divider are summarized in Table I and compared to the state of the art. The single divider shows a relative lock range larger than any previously reported divider in the frequency range of interest, i.e. 83% while consuming only 1.88 mW and having the best ever reported FOM of 19.6. The quadrature coupled divider exhibits an unprecedented 101% relative lock range while consuming 4.76 mW which results in an FOM of 10.3, larger than any divider reported in the prior art with similar supply voltage.

3.7 Conclusion

A universal framework for injection locking based on linear time-variant analysis is introduced. Its application to the DILFD results in new insights on the frequency divider operation and optimization criteria. The idea of quadrature coupling of the dividers is studied. The introduced linear time-variant framework which successfully modeled the quadrature injection, explained its effect on frequency division and prescribed an optimization criteria for the quadrature coupling to maximize the lock range. Finally, prototypes of a single divider and a quadrature coupled divider optimized based on our analysis have been fabricated and characterized which show unprecedented performance.

Table 3.1. Performance summary and comparison

	[30][1]	[31][1]	[34][1]	This Work[1]	
				Single DILFD	Coupled DILFD
Frequency [GHz]	12-32	27.9-53.5	25-53.6	26-63	24-73
Lock Range [%] [2]	90.9	62.9	72.7	83.1	101
P_{DC} [mW]	2.4	5.8	6.7	1.88	4.76
FOM [GHz/mW] [3]	8.33	4.41	4.26	19.68	10.29
Active Area [mm^2]	0.45	0.18	N/A	0.019	0.037
CMOS Technology	90 nm	65 nm	65 nm	28 nm	28 nm

[1]All measurements with a maximum input power = 0 dBm
[2]Lock Range=$2(f_{max}-f_{min})/(f_{max}+f_{min})$ [3]FOM=$(f_{max}-f_{min})/P_{DC}$

Appendix I: Analysis of The Injection Locking Based on Conservation of Energy

In this appendix we discuss how we can use the law of conservation of energy to obtain the first key equation governing the injection locking. Consider the linear time-variant model of the injection to an oscillator as depicted in Fig. 3.1b. According to the law of conservation of energy, the power injected to the tank by the cross-coupled pair and the injector must be equal to the power consumed by the tank, i.e.:

$$P_{Tank} = P_{inj} + P_{G_m} \tag{3.28}$$

The power consumed by the tank is:

$$P_{Tank} = \frac{V_0^2}{2R_p} \tag{3.29}$$

The power provided by the cross-coupled pair can be calculated by integrating the product of the output voltage and the cross-coupled pair current (form equation (3.7)) as:

$$P_{Gm} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} (G_{m_0} - G_{m_2})V_0^2 cos^2(\omega t + \phi).dt = \frac{V_0^2(G_{m_0} - G_{m_2})}{2} \tag{3.30}$$

Similarly, the power injected to the tank due to I_{inject} could be written as:

$$P_{inj} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} I_{inj}V_0\, cos(\omega t + \phi)cos(\omega t).dt = \frac{V_0 I_{inj} cos(\phi)}{2} \tag{3.31}$$

Finally, substituting the corresponding power components in (3.28) will result in (3.32):

$$\frac{1}{R_p} = G_{m_0} - G_{m_2} + \frac{I_{inj}}{V_0}\, cos(\phi) \tag{3.32}$$

Which is the same as the equation obtained in (3.8).

Appendix II: Analysis of Miller Frequency Dividers Based on The Proposed Framework

In this appendix we study a Miller frequency divider using our proposed analysis method. Consider the miller frequency divider of Fig. 3.18a. Its equivalent half-circuit model is depicted in Fig.

3.18b. The input clocks connected to the top transistors steer the current produced in the bottom transistor pair in turn which makes the equivalent operation equivalent of multiplication by a square wave toggling between +1 and -1 at a frequency of 2ω. We can represent this waveform as:

$$S(t) = \frac{4}{\pi} \sum_{n}^{\infty} \frac{sin(2n\omega t)}{n} \tag{3.33}$$

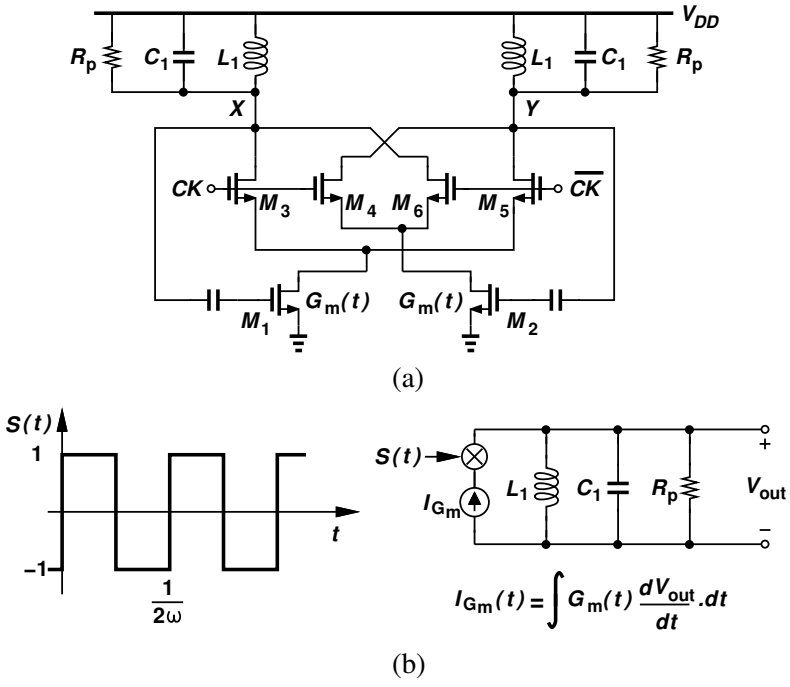


Figure 3.18. (a) A Miller frequency divider and (b) its equivalent half-circuit model.

The current produced in the bottom transistor pair gets multiplied by $S(t)$ and reaches the output. We are interested only in the first harmonic of the resultant current. Because $S(t)$ contains all even harmonics and current produced in the bottom transistors contains all odd harmonics of ω, there are infinite number of possible combinations between higher harmonics that can result in a first harmonic output current. However, as we pick higher harmonics, their coefficients both in $S(t)$ and in the current coming out of the bottom transistors will be smaller and negligible compared to the terms coming from the lower harmonics. Therefore we can reasonably only consider the first harmonic of the output current term that is a product of the first component of

$S(t)$, i.e. $4/\pi sin(2\omega t)$ and the first harmonic component of the bottom transistor pair current which according to (3.7) is:

$$I_{G_m} = (G_{m_0} - G_{m_2})V_0\, cos(\omega t + \phi) \tag{3.34}$$

Hence, we can write the output current coming from the bottom transistors as:

$$I_{G_m,out} = I_{G_m}\frac{4}{\pi}sin(2\omega t) \tag{3.35}$$

Considering only the first harmonic component of (3.35) will result in the following expression:

$$I_{G_m,out} = \frac{2}{\pi}V_0(G_{m_0} - G_{m_2})[sin(\omega t + \phi)cos(\phi) - cos(\omega t + \phi)sin(\phi)] \tag{3.36}$$

The tank current is similar to what was obtained in (3.4):

$$I_{Tank} = \frac{V_0}{R_p}\, cos(\omega t + \phi) + \frac{V_0}{L_1\omega}\, sin(\omega t + \phi) - V_0 C_1\omega\, sin(\omega t) \tag{3.37}$$

KCL at the output node requires that $I_{Tank} = I_{G_m,out}$ which results in the following two key equations:

$$\frac{1}{R_p} = -\frac{2}{\pi}(G_{m_0} - G_{m_2})sin(\phi) \tag{3.38}$$

$$2\Delta\omega C_1 = -\frac{2}{\pi}(G_{m_0} - G_{m_2})sin(\phi) \tag{3.39}$$

On the left side of (3.38) we have approximated $(\omega+\omega_0)/\omega$ by 2. Eliminating ϕ from the above two equations will result in the following:

$$\Delta\omega = \pm\frac{\omega_0}{2Q}\sqrt{[\frac{2}{\pi}(G_{m_0} - G_{m_2})R_p]^2 - 1} \tag{3.40}$$

Where $Q = R_p C_1\omega_0$. The value that changes in (3.40) as $\Delta\omega$ changes is $G_{m_0} - G_{m_2}$, which is the effective transconductance of the bottom transistor pair. As we come closer to the edge of lock, the output voltage amplitude shrinks and the effective transconductance could be approximated by the small signal transconductance at the equilibrium, i.e. g_m. Also right side of (3.40) is a monotonically increasing function of $G_{m_0} - G_{m_2}$ which reaches its maximum when $G_{m_0} - G_{m_2}$

reaches its maximum, i.e. g_m at the edge of lock. Therefore, one sided lock range could be found by substituting g_m for $G_{m_0} - G_{m_2}$ in (3.40) which results in (3.41). This result complies with the lock range obtained in [32].

$$\Delta\omega_{max} = \frac{\omega_0}{2Q}\sqrt{(\frac{2}{\pi}g_m R_p)^2 - 1} \tag{3.41}$$

CHAPTER 4

Conclusion

This dissertation presents new techniques for future RF and millimeter wave radios, namely, a universal RF receiver and a new framework to study injection locking that largely improves the lock range of millimeter wave direct injection locked frequency dividers (DILFDs).

Introducing multiple new techniques in the receiver design, specifically, multi-loop feedback receiver architecture, blocker rejection enhancement, power efficient wideband op amp and harmonic trap, the proposed receiver exhibits robust performance across the 400 MHz-6 GHz frequency range. Realized in 28-nm CMOS technology, the prototype provides sufficient tolerance to large out-of-bad blockers and performs channel selection filtering for channel bandwidths from 200 kHz to 160MHz. It exhibits a noise figure of 2.1 in the low noise mode and 4.2 dB in the harmonic rejection mode with greater than 60.8 dB harmonic rejection up to 2 GHz with no need for calibration while drawing 49 mW. The proposed receiver EVM performance is tested with LTE and 802.11 ax signals to guarantee the performance for different cellular and WiFi applications.

A new analysis frame work is introduced for the study of injection locking. Based on a linear time-variant model, this framework provides new insights into the injection locking phenomenon in the oscillators and frequency dividers. Application of this method to DILFDs provides new optimization conditions that largely improves the lock range. The analysis frame work also suggests that quadrature coupling will increase the lock range even further. Two prototypes are fabricated in 28-nm CMOS technology. A single DILFD exhibits a lock range of 26-63 GHz (relative lock range of 83%) while consuming 1.88 mW. A coupled DILFD operates over a lock range of 24-73 GHz (relative lock range of 101%) and consumes 4.76 mW with no need for tuning or adjustments.

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