

UC San Diego

UC San Diego Electronic Theses and Dissertations

Title

High efficiency switching-mode amplifiers for wireless communication systems

Permalink

<https://escholarship.org/uc/item/5fq8g09p>

Author

Hung, Tsai-Pi

Publication Date

2008

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA, SAN DIEGO

High Efficiency Switching-Mode Amplifiers for Wireless Communication Systems

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electrical circuits and systems)

by

Tsai-Pi Hung

Committee in charge:

Peter M. Asbeck, Chair
Prabhakar R. Bandaru
Andrew C. Kummel
Lawrence E. Larson
Paul K. Yu

2008

Copyright ©

Tsai-Pi Hung, 2008

All rights reserved

The dissertation of Tsai-Pi Hung is approved,
and it is acceptable in quality and form for
publication on microfilm:

Chair

University of California, San Diego
2008

***To my wife Chen-Hui,
my sister Tzu-Hsing,
and my parents for their unfailing love and faith***

Table of Contents

Signature Page	iii
Dedication.....	iv
Table of Contents	v
List of Figures.....	ix
List of Tables	xvi
Acknowledgements	xvii
Vita.....	xix
Publications	xx
Abstract	xxii

Chapter 1 INTRODUCTION

1.1 Power Amplifiers in Wireless Communication Systems	1
1.2 High Efficiency Switching Mode Amplifiers.....	6
1.3 Digital RF Transmitters	10
1.4 Scope of the Dissertation	12
1.5 Organization of the Dissertation.....	16
1.6 References	17

Chapter 2 CURRENT-MODE CLASS-D POWER AMPLIFIERS

2.1 Introduction	20
2.2 Basics of Current-Mode Class-D Amplifierrs	22

2.3	Design Considerations for Current-Mode Class-D Amplifiers	24
2.3.1	Higher order odd harmonic effects (η_{po})	25
2.3.2	Effect of non-zero transition time (η_{tt})	27
2.3.3	Non-Zero Knee Voltage of the Transistors (η_{tt}).....	29
2.3.4	Parasitic resistance of the LC resonator (η_{pp}).....	31
2.3.5	Loss of the output matching network (η_{pm}).....	32
2.3.6	Comparison of the simulated and calculated efficiency.....	32
2.3.7	Additional design considerations and limitations of analysis	33
2.4	Experimental CMCD Amplifier Design	36
2.5	Measurement Results.....	39
2.6	Conclusion	42
2.7	Acknowledgements	43
2.8	References	44

Chapter 3 VOLTAGE-MODE CLASS-D POWER AMPLIFIERS

3.1	Introduction	47
3.2	Operation of Voltage Mode Class-D Amplifiers.....	49
3.2.1	Idealized Operation of Voltage mode Class-D Amplifiers	49
3.2.2	Reactive Load.....	51
3.2.3	Duty Ratio	53
3.3	CMOS H-Bridge Class-D Amplifier	55
3.3.1	Shoot-Through Current and Suppression Technique	56
3.3.2	Implementation of CMOS H-Bridge VMCD Amplifier	59

3.3.3	Measurement Results of the CMOS H-bridge VMCD Amplifier	61
3.4	Loss Analysis and Efficiency Estimation for Non-ideal Operation	64
3.5	Summary.....	72
3.6	Acknowledgements	73
3.7	References	73

Chapter 4 CMOS OUTPHASING CLASS-D AMPLIFIER WITH CHIREIX COMBINER

4.1	Introduction	75
4.2	Outphasing Amplifier Systems and Combiners	76
4.2.1	Outphasing system overview.....	76
4.2.2	Conventional outphasing combiner.....	78
4.2.3	Chireix power combiner	82
4.3	CMOS Outphasing Class-D Amplifiers	86
4.3.1	CMOS Voltage mode Class-D Power Amplifier	86
4.3.2	Chireix Combiner Implementation.....	89
4.4	Outphasing Amplifier Measurement Results	90
4.5	Summary.....	94
4.6	Acknowledgements	94
4.7	References	94

Chapter 5 H-BRIDGE CLASS-D POWER AMPLIFIERS FOR DIGITAL PULSE MODULATION TRANSMITTERS

5.1	Introduction	96
-----	--------------------	----

5.2	Band-Pass Delta-Sigma Modulation Signals.....	99
5.2.1	Two-Level Quantization.....	99
5.2.2	Three-Level Quantization.....	103
5.3	Digital Operation of an H-bridge Class-D Amplifier.....	104
5.4	Conclusion.....	115
5.5	Acknowledgements	116
5.6	References	116

Chapter 6 DIGITAL POLAR MODULATED SWITCHING MODE AMPLIFIERS

6.1	Introduction	118
6.2	Digital Polar Modulation System and Signal Generation	120
6.3	Envelope Switching Class-E Amplifier.....	127
6.4	Class-E Amplifier Implementation and Measurement Results	132
6.5	Summary and Discussion	139
6.6	References	141

Chapter 7 CONCLUSIONS AND FUTURE WORK

7.1	Dissertation Summary	142
7.2	Conclusion.....	144
7.3	Future work	148
7.4	References	149

List of Figures

Figure 1.1. Simplified transmitter architecture with a power amplifier at the last stage.	2
Figure 1.2. Example of ACPR spectrum mask [1-2].....	3
Figure 1.3. Envelope power density distribution functions of constant envelope modulated signals (GSM) and non-constant modulated signals (CDMA and Multi-carrier) [1-5].	4
Figure 1.4. Efficiency vs. normalized output power of an ideal class-B power amplifier. The peak efficiency is 78.5%	5
Figure 1.5. Voltage and current waveforms of various switching mode amplifiers	7
Figure 1.6. (a) Schematics of an outphasing system using Class-F amplifiers (b) Comparison of the measured efficiency with ideal class-A and B amplifier as a function of output power) [1-6]	9
Figure 1.7. Block diagram of ET base station amplifier including signal generation and up/down conversion [1-7]	10
Figure 1.8. System diagram of a digital polar modulated PA [1-11]	11
Figure 1.9. Simplified block diagram of an outphasing system with a Chireix combiner	13
Figure 1.10. Simplified block diagram of a digital pulse modulation system and the representative time domain waveforms	14
Figure 1.11. The digital envelope polar modulation pattern (blue) and the envelope (red) of a two-tone signal.	15
Figure 2.1. Simplified schematic and voltage/current waveforms of the voltage mode class-D amplifier.....	22
Figure 2.2. Simplified schematic and voltage/current waveforms of the current mode class-D amplifier.....	23
Figure 2.3. Normalized voltage waveform across the load, showing distortion by the high order harmonic leakage current. With lower Q factor, the voltage waveform has more distortion	26
Figure 2.4. The efficiency factor η_{po} increases with the increasing Q factor. $Q=\omega \cdot R_{load} \cdot C$	27

Figure 2.5. Waveform of the current i_1 , considering a non-zero transition time (τ). ..	28
Figure 2.6. The efficiency factor η_H drops with increasing transition time (τ).	29
Figure 2.7. Simplified model for evaluating the effects of the knee voltage of the transistors.....	30
Figure 2.8. Switch model with parasitic reactance and finite transition time (τ).	33
Figure 2.9. The switch control waveforms for the highest collector efficiency.....	34
Figure 2.10. Simulated current waveform, showing spiking phenomena due to the overlap of voltage waveform and the time-varying conductance.....	35
Figure 2.11. Schematic of the CMCD amplifier	37
Figure 2.12. Simulated collector voltage and current waveform, showing desired characteristics of zero voltage switching	37
Figure 2.13. CMCD amplifier chip geometry (a) CMCD1: with pads for bondwire inductor. (b) CMCD2: with on-chip spiral inductor	38
Figure 2.14. Photograph of the CMCD amplifier prototype. The overall amplifier employed external matching and baluns.....	39
Figure 2.15. Measured efficiency vs. input power for CMCD1, showing collector efficiency of 78.5% at maximum PAE of 68.5%	40
Figure 2.16. Measured efficiency vs. input power for CMCD2, showing collector efficiency of 73.5% at maximum PAE of 64.6%	41
Figure 2.17. Measured collector efficiency, gain vs. frequency of CMCD1, showing the operation bandwidth of 300MHz for collector efficiency greater than 70%.	41
Figure 2.18. Measured Gain and Pout vs. input power	42
Figure 3.1. A voltage mode class-D amplifier consisting of two complementary FETs and a series resonator	49
Figure 3.2. The voltage and current waveforms of the idealized voltage mode class-D amplifier.....	50
Figure 3.3. The voltage and current waveforms of the idealized voltage mode class-D with a reactive load.....	52
Figure 3.4. The voltage and current waveforms of the idealized voltage mode class-D driven by the signals with non-50% duty ratio.....	54

Figure 3.5. The voltage and current waveforms of the voltage mode class-D amplifier (a) with shoot-through current (b) with shoot-through current suppression technique.....	56
Figure 3.6. The voltage mode class-D amplifier driven by (a) the direct approach (b) the modified driver stage for shoot-through current suppression	58
Figure 3.7. The voltage mode class-D amplifier chip.	60
Figure 3.8. Schematic of the prototype H-bridge class-D power amplifier consisting of two class-D PA, two quarter-wave transmission lines and a balun.....	60
Figure 3.9. The prototype H-bridge class-D power amplifier	61
Figure 3.10. The frequency response of the differential mode impedance of the combining network	61
Figure 3.11. Measured DC currents for switch and driver stage as a function of frequency	62
Figure 3.12. Measured drain efficiency as a function of frequency	63
Figure 3.13. Measured PAE and Pout as a function of frequency	63
Figure 3.14. Single VMCD amplifier with modified driver stage	64
Figure 3.15. Class-D amplifier voltage and current waveforms for efficiency estimation.....	66
Figure 3.16. Overlap voltage and current waveforms across the p-channel transistor during the transition	68
Figure 3.17. Comparison of the drain efficiency as a function of duty-ratio	70
Figure 3.18. Comparison of the output power as a function of duty-ratio	70
Figure 3.19. Comparison of the drain efficiency as a function of output power.....	71
Figure 3.20. Power loss ratio for each loss factor as a function of output power	72
Figure 4.1.(a): Simplified block diagram of an outphasing system with a Chireix combiner. The compensation reactances are complex conjugate ($\pm jX$)	77
Figure 4.1.(b): The input complex signal S_{in} can be decomposed into two constant envelope signals S_1 and S_2	78

Figure 4.2. (a)A simplified schematic of an outphasing amplifier system. (b) The input impedance of with different outphasing angle θ	79
Figure 4.3. The combining efficiency at different output power levels. ($R_s=1\Omega$, $Z_0=20\Omega$, $R_L=50\Omega$, $V_1=V_2=1V$ were used in the analysis).....	80
Figure 4.4. A simplified schematic of an outphasing amplifier system including the parallel capacitor C_p which represents the capacitance loss, one of the possible intrinsic losses for voltage mode class-D amplifiers	81
Figure 4.5. The system efficiency at different output power levels. ($R_s=1\Omega$, $Z_0=20\Omega$, $R_L=50\Omega$, $V_1=V_2=1V$ were used in the analysis).....	82
Figure 4.6. (a) A simplified schematic of an outphasing amplifier system with a Chireix combiner including the reactive compensation components. (b) The input impedance for different X while changing the outphasing angle.....	82
Figure 4.7. The combining efficiency of the Chireix combiner with different outphasing angle	84
Figure 4.8. A simplified schematic of an outphasing amplifier system with a Chireix combiner including the reactive compensation components and the output capacitor C_p	85
Figure 4.9. The system efficiency of the Chireix combiner with different outphasing angle.	85
Figure 4.10. Schematic of the voltage-mode Class-D power amplifier with shoot-through current suppression and a compensated inductor	87
Figure 4.11. Simulated efficiency and output power load-pull contours. Max efficiency of 62% and maximum output power of 17.5dBm were obtained at the peaks, respectively	88
Figure 4.12. Simulated efficiency and output power load-pull contours. Max efficiency of 62% and maximum output power of 17.5dBm were obtained at the peaks, respectively	89
Figure 4.13. Efficiency and output power measured with different outphasing angles. Maximum drain efficiency of 62% was achieved, together with a PAE of 42%.....	90
Figure 4.14. Normalized measured output power vs outphasing angle θ . A $\cos^2\theta$ curve is shown for comparison.	91
Figure 4.15. Drain efficiency measured as a function of output power with different reactive compensations	92

Figure 4.16. Measured PA output spectrum with CDMA signals. An ACPR of -45dBc was achieved.....	93
Figure 5.1. Simplified block diagram of possible future digital RF transmitters with bandpass delta-sigma modulators	97
Figure 5.2. Simplified block diagram of possible future digital RF transmitters with bandpass delta-sigma modulators	99
Figure 5.3. Spectrum of the delta-sigma modulated signals, showing that the quantization noise is shaped and removed out of band	100
Figure 5.4. (a): Expanded spectrum of Figure 5.3 from 700 MHz to 900MHz	100
Figure 5.4. (b): Expanded spectrum of Figure 5.3 from 797 MHz to 803MHz	101
Figure 5.5. In-band power ratio as a function of the feedback coefficient ratio B/A .	102
Figure 5.6. Simulated ACPR and EVM for CDMA signals after passing through delta-sigma modulator with a two level quantizer as a function of inband power ratio	102
Figure 5.7. Block diagram of a three level bandpass delta-sigma modulators that uses a three level quantizer.	103
Figure 5.8. Simulated ACPR and EVM for CDMA signals after passing through delta-sigma modulator with a three level quantizer as a function of inband power ratio	104
Figure 5.9. (a) Schematic of a Class-D power amplifier. (b) Schematic of an H-bridge Class-D power amplifier.....	105
Figure 5.10. Schematic of the prototype H-bridge class-D power amplifier consisting of two class-D PA, two quarter-wave transmission lines and a balun.....	105
Figure 5.11. Measured input and output spectrum for two level DSM signals with a inband power ratio of 30% and 24%, respectively	107
Figure 5.12. Measured Amplifier output spectrum with DSM signals	107
Figure 5.13. Measured ACPR and drain efficiency of the CMOS H-bridge amplifier for two level DSM signals with different inband power ratio	108
Figure 5.14. Measured drain efficiency as function of output power for two and three level DSM signals.....	110

Figure 5.15. Measured amplifier input and output ACPR as a function of output power for three level DSM signals	110
Figure 5.16. Measured power consumption at switch and driver stage and output power as function of output power	111
Figure 5.17. Measured amplifier rain efficiency as a function of output power	112
Figure 5.18. Estimated drain efficiency as a function of output power with reduced capacitance and transition time. (Based on $f=800\text{MHz}$, $R_{\text{on}}=0.7\text{ohm}$, $R=7\text{ohm}$, $V_{\text{dd}}=2\text{V}$ and no output circuit loss).....	114
Figure 6.1. Simplified block diagram of the digital polar modulation system proposed in [6-1].....	119
Figure 6.2. Simplified block diagram of the proposed digital polar modulation system	120
Figure 6.3. The envelope and phase signals of the two-tone signals with 2.5MHz spacing	122
Figure 6.4. The sampled envelope (blue circle) and the average sampled envelope (red star).....	122
Figure 6.5. The number of pulses for each block (NB=40).....	123
Figure 6.6. The digital envelope polar modulation pattern (blue) and the envelope (red) of a two-tone signal.....	123
Figure 6.7. The simulated spectrum of the digital polar modulated signals for NB=40.....	124
Figure 6.8. The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40	124
Figure 6.9. The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40	126
Figure 6.10(a). The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=20	126
Figure 6.10(b). The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40	127
Figure 6.11. The simplified schematics of the (a) conventional class-E amplifier (b) class-E amplifier with finite RF choke inductance proposed in [6-2]	128

Figure 6.12. The simplified schematics of the class-E amplifier with a diode on the supply path.....	129
Figure 6.13. The time domain waveforms of the envelope switching class-E PA (a) Two-tone envelope signals (b) the digital driving signals (c) the voltage waveform at the drain (d)the current waveforms at the drain	130
Figure 6.14. The drain voltage and current waveforms of the device.....	131
Figure 6.15. The simulated output spectrum of the class-E amplifier.....	131
Figure 6.16. The expanded view of the normalized output and input spectrum of the class-E amplifier	132
Figure 6.17. The schematic of the class-E amplifier prototype.....	133
Figure 6.18. The schematic of the class-E amplifier prototype with the diode.....	134
Figure 6.19. Measured spectrum of the digital pattern A (NB=40) with 100MHz frequency span	135
Figure 6.20. Measured spectrum of the digital pattern B (NB=20) with 100MHz frequency span	135
Figure 6.21. Measured spectrum of the digital pattern A (NB=40) with 6GHz frequency span	136
Figure 6.22. Measured spectrum of the digital pattern B (NB=20) with 6GHz frequency span	136
Figure 6.23. Comparison of the measured input and output spectrum of the broadband amplifier.....	137
Figure 6.24. Measured output spectrum of the Class-E amplifier.....	138
Figure 6.25. Measured output spectrum of the Class-E amplifier with diode.....	138
Figure 6.26. Comparison of the measured spectrum of two Class-E amplifiers	139

List of Tables

Table 2.1. Comparison of the total efficiency.	22
Table 3.1. Efficiency and power comparison of the conventional and the modified driving approach	59
Table 3.2. Circuit parameters used in the analytical results	70
Table 7.1. Summary of pros and cons of the investigated techniques	145

Acknowledgements

First and foremost, I would like to thank my advisor Professor Peter Asbeck for his invaluable guidance and support throughout my graduate studies. His never-ending patience, dedication and encouragement have been a great inspiration.

I would also like to thank my thesis committee: Professor Larry Larson, Professor Paul Yu, Professor Andrew Kummel, and Professor Prab Bandaru for providing precious feedback and suggestions.

It is my pleasure to work with my incredible colleagues. Their support, encouragement helped me during the various phases of my research. I would like to thank Dr. Masaya Iwamoto who initialized several projects related to my work in UCSD for his mentorship, thank Paul Draxler and Ian Langmore for enhancing my Matlab skill, and thank Andre Metzger, Jeremy Rode, Dr. Peter Zampardi and Don Kimball for their help in many projects. I also appreciate the discussion with Dr. David Choi and Marcus (Hsuan-Yu) Pan on outphasing amplifiers, and the discussion with Dennis Wang regarding semiconductor devices. I also would like to thank Dr. Dongjiang Qiao, Dr. Yu Zhao and Mingyuan Li for their encouragement and support. Many other group members have also been very helpful and supportive and that makes my stay in UCSD an enjoyable and memorable experience.

Family support makes this work possible. I would like to express my gratitude to my lovely wife, Chen-Hui, for her understanding and support. She has been my extraordinary other half. I also appreciate my sister, Tzu-Hsing, for her encouragement and consideration. I am deeply indebted to my mother and father for their unfailing love which always motivates me to move forward.

The material in chapter 2 is as it appears in “Design of high-efficiency current-mode class-D amplifiers for wireless handsets,” T. P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, *IEEE Trans. on Microwave Theory & Tech.*, vol. 53, pp. 144-151, Jan. 2005. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

Some of the material in chapter 3 and chapter 5 is as it appears in “Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters,” T. P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, *IEEE Trans. on Microwave Theory & Tech.*, vol. 55, pp. 2845-2855, Dec. 2007. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

The material in chapter 4 is as it appears in “CMOS Outphasing Class-D Power Amplifiers with Chireix Combiners,” T. P. Hung, D. K. Choi, L. E. Larson, and P. M. Asbeck, *IEEE. Microwave. and Wireless Comp. Letters*, vol. 17, pp. 619-621, Aug. 2007. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

Vita

- June 1999 B.S. Electrical Engineering, National Central University, Taiwan
- June 2001 M.S. Communication Engineering, National Chiao-Tung University,
Taiwan
- 2002 - 2008 Graduate Student Researcher, University of California, San Diego
- March 2008 Ph.D. Electrical Engineering, University of California, San Diego

Publications

T. P. Hung, D. K. Choi, L. E. Larson, and P. M. Asbeck, "CMOS Outphasing Class-D Amplifier with Chireix Combiner," *IEEE Microwave and Wireless Comp. Letters*, vol. 17, pp. 619-621, Aug. 2007.

T. P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," *IEEE Trans. on Microwave Theory & Tech.*, vol. 55, pp. 2845-2855, Dec. 2007.

T. P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "Design of high-efficiency current-mode class-D amplifiers for wireless handsets," *IEEE Trans. on Microwave Theory & Tech.*, vol. 53, pp. 144-151, Jan. 2005.

J. Rode, T. P. Hung, and P. M. Asbeck, "An All-Digital CMOS 915 MHz ISM Band 802.15.4 / ZigBee Transmitter with a Noise Spreading Direct Quantization Algorithm," accepted by *2008 IEEE MTT-S Int. Microwave Symp.*.

T. P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," in *2007 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1091-1094, June 2007.

T. P. Hung, L. E. Larson, and P. M. Asbeck, "CMOS Out-phasing Class-D Power Amplifiers with Chireix Combiners," presented in *2007 IEEE Power Amplifier Symposium*, Long Beach, CA, Jan. 2007.

J. Rode, T. P. Hung, and P. M. Asbeck, "Multilevel Delta-Sigma-Based Switching Power Amplifiers," presented in *2006 IEEE Power Amplifier Symposium*, San Diego, CA, Jan. 2006.

D. Qiao, D. Choi, Y. Zhao, D. Kelly, T. P. Hung, D. Kimball, M. Li, and P. Asbeck, "Antenna Impedance Mismatch Measurement and Correction for Adaptive CDMA Transceivers," in *2005 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 783-786, June 2005.

T. P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "High efficiency current-mode class-D amplifier with integrated resonator," in *2004 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 2035-2038, June 2004.

D. Qiao, T. P. Hung, F. Wang and P. Asbeck, "Measurement of Antenna Load Impedance for Power Amplifiers," presented in *2004 IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, San Diego, CA, Sept. 2004.

P. M. Asbeck, P. Draxler, I. Langmore, T. P. Hung, M. Li, D. Kimball and L. E. Larson, "Time domain characterization of power amplifiers nonlinearity and memory effects," presented in *62nd ARFTG Microwave Measurements Conf. – Nonlinear workshop*, Dec. 3, 2003

P. Draxler, I. Langmore, T. P. Hung, P. M. Asbeck, "Time domain characterization of power amplifiers with memory effects," in *2003 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 803-806, June 2003.

T. P. Hung and Tzuang, C.-K.C., "A fully all-planar integrated Ka-band FSK transceiver module" in *2001 Asia-Pacific Microwave Conf. Proc.*, vol. 2, pp. 962-965, Dec. 2001

T. P. Hung and Tzuang, C. -K.C., "Millimeter-wave active integrated planar antenna array emitting cone-shaped pattern," in *31th European Microwave Conf. Proc.*, vol. 2, pp. 21-24, London, UK, Sept. 2001.

C. J. Lee, T. P. Hung, S. C. Lin, H. S. Wu, C. Y. Tsai, K. F. Huang, Y. C. Chen, W. C. Lee and Tzuang, C. -K.C., "A fully all-planar integrated Ka-band FSK transceiver module" in *2001 Asia-Pacific Microwave Conf. Proc.*, vol. 3, pp. 1084-1087, Dec. 2001.

ABSTRACT OF THE DISSERTATION

High Efficiency Switching-Mode Amplifiers for Wireless Communication Systems

by

Tsai-Pi Hung

Doctor of Philosophy in Electrical Engineering (Electrical Circuits and Systems)

University of California, San Diego, 2008

Professor Peter M. Asbeck, Chair

Switching-mode amplifiers represent attractive possibilities for RF wireless communication systems because their high efficiency can potentially extend the battery life time for portable devices, lower the cost of heat-sinking equipment and increase the device reliability. The reason such circuits are not widely used at present is the difficulty in maintaining the signal fidelity required for the modern complex modulation formats such as EDGE (Enhanced Data rates for GSM Evolution), CDMA (Code Division Multiple Access) or OFDM (Orthogonal Frequency Division Multiplexing) signals. The objective of this dissertation is to investigate and analyze options for circuits and system configurations based on switching-mode amplifiers and as a result provide insight for use of switching amplifiers in modern wireless communication systems to achieve high linear amplification as well as high efficiency.

First, a current-mode class-D amplifier which is designed to achieve high efficiency at RF frequencies was investigated and the loss mechanisms were analyzed. Two current-mode class-D amplifiers based on GaAs HBTs with different novel on-

chip inductor implementations were designed, fabricated and measured. The results achieved efficiencies up to 78% (in nonlinear operation) at 700MHz were compared to demonstrate the circuit performance.

The counterpart of current-mode class-D amplifier, the voltage-mode class-D amplifier was also analyzed. The loss mechanisms were expressed in formulations which can be used to estimate the amplifier efficiency based on circuit parameters. A voltage-mode class-D was built in CMOS technology. A measured drain efficiency of 62% was achieved at 800MHz.

Based on the designed voltage-mode class-D amplifiers, several approaches for the implementation of linear amplifier were developed for CDMA signals, including digitally-driven outphasing amplifier systems and delta-sigma amplifier systems. The outphasing technique was shown to provide amplification with adequate linearity to achieve the ACPR specifications along with efficiency of 48% for CDMA signals. The limitation of the efficiency enhancement via using the Chireix structure was addressed based on the loss analysis results derived for voltage-mode class-D amplifiers.

The delta-sigma modulation approach was also investigated using the voltage-mode class-D amplifiers. The delta-sigma modulated signals were first generated to provide good noise shaping and linearity with CDMA signals. The switching amplifier systems based on the delta-sigma signals was then built and measured. The results show the linearity specification was achieved along with efficiency of 33%. Tradeoffs of efficiency and signals fidelity were analyzed for this architecture.

Finally, a new digital modulation scheme, digital polar modulation, was presented. The linearity of new modulation scheme was demonstrated by two-tone

signals. The system was able to show high efficiency of 54% along with good linearity (with IM3 below -39dBc). The results illustrate the promise of this approach for future digital RF transmitter systems.

Chapter 1

Introduction

1.1 Power Amplifiers in Wireless Communication Systems

With 3G wireless handsets gaining popularity, cell phones are becoming a one-stop multimedia station with features such as email, internet browsing, and video downloads. The new mobile devices require higher transmit-and-receive rates, resulting in greater power consumption and reduced available time for usage on a given battery charge. Therefore, minimizing the power consumption of the mobile devices is a critical challenge for both system and circuit design.

Figure 1.1 shows a simplified modem transmitter architecture. The RF power amplifier at the last stage is used to achieve signal amplification by converting a significant amount of DC power to the desired RF output power. That is also the most power hungry component in the transmitter chain, consuming up to 40% to 60 % of the overall power budget in some cases. Reduction of the power consumption at the amplifier stage can provide a significant increase in the battery life of the wireless device [1].

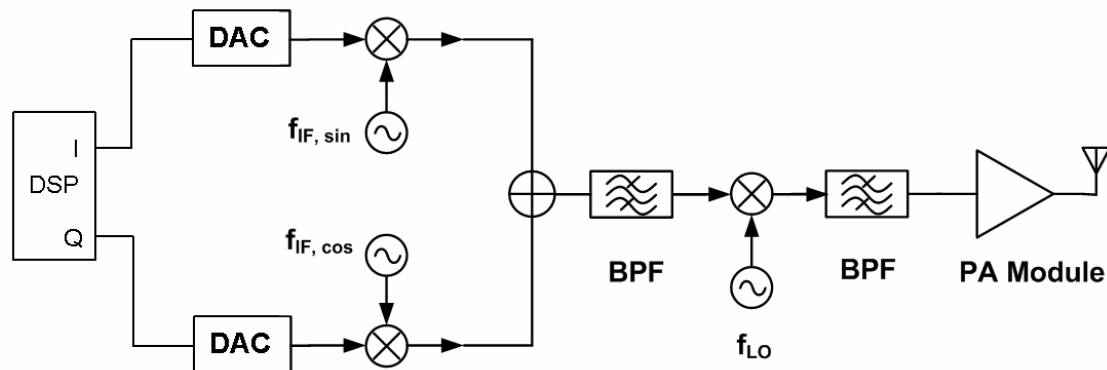


Figure 1.1 Simplified transmitter architecture with a power amplifier at the last stage.

In addition to energy saving, maintaining signal fidelity through the transmitter chain is also required. Frequency or phase modulated signals such as FM, FSK, and GMSK have constant envelopes, so do not require linear amplification. However, linear amplification is necessary when the signals contain both amplitude modulation and phase modulation such as modern shaped-pulse modulation (QAM, QPSK, and CDMA) and multiple carriers (OFDM) which have non-constant envelopes. Non-linear amplification causes both in-band and out-of-band distortion, resulting in loss of signal accuracy and interference with the signals in other channels. There are various figures of merit to characterize the system linearity. Adjacent Channel Power Ratio (ACPR) compares the desired channel power to the noise in a specified band at a specified frequency offset, as show in Figure 1.2. Error Vector Magnitude (EVM) describes the distance between the transmitted vectors and ideal vectors within a specified channel [2].

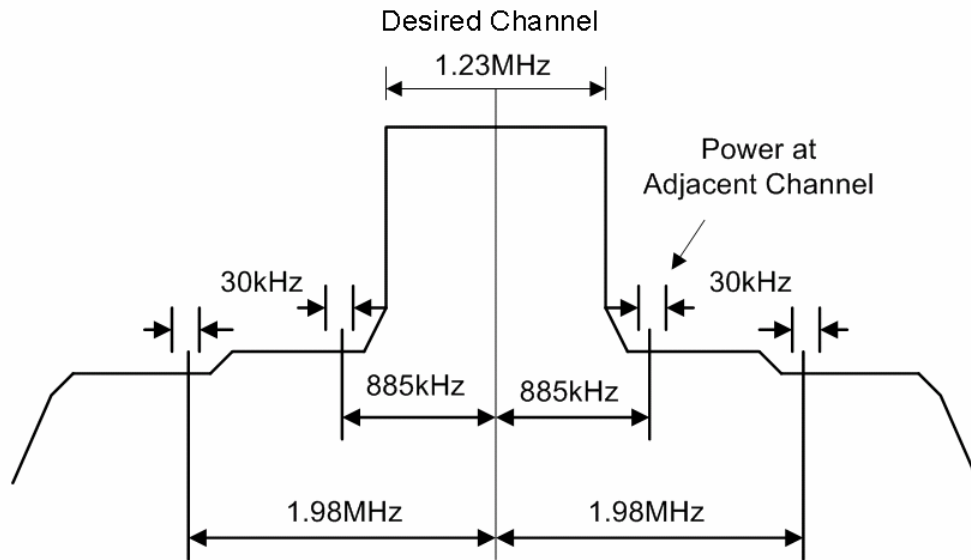


Figure 1.2: Example of ACPR spectrum mask [2].

Systems with amplitude modulation signals or multi-carrier signals generate time-varying output power. Peak-to-average power ratio (PAR) is used to characterize the relationship between peak power and the average power of the modulated signals. Typically, the amplifiers used in these systems need to be operated at a backed-off average power to avoid getting into saturation region during the peak excursions, thus maintaining linear amplification. Figure 1.3 shows the probability distribution functions (PDF) of three modulation schemes [5]. AMPS/GSM has constant envelopes, so its PDF is a delta function located at peak power. For $\pi/4$ QPSK and multi-carrier (OFDM), the peak-to-average ratio is about 5-8 dB and 8-13dB, respectively. The PDF indicates the amplifier stage spends very limited amount of time generating peak power for the non-constant envelope modulation signals, so the efficiency calculation needs special consideration.

Figure 1.4 shows an example ideal efficiency characteristics normalized to the output power of a class-B amplifier. Highest efficiency occurs at peak power and drops with output power. Therefore, for the amplifiers used in the non-constant envelope modulation system, the efficiency has to be averaged over conditions of usage. It is noteworthy that the amplifier efficiency at the lower power region has significant impact on the overall system efficiency.

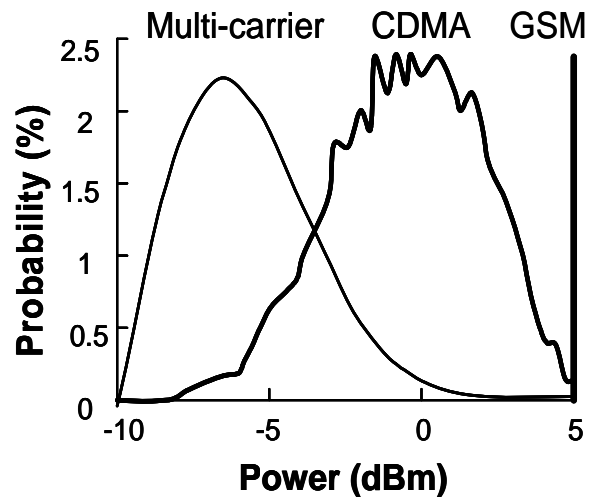


Figure 1.3: Envelope power density distribution functions of constant envelope modulated signals (GSM) and non-constant modulated signals (CDMA and Multi-carrier) [5]

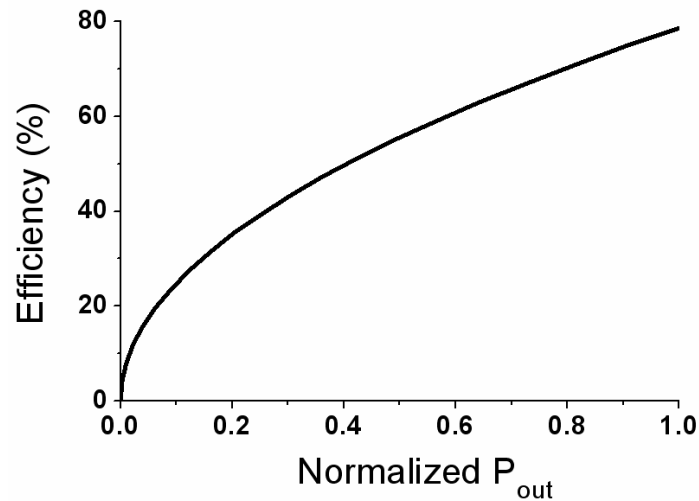


Figure 1.4: Efficiency vs. normalized output power of an ideal class-B power amplifier. The peak efficiency is 78.5%.

There is a wide variety of configurations for power amplifiers using different biasing conditions and load networks. They can be classified in two broad categories: those which attempt to preserve the original input signal at the output and those which do not attempt to do so. The first category corresponds to *linear amplifiers* and the second category corresponds to *non-linear amplifiers*. Due to the effort of preserving the wave-shape of the input signals, linear amplifiers usually have to consume a significant amount of power, resulting in lower efficiency. Class-A, Class-AB, and Class-B are the three main classes within this category [2,3,4].

Without the attempt for signal preservation, nonlinear amplifiers can obtain higher efficiency by operating in a region of strong gain compression, or by utilizing the active devices as switches. There are several classes within this category ranging from self-bias schemes (Class-C) to various forms of switching amplifiers (Class-D, E, F, and etc.). Among all the non-linear amplifiers, switching mode amplifiers can

operate in the most efficient way, ideally 100%, via achieving zero-voltage switching (ZVS) or zero-current switching (ZCS) [3]. This high efficiency feature makes the switching amplifier a very attractive candidate for wireless communication systems. The basics operation of different switching mode amplifiers can be found in many references [2, 3].

The high efficiency performance of switching amplifiers can be understood by examining the time domain waveforms, as discussed in the next section. The challenges of using switching mode amplifiers in modern wireless systems are also discussed.

1.2 High Efficiency Switching Mode Amplifiers

For switching mode amplifiers, energy loss associated with the active devices can be minimized via waveform engineering in either a time domain approach (reactance matching, such as Class-E amplifiers) or a frequency domain approach (harmonic termination, such as Class-F amplifiers).

The power dissipated at the transistor can be represented as

$$P_{loss} = \frac{1}{T} \int_0^T V(t) \cdot I(t) dt \quad (1-1)$$

Here V and I are the output voltage across the transistor and the output current flowing through the transistor which are time varying.

Figure 1.5 shows the $V(t)$ and $I(t)$ of the transistors in several forms of ideal switching mode amplifiers. One thing in common is that there is very little or no

overlap between V and I at any given time, leading to low power dissipation according to (1-1). For example, class-D amplifiers have square voltage waveform and half-rectified sinewave current. Very high efficiency can be then realized. M. Berkhout reported an integrated 200W class-D amplifier for audio applications [15]. The carrier frequency is at 350 kHz and efficiency great than 90% is achieved.

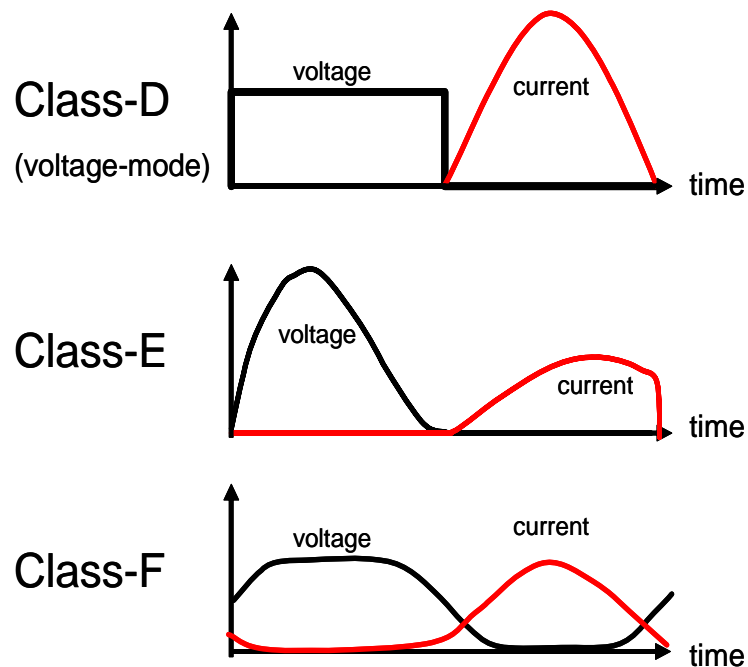


Figure 1.5: Voltage and current waveforms of various switching mode amplifiers

In reality, there are several non-ideal factors to degrade the amplifier efficiency such as output capacitance of the transistor, finite transition time, ON-state resistance, and non-ideal output networks. The loss due to the first two factors increases with higher frequency, so the switching amplifiers are difficult to implement in the RF frequency range. Techniques like the class-E configuration can minimize the output capacitance loss through zero-voltage switching, resulting in the potential of

maintaining high efficiency at high frequencies. G. K. Wong reported a class-E amplifier operating at 800MHz with GMSK signals [16]. A PAE of 74% was achieved.

Linearity is another critical issue for power amplifiers in modern communication systems employing non-constant envelope modulation. To achieve linear amplification, switching mode amplifiers can be combined into other linear transmitter architectures which adopt nonlinear components such as Outphasing, Envelope Elimination Restoration (EER) and so on. To restore the original signals at the amplifier output and maintain high system efficiency, the modulated amplitude has to be reproduced in a certain way, instead of passing through the switching amplifiers. In an outphasing system, the amplitude information is encoded into the phase difference of two constant-envelope driving signals and then reproduced after summing the amplifier outputs. In an EER system, the amplitude information at the output is reproduced through supply voltage modulation. The ideal operation of these linear amplification architectures can be found in various references [3, 4].

In idealized outphasing systems, the switching mode amplifiers are assumed to be ideal voltage-controlled voltage sources. Those voltage sources provide the current needed under any given load condition. The powers generated by the sources are linearly summed at the output. Further details of outphasing system will be reviewed in Chapter 3. In reality, some factors such as ON-state resistance, output capacitance, etc make the amplifiers not ideal voltage sources, thus degrading the linearity and efficiency of an outphasing system. J. Grundlingh reported an outphasing system composed of Class-F amplifiers for 802.11a applications, achieving a PAE of

33% at 7.8dB power back-off point [6]. The chip is implemented in GaAs pHEMT process using bondwire to implement the lumped inductor. The EVM of the chip set is better than -27dB when operating with 802.11a signals.

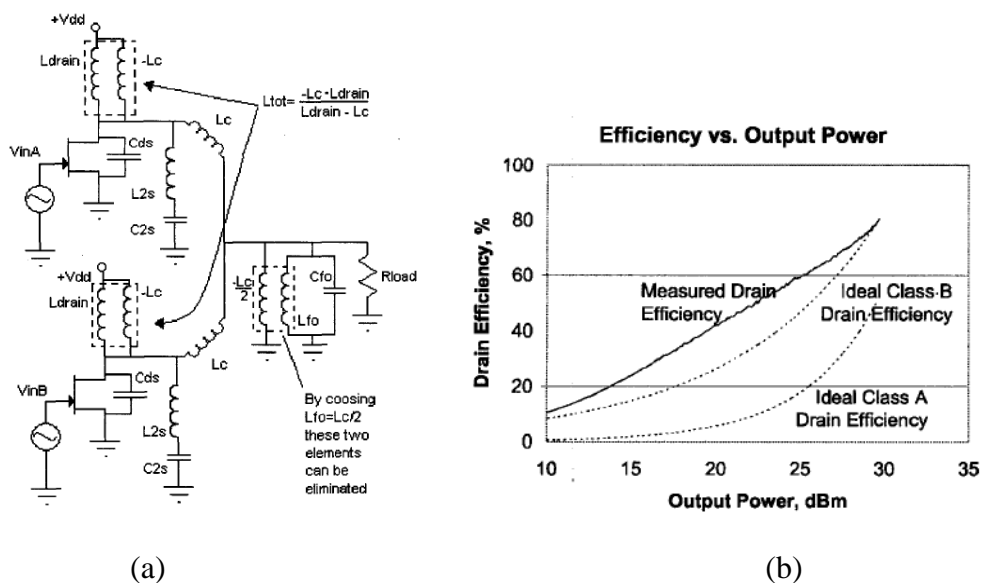


Figure 1.6: (a) Schematics of an outphasing system using Class-F amplifiers (b) Comparison of the measured efficiency with ideal class-A and B amplifier as a function of output power) [6]

D. Kimball, etc. reported an ET amplifier system for W-CDMA applications operating at 2.14GHz [7]. The measured average power-added efficiency is as high as 50.7% for a W-CDMA modulated signal with peak-to-average power ratio of 7.67dB at an average output power of 37.2W and gain of 10dB. The measured EVM is as low as 1.74% with ACPR of -51dB at an offset of 5MHz.

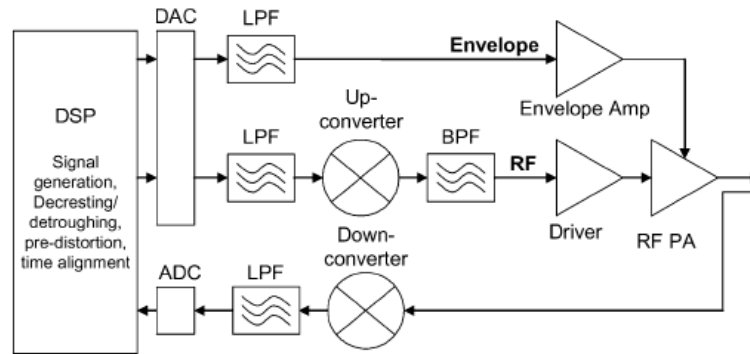


Figure 1.7: Block diagram of ET base station amplifier including signal generation and up/down conversion [7].

For the applications mentioned above, the switching amplifiers are driven by constant envelope signals in an analog fashion. However, the driving signals can be digital (binary) for switching mode amplifiers without degrading the amplifier performance. As a result, switching amplifiers can be driven by digital circuits directly, leading to the potential of system integration. The transmitter architecture which uses digital signals to control and drive switching mode amplifiers is called here a digital RF transmitter.

1.3 Digital RF Transmitters

Size and cost are always strong driving forces for mobile device innovation. Nowadays, the power amplifier is usually a separate chip used in conjunction with other baseband or low power circuits. This is because advanced technologies such as GaAs or SiGe can boost the amplifier performance, thanks to higher breakdown voltage, and also by preventing problems such as lossy substrate. Integrating the power amplifier with baseband digital circuits in CMOS technology is an exciting

challenge. Thanks to the advance of CMOS technology, digital circuits are able to operate at higher microwave frequencies where usually analog circuits used to be employed. Advantage of high-speed digital signal processing (DSP) opens a new era for power amplifier and transmitter design. Low costs, ease of integration, simplified systems are the major advantages to implement the wireless system in a digital way.

Current research effort on this topic is highly active. A. Kavousian reported a digitally modulated CMOS power amplifier for 64QAM OFDM system [11]. The amplifier architecture is shown in figure 1.8. The polar decomposition block generates both digital phase signals and amplitude signals which are sent to a decoder. According to the digital amplitude, the decoder controls the number of operated amplifiers to obtain corresponding output power level. A power-added-efficiency (PAE) of 7.2% is achieved with an output power of 13.6dBm for 64QAM OFDM signals.

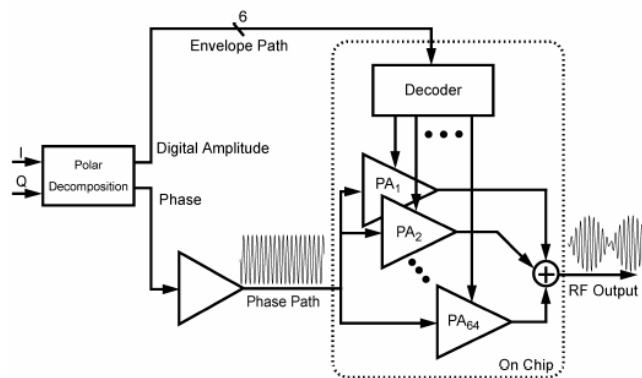


Figure 1.8: System diagram of a digital polar modulated PA [11].

1.4 Scope of the Dissertation

This thesis is dedicated to exploring the applications of switching mode amplifiers in modern communication systems. The main challenge is to utilize the high efficiency feature of switching mode amplifiers while meeting the linearity requirements in communication systems. The solution options explored here were initially depend on the modulation characteristics of the systems, beginning with constant envelope modulation (such as GSM), followed by non-constant envelope modulation (such as CDMA).

For constant envelope modulation system, there is no need to reproduce the amplitude signal variations at the amplifier output. Therefore, the effort was focused on maximize efficiency. The loss mechanisms of the switching mode amplifier were analyzed and possibilities were identified for improving the amplifier efficiency at high frequencies. Current-mode class-D amplifiers which have the potential to minimize the output capacitance loss were investigated. A prototype CMCD amplifier was demonstrated at 700MHz with GaAs HBT technology, achieving a collector efficiency of 78.5% and a PAE of 68.5% with an output power of 29.5dBm. Compared to commercial GSM amplifiers which have an average PAE of 50% to 55%, the CMCD amplifier shows a significant efficiency improvement. The analytical model developed here can estimate accurately the amplifier efficiency using known circuit parameters, providing useful design guidance.

For non-constant envelope modulation systems, to achieve adequate linearity, switching amplifier needs to be operated with specially designed inputs and load

structures. Three linear amplification architectures employing switching mode amplifiers were investigated: the outphasing amplifier system, the delta-sigma modulation system, and the envelope polar modulation system.

In an outphasing amplifier system, as shown in Fig. 1.9, the complex signals are separating into two constant envelope signals by SCS (signal component separator) such that the two switching-mode amplifiers in the outphasing amplifier system can be driven by constant envelope signals to maintain the efficiency. After combining the amplifier output, the signal fidelity can be preserved. In this thesis, the Chireix output combining technique was investigated to show the effect on the amplifier efficiency and the limit of efficiency boosting in the low power region. The outphasing amplifier system was demonstrated at 800MHz with CMOS technology and showed to achieve a drain efficiency of 48% with an output power of 15.4 dBm for CDMA IS-95 signals. This efficiency performance is superior to what is obtained in conventional amplifier using III-V devices. This amplifier can also potentially reduce the cost and be integrated with the baseband circuitry.

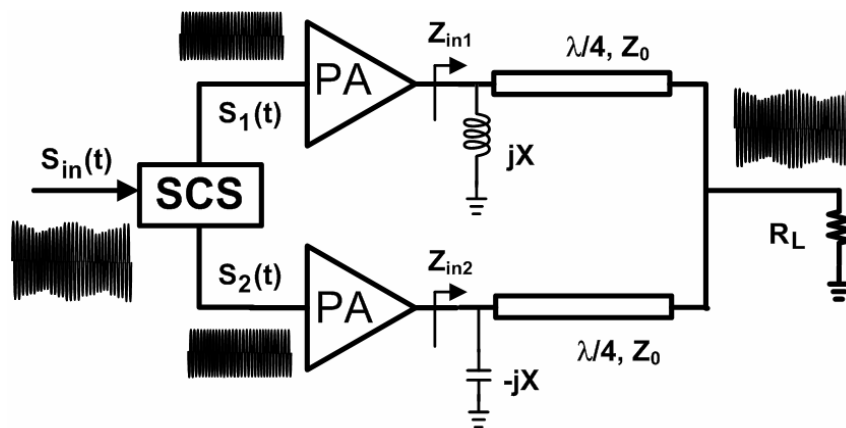


Figure 1.9: Simplified block diagram of an outphasing system with a Chireix combiner.

The second potential solution focused on an amplifier system with inputs modulated with digital patterns. By using voltage mode class-D amplifiers, the desired complex signals can be reproduced at the amplifier output as shown in Fig. 1.10. In this work, delta-sigma modulations (including both two-level and three-level modulation) were investigated.

The proposed delta-sigma amplifier was demonstrated in CMOS technology, achieving a drain efficiency of 33% with an output power of 15 dBm for CDMA signals. This amplifier efficiency is comparable to that attained in commercial components implemented with III-V devices, but potentially has lower cost and high integration capability due to the employed technology. The amplifier output exhibits signal accuracy when driven at maximum power level adequate to meet most of the linearity specifications for CDMA. Excess digital noise remains a vexing problem; however, other passive components in the transceiver system such as duplexers can be helpful to this problem by providing additional rejection.

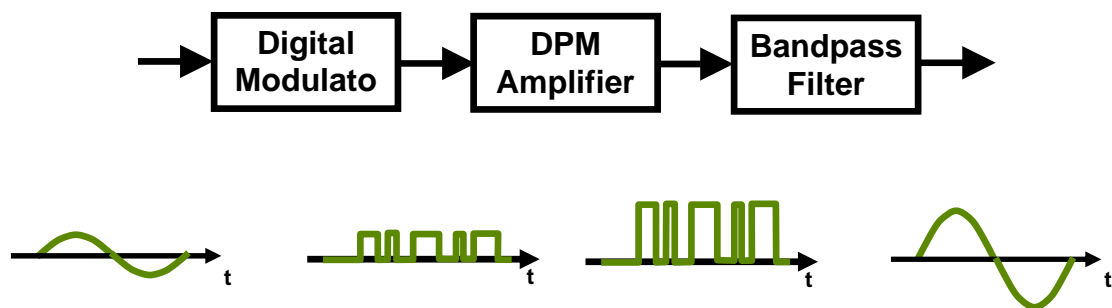


Figure 1.10: Simplified block diagram of a digital pulse modulation system and the representative time domain waveforms

The final proposed solution for non-constant envelope modulation systems is a system employing digital modulation of the envelope in a polar modulation system. The RF stage is based on a switching mode class-E amplifier. The main concept is to develop the modulation technique which can maintain signal fidelity and minimize the energy loss at the amplifier stage. The envelope switching digital patterns allow the amplifier to be operated in two modes, normal operation and OFF mode. At normal operation mode, the amplifier is operated as a normal class-E amplifier with high efficiency. At OFF mode, the amplifier is shut down to save power.

The proposed envelope switching amplifier was demonstrated using pHEMT technology, achieving a drain efficiency of 54% with an output power of 18.7 dBm while driven by a digital pattern encoding a two-tone signal. The third-order intermodulation product (IM3) was -39dB below the two fundamental tones (which corresponds to good linearity performance). This result demonstrates promising potential of this novel modulation scheme and amplifier configuration.

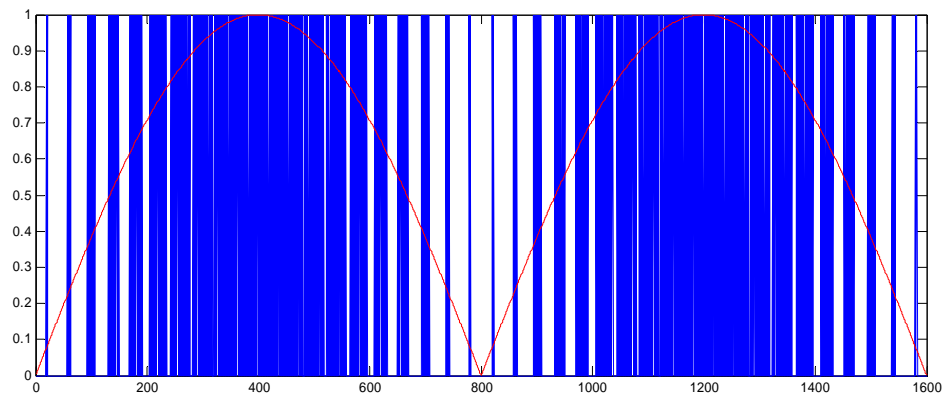


Figure 1.11: The digital envelope polar modulation pattern (blue) and the envelope (red) of a two-tone signal.

1.5 Organization of Dissertation

This dissertation is organized as below:

Chapter 1 outlines the background of switching mode power amplifier in wireless communication systems, highlighting concepts such as efficiency calculation for non-constant envelope signals, power back-off. The advantages of digital RF transmitters which are strong motivations for this work are also provided.

Chapter 2 discusses a high efficiency solution for constant envelope modulation systems, current-mode class-D amplifiers. The chapter begins with a discussion of the output capacitance loss of a voltage-mode class-D amplifier and then follows with the discussion of basic operation and design considerations of a current-mode class-D amplifier. Simulation, measurement results and loss analysis of a current-mode class-D amplifier are then discussed.

Chapter 3 is dedicated to CMOS voltage-mode class-D amplifier design. Shoot-through current suppression technique is introduced for efficiency enhancement and followed by the circuit implementation. The measured performance for an experimental amplifier prototype integrated in 0.18-um CMOS technology is presented. The design considerations of VMCD amplifiers are discuss and analyzed, leading to an equation-based analytical model for efficiency estimation. The comparisons of predicted amplifier performances with simulation results are provided.

Chapter 4 examines an outphasing class-D amplifier with a Chireix combiner which utilizes the VMCD amplifier presented in Chapter 3. It begins with the operation of an outphasing system and then follows with the amplifier load impedance

investigation which is a critical factor to achieve efficiency peaking in the low power region. The measured results including the efficiency and ACPR are shown.

In Chapter 5, an H-bridge class-D amplifier in a pulse modulation transmitter is presented. The first part of the chapter introduces the two and three level delta-sigma modulation approaches, followed by a section on the design of an H-bridge class-D amplifier which can accommodate both types of signals. The implementation and measured results are provided. An efficiency prediction using the analytical model for this application concludes the chapter.

Chapter 6 presents a new modulation scheme, envelope polar modulation. The modulation strategy is discussed with an example of two-tone signals, followed by the discussion and demonstration of class-E amplifier operation while driven by the modulated digital pattern.

The results of this thesis are summarized in Chapter 7, and possible future investigation areas are suggested.

1.6 Reference

- [1] T. H. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits*. New York: Cambridge University Press, 2004.
- [2] M. Albullet, *RF Power Amplifiers*. Atlanta: Noble Publishing, 2001.
- [3] S. C. Cripps, *RF power amplifiers for wireless communications*, Boston: Artech House, 1999.
- [4] P. B. Kennington, *High Linearity RF Amplifier Design*. Norwood, MA: Artech House, 2000.

- [5] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Potheary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
- [6] J. Grundlingh, K. Parker, and G. Rabjohn, "A high efficiency Chireix Out-phasing power amplifier for 5GHz WLAN applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Fort Worth, TX, June 2004, pp. 1535-1538.
- [7] D. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. E. Larson and P. M. Asbeck, "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs," *IEEE Trans. Microwave Theory & Tech.*, vol. 54, no. 11, pp. 3848-3856, Nov. 2006.
- [8] N. O. Sokal and A. D. Sokal, "Class E-A new class of high efficiency tuned single-ended power amplifiers," *IEEE J. Solid State Circuits*, vol. SC-10, pp. 168–176, June 1975.
- [9] F. H. Rabb, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 725–735, Dec. 1977
- [10] H. Kobayashi, J. M. Hinrichs and P. M. Asbeck, "Current-mode class-D power amplifiers for high efficiency RF application," *IEEE Trans. Microwave Theory & Tech.*, vol. 49, no. 12, pp. 2480-2485, December 2001.
- [11] A. Kavousian, D. K. Su, B. A. Wooley, "A digitally modulated polar PA with 20MHz signal BW," ISSCC
- [12] A. Long, J. Yao, and S. I. Long, "A 13 W current mode class D high efficiency 1 GHz power amplifier" *2002 45th Midwest Symp. on Circuits and Systems Dig.*, vol. 1, pp. 33-36, Aug., 2002.
- [13] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 51, no. 6, pp. 1677-1690, June 2003.
- [14] F. Bohn, S. D. Kee, and A. Hajimiri, "Demonstration of a harmonic-tuned class E/F_{odd} dual band power amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1631–1634.
- [15] M. Berkhout, "An integrated 200-W Class-D audio amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1198-1206, Jul. 2003.

- [16] G. K. Wong, and S. I. Long, "An 800MHz HBT class-E amplifier with 74% PAE at 3.0 volts for GMSK," in *Gallium Arsenide Integrated Circuit Symp. Dig.*, pp. 299-302, Oct. 1999.

Chapter 2

Current-Mode Class-D Power Amplifiers

2.1 Introduction

Power amplifier efficiency is a significant factor for the efficiency of most wireless systems. Poor efficiency of the last power amplifier stage leads to large energy loss, not only deteriorating system efficiency but also exacerbating thermal issues with devices.

Switching mode power amplifiers can potentially provide high collector efficiency up to 100% and partially mitigate thermal runaway concerns by operating transistors as switches [1-3]. However, due to parasitic reactance, transition time, and turn-on resistance of the transistors, amplifier efficiency degrades with increasing frequency. For instance, the class-D amplifier is very popular for high efficiency applications at low audio frequencies. However, it is hard to maintain this high efficiency at RF frequencies because the output shunt capacitance of the transistors causes significant loss. Energy $1/2CV^2$ is dissipated per cycle when the output capacitance, C , discharges from an initial voltage [1-5]. The class-E amplifier topology solves this problem by achieving zero voltage switching (ZVS) operation [6-12]. However, uncertain duty cycle, nonlinear capacitance and other parasitic reactance can degrade class-E operation.

Current mode class-D (CMCD) amplifier operation is similar to that of a conventional class-D amplifier (voltage mode class-D) with interchanged voltage and current waveforms. As a result, the output shunt capacitance loss can be eliminated due to ZVS. Recently, a CMCD amplifier was demonstrated to attain high efficiency (75.6%) at RF frequency (900MHz) with output power 28.6dBm (0.73W) using discrete circuit elements [13]. A CMCD power amplifier for the base station applications was also shown to achieve high efficiency (60%) with high output power (13W) [14]. An amplifier of the closely related class-E/ $F_{2, \text{odd}}$ with 85% drain efficiency at 7MHz has also been reported [15-17]. However, detailed design analysis of the CMCD amplifier has not been well developed. In this chapter, the factors degrading the CMCD amplifier efficiency are discussed analytically. We show that by integrating the parallel LC resonator on chip, it is possible to reduce the circuit complexity and eliminate parasitic reactance loss. Two CMCD amplifiers integrated with different LC resonator structures are compared and both show reasonable efficiency characteristics. The CMCD amplifier using a bondwire inductor achieves a collector efficiency of 78.5% at 700MHz with output power of 29.5dBm (0.89W) [18]. The design analysis and measurement results show CMCD amplifiers are a potential solution for wireless systems with constant envelope modulation. In the section 2.2, the basics of CMCD operation are described. Section 2.3 covers the analysis of efficiency in non-ideal circuits. Prototype CMCD amplifier designs and measurement results are shown in sections 2.4 and 2.5.

2.2 Basics of Current-Mode Class-D Amplifiers

Fig. 2.1 shows the simplified schematic and ideal voltage/current waveforms of a voltage mode class-D (referred to as conventional class-D) amplifier. By driving two transistors out of phase, the voltage across the transistors is a square waveform alternating between V_{CC} and zero. Through a series LC filter, higher order harmonics are blocked and only the fundamental component passes to the load. The current waveform becomes a half sine wave for each transistor. Ideally, since there is no overlap between voltage and current waveforms, efficiency of 100% can be achieved. However, if the transistors have output shunt capacitance, this capacitance must be charged or discharged to V_{CC} or ground. The resultant energy loss per cycle, E_C , can be expressed as

$$E_C = \frac{1}{2} C_{CE} V^2 \quad (2-1)$$

where C_{CE} is the collector-emitter capacitance and V is the collector-emitter voltage when the transistor is turned off. This output shunt capacitance discharge loss becomes dominant at high frequencies.

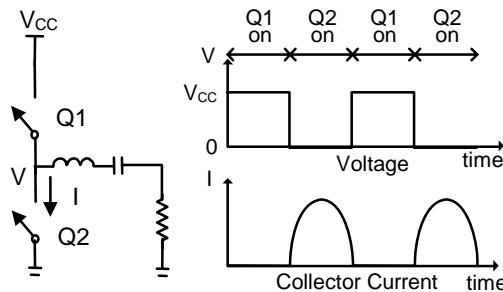


Figure 2.1: Simplified schematic and voltage/current waveforms of the voltage mode class-D amplifier

The current mode class-D amplifier, as shown in Fig. 2.2, is similar to the voltage mode class-D amplifier with interchanged voltage and current waveforms. The current through the transistors is a square wave while the voltage across the transistors is a half rectified sine wave. The overlap of high voltage and high current is thus avoided to attain high efficiency, and additionally, when the transistor turns on, the voltage across transistor is zero, so the output capacitance discharge problem is eliminated. A parallel LC resonator provides a short circuit for higher order harmonics and only the fundamental component reaches the load.

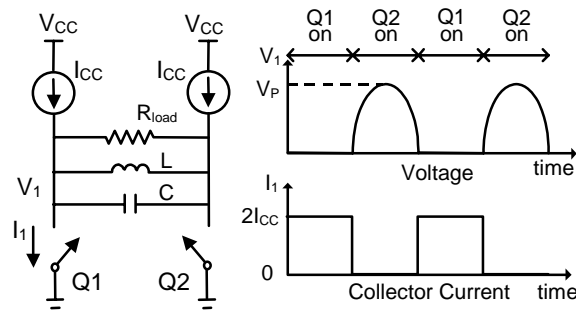


Figure 2.2: Simplified schematic and voltage/current waveforms of the current mode class-D amplifier.

In addition to the energy dissipated from stored energy in the switch output capacitance, there can be dissipation of energy stored in parasitic inductance in series with the switch. The loss per cycle is given by

$$E_L = \frac{1}{2} L_{series} I_L^2 \quad (2-2)$$

where L_{series} is the parasitic inductance; I_L is the current flowing through the inductance prior to the turn-off of the switch. While the CMCD amplifier is capable of

avoiding losses due to the parasitic capacitance through ZVS, losses associated with inductive parasitics are still present. In most cases (as described further below) it is beneficial to decrease L_{series} as far as possible. This can be accomplished if the LC resonator is integrated on-chip with the switching transistors.

2.3 Design Considerations for Current Mode Class-D Amplifiers

In practical operation, several factors distorting the ideal voltage/current waveforms tend to degrade the CMCD amplifier efficiency. For example, the real passive components have finite Q factors and the real transistors have parasitic reactance, non-zero turn-on resistance, non-zero transition time, and non-zero knee voltage. To simplify the discussion and to study the effects of each factor independently, this analysis evaluates each circuit imperfection factor separately. Combining all the factors can approximate the practical amplifier efficiency. The resultant CMCD amplifier efficiency, η_{CMCD} , can be expressed as

$$\eta_{CMCD} = \eta_{po} \cdot \eta_{tt} \cdot \eta_{tk} \cdot \eta_{pp} \cdot \eta_{pm} \quad (2-3)$$

where η_{po} represents the loss factor due to the odd harmonic leakage currents; η_{tt} represents the loss factor due to the finite transition time of the transistors; η_{tk} represents the loss factor due to the non-zero knee voltage of the transistors; η_{pp} represents the loss factor due to the parasitic resistance of the LC tank, and η_{pm} represents the loss factor for the output impedance matching network. In ideal operation, all these factors are equal to 1. The analysis results are useful to predict the

amplifier performance, and guide circuit design. Details of each factor are discussed in the following.

2.3.1 Higher order odd harmonic effects (η_{po})

The shunt capacitor, C, in the LC resonator is intended to provide a short circuit for the higher-order odd harmonic currents. Practically, there are higher order leakage current flowing through the load when the capacitor provides a non-ideal short circuit. If we assume the shunt inductor is an open circuit for the higher order currents, the leakage current (i_n) and the voltage across the load (v_{load}) can be expressed in terms of phase angle $\theta=\omega t$ by

$$i_n = \frac{4}{n\pi} I_{CC} \sin(n\theta), \quad (2-4)$$

$$v_{load} = -\frac{4}{\pi} I_{CC} \sin \theta \cdot R_{load} - \sum_{n=3,5,7..}^{\infty} \frac{4}{n\pi} I_{CC} \cdot \frac{\sin n\theta - nQ \cos n\theta}{1 + (n \cdot Q)^2} \cdot R_{load}, \quad (2-5)$$

where n is the harmonic index; I_{CC} is the DC current from the power supply; and R_{load} is the load resistance. The first term in (2-5) represents the voltage across the load induced by the fundamental current. The second term indicates the voltage induced by the higher order leakage current. The distortion of the voltage waveform across the load due to i_n depends on the Q factor of the resonator given by $Q=\omega \cdot R_{load} \cdot C$.

Fig. 2.3 shows the voltage waveform (normalized to $\frac{4}{\pi^2} I_{CC} R_{load}$) across the load with different Q values.

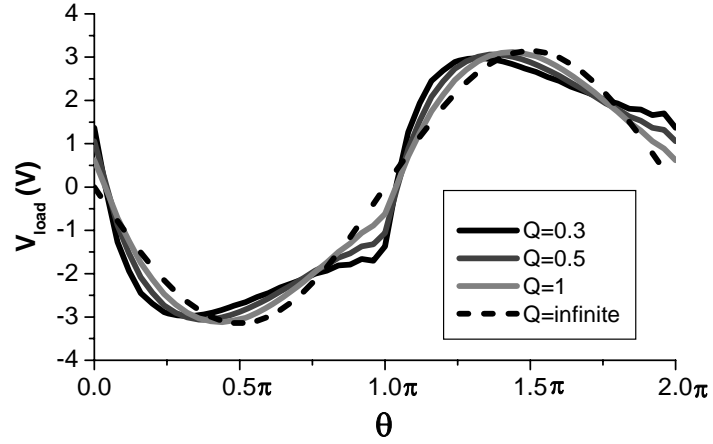


Figure 2.3: Normalized voltage waveform across the load, showing distortion by the high order harmonic leakage current. With lower Q factor, the voltage waveform has more distortion.

The total DC power consumption can be obtained by

$$\begin{aligned}
 P_{DC} &= \frac{1}{2\pi} \int_0^{2\pi} v_{load}(\theta) \cdot \left[\sum_{n=1,3,5,\dots}^{\infty} i_n \right] d\theta \\
 &= \frac{8}{\pi^2} I_{CC}^2 R_{load} + \sum_{n=3,5,7}^{\infty} \frac{8}{n^2 \pi^2} I_{CC}^2 R_{load} \frac{1}{1+(n \cdot Q)^2}
 \end{aligned} \tag{2-6}$$

Because the leakage currents do not affect the fundamental signal, the output power (P_{out}) remains at $\frac{8}{\pi^2} I_{CC}^2 R_{load}$. The efficiency factor, η_{po} , can be derived as

$$\eta_{po} = \frac{P_{out}}{P_{DC}} = \frac{1}{1 + \sum_{n=3,5,7}^{\infty} \frac{1}{n^2} \cdot \frac{1}{1+(n \cdot Q)^2}} \tag{2-7}$$

Fig. 2.4 shows the efficiency factor η_{po} with different Q factors. When Q is large enough, η_{po} can approximately reach 100%. This result suggests a high Q RLC

circuit is preferred to reduce the loss from the leakage currents. It also shows that third harmonic is the dominant term.

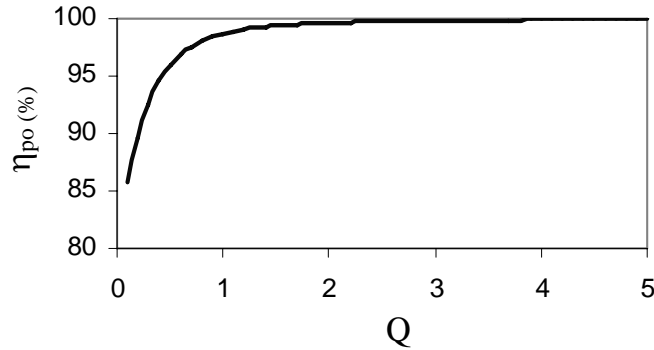


Figure 2.4: The efficiency factor η_{po} increases with the increasing Q factor. $Q = \omega \cdot R_{load} \cdot C$.

2.3.2 Effect of non-zero transition time (η_{tt})

When bipolar junction transistors operate in the saturation region, the forward-biased base-collector (BC) junction and the base-emitter (BE) junction store minority carriers in the base region, and potentially the collector region. To turn the transistors off, it takes time to remove these minority carriers before the BC junction becomes reverse-biased. For simplicity, a fixed time alignment between the voltage and current waveforms has been assumed. With different circuit embeddings, this alignment can vary (as discussed below). Based on this assumption, the current (i_1) flowing through the transistor Q1 is depicted in Fig. 2.5. τ represents the non-zero transition time, expressed in radians.

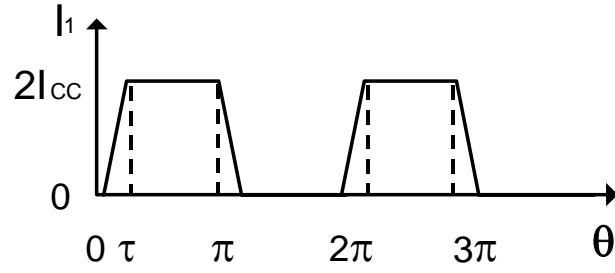


Figure 2.5: Waveform of the current i_1 , considering a non-zero transition time (τ).

By Fourier decomposition of the current waveform, the amplitude of the fundamental component of i_1 can be derived as

$$|i_{1_fund}| = \frac{8}{\pi} I_{CC} \frac{\sin(\tau/2)}{\tau}. \quad (2-8)$$

The DC term of the voltage is given by

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} V_G(\theta) d\theta + \frac{|v_{1_fund}|}{\pi}, \quad (2-9)$$

where

$$V_G(\theta) = \begin{cases} 2I_{CC}R_{ON}, & 0 \leq \theta \leq \pi + \tau, \\ 0, & \pi + \tau \leq \theta \leq 2\pi \end{cases} \quad (2-10)$$

and $|v_{1_fund}| = |i_{1_fund}| \cdot R_{load}$. R_{ON} is the turn-on resistance of the transistors.

The efficiency factor, η_{tt} , can be derived as

$$\eta_{tt} = \frac{\frac{16 R_{load}}{\pi R_{ON}} \frac{\sin^2(\tau/2)}{\tau^2}}{\pi + \tau + \frac{8 R_{load}}{\pi R_{ON}} \frac{\sin(\tau/2)}{\tau}}. \quad (2-11)$$

When R_{ON} is zero, the efficiency factor, η_{tt} , can be simplified as

$$\eta_{tt} = \frac{2 \sin\left(\frac{\tau}{2}\right)}{\tau}. \quad (2-12)$$

From (2-12), when τ is 0, η_{tt} can be 100%. Fig. 2.6 shows how η_{tt} degrades with increasing transition time.

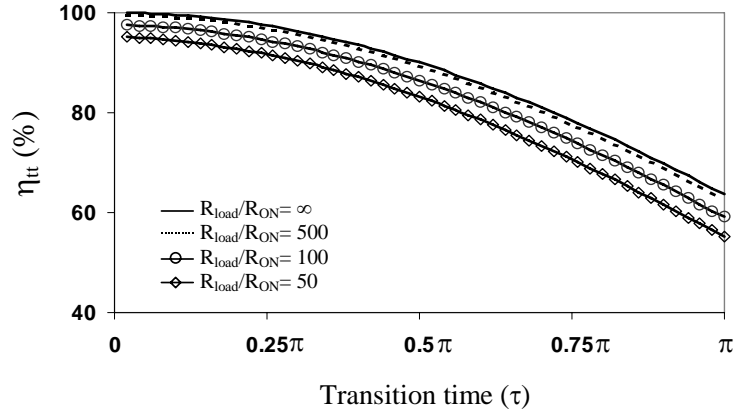


Figure 2.6: The efficiency factor η_{tt} drops with increasing transition time (τ).

2.3.3 Non-Zero Knee Voltage of the Transistors (η_{tt})

The knee voltage of a transistor includes an offset voltage (V_{offset}) and the voltage across the transistor on-state resistance (R_{ON}). A circuit model considering the transistor parasitic capacitance C_{CE} and the turn-on resistance of the transistors is shown in Fig. 2.7. The equations of the voltage and current waveform can be written as

$$i_1 = \begin{cases} 2I_{cc} - C_{CE}\omega_0\pi V_{cc} \cos(\theta), & 0 \leq \theta \leq \pi \\ -C_{CE}\omega_0\pi V_{cc} \cos(\theta), & \pi \leq \theta \leq 2\pi \end{cases}. \quad (2-13)$$

$$v_1 = \begin{cases} V_{offset} + (2I_{cc} - C_{CE}\omega_0\pi V_{cc} \cos(\theta))R_{ON}, & 0 \leq \theta \leq \pi \\ V_{offset} - V_p \sin(\theta) + (-C_{CE}\omega_0\pi V_{cc} \cos(\theta))R_{ON}, & \pi \leq \theta \leq 2\pi \end{cases}. \quad (2-14)$$

Using (2-13) and (2-14), we can derive the efficiency factor η_{tk} by

$$\begin{aligned}\eta_{tk} &= 1 - \frac{P_{loss}}{P_{DC}}, \\ &= 1 - \frac{2I_{CC}V_{offset} + 4I_{CC}^2R_{ON} + (C_{CE}\omega_0\pi V_{CC})^2R_{ON}}{2I_{CC}V_{CC}},\end{aligned}\quad (2-15)$$

where loss in the transistors (P_{loss}) is given by

$$P_{loss} = \frac{1}{\pi} \int_0^{2\pi} i_1 \cdot v_1 d\theta. \quad (2-16)$$

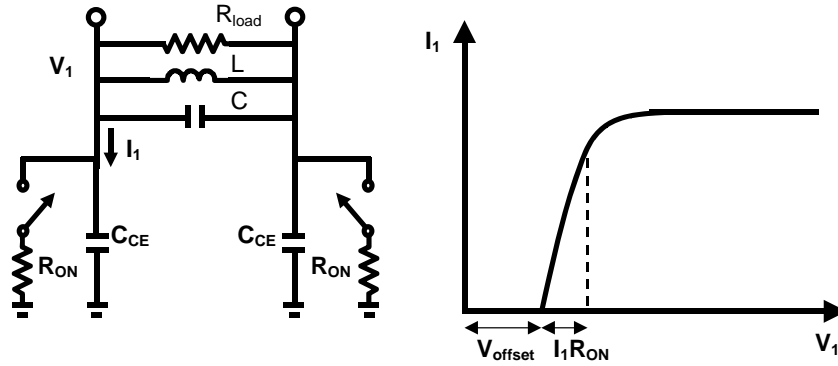


Figure 2.7: Simplified model for evaluating the effects of the knee voltage of the transistors.

In ideal operation, the parasitic capacitance C_{CE} can be absorbed in the LC resonator, so there is no power consumption due to the capacitance C_{CE} . However, if R_{ON} is not equal to zero, the capacitance term starts to degrade the amplifier efficiency. This result indicates that there is a design tradeoff between the transistor sizes.

2.3.4 Parasitic resistance of the LC resonator (η_{pp})

The finite Q factor of the LC resonator not only degrades the efficiency but also increases the stress of the transistors. According to the model shown in Fig. 2.7, R_{ON} is assumed to be zero. The efficiency factor, η_{pp} , can be expressed as

$$\eta_{pp} = \frac{G_{load}}{G_{load} + G'}, \quad (2-17)$$

where $G_{load} (=1/R_{load})$ is the conductance of the load. G' represents the total parasitic conductance from the capacitor and the inductor. G' increases as the Q factor of the inductor and the capacitor decreases. The waveform of the current flowing through the transistor Q1 (i_1) can be given by

$$i_1 = \begin{cases} \frac{1}{2} \pi^2 V_{CC} (G_{load} + G') - C_{CE} \omega_0 \pi V_{CC} \cos(\theta), & 0 \leq \theta \leq \pi \\ -C_{CE} \omega_0 \pi V_{CC} \cos(\theta), & \pi \leq \theta \leq 2\pi \end{cases}. \quad (2-18)$$

The peak of the current i_1 increases with lower Q during the time the transistor is turned ON. This higher current peak increases the stress of the transistors. The efficiency factor η_{pp} is a dominant factor for the experimental prototypes described below.

2.3.5 Loss of the output matching network (η_{pm})

Non-ideal passive components in the output matching network also degrade the efficiency. For an impedance transformation from R_{load} to R_p , the Q factor of the impedance transformation, Q_m , is given by

$$Q_m = \sqrt{\frac{R_p}{R_{load}} - 1}. \quad (2-19)$$

It is assumed that the matching network consists of a series inductor L_m with Q factor of Q_L . Then the efficiency factor η_{pm} can be expressed by

$$\eta_{pm} = \frac{Q_L}{Q_L + Q_m}. \quad (2-20)$$

η_{pm} decreases with the increasing ratio of Q_m and Q_L . Therefore, smaller impedance transformation ratio and higher Q factor for the matching network components are helpful to reduce the loss.

2.3.6 Comparison of the simulated and calculated efficiency

In order to validate the results of the preceding analysis, circuit simulation was carried out assuming an idealized CMCD amplifier, utilizing harmonic balance simulation approach with the Agilent ADS simulator. The switches were modeled as simplified elements depicted in Fig. 2.8. They have a conductance that varies as a function of time between a value of 0 (for the switch in open position) and a value of $G=1/R_{ON}$ (for the switch in closed position) according to a simple linear time dependence shown in the figure.

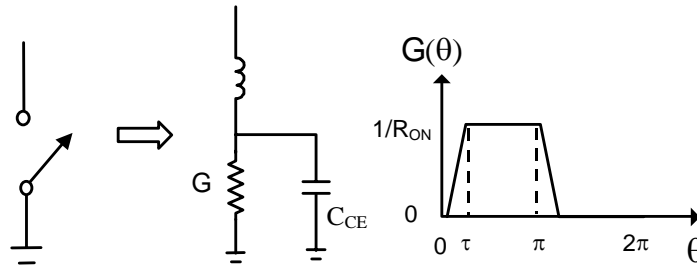


Figure 2.8: Switch model with parasitic reactance and finite transition time (τ).

Simulated efficiency for various CMCD designs, compared with the efficiency computed analytically by means of the preceding equations is shown in Table 2-1.

Parameter values were chosen to resemble the experimental circuits.

Table 2.1 Comparison of the total efficiency.

I_{CC} (A)	C_{CE} (F)	G' ($1/\Omega$)	Total efficiency (η_{CMCD})	
			Simulation	Calculation
0.15	0	0	83.3%	87.9%
0.15	4.5pF	0	82%	85.4%
0.15	4.5pF	0.0059	78.2%	80.7%

$V_{CC}=3.4V$, $Q=1.44$, $\tau=0.1\pi$, $R_{ON}=0.58\Omega$, $V_{OFFSET}=0.2V$ were used in simulations and calculations.

2.3.7 Additional design considerations and limitations of analysis

1) *Duty cycle of switching control waveform:* The efficiency is affected by the extent to which both switches in the CMCD amplifier are simultaneously on or partially on. The highest efficiency is obtained (via simulation) when the degree of overlap is minimized. This typically requires that the duty cycle for switch “on-time” is less than 50%, in order to account for the finite turn-on and turn-off time of the switches. For example, the highest collector efficiency is obtained for the waveform of Fig. 2.9.

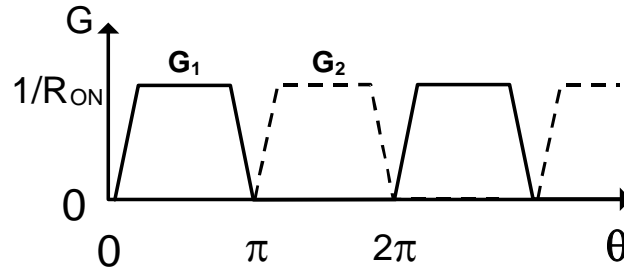


Figure 2.9: The switch control waveforms for the highest collector efficiency.

2) *Overlap of the conductance and switching voltage waveforms:* In the analysis of the non-zero transition time effect, for simplicity, the time varying conductance of the transistors is assumed to have 50% duty cycle and the current flowing through the transistor Q1 varies as shown in Fig. 2.5. However, the evaluation of the efficiency based on this assumption ignores the overlap of the voltage waveform and the time-varying conductance of the transistors. In practice, when there is substantial overlap between the transient of the switch conductance and the switch voltage, the current transient can be complex, and can display spiking behavior. Fig. 2.10 shows representative waveforms of the voltage (v_1) and the current (i_1) for substantial overlap. For short transition time, this loss can be neglected. The comparison of simulated and calculated results in Table I corresponds to non-zero transition time of 0.1π .

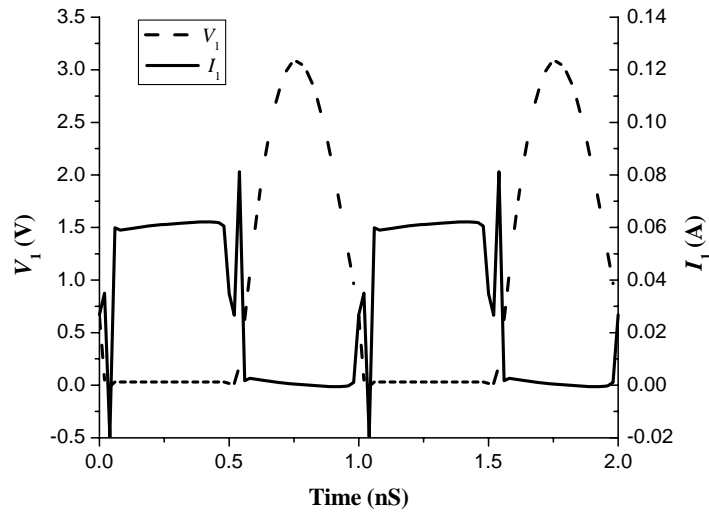


Figure 2.10: Simulated current waveform, showing spiking phenomena due to the overlap of voltage waveform and the time-varying conductance.

3) *Effect of series inductance*: As described in section II, the energy stored in parasitic switch inductance at the time that the switch is opened tends to be dissipated within the switch, and lost to the circuit. As a result, for highest efficiency in most circumstances the series inductance should be minimized. In cases where the switching transient is particularly long, however, leading to low values of efficiency factor η_{tt} (associated with transition time), it is found that adding inductance to the switch can improve efficiency. This results from the fact that the series inductance modifies the voltage across the switch, reducing its value during the current on-to-off transient, thereby lowering the switch loss (by more than the energy cost $1/2LI_{ON}^2$).

4) *Circuit symmetry*: In the analysis, the even harmonics are ignored because we assume the amplifier circuitry is symmetric. If this assumption fails, even harmonics will pass through the load and induce additional loss.

2.4 Experimental CMCD Amplifier Design

Current mode class-D amplifiers were implemented with GaInP/GaAs HBTs. Switching devices consisted of 80 emitter fingers of dimension $2\mu\text{m}\times 20\mu\text{m}$. Resistive ballasting was employed to prevent thermal runaway. Ground connections to the emitters were achieved with through-substrate vias. Harmonic balance simulation was performed by ADS circuit simulator. Fig. 2.11 shows the schematics of CMCD amplifier for simulation. A 180° input balun generates differential input signals and an output balun converts the balanced output to single-ended output signal. Input and output matching networks are applied for each transistor to increase tuning flexibility. Fig. 2.12 shows the simulated voltage and current waveforms. The voltage across the transistors shows the desired characteristic of zero voltage switching. The non-ideal current waveforms are due primarily to leakage currents through the parasitic capacitances of the transistors (and do not impact amplifier efficiency). If all passive components are assumed to be lossless, the simulated efficiency can reach 80%.

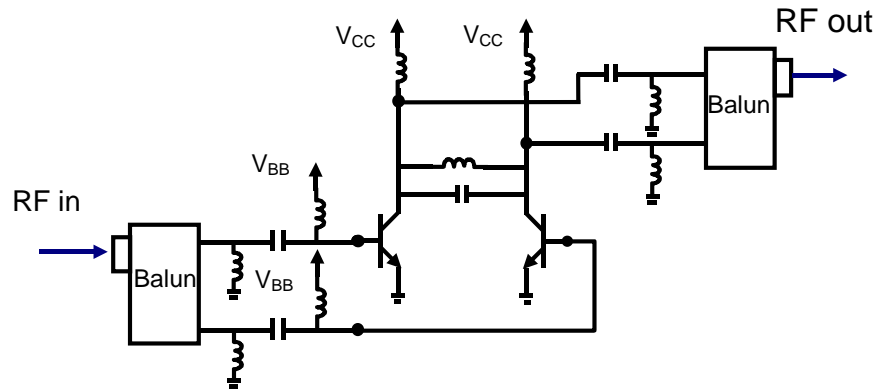


Figure 2.11: Schematic of the CMCD amplifier.

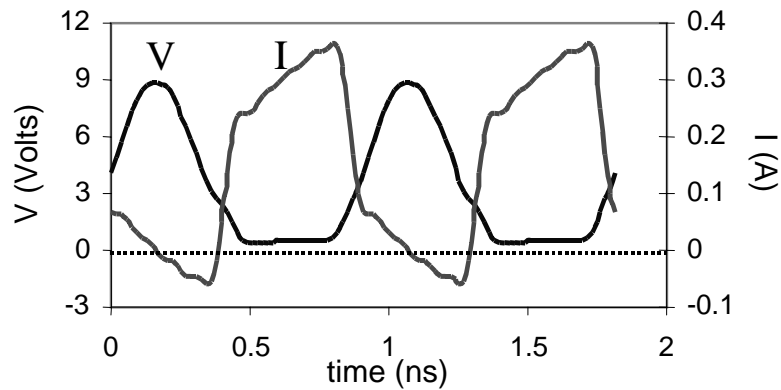


Figure 2.12: Simulated collector voltage and current waveform, showing desired characteristics of zero voltage switching.

Two CMCD amplifiers integrated with different LC resonator structures were fabricated and measured. Fig. 2.13 shows the CMCD amplifier chip layouts. The switching devices used in the two CMCD amplifiers are identical. For the chip marked as CMCD1 shown in Fig. 2.13 (a), the LC resonator comprises a bondwire inductor and a MIM capacitor. The capacitor is placed between two HBTs and two parallel bonding pads for making the bondwire inductor. The inductor consists of six Ω -shaped bondwire loops in parallel with spacing of 100 μm . The fabrication of the inductor is

reproducible with standard production wire-bonding techniques. This on-chip resonator minimizes the parasitic reactance and resistance along the LC path and uses the chip area more efficiently. For comparison, another amplifier chip CMCD2, as shown in Fig. 2.13 (b), uses a spiral inductor and a MIM capacitor to form the on-chip LC resonator.

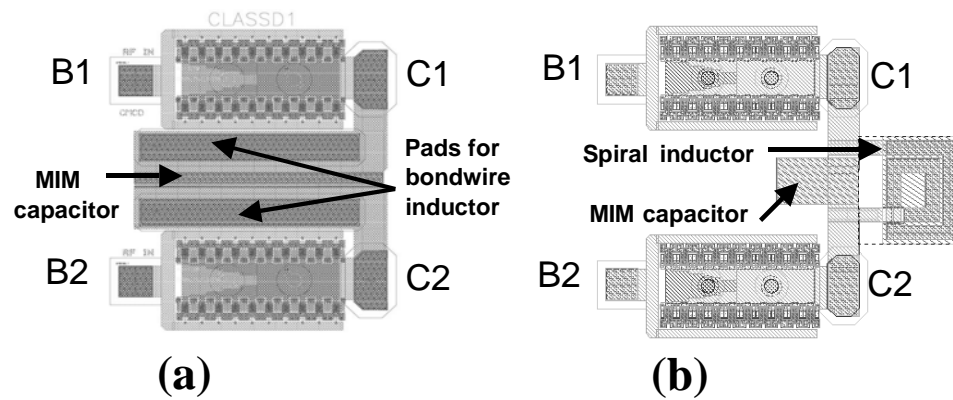


Figure 2.13: CMCD amplifier chip geometry (a) CMCD1: with pads for bondwire inductor. (b) CMCD2: with on-chip spiral inductor.

To evaluate the amplifier performance by the results of the preceding analysis, the required circuit parameters, R_{ON} , V_{offset} , C_{CE} , and τ were extracted from the transistor model. Q and Y' were obtained from the measurement. The parameters used in the calculation are listed in Table 1. If the loss factor η_{pp} (associated with the finite Q of the LC resonator) is not included, the efficiency η_{CMCD} is calculated to be 85.4%. With the factor of η_{pp} included, the efficiency η_{CMCD} of 80.7% can be estimated.

2.5 Measurement Results

Fig. 2.14 shows a photograph of the CMCD amplifier prototype. The input and output matching network were tuned for maximum efficiency. An Agilent ESG signal generator was used to generate an input signal sent to a commercial PA (Mini-circuits ZHL-2), which amplifies the power to the desired level. MA-COM 180° hybrids were used to convert the signal between single-ended and double-ended. The loss, including cable and broadband balun, is about 2dB between the input and output.

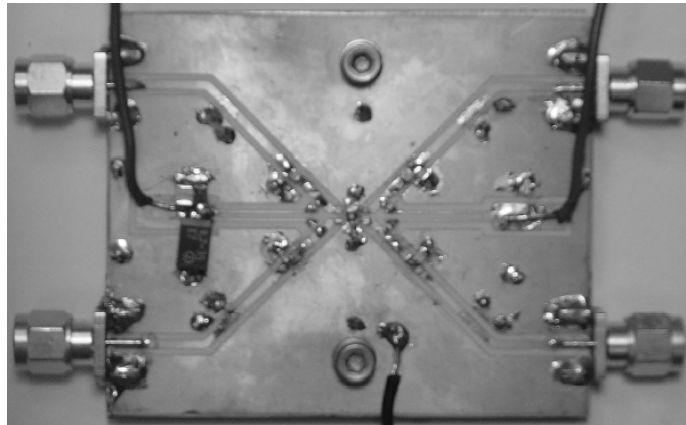


Figure 2.14: Photograph of the CMCD amplifier prototype. The overall amplifier employed external matching and baluns.

For both CMCD amplifier chips, the bases of the HBTs are biased to a turn-on voltage of 1.2V for operation as switches. The collector bias is set to 3.4V. Under these conditions, after calibrating the input and output loss of cable and balun, amplifier efficiency of the two CMCD amplifiers, CMCD1 and CMCD2, was measured against the input power, with results shown in Fig. 2.15 and Fig. 2.16, respectively. The collector efficiency and power-added efficiency (PAE) increase

dramatically with increasing the input power. When the input power is increased, the two transistors switch states with shorter transition times and the CMCD amplifier operates in switching mode. For CMCD1, collector efficiency reaches 78.5% at output power 29.5dBm (0.89W) with maximum PAE of 68.5% as shown in Fig. 2.15. For CMCD2, collector efficiency reaches 73.5% at output power 29.1dBm (0.81W) with maximum PAE of 64.6% as shown in Fig. 2.16. Examining Fig. 2.17, the CMCD1 amplifier shows a wide operating bandwidth. For collector efficiency higher than 70%, it has bandwidth of 300MHz. The measurement results show reasonable efficiency characteristics of CMCD amplifiers with different inductor implementation.

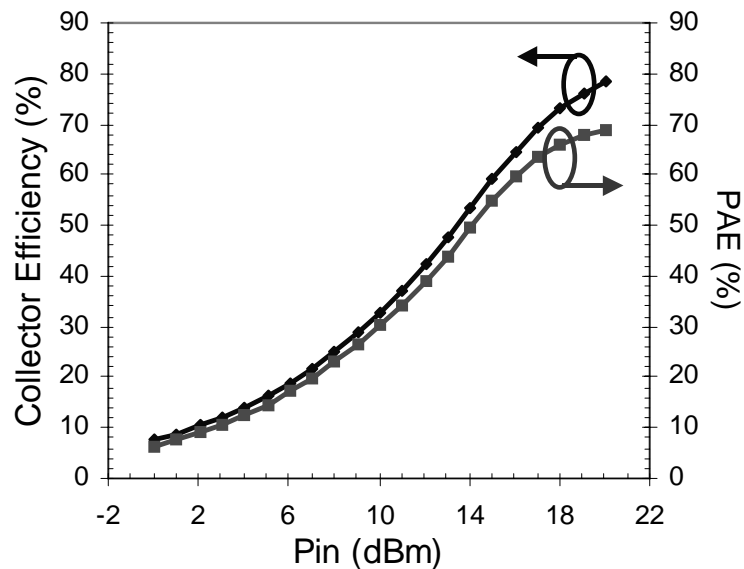


Figure 2.15: Measured efficiency vs. input power for CMCD1, showing collector efficiency of 78.5% at maximum PAE of 68.5%.

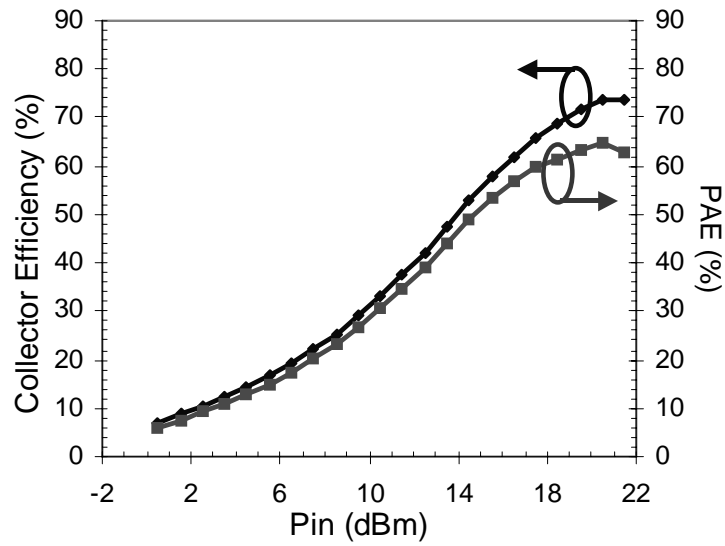


Figure 2.16: Measured efficiency vs. input power for CMCD2, showing collector efficiency of 73.5% at maximum PAE of 64.6%.

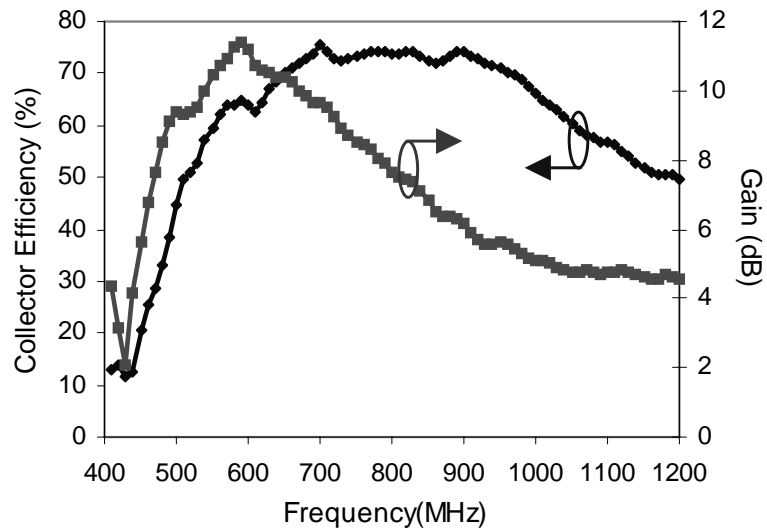


Figure 2.17: Measured collector efficiency, gain vs. frequency of CMCD1, showing the operation bandwidth of 300MHz for collector efficiency greater than 70%.

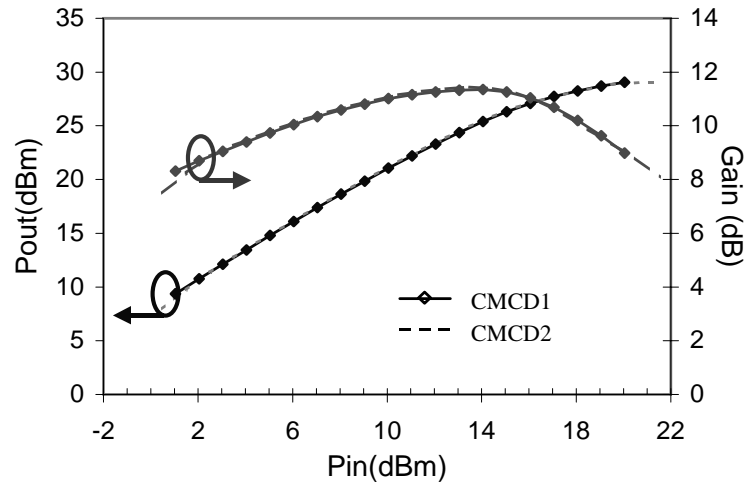


Figure 2.18: Measured Gain and Pout vs. input power.

The GaAs HBTs each have emitter area of $3200\mu\text{m}^2$. The peak current density at maximum power output is $0.11\text{ mA}/\mu\text{m}^2$. Fig. 2.18 shows the gain and output power of the CMCD amplifiers, which is nearly identical for the two structures. Due to gain reduction at high drive level, the PAE starts to drop when output power approaches its maximum value. One of the possible reasons for limited gain is saturation charge. The gain can be improved by superior matching, by suppressing saturation charge storage and by reducing the ballasting resistance, yielding higher PAE.

2.6 Conclusion

In this chapter, design considerations of the current-mode class-D amplifier have been discussed analytically. Based on the analytical results, the efficiency of the CMCD amplifier can be estimated from the transistor and circuit parameters, providing a useful guide for circuit design. Experimental CMCD amplifiers with

different integrated resonator structures have been demonstrated to achieve high efficiency. An amplifier with a bondwire inductor can reach a collector efficiency of 78.5% at an output power of 29.5dBm (0.89W) with a maximum PAE of 68.5%. This current mode class-D amplifier is suitable for wireless systems with constant envelope modulation. For example, by using larger transistors and adjusting the matching networks to achieve higher output power, the CMCD amplifiers have the potential for use in GSM applications.

To provide the required linearity, current-mode class-D amplifiers were considered to combine with modulated digital driving techniques such as delta-sigma modulation. However, two issues were coming along. First, the zero-voltage switching condition is no longer valid because the signals are non-periodic. Second, the RF chokes in CMCD amplifiers were utilized to supply constant current. When both bottom devices are OFF, a large voltage spike will be induced which may destroy the devices. These effects limit the usage of current-mode class-D amplifiers combining with digital driving techniques. Instead of current-switching configuration, voltage-switching configuration is considered the most suitable to combine with digital driving technique to achieve the linearity requirement which are further discussed in the following chapters.

2.7 Acknowledgements

The authors would like to thank Kenneth Weller of Skyworks Solutions, Inc. for access to industry resource and GaAs HBT fabrication.

The material in chapter 2 is as it appears in “Design of high efficiency current-mode class-D amplifier for wireless handsets,” T.-P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp.144-151, Jan. 2005. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

2.8 Reference

- [1] H. L. Krauss, C. W. Bostian, and F. H. Rabb, *Solid State Radio Engineering*. NewYork: Wiley, 1980.
- [2] M. Albulet, *RF Power Amplifiers*. Atlanta: Noble Publishing, 2001.
- [3] S. C. Cripps, *RF power amplifiers for wireless communications*, Boston: Artech House, 1999.
- [4] S. El-Hamamsy, “Design of high-efficiency RF class D power amplifier,” *IEEE Trans. Power Electron.*, vol. 9, pp. 297–308, May 1994.
- [5] W. J. Chudobiak, D. F. Pace, “Frequency and power limitations of class-D transistor amplifiers,” *IEEE J. Solid State Circuits*, vol. SC-4, no. 1, pp. 25–37, February 1969
- [6] N. O. Sokal and A. D. Sokal, “Class E-A new class of high efficiency tuned single-ended power amplifiers,” *IEEE J. Solid State Circuits*, vol. SC-10, pp. 168–176, June 1975.

- [7] F. H. Rabb, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 725–735, Dec. 1977
- [8] F. H. Rabb and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE J. Solid State Circuits*, vol. SC-13, pp. 912–914, Dec. 1978.
- [9] M. Kazimierczuk, "Class E tuned power amplifier with shunt inductor," *IEEE J. Solid State Circuits*, vol. SC-16, pp. 2–7, Feb. 1981.
- [10] M. Kazimierczuk and K. Puczek, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 149–159, Feb. 1987.
- [11] D. K. Choi, S. I. Long, "A physically based analytical model of FET class-E power amplifiers- Designing for maximum PAE," *IEEE Trans. Microwave Theory & Tech.*, vol. 47, no. 9, pp. 1712-1720, June 2003.
- [12] G. K. Wong and S. I. Long, "An 800 MHz HBT class-E amplifier with 74% PAE at 3.0 Volts for GMSK," in *IEEE GaAs IC Symp. Dig.*, Oct. 1999, pp. 299–302.
- [13] H. Kobayashi, J. M. Hinrichs and P. M. Asbeck, "Current-mode class-D power amplifiers for high efficiency RF application," *IEEE Trans. Microwave Theory & Tech.*, vol. 49, no. 12, pp. 2480-2485, December 2001.
- [14] A. Long, J. Yao, and S. I. Long, "A 13 W current mode class D high efficiency 1 GHz power amplifier" *2002 45th Midwest Symp. on Circuits and Systems Dig.*, vol. 1, pp. 33-36, Aug., 2002.
- [15] S. D. Kee, I. Aoki, and D. Rutledge, "7-MHz, 1.1-kW demonstration of the new E/F_{2,odd} switching amplifier class," *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 1505–1508.
- [16] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 51, no. 6, pp. 1677-1690, June 2003.
- [17] F. Bohn, S. D. Kee, and A. Hajimiri, "Demonstration of a harmonic-tuned class E/F_{odd} dual band power amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1631–1634.
- [18] T. P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "High efficiency current-mode class-D amplifier with integrated resonator," in

IEEE MTT-S Int. Microwave Symp. Dig., Fort Worth, TX, June 2004, pp. 2035-2038.

Chapter 3

Voltage-Mode Class-D Power Amplifiers

3.1 Introduction

Although current mode class-D power amplifiers, as discussed in the last chapter, can improve the amplifier efficiency by reducing the output capacitance loss, they have a major limitation. The high efficiency only occurs at maximum output power and correspondingly maximum input power such that the transistors are driven hard enough for rapid switchings. In the power back-off region, amplifier efficiency drops significantly due to the transition loss. Therefore, the CMCD amplifiers are only directly suitable to constant envelope modulation systems such as frequency modulation (FM) system or GSM system. Because of the non-linear operation, the amplifiers need to be further combined with other techniques such as an outphasing system or a digital RF transmitter system to achieve the required linearity such that they can be used in a non-constant envelope modulation system. In such systems, the amplifiers experience time-varying load impedance, which tends to degrade the efficiency of CMCD amplifiers.

With idealized switching operation, a voltage mode class-D (VMCD) amplifier can be approximated as a voltage source. This enables efficient operation with different load conditions. This important feature makes voltage mode class-D

amplifiers very suitable to use in various linear amplifier system techniques such as outphasing amplifier systems or digital RF systems for non-constant envelope modulation systems. The applications of voltage mode class-D amplifier in Outphasing and digital RF transmitter systems are discussed in Chapter 4 and Chapter 5, respectively, for CDMA systems. In this chapter, the design of voltage mode class-D amplifier is discussed, focusing on loss analysis and experimental demonstration.

There are many efficiency degrading sources in voltage mode class-D amplifiers such as output capacitance loss, shoot-through current loss, transition loss and ON- state resistance loss. In this chapter, the factors degrading the voltage mode class-D amplifier efficiency are discussed analytically. The proposed amplifier model allows efficiency prediction of voltage mode class-D amplifiers, indicating the loss mechanisms in relation to the output power. The analysis results help to understand the issues of using VMCD amplifier in outphasing system and digital RF transmitter system.

A prototype H-bridge voltage mode class-D amplifier applying the shoot-through current technique was also designed and demonstrated. The H-bridge VMCD amplifier achieves a drain efficiency of 62% at 800MHz with an output power of 21dBm. In the section 3.2, the basics of VMCD amplifier operation are described. Section 3.3 shows the design and measurement results of the prototype VMCD amplifier with shoot-through current suppression technique. The analysis of efficiency in non-ideal VMCD amplifiers is shown in section 3.4.

3.2 Operation of Voltage Mode Class-D Amplifiers

3.2.1 Idealized Operation of Voltage mode Class-D Amplifiers

Fig. 3.1 shows a voltage mode class-D amplifier with two complementary FETs and a series resonator. The two transistors are operated as switches. Fig. 3.2 illustrates the switched voltage V_2 , the load current I_{load} , and the currents flowing through the transistors I_1 and I_2 . The switched voltage waveform V_2 defined by the supply voltage V_{dd} is applied to the resonator, which exhibits a high impedance at all frequencies except for the resonant frequency, thus removing the out-of-band signals such as harmonics and quantization noise.

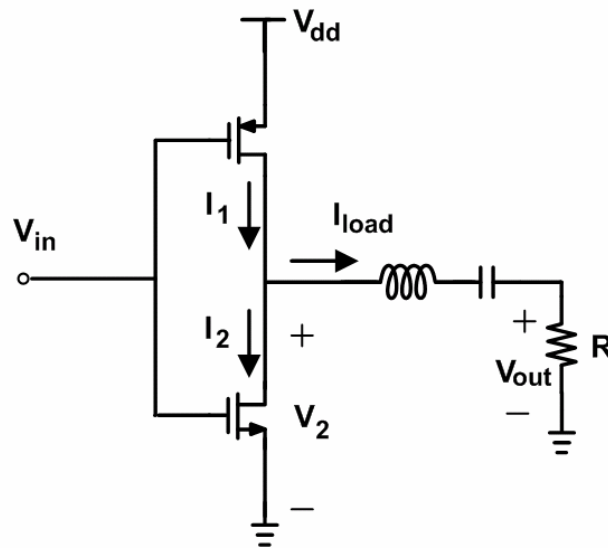


Figure 3.1: A voltage mode class-D amplifier consisting of two complementary FETs and a series resonator

The switched voltage can be written as

$$V_2(\theta) = \begin{cases} V_{dd}, & 0 \leq \theta \leq \pi \\ 0, & \pi \leq \theta \leq 2\pi \end{cases} \quad (3-1)$$

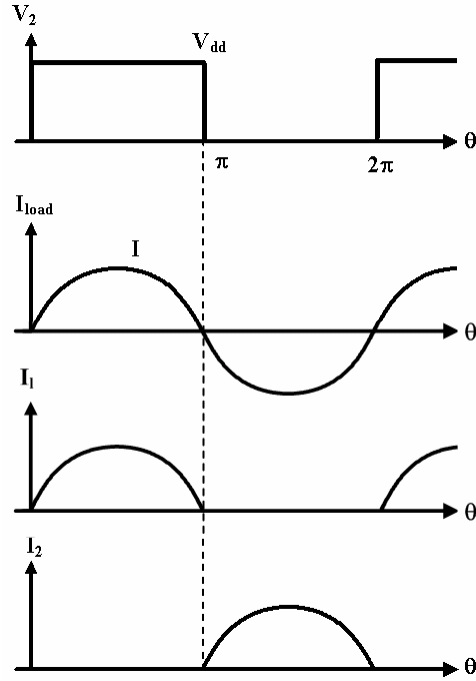


Figure 3.2: The voltage and current waveforms of the idealized voltage mode class-D amplifier

where V_{dd} is the supply voltage. Because of the resonator, the output voltage V_{out} is the fundamental component of V_2 . By using Fourier analysis, the output voltage waveform, $V_{out}(\theta)$, can be written as

$$V_{out}(\theta) = \frac{2}{\pi} V_{dd} \cdot \sin(\theta) \quad (3-2)$$

The load current is therefore also sinusoidal and can be expressed as

$$I_{load}(\theta) = I \cdot \sin(\theta) = \frac{2}{\pi} \frac{V_{dd}}{R} \cdot \sin(\theta) \quad (3-3)$$

where R is the load resistance. From (3-2) and (3-3), the output power can be obtained as

$$P_{out} = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \quad (3-4)$$

The DC current from the supply is the DC component of the current I_I which can be written as

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_1(\theta) d\theta = \frac{2}{\pi^2} \frac{V_{dd}}{R} \quad (3-5)$$

Therefore, the DC power consumption can be obtained as

$$P_{dc} = V_{dd} I_{dc} = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \quad (3-6)$$

From (3-4) and (3-6), it is noted that all the power from the supply (P_{dc}) goes to the load (P_{out}). Since there is no out-of-band-frequency component at the output due to the resonator, no DC power is dissipated at those frequencies.

3.2.2 Reactive Load

The idealized operation assumes the load impedance is pure resistive R such that the sinusoidal load current I_{load} is in-phase with the switched voltage V_2 . When using voltage mode class-D amplifiers in outphasing amplifier systems, the load impedance of the voltage mode class-D amplifiers usually is not pure resistive. It becomes $Z_{load} = R + jX$ and the load current I_{load} can be written as

$$I_{load} = \frac{2}{\pi} \frac{V_{dd}}{|Z_{load}|} \sin \left[\theta + \arctan \left(\frac{X}{R} \right) \right] \quad (3-7)$$

where X is the reactance of the load impedance.

Fig. 3.3 shows the voltage and current waveforms of a voltage mode class-D amplifier with a reactive load. The sinusoidal load current is no longer in-phase with the switched voltage waveform V_2 such that active devices have to supply reverse current in a certain period, as indicated in Fig. 3.3. This suggests transistors capable of conducting reverse currents such as FETs can be used without additional components as long as the reverse current flows through the channel instead of the substrate diode. For the transistors which cannot conduct reverse current such as bipolar junction transistors (BJT), diodes are required to protect the transistors and supply the reverse current .

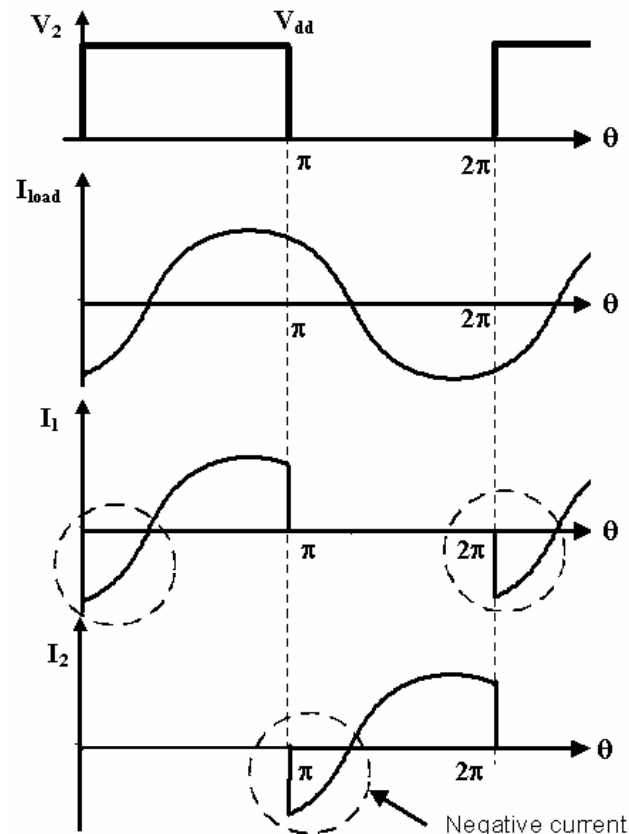


Figure 3.3: The voltage and current waveforms of the idealized voltage mode class-D with a reactive load.

Through the same derivation procedures in section 3.2.1, we can obtain the output power and the DC power of the VMCD amplifier with reactive load as

$$P_{out} = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \rho^2, \text{ where } \rho = \frac{R}{|Z_{load}|} < 1 \quad (3-8)$$

$$P_{dc} = V_{dd} I_{dc} = V_{dd} \cdot \frac{1}{2\pi} \int_0^\pi I_{load}(\theta) d\theta = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \rho^2 \quad (3-9)$$

Because of the amplitude of the load current is reduced, the output power also drops as shown in (3-8). However, with lower DC power consumption, the amplifier efficiency is unaffected.

Note that, the currents flowing through the devices need to jump at switching transitions. These jumps cause loss of the energy stored in parasitic inductance ($\frac{1}{2}LI^2$) associated with the series inductance of the transistor. This loss is not a concern in the amplifier with pure resistive load because of the zero switching current.

3.2.3 Duty Ratio

Thus far, we have been considering the voltage mode class-D amplifier driven by periodic signals with 50% duty ratio. When driving signals of the amplifier have non-50% duty ratio, the switched voltage V_2 , the load current and the current flowing through the devices are shown in Figure 3.4.

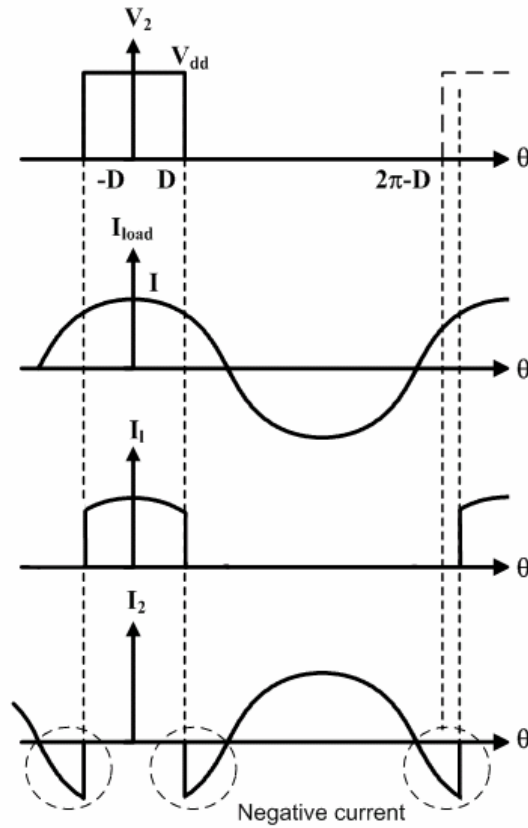


Figure 3.4: The voltage and current waveforms of the idealized voltage mode class-D driven by the signals with non-50% duty ratio.

The switched voltage V_2 can be expressed as

$$V_2(\theta) = \begin{cases} V_{dd}, & -D \leq \theta \leq D \\ 0, & D \leq \theta \leq 2\pi - D \end{cases} \quad (3-10)$$

By using Fourier analysis, the output voltage waveform, $V_{out}(\theta)$, can be written

as

$$V_{out}(\theta) = \left[\frac{2}{\pi} V_{dd} \cdot \sin(D) \right] \cos \theta \quad (3-11)$$

and the output power

$$P_{out} = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \sin^2(D) = P_{out,50\%} \cdot \sin^2(D) \quad (3-12)$$

where $P_{out,50\%}$ is the output power for $D=0.5\pi$, the 50% duty ratio case.

The DC power can be obtained by

$$P_{dc} = V_{dd} I_{dc} = V_{dd} \cdot \frac{1}{2\pi} \int_{-D}^D I_{load}(\theta) d\theta = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \sin^2(D) \quad (3-13)$$

Therefore, the amplifier efficiency is unaffected but the output power is lower. As shown in Fig. 3.4, in this case, the negative current flowing also exists when the VMCD amplifier is driven by non-50% duty ratio signals.

From section 3.2.2 and 3.2.3, we have shown that an idealized voltage mode class-D amplifier can maintain high efficiency when the load impedance changes as well as when the driving signals have non-50% duty ratio. This feature makes the VMCD amplifier in principle very suitable to linearized amplifier applications (Chapter 4, 5).

3.3 CMOS H-Bridge Class-D Amplifier

Implementing the voltage mode class-D amplifier in CMOS technology has the advantage of low cost, ease of integration, and simple circuitry. The switching transistors can conduct the reverse currents without requiring parallel diodes.

In practice, there are many sources degrading the efficiency of voltage mode class-D amplifiers such as shoot-through current loss, capacitance loss, transition loss and ON- state resistance loss. Among those losses, the shoot-through current loss can

be suppressed by using a circuit technique. After discussing the shoot through current loss and the suppression technique, the design of a prototype CMOS class-D amplifier is shown.

3.3.1 Shoot-Through Current and Suppression Technique

Because of finite transition speed of the transistors, there is generally a short period of time when both PMOS and NMOS transistors are ON during the transitions, resulting in a low resistance between power supply and ground. For example, for the circuit in Fig. 3.1, when the driving voltage V_{in} has a value which is higher than the threshold voltage of the NMOS and lower than the threshold voltage of the PMOS, both PMOS and NMOS are ON. Therefore, as shown in Fig. 3.5(a), a large current (known as shoot-through current) may be induced which can cause significant energy loss as well as potentially damage to the devices.

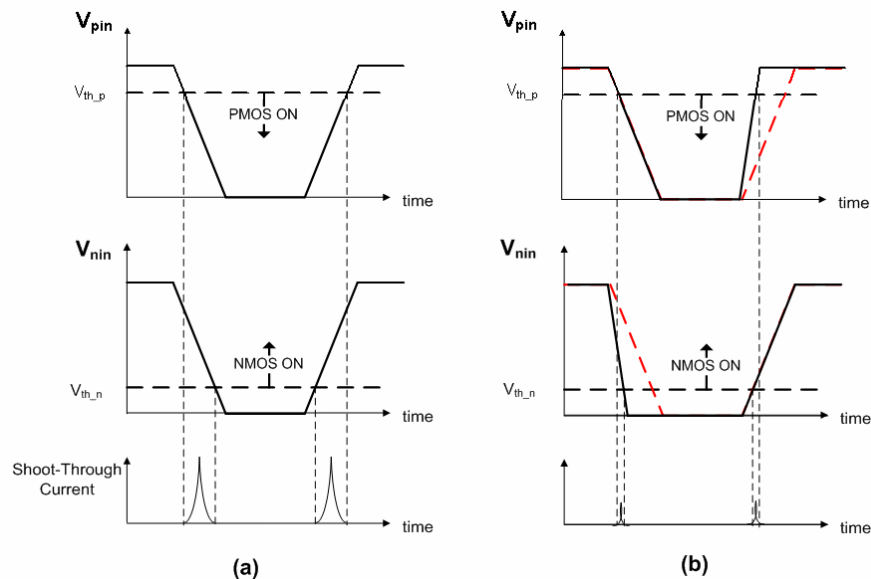


Figure 3.5: The voltage and current waveforms of the voltage mode class-D amplifier (a) with shoot-through current (b) with shoot-through current suppression technique.

To minimize this loss, the PMOS and NMOS were designed to have different driving circuits, as shown in Fig. 3.6(b), such that the transition of PMOS and NMOS can be controlled respectively. The overlap of the turn ON time between the PMOS and the NMOS during the transition can be minimized by modifying the pull-up and pull-down device size ratio of each driver stage. For example, the p-channel device M_{PP1} in the driver is used to turn-off the for the PMOS switching device M_{P1} . By increasing the size of M_{PP1} , M_{P1} can be turn off faster as shown in Fig. 3.5(b). Same strategy can be applied to turn off M_{N1} faster by increasing the size of M_{NN1} NMOS.

To be used in a digital RF transmitter with three-level digital driving signals which we will discuss in Chapter 5, the voltage mode class-D amplifier is configured in an H-bridge fashion as shown in Fig. 3.6. The amplifier consists of two class-D amplifiers which drive the load differentially.

The direct approach is as shown in Fig. 3.6(a); the switching stage is driven by a driver stage in a cascade configuration. This conventional driving method suffers from the shoot-through current loss. In Fig. 3.6(b), the shoot-through current is suppressed by the modified driving strategy.

The simulations of two configurations in Fig. 3.6 were performed in Agilent ADS for the efficiency and power comparison. The transistor model was provided by the foundry [10]. The transistor sizes of the NMOS and PMOS at the switching stage were 1.6mm and 4mm which were chosen such that they have similar current handling capability. The pull-up/pull-down device size ratio of the drivers, M_{NP1}/M_{NN1} and M_{PP1}/M_{PN1} were 1:1 and 5:1, respectively. The power supply voltage was 2V. The

simulated results are as shown in Table 3.1. The simulated results do not include the loss due to the parasitics of the matching network, the biasing and the power combining networks. The power added efficiency (PAE) is increasing by 15% and 13% through the modified driver when the driving signals have 50% and 30% duty ratio, respectively. The physical mechanisms that determine loss of efficiency will be discussed below.

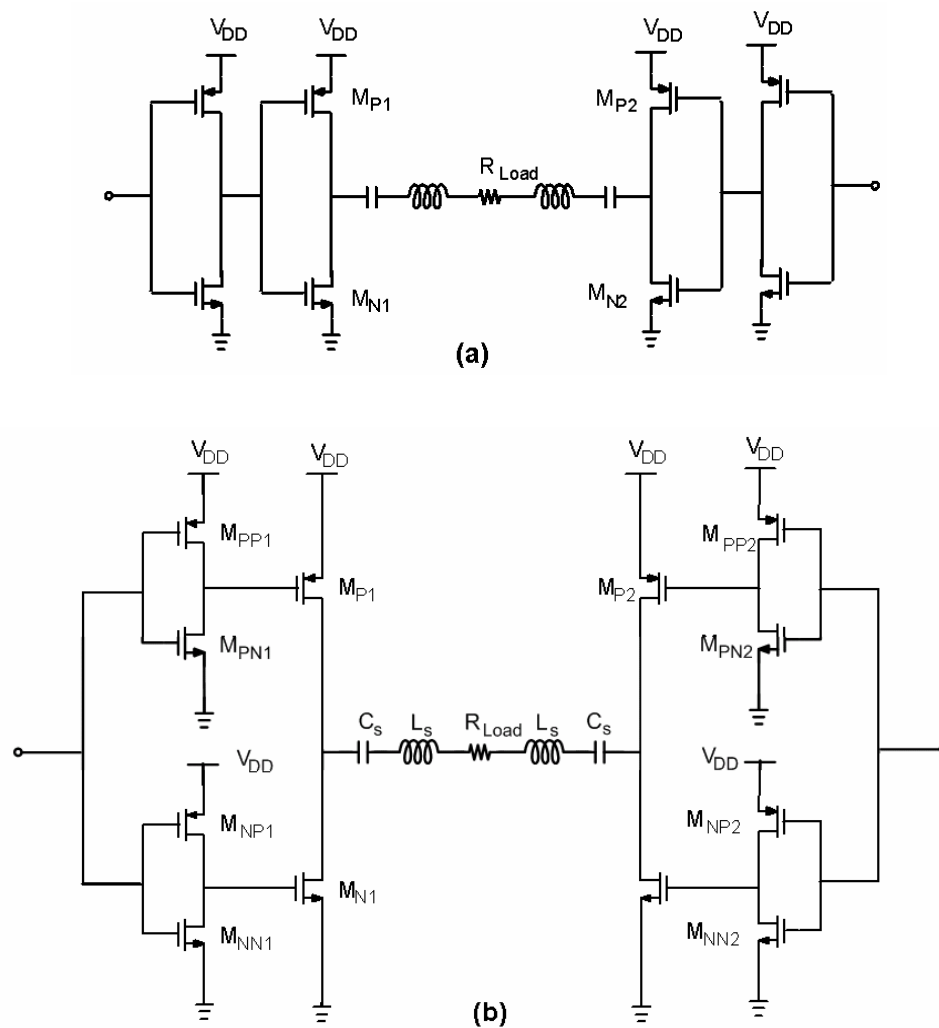


Figure 3.6: The voltage mode class-D amplifier driven by (a) the direct approach (b) the modified driver stage for shoot-through current suppression.

Table 3.1 Efficiency and power comparison of the conventional and the modified driving approach.

	Direct Approach		Modified Driver	
	50%	30%	50%	30%
Duty Ratio	50%	30%	50%	30%
Pdc_driver	86mW	94mW	131mW	138mW
Pdc_switch	453mW	331mW	341mW	227mW
Output power	340mW	207mW	340mW	201mW
PAE	63%	49%	72%	55%

3.3.2 Implementation of CMOS H-Bridge VMCD Amplifier

An H-bridge Class-D amplifier with shoot-through current suppression was designed and implemented with 0.18 μ m CMOS devices, as part of the Jazz BiCMOS technology. The chip size is about 0.5mm \times 0.5mm, as shown in Fig. 3.7. The sizes of the devices are the same as the ones used in the simulations. The bias of the driver and the switch stage are separated to monitor the power consumption respectively. Along with the DC bias lines, decoupling capacitors were implemented with a capacitance of 35pF at both driver and switching stages. These large on-chip capacitors minimize the impedance looking into the power supply, avoiding any voltage spike due to the bondwire inductance. Fig. 3.8 and Fig. 3.9 show the prototype H-bridge amplifier which consists of two Class-D amplifiers, two quarter-wave transmission line and a power combiner. The transmission line transforms the impedance seen by the amplifier from 25 Ω to 4 Ω . With the resonator following each amplifier, the

differential mode impedance shows high impedance at out-of-band frequencies except for the resonant frequency, as illustrated in Fig. 3.10. This feature avoids energy loss at out-of-band frequencies such as harmonics.

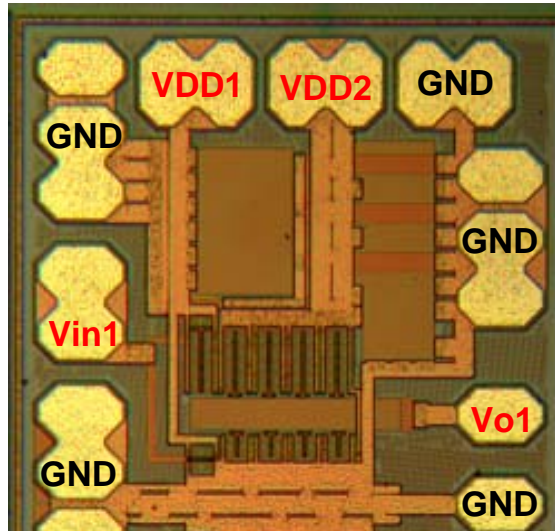


Figure 3.7: The voltage mode class-D amplifier chip.

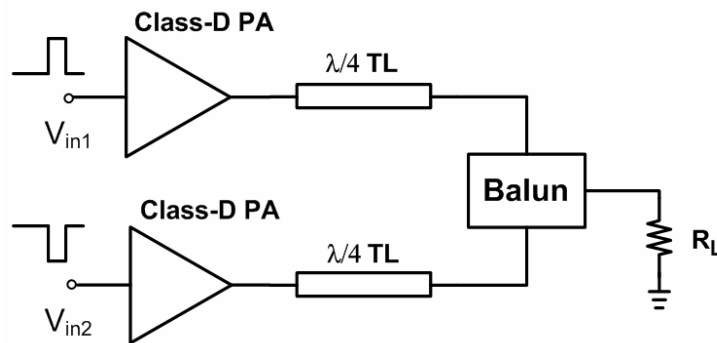


Figure 3.8: Schematic of the prototype H-bridge class-D power amplifier consisting of two class-D PA, two quarter-wave transmission lines and a balun.



Figure 3.9: The prototype H-bridge class-D power amplifier.

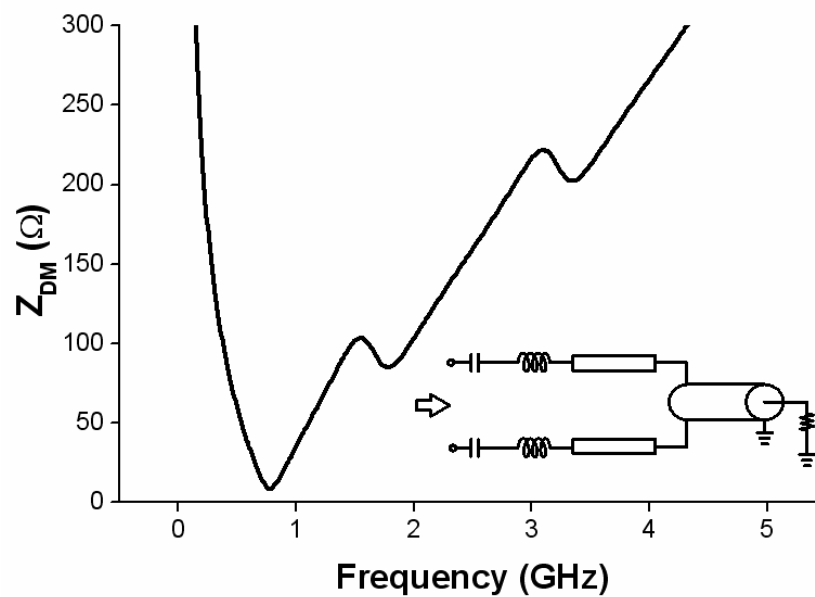


Figure 3.10: The frequency response of the differential mode impedance of the combining network.

3.3.3 Measurement Results of the CMOS H-bridge VMCD Amplifier

The drain efficiency and dc currents of the H-bridge Class-D amplifier were measured with periodic driving signals. Fig. 3.11 shows that the maximum current

occurs at the desired frequency (800MHz) and drops significantly at out-of-band frequencies, as expected from inclusion of the series resonators. Fig. 3.12 illustrates the drain efficiency as a function of frequency. Also shown is the efficiency simulated for the amplifier using Agilent ADS modeling of the transistors and matching components. The PAE and output power are shown in Fig. 3.13. The peak drain efficiency, PAE and output power were 62%, 45% and 21 dBm, respectively. Here the drain efficiency considers the switching stage power consumption only. The PAE quoted here considers the total DC power consumed by both driver and switching stage (since the input power to the driver is negligible in an integrated CMOS system).

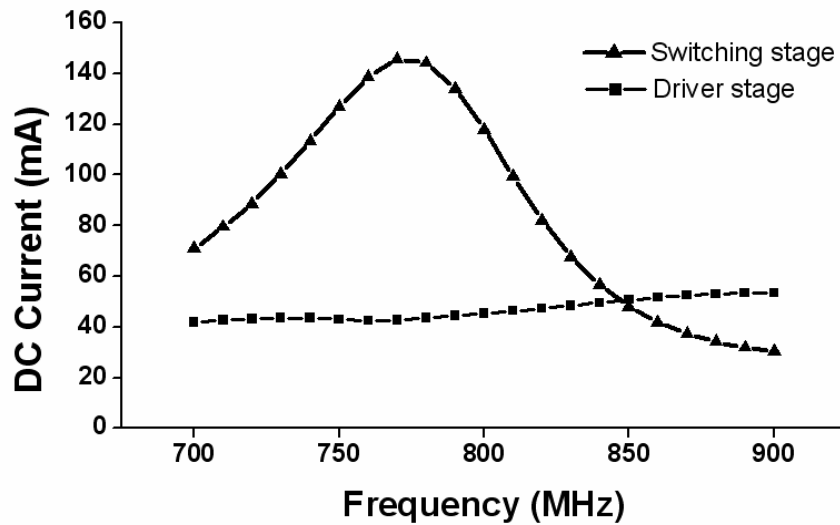


Figure 3.11: Measured DC currents for switch and driver stage as a function of frequency.

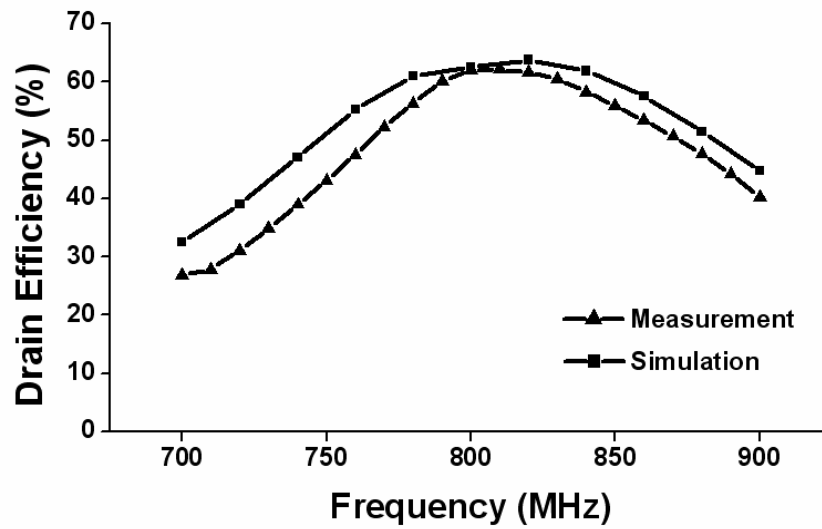


Figure 3.12: Measured drain efficiency as a function of frequency.

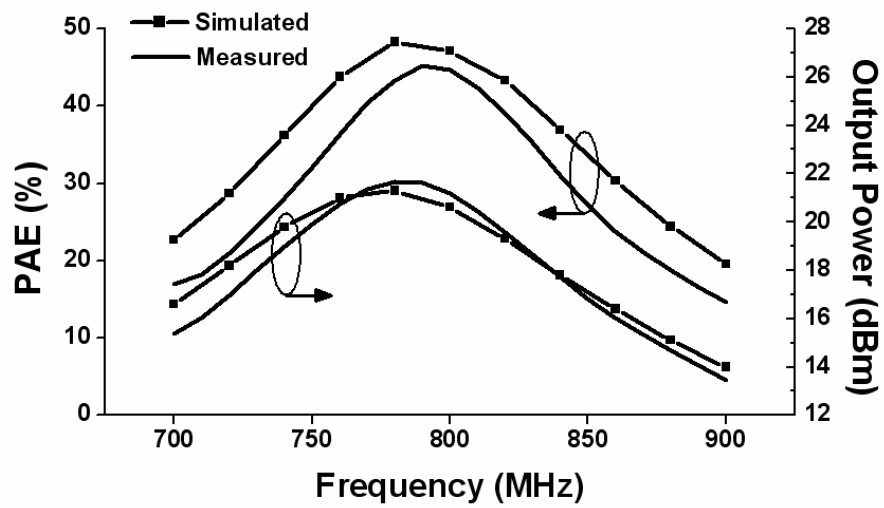


Figure 3.13: Measured PAE and Pout as a function of frequency.

3.4 Loss Analysis and Efficiency Estimation for Non-ideal Operation

In addition to the shoot-through current loss, other possible loss sources can also degrade the efficiency of voltage mode class-D amplifiers, including ON-state resistance, non-zero transition time and output capacitance loss.

An analytical model is proposed here to estimate the amplifier efficiency in relation to the output power for the amplifiers driven by the signals with different duty ratios. Using the modified driver configuration, the shoot-through current loss is minimized and not included in the model. The analysis begins with the half-bridge class-D amplifier, as shown in Fig. 3.14. We first consider operation with 50% duty ratio inputs.

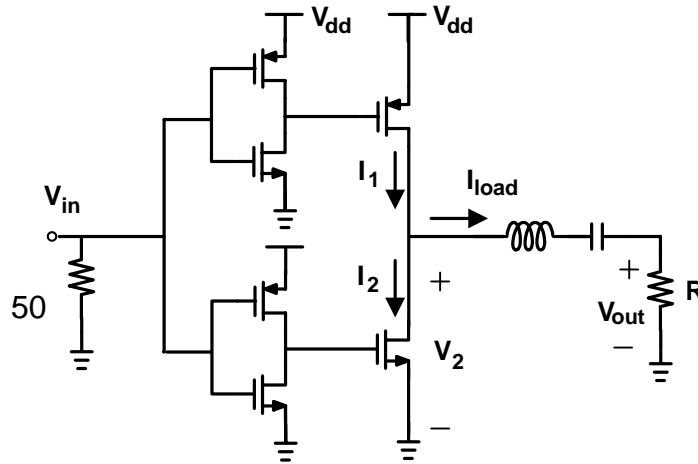


Figure 3.14: Single VMCD amplifier with modified driver stage

As shown in Fig. 3.15, the time domain voltage waveform V_2 of Fig. 3.14 differs from the V_2 in Fig. 3.4, considering the ON-state resistance and non-zero transition time. $V_2(\theta)$ can be expressed as

$$V_2(\theta) = \begin{cases} \frac{\theta}{\tau} V_{dd} - I \cdot R_{on} \cdot \cos \theta, & -(D + \tau) \leq \theta \leq -D \\ V_{dd} - I \cdot R_{on} \cdot \cos \theta, & -D \leq \theta \leq D \\ V_{dd} \left(1 - \frac{\theta - D}{\tau}\right) - I \cdot R_{on} \cdot \cos \theta, & D \leq \theta \leq D + \tau \\ -I \cdot R_{on} \cdot \cos \theta, & (D + \tau) \leq \theta \leq 2\pi - D \end{cases} \quad (3-14)$$

Because of the high Q series resonator, the load voltage $V_{out}(\theta)$ is only the fundamental Fourier component of $V_2(\theta)$. By using Fourier analysis, the output voltage waveform, $V_{out}(\theta)$, can be written as

$$V_{out}(\theta) = \left[\frac{4}{\pi} V_{dd} \cdot \sin(D) \frac{\sin(\tau/2)}{\tau} - I \cdot R_{on} \right] \cos \theta \quad (3-15)$$

where V_{dd} is the DC supply voltage; D defines the ON time duty ratio in radians; τ is the ON-OFF transition time in radians (assumed to be symmetric); R_{on} is the ON-state resistance and I is the amplitude of the output current (I_{load}). I_{load} is a function of the output voltage at the load, i.e.

$$I_{load}(\theta) = I \cos(\theta) = \frac{V_{out}(\theta)}{R} \quad (3-16)$$

Therefore, I can be written from (3-15) and (3-16) as

$$I = \frac{4}{\pi} \frac{V_{dd}}{R + R_{on}} \cdot \sin(D) \frac{\sin(\tau/2)}{\tau} \quad (3-17)$$

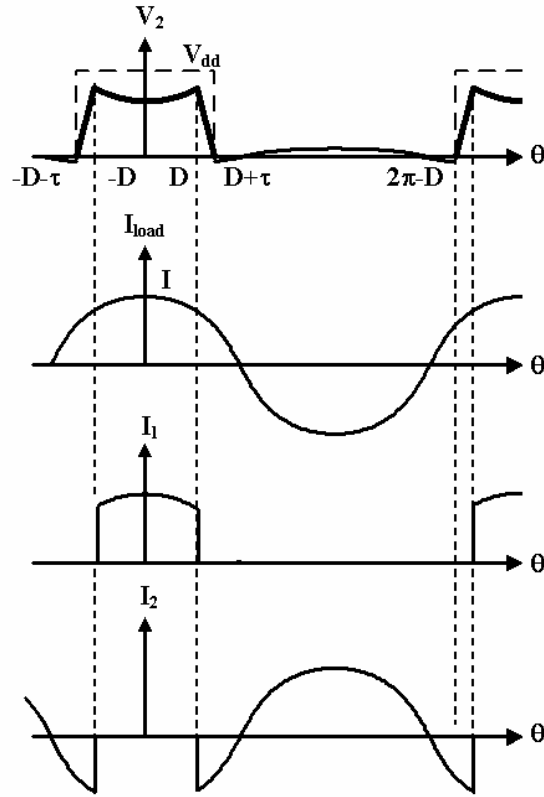


Fig. 3.15: Class-D amplifier voltage and current waveforms for efficiency estimation

From (3-17), the amplifier output power can be found to be

$$P_{out} = \frac{1}{2} I^2 R = \frac{8}{\pi^2} \frac{V_{dd}^2}{R} \left(\frac{R}{R + R_{on}} \right)^2 \cdot \sin^2(D) \frac{\sin^2(\tau/2)}{\tau^2} \quad (3-18)$$

From (3-18), the amplifier output power decreases with increasing R_{on} and transition time. For the amplifier driven by 50% duty-ratio signals ($D=\pi/2$) with ideal turn-on resistance ($R_{on}=0$) and transition time ($\tau=0$), the amplifier generates the maximum output power and equation (3-18) can be simplified as

$$P_{out} = \frac{2}{\pi^2} \frac{V_{dd}^2}{R} \quad (3-19)$$

To calculate the amplifier efficiency, the DC power consumption can be estimated by

$$P_{dc} = P_{out} + P_{Ron} + P_{overlap} + P_{capacitance} \quad (3-20)$$

where P_{out} is the output power; P_{Ron} is the loss due to the ON-state resistance of the devices; $P_{overlap}$ is the loss associated with transitions and P_{cap} is the loss due to the output capacitance of the devices. For high efficiency amplifiers, these contributions are additive to a close approximation.

The first two terms in (3-20), P_{out} and P_{Ron} , can be obtained by deriving the DC term of the current I_l , which corresponds to the current flowing through the p-channel device assuming zero transition time and zero output capacitance. Total power for P_{out} and P_{Ron} can be written as

$$P_{out} + P_{Ron} = V_{dd} \cdot \frac{1}{\pi} \int_0^D I \cdot \cos \theta d\theta = V_{dd} \cdot I \sin D \quad (3-21)$$

$P_{overlap}$ comes from the overlap of voltage and current waveform across the device during the transition. The shoot-through current loss is minimized and ignored here. I_{on} is defined as the current level when the transition occurs. Fig. 3.16 shows the overlap voltage and current waveforms across the p-channel transistor during the transition. The loss associated with the overlap can be written as

$$P_{overlap} = 2 \cdot \frac{1}{\pi} \int_0^{\tau} V_{dd} \cdot I_{on} \frac{\tau\theta - \theta^2}{\tau^2} d\theta = \frac{V_{dd}}{3\pi} \cdot I_{on} \cdot \tau \quad (3-22)$$

where $I_{on} = I \cdot \cos D$.

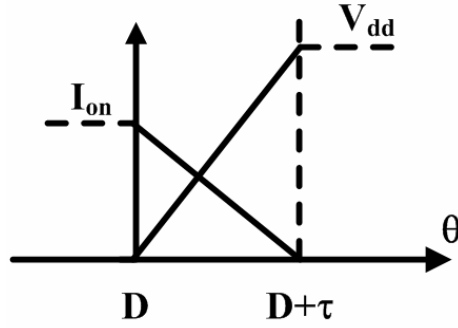


Figure. 3.16 Overlap voltage and current waveforms across the p-channel transistor during the transition

The device output capacitance loss is P_{cap} which can be written as

$$P_{capacitance} = C_p (V_{dd} - I \cos D \cdot R_{on})^2 \cdot f \quad (3-23)$$

With the output power and the DC power from (4) and (6), the amplifier efficiency can be obtained as

$$\eta = \frac{P_{out}}{P_{dc}} \quad (3-24)$$

From (3-14) to (3-24), we considered a Class-D amplifier and the loss associated with the switching transistor only. To expand the equations for an H-bridge amplifier with loss associated with passive components also, issues such as non-ideal Q of the inductor and the capacitor at the output, and output combiner loss are considered.

The output power for an H-bridge amplifier can be written as

$$P_{out} = 2 \cdot \frac{8}{\pi^2} \cdot \frac{V_{dd}^2}{R} \left(\frac{R}{R + R_{on} + R_Q} \right)^2 \cdot \sin^2(D) \frac{\sin^2(\tau/2)}{\tau^2} \cdot 10^{-10} \quad (3-25)$$

where R_Q is the parasitic resistance due to the finite Q of the inductor and capacitor at the output and L_C is the combiner loss in dB. R in (3-25) is defined as the differential load impedance.

Considering the parasitic resistance R_Q at the output, the output current amplitude I can be expressed as

$$I = \frac{4}{\pi} \frac{V_{dd}}{R + R_{on} + R_Q} \cdot \sin(D) \frac{\sin(\tau/2)}{\tau} \quad (3-26)$$

The total DC power consumption for the combined amplifier with the two Class-D amplifier components is

$$P_{dc} = 2 \times (P_{out} + P_{Ron} + P_{overlap} + P_{capacitance}) \quad (3-27)$$

where P_{out} , P_{Ron} , $P_{overlap}$ and P_{cap} are the same as (3-21)-(3-23) except that I is replaced by (3-26). The efficiency can be obtained by dividing the output power (3-25) by total DC power consumption (3-27)

To validate the analytical equations above, the results were compared with simulations and measurements when the H-bridge Class-D amplifier is driven by the periodic signals with different duty ratios. The circuit parameters such as supply voltage, R_{on} , transition time and output capacitance, as shown in Table 3.2, can be estimated from the simulation by using Agilent ADS. By applying the estimated circuit parameters to (3-25) and (3-27), the efficiency and output power for different duty-ratios are obtained as shown in Fig. 3.17 and Fig. 3.18, respectively. Fig. 3.19

shows drain efficiency for different output power levels. The analytical and simulated results show good agreement with the measurements.

Table 3.2 Circuit parameters used in the analytical results

Frequency	V_{dd}	C_p	τ	R_Q	R_{on}	R
800MHz	2V	4.7 pF	0.1π	0.8Ω	0.7Ω	7Ω

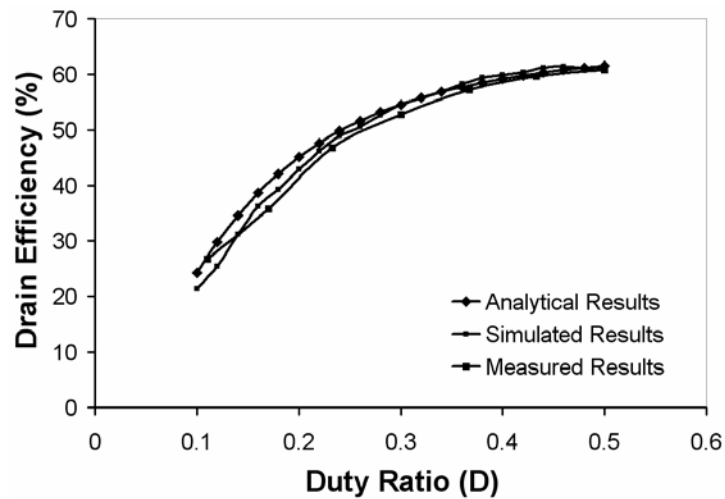


Figure. 3.17 Comparison of the drain efficiency as a function of duty-ratio

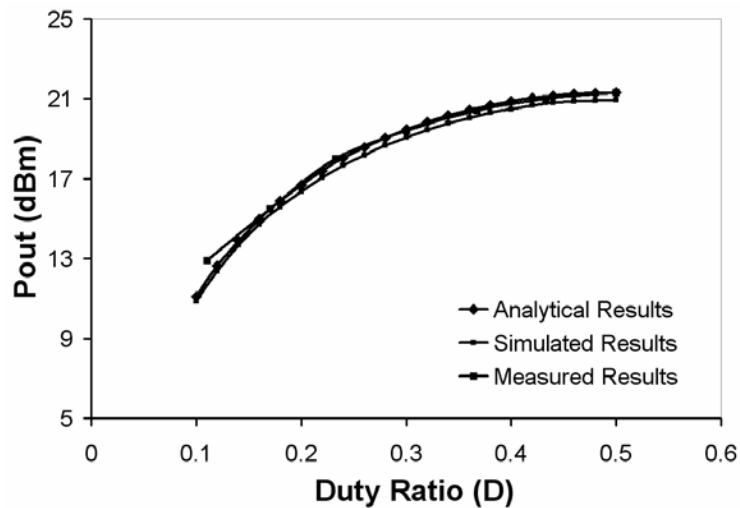


Figure. 3.18 Comparison of the output power as a function of duty-ratio

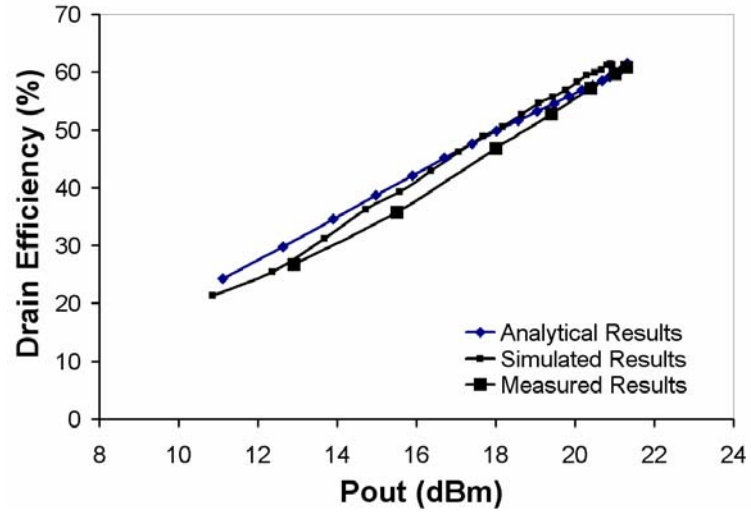


Figure. 3.19 Comparison of the drain efficiency as a function of output power

To analyze the loss associated with the transistors, each power loss factor including P_{RON} , P_{cap} and $P_{overlap}$, can be calculated separately. First, the total power loss is defined as the difference between P_{out} in (3-18) and P_{dc} in (3-20). P_{RON} can be calculated by subtracting (3-21) from (3-18). $P_{overlap}$ and P_{cap} can be obtained from (3-22) and (3-23), separately. Fig. 3.20 shows the contribution of each power loss component divided by total power loss, as a function of normalized P_{out} obtained with different duty ratios. The efficiency degradation is dominated by the capacitance loss (P_{cap}), which is independent of output power. The ratio of P_{RON} over total power loss decreases with duty ratio due to the fact that smaller currents flow through the transistor at lower output power.

The analysis results help to understand the amplifier operation when the amplifier is used in an Outphasing system (Chapter 4) or a DSM digital RF system (Chapter 5).

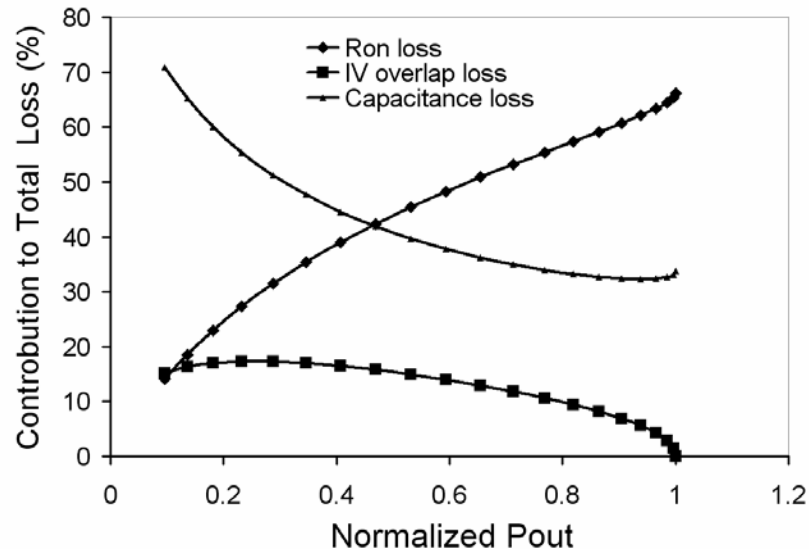


Figure. 3.20 Power loss ratio for each loss factor as a function of output power

3.5 Summary

In this chapter, design considerations of the voltage mode class-D amplifier have been discussed analytically. Based on the analytical results, the efficiency of the VMCD amplifier can be estimated from the transistor and circuit parameters, providing a useful guide for circuit design. A CMOS H-bridge Class-D was demonstrated in 0.18 μm BiCMOS technology at 800 MHz. A maximum efficiency of 62% is achieved with an output power of 21dBm. The efficiency analysis shows the contribution of different loss mechanisms as function of output power. By reducing the capacitance associated with the transistors, the amplifier efficiency can be

improved significantly, especially in the low power region. The results are helpful to analyze the amplifier performance when used in other linearized amplifier system.

3.6 Acknowledgements

Part of the material in chapter 3 is as it appears in “H-bridge Class-D power amplifiers for digital pulse modulation transmitters,” T.-P. Hung, J. Rode, L.E. Larson, and P. M. Asbeck, *IEEE International Microwave Symposium*, Honolulu, HI, June. 2007. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

3.7 Reference

- [1] P. M. Asbeck, L. E. Larson, and I. G. Galton, “Synergistic design of DSP and power amplifier for wireless communications,” *IEEE Trans. Microwave Theory and Techn.*, vol. 49, no. 11, pp. 2163-2169, Nov. 2001.
- [2] J. Rode, T. -P. Hung, and P. M. Asbeck, “Multilevel delta-sigma based switching power amplifiers systems,” presented in *IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, San Diego, CA, 2006.
- [3] S. Cripps, *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 1999.
- [4] M. Albulet, *RF Power Amplifiers*, Atlanta: Noble, 2001.
- [5] M. Iwamoto, A. Jayaraman, G. Hanington, P.F. Chen, A. Bellora, W. Thornton, L. E. Larson, and P. M. Asbeck, “Bandpass delta-sigma class-S amplifier,” *IEE Electronics Letters*, vol. 36, issue 12, pp. 1010-1012, June 2000.
- [6] J. Sommarek, A. Virtanen, J. Vankka, and K. Halonen, “Comparison of different class-D power amplifier topologies for 1-bit band-pass delta-sigma D/A,” in *2004 Proc. of Norchip Conf.*, pp. 8-9, Nov. 2004.

- [7] P. Wagh, P. Midya, P. Rakers, J. Caldwell, and T. Schooler, "An all-digital universal RF transmitter," in *2004 Proc. Of IEEE Custom Integrated Circuits Conf.*, pp. 549-552, Oct. 2004.
- [8] T. Johnson and S. P. Stapleton, "RF class-D amplification with bandpass sigma-delta modulator drive signals," in *IEEE Trans. Circuits and Syst. I*, vol. 53, no. 12, pp. 2507-2520, Dec. 2006.
- [9] T. O'Sullivan, R. A. York, and B. G. Galton, and P.M. Asbeck, "Adaptive duplexer implemented using single-path and multipath feedforward techniques with BST phase shifters," *IEEE Trans. Microwave Theory and Techn.*, vol. 53, no. 1, pp. 106-114, Jan. 2005.
- [10] Jazz 0.18um SiGe BiCMOS SBC18PT electrical specification [Online]. Available: <http://www.jassemi.com>
- [11] J. Jeong, S. Pornpromlikit, P. M. Asbeck and D. Kelly. "A 20 dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, pp. 684-686, Dec. 2006.
- [12] T. -P. Hung, J. Rode, L. E. Larson and P. M. Asbeck, "H-bridge Class-D power amplifiers for digital pulse modulation transmitters," accepted in *IEEE MTT-S Int. Microwave Symp*, Honolulu, HI, 2007.

Chapter 4

CMOS Outphasing Class-D Amplifier with Chireix Combiner

4.1 Introduction

With the increasing demands on power amplifier efficiency and linearity in modern wireless communication systems, outphasing architectures have drawn increasing attention because of their ability to achieve linear amplification along with potentially high efficiency by applying nonlinear amplifiers [1,3-6]. In 1935, Chireix proposed a reactively compensated combiner technique to further improve the outphasing system efficiency in the power back-off region via a load-pulling effect [2]. This efficiency enhancement technique can benefit the non-constant envelope modulation systems such as CDMA. However, the outphasing system and the reactively compensated technique are not suitable for all types of switching PA such as Class-E amplifiers which achieve high efficiency only for load impedance with a specific phase [3].

Although using nonlinear amplifiers and Chireix combining technique in an outphasing system have been proposed, the limitation and the effect of Chireix combining technique on the efficiency of practical switching amplifiers has not yet been analyzed.

In this chapter, the effect of Chireix combiner on the efficiency of an outphasing amplifier system are analyzed and demonstrated. In section 4.2, the analysis explains the limitation of the efficiency improvement in the power back-off region while applying Chireix combiner technique. In section 4.3 and 4.4, an outphasing amplifier was demonstrated using two Class-D amplifiers with the Chireix combining technique. A drain efficiency of 48% was achieved for CDMA signals, with an output power of 15.4 dBm and an ACPR of -45 dBc. This corresponds to a relative improvement of 24% compared to the PA without reactive compensation. The proposed outphasing class-D amplifier can be driven by digital signals directly, thus it is suitable for all-digital RF transmitters.

4.2 Outphasing Amplifier Systems and Combiners

4.2.1 Outphasing system overview

An outphasing system consists of a SCS (signal component separator), two nonlinear PAs, and a conjugate reactively loaded combiner, as shown in Fig. 4.1. The SCS converts non-constant envelope signals $S_{in}(t)$ to two constant envelope signals $S_1(t)$ and $S_2(t)$, which drive highly efficient nonlinear PAs, whose outputs are summed. Fig. 4.1(b) shows the vector decomposition of the input signal S_{in} . After combining the S_1 and S_2 at the amplifier output, the desired amplitude and phase information of the input signal can be recovered without distortion. This approach is also called Linear Amplification with Nonlinear Component (LINC).

Thanks to the constant envelope driving signals S_1 and S_2 , the nonlinear amplifiers such as switching amplifiers can be used to increase system efficiency without degrading the system linearity. This is the main advantage of outphasing systems. In practice, to achieve high system efficiency, not only efficient signal amplification is required for each amplifier, but also the amplifier output power needs to be combined efficiently. These two criteria both relate to the input impedance of the combiner which is also the load impedance of the amplifiers. The input impedance of conventional combiner and Chireix combiner are discussed in the following section as well as the effect on system and combining efficiency.

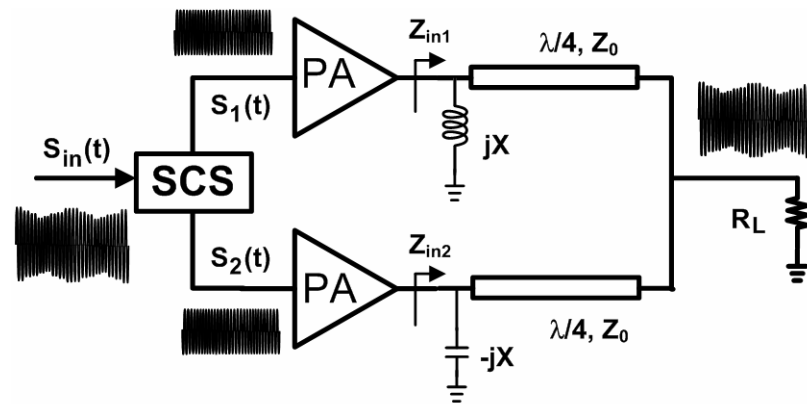


Figure 4.1(a): Simplified block diagram of an outphasing system with a Chireix combiner. The compensation reactances are complex conjugate ($\pm jX$).

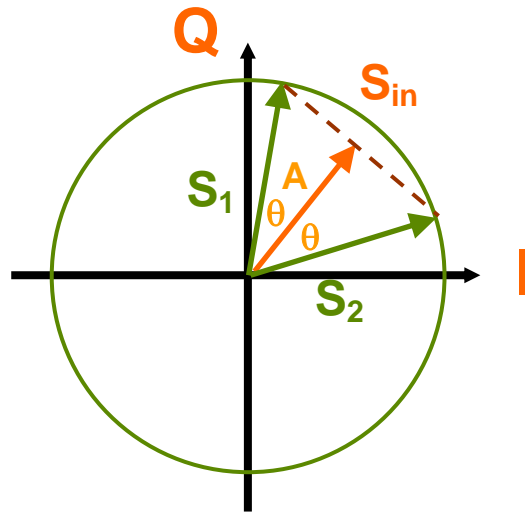


Figure 4.1(b): The input complex signal S_{in} can be decomposed into two constant envelope signals S_1 and S_2 .

4.2.2 Conventional outphasing combiner

Fig. 4.2(a) shows an outphasing system with a conventional outphasing combiner. The amplifiers are modeled as two ideal voltage sources with phase of θ_1 and θ_2 , respectively. The combiner consists of two quarter-wave transmission lines with characteristic impedance of Z_0 and R_L is the load impedance. The outphasing angle θ is defined as the phase difference of two voltage sources, $\theta = \theta_1 - \theta_2$. Under the condition of even mode excitation ($\theta = 0^\circ$), the input impedance Z_{in1} and Z_{in2} are equal

to Z_m , where Z_m is defined as $\frac{Z_0^2}{2R_L}$. When the amplifiers are driven differentially

($\theta = 90^\circ$, Odd mode excitation), Z_{in1} and Z_{in2} are infinite (open-circuit). By using the Even/Odd mode analysis [Pozar], the input impedance Z_{in1} and Z_{in2} can be written as functions of the outphasing angle θ as

$$Z_{in1} = Z_m(1 + j \tan(\theta)) \quad (4-1)$$

$$Z_{in2} = Z_m(1 - j \tan(\theta)) \quad (4-2)$$

Note that Z_{in1} and Z_{in2} are complex conjugate. Fig. 4(b) shows the input impedance on a smith chart as a function of the outphasing angle.

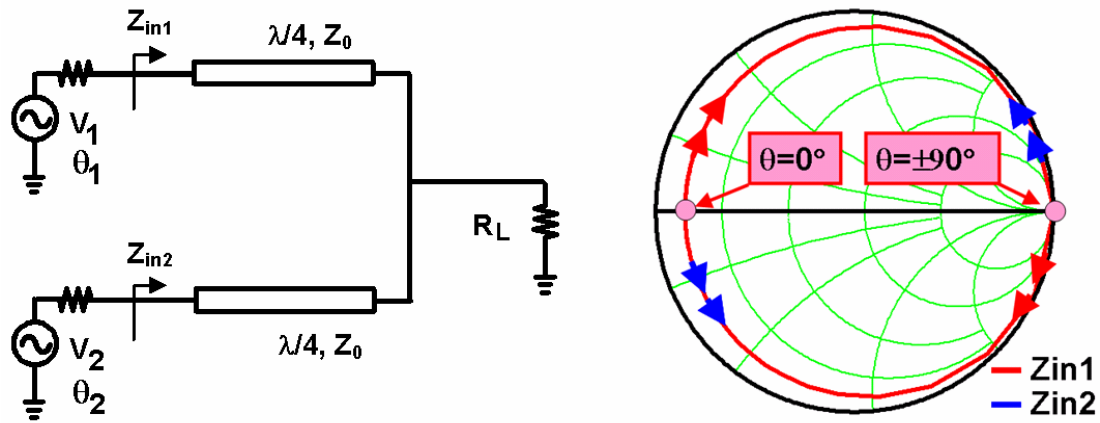


Figure 4.2: (a) A simplified schematic of an outphasing amplifier system. (b) The input impedance of with different outphasing angle θ .

For the system, the combining efficiency (η_{comb}) is defined as

$$\eta_{comb} = \frac{\text{Power delivered to the load}}{\text{Power delivered by the voltage sources}} \quad (4-3)$$

$$= \frac{P_{out}}{P_{out} + P_{loss_due_to_Rs}} \quad (4-4)$$

where P_{out} is the power delivered to the load R_L ; $P_{loss_due_to_Rs}$ is the power consumed at the source resistors. Because sum of the currents flowing through the two

source resistors equals to the current flowing through the load, $P_{loss_due_to_Rs}$ is proportional to P_{out} . Thus, the combining efficiency (η_{comb}) is a constant for all output power levels, as shown in Fig. 4.3. The in-phase driving ($\theta=0^\circ$) leads to the highest output power and $\theta=90^\circ$ corresponds to the lowest output power.

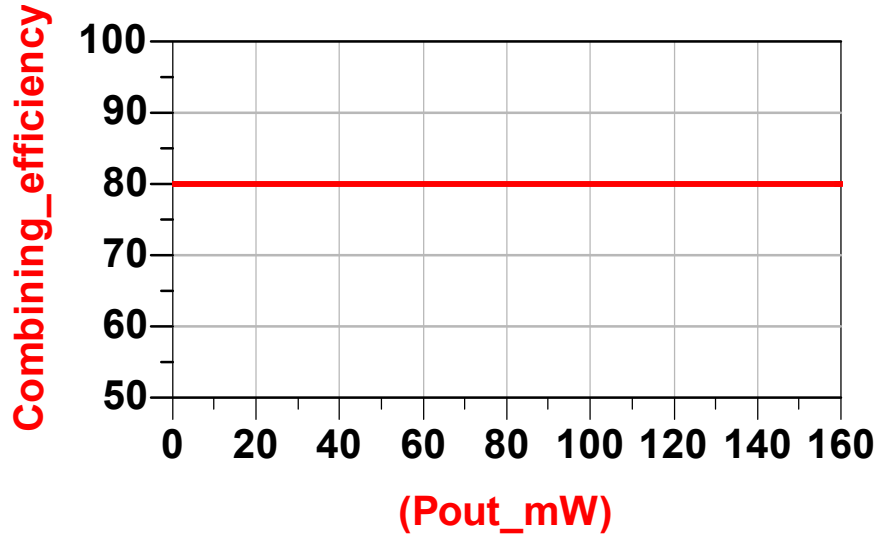


Figure 4.3: The combining efficiency at different output power levels. ($R_s=1\Omega$, $Z_0=20\Omega$, $R_L=50\Omega$, $V_1=V_2=1V$ were used in the analysis)

Note that the amplifiers are modeled as ideal voltage sources which provide the currents depending on the seen impedance, so there is no loss associated with the amplifier. However, if the amplifiers have any intrinsic loss which is independent to the output current or power, the overall system efficiency (η_{system}) needs to include the intrinsic loss as

$$\eta_{system} = \frac{P_{out}}{P_{out} + P_{loss_due_to_Rs} + P_{loss_int_insic}}. \quad (4-5)$$

where $P_{loss_intrinsic}$ is the intrinsic power loss associated with the amplifier.

Therefore, the system efficiency (η_{system}) will be degraded with any intrinsic loss from the amplifier.

For voltage mode class-D amplifiers, the power loss associated with the output capacitance can be considered as the intrinsic power loss because it is independent of the output power. An outphasing amplifier model including the output capacitance loss is shown in Figure 4.4. Because of the capacitors have to be charged and discharged through R_s , part of the energy delivered by the voltage source is consumed. This energy loss is only a function of the voltage swing of the voltage source, the capacitance and frequency. Figure 4.5 shows the efficiency of the amplifier model. The peak system efficiency occurs at the maximum output power which corresponds to the in-phase driving condition ($\theta=0^\circ$). When the PAs are under non-in-phase condition, the system efficiency drops monotonously with output power.

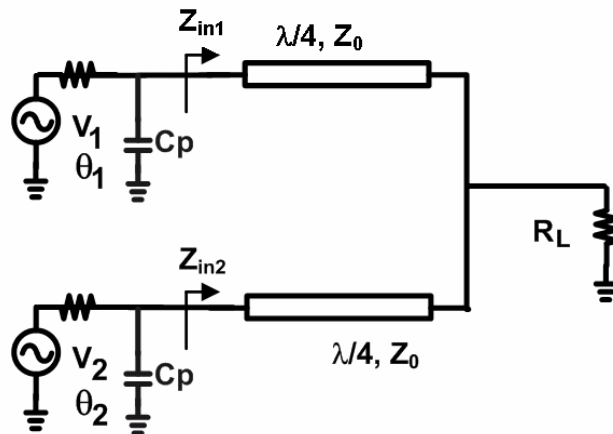


Figure 4.4: A simplified schematic of an outphasing amplifier system including the parallel capacitor C_p which represents the capacitance loss, one of the possible intrinsic losses for voltage mode class-D amplifiers

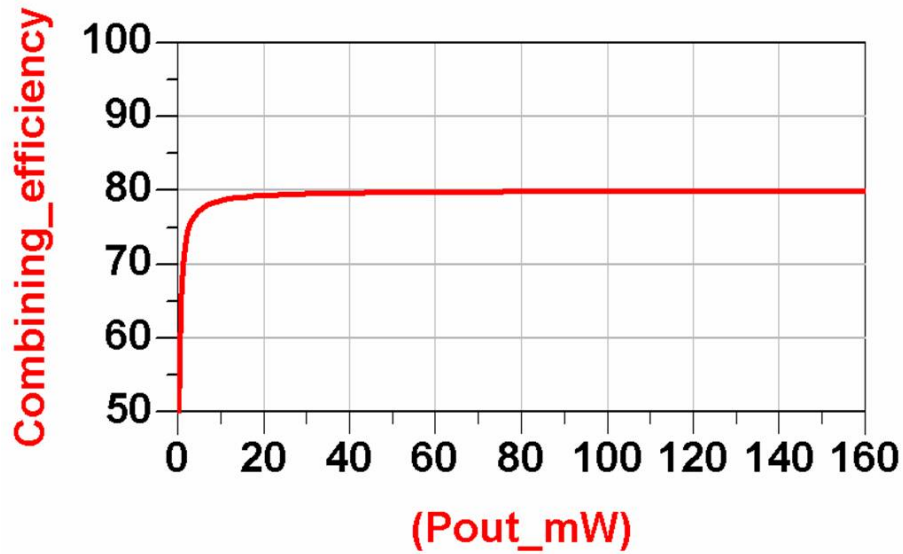


Figure 4.5: The system efficiency at different output power levels. ($R_s=1\Omega$, $Z_0=20\Omega$, $R_L=50\Omega$, $V_1=V_2=1V$ were used in the analysis)

4.2.3 Chireix power combiner

The Chireix combiner allows the PAs to obtain peak combining efficiency (η_{comb}) in the low power region under non-in-phase driving conditions via reactive compensation [2]. By adding two compensation components with conjugate reactance ($\pm jX$) into the conventional combiner discussed above, a Chireix combiner can be obtained as shown in Fig. 4.6(a). The highly efficient power combining occurs at the outphasing angles where the input impedance of the Chireix combiner Z_{in1} and Z_{in2} are equal and real, because the output signals of two PAs are now in-phase and summing at the load R_L . The choices of the compensation reactance X lead to the efficiency peaking in different power back-off region. The input impedance of the Chireix combiner in relation to the combining efficiency is discussed as follow.

In Fig. 4.6(a), the input impedance Z_{in1} and Z_{in2} of the Chireix combiner can be written as functions of the outphasing angle θ as

$$Z_{in1} = \frac{X^2 Z_m + jXZ_m [Z_m + \tan \theta \cdot (X + Z_m \tan \theta)]}{Z_m^2 + (X + Z_m \tan \theta)^2} \quad (4-6)$$

$$Z_{in2} = \frac{X^2 Z_m - jXZ_m [Z_m + \tan \theta \cdot (X + Z_m \tan \theta)]}{Z_m^2 + (X + Z_m \tan \theta)^2} \quad (4-7)$$

where X is the compensation reactance.

Fig. 4.6(b) shows the trajectories of the input impedance Z_{in1} and Z_{in2} as the outphasing angle θ changes from 0° to 89° for different compensation reactance X . When $X = 2Z_m$, there is one solution (outphasing angle) such that Z_{in1} and Z_{in2} are equal and real. When $X > 2Z_m$, there are two solutions (outphasing angles) at which Z_{in1} and Z_{in2} are equal and real. With increasing X , one of the impedance solutions moves toward higher resistance as indicated by the arrows. As the impedance is getting higher than the series resistance R_s , the ratio of power delivered to the load and power consumed at the R_s is higher, leading to a higher combining efficiency at lower output power. Fig. 4.7 shows the combining efficiency in relation to output power for different compensation reactance. The arrows in Fig. 4.7 indicate the efficiency peaking for $X = 2Z_m$, $4Z_m$ and $8Z_m$, respectively. The output power corresponds to the outphasing angle as well as the input impedance as indicated in Fig. 4.6(b). For $X < 2Z_m$, PA combining efficiency is limited by the fact that the output of both branches are never combining in-phase.

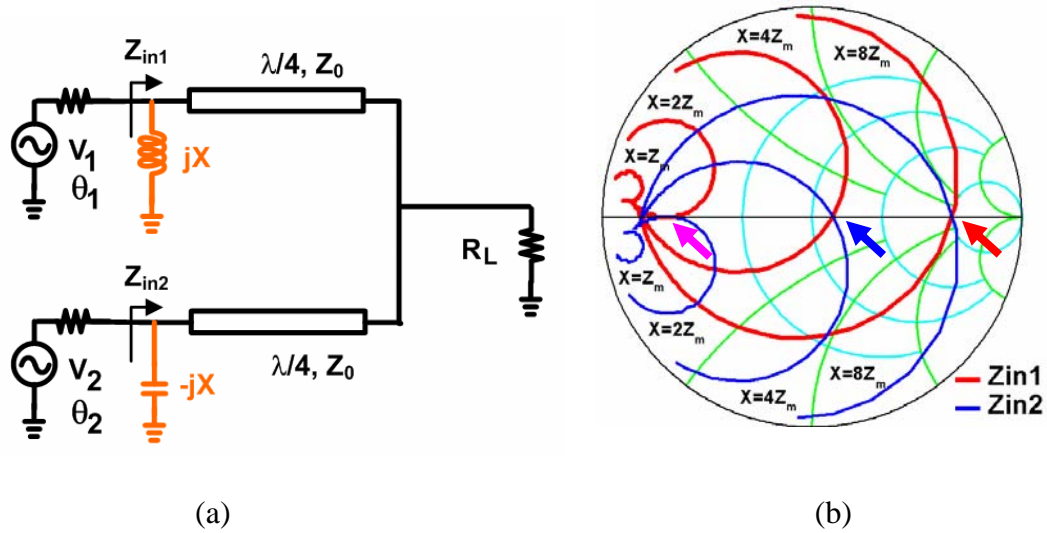


Figure 4.6(a): A simplified schematic of an outphasing amplifier system with a Chireix combiner including the reactive compensation components. (b) The input impedance for different X while changing the outphasing angle.

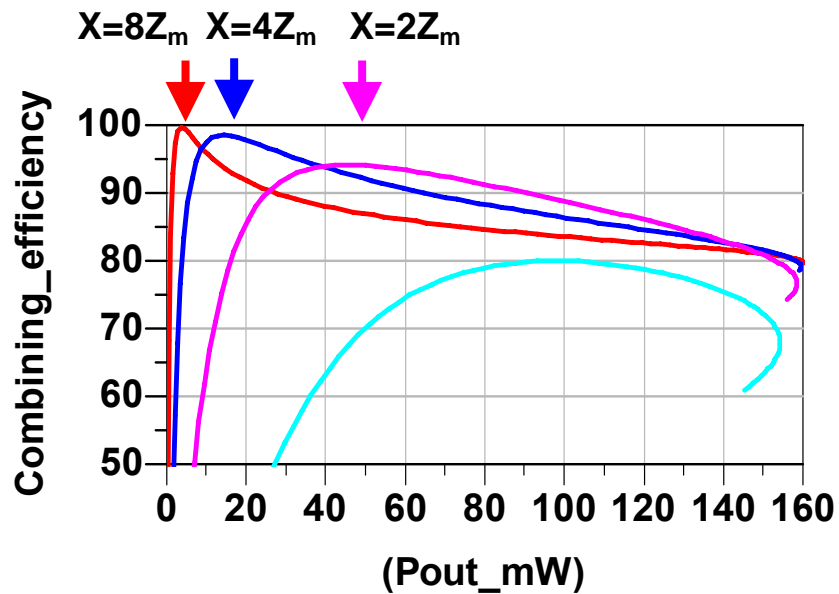


Figure 4.7: The combining efficiency of the Chireix combiner with different outphasing angle.

However, as mentioned in section 4.2.2, if the amplifiers have any intrinsic loss, the overall system efficiency (η_{system}) needs to include the intrinsic loss as shown in (4-5).

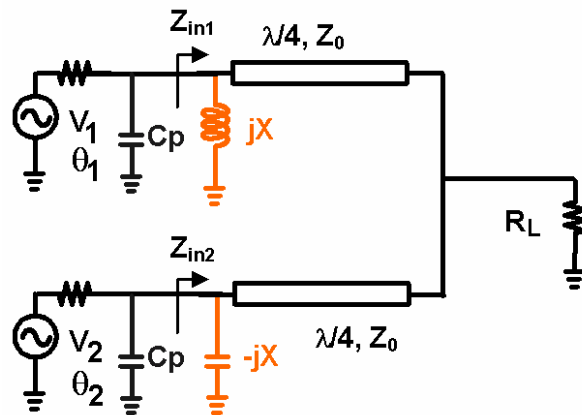


Figure 4.8: A simplified schematic of an outphasing amplifier system with a Chireix combiner including the reactive compensation components and the output capacitor C_p

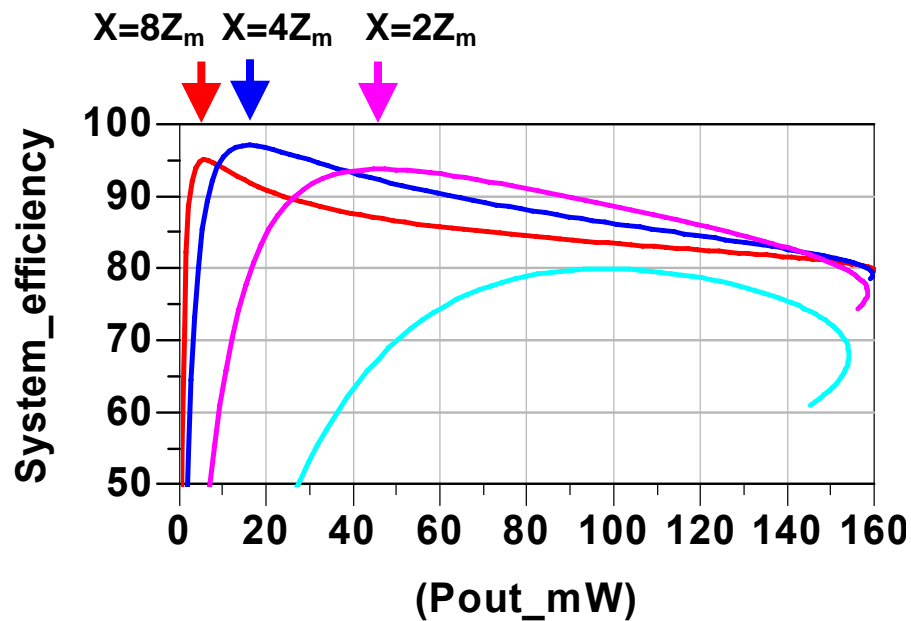


Figure 4.9: The system efficiency of the Chireix combiner with different outphasing angle.

As shown in Figure 4.9, the efficiency peaking in the low power region is thus limited by the intrinsic loss of the amplifier which is independent of the output power. When P_{out} is smaller, $P_{loss_intrinsic}$ further lowers the system efficiency. This makes efficiency peaking in lower P_{out} more difficult. The $P_{loss_intrinsic}$ mainly comes from output capacitance loss in Class-D amplifiers.

For the Chireix combiner, the efficiency peaking in the low power region is thus limited by the intrinsic loss of the amplifier which is independent of the output power. When P_{out} is smaller, $P_{loss_intrinsic}$ further lower the system efficiency. This makes efficiency peaking in lower P_{out} more difficult. The $P_{loss_intrinsic}$ mainly comes from output capacitance loss in Class-D amplifiers. The detail will be discussed in section 4.3.

4.3 CMOS Outphasing Class-D Amplifiers

4.3.1 CMOS Voltage mode Class-D Power Amplifier

A voltage-mode Class-D amplifier consists of two active devices and a series resonator. If the two devices are switched alternately, a voltage-mode class-D amplifier can be approximated as a voltage source. Therefore, voltage-mode class-D amplifiers can maintain high efficiency even while the phase of the load impedance varies. This makes them promising candidates for Chireix power combining.

As described in Chapter 3, during the ON/OFF transition of the active devices, there is a short period of time when both PMOS and NMOS are ON, resulting in a

short-circuit between the power supply and ground. A large current spike (known as shoot-through current) may occur, which causes significant energy loss. To minimize this loss, the PMOS and NMOS devices have different driving circuits, as shown in Fig. 4.10. By modifying the pull-up and pull-down device size ratio of the drivers, the overlap of the turn ON time between the PMOS and the NMOS during the transition can be minimized.

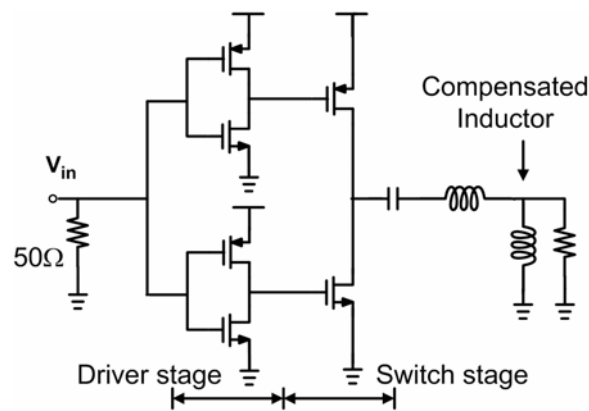


Figure 4.10: Schematic of the voltage-mode Class-D power amplifier with shoot-through current suppression and a compensated inductor.

Two voltage-mode Class-D amplifiers, configured for outphasing operation, with shoot-through current suppression were designed and implemented with in a 0.18 μm SiGe BiCMOS technology [7]. The transistor sizes of the NMOS and PMOS of the output stages were 1.6mm and 4mm. The pull-up/pull-down device size of the drivers for NMOS and PMOS were 0.2mm/0.2mm and 1mm/0.2mm, respectively. The PAs were biased at 1.8V. An inductor was added at both amplifier outputs, as shown in Fig. 4.10, to compensate the device output capacitance such that maximum output power and efficiency were achieved with purely real load impedance, resulting

in symmetric load-pull contours with respect to the resistance-axis. The 50Ω resistor at the input was for impedance matching which can be replaced by smaller driver stages as the PA is integrated in digital circuit systems. The simulated drain efficiency and output power contours of each amplifier as a function of load impedance are shown in Fig. 4.11. The corresponding peak drain efficiency and peak output power were 62% and 17.5 dBm, respectively.

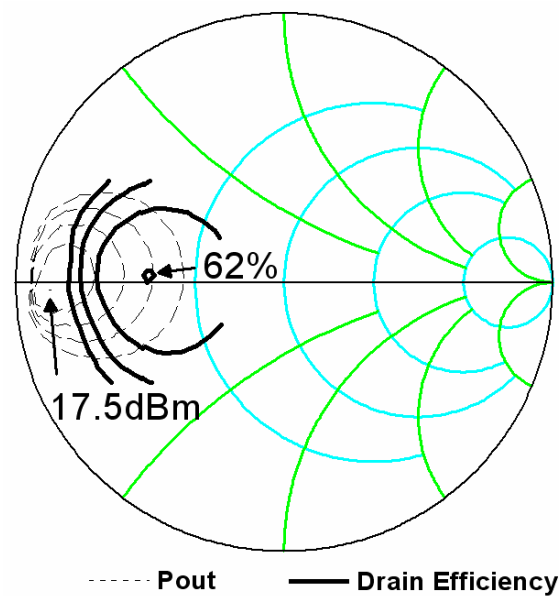


Figure 4.11: Simulated efficiency and output power load-pull contours. Max efficiency of 62% and maximum output power of 17.5dBm were obtained at the peaks, respectively.

The peak efficiency occurs at relative low impedance region is due to the output capacitance loss which is independent of the load impedance as well as the output power. From (4-5), with higher output power (lower load impedance), the system efficiency is higher.

4.3.2 Chireix Combiner Implementation

As discussed in section 4.2.3, the feature of Chireix combiner, efficiency peaking, is limited by the intrinsic loss of the amplifier such as the capacitance loss. Therefore, the reactive compensation X was chosen to be between $2Z_m$ to $4Z_m$ in order to demonstrate the efficiency improvement in the low power region.

Fig. 4.12 displays the outphasing class-D amplifier with the Chireix combiner. The Chireix power combiner was realized by a $\lambda/2$ microstrip line with characteristic impedance of 75Ω . A sliding capacitor shorting the $\lambda/2$ line to ground provides different reactive compensation to the amplifiers depending on the capacitor position [4]. When the capacitor is slid along the line, the impedances of the two compensation components change but still maintain a complex conjugate relationship, as required for the Chireix combiner.

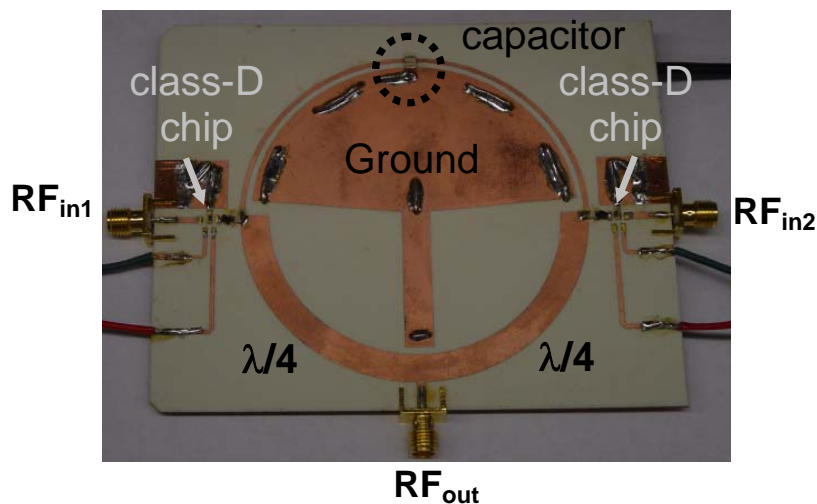


Figure 4.12: Simulated efficiency and output power load-pull contours. Max efficiency of 62% and maximum output power of 17.5dBm were obtained at the peaks, respectively.

4.4 Outphasing Amplifier Measurement Results

The CMOS Class-D outphasing amplifier was measured at 800MHz without reactive compensation. The measured power and efficiency are shown in Fig. 4.13. A maximum drain efficiency of 61% was achieved with an output power of 20 dBm and the peak PAE was 42%, in good agreement with the simulations. The input driving power while having the 50Ω impedance matching resistors is considerable. However, by embedding the PAs within digital circuit systems, this driving power consumption can be minimized further. Here, the drain efficiency includes only the switching stage power consumption, while the PAE includes the total DC power consumed by both driver and switching stage.

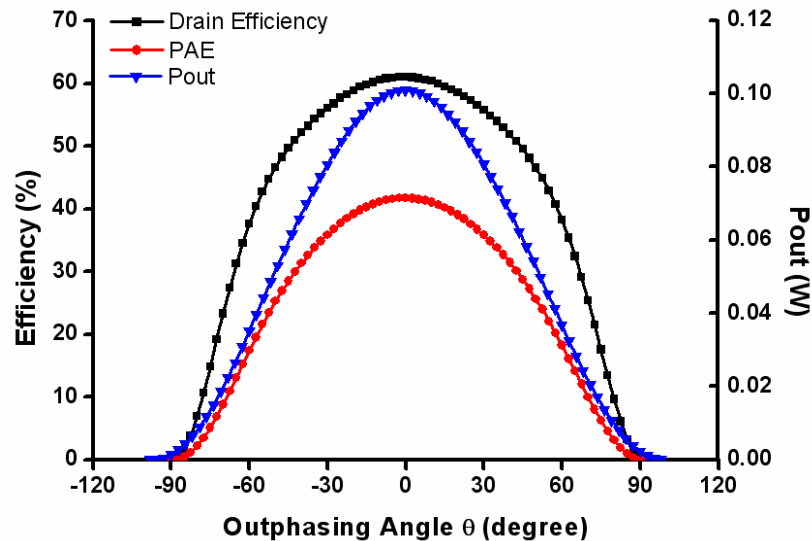


Figure 4.13: Efficiency and output power measured with different outphasing angles. Maximum drain efficiency of 62% was achieved, together with a PAE of 42%.

The measured normalized output power with different outphasing angles θ is shown in Fig. 4.14. Under the in-phase driving condition ($\theta=0^\circ$), the PA generates maximum output power; as θ is varied, the power closely follows $\cos^2\theta$, as expected.

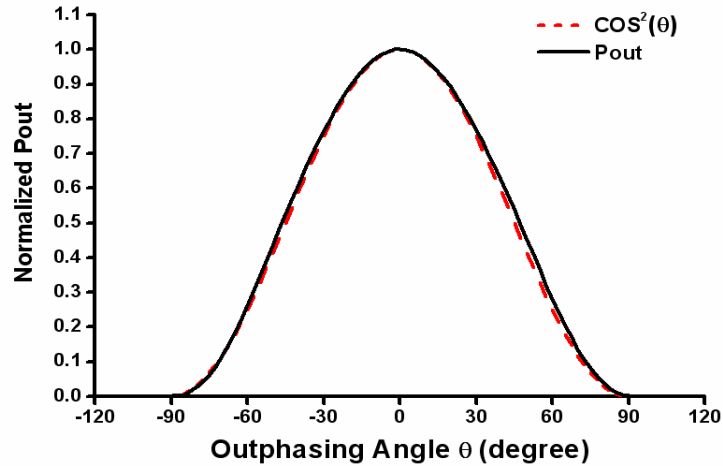


Figure 4.14: Normalized measured output power vs outphasing angle θ . A $\cos^2\theta$ curve is shown for comparison.

The outphasing amplifier was measured for reactive compensation with $X=4Z_m$, $2Z_m$, and Z_m , respectively, as shown in Fig. 4.15. With the reactive compensation $X=2Z_m$, a drain efficiency of 46% was achieved at 5dB power back-off, although the PAE drops to 22% due to the output-power-independent power consumption of the driver stage.

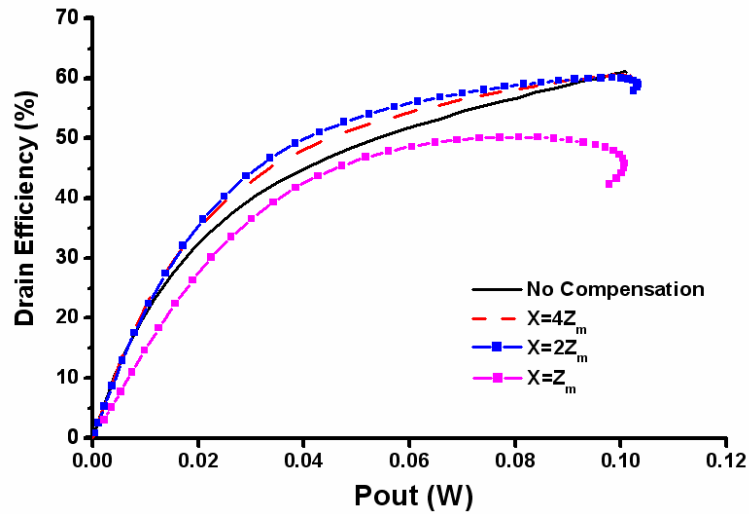


Figure 4.15: Drain efficiency measured as a function of output power with different reactive compensations.

The outphasing class-D PA was also measured with CDMA IS-95 signals which has a PAR (peak to average ratio) of 5.5dB. The SCS was implemented in Agilent ADS to generate the outphasing signals. With the SCS, the IS-95 signals were separated into two constant-envelope signals. The amplitude information of IS-95 signals was encoded to the phase difference the two constant-envelope signals as discussed in section 4.2.1. The generated two-channel signals were uploaded to two vector signal generators, respectively, with synchronized RF and IQ patterns. By using the Chireix compensation technique, the drain efficiency was improved from 38.6% to 48% (an increase by a factor of 1.24) while output power was increased from to 14.5dBm to 15.4dBm. Fig. 4.16 shows the measured amplifier output spectrum compared to the input signals. A measured ACPR of -45dBc was also obtained with output power of 15.4 dBm without any predistortion.

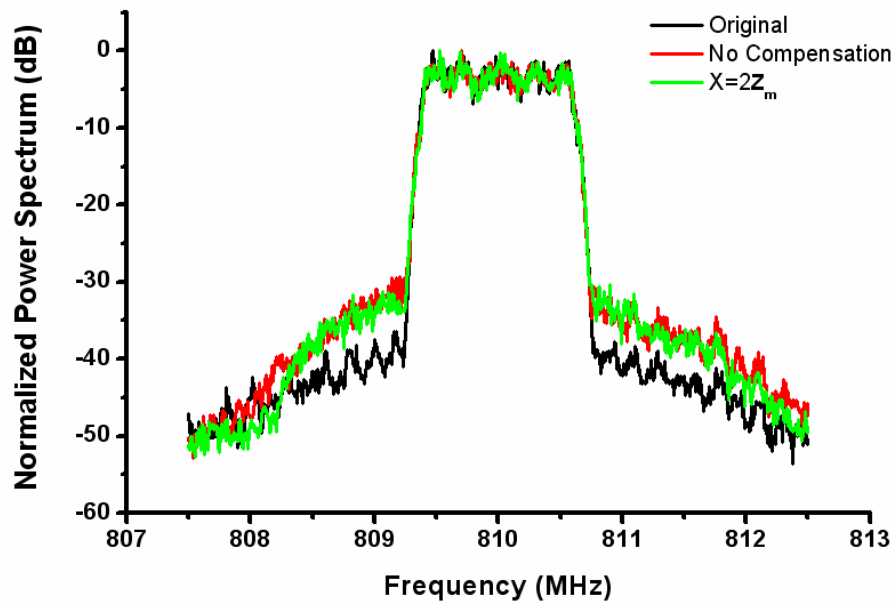


Figure 4.16: Measured PA output spectrum with CDMA signals. An ACPR of -45dBc was achieved.

The output power and efficiency of this amplifier approach can be expected to further improve with the application of stacked transistor technology [8], as well as reduced gate lengths.

4.5 Conclusion

A CMOS outphasing Class-D power amplifier with Chireix combiner was demonstrated. With the Chireix compensation technique, a drain efficiency of 48% was achieved (which represents an improvement factor of 1.24 compared to the PA without compensation). Without any predistortion, an ACPR of -45dBc was achieved. The outphasing PA is an attractive candidate for use in all-digital transmitters.

4.6 Acknowledgements

The authors are grateful to H.-Y. Pan, D. Kimball, J. Jeong and Prof. M. S. Gupta for their helpful discussion.

Part of the material in chapter 4 is as it appears in “CMOS outphasing Class-D Amplifier with Chireix combiner,” T.-P. Hung, D. K. Choi, L. E. Larson, and P. M. Asbeck, *IEEE Microwave and Wireless Components Letters*, vol. xx, pp.xxx-xxx, August 2007. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

4.7 Reference

- [1] Birafane and A. Kouki, “On the linearity and efficiency of outphasing microwave amplifiers,” *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 7, pp. 1702-1708, Jul.2004.
- [2] H. Chireix, “High Power Outphasing Modulation,” *Proc. IRE*, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.
- [3] X. Zhang, L.E. Larson and P. M. Asbeck, *Design of Linear RF Outphasing Power Amplifiers*, Boston: Artech House, 2003.
- [4] Hakala, D. K. Choi, L. Gharavi, et al., “A 2.14-GHz Chireix outphasing transmitter,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 6, pp. 2129-2138, June 2005.
- [5] W. Gerhard and R. Knoechel, “Differentially coupled outphasing WCDMA transmitter with inverse class F power amplifiers,” *IEEE MTT-RWS Dig.*, San Diego, Jan. 2006, pp. 355-358.
- [6] Stengel and W. Eisenstadt, “LINC power amplifier combiner method efficiency optimization,” *IEEE Trans. Vehicular Tech.*, vol. 49, no. 1, pp. 229-234, Jan. 2000.
- [7] Jazz 0.18um SiGe BiCMOS SBC18PT electrical specification [Online]. Available: <http://www.jassemi.com>

- [8] J. Jeong, S. Pornpromlikit, P. M. Asbeck and D. Kelly. "A 20 dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, pp. 684-686, Dec. 2006.

Chapter 5

H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters

5.1 Introduction

With the rapid advance of CMOS technology, digital signal processing (DSP) techniques can be used at clock frequencies reaching into the microwave region. As discussed in Chapter 1, there are several possible ways to implement so-called digital RF transmitters to achieve the advantages of high integration and low cost. In this chapter, a possible architecture based on band pass delta sigma modulation, as shown in Fig. 5.1, is discussed [1]. Via DSP techniques, the modulated baseband signals are generated, up-converted, and sent to a bandpass delta-sigma modulator (BPDSM). The BPDSM quantizes the signals into a binary format to drive the following amplifier stage. The associated quantization noise can be spectrally shaped out of band by the BPDSM. The bandpass filter following the amplifier avoids power dissipation at undesired frequencies to achieve high efficiency. In addition to binary signals, digital transmitters with three-level delta-sigma modulators are possible [2]. These can potentially exhibit higher amplifier efficiency by encoding more power in the desired frequency band while maintaining the signal quality.

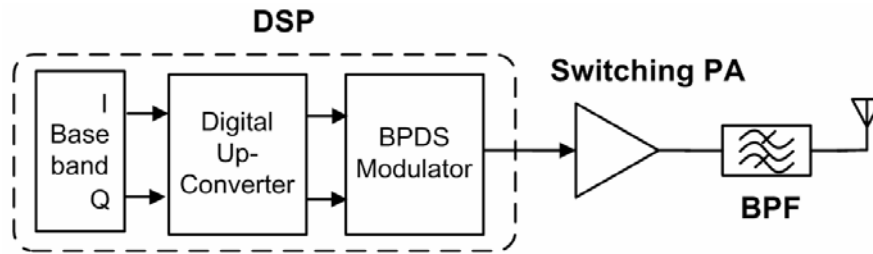


Figure 5.1: Simplified block diagram of possible future digital RF transmitters with bandpass delta-sigma modulators

Switching amplifiers are attractive candidates for digital RF transmitters because of their potential to obtain high efficiency. However, the suitable types of switching amplifiers are limited by the fact that the digital driving signals are non-periodic and broadband, so the amplifiers are difficult to maintain the performance as driven by narrow band signals. For instance, Class-E amplifiers can operate at RF frequencies efficiently by minimizing the output capacitance loss. However, the zero voltage switching condition for compensating the output capacitance loss cannot be maintained under non-periodic driving conditions, thus the conventional Class-E amplifier cannot achieve high efficiency when driven by the delta-sigma modulated signals.

Voltage mode Class-D switching amplifiers have the potential to maintain high efficiency even though the driving signals are not periodic. However, loss associated with the driving circuits, the active devices (including shoot-through current loss) and filters (poor power recycling) can degrade the performance significantly. Previously, a bandpass delta-sigma Class-S amplifier was demonstrated at 10MHz, showing 33%

drain efficiency with an IM3 of -40dBc [5]. A transformer-coupled amplifier was demonstrated at 170MHz with a drain efficiency of 8% [6]. A Class-D PA with a digital modulator based on quadrature pulse modulation was also demonstrated for EDGE signals [7].

The H-bridge class-D amplifier implemented in CMOS which has been discussed in Chapter 3 can be used in digital RF transmitters based on delta-sigma modulation (DSM) for linear and efficient signal amplification. The pull-up and pull-down devices of the Class-D amplifiers were driven separately to minimize the loss associated with the shoot-through currents. The H-bridge amplifier achieved a drain efficiency of 62% with 800MHz periodic signals. In this chapter, the case of this H-bridge class-D amplifier for CDMA signals is described. The amplifier was driven by delta-sigma modulated signals with a clock rate of 3.2GHz. For two-level delta-sigma signals, a drain efficiency of 31% was achieved with an output power of 15 dBm and an ACPR of -43dBc. The drain efficiency of the amplifier was improved to 33% by using three-level delta-sigma modulation signals while maintain an ACPR of -43dBc.

The band-pass delta-sigma signal generation is described in section 2, as well as the signal characteristics. In section 3, the amplifier operation and the factors degrading the efficiency of the Class-D amplifier driven by the delta-sigma modulation signals are considered. Analytical expressions for output power and efficiency derived in Chapter 3 allow the estimation of amplifier performance. The results are also described in section 3.

5.2 Band-Pass Delta-Sigma Modulation Signals

5.2.1 Two-Level Quantization

The driving signals of the H-bridge Class-D amplifier were generated by a simulated bandpass delta-sigma modulator driven by CDMA-like QPSK signals with bandwidth 1.25MHz and 5.5dB peak-to-average power ratio. The bandpass delta-sigma modulator, as shown in Fig. 5.2, was composed of two resonators, one two-level quantizer and two feedback loops, running at a clock rate of 3.2 GHz. The spectrum of the output binary signals is shown in Fig. 5.3. The desired signals are centered at 800 MHz (rather than in the range 825-850MHz due to limitations on our equipment for signal generation). Fig. 5.4(a) and Fig. 5.4(b) show an expanded view of the signal spectrum with 200MHz and 5MHz frequency span, respectively. The quantization noise was spectrally shaped and removed out of band. A bandpass filter is required to further reduce the out-of-band power including the harmonics and the quantization noise.

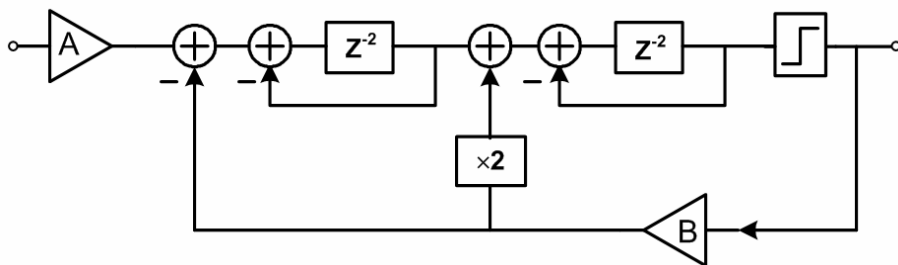


Figure 5.2: Simplified block diagram of possible future digital RF transmitters with bandpass delta-sigma modulators

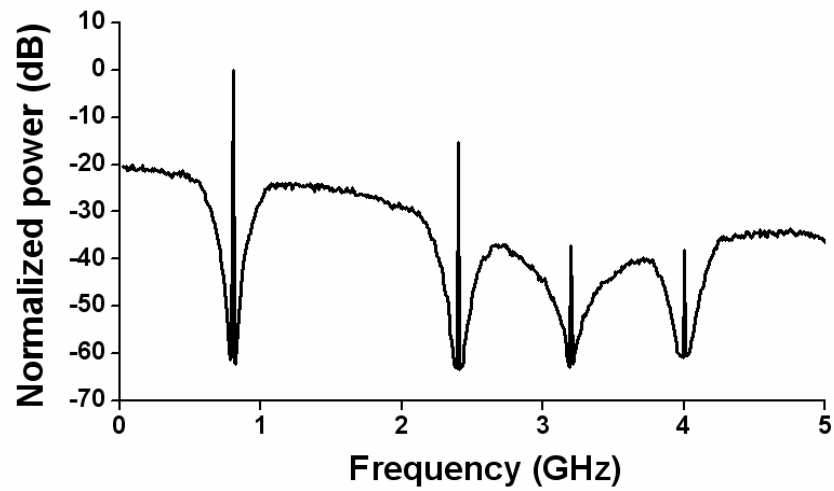


Figure 5.3: Spectrum of the delta-sigma modulated signals, showing that the quantization noise is shaped and removed out of band.

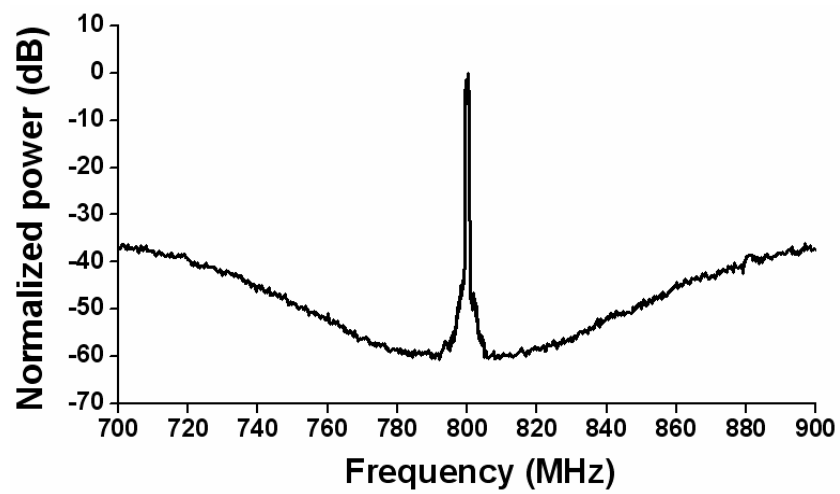


Figure 5.4(a): Expanded spectrum of Figure 5.3 from 700 MHz to 900MHz

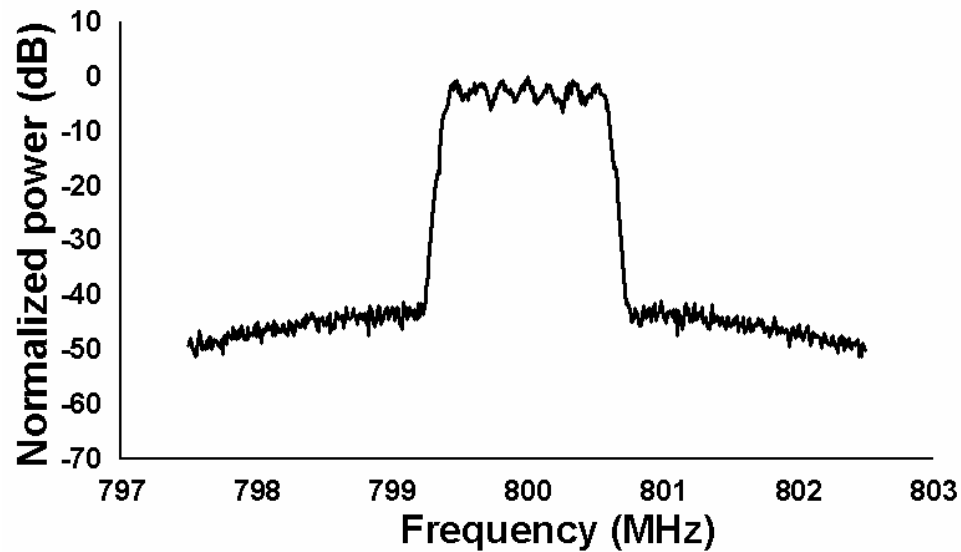


Figure 5.4(b): Expanded spectrum of Figure 5.3 from 797 MHz to 803MHz

For CDMA signals, the integrated power over the occupied signal bandwidth (1.25MHz) is defined as the in-band power. The in-band power ratio, i. e. the ratio of the in-band power to the total power contained in the digital signal, can be controlled and maximized by adjusting the feedback coefficient ratio, B/A , also defined as coding efficiency in [8]. Fig. 5.6 shows the in-band power ratio as a function of the feedback coefficient ratio B/A . Also shown is the in-band power ratio for the three-level DSM considered below. A lower feedback coefficient ratio gives a higher ratio of the desired in-band power to the total power. DSM driving signals with a higher in-band power ratio lead to higher amplifier output power. In turn, since some loss mechanisms such as capacitance loss are independent of the output power, higher output power leads to higher amplifier efficiency. However, signal quality is degraded with increasing in-band power ratio. Fig. 5.6 displays the simulated adjacent channel

power ratio (ACPR) and error vector magnitude (EVM) of the signals with increasing in-band power ratio. The maximum power ratio is determined by the EVM and ACPR specifications of the system, which determine the tradeoff between PA efficiency and signal quality.

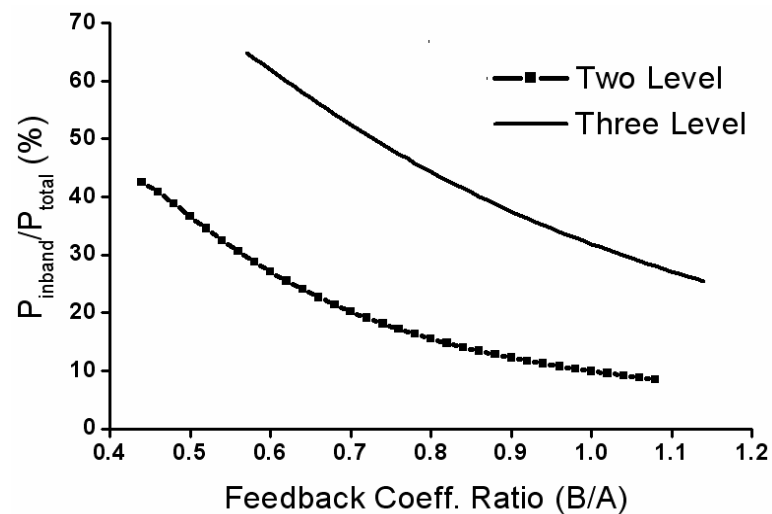


Figure 5.5: In-band power ratio as a function of the feedback coefficient ratio B/A

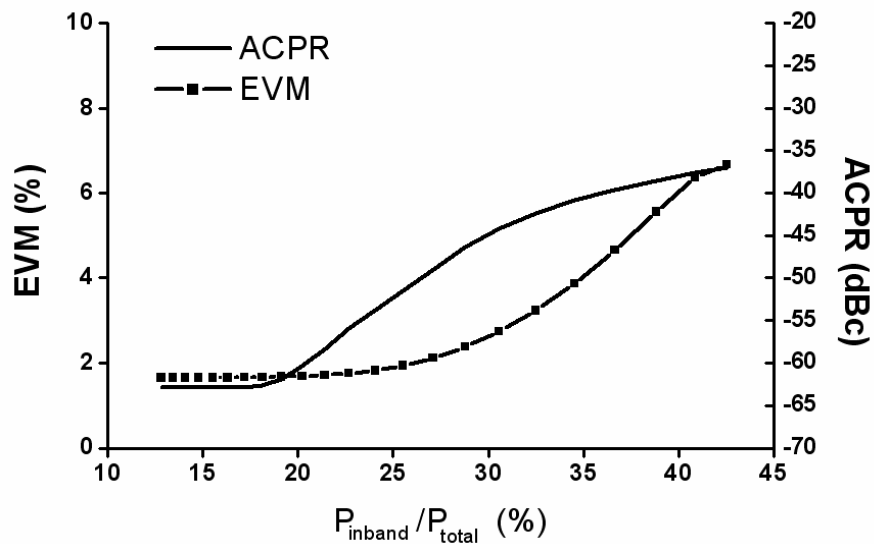


Figure 5.6: Simulated ACPR and EVM for CDMA signals after passing through delta-sigma modulator with a two level quantizer as a function of inband power ratio

5.2.2 Three-Level Quantization

Signals with higher in-band power ratio for a given signal quality factor (EVM or ACPR) have the potential to achieve higher amplifier efficiency. Changing to a three-level quantizer, as shown in Fig. 5.7, can increase the in-band power ratio. Fig. 5.8 shows the simulated ACPR and EVM of the three-level DSM signals as a function of in-band power ratio, with CDMA input signals. Compared to two-level DSM signals, more in-band power can be encoded in the three-level signals for given ACPR and EVM. However, to amplify the three-level delta-sigma signals, the amplifiers are required to differentiate between three input states and generate corresponding outputs. The CMOS H-bridge class-D described in Chapter 3 can fulfill the requirement and the amplifier operation with two and three level DSM signals is described in the next section.

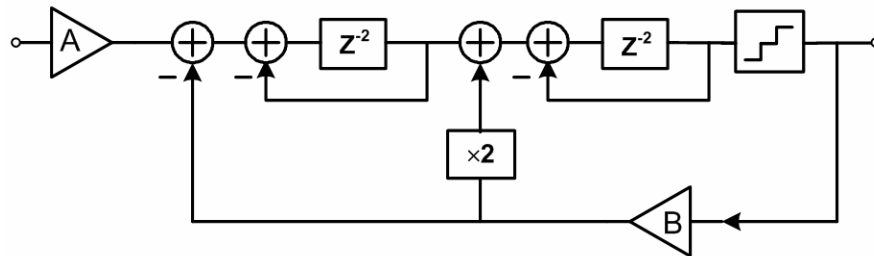


Figure 5.7: Block diagram of a three level bandpass delta-sigma modulators that uses a three level quantizer

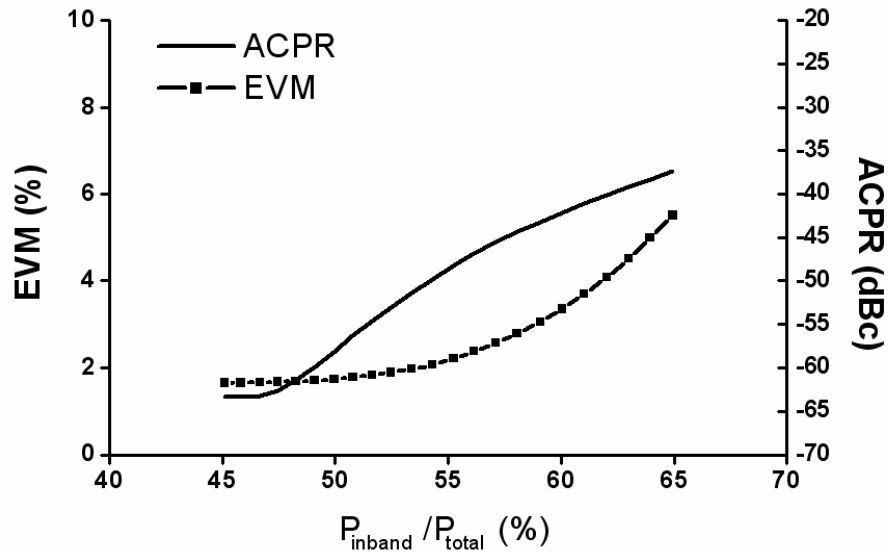


Figure 5.8: Simulated ACPR and EVM for CDMA signals after passing through delta-sigma modulator with a three level quantizer as a function of inband power ratio

5.3 Digital Operation of an H-bridge Class-D Amplifier

A single voltage mode Class-D amplifier is suitable for delta-sigma modulation systems employing two-level DSM signals. As shown in Fig. 5.9(a), the driving signal states correspond to the two states of the Class-D amplifier operation. For example, level 1 corresponds to S1 ON and S2 OFF. Level 0 corresponds to S1 OFF and S2 ON. However, a single Class-D amplifier is unable to differentiate the three driving states associated with three-level DSM signals. So, two Class-D amplifiers were configured in an H-bridge fashion, as shown in Fig. 5.9 (b). Two pairs of switches operate to produce the three different driving conditions. For example, level 1 corresponds to the condition (S11, S22 ON and S12, S21 OFF). Level -1 corresponds to (S11, S22 OFF and S12, S21 ON). Level 0 corresponds to (S11, S21 OFF and S12, S22 ON).

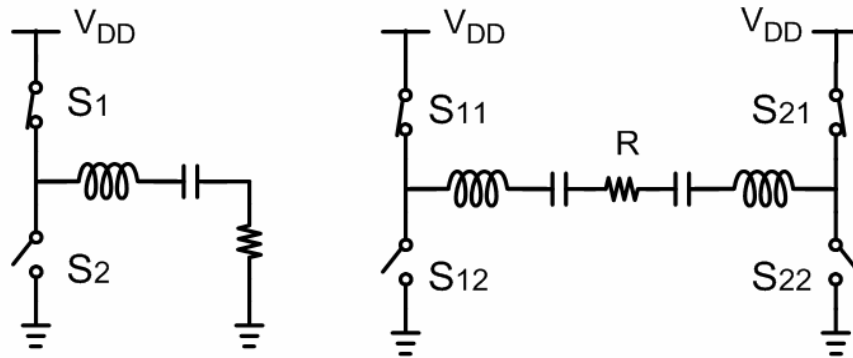


Figure 5.9: (a) Schematic of a Class-D power amplifier. (b) Schematic of an H-bridge Class-D power amplifier.

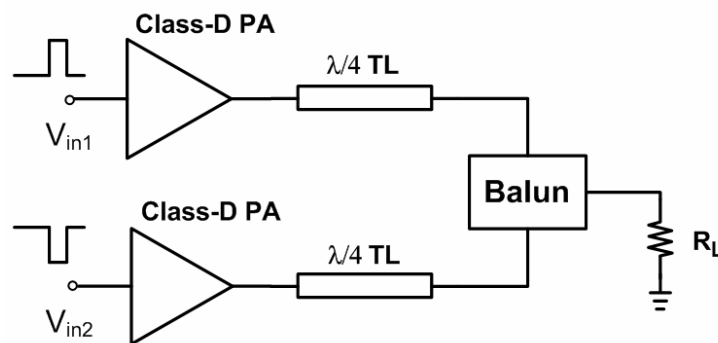


Figure 5.10: Schematic of the prototype H-bridge class-D power amplifier consisting of two class-D PA, two quarter-wave transmission lines and a balun.

The prototype H-bridge class-D amplifier with shoot-through current suppression was designed and implemented with 0.18 μ m CMOS devices, as discussed in Chapter 3. Fig. 5.10 shows the schematic of the amplifier. The driving signals V_{in1} and V_{in2} were complementary for two-level DSM signals and independent of each other for three-level DSM signals.

To characterize the amplifier for CDMA applications, a CDMA-like QPSK signal with a 1.25 MHz symbol rate and a 5.5 dB peak-to-average ratio was up-

sampled and fed to a bandpass delta-sigma modulator in Matlab. The resulting modulated binary pattern with a length of 12Mbits was stored in an Agilent 81134A pulse pattern generator, which outputs two complementary binary signals with amplitude of 2V. These two complementary signals drove the two Class-D PAs of the H-bridge amplifier directly. The input signal ACPR was measured after combining the differential signals with a quarter-wave coaxial combiner. The drain efficiency and the ACPR of the PA were measured for CDMA signals with different in-band power ratios. For the DSM signals with in-band power ratio of 24%, the amplifier obtained a drain efficiency of 26% with an ACPR of -49 dBc. For DSM signals with in-band power ratio of 30%, a drain efficiency of 31% was achieved with an ACPR of -43 dBc. The amplifier output spectra are shown in Fig. 5.11; both cases meet the CDMA specification which is -42 dBc at 885 kHz offset. Fig. 5.12 shows the output spectrum over a wide frequency range from 10MHz to 5GHz. The out-of-band signals were mainly rejected by the output resonator which has loaded Q of 6. The residual out-of-band emissions will be further rejected by the duplexer used in front of the antenna. The production of spurious signals within the receive band of a CDMA transceiver remains as a problem, however, which could possibly be addressed with an adaptive duplexer filter [9].

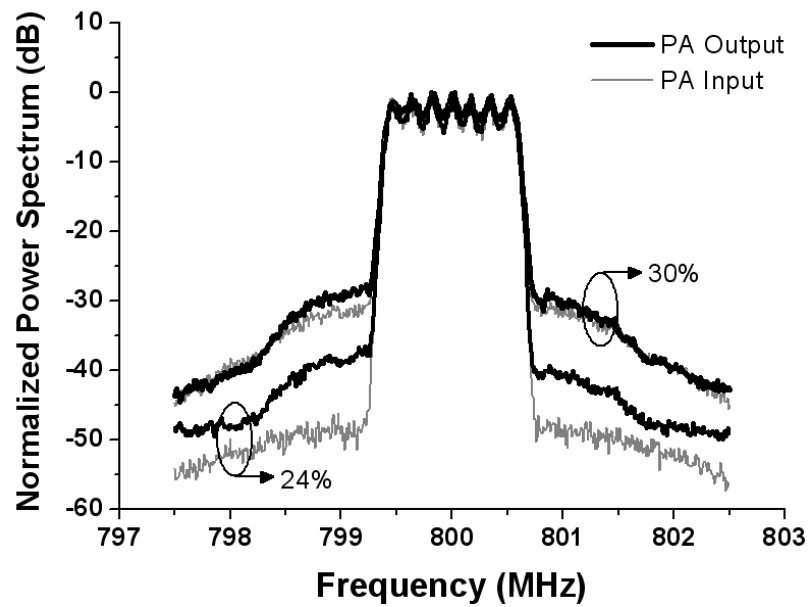


Figure 5.11: Measured input and output spectrum for two level DSM signals with a inband power ratio of 30% and 24%, respectively.

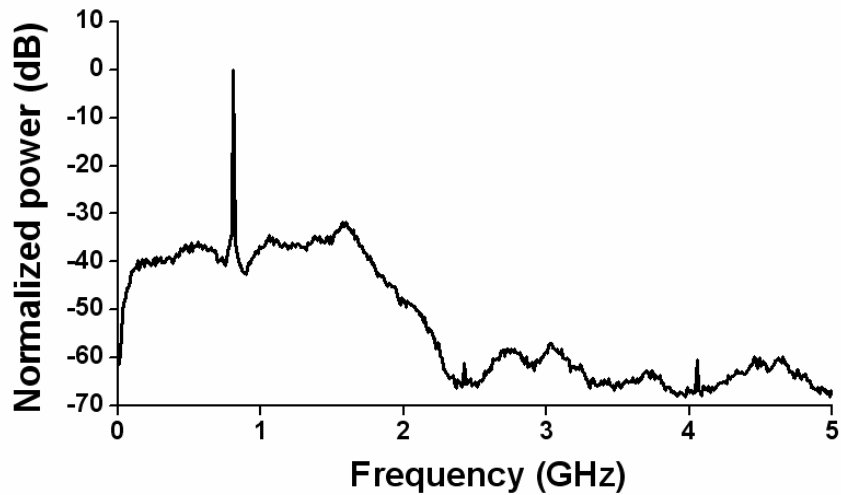


Figure 5.12: Measured Amplifier output spectrum with DSM signals

Fig. 5.13 displays the measured ACPR of the input and output of the PA and the drain efficiency. Higher efficiency could be obtained by increasing the encoded in-band power ratio, although the signal quality was degraded at the same time due to the

characteristics of the DSM. This signal quality degradation limits the amplifier efficiency in digital RF transmitters.

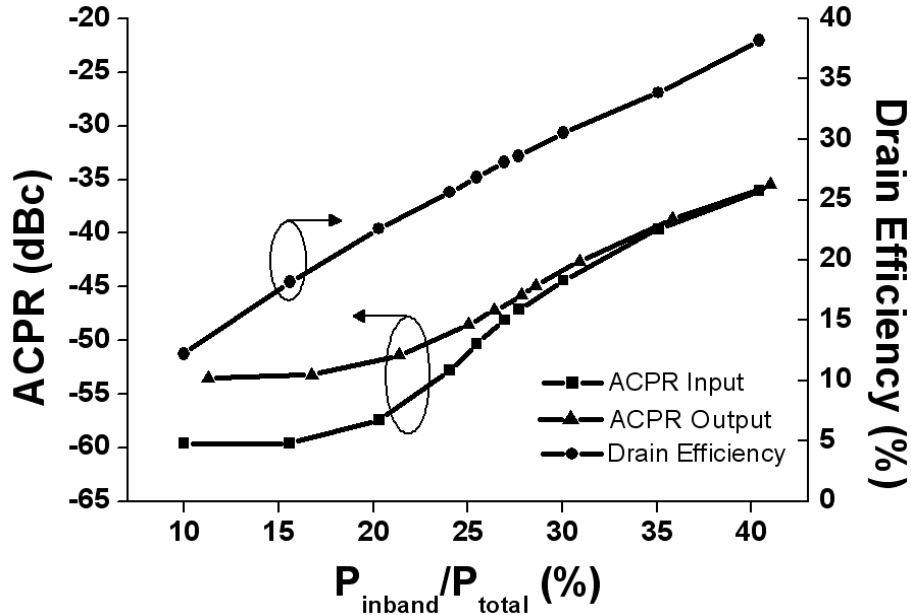


Figure 5.13: Measured ACPR and drain efficiency of the CMOS H-bridge amplifier for two level DSM signals with different inband power ratio.

It is noteworthy that in order to provide power control as needed in CDMA transmitters, the in-band power can be varied over an appreciable range (>20dB) during the generation of the DSM signal, by varying the B/A ratio. To achieve the large power control range >70dB needed in many CDMA systems, however, and to optimize efficiency, it is expected that supply voltage (V_{dd}) variation could be used (potentially together with selectable output attenuation at very low power).

The H-bridge amplifier was also measured with three-level DSM signals. Because each Class-D amplifier can only differentiate two driving levels, the three-level DSM signals have to be decomposed into two channel signals, V_{in1} and V_{in2} , and

each channel outputs two-level DSM signals, feeding to different branches of the H-bridge Class-D amplifier separately. Both DSM data streams were generated in Matlab and uploaded to the pulse pattern generator.

Fig. 5.14 shows a comparison of the amplifier efficiency using two and three-level DSM signals. The system with three-level delta-sigma modulator shows an efficiency enhancement from 31% to 33% for CDMA signals at output power of 15dBm. The ACPR was measured with three-level DSM signals as shown in Fig. 5.15. The large ACPR degradation at the low power region is believed to be related to effects such as imbalance between rise and fall time, mismatch between the two amplifiers, and non-ideal common-mode impedance. These effects are less important for two-level DSM signals due to differential operation.

In order to gain insight into the power dissipation of the amplifier, Fig. 5.16 shows the DC power consumption of the H-bridge Class-D PA as a function of the in-band power contained in the input two-level DSM waveforms. The figure shows that the output power linearly increases with the input in-band power. The power consumption at the switch stage gradually increases with the measured input in-band power while the power consumption at the driver stage stays almost constant. The overall power consumption increases because of switch stage loss contributions such as ON-state resistance (R_{on}) loss which increases with output power, as discussed in Chapter 3.

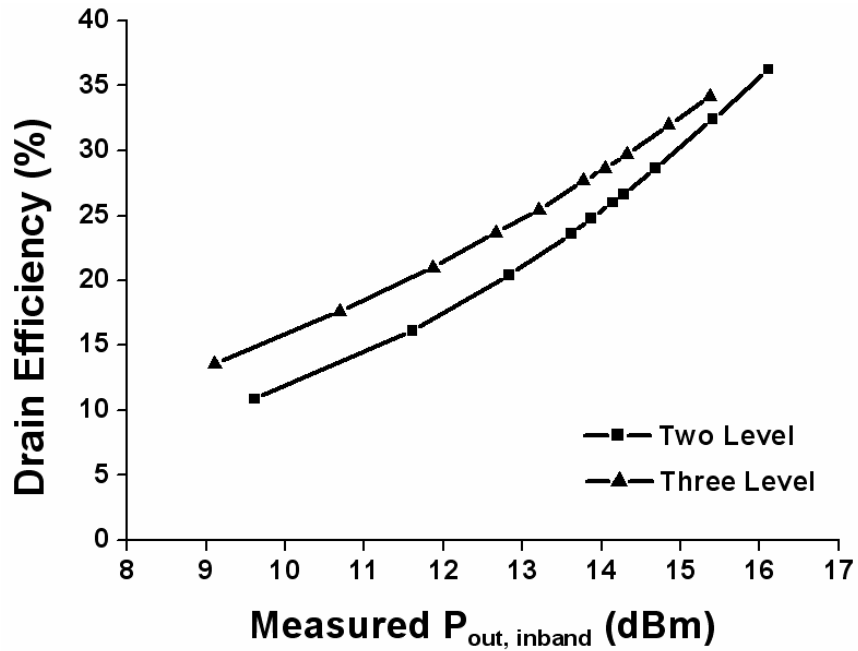


Figure 5.14: Measured drain efficiency as function of output power for two and three level DSM signals

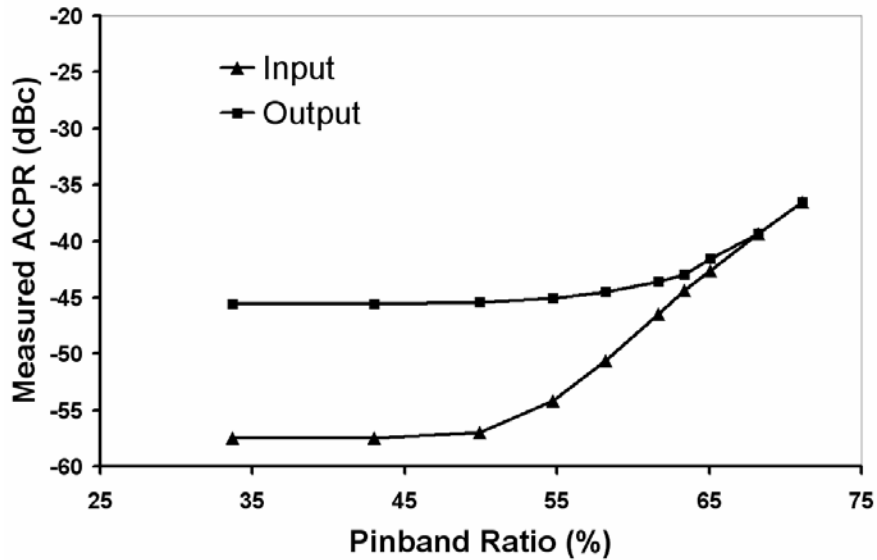


Figure 5.15: Measured amplifier input and output ACPR as a function of output power for three level DSM signals

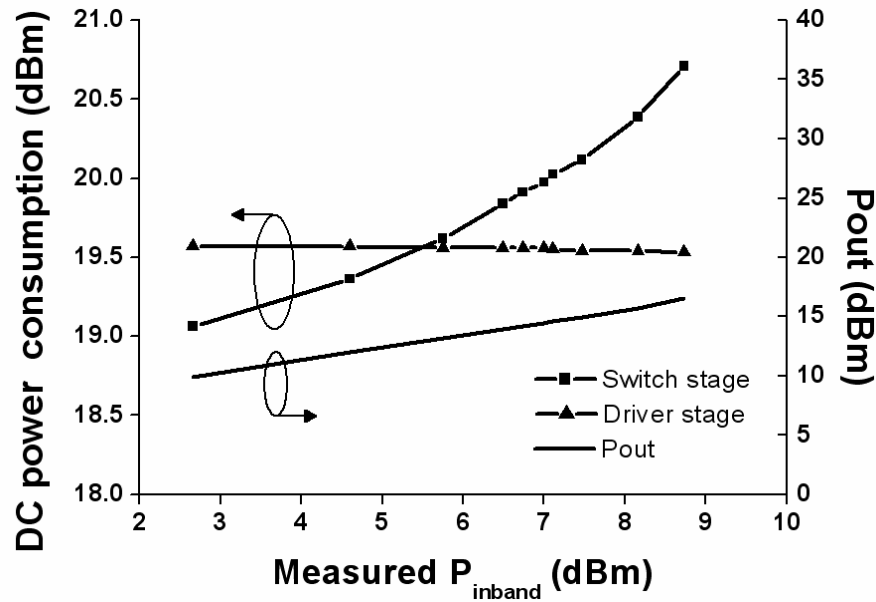


Figure 5.16: Measured power consumption at switch and driver stage and output power as function of output power

Fig. 5.17 shows the measured amplifier efficiency as function of output power for two-level DSM signals, three-level DSM signals and periodic signals with different duty ratio. The results show that the efficiency of the amplifier driven by the DSM signals is close to that for the amplifier driven by non-50% duty ratio signals with the same output power. To further justify this result, possible loss mechanisms differentiating the two situations are discussed below:

1) *Output capacitance loss*: Fig. 3.20 indicates that the output capacitance loss dominates the efficiency degradation in the low output power region. The capacitance loss depends on the average number of transitions per cycle, assuming the voltage drop due to ON-state resistance can be ignored due to the low current flowing through the transistors. Periodic signals have two transitions per cycle. For the generated DSM

signals (when the streams are longer than one Mbits to avoid statistical fluctuations), the average number of transitions per cycle is also very close to two, which leads to the same capacitance loss as for the periodic driving condition.

2) *Loss associated with out-of-band signals:* For the same desired output power, the amplifier driven by DSM signals consumes additional DC power due to generation of non-recycled out-of-band signals compared to the amplifier driven by periodic signals. The loaded Q of the output resonator determines the out-of-band signal rejection. A higher loaded Q can reduce the undesired power consumption due to the out-of-band signals. The choice of Q for the resonator is dependent on the bandwidth desired as well as by the signal and technology constraints. For the measured H-bridge amplifier, the output resonator has a loaded Q of 6, which leads to only a small difference ($<0.02\eta$) between the efficiency η of the DSM and the periodic case.

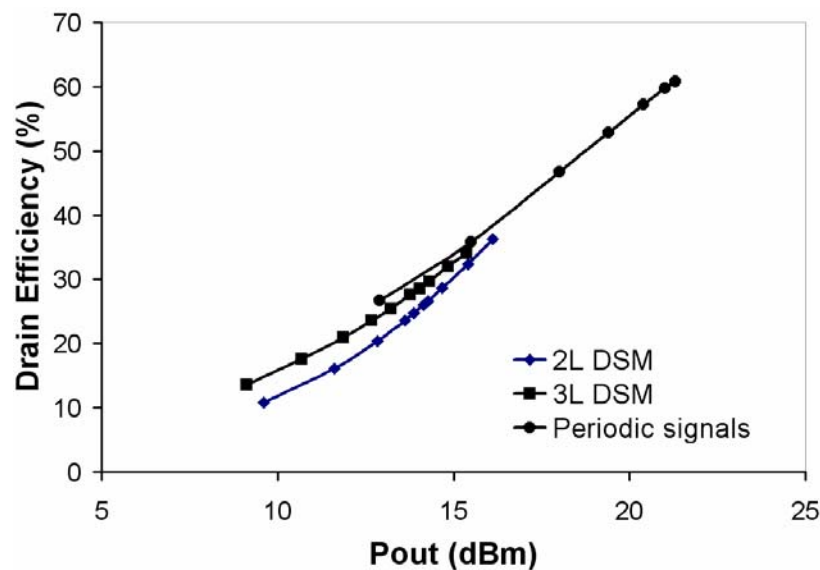


Figure 5.17: Measured amplifier drain efficiency as a function of output power

3) *Overlap loss*: The loss due to current and voltage overlap during the transition is a function of the amplitude of the currents when the transition occurs. For periodic signals, the current amplitude (I_{on}) is given in (3-22), which only depends on duty ratio (D) and the amplitude of the load current (I); for a given output power, I_{on} is a constant. However, for the DSM driving case, the current levels at the switching transition depends on the phase difference between the switched voltage waveform V_2 and the load current I_{load} . The overlap loss will be, in general, different for these different cases. For amplifiers with a short transition time, however, the average overlap loss is expected to be close to that of the periodic signals.

If the differences highlighted in the preceding paragraphs are neglected, the efficiency of the voltage-mode Class-D amplifier for DSM inputs is similar to that for operation with conventional narrowband inputs. This provides a simple way to estimate the amplifier efficiency with DSM signal driving signals. The derived equations for efficiency estimation of an H-bridge amplifier driven by periodic signals can be used.

In the aspect of improving efficiency, in addition to minimizing the loss associated with the passive components, active device improvements can also improve amplifier efficiency. Transistors based on silicon-on-insulator (SOI) technology can reduce the capacitance loss. Shorter gate length transistors with a stacked-transistor technique [11] can potentially reduce the transition time, lowering the overlap loss. The potential efficiency enhancement from these steps can be estimated by using the analytical equations (3-25) and (3-27) in chapter 3.

To estimate the efficiency enhanced Fig. 5.18 shows the drain efficiency as a function of output power for different values of output capacitance and delay. At an output power of 15dBm, amplifier efficiency can be improved from 42% to 63% by reducing the capacitance from 4.7pF to 1.2pF. By further reducing the transition time for 0.1π (62.5ps) to 0.05π (31.25ps), the amplifier efficiency can be improved to 70%. The results demonstrate the potential benefit of implementing the Class-D DSM amplifier with advanced technology.

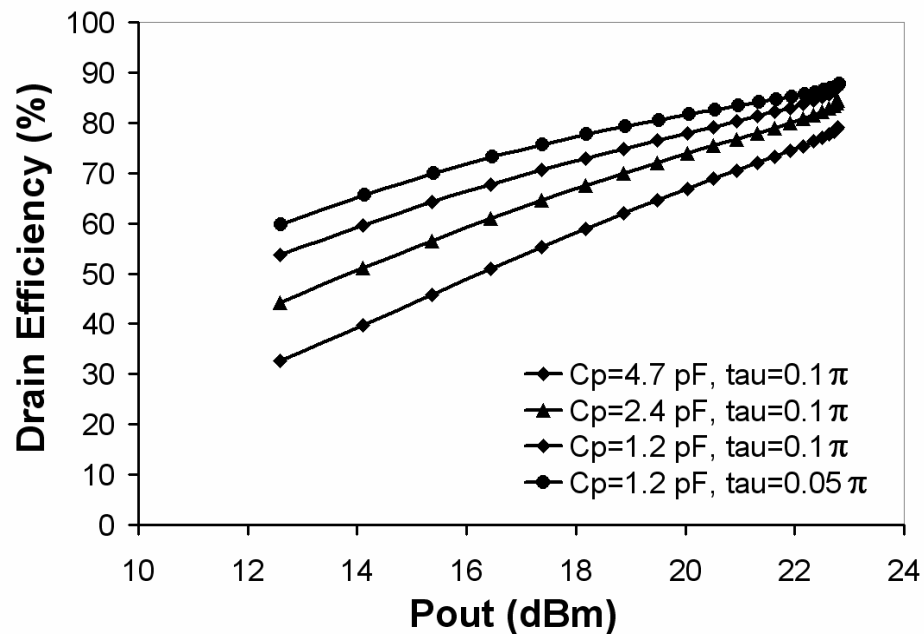


Figure 5.18: Estimated drain efficiency as a function of output power with reduced capacitance and transition time. (Based on $f=800\text{MHz}$, $R_{\text{on}}=0.7\text{ohm}$, $R=7\text{ohm}$, $V_{\text{dd}}=2\text{V}$ and no output circuit loss)

5.4 Summary

In this chapter, the digital pulse transmitter concept was discussed. An H-bridge Class-D amplifier for DSM CDMA signals was demonstrated at 800 MHz. The amplifier efficiency improved for DSM signals with higher encoded in-band power ratio. A drain efficiency of 31% was achieved with an ACPR of -43dBc for two-level DSM signals, with an in-band power ratio of 30%. An improved drain efficiency of 33% was achieved with an ACPR of -43dBc for three level DSM signals. The efficiency analysis shows the contribution of different loss mechanisms as function of output power. By reducing the capacitance associated with the transistors, the amplifier efficiency can be improved significantly, especially in the low power region. The results demonstrate the feasibility and potential of using the H-bridge Class-D amplifier in digital RF transmitters.

5.5 Acknowledgements

Part of the material in chapter 5 is as it appears in “H-bridge Class-D power amplifiers for digital pulse modulation transmitters,” T.-P. Hung, J. Rode, L.E. Larson, and P. M. Asbeck, *IEEE International Microwave Symposium*, Honolulu, HI, June. 2007. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

5.6 Reference

- [1] H. L. Krauss, C. W. Bostian, and F. H. Rabb, *Solid State Radio Engineering*. New York: Wiley, 1980.

- [2] M. Albulet, *RF Power Amplifiers*. Atlanta: Noble Publishing, 2001.
- [3] S. C. Cripps, *RF power amplifiers for wireless communications*, Boston: Artech House, 1999.
- [4] S. El-Hamamsy, "Design of high-efficiency RF class D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, pp. 297–308, May 1994.
- [5] W. J. Chudobiak, D. F. Pace, "Frequency and power limitations of class-D transistor amplifiers," *IEEE J. Solid State Circuits*, vol. SC-4, no. 1, pp. 25–37, February 1969
- [6] N. O. Sokal and A. D. Sokal, "Class E-A new class of high efficiency tuned single-ended power amplifiers," *IEEE J. Solid State Circuits*, vol. SC-10, pp. 168–176, June 1975.
- [7] F. H. Rabb, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 725–735, Dec. 1977
- [8] F. H. Rabb and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE J. Solid State Circuits*, vol. SC-13, pp. 912–914, Dec. 1978.
- [9] M. Kazimierczuk, "Class E tuned power amplifier with shunt inductor," *IEEE J. Solid State Circuits*, vol. SC-16, pp. 2–7, Feb. 1981.
- [10] M. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 149–159, Feb. 1987.
- [11] D. K. Choi, S. I. Long, "A physically based analytical model of FET class-E power amplifiers- Designing for maximum PAE," *IEEE Trans. Microwave Theory & Tech.*, vol. 47, no. 9, pp. 1712-1720, June 2003.
- [12] G. K. Wong and S. I. Long, "An 800 MHz HBT class-E amplifier with 74% PAE at 3.0 Volts for GMSK," in *IEEE GaAs IC Symp. Dig.*, Oct. 1999, pp. 299–302.
- [13] H. Kobayashi, J. M. Hinrichs and P. M. Asbeck, "Current-mode class-D power amplifiers for high efficiency RF application," *IEEE Trans. Microwave Theory & Tech.*, vol. 49, no. 12, pp. 2480-2485, December 2001.
- [14] A. Long, J. Yao, and S. I. Long, "A 13 W current mode class D high efficiency 1 GHz power amplifier" *2002 45th Midwest Symp. on Circuits and Systems Dig.*, vol. 1, pp. 33-36, Aug., 2002.

- [15] S. D. Kee, I. Aoki, and D. Rutledge, "7-MHz, 1.1-kW demonstration of the new E/F_{2,odd} switching amplifier class," *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 1505–1508.
- [16] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 51, no. 6, pp. 1677-1690, June 2003.
- [17] F. Bohn, S. D. Kee, and A. Hajimiri, "Demonstration of a harmonic-tuned class E/F_{odd} dual band power amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1631–1634.
- [18] T. P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "High efficiency current-mode class-D amplifier with integrated resonator," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Fort Worth, TX, June 2004, pp. 2035-2038.

Chapter 6

Digital Polar Modulated Switching Mode Amplifiers

6.1 Introduction

The proposed delta-sigma modulation approach in digital RF transmitter systems in Chapter 5 encodes the CDMA signals via the delta sigma modulator and drives the switching mode amplifier directly. It has been demonstrated that this approach is able to simplify the system complexity while providing linear amplification efficiently. However, as analyzed in chapter 5, one of the loss mechanisms, device output capacitance loss, dominates the efficiency performance of the amplifier due to the fact that it is independent of the amplifier output power. The smaller output power therefore leads to worse efficiency. It is difficult to tune out this output capacitance through inductors because of the wide bandwidth of the delta-sigma signals. Using advanced technology such as SOI to minimize the output capacitance is one of the possible solutions to make this approach more attractive.

To overcome the capacitance loss problem, an alternative system approach is also possible. From the system aspect, an amplifier configuration featuring zero-voltage-switching is highly desired and the driving signals need to be generated to maintain this high efficiency operating condition. This requirement suggests the digital polar modulation system as shown in Figure 6.1 which is similar to the concept

proposed in [1]. The digital polar modulation system consists of a switching amplifier with a controlled switch in the power supply path and in the digital signal modulator. The digital signal modulator first separates the complex modulation signals into envelope and phase signals, and then encodes the envelope with digital technique such as Pulse Width Modulation (PWM) or Delta-Sigma Modulation (DSM). The resulting digital envelope signals are used to control the switch and also modulate the digital phase signal. The modulated signals are sent to drive the switching amplifier directly. When the digital envelope is at the ON state, the switching amplifier is driven by phase signals only, thus working in a normal mode or high efficiency mode. When the digital envelope signal is at the OFF state, the switching amplifier is turned OFF as well as the supply switch. Therefore, the amplifier can avoid energy loss at OFF state by not drawing any DC current from the supply.

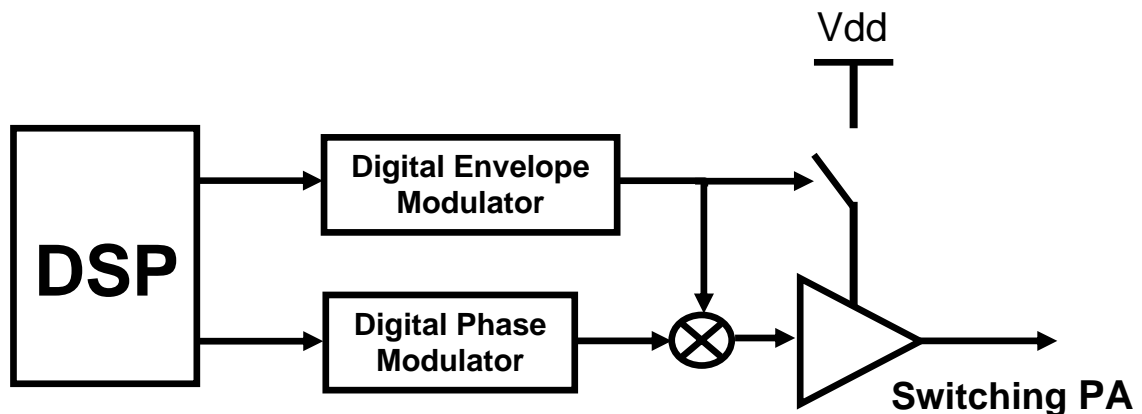


Figure 6.1: Simplified block diagram of the digital polar modulation system proposed in [1].

Compared to the approach discussed in Chapter 5, this approach allows the usage of a zero-voltage-switching amplifier configuration to solve the capacitance problem with appropriate modulation schemes. However, an additional switch is

required and aligning the switch control signal is also a challenge. To avoid these issues, the switch can be replaced with a diode which does not need additional control signal to turn ON or OFF the amplifier supply.

In this chapter, the digital polar modulation system without the supply switch is discussed. The signal generation is shown in section 6.2. The amplifier design and the experiment results are shown in section 6.3.

6.2 Digital Polar Modulation System and Signal Generation

The proposed digital polar modulation system is shown in Fig. 6.2. The switching PA is driven by the digital polar modulated signals directly and no other control signal is required to turn off the amplifier. The complex modulated signals are separated into digital envelope and digital phase signals and combined before sending to the PA. When the digital envelope is at low state, the amplifier will be at OFF mode. There are several possible ways to implement the digital signal generation. To illustrate the concept, one of the approaches is discussed in the follows. A two-tone signal is considered as an example.

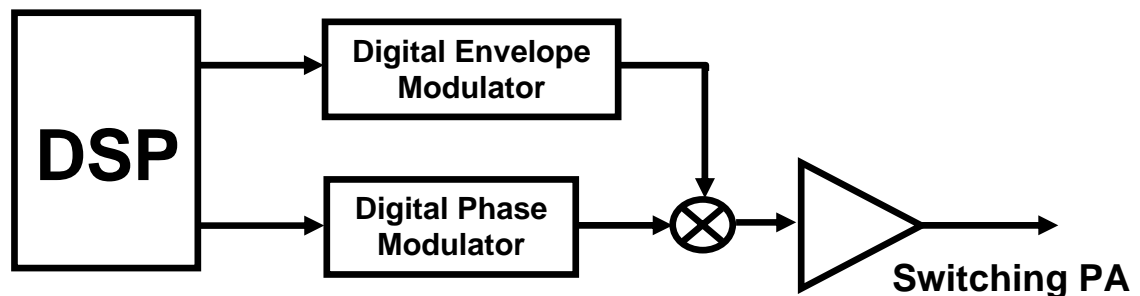


Figure 6.2: Simplified block diagram of the proposed digital polar modulation system.

For complex signals, the envelope signal is digitized into digital envelope signals. The resulting digital signals are controlled by two parameters, number of blocks (NB) and maximum number of pulses per block (MN). The product of these two parameters, total number of pulses per envelope cycle, however, is a fixed number which equals to $\frac{f_{clock}}{\Delta f}$, where f_{clock} is the clock/carrier frequency and Δf is the frequency separation of the two tones.

To clarify the signal generation, two-tone signals with separation of 2.5 MHz at a center frequency of 1GHz are considered. Fig. 6.3 shows the envelope signal and the phase signal of the two-tone signals for half envelope period. This period is divided into 40 blocks (NB=40), so each block has a maximum number of pulses of 20 pulses (MN=20). The number of pulses for each block is chosen according to the sampled average envelope to represent the envelope signals. Figure 6.4 shows the sampled envelop in blue circle for the first half period. The red star in Figure 6.4 represents the average sampled envelope for each block. Figure 6.5 displays the number of pulses for each block. It is noted that the number of pulses are chosen to represent the envelope all even number which is to ensure the pulses within one block is centered at the middle of the block. It is also noticed that the tradeoff between choosing the number of blocks and the number of pulses per block. The choice of the number of blocks and the number of pulses per block will lead to different resolution for the sampled envelope and also the spurious tone in frequency domain. Fig. 6.6 shows the envelope of the two-tone signals and the digital polar modulated signals.

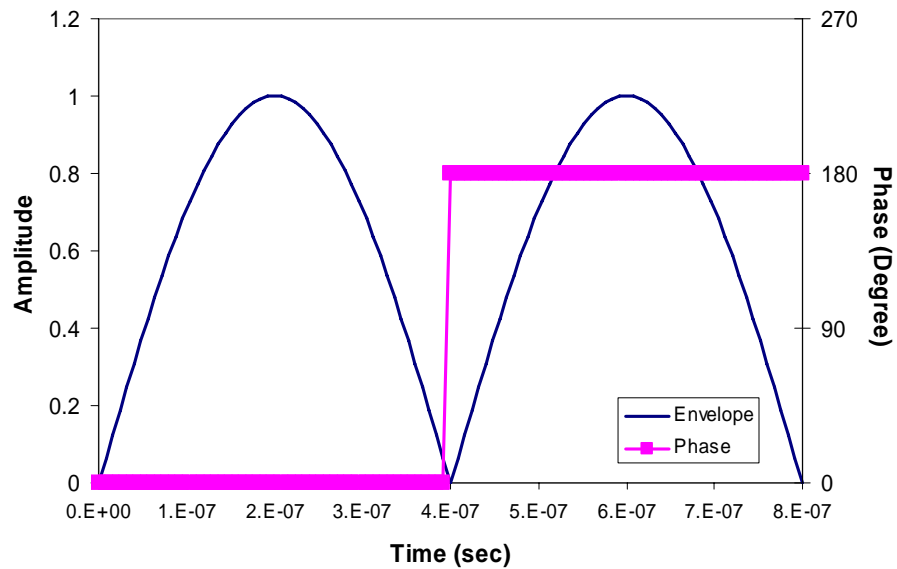


Figure 6.3: The envelope and phase signals of the two-tone signals with 2.5MHz spacing.

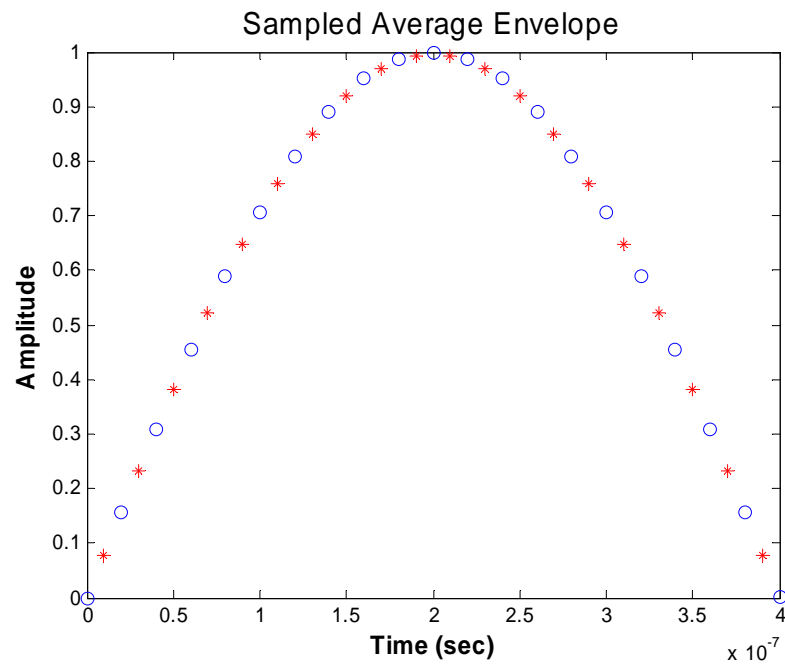


Figure 6.4: The sampled envelope (blue circle) and the average sampled envelope (red star).

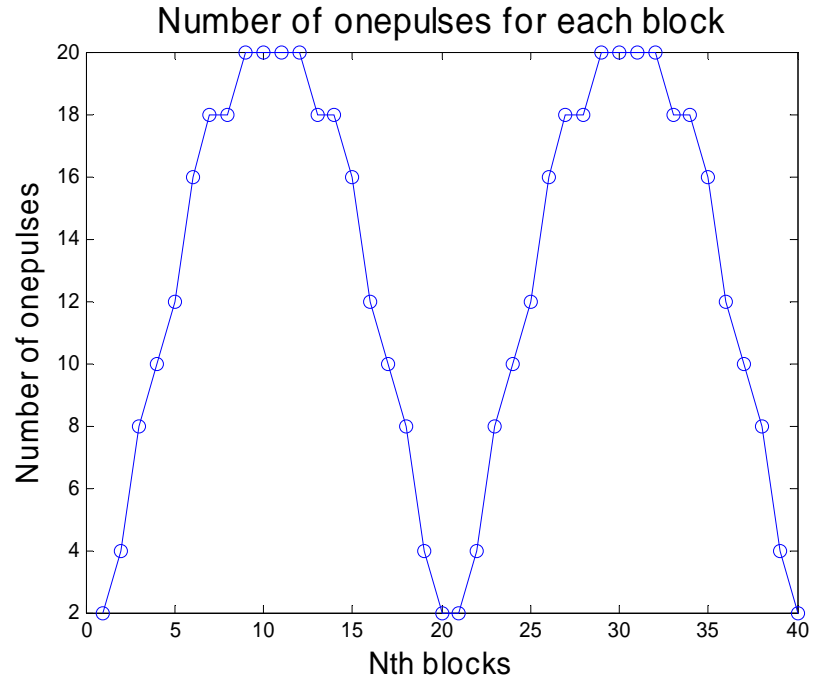


Figure 6.5: The number of pulses for each block (NB=40).

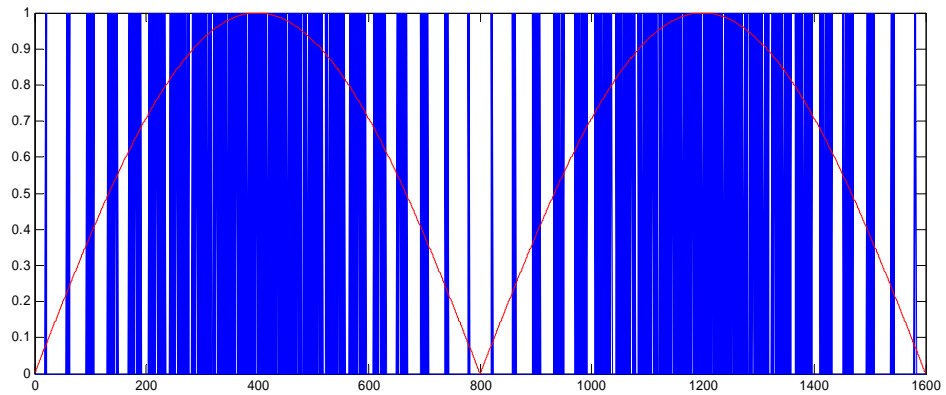


Figure 6.6: The digital envelope polar modulation pattern (blue) and the envelope (red) of a two-tone signal.

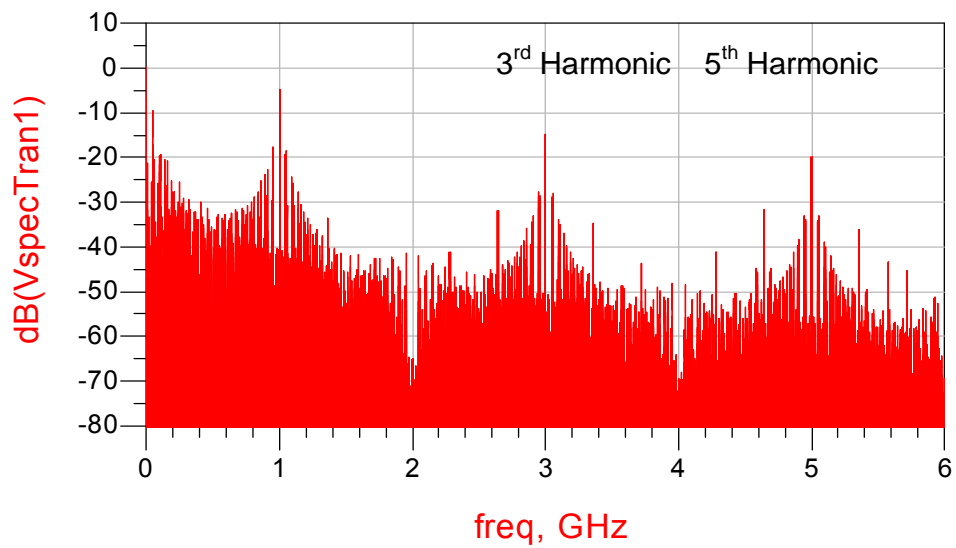


Figure 6.7: The simulated spectrum of the digital polar modulated signals for NB=40.

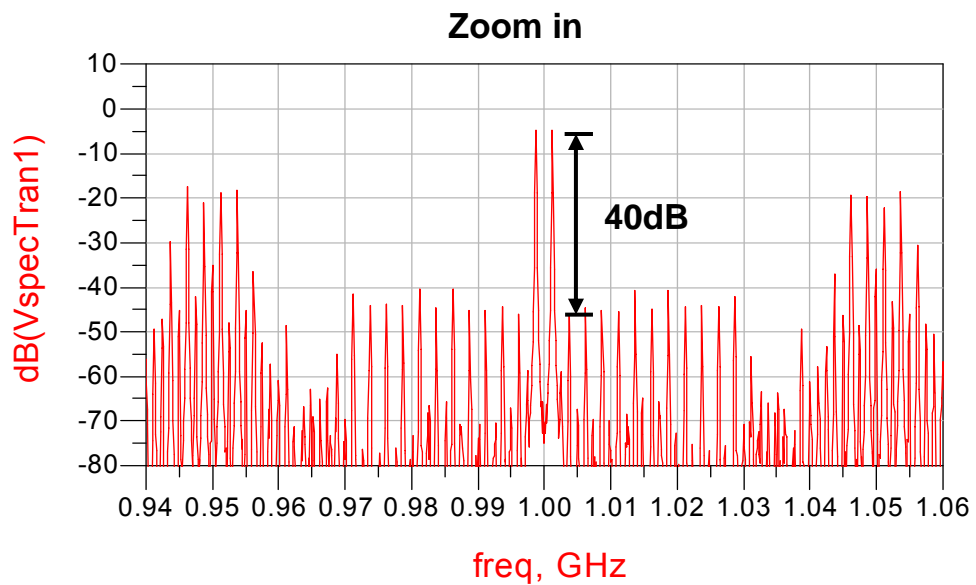


Figure 6.8: The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40.

Fig. 6.7 and Fig. 6.8 show the two tone signals in the frequency domain with different zoom-in frequency ranges. Fig. 6.7 shows that the modulated digital signal has components at odd harmonic frequencies due to the digital square waveforms. Fig. 6.8 shows the zoomed-in view at the fundamental frequency. The close-by spurious tones are 40dB lower than the two-tones. Larger spurious tones show up at the frequencies about 50MHz far away which is less problematic because of the large frequency offset. The frequencies of the spurious tones are related to the number of blocks and the number of pulses per block.

Fig. 6.9 shows the number of pulses for each block when the number of blocks of 20 is chosen ($NB=20$). With less number of blocks, the envelope can be sampled in higher resolution because of the higher maximum number of pulses per block ($MN=40$). The spectrum of the digital signal is shown in Fig. 6.10 (a). Fig. 6.10(b) shows the spectrum of the case with the number of blocks of 40. It is shown that with less number of blocks, Fig. 6.10(a), the close-by spurious is lower by more than 20dB within 10MHz offset. However, larger spurious is closer to the fundamental tone which previously is at 40MHz offset. These two charts display the tradeoff of sampling the signal envelope.

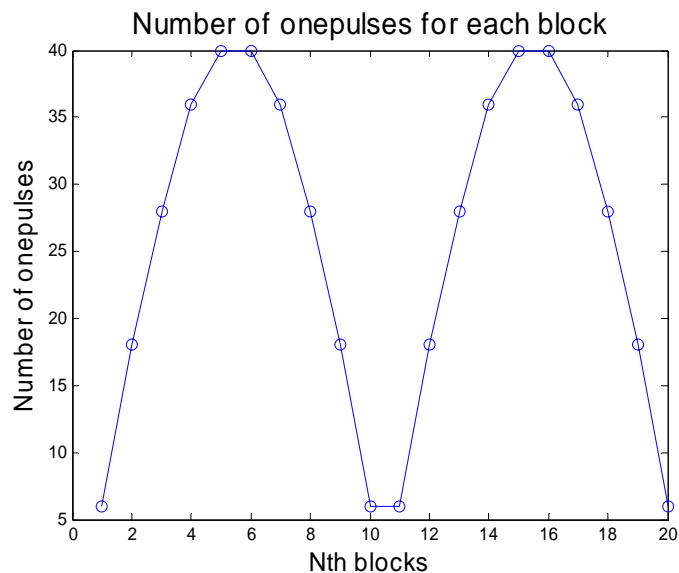


Figure 6.9: The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40.

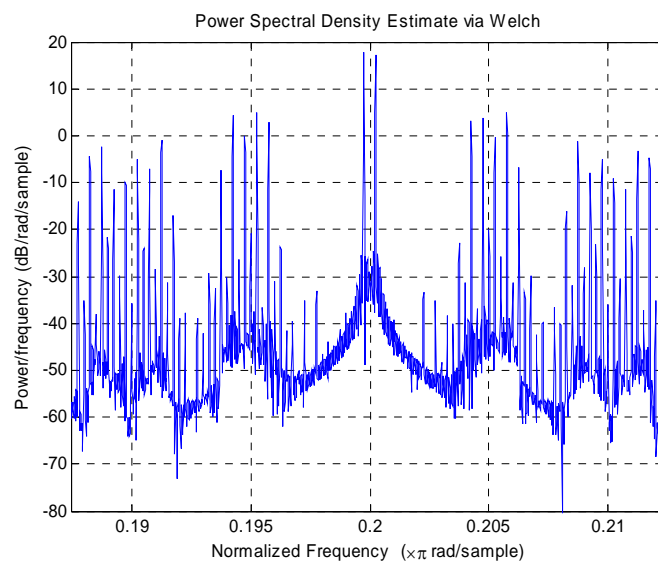


Figure 6.10(a): The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=20.

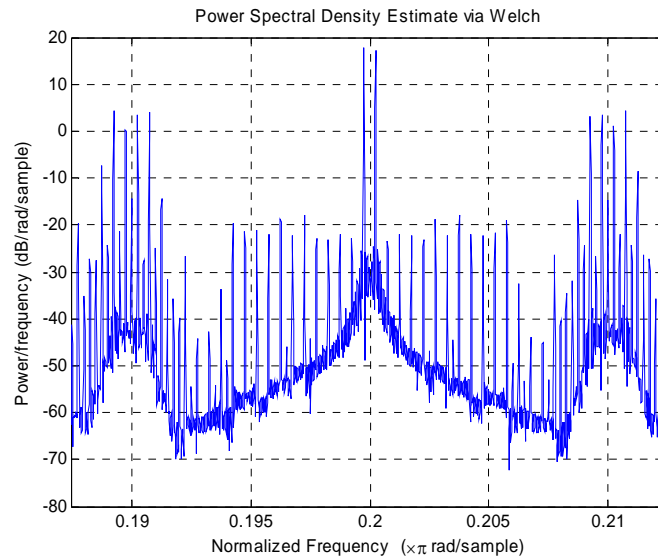


Figure 6.10(b): The zoom-in view of the simulated spectrum of the digital polar modulated signals for NB=40.

6.3 Envelope Switching Class-E Amplifier

The simplified schematic of conventional Class-E switching amplifiers is shown in Fig. 6.11. It consists of a RF choke, a compensation capacitor, a series LC resonator, and an active device. By operating the active device as a switch, the amplifier can minimize the power consumption. The output capacitance loss is also minimized by obtaining the zero-voltage switching condition at specific load impedance via choosing proper compensation capacitor and the LC resonator. Because the infinite inductance of a RF choke is not realistic, a Class-E amplifier with finite RF choke inductance was proposed by Grebennikov [2]. The design equations are shown in table.6.1.

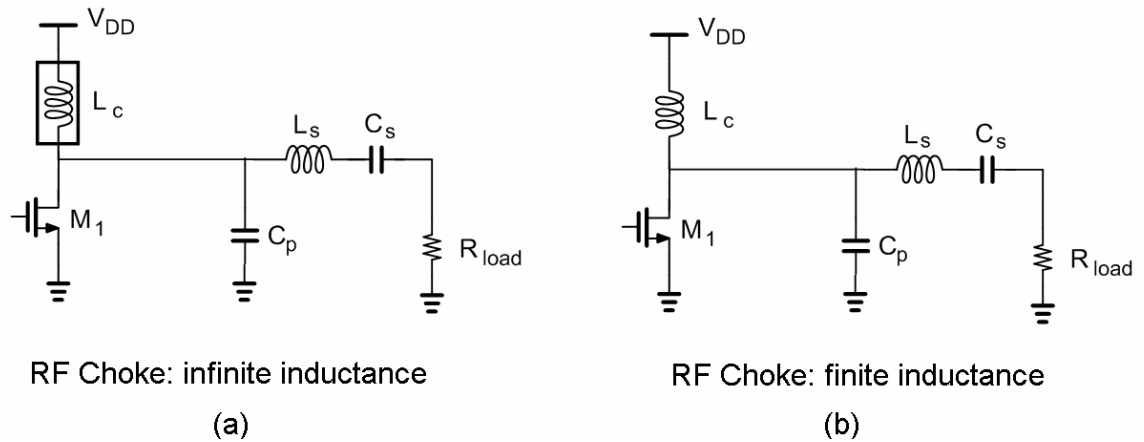


Figure 6.11: The simplified schematics of the (a) conventional class-E amplifier (b) class-E amplifier with finite RF choke inductance proposed in [2].

The Grebennikov Class-E amplifier works efficiently while driven by narrowband signals. To be used in the digital polar system, a diode is required in the supply path to support two operation modes as shown in Fig. 6.12. When the envelope signal is at ON state, phase signals are sent to drive the Class-E amplifier. The diode is turned ON to supply the drain current when necessary. When the envelope signal is at OFF state, the switch is OFF and the diode is also turned OFF to avoid DC current from the supply. While the amplifier operating at this mode, there is no DC short between the drain of the device and the supply or ground. A capacitor in parallel with the diode is necessary to resonant with RF choke to form an AC short at the resonant frequency.

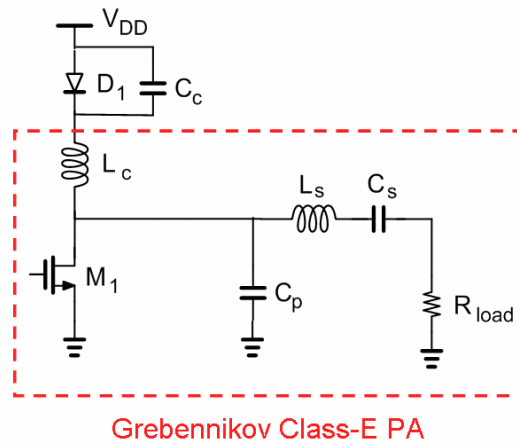


Figure 6.12: The simplified schematics of the class-E amplifier with a diode on the supply path.

A GaAs pHEMT was used to perform the simulation in Agilent ADS. The width of the device is 5mm. The designed center frequency is at 1GHz. The simulated results are as shown in table. The digital signals were generated in Matlab and imported to ADS for simulation.

Fig. 6.13 shows the time domain waveforms of the class-E amplifier driven by the two-tone digital signals including the envelope signals, the modulated digital input signals, the drain voltage and the drain current of the device. At ON state, the device works as a class-E amplifier driven by phase modulated digital signals. As shown in Fig. 6.14, the zero-voltage-switching condition was achieved during the ON state. At OFF state, the drain voltage stays at supply voltage and no current drawing from the supply. During the ON-OFF transition, it is noticed that the drain voltage takes about 5nsec before reaching the steady-state. This settling time is determined by the Q of the output resonator. Higher Q results in longer settling time.

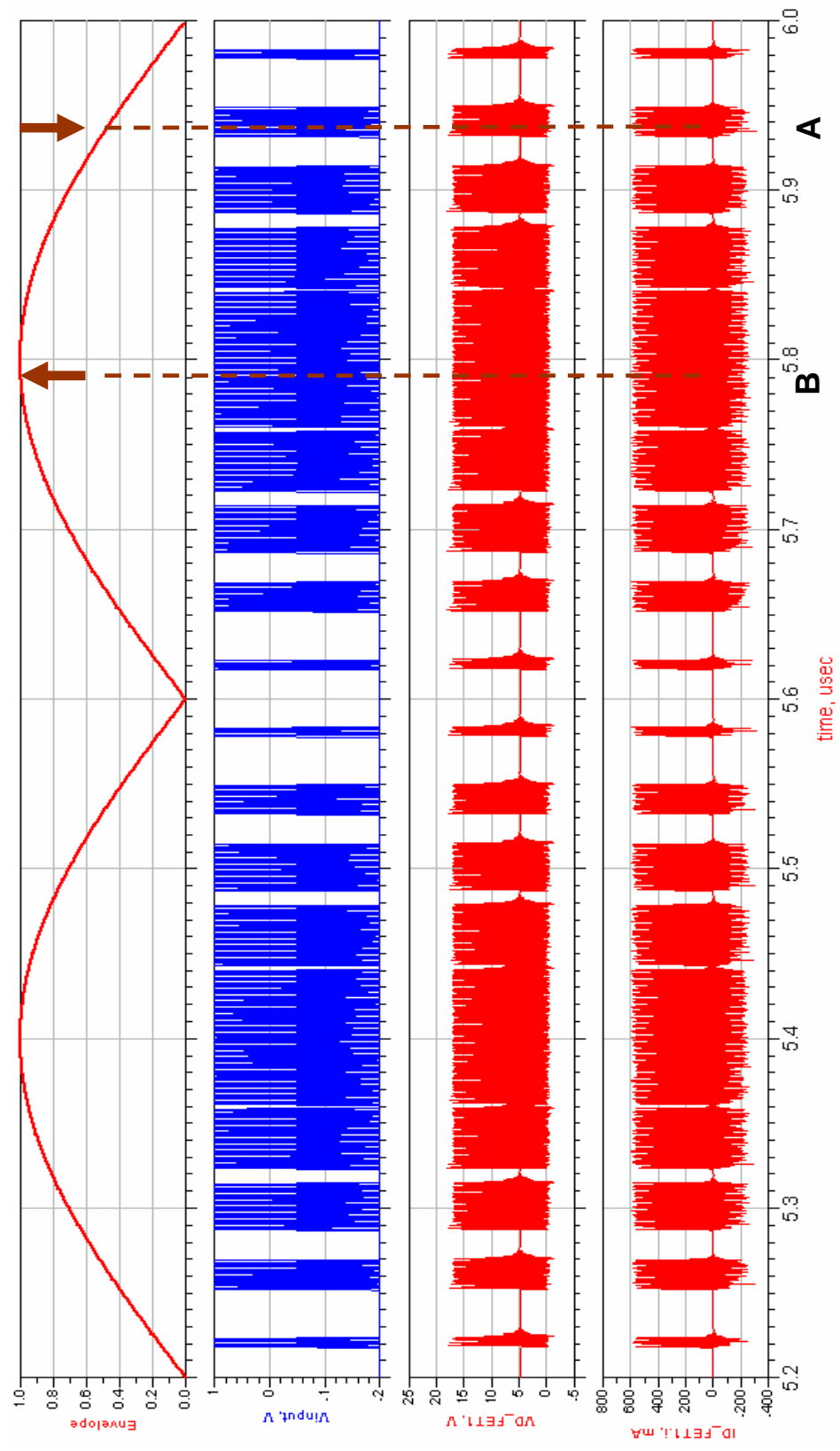


Figure 6.13: The time domain waveforms of the envelope switching class-E PA (a) Two-tone envelope signals (b) the digital driving signals (c) the voltage waveform at the drain (d) the current waveforms at the drain

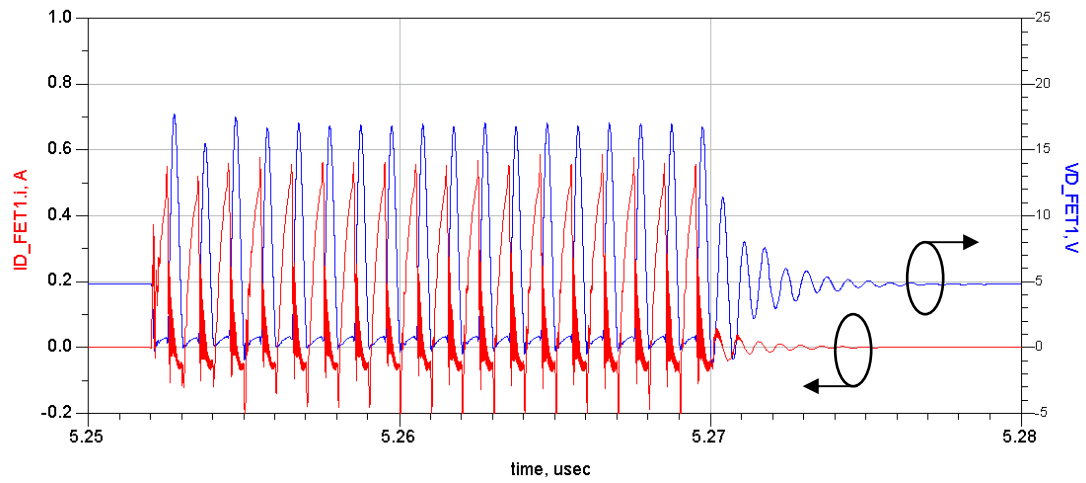


Figure 6.14: The drain voltage and current waveforms of the device.

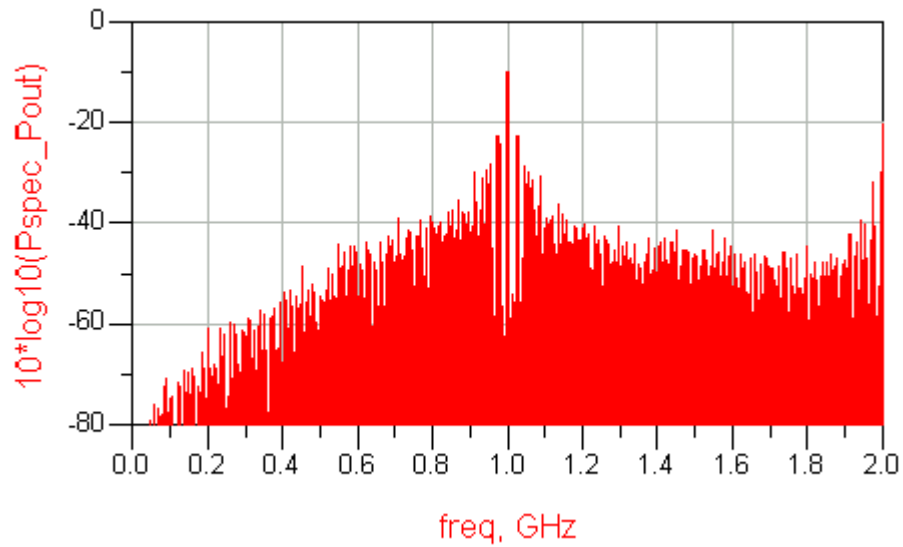


Figure 6.15: The simulated output spectrum of the class-E amplifier

Fig. 6. 16 show the amplifier output spectrum for the two-tone signals. An IM3 of -45dBc was achieved.

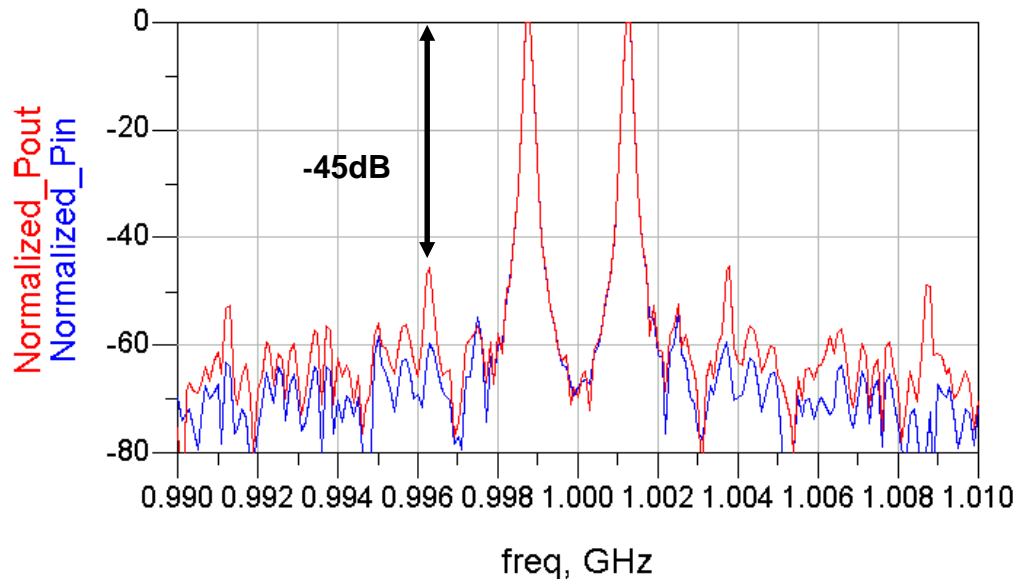


Figure 6.16: The expanded view of the normalized output and input spectrum of the class-E amplifier

6.4 Class-E Amplifier Implementation and Measurement Results

A Class-E amplifier was implemented with a GaAs pHEMT device which has a width of 5mm. The pHEMT device was assembled on a laminate with a shunt capacitor from the drain to the source such that the parasitics along the connection between the capacitor and the device can be minimized. The shunt capacitor has a capacitance of 3pF. The schematic of the class-E is shown in Fig. 6.xx. Because of the wide bandwidth of digital envelope modulation signals, the input network of the class-E amplifier needs to be wideband. Narrow-band matching network will lead to signal

distortion and degrade the system linearity. A 50ohm resistor to ground was used to terminate the input line without impedance matching. At the amplifier output, a series resonator and a shunt capacitor were used to obtain the desired load impedance for zero-voltage switching (ZVS) operation condition. The desired load impedance is $18+j12$ ohm from the simulation. The series resonator includes a high Q coil inductor which has a Q of 80 to minimize the loss due to parasitic resistance. The class-E amplifier was measured with a signal generator generating periodic signals and a spectrum analyzer. A drain efficiency of 67% was achieved with an output power of 18.7 dBm at 1GHz. The drain was biased at 4V and the gate was biased at -1.5V.

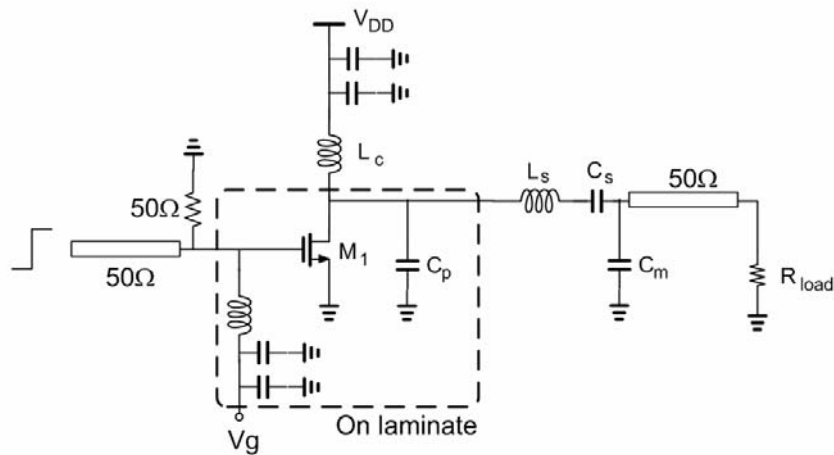


Figure 6.17: The schematic of the class-E amplifier prototype

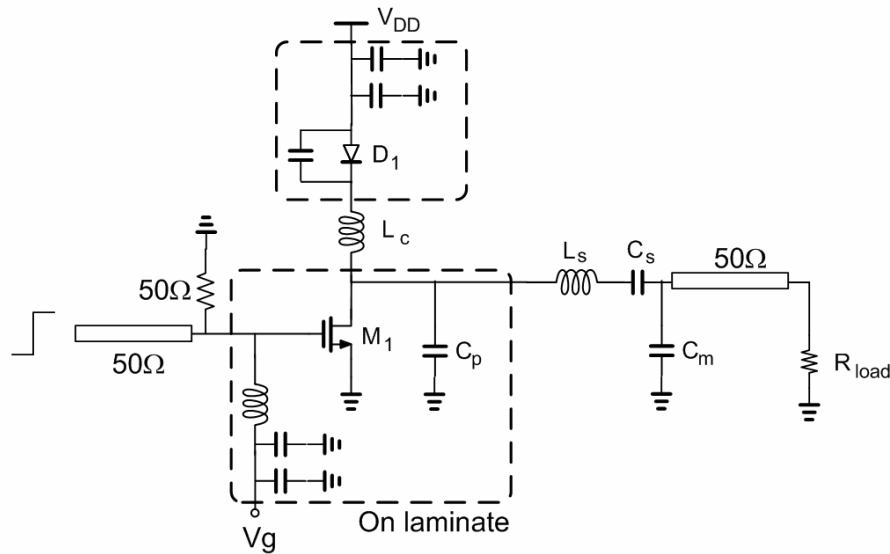


Figure 6.18: The schematic of the class-E amplifier prototype with the diode

A class-E amplifier with a diode was also implemented as shown in Fig. 6.18. The diode was also implemented on a laminate with a shunt capacitor. The diode has a width of 1mm. Due to the series resistance and the transition time of the diode, the class-E amplifier efficiency was degraded to 54% with an output power of 18.4dBm under the same bias conditions.

Two digital polar modulation signals with different sampling approach were generated in Matlab and sent to Agilent pattern generator. With an amplitude of $V_{p-p}=1V$, the output spectrum on a 50ohm load are shown in Fig. 6.19, Fig. 6.20, Fig. 6.21 and Fig. 6.22 for different frequency spans. Pattern A shows a IM3 of -40dBc and pattern B shows a IM3 of -60dBc. These results agree with the Matlab simulation well. The signal pattern B was chosen to perform the amplifier measurement because of the superior IM3.

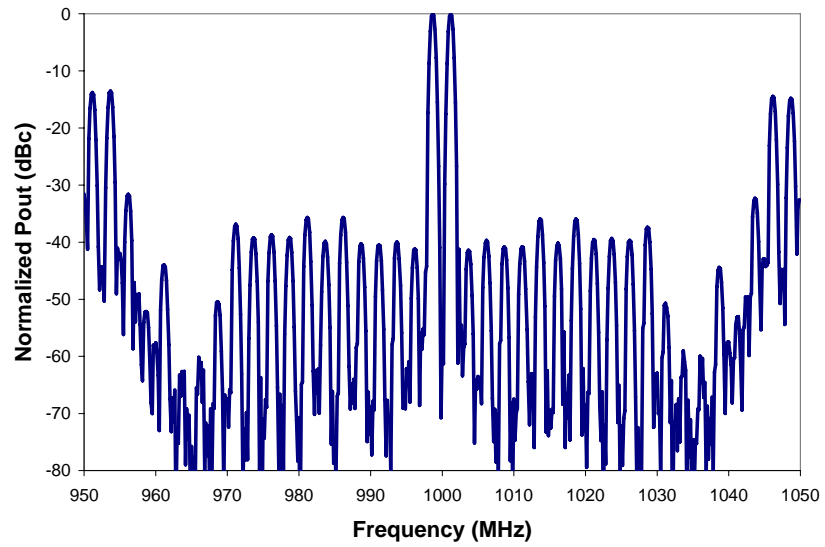


Figure 6.19: Measured spectrum of the digital pattern A (NB=40) with 100MHz frequency span

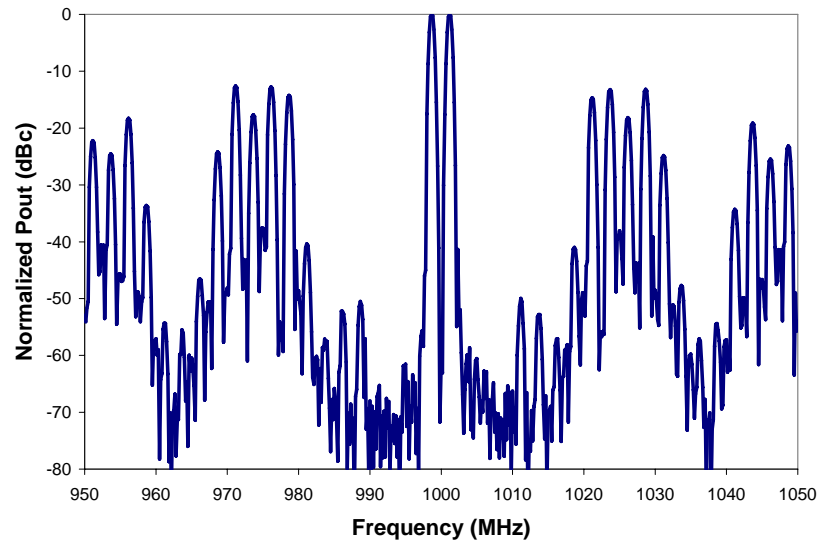


Figure 6.20: Measured spectrum of the digital pattern B (NB=20) with 100MHz frequency span

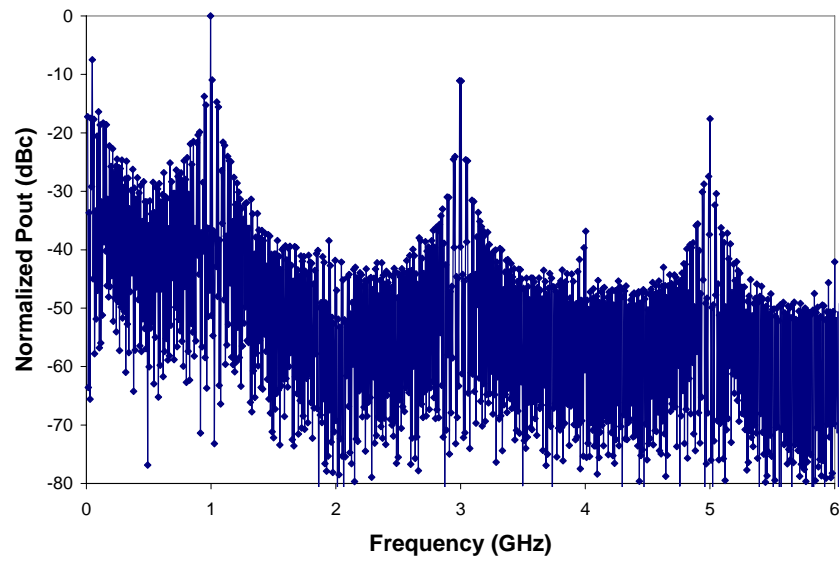


Figure 6.21: Measured spectrum of the digital pattern A (NB=40) with 6GHz frequency span

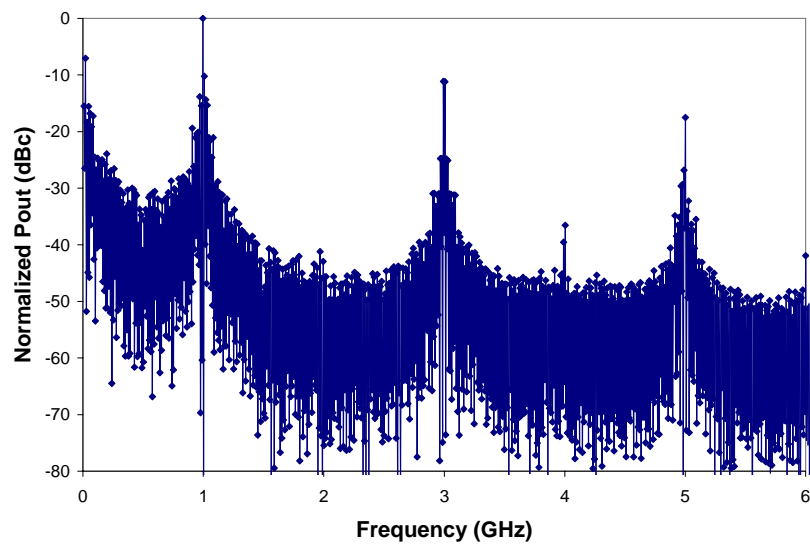


Figure 6.22: Measured spectrum of the digital pattern B (NB=20) with 6GHz frequency span

The maximum available voltage swing of the pattern generator output is only 2V peak-to-peak. This amplitude is not enough to drive the class-E amplifier to achieve the highest efficiency operation. Thus, a Mini-circuits broadband amplifier (ZLH-2) which has a bandwidth from 10MHz to 1GHz was used. Fig. 6.23 shows the

comparison of the normalized input and output signals of the broadband amplifier. The signals fidelity was maintained well around and below 1GHz. Only the harmonics were limited. An IM3 of -51dBc was achieved, verifying the signal quality. The output of the broadband amplifier was used to drive the class-E amplifiers directly.

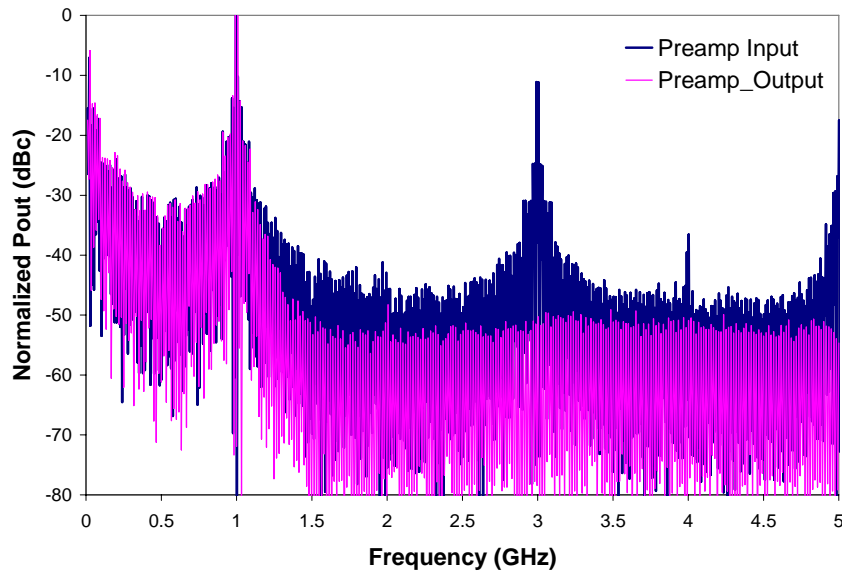


Figure 6.23: Comparison of the measured input and output spectrum of the broadband amplifier

The class-E amplifier output spectrum is shown in Fig. 6.24. Fig 6.25 shows that the amplifier generates no harmonic distortion and Fig.6.26 shows that a symmetric IM3 of -39dBc was achieved. The class-E amplifier can achieve an efficiency of 54% with an output power of 18.7dBm while driven by the broadband amplifier.

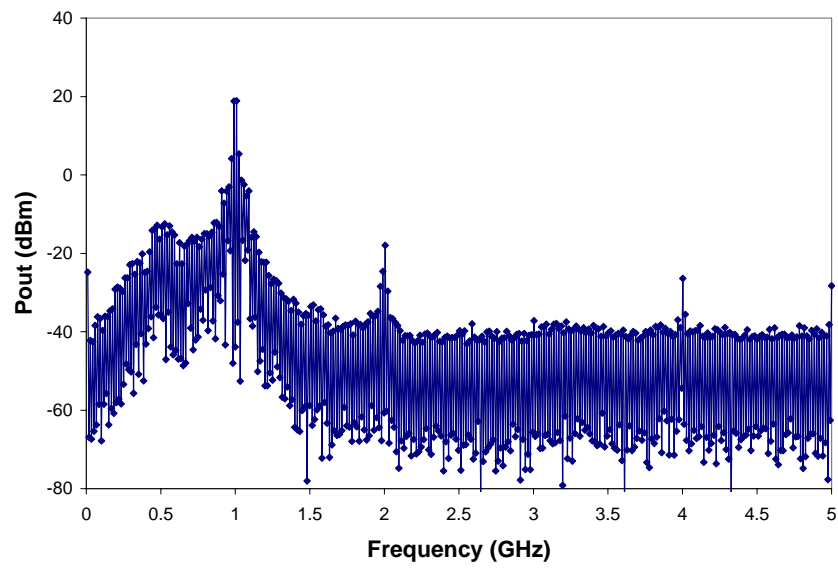


Figure 6.24: Measured output spectrum of the Class-E amplifier

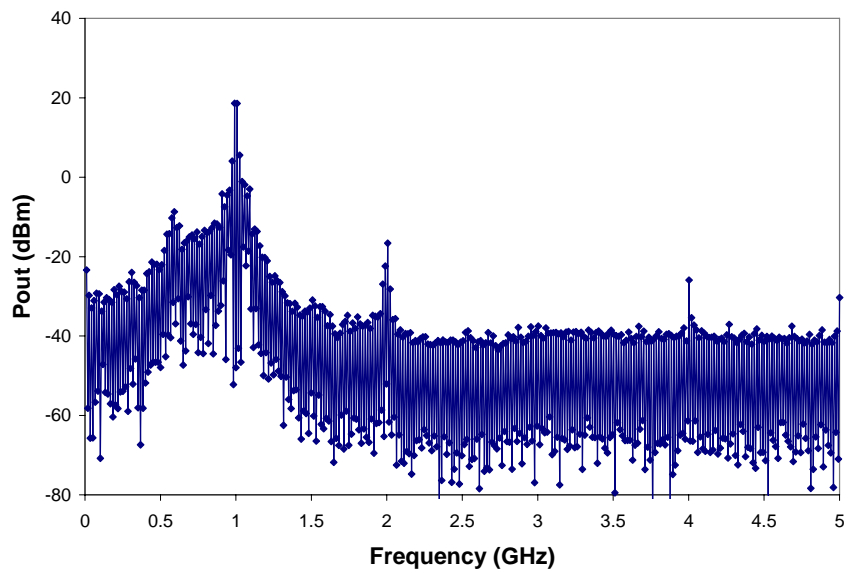


Figure 6.25: Measured output spectrum of the Class-E amplifier with diode

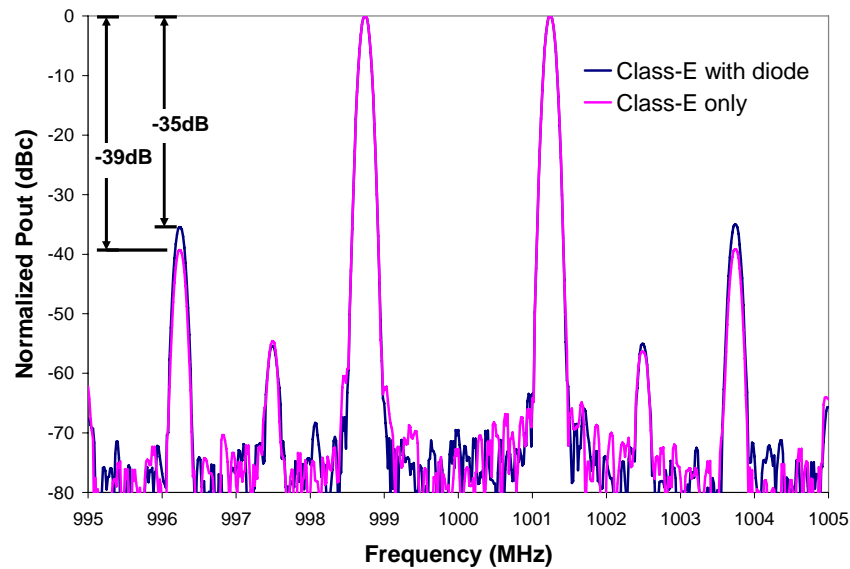


Figure 6.26: Comparison of the measured spectrum of two Class-E amplifiers

The class-E with a diode was also measured in a same way. Fig. 6.26 shows the amplifier output spectrum. A symmetric IM3 of -35dBc was achieved. The class-E amplifier can achieve an efficiency of 42% with an output power of 18.4dBm.

6.5 Summary and Discussion

A new digital polar modulation system with a class-E amplifier was investigated. The proposed modulation scheme is able to digitize the complex signals with relatively low clock frequency, 1GHz. The linearity was demonstrated with two-tone signals which are centered at 1GHz and have a frequency separation of 2.5MHz. The measured two-tone spectrum can achieve an IM3 of 60dBc for input drive signals using appropriate high performance signal generators.

With the assistance of a broadband amplifier, the system with a class-E amplifier can be evaluated. The class-E can achieve a drain efficiency of 54% with an output power of 18.7dBm and an IM3 of -39dBc. The class-E amplifier with the diode can achieve a drain efficiency of 42% with an output power of 18.4 dBm and an IM3 of -35dBc. The performance degradation is due to the parasitic resistance of the diode on the supply path.

The results show the potential of the modulation scheme and the amplifier configuration. This digital polar modulation system can be used for complex modulation signals, but there are several issues need further investigation.

1). *Spurious tones*: The superior IM3 was obtained by adjusting the sampling rate for the envelope. However, choosing $NB=20$ makes the spurious tone move closer to the signal band with only 20MHz offset. These large spurious tones lead to the issue of noise at receive band.

2). *Amplifier driving signals and input matching network*: To improve the amplifier efficiency, large device with less ON-state resistance is highly desired. However, larger device needs higher current driving capability of the driving stage due to the significant input capacitance. Narrow-band matching network can distort the wideband digital signals easily, so wide-band matching network which has flat frequency response over the bandwidth of the driving signals is necessary.

In this work, a broadband amplifier was used to drive the class-E amplifier. The IM3 at the broadband amplifier output can achieve a decent value of -51dBc. However, the absence of high order harmonic components in the input drive signal

due to the bandwidth limitation of the broadband amplifier may lead to ACPR regrowth for complex modulation signals such as CDMA.

3). *Energy saving during the OFF state of the switching mode amplifier:* When the envelope pulses are high (ON-state), the switching amplifier is driven by phase modulated signals, thus working in the high efficiency mode. However, saving or recycling the energy at OFF state is also critical. Creating a DC open and AC short on the drain of the active device to ground is a possible way to achieve the energy saving but the added components may degrade the efficiency due to the large series parasitic resistance.

6.6 References

- [1] J. Jeong and Y. E. Wang, "A Switching Mode Power Amplifier for Envelope Delta-Sigma Modulation (EDSM)," presented in *2007 IEEE Power Amplifier Symposium*
- [2] A. V. Grebennikov, and H. Jaeger, "Class E with parallel circuit – a new challenge for high-efficiency RF and microwave power amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1627-1630, 2002.

Chapter 7

Conclusions and Future Work

7.1 Dissertation Summary

With the progress of wireless communication technologies, increasingly advanced features of mobile devices are expected by users. Those advanced features usually require higher data rate and consume more power, resulting in reduced battery life. Switching mode amplifiers have drawn considerable attention in the wireless circuit and system design community because of their inherent high efficiency, initially demonstrated at audio frequencies. By solving the output capacitance loss issues, it has been shown that switching amplifiers can maintain these high efficiency characteristics at RF frequencies. However, their linearity needs improvement in order for them to be used in communication systems with non-constant envelope signals. This dissertation is dedicated to investigate the switching mode amplifiers for high efficiency and linear communication systems.

This dissertation begins with analysis of design considerations of current-mode class-D amplifiers. The efficiency of a CMCD amplifier can be estimated from the transistor and circuit parameters according to the analytical results presented here, providing a useful guide for circuit design. Technique for efficiency estimation of VMCD amplifiers is also provided in this thesis.

Experimental CMCD amplifiers with different integrated resonator structures are demonstrated, and shown to achieve high efficiency. An amplifier with a bondwire inductor can reach a collector efficiency of 78.5% at an output power of 29.5dBm (0.89W) with a maximum PAE of 68.5%. This current mode class-D amplifier is suitable for wireless systems with constant envelope modulation.

A prototype voltage-mode class-D amplifier implemented in CMOS technology is able to achieve a drain efficiency of 62% with an output power of 21dBm and a PAE of 45%.

Voltage-mode class-D amplifiers are demonstrated with an outphasing architecture for linear amplification. The load impedance of the amplifiers is analyzed and the limitation of using a Chireix combiner to maximize efficiency is discussed. A CMOS outphasing class-D amplifier was demonstrated at 800MHz. With the Chireix compensation technique, a drain efficiency of 48% was achieved (which represents an improvement factor of 1.24 compared to the PA without Chireix compensation). Without any predistortion, an ACPR of -45dBc was achieved. The combination of high efficiency and adequate linearity makes the outphasing PA an attractive candidate for use in all-digital transmitters.

Another approach to implement all-digital transmitters based on delta-sigma modulation is also investigated. A comparison of two and three level delta-sigma modulations is made, followed by the demonstration of an H-bridge Class-D amplifier for DSM CDMA signals at 800 MHz. A drain efficiency of 31% was achieved with an ACPR of -43dBc for two-level DSM signals, with an in-band power ratio of 30%. An

improved drain efficiency of 33% was achieved with an ACPR of -43dBc for three level DSM signals. The efficiency analysis shows the contribution of different loss mechanisms as function of output power. It is predicted that by reducing the output capacitance associated with the transistors, the amplifier efficiency can be improved significantly, especially in the low power region. The results indicate the feasibility and potential of using the H-bridge Class-D amplifier in digital RF transmitters with advanced transistor technologies.

In the final part, a digital modulation system including a novel modulation scheme and a class-E amplifier was investigated. The proposed modulation scheme separates the complex signals into envelope and phase signals and digitizes them separately. The envelope signals can be digitized in a pulse-width modulation format and the phase signals are digitized with a clock frequency which equals to the carrier frequency. After combining the digital envelope and phase signals, the signals are used to drive the switching-mode class-E amplifier. The linearity of the system was demonstrated with two-tone signals which are centered at 1GHz with a frequency separation of 2.5MHz. The class-E amplifier can achieve a drain efficiency of 54% with an output power of 18.7dBm and an IM3 of -39dBc (which corresponds to good linearity). The result makes the novel digital modulation system a promising configuration for wireless communication systems.

7.2 Conclusion

In this dissertation, several circuit and system options for use of switching-mode power amplifiers in wireless communications are investigated and analyzed

including current-mode class-D amplifiers, outphasing amplifier systems, voltage-mode class-D amplifier with delta-sigma modulation and class-E amplifier with digital polar modulation. Table 7.1 shows the summary of the pros and cons of these techniques.

Table 7.1 Summary of pros and cons of the investigated techniques.

	PROS		CONS		
	ZVS	Linear Amplification	High clock rate	Rx Band Noise	CV ² loss
CMCD PA	√				
Chireix PA System		√			√
VMCD PA with DSM		√	√	√	√
Class-E with DPM	√	√		√	

The CMCD amplifiers can alleviate the output capacitance loss issue and be operated efficiently by achieving ZVS (zero-voltage-switching) condition. Therefore, they are suitable for constant envelope modulation systems such as GSM. However, this advantage is no longer valid if the CMCD amplifiers are driven by signals with a duty-cycle far away from 50%. The non-zero voltage across the output capacitor at transitions can degrade the amplifier efficiency considerably. This result indicates that CMCD amplifiers do not have the ZVS advantage over VMCD amplifiers for use in a pulse-width modulation system.

The Chireix PA system was demonstrated and shows linear amplification with VMCD amplifiers. The efficiency is comparable to the results which present

commercial products implemented with III-V devices can provide (around 35%). According to the loss analysis, the efficiency can be further improved by using the advanced technology with low device output capacitance. However, the amplifier performance suffers from mismatch between two amplifier branches, and load impedance mismatch.

A VMCD amplifier with DSM is able to provide linear amplification but high sampling-rate is required to obtain digital signals with adequate linearity (a clock rate of 4X carrier frequency is used in this work). This higher switching-rate requirement leads to more power loss due to the charge/discharge of the device output capacitance.

Recently, advanced technologies such as GaN and SIO (silicon-on-insulator) give an opportunity to solve the output capacitance loss issue. A Class-F amplifier implemented with GaN technology was reported [1]. A PAE of 85% was achieved with an output power of 47dBm. The results show the potential of applying the low capacitance technology to switching mode amplifiers.

Due to the limit availability of p-channel devices in present GaN technology, a special driving technique is required for the topologies with complementary devices such as voltage-mode class-D. Transformers have been widely used to drive the complementary circuits, especially in audio frequencies applications. However, due to the bandwidth of the digital modulation signals, the transformers used in this application require wide bandwidth in order to preserve the digital waveforms such that the circuits can be driven by two exactly complementary digital signals. For SOI

technology, p-channel devices are usually provided, so there is no additional driving technique required.

In addition to the capacitance loss problem, two issues need to be addressed for the use of switching-amplifiers in wireless communication systems. As shown in Table 7.1, the issue of noise in the receiving band is still an important common problem for the amplifier system with pulse-width modulations. The frequency spacing between is usually much smaller than the carrier frequency (20MHz spacing for CDMA IS-95 signals). With such a narrow spacing, filtering the noise in the receiving band requires a high Q filter which can be only implemented in a bulky fashion and is not suitable to be integrated within portable devices. Other options may be helpful to the issue such as using the rejection of duplexer which provides 40~45dB rejection at receiving frequencies, or creating zeros in receiving band by the delta-sigma modulator. However, it is still a challenge to achieve the required suppression.

Another issue is that the switching mode amplifiers usually exhibit low power gain. To operate the active devices as switches, large signal swing at the amplifier input is necessary to turn on/off the transistor in a relatively short time and as a result it is difficult to obtain a high power gain at switching amplifier stage. For some digital transmitter systems employing wide-band digital modulation signals, a narrow band matching network is not adequate to preserve the digital input waveforms with wide bandwidth, so this issue becomes worse. This issue can be possibly solved by using a transistor technology with less input device capacitance or improving the modulation

scheme such that the narrow band matching network does not degrade the signal fidelity significantly.

Although some remaining challenges have been indicated above, switching mode amplifiers have shown a great potential to be used in wireless communication systems with the promising results shown in this work. By combining linear-amplification techniques such as delta-sigma modulation, Chireix system, or digital polar modulation, high linearity and high efficiency switching amplifier configurations are very attractive possibilities for modern communication systems.

7.3 Future Work

7.3.1 Effect of Load Mismatch on Outphasing Amplifiers

As discussed in Chapter 4, the outphasing amplifier can utilize Chireix power combining technique to improve the system efficiency in the low power region through load-pulling effect. In this work, an ideal load impedance of 50ohm is used for analysis and experiment. In reality, the load impedance of the amplifier may vary due to the fact that the input impedance of the antenna can vary over a wide range according to the usage environment (characterized by a voltage standing wave ratio (VSWR) of up to 10:1). This large impedance variation causes degradation in efficiency and linearity of outphasing amplifiers. Investigation of this load mismatch effect is suggested to quantify the possible performance degradation.

One of the possible solutions is applying predistortion to the input digital signal based on the load impedance which can be detected by the load impedance measurement technique [2].

7.3.2 Digital Pulse Modulation Signal Generation

A new modulation technique has been demonstrated with two-tone signals in Chapter 6. It is shown that both spurious response of the digital signals and amplifier efficiency depend on sampling of the envelope signal and the positioning of pulses. The measurement shows promising results for two-tone signals. However, to use this technique in more complex modulation systems such as CDMA, it is still a challenge to achieve linearity and spurious response due to more stringent requirement. It is worth investigating that using other techniques such as delta-sigma modulation to digitize the envelope signals.

7.4 References

- [1] D. Schmelzer, and S. I. Long, "A GaN HEMT Class-F Amplifier at 2GHz With > 80% PAE," *IEEE J. Solid-State Circuits*, vol.42, no.10, pp.2130-2136, Oct. 2007.
- [2] D. Qiao, D. Choi, Y. Zhao, D. Kelly, T. P. Hung, D. Kimball, M. Li, and P. Asbeck, "Antenna Impedance Mismatch Measurement and Correction for Adaptive CDMA Transceivers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2005, pp. 783-786.