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AN INVESTIGATION OF DEPLETION IN ASTROPIX, A HIGH VOLTAGE MONOLITHIC CMOS SENSOR

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Abstract

An Investigation of Depletion in Astropix, a High Voltage Monolithic CMOS Sensor

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Future space based particle physics experiments require detectors to be low power to ensure efficiency where no large amounts of energy can be continuously provided. The AstroPix chip aims for a power consumption of $1.5mW/cm^2$ and energy resolution of 2% at 600keV per sensor. To determine the readiness of several wafers of different resistivities, 3 experiments were conducted. CV and IV data were taken using a probe station in SCIPP's electronics room. The results determined that while the IV relationship looked normal for sensors with lower resistivities (from wafers 2 and 6), the sensors with higher resistivities (from wafers 10 and 11) had much higher current than anticipated, which inhibited the use of high voltage as breakdown occurred early.

Another experiment consisted of taking data from a laser edge-TCT scan; this test confirmed the strange behavior of high resistivity chips as voltage amplitude pulses lost their shape and amplitude with higher bias voltages which is contrary to intuition and the behavior of the lower resistivity chips. This led to the idea that with a high enough bias voltage, the leakage current incapacitates some of the transistors in W10 and W11 chips.

The last experiment conducted was an infrared radiation scan of certain chips with the intention of furthering the investigation of the aforementioned anomalies. The result was that the backs of the high resistivity chips had different potentials than the fronts of the chips; when conducting tape was used on the backside of these chips, the current hit

compliance (10mA) at a low voltage (10V). However, when using insulating tape or testing the chip on a metal chuck with probes in the high voltage and grounding pads, the chip was able to reach a higher voltage (220V) with the same current limit. This test shed light on instances of higher power dissipation along the edges of certain chips which led to ideas about design flaws and differences in how different chips distributed current and dissipated power.

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To my parents,

Jill and Bill,

Thank you for always supporting me.

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1

Introduction

1.1 Motivation

AMEGO-X or All-Sky Medium Energy Gamma ray Observatory eXplorer is a MIDEX (medium-class explorer) mission that uses particle physics technology to detect and reconstruct medium-energy gamma rays, focusing on the MeV range [1]. Gamma rays in the sky have energies ranging from 20keV-10GeV. These particles teach us about high energy astronomical events including short gamma ray bursts and active galactic nuclei. Information provided by Nasa's AMEGO-X mission will provide insights into the types of cosmic rays within our universe by creating a detailed "all-sky map" of gamma ray source and emission locations [2]. In order to localize these events well enough to accurately track and remap the trajectories of particles from photoabsorption, Compton scattering, and pair production–three processes of interaction between high energy photons and other materials– the detector must have high resolution, low noise, and low power [1]. AstroPix, a monolithic silicon sensor which uses high voltage complementary metal oxide semiconductor technology
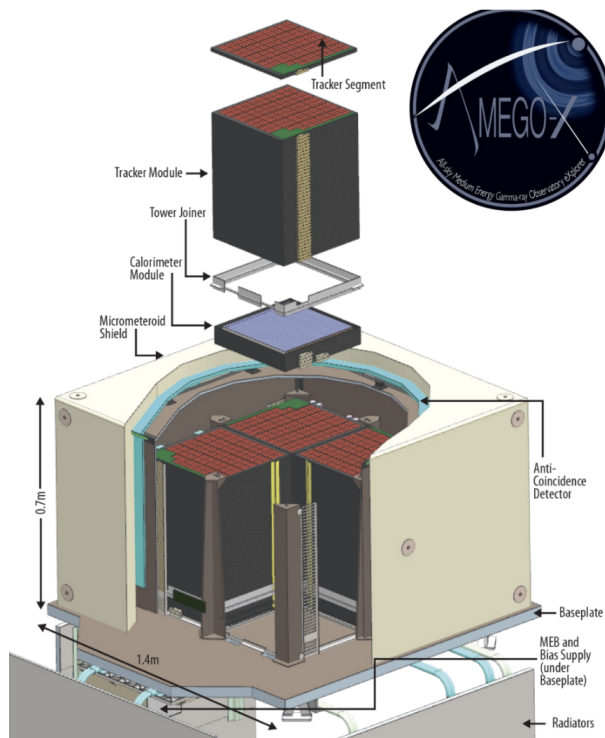
Figure 1.1: AMEGO-X schematic [3].

(HV CMOS), is being tested and developed for use in this mission and future space based missions [1]. AstroPix chips have low power consumption, are self triggered (read out only active 'hits'–amplitudes caused by a particle moving through the sensor), and are able to target the MeV energy range of passing particles [3].

The Electron Ion Collider (EIC) is said to be the future of nuclear physics. The collider is composed of two particle accelerators: one moves a beam of electrons, and the other moves a beam of protons or heavier atomic nuclei. Both beams move close to the speed of light and eventually intersect in order to effectively image within particles. This will give insight into the strong nuclear force that binds quarks and gluons within the nucleus as well as help explain the layout of quarks and gluons within protons and neutrons. This important information will help explain how gluons might carry so much mass and clarify
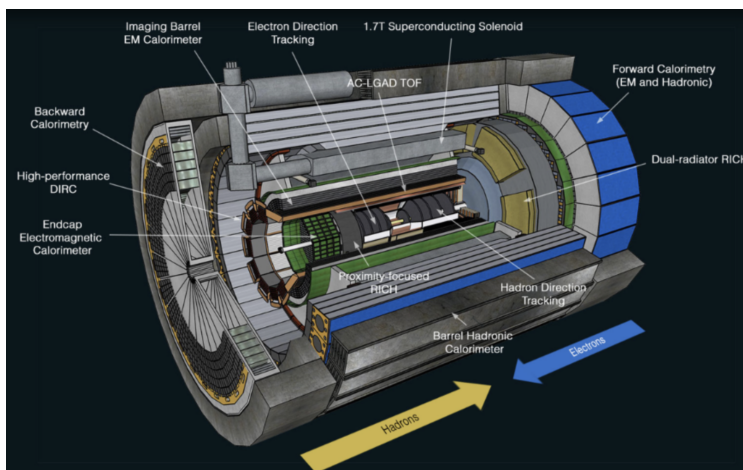
Figure 1.2: Diagram of EIC [5].

how much quarks versus gluons contribute to defining a particle's spin [4]. Within the collider, there are several calorimeters. A calorimeter is a device that measures the energy lost by a particle as it passes through. The EIC's barrel imaging calorimeter will be used to measure the energies of particles that spray off from the interaction after high energy electrons scatter off of a quark [5]. AstroPix is ideal for use in the barrel imaging calorimeter due to its high performance in low energy pion and electron separation, and its exceptional energy and position resolution [3]. This high resolution allows for accurate tracking and mapping of particle showers during each interaction.

1.2   Silicon Technology

Silicon has come to dominate modern technology and electronics due its efficiency as a semiconductor. Semiconductors are comparable to insulators in a low temperature regime and comparable to conductors in a high temperature regime [6]. Doping is the process of controlling the conductivity of a semiconductor by infusing impurities into the

naturally pure silicon crystal lattice [7].

In n-type doping, impurities such as Phosphorus (with five valence electrons) are introduced into the environment almost entirely dominated by Silicon (with four valence electrons). Therefore, as Phosphorus takes a spot in the crystal lattice, there is an extra electron that is only lightly bound to the atom it came from; this electron is able to move about the lattice when an electric field is present [7]. This is the n-type bulk.

In p-type doping, impurities with three valence electrons–such as Boron–are introduced into Silicon's crystal lattice. Here, one of Silicon's valence electrons is left unpaired, essentially creating a hole and the p-type bulk. This hole is able to move around within the lattice as nearby electrons (one at a time) move to fill it [7].

When n-type and p-type regions are combined, thermal diffusion causes the electrons to move toward the p-type region and holes to move toward the n-type region. This results in a junction which contains static positive charges on one side and static negative charges on the other side. Past the junction, the bulk areas contain mobile charge carriers; on one side there are positive mobile charge carriers and one the other side there are negative mobile charge carriers [7].

In applying voltage, one can either forward bias (allowing the current to flow naturally) or reverse bias the diode. Reverse biasing is when negative potential is applied to the p-region and positive potential is applied to the n-region. The positive charge carriers in the p-type region are attracted toward the negative terminal and vice versa, causing the depletion depth to increase as the potential barrier is increased [7]. The depletion region's depth is defined by Equation 1.1
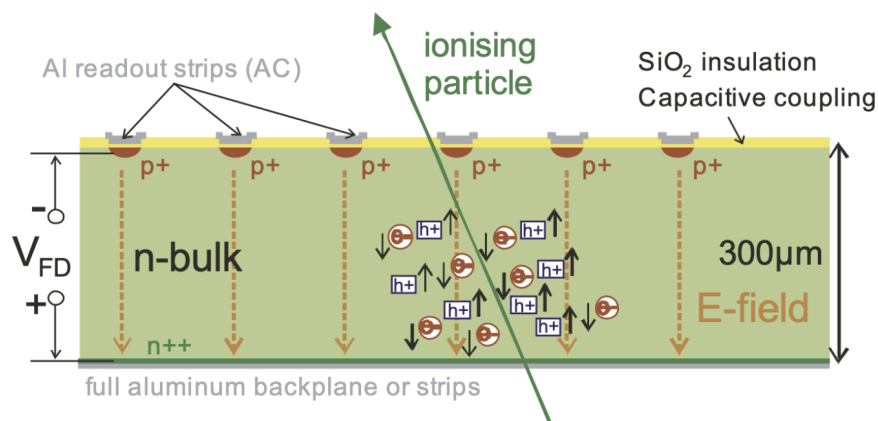
Figure 1.3: Cross section of a pn-junction with bias voltage [7].

$$depth = \sqrt{2\epsilon\sigma\mu V_{bias}} \tag{1.1}$$

where ϵ is the permittivity, σ is the resistivity of the bulk, and μ is the mobility (where we often use $\sigma = \frac{1}{e\mu N_d}$ where N_d is the donor dopant density) [7]. Current increases with $\sqrt{V_{bias}}$ until the sensor is fully depleted and can therefore act as a detector [7]. The structure of the pn-junction and depletion depth is depicted in Figure 1.3.

Increasing the bias voltage increases the signal charge and decreases noise as a particle passes through the detector, but voltage should only be increased up to breakdown [6]. "Breakdown" happens when the voltage and electric field become too high and electrons begin making secondary electron-hole pairs, which induces positive feedback, increases noise, and causes a sharp increase in current which can damage the sensor [6]. Power consumption of the sensor is defined by leakage current, which is defined by thermal flow of electrons and holes to the pixel junctions, and which is correlated with noise. Specifically, leakage current is defined in Equation 1.2

$$I_L = \frac{e n_i w A}{2 \tau_L} \tag{1.2}$$

where n_i is the intrinsic carrier density, w is thickness, A is the junction surface area, e is the elementary charge of $1.6 * 10^{-19}$ C, and τ_L is generation lifetime of minority carriers [7].

1.3 Complementary Metal Oxide Semiconductor - Monolithic Active Pixel Sensors (CMOS-MAPS)

'Complementary metal oxide semiconductors' refers to the type of circuitry used in electronic readout devices; CMOS use PMOS (P-channel metal oxide semiconductor) and NMOS (N-channel metal oxide semiconductor) transistors in conjunction; Figure 1.4 shows a cross section of this layout. When a signal from a sensor reaches the CMOS device, the signal is amplified and a comparator (enabled by the NMOS transistor) determines whether the signal is large enough to pass on. This signal is then put through a readout cell which filters unwanted signals/noise to help determine the true shape of the pulse. The signals from each readout cell within one column go through an end-of-Column cell, where a digital control units reads out the data, in the form of a Time over Threshold (ToT) step function that determines how long the given signal had amplitude greater than that of a predetermined threshold. The control unit therefore formats the information and sends it out of the cell with a time stamp [9]. Externally (within the oscilloscope), the pulse is reconstructed by taking averages of several pulses and by comparing the pulse geometries to theoretical shapes.
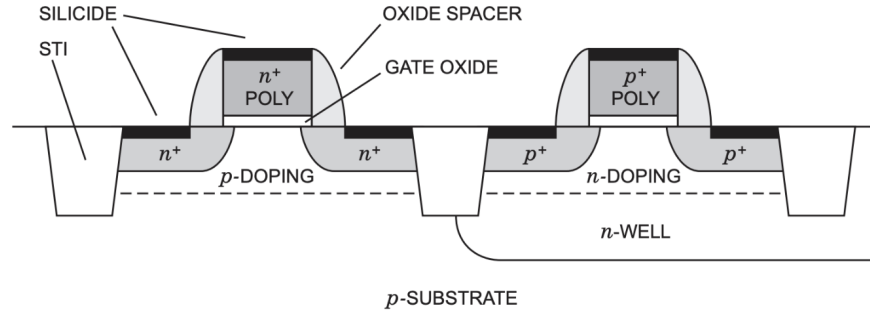
Figure 1.4: Cross section of a typical CMOS structure. An NMOS transistor is on the left and a PMOS transistor (which is separated from the p-substrate by an n-well) is on the right. p^+, doped polysilicon, and n^+, doped silicide are the gate electrodes which sit on top of the oxides and regulate the current within the transistor channels [6].

MAPS (monolithic active pixel sensors) use classical silicon semiconductor technology, but are 'monolithic', meaning that there are both detector and data digitisation technology present [8]. Specifically, these sensors are connected to readout devices–CMOS electronics for CMOS-MAPS like AstroPix–within each pixel, meaning that there is no need to bump or wire bond sensors to readout devices. Considering that the plans for AstroPix (both the EIC's barrel imaging calorimeter and AMEGO-X) will utilize thousands of sensors, there will be several million fewer wire bonds due to this technology. This directly influences installation time and causes lower noise and lower power consumption. Figure 1.5 depicts the general steps in the CMOS electronics, with a sensor present.

While CMOS-MAPS chips are useful in collider based particle physics due to their high radiation tolerance, this technology is ideal for use in space considering the low power consumption and high precision within an energy range that allows for Compton scattering, photoabsorption, pair-production [8].
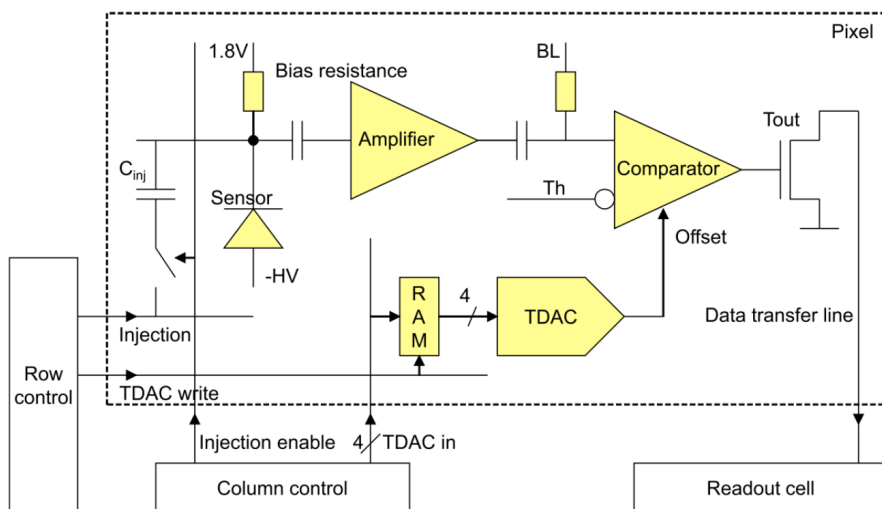
Figure 1.5: Monolithic CMOS electronics within each pixel [9].

1.4 AstroPix Background

AstroPix have been developed through iterations of ATLASPix, pixel sensors built for use in a ground-based particle accelerator. By optimizing certain functionalities such as power consumption, pixel size, and detector readout, AstroPix were created with the intention of space-based gamma ray detection [10].

Several versions of AstroPix have been developed (from V1 to the new V4) but all experiments mentioned in this thesis regard V3. The projected finish of the project is with a V5 chip, which will address the intended power consumption, depletion depth, and other characteristics, presented in Table 1.1 and Table 1.2.

Pixel pitch	Thickness	Power consumption	Dynamic range	Energy resolution
$500x500 \ \mu m^2$	$500\mu m$	$< 1mW/cm^2$	$25keV - 700keV$	$< 10\%(FWHM)at60keV$

Table 1.1: Requirements for AstroPix to be accepted for use in AMEGO-X [14].

Version	V1	V2	V3	V4	V5
Pitch	$175\mu m$	$250\mu m$	$500\mu m$	$500\mu m$	$500\mu m$
Power dissipation	$14.7\frac{mW}{cm^2}$	$3.4\frac{mW}{cm^2}$	$< 1\frac{mW}{cm^2}$	$< 1\frac{mW}{cm^2}$	$< 1\frac{mW}{cm^2}$
Pixel matrix	$18x18$	$35x35$	$35x35$	$16x16$	$35x35$

Table 1.2: V1-V5 Dimensional changes [3].

The earlier iteration of the sensor (V1) had smaller pixel pitch (less than 250 by 250 microns) and a smaller chip, resembling the dimensions of pixels and chips used, for example, in the pixel sensors of the ATLAS experiment. An important improvement from V1 to V2 is that the pixels of V2 are equipped with technology for recording the digital data instead of solely the analog data, leading to a more digitised version of the chip. Version 3 hits the AMEGO-X pixel pitch requirement of 500 by 500 microns, which is notably larger than that of the previous versions. Version 3 is also equipped to meet the requirement for the power consumption of $< 1mW/cm^2$, though the power of the high resistivity chips that have been tested at SCIPP show a higher power consumption than expected. V4 will begin to be tested in 2024 and 2025, and V5 will follow shortly after, with no scheduled changes except for bug fixes to V4.

1.5 Experimental Theory

1.5.1 CV and IV testing

Conducting Current-Voltage (IV) and Capacitance-Voltage (CV) tests are an important step in learning about the basic relationships between current, voltage, and capac-

itance. Specifically, IV tests are often used to determine leakage currents and breakdown voltages. Leakage current increases linearly until breakdown voltage is reached, where current will sharply increase. CV tests are used to determine doping concentrations and depletion depths. In a detector, the space charge region–or depletion region–is free of mobile charges and can be treated as a parallel plate capacitor with a silicon dielectric inside; capacitance increases linearly with $\frac{1}{\sqrt{V}}$ as shown by Equation 1.3

$$\begin{cases} C = A\sqrt{\frac{\epsilon_{si}}{2\sigma\mu V_{bias}}} & \text{for } V_{bias} \leq V_{fulldepletion} \\ C = \frac{A\epsilon_{si}}{D_{depletion}} = constant & \text{for } V_{bias} > V_{fulldepletion} \end{cases} \tag{1.3}$$

[6], [7]. Together, these tests provide useful information about the possible different trends within AstroPix chips of different resistivities. The IV tests for this experiment are also coupled with the laser edge-TCT scanning as multiple chips were tested before and after edge polishing to ensure that edge polishing (an important step before the laser scanning can be done) does not alter breakdown voltage or leakage current values.

1.5.2 Laser Edge-TCT Scanning

Laser Edge Transient Current Technique (e-TCT) is an efficient way to measure the depletion in a silicon sensor by using an infrared laser to induce a transient signal on the detector's edge to scan the depth of the pixel [11]. In this test, it is ideal for the edge of the sensor to be polished so that a scan along the thickness does not include laser reflections off sharp edges or blurred distinctions between the depletion depth and bulk.

The data is collected and analyzed using a Particulars laser setup and creating 1 and 2 dimensional histograms comparing voltage amplitudes at different positions for each

chip over a range of bias voltages.

The e-TCT technique measures depletion depth by picking up on signal current. When a bias voltage is applied to the AstroPix, each pixel undergoes depletion due to the induced electric field. The laser pulse induces charge carriers (electrons and holes); in the space charge region, the electric field present causes the new, non-static electrons and holes to quickly (depending on the bias voltage) drift toward the electrodes on the top and bottom surfaces of each pixel. This movement of charge generates a current which is tracked and amplified through the sensor electronics. The amplification and shaping digitises the pulse into a more uniform, readable form that is displayed on the oscilloscope; though the pulse is representative of the current, the timing and shape might be different on the oscilloscope than in the sensor.

There should only be signal current where the laser induces charge carriers into the depletion region. In the undepleted bulk (which is essentially conductive), electrons and holes are non-static and generally recombine as the electric field is not present–except for a small gradient–to cause drift and induce a current which causes a signal.

By studying the resulting histograms, we can determine how large the depletion regions are for certain pixels for a multitude of bias voltages.

1.5.3 Infrared Mapping

After conducting IV and CV tests and performing the laser edge-TCT scan for the variety of AstroPix chips with different resistivities, there was a constant issue for the high resistivity (Wafers 10 and 11) chips in that the current was unusually high for the voltage applied, and the voltage amplitude decreased when bias voltage increased. This unusual

behavior led to the hypothesis that there might be a specific location or locations on the surface of the chip where the current or voltage was being disrupted. Additionally, this high leakage current means that the chip is dissipating more power than it should, and these 'locations' might correspond to where the high power onset might be.

When objects have a temperature greater than zero, the atoms and molecules within these objects vibrate and oscillate due to thermal energy. These oscillations of charged particles inside atoms produce electromagnetic radiation, therefore giving off light [12]. Also, within circuits, resistors turn diffusive energy from a battery or power source into heat energy in the form of Joule heating. When current running through the circuit is abnormally high, this means an abnormally high amount of energy is transferred into heat, resulting in higher temperatures than normal.

In this experiment, AstroPix chips are placed in a dark environment to minimize interference with other sources. When the sensor is biased, it gains energy. Planck's law describes the relationship between the distribution of emitted electromagnetic radiation and the energy density of the body at a certain temperature (T). The energy density is given by

$$E = \frac{2\pi h v^3 n^2}{c_0^2 [e^{\frac{hv}{kT}} - 1]} \tag{1.4}$$

where h is Planck's constant, c_0 is the speed of light in the material, v is frequency, and k is the Boltzmann constant [12]. Therefore, the distribution of wavelengths emitted by an object depends on the object's temperature. Namely, the emitted spectrum of wavelengths shift to smaller values as the temperature of the body increases.

The higher current that was evident from the probe station IV tests contributes

to a higher power consumption throughout the circuit as ($Power = VI$) and the higher power means more energy, ($Power = \frac{Energy}{Time}$), which radiates as heat as is detected by the camera.

The thermal IR camera is able to pick up on the infrared spectrum of electromagnetic wavelengths, similar to a normal camera, but for a different range of wavelengths of light. The radiation emitted by the sensor hits thousands of detectors on the surface on an infrared camera's sensor which then filter the wavelengths of radiation and calibrate these values to report an apparent temperature of the object based on the quantity and wavelength of radiation [13]. Thus, this infrared camera was used to identify the locations on the chip of higher current, to spot a possible manufacturing issue with Wafer 10 and 11 sensor circuitry.

2

IV and CV Testing

2.1 Procedure

A probe station in SCIPP's electronics room was used to perform IV and CV tests on sensors with varying resistivities. This station consists of a microscope, a circular copper plate, various connections, and a light blocking door. Two micron-fine tungsten probes are cleaned prior to use. By using a microscope with concentrated light from a fiber optic illuminator, I could correctly position the two probes onto the sensor; one touched down on the high voltage pad and one touched the grounding pad. Each of the probes is connected to a power supply, with HV and ground inputs respectively. To ensure that the metal probes are in contact with oxidization openings in the pads, the surface of the sensor on those pads are first scratched into, where a vacuum hole under the center of the sensor suctions down to prevent movement. Figure 2.1 shows the setup for these tests.

Upon confirming this contact, the metal door is placed on and the light through the microscope is turned off. Though particle detectors including AstroPix detect ionizing

Figure 2.2: Microscope point of view; The probe to the left makes contact with the HV pad and the probe to the right makes contact with the ground pad.

Figure 2.1: Probe station setup.

radiation, these detectors and especially small pixels can have sensitivity to non-ionizing radiation, such as from the visible light spectrum. Therefore it is important for the sensor to be in a dark environment while testing [6]. Additionally, exposure to light during an electrical test can cause a high leakage current due to the photoelectric effect, which might damage the sensor.

After turning on the power supply, an Automated Data Acquisition Program is used to apply a range of voltages over a certain time frame to create precise IV and CV curves. For both tests, the bias voltages ranged depending on the sensor used while the current compliance depended on what type of test was being performed as well as the resistivity of the sensor. The tests concluded when either the current compliance was hit, or the ending voltage had been applied. The voltage decreased (the absolute value increased) in steps of a set value instead of a continuous flow; generally the step size was 2V. Table 2.1

notes which sensors were tested, and when.

Chip name	Test	Resistivity	First date tested
W11S04	CV/IV	10k Ohm-cm	Oct 31
W11S03	CV/IV	10k Ohm-cm	Nov 9
W10S10	CV/IV	10k Ohm-cm	Oct 31
W10S09	CV/IV (p)	10k Ohm-cm	Nov 7
W08S12	CV/IV (p)	200-400 Ohm-cm	Oct 28
W06S12	CV/IV (p)	200-400 Ohm-cm	Oct 28
W02S09	CV/IV (p)	20 Ohm-cm	Oct 28

Table 2.1: Chips used for IV/CV.

The (p) next to several of the tests denotes that that sensor had an edge polished. Specifically, IV and CV data was taken before polishing, and IV data was taken after polishing, to determine whether or not edge-polishing a chip affected the breakdown voltage. The polishing was done by Aware Deshmukh and Figures 2.3 and 2.4 depicts a chip before and after edge polishing.

2.2 Results

2.2.1 IV

The next six plots show the IV characteristics of sensors from wafers 2, 6, 8, 10, and 11. More specifically, the pre-polish and post-polish relationships are depicted in the
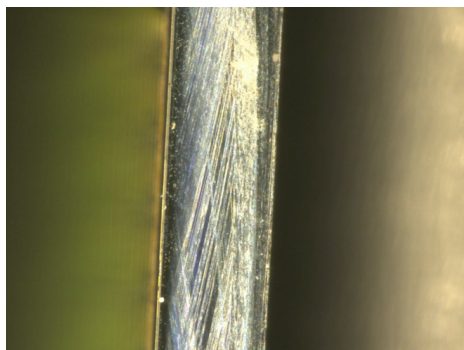
Figure 2.3: Pre-polished edge: scratches are visible.
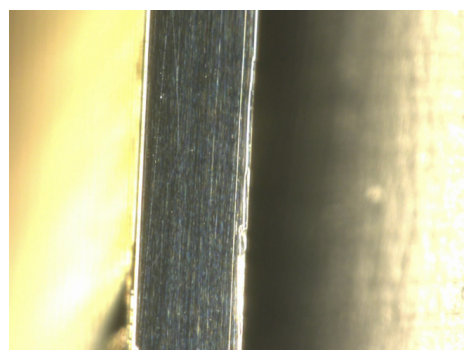
Figure 2.4: Post-polished edge: for the most part, the edge is smooth free of scratches.

next four plots where they are separated by the low and mid range of wafer resistivties and the high range of wafer resistivties. They are additionally separated by linear versus logarithmic scales.

The IV curves (pre-polish) for wafers 10 and 11, containing various tests for each sensor, are shown in the next two plots. The first plot shows a low voltage range, with current compliance at either $50\mu A$ or $100\mu A$ while the second plot shows a special high voltage range for various high resistance sensors, with current compliance abnormally high, at $10mA$.

2.2.2   CV

The following three figures show CV tests for wafer 2, wafer 8, and wafer 10/11. They also include a theoretical function, which depicts the linear relationship between $\frac{1}{C^2}$ and bias voltage, to show generally how the sensors should function in this test given the individual resistivities.
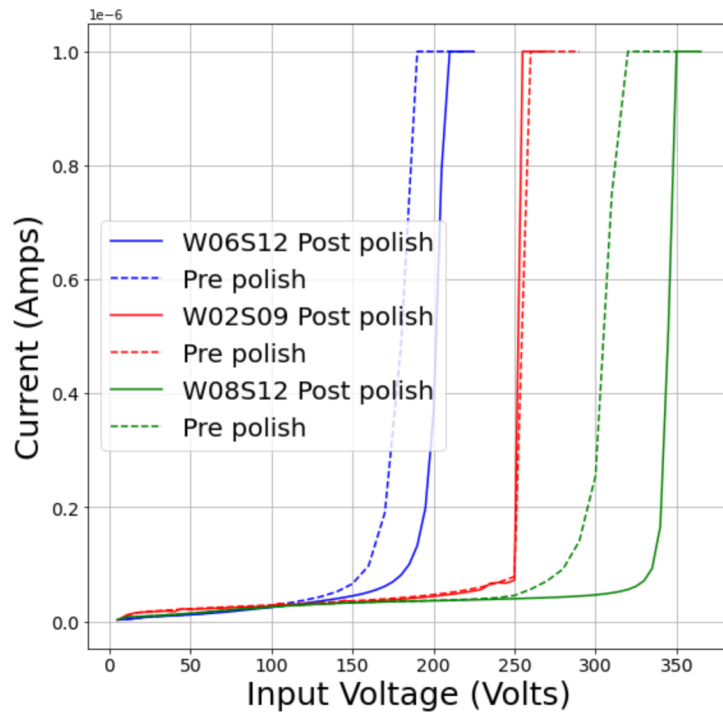
Figure 2.5: Pre/post edge polishing IV for W02S09, W06S12, W08S12.

2.3   Analysis

IV curves provide breakdown voltages and leakage current values. Over the range of applied voltage, the leakage current should have a small positive slope until the voltage hits breakdown; here, there should be a sharp exponential increase in the current.

Breakdown voltages can be estimated by determining the intersection between a quasi-linear, low slope trend and a sharp exponential increase. Once the breakdown voltage has been applied, the leakage current rapidly increases as a function of voltage. Current compliance is often set just over breakdown voltage to ensure that the current does not exceed a dangerous level for the sensor.

From Figure 2.5, each plot shown exhibits the expected behavior of an IV-curve. When considering the relationships between pre and post-polishing, each wafer is different.
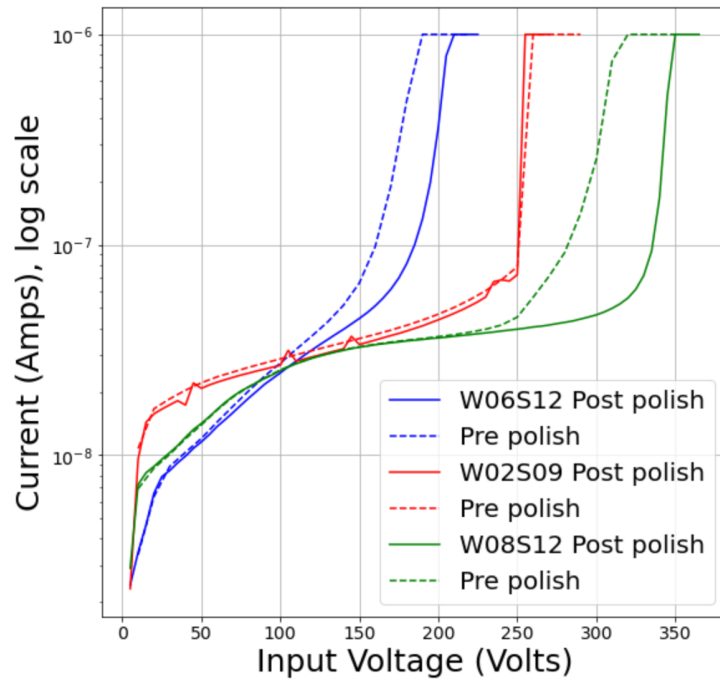
Figure 2.6: Pre/post edge polishing IV (log scale) for W02S09, W06S12, W08S12.

Wafer 2 exhibits no large change as breakdown is consistently around 250V regardless of polishing status. W6 exhibits a small change, where breakdown voltage increases post polish. Wafer 8 shows the biggest change between polishing, where the change in breakdown voltage is about twice the value of the W6 change. In Figure 2.7, the pre and post-polishing values are starkly similar. While this is encouraging that the polishing process does not disrupt breakdown voltages for this wafer, the breakdown values here are very

W06S12 post	W06S12 pre	W02S09 post	W02S09 pre	W08S12 post	W08S12 pre
175V	140V	250V	250V	330V	260V

Table 2.2: Estimated breakdown voltages for Figure 2.5. "post" refers to post polishing and "pre" refers to pre-polishing.
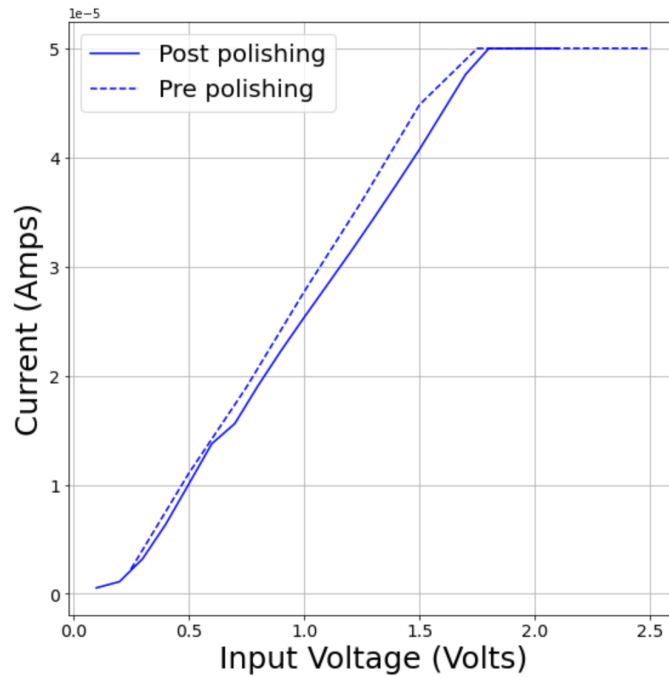
Figure 2.7: Pre/post edge polishing IV for W10S09.

difficult to estimate. The plot shows linearity with no exponential rise. Additionally, compliance is hit after only about 1.75V applied. Though the high resistance requires that less bias voltage is applied to reach the same depletion depth as lower resistivity chips, the voltage should still surpass a few hundred volts without returning such high current values. Considering the low voltage tests from Figure 2.8, the current is consistently higher than normal. The shapes of the plots are also unusual; each test seems to exhibit linearity until compliance is hit. Additionally, each test, from multiple chips on multiple wafers, has the same strange behavior, confirming the results. The high voltage tests shown in Figure 2.9 exhibit the same high current behavior. While both tests for W11S03 seem to have a quasi-linear relationship between voltage and current, the curves for all tests of W10S09 and W10S10 chips look more exponential. There is no sharp transition to exponential growth. Considering that there are multiple tests for each sensor and that all six high voltage tests
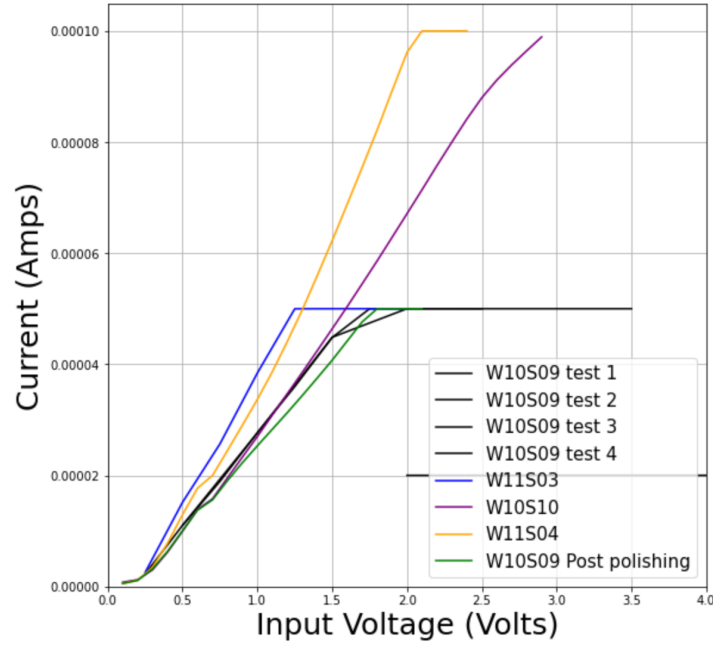
Figure 2.8: Various low voltage IVs for W10, W11.

have similarly strange results, the cause of these oddities is likely a high resistivity sensor characteristic rather than a random error.

The abnormalities of W10 and W11 plots prevent breakdown voltage estimations from the method used in Table 2.2.

To determine the voltage at full depletion, the CV relationships are helpful. Considering the relationship between capacitance and voltage given by Equation 1.3, capacitance has an inversely proportional relationship to depletion depth and $\frac{1}{C^2}$ has a directly proportional relationship to voltage. Once the sensor is fully depleted, the capacitance will remain constant. The plots for $\frac{1}{C^2}$ vs V should therefore be initially linear and eventually plateau and remain at a constant capacitance value. At the intersection of these two sections is the depletion voltage.

The reason we do not see the plateau in any of the additional function lines for
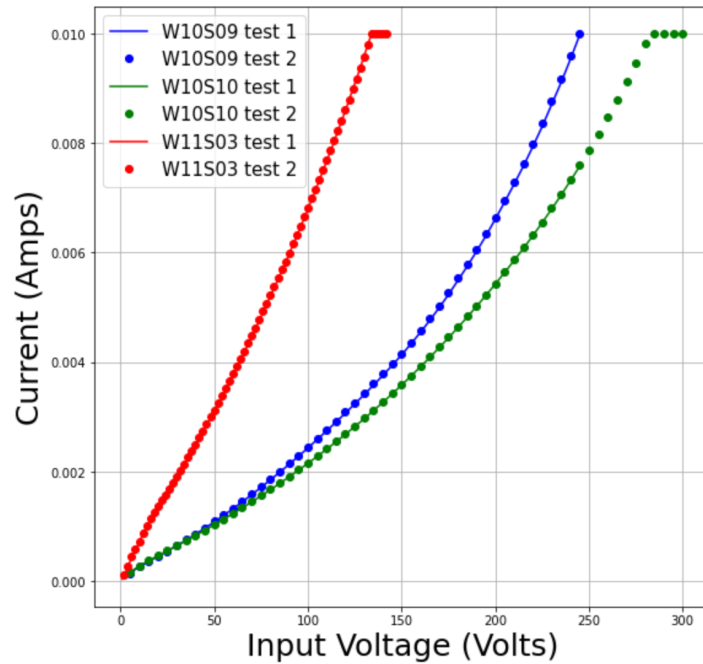
Figure 2.9: High voltage IVs on W10 and W11 sensors.

Figures 2.10, 2.11, and 2.12 is that the chips are not yet fully depleted; to reach full depletion, higher voltages than the applied range would be required. Equation 1.1 is used to calculate these values, and they are listed in Table 2.3.

Figures 2.10, 2.11, and 2.12 do not have experimental data in concordance with theory. In Figure 2.10, the linear trending data on the left side of the plot is actually just 2-3 data points. If more data points were taken, that section would likely look more like exponential growth. Though the data seems to be leveling off, the expected plateau would occur at a much higher voltage, where full depletion happens. Therefore, this non-linear and increasing curve is unexpected. Figure 2.11 has odd behavior around 150V; up to this voltage, the data trends positively and looks almost linear, similar to that of the additional function. After the peak around 150 volts, the slope abruptly increases and no longer resembles the theoretical data. The reason for the low slope trend sharply becoming
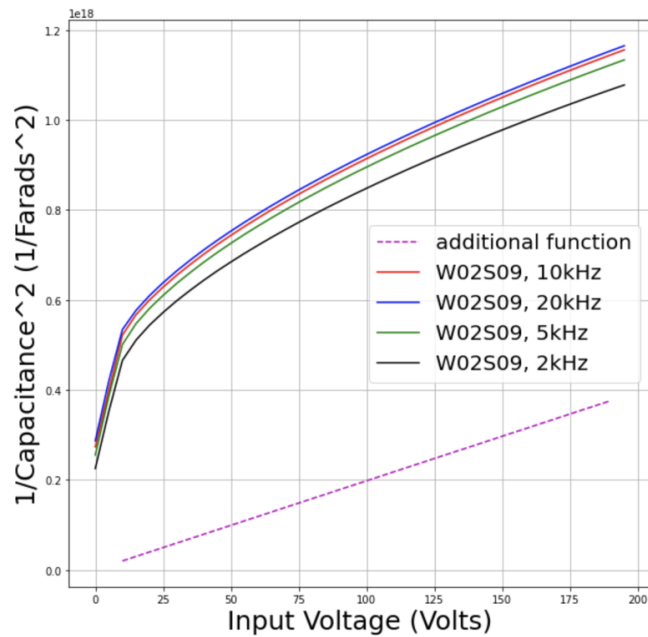
Figure 2.10: W02S09 CV at 2-20kHz with additional function.

a high slope curve is unknown. In Figure 2.12, several of the W11 lines show possible linearity, but the slope of these lines is almost zero. The high frequency data for W10S09 is similar to the black theoretical function, except that it is quasi-exponential instead of starkly linear.

When considering the curves of each 'additional function' shown, one must understand that they assume full pitch depletion. The chips tested experimentally are unable to have full pitch depletion in the applied voltage range. When a low voltage is applied, only the implant (where charges are collected) initially depletes; with a higher bias voltage, the depletion depth expands past the implant in width and depth of the sensor, allowing for full area depletion. Due to this geometrical limitation in the low voltage, the additional functions do not perfectly represent the intended behavior, but still serve as usable comparisons.
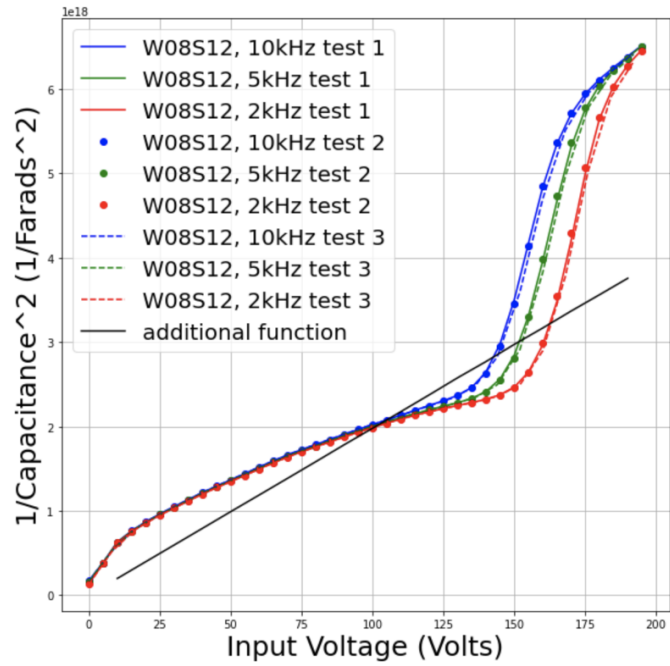
Figure 2.11: W08S12 CV at 2-10kHz with additional function.

Of the three CV Figures in this section, Figure 2.11 is most comparable to what is expected. Considering that each of the sensors should have the same geometry, the higher resistivity of the chip has a direct correlation to the depletion depth. Increasing the depletion depth would help make the additional function a more accurate estimation as depletion gets closer to encompassing the full pitch.
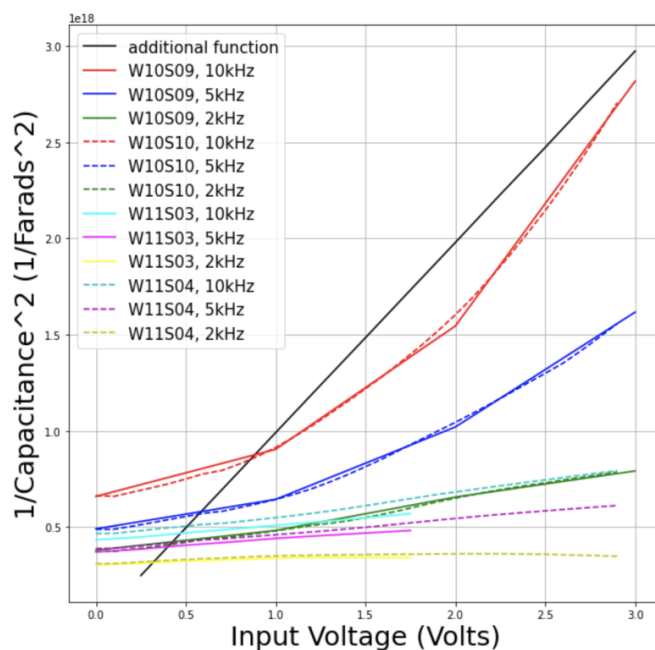
Figure 2.12: W10 and W11 CV at 2-10kHz with theoretical function.

Wafer	2	6&8	10&11
Voltage required for full depletion	134.4kV	13.4kV-6.7kV	268V

Table 2.3: Full depletion voltages per wafer. The mobility, σ, changes with temperature and is different for electrons versus holes. The mobility used to determine the breakdown values is that of a p-type bulk: $450\frac{cm^2}{Vs}$ [7]. The range of voltage in the 3rd column corresponds to the range of resistances for wafers 6 and 8.

3

Laser e-TCT Scan

3.1 Procedure

Chip Name	Test	Resistivity
W02S09	laser edge-TCT scan	20 Ohm-cm
W06S04	laser edge-TCT scan	200-400 Ohm-cm
W10S09	laser edge-TCT scan	10000 Ohm-cm

Table 3.1: Chips used in TCT scan.

Laser edge-TCT scanning is an efficient way to estimate depletion depth in a different way. In the same electronics room as the probe station at SCIPP, an aluminum box encapsulates a THORLABS BE15M-B laser and associated machinery.

The sensor was placed purposefully to ensure that the laser would be able to hit along the analog pixel row (the bottom row of pixels in each V3 chip). A pink wavelength was initially used to focus the beam appropriately on the chip in all 3 dimensions. During
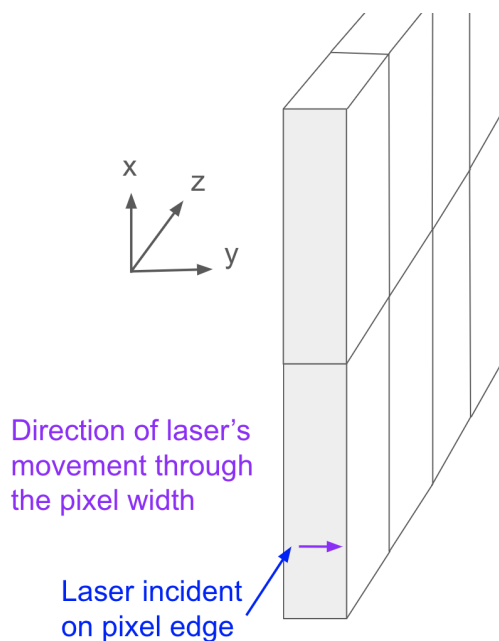
Figure 3.1: Sensor setup and coordinate axes mentioned.

the actual test, a metal lid is placed on top of the box to seal it and prevent the laser from reaching one's line of sight. The pink wavelength beam is turned off and an infrared laser is switched on. The beam no longer moves, and there is no further motion of the chip in the $\hat{z}$ direction. An infrared laser is used because above around 800nm, the absorption coefficient of silicon begins to decrease and therefore greater wavelengths of light are able to traverse the depth of the sensor more efficiently.

A complication with the connector location prompted the creation of a custom cable connection for an obstacle free path for the laser. Though it would be ideal for the edges of the chips undergoing laser e-TCT testing to be polished in order to prevent refraction from jagged edges and inconsistencies in the movement of the laser, the custom setup changes interfered with the placement of the chip and forced the laser beam to be incident on each chip's unpolished edge.

After biasing the sensor using a CAEN HV power supply, a motion stage is set with an intended value of micrometers to move in $\hat{y}$ so that the entire depth of one pixel moves through the beam line. Once this scan through the chip's depth is done, the stage then moves in the $\hat{x}$ direction, up to the next row of pixels, and the process repeats. Only the bottom analog row of pixels in each V3 sensor are scanned.
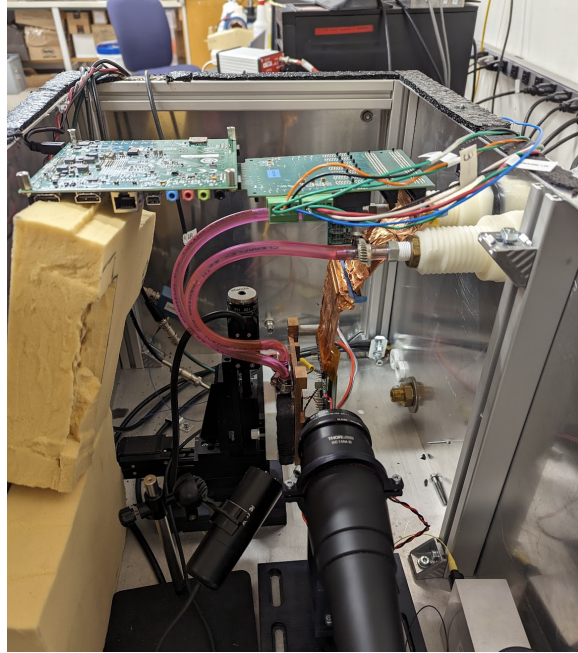
Figure 3.2: Laser setup. The sensor is underneath the gold tape, sitting in front of the laser. Photo courtesy of Amanda Steinhebel.

The tests were taken by biasing a specific voltage on one chip and taking a scan through the depth of a row of pixels as an oscilloscope connected to a custom made FPGA board reads the analog data to determine the various wave forms. More precisely, the motion stage moves the sensor by a number of microns and stops, waiting for a threshold of triggers to be surpassed. During this waiting time, 100 wave forms are created by the oscilloscope and averaged to one wave form. This process is repeated until the whole width

of the sensor has been covered. This completes one scan. Each 'bin' in the 2D histograms, shown in the next section, represents one average wave form's maximum amplitude.

Once one scan is done, the bias voltage is changed and the test is repeated, yielding different data for each bias voltage for each chip. Only the analog data is recorded because the wave forms provide important information in the context of this experiment. Considering the strange behavior of wafer 10 and wafer 11 sensors from the previous experiment, insight into the relationship between bias voltage and amplitude can help pinpoint the issue.

A second test was performed on W06S04 and W10S09 to include a more comprehensive voltage range. For each sensor, a bias voltage was applied and the pink wavelength was used to determine a location in the bottom corner pixel's width where the pulse amplitude was strong. Once this location was determined, the bias voltage was turned off and then manually increased, in 10V steps up to 400V for W06S04 and in 1V steps up to 10V for W10S09. At each voltage step, the wave form produced by the oscilloscope was saved and translated into csv files. This test provides insight about the changes in pulse shape and amplitude over a range a bias voltage, with the position of the laser beam not changing. We can determine depletion thresholds as well as denote pulse shape inconsistencies from this data.

3.2   Results

Figures 3.3, 3.9, 3.17 exhibit how the amplitude of current is measured. 2D histograms–where the x and y axes are both position in μm–with adjusting scales are shown for each bias voltage.

Figures 3.6 through 3.8, 3.12 through 3.14, and 3.20 through 3.22 are pulse

max (pmax) profiles. These plots utilize pulse data and amplitudes from a defined range of position values in the 2D histograms. The data ranges are noted by the yellow, red, and white rectangles highlighted in 3.3, 3.9, and 3.17. The yellow rectangles denote the x-projections where a range of y-values is selected for each bias voltage histogram. For each vertical band of bins within the yellow rectangle, the max voltage amplitudes are summed. Each subsequent sum corresponds to one x position and the amplitude sums versus position are plotted. Therefore, the x-projection pmax plots have dimensions of position ($\hat{x}$) by voltage amplitude while the y-projection pmax plots follow the same steps but with a selected range of values in x. The resulting dimensions of y-projection pmax plots are position ($\hat{y}$) by voltage amplitude; there are two y-projection plots, one spanning a weak amplitude x range and one spanning a strong amplitude x range.

Figures 3.4 and 3.5 are pulse scans. These plots show the average wave form created by the oscilloscope for a specific position along the sensor's width, as noted by the 2D histograms shown above with either a blue or a black dot at the intended location. The blue dot denotes the location of a strong amplitude region from which the pulse was taken. The black dot denotes the location of a weaker amplitude region from which the pulse was taken.

Regarding 3.6 and 3.7, it is important to note that the amplitudes for each voltage are slightly greater for the weak amplitude region than the strong amplitude region. This is solely due to the weak amplitude region highlighted by the red band in the W2 2D histograms having a larger volume than the strong amplitude region highlighted by the white band in the W2 2D histograms.

Figures 3.10 and 3.11 are also pulse scans. Here, the weak amplitude pulse data
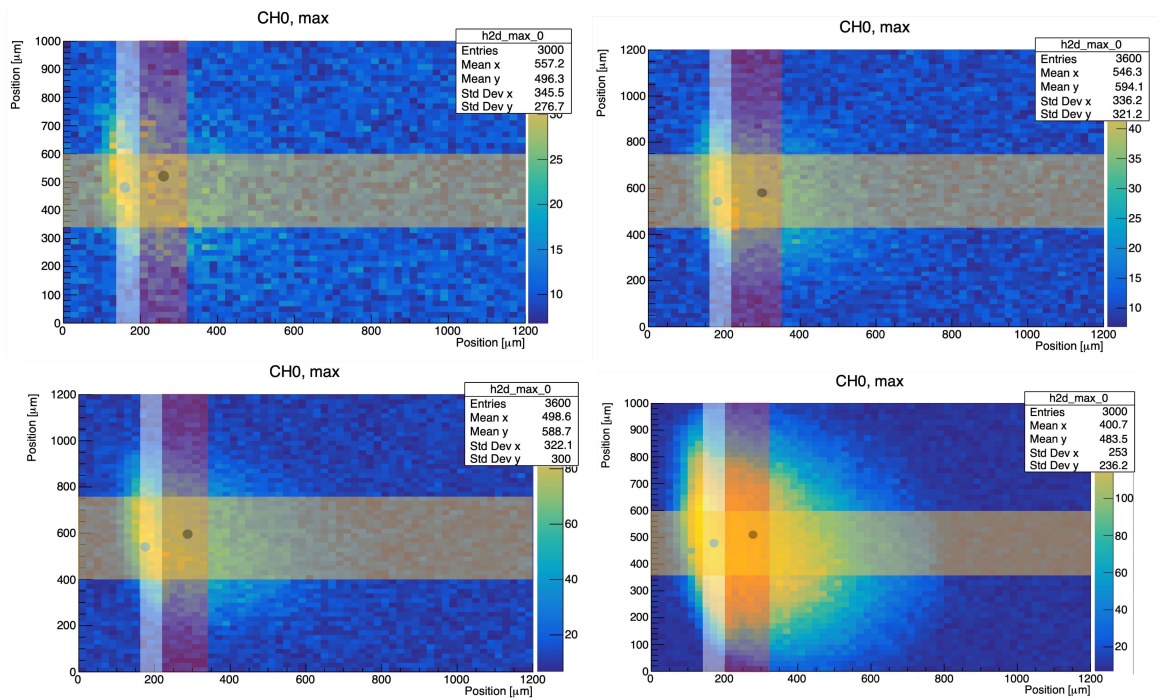
Figure 3.3: W2: Voltage amplitude 2D histograms; the top left is 40V, the top right is 100V, the bottom left is 180V, and the bottom right is 230V.

is taken from the black dot and the strong amplitude pulse data is taken from the blue dot in Figure 3.9.

Figures 3.15 and 3.16 show the results of the second test described in the procedure section. The wave forms over a range of voltages are shown, followed by an analysis of the maximum amplitude values as a function of bias voltage.

Figures 3.18 3.19 are pulse scans. Once again, the weak amplitude pulse data is taken from the black dot and the strong amplitude pulse data is taken from the blue dot in Figure 3.17.

Figures 3.23 and 3.24 display the results of the second test described in the procedure section. The wave forms over a range of voltages are shown, followed by an

Figure 3.4: Wafer 2 weak amplitude pulse scan.

Figure 3.5: Wafer 2 strong amplitude pulse scan.

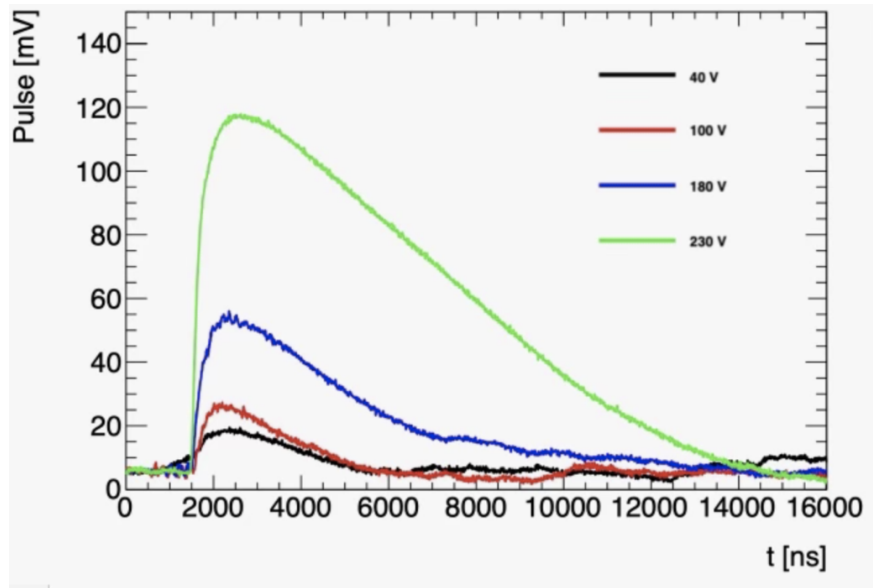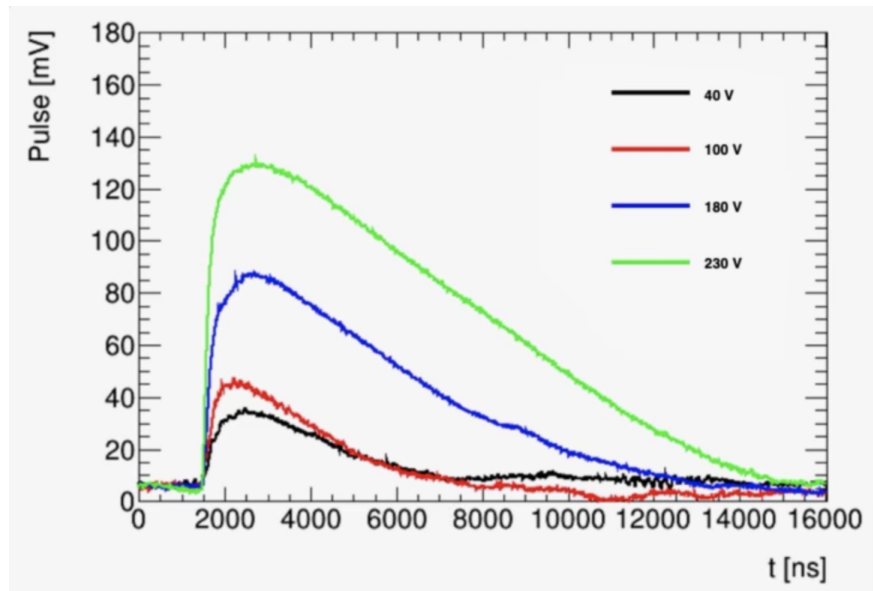Figure 3.6: Wafer 2 weak amplitude y-projection pmax (red band).

Figure 3.7: Wafer 2 strong amplitude y-projection pmax (white band).

Figure 3.8: Wafer 2 strong amplitude x-projection pmax (yellow band).

analysis of the maximum amplitude values as a function of bias voltage.

3.3 Analysis

The signal amplitude depicted by each of the 2D histograms (from Figures 3.3, 3.9, and 3.17) is an important aspect in understanding the depletion depth. Specifically, the laser simulates a continuous flow of charged particles passing through the depletion depth. This continuous stream of photons causes charge carriers in the depletion depth to move to the collection electrodes on each pixel. This movement of charged particles creates a current which is converted to a voltage value by an amplifier. The amplitude of the resulting voltage reflects the strength/quantity of current produced. In this way, the depletion depth can be estimated by each wafer's 2D histograms; where the region is not depleted, the charge carriers will simply recombine with each other and no current will be produced, so no signal
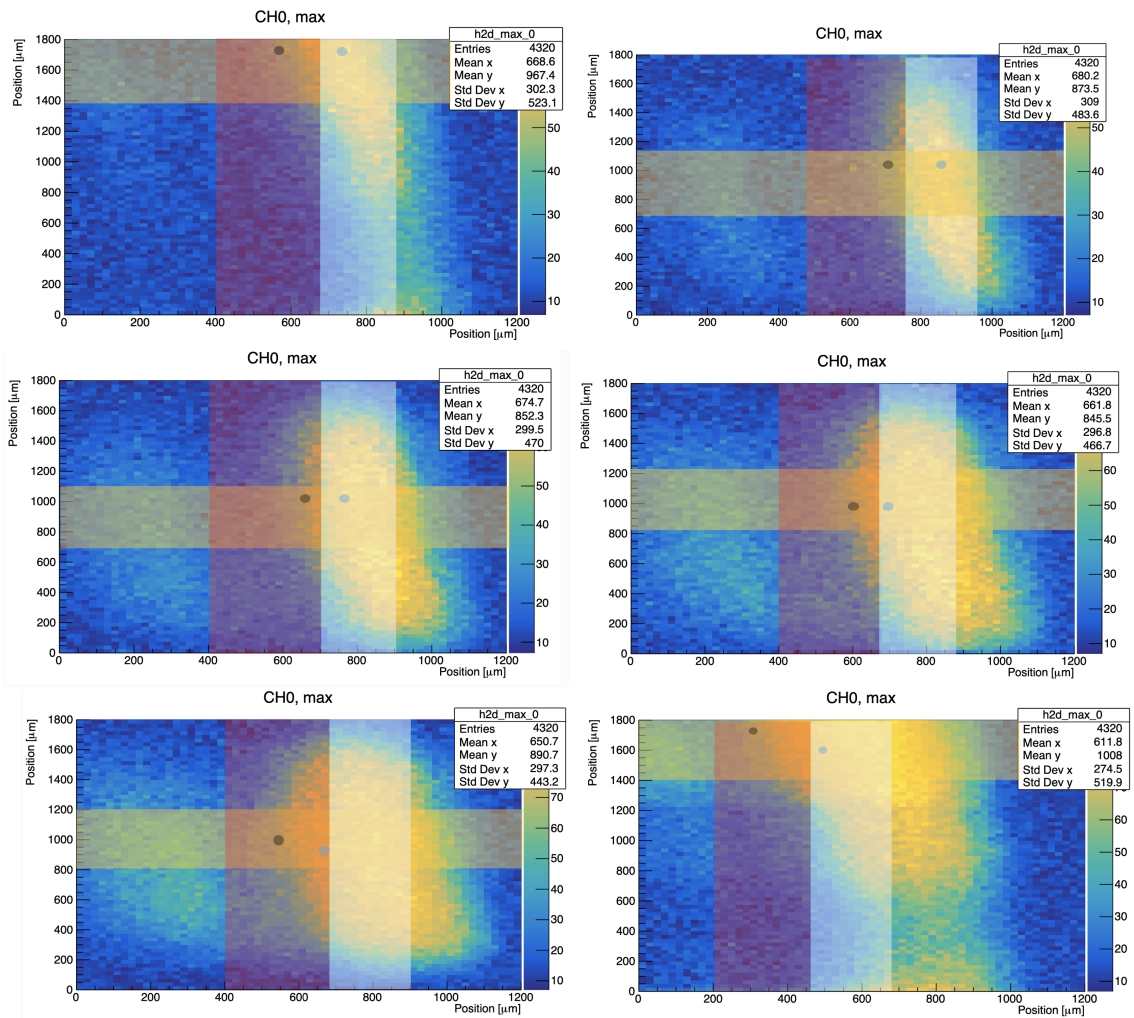
Figure 3.9: W6: Voltage amplitude 2D histograms. The top left is 50V, the top right is 100V, the middle left is 200V, the middle right is 300V, the bottom left is 380V, and the bottom right is 400V.
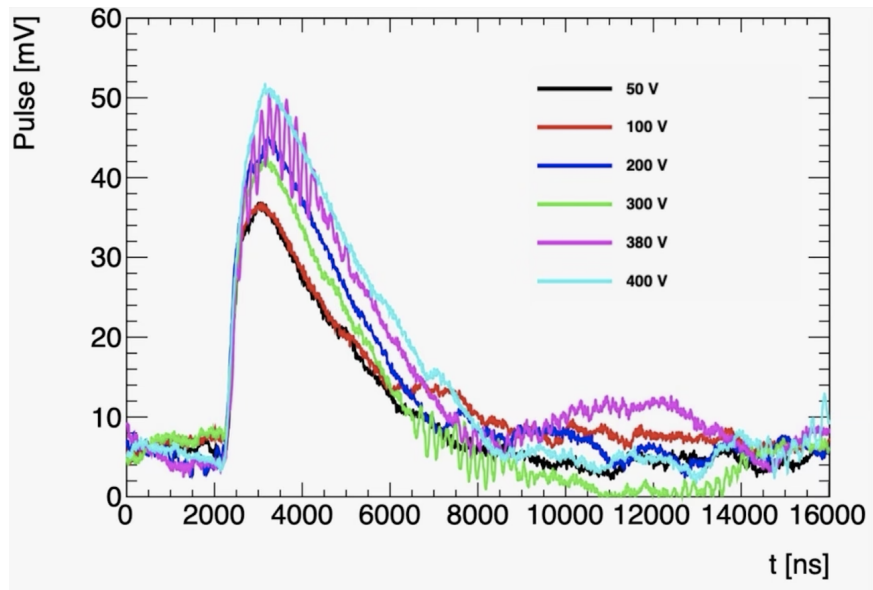
Figure 3.10: Wafer 6 weak amplitude pulse scan.
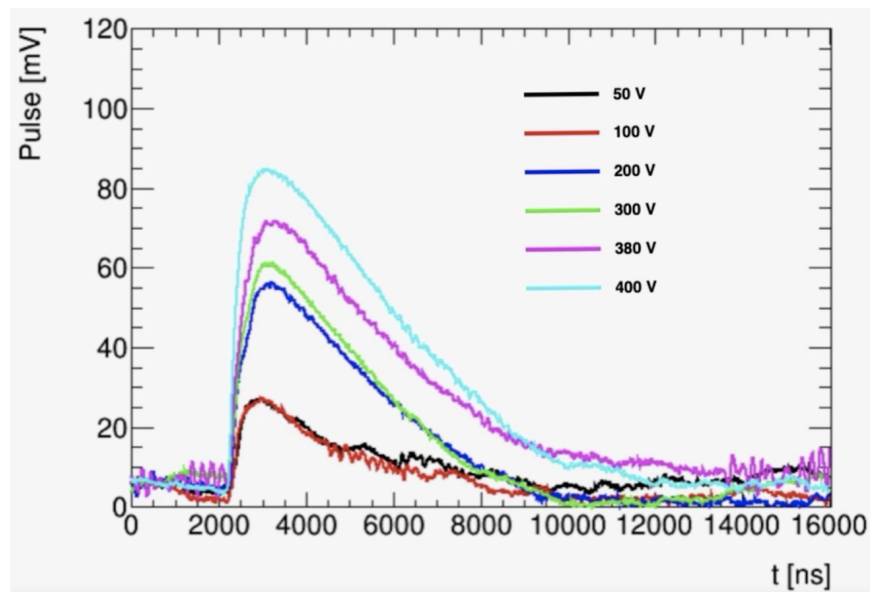
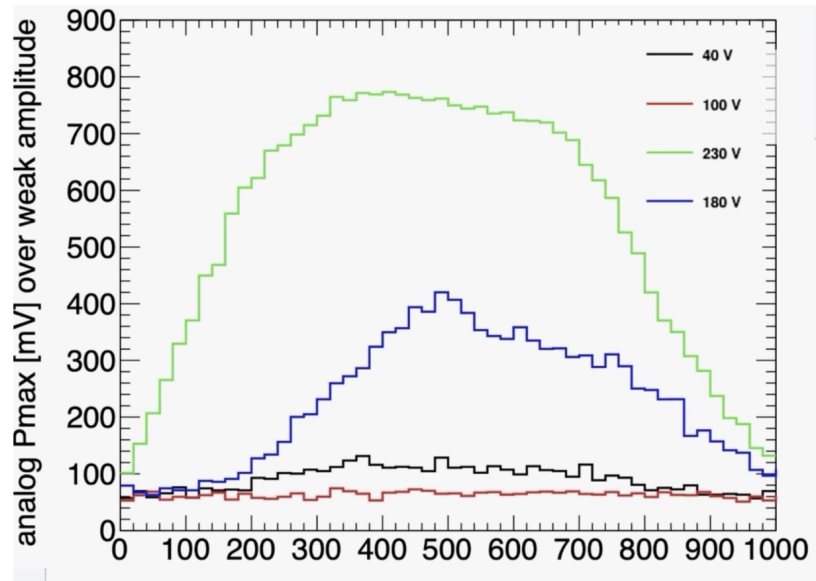Figure 3.11: Wafer 6 strong amplitude pulse scan.

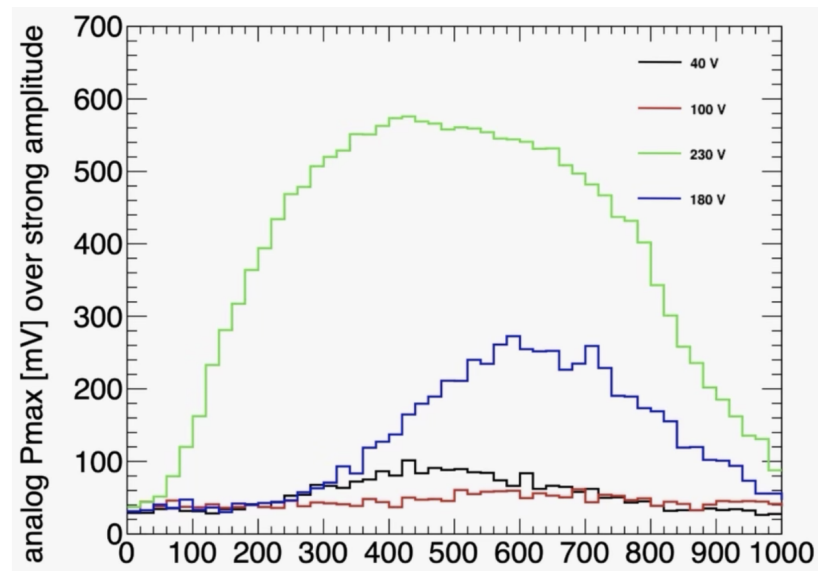Figure 3.12: Wafer 6 weak amplitude y-projection pmax (red band).

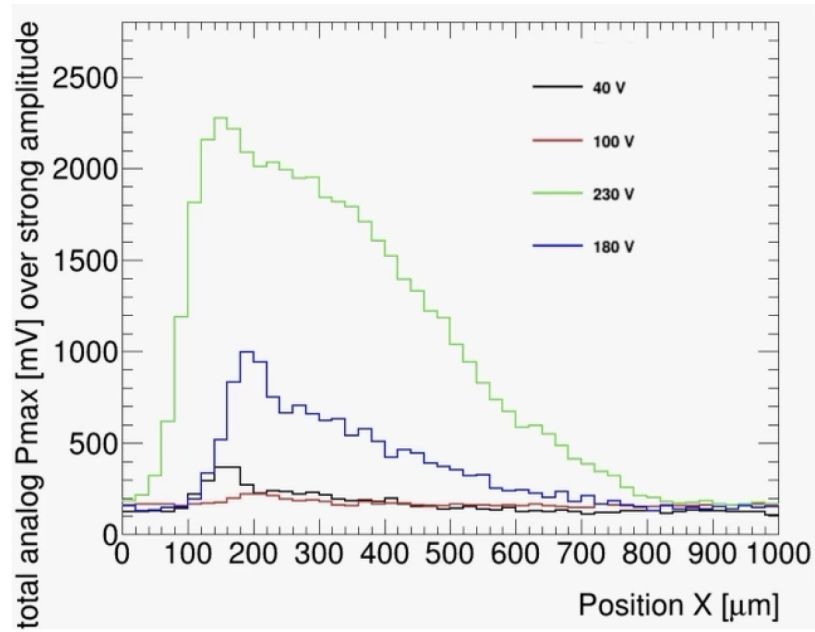Figure 3.13: Wafer 6 strong amplitude y-projection pmax (yellow band).

Figure 3.14: Wafer 6 strong amplitude x-projection pmax (white band).
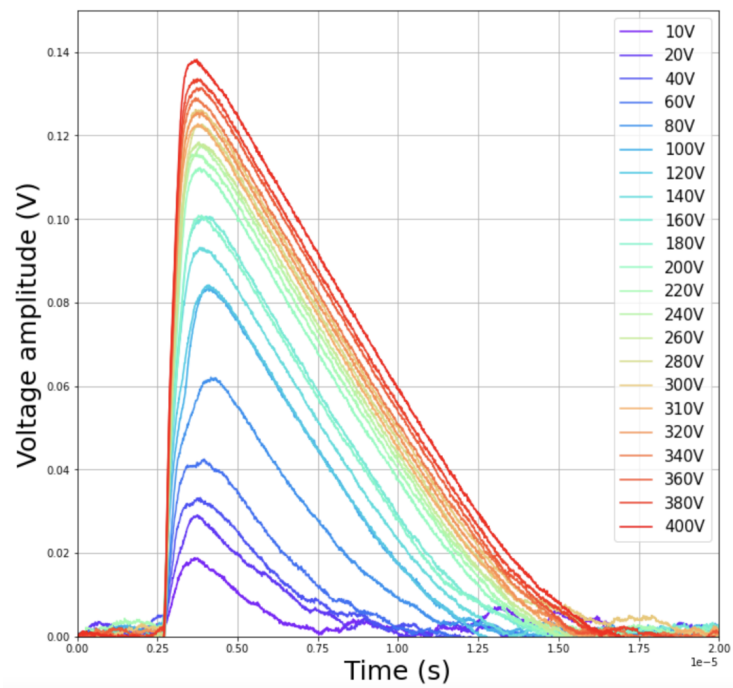
Figure 3.15: W6 voltage wave forms.
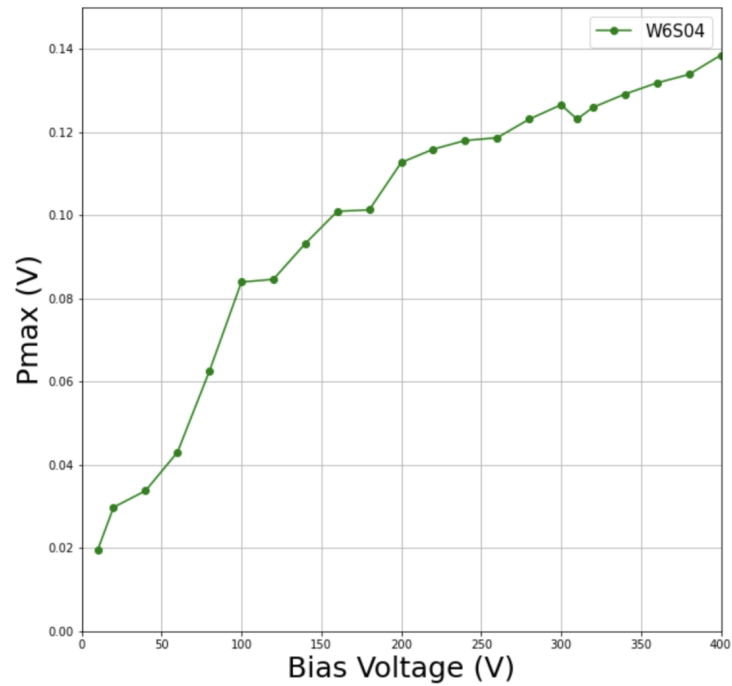
Figure 3.16: W06S04 pmax per applied voltage.

will be read out. Therefore, with a higher bias voltage, the depletion region will increase and more current will be produced, creating a greater amplitude of voltage.

Figure 3.3 shows that as the bias voltage increases, the area of voltage amplitude and the amplitude itself increases. This relationship is supported by the associated pulse and pmax plots in Figures 3.4 through 3.8, where the pulse scans show that voltage amplitude is higher for each bias voltage in the strong amplitude area than in the weak amplitude area. The pmax plots do not show this relationship–however, this is likely due to the fact that the vertical width of the red and white (strong and weak) y-projection bands are not equal; the weak band is wider and therefore allows more values to be projected. Regardless of this, it is clear that the W2 data shows the expected relationship between bias voltage and resulting voltage amplitude.
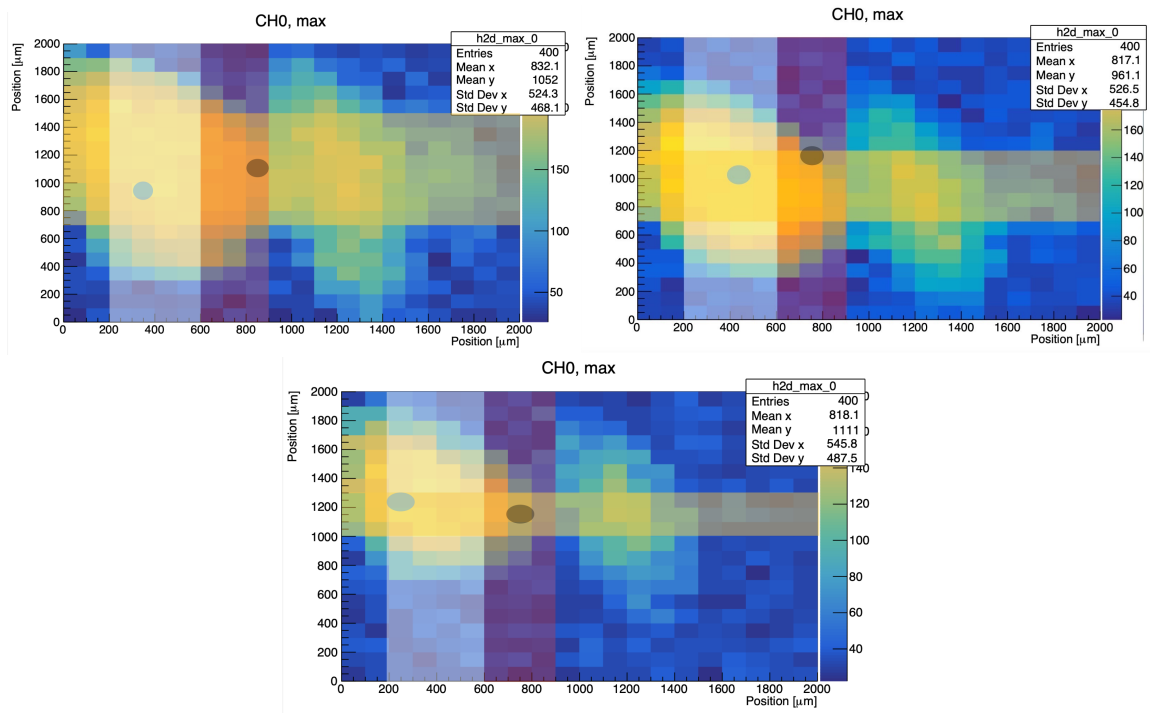
Figure 3.17: W10: Voltage amplitude 2D histograms. The top left is 2V, the top right is 4V, and the bottom left is 8V.
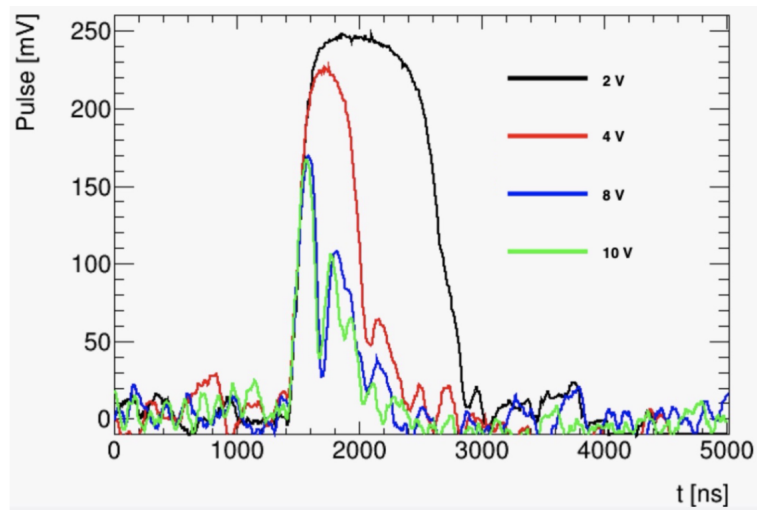

Figure 3.18: Wafer 10 strong pulse scan.
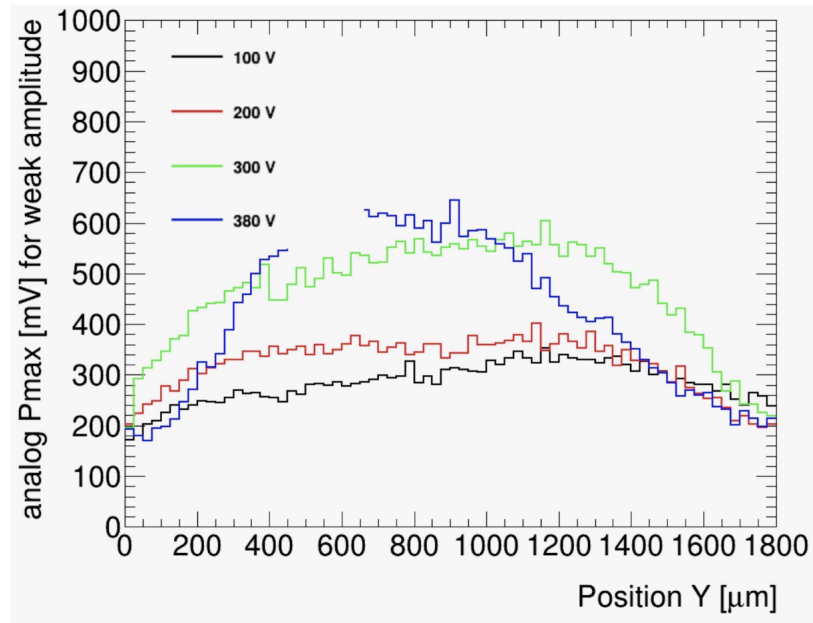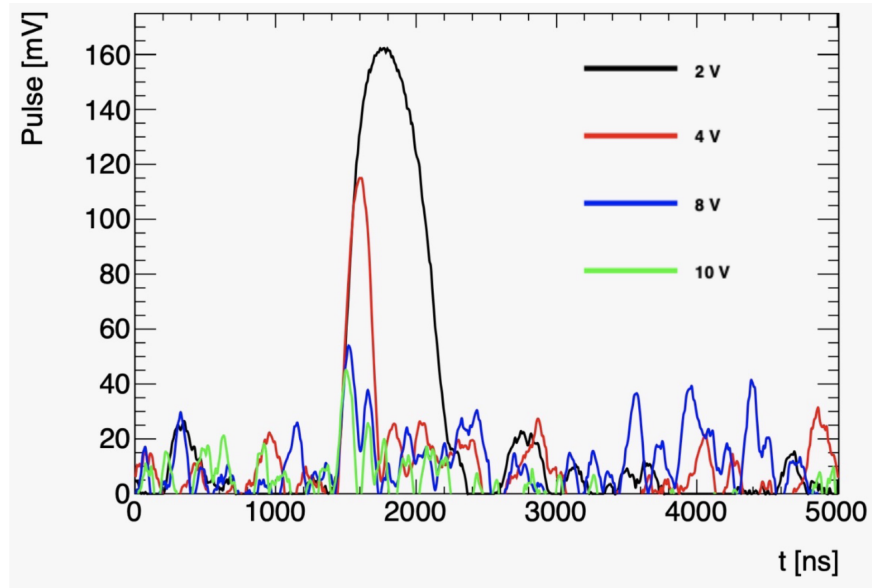
Figure 3.19: Wafer 10 weak pulse scan.
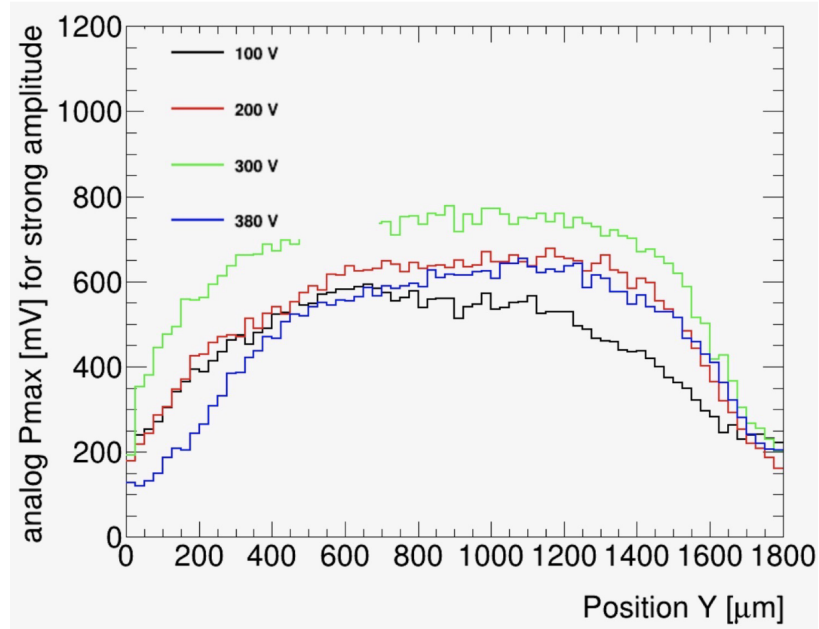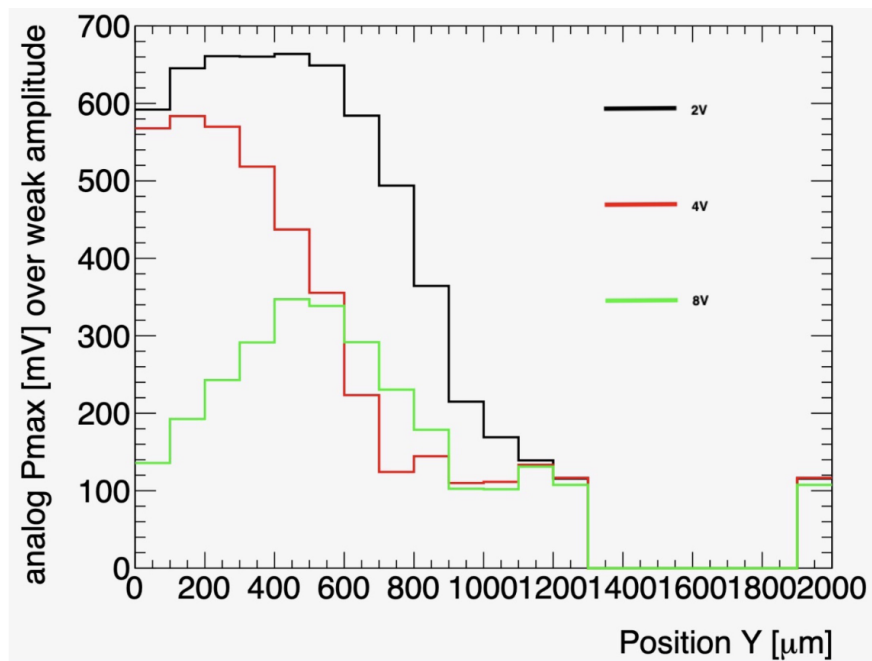

Figure 3.20: Wafer 10 weak amplitude y-projection pmax (red band).
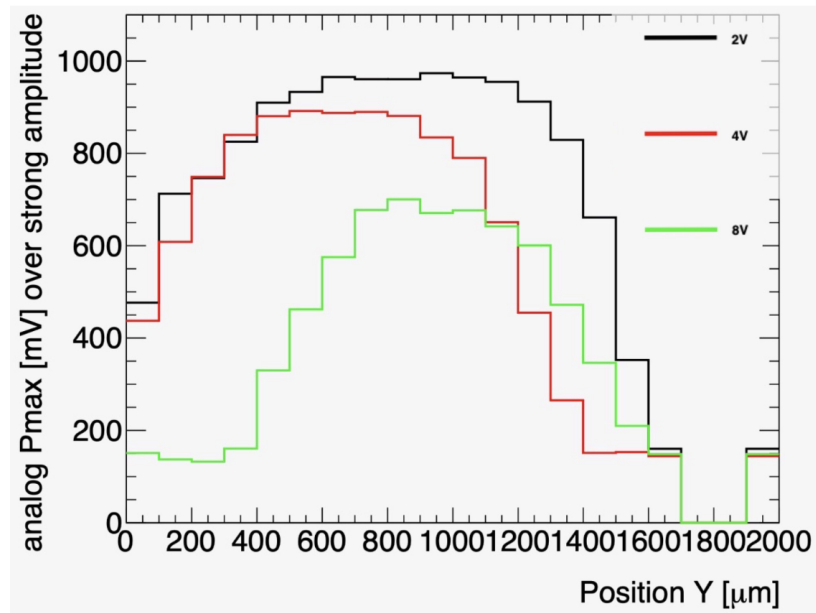
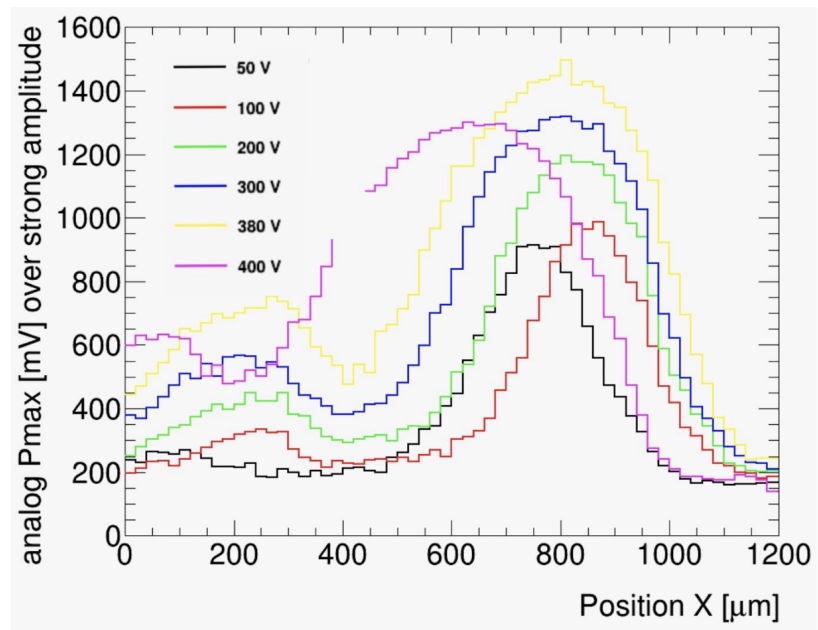Figure 3.21: Wafer 10 strong amplitude y-projection pmax (white band).
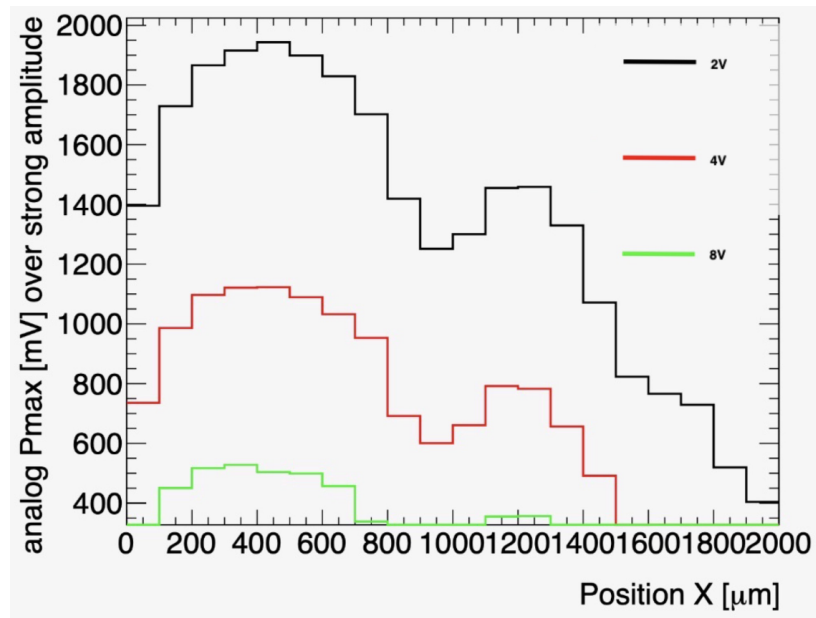
Figure 3.22: Wafer 10 strong amplitude x-projection pmax (yellow band).
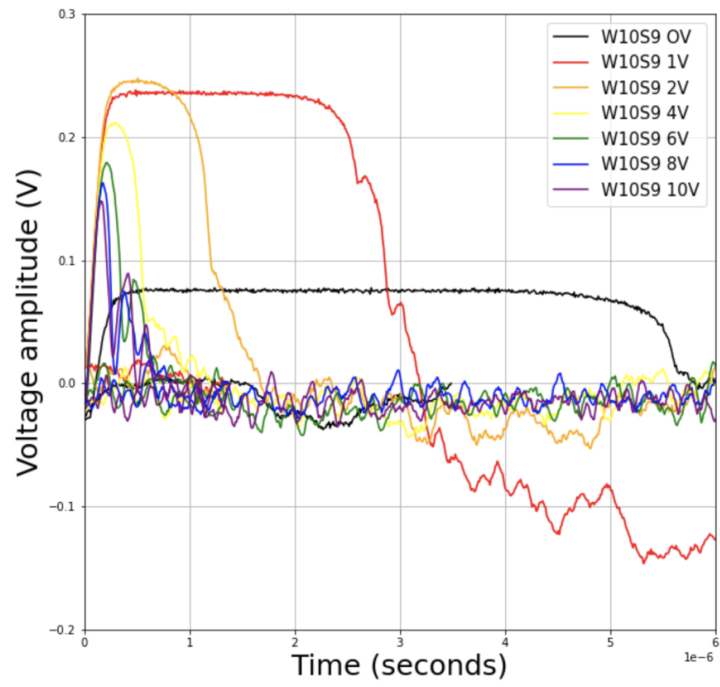
Figure 3.23: W10 voltage wave forms.
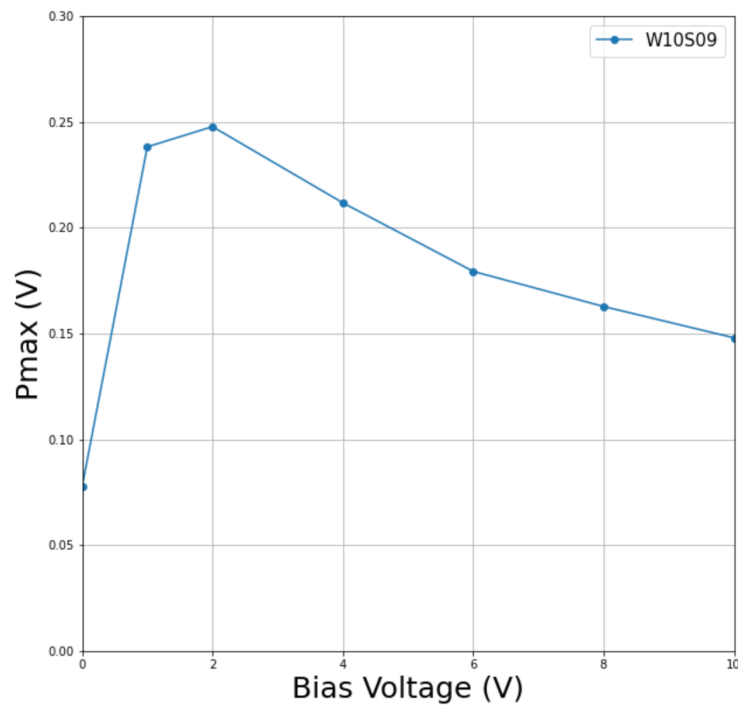
Figure 3.24: W10S09 pmax per applied voltage.

One oddity that will recur in this section is that the range of where there seems to be high voltage amplitude is greater than $500\mu m$. The full depletion depth should not exceed the depth of the sensor itself, and even the slowly dissipating amplitude of Figure 3.3 shows that there is some signal past $500\mu m$ for high bias voltage.

The wafer 6 histograms depicted by Figure 3.9 show a halo effect that extends beyond $500\mu m$ pixel pitch. This affect is also strongly present in the wafer 10 histograms from Figure 3.17. Looking at the position axis of these histograms, there is signal from about 0-1000μm and 0-1500μm for wafer 6 and wafer 10 respectively. These halos are also evident in many of the varying pmax plots. Signal amplitude continues consistently past the $500\mu m$ mark, regardless of the bias voltage (similar to wafer 2, except that wafer 2 did not include a second strong patch of amplitude in the 2D histograms). The exact reason for this halo effect is unknown, but it is believed to be related to neighboring pixels. The beam line should only hit on a single pixel at a time, but there is a possibility of signal diffusion through subsequent pixels. However, this would be abnormal; signal injection should only return amplitude where a region is depleted. With low bias voltage, the whole $500\mu m$ should not return amplitude. If signal amplitude occurs across 2-3 pixels, then diffusion/reflection is widespread.

One theory about this halo affect is that it occurred from not polishing the sensor's correct edge. Considering that there is no data for an e-TCT scan of these sensors with a polished edge, it becomes difficult to pinpoint how the plots and histograms might look different in the case that the correct edges were polished. We know however that sharp edges definitely cause scattering of light, but it is difficult to say how correlated this scattering would be with the halo effect.

Looking closely at the W10 histograms of Figure 3.17, the signal amplitude is higher for lower bias voltage, and vice versa. A normal wafer should have the opposite relationship–voltage and depletion depth are proportional so signal amplitude should increase with voltage. The pulse plots of Figures 3.19 and 3.18 also show this inverted behavior. Not only does the current amplitude decrease when the bias voltage is increased, but the pulses lose their shape. This suggests that when bias voltage gets 'too high' for high resistivity wafers, it is possible that some of the chip's transistors become incapacitated. The pmax plots also validate this, with the highest voltage amplitude in both the strong and weak y-projections occurring at 2V, and the lowest voltage amplitude occurring at 8V. Looking at Figure 3.22, the halo is clearly visible as another patch of higher amplitude to the right of the main pixel's x position range.

Figure 3.15 clearly shows that pulse shape is consistent in a wide range of bias voltages. The voltage amplitude and time scales decrease as voltage decreases, as expected. To clarify this plot, Figure 3.16 shows how the maximum amplitude value trends positively with increasing bias voltage.

The same two plots but for wafer 10, Figures 3.23 and 3.24 do not exhibit the same behavior. The wave forms do not have the same shape and, similar to the pulse and pmax plots for W10, the voltage amplitudes and pulse widths decrease with an increase in bias voltage. For all bias voltages, the pulse shapes do not fall off slowly after their peaks; instead, the plateaus leading to the peaks have almost the same time scale as the fall off from the peaks. Figure 3.24 shows a downward trend in maximum amplitude as bias voltage increases, contrary to how W2 and W6 behaved.

The depletion depths for each sensor according to bias voltage, are estimated in

Tables 3.2, 3.3, and 3.4. These values are determined by taking the full width half max of the strong amplitude x-projections, present in Figures 3.8, 3.14, and 3.22.

These depletion depth estimates reinforce the halo effect visible in many of the above plots. Table 2.3 shows that the required bias voltages to reach full depletion are hundreds to thousands of volts higher than what was applied for the e-TCT tests. Therefore, none of the sensors should be reaching full depletion of $500\mu m$. Wafer 10 shows the highest values for depletion depth that greatly surpass the full depth of a single pixel. The reason for these large values is undetermined, but is likely related to electrical or optical diffusion resulting in signal reflection or smearing.

Bias Voltage	40V	100V	180V	230V
Depletion Depth	$80\mu m$	undetermined	$180\mu m$	$360\mu m$

Table 3.2: Wafer 2 depletion depth estimates.

Bias Voltage	50V	100V	200V	300V	380V	400V
Depletion Depth	$250\mu m$	$250\mu m$	$300\mu m$	$375\mu m$	$500\mu m$	$550\mu m$

Table 3.3: Wafer 6 depletion depth estimates.

Bias Voltage	2V	4V	8V
Depletion Depth	$900\mu m$	$800\mu m$	$450\mu m$

Table 3.4: Wafer 10 depletion depth estimates.

4

Infrared imaging

4.1 Procedure and Results

After confirming the abnormal results of wafer 10 and 11 in regards to voltage, current, and depletion depth relationships, infrared imaging studies were used to look for possible defect locations within certain circuitry. Specifically, the abnormally high current values suggest that more power is produced and dissipated. The IR imaging studies are an attempt to capture the specific locations of power dissipation in the form of thermal radiation. Considering that the peak wavelength emitted, λ_{max}, is inversely proportional to temperature, an infrared camera can calculate various temperature changes depending on measured energy which depends on emitted wavelength in the infrared. Forward looking infrared (FLIR) cameras detect long wave infrared radiation, in the range from $8\mu m$ to $14\mu m$ [15].

Sensor	Test
W02S09	Manual IV
W06S12	Probe station V_{bias} comparison
W10S09	Backside testing for hot spots
W10S10	Manual IV
W11S03	Front side imaging
W11S04	Front side imaging

Table 4.1: Sensors used in various IR tests.

4.1.1 Frontside imaging

A Flir A325sc thermal imaging camera is set in a black box with the lens facing downward toward the top surface of a sensor. Each sensor tested was individually wire bonded onto a PCB and a custom cable connection was made to connect a Keithley 2410 HV power supply to the PCB's HV ring. The PCB containing each sensor is connected with double sided tape to a metal box intended to provide the sensor with some height in the box as the Flir camera has limited range in $\hat{z}$. The camera is connected to an HP Envy dv6 and a Research IR program shows heat scans in real time and is able to plot various data. Two lenses were used, one of higher magnification and one of lower magnification. A large black piece of felt is lowered over the open side of the box so that the sensor is covered in darkness on all sides and any light reflections are limited. The voltage is manually altered, with ranges depending on the sensor and test intention. With each large change in voltage, a heat map is saved with the respective color-temperature scale. Aspects of Research IR allow for certain sections of the on-screen image to be highlighted and their temperature

ranges compared, which is useful in determining whether specific locations on the sensor have higher temperatures than others with the same bias voltage. In addition to front side imaging, the blank PCB board was tested with the same manual IV to ensure that it did not carry any excess current. The board reached up to 300V before hitting a very low current of 5nA and was determined to be unproblematic. The $1K\Omega$ resistor in the PCB was changed to a 5Ω resistor as well and the IVs before and after the change were compared.

Figure 4.1: Example of sensor placement and bonding for front side image testing.

Figure 4.2 depicts three different tests, two before the $1K\Omega$ resistor was replaced, and one test with the 5Ω resistor in the PCB. The voltages plotted were not the actual bias voltages, but instead taken into account the voltage being applied only to the sensor, after passing through the PCB resistor in series. The voltage drop over the 5Ω resistor

is negligible in comparison to the voltage drop over the $1K\Omega$ resistor. It is clear that the current still rises quicker with the $1K\Omega$ PCB resistor.
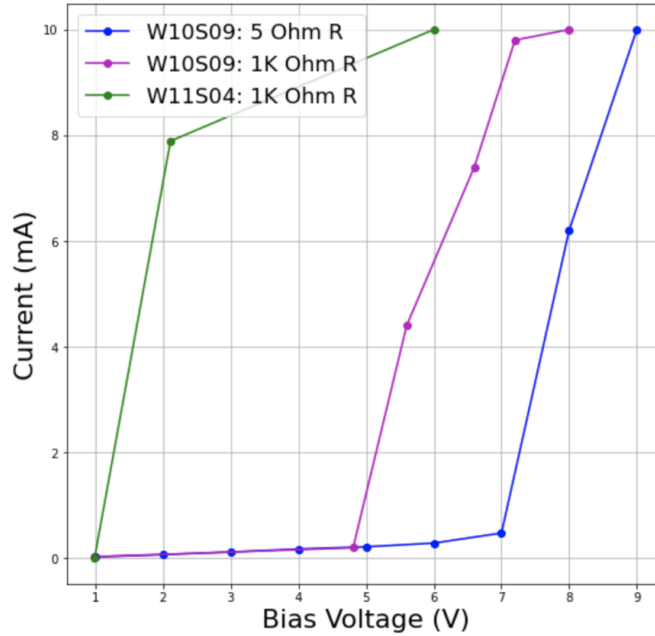
Figure 4.2: W10S10, W10S09, W11S03 IVs with different PCB resistances.

These IV curves can be compared to those of Figure 2.9 where each of the sensors hit the same compliance after hundreds of volts had been applied.

4.1.2 Backside imaging

After testing the blank board, questions about problems originating on the back of sensors arose. For effective backside imaging, the sensor is turned 180° around its depth so that the front is facing the plate it sits on and the camera faces the back of the sensor. Instead of wire bonding to a PCB, the sensor is taped down with electrical tape and wire bonds attach the sensor to metal pads that sit on an FR4 (fiberglass and epoxy) plate. The pads are soldered to the HV and grounding connections that feed back to the Keithley 2410

power supply. The lens was changed to a higher magnification and IVs were taken with imaging of W11S03, W10S10, and W02S09.

Figure 4.3: Backside imaging sensor setup before the felt is lowered down.

Figure 4.4 shows temperature color maps from different bias voltages applied to W10S10. The color scales are on the right of each photo; as the voltage increases, the maximum temperature on the scale for each photo does as well.

Figure 4.5 depicts an IV curve from back side mounting of W10S10; the data roughly matches that of the probe station from Chapter 2.

4.1.3 Manual IV at probe station

To continue the investigation of possible backside anomalies, another experiment was conducted to compare the bias voltage to the voltage moving through the back of the sensor. A sensor was set up in the probe station as if to take an IV curve using the metal probes, but a voltmeter was used to measure the potential difference between the cord connecting to the HV pad and the ground from the power supply. Afterwards, a
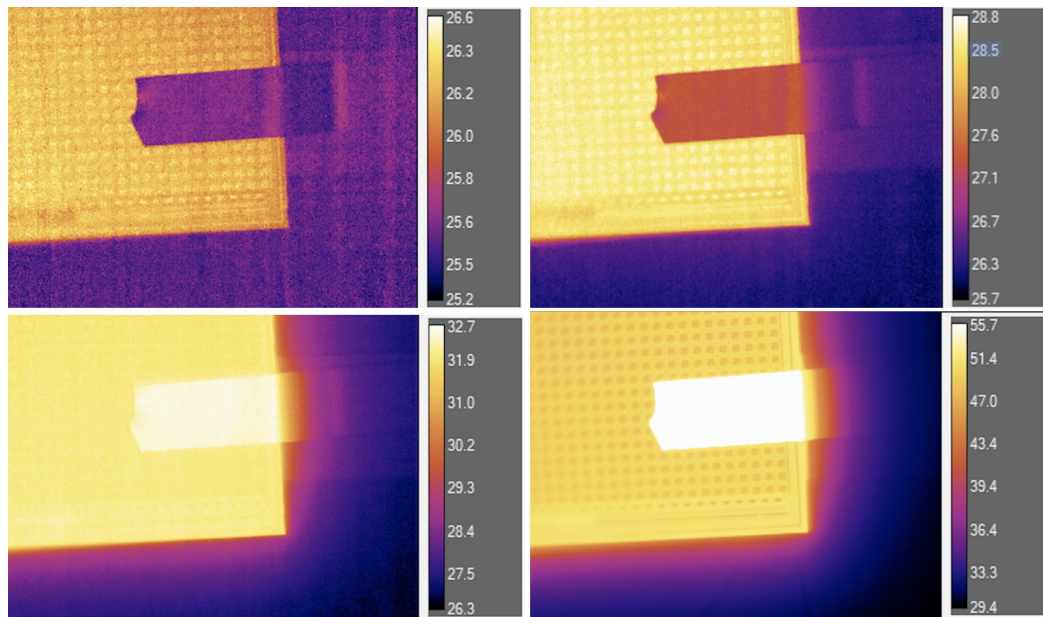
Figure 4.4: W10S10 backside heat maps. The top left is 0V, the top right is -50V, and the bottom left is -100V, and the bottom right is -200V.

voltmeter was also used to test the potential difference between the same grounding cord and the copper circular plate that the sensor sits on. The first voltmeter measurements represent the bias voltage being applied to the sensor through the conduction pads. The second voltmeter measurements represent the potential present in the back of the sensor, which should match the bias. W06S12 and W10S09 were tested in this experiment. Figure 4.6 depicts the differences between the bias voltage and the chuck voltage (measured from the copper plate) from the probe station setup. While the relationship between the two voltages looks linear for W06S12, the back side voltage of W10S09 seems to have a minimal response to the bias voltage.

Figure 4.7 shows the same test as the previous figure, but for W10S09. There is a slight difference in the two voltages when increasing the voltage versus decreasing the voltage.
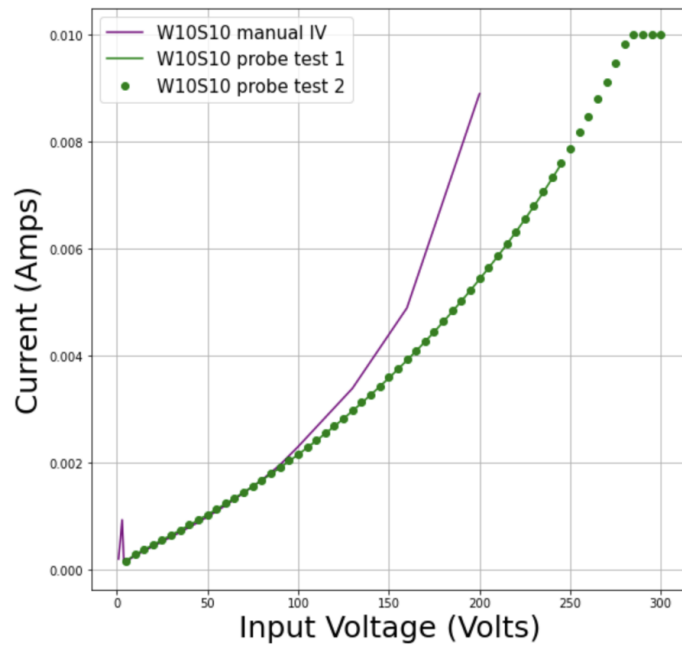
Figure 4.5: W10S10 HV IV on probe station and manual IV with backside up.

4.1.4 Insulating tape connection

To try and eliminate any shorting of the back of various chips, the conductive tape that connected the back of the sensor to the metal space in the PCB was replaced with insulating tape. This inhibits any transfer of charge from the bottom of the sensor to the surface of the PCB, except where the wire bonds connect to the high voltage. The same manual IVs are taken with front side imaging. W10S09 was tested in this regime. Figure 4.8 compares the probe station IV test from Chapter 2 with a front facing manual IV with insulating tape for W10S09.

4.1.5 Temperature mapping

Using various 'domain of interest' mapping settings from Research IR, several boxes were selected on the surface of W10S10. In a normal IV test with steps of 10V up to
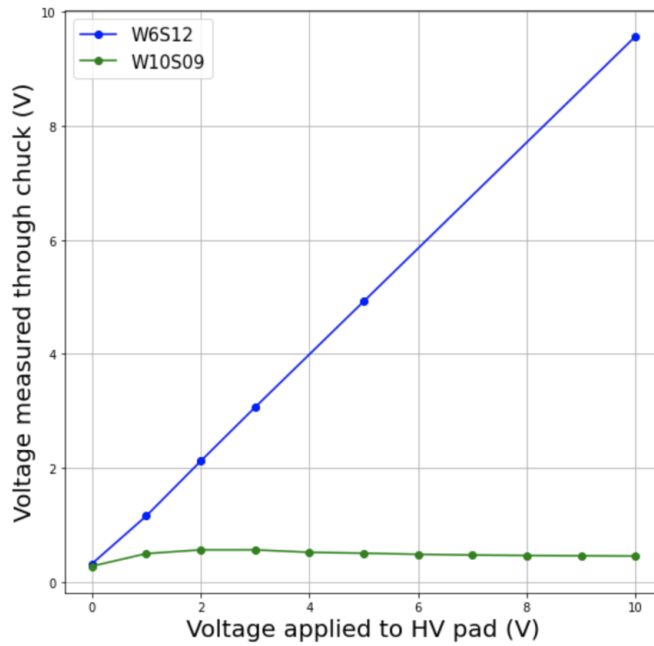
Figure 4.6: W6S12 and W10S09 bias vs measured voltage.

-180V, the temperature changes of 4 locations on the backside of the sensor are compared. In one test, the voltage is increased up to the maximum with a pause of 2-3 seconds before each ramp and a pause of about 2 minutes before decreasing the bias back down to zero. In the subsequent test, the voltage is increased to the maximum with a 10 second pause before each ramp, and decreased with relatively the same time scale. Figures 4.9, 4.10, and 4.11 correspond with Temperature vs Time plots for different locations on the W10S10; the 'boxes' are spaced out so that Box 1 covers the surface of a pixel, Box 2 covers the edges of adjacent pixels, Box 3 covers the bottom left of the sensor, and Box 4 covers the left edge of the sensor.
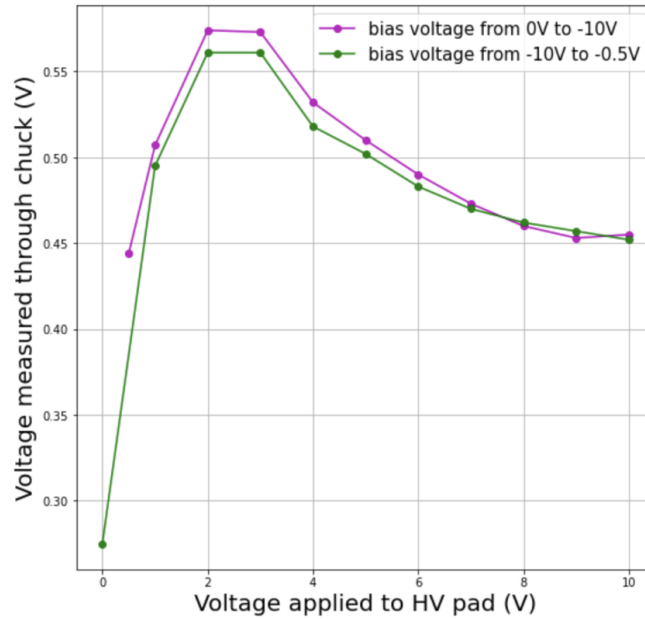
Figure 4.7: W10S09 bias vs measured voltage.

4.2   Discussion

The front side IV tests with either PCB resistor show a steeper curve that the tests conducted in Chapter 2, where the high resistivity sensors were able to reach 100-300V before hitting the 10mA compliance. Considering that the test results show consistently high current even after the PCB resistor was changed and the test was taken for 2 different sensors, this suggested a problem with the manual IV setup.

The later probe station manual IV tests (comparing the chuck to bias voltage with the voltmeter) were an attempt to determine whether the high current was stemming from the backside of the sensor. Considering Figures 4.6 and 4.7, there is a large difference between the bias and read out voltages for W06S12 and W10S09. While W06S12 behaves as expected, W10S09 seems to have no reaction to a changing bias voltage. The sensor is held down to the copper plate (chuck) by a vacuum hole which touches near the center of
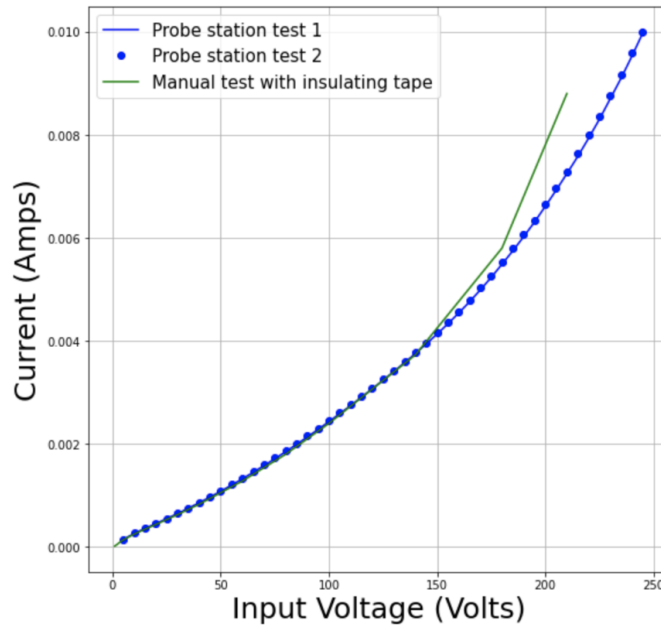
Figure 4.8: W10S09: Probe station IVs and manual IVs with insulating tape.

the sensor's backside surface area. This suggests a potential gradient through the backside surface of the sensor, where high voltage is present along the edges, and fixed low voltage is present near the center. Specifically, there could be complications in the p-type bulk brought about by the high resistivity substrate.

The insulating tape in a front-facing setup is used to troubleshoot any shorting of the backside potential by replacing the conductive connection to the PCB. Figure 4.8 depicts the similarities between Chapter 2's IV curve with W10S09 and the IV taken with the insulating tape. While there are slight deviations, possibly in the form of a lasting excess of current with the manual IV IR setup, the plot similarities support the idea that potential gradient on the sensor's backside can be minimized with an insulating back connection.

To continue with the original goal of the test, trying to understand where the power dissipation originates, W10S10 underwent more thermal imaging to check for hot
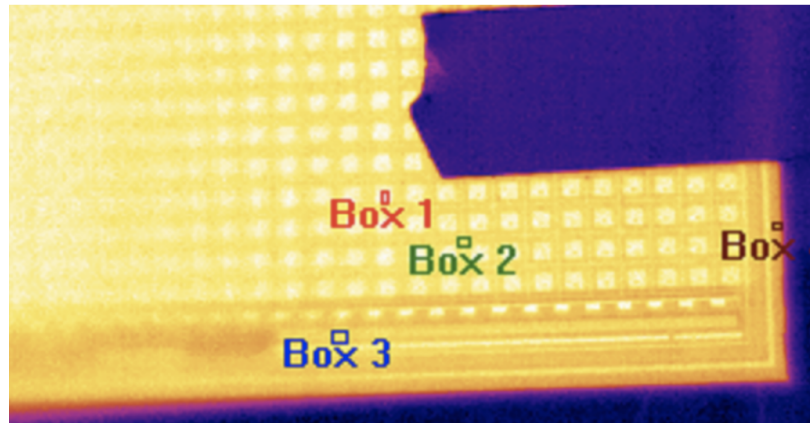
Figure 4.9: Boxes 1-4 locations.
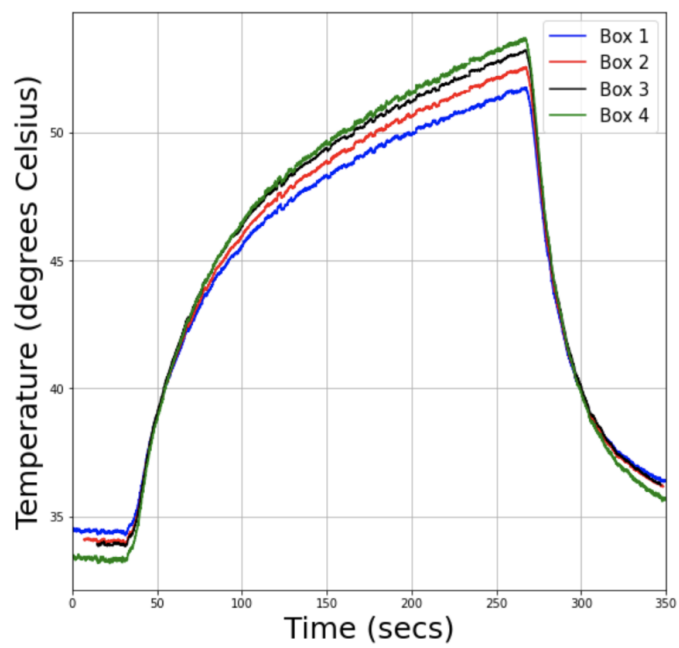
Figure 4.10: Voltage fast ramping with temperature vs time for different locations on W10S10.
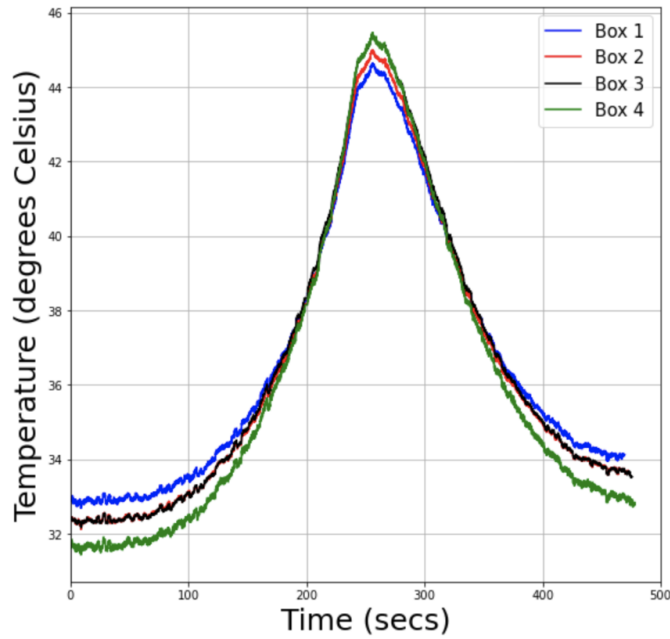
Figure 4.11: Temperature vs time for different locations on W10S10.

spots. This time, the sensor was imaged upside down after IV tests were taken in that orientation. Figure 4.4 shows the temperature increase throughout the sensor as the bias voltage increases. Figures 4.9, 4.10, and 4.11 elaborate on the temperature changes. Considering that silicon is transparent to the Flir camera in the temperature range used, imaging upside down provides the same results in terms of temperature origin as when the sensor is right side up (except for an inverted image). For doped silicon, any temperature gradient over a small area becomes visible and can be significant in terms of sensor functionality. The separation between each box is only a matter of microns (possibly millimeters) and therefore temperature changes of even only 1° C are notable. Figures 4.10 and 4.11 reinforce that Box 4 is the hottest and Box 1 is the coolest. We can conclude that the edges of the chip dissipate more power.

5

Conclusion

5.1 CV/IV Studies

Current-Voltage studies were performed to learn about breakdown voltages for each wafer and Capacitance-Voltage studies were performed to estimate each sensor's depletion depth.

Wafer 2 sensors have a resistivity of 20 Ohm-cm, wafers 6 and 8 have a resistivity of 200-400 Ohm-cm, and wafers 10 and 11 have a resistivity of 10k Ohm-cm. Wafers 2, 6, and 8 showed conventional exponential curves for IV tests and hit breakdown after applying 100-300V. After edge polishing of the sensors, W06S12 and W08S12 had higher breakdown voltages by 30-50 volts while W02S09 did not have a noticeable difference. Various W10 and W11 sensors exhibited unusual linear IV curves which made it increasingly difficult to determine the breakdown voltages. Further testing of W10 and W11 sensors showed that current was abnormally high with sensors hitting a compliance of 10mA around 125-275 volts.

None of wafers 2, 8, 10, or 11 have CV tests that comply with theory. However, the deviations per wafer are different. More specifically, W2 exhibits a non-linear and exponentially growing curve before full depletion. W6 has data that follows theory with a positive linear trend until around 150V, and then a sharp increase in $\frac{1}{C^2}$. For W10, high frequency (10kHz) capacitance data begin to resemble the theoretical function's slope, except that the experimental data seems more exponential than linear.

One reason why none of the CV tests comply with the theoretical functions is that the theoretical functions assume full pitch depletion. At bias voltages much lower than what is required to generate full depletion, only the implant and area near the implant depletes. Beside this geometrical limitation in the relative low voltage regimes, the reason for larger CV shape discrepancies is unknown.

It is important to note that due to the geometry of the probe station setup, it is likely that the copper plate only makes contact with the sensor at one location: right near the vacuum hole. Considering that these sensors lack metallization on their backside, the placement of the sensor on the vacuum hole could impact certain measurements if the sensor's backside conductivity is non-uniform. A better setup would be if there were several vacuum holes touching on the sensor at different spots; this would ensure that the backside potential is uniform.

5.2 Laser e-TCT Studies

Laser Edge Transient Current Technique studies were performed to determine depletion depth estimates for various wafers by utilizing the full width half maximum (FWHM) of high voltage amplitude x-projections. This test is also intended to shine light on individ-

ual relationships between bias voltage and signal amplitude for the different wafers, whether it be through 2D voltage histograms, pulse (waveform) analyses, or pulse max profiles.

Upon scanning through the depths of W02S09, W06S04, and W10S09, further abnormalities surfaced. The signal amplitudes for 2D voltage amplitude histograms as well as pulse and pmax plots for W2 and W6 show that signal decreases for decreasing voltage. Conversely, W10 data for the same tests show that signal increases for decreasing voltage. Knowing that an increased bias voltage will increase the depletion depth of a pixel, the larger space charge region allows for charge carriers to induce current throughout a larger volume of the pixel, increasing the current signal which translates to a voltage amplitude. Therefore, the behavior of W2 and W6 chips are as expected, where the W10 behavior is atypical.

The voltage wave forms from the manual voltage ramping tests in the e-TCT setup augment the W10 abnormalities. Not only does the voltage amplitude decrease with an increased bias voltage, but the wave forms lose their shape; the widths of pulses in terms of time decrease almost exponentially and the peaks themselves shorten as the voltage increases. This led to the interpretation that for high resistivity wafers, the bias voltage range is too high. The voltage therefore incapacitates various transistors which interferes with the regulation of voltage and amplification of signals.

Additionally, the W6 and W10 voltage amplitude 2D histograms and pulse/pmax plots show an halo effect where there is strong signal past 500 microns in depth. One theory about this phenomenon is that electrical and optical diffusion is prominent and allows for subsequent pixels to possibly receive particles from the laser beam, inducing current in various depletion regions.

5.3   IR Studies

IR studies were conducted in order to determine where high power dissipation was emanating from on high resistivity wafers. Along the way, an issue arose with a manual IV setup that led to further conclusions regarding wafers 10 and 11.

For low resistivity wafers, manual IV tests on sensors bonded to PCBs returned results comparable to those from probe station IV tests. Wafers 10 and 11 manual IVs hit compliance of 10mA consistently at or before 20V; this result suggested a problem with the manual IV setup that only manifested when testing high resistivity chips. This issue became clarified upon testing various sensors by comparing the potential differences between the bias voltage moving through the HV pads on the lower left side of the chip and the voltage through the copper plate, representing the potential in the middle of the sensor's backside area. W10S09 had relatively constant chuck potential readings, only varying from [-0.275V,-.574V] over a range of [0, -10V] bias voltage. However, the potential difference between chuck and bias voltage for W06S12 was small as chuck voltage changed from [-0.317V, -9.57] over the same [0, -10V] bias voltage range. This results in the idea of a potential gradient across the backside surface area of the high resistivity sensors. Using insulating tape to connect the PCB to the bottom of the sensor solved the high current issue from the initial manual IV tests at the black box, further supporting the potential gradient hypothesis.

In regards to thermal imaging, for W10S10, various heat maps showed increased temperatures on the edges of the sensor and lower temperatures in and around the pixels. This result for W10S10 denotes higher power dissipation on the edges of the chip and lower dissipation near the center, further supporting the idea of a voltage gradient along the

backside of high resistivity wafers. Lower resistivity sensor infrared images are not included because the lower current per bias voltage causes less power dissipation and therefore smaller variations in the heat map; this behavior is expected for unproblematic sensors with low current.

This conclusion provides a possible explanation of why the initial IV tests on the probe station from Chapter 2 would exhibit significantly high current. The voltage gradient through the sensor backside and increased heat on the sensor edges indicates increased resistance or current present at the sensor edges. Additionally, there is a temperature difference between the pixel edge and the pixel center, where the pixel edge is hotter. This indicates that additional surface leakage currents must be induced in each pixel's CMOS electronics and in the sensor's edges to create the temperature differences. Moreover, a sensor's resistivity determines how conductive the substrate material is. With a very high resistivity (10k Ohm-cm), it is likely that more leakage current would be flowing through the transistor channels. The leakage current might be so high that it incapacitates parts of the transistors or amplifiers in certain pixels. This would make the pulse shapes inconsistent for high resistivity wafers over even a small voltage range, as seen in Chapter 3. This higher leakage current would be the cause of the increased power dissipation of the sensor and the CMOS electronics, as seen in Chapter 4.

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