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Publication Date

2023-03-01

Peer reviewed

2023 IEEE American Power Electronics Conference (APEC 2023)

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***Abstract*—Prior work has shown that a power converter's commutation loop inductance is critical to switching performance. For designs with surface-mount components, this inductance may be minimized through the use of clever layout techniques. But for many applications, power transistors with large through-hole packages are used, due to their low junction-to-case thermal impedance and compatibility with heatsinks, both of which allow for high power handling capability. In this work, a small surface-mount GaN transistor is added in parallel to the large through-hole Silicon power transistor to improve switching performance. Together with a low-side anti-parallel diode and decoupling capacitor, it forms a smaller commutation loop such that the switching transition can be fast with low overlap loss. A simple method is introduced to control both the power and decoupling devices with a single gate driver. A 250 W, 50 V buck converter is designed, with measured results demonstrating significant improvements in efficiency.**

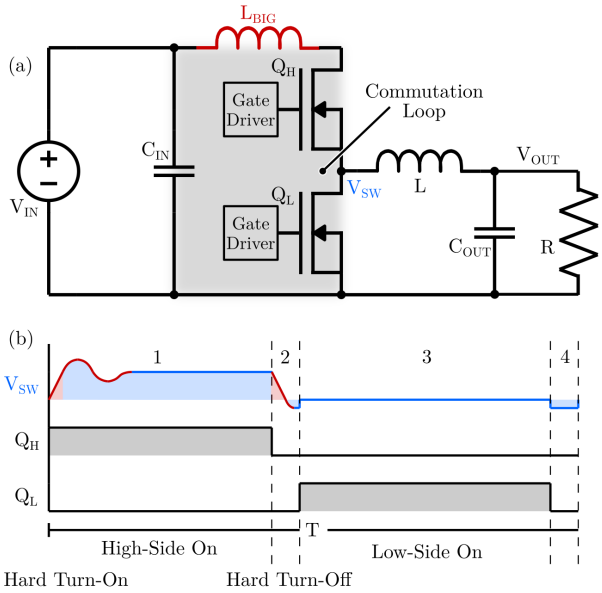

Fig. 1: Normal buck converter with commutation loop inductance modeled as a single lumped L_{BIG}. (a) Schematic, (b) Modulation diagram highlighting the overshoot, reduced switching speed, and EMI caused by this parasitic inductance.

I. Introduction

Prior work has shown that a power converter's commutation loop inductance, which arises from the physical layout of the switching components, is critical to its performance [1]–[3]. This parasitic inductance affects the switching speed, voltage overshoot, and electromagnetic interference. For designs with small, surface-mount devices, it may be minimized through the use of clever layout techniques [4]–[7]. But for many applications, power transistors with larger through-hole packages (e.g. TO-220, TO-247, TO-252) are used, due to their low junction-to-case thermal impedance and compatibility with heatsinks, both of which allow for high power handling capability. These devices have long leads which inhibit low commutation loop inductance design. Fig. 1a shows a standard buck converter schematic with the commutation loop inductance modeled as L_{BIG}. During switching transitions, this large inductance will resonate with the output capacitance, C_{OSS}, of the devices, and large voltage overshoot will occur. Furthermore, the large gate-to-source inductance can lead to false turn-ons via the Miller effect. In order to mitigate these issues, gate resistance may be increased to slow down the switching transition, but this will cause even greater overlap loss. Alternatively, various snubber circuits have been developed to reduce overshoot, overlap loss, and output capacitance hard-charging loss [8]. These circuits are designed to redirect the reactive energy in the main commutation loop. Dissipative snubbers typically do not provide significant efficiency improvements, while regenerative snubbers require extra active circuitry along with magnetics, which increases size, complexity, and cost [9]–[12].

In this work, a small surface-mount switch is added in parallel to the large through-hole power transistor in a buck converter to improve switching performance. Unlike other snubbers, this switch will act in place of the main power device during the switching transitions, and will form a much smaller commutation loop together with the low-side anti-parallel diode and decoupling capacitors. The switching transition can therefore be fast with low overlap loss. The use of hybrid switches has

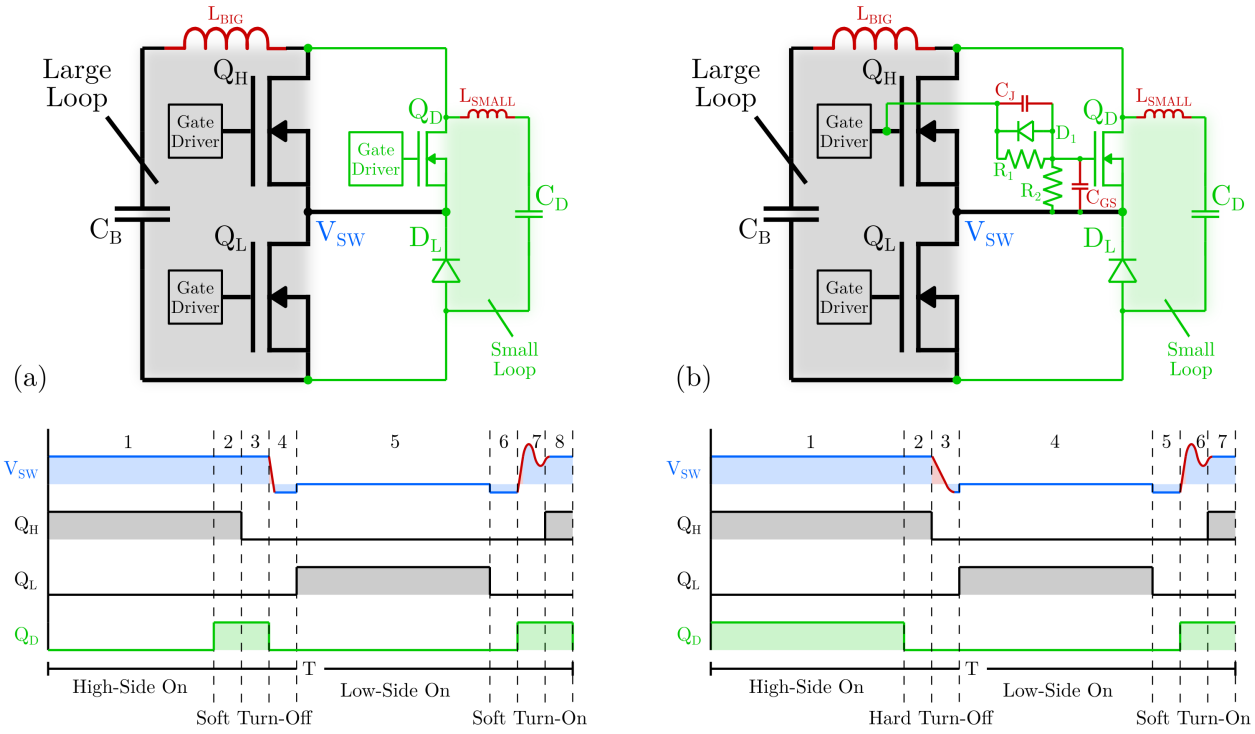

Fig. 2: Schematic and modulation diagram for each decoupling device method. Main loop shown in black, decoupling loop in green, and parasitic components in red. (a) Method 1: Requires separate gate driver and two on-times for Q_D, (b) Method 2: Gate signal voltage divider utilized so only one high-side gate driver is needed.

been demonstrated, typically for a field-effect transistor (FET) in parallel with an insulated gate bipolar transistor (IGBT) [13], [14]. This work extends prior art by paralleling a GaN HEMT with a Silicon FET and focusing on commutation loop and gate drive design considerations to develop a practical, high-performance solution.

A 250 W, 50 V buck converter is designed with TO-247 package devices to validate this concept. Two gate drive methods are tested, and measured results demonstrate significant improvements in efficiency. The remainder of this paper is organized as follows: Section II details the principle of operation for each method while Section III introduces hardware to validate the proposed approach and presents efficiency measurements. Finally, Section IV concludes the paper.

II. Design

This work proposes a circuit which provides a parallel low inductance path during the switching intervals. One active switch is required, which is named a decoupling device. Along with a decoupling capacitor and low-side anti-parallel diode, it comprises a small commutation loop which undergoes the hard-switching transitions, while the main power transistor handles the steady-state current conduction. Two different gate drive methods are compared for use within a buck converter.

A. Normal Buck Operation

Fig. 1b shows the modulation diagram for a standard buck converter. There are 4 states of circuit operation. State 1: The high-side transistor, Q_H, turns on, and the high-side on phase begins. This turn-on is "hard" or lossy. The large di/dt in L_{BIG} causes voltage overshoot on the switch node which generates EMI and can damage the active devices if their blocking voltage is not sufficiently overrated. Energy stored in the output capacitance of Q_H ($C_{OSSH}V_{IN}^2/2$) and the energy required to charge up the output capacitance of the low-side transistor, Q_L, ($C_{OSSL}V_{IN}^2/2$) are both lost. In addition, during the switching transition, Q_H conducts current and blocks voltage simultaneously, which creates overlap loss proportional to the duration of the switching interval. These switching loss mechanisms diminish efficiency and generate heat. State 2: Q_H turns off slowly due to L_{BIG} and incurs overlap loss once again. The buck converter will naturally soft-discharge the output capacitances here, so hard-charging loss and diode conduction loss can be greatly reduced or even eliminated, provided that the deadtime duration is controlled appropriately and the switch can turn off quickly enough, which may be challenging for large parts. State 3: Q_L turns on softly and the low-side on phase begins. State 4: Q_L, turns off and diode conduction occurs.

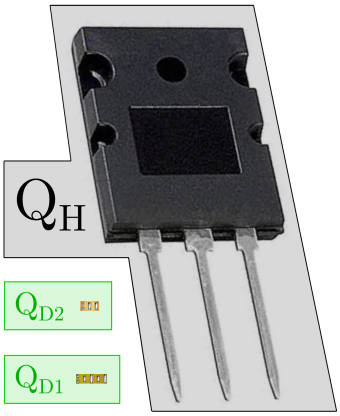

Fig. 3: Demonstrating size difference between the main power and decoupling devices.

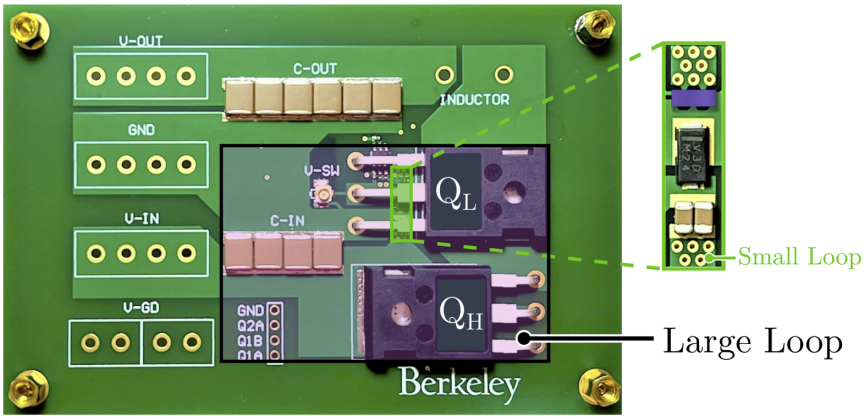

Fig. 4: Annotated picture of hardware used for measurements. Large commutation loop of Q_H, Q_L, and C_{IN} highlighted. Small commutation loop of Q_D, C_D, and D_L shown in green inset.

Table 1: Hardware Prototype Component List

Component	Part Number	Parameters
Main Power Transistors (Q_H,Q_L)	IXYS IXFH180N20X3	200 V, 6.3 mΩ
Decoupling Device 1 (Q_{D1})	EPC 2207	200 V, 22 mΩ
Decoupling Device 2 (Q_{D2})	EPC 2012C	200 V, 100 mΩ
Bulk Capacitors (C_{IN})	TDK CGA9P3X7T2E225K250KA	250 V, 2.2 uF
Decoupling Capacitors (C_D)	TDK C2012X7T2W473K125AA	450 V, 47 nF
Anti-Parallel Diode (D_L)	Vishay V3P22HM3/H	200 V, 3 A
Gate Driver	TI LM5114A	5 V, 7.6 A

B. Method I: Interval Only

Fig. 2a shows the schematic and the modulation diagram for Method 1. The decoupling device is labeled Q_D. It is placed in parallel with Q_H because the high-side transistor has hard transitions in a buck converter (in a boost topology, the decoupling device would be connected parallel to the low-side power transistor). The decoupling device operates only during the switching intervals, and remains off during the rest of the period. For this method, there are 8 separate states of circuit operation. State 1: Normal high-side on phase. State 2: Q_D turns on so that it can carry the full load current during the high-side turn-off transition. State 3: Q_H turns off softly because Q_D maintains current conduction. State 4: Q_D turns off very fast with little overlap loss as a result of a highly compact gate drive loop and small commutation loop inductance, L_{SMALL} (highlighted in green in Fig. 2a). Subsequently, as with the conventional buck, the output capacitances of Q_H and Q_L are soft-charged and discharged, respectively, with low loss until the switch node, V_{SW}, reaches zero volts and diode D_L begins conducting. State 5: Normal low-side on phase. State 6: Q_L turns off and diode D_L resumes conduction for the allotted deadtime duration (ideally short for reduced losses). State 7: Q_D turns on and initiates fast rise in switch node voltage, with low overlap loss or overshoot due to L_{SMALL}. State 8: Q_H turns on softly because Q_D is already on and begins to conduct the load current. The decoupling switch is not sized to carry the full load current continuously, only during the short switching transitions, so it can be small and it does not require a heatsink. The gate signals of the main power transistors are unaffected by the addition of the decoupling switch, but Q_H now turns on and off softly, and the switching transitions are much faster than what is achievable with only the large commutation loop, leading to reduced overlap loss. One major drawback of this method is that the decoupling switch requires its own high-side gate driver and PWM signal. This adds cost and complexity, but brings improvements in efficiency which in many applications may be preferred.

C. Method II: Fully Parallel

An alternative option is to utilize the same gate signal for both Q_H and Q_D. GaN HEMTs and Silicon FETs have different optimal gate drive voltages, however, so 3 small surface-mount passive components must be added to divide the gate signal down. In this case, the only added circuitry is Q_D and these passives (along with D_L and C_D, which are often utilized even without a decoupling device). Fig. 2b shows the schematic and modulation for this option. Q_D will naturally turn on before Q_H, due to its much lower gate capacitance and package inductance. It will also turn off before Q_H, producing no altering effect. However, as previously noted, the high-side turn-off transition is inherently soft in a buck converter, and thus the high-side turn-on is much more important for efficiency. With Method I, the switch could be sized very small because it does not carry the load current for long. For Method II, Q_D must be sized with sufficiently large R_{DSON} so that Q_H carries most of the current when both Q_D and Q_H are on, but it cannot be so large that it creates excess loss or heat while it carries the full load current during the switching transition. In this work, the on-resistance of Q_D is chosen to be approximately 10x that of Q_H. State 1: Normal high-side on phase. State 2: Q_D turns off before Q_H (due to smaller $R_{Gate}C_{ISS}$ time constant). Here, D_1 enables this fast turnoff by the gate driver. State 3: Q_H is turned off slowly due to L_{BIG} and diode-conduction dead-time occurs. State 4: Normal low-side on phase. State 5: Diode-conduction dead-time after Q_L turns off. State 6: Q_D turns on before Q_H and initiates fast rise in switch node voltage, with little overlap loss and minimal overshoot or ringing due to the small commutation loop inductance, L_{SMALL}. The junction capacitance of D_1, C_J, is sized such that it forms a high-frequency voltage divider with the input capacitance of the decoupling device, C_{GS}. R_1 and R_2 form the low-frequency portion of the divider. Together, these components allow for the GaN switch to be driven at any voltage level lower than the Silicon gate drive voltage, with minimal delay. State 7: Q_H turns on softly because Q_D is already on.

III. Results

A 50 V, 250 W buck converter is designed to assess the merit of the proposed decoupling device and corresponding gate drive circuit. Fig. 4 shows an annotated picture of the hardware. The main power transistors are placed very close together, with the drain tabs soldered onto the PCB. This provides the lowest possible commutation loop inductance for the large loop, and real designs (e.g. with the power transistors mounted to heatsinks) could see far worse performance if decoupling is not employed. Q_D, C_D, and D_L are placed underneath the leads of the low-side device, as shown in the inset of Fig. 4,

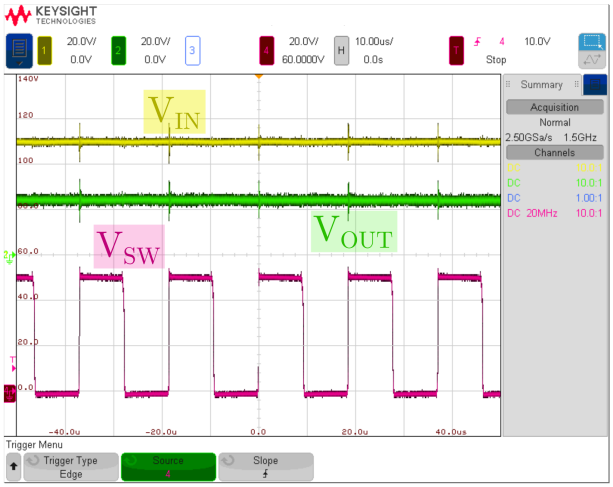

Fig. 5: Measured switch node and output voltage waveforms.

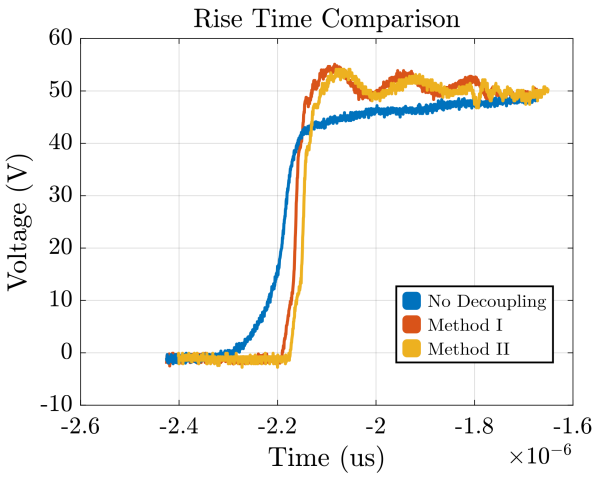

Fig. 6: Measured rise times for each method.

with a hybrid layout [2], [15] to minimize the small loop inductance as well. Fig. 3 highlights the dramatic difference in size for the decoupling devices utilized in this work (chip-scale land grid array package) versus the main power transistors (TO-247 package). Table 1 lists the components used. Efficiency measurements with forced air cooling are taken at a switching frequency of 50 kHz, as shown in Fig. 7 and Fig. 8, comparing operation without the decoupling device, Method I with an EPC2207 used for Q_D, and Method II with an EPC2012C as Q_D. As can be seen, up to a 55% reduction in power loss can be achieved when the proposed decoupling is employed. Fig. 5 shows the switch node, input, and output voltage, while Fig. 6 demonstrates the drastic decrease in rise time afforded by this technique.

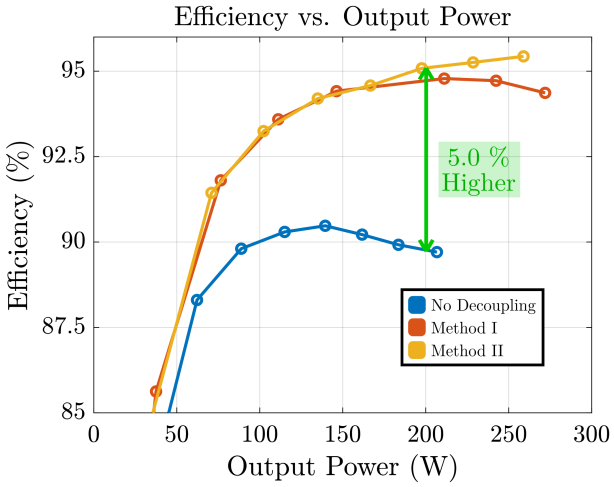

Fig. 7: Measured efficiency data across output power.

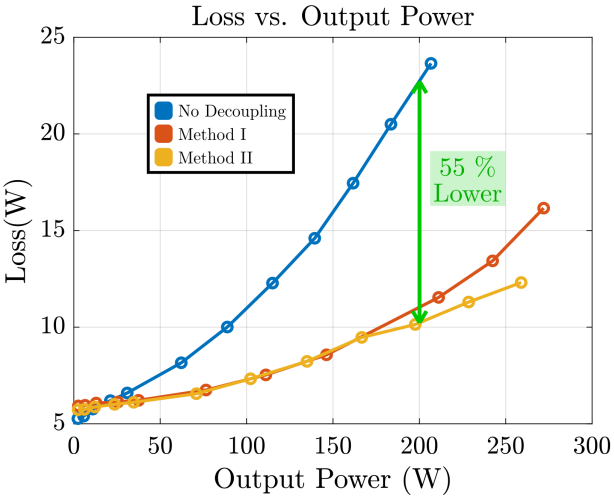

Fig. 8: Total converter loss across output power.

IV. Conclusion

This paper has presented a circuit design which places a small GaN HEMT in parallel with the large Silicon through-hole power transistor to greatly reduce the commutation loop inductance and increase the switching speed. Two different gate drive schemes are explained and then compared experimentally in a 50 V, 250 W buck converter. For both methods, significant improvements in efficiency were realized. More than 50% of the losses were eliminated with the decoupling device added. Method 1 allows for fast turn-on and turn-off switching transitions. Method II does not require an added gate signal or driver, but still achieved very similar efficiency results to Method I, so it provides good performance with minimal added complexity and cost.

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