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Publication Date

2022-03-24

DOI

10.1109/apec43599.2022.9773452

A Symmetric Dual-Inductor Hybrid Dickson Converter for Direct 48V-to-PoL Conversion

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***Abstract*—This work introduces a new Symmetric Dual-Inductor Hybrid (SDIH) Dickson DC-DC converter topology that is suitable for large conversion ratios where regulation is required, such as direct 48 V to Point-of-Load (PoL) applications. A Dickson-type switched-capacitor network is used to effectively produce two interleaved PWM drives with a greatly reduced voltage amplitude relative to the input line voltage, in turn allowing magnetic volume to be reduced while retaining modest switching frequencies. Both even and odd order switched-capacitor networks can be used with straight-forward split-phase switching allowing either network type to achieve complete soft-charging of all fly capacitors. Additionally, charge flow is well balanced through all elements, with equal capacitor and inductor values being preferred. Subsequently this topology is expected to simplify component selection, improve electrical and thermal performance, and reduce cost. A discrete prototype measuring 0.176 inch^3 demonstrates very high measured power densities of 768 W/in^3, 751 W/in^3, and 598 W/in^3 for regulated output voltages of 3 V, 2 V, and 1 V respectively while switching at a frequency of 750 kHz.**

I. Introduction

As data center power consumption continues to increase, the prevalence of higher bus voltages, including 48 V, have become common place in an attempt to reduce ohmic losses in the power distribution network. However, this shift towards high voltage local power distribution necessitates highly compact power converters with very large conversion ratios and regulation capability, which are situated proximal to the intended low voltage load. As such, significant effort has been put into improved power delivery techniques, with power density being a key metric used in surveying eligible converter architectures. In this work we introduce a new converter topology that is similar to the recently introduced Dual-Inductor Hybrid (DIH) Dickson converter [1]–[4]. However, due to its symmetry the proposed design inherently has balanced charge flow through both of its inductors and all of its switches, simplifying design effort and improving component utilization [5], [6]. To ensure complete soft-charging [7] of all fly capacitors, split-phase switching [4], [8] is required on two pairs of switches for either odd or even order switched-capacitor networks, although; both pairs operate with a 180° phase shift, and as such the timing of only one split-phase event need be calculated in practice.

An earlier rendition of this topology, instead using a Cockcroft-Walton type capacitor network, was alluded to in [9], but suffers from much increased split-phase timing complexity when active devices are used in place of diodes, particularly at higher conversion ratios [10]. Conversely, the switching complexity of the Dickson variant proposed here remains fixed, irrespective of conversion ratio, with straight-forward duty-cycle adjustments enabling output regulation.

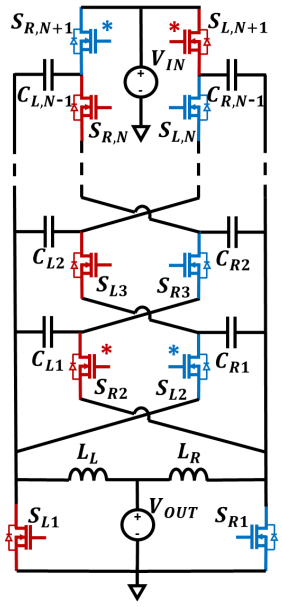

Fig. 1: Proposed Symmetric Dual-Inductor Hybrid Dickson converter. Switches requiring split-phase switching [4], [8] are marked with an asterisk (*), assuming all fly capacitors are equal in size.

Section II describes converter operation and briefly calculates both conversion ratio and split-phase timing requirements. Section III showcases a hardware prototype and compares its results with recent state-of-the-art converter solutions. Section IV concludes the paper.

II. Proposed Symmetric Dual Inductor Hybrid (SDIH) Dickson Converter

The switching progression for the proposed topology is illustrated in Fig. 2 where all capacitors are set equal in size and where the phases progress left to right, *Phase* 1*A* → *Phase* 1*B* → *Phase* 2 → *Phase* 3*A* → *Phase* 3*B* → *Phase* 4, before repeating as part of a periodic sequence. Due to the symmetry of the converter, phases {1A, 1B, 2} are largely identical to phases {3A, 3B, 4} respectively. As such, phases within the groupings {1A, 3A}, {1B, 3B}, and {2, 4} are all set equal in duration, simplifying control effort.

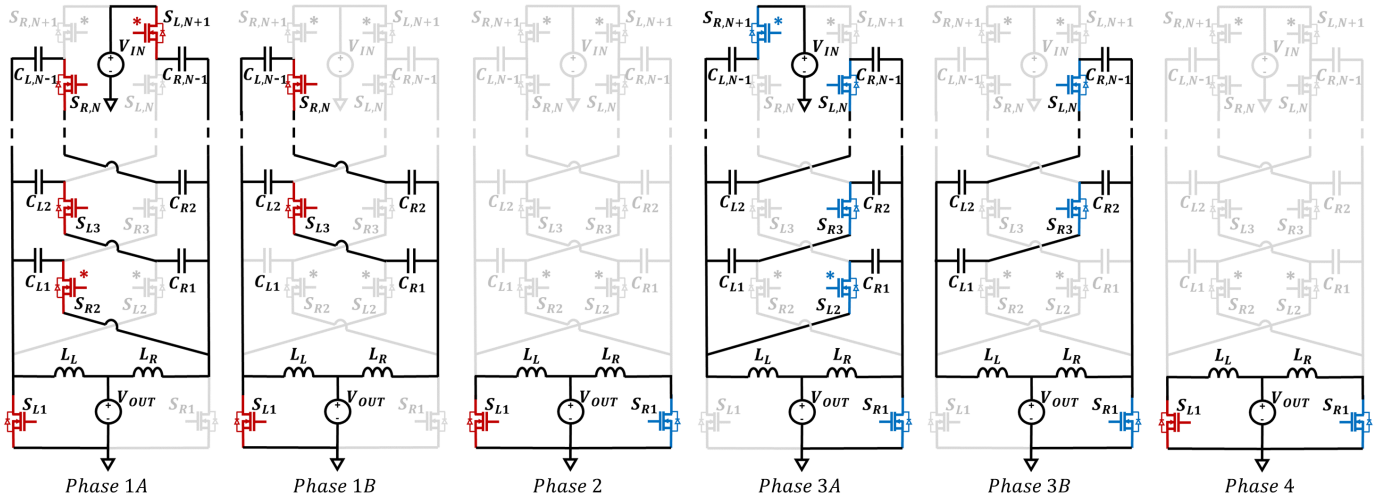

Fig. 2: Phase progression of the proposed SDIH-Dickson converter when optimized for step-down split-phase operation. Phases 1 and 3 are split into sub-intervals, A and B, thereby allowing all fly capacitors to undergo complete soft-charging [4], [8]. The four switches requiring split-phase operation are marked with an asterisk (*) and reside only at the extreme ends of the switched-capacitor network when all fly capacitors are set equal.

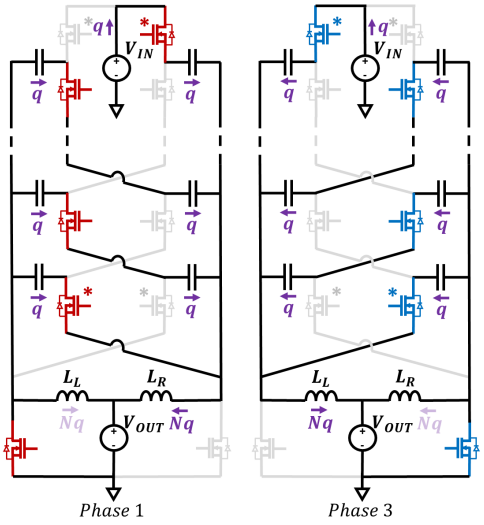

Fig. 3: Charge flow analysis through phases 1 and 3. Here sub-phases A and B are consolidated for simplicity.

The overall conversion ratio, assuming small inductor current ripple, is deduced by first applying the charge flow analysis described in [5], as depicted in Fig. 3, where relative charge quantities are normalized around the high-side charge quantity, q, conducted from V_{IN} during both Phases 1 and 3. Here, we find that each inductor conducts a charge quantity of $N \times q$ during both Phase 1 and Phase 3, where N is the order of the switched-capacitor network. Subsequently the overall converter conversion ratio can be calculated as

$$\frac{V_{IN}}{V_{OUT}} = \frac{I_{OUT}}{I_{IN}} = \frac{2Nq}{DT} \times \frac{T}{2q} = \frac{N}{D} \tag{1}$$

where

$$D = \frac{t_{1A} + t_{1B}}{T} = \frac{t_{3A} + t_{3B}}{T} \tag{2}$$

and lossless energy transfer is assumed. Note that there exists a maximum allowable duty ratio of $D_{MAX} = 0.5$ above which Phases 1 and 3 begin to erroneously overlap. As such, the minimum conversion ratio is $2N:1$.

To enable complete soft-charging of all fly capacitors, both Phases 1 and 3 are split into respective sub-phases A and B (as depicted in Fig. 2), effecting a technique termed split-phase switching in [8]. To determine the relative phase duration of Phase 1A with respect to Phase 1B — and likewise for 3A and 3B — split-phase analysis, such as that described in [8] and [11] is applied. By again assuming small inductor current ripple (as in [8]), the relative duration of A and B phases is described by

$$\frac{t_B}{t_A + t_B} = \frac{N-2}{2N} \tag{3}$$

However, do note that for finite inductor current ripple, the ideal split-phase timing deviates from that predicted by (3), with t_B becoming relatively shorter [3].

III. Experimental Results

A hardware prototype with an $N = 6$ switched-capacitor network, depicted in Fig. 4, was constructed on a 4-layer 0.6 mm thick PCB to validate the proposed topology. Power was delivered to the gate-drivers of all fourteen switches using cascaded bootstrapping [12], as illustrated in Fig. 5. Table I lists all components used. Despite their reduced energy density relative to Class II dielectrics, Class I (C0G) fly capacitors were used here for both their fine matching tolerance, stability, and low loss when subject to large voltage ripple [13], [14]. Figure 6 depicts the converter's volume breakdown where total converter volume is defined as a best-fit cuboid encompassing the entire design, including input and output capacitors.

Figure 8 plots measured efficiency versus output power at output voltages of 3 V, 2 V and 1 V, and omits a gate drive power loss of 1.62 μJ per switching period to facilitate comparison with data reported in prior art. Here we observe that below an output power of 60 Watts the inductor currents undergo a periodic reverse bias, thereby effecting zero-voltage switching on all switches and yielding a slight efficiency increase.

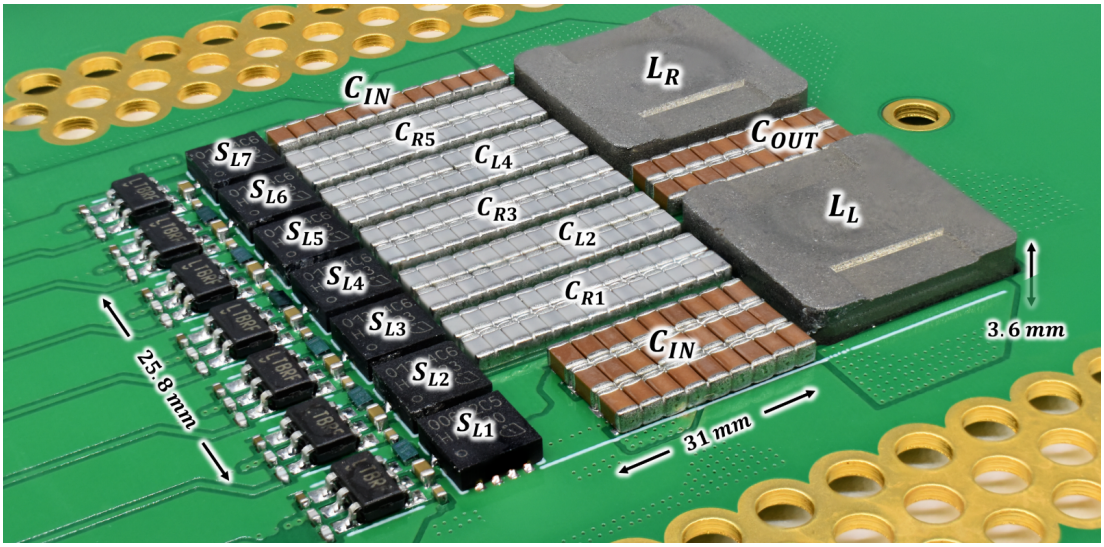

Fig. 4: Photograph of the constructed SDIH prototype with a capacitor network order of $N = 6$. Due to the proposed topologies symmetry, the reverse side is largely identical with inverse component naming on fly capacitors and switches. A best-fit cuboid encompassing all components measures 25.8 mm x 31 mm x 3.6 mm, where the converter's overall height is limited by through-plane inductors L_L and L_R.

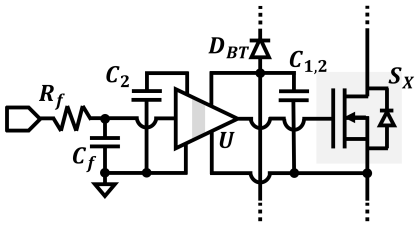

Fig. 5: Schematic of the gate driving circuitry and bootstrap power delivery used for all primary switches $S_{L,1-7}$ and $S_{R,1-7}$.

TABLE I: COMPONENT DETAILS

Component	Details	Part Number
L_L, L_R	150nH 55A 0.75mΩ	IHLW-4040CF-11
C_{IN}, C_{OUT}	98× 2.2μF 50V X5R 0603	GRT188R61H225KE13D
$C_{L,1\text{-}5}$, $C_{R,1\text{-}5}$	28× 10nF 50V C0G 0603	GRM1885C1H103JA01D
S_{L1}, S_{R1}	0.65mΩ 25V 298A	IQE006NE2LM5CGATMA1
$S_{L,2-7}$, $S_{R,2\text{-}7}$	1.35mΩ 40V 205A	IQE013N04LM6CGATMA1
U	High-side Gate Driver	LTC4440
D_{BT}	30V 0.5A Schottky	VSKY05301006
C_1	2.2μF 35V 0402	C1005X5R1V225K050BC
C_2	0.1μF 25V 0201	C0603X5R1E104K030BB
C_f	20pF 50F 0201	GRM0335C1H200JA01D
R_f	100Ω 0201	RMCF0201FT100R

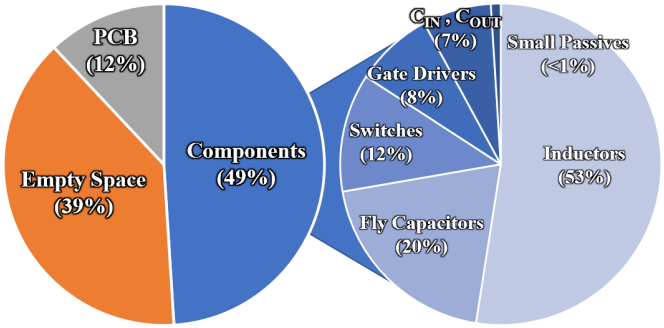

Fig. 6: Volume breakdown of the hardware prototype. Overall converter volume breakdown (left) and component volume breakdown (right).

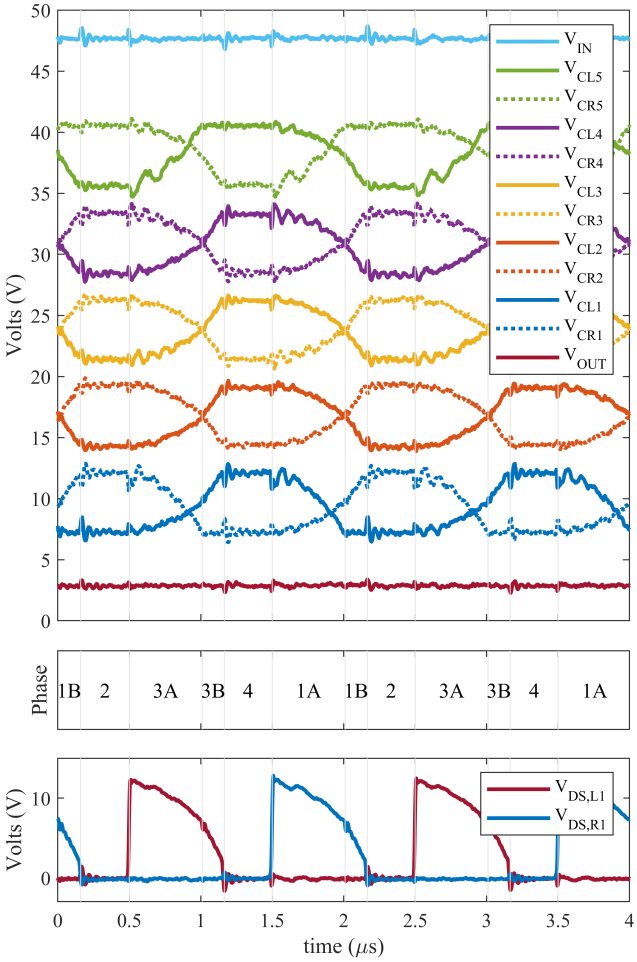

Fig. 7: Measured waveforms exhibiting large voltage ripple across all fly capacitors (top), implying effective passive utilization. The absence of abrupt voltage transitions on the fly capacitors illustrates complete soft-charging. $f_{SW} = 500\,\text{kHz}$, $I_{load} = 20\,A$. Drain-to-source voltages of switches S_{L1} and S_{R1} are also depicted (bottom) and represent the PWM signals presented to inductors L_L and L_R.

TABLE II: COMPARISON WITH PRIOR WORK

	APEC 2017 [15]	TIA 2019 [3]	COMPEL 2019 [16]	COMPEL 2020 [17]	ECCE 2021 [4]	**This work**
Conversion Ratio:	48V to 1V	48V to 1V-2V	54V to 1.5V	48V to 1V-2.5V	48V to 1V-3V	**48V to 1V-3V**
Topology:	Sigma (DCX + Buck)	DIH	LEGO-PoL	MLB-PoL	DIH	**SDIH**
Switch Type:	GaN FET	GaN FET & Diode	MOSFET	MOSFET	MOSFET	**MOSFET**
f_{SW} :	600 kHz	300 kHz	500 kHz	250 kHz	750 kHz	**750 kHz**
Inductor:	36 μH & 190 nH	2 × 1.5 μH	12 × 1 μH	2 × 600 nH	2 × 1 μH	**2 × 150 nH**
Peak Efficiency: (excl. Gating Loss)	93.5% @1V	95.02% @2V 93% @1V	93.1% @1.5V	95.6% @2.5V 95.1% @2V 93.1% @1V	93.8% @3V 92.2% @2V 87.5% @1V	**89.8% @3V** **88.2% @2V** **83.5% @1V**
$P_{OUT\text{-}MAX}$:	80 A @1V	10 A @2V 10 A @1V	300 A @1.5V	65 A @2.5V 65 A @2V 65 A @1V	50 A @3V 60 A @2V 70 A @1V	**45 A @3V** **66 A @2V** **105 A @1V**
Efficiency @ $P_{OUT\text{-}MAX}$: (excl. Gating Loss)	92% @1V	94.5% @2V 92.3% @1V	78% @1.5V	92.1% @2.5V 91.3% @2V 86.8% @1V	91.1% @3V 88.1% @2V 80% @1V	**88.0% @3V** **83.4% @2V** **71.5% @1V**
Component volume[(a)]	-	1.436 cm^3	5.859 cm^3	1.842 cm^3	2.756 cm^3	**1.197 cm^3**
Power Density[(a)]: ($W/inch^3$)	-	228 @2V 114 @1V	1,259 @1.5V	1,445 @2.5V 1,156 @2V 578 @1V	892 @3V 715 @2V 422 @1V	**1,848 @3V** **1,807 @2V** **1,438 @1V**
Power Density[(b)]: ($W/inch^3$)	420 @1V	-	152 @1.5V	494 @2.5V 395 @2V 198 @1V	524 @3V 419 @2V 246 @1V	**768 @3V** **751 @2V** **598 @1V**

[(a)]Considering power stage components only (fly capacitors, inductors, switches, and diodes).
[(b)]Best-fit cuboid encompassing entire converter solution.

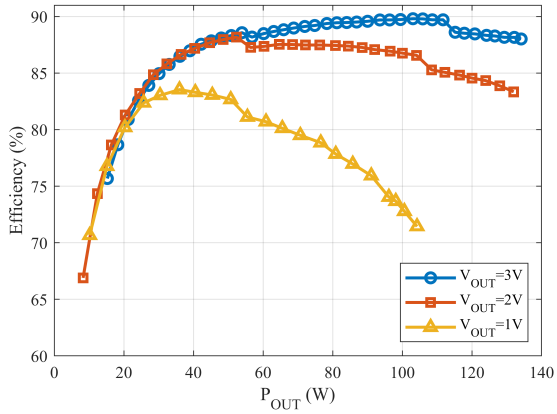

Fig. 8: Measured efficiency curves for the proposed SDIH-Dickson topology while switching at 750 kHz.

At heavier loads the voltage ripple on the fly capacitors is increased to the extent that the voltage expressed on $V_{DS,L1}$ and $V_{DS,R1}$ eventually extends to 0 V during Phases 1 and 3, inducing reverse conduction in S_{L1} and S_{R1} (waveforms in Fig. 7 are approaching this condition). Once reached, the efficiency sees an additional decrease with body diode conduction losses introduced at heavier loads. To circumvent this occurrence, the Farad value of the fly capacitors, or the converter switching frequency, f_{SW}, may be increased.

We note that switches S_{L2-7} and S_{R2-7} were chosen for ease of implementation, given their identical footprint to S_{L1} and S_{R1}, but are significantly oversized. As such, a future iteration can expect a significant reduction in switching losses.

To exemplify converter operation, Fig. 7 depicts measured voltage waveforms at a relaxed switching frequency of 500 kHz. Bar some imposed measurement and switching noise, all fly capacitors experience gradual voltage transitions, implying complete soft-charging with no abrupt changes in voltage. Moreover, in this demonstration fly capacitors are operated with very large voltage ripple (∼5V), indicating very high passive component utilization. Table II compares this work against recent state-of-the-art, demonstrating compelling measured power densities with this design, despite the use of low density Class I dielectrics and greatly oversized switches.

IV. CONCLUSION

This paper demonstrates a new Hybrid Dickson-type topology that is well suited for large regulated conversion ratios, such as 48V-to-PoL applications. Due to the symmetry of the proposed topology, charge flow is equally distributed through all opposing components and the clock timing complexity required — in order to facilitate complete soft-charging of all fly capacitors — is fixed and independent of capacitor network order (odd and even inclusive). Subsequently, a 48 V discrete hardware prototype demonstrates very high power densities of 768 W/in^3, 751 W/in^3, and 598 W/in^3 for regulated output voltages of 3 V, 2 V, and 1 V respectively.

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