UNIVERSITY OF CALIFORNIA
RIVERSIDE

# Millimeter-Wave Radio Frequency Switch Design for 5th Generation Wireless Networks and Advanced Electrostatic Discharge Design

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Mengfu Di

March 2022

Dissertation Committee:
Dr. Albert Wang, Chairperson
Dr. Ming Liu
Dr. Ran Cheng

The Dissertation of Mengfu Di is approved:

_____

_____

_____

Committee Chairperson

University of California, Riverside

ACKNOWLEDGEMENTS

This day has finally come for me to put a summary on the 4 years of PhD. It is a long journey full of memory and adventure, especially for the past two years in pandemic. As an individual who was confined in his apartment and hardly stepped out, I even wanted to write a novel on Covid-19 as a tribute to The Plague by Albert Camus. And due to practical reason, I completed my thesis instead of a novel. Afterall, life is life.

I am not walking alone on the road of PhD, and I could not have gone so far without the people around me. I would like to thank those people who have been so kind and helpful to me throughout this time.

First, I want to offer my heartfelt gratitude to Prof. Albert Wang, my advisor. He is a role model for me to follow for the entire life, in every aspect of research, work and life.

Besides my advisor, I would like to thank the rest of my dissertation committee: Prof. Ming Liu and Prof. Ran Cheng, for their suggestions and guidance.

It's my honor to get to know my fellow labmates, Dr. Chenkun Wang, Dr. Feilong Zhang, Dr. Qi Chen, Dr. Cheng Li, Mr. Han Wang, Ms. Zijin Pan, Mr. Weiquan Hao and Mr. Xunyu Li. I have learned so much from each of you and I will keep in mind the time we spent together in the lab.

I am grateful to OnSemiconductor and GlobalFoundries for providing me an opportunity to join as an intern. And thank my managers and supervisors: Carol Zhan, Lin Lin and Robert Gauthier, for patiently mentoring me and making me a part of the team.

Last and most importantly, I want to thank my parents and my girlfriend, Manjing Gao. I was like a raft in the middle of stormy sea, you were the lighthouse to guide my direction at the darkest night.

ABSTRACT OF THE DISSERTATION

Millimeter-Wave Radio Frequency Switch Design for 5th Generation Wireless Networks and Advanced Electrostatic Discharge Design

by

Mengfu Di

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, March 2022
Dr. Albert Wang, Chairperson

The fifth generation of wireless network technology is known as 5G. After 1G, 2G, 3G, and 4G, 5G is the next step in the wireless development. Compared with 4G Long Term Evolution (LTE), higher amounts of data can be transmitted more efficiently with 5G. This translates into superior speed data for dense areas, network access everywhere and low latency/high mobility connection, which can provide support for future user cases such as internet of things (IoTs), automotive, real-time remote surgery or cloud gaming. From these user cases, we can define the requirements of 5G: higher data rate, lower latency and better coverage. To achieve these requirements, there are several practical things we can do and actually, all research groups and companies are moving towards those directions, like macro base-station, beamforming, massive multiple input multiple output (MIMO) and millimeter-wave (mm-wave) band communication. These technologies will rely on more complex multi-band, multi-frequency front end module (FEM). The number

of both antenna and FEM will increase for 5G. So as a bridge from chip to outside antenna, the antenna switch modules (ASM) performance will be more and more critical. Their performance must satisfy not only the criteria of insertion loss and isolation, but also the needs of 5G applications, which include faster data speeds, higher power and enhanced reliability.

In this dissertation, ESD protected 28GHz, 38GHz and 60GHz wide-band travelling wave switches are presented in Chapter 3, which achieves comparable performance with state-of-art design and is the first travelling wave switch on SOI with co-design ESD protection. To reach a higher data rate with available frequency bands, millimeter wave (mm-wave) switches (38GHz/60GHz) has been demonstrated with the consideration of reliability issue of electrostatic discharge (ESD) which will introduce severe parasitic effects under this frequency level and degrade the performance of RFICs. The insertion loss and isolation together with ESD protection capability have been compared which shows the importance of ESD-RFIC co-design.

On the other hand, it is reported recently that conventional pad-based charged-device-model (CDM) ESD protection method may be theoretically wrong. Chapter 4 analyzes the failure of classic pad-based ESD protection methods in CDM ESD protection and discusses a disruptively new non-pad-based internally distributed CDM ESD protection concept, which is demonstrated in an oscillator IC designed and fabricated in a 45nm SOI CMOS process. Design of novel interposer and through-silicon-via (TSV) based internal-distributed CDM ESD protection mesh networks are also presented.

For first-silicon success and time-to-market, successful simulation before silicon is critical, especially for high-cost advanced technologies. The same is true for ESD protection. Chapter 5 introduces a new mixed-mode TCAD ESD simulation flow using combined HBM-TLP stimuli, or CDM-VFTLP stimuli, to enable ESD protection design prediction and verification. It provides a thorough analysis of various TCAD ESD simulation scenarios using both real-world HBM and CDM ESD waveforms, and their corresponding TLP and VFTLP square waveforms, in both single-pulse and pulse train manners, as stimuli.

However, for large size MOSFET RF switch (width > 1mm), they are usually used as ESD self-protection device, which means no external ESD device will be added. In Chapter 6, we discussed the implementation of a novel ESD shell model which enables the ESD self-protection simulation for RF switches for cell phone FEMs. As verified in hardware, >98% accuracy using simulation results can be achieved. Moreover, the ESD shell model can be easily placed in parallel to the FET base model in the schematic which is a simple and cost-effective solution to enable predictive ESD simulations of FEM switch devices.

# Contents

# List of Figures

# List of Tables

# Chapter 1 Introduction to 5G

## 1.1 Past, Present and Future

Wireless communication aims to deliver high-quality, dependable communication, and each new generation marks a significant jump in that direction as shown in Figure 1-1. The first generation (1G) of cell phone technology started in the late 70's. 1G used analog signal to transfer information, which only support voice call for a limited number of users simultaneously. The data transmission was at 150MHz and it had a maximum data speed of 2.4 Kbps, which sounds funny nowadays. Due the analog signal, phones' battery life was low, the voice quality was poor with no security, and lost calls were common.

Second-generation (2G) systems, as opposed to first-generation (1G) systems, employ digital multiple access technologies such as TDMA (time division multiple access) and

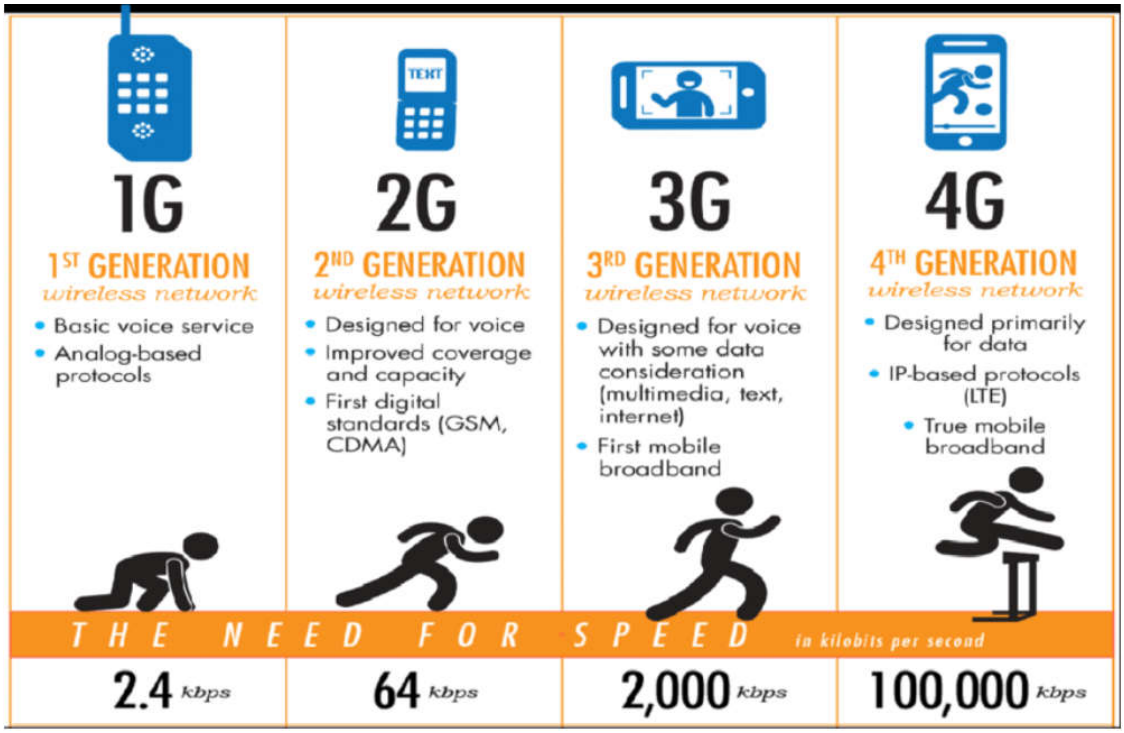



*Figure 1-1 Comparison between different generations of communication technology from 1G to 4G*

CDMA (code division multiple access) at 900MHz. To accommodate multiple users at the same time, the Global System for Mobile Communications, or GSM, employs TDMA technology. Worldwide, 2G networks are now still in use. Voice and limited data communications, such as fax and short messaging service (SMS), are supported by 2G, and most 2G networks offer various levels of encryption and security. With General Packet Radio Service (GPRS), the maximum speed is 50 Kbps, or 1 Mbps with Enhanced Data Rates for GSM Evolution (EDGE).

The third-generation (3G) mobile systems introduced web browsing, email, video call, picture sharing and other smartphone technology. The provision of seamless streaming services was the technological challenges addressed by third-generation (3G) mobile systems. The main network architecture of the 3G standard is UMTS, which stands for Universal Mobile Telecommunications System. This network combined features of the 2G network with new technology and protocols to provide much higher data rates. Advanced multiple access techniques were also being invented. Wideband Code Division Multiple Access (WCDMA) and CDMA Evolution Data Optimized (EVDO) provide data rates of up to 2 Mbit/s indoors, while WCDMA evolved to high-Speed Packet Access (HSPA) in the mid-2000s, allowing data rates of up to 14Mbps.

Currently, the most widely utilized technology is 4G Long-Term Evolution (LTE), which boosts capacity and internet speed by combining new radio interfaces with core network upgrades. Frequency division duplex (FDD) and time division duplex (TDD) have been employed in mobile communication in over 40 bands (TDD). When the device is moving, the maximum speed of a 4G network is 100 Mbps or 1 Gbps. For low mobility

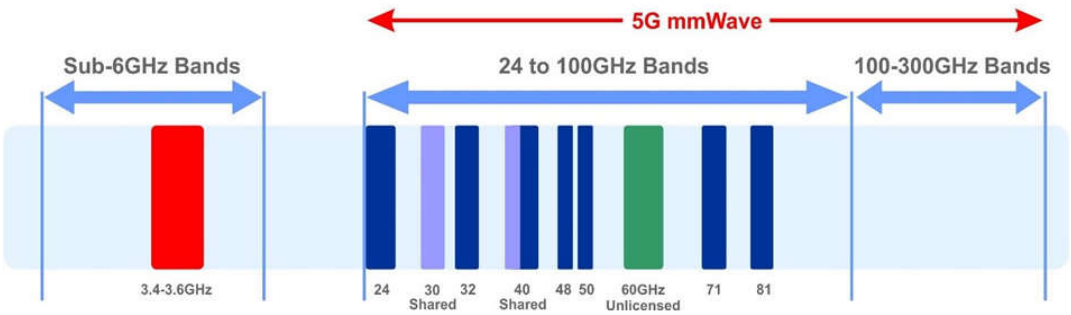



*Figure 1-2 5G spectrum driving towards the future.*

communication, such as when stationary or strolling, latency is decreased from roughly 300ms to less than 100ms, and congestion is greatly reduced. It can provide applications include amended mobile web access, IP telephony, gaming services, mobile Web, video conferencing, 3D television, and cloud computing. The key technologies that have made this possible are MIMO (Multiple Input Multiple Output) and OFDM (Orthogonal Frequency Division Multiplexing).

The fifth generation of mobile networks, or 5G, is the most recent cellular generation. It is enabled by a technology called New Radio (NR) which is based on OFDMA. 5G differs from previous generations of mobile networks in that it can accommodate a wide range of use cases because to its inherent flexibility. 5G is extremely fast and can accommodate a huge number of devices, allowing many sectors to digitize. It also has the ability to work in a variety of frequency ranges, including both high and low frequencies. The higher frequency bands have limited coverage but extremely low latency (less than 1 millisecond), making them ideal for real-time services. Lower frequency bands, inherently, have higher latency but much better coverage. As a result, lower frequency bands can help

with broad coverage of 5G in more areas (sub 6 GHz). Higher frequency bands (millimeter -wave), on the other hand, offer reduced latency and are thus perfect for real-time applications such as self-driving vehicles, manufacturing, virtual reality (VR), and IoT (Internet of Things) services.

Figure 1-2 shows the key spectrum driving toward 5G. The 28GHz, 38GHz and 60 GHz frequency bands will be the first commercial mm-wave 5G bands

## 1.2 RF Front-End Module

From these user cases discussed above, we can define the requirements of 5G: higher data rate, lower latency and better coverage. To achieve these requirements, there are several practical things we can do and actually, all research groups and companies are moving towards those directions, like macro base-station, beamforming, massive multiple input multiple output (MIMO) and millimeter-wave (mm-wave) band communication. These technologies will rely on more complex multi-band, multi-frequency front-end module (FEM).

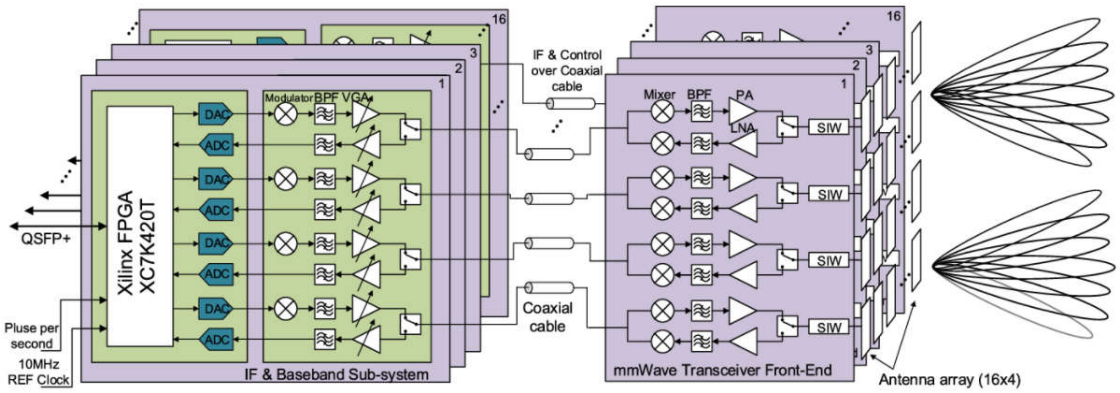



*Figure 1-3 5G MIMO Front-end-module block diagram* [1]

A front-end module is a generic word for all the circuitry between the antenna and the baseband processor in all RF signal transceivers, including Wi-Fi, Bluetooth, cellular, and GPS. It includes all components in the receiver that process the signal at the original modulated RF signal till demodulator, as well as all components in the transmitter that process the modulated intermediate frequency (IF) to antenna. The RF front-end module, which comprises the essential components such as switch, filter, low noise amplifier (LNA), power amplifier (PA), mixer, and so on, is shown in Figure 1-3. The MIMO application's multi-antenna front end necessitated the integration of multiple RFFE modules on a single chip. This example of 5G beamforming module gives good concepts of 5G front end. We will have small antenna array for MIMO purpose working at mm-wave frequency. Each antenna requires at least one LNA and one PA for receiving and transmitting. And we will have multiple modules for different purpose. As a result, we can imagine that there will be massive RF blocks working at higher frequency in the future.

## 1.3 RF Switches

As mentioned in the previous section, the number of both antenna and FEM will increase for 5G, as shown in Figure 1-3. So as a bridge from chip to outside antenna, the antenna switch modules (ASM) performance will be more and more critical. Their

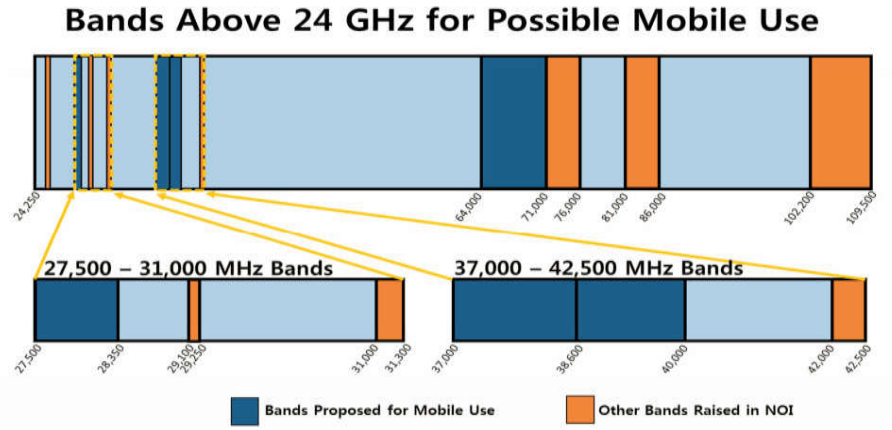



*Figure 1-4 Approved mm-wave bands for 5G research.*

performance must meet not just insertion loss and isolation requirements, but also the requirements of 5G applications, which include faster data throughput, more power, and increased reliability.

An RF switch, as we all know, is a device that allows high-frequency signals to be routed across a transmission line. It's a crucial block in all RFFEs for the usage of antenna switches, which alter the signal path from antenna to various transceivers, band switches, which change the signal from one band to another, and transmitter/receiver (T/Rx) switches, which change the signal direction.

Furthermore, on July 14, 2016, the Federal Communications Commission (FCC) cleared the spectrum for 5G, which included the 28GHz, 38GHz, and 60GHz bands shown in Figure 1-4 [2]–[4]. Larger bandwidth allocations are possible with mm-wave carrier frequencies, which translates to faster data transmission rates. Mm-wave spectrum would allow service providers to dramatically increase channel capacity beyond the 20MHz channels now utilized by 4G consumers. The data capacity of mobile radio channels is

substantially improved by expanding the RF channel bandwidth, while the latency of digital traffic is greatly reduced, thereby enabling much more data.

Achieving 5G criteria for mm-wave RF switch would be difficult. It will be crucial to figure out how to cope with sensitive capacitance and inductance at high frequencies. Furthermore, high frequency mm-wave bands are posing a challenge to switch structure architecture and performance. In the mm-wave spectrum, a normal series-shunt switch can only handle frequencies lower than 10GHz, with inadequate insertion loss, return loss, and isolation. The question of how to achieve the same performance as the 4G standard in mm-wave frequency bands is currently being researched.

# Chapter 2 Introduction to ESD Protection

## 2.1 ESD On-Chip Protection

Electrostatics, often known as static electricity, is a daily phenomenon as old as human history. Greeks discovered static electricity about 600 BC by rubbing amber with a piece of fur and observing the attraction of lightweight items to the amber, as shown in Figure 2-1. Although it is possible that this was not the first observation of static electricity production, it is thought to be the earliest reported experiment. ESD failure occurs when electrostatic charges are transferred between two objects, and the accompanying quick and massive ESD transients can destroy electronic devices.

The severe ESD damage problem, on the other hand, was not regarded seriously until microelectronics technologies began to play a part in our daily lives. In the 1970s, the number of electronic component and system failures due to ESD incidents increased virtually dramatically in the electronics industry. The nature of ESD failure falls into two categories: (1) High power/current which cause thermal damages and (2) High electrical field that induces rupture to dielectric layer. For typical fabrication process, some


*Figure 2-1 Common and natural ESD phenomena in daily life*

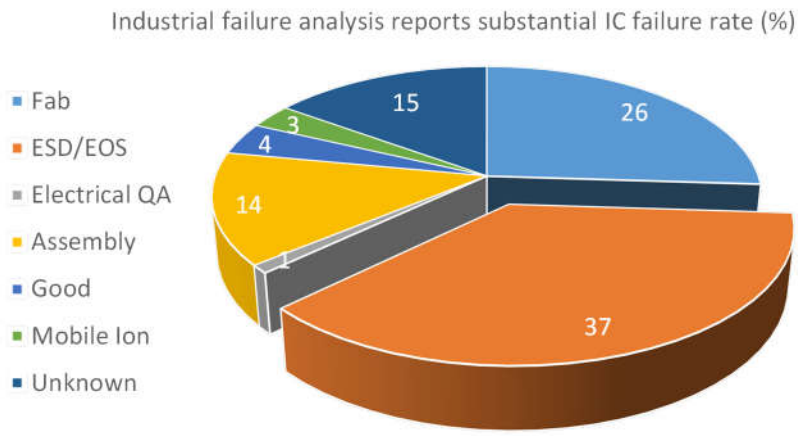



*Figure 2-2 Industrial failure analysis reports substantial IC failure rate*

*Figure 2-3 ESD symbol used in lab.*

electronic devices can be damaged by an ESD transient of as low as 10 volts. Unfortunately, as IC technologies continue to advance into sub-32nm nodes and chip complexity continues to increase, IC become increasingly vulnerable to ESD damages due to thinner metal connections and dielectric layers. It is reported that up to 35% of total IC field are ESD induced, with estimated annual costs running to several billion dollars as shown in Figure 2-2.

Understanding of ESD basics has advanced dramatically during the last three decades. As a result, a broad range of methods have been presented in reality to safeguard electronic

elements and systems from ESD hits at various levels. At the top level, there should be a systematic ESD control program in manufacturing, transportation and application fields to prevent accumulation of electrostatic charge and provide a safe way for discharging. Common practices include well-grounded static protective work areas and platforms; ESD protective floor, shoes, clothing and wrist straps; yelling or use of ESD symbols in work places as shown in Figure 2-3. However, for IC Designers, our goal is using our talent to design on-chip ESD protection structures. The ideal way is to protect IC parts at chip level by designing and integrating ESD protection sub-circuits on chips. Today, ESD diodes, BJT (bipolar junction transistor), NMOS transistor, SCR (silicon-controlled rectifier), etc., are widely used for ESD protection.

The fundamental requirements for on-chip ESD protections are (1) low impedance discharging channel to dissipate transient current and (2) preventing high voltage pulse that might causes rupture. In order to meet these requirements, ESD device design has to fit in

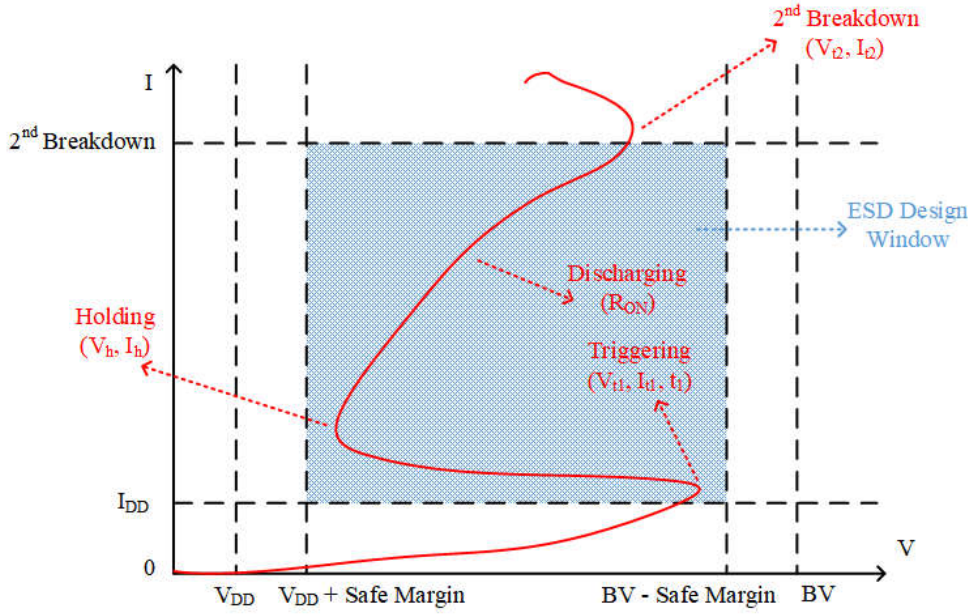



*Figure 2-4 Illustration of ESD design window.*

ESD design window as shown in Figure 2-4. An ESD Design Window is determined by the breakdown voltage (BV) and power supply voltage (VDD) of the core circuit under protection with a sufficient safe margin.

ESD protection necessitates the precise design of ESD-critical parameters, which includes the ESD triggering voltage ($V_{t1}$), the ESD holding voltage ($V_h$), the ESD discharging resistance ($R_{ON}$), and the ESD failure voltage and current ($V_{t2}$, $I_{t2}$). The triggering voltage must be lower than the BV of the core IC ($V_{t1} < BV$) to prevent any ESD damage; meanwhile, to avoid latch-up effect, the holding voltage must be greater than the supply voltage (i.e., $V_h > VDD$).

On-chip ESD designs are facing several challenges: interaction between core circuits and ESD devices, parasitic effects, lack of accurate high-current ESD device models and CAD tools, time-consuming, non-portability and product-specific. What's worse, the BV of IC devices falls considerably when IC technology scales down, but supply voltage drops relatively modestly, which results in a narrower ESD design window for designers. Hence, it's imperative for IC designers to acquire adequate knowledge on ESD protection design and to maintain on the front page of the new development in the field.

## 2.2 ESD Test Models

ESD phenomena have different root causes; accordingly, different ESD protection solutions and ESD protection design characterization methods were developed. Commonly used ESD testing models include human body model (HBM), machine model (MM), charged device model (CDM) and transmission line pulse (TLP) model. Therefore,

various industrial ESD testing standards were developed that have been constantly revised to address the emerging issues of ESD protection for advanced IC technologies [5]. For example, HBM model was initially developed as a military standard [6], which, though, still serving as the foundation model, has been constantly revised over years, leading to several different industrial HBM standards for varying reasons [7]. On the other hand, as IC technologies continue to advance into sub-32nm nodes and chip complexity continues to increase, CDM ESD model is becoming a major ESD failure challenge [8].

### 2.2.1 Human Body Model (HBM)

It is important to first understand the HBM ESD test model, which has been widely used in the field, largely due to its "reliability" in terms of testing repeatability and

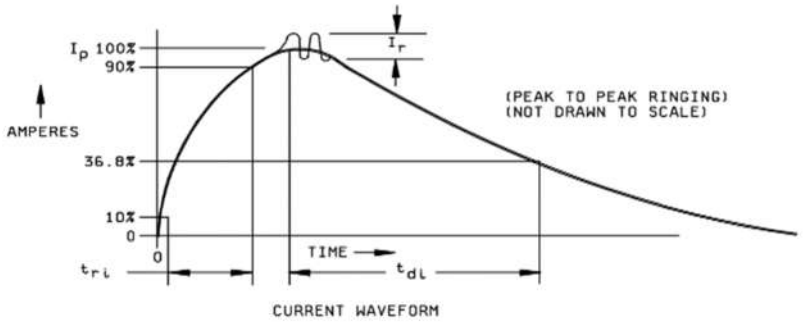



*Figure 2-5 HBM ESD waveform [6].*

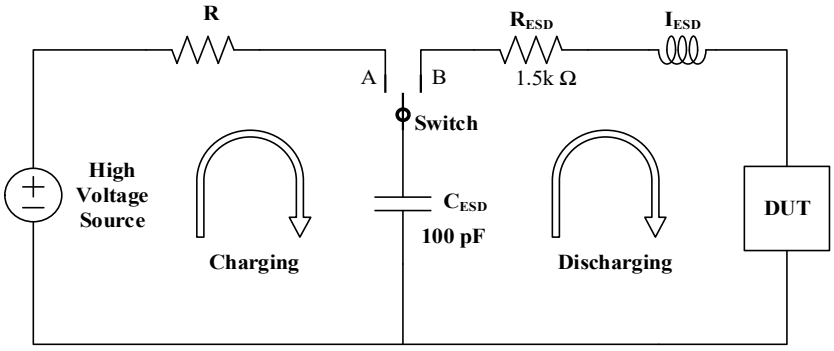



*Figure 2-6 An equivalent circuit model for a standard HBM ESD tester*

reproducibility. Figure 2-5 depicts the original HBM ESD waveform defined in the MIL-STD-883E Standard [6], upon which many later-day industrial HBM ESD test models were developed, such as the newest ANSI/ESDA/JEDEC JS-001-2017 [7]. The key parameters for this HBM ESD waveform include the pulse rising time of $t_r$ (<10ns) and decay time of $t_d$ (150ns ± 20ns). Figure 2-6 illustrates the equivalent circuit model for the HBM ESD model where a human body accumulates static charges by a charging procedure and ESD discharging occurs when a hand touches an IC part, called a device under test (DUT). Consequently, an HBM ESD transient will zap the IC part, resulting in thermal failure and/or dielectric breakdown to the IC. Due to the fact that the HBM ESD phenomenon is well understood and the HBM ESD waveforms are relatively slow, HBM ESD protection designs have been fairly successful today in the industry.

### 2.2.2 Machine Model (MM)

Machine model, on the other hand, represents a charged machine/tool discharging through the DUTs. This event is faster and has a higher current level than HBM. The waveform is also significantly different; the MM waveform is a bi-directional damped oscillation. The test procedure for MM is similar to HBM, but the MM is represented by a capacitor in series with an inductor.

### 2.2.3 Charged Device Model (CDM)

CDM ESD phenomenon is entirely different from HBM and MM models. As illustrated in Figure 2-7, CDM ESD model features a self-charging/discharging procedure that models a real-world ESD phenomenon where an IC (or broadly, an electronic component) is charged by various possible procedures, triboelectrically or by electrostatic

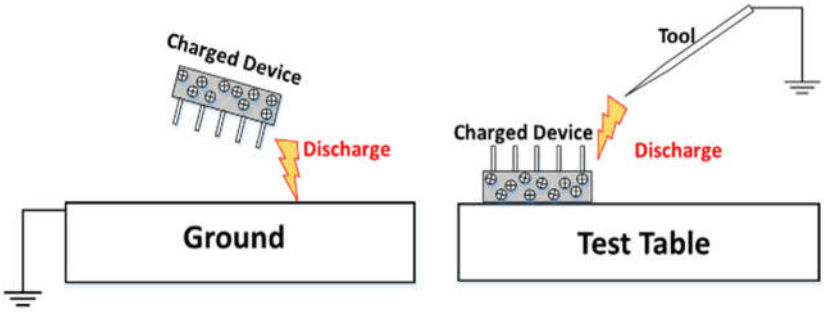



*Figure 2-7 Occasions when CDM ESD happens.*

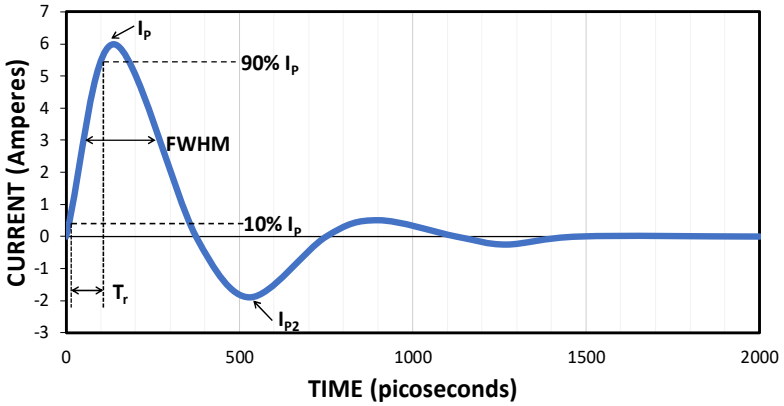



*Figure 2-8 A classic CDM ESD discharging waveform [9].*

field induction, during its life time and accumulates substantial electrostatic charges inside. If the IC is then grounded, the charges stored inside will discharge into the ground. The resulting CDM ESD transient flowing from inside of the IC to the ground may cause thermal or dielectric failures to the IC. Compared to HBM ESD model, the CDM ESD pulse is very short (full width at half maximum, or, FWHM = 250~600ps) and rises extremely fast ($t_r$ <250ps), as depicted in Figure 2-8 [9]. For example, the newest CDM ESD standard (ANSI/ESDA/JEDEC JS-002-2014) describes the device level CDM ESD testing procedures, where the DUT is charged through electrostatic field induction, and the static charges generated and stored inside the DUT will be discharged into the ground when

the pogo pin moves close to and/or touches the DUT later. The CDM ESD tester models the real-world CDM ESD charging and discharging procedures. As the DUT, an IC can be a bare die or a packaged device. The Ground may be a printed circuit board (PCB) on which the IC is mounted.

### 2.2.4 Transmission Line Pulse (TLP)

TLP ESD testing is an alternative to the fail-or-pass HBM zapping method [10]. In a TLP tester, a transmission line is pre-charged and then discharges into DUT. A TLP tester produces a well-defined square waveform with $t_r$ and $t_d$ similar to an HBM ESD waveform as in Figure 2-9. To make the TLP pulses and HBM waveforms equivalent in terms of the transient ESD behaviours and energy involved, a TLP tester typically sets $t_r$~10ns and $t_d$~100ns. TLP testing is generally non-destructive. During TLP testing, a series of square waves (pulse train) is produced to stress the DUT with the pulse height starting very low and increasing gradually. After each TLP pulse, the $I_{leak}$ of DUT will be monitored. When an TLP pulse reaches to certain high level, ESD failure will occur, which typically

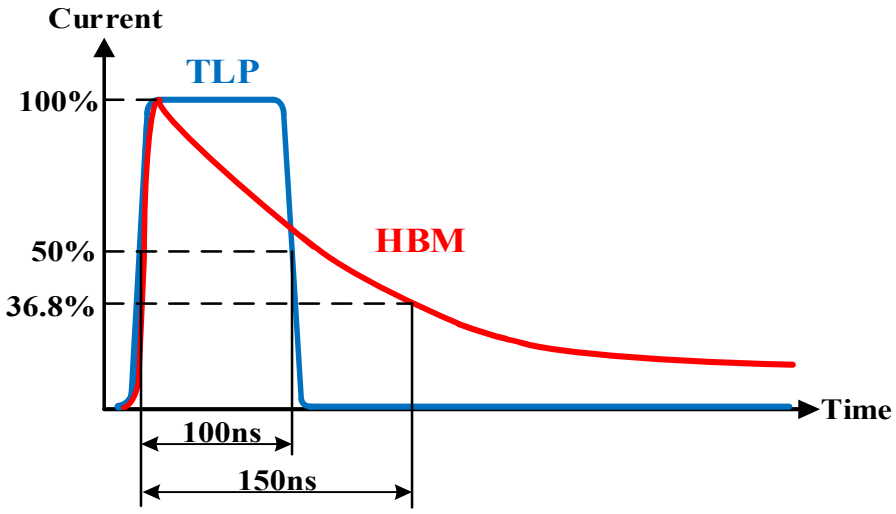



*Figure 2-9 Typical TLP waveform*

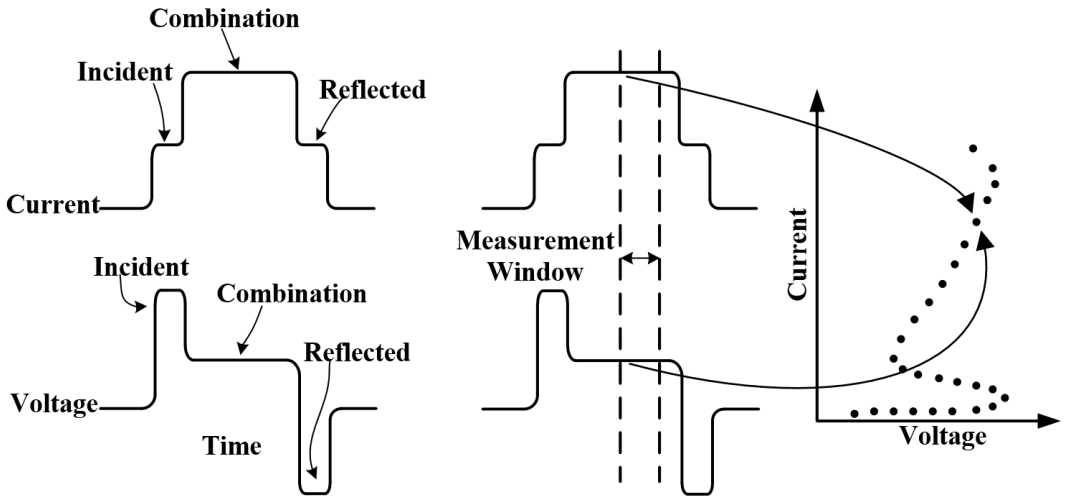



*Figure 2-10 Illustration of TLP testing process*

corresponds to an abrupt increase in the DUT leakage. Figure 2-10 depicts conceptually the whole TLP stressing flow. After each TLP pulse stress, the oscilloscope captures the voltage and current of DUT, hence producing a transient ESD discharging I-V curve for the DUT under ESD stressing. Correspondingly, very fast TLP (VFTLP) is used to study devices under CDM circumstances. To assess CDM performance, the pulse width utilized in a VFTLP testing is generally between 1ns and 3ns, with rise and fall periods on the order of 100ps - 500ps.

## 2.3 ESD Protection Strategies and Devices

To address the ESD discharge risk, each pad on an IC die must be protected by ESD protection structures as illustrated in Figure 2-11, where a possible discharging path from zapped I/O pin to the ground is shown. The current is bypassed by the ESD device and power clamp, without passing through the internal circuit. A classic full-chip ESD protection circuit schematic uses a pad-based ESD protection network on-chip to ensure

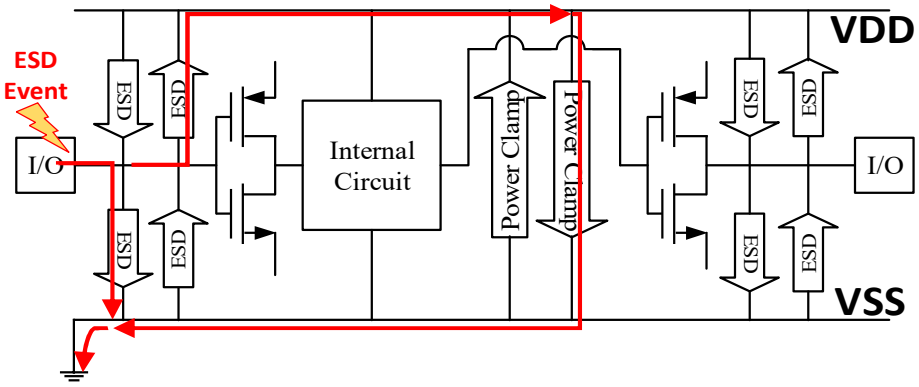



*Figure 2-11 Illustration of IC chip ESD protection strategy*

an ESD discharging path between pads. ESD protection is realized by preventing an ESD pulse from getting inside the IC.

Most commonly used stand-alone ESD structures includes ESD diode, diode string, gate grounded NMOS (GGNMOS), silicon-controlled rectifier (SCR) and diode -triggered SCR (DTSCR). In the following, the structure and ESD characteristics of each type of structures are shown for 45nm RF silicon-on-insulator (SOI) process.

a) ESD Diode

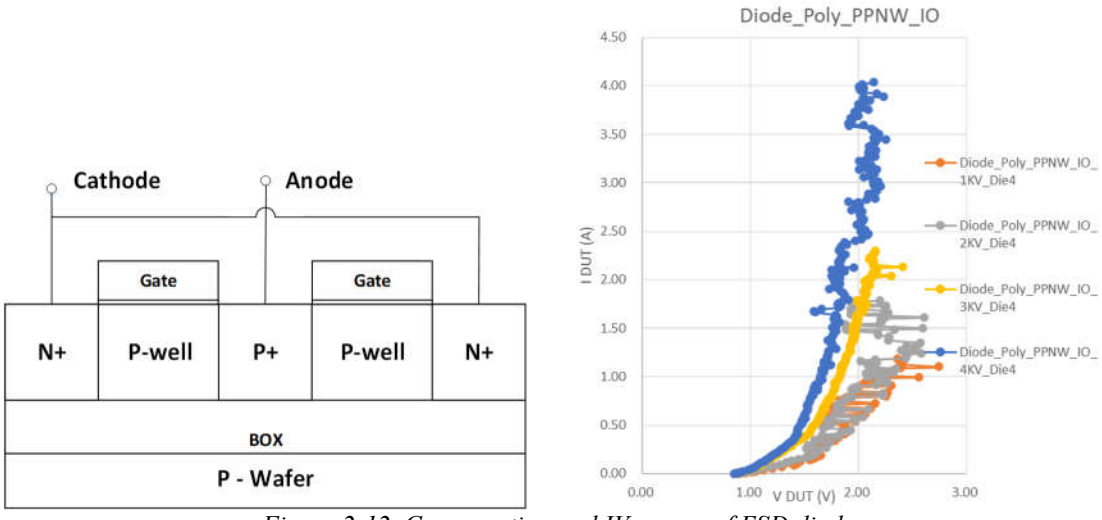



*Figure 2-12 Cross-section and IV curves of ESD diode*

Diode is the most basic ESD protection structure. Figure 2-12 shows the cross-section of ESD diode over a BOX layer and its I-V curves. The ESD current injects from the anode side to cathode. From the I-V curve, we can see the forward turn-on voltage is only around 0.65V for Si. We can use a diode string to address the problem. Double-diode structure is widely used in lots of full-chip bi-directional protection.

b) Diode String

The trigger voltage of a diode string is increased by stacking the diodes, which can fit some high voltage applications. The number of diodes has a big impact on the $V_{t1}$.

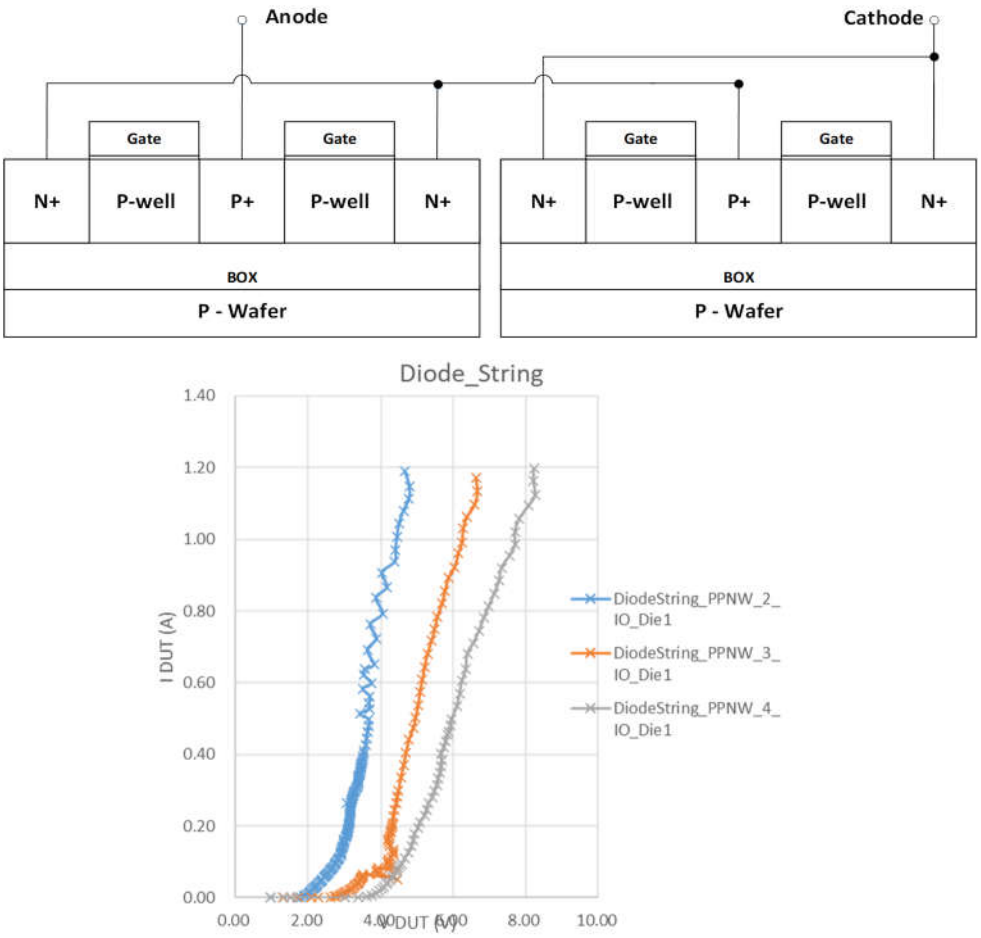



*Figure 2-13 Cross-section and IV curves of ESD diode string*

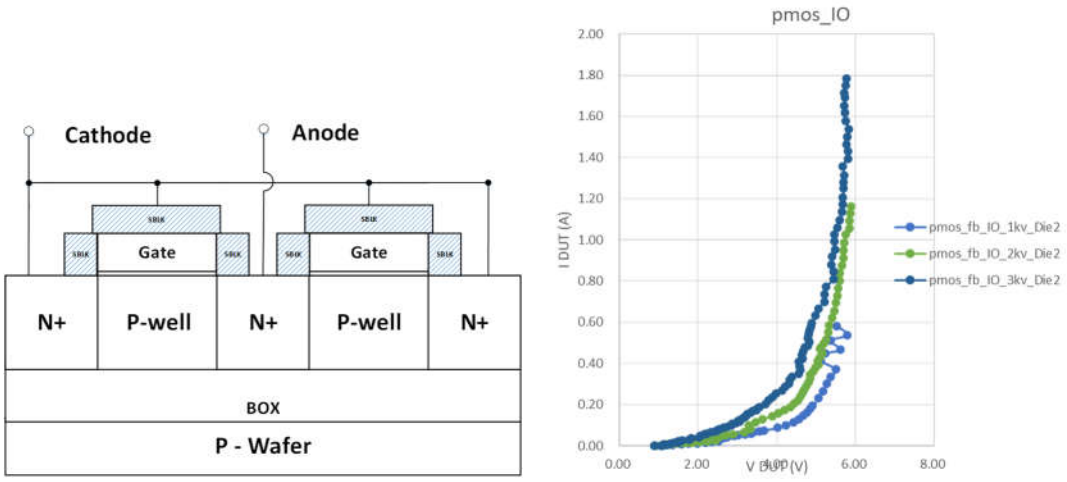



*Figure 2-14 Cross-section and IV curves of ESD gated MOSFETs*

Furthermore, the parasitic capacitor in series reduces the overall capacitance. Figure 2-13 shows the X-section of diode string and the I-V curves of a 2-diode string.

c) GGNMOS

Because of its snapback I-V curve, the GGNMOS structure is often utilized as a high voltage protection. The snapback is induced by the avalanche breakdown of parasitic BJT inside the MOSFETs, which forms a low-impedance channel. $V_{t1}$ is determined by its BV, while the snapback depth and $V_h$ are directly related to impact ionization, base width, BJT current gain and resistance in the path. Figure 2-14 shows the X-section of GGNMOS.

d) SCR

The parasitic SCR (Silicon Controlled Rectifier) consists of a pair of parasitic PNP and NPN transistors. It is an excellent ESD protection device due to its deep snapback characteristic and very area-efficient handling capacity. SCR has a greater trigger voltage than GGNMOS because the N-well/P-well junction must be broken down first before the parasitic BJTs can be triggered. It's presently employed for high frequency IC design with

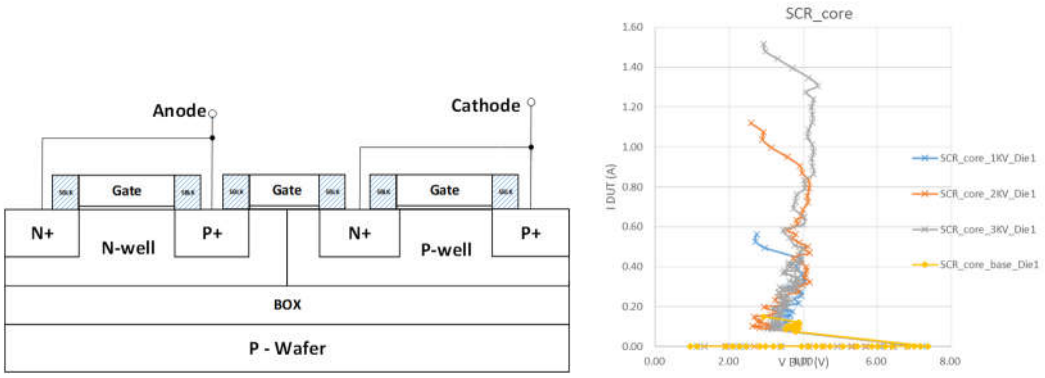



*Figure 2-15 Cross-section and IV curves of SCR*

a lower size and same current handling capacity. Figure 2-15 shows the cross-section of basic PNPN SCR structure.

e) DTSCR

The trigger voltage of SCRs, which is typically around 10V, is too high for use in low-voltage contemporary applications. Using the diode to assist trigger the intrinsic BJT with

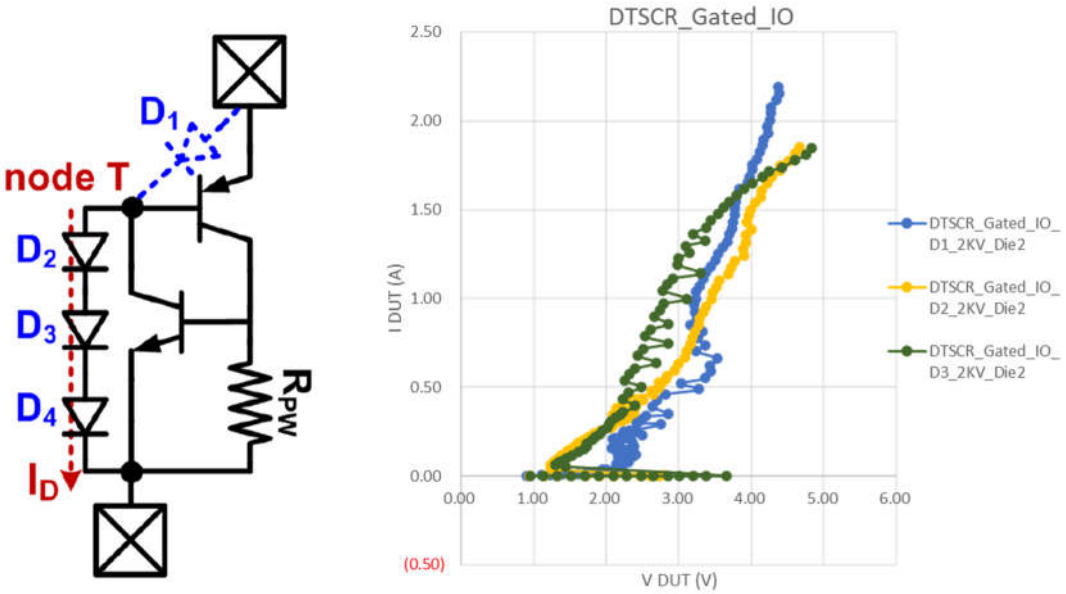



*Figure 2-16 Illustration and IV curves of Diode-string SCR*

parasitic base current is one solution to this problem. The trigger voltage may be controlled using a diode string. The equivalent schematic is showed in Figure 2-16.

# Chapter 3 5G mm-Wave RF Switch Design

This Chapter presents the first co-design analysis of 28GHz, 38GHz and 60GHz broadband single-pole double-throw (SPDT) distributed travelling wave RF switches. The 28GHz switch is implemented in a foundry 22nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology, featuring 9KV full-chip human body model (HBM) electrostatic discharge (ESD) protection, while the 38GHz and 60GHz switches are implemented in a foundry 45nm SOI CMOS technology with ESD protection at all I/O pads.

These ESD-protected millimeter wave (mmWave) SPDT switches are designed for highly reliable above-6GHz 5th-generation (5G) mobile systems. Adverse influences of the inherent ESD-induced parasitic effects are characterized, revealing that the ESD effects can severely affect RF switch performance in mmWave bands. A new ESD-mmWave-switch co-design technique was developed to address this ESD design challenge for mmWave switches, which was validated in Si measurements, e.g., improving the switch insertion loss (IL) by ~4dB for the 28GHz SPDT travelling wave switches fabricated. This design also achieves the highest reported charged device model (CDM) ESD protection of ~1.84A in Si testing. This study proves that ESD-mmWave-switch co-design is critical to RF front-end designs for 5G mobile systems, which typically require robust ESD protection, but are also very sensitive to the inevitable ESD-induced parasitic effects.

## 3.1 28GHz Travelling-Wave Switch in 22nm FDSOI

RF switches are indispensable components to RF front-end modules (FEM) and systems-on-chip (SoC) for mobile systems, particularly for complex 5G wireless applications utilizing ultrawide frequency spectrums, large number of dynamic frequency channels, and time division duplexing (TDD) technology across millimeter-wave frequency bands. Meanwhile, full-chip ESD protection is an emerging challenge for mmWave IC designs. Unfortunately, any on-chip ESD protection structures come with inevitable ESD-induced design overhead effects, e.g., parasitic capacitance ($C_{ESD}$), leakages and noises. Obviously, high-frequency broadband RF ICs are very sensitive to these ESD-induced parasitic effects, which requires careful design considerations [11] [12]. On the other hand, monolithic RF ICs and SoCs for consumer electronics typically require very robust ESD protection, which translates into much more severe ESD-induced parasitic effects that is becoming increasingly unacceptable to high-performance RF ICs for 5G systems [13]-[15]. Substantial R&D efforts have been devoted to RF ESD protection designs, mainly to minimize the ESD-induced parasitic $C_{ESD}$ to reduce the adverse ESD impacts on RF ICs. Consequently, ESD-RFIC co-design becomes an important design technique for modern broadband RF ICs. Recently, [14] reports co-design of ESD protection and SP10T switches for 4G smartphones. [15] discusses co-design of ESD protection and power amplifiers (PA). In mmWave frequency bands, ESD-protected PAs and low noise amplifiers (LNA) were reported, which however did not include ESD co-design considerations [16] [17]. Recently, significant influence of ESD protection on 28/38GHz RF switches for 5G mobiles was reported, showing severe insertion loss

degradation of 5~10dB due to 4KV HBM ESD protection, which indicates that conventional RF ESD design techniques are incapable of handling robust ESD protection for millimeter-wave RF ICs [18]. It is obvious that ESD-RFIC co-design in mmWave frequency bands, particularly for above-6GHz 5G RF ICs, must be studied comprehensively and understood thoroughly, especially considering both HBM and CDM ESD protection for very high frequency and ultrawide bandwidth RF FEM designs. This paper, an extension to a conference brief [19], presents a comprehensive co-design analysis study of a 9KV-ESD-protected 28GHz distributed travelling wave mmWave SPDT RF switch designed and fabricated in a 22nm FD-SOI technology for 5G systems, aiming to provide a practical ESD-mmWave-switch co-design technique for above-6GHz 5G wireless systems.

### 3.1.1 28GHz MmWave Travelling-Wave Switch Design

Conventional series-shunt transistor circuit topology offers excellent switch performance for sub-6GHz RF switches. Unfortunately, in the above-6GHz frequency bands, e.g., 28/38GHz, the specifications of series-shunt transistor RF switches suffer severe performance degradation [18]. Several designs were reported to address the mmWave switch design challenges using various design methods, for instance, using a unique SOI substrate featuring very high resistivity and a trap rich layer to alleviate the coupling effect [20], utilizing a special coupling line based artificial resonator structure for sub-terahertz operations [21] [22], and resorting to various MEMS structures and emerging materials [23]-[25]. Alternatively, travelling-wave-based RF switch topology becomes very attractive to ultrawide band millimeter-wave switches [26]-[29].

This work adopts a unique distributed travelling wave switch schematic to design a mmWave SPDT RF switch for 28GHz 5G mobile systems. Figure 3-1 depicts the travelling wave mmWave SPDT switch implemented in a foundry 22nm fully-depleted SOI technology. This three-stage distributed travelling wave SPDT structure consists of inductive transmission lines (TL) and the corresponding controlling transistors. This distributed travelling wave SPDT circuit does not use quarter-wave transmission lines in order to reduce the switch die area for high-frequency operations of 28GHz and to avoid using long trace that will increase insertion loss (IL) along the lossy transmission lines. The series transistors (M1, M2) provide extra control of the SPDT switching status and improve its isolation (Iso). For power handling capability consideration, thick-oxide long-channel nMOSFETs are used for both series and shunt transistors (M1-M8). In this design, the on-state resistance (Ron) and off-state capacitance (Coff) of the unit-width MOSFET were extracted first, which allows to optimize the MOSFET widths jointly with the

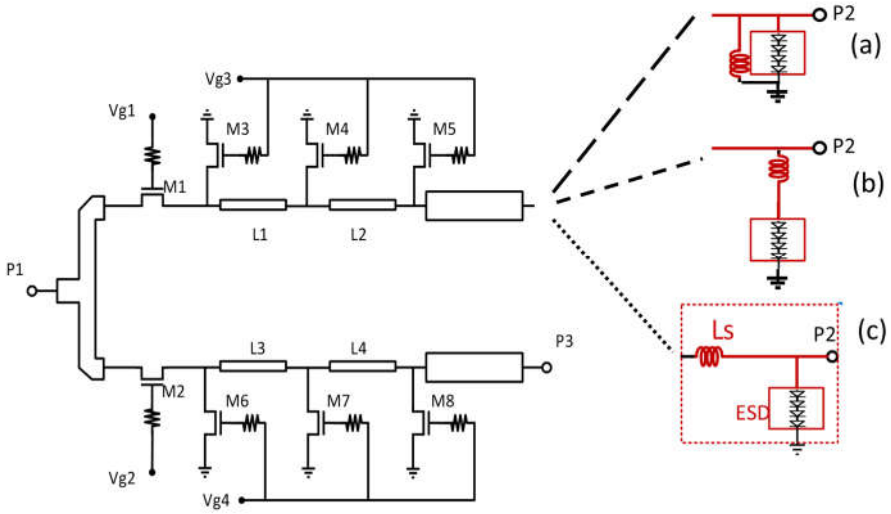



*Figure 3-1 Schematic of the ESD-protected distributed travelling-wave mm-wave SPDT switch featuring: (a) narrow-band LC shunt resonator ESD protection, (b) LC series resonator ESD protection with a center frequency far away from the operating frequency, and (c) L-shape ESD protection.*

transmission lines for careful design trade-off. The inductive transmission line was designed to have a characteristic impedance of 70Ω. Generally, a complex massive-MIMO architecture in mmWave 5G systems requires many transmitting/receiving (TRx) switches. Accordingly, this design selects short transmission line segments with smaller inductance to save the SPDT switch die area. Correspondingly, the shunt MOSFETs are designed with smaller sizes to meet impedance requirements. Consequently, the controlling MOSFET sizes are designed as following: channel length L = 100nm for M1-M8, channel width W = 115μm for M1 and M2, and W = 20.3μm for M3-M8, respectively. A 10KΩ resistor is added to the gate to provide AC isolation.

### 3.1.2 Full-Chip ESD Protection Design

This 28GHz mm-wave SPDT switch was designed with full-chip 9KV HBM ESD protection. Figure 3-2 shows the ESD protection utilizing a four-diode-string ESD protection structure and optimized by TCAD ESD simulation to prevent switch power dropout due to ESD-induced leakage. The gated diodes feature floating gates. The diode-string ESD protection structure is implemented in the "hybrid" region in the FDSOI technology, where the buried oxide isolator layer (BOX) in the SOI substrate was

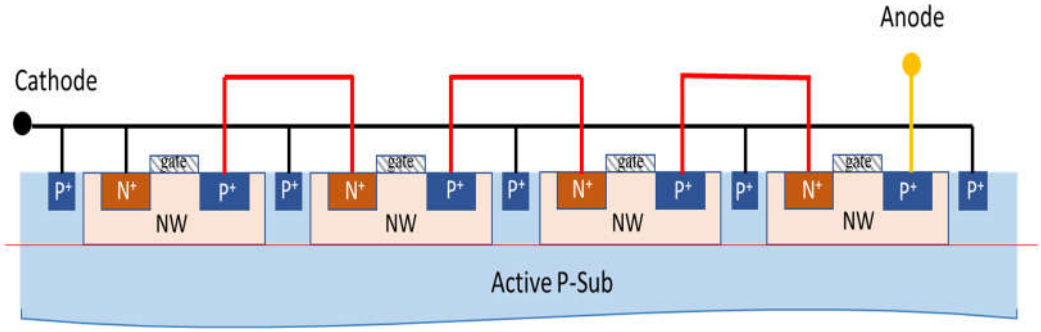



*Figure 3-2 A cross-section view for the gated four-diode-string ESD protection structure designed in this work.*

purposely removed in the ESD device layout area to allow direct ESD current discharging through the bulk region, which improves the ESD discharging conduction and heat dissipation via the substrate, and therefore greatly enhances its ESD current handling capability as predicted by TCAD ESD simulation. Figure 3-3 shows the ESD protection diodes produced by TCAD simulation using a representative process, with and without the SOI BOX. Standard HBM zapping waveforms, generated by an HBM ESD equivalent circuit, are used as ESD zapping stimuli for transient TCAD ESD simulation. Figs. 3-4 and 3-5 depict the simulated transient HBM ESD discharging characteristics for the two ESD protection structure splits (i.e., with and without BOX), respectively, revealing the transient ESD discharging current flows and lattice temperature distribution. It is observed that the ESD protection structure with SOI BOX suffers from higher local overheating compared to its non-BOX counterpart. This is obviously attributed to more severe ESD discharging current crowding and poorer heat dissipation inside the active ESD structure with SOI BOX isolation. TCAD ESD simulation for exemplar ESD diode strings show that the ESD structure with a SOI BOX fails at 1.13KV ($I_{t2}$ ~ 0.75A), while the ESD diode without a SOI BOX passes a much higher level of 2.37KV ($I_{t2}$ ~ 1.56A). Commonly used ESD protection diodes utilize either gated diode or shallow trench isolation (STI) diode structure. Compared to a STI ESD diode, a gated ESD diode is generally more ESD-robust due to its short and straight ESD discharging conduction path, which results in lower ESD discharging resistance and faster ESD triggering speed [30] [31]. Therefore, this design

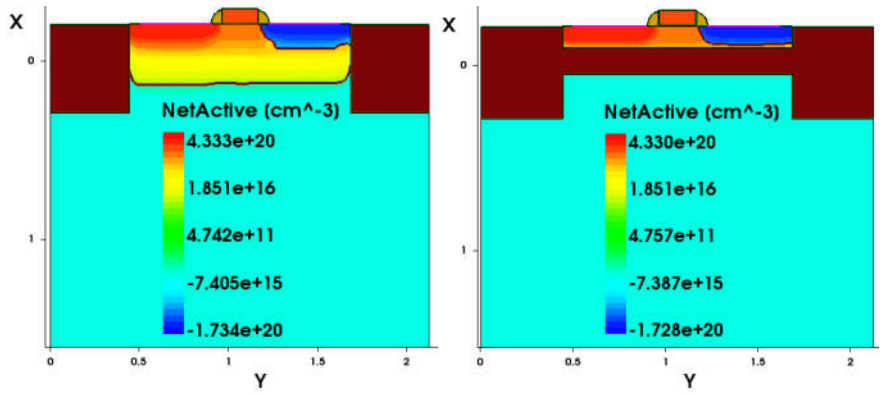



*Figure 3-3 TCAD ESD simulation reveals transient ESD discharging characteristics for the two diode-string ESD protection structures with (Right) and without (Left) a SOI BOX: ESD diode cross-sections。*

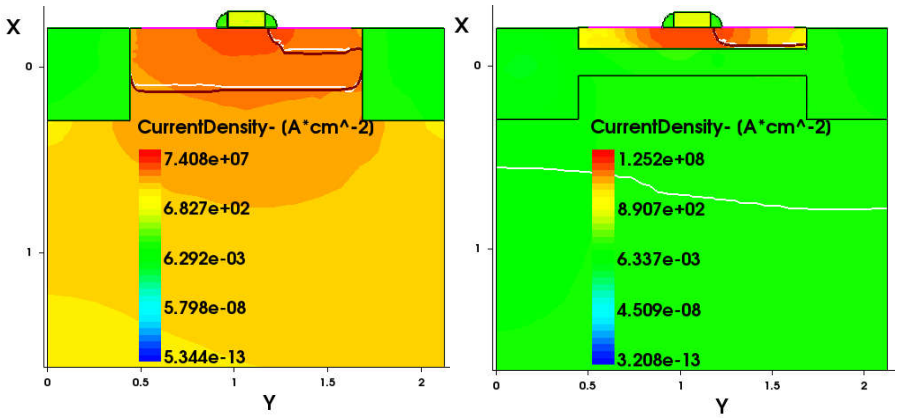



*Figure 3-4 TCAD ESD simulation reveals transient ESD discharging characteristics for the two diode-string ESD protection structures with (Right) and without (Left) a SOI BOX: ESD discharging current flows.*

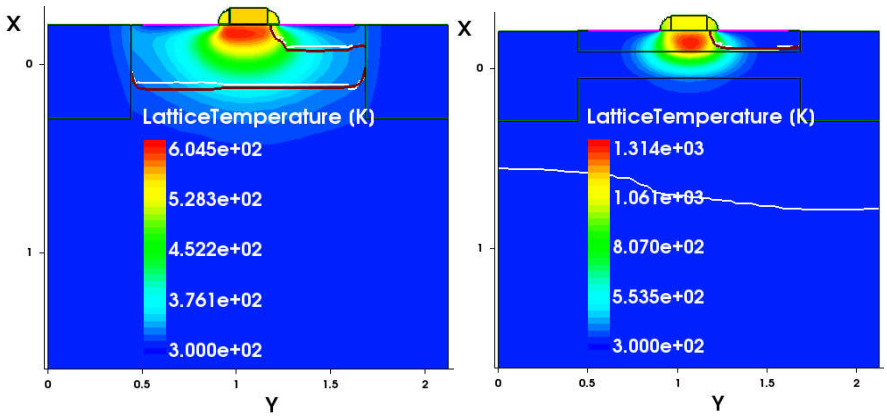



*Figure 3-5 TCAD ESD simulation reveals transient ESD discharging characteristics for the two diode-string ESD protection structures with (Right) and without (Left) a SOI BOX: transient lattice temperature.*

utilizes gated four-diode-string ESD protection structure as shown in Figure 3-2. The gated

ESD diode structures were optimized for a gate length of 150nm and a diode width of 500µm for 9KV HBM ESD robustness. The four-diode-string ESD protection structure is designed to feature an ESD triggering voltage of $V_{t1}$~2V and to handle an output power of 19dBm for 5G mobile systems. The ESD-induced parasitic capacitance of the gated four-diode-string is estimated to be $C_{ESD}$~50fF, which is used for ESD-SPDT co-design to be discussed later. Chip-level transient HBM ESD simulation was carried out to evaluate the ESD protection of the 28GHz mmWave SPDT circuit. Figure 3-6 depicts the simulated ESD voltage clamping behaviors at the SPDT output ports under exemplar 2KV HBM zapping, which reveals that, without ESD protection, the SPDT suffers high transient voltage stressing of up to 13V at the output node that causes breakdown ESD failure to MOSFET M5 due to very low breakdown voltage of 22nm FDSOI CMOS (BV ~ 8.7V); while the output voltage is effectively clamped to a low level of 4V in the SPDT with ESD protection.

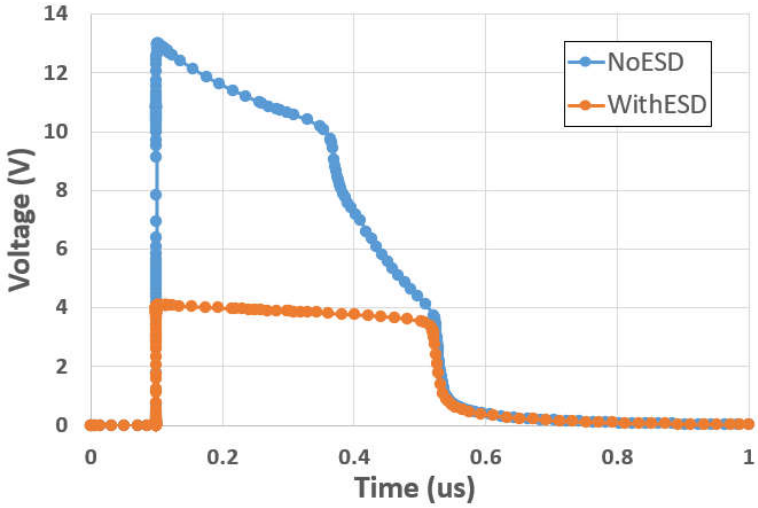



*Figure 3-6 Chip-level transient ESD discharging simulation shows transient voltage at the output nodes of the SPDT design splits without and with ESD protection under 2KV HBM ESD zapping. Without ESD protection, ESD failure occurs to M5 due to high transient voltage of ~13V. With ESD protection, the SPDT is safe due to a low clamping voltage of ~4V.*

### 3.1.3 ESD-mmWave-Switch Co-Design

The conventional shunt L-C resonator ESD protection scheme, shown in Figure 3-1(a), is not suitable for broadband RF ICs because the high-Q resonator makes this ESD protection scheme intrinsically be narrow band in nature. Alternatively, [32] reports a series L-C ESD protection topology for mmWave RF ICs as shown in Figure 3-1(b), which creates a notch at low frequency and shows less impact to ultra-high frequency circuits. [33] discusses a similar design using transmission lines for the inductors for ultra-high frequency ESD protection. However, this series L-C ESD protection method is not suitable for CDM ESD protection because the series inductor adds significant extra delay in ESD triggering under CDM ESD zapping, hence easily resulting in early CDM ESD failure.

To address this ESD design problem, we devised a novel L-shaped ESD protection topology to simultaneously address both RF impedance mismatching and CDM ESD discharging challenges in mmWave broadband designs as depicted in Figure 3-1(c), which

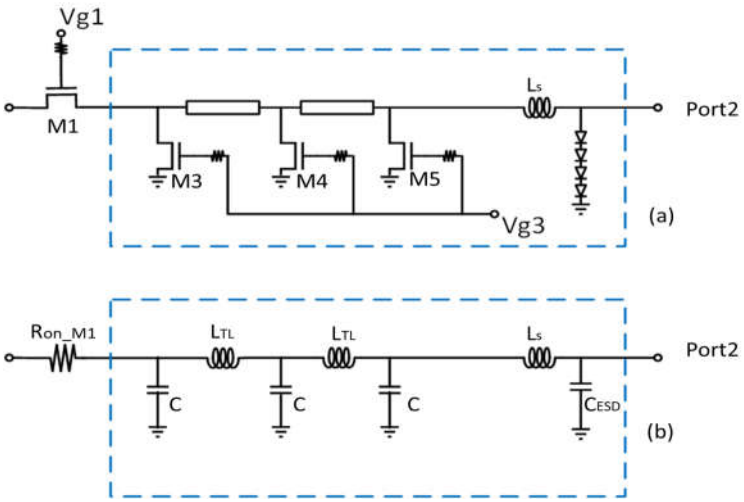



*Figure 3-7 Equivalent circuit model for the traveling wave switch with L-shaped ESD protection structure for co-design consideration: (a) schematic of a switch branch circuit with four-diode-string ESD protection, and (b) equivalent circuit model with the ESD protection represented by CESD.*

provides the desired broadband ESD response without causing circuit performance degradation to mmWave switches. Conceptually, the L-shape ESD matching network consists of the $L_S$ and ESD-induced parasitic capacitance, $C_{ESD}$. Under CDM ESD stressing, the ESD protection structure forms a low-$R_{on}$ CDM ESD discharging path. This L-shaped ESD protection scheme can instantaneously reduce the harmful high-frequency CDM ESD pulse magnitude and substantially delay the CDM ESD pulse propagation into the internal circuit, hence, providing efficient CDM ESD protection in addition to robust HBM ESD protection. Figure 3-7 depicts the equivalent circuit of the L-shape ESD protection network used for ESD-mmWave-switch co-design analysis. In On-state, the travelling wave switch is equivalent to a distributed transmission line network formed by inductors and capacitors [34]. Ignoring the resistive loss, the characteristic impedance of the transmission line network can be expressed,

$$Z_0 = \sqrt{\frac{L_{TL}}{(C_{TL}+C_{FET})}}. \qquad (1)$$

By carefully choosing an appropriate inductor value through co-design considerations to set

$$\sqrt{\frac{L_{TL}}{(C_{TL}+C_{FET})}} = \sqrt{\frac{L_S}{C_{ESD}}}, \qquad (2)$$

the L-shape ESD protection block can be absorbed as an extra stage of the equivalent transmission line circuit for the ESD-protected travelling wave switch circuit branch. By careful design, the ESD-included characteristic impedance can be precisely set to match the source and load impedance, which leads to a lower VSWR circle, hence less RF signal power loss from mismatch, and eliminates the inherent ESD-induced impacts to the On-

state insertion loss. When the travelling wave switch is in Off-state, the turned-off series transistor (M1) and turned-on shunt transistor (M3) will block most RF power. Therefore, the L-shape ESD protection structure will have minimum impact on the isolation. In this design, the $L_S$ is calculated to be 125pH per Eq. (2). Including the parasitic effects of the backend metal lines and device structures, the inductor was optimized by HFSS simulation to have an inductance of 152pH with Q~25 at 28GHz.

### 3.1.4 Characterization and Discussion

Fabricated in a foundry 22nm FDSOI CMOS technology, the ESD-protected distributed travelling-wave 28GHz SPDT switches were characterized for both RF and ESD protection performance. Figure 3-8 shows a die photo for the fabricated 28GHz SPDT mmWave switch optimized by ESD-mmWave co-design. Figure 3-9 and 3-10 depict the key SPDT switch Specs, insertion loss and isolation respectively, measured using an RF probe station and Agilent-E8363B PNA Network Analyzer. It is observed that, from 5GHz

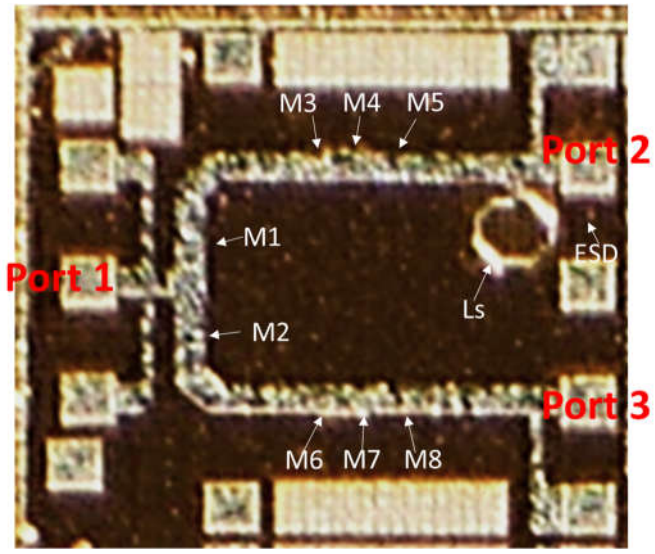



*Figure 3-8 Die photo for the ESD-protected 28GHz distributed mm-wave travelling wave SPDT switch fabricated in a foundry 22nm FDSOI CMOS technology.*

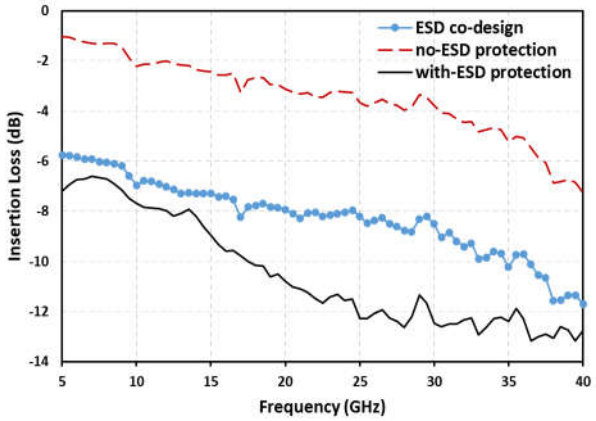



*Figure 3-9 Measured IL for the SPDT switch splits: without ESD protection, with ESD protection (but no co-design optimization), and with ESD protection and co-design optimization.*

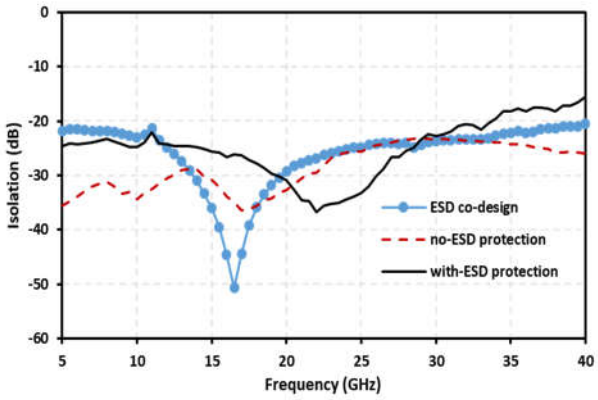



*Figure 3-10 Measured Iso for the SPDT switch splits: without ESD protection, with ESD protection (but no co-design optimization), and with ESD protection and co-design optimization.*

to 20GHz, the SPDT switch without ESD protection structure achieves IL of 1.0dB ~ 3.1dB and Iso better than 30dB. Across the 5G n257 and n258 bands required, IL is better than 3.9dB and Iso is better than 23dB. Table-I compares this work with relative designs reported, showing comparable broadband switch performance in the mmWave bands. Figure 3-9 clearly shows the negative impacts of ESD-induced $C_{ESD}$ on mmWave SPDT performance, i.e., a substantial degradation in IL, as much as an increase of ~12.6dB at 28GHz. By ESD-mmWave co-design, the ESD-induced IL degradation was successfully

recovered by ~4dB across the whole 5-40GHz bandwidth measured. It is worth noting that, though the ESD-switch co-design concept is straightforward, the ESD co-design was not yet able to completely recover all the ESD-induced SPDT performance degradation as expected in this design for the following reasons: Ideally, accurate measurement of Si ESD structures before ESD-switch co-design is needed in order to achieve better results in practice designs, which requires two design iterations, or such ESD testing data must be available to designers when designing an ESD-protected switch. Unfortunately, since this

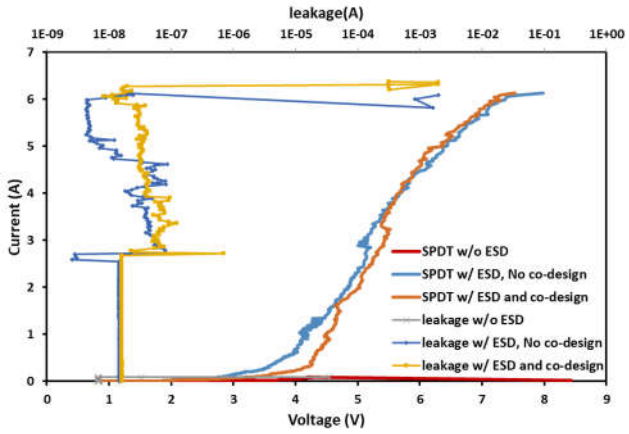



*Figure 3-11 Measured HBM ESD protection performance of the mm-wave SPDT switches splits by TLP ESD testing shows that the best reported full-chip HBM ESD protection robustness of at least 9KV in mm-wave bands (linear scale).*

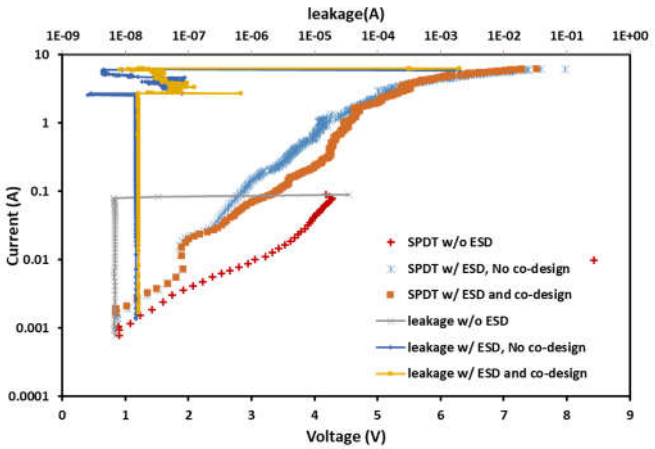



*Figure 3-12 Zoom-in for the measured HBM ESD protection performance of the mm-wave SPDT switches reveals the ESD triggering details in log scale.*

was a design under an MPW tapeout program with limited foundry supports and allowed one Si fabrication opportunity only, this travelling wave switch design could not be carried out following the ideal ESD-mmWave-switch co-design procedures. In addition, the EM simulation parameters, such as materials permittivity, could not be accurately calibrated due to lack of foundry technology data on HFSS simulation models. Nevertheless, this work clearly demonstrates the severe performance impacts of ESD protection on mmWave travelling wave switch circuits and confirms that ESD-mmWave-switch co-design is important, useful and practical to design optimization of RF switches in mmWave bands.

Next, on-chip ESD protection characterization was conducted for both HBM ESD stressing by transient transmission line pulsing (TLP) ESD testing (Barth 4002 TLP+) and CDM ESD stressing by very-fast transmission line pulsing (VFTLP) ESD testing (Barth 4012 VFTLP+). Figure 3-11 presents exemplar HBM ESD protection measurement result at P2-to-GND port by TLP ESD stressing for the three SDPT design splits, i.e., without ESD protection, with ESD protection (but no co-design), and with ESD protection and co-design optimization. The TLP testing pulse waveform conditions were set as: rising time $t_r$ = 10ns and duration $t_d$ = 100ns. The measured transient ESD discharging I-V curves shown in Figure 3-11 and their zoom-in details depicted in Figure 3-12 clearly show that the non-ESD-protected SPDT switch failed at very low ESD current level of $I_{t2}$ ~ 0.1A (i.e., HBM ESD robustness of ~150V only). As a comparison, the L-shaped 4-diode-string ESD protection structure can protect the SPDT switch up to $I_{t2}$ ~ 6A (i.e., at least 9KV for HBM ESD protection), with ESD co-design optimization included. To our best knowledge, this is the highest full-chip ESD protection level reported for mmWave RF switches by

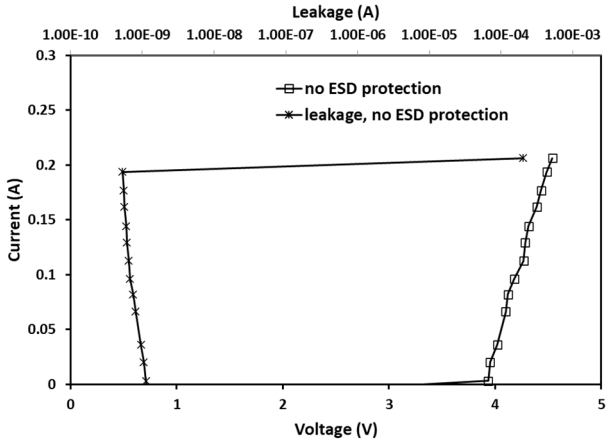



*Figure 3-13 Measured CDM ESD protection performance of a sample mm-wave SPDT switch without ESD protection by VFTLP ESD testing shows that the SDPT can be easily damaged by CDM ESD pulses at a low level of ~0.2A only.*

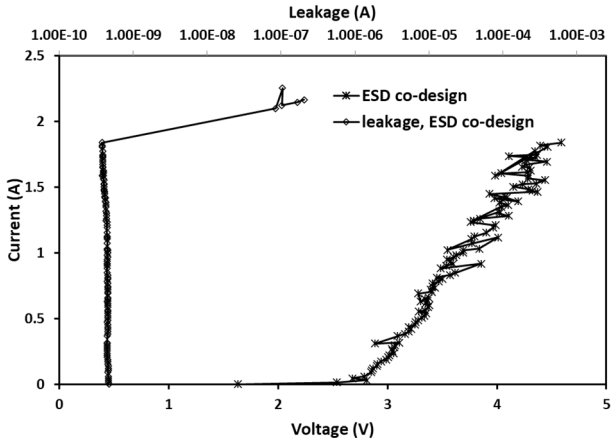



*Figure 3-14 VFTLP-measured CDM ESD protection performance of a sample mm-wave SPDT switch with on-chip ESD protection and optimized by ESD-switch co-design shows that the L-shaped ESD protection structure provides very robust CDM ESD protection up to 1.84A.*

measurement. Figure 3-13 and Figure 3-14 present the measured CDM ESD discharging I-V curves by VFTLP testing for the SPDT switches without ESD protection and with ESD protection including ESD-SPDT co-design. The VFTLP testing pulse waveforms were set at $t_r$ = 100ps and $t_d$ = 1ns. Figure 3-13 shows that, without on-chip ESD protection, the SPDT switch failed at very low CDM ESD stressing level, i.e., merely ~0.2A. In comparison, Figure 3-14 shows that using our novel L-shaped ESD protection structure, the 28GHz SPDT switch passed a very high CDM ESD protection level of ~1.84A. To our

| Refs. | Processes | Freq. (GHz) | Topologies | IL (dB) | Iso (dB) | ESD Protection |
|---|---|---|---|---|---|---|
| [18] | 45nm SOI CMOS | 26-30 | Series-shunt with feed forward capacitor | <10 (8.8)[a] | >15 (19.6)[#] | 4KV |
| [27] | 180nm CMOS | DC-50 | Travelling wave | <6* (5.0)[#] | >26* (27)[#] | No |
| [29] | 65nm triple-well CMOS | 20-80 | Travelling wave | <5* (3.0)[#] | >15* (19)[#] | No |
| [35] | 180nm SOI CMOS | DC-40 | Series-shunt with matching inductor | <5* (2.3)[#] | >17* (17)[#] | No |
| **This work** | **22nm FDSOI** | **5-30** | **Travelling wave without ESD protection** | **<3.9 (3.9)[#]** | **>23 (24)[#]** | **No** |
| **This work** | **22nm FDSOI** | **5-30** | **Travelling wave - ESD protection co-design** | **<8.8 (8.8)[#]** | **>22 (25)[#]** | **9KV** |

*Table 3-1 Comparison of relevant mmwave switch performance*

best knowledge, this is the best-reported measured CDM ESD protection result for travelling wave RF switches in mmWave bands.

This section reports the first comprehensive ESD-mmWave-switch co-design analysis of mmWave 28GHz travelling wave SPDT switches designed and fabricated in foundry 22nm FDSOI CMOS technology for 5G n257 and n258 bands. The measured IL and Iso are comparable to the state-of-the-art mmWave switches around 28GHz. ESD testing shows that the novel L-shape ESD protection design can absorb the ESD parasitic capacitance into the travelling wave structure and substantially improve the performance of broadband RF switches in mmWave bands. The ESD-co-designed switch achieves the highest reported HBM ESD robustness of 9KV and the best-reported CDM ESD protection level of 1.84A in Si measurements. It is observed that the inevitable ESD-induced parasitic effects can severely affect RF switch performance in mmWave bands, which can be substantially recovered by careful ESD-switch co-design. This study proves that ESD-mmWave-switch co-design is important and useful in optimizing mmWave broadband

switch designs for 5G mobile systems, which typically requires robust ESD protection, but is also very sensitive to any inherent ESD-induced parasitic effects.

## 3.2 38/60GHz Travelling Wave Switch in 45nm RFSOI

The 45nm SOI CMOS technology from GlobalFoundries provides great power and performance for a wide variety of applications [36]. Significant transistor performance, including reduced junction capacitance and power improvement over traditional bulk technology, are obtained with their 6th generation of cutting-edge SOI technology. There are various advantages to eliminating junction, such as the lack of N or P wells. There is no route for the leakage current in the largely exhausted floating body gadget. Furthermore, by removing the N-well, the N-well proximity effect is removed from the FET models, and the shallow STI lowers stress effects. Last but not least, because the floating body voltage in SOI is a function of the supplied S/D voltages and previous operation, it may be employed to minimize switching time and voltage drop across pass gate and source follower circuits. When compared to a bulk technology, SOI has various advantages, including a lower S/D capacitance, which enhances the device's power performance. And because bulk analog circuits share the same substrate, there will be interference coupling across the substrate. This can be reduced by using region substrate connections and high-resistance silicon, but in SOI, the isolation given by the BOX and shallow trench isolation (STI) nearly eliminates this coupling.

Due to its high-speed response, outstanding power capability, decreased capacitance, and great isolation approaches, this cutting-edge SOI technology has a potential use for ultra-high frequency, low cross-talk RFIC design, particularly for RF switch.

### 3.2.1 38/60GHz MmWave Travelling-Wave Switch Design

This triangle in Figure 3-15 can give a basic concept of switch performance. At the top is the topology, how many threw you need? The most widely used is single pole double threw (SPDT). One for receiver and the other one for transmitter. Second is the function or we can say purpose of the switch. It can be used to switch the transmitter or receiver. It can also be used to switch different bands. At the bottom are the specs for each switch. The insertion loss indicates the ratio of output power and input power when the switch is ON. The isolation indicates the ratio when the switch is OFF. On another word, we need the switch has less loss when it's ON and block everything when it's OFF. So ideal switch should have 0 insertion loss (IL) and infinite isolation (ISO). Another important spec is

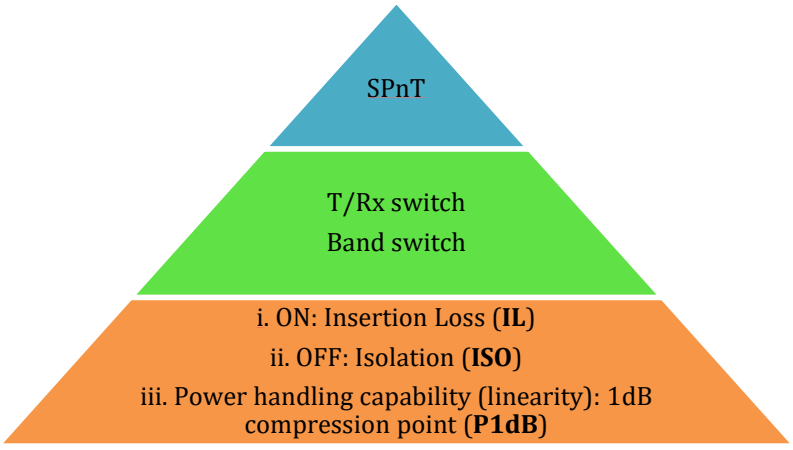



*Figure 3-15 Design consideration for RF switches performance*

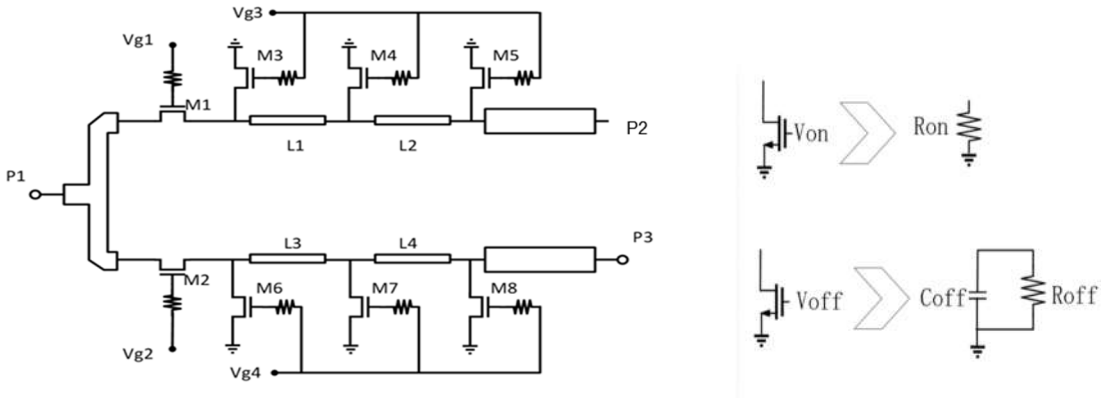



*Figure 3-16 schematic of an SPDT traveling-wave switch and equivalent model for MOSFETs*

1dB compression point (aka P1dB). It indicates the linearity. If you don't want to loss 1dB power, you have to limit your input power smaller than P1dB.

The traveling-wave idea has been used to create millimeter-wave passive FET switches with bandwidths of dc–28 GHz. The schematic of an SPDT traveling-wave switch is shown in Figure 3-16. For the shunt MOSFETs, the source terminals are linked to ground, whereas the drain terminals are connected to transmission lines.

When the shunt MOSFETSs are turned off, it behaves like a Coff. The Coff and TL form an artificial transmission line (TL). And the equivalent characteristic impedance of the artificial TL will match to 50ohm if the device periphery and transmission lines are properly selected and, thus, the input signal can easily flow to output. While the MOSFETs are off states, the single pole single threw (SPST) traveling-wave switch can be reduced as Figure 3-17.

When the shunt MOSFETs are turned on, it is just a low Ron and bypass the signal to the ground and isolate it from the output. The series MOSFETs are applied to further improve the isolation when the switch is OFF.

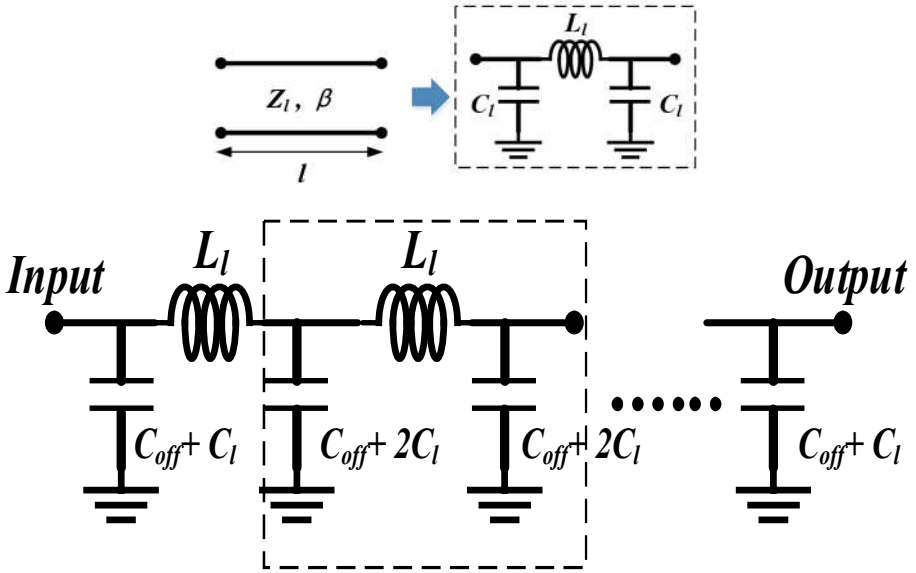



*Figure 3-17 Equivalent circuit for STSP switch when the shunt MOSFETs are in OFF state.*

For optimal performance, many parameters need to be optimized during the design process: size (width) of the MOSFETs, characteristic impedance of TL, length of TL and number of shunt MOSFETs. The design flow is illustrated in Figure 3-18:

1. In order to analyze the traveling-wave switch performance, we use simplified model of Ron and Coff for the MOSFETs. With the PDK provided by the foundry, simulation is performed to determine the relation of Ron and Coff with device width (Wg), as shown in Figure 3-19. By using these equations, the Ron and Coff can be written as functions of device width.
2. By using the equivalent pi model of TL and calculating ABCD matrix, we can easily represent IL and ISO of the SPST travelling-wave switch as functions of design parameters, such as length of the transmission line, device size, and number of transistors, which are discussed above. Then we use MATLAB to find the

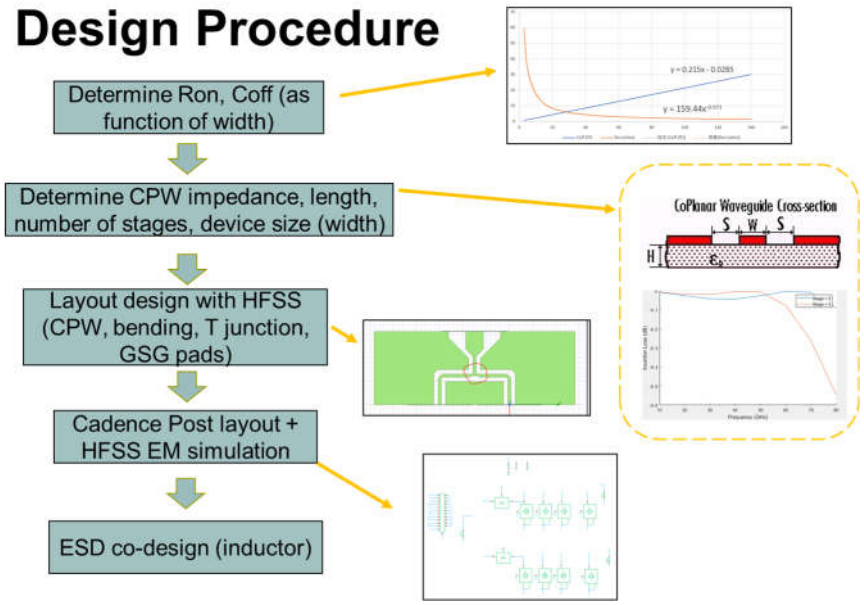



*Figure 3-18 Design procedure of the traveling-wave switch*

optimized value of these parameters, as shown in Figure 3-20. These values can be start point of our design.

3. Next, with the MOSFETs size from the last step, we go to Cadence post-layout simulation to find the actual Coff and Ron with metal connection, then optimize the metal connection and layout for smallest Coff and Ron. After this, we can go back to MATLAB with actually optimized Coff and Ron, to find the correspondingly optimized TL length, TL characteristic impedance and number of shunt MOSFETs.
4. Design the transmission line in HFSS to match the optimized values of TL length, TL characteristic impedance and number of shunt MOSFETs from the last step. The design also includes the GSG pads, T junction and bend for minimal signal loss at discontinuities, as shown in Figure 3-21 and 3-22. The line characteristic

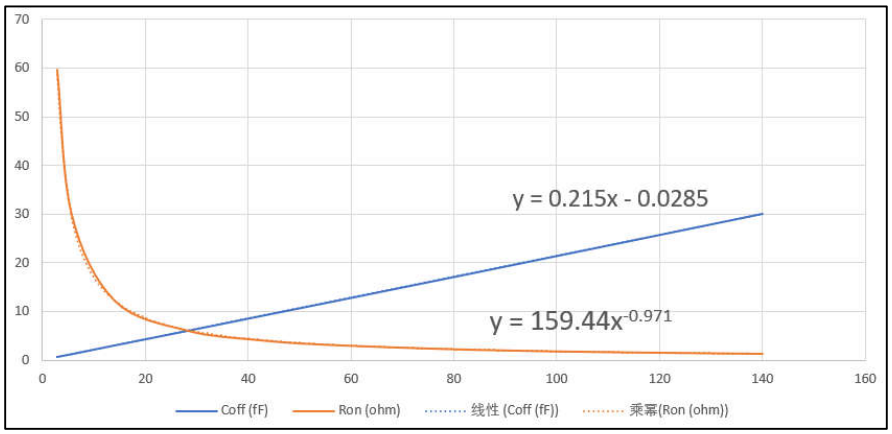



*Figure 3-19 Relation of Ron and Coff to device width (Wg)*

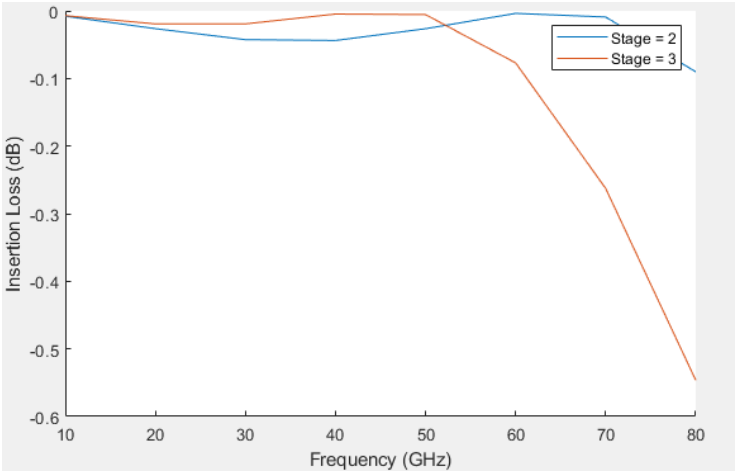



*Figure 3-20 Modeling the SPST switch in MATLAB to find the optimized design parameters*

impedance is changed by the discontinuity, and the bend adds shunt capacitance if it is not compensated. The other issue with bends is that the effective length of the transmission line becomes shorter than the centerline length, causing significantly greater harm to the intended performance of a finely tuned circuit. Then with the extracted S parameter from HFSS and post-layout shunt MOSFETs, we can now find the optimized series MOFETs size (for best IL and ISO in Cadence simulation).

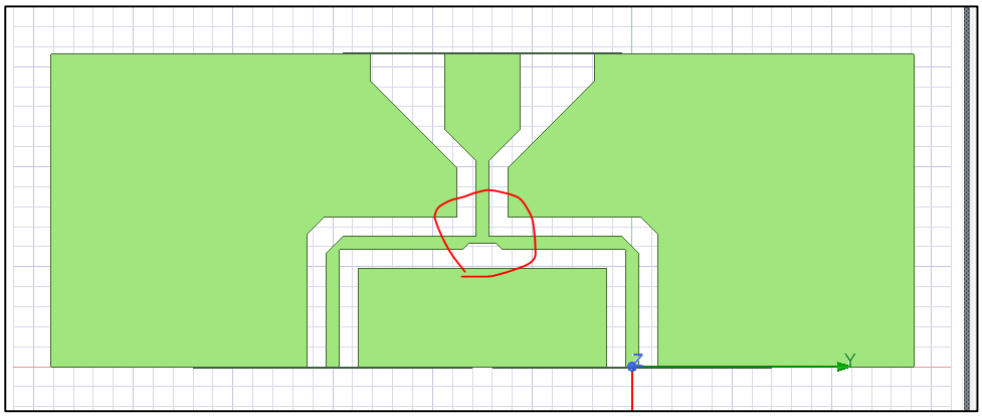


*Figure 3-21 GSG pad, T junction and bend design in HFSS*

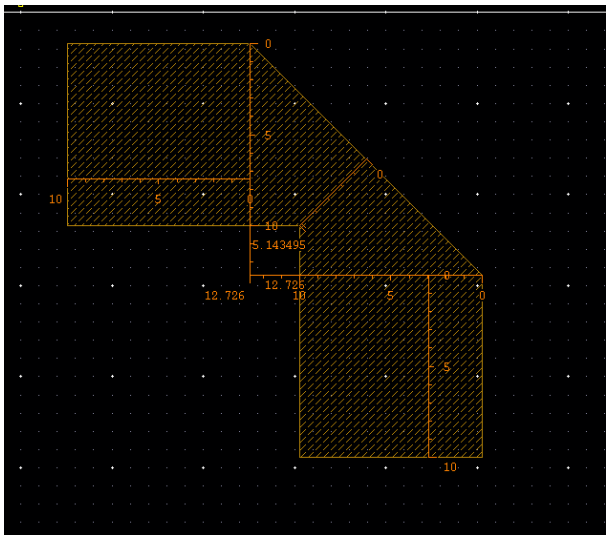



*Figure 3-22 Compensations at the bend of the transmission line*

5. Now, final layout and devices size determined, we can combine the S parameter from HFSS with the post-layout simulation in cadence to get the final IL and ISO performance as shown in Figure 3-23. After that, we can add ESD protections to all the pads with impedance matching. And the final layout is shown in Figure 3-24.

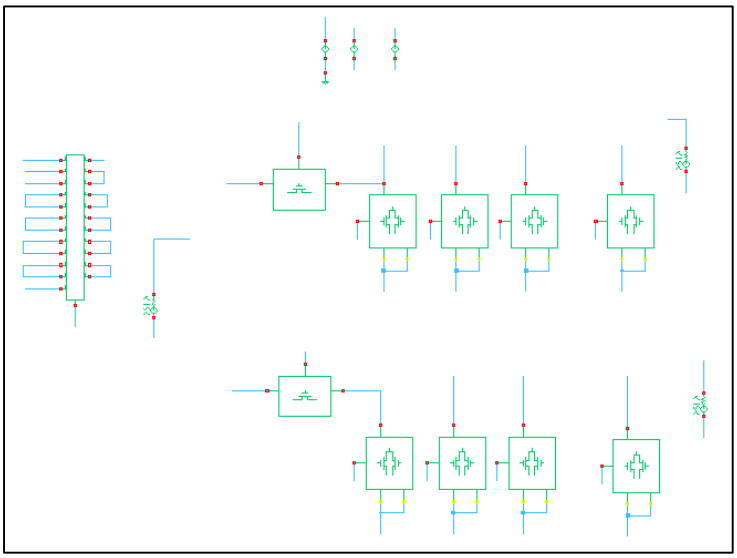


*Figure 3-24 Simulation deck in Cadence for post layout combined with HFSS EM simulation.*

There are several problems we need to address during the design process. First, for the state of art, people only use a single MOSFET in the travelling-wave switch [37]. However, for 4/5G technology, the power can be > 24dBm (5V voltage swing). At the advanced

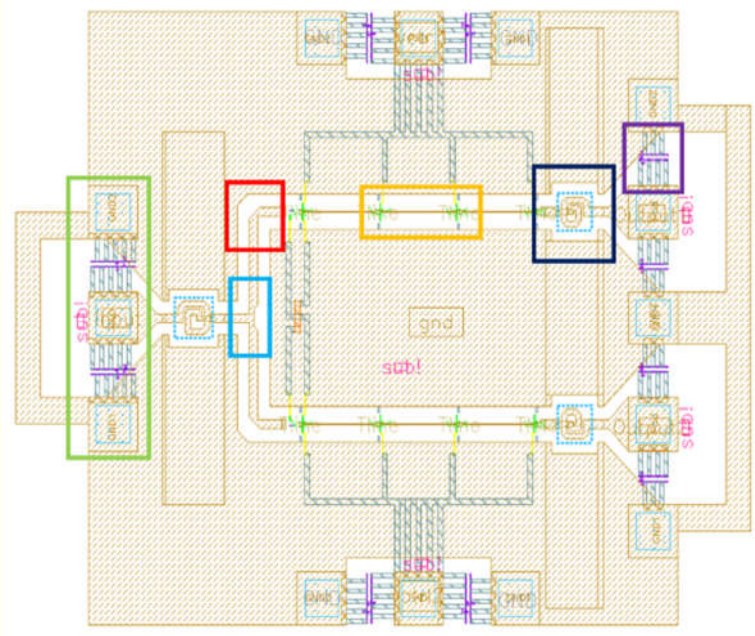


*Figure 3-23 Final layout for the 38Ghz traveling-wave switch*

technology node such as 45nm, a single MOSFETs cannot handle such high power. So, we came up with the stacked MOSFETS as shown in Figure 3-25, which can withstand twice the voltage swing as before (6dB higher).

Second, coplanar waveguide (CPW) is used as the transmission line, which is shown in Figure 3-26. It is formed from a conductor separated from a pair of ground planes, all on the same plane, atop a dielectric medium. In the ideal case, the thickness of the dielectric is infinite; in practice, it is thick enough so that EM fields die out before they get out of the substrate.

Microstrip and CPW are both proven high-frequency circuit methodologies and both can provide excellent performance at microwave frequencies and beyond. They offer

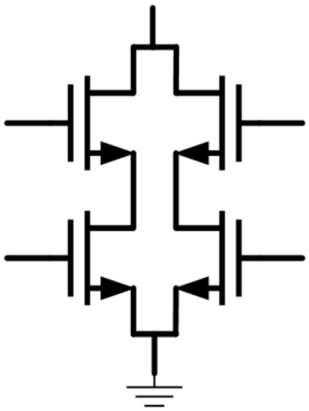


*Figure 3-25 Stacked MOSFETs for higher voltage swing.*

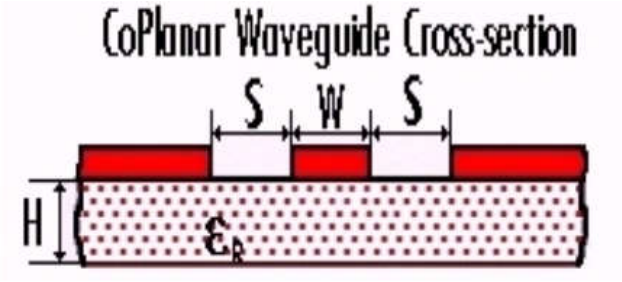



*Figure 3-26 Illustration for the coplanar waveguide*

different approaches to laying out the circuit. In general, at microwave frequencies, microstrip circuits will suffer less loss than CPW circuits, especially due to manufacturing variations. But when an application calls for higher, millimeter-wave frequencies, CPW circuits will suffer less dispersion and radiation losses than microstrip circuits. Also at millimeter-wave frequencies, CPW circuit approaches provide better bandwidth than microstrip circuits. In addition, when necessary, mode suppression can be achieved more readily with CPW circuits than with microstrip circuit approaches.

Both technologies operate by means of a dominant quasi-transverse-electromagnetic (quasi-TEM) propagation mode. CPW circuits, with their enhanced ground structures, are somewhat more mechanically complex to fabricate. But CPW circuits also feature low dispersion compared to microstrip circuits, with lower radiation loss than microstrip circuits especially at frequencies extending into the millimeter-wave range. With their

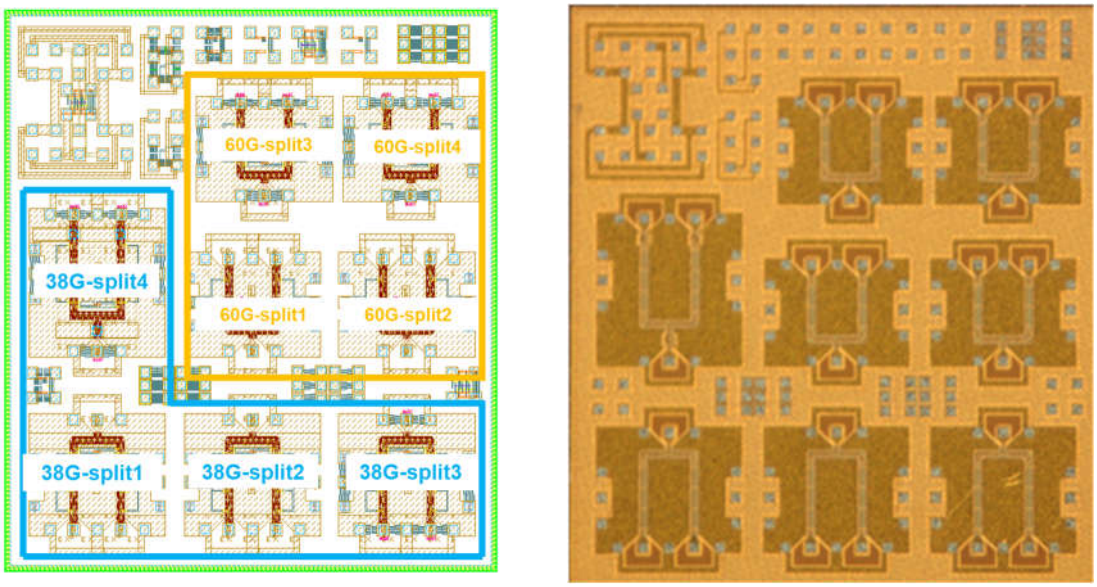



*Figure 3-27 The overall floor plan and die photo for the 38Ghz and 60Ghz RF switches.*

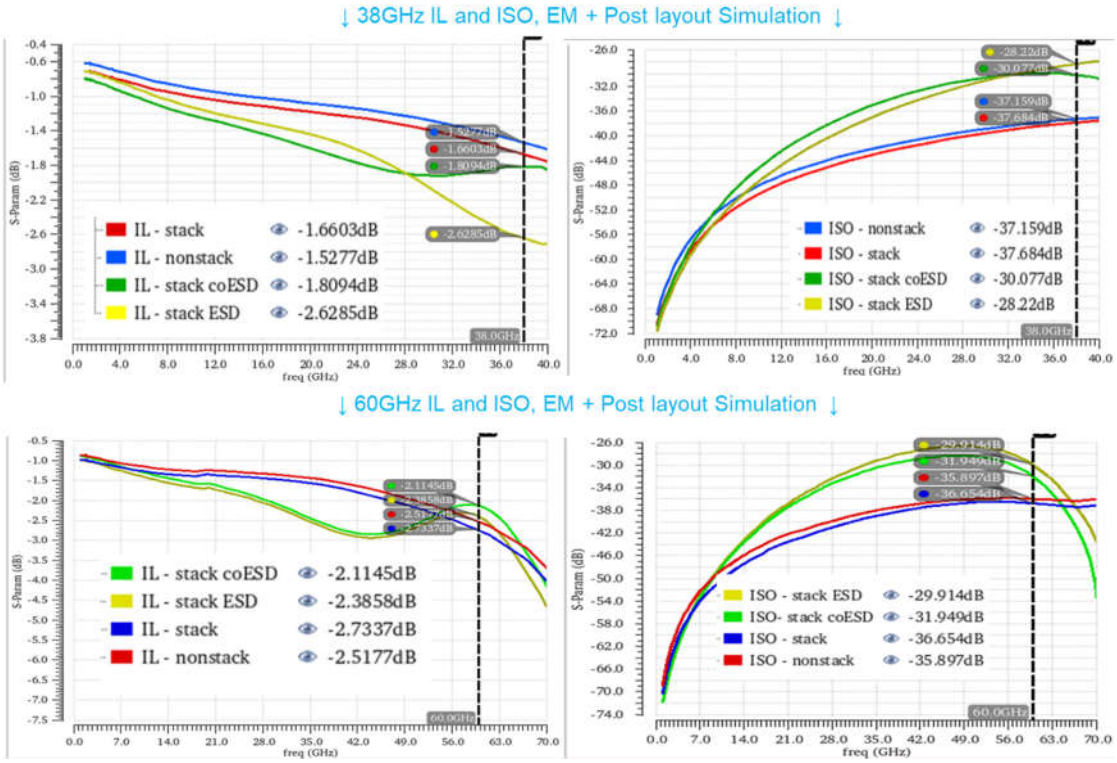



*Figure 3-28 IL and ISO of the 38Ghz and 60Ghz RF switches.*

enhanced ground structures, CPW circuits are capable of wider effective bandwidths than microstrip circuits and wider impedance ranges than microstrip circuits.

### 3.2.2 Results and Discussion

The overall floorplan is shown here in Figure 3-27. Each RF switch has 4 splits: Split1 has single MOSFET; Split 2 uses stacked MOSFETs; Split 3 is added with ESD protection; Split 4 includes impedance matching with ESD codesign.

The simulation results are shown below in Figure 3-28. Here for the 4 splits of 38Ghz and 60Ghz switch, the test equipment is broken down and the results are from Post layout Simulation combined with HFSS EM simulation.

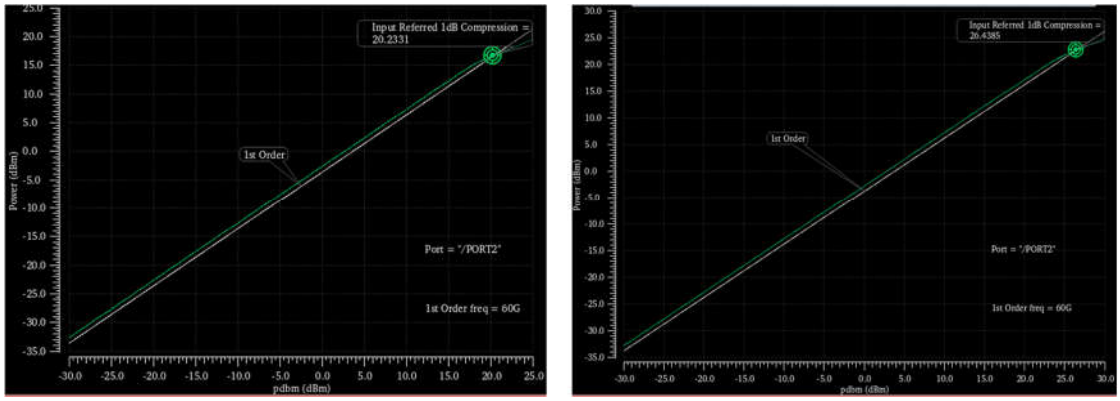



*Figure 3-29 P1dB of the 38Ghz and 60Ghz RF switches.*

| Frequency | Parameters | non-stack | stacked | stack+ESD | stack+coESD |
|---|---|---|---|---|---|
| *38GHz* | IL (dB) | **1.52** | 1.66 | 2.62 | 1.81 |
| | ISO (dB) | 37.2 | **37.7** | 28.2 | 30.1 |
| | P1dB (dBm) | 21.5 | **27.2** | **27.2** | 27.2 |
| | ESD protection | Non | Non | 2KV | 2KV |
| *60GHz* | IL (dB) | 2.51 | 2.73 | 2.38 | **2.11** |
| | ISO (dB) | 35.9 | **36.7** | 29.9 | **31.9** |
| | P1dB (dBm) | 20.2 | **26.4** | **26.4** | **26.4** |
| | ESD protection | Non | Non | 2KV | **2KV** |

*Table 3-2 Summary table for the RF switches performance.*

Here are the highlights. The task is to design RF switches working at 38 and 60Ghz. The traveling wave-topology is used. For the 38GHz one, IL~1.5dB, ISO > 37dB. As for the 60GHz one, IL~2.5dB, ISO > 35dB. Meanwhile, it shows high Power linearity with 1dB point at 27dBm. The P1dB of stacked MOSFETs splits are 6dB higher than those of non-stack MOSFETSs, as shown in Figure 3-29. Because the stacked MOSFETs can withstand twice the voltage swing, which translates into 6dB higher power. Also, all I/O pads are ESD-protected without much degradation of RF performance.

Table 3-2 here summarizes the results for the 4 splits. In conclusion, the 38GHz and 60GHz SP2T mm-wave switches are successfully designed using travelling wave topology.

For the 4th splits with stacked MOSFETs and co-ESD design, it has achieved good performance of IL, ISO, P1dB with ESD protection.

# Chapter 4 Advanced CDM ESD Protection Design

## 4.1 Pad-Based CDM ESD Protection Methods Are Faulty

As previously discussed in the chapter 2, ESD failure is regarded as the most challenging reliability problem for ICs, which requires on-chip ESD protection for all ICs [5, 13, 30, 38-39]. ESD phenomena are classified according to the origins, leading to various industrial ESD test standards, such as HBM, CDM and IEC [6, 7, 9]. These industrial ESD testing standards have been constantly evolving to accommodate the new understanding of ESD phenomena, especially for advanced IC technologies. Nowadays, as IC technology continues to scale down and chip complexity rapidly increases, CDM ESD protection emerges as a major IC reliability design challenge, particularly at sub-28nm nodes and for FinFET CMOS. Recognizing that a CDM ESD event is extremely fast compared to an HBM ESD event, the main research efforts in CDM ESD protection designs have been devoted to making CDM ESD devices faster. In practical designs, the classic pad-based HBM ESD protection approaches have been commonly used for CDM ESD protection. On the other hand, CDM ESD protection remains a black magic full of uncertainties today, being a huge headache to IC designers [8, 41, 42]. The commonly asked questions about CDM ESD protection are: Why are CDM ESD test results often not repeatable, reproducible and unreliable? Why does an IC still fail in CDM zapping in field although the chip passed the CDM test in production? Why does CDM ESD failure seem to be so random in field? In short, the fundamental question to ask is that, does the popular pad-based on-chip CDM ESD protection approach really work? Chapter 4.1 provides a thorough analysis that concludes that the classic pad-based CDM ESD protection methods

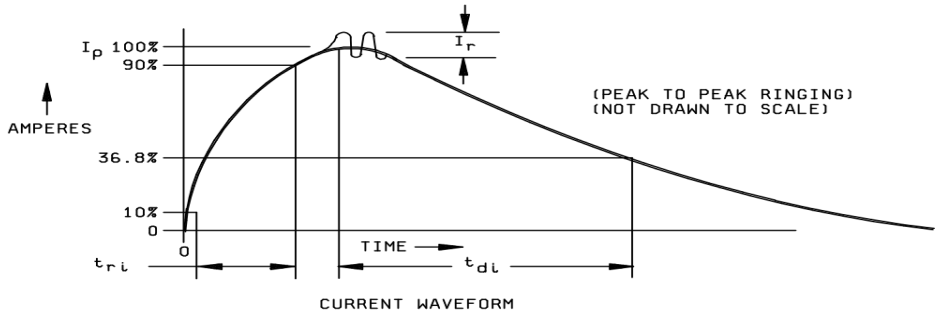



*Figure 4-1 The HBM ESD waveform defined in [7].*

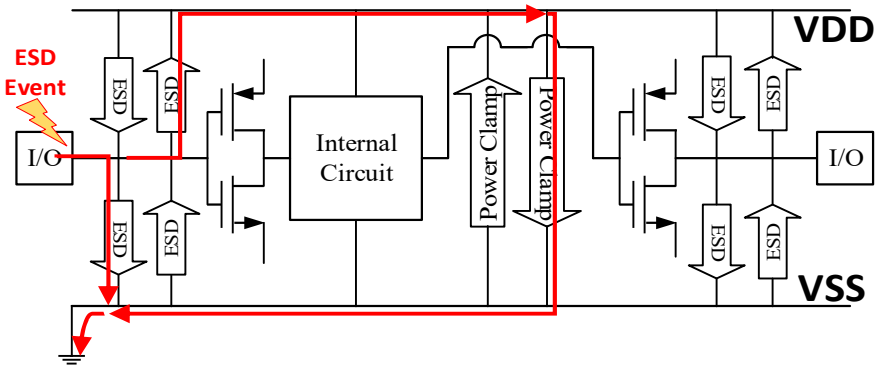



*Figure 4-2 Classic pad-based full-chip ESD protection scheme relies on the ESD devices at pads to form low-R paths to discharge the incoming HBM ESD transients, i.e., blocking external alien charges from getting into the IC core. It works for any "from-external-to-internal" ESD events.*

are fundamentally faulty and points out the misconception with the existing pad-based CDM ESD protection methodology [43].

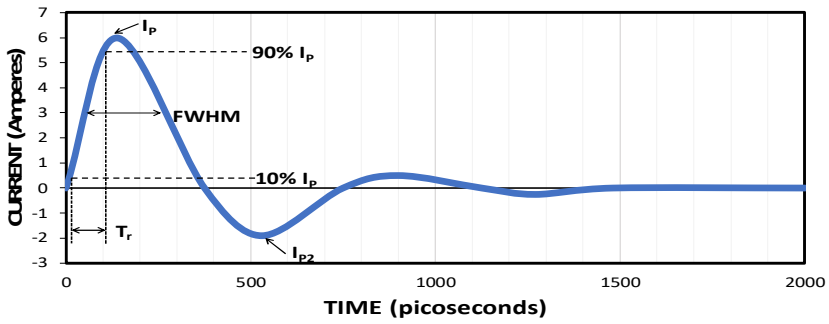
### 4.1.1 HBM ESD Protection: From-External-to-Internal

HBM ESD is an "external-oriented" ESD phenomenon where electrostatic charges accumulated inside a human body will discharge into the IC core through an IC pad when touching the IC [5]. Figure 4-1 depicts the transient HBM waveform, defined by the original MIL-STD-883E Standard, which is used to zap IC pads, and the HBM pulse flowing into the IC core may cause HBM ESD failures [6]. The ANSI/ESDA/JEDEC JS-001-2017 Standard provides details to build an HBM ESD tester to faithfully model the

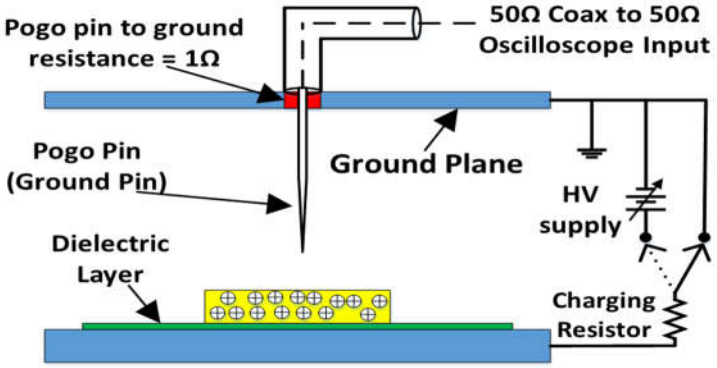
real-world HBM ESD events [7]. The key parameters for an HBM pulse are waveform rising time (tr~10ns) and decay time (td~150ns). Figure 4-2 depicts the classic pad-based on-chip HBM ESD protection method where ESD protection devices are placed at the IC pads (I/O, VDD, VSS, etc.), which will be turned on at ESD stressing to form low-R conduction paths to bypass the incoming HBM transients into ground. In principle, pad-based HBM ESD protection works in a way that the incoming alien charges from a human body are blocked by the ESD devices at the pads from getting into the IC core, hence, realizing ESD protection. HBM ESD protection requires careful design of the ESD-critical parameters including triggering voltage (Vt1), triggering time (t1) and discharging resistance (RON) [5]. In theory, the pad-based ESD protection method is a "from-External-to-Internal" ESD protection method where the ESD devices at pads serve as the "guard" at the "gate" (i.e., pad) to defend against the "external-oriented" HBM ESD events, which, however, does not apply to the "internal-oriented" CDM ESD events.

### 4.1.2 CDM ESD Protection: From-Internal-to-External

CDM ESD is an "internal-oriented" event in nature that is completely different from the "external-oriented" HBM event. CDM ESD is a self-charging/discharging ESD phenomenon where, in real world, an IC may be charged by various possible mechanisms, triboelectrically or field induction, during their lifetime. The induced electrostatic charges are stored inside the IC in a random and distributed way. When the IC is grounded, the static charges stored inside will discharge into the ground. The resulting strong and ultrafast CDM ESD transients flow from the IC core outward to the ground, resulting in CDM ESD failures [5]. Figure 4-3 shows the waveform and test set-up per CDM ESD standards [9].




**(a)**




**(b)**

*Figure 4-3 Illustration of the standard CDM ESD test model: (a) CDM ESD discharging waveform, and (b) FICDM CDM ESD test set-up.*

A CDM ESD pulse is ultrafast and very short (tr~100ps, td~2ns) compared to an HBM ESD pulse (tr~10ns, td~150ns). The latest CDM ESD standard (ANSI/ESDA/JEDEC JS-002-2014) provides details for building a field-induction CDM (FICDM) ESD tester including two steps: 1) charge an IC part by field induction; 2) discharge the charged device, i.e., device under test (DUT), by using the pogo pin to touch the DUT to ground it. As such, the static charges stored inside the DUT will discharge into the ground, which is apparently an "internal-oriented", "from-internal-to-external" procedure, completed different from an "external-oriented", "from-external-to-internal" HBM ESD event. The sharp difference in nature for CDM and HBM ESD events suggests that their ESD protection methods shall

be different too. However, the classic pad-based ESD protection methods have been commonly used for CDM ESD protection; while the main CDM ESD design effort has been devoted to making a CDM ESD device faster. We believe that the pad-based CDM ESD protection method is fundamentally faulty, which leads to the uncertainty and randomness of CDM ESD design failures that we observed today for the following reasons. First, since the problematic static charges (the "bad guys") are already staying inside an IC part, the ESD devices at pads lose their key function as the "guard" at gate, i.e., blocking the external alien charges from getting into the IC core as in an HBM ESD protection case. Second, theoretically, since the charges stored inside an IC must run through the IC core before being discharged into GND, it is highly possible that internal CDM damages may occur somewhere inside the IC core due to voltage or current build-up. Third, CDM failures depend on the internal current flow routing during CDM discharging, which is very sensitive to both the amount of static charge accumulated inside the IC and, critically, their internal distribution (i.e., location) within the IC core. Theoretically, the internal distribution of static charges can be anywhere, random and time-varying during the lifetime of an IC product. Fourth, the industrial standard FICDM is an accelerated "short" charge induction procedure, which does not faithfully represent the true CDM charging procedures in real world that is a "lifetime" problem. As such, the charges induced into the DUT device during the charging procedure using an FICDM-based CDM tester may not fully distribute throughout the IC chip as is in real world, hence, resulting in great variation in CDM ESD failures. Therefore, the FICDM CDM ESD testing method is over-simplified, which adds

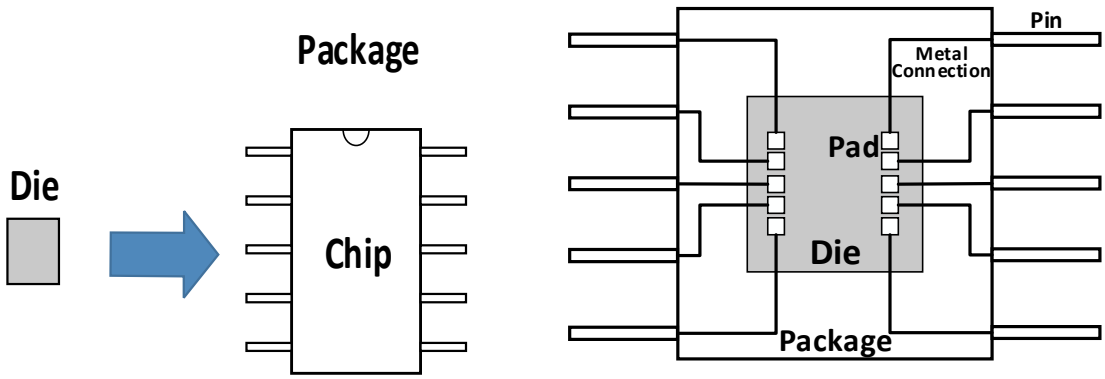



*Figure 4-4 Illustration of the standard CDM ESD test model: (a) CDM ESD discharging waveform, and (b) FICDM CDM ESD test set-up.*

another major uncertainty to CDM ESD testing. In brief, the above analysis suggests that the classic pad-based CDM ESD protection method is fundamentally faulty, causing uncertainty of CDM ESD protection designs and random CDM ESD failures in field, which will be validated by case studies below.

### 4.1.3 Faulty Pad-based CDM ESD Protection Cases

As depicted in Figure 4-4, in principle, CDM ESD failures can occur at any level: bare silicon dies, packaged ICs or system modules [38] [44]. Therefore, robust CDM ESD protection must be designed to protect ICs at any level. Classically, complete full-chip ESD protection requires a global ESD protection network consisting of ESD devices at every pad, so that there is always a low-R ESD discharging path between every two pads under ESD stressing [5]. This is the way to ensure full-chip ESD protection, which works well for "from-external-to-internal" HBM ESD protection. For a packaged IC, the global full-chip ESD protection network may exist on the chip as shown in Figure 4-5 where the central ESD block depicts a pad-based ESD protection network connected to all pads on a

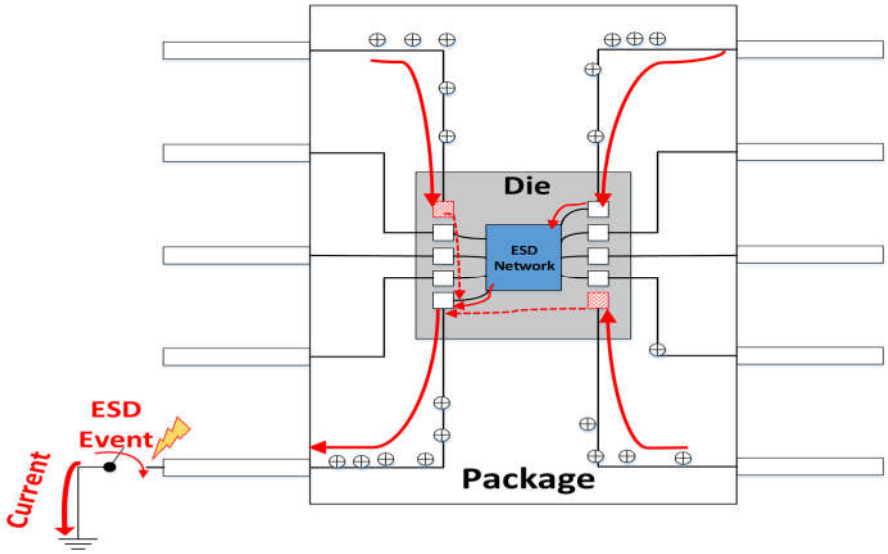



*Figure 4-5 Ideally, a pad-based global ESD network for a packaged IC has ESD devices at all pads to ensure a low-R ESD discharge path between any two pads on a die. Red pads have missing ESD turn-on, forcing charges flowing into the IC die (dashed lines) and causing possible CDM failures.*

chip. For a CDM-charged packaged IC, the static charges are often considered to be stored on the package frame and/or on the power buses [8]. If so, under CDM ESD stressing, i.e., one package pin is suddenly grounded as depicted in Figure 4-5, the stored charges on the package will, conceptually, always be able to find a way to discharge into the grounded pin, either directly through the package metal buses if located nearby, or, through the global ESD protection network connected to the pads on a chip, then discharge into the grounded pin. Either way, the charges stored on the package frame are external to the IC die. This means that, from the viewpoint of the IC die, a CDM ESD event for the packaged IC is similar to the "from-external-to-internal" HBM ESD event for the IC die inside the package. Therefore, the pad-based HBM ESD protection approach shall work, ideally, for the packaged IC in CDM ESD events. Unfortunately, real-world designs are never ideal. In one case, common in practical ESD designs, an ESD device may not be optimized in both

directions for the ESD-critical parameters (t1, Vt1, RON, etc.). Therefore, some ESD devices cannot be turned on in either forward or reverse direction. Since CDM ESD discharge in a packaged IC can be random, this means there are always situations where one or more ESD devices at pads in the global ESD network cannot be turned on in certain direction under the CDM ESD stressing. As a result, the charges stored randomly on a package frame will inevitably run into the internal core circuit, resulting in internal CDM ESD damage, even though the charges will eventually be discharged into the grounded package pin. This is almost unavoidable in practical designs. In a second case, for high frequency, wide bandwidth ICs or high data rate ICs, the signal pads are often not ESD-protected in order to avoid ESD-induced parasitic effects that will affect the high-speed IC performance, as shown in Figure 4-6. In such cases, the global ESD protection network is incomplete. Hence, under CDM ESD stressing, there are always situations where the

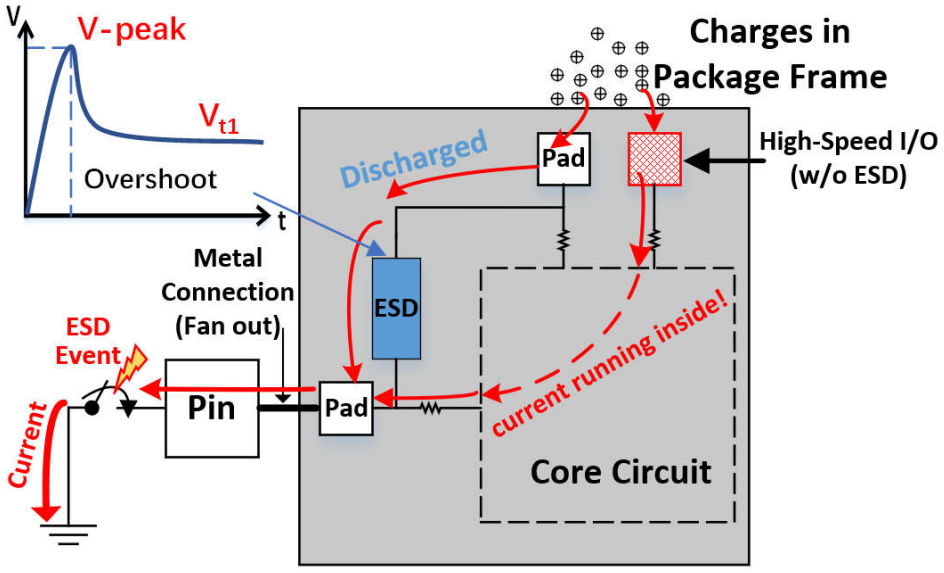



*Figure 4-6 Often, data pads for high-frequency or high-speed links do not have ESD protection devices to avoid ESD-induced parasitic effects. Red pad missing ESD device, and forcing charges flowing into the core (dashed line) and causing possible CDM failures.*

charges stored on the package frame will route into the internal core circuit on the way to package GND, resulting in CDM ESD damages to the core circuit. In summary, the classic pad-based CDM ESD protection method, theoretically, will not work in many scenarios for packaged ICs.

Recently, CDM ESD failure to unpackaged bare IC dies becomes a major reliability concern, which is more devastating compared to packaged ICs. As depicted in Figure 4-7, for a bare Si die, the charges induced by whatever procedures, are stored inside the IC die randomly, unpredictably and anywhere, e.g., in the substrate, along the metal rails or locally to transistors [38] [44]. Using the classic pad-based ESD protection method, as shown in Figure 4-7, simply will not provide CDM ESD protection for the bare IC die. In the case where the charges are stored nearby the GND pad (e.g., VSS), it is possible that the charges may be discharged safely into the nearby ground through the ESD device at a close-by pad. Unfortunately, such an ideal case would be in dream only. For a large and

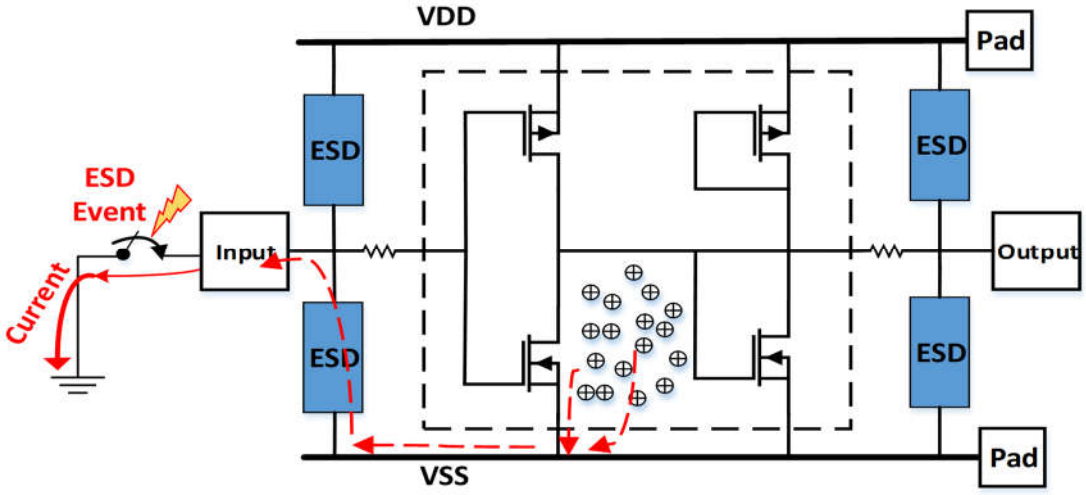



*Figure 4-7 Illustration of using classic pad-based CDM ESD protection method to discharge the electrostatic charges randomly stored inside an IC die.*

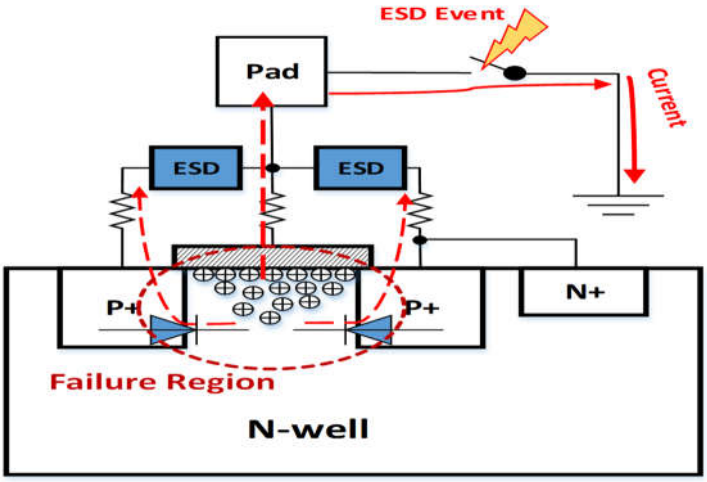



*Figure 4-8 In a case when substantial static charges are stored locally to a MOSFET on a chip, under CDM ESD stressing, some charges will inevitably run through the S/D junction or the gate, resulting in CDM ESD damages regardless if pads are ESD-protected.*

complex chip, the chance is that substantial charges are distributed everywhere randomly on a die that must find their way out to the grounded pad under CDM ESD stressing. Therefore, the charges will flow throughout the internal IC die before discharging into GND, randomly and unpredictably. This means that internal CDM ESD damages will occur even if the pad-based global ESD network would function properly. Even if the pad-

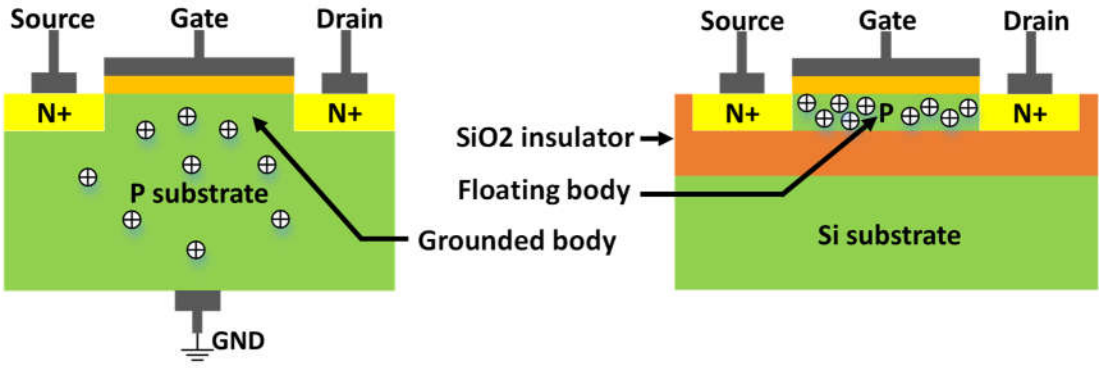



*Figure 4-9 In an SOI IC die, static charges may be stored locally in a MOSFET that is completed isolated from the rest of the chip. Under CDM ESD stressing, these locally stored charges may cause gate ESD damage. (L) charges stored in a bulk MOSFET, and (R) charges stored in an SOI MOSFET.*

based ESD devices were designed perfectly and verified individually by CDM ESD testing, it likely will not provide CDM ESD protection as expected on a chip. Figure 4-8 shows a case where, during a CDM event, the locally stored charges may be capacitively coupled through the gate to a pad when discharging, inevitably causing CDM ESD damage to the gate. Similar CDM ESD failures were reported for 14nm FinFET design, which failed CDM test at low CDM stress (<100V) and the ESD failure was attributed to electrical overstress to the metal gate during CDM stress [42]. The random CDM ESD failure becomes even worse for SOI chips where each MOSFET is isolated from the rest of the circuit. Consequently, as shown in Figure 4-9, the CDM induced charges are likely stored and confined locally to a MOSFET, which will most likely run through the local gate during discharging and cause gate damage even if all pads are ESD-protected by design. From the above analysis, we believe that the classic pad-based ESD protection method, while working nicely for "from-external-to-internal" HBM ESD events by blocking external charges from getting into the core circuit through pads, it, in principle, will not protect ICs against "from-internal-to-external" CDM ESD stressing. This discovery likely explains why CDM ESD design is still a black magic full of uncertainty, and the "luck" makes CDM ESD designs essentially unpredictable and unreproducible today.

### 4.1.4 Faulty CDM ESD Protection by Circuit Analysis

The validation was conducted by circuit analysis using a 3-stage oscillator IC designed in a foundry 45nm SOI CMOS as shown in Figure 4-10, which uses the classic pad-based ESD protection scheme for CDM ESD protection where the three pads, VDD, VSS and

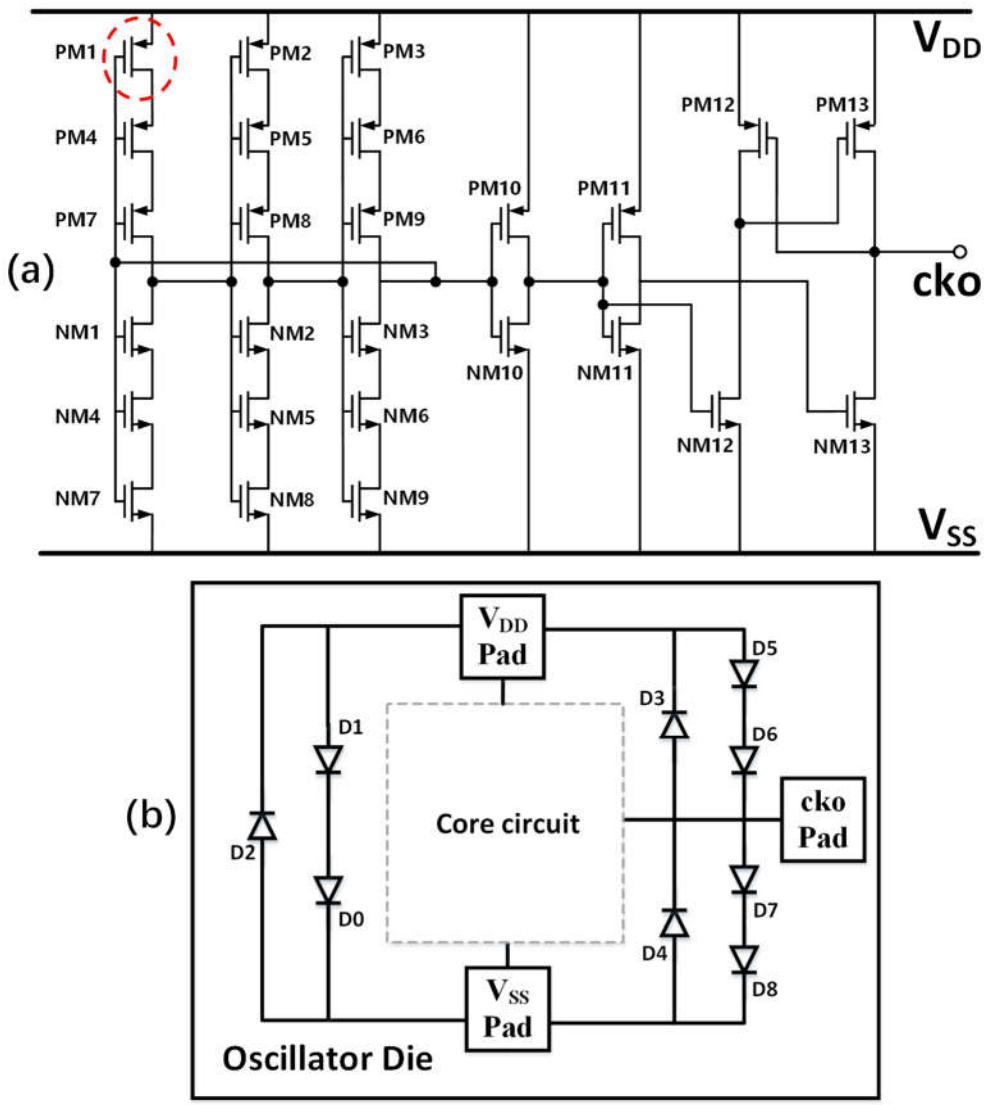



*Figure 4-10 A 3-stage oscillator designed in 45nm SOI in this study is protected by traditional pad-based CDM ESD protection scheme: (a) circuit schematic, (b) IC die diagram including core schematic and ESD network.*

cko (Output), are protected by diode ESD devices. Per the foundry Design Rules, we chose the ESD diodes with a total finger width of 360μm for the targeted 500V CDM ESD protection (10A). SPICE circuit simulation was conducted for three CDM ESD testing scenarios for comparison.

A. New Pseudo-Distributed FICDM ESD Test Model

Figure 4-11 depicts the lumped equivalent circuit model for the commonly used FICDM test setup by ANSI/ESDA/JEDEC JS-002-2014 Standard [9], where CDUT is the capacitance between the DUT and the induction field plate, CDG is the capacitance between the DUT and the discharge ground plate and CFG is the capacitance between the field plate and the ground plate. From the previous discussion, the over-simplified FICDM tester circuit model fails to accurately model the real-world CDM events because the lumped capacitance circuit simply cannot reflect the full distribution nature of the CDM charge storage inside a DUT IC, hence, leading to major CDM testing uncertainties in field. To address this problem, we propose a new pseudo-distributed equivalent circuit model for an enhanced FICDM-like CDM test setup as depicted in Figure 4-12. In the new model, $C_{DG}$ is considered as a distributed capacitor net ($C_{DG1}$, $C_{DG2}$, … $C_{DGx}$) across all IC pads, which, in first order approximation, may be equal for each pad assuming all pads are same. $C_{DUT}$ is decomposed into two parts: $C_{die\text{-}FP}$ for the capacitance from die substrate to field plate and $C_{DF}$ for the capacitance from each pad to the field plate, which comprises a

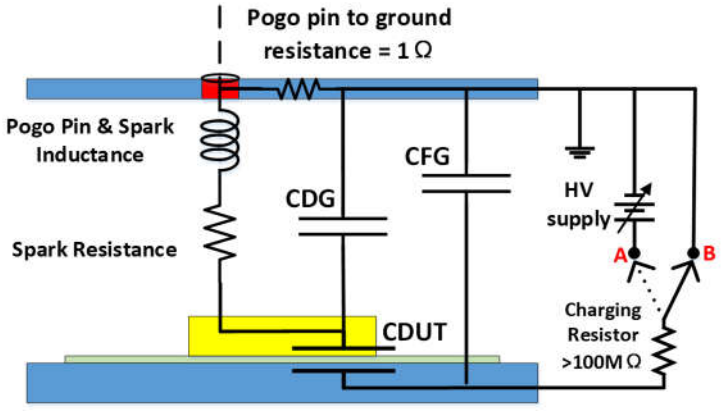



*Figure 4-11 A simplified FICDM tester circuit schematic [9].*

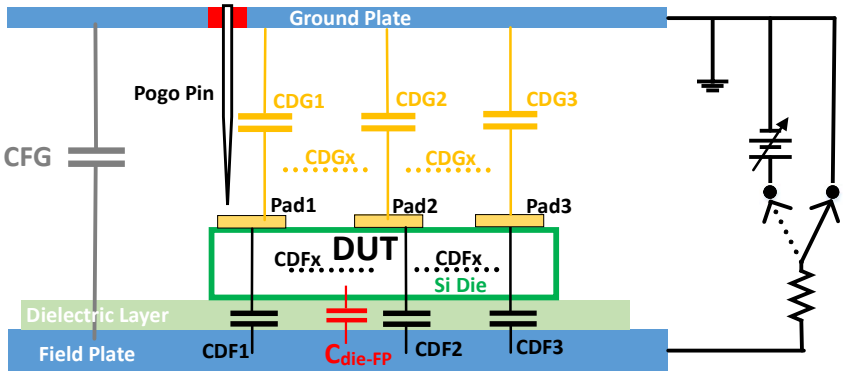



*Figure 4-12 Our new pseudo-distributed circuit model for FICDM tester.*

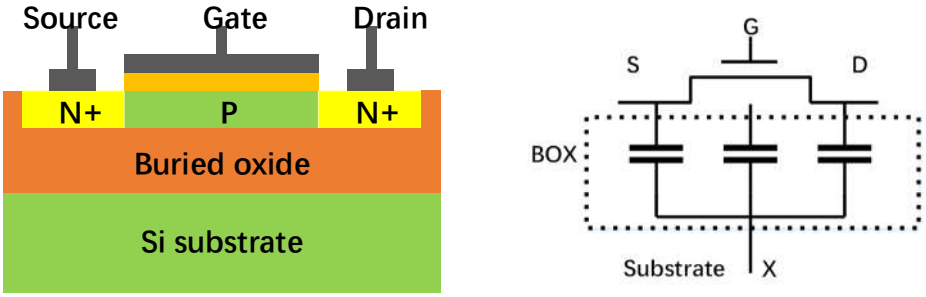



*Figure 4-13 A MOSFET in 45nm SOI CMOS: cross-section and BOX/substrate model with X node being the substrate.*

distributed capacitor net ($C_{DF1}$, $C_{DF2}$, … $C_{DFx}$) across all package pads. $C_{die\text{-}FP}$ can be estimated per the IC die area with respect to the size of the small calibration metal disc of an FICDM tester. $C_{DF1}$, $C_{DF2}$, … $C_{DGx}$ are considered equal for each pad. For the 3-pad oscillator IC designed within a 2mm x 2mm die in 45nm SOI CMOS in this study, the estimated values are: $C_{DG1,2,3}$≈0.61pF, $C_{DF1,2,3}$≈ 2.114pF, $C_{die\text{-}FP}$≈0.437pF and $C_{FG}$≈17.0pF. We call it a pseudo-distributed FICDM test model because the capacitor networks are largely depending upon how fine the grid is for the capacitor mesh associated with the DUT; nevertheless, it is a much-improved model over the lumped FICDM test model commonly used. Figure 4-13 depicts a MOSFET in 45nm SOI where capacitance

associated with the buried oxide (BOX) layer and the substrate node "X" are included in the foundry PDK, hence avoiding extra effort needed to model it [45].

B. Scenario-1: External-Oriented CDM ESD Zapping

Three CDM ESD discharge scenarios were studied for the oscillator IC designed in 45nm SOI. Depicted in Figure 4-14, Scenario-1 models HBM-like CDM ESD zapping method where a fast CDM pulse, defined by CDM ESD test model [9], is used to zap the oscillator IC die, similar to very-fast transmission-line pulsing (VFTLP) testing (i.e., from-external-to-internal stressing) to emulate CDM zapping [5]. In all scenarios, the $V_{DD}$ pad was zapped. CDM ESD stimuli of varying levels (voltage and current) are used to zap the DUT IC die. The simple ESD failure criterion used in this study is the gate voltage breakdown ($|V_{GS}|$ or $|V_{GD}|$) of any MOSFET, which is $BV_{OX}$ ~6.5V, during the CDM pulse period of 2ns. Figure 4-15 depicts the transient CDM discharging voltage waveforms by SPICE for an exemplar MOSFET PM1, which shows that, under both 500V and 50V CDM

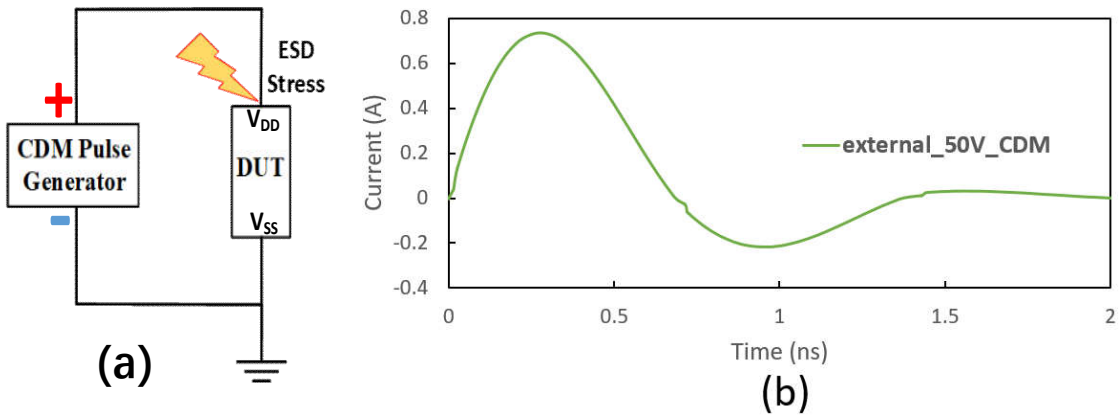



*Figure 4-14 Scenario-1 HBM-like CDM ESD stressing where an external CDM pulse is applied to the DUT (oscillator IC die) by zapping the VDD pad with respect to the VSS pad (GND): (a) schematic, and (b) CDM zapping waveform used per CDM standard.*

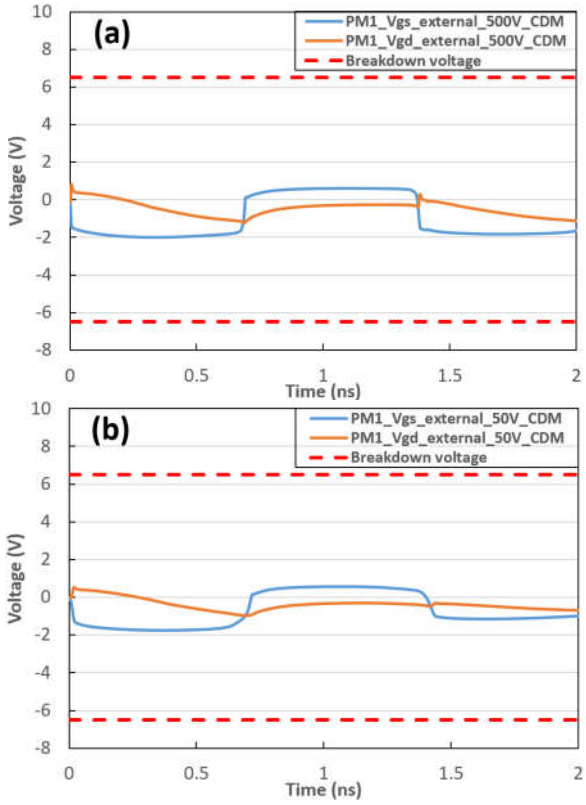



*Figure 4-15 Exemplary transient voltage analysis for VGS and VGD of PM1 of the oscillator IC under Scenario-1 CDM zapping: (a) 500V CDM stressing, and (b) 50V CDM stressing.*

zapping, no CDM-induced MOSFET breakdown occurs. Table 4-1 summarizes the maximum $V_{GS}$ and $V_{GD}$ of PM1 under CDM zapping, showing that the peak transient $V_{GS}$ and $V_{GD}$ increased slightly as CDM increases from 50V to 500V, meaning the pad-based ESD protection works well in defending against external-oriented ESD stressing. Figure 4-16 shows more details on the CDM discharging behaviours under the 50V $V_{DD}$-to-$V_{SS}$ CDM zapping. It is observed that, due to CDM discharging waveform oscillation, two CDM discharge paths are turned on alternatively: D1+D0 path during the positive cycle, and D2 path during the negative cycle, each taking almost the full load of CDM discharging

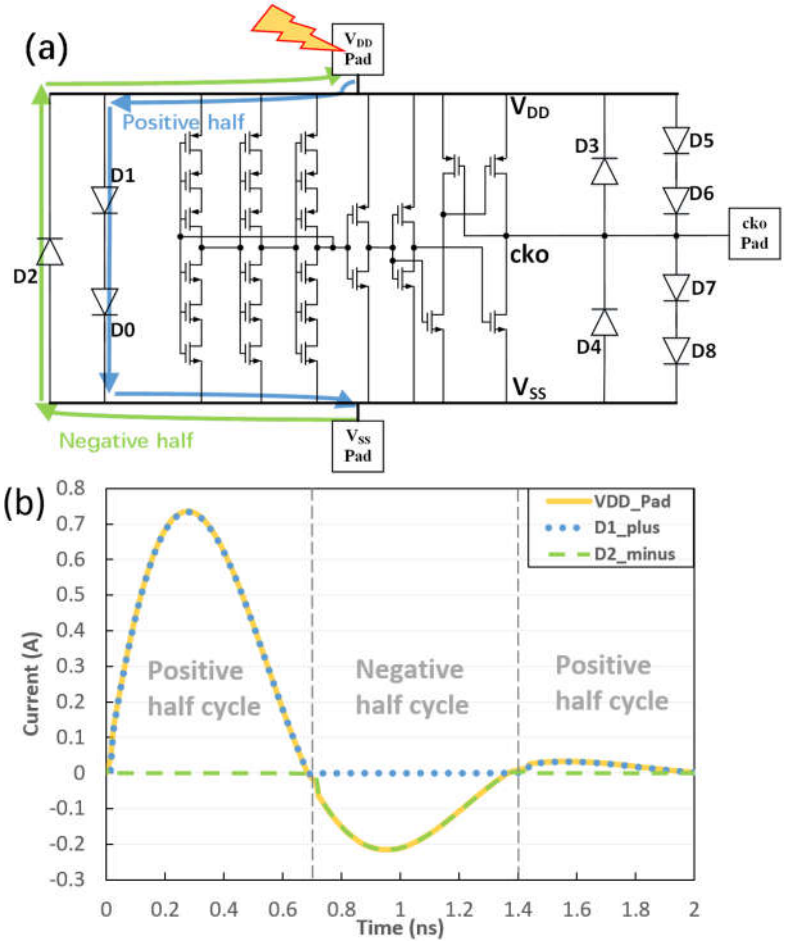



*Figure 4-16 CDM ESD stressing Scenario-1 using an external 50V CDM pulse to zap VDD pad w.r.t. VSS pad: (a) CDM ESD discharge paths, and (b) transient CDM current waveforms.*

current during its functional cycle. CDM discharging current flowing into the IC core is negligible, hence provides CDM ESD protection.

C. Scenario-2: Enhanced FICDM ESD Zapping

Scenario-2 models from-internal-to-external FICDM ESD zapping, where the DUT IC die is charged by induction and then discharges by grounding the $V_{DD}$ pad. Figure 4-17 depicts the FICDM ESD simulation schematic deck where “GND” and “Field” represent

| Scenario-1 External-Oriented CDM Zapping | | | | |
|---|---|---|---|---|
| | 50V CDM | 100V CDM | 250V CDM | 500V CDM |
| Max $\|V_{GS}\|$&$\|V_{GD}\|$ (V) | 1.76 | 1.82 | 1.91 | 2.02 |
| Scenario-2 Internal-Oriented Lumped FICDM Zapping | | | | |
| | 25V CDM | 50V CDM | 75V CDM | 100V CDM |
| Max $\|V_{GS}\|$&$\|V_{GD}\|$ (V) | 4.51 | 7.44 | 8.04 | 8.21 |

*Table 4-1 Summary of peak $|V_{GS}|$ and $|V_{GD}|$ of PM1 under CDM zapping*

the ground plate and field plate, respectively, and "sub" is the "X" node of MOSFET. A voltage-controlled switch models the spark as the pogo pin approaches DUT pad. Voltage source $V_{CDM}$ is the FICDM charging voltage. Voltage source $V_0$ controls the switch to trigger CDM discharging. Figure 4-18 depicts the transient CDM discharge voltage waveforms by SPICE for exemplar MOSFET PM1under FICDM zapping with the extracted maximum transient $V_{GS}$ and $V_{GD}$ of PM1 listed in Table 1. It is observed that CDM failure occurs to some MOSFETs, e.g., $V_{GS}$ breakdown at PM1. Figure 4-19 shows more details on the CDM discharging behaviours under the 50V FICDM zapping at $V_{DD}$ pad. It is observed that, due to CDM discharging waveform oscillation, four CDM discharge paths are turned on alternatively: D1+D0 path ($V_{DD}$ to $V_{SS}$) and D5+D6 path ($V_{DD}$ to cko) during the positive cycle, and D2 path ($V_{SS}$ to $V_{DD}$) and D3 path (cko to $V_{DD}$) during the negative cycle, respectively, together taking the full load of CDM discharging current during their functional cycles. This is sharply different from Scenario-1 where the external CDM pulse zapping the $V_{DD}$ pad can be readily discharged via one path starting from the zapping node ($V_{DD}$). However, in Scenario-2, due to the distributed nature of

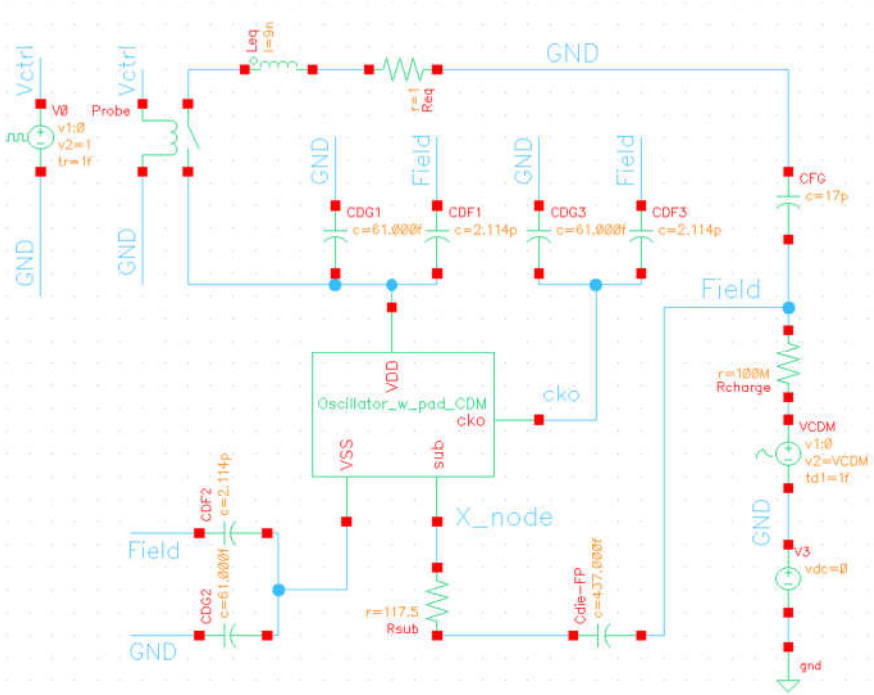



*Figure 4-17 A schematic deck used in Scenarios-2/3 to simulate the oscillator under CDM ESD stressing due to internal charges where "$V_{DD}$" pad is zapped.*

internal charge storage, the static charges may stay anywhere inside the IC core. Specifically, the charges accumulated near both $V_{SS}$ pad and cko pad will find different paths to discharge. Consequently, the discharging currents running through the different paths within the chip caused internal CDM failure at ~50V stressing level. Apparently, the "from-external-to-internal" CDM zapping method over-evaluated the ESD capability (passed ~500V), while the "from-internal-to-external" FICDM zapping shows internal CDM failures at a much lower stressing level (failed ~50V). It is important to understand that, without considering the charges stored inside the IC die that can be modelled using a distributed inside-die capacitor mesh (i.e., Scenario-3), even the enhanced FICDM model is still equivalent to an "external-oriented" CDM zapping to the IC die. Further and critically, since the internal distribution of static charges inside an IC core may be random

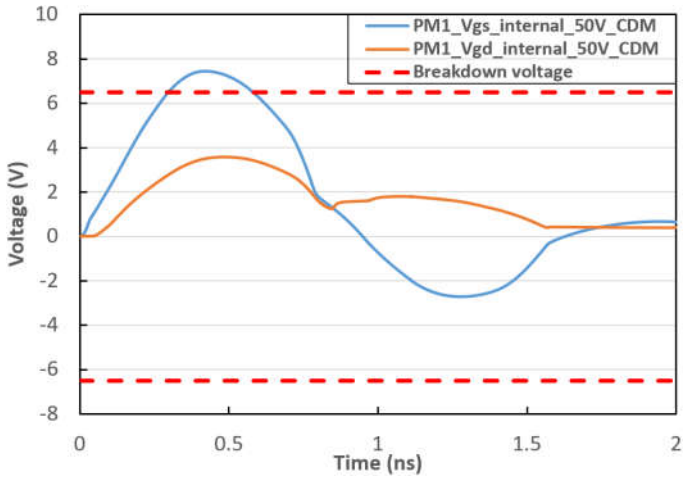



*Figure 4-18 Exemplary transient voltage analysis for $V_{GS}$ and $V_{GD}$ of PM1 of oscillator IC under Scenario-2 CDM zapping by the 50V CDM pulse.*

during its lifetime, the actual field CDM failure can be unpredictable regardless of the in-house test results from the existing FICDM test method. Here arises the key question: how good and useful is the FICDM ESD test method?!

D. Scenario-3: Distributed Real-World CDM ESD Zapping

Scenario-3 is a new model proposed to, ideally, accurately describe the real-world CDM ESD phenomena, i.e., the charges accumulated inside an IC device, by whatever way during its lifetime, may be randomly distributed throughout the whole chip, which cannot be modelled by the over-simplified lumped FICDM model. The internally distributed charges can be modelled by a distributed capacitor mesh network within the IC die. Figure 4-20 depicts the near-real-world CDM ESD discharging simulation schematic deck. Assume that the internal static charges may be distributed randomly, we designed three Splits to simulate three simple, yet representative CDM discharge cases: each assuming

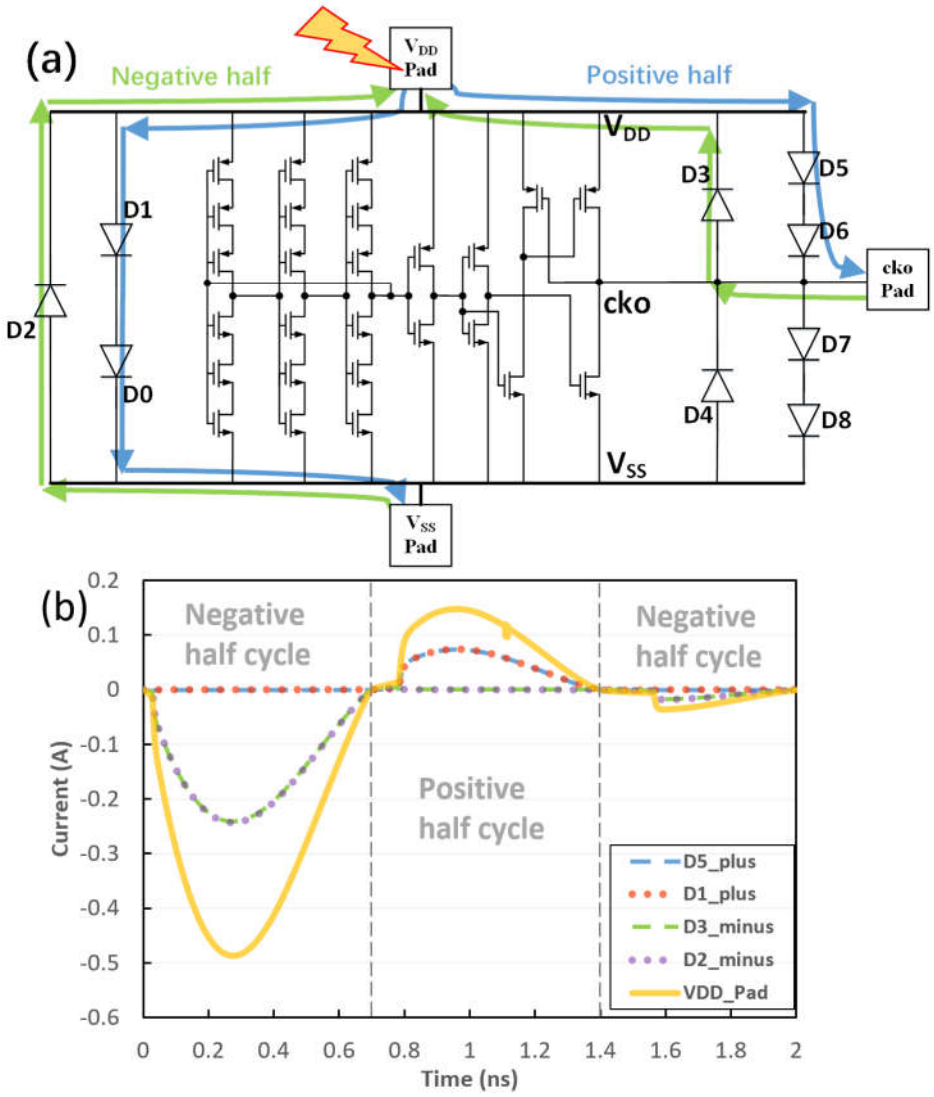



*Figure 4-19 CDM ESD stressing Scenario-2 where VDD pad is zapped by a CDM pulse from internal charges per FICDM model: (a) CDM discharge paths, and (b) transient CDM current waveforms.*

substantial charges are stored locally at MOSFET NM1, PM9 & NM5. We expect different internal CDM discharging routes for each Split. During the simulation, CDM current pulses (stimuli) of varying strengths are studied, reflecting varying charge distribution inside the IC chip. Figure 4-21 depicts the transient voltage behaviours of exemplar MOSFETs under CDM stressing originated from different internal charge storage distribution cases when

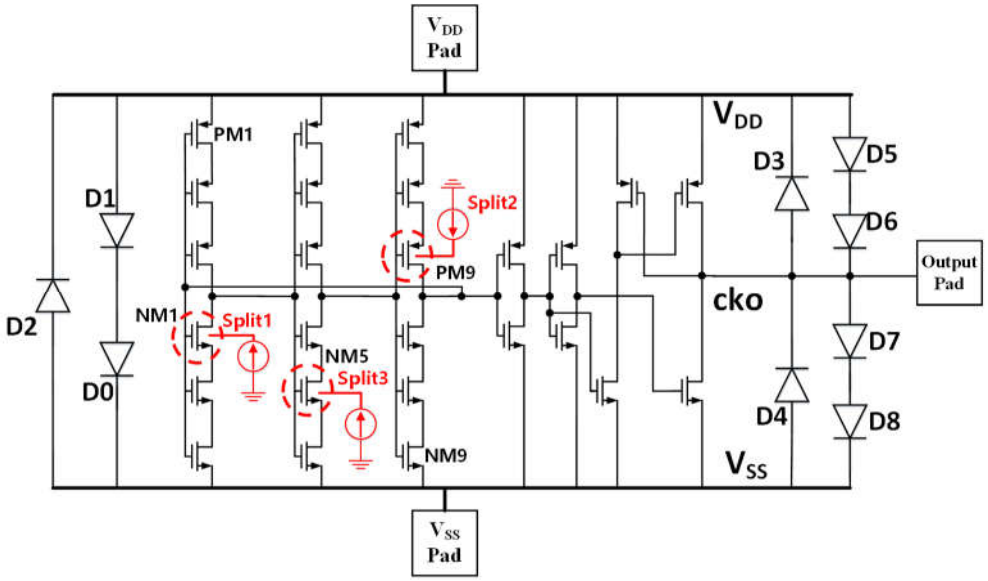



Figure 4-20 *Scenario-3 internal-oriented CDM ESD stressing schematic deck where VDD pad is zapped by internally generated CDM pulses from internal charges accumulated locally to NM1 (Split 1), PM9 (Split 2) and NM5 (Split 3).*

the local CDM zapping strength is equivalent roughly to 1% of that under FICDM stressing in Scenario-2. It is readily observed that CDM-induced voltage breakdown failure occurs to different MOSFETs depending on the storage locations of the internal charges, i.e., Split 1 (PM1 gate), Split 2 (PM1 gate and NM9 gate) and Split 3 (none). In addition to fully illustrating the varying CDM failures caused by random distribution of internal charges within a chip, the observed CDM failure level is much lower than that in Scenario-2, roughly ~1% of the CDM stressing level in our examples. This study clearly shows that CDM failure is closely related to the internal distribution of the charges accumulated inside an IC die and the lumped FICDM test model is over-simplified. It shows that, for the oscillator IC die with all pads protected by ESD devices, the new internal-distributed CDM zapping model predicts internal CDM failures occurring at much lower ESD level than that predicted by using the lumped FICDM zapping model. Therefore, the classic pad-based CDM ESD protection method is fundamentally faulty. A novel CDM protection method is

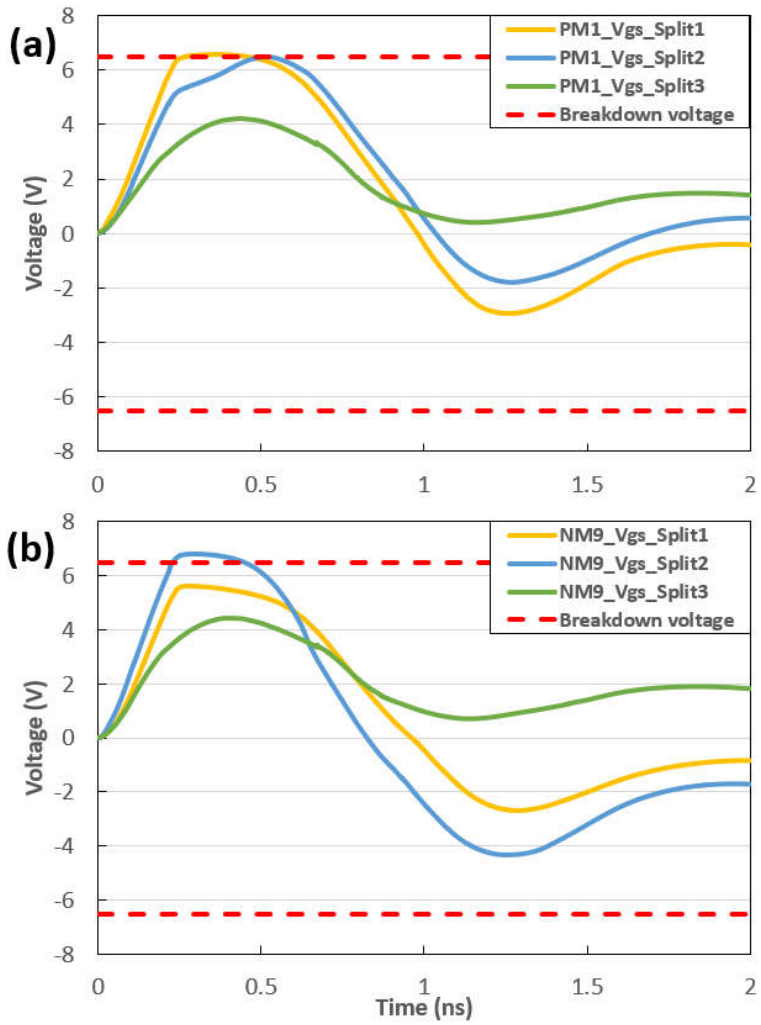



*Figure 4-21 Transient ESD discharge voltage waveform analysis for the oscillator IC die in Scenario-3 under internal-distributed CDM zapping to $V_{DD}$ pad. The local CDM zapping strength is equivalent to ~1% of that for lumped FICDM zapping in Scenario-2; however, internal CDM failures (gate breakdown) occur at varying locations in the three internal zapping splits: (a) MOSFET PM1, and (b) MOSFET NM9.*

being explored currently. We proposed a new internally distributed CDM ESD protection method as a disruptive solution that is under development. The basic idea is that an IC die can be smartly partitioned to reflect the distributed nature of internal charge storage and ESD devices of smaller footprints will be placed at selected internal circuit nodes per the smart portioning. Therefore, as static charges are generated and accumulated internally and locally, and when reaching to a given local potential threshold, the local ESD device will

be triggered to discharge the static charges locally. Therefore, the new internally distributed ESD mesh network can provide adequate whole-chip CDM ESD protection, efficiently addressing the "from-internal-to-external" CDM ESD events by a novel "internal-oriented" ESD discharge mechanism.

In summary, CDM ESD protection is a challenging design problem, which has been notoriously unpredictable, unproducible and unreliable in field. Validated by analyzing an oscillator IC designed in a foundry 45nm SOI CMOS, the comprehensive study in Chapter 4.1 found that the magic uncertainty of CDM ESD protection is closely related to the somewhat random internal distribution of the electrostatic charges accumulated inside IC chips during their life time, which cannot be accurately modelled by the over-simplified lumped FICDM CDM test method. It concludes that the classic pad-based ESD protection method, working nicely for the "external-oriented", "from-external-to-internal" HBM CDM protection, is fundamentally faulty for "internal-oriented", "from-internal-to-external" CDM ESD events. It hence calls for new revolutionary on-chip CDM ESD protection solutions and more accurate CDM test models.

## 4.2 Non-Pad-Based in Situ in-Operando CDM ESD Protection Using Internally Distributed Network

Previously, it is reported in Chapter 4.1 that conventional pad-based CDM ESD protection method may be theoretically wrong because CDM ESD phenomena are internal-oriented and "from-internal-to-external" in nature [46]. In addition, traditional in-plane side-by-side ESD protection designs not only consume significant Si die area, but also are

extremely layout-unfriendly, particularly for large and high-pin-count chips in beyond-28nm IC technologies [30]. This Chapter 4.2 discusses a disruptively new non-pad-based internally distributed CDM ESD protection concept, which is demonstrated in an oscillator IC designed and fabricated in a 45nm SOI CMOS process. Design of novel interposer and through-silicon-via (TSV) based internal-distributed CDM ESD protection mesh networks are also presented.

### 4.2.1 Internal-Distributed CDM ESD Protection

It is important to understand that CDM ESD phenomena are entirely different from HBM ESD events in nature. In principle, HBM ESD is an external-oriented event where electrostatic charges stored in a human body can be discharged into an IC, causing ESD damage to the chip. Correspondingly, the classic pad-based on-chip ESD protection

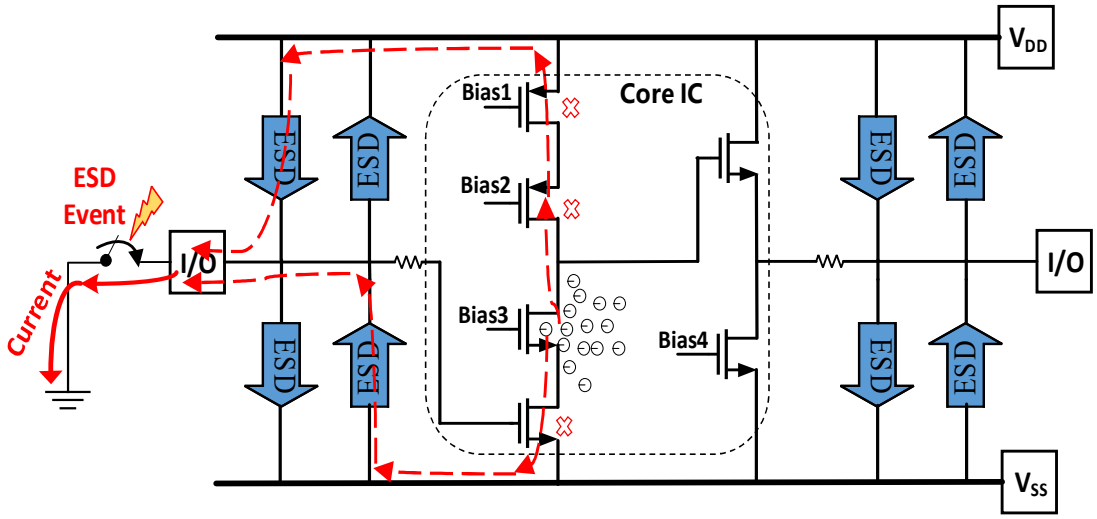



Figure 4-22 *Illustration of traditional pad-based CDM ESD protection scheme where internally stored charges may cause internal CDM ESD failures (marked X) when discharging from their internal locations to external GND through ESD devices at pads.*

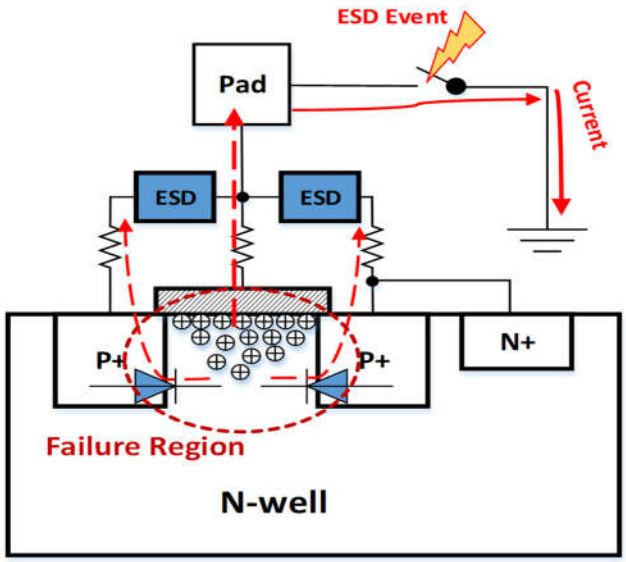



Figure 4-23 *An exemplary case shows possible internal CDM ESD failure at SD junction or gate in a pad-based CDM ESD protection scenario.*

follows a "from-external-to-internal" protocol, meaning, properly designed ESD protection devices are connected to each pad, which will be triggered by an incident ESD transient and provides a conduction path from the pad to ground (GND) to shunt the incoming HBM ESD pulse, hence protecting the IC from ESD damage. Essentially, a pad-connected ESD protection device serves as a "guard" at the "door" to prevent any alien electrostatic charges (i.e., the intruders) from getting into the IC die. This ESD protection principle works nicely for all external-oriented ESD events, such as HBM, MM and IEC ESD events. In the contrary, a CDM ESD event is an internal-oriented phenomenon where electrostatic charges are introduced into an IC part via various ways during its full lifespan, such as triboelectric generation or field induction, and the static charges created can be stored inside an IC die in random and distributed manners, anywhere and being time variant. It is this "anytime anywhere" feature that makes CDM ESD phenomena completely different from HBM ESD events, which, theoretically, disqualifies the classic pad-based ESD

protection method from offering CDM ESD protection. Figure 4-22 illustrates the conventional pad-based CDM ESD protection scheme where the ESD protection devices at pads are supposedly to provide ESD protection against CDM ESD transients. Unfortunately, even if a perfect pad-based ESD protection network exists on a chip, during an CDM ESD event, since the internally stored electrostatic charges are randomly located in a distributed way, these static charges must find their routes from where they stay to selected pad(s) to be discharged into GND. Obviously, as the stored electrostatic charges find their way out, they have to run through an IC core following an "from-internal-to-external" protocol, and apparently, it is entirely possible that internal CDM ESD failures (voltage or current breakdown) may occur even if the pad-based ESD protection devices function perfectly in ESD discharging [46]. Figure 4-23 depicts another possible CDM ESD failure case where substantial electrostatic charges are stored locally around a large MOSFET and some static charges will inevitably run through an S/D junction or a Gate along any ESD discharging path, resulting in internal CDM ESD failure regardless of the pad-based ESD protection network. Moreover, the industrial standard field-induction CDM (FICDM) testing method is an over-simplified short-time accelerated charge induction technique, which cannot truthfully model the real-world CDM ESD charging and storing procedures (i.e., random distribution across a chip), hence, the true CDM discharging phenomenon, therefore adding another factor to the uncertainty of CDM ESD failures in design, testing and field application phases [8]. Therefore, the classic pad-based CDM ESD protection method is believed to be fundamentally faulty [46].

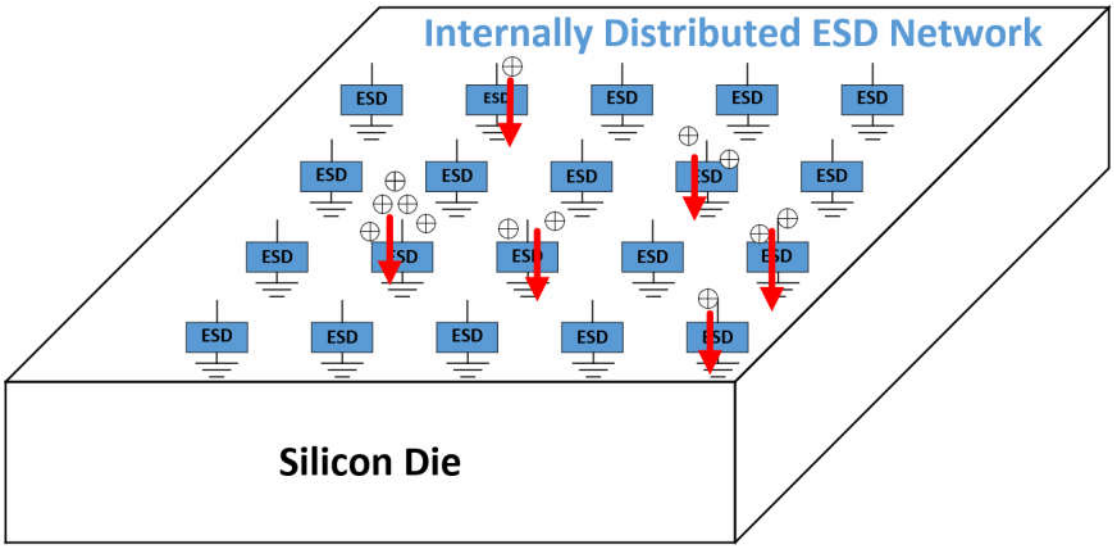



Figure 4-24 *Illustration of the new internal-distributed CDM ESD protection method for ICs.*

Understanding that electrostatic charges are introduced to an IC anytime and can be stored inside the IC randomly in a distributed manner, a new non-pad-based internally distributed CDM ESD protection technique is devised for *in situ in-operando* ESD protection on a chip [47]. As depicted conceptually in Figure 4-24 illustrates the new concept of internally distributed CDM ESD protection mesh network to deal with the nature of internal charge distribution, which is addressed by a unique Smart Partitioning technique that can intelligently partition the IC die according to circuit functions, layout floor plan, as well as device properties and sizes. The internal-distributed CDM ESD protection mesh comprises smaller-sized ESD protection devices, designed and embedded inside the IC die, which are placed at selected internal nodes per the smart portioning protocol according to the internal/local CDM charge distribution. Therefore, as electrostatic charges are generated and accumulated internally and locally, and when they locally reach to a given local potential threshold (corresponding to a certain amount of

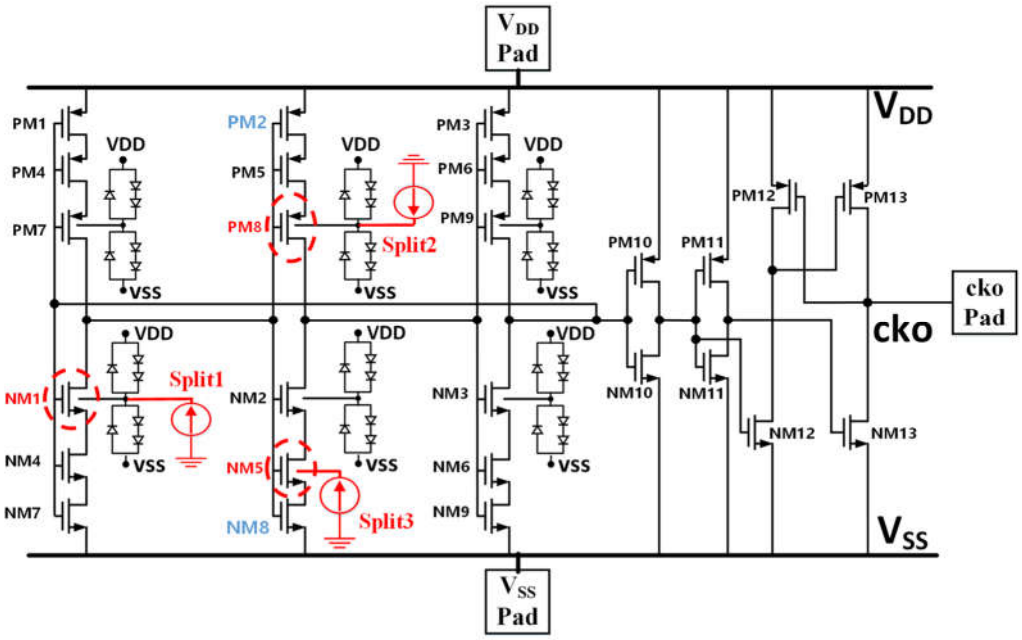



Figure 4-25 *A 3-stage oscillator IC designed in a 45nm SOI CMOS where the large MOSFETs (NM1, NM2, NM3, PM7, PM8 & PM9) likely hold a large number of static charges locally. An internally distributed CDM ESD mesh is designed with smaller ESD protection devices connected to selected internal nodes according to smart partitioning. There are no pad-based ESD protection devices on the chip. CDM ESD simulation has three splits reflecting varying internal charge distribution and different CDM zapping source locations: Split-1 for NM1, Split-2 for PM8 and Split-3 for NM5.*

static charges), the internal/local ESD protection device will be triggered off to form a low-R conduction path to a local GND, therefore, the electrostatic charges will be discharged locally without having to collectively flow through the internal die to find their ways to GND for ESD discharging. Therefore, the new internally distributed ESD protection mesh can provide adequate whole-chip CDM ESD protection in a *in situ in-operando* fashion. Consequently, the new internal-distributed CDM ESD protection mesh network can effectively address the "from-internal-to-external" CDM ESD phenomena that could not be handled by any traditional pad-based ESD protection methods. It is worth noting that, due to internal and dynamic charge distribution, substantially smaller ESD protection devices may suffice to handle the same level of CDM ESD transient compared to larger

ESD protection devices needed in a traditional pad-based ESD protection scheme. This translates into reduced layout size consumed by ESD protection structures.

The new internally distributed CDM ESD protection technique was first validated by chip level simulation using a CDM-protected 3-stage oscillator IC designed in foundry 45nm SOI CMOS technology. Figure 4-25 shows the schematic for the 3-stage oscillator

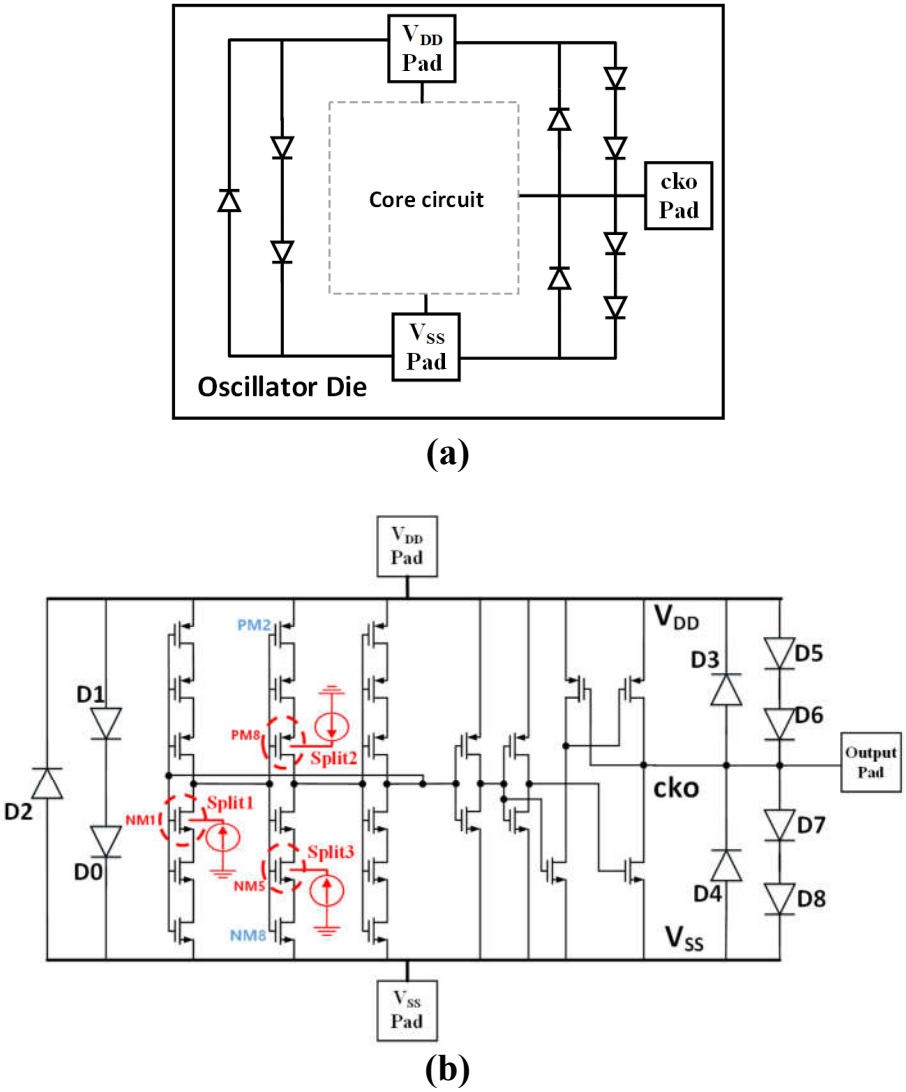
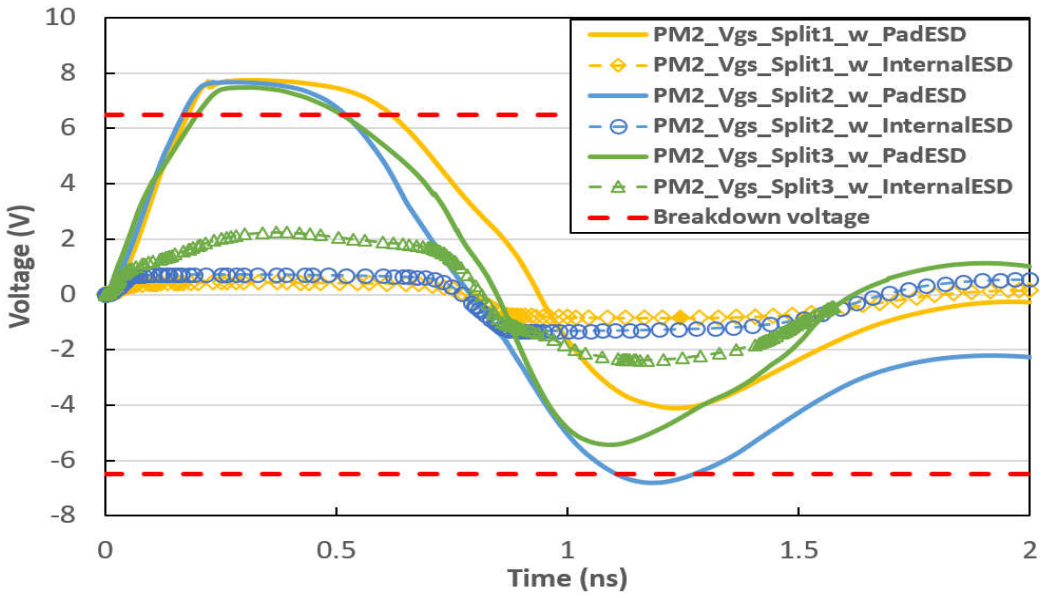


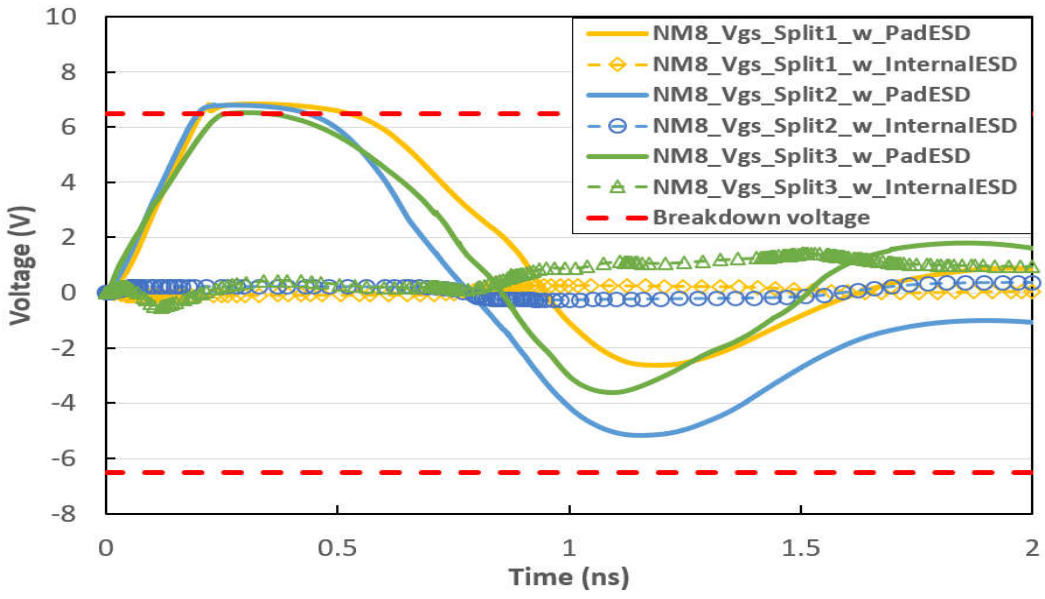

*Figure 4-26 A traditional pad-based CDM ESD protection scheme for the same oscillator IC: (a) diagram for full-chip ESD protection network, and (b) oscillator schematic. The same three splits are simulated: Split-1 for NM1, Split-2 for PM8 and Split-3 for NM5.*

IC where six large MOSFET devices (NM1, NM2, NM3, PM7, PM8 and PM9) are identified as the main storage bins of the internal electrostatic charges on the chip, reflecting varying internal static charge distribution. Per the smart partitioning rule, smaller-sized internal/local ESD protection structures will be placed at the internal circuit nodes associated with these large MOSFETs. The internal ESD protection structures used in this work are anti-parallel ESD protection diodes that form the internally distributed CDM ESD protection mesh network. For comparison, Figure 4-26 shows a traditional pad-based CDM ESD protection network for the same oscillator IC using same ESD protection diodes of larger size. The CDM ESD design target is 500V CDM (failure current $I_{t2}$~10A), which requires the ESD diode being 360μm wide (finger width) for the pad-based ESD design. It is worth to note that, since an internal ESD protection device only needs to handle much smaller amount of locally accumulated static charges that is a small fraction of the total amount of electrostatic charges expected for the whole chip for the same ESD protection level, these internal ESD protection devices are much smaller than that of pad-based ESD protection structures. Accordingly, for the new internal-distributed CDM ESD protection mesh, the internal ESD protection diode features a smaller size of 60μm in width, hence, dramatically reducing the ESD-induced design overhead.

SPICE ESD circuit simulation was conducted for the two CDM ESD protected oscillator IC cases shown in Figure 4-25 and 4-26 using a new near-real-world CDM ESD discharging circuit model and simulation method recently proposed to overcome the problem of FICDM ESD model [46]. Figure 4-25 depicts the CDM ESD simulation deck that features a new non-pad-based internal-distributed CDM ESD protection mesh network




**(a)**




**(b)**

*Figure 4-27 Exemplary transient voltage analysis for VGS of PM2 and NM8 of the ICs under equivalent 50V CDM ESD zapping: (a) gate breakdown failures occur in the IC using classic pad-based CDM ESD protection network, and (b) the IC using the new internal-distributed CDM ESD protection mesh passed CDM ESD zapping.*

comprising internal CDM ESD diodes connected to the large charge storage devices, NM1, NM2, NM3, PM7, PM8 and PM9. Figure 4-27 shows the comparison case featuring traditional pad-based CDM ESD protection network. For both cases, the IC dies are pre-charged before CDM ESD discharging. Three CDM ESD discharging splits were studied in CDM ESD simulation to reflect the nature of varying internal static charge distribution, hence CDM ESD discharging scenarios where discharging initiated by charges at different internal locations: Split-1 for charges stored in NM1, Split-2 for charges stored at PM8 and Split-3 for charges accumulated at NM5. Note that Split-3 reflects a general situation where static charges may be randomly accumulated at NM5, which is not a main charge storage bin though. Figure 4-25 models near-real-world CDM ESD discharging where internal charges stored in NM1, PM8 and NM5 are discharged by grounding the $V_{DD}$ pad. As a comparison, Figure 4-26 depicts traditional CDM ESD discharging where internal charges will be discharged to the $V_{DD}$ pad through the pad-based ESD protection devices. It is expected that different CDM ESD discharge paths will act in the three splits shown in Figure 4-25 and 4-26. During CDM ESD simulation, CDM ESD stimuli of varying strengths are used to evaluate different CDM ESD discharging capabilities of the Splits. The CDM ESD failure criterion used is the gate voltage breakdown ($|V_{GS}|$ or $|V_{GD}|$) of any MOSFET, which is $BV_{OX}$~6.5V for the transient CDM discharging voltage waveforms by SPICE for exemplar MOSFETs, PM2 and NM8, for the splits under 50V CDM ESD zapping where the equivalent internal/local pulse strength is about 2% of 50V when zapped at a pad. It is observed that CDM ESD voltage breakdown failures occurred at the gate of

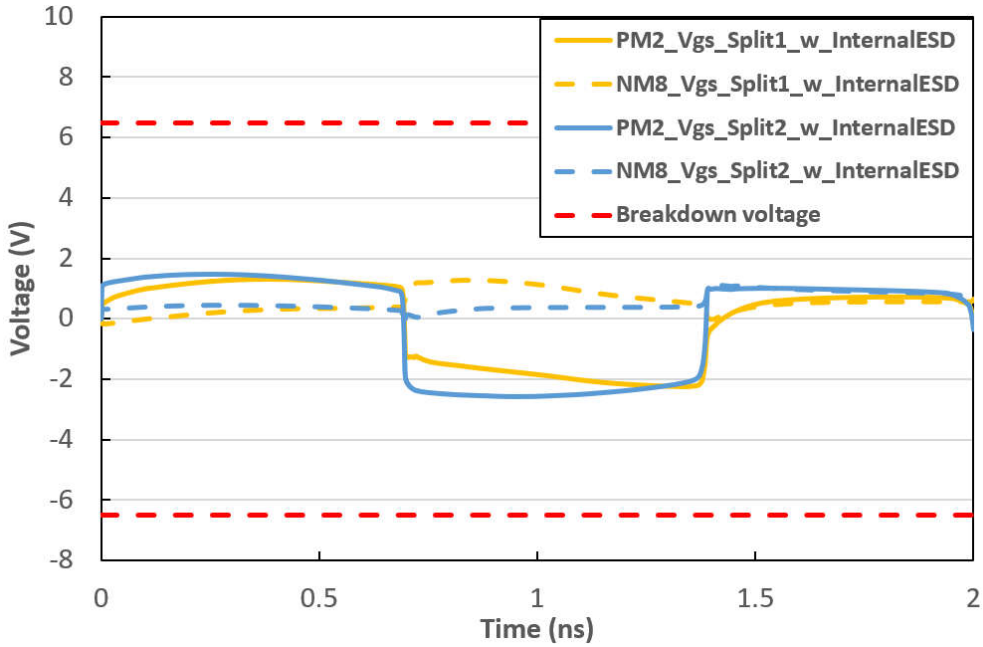



Figure 4-28 *Exemplary transient voltage analysis for $V_{GS}$ of PM2 and NM8 of the ICs under 500V CDM ESD zapping shows now voltage breakdown failure in the IC using the new internal-distributed CDM ESD protection mesh network.*

PM2 and NM8 for the IC case of using traditional pad-based CDM ESD protection; however, the IC using new internal-distributed CDM ESD method passed 50V CDM ESD zapping.

To further evaluate the ESD protection capability of the new internal-distributed CDM ESD mesh network, CDM ESD pulse strength increases in CDM ESD simulation for the IC case of Figure 4-25 and Figure 4-28 shows that it can survive 500V CDM ESD zapping without any gate breakdown failure. This chip-level CDM ESD circuit simulation proves that the new internally distributed CDM ESD protection concept is effective.

A simplified oscillator IC, as depicted in Figure 4-29, was designed and fabricated in a foundry 45nm SOI CMOS using the new internal-distributed CDM ESD protection method as a demo. The internally distributed CDM ESD protection net consists of simple

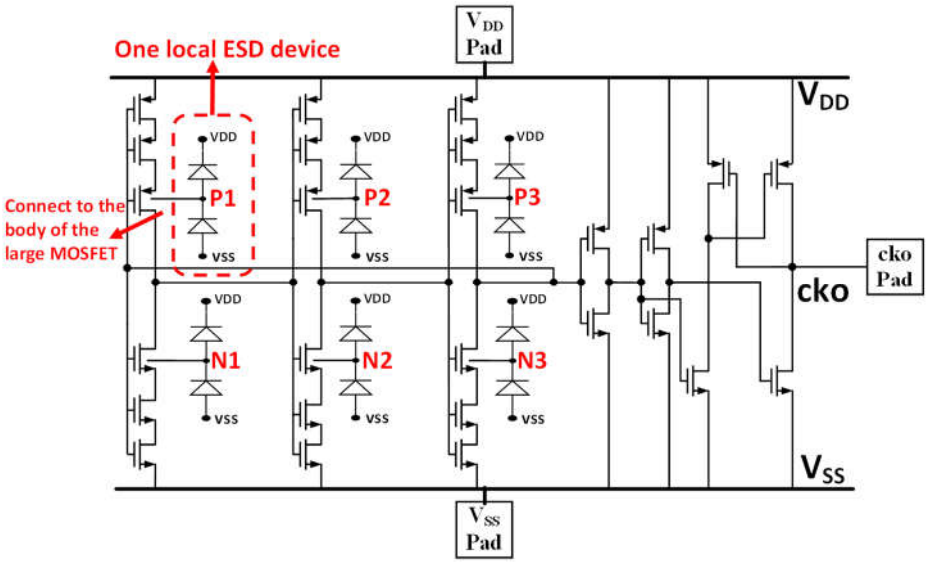



*Figure 4-29 Schematic for an oscillator demo IC featuring internal-distributed CDM ESD protection mesh and fabricated in a 45nm SOI CMOS.*

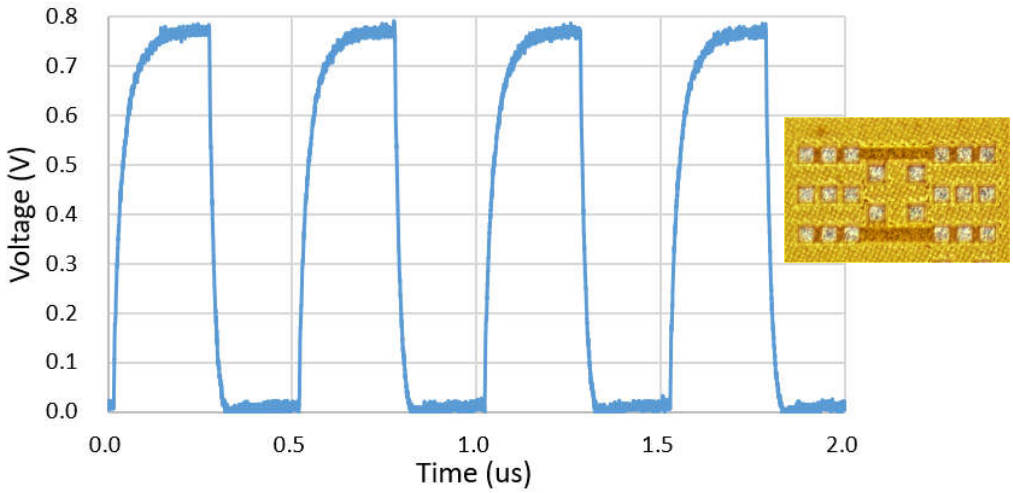



*Figure 4-30 Measured output waveform of the oscillator IC fabricated in a 45nm SOI.*

ESD protection diodes that are placed at the internal circuit nodes associated with the six large MOSFETs (P1, P2, P3, N1, N2 and N3), being the main local static charge storage bins reflecting internal charge distribution in real ICs. Figure 4-30 shows the measured output voltage waveform for the fabricated oscillator IC. Due to lack of commercial CDM ESD zapping tester in our lab, we chose to conduct VFTLP stressing test to evaluate CDM

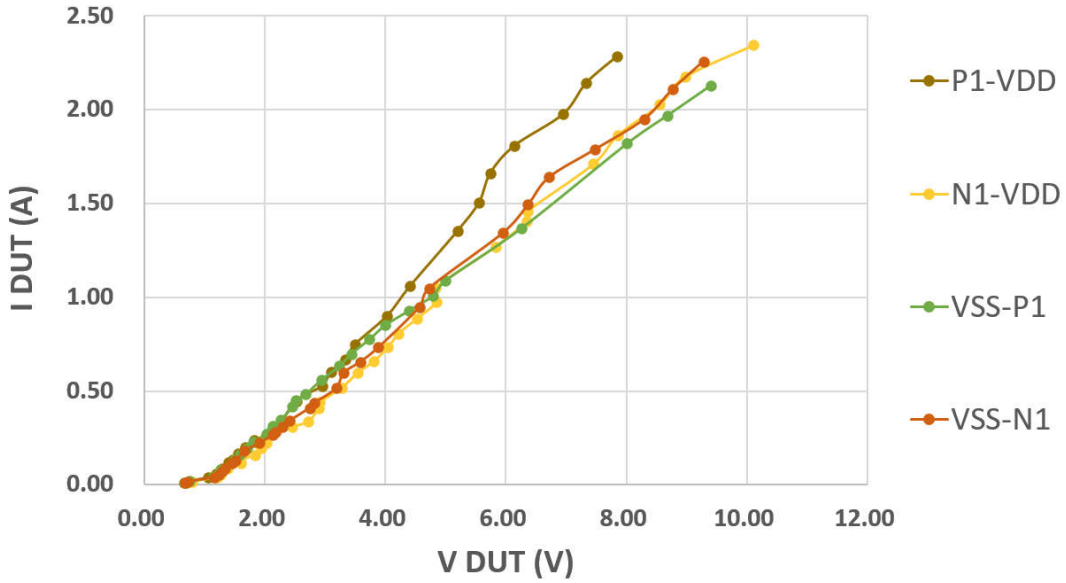



Figure 4-31 *Measured ESD discharge I-V curves for the IC with internally distributed CDM ESD protection mesh by applying VFTLP pulses to the internal nodes.*

ESD protection for the fabricated IC dies. The VFTLP tester used is Barth 4012 VFTLP+ model. During VFTLP testing, the GS probe was applied directly to the internal circuit nodes where the internal-distributed CDM ESD protection diodes are connected. Therefore, VFTLP testing can effectively and adequately check if the internal CDM ESD devices can respond to the ultrafast CDM ESD pulses and provide CDM ESD protection internally and locally. Figure 4-31 presents exemplar CDM ESD discharging I-V curves at various internal circuit nodes stressed by VFTLP pulse routines, which clearly shows that the internal-distributed CDM ESD protection didoes can effectively discharge the CDM ESD pulses in VFTLP test, to the CDM level of higher than $I_{t2}$~2A. The demo circuit, while simple, readily validated that the new internal-distributed CDM ESD protection method works in real Si, which will be further improved in our on-going designs.

### 4.2.2 Interposer Internal-Distributed ESD Protection

The new internal-distributed CDM ESD protection method can be realized in some novel ways for added benefits. Traditionally, on-chip ESD protection utilizes large co-planar ESD protection structures in a side-by-side manner, i.e., in-plane layout design with the core IC circuitry, which causes substantial ESD-induced design overhead (i.e., ESD-induced parasitic capacitance, leakage, and noises, as well as Si area consumed by large ESD protection devices and IC layout difficulty) [5, 13, 48]. In general, higher ESD protection robustness makes the ESD design overhead problem even worse. We recently devised two novel 3D ESD protection techniques, interposer ESD protection and TSV-based ESD protection [49] [50], which are utilized to further improve the new internal-distributed CDM ESD protection method.

In 3D IC packaging, an interposer is a separate Si substrate used to host complex metal interconnects to electrically connect multiple IC dies into a system-in-a-package (SiP). An

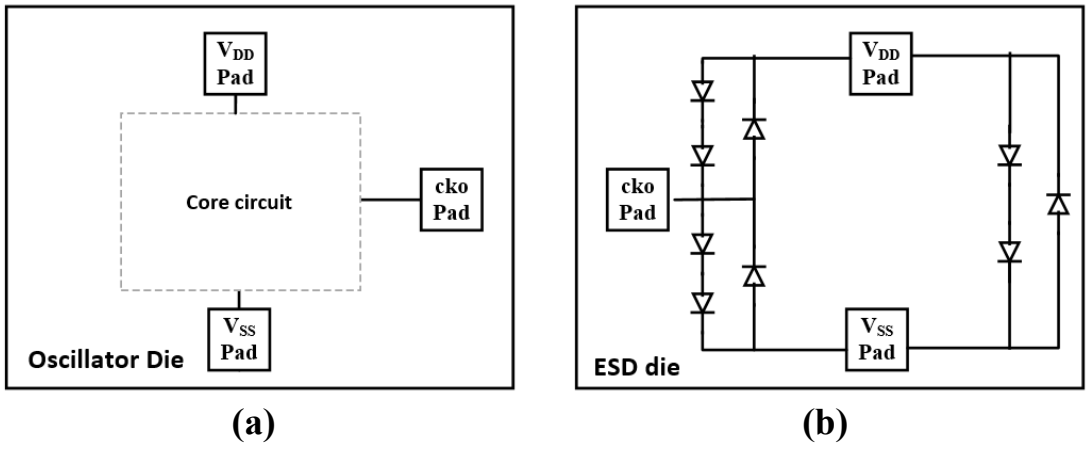



*Figure 4-32 Illustration of interposer-based internal-distributed CDM ESD protection solution utilizing two dies: (a) an active core IC die, and (b) a dedicated interposer CDM ESD protection die.*

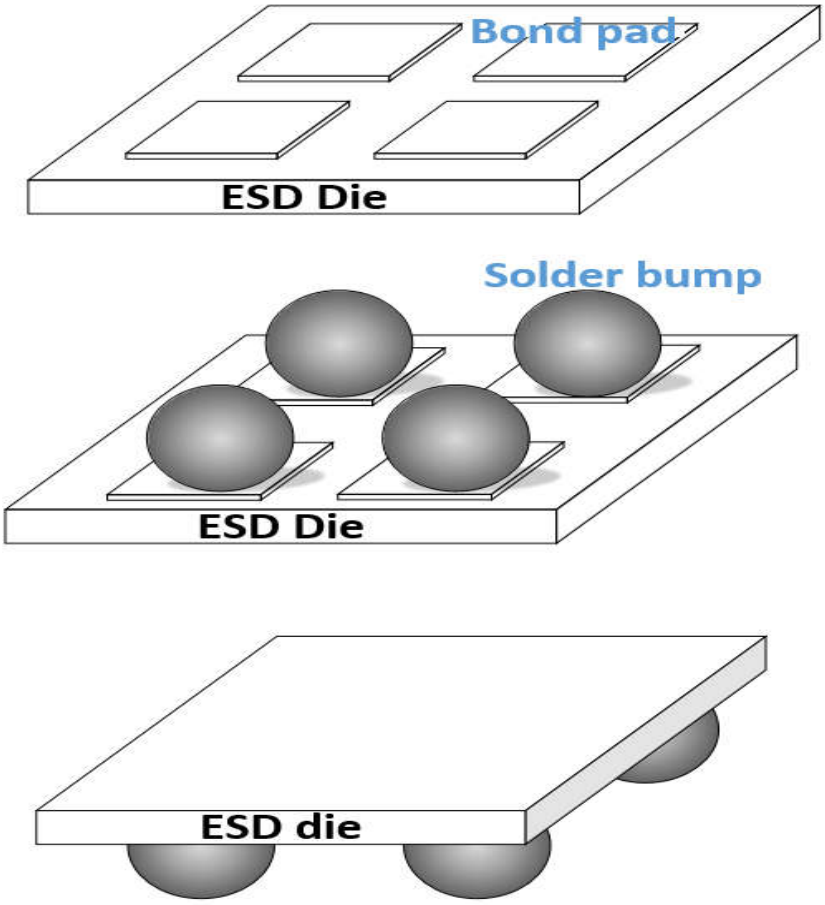



Figure 4-33 *Illustration of making an interposer-based CDM ESD protection using solder bumps for connection to an active IC core die.*

interposer-based ESD protection technique works as following: all large and troublesome ESD protection structures are removed from the IC die and are placed in a separate interposer Si substrate, resulting in one active die for the IC core only and an interposer die housing the complex ESD protection network as illustrated in Figure 4-32 for traditional pad-based ESD protection designs. The two dies are then interconnected vertically together for an ESD-protected chip, equivalent to the chip shown in Figure 4-26. Before processing the flip chips, solder bump must be carefully added onto the bond pads of interposer ESD die as shown in Figure 4-33. Solder bumps can be easily deposited on the bond pads during

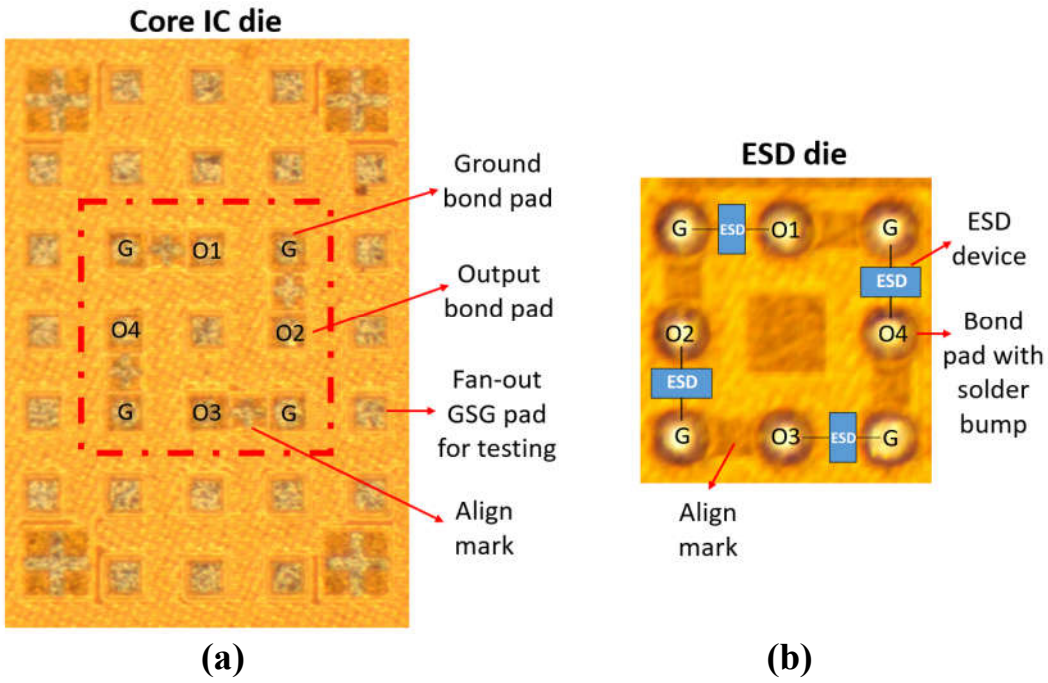



*Figure 4-34 Illustration of interposer-based internal-distributed CDM ESD protection solution utilizing two dies: (a) an active core IC die, and (b) a dedicated interposer CDM ESD protection die.*

foundry fabrication. Solder bumps have various functions: 1) to provide electrical connections for the two dies, 2) to provide thermal conduction for ESD-generated heat, and 3) to provide mechanical support to the flip-chips. The interposer ESD die is flipped over so that its bond pads face down, and are aligned with and bonded to the matching pads on the active IC die. the interposer ESD protection method was validated experimentally using a single-pole four-throw (SP4T) RF switch IC deigned and fabricated in a 45nm SOI, with the prototype dies shown in Figure 4-34. The no-ESD SP4T core circuit die has four outputs (O1, O2, O3 and O4) requiring ESD protection, which is provided by a separate interposer ESD die. The signal pads and ground pads (G, for GSG testing) are aligned in design for solder bump bonding following a flip-chip bonding process shown in Figure 4-35. The interposer ESD protection technique is perfectly suitable for the new internal-

distributed CDM ESD protection method for improved CDM ESD robustness. Using the oscillator IC shown in Figure 4-25 as an example, all internal-distributed anti-parallel ESD protection didoes originally embedded in the IC die are removed from the SP4T chip, making it an ESD-free active IC die only. These ESD protection didoes are designed into a separate interposer die dedicated to ESD protection that houses the required internal-distributed CDM ESD protection mesh network. The oscillator core die is modified to have the selected internal nodes (P1, P2, P3, N1, N2 & N3) ready for ball bonding with the interposer CDM ESD protection die, using small internal "pads" according to the solder

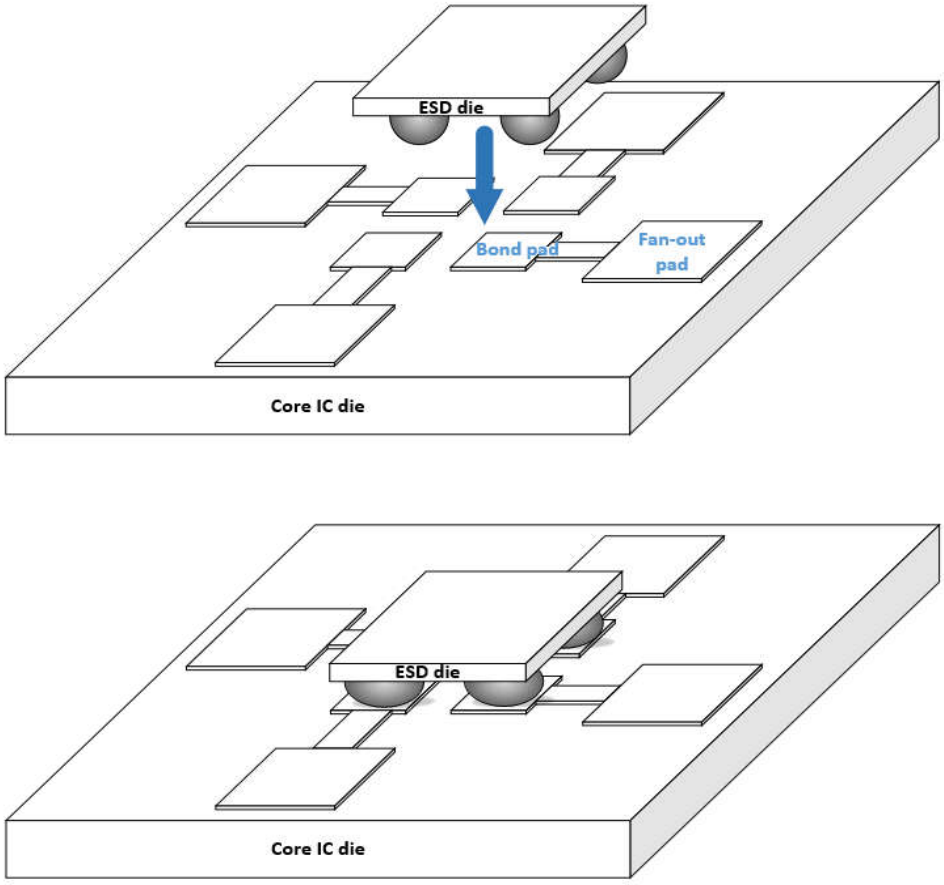



Figure 4-35 *A SiP process flow for a SP4T RF switch IC utilizing interposer-based internal-distributed CDM ESD protection, featuring bump bonding.*

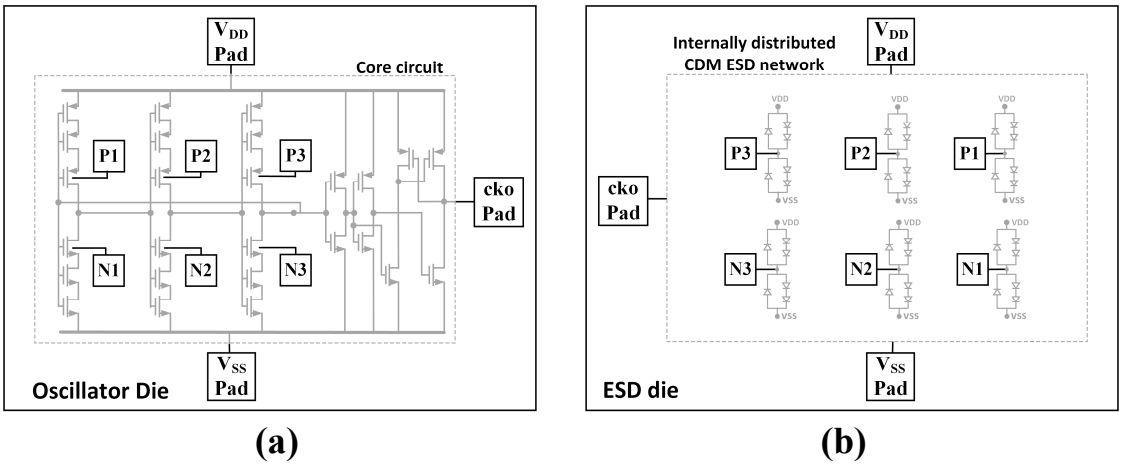



*Figure 4-36 Illustration of a two-die interposer-based internal-distributed CDM ESD protection design for an exemplar oscillator IC in 45nm SOI: (a) active oscillator core IC die, and (b) interposer CDM ESD protection die for internal-distributed CDM ESD protection.*

bumps used. The two- die design is illustrated in Figure 4-36 for the no-ESD core die and dedicated interposer CDM ESD protection die. The two dies are bonded together through 3D heterogeneous integration to deliver the full ESD-protected oscillator IC with internal-distributed CDM ESD protection. Compared to realizing internal-distributed CDM ESD protection using conventional in-plane side-by-side ESD protection devices, the flip-chip interposer-based internally distributed CDM ESD protection method offers many benefits: 1) Because the ESD protection devices are "taken out" of the core circuit die, the area budget can be greatly reduced which is vitally important to complex chips. 2) Correspondingly, the ESD-induced parasitic capacitance, leakage and noises can be significantly minimized. 3) With the entire ESD protection network in a separate interposer ESD die, smart partitioning will allow a more widely distributed CDM ESD protection mesh network that will further improve full-chip CDM ESD protection capability while using smaller-sized ESD protection devices. 4) Obviously, the solder bumps also serve to

dissipate ESD-induced heat more efficiently. 5) The interposer CDM ESD protection die can be readily replaced, hence substantially mitigate the product costs possibly caused by the unavoidable CDM ESD failures. 6) The flip chip process is a very mature 3D heterogeneous integration technology. In short, the benefit of using dedicated interposer-based internal-distributed CDM ESD protection technology is potentially significant. Clearly, the interposer-based internally distributed CDM ESD protection scheme theoretically does no consume any Si area on an IC die.

### 4.2.3 TSV-Based Internal-Distributed ESD Protection

Another alternative solution to the traditional in-plane side-by-side ESD protection method is to use in-hole (TSV like) vertical ESD protection structure. In principle, a deep TSV-type hole can be etched into a Si substrate that houses a truly vertical ESD protection diode. Unlike conventional in-plane planar ESD protection structures that require careful lateral electrical connection (metals or diffusion regions), an in-TSV ESD protection diode has one terminal connected to an overhead pad and the other electrode vertically and directly connected to a local GND to the backside of the substrate. The innovative in-TSV ESD protection diode concept is depicted in Figure 4-37 and recently validated

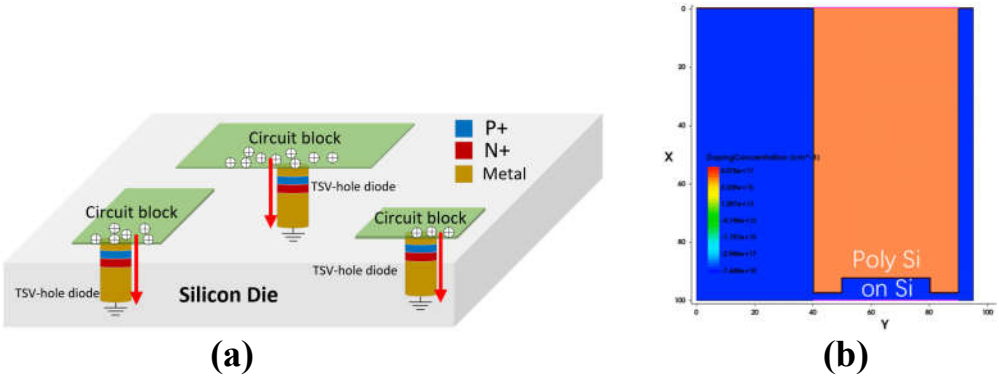



*Figure 4-37 Concept of the new in-TSV ESD protection diode for distributed ESD protection: (a) concept view, and (b) cross-sectional view by TCAD.*

experimentally where a vertical poly-Si PN junction ESD protection diode is formed inside a deep TSV hole in CMOS [40]. From Figure 4-37a, it is obvious that the novel in-TSV ESD protection diodes can be utilized to construct the new internal-distributed CDM ESD protection mesh network in CMOS ICs. Compared to the internal-distributed CDM ESD protection scheme using traditional in-plane side-by-side planar ESD protection devices, the in-TSV type internally distributed CDM ESD protection design offers several key advantages: First, it dramatically reduces the Si area consumed by ESD protection devices and their lateral diffusion interconnects, ideally zero extra die area needed because an in-TSV ESD protection diode is placed under the active IC die. Second, it is very layout-friendly due to its true 3D structural nature. Third, since an in-TSV ESD protection diode can be readily placed locally under any transistor on a die, it allows great freedom to construct a comprehensive internal-distributed CDM ESD protection mesh on an IC die. Fourth, the local and vertical interconnects to in-TSV ESD protection diodes can significantly improve ESD discharging efficient that also helps to minimize ESD heating. Fifth, the local vertical metal pillar serves to dissipate any ESD-generated heat efficiently. In summary, the new in-TSV based internal-distributed CDM ESD protection scheme is a very efficient full-chip CDM ESD protection technology.

The concept of in-TSV ESD protection structure is validated experimentally using a new CMOS-compatible process in our cleanroom facility, which can be readily transferred to foundry processes. Referring to Figure 4-37, the process starts creating a deep TSV-like hole (not a through-substrate hole as a TSV though) in a Si substrate. To etch a high aspect ratio in-TSV hole in our cleanroom with limited processing tools, we developed a unique

process module to first etch a 100µm-deep ring into Si wafer, which is followed by thermal oxidation to form a $SiO_2$ layer covering the inner wall of the deep hole. Next, a center Si pillar (heavy P-doped) inside the TSV-like hole was created by deep reactive ion etch (RIE). A poly-Si layer (ideally, single-crystal Si is preferred) was then deposited on top of the p-type center Si pillar inside the deep hole, which was then N-doped by ion implantation. A vertical poly-Si PN junction ESD protection diode was finally created inside the TSV hole that is connected by metals (TSV metal pillar) for testing. While the fabrication process seems to be a little involving due to our cleanroom facility limitation, such in-TSV ESD protection didoes can be easily made in any foundry CMOS flows. Due to our process limitation in high aspect-ratio etching, the prototype device has a diameter of 400µm inside a TSV hole of 100µm deep, shown in Figure 4-38. To characterize CDM ESD protection

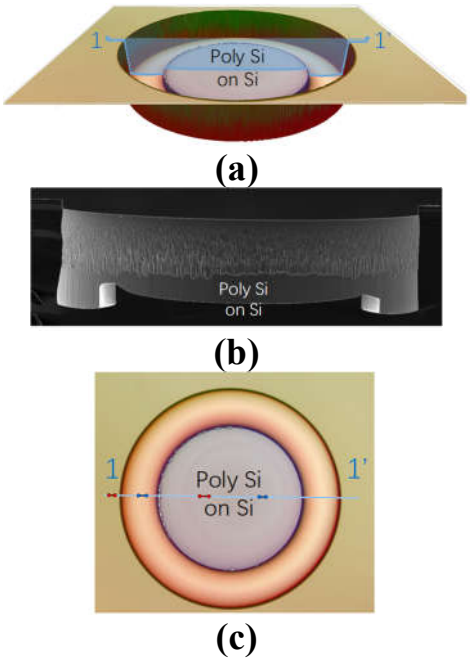



*Figure 4-41 Images for prototype in-TSV poly-Si/Si PN diode ESD protection diode fabricated inside a 100µm deep TSV hole: (a) a 3D image by confocal microscope, (b) a cross-section view along 1-1' cutline of the PN diode by SEM, and (c) a top view of in-hole ESD diodes by optical microscope along 1-1' cutline.*

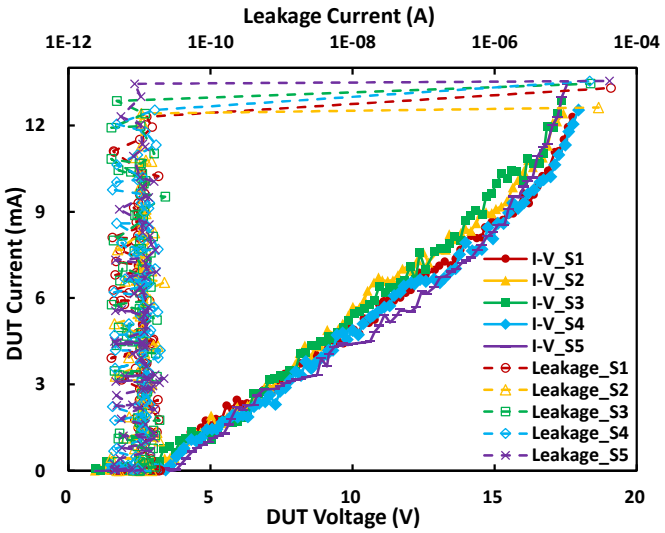



*Figure 4-45 TLP-measured transient ESD discharging I-V curves for prototype in-TSV ESD diodes confirm the ESD protection function and low ESD-induced leakage.*

function of the prototype vertical in-TSV ESD didoes, VFTLP test should be used for CDM ESD test. However, it is extremely difficult to add GS (ground-signal) pads, required for VFTLP testing, on the demo device due to our cleanroom limitation. Instead, the fabricated in-TSV ESD protection diode samples were characterized by TLP testing (Barth 4002 TLP tester) to prove that the new vertical TSV-like ESD diode structure works for ESD protection. Figure 4-39 depicts the TLP-measured transient ESD discharging I-V curves for prototype in-TSV ESD protection diodes, which clearly demonstrate the expected ESD discharging I-V characteristics and very low leakage. The multiple-sample testing results obtained also serve to show the desired function uniformity and stability of the prototype vertical in-TSV ESD protection didoes. The extracted ESD triggering voltage is $V_{t1} \sim 2.0V$ and the ESD thermal breakdown current is $I_{t2} \sim 13mA$ for the poly-Si diode prototypes. In terms of device construction, PN junction creation, impurity doping, and metal interconnects, the prototype in-TSV ESD protection diode fabricated in our cleanroom are yet to be optimized. The prototype devices are for proof of concept purpose only.

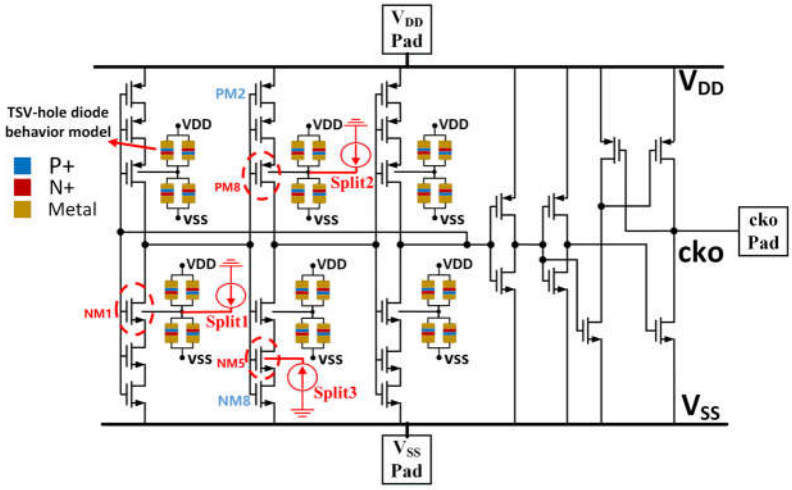



*Figure 4-49 A 3-stage oscillator IC designed in 45nm SOI with TSV-based internally distributed CDM ESD network.*

The new TSV-based internally distributed CDM ESD protection technique was also verified by chip-level ESD simulation using the same oscillator IC described preciously. Considering that the in-TSV ESD diode prototypes were made in our cleanroom facility, not available in any commercial foundries yet, the validation was conducted by CDM ESD simulation similar to the procedures discussed earlier. Figure 4-40 shows the schematic for the 3-stage oscillator IC designed in a 45nm SOI CMOS where the internal-distributed CDM ESD protection mesh network was formed by in-TSV ESD protection diodes. Similarly, the in-TSV ESD protection diodes are connected between the internal/local nodes and local GND to emulate the function of the in-TSV ESD protection diodes. Per smart partitioning, the concerned internal nodes are NM1, NM2, NM3, PM7, PM8 and PM9, which are considered to be the main internal charge storage bins. ESD protection device behavioral models were developed for the prototype in-TSV ESD diodes fabricated. For meaningful full-chip CDM ESD simulation, larger in-TSV ESD protection diodes of about 500 times of the prototype fabricated were used in chip-level CDM ESD simulation

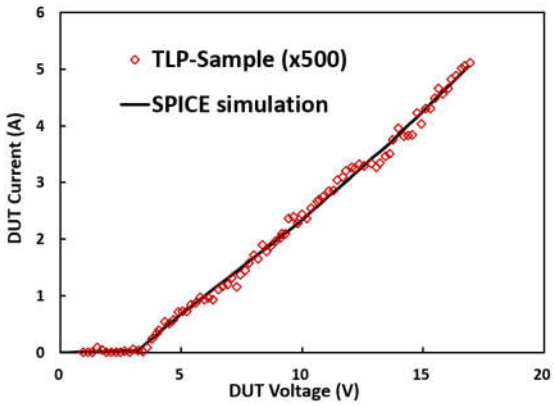
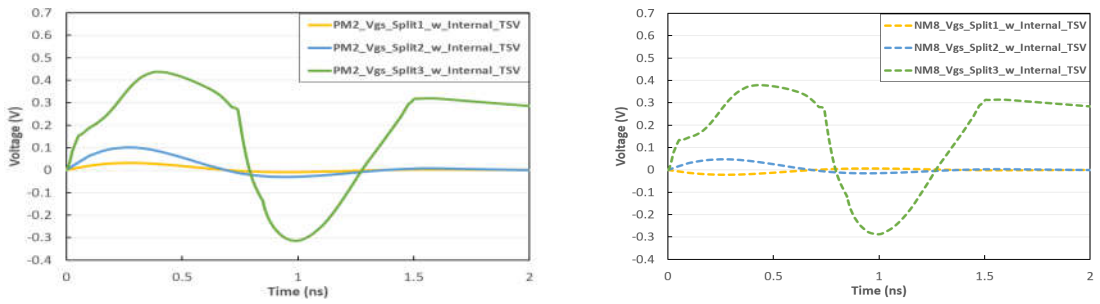



*Figure 4-53 An exemplar TSV-like ESD protection diode of practical size is created using the diode behavioral model extracted from TLP testing for the prototype in-TSV ESD protection diode fabricated.*

utilizing the ESD diode behavioral models extracted as shown in Figure 4-41. Chip-level CDM ESD protection simulation was conducted for the oscillator IC with three splits similar to that discussed before, i.e., modeling the CDM ESD discharging initiated by internal charges stored at NM1 (Split-1), PM8 (Split-2) and NM5 (Split-3), which are discharged against the grounded $V_{DD}$ pad as shown in Figure 4-40. Figure 4-42 presents the transient CDM discharging voltage waveforms by SPICE for the exemplar MOSFET PM2 and NM8 under CDM ESD zapping of pulse strength equivalent to 50V CDM ESD stressing at pads, ~2% of the pulse when zapping internally. Compared with the results




**(a)** **(b)**

*Figure 4-57 Exemplary transient voltage analysis for VGS of PM2 and NM8 of the ICs using TSV-based internal-distributed CDM ESD protection network under equivalent 50V CDM ESD zapping: (a) gate breakdown failures occur in the IC using classic pad-based CDM ESD protection network, and (b) the IC using the new internal-distributed CDM ESD protection mesh passed CDM ESD zapping.*

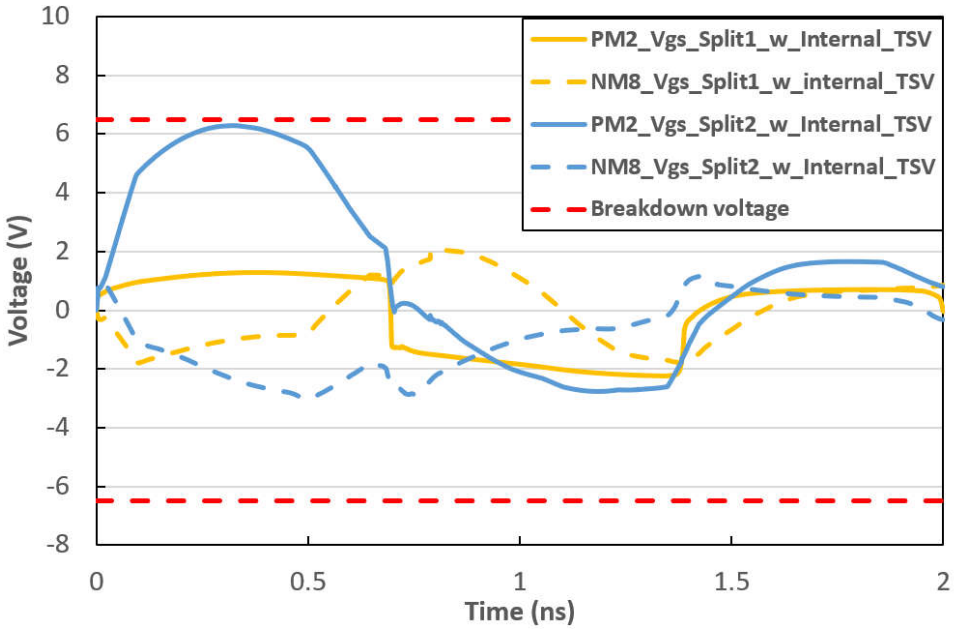



*Figure 4-61 Exemplary transient voltage analysis for VGS of PM2 and NM8 of the ICs using TSV-based internal-distributed CDM ESD protection network passes 350V CDM ESD zapping without gate voltage breakdown failure.*

shown in Figure 4-27, the IC die using the TSV-based internally distributed CDM ESD protection network passed equivalent 50V CDM zapping without any gate breakdown failure. The CDM ESD zapping level was then increased to evaluate the CDM ESD protection potential, which indicates that the chip can sustain ~350V CDM ESD zapping without reaching to $BV_{OX}$~6.5V in 45nm SOI CMOS as depicted in Figure 4-43. It is worth-noting that, while the TSV-based internally distributed CDM ESD protection is partially validated experimentally, the new technology is still in its infancy and significant research in currently on-going to better understand its mechanisms and improve its performance. Obviously, the TSV-based internally distributed CDM ESD protection design can dramatically reduce the die area normally consumed by ESD protection structures.

In summary, Chapter 4.2 reports a comprehensive study of a novel non-pad-based internally distributed CDM ESD protection technique, which aims to overcome the design uncertainties in full-chip CDM ESD protection designs associated with the faulty traditional pad-based CDM ESD protection methods. Further improvements can be achieved by using novel interposer or TSV-like ESD protection structures to form the internal-distributed CDM ESD protection mesh network. The internally distributed CDM ESD protection concept is validated by both ESD simulation and partial experiments with prototype IC designed in 45nm SOI CMOS. The novel internally distributed CDM ESD protection method, especially in interposer and TSV formats, can dramatically reduce the die area normally consumed by large pad-based ESD protection structures, hence, partially resolving the ESD-induced design overhead problem. The actual benefit of layout reduction for a chip is entirely depending on a specific IC design. The new CDM ESD protection technique has the potential to provide robust on-chip CDM ESD protection for complex ICs in advanced technologies.

# Chapter 5 Mixed-Mode Multiple-Stimuli ESD Simulation

Electrostatic discharge (ESD) protection is a grand design challenge for complex ICs in advanced technologies. ESD simulation is indispensable to guide ESD protection designs. However, no existing ESD simulation methods may accurately predict ESD protection designs in a universal manner due to various inherent limitations. TCAD-based ESD simulation is very useful for ESD protection designs. Transmission line pulse (TLP) and very fast TLP (VFTLP) are widely used to evaluate human body model (HBM) and charged device model (CDM) ESD protection designs, which provide rich details for calibrating TCAD ESD simulation for design prediction and validation. Using various ESD protection devices fabricated in 28nm CMOS and 45nm SOI CMOS technologies, a comprehensive experimental and simulation study finds that the ESD stimuli used in TCAD ESD design simulation have profound impacts on many subtle ESD protection behaviors, particularly in comparison with ESD testing. Chapter 5 cautions against over-interpretation of TCAD ESD simulation results, obtained using any specific ESD stimulus, attempting to accurately predict practical ESD protection designs. A mixed-mode multiple-stimuli ESD simulation method is therefore developed to address the ESD stimulus induced ESD performance variation, hence offering a technique to achieve ESD protection design prediction.

On-chip electrostatic discharge (ESD) protection is required for ICs against ESD failures. On-chip ESD protection design becomes very challenging for high-performance and complex chips fabricated at advanced technology nodes [5, 13, 39, 51, 52]. Full-chip ESD protection design verification and prediction are the ultimate goal in practical ESD

protection designs, which can only be achieved by careful ESD CAD simulation. These days, TCAD-based ESD simulation design method has been commonly used for ESD design optimization [51]. One critical decision to make in conducting TCAD ESD design simulation is to decide what input ESD stimulus to use to ensure accurate simulation of real-world ESD stressing events at chip level in order to avoid the possible "junk-in, junk-out" situation. Typically, a transient human body model (HBM) or charged device model (CDM) ESD waveform specified in selected ESD testing standards, or similarly, a fast square waveform produced by a transmission line pulse (TLP) or very fast TLP (VFTLP) ESD tester, is used as the input ESD zapping stimulus for TCAD ESD simulation [39, 51, 52]. However, several major unanswered problems exist in TCAD ESD simulation that can seriously affect the ESD simulation accuracy. First, the HBM and TLP ESD test set-ups are not identical to each other, and the same applies to CDM and VFTLP testers. While an HBM or CDM ESD event models the real-world ESD phenomenon, the corresponding TLP or VFTLP testing is merely an emulation of the real-world HBM or CDM ESD event, respectively. Accurate correlation between HBM ESD zapping and TLP ESD testing is still debatable today, which is even more true for the CDM and VFTLP measurement pair. Second, TLP or VFTLP testing utilizes a square waveform pulse train, not one simple square waveform similar to the corresponding single HBM or CDM waveform in real world. Hence, using a TLP or VFTLP square waveform pulse train inherently introduces errors in TCAD ESD simulation to model actual single-wave HBM or CDM ESD zapping test. On the other hand, using single-pulse TLP or VFTLP waveform in ESD simulation to model the TLP or VFTLP testing procedures also has fundamental uncertainty. Therefore,

while HBM or CDM zapping is always required to evaluate ESD protection level and the corresponding TLP or VFTLP testing reveals rich transient ESD discharge details for HBM or CDM ESD protection designs, what would be the trustable TCAD ESD simulation procedure, particularly in terms of the ESD stimuli used, that can correlate HBM zapping with TLP stressing, or CDM with VFTLP ESD testing, respectively, hence accurately predicting ESD protection designs in Si? This paper, extended from a conference report [53], provides a thorough analysis of various TCAD ESD simulation scenarios using both real-world HBM and CDM ESD waveforms, and their corresponding TLP and VFTLP square waveforms, in both single-pulse and pulse train manners, as stimuli. It concludes that TCAD ESD simulation using either HBM (or CDM waveform), or the corresponding TLP (or VFTLP) pulse stimulus, alone, is insufficient in achieving ESD simulation accuracy. The paper introduces a new mixed-mode TCAD ESD simulation flow using combined HBM-TLP stimuli, or CDM-VFTLP stimuli, to enable ESD protection design prediction and verification.

## 5.1 HBM and CDM ESD Zapping

The HBM ESD test model describes the human body induced ESD phenomena where electrostatic charges stored in a human body will discharge into an IC affected, resulting in HBM ESD failures. Figure 5-1 depicts the original HBM ESD zapping waveform [6]. The key parameters for the standard HBM ESD waveform include the pulse rising time of $t_r$ ~10ns and decay time (duration) of $t_d$ ~ 150ns (± 20ns).

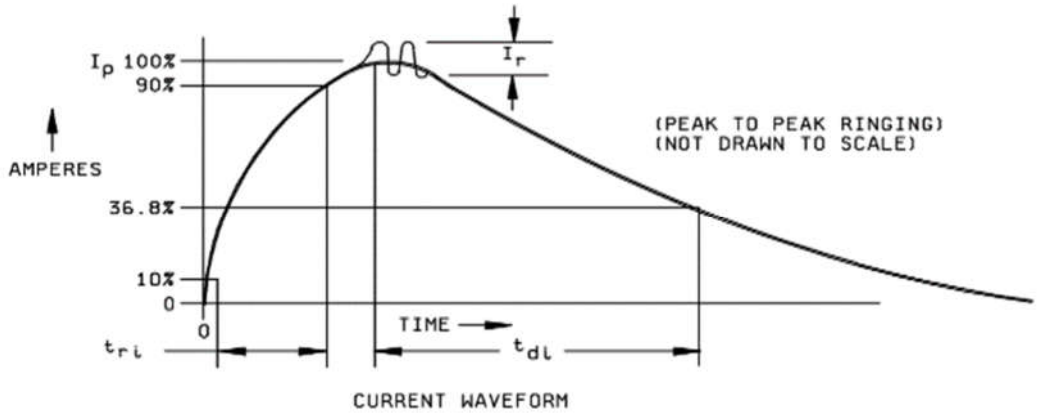



*Figure 5-1 The classic HBM ESD waveform [7].*

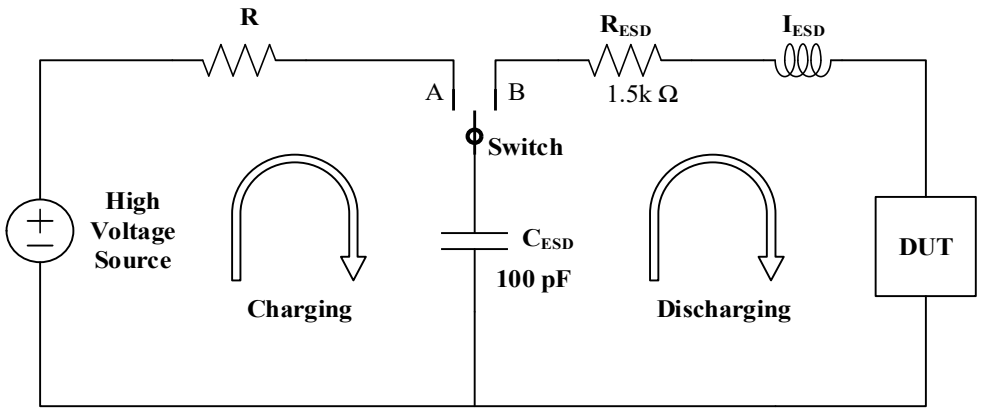



*Figure 5-2 An equivalent circuit model for a standard HBM ESD tester including the charging and discharging procedures.*

Figure 5-2 illustrates the equivalent circuit model for a standard HBM ESD tester where the capacitor $C_{ESD}$ of 100 pF models a human body that is pre-charged. When touching a device under test (DUT), the electrostatic charges stored will be discharged into DUT through a human body resistor of $R_{ESD}$ ~ 1500Ω and a parasitic inductor of $L_{ESD}$. The amplitude of the ESD pulse produced by an HBM ESD tester varies. For example, the peak transient current flowing into the DUT through the $R_{ESD}$ of 1500Ω will be about 0.66A when $C_{ESD}$ is pre-charged to 1KV. The HBM ESD discharge pulses can be considered as RC exponentially decaying waveforms.

CDM ESD phenomenon is completely different from HBM ESD events. HBM ESD is fundamentally a "from-external-to-internal" discharging event in nature, while CDM ESD describes a "from-internal-to-external" discharging phenomenon [47]. During a CDM ESD event, an IC is pre-charged, unavoidably and throughout its lifetime, and the electrostatic charges are distributed inside the chip. As such, when the IC is grounded (e.g., placed onto a PCB board), the charges stored inside the chip will be discharged into a ground, causing internal CDM ESD damages. Therefore, a CDM ESD failure is internal-oriented, while an HBM ESD damage is external-initiated. Figure 5-3 illustrates different CDM ESD charging and discharging scenarios including triboelectric charging and field induction CDM event (FICDM) [9]. Compared to HBM ESD model, the CDM ESD pulse is very short (full width at half maximum, or, FWHM = 250~600ps) and rises extremely fast ($t_r$ <250ps), as depicted in Figure 5-4 [9].

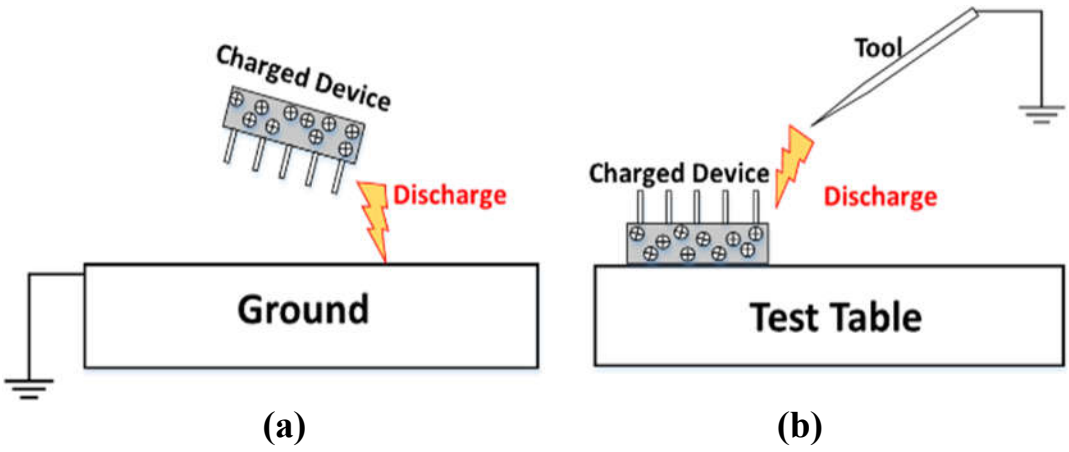



*Figure 5-3 Different real-world CDM ESD charging and discharging scenarios: (a) triboelectric-induced electrostatic charges accumulated inside a chip will be discharged when the IC is grounded, resulting in CDM ESD failures, and (b) a FICDM ESD testing model induces electrostatic charges into an IC and CDM discharging is initiated by contacting IC pin using a pogo pin. [9]*

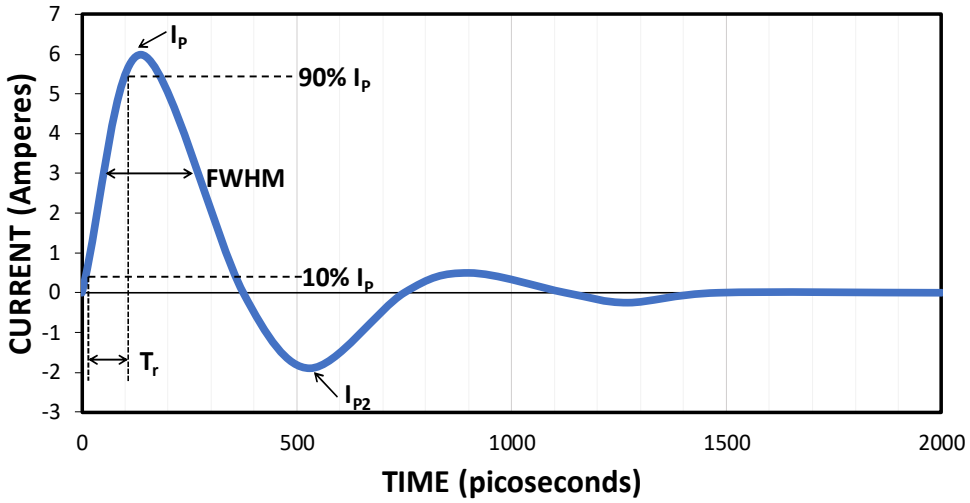



*Figure 5-4 A typical CDM ESD discharging waveform [9].*

Before and after each HBM or CDM ESD zapping test, a DUT is characterized for its general functional Specs, commonly using DC testing for its leakage current ($I_{leak}$), and the Specs degradation is monitored as ESD failure criteria. For example, if $I_{leak}$ increases by orders of magnitude after HBM or CDM ESD zapping, an IC is considered failed the ESD testing, typically giving a voltage level ($V_{t2}$) in KV or a thermal breakdown current level of $I_{t2}$. HBM or CDM ESD testing is destructive and does not provide useful transient ESD details; on the other hand, TLP or VFTLP testing is generally non-destructive and delivers instantaneous ESD discharging I-V-t characteristics that provide rich information for ESD CAD simulation calibration and design optimization.

## 5.2 TLP and VFTLP ESD Testing

TLP or VFTLP ESD testing is an alternative to the fail-or-pass HBM or CDM zapping method[10]. For industrial standard TLP testing shown in Figure 5-5, a transmission line

is pre-charged and then discharges into DUT. A TLP tester produces a well-defined, well-controlled square waveform pulse with $t_r$ and $t_d$ related to an HBM ESD waveform as in Figure 5-6. To make the TLP pulses and HBM ESD waveforms equivalent in terms of the transient ESD behaviors and the energy involved, a TLP tester typically sets $t_r$ = 10ns and $t_d$ = 100ns. TLP testing is generally non-destructive because the pulse can be well-controlled. During TLP testing, a series of square waveforms (i.e., a pulse train) are produced to stress the DUT with the pulse height starting very low and increasing gradually

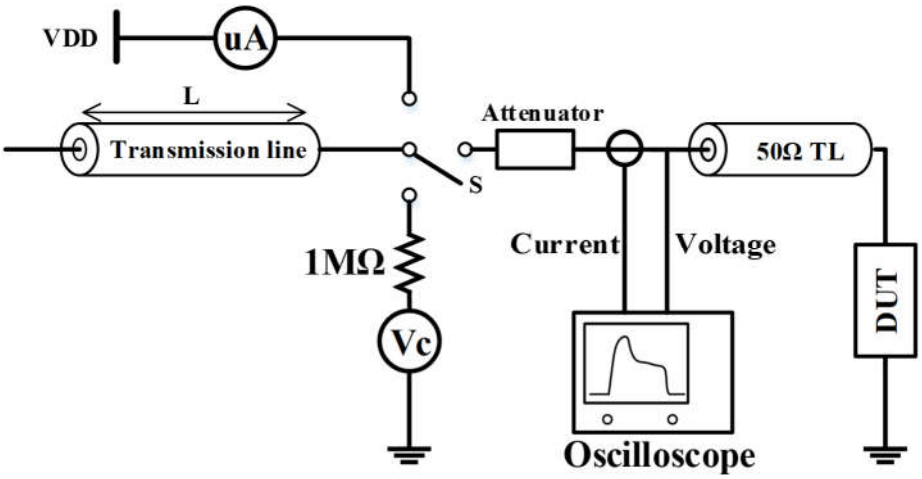



*Figure 5-5 An equivalent circuit model for TLP tester.*

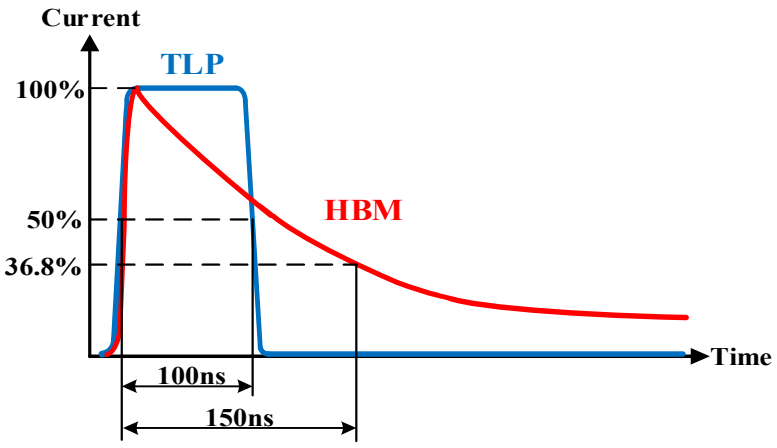



*Figure 5-6 Correlating TLP and HBM waveforms in terms of the pulse rise time and the energy involved.*

at a selected voltage step. After each stressing TLP pulse, the current and voltage of the DUT will be obtained, and the $I_{leak}$ of DUT will be monitored. When an TLP pulse reaches to certain high level, ESD failure will occur, which typically corresponds to an abrupt jump in the DUT leakage. Figure 5-7 depicts conceptually the whole TLP stressing flow. After each TLP pulse stress, the oscilloscope captures the voltage and current of the DUT, hence producing an instantaneous ESD discharging I-V curve for the DUT under TLP ESD stressing, which provides details for TCAD ESD simulation calibration. The observed I and V waveforms for DUT during TLP stressing contain both incident and reflected waves that are superimposed after a time delay, hence resulting in varying shapes in the I and V waveforms monitored as depicted in Figure 5-7. Since the actual waveform shapes (i.e., the top) of the current and voltage waves captured by the oscilloscope are not flat, a TLP tester is designed to take the average I and V values by integrating the observed I and V

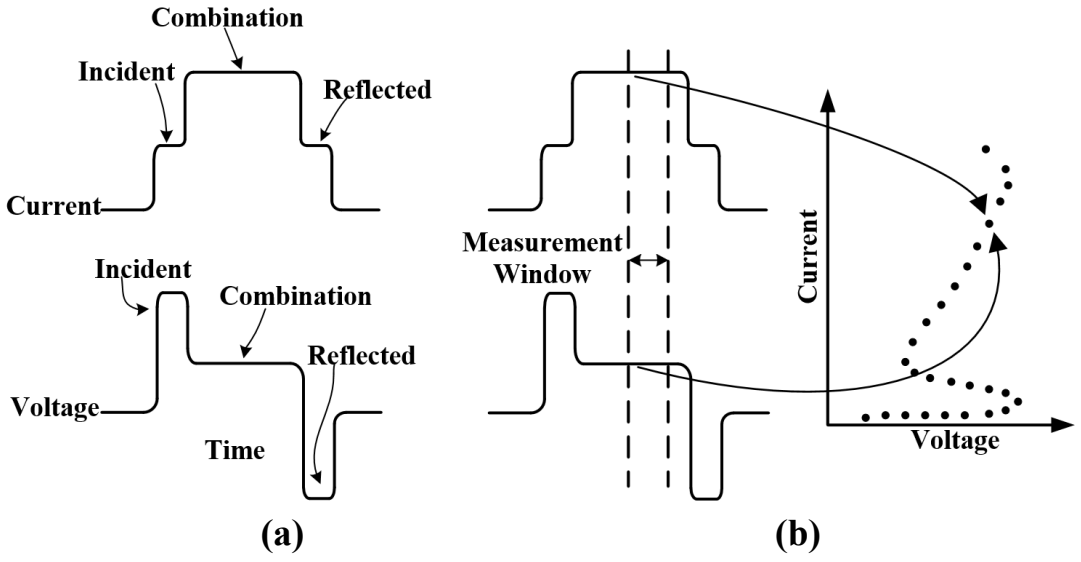



*Figure 5-7 Illustration of standard TLP testing procedure shows incident and reflected I and V waveforms, as well as the combined I and V waves across DUT: (a) incident and reflected pulses, and (b) superimposed I and V waves and the instantaneous ESD discharging I-V curve obtained.*

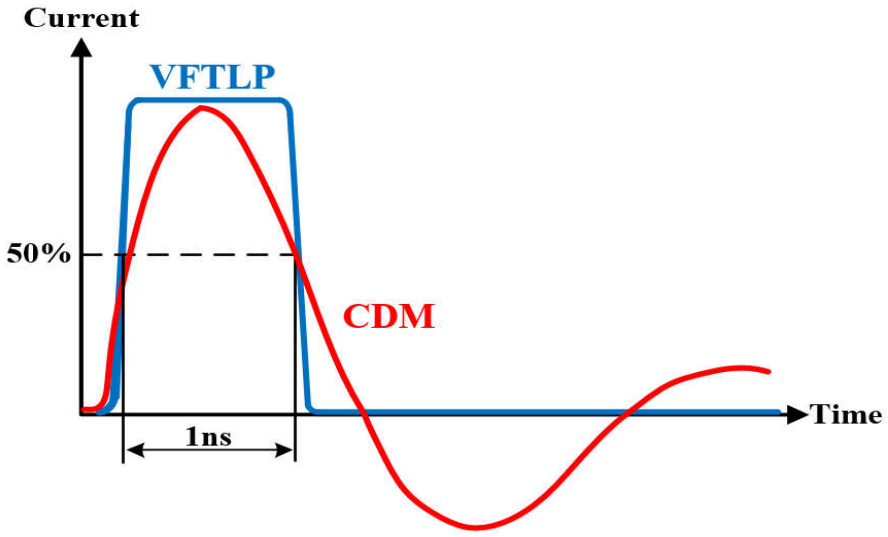



*Figure 5-8 Correlating VFTLP and CDM waveforms.*

waves within a small pulse window (typically 70% - 90%) in time domain as indicated by the vertical dash-lined segment in Figure 5-7b. The similar testing procedure applies to VFTLP ESD stressing measurement for CDM ESD characterization where the key difference is that a VFTLP pulse is ultrafast ($t_r$~0.1ns) and very short ($t_d$~1ns), which is illustrated in Figure 5-8.

In this work, the TLP tester used is Barth 4002 TLP model and the VFTLP tester used is Barth 4012 VFTLP+ model.

## 5.3 Mixed-Mode Multi-Stimuli TCAD ESD Simulation

A. HBM and VFTLP ESD Simulation

Impacts of HBM and TLP ESD input stimuli on TCAD ESD simulation was studied using several ESD protection structures. Figure 5-9 shows a shallow-trench-isolated (STI) ESD protection diode and a silicon-controlled rectifier (SCR) ESD protection device

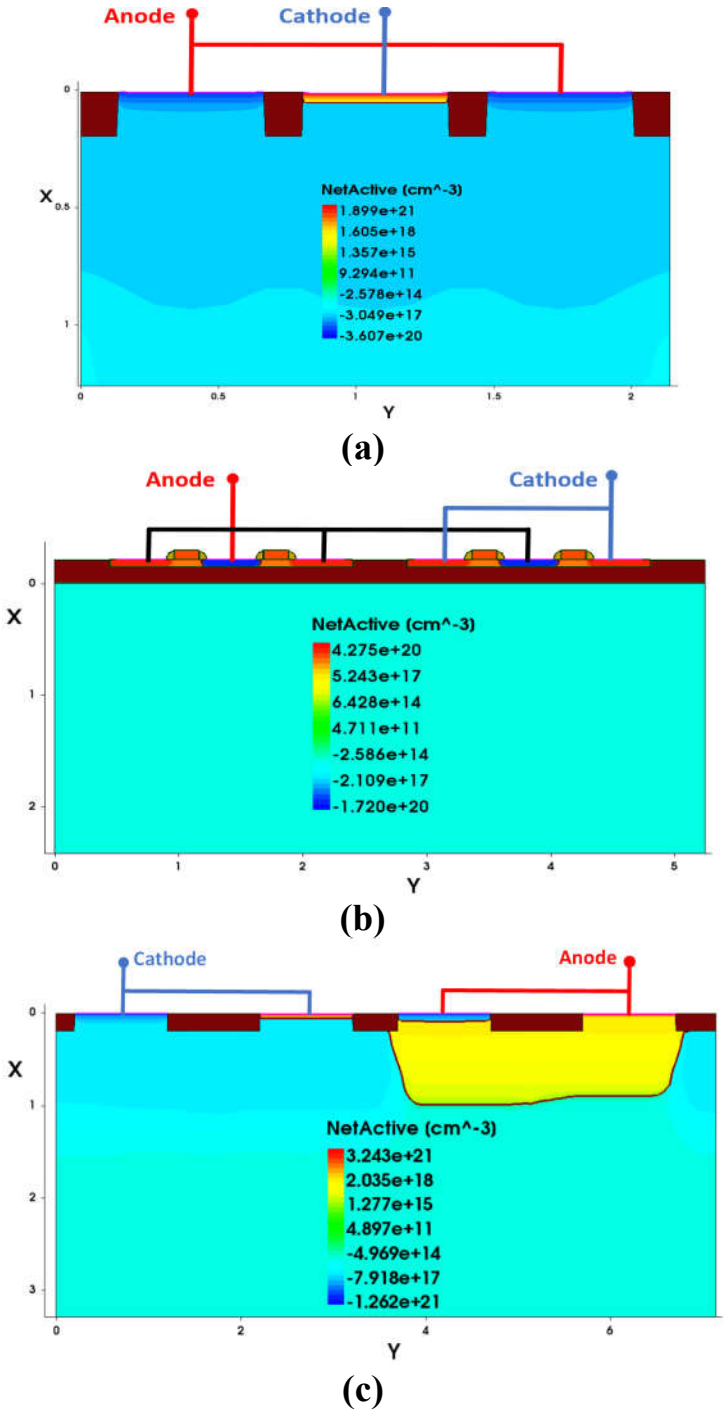



*Figure 5-9 Cross-section views for the ESD protection structures in this work by TCAD: (a) a STI ESD protection diode, (b) a diode-string ESD protection structure, and (c) a SCR ESD protection structure.*

fabricated in 28nm bulk CMOS, and a diode-string ESD protection structure fabricated in 45nm SOI CMOS. These ESD protection devices were designed using TCAD ESD simulation.

These fabricated ESD protection devices were characterized using a TLP tester, which was compared with TCAD ESD simulation using different ESD stimuli. For comprehensive and fair comparison, mixed-mode TCAD ESD simulation for these ESD protection devices were conducted using three different ESD input waveforms as depicted in Figure 5-10: a single-pulse TLP square waveform, a single-pulse HBM waveform (real-world ESD pulse) and a square-waveform TLP pulse train (used in standard TLP testers). The single-pulse HBM ESD waveform corresponds to real-world HBM zapping event and the TLP pulse train models the industrial standard TLP tester. For typical HBM ESD zapping, a 1KV HBM ESD pulse delivers a peak ESD current of $I_{peak}$~0.66A and a 2KV

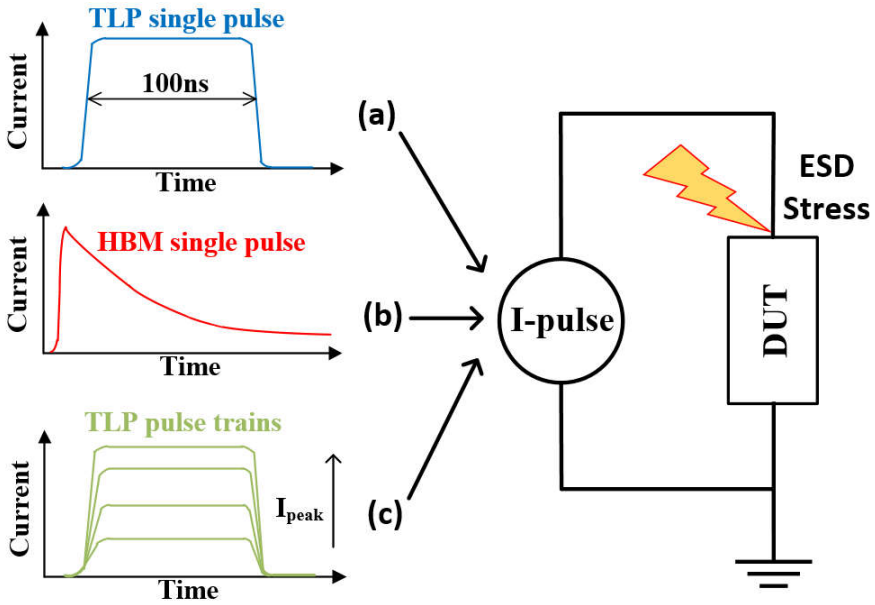
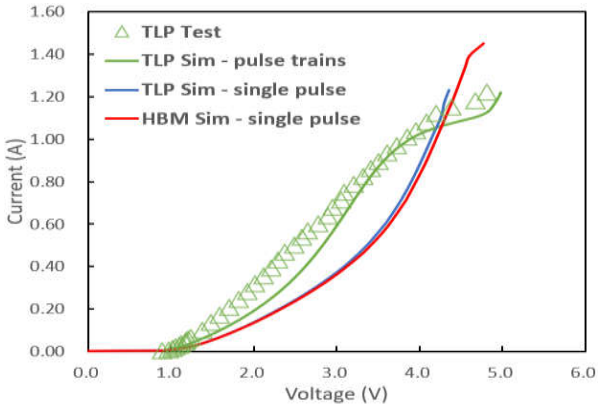
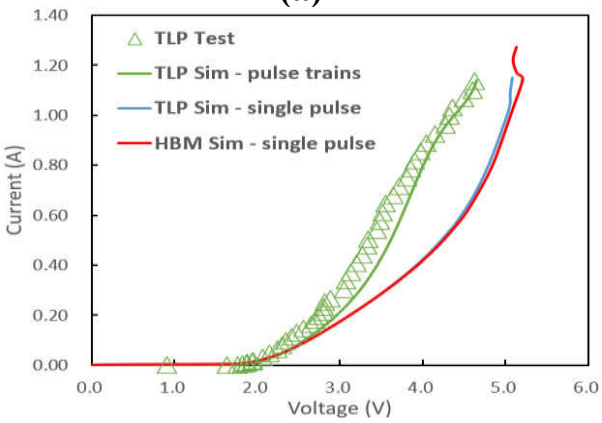


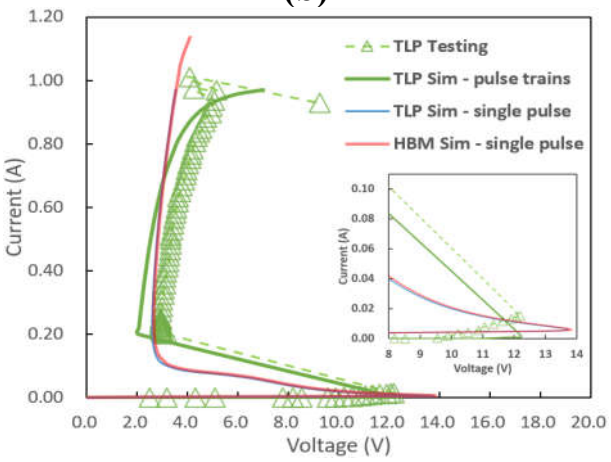

*Figure 5-10 New mixed-mode multi-stimuli TCAD ESD simulation set-up uses (a) single-pulse TLP ESD stimulus, (b) single-waveform HBM ESD stimulus, and (c) a square-waveform TLP pulse train ESD stimulus.*




**(a)**




**(b)**




**(c)**

*Figure 5-11 Instantaneous ESD discharging I-V curves obtained by TLP ESD testing, and TCAD ESD simulation using single-pulse TLP stimulus, square-waveform TLP pulse train stimulus, and single-waveform HBM ESD stimulus for (a) STI ESD protection diode, (b) diode-string ESD protection structure, and (c) SCR ESD protection device.*

HBM waveform produces $I_{peak}$~1.32A to stress the DUT. For equivalent ESD triggering speed and ESD-associated energy, the TLP pulses use $t_r$~10ns and $t_d$~100ns, corresponding to HBM ESD waveform of $t_r$~10ns and $t_d$~150ns. For TCAD ESD simulation, the ESD failure criterion is the thermal breakdown current ($I_{t2}$) caused by the maximum lattice temperature ($T_{max}$) reaching to 1688K in Si, causing Si melting inside an ESD protection device. TCAD ESD simulation provides rich insights on transient ESD discharging behaviors, which are carefully studied. First, Figure 5-11 shows that single-waveform HBM ESD simulation predicts an ESD protection level of $I_{t2}$~1.45A (~2.19KV) for the STI ESD protection diode, $I_{t2}$~1.27A (~1.92KV) for the diode-string ESD protection structure and $I_{t2}$~1.13A (~1.72KV) for the SCR ESD protection device under HBM ESD zapping, respectively. Unfortunately, since no HBM ESD zapping tester in our lab, there are no HBM ESD zapping test data to compare with. Second, using a square-waveform TLP pulse train, ESD simulation predicts that $I_{t2}$~1.22A for the STI ESD protection diode, $I_{t2}$~1.14A for the diode-string ESD protection structure and $I_{t2}$~0.97A for the SCR ESD protection device, which match the ESD protection capability results obtained by actual TLP test very well. In fact, the transient ESD I-V curves for the STI ESD protection diode, diode-string ESD protection structure and SCR ESD protection device from both TLP pulse train simulation and TLP testing agreed with each other very well for the whole ESD discharging I-V curves. In the SCR ESD protection device, the TLP pulse train ESD simulation accurately predicts the trigger voltage of $V_{t1}$~12.2V and turn-on resistance of $R_{on}$~3.3Ω in TLP testing. This clearly states that well-calibrated TCAD ESD simulation using square-waveform TLP pulse trains as ESD stimuli can be used to evaluate TLP ESD

| | SIM: single HBM pulse | SIM: single TLP pulse | SIM: TLP pulse train | TLP Test (pulse train) |
|---|---|---|---|---|
| STI Diode | 1.45A | 1.22A | 1.22A | 1.22A |
| Diode String | 1.27A | 1.14A | 1.14A | 1.14A |
| SCR | 1.13A | 0.97A | 0.97A | 0.97A |

*Table 5-1 HBM and TLP ESD $I_{t2}$ Comparison*

testing results. However, it is critical to understand that TLP testing is different from real-world HBM zapping, which is always required for rating the ESD protection for IC products. Unfortunately, the ESD $I_{t2}$ results from TLP pulse train ESD simulation is very different from that of single-pulse HBM ESD waveform simulation. On the other hand, the entire transient ESD discharging I-V characteristics obtained from single-pulse TLP simulation and single-waveform HBM ESD simulation match each other very well, except for the clear difference in $I_{t2}$. Meanwhile, the full ESD discharging I-V curve obtained by single-pulse TLP simulation is very different from that from both square-wave TLP pulse train simulation and TLP testing, even though the $I_{t2}$ results agree with each well. Table 5-1 summarizes the ESD protection levels ($I_{t2}$) obtained from TLP ESD testing and TCAD ESD simulation, which clearly shows the difference. The comparison clearly suggests that one has to be cautious in using TCAD ESD simulation to predict actual ESD protection design performance. Third, to further understand the difference in single-wave HBM and single-pulse TLP ESD simulation, the time-domain dynamic ESD discharging behaviors are examined in details, including the transient $T_{max}$-t and I-t characteristics for the ESD

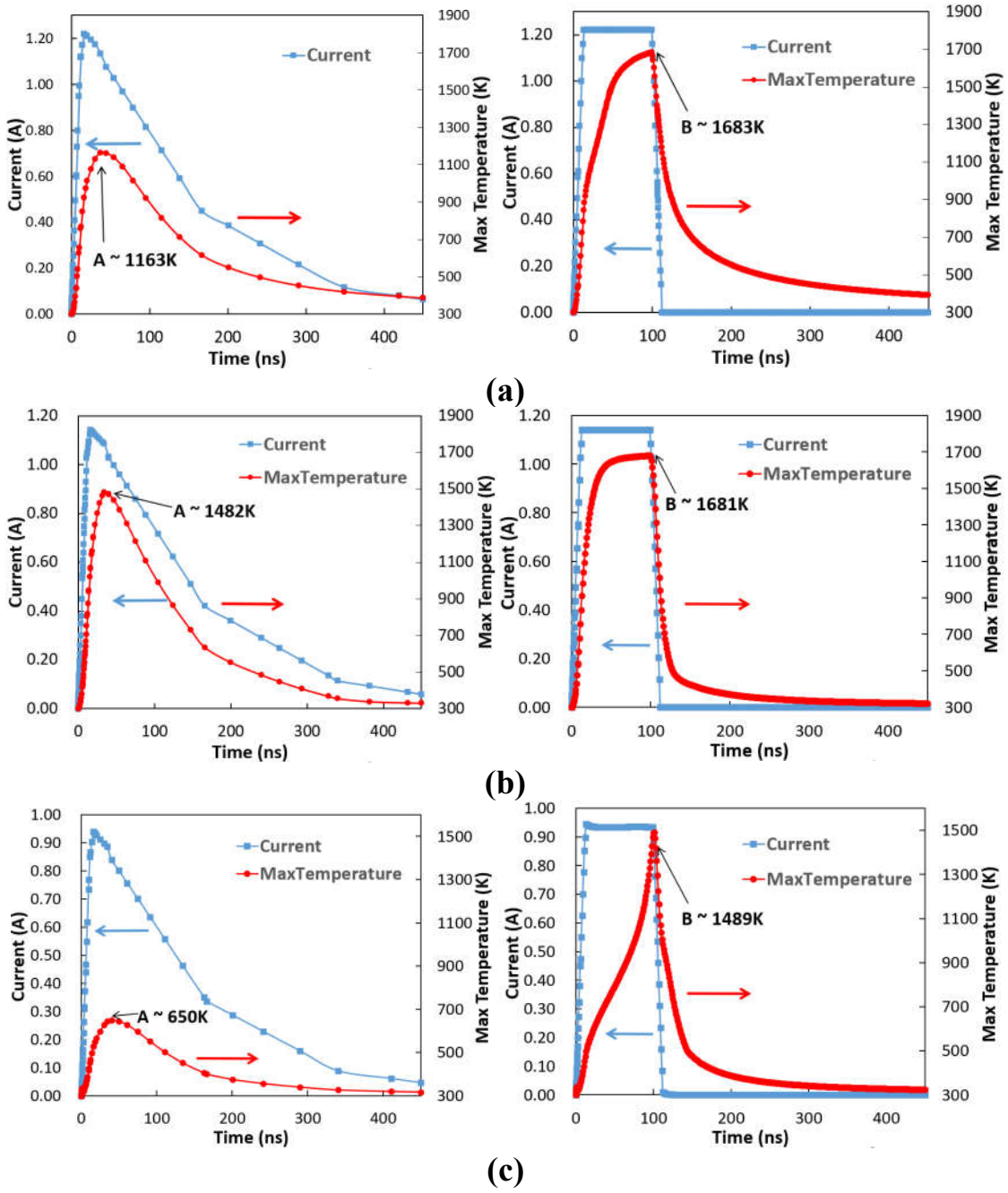



*Figure 5-12 Comparison of transient I-t curve (blue) and Tmax-t curve (red) obtained by single-wave HBM ESD simulation (L) and single-pulse TLP ESD simulation (R) for (a) an ESD protection diode, (b) a diode-string ESD protection structure, and (c) a SCR ESD protection device.*

protection devices as shown in Figure 5-12. In ESD simulation, the resulting $I_{peak}$ from both single TLP pulse and single HBM waveform simulation are almost same, i.e., $I_{peak}$ ~ 1.22A for STI ESD protection diode, $I_{peak}$ ~ 1.14A for the diode-string ESD protection structure and $I_{peak}$ ~ 0.97A for SCR ESD protection device. However, the $T_{max}$ from single-pulse TLP simulation is much higher than that from single-waveform HBM ESD simulation for all ESD protection devices. It is observed that, using single-wave HBM stimuli, $T_{max}$ curve generally follows the transient ESD discharging I-curve in t-domain with a slight delay at the peak (labelled point-A). While for single-pulse TLP stimulus ESD simulation, $T_{max}$ is not only much higher, it also stays high for a long period of ~100ns corresponding to the flat waveform top segment of the single TLP square pulse. This means that more significant heat generation and accumulation exist for the ESD protection devices under single-pulse TLP stressing compared to under single-wave HBM zapping. This further suggests that, while TLP testing provides useful ESD discharging behavioral information, one should be very cautious in using TLP results, both from testing and simulation, to predict the actual HBM zapping results. Fourth, Figure 5-11 shows that the $R_{ON}$ of the ESD protection devices under TLP pulse train simulation is different from that obtained by single-waveform HBM ESD simulation. Further, $V_{t1}$ of the SCR ESD protection device by TLP pulse train simulation and testing is smaller than that from ESD simulation using single HBM waveform, which is likely attributed to the fact that in both TLP pulse train ESD simulation and TLP testing (also using pulse train), the instantaneous ESD discharging I-V curves for DUT are obtained by an integration within a later 70%-90% window of the whole square waveform duration, excluding any possible overshoot often observed in ESD

discharging (Figure 5-13); however, in single-wave HBM ESD simulation and real-world HBM zapping test, the whole HBM waveform, including all possible overshoot and the waveform tail, are included in the calculation for obtaining the instantaneous I and V values during HBM ESD stressing. This is a major difference that may cause discrepancy in ESD simulation and testing in practical ESD protection designs.

From the above analysis, it is clear that while TCAD ESD simulation is very useful, TCAD ESD simulation using an ESD stimulus of a single-wave HBM waveform, a single-pulse TLP waveform, or a square-waveform TLP pulse train alone, is rather insufficient in accurately correlating with TLP testing and predicting real-world HBM zapping results. A mixed-mode multi-stimuli TCAD ESD simulation method using combined HBM and TLP pulse train as ESD stimuli is critical to accurately predict ESD protection designs.

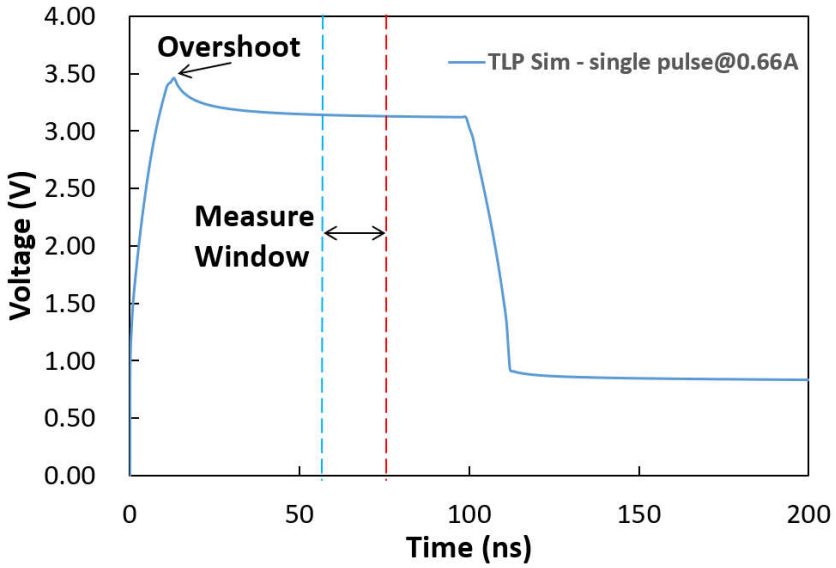



*Figure 5-13 Single-pulse TLP simulation for an ESD protection diode shows an overshoot typically occurring, which is outside the 70%-90% integration window in obtaining the transient ESD discharging I-V curve during TLP testing. This contribute to errors in estimating the I and V values.*

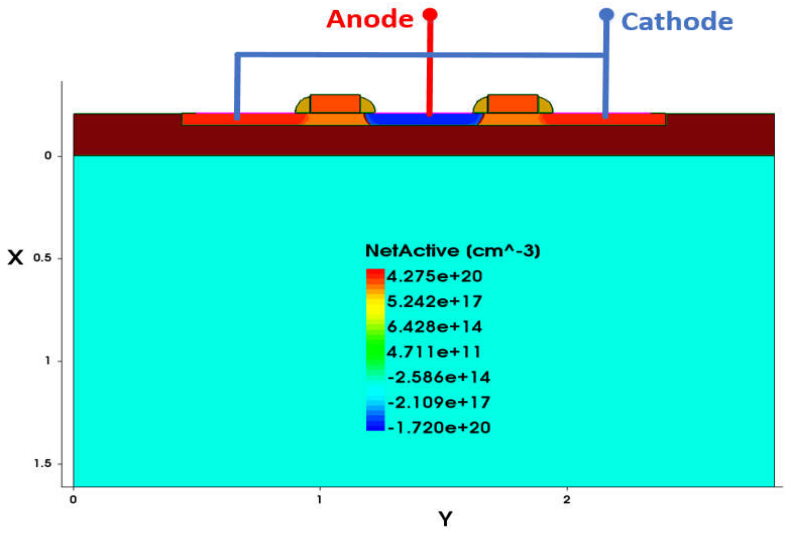



*Figure 5-14 Cross-section for an ESD protection diode fabricated in 45nm SOI CMOS.*

B. CDM and VFTLP ESD Simulation

Similar to the HBM and TLP simulation discussed earlier, the same approach was applied to study the impacts of CDM and VFTLP input stimuli on TCAD ESD simulation using an ESD protection diode fabricated in a foundry 45nm SOI CMOS technology which is shown in Figure 5-14. Mixed-mode TCAD ESD simulation was conducted using three different ESD input waveforms as depicted in Figure 5-15: single-pulse VFTLP square waveform, single-pulse CDM waveform and a square-waveform VFTLP pulse train. The fabricated ESD diode was characterized using a VFTLP tester.

The CDM ESD waveform used in this work follows the ESDA CDM ESD standard [9], where a 50V CDM pulse has $I_{peak}$~0.72A. Similar to TLP, for equivalent CDM ESD triggering speed and ESD energy, the VFTLP pulses use $t_r$~0.1ns and $t_d$~1ns. First, Figure 5-16 shows that CDM ESD simulation predicts an ESD protection level of $I_{t2}$~3.5A (~240V) for the ESD protection diode made in 45nm SOI CMOS. Unfortunately, since there is no

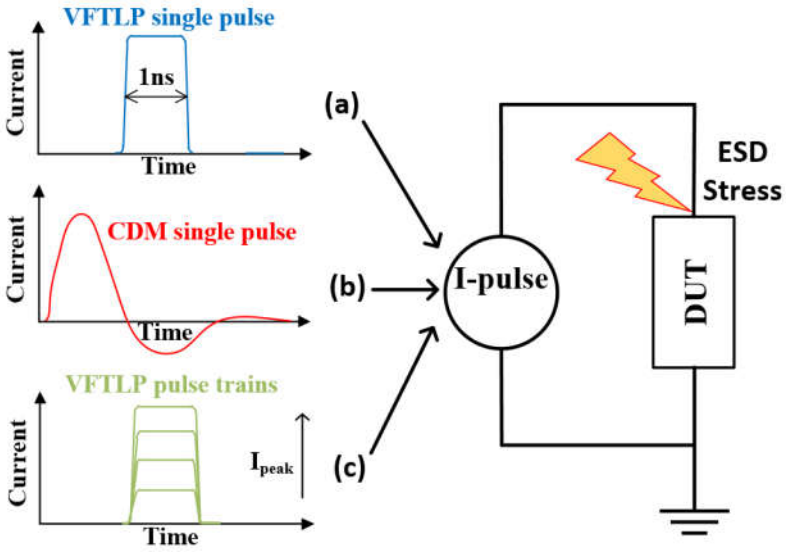



*Figure 5-15 New mixed-mode multi-stimuli TCAD ESD simulation set-up uses single VFTLP pulse, single CDM ESD waveform and a VFTLP pulse train as the ESD input stimulating signal.*

CDM zapping tester in our Lab, CDM ESD simulation could not be compared with CDM zapping test. Second, square-waveform VFTLP pulse train ESD simulation predicts that $I_{t2}$~2.28A for the ESD protection diode, which match well with VFTLP testing. In fact, the transient ESD discharging I-V characteristics for both VFTLP pulse train simulation and VFTLP testing match each other very well for the whole CDM ESD discharging I-V curves. This again suggests that well-calibrated TCAD ESD simulation using VFTLP pulse trains as stimuli can be used to evaluate VFTLP testing results. However, it is noteworthy that VFTLP testing is actually different from CDM zapping and may not be used to predict real-world CDM ESD zapping results. It is further observed that the ESD discharging I-V curves by single-pulse VFTLP simulation and single-waveform CDM ESD simulation agree with each other nicely, except for difference in the $I_{t2}$ results. On the other hand, the $I_{t2}$ of single-pulse VFTLP simulation also matches that of VFTLP testing well, but their ESD discharging I-V characteristics are very different. Table 5-2 summarizes the ESD $I_{t2}$

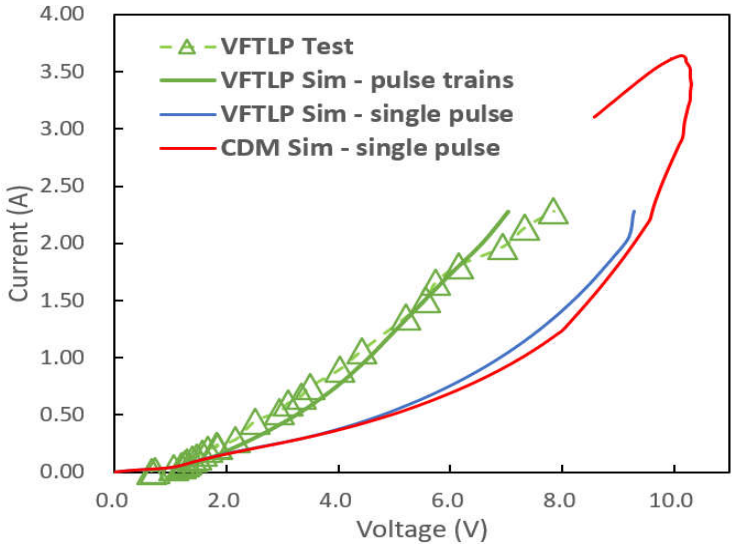



*Figure 5-16 Instantaneous CDM ESD discharging I-V curves for an ESD protection diode made in 45nm SOI CMOS obtained from VFTLP testing (pulse train) and TCAD ESD simulation using single-pulse VFTLP stimulus, single-waveform CDM stimulus and a VFTLP pule train.*

results extracted from VFTLP testing and TCAD ESD simulation using different ESD stimuli, which clearly shows the difference in between. Third, because the CDM and VFTLP ESD tests differ significantly, correlating the two results is much more difficult than doing so for HBM and TLP measurements [54]. To further understand the difference in CDM and VFTLP ESD simulation, time-domain ESD discharging behaviors are studied in details, including the transient $T_{max}$-t and I-t characteristics for the ESD diode as given in Figure 5-17. In CDM ESD simulation, the resulting $I_{peak}$ from both single-pulse VFTLP and single-waveform CDM stressing are almost same, with $I_{peak}$ ~ 2.28A for the ESD protection diode in 45nm SOI. However, the $T_{max}$ under single-pulse VFTLP stimulus is much higher than that that obtained by using a CDM ESD stimulus. It is observed that, for single-waveform CDM ESD simulation, $T_{max}$ curve generally follows the transient CDM ESD waveform in t-domain with a slight delay at the peak (labelled point-A). Also, there is a second peak of the $T_{max}$ after the I-curve oscillates into the negative cycle. This is

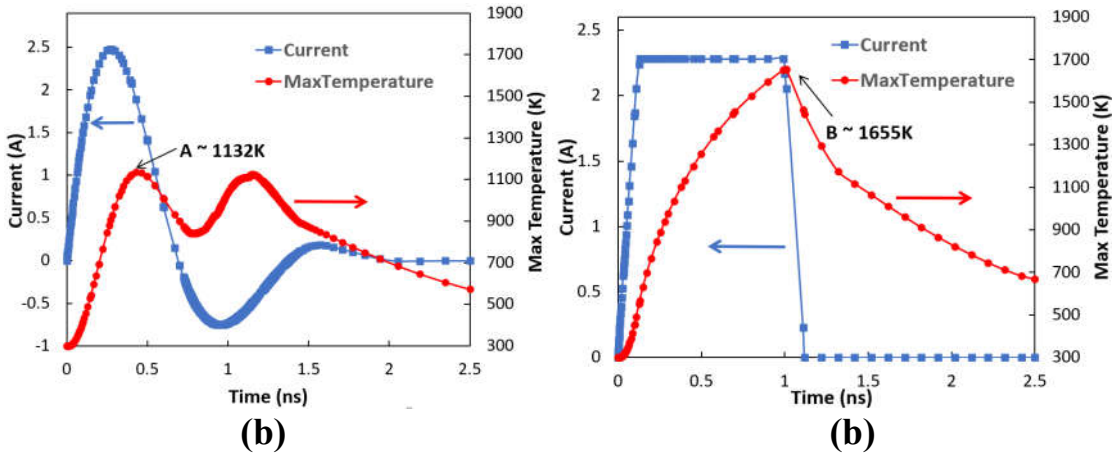



*Figure 5-17 Comparison of transient I-t curve (blue) and Tmax-t curve (red) obtained by (a) single-waveform CDM ESD simulation, and (b) single-pulse VFTLP ESD simulation, for an ESD protection diode made in a 45nm SOI CMOS.*

because as the real-world CDM waveform is oscillatory featuring strong first and substantial second peaks; however, the VFTLP waveforms are single-directional square waveforms. However, in single-pulse VFTLP simulation, $T_{max}$ is not only much higher, but also stays high for the most period of ~1ns of the VFTLP square waveform. This translates into more heat generation and accumulation within the ESD protection devices under VFTLP pulse stressing compared to during CDM zapping. This again states that, while VFTLP ESD simulation and testing provides useful ESD discharging information, one should be very cautious in not over-interpreting the VFTLP results aiming to accurately predict actual CDM ESD protection performance. Fourth, similar to TLP case, commercial VFTLP testers take a data integration across the later 70%-90% window of the DUT voltage and current waveforms obtained during VFTLP ESD stressing to estimate the instantaneous I and V values to construct the dynamic ESD discharging curves. This

VFTLP testing mechanism most likely misses the unavoidable overshoot during VFTLP characterization. On the other hand, using CDM ESD waveform can catch such overshoots. Therefore, the procedures of VFTLP stressing and CDM ESD zapping also contribute to the discrepancies in VFTLP and CDM ESD characterization in both simulation and testing.

In summary, no existing ESD simulation techniques may precisely predict practical ESD protection designs universally yet. This Chapter 5 reports a comprehensive and comparison study of impacts of various ESD input stimuli on transient ESD discharging behaviors in TCAD ESD simulation in comparison with ESD testing. Experiment and simulation of various ESD protection devices made in 28nm CMOS and 45nm SOI CMOS, using TLP and VFTLP ESD testing, and TCAD ESD simulation using single-waveform HBM/CDM ESD stimuli, single-pulse and pulse-train TLP/VFTLP ESD stimuli, clearly show that differences in ESD discharging characteristics exist in these ESD evaluation methods. Therefore, one must be cautious not over-interpreting TCAD ESD simulation details, obtained using any specific/individual ESD stimulus, to attempt to precisely predict practical ESD protection designs, as well as to correlate TLP/VFTLP stressing with HBM/CDM ESD zapping measurements. It concludes that it is important to use a mixed-

| | SIM: single CDM pulse | SIM: single VFTLP pulse | SIM: VFTLP pulse train | VFTLP Test (pulse train) |
|---|---|---|---|---|
| Diode | 3.5A | 2.28A | 2.28A | 2.28A |

*Table 5-2 CDM and VFTLP ESD $I_{t2}$ Comparison*

mode multiple-stimuli ESD simulation method in meaningfully and accurately characterizing ESD protection designs, as well as for ESD design prediction and validation.

# Chapter 6 RF Switches ESD Shell Model

High current simulation capability under electrostatic discharge (ESD) conditions for ESD self-protected front-end module (FEM) switch applications in an RF SOI Technology is shown for the first time. A methodology showing how to adequately characterize CMOS switch devices under ESD conditions is reviewed. Additionally, a methodology for extraction of a high current compact wrapper model which includes the parasitic bipolar transistor placed in parallel with the base MOSFET compact model is shown. Successful compact model simulation to hardware correlation is shown under ESD stress events.

One of the challenging reliability problems for all ICs is electrostatic discharge (ESD) failure. On-chip ESD protection becomes even more of a design challenge for high-frequency circuits in general and more specifically high-speed RF switches [5, 13, 30, 47]. ESD protection is needed for all kinds of IC designs to survive the ESD damage resulted from a transient transfer of electrostatic charges between the victim IC and other objects during manufacture, assembly and operation process. However, ESD parasitic capacitances can have a significant impact on the RF performance of cell phone front end module (FEM) switches. Adding ESD protection devices to the switches will introduce parasitic components and can degrade isolation loss and harmonics [55]. Large switch devices (>=1mm) are commonly used in cell phone FEM applications where the switch devices themselves use their ESD self-protection capability to protect against ESD events. To ensure IC design success, it is an essential step before final tapeout to conduct comprehensive IC design verification. Verification includes using spice simulation to predict the ESD self-protection level using high current compact models. However, the

current core model for the MOSFET only covers the normal operation region before the D/S breakdown point where the high ESD current happens. Normal simulations (non-ESD) fail to provide accurate prediction of the ESD self-protection level since circuit designers can only simulate "FET" mode. To address this problem and enable high current ESD simulation for the RF switch, we introduce a novel ESD shell model which can be easily integrated in parallel to the core model and achieve ESD prediction for both transmission line pulse (TLP) and human body model (HBM) stimulus sources.

Through various simulation and testing using both HBM and 100ns TLP zapping, Chapter 6 reports the first ESD shell model for prediction of ESD self-protection level for RF switches. The test samples were stacked-FET RF switches fabricated in a 130nm RF SOI technology and the TLP test was done on the wafer level. It is concluded that simulation only using the core model of MOSFETs is insufficient for ESD prediction. With the ESD shell model as proposed, excellent prediction of the ESD self-protection capability level is achieved. This chapter is organized as follows: Chapter 6.1 discusses the background on self-protection capability of switches and the need for an ESD shell model. Chapter 6.2 provides the shell model generation process. Chapter 6.3 covers the switch model simulation to measurement correlation.

## 6.1 ESD Self-Protection Capability of FEM Switches

RF switches play a more important role in today’s wireless communication as the 5G era is arriving. 5G technology is promising to support a large number of connections with

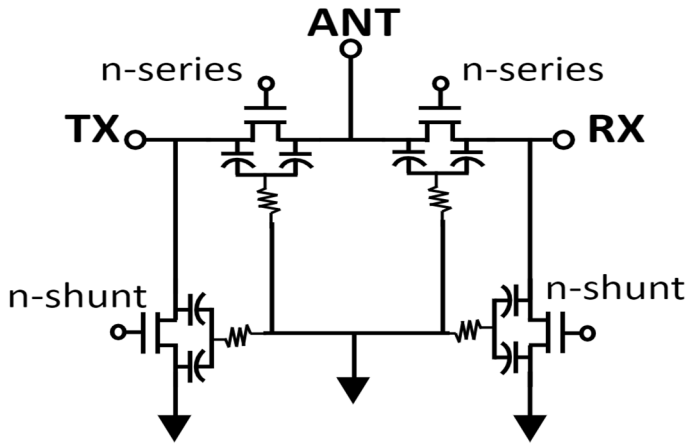



*Figure 6-1 SPDT series-shunt switch schematic, which is typically used to connect a transmitter (TX) and a receiver (RX) to a common antenna (ANT). For both series and shunt FETs, n-transistors can be stacked in series to meet high voltage level requirements.*

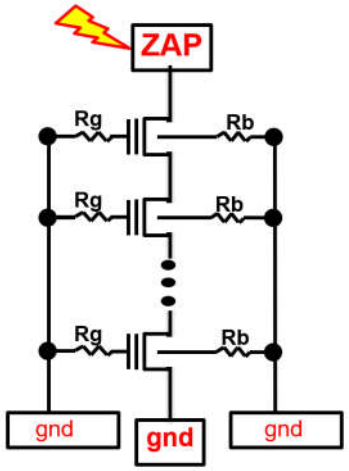



*Figure 6-2 Stacked FETs in the RF switch. The gate and body of each transistor are connected to ground through resistors Rg and Rb, which helps to achieve even distribution of drain to source voltage among these stacked transistors. The ZAP pad is zapped by ESD stress during simulation and test.*

improved data rate, mobility, coverage, power consumption and latency for autonomous driving, wearable devices and Internet of Things (IoT). Everything connected in the wireless network needs to communicate over a wide range of frequencies using multi-band RF transceivers, which drives the use of RF switches to provide isolation for noise/interference coupling among different circuit blocks inside multi-band RF chips [56]. Figure 6-1 shows the schematic of a single-pole double-throw (SPDT) transmit/receive

(T/R) switch in series-shunt topology [57]. Figure 6-2 shows the stacked FETs which are commonly used in RF switches to handle different input/output power levels as needed for the given application.

The series MOSFETs serve the main switching function between antenna and T/R, while the shunt MOSFETs are used to ground RF signals on the off-branch and improve the isolation of the switch. With reduced S/D capacitance and substrate coupling, silicon-

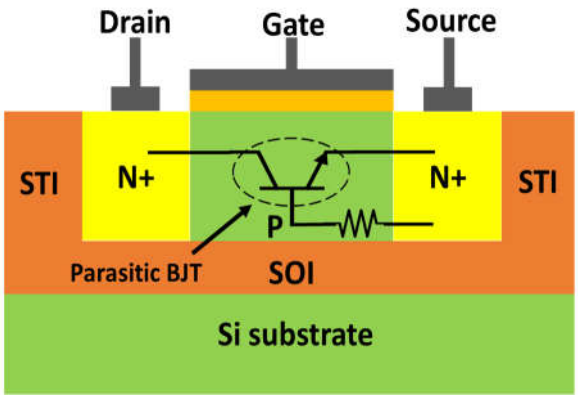



*Figure 6-3 Cross-section of a NMOS device in SOI CMOS technology depicting a parasitic NPN bipolar transistor (BJT) between the source and drain terminals. This parasitic BJT can be used as an ESD protection device since it can conduct high currents without getting damaged.*

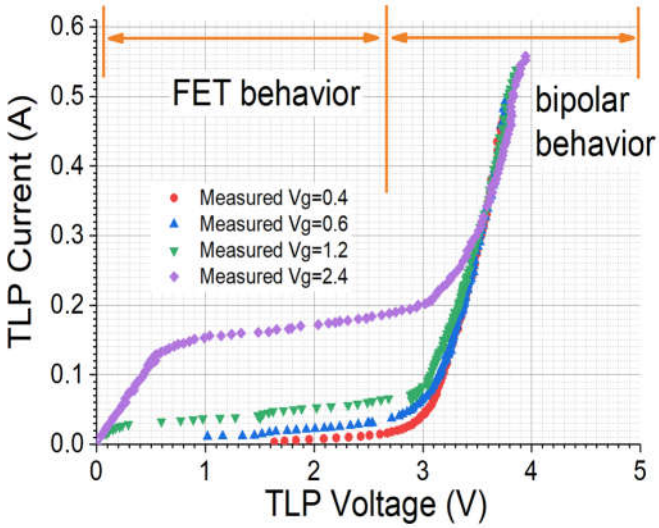



*Figure 6-4 TLP measurement data for single NMOS from a 130nm RF SOI technology shows FET and bipolar behavior changing at about 3V.*

on-insulator (SOI) technology delivers outstanding performance for ultra-high frequency RFIC design especially for 5G RF switches [58]. Due to its high sensitivity to the parasitic components from added ESD protection devices, large switches (width >=1mm) are frequently used as ESD self-protection devices by circuit designers. The large width MOSFET is able to handle a certain amount of ESD current once the parasitic bipolar in Figure 6-3 is triggered to give a low-resistance path for discharging under ESD events.

The TLP I-V curves for single MOSFET are given in Figure 6-4, where the two regions of normal FET behavior and bipolar behavior are clearly identified. During the test, we applied TLP stress to the drain, with the source being grounded and the gate being biased under various DC voltages $V_{gs}$.

When a ESD pulse zaps the switch in Figure 6-1 at TX, RX or ANT nodes, the transient current will find its path to the ground through either series-shunt stacks or just shunt stacks. Schematic level compact model-based simulation is a powerful way to analyze, optimize and verify ESD designs. The ultimate goal is to achieve ESD design verification and prediction for achieving ESD protection target levels which require accurate ESD simulation and testing procedures. However, the core model for the MOSFET only covers the normal FET region before the point where the bipolar behavior happens. The simulation is not capable of providing accurate prediction of the ESD self-protection level of the switches. A parasitic bipolar model needs to be added in parallel to the FET model for ESD simulation. The implementation of the "shell model" is illustrated in Figure 6-5.

The shell model is programmed using Verilog-A and the simulator is Spectre in Virtuoso from Cadence. The shell model has 5 terminals (D, $D_0$, G, S, B) where (D, G, S,

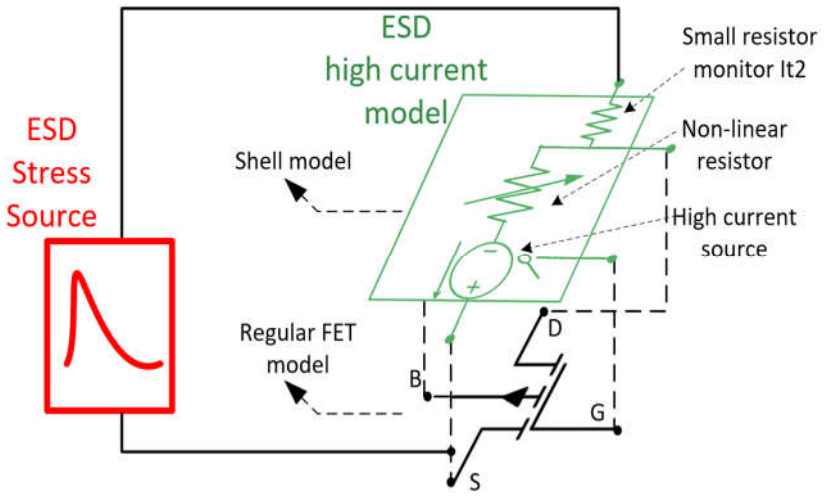



*Figure 6-5 Implementation of ESD shell model, where the shell model is parallel to the core FET model with (D, G, S, B) of the shell model connected to (Drain, Gate, Source, Body) of the core FET model respectively.*

B) of the shell model are connected to (Drain, Gate, Source, Body) of the core FET model respectively. Between the shell model's D and $D_0$ is a small resistor monitoring failure when reaching failure current level ($I_{t2}$). The current flow through the monitor resistor will be the total current of shell model current and core FET model current. The ESD shell model enables the simulation in the high current region. It can be easily connected into the existing core FET model in the schematic. Also, it will have minimal to no impact on the normal operation of the FET model since the trigger point of the parasitic BJT inside the shell model occurs at a much higher voltage than the FET nominal operating ($V_{DD}$) voltage which is < 1.32V. Meanwhile, the shell model is only enabled during ESD simulation. While the switch is in RF simulation, the shell model is turned off, thus having no influence on the RF performance.

## 6.2 Model Generation Process

Next, we study the process for shell model generation for the single MOSFET used in RF switches. We use the device from a 130nm RF SOI technology where the $I_{t2}$ is plotted versus gate to source voltages ($V_{gs}$) and body to source voltages ($V_{bs}$) as shown in Figure 6-6 and Figure 6-7. We will further show that the ESD shell model matches well with TLP

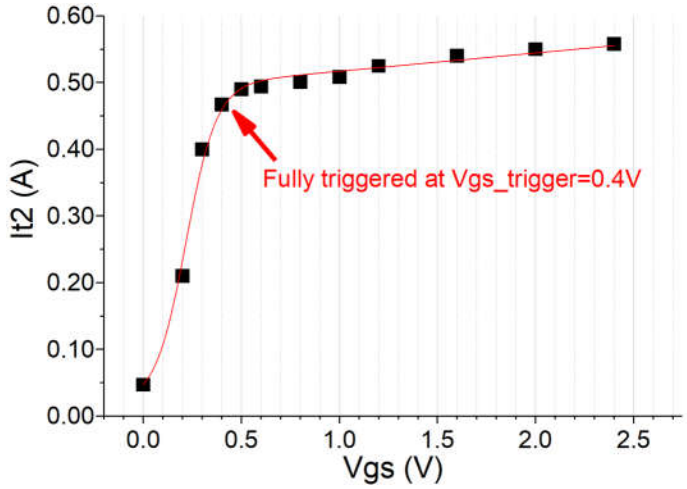



*Figure 6-6 TLP measurement data $I_{t2}$ vs. $V_{gs}$ (black dots) for single NMOS from a 130nm RF SOI technology, which shows that $I_{t2}$ has a strong dependence on $V_{gs}$ in this technology and this effect is modeled by a hyperbolic equation (red line) in the shell model.*

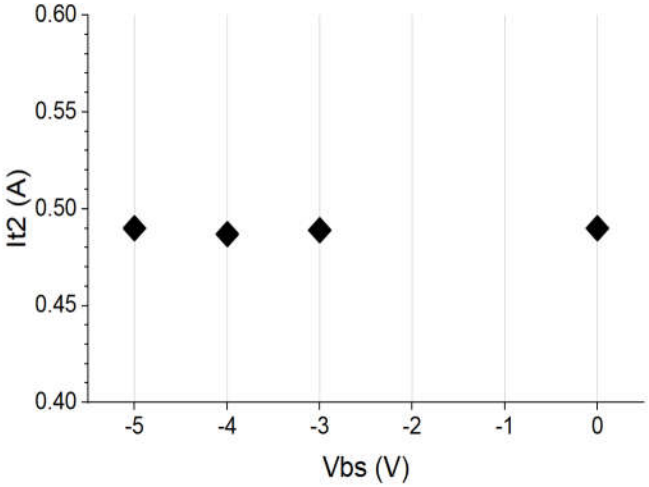



*Figure 6-7 TLP measurement data $I_{t2}$ vs. $V_{bs}$ ($V_{gs}$=0.5V) for single NMOS from a 130nm RF SOI technology, which shows no dependence on $V_{bs}$ and required no additional equation inside the shell model to fit $I_{t2}$ with $V_{bs}$.*

100ns measurement results. Figure 6-8 illustrates the compact model generation process of the shell model for a single MOSFET.

First, we need to measure the TLP/SOA data using various biasing conditions and device dimensions including different gate bias, body bias, width and length for the selected MOSFET. The TLP measurements provide ESD I-V curves for the device under test (DUT) which include the ESD-critical parameters such as the ESD triggering voltage ($V_{t1}$), parasitic bipolar holding voltage ($V_{hold}$), parasitic bipolar resistance ($R_{ON}$) and failure current ($I_{t2}$), among which $V_{t1}$ is the voltage level where the DUT is turned on and starts to conduct the ESD transient and $V_{hold}$ is the voltage level when DUT has latched in snapback

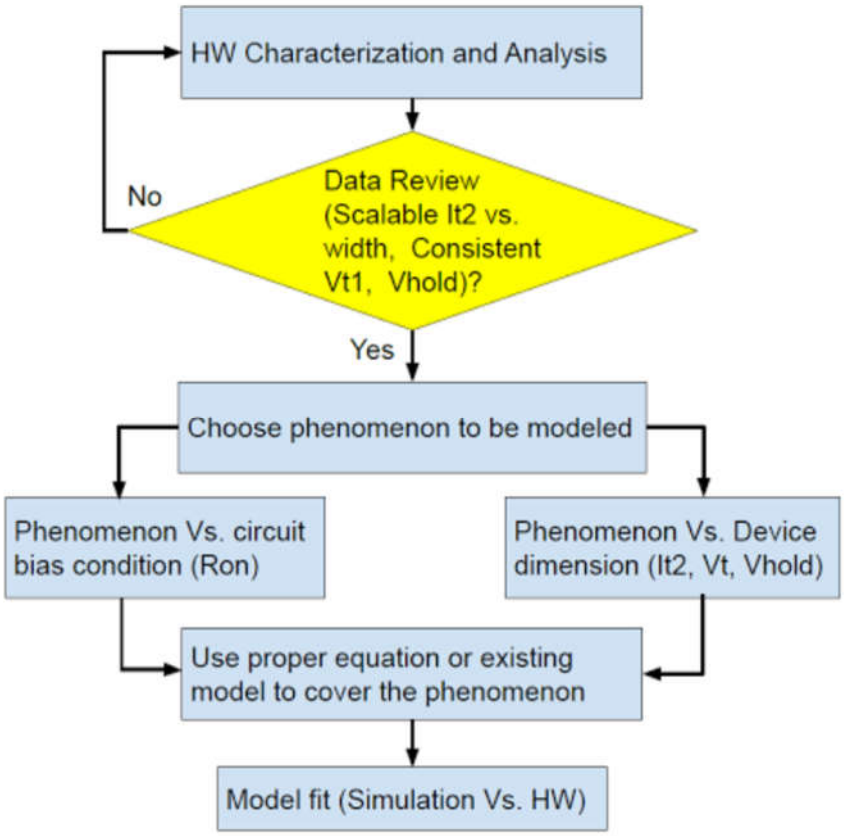



*Figure 6-8 Flow chart of shell model generation*

state. Next, we need to review the test results and find the “golden" die, which presents a stable, consistent and average measurement result, for building the shell model. The “golden” die is measured with “typical” ESD-critical parameters which show scalable $I_{t2}$ and $R_{ON}$ versus width, consistent $V_{t1}$ and $V_{hold}$. Then we can build the shell model using these extracted parameters; Third, we need to examine the data collected from those “golden” splits and find out whether the ESD-critical parameters have any dependence on the gate bias, body bias and gate length which will be modeled using proper equations. For instance, $I_{t2}$ has a strong dependence on $V_{gs}$ in this technology so this effect must be included in the shell model as shown in Figure 6-6. The red line in Figure 6-6 is the fitting curve which is modeled by a hyperbolic equation inside the shell model. $I_{t2}$ is relatively constant under different $V_{bs}$ as shown in Figure 6-7 showing no dependence on $V_{bs}$, which in turn leads to no additional equation needed inside the shell model to fit $I_{t2}$ with $V_{bs}$. Fourth, the accuracy of the ESD shell model can be evaluated by comparing the I-V curves and the ESD critical parameters between simulation and hardware.

Figure 6-5 shows the testbench for ESD simulation. The Monte Carlo PSP model provides the basic $I_d/V_d$ characteristics of the MOSFET used and in parallel with it are the ESD stress source (red) and the shell model (green). Inside the shell model, there is a nonlinear resistor and a current source. The resistor represents the $R_{ON}$ resistance variation during ESD stress due to self-heating and velocity saturation. The current source behaves as a low resistance path and conducts the majority of the ESD current after DUT voltage is beyond $V_{t1}$. Since there is a correlation between $I_{t2}$ and $V_{gs}$ (Figure 6-6), the model failure

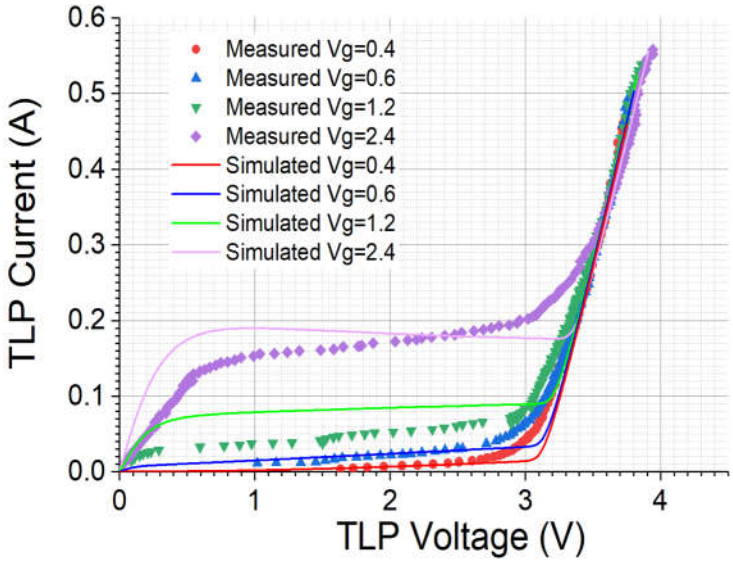



*Figure 6-9 Single MOSFET TLP I-V curves: simulation vs. measurement. The MOSFET is biased at various gate voltage $V_g$ and the results show excellent match between shell model and hardware.*

equation is a function of $V_{gs}$ (at $V_{t1}$ trigger point) and will stop the simulation when total current reaches $I_{t2}$ at corresponding $V_{gs}$.

Figure 6-9 shows the I/V curves of shell model simulation and hardware TLP test for the device measured. Not only do I-V curves and the ESD critical parameters match well, but also the dependence of $I_{t2}$ on $V_{gs}$ is well represented by the shell model. The normal operation of this device is up to 1.32V max and from approximately 1.8V to 3.2V the base model is not well fit in that region leading to some error, however, from ~3.4V and higher the parallel parasitic bipolar shell model kicks in and gives excellent fitting results. The region from 1.8V to 3.2V base model difference is not significant since under ESD conditions the switch devices go into bipolar turn-on and the main ESD voltage clamping and failure current will be above ~3.4V when the shell model turns on. Currently the shell model simulation only treats the source and drain junction fail. Gate failure could be a

future enhancement since now we only see small $V_{gs}$ values ~1V or less, which is well below the GOX breakdown voltage.

## 6.3 Simulation to Measurement Correlation

With the shell model generated for the single MOSFET, the next step is to verify the simulation to measurement correlation. In applications such as the one shown in Figure 6-2, RF switches can utilize stack structures of 12 or more in series to handle higher power. The simulation to measurement correlation is thoroughly examined for stacked MOSFETs with different stack heights and various gate and body resistance ($R_g$ and $R_b$). As shown in Figure 6-2, $R_g$ is connected between gate of each MOSFET and ground, and $R_b$ is connected between body of each MOSFET and ground. Figure 6-10 shows the $I_{t2}$ of RF switches with 6, 8 and 12 stack height under HBM test, TLP test and TLP simulation.

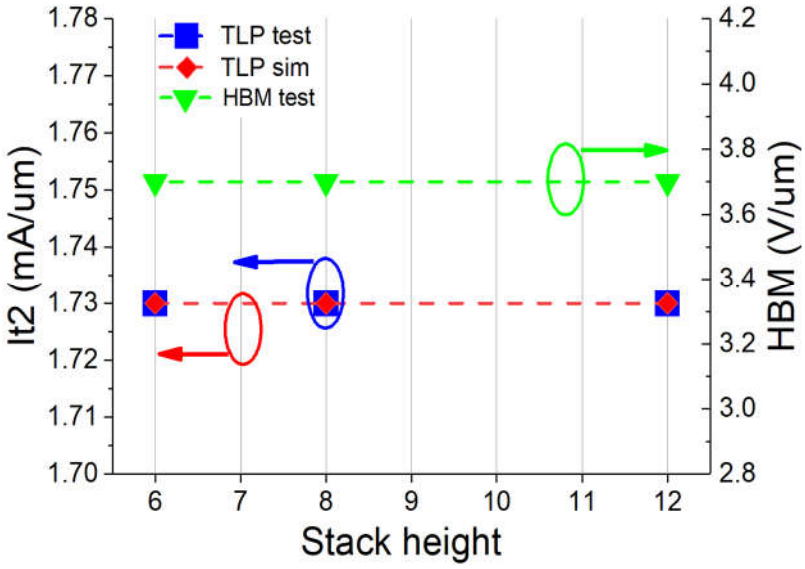



*Figure 6-10 TLP $I_{t2}$ and HBM failure level vs. series stack height. It shows that simulation accurately predicted the failure level of the TLP test for different stack heights and $I_{t2}$ stays at the same level with the increasing stack height. The gate length of the MOSFETs is $L_g$=160nm.*

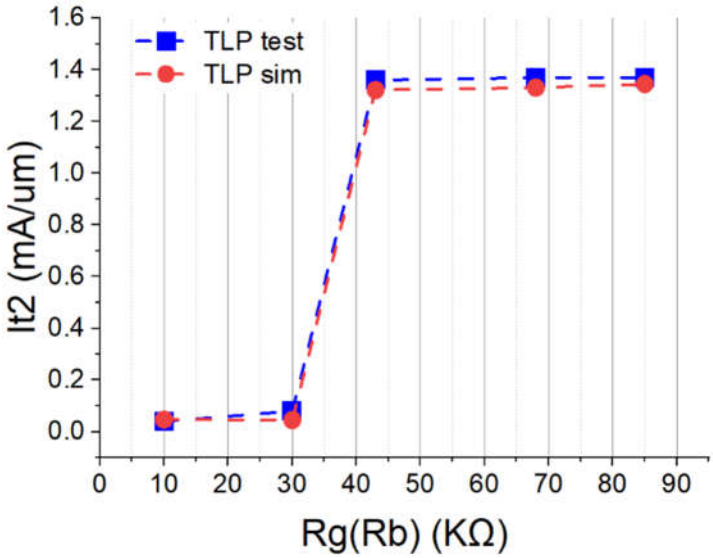



*Figure 6-11 TLP $I_{t2}$ vs. $R_g(R_b)$ resistance. In each of these 5 splits, $R_g$ and $R_b$ are equal ($R_g$=$R_b$=10KΩ, 30KΩ, 43KΩ, 68KΩ and 85KΩ). The gate length of the MOSFETs is $L_g$=240nm.*

Figure 6-11 shows the $I_{t2}$ of stacked RF switches with different gate and body resistances under TLP test and simulation.

As presented in Figure 6-10, the simulation accurately predicted the failure level of the TLP test for different stack heights. Also, we can observe that $I_{t2}$ stays at the same level with the increasing stack height. When comparing the HBM test with the TLP test, we can observe that the $I_{t2}$ of HBM test, which is equivalent to 2.47mA/um or 3.7V/um, is larger than that of TLP test which is 1.73mA/um. This is reasonable because the TLP pulse can do more damage to the DUT than the HBM pulse of the same level due to the longer duration of the current pulse. For the standard TLP pulse, it will stay at the peak current for ~80ns and accumulate more heat inside the DUT. However, for the HBM pulse, it will drop right after reaching the peak current, resulting in a much quicker heat dissipation and smaller overall self heating as discussed in [53].

In Figure 6-11, the simulation shows a trend of $I_{t2}$ increasing with $R_g$($R_b$) resistance, same as the TLP experimental test results. In each of these 5 splits, $R_g$ and $R_b$ are equal ($R_g$=$R_b$=10KΩ, 30KΩ, 43KΩ, 68KΩ and 85KΩ). The overall accuracy of the simulation can reach ~98%. Meanwhile, it is important to note in Figure 6-12 that the $I_{t2}$ is quite small

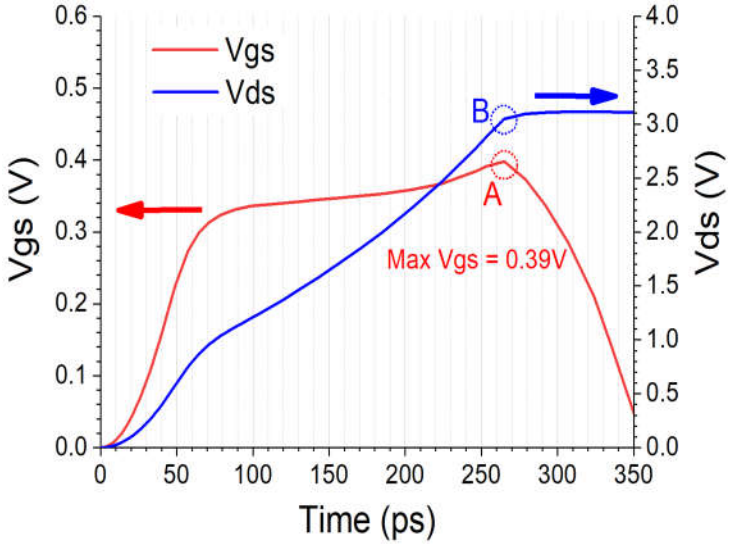



*Figure 6-12 TLP simulation results of stacked RF switches: $V_{gs}$ (red line) and $V_{ds}$ (blue line) of the top FET vs. time, with $R_g$=$R_b$=30KΩ. $V_{ds}$ enters the flat region after point B, where the parasitic bipolar is triggered and the voltage is clamped at ~3.1V. At the same time, the $V_{gs}$ starts to drop after reaching the peak value ~0.39V at point A.*

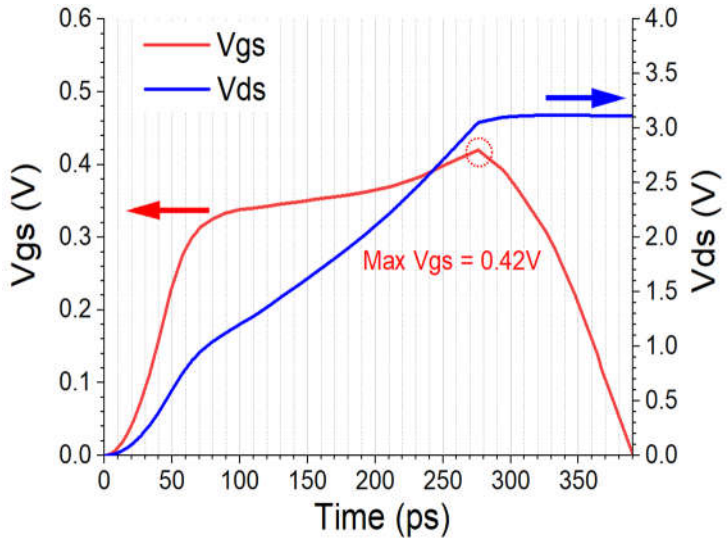



*Figure 6-13 TLP simulation results of stacked RF switches: $V_{gs}$ (red line) and $V_{ds}$ (blue line) of the top FET vs. time, with $R_g$=$R_b$=85KΩ. The peak value of $V_{gs}$ is ~0.42V.*

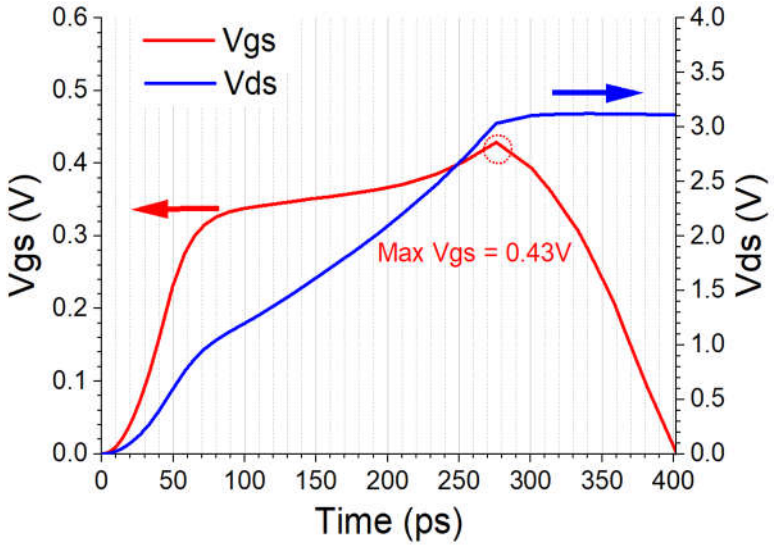



*Figure 6-14 TLP simulation results of stacked RF switches: $V_{gs}$ and $V_{ds}$ of the top FET vs. time, with $R_g$=$R_b$=150KΩ. The peak value of $V_{gs}$ is ~0.43V.*

at lower $R_g(R_b)$, after $R_g(R_b) > 43K\Omega$, $I_{t2}$ jumps up to a larger value. This can be interpreted as following: The $I_{t2}$ is determined by the $V_{gs}$ as shown in Figure 6-6. But the $V_{gs}$ along with the $V_{ds}$ of the MOSFETs in the stacked RF switches are changing during the time span of the TLP pulse as shown in Figure 6-12, Figure 6-13 and Figure 6-14.

Once the $V_{gs}$ voltage reaches a certain value ($V_{g\_trigger}$) during the ESD event, the parasitic bipolar will be fully turned on and start conducting a large amount of current. Since the bipolar is in the latchup state after turning on, it will still be able to conduct the same amount of current even though the transient $V_{gs}$ falls down later. Then the $I_{t2}$ will stay at the maximum value ever reached and only be determined by the maximum $V_{gs}$ during the TLP test. The $V_{gs}$ value when the $V_{ds}$ reaches the bipolar trigger voltage $V_{t1}$ is key since it determines the $I_{t2}$ of the parasitic NPN beneath the MOSFET. The gate resistor value modulates the gate voltage at $V_{t1}$ during an ESD event which in return can modulate the $I_{t2}$ of the parasitic NPN.

Meanwhile the maximum $V_{gs}$ of the MOSFETs in the stacked RF switches is found in the simulation to increase with larger $R_g(R_b)$ as shown in Figure 6-15. For the small $R_g(R_b)$, the maximum $V_{gs}$ will hardly reach $V_{g_}$trigger, which is 0.4V as indicated in Figure 6-6, and will not be fully turned on. When the $V_{gs}$ drops later, the $I_{t2}$ will also drop as shown in the $I_{t2}$ vs. $V_{gs}$ curve and result in an early failure. For the example of Figure 6-12 with $R_g$=$R_b$=30KΩ, the $V_{ds}$ of the top FET in the stack enters the flat region after point B, where the parasitic bipolar is triggered and the voltage is clamped at ~3.1V. At the same time, the $V_{gs}$ starts to drop after reaching the peak value at point A. However, this maximum $V_{gs}$ is slightly smaller than the $V_{g\_tigger}$ (Figure 6-15). So the bipolar is not fully turned on at the $V_{t1}$ point and the $I_{t2}$ level will decrease as the $V_{gs}$ drops at the $V_{t1}$ point, yielding a low failure level as indicated in Figure 6-11.

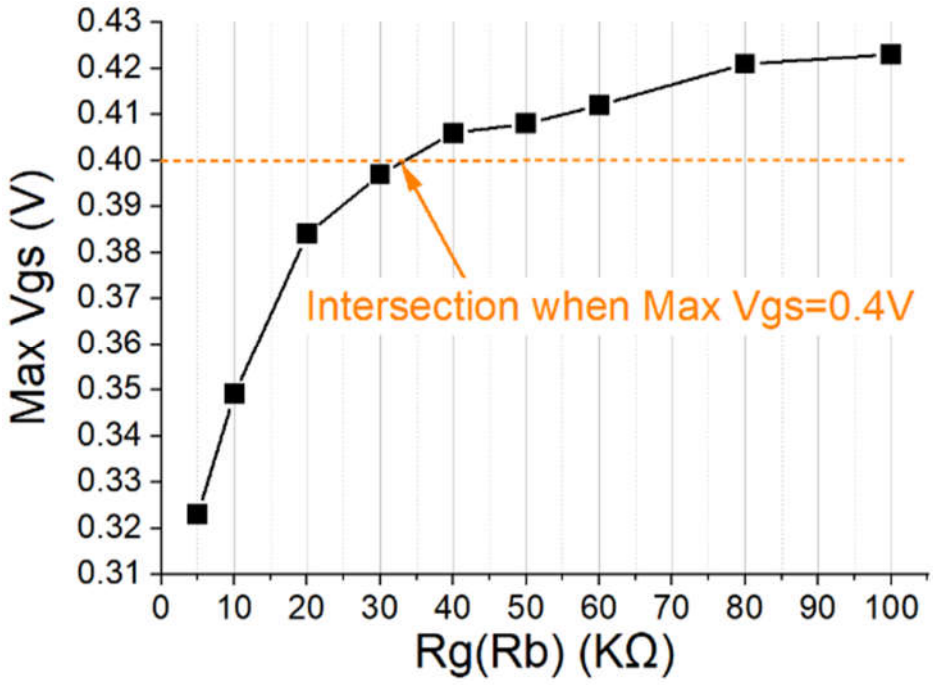



*Figure 6-15 TLP simulation results of stacked RF switches with different $R_g$ and $R_b$: Maximum $V_{gs}$ of the top FET vs. $R_g(R_b)$.*

As for the large $R_g(R_b)$, typically larger than 30KΩ, the $V_{gs}$ can surpass the $V_{g\_trigger}$ as shown in Figure 6-15 and the parasitic bipolar will be fully turned on (each single finger fully on, multiple fingers in parallel all on), capable of maintaining the conduction of high current even though the $V_{gs}$ drops later and yielding a large $I_{t2}$ value. For the example of $R_g$=$R_b$=85KΩ and 150KΩ in Figure 6-13 and Figure 6-14, the maximum $V_{gs}$ has surpassed the $V_{g\_trigger}$ and so the $I_{t2}$ level will only be determined by the maximum $V_{gs}$ at the $V_{t1}$ trigger point.

In summary, we discussed the implementation of a novel ESD shell model which enables the ESD simulation for RF switches for cell phone FEMs in Chapter 6. By fitting the ESD compact model from experimental test data, the ESD shell model can accurately predict the failure level of series/shunt switch self-protection ESD capability. As verified in hardware, the RF switches with different stack heights and $R_g(R_b)$ resistance, >98% accuracy using simulation results can be achieved. Moreover, the ESD shell model can be easily placed in parallel to the FET base model in the schematic which is a simple and cost-effective solution to enable predictive ESD simulations of FEM switch devices.

# Chapter 7 Conclusion

In this dissertation, ESD protected 28GHz, 38GHz and 60GHz wide-band travelling wave switches have been presented, which achieves comparable performance with state-of-art design and is the first travelling wave switch on SOI with co-design ESD protection. To reach a higher data rate with available frequency bands, millimeter wave (mm-wave) switches has been demonstrated with the consideration of reliability issue of electrostatic discharge (ESD) which will introduce severe parasitic effects under this frequency level and degrade the performance of RFICs. The insertion loss and isolation together with ESD protection capability have been compared which shows the importance of ESD-RFIC co-design.

On the other hand, this dissertation presented several highlights of advanced ESD protection designs. It is reported recently that conventional pad-based charged-device-model (CDM) ESD protection method may be theoretically wrong. We analyzed the failure of classic pad-based ESD protection methods in CDM ESD protection and discussed a disruptively new non-pad-based internally distributed CDM ESD protection concept, which is demonstrated in an oscillator IC designed and fabricated in a 45nm SOI CMOS process. Design of novel interposer and through-silicon-via (TSV) based internal-distributed CDM ESD protection mesh networks were also presented. We also introduced a new mixed-mode TCAD ESD simulation flow using combined HBM-TLP stimuli, or CDM-VFTLP stimuli, to enable ESD protection design prediction and verification. It provides a thorough analysis of various TCAD ESD simulation scenarios using both real-world HBM and CDM ESD waveforms, and their corresponding TLP and VFTLP square

waveforms, in both single-pulse and pulse train manners, as stimuli. Besides, we discussed the implementation of a novel ESD shell model which enables the ESD self-protection simulation for RF switches for cell phone FEMs. As verified in hardware, >98% accuracy using simulation results can be achieved. Moreover, the ESD shell model can be easily placed in parallel to the FET base model in the schematic which is a simple and cost-effective solution to enable predictive ESD simulations of FEM switch devices.

In the future, multiple-pole-multiple-throw (MPMT) RF switches can be explored with ESD co-design at mmWave frequency. The challenge of utilizing travelling-wave topology on MPMT RF switches is huge and need to be studied to achieve good performance. Also, the parasitic effect of ESD protection for MPMT RF switches will require more co-design effort for compensation. Advanced ESD protection methods such as interposer and TSV based internal-distributed CDM ESD protection mesh networks are promising with the edge-cutting fabrication, packaging and assembly techniques.

# References


[1] Yang, B., Yu, Z., Lan, J., Zhang, R., Zhou, J., & Hong, W. (2018). Digital Beamforming-Based Massive MIMO Transceiver for 5G Millimeter-Wave Communications. IEEE Transactions on Microwave Theory and Techniques, 66, 3403-3418.

[2] U. L. Rohde, A. K. Poddar, I. Eisele, and E. Rubiola, "Next generation 5G radio communication NW," in *2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFC)*, 2017, pp. 113–116.

[3] M. Agiwal, A. Roy, and N. Saxena, "Next Generation 5G Wireless Networks: A Comprehensive Survey," *IEEE Commun. Surv. Tutorials*, vol. 18, no. 3, pp. 1617–1655, 2016.

[4] Federal Communications Commission, "Use of Spectrum Bands Above 24 GHz for Mobile Radio Services (FCC-CIRC1711-02)," 2017.

[5] A. Wang, *On-Chip ESD Protection for Integrated Circuits: an IC Design Perspective*, Kluwer, Boston, 2002, ISBN: 0-7923-7647-1.

[6] "Electrostatic Discharge Sensitivity Classification", Method 3015.7, MIL-STD-883E, Dept. of Defence, March 1989.

[7] "For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Component Level", *ESDA and JEDEC*, ANSI/ESDA/JEDEC JS-001-2017, ESD Association and JEDEC Solid State Technology Association.

[8] H. Wang, et al, "Chip-Level CDM Circuit Modeling and Simulation for ESD Protection Design in 28nm CMOS", *Proc. IEEE ICSICT*, 2018, **DOI:** 10.1109/ICSICT.2018.8564936.

[9] "For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level", *ESDA and JEDEC*, *ANSI/ESDA/JEDEC JS-002-2014*, ESD Association and JEDEC Solid State Technology Association, 2014.

[10] T. Maloney, "Transmission Line Pulsing Techniques for Circuit Modelling of ESD Phenomena", *Proc. EOS/ESD Symp.*, pp. 49–54, 1985.

[11] B. Qin, X. Wang, H. Xie, L. Lin, H. Tang, A. Wang, H. Chen, B. Zhao, L. Yang and Y. Zhou, "1.8pJ/pulse programmable Gaussian pulse generator for full-band non-carrier impulse UWB transceivers in 90nm CMOS", *IEEE Trans. Industrial Electronics, Vol. 57, No. 5,* pp. 1555-1562, May 2010.

[12] H. Xie, X. Wang, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, F. Yao, A. Wang and Y. Zhou, "A 52mW 3.1-10.6GHz fully integrated correlator for IR-UWB transceivers in 0.18μm CMOS", *IEEE Trans. Industrial Electronics, Vol. 57, No. 5,* pp. 1546-1554, May 2010.

[13] A. Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang and C. Zhang, "A review on RF ESD protection design", *IEEE Trans. Electron Devices, Vol. 52, No. 7,* pp. 1304-1311, July 2005.

[14] X. S. Wang, X. Wang, F. Lu, C. Zhang, Z. Dong, L. Wang, R. Ma, Z. Shi, A. Wang, M-C F. Chang, D. Wang, A. Joseph and C. P. Yue, "Concurrent design analysis of high-linearity SP10T switch with 8.5 kV ESD protection", *IEEE J. Solid-State Circuits, Vol. 49, No. 9*, pp. 1927-1941, September 2014.

[15] X. Wang, X. Guan, S. Fan, H. Tang, H. Zhao, L. Lin, Q. Fang, J. Liu, A. Wang and L. Yang, "ESD-protected power amplifier design in CMOS for highly reliable RF ICs", *IEEE Trans. Industrial Electronics, Vol. 58, No. 7,* pp. 2736-2743, July 2011.

[16] K. Raczkowski, S. Thijs, W. De Raedt, B. Nauwelaers and P. Wambacq, "50-to-67GHz ESD-protected power amplifiers in digital 45nm LP CMOS", *IEEE ISSCC Tech. Digest*, pp. 382-383, 2009.

[17] M. Tsai, S Hsu, F. Hsueh, C. Jou, S. Chen and M. Song, "A wideband low noise amplifier with 4 kV HBM ESD protection in 65nm RF CMOS*", IEEE Microwave and Wireless Components Letters, Vol. 19, No. 11*, pp. 734-736, November 2009.

[18] C. Wang, F. Lu, Q. Chen, F. Zhang, C. Li, D. Wang and A. Wang "A study of impacts of ESD protection on 28/38GHz RF switches in 45nm SOI CMOS for 5G mobile applications", *Proc. IEEE Radio and Wireless Symposium*, pp. 157-160, 2018.

[19] F. Zhang, C. Li, M. Di, Z. Pan, H. Wang and A. Wang, "ESD co-design of mm-wave RF switch in 22nm SOI", *Proc. IEEE Electron Devices Technology and Manufacturing Conference (EDTM)*, 2021.

[20] B. Yu, K. Ma, F. Meng, K. S. Yeo, P. Shyam, S. Zhang and P. R. Verma, “DC-30 GHz DPDT switch matrix design in high resistivity trap-rich SOI”, *IEEE Trans. Electron Devices, Vol 64, No. 9,* pp. 3548 – 3554, September 2017.

[21] K. Ma, S. Mou and K. S. Yeo, "A miniaturized millimeter-wave standing-wave filtering switch with high P1dB", *IEEE Trans. Microwave Theory and Techniques, Vol. 61, No. 4,* pp. 1505-1515, April 2013.

[22] F. Meng, K. Ma, K. S. Yeo and S. Xu, “Monolithic sub-terahertz SPDT switches with low insertion loss and enhanced isolation", *IEEE Trans. Terahertz Science and Technology, Vol.8, No.2*, pp.192-200, March 2018.

[23] C. Chen and D. Peroulis, “Liquid RF MEMS wideband reflective and absorptive switches”, *IEEE Trans. Microwave Theory and Techniques, Vol. 55, No. 12*, pp. 2919-2929, December 2007.

[24] C. D. Patel and G. M. Rebeiz, “A high-reliability high-linearity high-power RF MEMS metal-contact switch for DC–40-GHz applications’, *IEEE Trans. Microwave Theory and Techniques, Vol. 60, No. 10*, pp. 3096-3112, October 2012.

[25] T. Singh and R. R. Mansour, “Characterization, optimization, and fabrication of phase change material germanium telluride based miniaturized DC–67 GHz RF switches”, *IEEE Trans. Microwave Theory and Techniques, Vol. 67, No. 8,* pp. 3237-3250, August 2019.

[26] H. Y. Chang and C. Y. Chan, “A low loss high isolation DC-60 GHz SPDT traveling-wave switch with a body bias technique in 90 nm CMOS process”, *IEEE Microwave and Wireless Components Letters, Vol. 20, No. 2*, pp. 82-84, February 2010.

[27] M.-C. Yeh, Z.-M. Tsai, and H. Wang, “A miniature DC-to-50 GHz CMOS SPDT distributed switch”, *Proc. European Microwave. Conference*, pp. 665-668, 2005.

[28] K. T. Trinh, H. Kao, H. Chiu and N. C. Karmakar, “A Ka-band GaAs MMIC traveling-wave switch with absorptive characteristic”, *IEEE Microwave and Wireless Components Letters, Vol. 29, No. 6*, pp. 394-396, June 2019.

[29] X. Tang, E. Pistono, P. Ferrari and J. Fournier, “A traveling-wave CMOS SPDT using slow-wave transmission lines for millimeter-wave application”, *IEEE Electron Device Letters, Vol. 34, No. 9*, pp. 1094-1096, September 2013.

[30] F. Lu, R. Ma, Z. Dong, L. Wang, C. Zhang, C. Wang, Q. Chen, X. S. Wang, F. Zhang, C. Li, H. Tang, Y. Chengand A. Wang, “A systematic study of ESD protection co-design with high-speed and high-frequency ICs in 28 nm CMOS”, *IEEE Trans. Circuits and Systems I: Regular Papers*, *Vol. 63, No. 10,* pp. 1746-1757, October 2016.

[31] J.-R. Manouvrier, P. Fonteneau, C.-A. Legrand, P. Nouet and F. Azais, “Characterization of the transient behavior of gated/STI diodes and their associated BJT in the CDM time domain”, *Proc. IEEE EOS/ESD Symposium,* 2007.

[32] S. Thijs, K. Raczkowski, D. Linten, J.-C. Tseng, T.-H. Chang, M.-H. Song and G. Groeseneken, “CDM protection for millimeter-wave circuits”, *Proc. IEEE EOS/ESD Symposium,* 2011.

[33] K. Ma, K. Wang and K. S. Yeo, “Miniature passive structures, high frequency electrostatic discharge protection networks, and high frequency electrostatic discharge protection schemes”, *US Patent No: 9496253*, 2016.

[34] H. Mizutani and Y. Takayama, “DC-110-GHz MMIC traveling-wave switch”, *IEEE Trans. Microwave Theory and Techniques*, *Vol. 48, No. 5,* pp. 840-845, May 2000.

[35] A. S. Cardoso, P. Saha, P. S. Chakraborty, D. M. Fleischhauer, and J. D. Cressler, “Low-loss, wideband SPDT switches and switched-line phase shifter in 180-nm RF CMOS on SOI technology”, *Proc. IEEE Radio and Wireless Symposium*, pp. 199-201, 2014.

[36] M. Horstmann *et al.*, “Advanced SOI CMOS transistor technologies for high-performance microprocessor applications,” in *2009 IEEE Custom Integrated Circuits Conference*, 2009, pp. 149–152.

[37] Lin, K-Y., et al. "Millimeter-wave MMIC passive HEMT switches using traveling-wave concept." *IEEE Transactions on Microwave Theory and Techniques* 52.8 (2004): 1798-1808

[38] S. Voldman, *ESD Testing: From Components to Systems,* Wiley & Sons, 2017.

[39] H. Feng, et al, "A Mixed-Mode ESD Protection Circuit Simulation-Design Methodology", *IEEE J. Solid-State Circuits, Vol.38, No. 6*, pp. 995-1006, June 2003.

[40] F. Zhang, et al, "A Full-Chip ESD Protection Circuit Simulation and Fast Dynamic Checking Method Using SPICE and ESD Behavior Models", *IEEE Trans. on Computer-Aided Design of ICs and Systems,* 2018. **DOI:** 10.1109/TCAD.2018.2818707.

[41] C. Shaalini, et al "Failure analysis on 14 nm FinFET devices with ESD CDM failure", *Microelectronics Reliability* 88 (2018): 321-333.

[42] J. Karp, et al. "FinFET MPSoC 32 Gb/s Transceivers: Custom ESD protection and verification", *Proc. IEEE MWSCAS*, pp.1-4, 2016.

[43] M. Di, et al, "Misconception with Pad-Based CDM ESD Protection", *Proc. IEEE Electron Devices Technology and Manufacturing (EDTM) Conference,* pp. 266-269, 2020.

[44] N. Jack, "Charged Device Model ESD Protection and Test Methods for ICs", a PhD Dissertation, University of Illinois at Urbana-Champaign, 2012.

[45] K. H. Meng, et al, "Full-Component Modeling and Simulation of Charged Device Model ESD", *IEEE Trans. Computer-Aided Design of ICs and Systems, Vol. 35, No.7,* pp. 1105-1113, 2015.

[46] M. Di, C. Li, Z. Pan and A. Wang, "Pad-Based CDM ESD Protection Methods Are Faulty", *IEEE J. of Electron Devices Society, Vol. 8,* pp. 1297-1304, September, 2020, DOI: 10.1109/JEDS.2020.3022743.

[47] M. Di, Z. Pan, C. Li and A. Wang, "Internal-Distributed CDM ESD Protection", *Proc. IEEE EDTM*, pp.313-315, 2021, DOI: 10.1109/EDTM50988.2021.9421054.

[48] C. Li, Q. Chen, J. Ng, F. Zhang, H. Wang, M. Di, Z. Pan, T. Wu, K. Zhang, X. Xie, Y. Xie and A. Wang, "Design, Fabrication and Characterization of Single-Crystalline Graphene gNEMS ESD Switches for Future ICs", *IEEETrans. Device and Materials Reliability*, 2021, DOI: 10.1109/TDMR.2021.3090311.

[49] A. Wang, "Interposer-Based ESD Protection Structures", *US Provisional Patent App. No. 62/412,105*, 2016.

[50] A. Wang, “ESD Protection Structures Using TSV in ICs”, *US Provisional App. No. 62/385,770*, **2016.**

[51] T. Cilento, M. Schenkel, C. Yun, R. Mishra, J. Li, K. Chatty, R. Gauthier, “Simulation of ESD Protection Devices in an Advanced CMOS Technology Using a TCAD Workbench Based on an ESD Calibration Methodology”, *Microelectronics Reliability, 50,* pp. 1367-1372, 2010.

[52] C. Wang, F. Zhang, F. Lu, Q. Chen, C. Li, M. Zhao, H. Gu, G. Feng, H. Wu, T. Tang, Y. Cheng and A. Wang, “A Comparison Study of DTSCR by TCAD and VFTLP for CDM ESD Protection”, *Proc. IEEE International Symp. Physical & Failure Analysis of ICs (IPFA)*, 2017, **DOI:** 10.1109/IPFA.2017.8060146C.

[53] M. Di, Z. Pan, C. Li and A. Wang, “A New Multi-Stimuli-Based Simulation Method for ESD Design Verification”, *Proc. IEEE Electron Devices Technology and Manufacturing Conference (EDTM),* pp. 4-6, 2021, **DOI:** 10.1109/EDTM50988.2021.9420890.

[54] Y. Xue, “Correlation of Very Fast Transmission Line Pulse (VFTLP) and Field-Induced Charged Device Model (CDM) Testing”, *Proc. IEEE IPFA*, 2012, DOI: 10.1109/IPFA.2012.6306309.

[55] Zhang, Feilong, et al. "A 28GHz SPDT TRx Switch with 9KV ESD Protection in 22nm SOI CMOS for 5G Mobiles," *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Jose, CA, USA, 2019, pp. 1-2, doi: 10.1109/S3S46989.2019.9320736.

[56] Wang, Chenkun, et al. "A study of interferences inside an RF switch array in 45nm SOI CMOS." *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*. IEEE, 2017.

[57] L. Lin, R. Gauthier, A. Loiseau and X. Lu, "Design Optimization of a Breakdown Silicon Controlled Rectifier (BDSCR) for Cell Phone Antenna Switch Pin Electrostatic Discharge (ESD) Protection," *2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, Reno, NV, USA, 2018, pp. 1-8, doi: 10.23919/EOS/ESD.2018.8509768.

[58] Li, Chaojiang, et al. "1W< 0.9 dB IL DC-20GHz T/R switch design with 45nm SOI process." *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, 2017.