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Integrated Neural Interfaces

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***Abstract*—Electronic interfaces to the nervous system are increasingly important for experimental neuroscience as well as medical diagnostics and therapies. Existing neural interfaces are limited, however, by the use of passive recording and stimulation devices that are connected to active electronics on separate physical platforms through large amounts of passive wiring. This manuscript proposes a new approach to integrate active electronics directly with neural recording and stimulation devices using state-of-the-art silicon processing, assembly, and packaging techniques. System concepts are described for fully wireless operation as well as wireline interfacing through FDA-cleared implantable leads and connectors. The approach offers a more modular paradigm of neural interface design, which is greatly needed as the demand for higher channel counts grows.**

Keywords—neural interface, implantable device, neural recording, neural stimulation, neural amplifier, packaging and assembly, heterogeneous integration

I. Introduction

Neural interfaces that connect electronic systems with biological neurons have emerged as a major topic of research in the last decade [1], impacting fields ranging from electrical and biomedical engineering to neuroscience and medical practice. Our capability to record from and stimulate individual neurons has progressed from single-cell experiments to interfacing with a few hundred neurons simultaneously, largely driven by microfabrication of neural recording and stimulation devices comprising arrays of sensors and/or actuators arranged in separate channels [2]. While the most ubiquitous interface technology may arguably be microfabricated silicon electrode arrays used for electrical recording and stimulation, optical and magnetic interface modalities are also very important and can enable single-cell specificity and large-scale sensing to degrees that are impractical with electrode-based interfaces [3].

Currently, the field is progressing toward separate but inter-related goals for i) experimental neuroscience, and ii) medical devices. Common themes in both areas include interfacing with larger populations of neurons [3], and achieving robust operation while subjects behave naturally in dynamic, real-world environments [4]. For example, the USA's BRAIN Initiative calls for recording and stimulation of 1,000,000+ independent sites, simultaneously, as well as unconstrained experimental paradigms that shed light on the relationships between neural activity and behavior, motivating fully wireless operation (e.g. Fig. 1). Unfortunately, implantable electronic systems needed to support these goals are generations behind, whether the interface is electrical, optical, or otherwise.

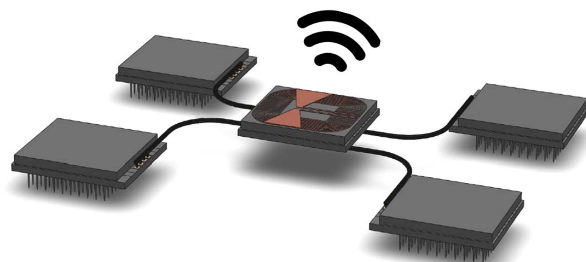

Fig. 1. Multi-platform wireless neural interface concept (illustration)

A long-standing problem has been integration of active electronics with neural recording and stimulation devices. Efforts have been made to combine electronics with both rigid and flexible materials that act as substrates for recording and stimulation sites [5]–[13], but the community still lacks a platform technology of this nature that is robust, accessible, and extensible. Existing devices have proven to be difficult and expensive to create, requiring multidisciplinary expertise in materials, physiology, and electronics. Key challenges are i) the scale of electronics required to enable highly functional systems with many channels, and ii) guaranteeing that integrated neural interfaces can last in implanted environments for long periods of time without suffering failures from packaging, wires, and bio-response. These challenges still exist despite extensive work on neural interface electronics [14]–[16], as well as monolithically integrated CMOS-compatible silicon electrode arrays [7], [12], and is reflected by the lack of publications that demonstrate chronic operation of integrated neural interfaces. For the purposes of this discussion, we will define *chronic* to imply usability over periods of at least several months, without surgical revision. The requirement for chronic medical use, of course, is generally longer (5-10 years).

While some neural interface technologies are now considered mature, for example "neural amplifiers" and silicon electrode arrays, existing solutions do not readily scale to contemporary goals for channel counts, which they were not originally designed for. Hence, the community needs to rethink neural interface technology, representing a wealth of opportunity for electronic circuit and system designers in particular. This article describes a new "Chiplet" approach to integrated neural interfaces that creates modularity, reduces design time and effort, removes failure modes, and facilitates sharing and deployment of technology from different sources. Compared to similar efforts [5], [8], [10], [13], this approach breaks a large multichannel ASIC design into much smaller Chiplets that offer greater modularity and more potential for system optimization, enabled by state-of-the-art assembly and

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packaging. The Chiplet approach is described here in the context of silicon electrode arrays, but has broad implications for other types of electrodes, optogenetic interfaces, and *in vivo* imaging. These technologies all generally require fully implantable electronics placed close to the sensing/actuating elements in order to achieve robust operation in real-world environments with mobile subjects and patients.

Section II presents background information on neural interfaces, Section III describes our heterogeneous Chiplet integration approach and Section IV concludes the paper.

II. Background

Neural interfaces generally require active electronics for acquiring neural signals, stimulating neurons, communicating data, and managing power. These electronic functions may be distributed across diverse platforms, e.g. on the interface device itself [12], in head-mounted systems [4], [16], and/or bench-top instruments. Fully implantable active electronics are becoming critical for streamlining the overall system, allowing multiplexing of acquired data and stimulation commands onto a handful of wires, or wireless channels. Active multiplexing is increasingly required as channel counts grow, since passive wiring poses severe limitations to reliability, lifetime, and size. Wires and connection points fail, they couple forces to implanted devices that exacerbate biological response, they create pathways for infection, interference and crosstalk, and present surgical complications from stiffness and size [2], [17]. For chronic applications, it's impractical to interface devices with thousands of channels or more with one-wire-per-channel architectures that connect neural recording and stimulation sites to electronics on other physical platforms.

For these reasons, there is great motivation to create neural interfaces that integrate active electronics close to the recording and stimulation sites. Currently, neural interfaces used in chronic experiments are passive and rely on large bundles of wires that limit channel counts to a few hundred [2], [17]. While active neural interfaces have been pursued for a surprisingly long time, to date there are still no reports of miniaturized, chip-scale devices remaining useable for periods of months or years. In contrast, passive intracortical microelectrode arrays have remained functional in non-human primate subjects for up to six years [18], albeit with a maximum of ~100 channels. To move the field forward, platform technology must be invented to integrate active electronics with neural recording and stimulation arrays with high reliability, and low overhead in size and complexity. This effort is especially important for scaling channel count and density to current goals (100-1000 chs/mm^2 [12], [19]–[21]).

The main challenges involved in designing next generation integrated neural interfaces are i) the scale of electronics required for interfacing with hundreds or thousands of channels, ii) reliability and yield in physically integrating the interface electronics with neural recording and stimulation devices, iii) hermetic packaging of the electronics to prevent fluid infiltration over long periods of time, and iv) robust and high performance communication and power interfaces.

Most previous efforts have focused on monolithic approaches [6], [7], [11]–[13], where extensive multichannel circuitry is designed into one large chip that is integrated with arrays of sites on separate substrates (heterogeneous) or on the chip itself (homogenous). Monolithic integration, however, is cumbersome and rigid because all functions must be designed into a single chip in a single process technology. Furthermore, larger and larger chips complicate physical integration and pose yield and reliability problems since single defects can render the entire system unusable. These same issues have caused the semiconductor industry to shift toward integrating multiple chips into single packages (e.g. in FPGA technology), facilitated by silicon interposer substrates that contain low parasitic, chip-scale interconnect [22]. We propose to extend this approach by breaking apart a large, monolithic ASIC into many small Chiplets, creating a new modular paradigm of neural interfaces that allows designers to mix and match electronic functions and rapidly produce systems that are customized to particular applications. The approach is based on physical processing techniques that reliably integrate dozens or hundreds of Chiplets without significant performance penalties in size, power consumption, or signal fidelity.

III. Chiplet Integration Approach

A. Architecture and Physical Integration

Fig. 2 shows an illustration of the Chiplet integration approach, applied to the commonly used 100-channel Utah Electrode Array (UEA) [2]. While the UEA is shown here for demonstration purposes, the Chiplet approach and integration technology is widely applicable to other types of microelectrode arrays (flexible and rigid), as well as emerging optical arrays and *in vivo* imaging systems.

Separate, fine-grained Chiplets are used for front-end signal conditioning (blue), column-parallel analog to digital conversion (red), electrical stimulation (yellow), and system control, power management, and communication (black). The Chiplets are integrated with the microelectrode array through thermal compression flip-chip bonding [23], [24] onto redistribution layers (RDLs) on the backside of the array, which support chip-scale routing with low parasitics. The RDLs are fabricated with back-end-of-line techniques used for silicon interposers [22]. Similar integration technology is already being used in high performance FPGAs and RF microsystems for high-speed signal connectivity and power distribution. 2.5D integration techniques are also applicable, e.g. vertical stacking of stimulation and recording Chiplets supported by through-silicon-vias (TSVs) [25]. Overall system size can be reduced through thinning the Chiplet dice (e.g. to ~100 µm). The electronics are hermetically sealed with a silicon lid fabricated with reactive ion etching and bonded to the array substrate with a reflow solder process [26].

The key new idea is to break apart a large, monolithic ASIC into small Chiplets that can be mixed and matched in different geometries, to support diverse types of neural recording and stimulation devices. This approach will provide a greatly needed modular paradigm to neural interface design that is customizable, extensible, and standardized. Additional functions can be easily added without redesigning the entire system, e.g. a local signal processing Chiplet for spike detection or sorting, compression of raw data, etc. This

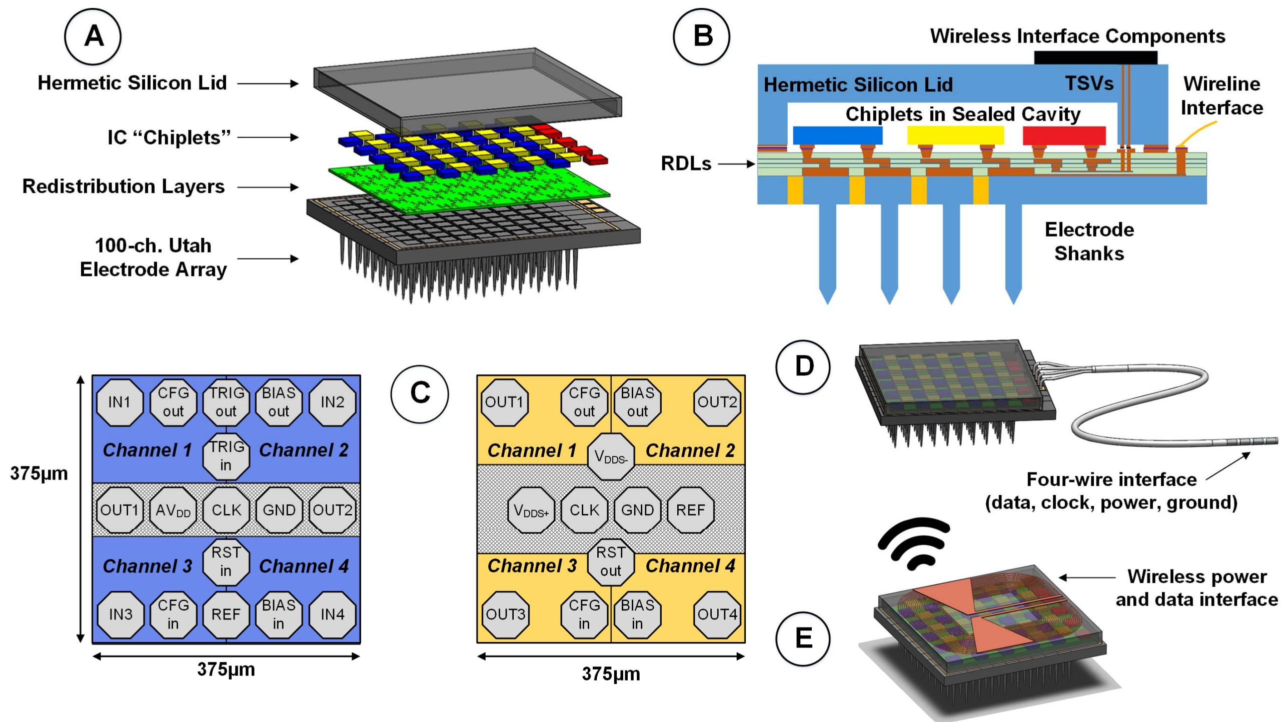

Fig. 2. Chiplet integration approach applied to the standard 100-channel Utah Electrode Array. Exploded assembly drawing (A), scaled-down cross section of assembled device (B), example floorplans for signal conditioning and stimulation Chiplets (C), assembled devices with multiplexed wireline interface using a FDA-cleared neuromodulation lead [28] (D), assembled device with wireless interface using a coil and antenna integrated on the lid (E).

extensibility can be achieved through design rules for pad placement on the Chiplets, conforming to a standardized routing grid for power and signal lines in the RDL, as well as electrical specifications for compatibility with other Chiplets. Fig. 2C shows example floorplans of signal conditioning and stimulation Chiplets, where standard-size flip-chip bondpads (70x70 μm^2) are used for connectivity. Integrating four channels per Chiplet alleviates overhead from the bondpads, and facilitates assembly while offering a suitably fine-grained implementation. More aggressive fine-pitch bondpad schemes are possible with advanced processing techniques [23]. From a circuit perspective, potential limitations stem from parasitic capacitance incurred by bondpads, ESD diodes, and routing in the RDL. These parasitics can be made quite small, as the RDL contains chip-scale routing similar to what would be needed in a monolithic ASIC (~0.1 fF/µm wiring parasitics), and ESD constraints are relaxed compared to fully packaged chips.

B. Communication and Power Interfaces

The ultimate goal of the Chiplet approach is fully wireless operation of implanted neural interface modules (Figs. 1 and 2E) that are free of problem-causing percutaneous leads and connectors [17]. Wireless operation is key for experimental neuroscience with freely behaving subjects [4], as well as potential translation to human use [27]. However, we have also been exploring high-speed serial communication over FDA-cleared implantable leads and connectors that are commonly used in cardiac pacing and neuromodulation applications [28] (Figs. 2D and 3). These multi-conductor leads and connectors have been developed over the course of decades [29], and are optimized for biocompatibility and robust operation in chronic implant environments. Using this type of interconnect to interface with many channels relies on implantable electronics to serialize/deserialize and transmit/receive data, e.g. implemented in a Chiplet that performs system control, communication, and power management (Fig. 2). Replacing high channel count passive wire bundles with a robust, connectorized serial link has major advantages for system reliability and surgical implications, which currently limit chronic channel counts to a few hundred.

Robust implantable interconnect is useful both as a stepping stone in the development of wireless implants, as well as a subcomponent in wireless systems themselves. For example, Fig. 1 shows a wireless system concept that employs multiple neural interface modules connected to a centralized wireless hub through four-conductor neuromodulation leads that support data, clocking, power, and ground connections. These wireline connections can enable operation of submodules spread across distant regions of the body, including deep structures that are difficult to interface with wirelessly due to attenuation of radiated electromagnetic energy [30] or reflection of acoustic waves by bone [31]. Compared to wireless interfacing, wirelines generally offer higher data rates, lower power consumption, enhanced reliability and security, and extended reach.

Fig. 3 shows eye diagrams measured at the receiver of a one meter long serial link implemented with a connectorized neuromodulation lead in a bench-top saline test setup used to emulate an implanted environment (described in [28]). Using

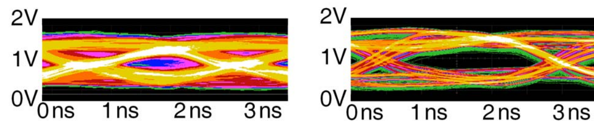

Fig. 3. Measured eye diagrams of a 1 meter serial link implemented with a Medtronic 37081 neuromodulation extension lead [28]. This biocompatible interconnect is optimized for implantation (see Fig. 2D). Measured eye diagram at 400 Mbps in saline solution without equalization (left), and with three-tap feedforward transmitter equalization (right).

three-tap feedforward equalization at the transmitter we achieved a 400 Mbps data rate over one pair of conductors, with a bit error rate $<10^{-12}$. This rate is large enough to transmit over 1000 channels of neural data acquired with typical parameters (10 bit resolution at 30 kS/s/channel).

IV. CONCLUSIONS

This manuscript proposes a modular "Chiplet" paradigm of integrated neural interfaces for heterogeneous physical integration of active electronics with neural recording and stimulation devices. The modularity offers flexibility in large-scale neural interface design, the ability to test system components individually before integration, relaxed tolerances for physical integration, and an avenue for sharing and reuse of integrated circuit technology that breaks the constraints of large, monolithic ASICs. The Chiplet approach leverages state-of-the-art silicon processing and assembly techniques that were developed in the semiconductor industry to provide an alternative path to system scaling that utilizes smaller chips.

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