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Dynamical Modeling and Control of the Flying Capacitor Multilevel Converter in
High-Density, High-Efficiency AC/DC and DC/AC Applications

By

Roderick Sterndale Bayliss III

A dissertation submitted in partial satisfaction of the

requirements for the degree of

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in

Engineering – Electrical Engineering and Computer Sciences

in the

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of the

University of California, Berkeley

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Roderick Sterndale Bayliss III

Abstract

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Professor Robert Pilawa-Podgurski, Chair

Power electronics that are extremely energy efficient and power dense are becoming increasingly required for critical applications such as data center power delivery, renewable energy, and electric transportation. This dissertation primarily investigates a power conversion topology which leverages physical scaling laws to achieve higher performance power conversion, the flying capacitor multilevel (FCML) converter. The FCML converter utilizes low voltage semiconductor switches and energy dense capacitors to enable more energy efficient and more power dense converters.

Successful FCML converter operation, however, is contingent upon the flying capacitor voltages within the converter being at well-defined voltages (so called balanced flying capacitor voltages). If the balanced flying capacitor voltage distribution is not maintained, switch voltage stress and inductor volt-second stress are significantly increased. This thesis addresses the problem of flying capacitor voltage balance through several avenues. First, the impact of the semiconductor switch parasitic output capacitance C_{oss} on the flying capacitor voltage balance is elucidated through analytical modeling. The charge flow quantities induced by the switch C_{oss} are found to have a naturally balancing effect on the flying capacitor voltages. Second, active flying capacitor voltage balancing controllers are developed for applications where the flying capacitor voltage requirement is particularly challenging to adhere to. These applications require flying capacitor voltage references which vary at hundreds of volts and at frequencies in the hundreds of hertz, an atypical and hard to achieve requirement. Finally, recommendations for future directions of research are provided.

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Chapter 1

Introduction

1.1 Background

Power electronic converters play critical roles in applications that require high-performance processing of electrical energy such as data centers, electric vehicles, and renewable energy. Power electronic designers must constantly improve the energy efficiency, reduce the size and cost, and maximize the reliability and transient response capability of their power converters for increasingly demanding applications. Power electronics is a wonderful art requiring the mastery of the domains of circuits, controls, electromagnetism, heat transfer, high frequency mixed-signal design, among other disciplines.

This dissertation focuses on one topology which leverages several key physical component characteristics to improve power conversion performance: the flying capacitor multilevel (FCML) converter, introduced in 1992 [1]. The topology has shown promising performance in single-phase dc/ac inverters [2], [3], [4], [5] and dc/dc converters [6]. Although the topology was initially developed to remedy the lack of high voltage switches in high voltage power conversion applications [1], the FCML converter has been shown capable of outperforming conventional topologies in lower voltage applications.

The flying capacitor multilevel (FCML) is a converter topology which leverages an energy storage discrepancy between capacitive and inductive energy storage and low voltage semiconductor switches to enable power converter designs showcasing higher power density and efficiency.

Passive components, that is inductors, transformers, and capacitors, often dominate the volume and mass of power electronic converters. Therefore, particular attention must be paid to passive components to improve converter size and weight. There is, however, a large asymmetry in the performance of electrical energy storage between these components. Fig. 1.1 illustrates the volumetric energy density of a commercial survey of inductors and capacitors, from the authors of [7]. As can be observed, the most energy dense capacitor is approximately a factor of 1000 more energy dense than the most dense inductor.

The second physical asymmetry the FCML converter leverages is the relative performance

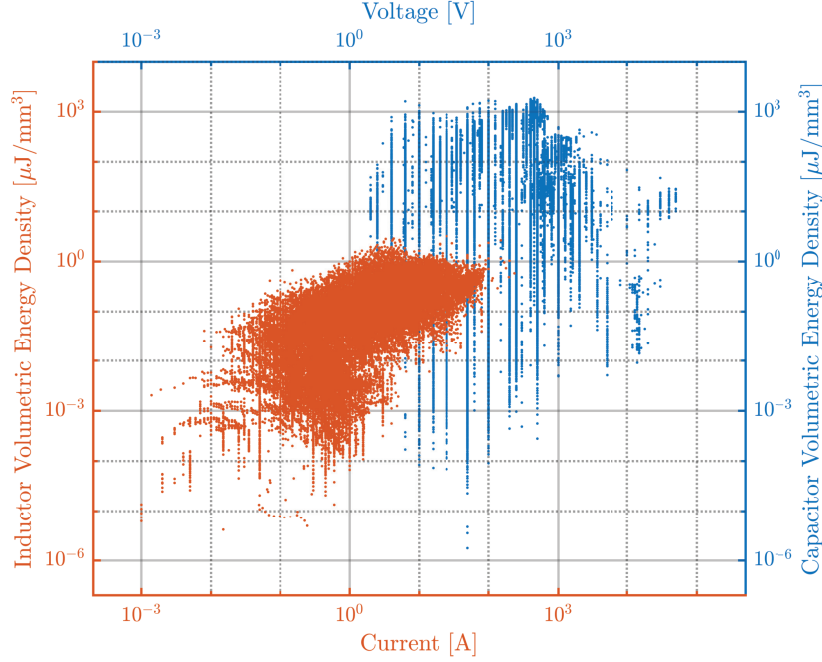


Figure 1.1: Volumetric energy density of commercially available capacitors and inductors surveyed in [7]. The inductor energy is calculated as $LI^2/2$ while the capacitor energy is calculated as $CV^2/2$ where I is the maximum current able to be processed by the inductor and V the maximum voltage able to be processed by the capacitor. Of note is that the most energy-dense capacitor has an energy density approximately a factor of 1000 larger than the most energy-dense inductor.

of low voltage semiconductor switches. As analyzed in [8], [9], semiconductor switches rated for lower blocking voltages outperform semiconductor switches rated for higher blocking voltages. The switch area-specific ON-resistance R'_{on} and area-specific charge-equivalent output capacitance C'_Q [10] scale via a power law relationship with the switch blocking voltage (i.e., $R'_{\text{on}} \propto V_{\text{ds}}^{\alpha_R}$ and $C'_Q \propto V_{\text{ds}}^{\alpha_C}$ where $1.1 < \alpha_R < 2.5$ and $-1.6 < \alpha_C < -0.7$ depend on the semiconductor technology). As derived in [8], [9], these power law relationships imply that a series connection of M low voltage switches blocking some dc bus voltage V_{dc} (and thus rated for at least V_{dc}/M) will attain a lower semiconductor loss than a single switch which blocks the entire dc bus voltage. In general, a simple series connection of low voltage switches is hard to achieve practically as auxiliary circuits or controllers must ensure the voltage across each switch is shared evenly, preventing any one switch from suffering an over-voltage event.

A schematic drawing of a six-level FCML converter is provided in Fig. 1.2. Typical FCML converter operation requires that the flying capacitor voltages $v_{C,k}$ are at a “balanced” distribution with $v_{C,k} = kV_{\text{in}}/(N-1)$ where N is the level count of the converter. The level count defines the “order” of the topology where an N -level FCML converter has $N-1$ switch pairs ($S_{H,i}/S_{L,i}$), $N-2$ flying capacitors, and N voltage levels present in the switch node voltage v_{sw} . When the flying capacitor voltages attain the balanced voltage distribution, the

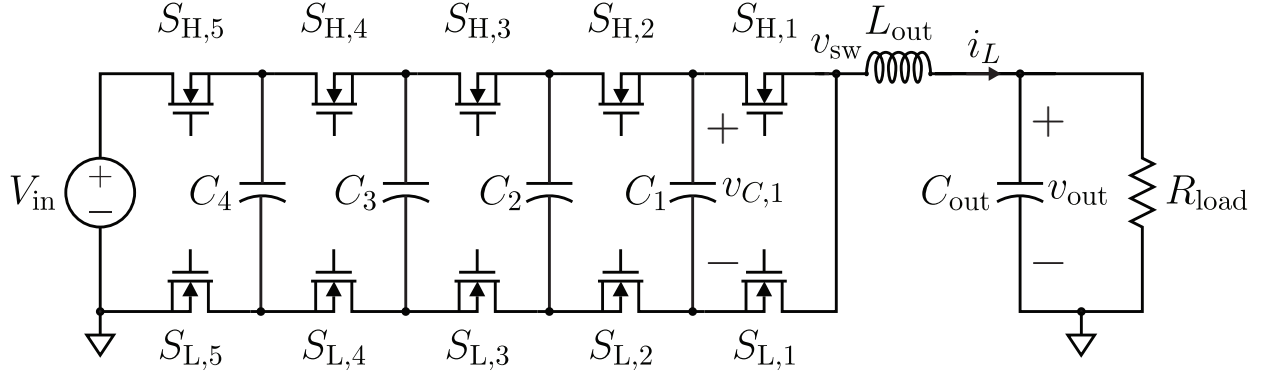


Figure 1.2: Schematic drawing of a six-level flying capacitor multilevel (FCML) converter. The flying capacitors C_1 through C_4 enable equal distribution of the input voltage stress across the semiconductor switches and reduce the volt-seconds applied to the output inductor L_{out} . The FCML converter is the primary converter under investigation for this dissertation.

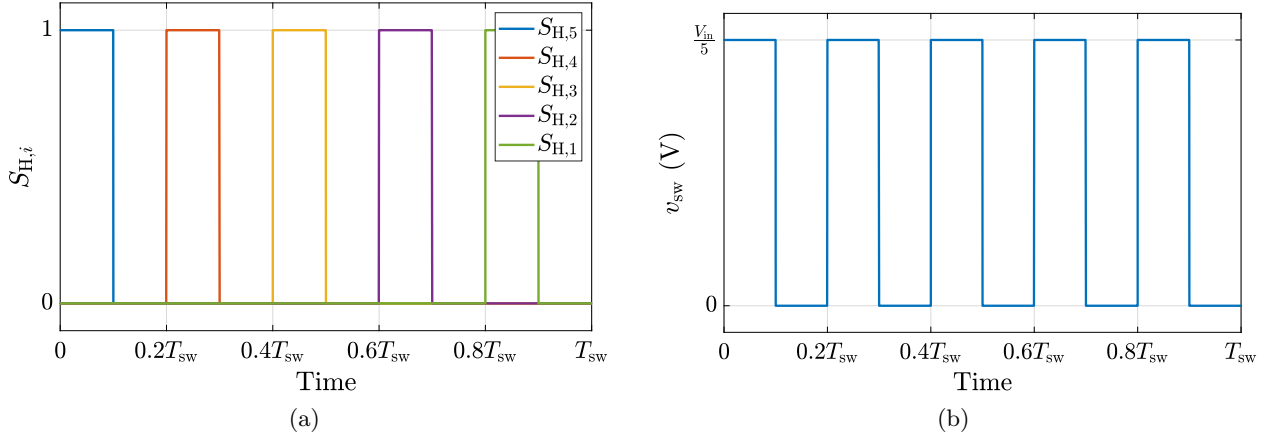


Figure 1.3: (a) Symmetric Phase Shifted Pulse Width Modulation (PS-PWM) gating signals for the high side transistors $S_{H,i}$ for a six-level FCML converter operating at a duty cycle of $D = 10\%$. (b) Switch node voltage v_{sw} for the six-level FCML converter when the flying capacitor voltages are balanced and have negligible voltage ripple. The output voltage is 10 V, the average inductor current is 10 A, and the output power is 100 W.

switch blocking voltage stress is minimized at $V_{in}/(N - 1)$ and the volt-seconds applied to the inductor L_{out} is also minimized.

Symmetric phase shifted pulse width modulation (PS-PWM) [1] is the most common modulation scheme for the FCML converter. For symmetric PS-PWM operation, all high side switches $S_{H,i}$ are gated with a signal with the same duty cycle D and the high side switching signals are circularly phase shifted throughout the switching period (with phase shift $360^\circ/(N - 1)$). The low side transistors $S_{L,i}$ are gated with the complement of the high side signal. Fig. 1.3 shows the high side gating signals and the switch node voltage v_{sw} for a six-level FCML converter where the flying capacitor voltages are balanced. Fig. 1.4 provides the input and flying capacitor voltages and inductor current when the flying capacitor

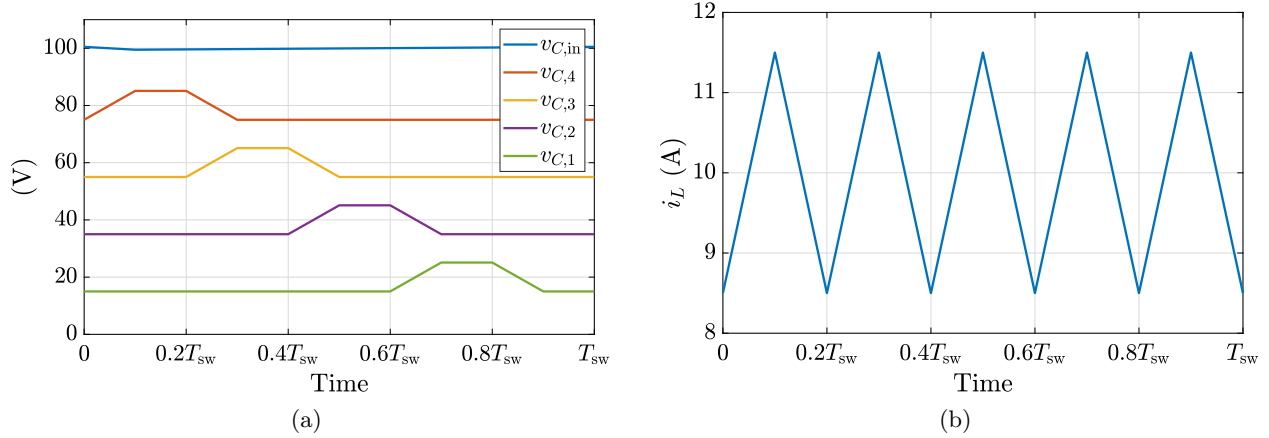


Figure 1.4: (a) Input and flying capacitor voltages for a six-level FCML converter. The flying capacitor mid-range voltages are “balanced” when they achieve distribution $v_{C,k} = kV_{in}/(N - 1)$ where N is the level count of the converter. (b) Inductor current i_L for the six-level FCML converter. The inductor current is periodic with frequency $5f_{sw}$ when the flying capacitor voltages are balanced where f_{sw} is the switching frequency.

voltages are balanced.

One key concern in utilizing the FCML converter is the flying capacitor voltage distribution. If the balanced flying capacitor voltage distribution is lost, the switch blocking voltage stress increases (potentially catastrophically) and inductor volt-second stress is heightened. Allotting for increased switch voltage headroom or increased inductance to counteract the aforementioned drawbacks of flying capacitor voltage imbalance can seriously degrade the FCML converter performance. This dissertation primarily focuses on the flying capacitor voltages within the FCML converter, developing models for how they naturally evolve and depend on system parameters and developing controllers for FCML converters which have stringent flying capacitor voltage requirements.

1.2 Organization of Thesis

Chapter 2 discusses the impact of the switch parasitic output capacitance C_{oss} on flying capacitor voltage balancing in the FCML converter. This chapter develops an analytical description of the C_{oss} -induced charge flow quantities and their impact on the flying capacitor voltages. These charge flow quantities are shown to have a negative feedback and naturally balancing effect on the flying capacitor voltages. Inclusion of the impact of C_{oss} on the flying capacitor voltages is particularly important for conversion ratios where contemporary converter models are unable to predict the flying capacitor voltage distribution (e.g., at a duty cycle of 50% for a five-level FCML converter).

Chapter 3 discusses a buck-type power factor correction (PFC) architecture for step-down grid-tied rectifiers. Buck-type PFC converters are able to implement single-stage rectification for many single-phase rectifiers. The FCML converter is considered as a topology

to implement the architecture, leveraging the topology's inherent utilization of low voltage semiconductor switches and reduced magnetic volume to create an overall high performance power conversion system. To utilize the FCML converter in a buck-type PFC, however, the flying capacitor voltages must vary by hundreds of volts at frequencies of hundreds of hertz to maintain flying capacitor voltage balance. To achieve flying capacitor voltage balance in this application, an active flying capacitor voltage balancing controller is developed which operates in tandem with the inductor current controller.

Chapter 4 discusses a topological variant of the output-inductor FCML topology introduced in the Chapter 3, an *input-inductor* FCML converter for buck-type PFC converters. The input inductor FCML converter is able to maintain the benefits of reduced magnetic volume and utilization of low voltage switches while additionally reducing the input current and thus grid current filtering requirements.

Chapter 5 discusses an FCML buck-boost converter to perform single-stage inversion for a photovoltaic micro-inverter. Compared to the buck-type PFC converters discussed in Chapters 3 and 4, the converter in this chapter includes the capability to both buck and boost the input voltage to further improve grid current quality. This chapter also analyzes and proposes compensation schemes for the reactive power flow within the converter due to the flying capacitors.

Chapter 6 discusses an eight-level, three-phase rectifier for high performance, high voltage ac/dc rectifiers. This chapter investigates the modulation techniques, EMI filter design, and control architectures required to practically realize the FCML topology for this application.

Chapter 7 discusses a capacitively-isolated, high-step-down ratio dc/dc converter utilizing the FCML converter. The natural voltage-division performed by the FCML converter works synergistically with a series resonant tank to create a high-step-down ratio dc/dc converter.

Chapter 8 investigates motor drive systems and active input filters. The circuit analyzed in this chapter is found to be particularly useful for multi-drive system architectures (e.g., electric vehicles, spacecraft) where physical system design may result in resonances which are easily excited by nominal system operation.

Finally, Chapter 9 concludes the thesis. Schematics of implemented prototypes and software used in analysis and firmware used in the implemented controllers are provided in the Appendices.

Chapter 2

On the Role of Switch Output Capacitance on Passive Balancing within the Flying Capacitor Multilevel Converter

Portions of this chapter are adapted in part or in whole from [11].

2.1 Introduction

A key practical challenge in the utilization of high-performance FCML converters is the voltage balancing of the flying capacitors, the focus of this chapter. Specifically, this chapter demonstrates the effect of transistor output capacitance C_{oss} on natural flying capacitor voltage balancing, and derives key equations along with experimental validation.

Several works [12], [13], [14], [15] have discovered “unbalanced” conversion ratios, at which the flying capacitor voltages theoretically do not passively balance to their desired steady-state values and instead diverge. These “unbalanced” conversion ratios are defined as conversion ratios where $D \cdot (N - 1)$ and $(N - 1)$ are not co-prime, where D is the duty cycle of the high-side switches $S_{H,k}$ in the FCML converter operated with symmetric phase-shifted PWM (PS-PWM), and where $D \cdot (N - 1)$ is an integer. Of note, however, is that these theoretically unbalanced operating points and divergent flying capacitor voltages are not typically observed in experimental hardware [13], pointing to a gap in the understanding of all pertinent balancing mechanisms within the converter. Of particular interest in this work is the combination of a five-level FCML converter operated at a duty cycle of $D = 50\%$ as it is the simplest FCML converter which exhibits this theoretical behavior.

This work analyzes the natural balancing of the capacitor voltages in an FCML converter, and extends past work to also include the impact of switch output capacitance. Crucially, it is discovered that the transient charge flow between flying capacitors and parasitic switch

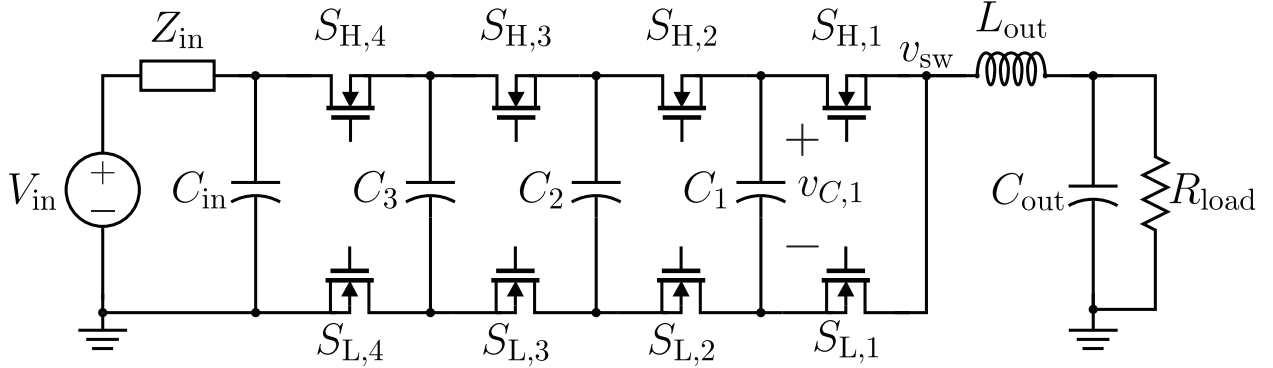


Figure 2.1: Simplified five-level FCML converter circuit schematic with input impedance explicitly drawn. The ground-referenced switch-node voltage v_{sw} is explicitly labeled.

output capacitance C_{oss} during switch transitions has a naturally balancing effect, which has previously not been documented. A detailed state-space model is developed to include this balancing mechanism, and through hardware validation, it is shown that the proposed model accurately captures the experimental behavior, which was not achieved by previous models.

This work has two key contributions: 1) Identification of the role of the switch output capacitance in the natural balancing of the flying capacitor voltages, along with an analytical expression of the strength of the balancing mechanism. 2) Development of an analytical model incorporating said balancing mechanism, which shows excellent agreement with experimental results. Together, these two contributions yield — for the first time — a model of FCML converter natural balancing that matches experimental observations during practical operating conditions (e.g., start-up transients).

2.2 Flying Capacitor Multilevel Converter Balancing Mechanisms and Unbalanced Conversion Ratios

The promise of the FCML topology to enable the incorporation of high-performance low-voltage switches [8] with an even voltage stress distribution requires that the voltages of the flying capacitors not deviate too far from their ideal distribution. If this constraint is violated, the system efficiency will decrease and in the worst case, the switches will be exposed to a voltage higher than their ratings, yielding converter failure.

Previous works [12], [13], [15], [16], [17], [18], [19] have analyzed the mechanisms by which the flying capacitors within an FCML converter converge to the balanced steady-state voltage distribution $v_{C,k} = (kV_{in})/(N - 1)$ where N is the number of discrete levels in the switch node waveform, and k ranges from 1 to $N - 2$, with capacitor voltages as annotated in Fig. 2.1. [1] demonstrates that with symmetric Phase-Shifted PWM (PS-PWM) modulation, the flying capacitor voltages dynamically balance to the aforementioned voltage distribution. Furthermore, if the high-side switches $S_{H,k}$ are operated with a duty cycle D , and the low-side

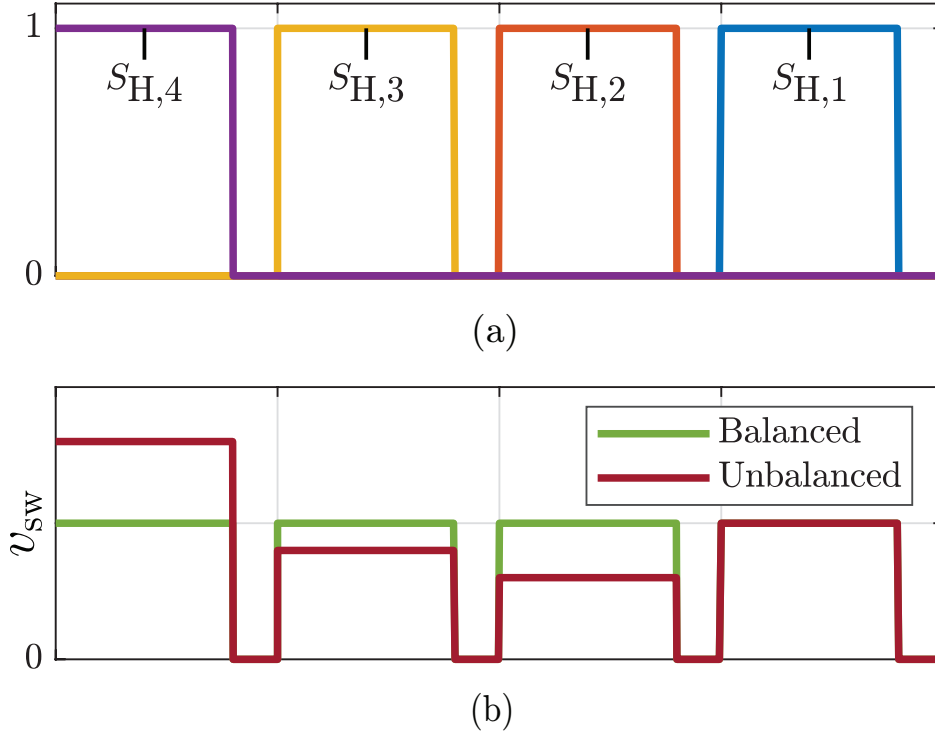


Figure 2.2: (a) Example symmetric phase-shifted PWM (PS-PWM) switching signals for a five-level FCML converter operated at a duty cycle $D = 0.2$. (b) Switch-node voltage v_{sw} resulting from both a balanced and an example unbalanced flying capacitor voltage distribution. When the flying capacitor voltages are balanced, the voltage stress applied to the switches and the volt-seconds applied to the output filter inductor are minimized. The unbalanced case shown has flying capacitor voltages of $v_{C,1} = 0.25V_{\text{in}}$, $v_{C,2} = 0.4V_{\text{in}}$, and $v_{C,3} = 0.6V_{\text{in}}$.

$S_{L,k}$ switches in a complementary fashion, the output voltage will be $V_{\text{out}} = D V_{\text{in}}$. Example switching signals and switch node voltages for balanced and unbalanced flying capacitor voltages are shown in Fig. 2.2.

When the flying capacitor voltages are balanced, the lowest frequencies present in the switch node waveform are dc and $(N - 1)f_{\text{sw}}$. According to previous analyses [13], [20], natural balancing occurs because unbalanced flying capacitor voltages create a switch node voltage which has harmonic content between f_{sw} and $(N - 2)f_{\text{sw}}$, as can be seen in Fig. 2.2. When these “lower-order” voltage harmonics are present, they induce current and losses in the RLC circuit of the output filter. These losses work to drive the flying capacitor voltages to their balanced distribution. However, at certain combinations of level count and duty cycle, the flying capacitor voltages are unable to be independently impacted by the RLC circuit dynamics of the output filter [14], [15] and thus natural balancing fails. Fig. 2.3 shows the equivalent circuits for a five-level FCML converter operated with symmetric PS-PWM at a duty cycle of 50%. At this operating point, it can be seen that capacitors C_1 and C_3 are always connected in series when connected to the output filter. Since these flying capacitor voltages cannot be independently changed, the flying capacitor voltages theoretically will

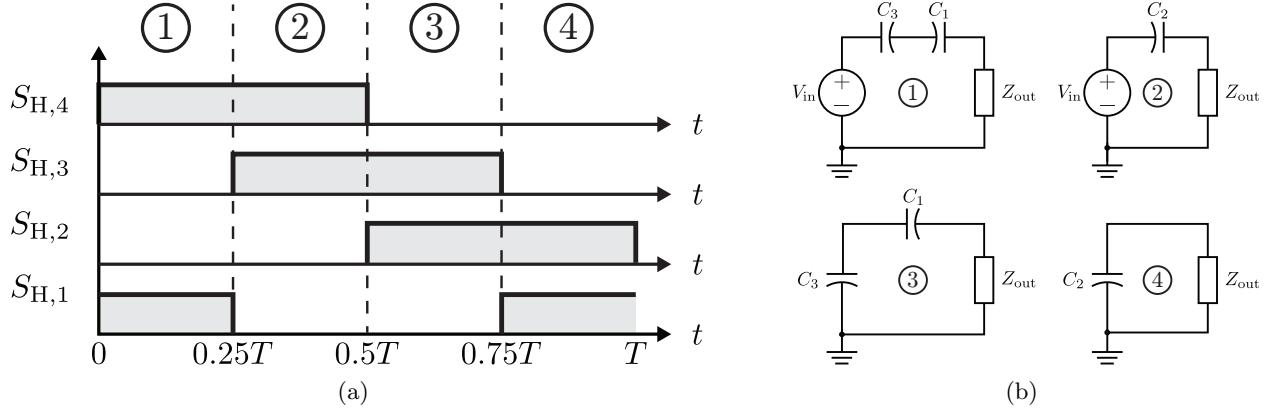


Figure 2.3: (a) Gate signals for a five-level FCML converter operated with PS-PWM at a duty cycle of 50%. (b) Equivalent circuits of the FCML converter. Z_{out} represents the impedance of the output filter inductor and capacitor and load resistance as connected in Fig. 2.1.

not balance.

2.3 Switch Output Capacitance (C_{oss}) Impact on Flying Capacitor Natural Balancing

To resolve the discrepancy between previous literature and experimental evidence regarding natural balancing at the “unbalanced” conversion ratios [13], [15], there must exist some mechanism not included in the aforementioned works’ simplified model of the FCML converter that acts to drive the flying capacitor voltages to the balanced state, even at “unbalanced” conversion ratios. One such mechanism not previously modeled is charge redistribution induced by the switch parasitic output capacitance. During each switching event, the output capacitance C_{oss} of a switch which was previously on is charged from ≈ 0 V to a linear combination of the flying capacitor voltages and the input voltage. For example, when $S_{H,2}$ switches from ON to OFF and $S_{L,2}$ switches from OFF to ON, the C_{oss} of $S_{H,2}$ is charged from ≈ 0 V to $v_{C,2} - v_{C,1}$. Similarly, the C_{oss} of $S_{H,1}$ will be charged from ≈ 0 V to $v_{C,1}$ when $S_{H,1}$ switches from ON to OFF. As will be shown in the subsequent analysis, these previously unmodeled charge flows due to C_{oss} are functions of the flying capacitor voltages and provide an inherent balancing mechanism in the FCML converter.

2.3.1 Charge Flow Analysis

To provide a tractable, analytical description of this charge flow mechanism, we make the following simplifying assumptions: 1) all switches are commuted with zero dead-time and in perfect complementary fashion, and 2) the flying capacitors and C_{oss} parasitic capacitances are linear. These simplifying assumptions will be examined and re-evaluated in Section 2.3.3. Examining the switching event illustrated in Fig. 2.4, at $t = 0$, $S_{H,2}$ opens and $S_{L,2}$ closes. The

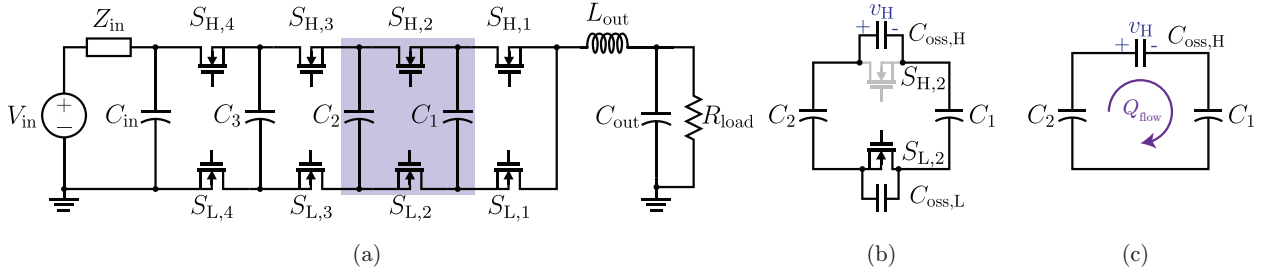


Figure 2.4: (a) Simplified five-level FCML converter circuit schematic with source input impedance explicitly drawn and switching cell 2 highlighted. (b) Switching cell 2 with switch output capacitances C_{oss} explicitly drawn. At $t = 0$ a commutation of the S_2 switching cell occurs, with $S_{H,2}$ turning OFF and $S_{L,2}$ turning ON. (c) Equivalent circuit after $t = 0$ for analyzing commutation charge flow. Charge quantity Q_{flow} circulates around the commutation loop, discharging C_2 and charging C_1 and $C_{\text{oss,H}}$. Parasitic resistances are omitted for clarity.

charge quantity circulating during this commutation event can be expressed in terms of the flying capacitor voltages at $t = 0$ and $t = t_f$, where t_f is the time at which the system voltages have approximately settled. Expressing the charge flowing in the highlighted commutation loop of Fig. 2.4 as Q_{flow} :

$$Q_{\text{flow}} = C_{\text{oss,H}} \Delta v_H = C_{\text{oss,H}} \cdot (v_H(t_f) - v_H(0)) \quad (2.1)$$

$$v_H(t_f) = v_{C,2}(t_f) - v_{C,1}(t_f), \quad v_H(0) \approx 0$$

$$Q_{\text{flow}} \approx C_{\text{oss,H}} \cdot (v_{C,2}(t_f) - v_{C,1}(t_f)) \quad (2.2)$$

In this process, charge Q_{flow} leaves C_2 and is deposited on C_1 . The flying capacitor voltages, $v_{C,1}$ and $v_{C,2}$, after a commutation event are thus functions of this Q_{flow} :

$$\begin{aligned} v_{C,2}(t_f) &= v_{C,2}(0) - \frac{Q_{\text{flow}}}{C_2} \\ &= v_{C,2}(0) - \frac{C_{\text{oss,H}}}{C_2} \cdot (v_{C,2}(t_f) - v_{C,1}(t_f)) \\ &= \frac{C_2}{C_2 + C_{\text{oss,H}}} v_{C,2}(0) + \frac{C_{\text{oss,H}}}{C_2 + C_{\text{oss,H}}} v_{C,1}(t_f) \end{aligned} \quad (2.3)$$

$$\begin{aligned} v_{C,1}(t_f) &= v_{C,1}(0) + \frac{C_{\text{oss,H}}}{C_1} \cdot (v_{C,2}(t_f) - v_{C,1}(t_f)) \\ &= \frac{C_1}{C_1 + C_{\text{oss,H}}} v_{C,1}(0) + \frac{C_{\text{oss,H}}}{C_1 + C_{\text{oss,H}}} v_{C,2}(t_f) \end{aligned} \quad (2.4)$$

Substituting (2.3) into (2.4) yields:

$$\begin{aligned} v_{C,1}(t_f) \left[1 - \frac{C_{\text{oss,H}}^2}{(C_1 + C_{\text{oss,H}})(C_2 + C_{\text{oss,H}})} \right] &= \\ \frac{C_1}{C_1 + C_{\text{oss,H}}} v_{C,1}(0) + \frac{C_{\text{oss,H}} C_2}{(C_1 + C_2)(C_2 + C_{\text{oss,H}})} v_{C,2}(0). \end{aligned} \quad (2.5)$$

Finally, by rearranging we obtain an equation for $v_{C,1}$ at the end of a commutation event:

$$v_{C,1}(t_f) = \frac{v_{C,1}(0) \cdot (C_1 C_2 + C_1 C_{\text{oss,H}}) + C_2 C_{\text{oss,H}} v_{C,2}(0)}{C_1 C_2 + C_{\text{oss,H}} (C_1 + C_2)}. \quad (2.6)$$

As expressed in (2.6), the flying capacitor voltages rapidly change after a commutation event due to C_{oss} -induced charge redistribution.

Under the assumption of zero dead-time, both high-to-low switch transitions and low-to-high switch transitions experience the same charge flow. Table 2.1 summarizes each flying capacitor voltage after a commutation event (obtained by the same process that yielded (2.6)). These approximations assume that the commutation events are “local”, that is, only the flying capacitors connected to a commutating switching cell participate in C_{oss} charge redistribution¹. Additionally, if two cells commute at the same time, the voltage at the end of the event can be approximated by a cascade of two separate switching events. Note that the entries in Table 2.1 are generalizable to FCML converters with arbitrary level counts as can be seen by the symmetry in the equations for the S_2 and S_3 switching cell. That is, the form of the equations for switching cell S_2 apply to all switching cells with two flying capacitors.

In reality, commutations are not perfectly instantaneous and practical converters will introduce a deadtime period where $S_{H,k}$ and $S_{L,k}$ are OFF simultaneously. These non-zero deadtimes will impact the previously described charge flows in the following ways. For the sake of simplicity, we assume the inductor current i_L is positive (i.e., flowing to the output in Fig. 2.4(a)). After $S_{L,k}$ turns OFF and before $S_{H,k}$ turns ON, the inductor current i_L will discharge the $C_{\text{oss,L}}$ of $S_{L,k}$. If this capacitance is fully discharged, the body diode (or effective body diode) of this switch will turn ON. If this occurs before $S_{H,k}$ switch turns on, the low side capacitance will then be charged from $-V_d$, the “diode voltage”, up to a combination of the flying capacitor voltages rather than from ≈ 0 V as the equations in Table 2.1 assume. In practice, this slight approximation error was found to be negligible. Conversely, after $S_{H,k}$ turns OFF and before $S_{L,k}$ turns ON, $C_{\text{oss,H}}$ will be partially charged and $C_{\text{oss,L}}$ partially discharged by the inductor current. This will reduce the charge flow when $S_{L,k}$ turns ON. Similar to neglecting the body diode voltage drop, this approximation error was found to have negligible impact.

¹In reality, flying capacitors that are not directly connected to a switching cell are weakly connected to the cell through the C_{oss} of a turned OFF switch. For example, C_2 is in parallel with the series combination of C_3 and C_{oss} when the S_2 switching cell commutes. However, due to the relative sizing of C_{fly} and C_{oss} (i.e., $C_{\text{fly}} \gg C_{\text{oss}}$) in practical implementations of the topology, the modeling error introduced is negligible.

Table 2.1: Tabulated analytical solutions to the flying capacitor voltages after a commutation event occurs for a five-level FCML converter.

Switching Cell	Flying Capacitor Voltage After Event
S_1	$v_{C,1}(t_f) = v_{C,1}(0) - \frac{C_{\text{oss}}}{C_1 + C_{\text{oss}}} v_{C,1}(0)$
S_2	$v_{C,1}(t_f) = v_{C,1}(0) + \frac{C_2 C_{\text{oss}}}{C_1 C_2 + C_{\text{oss}}(C_1 + C_2)} (v_{C,2}(0) - v_{C,1}(0))$ $v_{C,2}(t_f) = v_{C,2}(0) + \frac{C_1 C_{\text{oss}}}{C_1 C_2 + C_{\text{oss}}(C_1 + C_2)} (v_{C,1}(0) - v_{C,2}(0))$
S_3	$v_{C,2}(t_f) = v_{C,2}(0) + \frac{C_3 C_{\text{oss}}}{C_2 C_3 + C_{\text{oss}}(C_2 + C_3)} (v_{C,3}(0) - v_{C,2}(0))$ $v_{C,3}(t_f) = v_{C,3}(0) + \frac{C_2 C_{\text{oss}}}{C_2 C_3 + C_{\text{oss}}(C_2 + C_3)} (v_{C,2}(0) - v_{C,3}(0))$
S_4	$v_{C,3}(t_f) = v_{C,3}(0) + \frac{C_{\text{oss}}}{C_3 + C_{\text{oss}}} (V_{\text{in}} - v_{C,3}(0))$

2.3.2 Analytical FCML Converter Model Incorporating C_{oss} Induced Charge Flow

Given that the C_{oss} -induced voltage changes per commutation event are very small compared to the average values of the flying capacitor voltages², it is difficult to ascertain a priori whether the flying capacitor voltages will settle to a balanced state and if they do, how quickly transients settle. To investigate the circuit response, an analytical model was developed in MATLAB to solve for the state variables within the circuit as a function of time. To analytically simulate the circuit, each switching configuration is associated with a set of state-space matrices. As an example, consider the symmetric PS-PWM switch configuration to generate an approximate switch node voltage of $V_{\text{in}}/2$ with switches $S_{H,1}$, $S_{L,2}$, $S_{L,3}$, and $S_{H,4}$ ON while complementary switches are OFF. The circuit associated with this switching configuration is illustrated in Fig. 2.5. The state-space description of this circuit is:

$$\dot{x}(t) = \frac{d}{dt} \begin{bmatrix} v_{C,1} \\ v_{C,2} \\ v_{C,3} \\ i_L \\ v_{\text{out}} \\ v_{C_{\text{in}}} \\ i_{Z_{\text{in}}} \end{bmatrix} = \mathbf{A} \begin{bmatrix} v_{C,1} \\ v_{C,2} \\ v_{C,3} \\ i_L \\ v_{\text{out}} \\ v_{C_{\text{in}}} \\ i_{Z_{\text{in}}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ L_{\text{in}}^{-1} \end{bmatrix} V_{\text{in}} \quad (2.7)$$

²For example, in the converter shown in Section III, the flying capacitor voltages may change by less than a tenth of a percent in a commutation event.

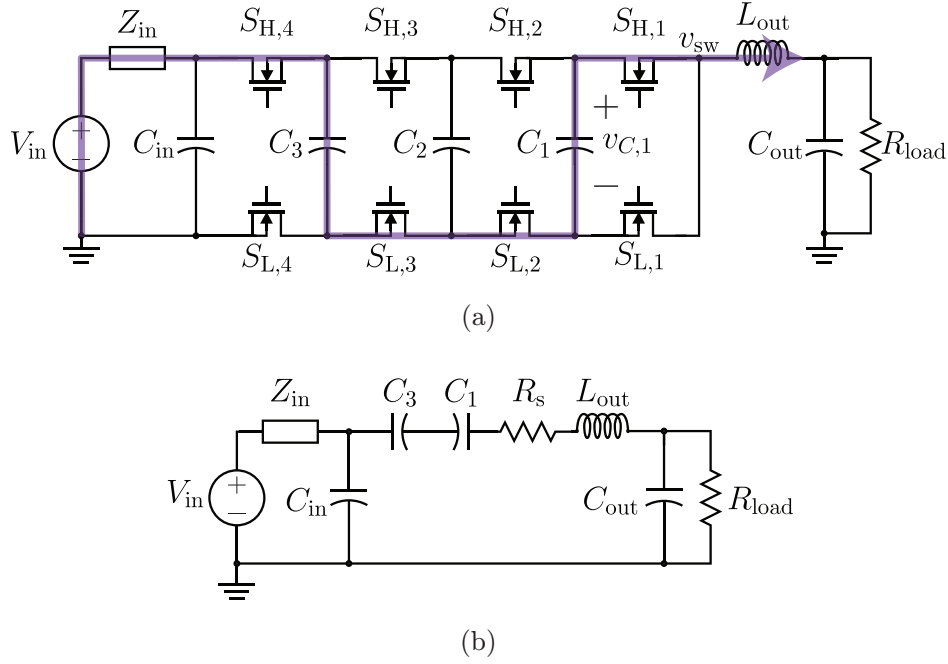


Figure 2.5: (a) Circuit schematic of a five-level FCML converter to generate a switch-node voltage of $V_{\text{in}}/2$ with current path highlighted and input network explicitly drawn. (b) Equivalent circuit used to obtain the state space description of Eq. 2.7. R_s models the sum of series resistances in the power path (e.g., inductor and FET resistance, etc.).

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & -C_1^{-1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_3^{-1} & 0 & 0 & 0 \\ L_{\text{out}}^{-1} & 0 & -L_{\text{out}}^{-1} & -R_s L_{\text{out}}^{-1} & -L_{\text{out}}^{-1} & L_{\text{out}}^{-1} & 0 \\ 0 & 0 & 0 & C_{\text{out}}^{-1} & -(C_{\text{out}} R_{\text{load}})^{-1} & 0 & 0 \\ 0 & 0 & 0 & -C_{\text{in}}^{-1} & 0 & 0 & C_{\text{in}}^{-1} \\ 0 & 0 & 0 & 0 & 0 & -L_{\text{in}}^{-1} & 0 \end{bmatrix} \quad (2.8)$$

Where R_s is the sum of series resistances within the sub-circuit comprising inductor resistance, switch on-state resistance, flying capacitor ESR, and any other parasitic resistances.

The state variables at the end of a switching state $x(t_f)$ are then found by solving the state evolution equation:

$$\dot{x}(t) = \mathbf{A} x(t) + \mathbf{B} V_{\text{in}}(t) \quad (2.9)$$

as a function of the state variables at the beginning of a switching state $x(t_0)$. This solution is [21]:

$$x(t_f) = \exp(\mathbf{A}(t_f - t_0))x(t_0) + \int_{t_0}^{t_f} \exp(\mathbf{A}(t_f - \tau))\mathbf{B}V_{\text{in}}(\tau)d\tau \quad (2.10)$$

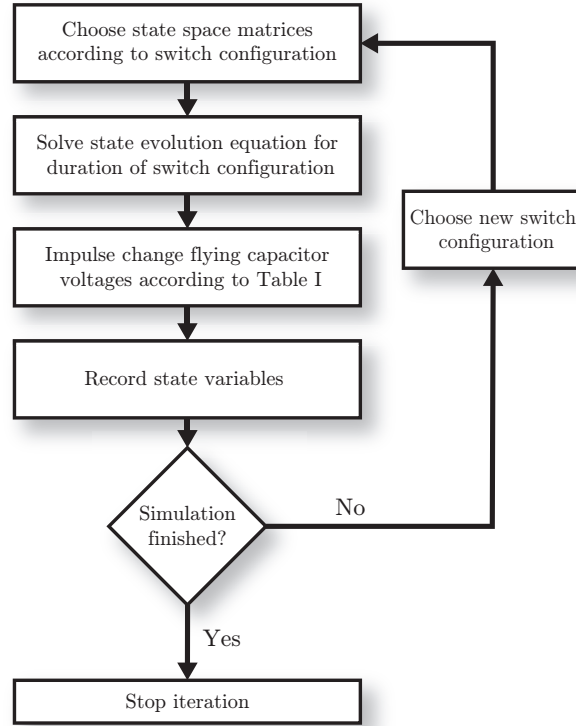


Figure 2.6: Flowchart illustrating the MATLAB algorithm developed to obtain the FCML converter state variables as a function of time.

where $x(t_0)$ is the initial condition for the state variables and $x(t_f)$ the final state value. To save memory and computational load, the state variables are only solved at each switching instance, thus the time steps of the solver are the same as those of the switching instances of the converter. By “stitching” together these final and initial states and continually solving the state evolution equation we can obtain time-series data of the converter’s state variables.

To incorporate the charge flow quantities and voltage changes induced by the switch output capacitance, the flying capacitor voltages at the end of a switching state are changed according to Table 2.1. These modified flying capacitor voltages are then used as the initial value for the next state evolution equation solver. The developed algorithm is shown in the flowchart of Fig. 2.6.

2.3.3 Extension to Nonlinear Capacitances

In many practical implementations of the FCML converter, nonlinear flying capacitors and nonlinear device C_{oss} will be employed, requiring an increase in simulation complexity for model fidelity. Class 2 ceramic capacitors (e.g., X6S) are often used for the flying capacitors due to their superior energy density compared to Class 1 capacitors [7]. This benefit in density comes at the penalty of a strongly nonlinear small-signal capacitance versus bias

voltage characteristic. To incorporate this impact in an analytical simulation, the state space matrices can be modified by updating the flying capacitance values with a look up table using the flying capacitor voltage at the start of a switching phase. This process implicitly assumes the flying capacitor voltage will not change drastically over a switching phase, an assumption which is generally true in practical implementations.

A more severe nonlinearity is encountered in the transistor output capacitance, C_{oss} . Fig. 2.7 depicts the C_{oss} vs. V_{ds} curve for the EPC2302 [22], a high performance 100 V eGaN FET. In many implementations, the output capacitance swings from ≈ 0 V to a significant fraction of $V_{\text{ds,max}}$ during a commutation event. Accurate models attempting to capture the impact of C_{oss} in this operating regime thus need to include this nonlinearity. At the end of a commutation event, the output capacitance of a switch that was previously ON is charged from ≈ 0 V to a combination of the flying capacitor and input voltages. During this process an amount of charge Q is transferred within the converter. For linear capacitances, this charge is $Q = CV_{\text{final}}$ where V_{final} is the voltage across the C_{oss} at the end of a commutation event. For nonlinear capacitances however, this charge Q is a nonlinear function of the final voltage. It is therefore necessary to know the charge flow induced by this voltage change across C_{oss} to determine the flying capacitor voltages after a commutation event.

Fig. 2.7(b) shows the Q_{oss} vs. V_{ds} curve for the EPC2302 obtained from the manufacturer provided LTSPICE model. Above a certain v_{ds} voltage (in this case ≈ 15 V), the slope of the curve decreases drastically. A faithful approximation is thus obtained through a two-part piecewise linear fit of the curve. This linear fit can be used to approximate the charge flow induced by the charging of the device's C_{oss} when solving for the flying capacitor voltages after a commutation event. This charge flow is described by

$$Q_{\text{oss}}(v) = \begin{cases} C_{\text{high}}v & v < V_b \\ C_{\text{high}}V_b + C_{\text{low}}(v - V_b) & v > V_b \end{cases} \quad (2.11)$$

To illustrate this technique, we use the commutation event of the S_2 switching cell in a five-level FCML converter (illustrated in Fig. 2.4) and assume that $v_{C,2}(t_f) - v_{C,1}(t_f) > V_b$ as an example.

$$v_{C,2}(t_f) = v_{C,2}(0) - \frac{Q_{\text{flow}}}{C_2} \quad (2.12)$$

$$Q_{\text{flow}} = C_{\text{high}}V_b + C_{\text{low}}(v_{C,2}(t_f) - v_{C,1}(t_f) - V_b) \quad (2.13)$$

Similar to (2.2), (2.13) expresses the charge flow as a function of the flying capacitor voltages at the end of a commutation event. The flying capacitor voltages can be solved in a similar manner to that presented in Section 2.3.1.

Fig. 2.8 shows simulations of a five-level FCML converter which demonstrates the inclusion of the nonlinear C_{oss} and a piecewise linear approximation as a comparison. This simulation operates at a significantly higher v_{in} , up to 320 V. At this input voltage, the v_{ds} of the switches reaches 80 V, a high enough voltage to encounter the nonlinearity in the

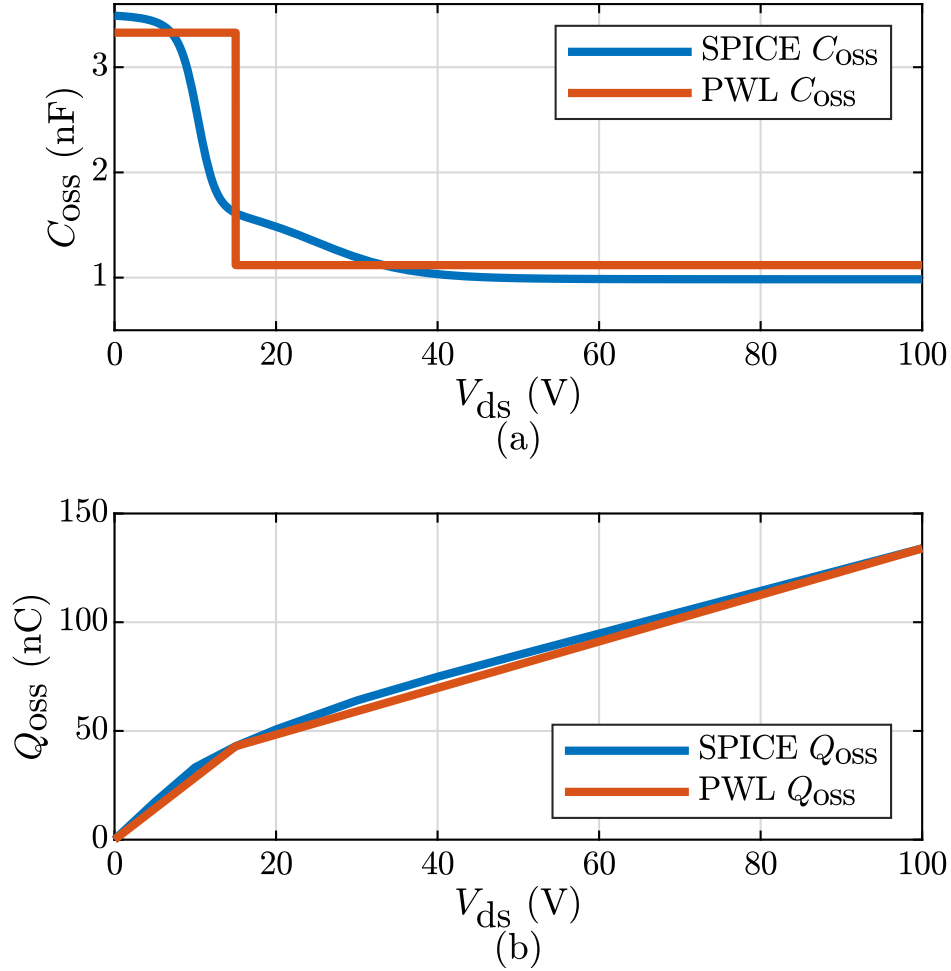


Figure 2.7: (a) C_{oss} characteristics for an example EPC2302 device [22]. Data are obtained by differentiating the manufacturer provided LTSPICE Q - v curve. (b) Q_{oss} vs. V_{ds} for the EPC2302. This curve is well approximated by a two-part piecewise linear (PWL) function.

$C_{\text{oss}}(v_{\text{ds}})$ curve. A PLECS simulation using variable capacitors and look up tables implements the nonlinear C_{oss} curve from the EPC2302 [22] datasheet. Fig. 2.8(a) implements the piecewise linear C_{oss} model described above while Fig. 2.8(b) assumes that the C_{oss} is constant at the value of $C_{\text{oss}}(v_{\text{ds}} = 0 \text{ V})$. Since $C_{\text{oss}}(v_{\text{ds}})$ drops significantly above $v_{\text{ds}} = V_{\text{b}}$, assuming a constant C_{oss} predicts a circuit that exhibits a more damped response than the PLECS simulation.

2.3.4 Comparison to Insufficient Input Capacitance

The balancing mechanism produced by C_{oss} -induced charge flow serves to work in tandem with natural balancing and combat other imbalance mechanisms. One such imbalance mechanism found to have a significant impact in [16], [23] is that of input voltage ripple due to

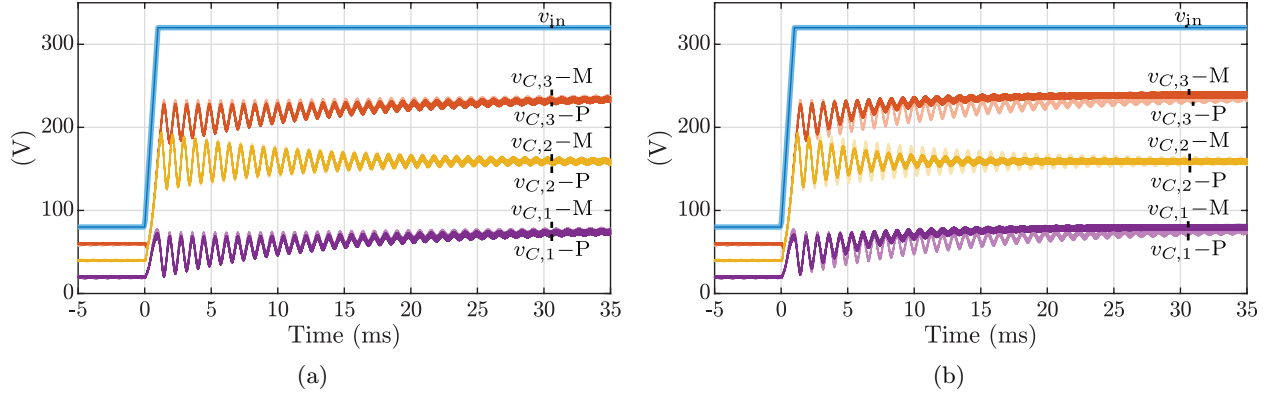


Figure 2.8: Transient simulation of a five-level FCML converter including nonlinear C_{oss} . (a) Analytical model incorporating PWL C_{oss} . (b) Analytical model assuming a constant $C_{\text{oss}} = C_{\text{oss}}(v_{\text{ds}} = 0)$. Traces labeled $v_{C,i}-P$ are from obtained from PLECS while $v_{C,i}-M$, are obtained from an analytical MATLAB simulation. The nonlinear C_{oss} are implemented in PLECS via variable capacitors and a look up table derived from the EPC2302 [22] datasheet.

insufficient input capacitance. The authors in [16], [23] found that this imbalance mechanism had a much stronger impact than other mechanisms (e.g., gate driver delay mismatch).

To compare the impacts of the C_{oss} -induced balancing mechanism and the insufficient input capacitance unbalancing mechanism, a simulation study was performed. In one simulation the influence of C_{oss} -induced charge flow is included while in the other, a traditional simulation (i.e., one without C_{oss}) is performed. The results of this study for a five-level FCML converter are shown in Fig. 2.9 with simulation parameters reported in Table 2.2. A model excluding C_{oss} significantly overpredicts the steady-state error of the flying capacitor voltages. Although a model including C_{oss} accurately predicts a slight steady-state error, C_{oss} -induced charge flow drives the converter closer to the ideal balanced voltage distribution. Thus, including the impact of the C_{oss} charge flow in a converter model will predict a more realistic flying capacitor voltage distribution. Note, the steady-state values reported are the midrange of the capacitor voltage waveform (i.e., $[\max(v_{C,k}) - \min(v_{C,k})]/2$).

This example illustrates a key aspect of C_{oss} -induced balancing: The C_{oss} -induced charge flow by no means guarantees that the flying capacitor voltages will be perfectly balanced. Known imbalance mechanisms such as gate driver delay mismatch, switch on-resistance mismatch, and insufficient input capacitance work in opposition to C_{oss} charge flow and may result in a flying capacitor voltage distribution that deviates from the ideal. Additionally, the “strength” of the C_{oss} -induced balancing mechanism depends on both C_{oss} and the capacitance of the flying capacitors C_{fly} . Larger C_{oss} and smaller C_{fly} result in a more pronounced C_{oss} -induced balancing impact.

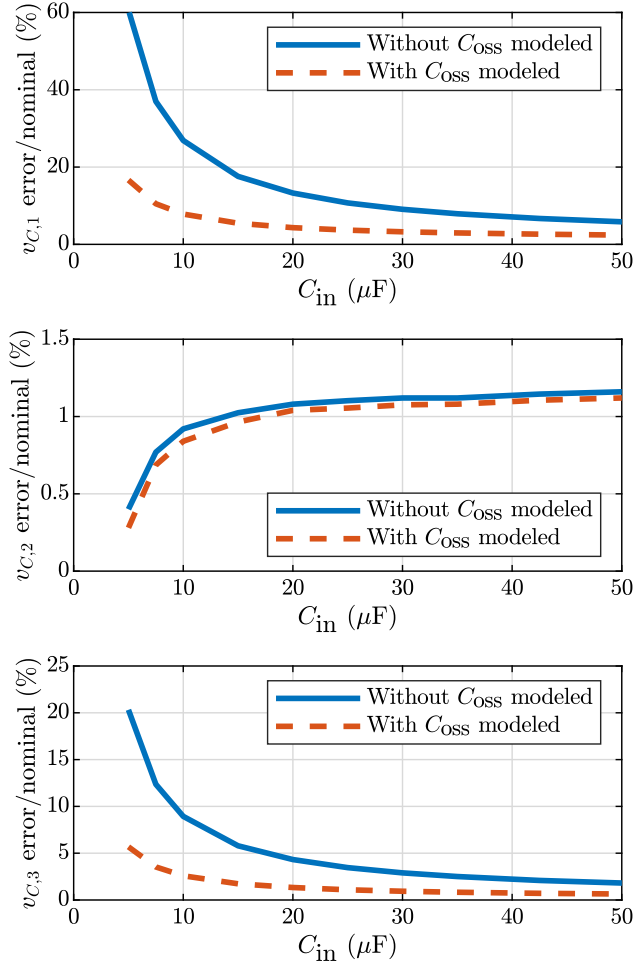


Figure 2.9: Simulation study results investigating the steady-state error distribution of flying capacitor voltages. Including the impact of C_{oss} -induced charge flow predicts a more balanced distribution of flying capacitor voltages than a model without. Reported voltages are the midrange of the flying capacitor voltage waveform.

2.4 Experimental Validation

To validate the theory of C_{oss} -induced natural balancing of the flying capacitor voltages, we imposed input voltage transients on several five-level FCML converter prototypes and observed the oscillatory response of the flying capacitor voltages and the time-domain response of the circuit. To experimentally observe all pertinent frequencies, the step input voltage excitation must have a rise time sufficiently fast to excite higher frequency oscillations. To accomplish this, the circuit highlighted in the top left of Fig. 2.11 was devised. Before the step occurs, the gate of the MOSFET S_{tr} is held low (where $S(t)$ is the switching signal applied to S_{tr}) and $V_{\text{in,FCML}} = V_{\text{in}} - V_{\text{Z}}$, where V_{Z} is the Zener voltage, is applied to the FCML converter's input port. To activate the step, the gate of S_{tr} is pulled high, increasing the input voltage to the converter to V_{in} at a high slew rate. The outputs of both converters

Table 2.2: Simulation parameters for study in Section 2.3.4

Parameter	Value	Parameter	Value
V_{in}	50 V	R_{load}	$2\ \Omega$
L_{in}	$1\ \mu\text{H}$	C_{out}	$44\ \mu\text{F}$
R_{in}	$0.1\ \Omega$	L_{out}	$10\ \mu\text{H}$
f_{sw}	120 kHz	D	0.251
C_{fly}	$5\ \mu\text{F}$	C_{oss}	3.5 nF

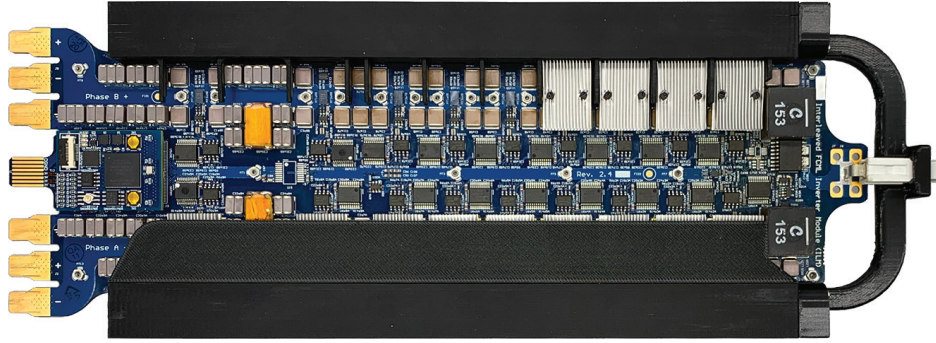


Figure 2.10: A top-down view of the ten-level FCML converter prototype [3] used to obtain the experimental data shown in Fig. 2.12. Each PCB contains two, interleaved ten-level FCML converters switching at a frequency of 115 kHz with LC filters on board. Circuit parameters are given in Table 2.3. The converter is configured for five-level operation by turning ON switches $S_{\text{H},5-9}$ and $S_{\text{L},5-9}$. One of the two FCML converters is left disconnected for the experiments performed in this work.

were connected to a constant $9.8\ \Omega$ load. To add further experimental evidence of the proposed C_{oss} -induced balancing theory, two FCML converter prototypes were developed. The prototypes differ significantly in converter parameters found to influence natural balancing dynamics. A summary of the differences in the two prototypes is provided in Table 2.5.

Table 2.3: Circuit Parameters Used in Experiment in Fig. 2.12

Component	Description	Part Name
Power Semicond.	200 V, 10 m Ω , 450 pF*	EPC2034
C_{fly}	$4.4\ \mu\text{F}$	C5750X6S2W225K250KA
L_{out}	$7.5\ \mu\text{H}$	XAL1510-153
C_{out}	$0.6\ \mu\text{F}$	C5750C0G2J104J280KC

*This is the C_{oss} for $v_{\text{ds}} = V_{\text{rated}}/2$.

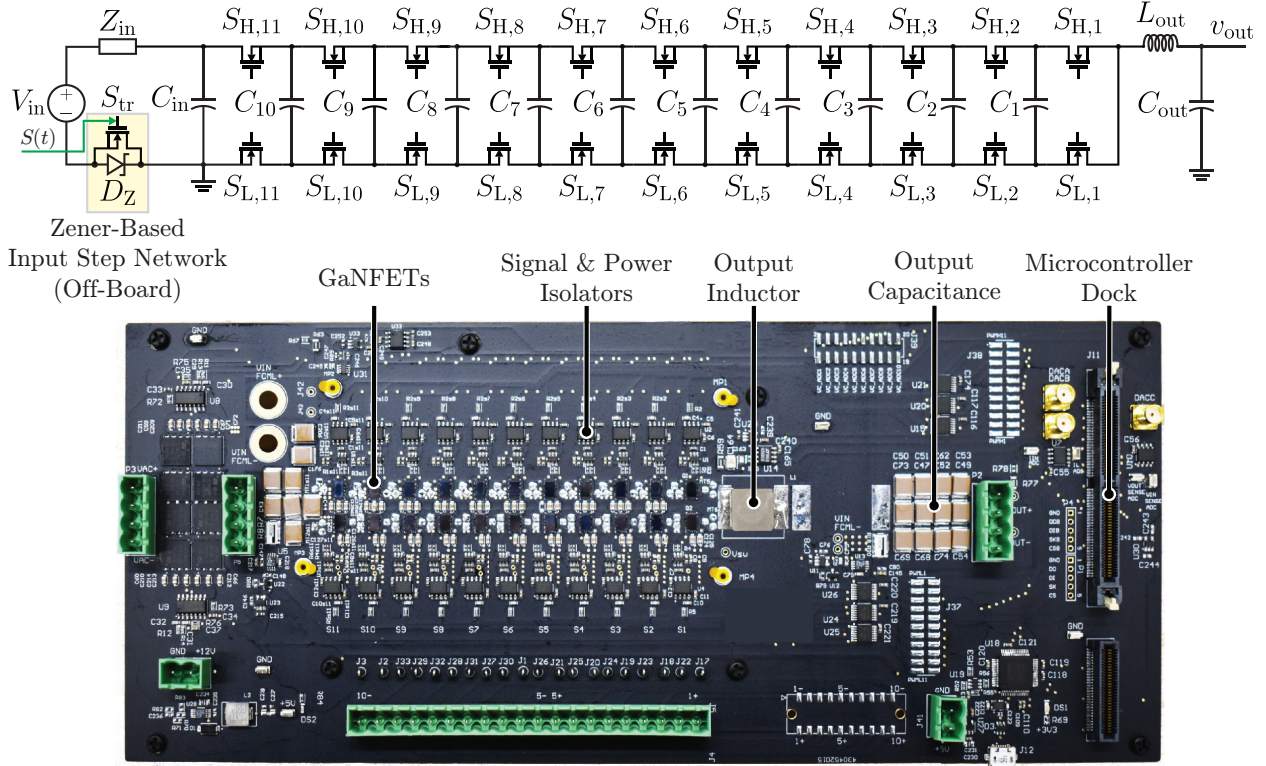


Figure 2.11: Hardware photograph of prototype 2, a twelve-level FCML converter configured for five-level operation for the experiments performed in Fig. 2.13. Highlighted in the top left corner of the figure is the input step network. By adjusting the switching signal $S(t)$ from OFF to ON, the input voltage to the FCML is raised from $V_{in} - V_Z$ to V_{in} where V_Z is the Zener voltage of the external Zener diode D_Z in series with the input port of the FCML converter. The converter is configured for five-level operation by turning ON switches $S_{H,5-11}$ and $S_{L,5-11}$. Pertinent component parameters are given in Table 2.4.

2.4.1 Prototype 1 Validation

Presented in Fig. 2.12 are the results from this input voltage step study applied to the FCML converter shown in Fig. 2.10. As can be seen, both the analytical simulation and measured results agree very well when including the impact of C_{oss} -induced charge flow on the FCML converter as derived in Section 2.3. If the impact of C_{oss} is not included and the FCML converter is modeled in the traditional way, the flying capacitor voltages will not converge to a balanced state as the experiment does. These results are significant as they indicate that previous models of the FCML converter were inadequate as they neglected a key parasitic element in the circuit rather than a flaw in the analysis of the simplified circuit. The converter was operated with symmetric PS-PWM at a constant switching frequency of 115 kHz.

Table 2.4: Circuit Parameters used in Experiments in Fig. 2.13

Component	Description	Part Name
Power Semicond.	100 V, 1.8 m Ω , 1 nF*	EPC2302
C_{fly}	8.8 μF	C5750X6S2W225K250KA
L_{out}	10 μH	IHLP5050CEER100M01
C_{out}	44 μF	C5750C0G2J104J280KC

*This is the C_{oss} for $v_{\text{ds}} = V_{\text{rated}}/2$.

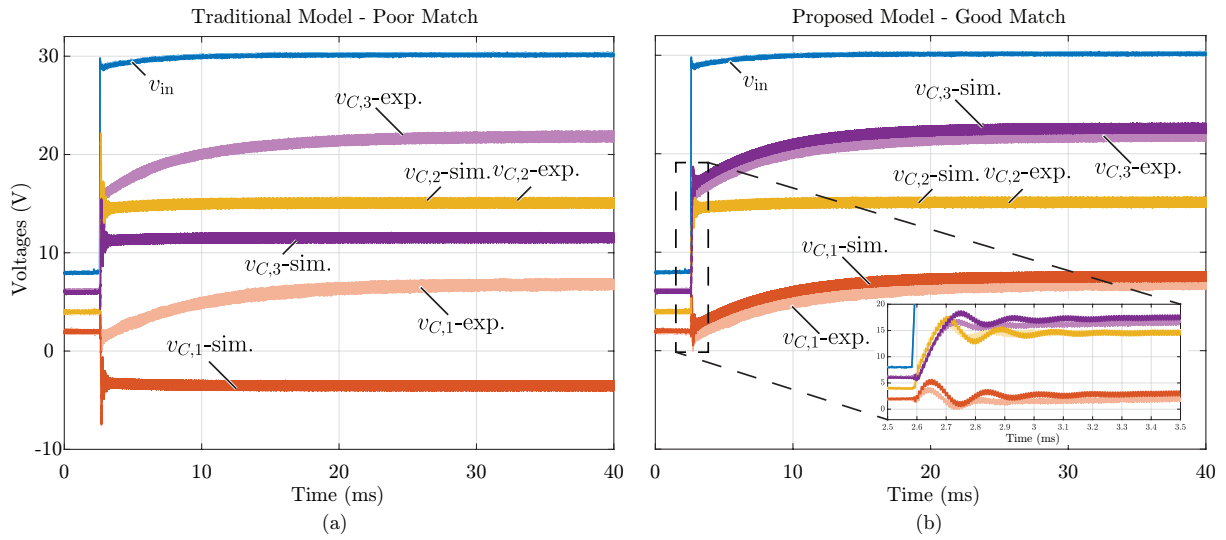


Figure 2.12: Measured data from prototype 1, a five-level FCML converter [3] shown in Fig. 2.10. The FCML converter was excited with an ≈ 22.5 V input voltage step by the input step network highlighted in the top left of Fig. 2.11 while operating at a duty cycle of 50%. Waveforms labeled “-sim.” are simulation data while those labeled “-exp.” are experimental data. (a) A simulation of a traditional model (i.e., one that does not include the impact of C_{oss}) compared with experiment. This model is clearly deficient in modeling the flying capacitor voltages’ transient response. (b) Transient response of model including the impact of C_{oss} which predicts the flying capacitors natural convergence to their balanced values as experiment does. The inset in (b) shows a zoomed in view of the initial transient response of the flying capacitor voltages, which exhibits an oscillatory behavior. Both simulations employed the algorithm shown in Fig. 2.6.

2.4.2 Prototype 2 Validation

Fig. 2.13(a) shows the transient response of prototype 2, shown in Fig. 2.13(b), while operating at a “balanced” conversion ratio of 25%. Since the RLC circuit dynamics investigated in previous works [20], [24] are now able to participate in driving the flying capacitors to their balanced voltages at this conversion ratio, the flying capacitor voltages converge much faster to their balanced values compared to the case of a conversion ratio of 50%, shown in Fig 2.13(b). The component parameters are given in Table 2.4 and the converter was operated at a switching frequency of 75 kHz. The six highest voltage switch pairs were held

Table 2.5: Prototype Parameter Comparison

Parameter	Ratio
$R_{\text{ds},1}/R_{\text{ds},2}$	5.5
$C_{\text{fly},1}/C_{\text{fly},2}$	2
$C_{\text{out},1}/C_{\text{out},2}$	73
$C_{\text{oss},1}/C_{\text{oss},2}$	0.5

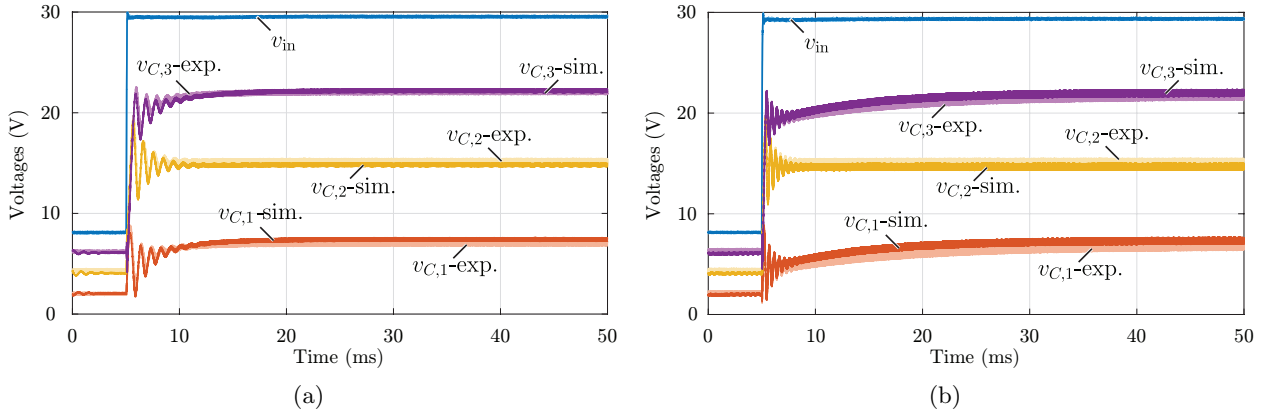


Figure 2.13: Measured data from prototype 2, a five-level FCML shown in Fig. 2.11. (a) operated at a “balanced” conversion ratio of 25% and (b) an “unbalanced” conversion ratio of 50%. The input port of the FCML converter was excited with the same input voltage excitation as the experiment presented in Fig. 2.12. Compared to the experiment presented in Fig. 2.12, prototype 2 operates at a slower switching frequency (65% that of prototype 1) and utilizes a larger output capacitor ($73\times$ that of prototype 1). Despite these differences the presented model and experiment agree quite well. Waveforms labeled “-sim.” are simulation data while those labeled “-exp.” are experimental data.

constantly ON to generate the five-level converter.

2.5 Chapter Remarks

This work has analyzed a key parasitic element, the switch output capacitance C_{oss} , and its impact on the ability of the flying capacitors within a FCML converter to balance to their desired voltages. Without the inclusion of this previously neglected balancing mechanism, simulation and analytical models of the FCML converter are unable to track experimental data. Ensuring model fidelity of the FCML converter is critical for both flying capacitor voltage estimation (e.g., for converter health monitoring) and active balancing control of the flying capacitor voltages. Although C_{oss} -induced balancing reduces switch voltage stress and inductor current harmonics, the flying capacitor voltages are balanced through a lossy mechanism. That is, FCML converter implementations which do not exhibit soft-switching will incur increased switching and/or overlap losses due to increased C_{oss} . Thus, attempts

to force balanced flying capacitor voltages through increased C_{oss} will be met with increased switching losses. Using the modeling techniques presented in this chapter, the designer can assess the impact of parasitic device C_{oss} and whether additional external capacitance is beneficial.

Chapter 3

A Combined Power Factor Correcting and Active Voltage Balancing Control Technique for Buck-Type AC/DC Grid-Tied Flying Capacitor Multilevel Converters

Portions of this chapter are adapted in part from [25].

3.1 Introduction

Grid-connected applications with low voltage dc outputs require rectification of the ac mains service and successive stages of down-conversion to provide voltage at the point of load. These applications include data center power delivery, industrial LED lighting, and low voltage battery storage. Fig. 3.1 illustrates two potential power conversion architectures to generate a 48 V dc output from a single-phase grid. Conventionally, a two-stage solution is employed as the power conversion architecture: the rectifier, which performs power factor correction (PFC), boosts the mains voltage to an intermediate dc voltage higher than the peak of the line (e.g., 400 V for a 240 V_{rms} single-phase ac system) and a second dc-dc stage converts this voltage to a lower dc voltage (e.g., 48 V). In all two-stage power conversion approaches, the overall system suffers cascaded efficiency penalties and potentially lower power density due to the integration of two separate power conversion stages. As an example of achievable two stage power conversion efficiency, a recent GaN-based totem-pole boost PFC converter prototype achieved an efficiency of 97% [26] and a GaN-based 400 V-48 V dc/dc converter prototype achieved an efficiency of 97.2% [27]. The total grid-to-48 V total power conversion efficiency is thus 94.3%, the product of the two conversion stages' efficiencies. Similarly, commercial converters are able to achieve grid-to-48 V efficiencies of $\approx 92\%$ [28].

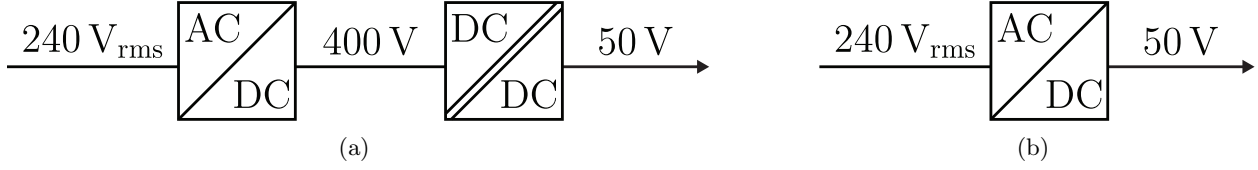


Figure 3.1: Two power conversion architectures to generate 48 V from a single-phase 240 V_{rms} grid. (a) Conventional two-stage approach consisting of a boost-type PFC rectifier and a high step-down-ratio dc/dc converter. (b) Single-stage approach consisting of a buck-type PFC rectifier.

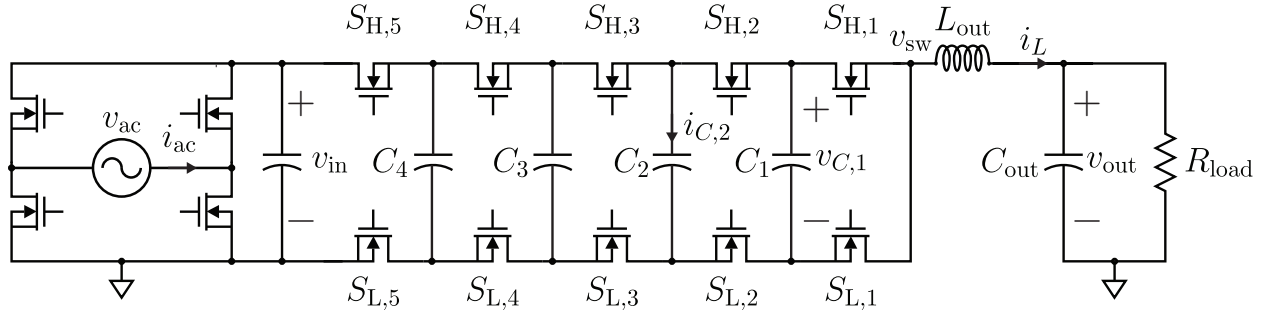


Figure 3.2: Circuit diagram of an ac/dc buck-type PFC rectifier utilizing a six-level FCML converter with an input synchronous rectifier.

One promising alternative to this conventional architecture is a single-stage conversion architecture [29], [30], [31], [32], [33]. This architecture directly converts the incoming mains to a lower voltage (e.g., 48 V) in a single stage. If the power converter used to implement the ac-dc stage is buck-type (i.e., the converter does not operate when $|v_{ac}| < V_{out}$), the power factor of the grid current will be less than one. However, as investigated in [34], extremely high power factors can still be achieved for typical grid and output voltages.

This work investigates a novel application of the FCML converter by utilizing the topology as the power stage within a buck-type PFC rectifier, which presents efficiency and power density advantages, but also challenges associated with control and device ratings. These challenges are addressed in this work, with a number of innovative design approaches and control techniques. A schematic drawing of a six-level FCML converter configured as a buck-type rectifier is shown in Fig. 3.2.

Compared to buck-type FCML inverters and boost-type FCML rectifiers, in buck-type FCML rectifiers, the flying capacitor voltages must track fractions of the rectified grid voltage to achieve the minimal switch voltage stress. If the flying capacitor voltages deviate too far from the ideal balanced distribution, the switches must be rated for a larger voltage and converter efficiency will degrade as a result. The modulation scheme utilized for most FCML converters, symmetric phase shifted PWM (PS-PWM) [1], is typically unable to achieve the desired flying capacitor voltages in high performance buck-type PFC rectifiers. Fig. 3.3 shows symmetric PS-PWM gating waveforms, switch node voltage v_{sw} , and inductor current i_L for a six-level FCML converter at a dc-dc operating point with balanced flying capacitor voltages.

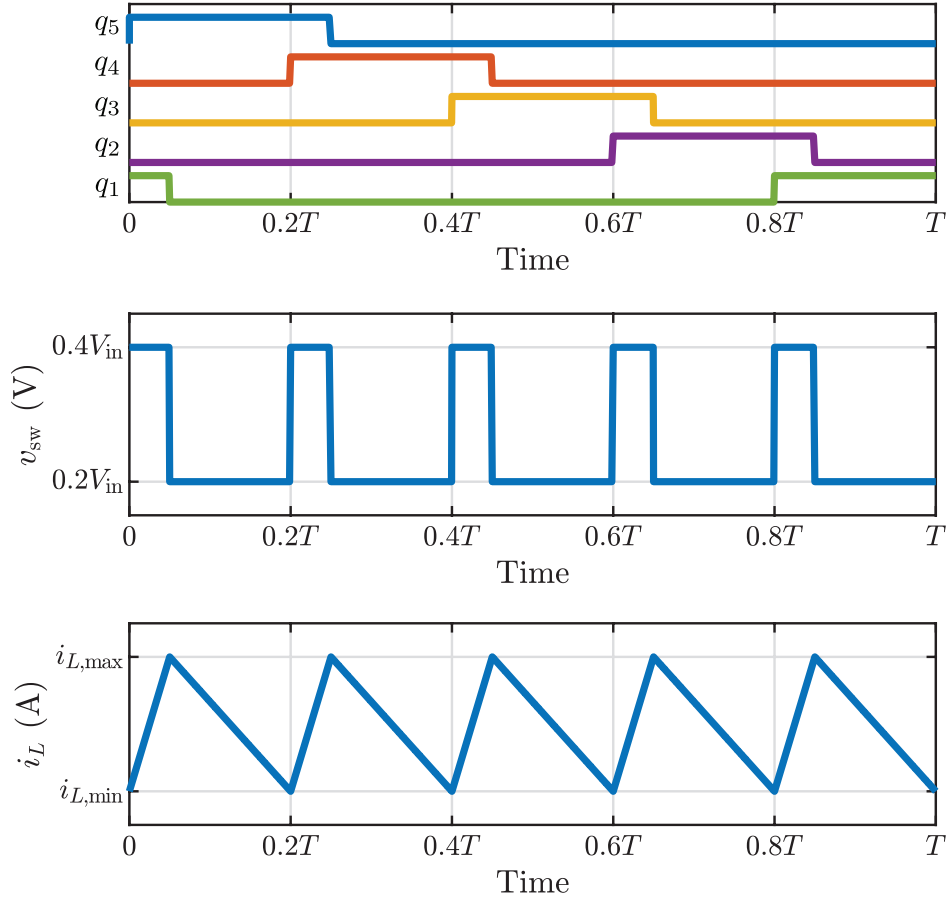


Figure 3.3: Gating signals q_k , switch node voltage v_{sw} , and inductor current i_L for a six-level FCML converter operated with symmetric phase shifted PWM (PS-PWM) at a duty cycle of 25% with balanced flying capacitor voltages. Signals q_k have the same duty cycle and are equally phase shifted throughout the switching period. Signal q_k drives switch $S_{H,k}$ at a period T while the complement of q_k drives switch $S_{L,k}$. This modulation scheme is typically unable to achieve flying capacitor voltage balance for buck-type FCML rectifiers. Section 3.3 explores controllers which depart from this modulation scheme to achieve flying capacitor voltage balance.

Work in [35] modeled the natural frequency response of the flying capacitor voltages in relation to input voltage v_{in} perturbations when operated with symmetric PS-PWM. For the same FCML converter parameters utilized in this work, the maximum v_{in} frequency before switch voltage stress began to increase significantly was approximately 20 Hz. This increased switch voltage stress is due to the flying capacitor voltages being unable to maintain their balanced distribution for excitations above this frequency. Thus to utilize low voltage switches in buck-type FCML rectifiers, rather than relying on the natural balancing dynamics of the flying capacitor voltages, active flying capacitor voltage controllers must be used to achieve the desired flying capacitor voltage distribution.

This work proposes an active flying capacitor voltage balancing controller which operates in tandem with the inductor current controller to achieve high performance buck-type PFC

rectification with the FCML converter. The controller measures both the flying capacitor voltages and the inductor current and adjusts the duty cycles applied to the transistors to achieve control of these state variables.

Previous works have shown that active flying capacitor voltage balancing can be achieved purely through inductor current control (i.e., without sensing of the flying capacitor voltages). These works have achieved flying capacitor voltage balancing in the presence of line voltage transients or intentionally added converter asymmetries through both sampled [36], [37] and analog [38] inductor valley current control. Although these alternative control schemes are able to achieve steady-state and low frequency flying capacitor voltage balancing, the effectiveness of these controllers in the presence of the twice line frequency, large signal excitations required of buck-type PFC rectifiers has yet to be shown. Additionally, since the controllers work entirely upon control of the inductor current, they require high-speed, accurate analog current sensing and they lack explicit monitoring and control of the flying capacitor voltages.

3.2 FCML Converter as a Buck-Type PFC

Ideal N -level FCML converter operation requires that the flying capacitor voltages $v_{C,k}$ maintain the balanced voltage distribution $v_{C,k} = k \cdot v_{io} / (N - 1)$ where v_{io} is the output voltage of a boost-type FCML converter or the input voltage in a buck-type FCML converter [1] and N is the number of voltage levels apparent in the switch node waveform v_{sw} . The v_{io} voltages for a boost-type and buck-type FCML rectifier are labeled in Fig. 3.4. If the aforementioned flying capacitor voltage distribution is achieved, the switch blocking voltage stress is evenly distributed across all the switches at a value of $v_{ds} = v_{io} / (N - 1)$ and low-voltage, high figure-of-merit switches can be employed [1], [9]. Many FCML converter designs rely on “passive balancing” to achieve the desired flying capacitor voltage distribution, gating the switches in the converter with symmetric phase-shifted PWM (PS-PWM). This approach relies on the natural dynamics of the FCML converter, such as those investigated in [20], [24], [39], [40], [41], [42], [43] and Chapter 7 to passively balance the flying capacitor voltages to the ideal distribution.

The buck-type PFC rectifier presents a unique challenge for FCML converter control as passive balancing is typically unable to achieve the ideal flying capacitor voltage distribution. As an illustrative example, Fig. 3.4 compares the salient state variables of a boost-type [44], [45], [46], [47], [48] and buck-type FCML PFC converter. The flying capacitor voltages within a boost-type PFC rectifier are ideally constant with respect to time as typically these rectifiers are designed to operate with an output voltage with relatively small ripple. Given that the output voltage is roughly constant, passive balancing can be usually relied upon to achieve the desired flying capacitor voltage distribution, requiring no active flying capacitor voltage control. In contrast, since the input voltage of the buck-type PFC converter is a rectified version of the grid voltage, the flying capacitor voltages must track this voltage variation to minimize switch voltage stress. Practical switching frequencies, flying capacitances, and

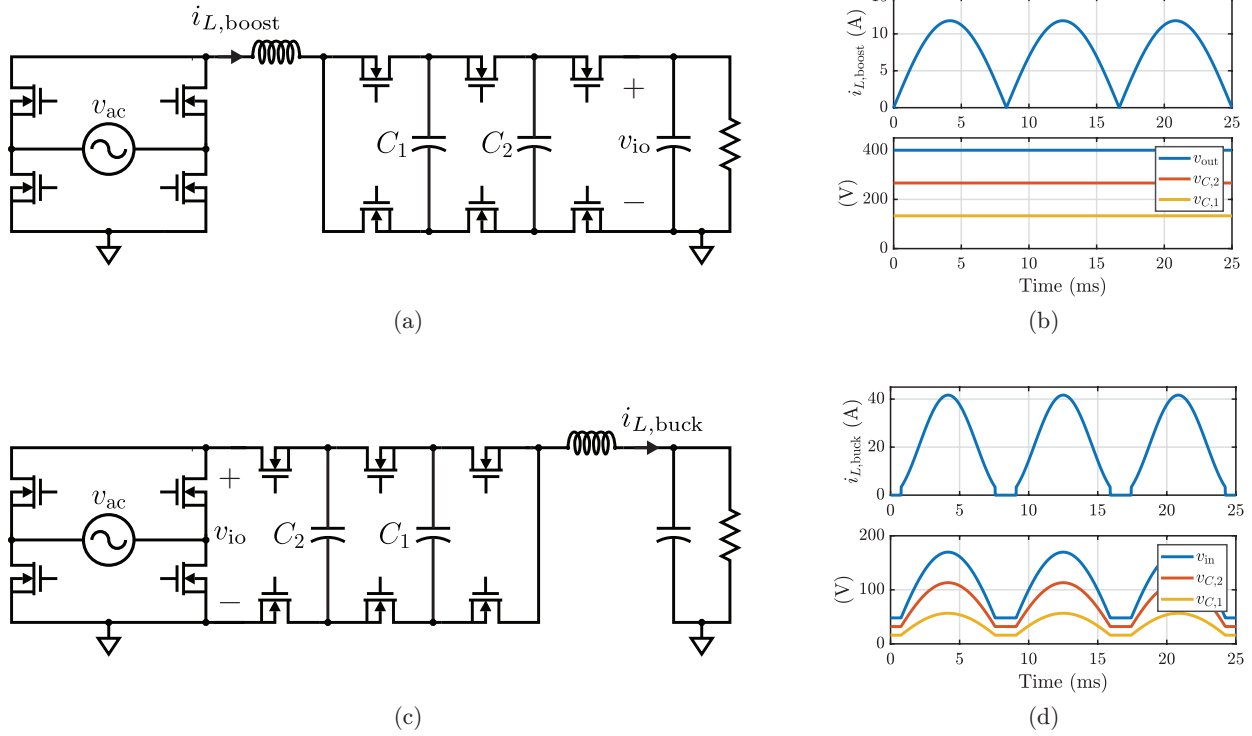


Figure 3.4: Comparison between boost-type and buck-type four-level FCML PFC rectifiers. (a) Four-level boost-type FCML rectifier. (b) Nominal inductor current and capacitor voltages for the boost-type FCML rectifier. (c) Four-level buck-type FCML rectifier. (d) Nominal inductor current and capacitor voltages for the buck-type FCML rectifier. The boost-type FCML PFC converter operates at $v_{ac} = 120 \text{ V}_{\text{rms}}$ and $V_{\text{out}} = 400 \text{ V}$. The buck-type FCML PFC converter operates $v_{ac} = 120 \text{ V}_{\text{rms}}$ and $V_{\text{out}} = 48 \text{ V}$. Both converters process $P_{\text{out}} = 1 \text{ kW}$. The flying capacitor voltages in the buck-type rectifier must track reference values that correspond to fractions of the time-varying grid voltage. The large-signal line frequency variation in the flying capacitor voltage reference presents a challenge compared to boost-type FCML rectifiers where the capacitor voltages must only track a dc reference voltage.

output inductance values limit the “bandwidth” of passive balancing to a few hertz [35], making reliance on passive balancing for the buck-type FCML rectifier infeasible to track the grid frequency. Previous work [31] attempting to rely upon passive balancing for a buck-type FCML rectifier increased the bandwidths of passive balancing by significantly reducing both the converter switching frequency and the output inductance L_{out} . The excessively large inductor current ripple, however, negatively impacted converter efficiency, power density, and grid current quality.

This work directly addresses the challenge of flying capacitor voltage tracking at the twice-line frequency by employing an active flying capacitor voltage balancing controller which works in tandem with the inductor current controller. With this control strategy, the switch voltage stress can be reduced and the inductor current track the desired reference. More details on the control structure are provided in Section 3.3.

Finally, single-phase buck-type PFC rectifiers are unable to achieve unity power factor

Table 3.1: Theoretical Buck-Type PFC Mains Current Quality

Input Voltage	Output Voltage	Power Factor	THD
240 V _{rms}	48 V _{dc}	0.999	3.47%
208 V _{rms}	48 V _{dc}	0.999	4.31%
120 V _{rms}	48 V _{dc}	0.9951	9.97%

grid current. This is due to the fact that the converter should not operate when $|v_{ac}(t)| < V_{out}$. When the grid voltage magnitude is smaller than the converter output voltage, there is not a valid periodic steady state solution for the converter and the converter currents will be uncontrolled. To prevent this uncontrolled operation, the converter will turn OFF and conduct no grid current during these portions of the line cycle (see Fig. 3.4(d)). Although previous works have shown that this mode of operation is acceptable, we reiterate the high quality of mains current achievable for typical mains and output voltages [32], [34]. Table 3.1 provides the theoretical input current quality for a buck-type PFC rectifier, derived in [35].

3.3 Flying Capacitor Voltage and Inductor Current Control

The derivation of the control law utilized in this work follows that of [49], [50]. However, this work, which operates the FCML converter as a step-down rectifier, requires that the flying capacitor voltages track a U.S. mains twice-line frequency (120 Hz) large-signal reference and that the inductor current begins and ends at zero current every half-line cycle. The controller design in this work thus builds upon these previous works to achieve a satisfactory solution for the buck-type PFC application. The controller for this application will be discussed after first analyzing the FCML converter to generate a suitable plant model.

3.3.1 Plant Model Derivation

The FCML converter contains an inherent cross-coupling between the inductor current and the flying capacitor voltages. In this work, we utilize state space averaging [51] (denoting $\langle x \rangle$ the average value of x over a switching period) to analyze the plant and develop a decoupled control law from the plant characteristics. Moreover, we assume that the input and output voltages, flying capacitor voltages, and inductor current are well approximated by their average values, such that the assumptions of state space averaging hold. Under

these assumptions, the time-averaged capacitor current $\langle i_{C,k} \rangle$ is

$$C_k \frac{d}{dt} \langle v_{C,k} \rangle = \langle i_{C,k} \rangle = \langle (q_{k+1} - q_k) i_L \rangle \quad (3.1)$$

$$\approx \langle q_{k+1} - q_k \rangle \langle i_L \rangle = \Delta d_k \langle i_L \rangle, \quad (3.2)$$

where d_k is the duty cycle of switching cell k and $\Delta d_k = d_{k+1} - d_k$. For FCML converters operated with symmetric PS-PWM (i.e., $\Delta d_k = 0$), the state space averaged model predicts flying capacitor voltages which are constant with respect to time. Thus, this model cannot capture the passive flying capacitor voltage balancing mechanisms inherent to the FCML converter [20], [41], [52]. However, as will be shown, the state space averaged model is sufficient to capture flying capacitor voltage dynamics that result from nonzero Δd_k .

Similarly, the average inductor current evolution is

$$\begin{aligned} L_{\text{out}} \frac{d}{dt} \langle i_L \rangle &= \langle v_L \rangle \\ &= \left\langle v_{\text{in}} q_{N-1} - v_{\text{out}} - \sum_{k=1}^{N-2} (q_{k+1} - q_k) v_{C,k} \right\rangle \\ L_{\text{out}} \frac{d}{dt} \langle i_L \rangle &\approx v_{\text{in}} d_{N-1} - \langle v_{\text{out}} \rangle - \sum_{k=1}^{N-2} \Delta d_k \langle v_{C,k} \rangle. \end{aligned} \quad (3.3)$$

Linearizing this model, denoting the small signal variables as $\tilde{x}$ and quiescent operating variables as X (i.e., $x = X + \tilde{x}$), about the quiescent point where all flying capacitors are balanced (i.e., $V_{C,k} = k \cdot V_{\text{in}} / (N - 1)$) and all duty cycles are equal (i.e., $\Delta d_k = 0$) yields

$$C_k \frac{d}{dt} \langle \tilde{v}_{C,k} \rangle = I_L \Delta \tilde{d}_k \quad (3.4)$$

and

$$L_{\text{out}} \frac{d}{dt} \langle \tilde{i}_L \rangle = V_{\text{in}} \tilde{d}_{N-1} - \sum_{k=1}^{N-2} \frac{k V_{\text{in}}}{N - 1} \Delta \tilde{d}_k - \langle \tilde{v}_{\text{out}} \rangle. \quad (3.5)$$

Here it can be seen that the average flying capacitor voltages respond only to the differences in adjacent duty cycles while the average inductor current responds to a weighted sum of all duty cycles and the output voltage.

A schematic diagram showing the plant model under the assumption of state space averaging is shown in Fig. 3.5(a). One control design objective, shown in Fig. 3.5(b), is to achieve flying capacitor voltages $v_{C,k}$ that are controlled independently from the controlled inductor current i_L . The loop gain for each state variable in this example control system is designed to be a single pole integrator with cutoff frequency ω_C and ω_L , resulting in a

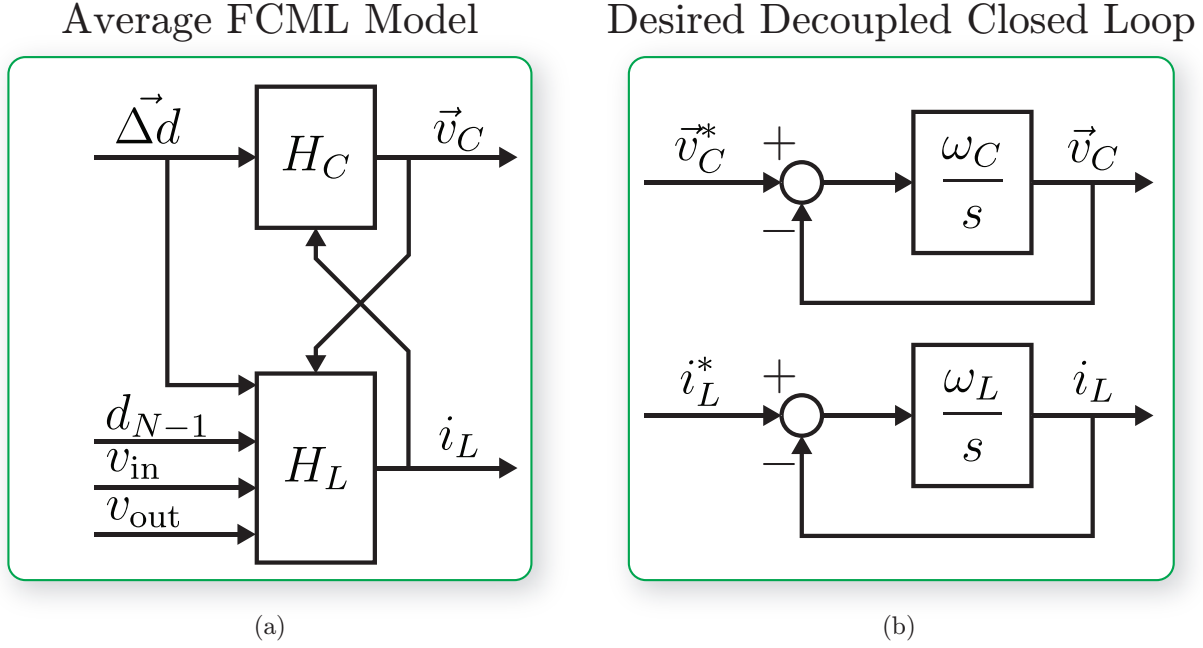


Figure 3.5: (a) Block diagram of the state-space averaged model of an FCML converter explicitly showing the cross-coupling between flying capacitor voltages $\vec{v}_C$ and inductor current i_L . Block H_C is described by (3.2) and block H_L is described by (3.3). (b) Block diagram of the desired decoupled closed loop system with input reference flying capacitor voltages $\vec{v}_C^*$ and reference inductor current i_L^* . The controller is designed to both decouple and control the flying capacitor voltages and the inductor current.

single-pole low pass filter closed loop transfer function for each flying capacitor voltage and the inductor current.

As a further illustrative example, Fig. 3.6 provides a time-domain perspective on how the flying capacitor voltages respond to differences in duty cycles Δd_k . This three-level FCML converter example simplifies converter behavior by modeling the inductor current as a constant current source. In reality, the average inductor current will respond to non-zero Δd_k as (3.3) predicts. Judicious controller design must thus be able to decouple the impact of Δd_k on the inductor current i_L .

3.3.2 Controller Design

Given the derived plant model of Fig. 3.5(a), one control design approach is to apply linear state feedback decoupling [53], [54] to decouple the state variables. Linear state feedback decoupling simplifies control design by cancelling the inherent state variable cross-couplings, creating multiple single-input single-output (SISO) systems from the multi-input multi-output (MIMO) plant as shown in Fig. 3.5(b). From a small signal, averaged perspective, the flying capacitor voltages $v_{C,k}$ are inherently decoupled from the small signal dynamics of the inductor current i_L and other flying capacitor voltages $v_{C,k}$ as evidenced by (3.4).

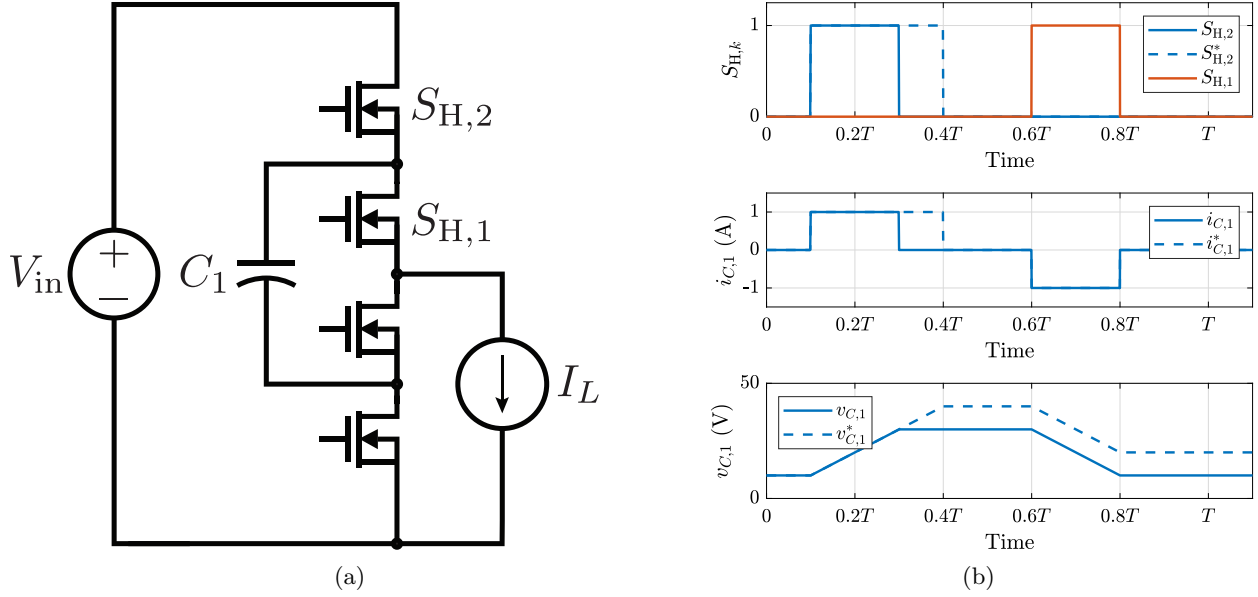


Figure 3.6: Illustration of the flying capacitor voltage characteristics described by (3.2). (a) Three-level FCML converter schematic in which the inductor current is modeled as a dc current source $I_L = \langle i_L \rangle$. (b) Switching signals and flying capacitor waveforms under nominal PS-PWM and active balancing. The duty cycle of $S_{H,2}^*$ has been slightly increased, resulting in a positive Δd_1 . Under the assumption of constant current I_L , $\Delta d_1 > 0$ results in an increase in charge deposited on C_1 and an increase in $v_{C,1}$ at the end of the switching period as (3.2) predicts.

Controlling Δd_k in response to flying capacitor voltage imbalance is thus a straightforward and effective control strategy for regulating the flying capacitor voltages.

As (3.5) shows, the inductor current will respond both to the outputs of the flying capacitor voltage balancing controllers and d_{N-1} . To decouple the inductor current from the flying capacitor voltage balancing controllers, we decompose d_{N-1} into a feedback part which is the output of the inductor current feedback loop and a feedforward path

$$d_{N-1} = u + \mathbf{B} \vec{\Delta} d, \quad (3.6)$$

where u is the output of the inductor current feedback loop and the vector $\mathbf{B}$ decouples the active flying capacitor voltage balancer controller output from the inductor current loop with:

$$\mathbf{B} = \frac{1}{N-1} [1 \quad 2 \quad \dots \quad k]. \quad (3.7)$$

After applying linear state feedback decoupling, the plant dynamics in the Laplace domain are represented as:

$$C_k \frac{d}{dt} \langle \tilde{v}_{C,k} \rangle = \Delta d_k \langle i_L \rangle \rightarrow \langle \tilde{v}_{C,k} \rangle(s) = \frac{I_L}{s C_k} \tilde{\Delta} d_k(s) \quad (3.8)$$

$$L_{out} \frac{d}{dt} \langle \tilde{i}_L \rangle = V_{in} u - \langle \tilde{v}_{out} \rangle \rightarrow \langle \tilde{i}_L \rangle(s) = \frac{1}{s L_{out}} (V_{in} u(s) - \langle \tilde{v}_{out} \rangle(s)) \quad (3.9)$$

We continue the controller design to achieve the design objective, shown in Fig. 3.5(b), of a flying capacitor voltage loop gain of $T_{v_C}(s) = \omega_C/s$. We represent the active flying capacitor voltage balancing controller as $G_{v_C,k}$ with output $\Delta\tilde{d}_k$:

$$\langle v_{C,k} \rangle(s) = \frac{I_L}{sC_k} G_{v_C,k} \cdot \langle v_{C,k,\text{error}} \rangle(s) \quad (3.10)$$

$$\Delta d_k = G_{v_C,k} \langle v_{C,k,\text{error}} \rangle(s) \rightarrow \Delta d_k = \frac{C_k \omega_C}{I_L} \langle v_{C,k,\text{error}} \rangle(s), \quad (3.11)$$

where $v_{C,k,\text{error}} = v_{C,k}^* - v_{C,k}$. The active flying capacitor voltage balancer $G_{v_C,k}$ is thus a proportional controller to achieve the desired loop gain. To achieve the desired inductor current loop gain of $T_{i_L}(s) = \omega_L/s$, we design the inductor current controller with

$$\tilde{d}_{N-1} = u + \sum_{k=1}^{N-2} \frac{k \Delta\tilde{d}_k}{N-1} \quad (3.12)$$

$$= \frac{1}{V_{\text{in}}} (\omega_L i_{L,\text{error}} + \langle \tilde{v}_{\text{out}} \rangle) + \sum_{k=1}^{N-2} \frac{k \Delta\tilde{d}_k}{N-1}. \quad (3.13)$$

A schematic diagram of the control architecture is provided in Fig. 3.7. As discussed in [49], the desire to mitigate inaccuracies in the plant model and to increase resiliency to disturbances motivate the cascade of a PI controller with the proportional feedback linearizing controller described above, as can be seen in Fig. 3.7(b). In [49], it is recommended to design the PI controller with proportional gain $K_p = 1$ and integral gain $K_i = \omega_L$ to “keep a first order transfer function between” the inductor current i_L and the inductor current reference i_L^* .

In this work, however, we introduce a constant scaling term γ in the design of the controller. In experiment, with $\gamma = 1$ (i.e., that same controller design as in [49]) it was noticed that the inductor current waveform exhibited oscillations at a frequency of approximately 1 kHz. By reducing γ to 0.25, the zero frequency of the PI controller is reduced by a factor of γ^2 , improving the phase margin of the inductor current loop. This controller modification resulted in the virtual elimination of the observed oscillations.

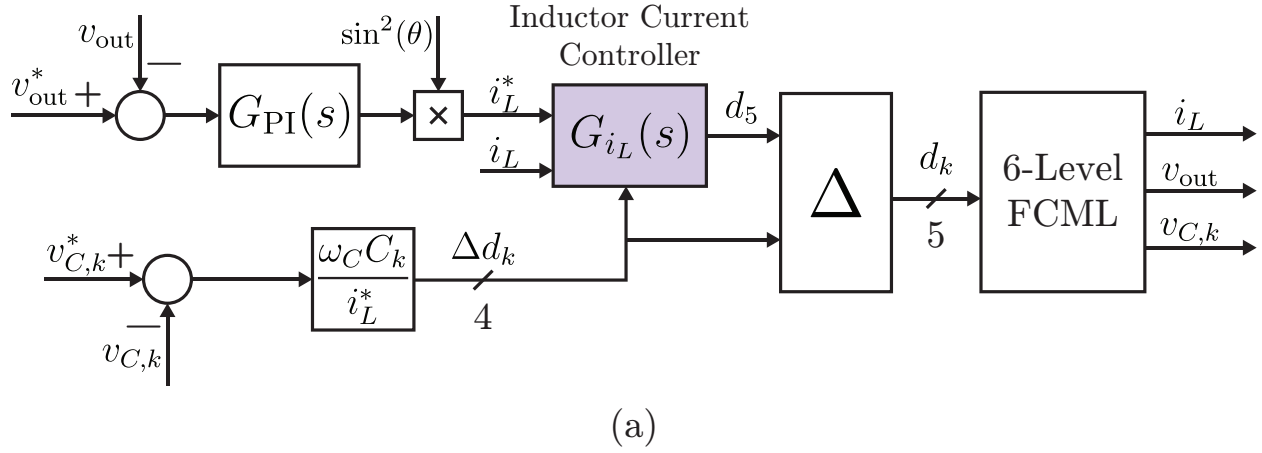
Assuming the controller is able to perfectly linearize the plant (i.e., reject the contribution of Δd_k and V_{out} on the inductor current i_L), the loop gain of the inductor current loop is

$$T_{i_L}(s) = \frac{\omega_L(s(1 + \gamma^{-1}) + \omega_L \gamma)}{s^2}. \quad (3.14)$$

For $\gamma = 1$, the crossover frequency ω_c of T_{i_L} is

$$\omega_c = \omega_L \sqrt{\sqrt{5} + 2} \approx 2.06 \omega_L. \quad (3.15)$$

Above the zero at $\omega_L \gamma / (1 + \gamma^{-1})$, the loop gain is approximately $T(s) \approx (1 + \gamma^{-1}) \omega_L / s$. The crossover frequency is thus $\omega_c \approx (1 + \gamma^{-1}) \omega_L$. (3.15) provides the explicit relationship



Inductor Current Controller

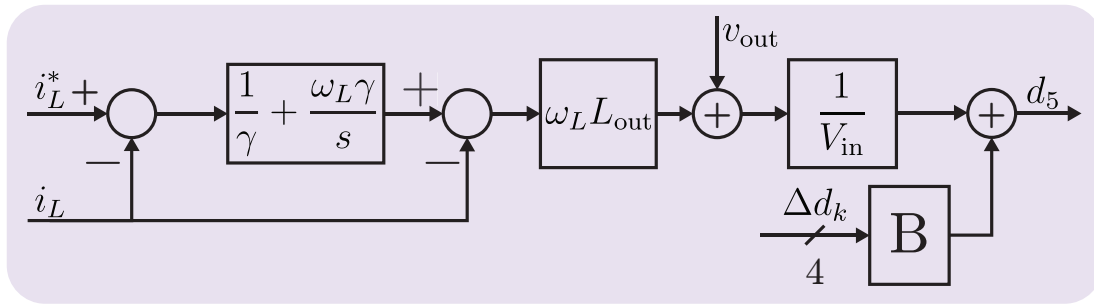


Figure 3.7: Block diagram for the implemented combined active flying capacitor voltage balancer and inductor controller for a six-level FCML converter. (a) Overall control structure. (b) Inductor current controller which includes both linearization terms and a cascaded PI controller. The Δ block reconstructs the duty cycles from the d_5 and Δd duties through the following formula: $d_k = d_{k+1} - \Delta d_k$. The **B** block scales the output of the active balancing controller such that the inductor current is unaffected by the active flying capacitor voltage balancer as described by (3.7).

between controller parameter ω_L and inductor current loop crossover frequency ω_c . For a controller with $\gamma = 1$, the closed loop transfer function from i_L^* to i_L is

$$\frac{i_L^*}{i_L}(s) = \frac{\omega_L}{s + 0.75\omega_L}, \quad (3.16)$$

a first-order transfer function with bandwidth ω_L .

Fig. 3.8 plots two theoretical inductor current loop gains; the first controller is configured with $\omega_L = 20 \times 10^3$ rad/s and $\gamma = 1$ while the second controller has the same ω_L and $\gamma = 0.25$. The controller with $\gamma = 1$ attains a crossover frequency of 41.2×10^3 rad/s with 76.3° of phase margin while the controller with $\gamma = 0.25$ has a crossover of 100×10^3 rad/s with a phase margin of 89.4° . The proposed constant scaling term is thus able to achieve improved crossover frequency *and* phase margin, compared to previous approaches.

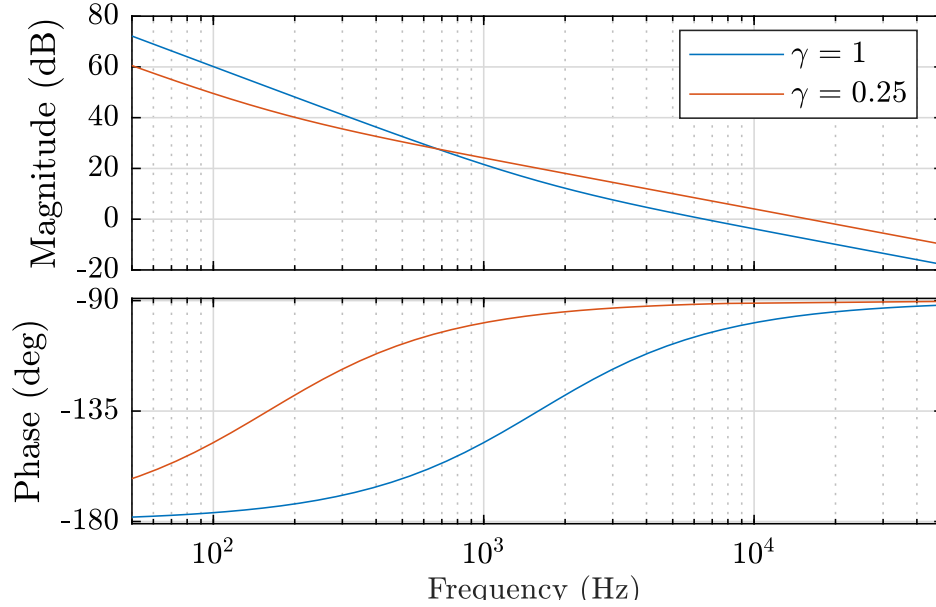


Figure 3.8: Simulated inductor current loop gain T_{iL} for $\omega_L = 20 \times 10^3 \text{ rad/s}$. The controller designed with $\gamma = 0.25$ achieves both a larger crossover frequency and phase margin compared to the controller configured with $\gamma = 1$.

3.3.3 Simulation Validation

A simulation study is performed to compare the effectiveness of the proposed active flying capacitor voltage balancing control strategy to passive balancing. Both simulations involve a six-level FCML buck-type PFC rectifier operating at $V_{ac} = 240 \text{ V}_{\text{rms}}$, $V_{out} = 48 \text{ V}$, $P_{out} = 800 \text{ W}$, $f_{sw} = 100 \text{ kHz}$, $C_{fly} = 10 \mu\text{F}$, $L_{out} = 6.8 \mu\text{H}$, $\omega_C = 2\pi \times 10^3 \text{ rad/s}$, and $\omega_L = (2\pi)4 \times 10^3 \text{ rad/s}$. The simulation used linear capacitors with the aforementioned capacitance for the flying capacitors rather than capacitors whose small-signal capacitance depends on the dc bias voltage. The utilization of nonlinear flying capacitors is discussed in Section 4.3. The converter operated with active balancing utilizes the previously described control laws while the converter relying on passive balancing sets all $\Delta d_k = 0$.

Fig. 3.9 compares the response of the flying capacitor voltages and the maximum switch v_{ds} stress. The v_{ds} stress is calculated as follows: for switches between two flying capacitors (e.g., $S_{H,2-4}$ for a six-level FCML converter), the v_{ds} stress is the difference in the adjacent flying capacitor voltages; $v_{ds,1} = v_{C,1}$ and $v_{ds,5} = v_{in} - v_{C,4}$ for the final two switch pairs. The maximum v_{ds} stress for the actively balanced FCML rectifier is 75.9 V while the passive balance rectifier is 139.3 V , over $1.8\times$ larger. Active flying capacitor voltage control is thus vital to achieve high converter efficiency through the use of low voltage semiconductor switches.

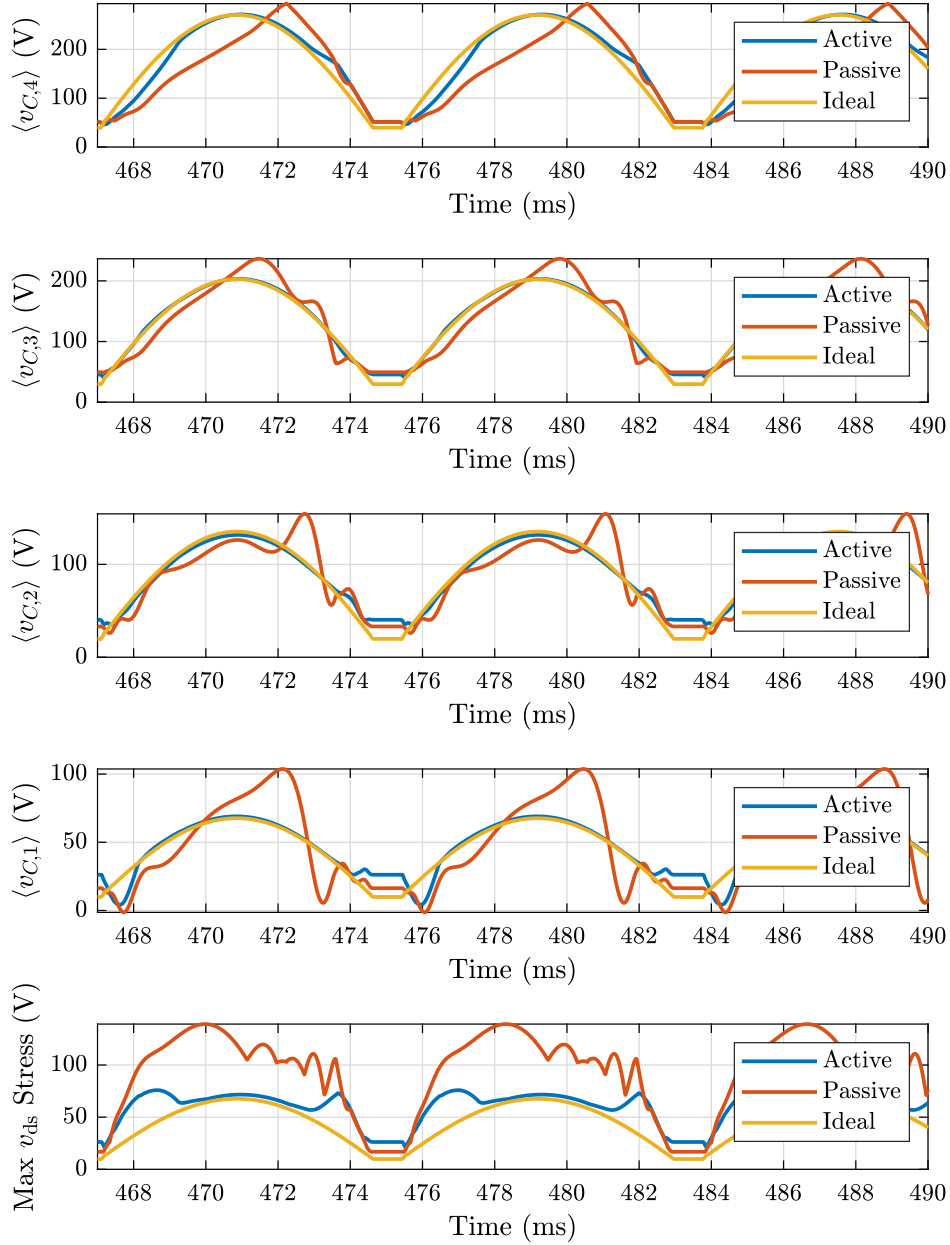


Figure 3.9: Simulated six-level FCML buck-type rectifier average flying capacitor voltages $\langle v_{C,k} \rangle$ and maximum v_{ds} stress operated under active and passive balancing. The converter operated with passive balancing is unable to achieve flying capacitor voltage balance and results in severe increased switch voltage stress.

3.4 Experimental Results

The aforementioned control structure was implemented and tested experimentally using a six-level hardware prototype operated at a switching frequency of 100 kHz (i.e., an effective switching frequency seen at the switch node voltage v_{sw} of 500 kHz.). A photograph of

Table 3.2: Circuit Parameters

Component	Description	Part Number
$S_{L,H,k}$	100 V, 1.8 m Ω eGaN FET	EPC2302
C_{fly}	$4 \times 2.2 \mu\text{F}$	C5750X6S2W225K250KA
L_{out}	10 μH	IHLP6767GZER100M51
C_{out}	$18 \times 2.2 \mu\text{F}$	C5750C0G2J104J280KC
C_{buf}	$3 \times 18 \text{ mF}$	380LX183M063A082
Rectifier	650 V, $2 \times 69 \text{ m}\Omega$	STL57N65M5
C_{in}	$14 \times 2.2 \mu\text{F}$	C5750X6S2W225K250KA
L_{line}^*	10 μH	IHLP6767GZER100M51
C2000 DSP	32-bit MCU with 800 MIPS	TMS320F28379D
AC source	2 kVA power source	Chroma 61504
Power analyzer	0.05% accuracy	Keysight PA2201A

* L_{line} was connected in series with the ac voltage source.

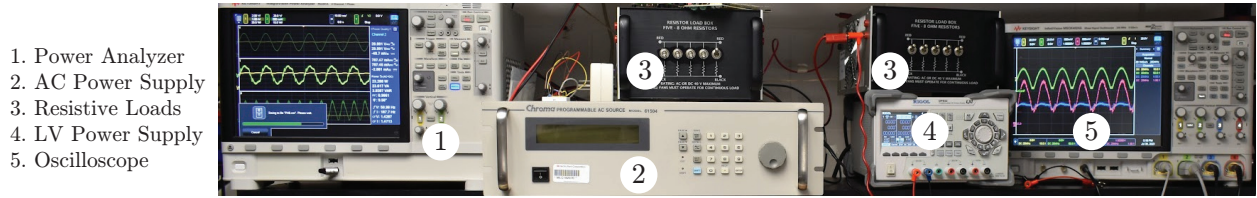


Figure 3.10: Photograph of experimental setup. The ac power supply used is a Chroma 61504 while power factor is computed by the Keysight PA2201A.

the experimental equipment is provided in Fig. 3.10 while an annotated photograph of the hardware prototype is provided in Fig. 3.11. The components associated with this hardware prototype are given in Table 2.4. Converter control and switching signal generation were performed by one core of the C2000 F28379D digital signal processor (DSP). The DSP samples the system variables and executes the control law within a single switching period of 10 μs . The flying capacitor voltages were delivered to the onboard ADCs of the DSP through an analog front end composed of a resistor divider followed by an AD8429 non-isolated instrumentation amplifier. The inductor current was measured through a ground referenced current sense resistor and LT1999 current sense amplifier. The flying capacitor voltage and inductor current sensing circuits are shown schematically in Fig. 3.11(b) and (c). The following experimental parameters were utilized for the presented results: $v_{\text{ac}} = 120 \text{ V}_{\text{rms}}$, $V_{\text{out}} = 48 \text{ V}$, and $R_{\text{load}} = 5.3 \Omega$. A cascaded second order generalized integrator (SOGI) architecture [55], [56] was used to generate the reconstructed direct and quadrature grid voltages for phase-locking.

This work utilized Class II MLCC capacitors (part number provided in Table 2.4) to con-

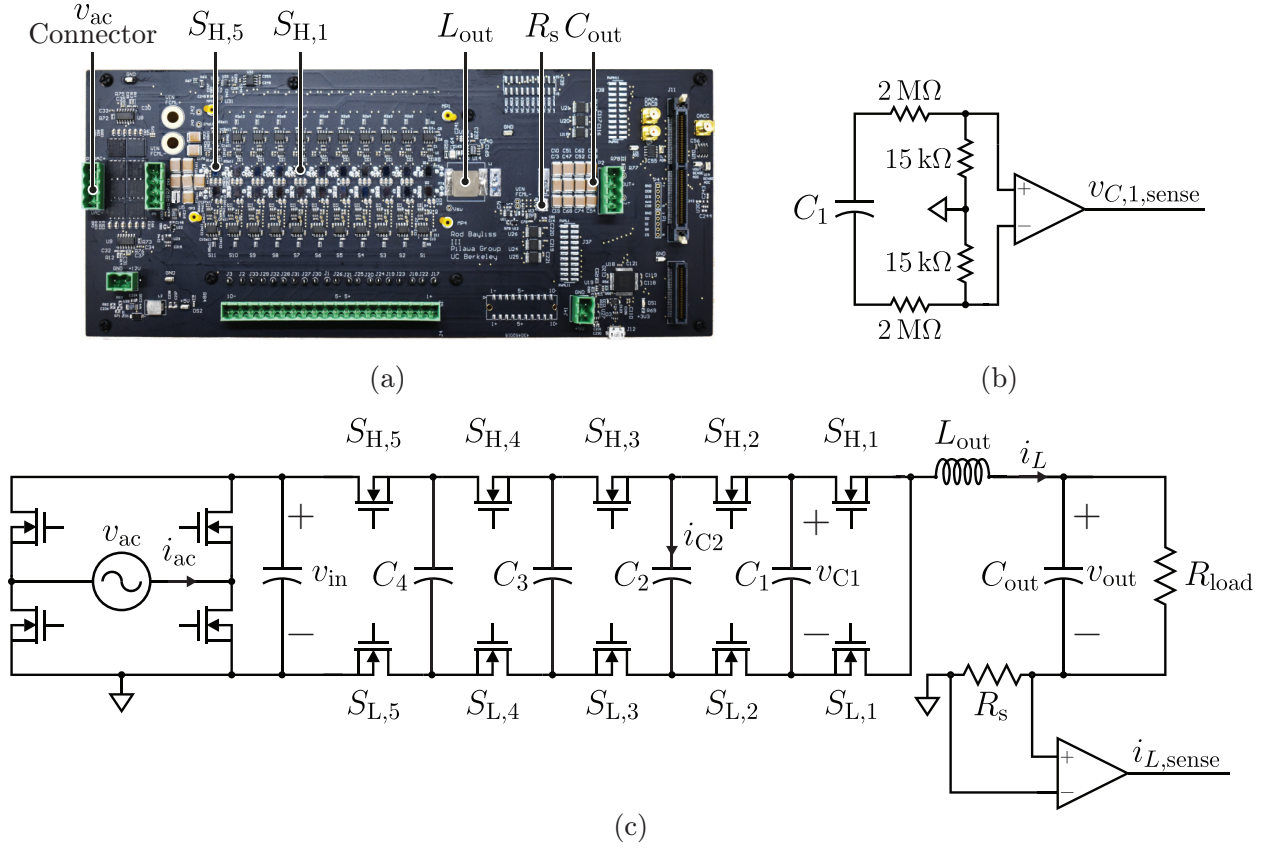


Figure 3.11: (a) Annotated photograph of the FCML converter hardware prototype. Circuit parameters for the FCML converter are given in Table 2.4. This 12-level FCML converter is configured to operate as a five-level FCML converter by soldering a wire which connects the source of $S_{H,1}$ to the drain of $S_{L,1}$ and to the inductor L_{out} . (b) Schematic of flying capacitor voltage sensing circuit, shown for flying capacitor C_1 . The flying capacitor voltages are measured with a non-isolated instrumentation amplifier (part number AD8429). All four flying capacitor voltages are sensed via copies of this circuit. (c) Six-level FCML converter schematic with inductor current sensor explicitly drawn. The inductor current i_L is measured by a ground-referenced current sense resistor R_s and differential amplifier (part number LT1999).

struct the input, output, and flying capacitors due to their superior energy density compared to other capacitor technologies [7]. One notable characteristic of the class II dielectric is the small-signal capacitance dependence on the dc bias voltage; generally, the capacitance decreases with dc bias voltage. For the capacitor used in this work, at the rated dc bias voltage the small-signal capacitance is reduced to $\approx 18\%$ of the zero-bias value. At the peak of the input voltage ($V_{pk} = 169.7\text{ V}$), the highest voltage flying capacitor C_4 has a capacitance of $4.2\text{ }\mu\text{F}$ while the lowest voltage flying capacitor C_1 has a capacitance of $8\text{ }\mu\text{F}$. To account for this dynamic capacitance variation, the controller updates the modeled capacitance using a linear fit of the small signal capacitance with reference flying capacitor voltage at each sampling period. The controller utilizes the following formula to calculate the small-signal

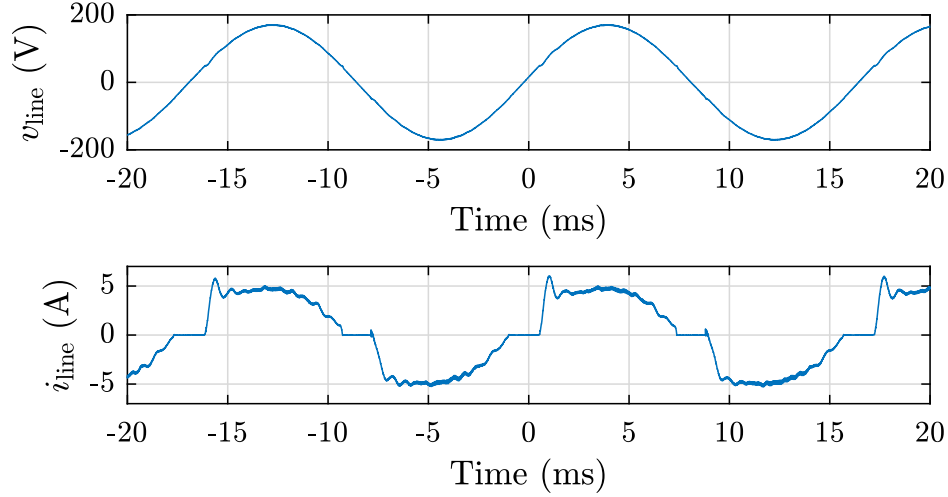


Figure 3.12: Measured line voltage v_{line} and line current i_{line} . The measured input current achieves a power factor of 0.9697, a phase shift of 14.14° , and a THD of 19.5% as measured by a Keysight PA2201A power analyzer.

flying capacitor capacitance,

$$C_k = 4 \cdot (2 \times 10^{-6} - 1 \times 10^{-8} v_{C,k}).$$

Through experimental testing, the controller parameters were set as $\omega_C = 3 \times 10^3 \text{ rad/s}$ and $\omega_L = 20 \times 10^3 \text{ rad/s}$. These controller gains resulted in flying capacitor voltages which tracked their references sufficiently well to limit the switch voltage stress while achieving high power factor input current.

Fig. 3.12 plots the measured converter input current and the measured high power factor of 0.969 reflects satisfactory power factor correction. The input current i_{line} achieves a THD of 19.5%, 9.5 percentage points higher than the theoretically minimal THD for the given input and output voltage [35]. The degradation of THD is likely due to the overshoot present in the mains current when the input voltage becomes greater than the output voltage and the converter begins switching. This overshoot is primarily caused by the limited controller sampling frequency relative to large dv_{in}/dt near the zero-crossing and the small output inductance employed in this work. Fig. 3.13 provides simulation results showcasing the impact the output inductance has on the inductor current overshoot when the converter is turned on. The crossover frequency and phase margin of the three converters are nearly identical. However, the circuits employing the smaller output inductances exhibit more overshoot. The input voltage to the buck converter under test is equal to $v_{\text{in}} = \max \{240\sqrt{2}\text{abs}(\sin \omega t), 48\}$ while the output voltage is a constant 48 V. All three converters operate at a digital control sampling frequency of 100 kHz and a switching frequency of 500 kHz. The inductor current loops for all three circuits attain a crossover frequency of 9.6 kHz with a phase margin of 63° . A full investigation of this zero-crossing distortion remains an area of interest for future work.

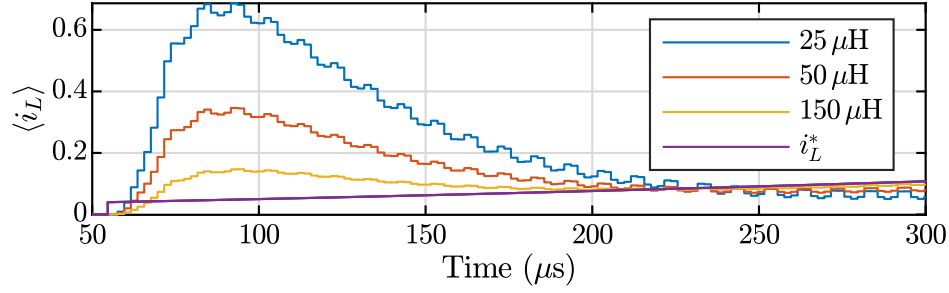


Figure 3.13: Simulation results of the average inductor current $\langle i_L \rangle$ and inductor current reference i_L^* for a buck converter operating with the ideal buck-type PFC input voltage and a constant output voltage. Immediately after the converter begins switching, the large dv_{in}/dt causes an overshoot in the inductor current. This effect is exacerbated for small inductance values. The input voltage is defined by $v_{in} = \max \{240\sqrt{2}\sin(\omega t), 48\}$.

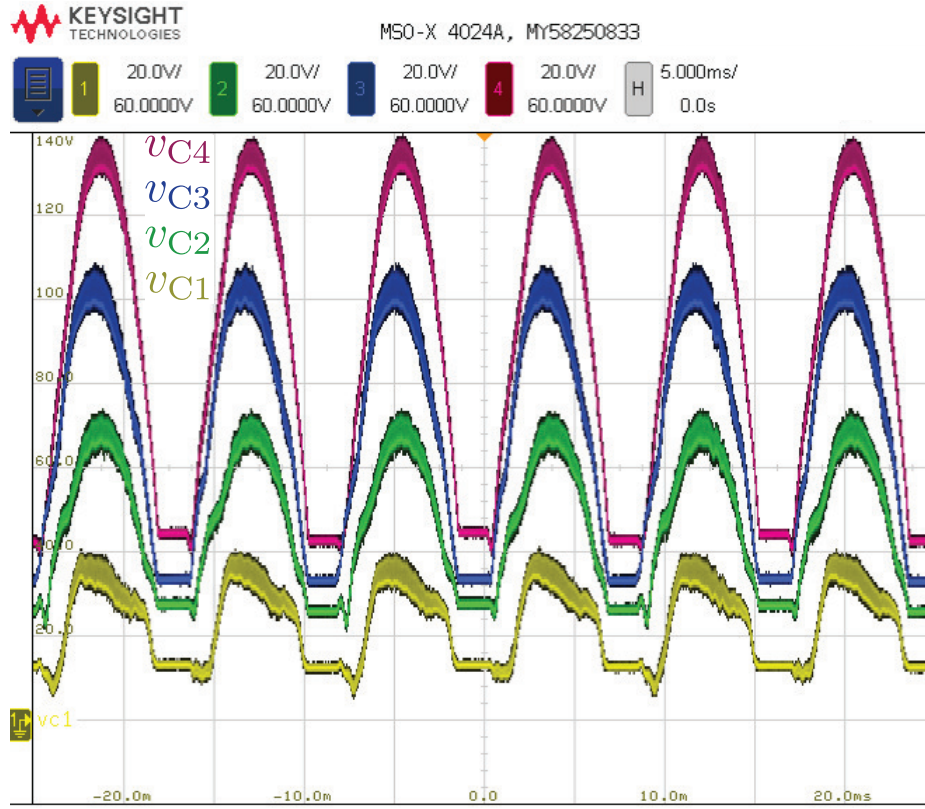


Figure 3.14: Measured flying capacitor voltages. The flying capacitor voltages are able to track their reference values sufficiently well to limit the peak switch voltage stress.

Fig. 3.14 shows oscilloscope captures of the flying capacitor voltages while Fig. 3.15 shows the drain-source voltage stress applied across the switches. Through the developed active balancing control strategy, the flying capacitor voltages are able to track the 120 Hz sinusoidal reference and limit the switch voltage stress. The peak drain-source voltage stress

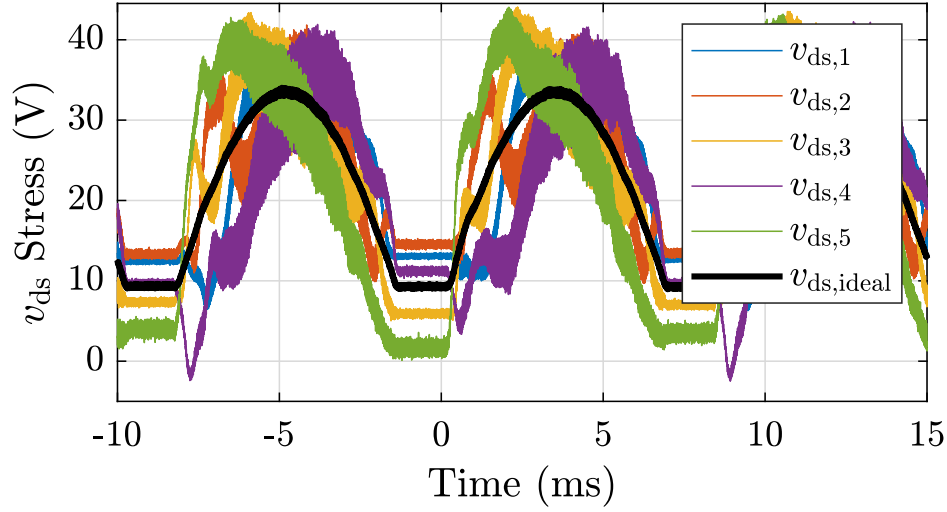


Figure 3.15: Measured switch drain-source voltage stress for the operating conditions described in Section 4.3. Ideally the peak switch drain-source voltage is $v_{in}/(N-1)$ which is achieved when all flying capacitor voltages are at the balanced distribution. The peak drain-source voltage stress was 44.5 V which is 31% higher than the ideal voltage stress.

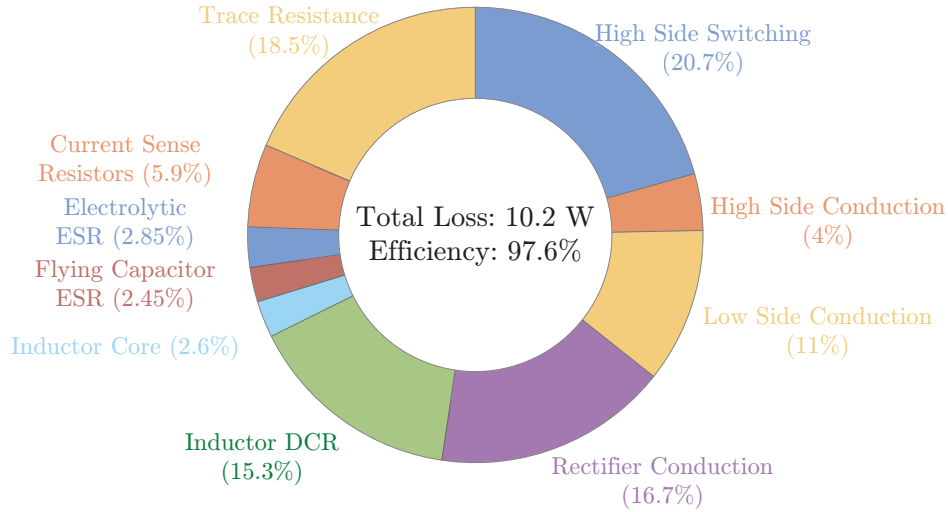


Figure 3.16: Simulated loss breakdown for $P_{out} = 420$ W. DC trace resistance was estimated through FEA simulations performed in ANSYS Maxwell.

was 44.5 V, 31% higher than the ideal voltage stress.

This work employs high energy density X6S capacitors for the flying capacitors (part number provided in Table 2.4). Although previous works have documented losses associated with applying a large ac voltage swing on the capacitors [57], [58], [59], the magnitude of the flying capacitor voltage swing in this work was sufficiently small to not excite excessive hysteretic dielectric losses through this mechanism. Utilizing the polynomial fit of the measured large signal losses for the input and flying capacitors provided in [58], the flying

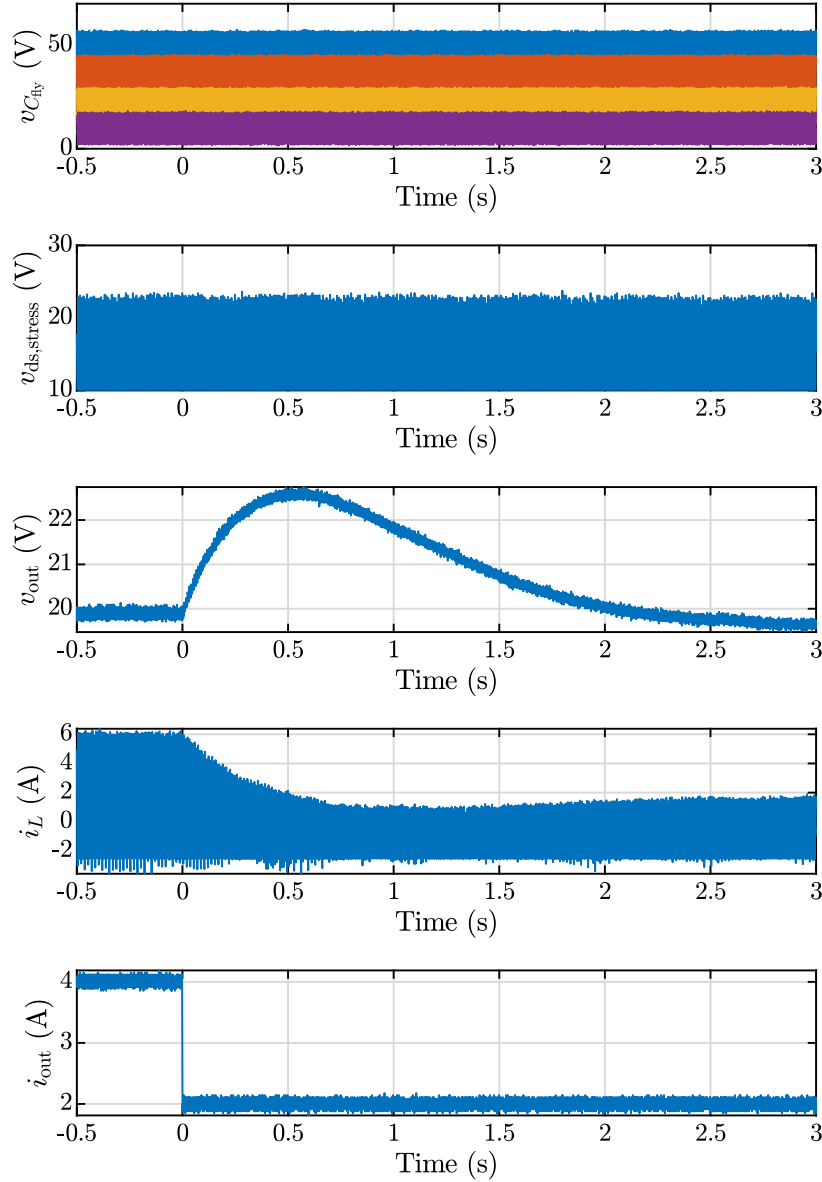


Figure 3.17: Measured prototype transient response when subjected to an output current step. The converter is connected to a 50 V_{rms} ac voltage source while the electronic load is commanded to step from 4 A to 2 A . Throughout the transient, flying capacitor voltage balance is maintained as indicated by the nearly constant peak $v_{\text{ds, stress}}$.

capacitor losses were calculated to be 100 mW . The input capacitor, which experiences the largest voltage swing, exhibits a loss of 213 mW . The flying capacitors within the study of [58] were excited with a 120 Hz sinusoidal voltage source with a dc bias, in contrast with the ideal flying capacitor voltages within an FCML buck-type PFC which are (predominantly) rectified sinusoids. Thus to approximate the hysteretic losses using the aforementioned data, we utilized the ideal peak to peak flying capacitor voltage $(k \cdot V_{\text{ac, peak}} / (N - 1) - V_{\text{out}})$ and

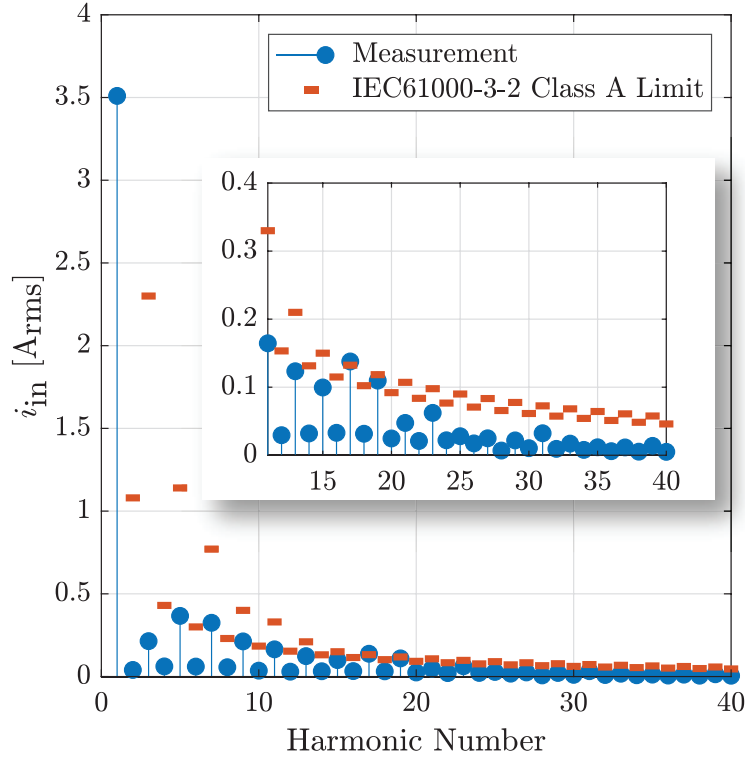


Figure 3.18: Measured input current harmonics reported by the Keysight Power Analyzer PA2201A. At an output power of 432 W, all harmonics pass except for the 17th harmonic (1.02 kHz) which is 4% over the limit. Note that the IEC61000-3-2 limits [60] are strictly applicable only for equipment operated at an input voltage above $v_{ac} = 230 \text{ V}_{\text{rms}}$. However the comparison is reported here to convey the magnitude of the harmonics relative to industry standards.

mean flying capacitor voltage across a line cycle to approximate the peak to peak ac voltage and dc voltage required of the 3rd order polynomial fit in [58].

When rectifying the $120 \text{ V}_{\text{rms}}$, 60 Hz ac voltage source, the measured converter power loss was 18.12 W for a conversion efficiency of 94.6% at an output voltage of 47.4 V and an output power of 402 W as reported by the Keysight PA2201A power analyzer. Fig. 3.16 provides a simulated loss breakdown conducted in PLECS. The simulation was conducted at $P_{\text{out}} = 420 \text{ W}$ and $V_{ac} = 120 \text{ V}_{\text{rms}}$. Transistor losses were estimated using the device models provided by EPC [61]. Given the hard-switched nature of the topology, the overlap and output capacitance losses of the high side transistors are significant at 20.7% of the total simulated loss. Since the converter operates at a relatively low duty cycle for much of the line cycle, the conduction losses for the high side transistors are low. To improve the converter efficiency, future designs should utilize switching cells with asymmetrical transistor die sizes (e.g., as was done in [62]). The performed simulation underestimates the experimentally measured converter losses as the simulation likely under-predicts the nonlinear inductor core

losses, transistor switching losses, and other high frequency effects.

Fig. 3.17 provides the measured transient response of the converter when the prototype was subjected to a load current step. For this experiment, the converter was connected to a 50 V_{rms} ac voltage source and a constant current electronic load. The electronic load was commanded to step from 4 A to 2 A while the converter attempted to maintain a constant output voltage of 20 V. Throughout the transient event, the flying capacitor voltages are well balanced as indicated by the peak transistor voltage stress $v_{\text{ds, stress}}$ which does not appreciably increase.

Finally, Fig. 3.18 shows the harmonics of the input current plotted against the IEC61000-3-2 Class A limit. All harmonics except for the 17th harmonic pass the harmonic limit. Although these limits are strictly only applicable for equipment operated above $v_{\text{ac}} = 230\text{ V}_{\text{rms}}$, the result provides further validation of the low harmonic distortion and high power factors able to be obtained by the buck-type PFC approach.

3.5 Chapter Remarks

This chapter presented a buck-type Power Factor Correction (PFC) ac-dc converter employing a six-level FCML converter. To achieve adequate flying capacitor voltage balancing, an active balancing control strategy is developed. After utilizing state space averaging to construct a model for the flying capacitor voltage and inductor current dynamics, a linear state feedback decoupling controller was designed and tested. It is confirmed through hardware validation that the flying capacitor voltages are able to track their ideal, balanced references sufficiently well and high power factor input current (> 0.969) is achieved.

Chapter 4

An Input Inductor Flying Capacitor Multilevel Converter Utilizing a Combined Power Factor Correcting and Active Voltage Balancing Control Technique for Buck-Type AC/DC Grid-Tied Applications

Portions of this chapter are adapted in part from [63].

One drawback inherent to many buck-type PFC approaches, including that of the previous chapter, is the relatively “noisy” input current drawn by the converter. The input current to the converter of the buck-type PFC of Chapter 3 is the current through the drain of the first high-side transistor $S_{H,5}$. At the peak of the line cycle where the duty cycle is lowest and output current is highest, this results in current being drawn with a very large crest ratio. Therefore, significant EMI filtering must be deployed upstream of the converter to mitigate differential mode emissions, degrading overall system efficiency and power density. This chapter addresses this drawback through a topological variant of the traditional FCML converter, termed the input inductor FCML converter, discussed in Section 4.1. Experimental verification of the proposed topology and control scheme is provided in Section 4.3.

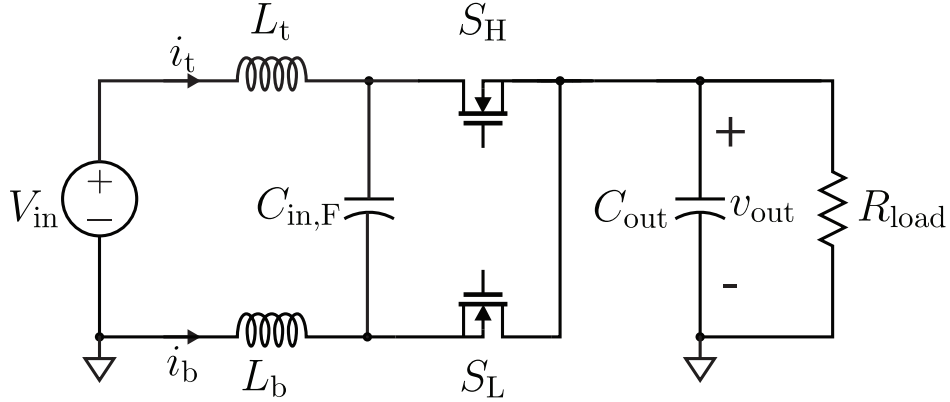
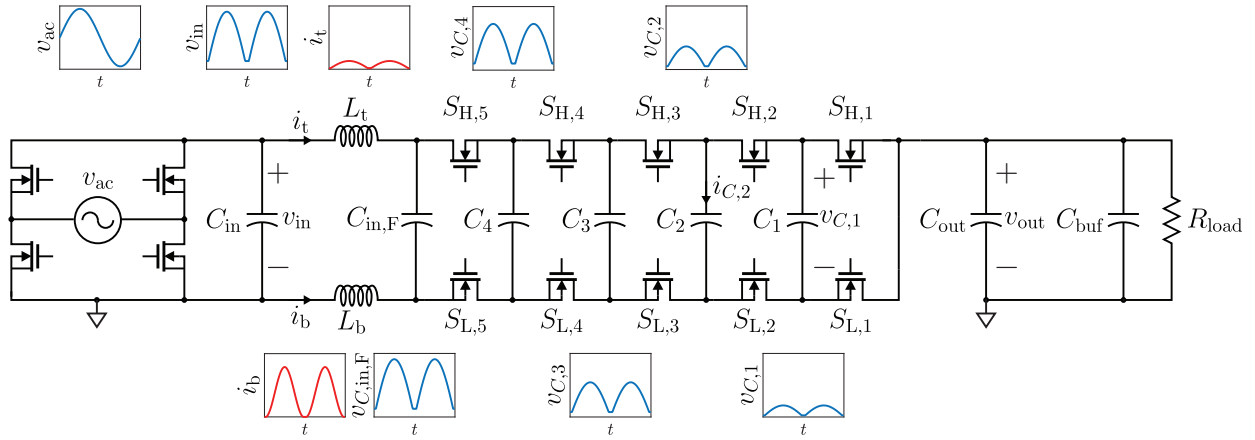


Figure 4.1: Circuit diagram of an input inductor buck dc-dc converter.

Figure 4.2: Circuit diagram of an ac/dc PFC rectifier utilizing a six-level input inductor FCML converter with an input synchronous rectifier. C_{out} serves to buffer switching frequency ripple while C_{buf} performs twice-line frequency power buffering.

4.1 Input Inductor Flying Capacitor Multilevel Converter

The input inductor FCML converter [64], [65], [66], [67] is a topological variation of the standard output inductor FCML converter. This converter topology belongs to a class of converters with “nonpulsating” port currents [64], enabling a reduction in required input current filtering. This topology was shown to be a promising candidate in buck-type PFC applications in [65]. A schematic drawing of an input inductor buck dc-dc converter is shown in Fig. 4.1 and a drawing of a six-level input inductor FCML rectifier is shown in Fig. 4.2. The converter maintains the same input-output voltage characteristic as an output inductor FCML converter with $V_{out} = DV_{in}$ where D is the duty cycle applied to all high-side switches S_H and $S_{H,k}$.

Compared to the output inductor FCML converter, the input inductor variant requires

significantly less input current filtering for the same peak magnetic energy storage, a useful proxy for inductor size [68]. This is a consequence of the topology's “nonpulsating” port currents property. First, we derive the total stored magnetic energy in both an output inductor buck converter and an input inductor buck converter. We assume the inductance of all inductors are chosen such that the inductor current ripple ratio $\alpha = \Delta i_L / I_L$ is the same, where Δi_L is the peak-to-peak current ripple and I_L is the average current in inductor L .

The peak energy E_{L_o} stored in the inductor L_o , which carries an average current I_{out} , for the output inductor buck converter can be derived as

$$\begin{aligned} E_{L_o} &= \frac{1}{2} L_o I_{\text{pk}}^2 = \frac{1}{2} L_o \left(I_{\text{out}} + \frac{\Delta i_{L_o}}{2} \right)^2 \\ &= \frac{1}{2} L_o I_{\text{out}}^2 \left(1 + \frac{\alpha}{2} \right)^2. \end{aligned} \quad (4.1)$$

The inductance L_o is then defined by the desired current ripple ratio α ,

$$L_o = \frac{D(V_{\text{in}} - V_{\text{out}})}{\alpha f_{\text{sw}} I_{\text{out}}} \quad (4.2)$$

yielding a peak inductor energy of

$$E_{L_o} = \frac{D(V_{\text{in}} - V_{\text{out}}) I_{\text{out}} (1 + \alpha/2)^2}{2\alpha f_{\text{sw}}} \quad (4.3)$$

The input inductor buck converter, shown schematically in Fig. 4.1, contains two inductors L_t and L_b . We derive the average inductor currents relative to the output current $I_{\text{out}} = V_{\text{out}} / R_{\text{load}}$ by performing a charge balance on $C_{\text{in,F}}$ in order to establish a comparison against the output inductor buck converter:

$$I_{C_{\text{in,F}}} = -DI_b + (1 - D)I_t = 0 \quad (4.4)$$

$$I_b = \frac{1 - D}{D} I_t \quad (4.5)$$

$$I_b + I_t = I_{\text{out}} \quad (4.6)$$

$$I_t = DI_{\text{out}}, \quad I_b = (1 - D)I_{\text{out}}. \quad (4.7)$$

The peak energy E_{L_t} stored in L_t is

$$\begin{aligned} E_{L_t} &= \frac{1}{2} L_t \left(I_t + \frac{\Delta i_{L_t}}{2} \right)^2 \\ &= \frac{1}{2} L_t \left(DI_{\text{out}} + \frac{\alpha DI_{\text{out}}}{2} \right)^2 \\ &= \frac{1}{2} L_t D^2 I_{\text{out}}^2 \left(1 + \frac{\alpha}{2} \right)^2 \end{aligned} \quad (4.8)$$

As in the output inductor buck converter, the inductances are defined by the desired current ripple ratios α :

$$L_t = \frac{D(V_{\text{in}} - V_{\text{out}})}{\alpha f_{\text{sw}} I_t} = \frac{(V_{\text{in}} - V_{\text{out}})}{\alpha f_{\text{sw}} I_{\text{out}}} \quad (4.9)$$

$$E_{L_t} = \frac{(V_{\text{in}} - V_{\text{out}}) D^2 I_{\text{out}} (1 + \alpha/2)^2}{2\alpha f_{\text{sw}}}. \quad (4.10)$$

The peak energy E_{L_b} stored in L_b is

$$\begin{aligned} E_{L_b} &= \frac{1}{2} L_b \left(I_b + \frac{\Delta i_{L_b}}{2} \right)^2 \\ E_{L_b} &= \frac{1}{2} L_b \left((1 - D) I_{\text{out}} + \frac{\alpha(1 - D) I_{\text{out}}}{2} \right)^2 \\ &= \frac{1}{2} L_b (1 - D)^2 I_{\text{out}}^2 (1 + \alpha/2)^2 \end{aligned} \quad (4.11)$$

$$L_b = \frac{D(V_{\text{in}} - V_{\text{out}})}{\alpha f_{\text{sw}} (1 - D) I_{\text{out}}} \quad (4.12)$$

$$E_{L_b} = \frac{D(V_{\text{in}} - V_{\text{out}}) (1 - D) I_{\text{out}} (1 + \alpha/2)^2}{2\alpha f_{\text{sw}}}. \quad (4.13)$$

Finally, the total peak magnetic energy is

$$E_{L_t} + E_{L_b} = \frac{D(V_{\text{in}} - V_{\text{out}}) I_{\text{out}} (1 + \alpha/2)^2}{2\alpha f_{\text{sw}}}, \quad (4.14)$$

which is identical to (4.3). Thus the total peak magnetic energy in an input inductor buck converter is the same as that of an output inductor buck converter under the constraint of equal current ripple ratio in all inductors.

The inductor in an output inductor N -level FCML converter is subjected to the same voltages as the two inductors in an N -level input inductor FCML converter. Additionally, the inductors carry the same average currents as the corresponding inductors in the buck converters. Thus the preceding analysis is directly applicable and the property of constant total peak magnetic energy across both the input and output inductor variants of the FCML converter holds.

Fig. 4.3 illustrates simulation waveforms of the input and flying capacitor voltages and both inductor currents of the input inductor FCML converter when at a dc/dc operating point corresponding to the peak of the line cycle when processing ≈ 800 W of output power (i.e., $V_{\text{in}} = 240\sqrt{2}$ V, $i_{L_t} + i_{L_b} = 2P_{\text{out}}/V_{\text{out}}$), for the case of non-negligible input and flying capacitor voltage ripple. The component values are provided in Table 4.2 and the switching frequency f_{sw} is 100 kHz.

The top inductor current i_{L_t} exhibits a relatively large ripple component at the switching frequency (as can be noticed by its periodicity at $T_{\text{sw}} = 10 \mu\text{s}$ rather than $T_{\text{sw}}/(N - 1) =$

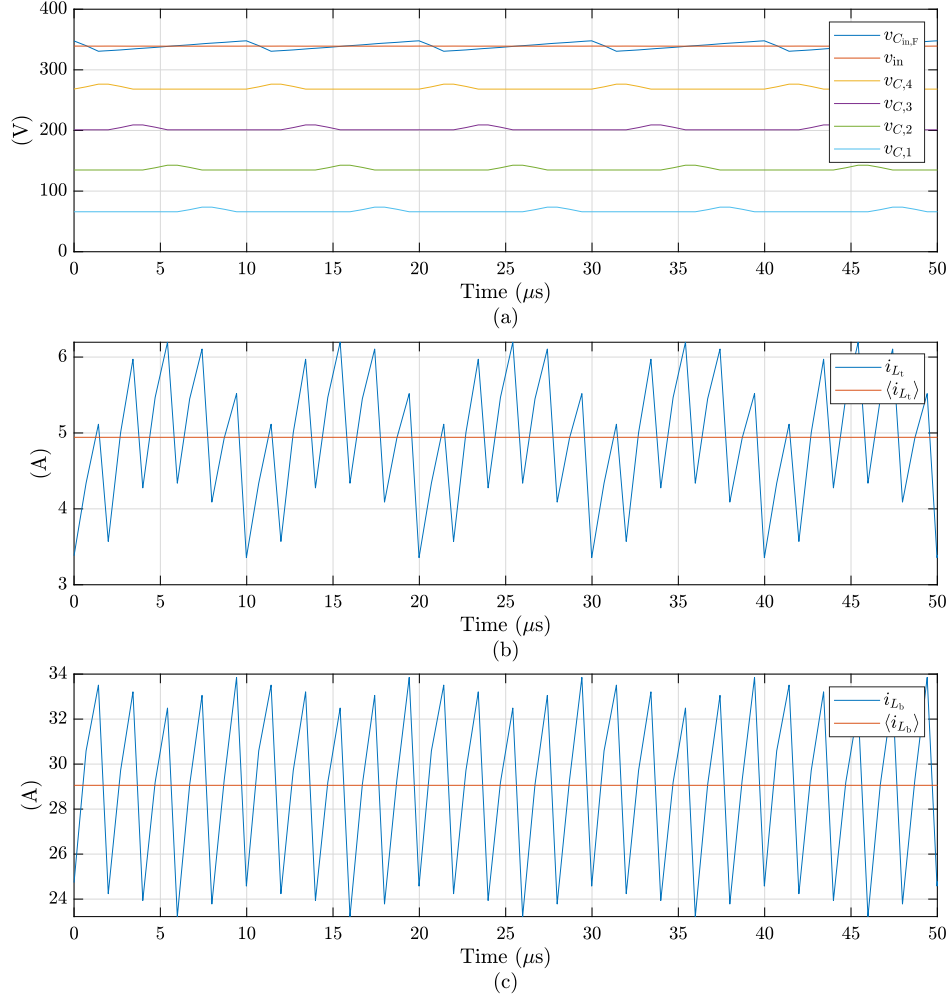


Figure 4.3: Simulated input inductor six-level FCML converter input and flying capacitor voltages and inductor currents when operating at a dc/dc operating point of $V_{in} = 240\sqrt{2}$ V, $V_{out} = 48$ V. (a) Input and flying capacitor voltages. (b) Top inductor current i_{L_t} and average top inductor current $\langle i_{L_t} \rangle$. (c) Bottom inductor current i_{L_b} and its average.

$0.2T_{sw} = 2 \mu s$.) Typically, when the flying capacitor voltages within an FCML converter are balanced, the inductor current ripple has even peaks and valleys and the lowest frequencies present in the inductor current waveform are dc and $(N - 1)f_{sw}$, a property leveraged by several current program modulated FCML converters [36], [38], [69]. However, when there is non-trivial input capacitor voltage ripple, the inductor current attains a harmonic component at f_{sw} since the input capacitor voltage has a ripple component at f_{sw} , a phenomenon investigated in [16]. The ratio of the peak-to-peak voltage to the average voltage of the input capacitor voltage in the simulation shown in Fig. 4.3 is 5%. Compared to FCML converters connected to a dc bus at the input, both the input inductor and output inductor buck-type PFC rectifiers are penalized with excessive input capacitance due to the reactive power

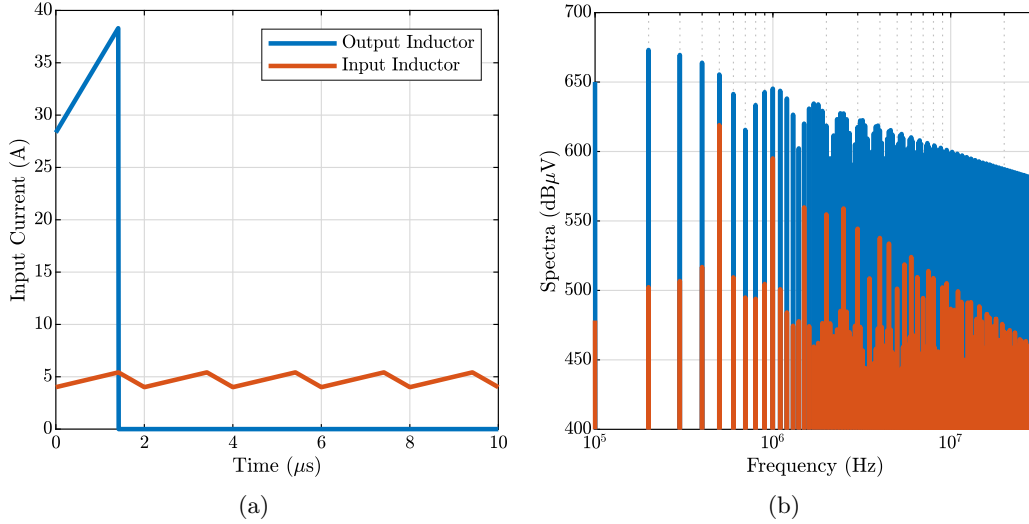
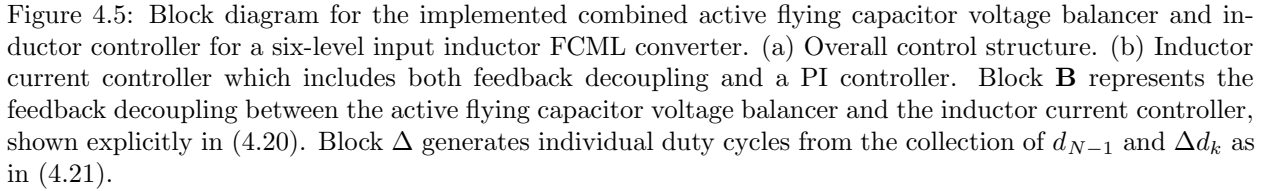


Figure 4.4: Simulation comparison of the input current waveform in (a) the time-domain and (b) spectra in the frequency-domain between an output inductor and input inductor FCML converter. Both converters employ a six-level FCML converter operating at the same dc-dc operating point of: $V_{in} = 339$ V, $V_{out} = 48$ V, $P_{out} = 1.6$ kW, $f_{sw} = 100$ kHz. The inductances of the three inductors were chosen such that the inductor current ripple ratio was 30%. The spectra voltage is the voltage that would be measured across a $50\ \Omega$ resistor conducting the input current (as would occur in a line impedance stabilization network). As noted in Section 4.1, the peak magnetic energy stored in the two converters is the same.

drawn by the input capacitor (as the input capacitor voltage follows a $|\sin(\omega t)|$ waveform). The reactive power drawn by the input capacitor increases the apparent power processed by the converter, reducing the converter efficiency. For a simulation with increased input capacitance and an input capacitor voltage ripple ratio of 0.5%, the top inductor ripple magnitude is reduced from 2.84 A peak-to-peak to 1.96 A peak-to-peak.

4.1.1 Input Current Comparison

Typically, the input current of PFC converters must adhere to conducted emissions standards (e.g., CISPR 32) and the input inductor variant offers a distinct advantage over the output inductor variant in this regard. To assess the filtering effort required, we define the input current as the current supplied by the grid assuming the grid behaves as a perfect voltage source (i.e., the current that flows through $S_{H,N-1}$ for the output inductor FCML converter and i_t for the input inductor FCML converter). Fig. 4.4 shows a comparison in the input current spectra between an input inductor and output inductor FCML converter. Both converters in this simulation study operate at the same input/output voltages, output power, and switching frequency. Since both inductors operate at the same ripple ratio, the total magnetic energy is the same. However, due to the “nonpulsating” continuous input current property of the input inductor FCML converter, the input current spectra are significantly reduced: up to 175 dBμV over the frequency range of 150 kHz–3 MHz. This reduction in



Finally, in comparison with the output inductor variant, the input inductor FCML converter reduces the effort required for power factor correction control. Since L_t is directly in series with the rectified input voltage source, control of i_t directly controls the input current. In comparison, for the output inductor FCML converter, controlling the output inductor current does not directly dictate the input current as $\langle i_{\text{in}} \rangle = D \langle i_L \rangle$ where $\langle x \rangle$ denotes the average value of x over a switching period and D is the duty cycle applied to the high-side switches. Additionally, the input and flying capacitors within the output inductor FCML converter present a reactive power draw to the grid [31]. To compensate this reactive power draw and maintain high power factor, the inductor current reference must be modified to be bipolar rather than strictly positive. This presents control challenges for the active flying capacitor voltage balancing controller as the inductor current crosses zero.

4.2 Controller Development

A significant challenge associated with using an FCML converter in a buck-type PFC application is the large-signal, time-varying input voltage. That is, the voltages on C_{in} and $C_{\text{in,F}}$ follow a rectified sinusoid value with a frequency of twice the mains frequency (e.g., 120 Hz). In order to utilize low voltage switches, the voltages on the flying capacitors within the converter must maintain a “balanced” distribution where $v_{C,k} = (kv_{\text{in}})/(N - 1)$ where k ranges from 1 to $N - 2$. If this flying capacitor voltage distribution is not maintained, excessive voltage stress will be applied to the switches, potentially resulting in converter failure. Typically, the FCML converter is operated with symmetric phase shifted-PWM (PS-PWM); in this scheme each high-side switch is modulated with the same duty cycle and switch gating signals are evenly phase shifted [1], yielding *passive balancing* of the flying capacitor voltages [20], [39]. The bandwidths of passive balancing are often insufficient to

allow the flying capacitors to track a twice-line-frequency reference as would be required in a buck-type PFC application [31].

4.2.1 Plant Model

Active flying capacitor voltage balancing changes the modulation scheme of the converter to achieve the desired flying capacitor voltage distribution. The derivation of this control law is similar to the derivations of [49], [70] and was shown to be effective in an output inductor FCML converter for buck-type PFC applications in [71]. We use state space averaging [51] to analyze the plant and make the simplifying approximation that $v_{C_{in,F}} \approx v_{C_{in}}$. First, we develop a model for the flying capacitor voltages assuming that the high-side switches $S_{H,k}$ are driven by switching signals q_k which have duty cycles d_k :

$$\begin{aligned}\langle i_{C,k} \rangle &= C_k \frac{d}{dt} \langle v_{C,k} \rangle = \langle (q_{k+1} - q_k)(i_t + i_b) \rangle \\ &\approx \langle q_{k+1} - q_k \rangle \langle i_t + i_b \rangle \\ &= (d_{k+1} - d_k)(I_t + I_b) \end{aligned} \tag{4.15}$$

$$= \Delta d_k (I_t + I_b), \tag{4.16}$$

where $I_t = \langle i_t \rangle$. Thus the flying capacitor voltages respond primarily to Δd_k , the differences in duty cycles of adjacent switch pairs. To develop a plant model for the top inductor current i_t , we analyze the voltage across L_t :

$$\langle v_{L_t} \rangle = \left\langle v_{C,in} q_{N-1} - v_{out} - \sum_{k=1}^{N-2} (q_{k+1} - q_k) v_{C,k} \right\rangle \tag{4.17}$$

$$L_t \frac{d}{dt} \langle i_t \rangle \approx \langle v_{C,in} \rangle d_{N-1} - \langle v_{out} \rangle - \sum_{k=1}^{N-2} \Delta d_k \langle v_{C,k} \rangle. \tag{4.18}$$

The inductor current thus primarily responds to a weighted sum of all of the duty cycles and the output voltage v_{out} . We can focus exclusively on the flying capacitor voltages $v_{C,k}$ and the top inductor current i_t as the control objectives are to regulate the input current and the flying capacitor voltages. The active flying capacitor voltage balancer can thus adjust Δd_k to control the flying capacitor voltages $v_{C,k}$ and the inductor current controller can adjust d_{N-1} to control the inductor current i_t . As in [71], feedback decoupling [49], [53] can be employed to remove the dependence of the inductor current on the output of the active flying capacitor voltage balancer Δd_k . Fig. 4.5 shows a control block diagram of the implemented control strategy.

Table 4.1: System Specifications

Parameter	Value
v_{ac}	208-240 V _{rms}
V_{dc}	48 V
$P_{out,max}$	820 W
f_{sw}	100 kHz

4.2.2 Controller Design

The duty cycle control law is thus given by:

$$\Delta d_k = \frac{\omega_C C_k}{i_{out}^*} = \frac{\omega_C C_k V_{out}}{i_t^* V_{in}} \quad (4.19)$$

$$d_{N-1} = \frac{1}{V_{in}} \left((i_{PI} - i_t) L_t \omega_L + v_{out} + \sum_{k=1}^{N-2} \Delta d_k v_{C,k} \right) \quad (4.20)$$

$$d_k = d_{k+1} - \Delta d_k, \quad k \in (1, N-2), \quad (4.21)$$

where i_{PI} is the output of the PI controller shown in Fig. 4.5(b). The following control parameters were chosen empirically: $\omega_L = 2\pi \cdot 2.78 \times 10^3$ rad/s, $\omega_C = 2\pi \cdot 477$ rad/s, $\gamma = 0.35$.

The output of the active balancer Δd_k is followed by a saturation block with symmetrical limits of $\pm 1\%$. Near the zero-crossing of the grid voltage, the slew rates of the flying capacitor voltages are largest and the inductor currents are smallest. These two properties result in large control actions from the active flying capacitor voltage balancer. By introducing a saturation block, the destabilizing effect of excessively large Δd_k can be avoided and minimal switch voltage stress maintained. Compared to [49], the inductor current controller uses measured flying capacitor voltages (rather than their quiescent values) when calculating the feedforward component of d_{N-1} (i.e., $\Delta d_k v_{C,k}$ rather than $\Delta d_k \cdot k V_{in} / (N-1)$ in (4.21)). This design choice resulted in improved current quality, particularly near the zero-crossings of the grid voltage. As in [71], by introducing scaling constant γ to the PI controller's proportional and integrator terms (cf. [49]), a larger phase margin and high-frequency gain are achieved. However, the system is no longer designed to be first-order, one of the objectives in [49].

4.3 Experimental Results

A hardware prototype, shown in the annotated photograph of Fig. 4.6, was developed to validate the proposed topology and control structure. The overall prototype volume is $222 \text{ mm} \times 127.5 \text{ mm} \times 8.13 \text{ mm}$. The volume of the power stage is $157 \text{ mm} \times 61 \text{ mm} \times 8.13 \text{ mm}$ resulting in a power stage volume of 77.86 cm^3 . Relevant system specifications are provided in Table 4.1 and component parameters are provided in Table 4.2. A second order

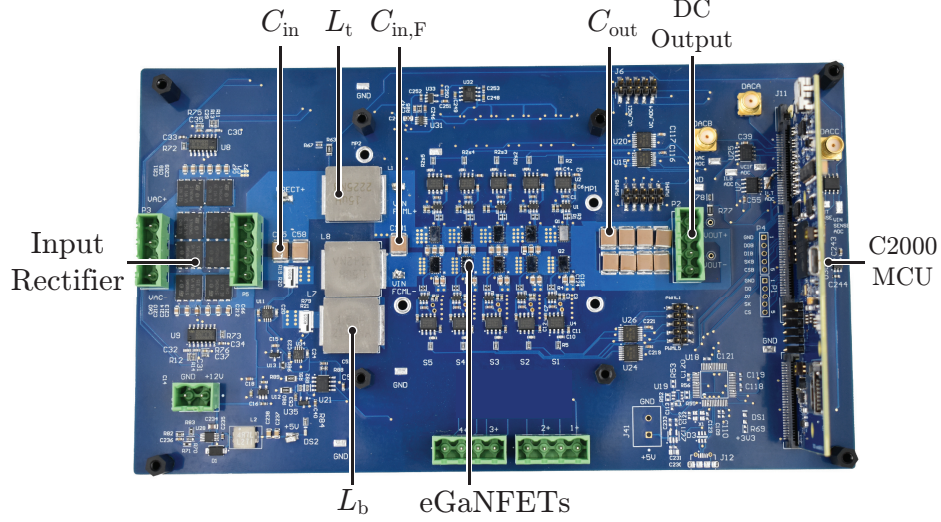


Figure 4.6: Photograph of the hardware prototype. A component list of the power stage is provided in Table 4.2. Prototype PCB dimensions: 222 mm $\times$ 127.5 mm.

Table 4.2: List of Main Components

Parameter	Value	Part Number
Power Semicond.	1.8 m Ω 100 V	EPC 2302
Rectifier Semicond.	61 m Ω 650 V	STL57N65M5
L_t	15 μ H	IHLP6767DZER150M11
L_b	3 μ H	IHLP6767DZER1R5M11*
C_{buf}	162 mF	380LX183M063A082
C_{in}	4.4 μ F	C5750X6S2W225K250KA
$C_{in,F}$	11 μ F	C5750X6S2W225K250KA
C_{out}	30.8 μ F	C5750X6S2W225K250KA
C_1	8.8 μ F	C5750X6S2W225K250KA
C_2	13.2 μ F	C5750X6S2W225K250KA
C_3	17.6 μ F	C5750X6S2W225K250KA
C_4	22 μ F	C5750X6S2W225K250KA

* L_b is composed of two 1.5 μ H inductors in series.

generalized integrator (SOGI) [55] was used to generate the reconstructed grid voltages for phase-locking. A discrete 10 μ H inductor was inserted in series with the ac power supply to emulate a realistic grid inductance.

As can be observed in Fig. 4.7, the flying capacitor voltages track the rectified sinusoidal

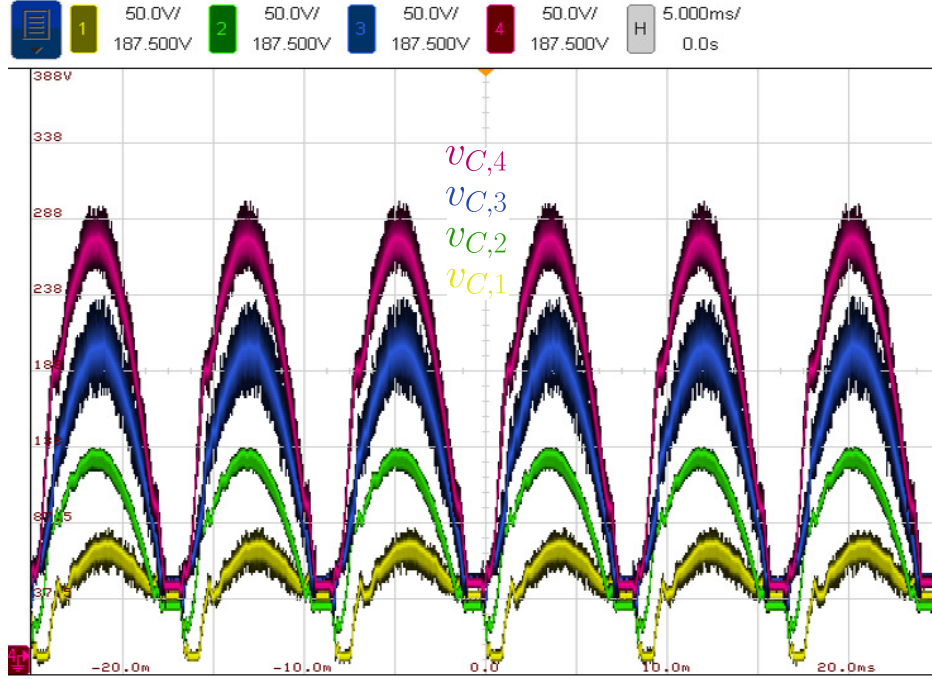


Figure 4.7: Measured flying capacitor voltages. The flying capacitor voltages are able to track their reference values sufficiently well to limit the peak switch voltage stress.

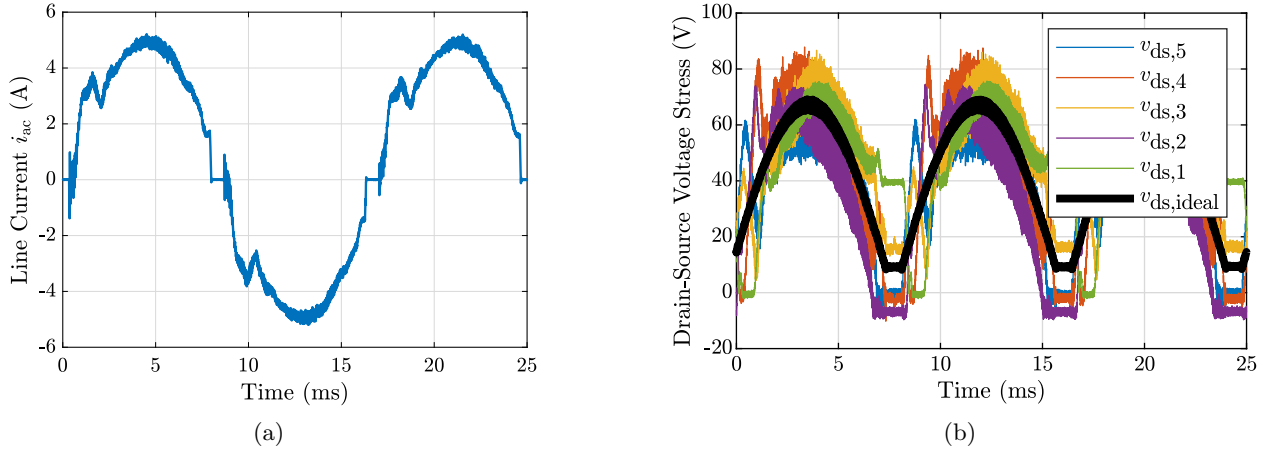


Figure 4.8: (a) Measured input current and (b) switch voltage stress when operating at $v_{ac} = 240 \text{ V}_{\text{rms}}$, $V_{\text{out}} = 48 \text{ V}$, and $P_{\text{out}} = 817 \text{ W}$. High fidelity control of the input current to achieve high power factor and sufficient flying capacitor voltage balancing to limit the peak switch voltage stress are the most pertinent goals of the controller. The input current achieves a power factor of 0.9898 as measured by a Keysight PA2201A power analyzer. Ideally, the peak switch drain-source voltage is $v_{\text{in}}/(N - 1)$ (plotted in black). This ideal voltage stress is achieved only when all flying capacitor voltages are at the balanced distribution. The peak switch voltage stress is 88.37 V.

reference, indicating low voltage stress on the switches. Fig. 4.8 shows the measured input current and switch voltage stress. The input inductor current i_t tracks its rectified sinusoid

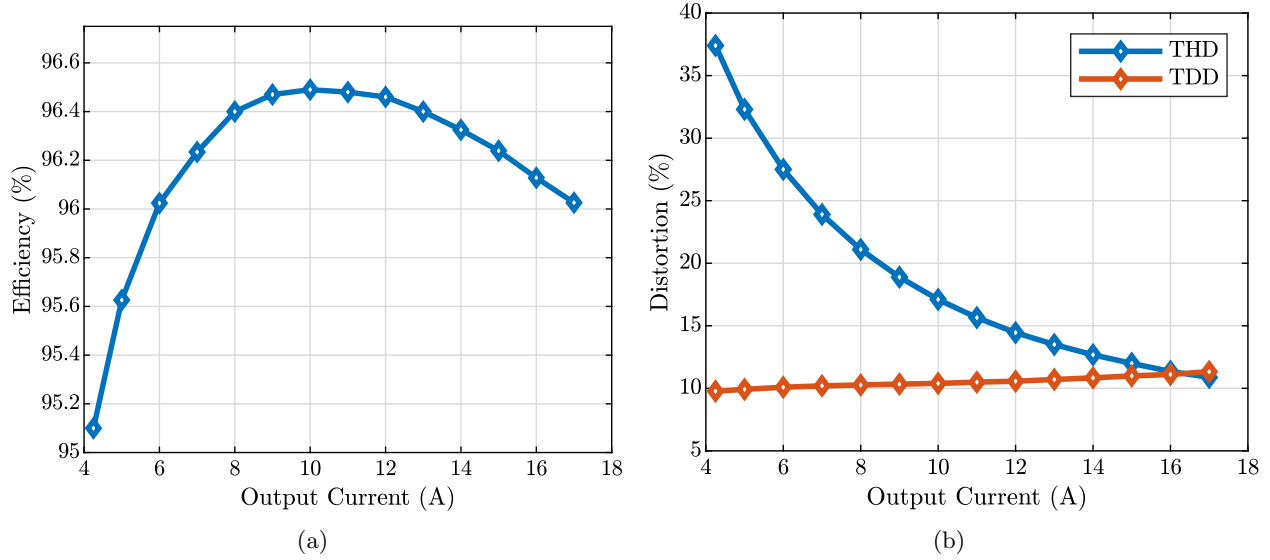


Figure 4.9: (a) Measured efficiency and (b) line current THD and TDD for the operating point $v_{ac} = 208 \text{ V}_{\text{rms}}$, $V_{\text{out}} = 48 \text{ V}$. The measured peak efficiency is 96.49% at $P_{\text{out}} = 480 \text{ W}$. The measured line current passes the IEC61000-3-2 Class A harmonic limits for all measured points.

reference, yielding high power factor and low THD input current. Additionally, as evidenced by Fig. 4.8(b), the active flying capacitor voltage balancing controller is able to maintain low switch voltage stress across the full ac cycle. Switch drain-source voltage stress is calculated as the differences in adjacent flying capacitor voltages for $v_{\text{ds},2,3,4}$. $v_{\text{ds},5} = v_{C,\text{in},F} - v_{C,5}$ and $v_{\text{ds},1} = v_{C,1}$. The peak switch voltage stress is 88.37 V.

At an input voltage of $208 \text{ V}_{\text{rms}}$, the converter achieves a full-power (820 W) efficiency of 95.64% at a power factor of 0.993 and current THD of 9.79% and a peak efficiency of 96.49% at an output power of 480 W. At an input voltage of $240 \text{ V}_{\text{rms}}$, the converter achieves a full-power efficiency of 95.72% at a power factor of 0.990 and current THD of 12.75% as measured by a Keysight PA2201A power analyzer. Fig. 4.9 shows the efficiency and line current distortion characteristic with respect to output current. Total demand distortion (TDD) is defined as $\text{TDD} = \text{THD} \cdot I_1 / I_D$, where THD is the total harmonic distortion, I_1 the fundamental current magnitude and I_D the rated fundamental current. From 25% power to full load, the TDD is below 12%. Across this power range, the measured line current harmonics stay well within the IEC61000-3-2 Class A limits.

4.4 Chapter Remarks

This chapter presented an input inductor FCML converter for a buck-type PFC rectifier utilizing an active flying capacitor voltage balancing controller. The input inductor topology reduces both the control and filtering effort required for achieving high quality mains current compared to an output inductor topology. To utilize the FCML converter in this application,

an active flying capacitor voltage balancing control scheme was developed which operates in tandem with the input current controller. The proposed topology and controller were validated on a hardware prototype resulting in a peak efficiency of 96.49% and a current THD of 9.79% at full load converting 208 V_{rms} to 48 V. Compared to a two-stage approach employing the step-up rectifier of [72] and the dc-dc converter of [73], the prototype power stage performance is double the power density (10.6 kW/L vs. 5 kW/L) and half the power loss (96.5% vs. 93.4% peak efficiency).

Chapter 5

FCML Converter-Based Single-Stage Buck-Boost Solar Micro-Inverter

The buck-type PFC rectifier utilizing the FCML converter has been shown in the Chapters 3 and 4 to enable efficient, power-dense rectifiers for grid-tied applications with dc voltages lower than the mains voltage. Another promising application area for this topology is that of solar micro-inverters. A solar micro-inverter directly processes energy from a solar photovoltaic (PV) panel to deliver power to the grid. Since solar panel voltages are typically much lower than the grid voltage (e.g., $V_{PV} = 20\text{ V} \sim 60\text{ V}$), a micro-inverter must both boost the panel voltage and invert it to deliver power to the grid [74]. Fig. 5.1 illustrates a high-level block diagram comparing a two-stage power conversion approach for implementing a solar micro-inverter with the proposed single-stage approach described in this chapter.

Compared to the buck-type PFC rectifier investigated in the previous chapters, there are several motivating factors to include a capability for the converter to process power when the magnitude of the grid voltage $|v_g(t)|$ is smaller than the PV panel voltage V_{PV} . The grid current quality requirements for renewable energy resources (regulated by standards such as IEEE 1547 [75]) are more stringent than those for other applications. The total rated current distortion (TRD), for example, must be less than 5% for power converters connected to renewable energy resources. Additionally, attempts to maximize the overall system efficiency may motivate configurations which operate with higher panel voltages (e.g., two solar modules connected in series), reducing the grid conduction angle and grid current quality if the converter must turn OFF when $|v_g(t)| < V_{PV}$.

By reversing the nominal power flow direction and adding a power conversion stage which operates when the grid voltage magnitude is smaller than the PV panel voltage, the buck-type PFC of Chapters 3 and 4 can be converted into a *buck-boost-type* inverter. A schematic drawing of the buck-boost inverter investigated in this chapter is provided in Fig. 5.2. The additional buck stage (composed of switches S_{Hb} and S_{Lb}) enables the inverter to continue to process power when the magnitude of grid voltage is lower than the panel voltage, enabling uninterrupted and higher quality grid current and power flow. Also shown is a two-stage differential-mode conducted EMI filter composed of L_f and C_f to achieve satisfactory grid

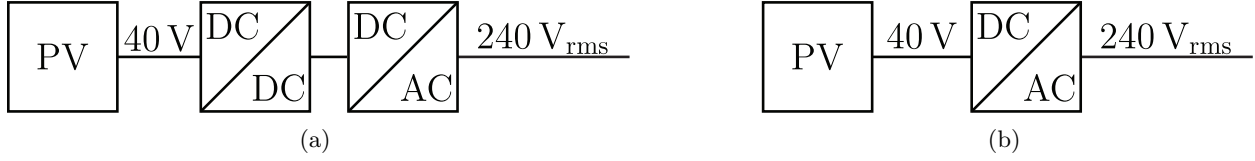


Figure 5.1: (a) Two-stage and (b) single-stage solar micro-inverter. The power converter must both boost and invert the low voltage solar panel voltage (labeled PV in the schematic, $20 \sim 60$ V) to the grid voltage. The two-stage approach boosts the panel voltage to a higher dc voltage (e.g., 400 V) then inverts the midpoint voltage with a buck-type dc/ac inverter. The single-stage micro-inverter boosts and inverts the panel voltage in a single power conversion stage. The trade-offs in power conversion architectures are very similar to the buck-type PFC considerations discussed in the previous chapters.

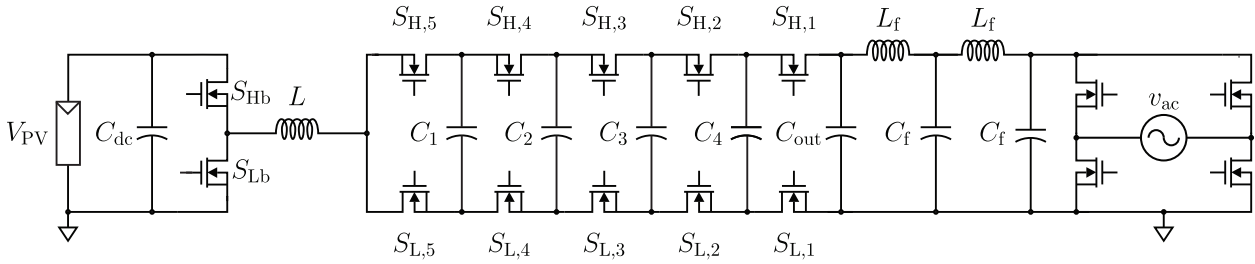


Figure 5.2: Single-stage photovoltaic micro-inverter utilizing a buck converter cascaded with a six-level FCML converter. A two-stage differential-mode EMI filter is located on the dc-side of the unfolded.

current quality.

5.1 Capacitive Reactive Power Consumption

Ideal micro-inverter operation requires that the the output, filter, and flying capacitor voltages track fractions of the (rectified) grid voltage. These capacitors will thus present a reactive power demand on the converter as the capacitors are charged and discharged over the line cycle. Compared to conventional micro-inverter topologies, the flying capacitors in the FCML converter add an additional reactive power load. This reactive power draw must be processed by the converter if the grid current is to attain unity power factor, increasing the apparent power processed by the converter and reducing the converter efficiency.

Fig. 5.3 provides a block diagram overview of the power flow within the micro-inverter system over a line cycle. The dc-bus capacitor C_{dc} must buffer both the twice-line frequency active power pulsations and the reactive power required to charge and discharge the output and flying capacitors present within the micro-inverter.

To illustrate the capacitor reactive power flow's impact on the converter, we derive the inductor current reference i_L^* required to deliver unity power factor power to the grid via an energy (or power) balance argument. The desired inductor current reference is derived by considering the required power drawn from the dc source P_{dc} . The dc source is composed of the parallel combination of the PV panel and buffering capacitance C_{dc} , supporting both active and reactive power flows. The desired dc source power is thus decomposed into a fully

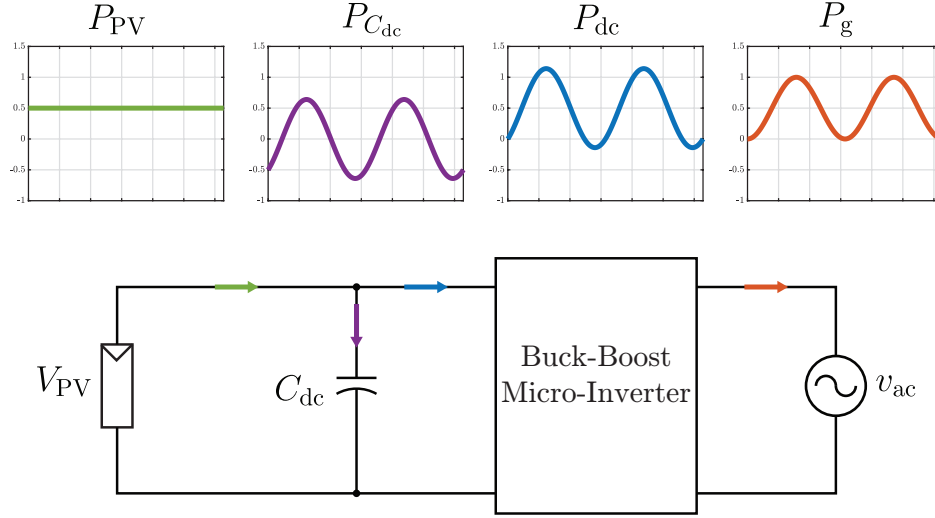


Figure 5.3: Block diagram illustrating the power flow within the single-stage solar micro-inverter over a single line cycle. The converter draws constant power P_{PV} from the photovoltaic panel and delivers unity power factor power to the grid P_g . The power processed by the buffer capacitor $P_{C_{dc}}$ includes both the twice-line frequency active power pulsations and the reactive power drawn by the output and flying capacitors within the micro-inverter.

active power component and a fully reactive power component

$$P_{dc}(t) = P_g(t) + Q(t), \quad (5.1)$$

where $P_g(t)$ is the time-varying active power drawn from the PV panel and buffer capacitor and delivered to the grid, and $Q(t)$ is the reactive power utilized to charge and discharge the flying and output capacitors. This reactive power component could be modified to support leading or lagging grid currents. To deliver active, unity power factor power to the grid, the active power reference $P_g(t)$ must satisfy

$$P_g(t) = 2P_{out} \sin^2(\omega t) = 2P_{out} \sin^2(\theta), \quad (5.2)$$

where P_{out} is the average power delivered to the grid and $\theta = \omega t$ is the grid angle.

Following a similar derivation as in [31], the charging and discharging of the flying and output capacitors over the line-cycle induces a reactive power flow $Q(t)$. To deliver unity power factor power to the grid, the dc port must supply this reactive energy. The desired voltages on the flying and output capacitors can be represented as

$$v_c(t) = |V_C \sin(\omega t)|, \quad (5.3)$$

where V_C is the peak of the grid voltage V_{pk} (e.g., $240\sqrt{2}$ V) for the output capacitors and fractions of the grid voltage for the flying capacitors. Utilizing the constitutive current-

voltage relationship for a capacitor, the power flow into the capacitors can be derived as

$$i_c(t) = C \frac{d}{dt} V_C |\sin(\omega t)| \quad (5.4)$$

$$= V_C C \omega \frac{\cos(\omega t) \sin(\omega t)}{2 |\sin(\omega t)|} \quad (5.5)$$

$$P_c(t) = v_c(t) i_c(t) \quad (5.6)$$

$$= V_C^2 C \omega \cos(\omega t) \sin(\omega t) = V_C^2 C \omega \cos(\theta) \sin(\theta). \quad (5.7)$$

This power flow is fully reactive and must exist regardless of the active energy drawn from the PV panel and delivered to the grid. The total capacitor reactive power draw $P_{C,\text{total}}$ is the sum of the individual capacitor reactive power flow quantities

$$Q(t) = P_{C,\text{total}}(t) = P_{C_{\text{out}}}(t) + P_{C_f}(t) + P_{C_{\text{fly}}}(t) \quad (5.8)$$

For the output and EMI filter capacitors where $V_C = V_{\text{pk}}$,

$$P_{C_{\text{out}}}(\theta) + P_{C_f}(\theta) = (C_{f,\text{tot}} + C_{\text{out}}) V_{\text{pk}}^2 \omega \cos(\theta) \sin(\theta). \quad (5.9)$$

For the flying capacitors, assuming all flying capacitors have the same capacitance C_{fly} , the reactive power flow can be generalized as

$$v_{C,i}(\theta) = \frac{i}{(N-1)} v_{C_{\text{out}}}(\theta) \quad (5.10)$$

$$P_{C_{\text{fly}}}(\theta) = C_{\text{fly}} \omega \cos(\theta) \sin(\theta) \frac{V_{\text{pk}}^2}{(N-1)^2} \sum_{i=1}^{N-2} i \quad (5.11)$$

$$\sum_{i=1}^{N-2} i^2 = \frac{(N-2)(N-1)(2N-3)}{6} \quad (5.12)$$

$$P_{C_{\text{fly}}}(\theta) = \omega \cos(\theta) \sin(\theta) V_{\text{pk}}^2 C_{\text{fly}} \frac{(N-2)(2N-3)}{6(N-1)}. \quad (5.13)$$

Thus the total reactive power draw can be summarized as

$$P_{C,\text{total}}(\theta) = V_{\text{pk}}^2 \omega \sin(\theta) \cos(\theta) \left(C_{f,\text{tot}} + C_{\text{out}} + C_{\text{fly}} \frac{(N-2)(2N-3)}{6(N-1)} \right) \quad (5.14)$$

$$P_{C,\text{total}}(\theta) = V_{\text{pk}}^2 \omega \sin(\theta) \cos(\theta) C_{\text{eff}}, \quad (5.15)$$

where C_{eff} is the sum of the output, EMI filter capacitance, and a ratio of the flying capacitance C_{fly} . Thus the total power drawn from the dc source as a function of the grid angle θ is

$$P_{\text{dc}}(\theta) = 2P_{\text{out}} \sin^2(\theta) + V_{\text{pk}}^2 \omega C_{\text{eff}} \sin(\theta) \cos(\theta). \quad (5.16)$$

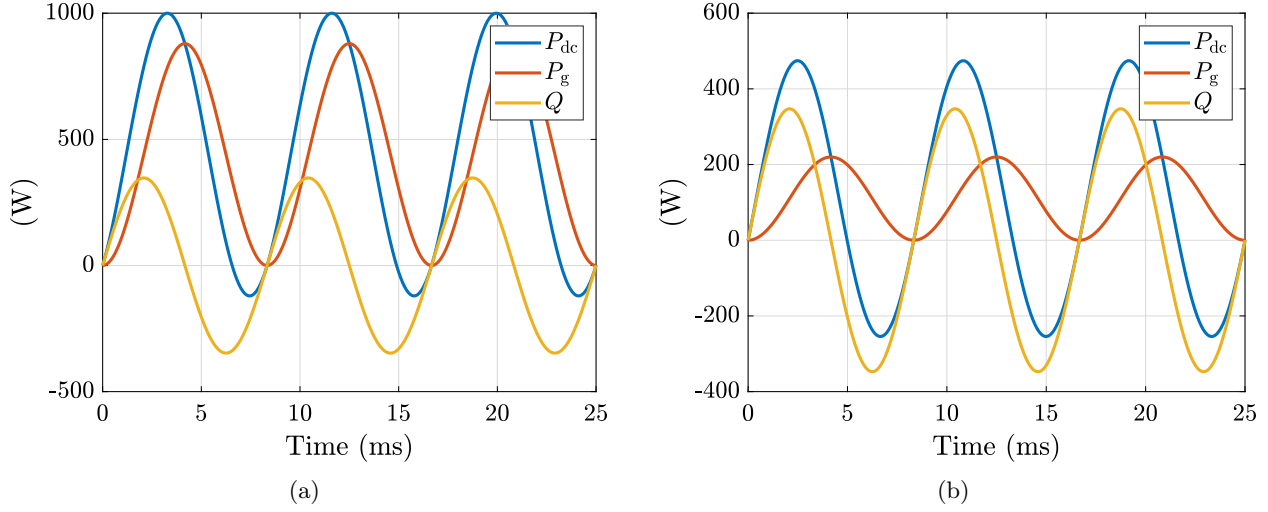


Figure 5.4: Power flow from the dc source decomposed into the unity power factor component delivered to the grid P_g and the reactive power component Q required to slew the flying and output capacitor voltages. The dc source power draw is the sum of the two power components $P_{dc} = P_g + Q$. (a) Average grid power $\langle P_g \rangle = 440$ W. (b) Average grid power $\langle P_g \rangle = 110$ W.

The desired power drawn from the dc source is visualized in Fig. 5.4 for two output power set points. At the lower power operating point in Fig. 5.4(b), the converter must process a significant reactive and thus apparent power despite delivering a quarter of the output power as in Fig. 5.4(a). This manifests as a non-trivial amount of current and losses being processed by the converter to support the charging and discharging of the output and flying capacitors.

5.2 Control Architecture

The modulation scheme explored in this work utilizes both the buck converter and the FCML converter switches operating with PWM continuously. Although this scheme incurs additional switching losses (as only the buck or the FCML switches need to be operated with PWM depending on the grid voltage), the controller operates on a continuously modulated plant with relatively minor discontinuous transitions.

5.2.1 Inductor Current Reference

For the control scheme proposed in this work, the desired power drawn from the dc bus $P_{dc}(t)$ determines the inductor current reference i_L^* . This desired power flow may be determined for example by a higher level controller such as maximum power point tracking algorithm. The current drawn from the dc source is a product of the high-side duty cycle of the buck

converter and the inductor current

$$P_{dc}(t) = V_{dc}i_{dc} = V_{PV}d(t)i_L^*(t). \quad (5.17)$$

Given the grid voltage $v_g(t)$, the duty cycle for the buck converter is

$$d(t) = \frac{|v_g(t)|}{V_{PV} + |v_g(t)|}, \quad (5.18)$$

resulting in an inductor current reference which depends on the desired active and reactive power as

$$i_L^*(t) = \frac{V_{PV} + |v_g(t)|}{V_{PV}|v_g(t)|}(P_g(t) + Q(t)). \quad (5.19)$$

Substituting the previously derived relationship for the active and reactive power

$$P_g(\theta) = 2P_{out} \sin^2(\theta), \quad Q(\theta) = \omega C_{eff} V_{pk}^2 \cos(\theta) \sin(\theta) \quad (5.20)$$

$$i_L^*(\theta) = \left(\frac{V_{PV} + V_{pk} |\sin(\theta)|}{V_{PV} V_{pk} |\sin(\theta)|} \right) (2P_{out} \sin^2(\theta) + \omega C_{eff} V_{pk}^2 \cos(\theta) \sin(\theta)). \quad (5.21)$$

Finally, this yields the desired inductor current reference

$$i_L^* = (V_{PV} + V_{pk} |\sin(\theta)|) \left(\frac{2P_{out}}{V_{PV} V_{pk}} |\sin(\theta)| + \frac{\omega C_{eff} V_{pk}}{V_{PV}} \cos(\theta) \text{sgn}(\sin(\theta)) \right). \quad (5.22)$$

Fig. 5.5 shows the inductor current reference i_L^* for two separate average grid output powers of 440 W and 110 W. The shape of the waveform is a consequence both of the active and reactive power flowing through the converter and the duty cycle of the buck converter evolving over the line cycle. The rms current $i_{L,rms}^*$ is 12.04 A for the 440 W operating point and 6.01 A for the 110 W operating point. Consider the inductor current reference with zero reactive current processed to understand the impact of the reactive power flow. Setting $Q(\theta) = 0$, yields $i_{L,rms}^* = 10.77$ A for the 440 W operating point and $i_{L,rms}^* = 2.69$ A for the 110 W operating point. At the higher power setpoint, the reactive current increases the rms current by just over 10% while at the lower operating point, the inductor current rms value is increased by over a factor of 2.2 $\times$, significantly degrading the low power efficiency of the converter.

5.2.2 Inductor Current Controller

The inductor current controller is derived by analyzing the buck-boost converter and an alternative controller structure to decouple the influence of the active flying capacitor voltage balancer is derived. For simplicity we derive the controller for a four-level FCML boost bridge leg. The (switched) inductor voltage $v_L(t)$ is the difference of the input half-bridge buck and FCML boost bridges

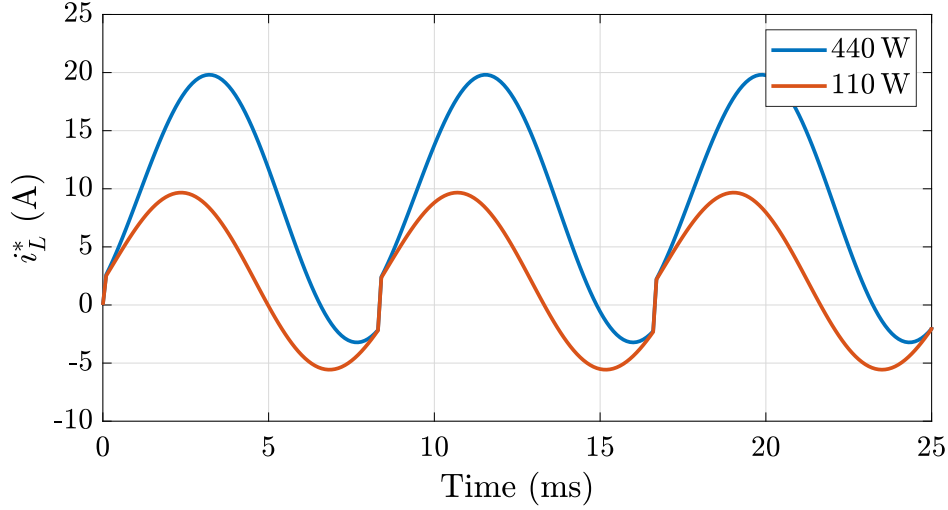


Figure 5.5: Inductor current reference i_L^* for an average grid power of 440 W and 110 W. Significant reactive power must be processed by the converter to charge and discharge the flying and output capacitors, incurring conduction and switching loss penalties as output power is decreased.

$$v_L(t) = v_{\text{buck}}(t) - v_{\text{FCML}}(t).$$

The buck bridge imposes $v_{\text{buck}}(t) = q_b(t)V_{\text{in}}$ where $q_b(t)$ is the gating signal of the high-side transistor in the buck bridge. The FCML bridge imposes

$$v_{\text{FCML}}(t) = (q_1(t) - q_2(t))v_{C,1}(t) + (q_2(t) - q_3(t))v_{C,2}(t) + v_{\text{out}}q_3(t),$$

where $q_i(t)$ are the gating signals of the high-side transistors within the FCML bridge.

After applying the averaging operator $\langle x \rangle$ and the small-ripple approximation ($\langle xy \rangle \approx \langle x \rangle \langle y \rangle$), the average FCML bridge voltage is

$$\langle v_{\text{FCML}} \rangle(t) \approx d_1(t)v_{C,1}(t) + (v_{C,2}(t) - v_{C,1}(t))d_2 + (v_{\text{out}} - v_{C,2}(t))d_3(t),$$

where $d_i(t)$ are the duty cycles of the high side switches. To obtain an linear, time-invariant (LTI) description of the inductor current, we linearize the expression for the inductor voltage and ignore the output voltage perturbation with

$$d_i = D + \tilde{d}_i, \quad v_{C,i} = \frac{iV_{\text{out}}}{3} + \tilde{v}_{C,i} \quad (5.23)$$

$$\langle v_{\text{FCML}} \rangle = V_{C,1}\tilde{d}_1 + (V_{C,2} - V_{C,1})\tilde{d}_2 + (V_{\text{out}} - V_{C,2})\tilde{d}_3 + D\tilde{v}_{C,1} + D(\tilde{v}_{C,2} - \tilde{v}_{C,1}) + D(-\tilde{v}_{C,2}). \quad (5.24)$$

Substituting the quiescent values for the flying capacitor voltages and recognizing that the small-signal contributions of the flying capacitor voltages on the inductor voltage are zero

yields

$$\langle v_{\text{FCML}} \rangle(t) = \frac{\tilde{d}_3 + \tilde{d}_2 + \tilde{d}_1}{3} = d_{\text{cm,HS}} V_{\text{out}}. \quad (5.25)$$

The inductor current controller can thus command the *common-mode* duty cycle of the FCML converter high side switches $d_{\text{cm,HS}}$ and naturally reject the disturbance of the active flying capacitor voltage balancer, resulting in the following linearized description of the inductor current

$$\langle \tilde{v}_L \rangle(t) = d_{\text{buck}} V_{\text{in}} - V_{\text{out}} d_{\text{cm,HS}}. \quad (5.26)$$

Assuming the buck bridge is driven with the same duty cycle as the low side transistors in the FCML bridge $d_{\text{cm}} = -d_{\text{cm,HS}}$ results in

$$\langle \tilde{v}_L \rangle(t) = (V_{\text{in}} + V_{\text{out}}) d_{\text{cm}} = L \frac{d\tilde{i}_L}{dt}. \quad (5.27)$$

This structure is an alternative way to mitigate the impact of the active flying capacitor voltage balancing controllers on the inductor current control compared to Chapters 3 and 4. That is, rather than choosing d_{N-1} as the “control handle” for the inductor current, the common mode duty cycle $d_{\text{cm,HS}}$ can be chosen.

The flying capacitor voltages respond in the same fashion as the output inductor and input inductor buck-type PFC models. The capacitor voltage change is determined by

$$v_{C,i} = (q_{L,i+1} - q_{L,i}) i_L \quad (5.28)$$

$$C_i \frac{d}{dt} v_{C,i} \approx (d_{L,i+1} - d_{L,i}) I_L = \Delta d_{L,i} I_L, \quad (5.29)$$

where $d_{L,i}$ are the duty cycles of the low-side switches within the FCML bridge. The same proportional controller demonstrated in Chapters 3 and 4 where flying capacitor voltage errors result in differential duty cycles Δd adequately controls the flying capacitor voltages.

The common-mode duty cycle d_{cm} can be decomposed into a feed-forward portion and a feedback portion. The former is derived from the steady-state operating point of a non-inverting buck-boost converter where

$$\langle V_L \rangle = D V_{\text{in}} + (1 - D)(-V_{\text{out}}) = 0 \quad (5.30)$$

$$V_{\text{out}} = D(V_{\text{in}} + V_{\text{out}}) \quad (5.31)$$

$$D = \frac{V_{\text{out}}}{V_{\text{in}} + V_{\text{out}}}. \quad (5.32)$$

The feedback portion u is generated from a PI controller where

$$u = K_p i_{L,\text{error}} + K_i i_{L,\text{error,sum}}$$

The proportional gain K_p is chosen to achieve a desired inductor current loop crossover frequency ω_c . Given the controller structure, $K_p = \omega_c$. The integral gain K_i is chosen to provide low frequency loop gain without degrading the phase margin significantly [76]. The zero of the PI controller is chosen to occur at one fifth of the crossover frequency, resulting in $K_i = \omega_c^2/5$. This results in a common mode duty cycle command of

$$d_{\text{cm}} = \frac{v_{\text{out}} + Lu}{V_{\text{PV}} + v_{\text{out}}}.$$

Finally, the inductor current controller output d_{cm} and flying capacitor voltage controller outputs Δd_i must be translated into duty cycle commands for the individual switch pairs. The high-side switch in the buck converter will be commanded with duty cycle d_{cm} . The matrix transformation to derive the FCML duty cycle commands can be derived by first defining the relationship between d_{cm} and Δd_i as

$$\begin{bmatrix} d_{\text{cm}} \\ \Delta d_1 \\ \Delta d_2 \end{bmatrix} = \begin{bmatrix} 1/3 & 1/3 & 1/3 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix}. \quad (5.33)$$

The inverse of this similarity transform yields the desired mapping

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} 1 & -2/3 & -1/3 \\ 1 & 1/3 & -1/3 \\ 1 & 1/3 & 2/3 \end{bmatrix} \begin{bmatrix} d_{\text{cm}} \\ \Delta d_1 \\ \Delta d_2 \end{bmatrix}. \quad (5.34)$$

This matrix operation to generate the duty cycle references can be somewhat computationally expensive, especially for higher level count converters.

5.3 Simulation Results

A simulation in PLECS was performed to evaluate the proposed topology and control structure of the non-inverting buck-boost FCML micro-inverter. The operating and converter parameters are provided in Table 5.1. It is interesting to note the asymmetry in the switching frequencies of the FCML bridge and the buck converter bridge. The controller (derived from an averaged model of the converter) does not constrain a switching frequency relationship between the two bridges, however further considerations (e.g., EMI filtering, inductor current ripple) may further constrain switching frequency selection.

The crossover frequency for the inductor current loop was chosen to be 5 kHz, resulting in a proportional gain $K_p = \omega_c = (2\pi)5 \times 10^3$ rad/s. and an integral gain $K_i = \omega_c^2/5$. The proportional gain of the flying capacitor voltage controllers were all chosen to be $K_{p,\text{Cfly}} = (2\pi)2 \times 10^3$. The flying capacitor voltage controller outputs saturated to a maximum $\Delta d_{\text{sat}} = \pm 10\%$.

Fig. 5.6 presents the flying and output capacitor voltages along with the inductor current and its reference tracking capabilities. During the displayed time frame, the converter goes

Table 5.1: Non-Inverting Buck Boost Operating and Converter Parameters

Parameter	Value
V_{panel}	60 V
V_{ac}	240 V _{rms}
$f_{\text{sw,FCML}}$	75 kHz
$f_{\text{sw,Buck}}$	125 kHz
L	45 μH
C_{fly}	1.3 μF
C_{out}	5 μF
L_{f}	10 μH
C_{f}	2.5 μF

from processing a average output power of 440 W to processing an average output power of 110 W. At the lower power operating point, the inductor current reference undergoes a zero-crossing when there is still significant grid voltage. When there is zero reactive power compensation (i.e., only active power is drawn from the dc source), the inductor current zero-crossing occurs coincidentally with the zero-crossing of the grid voltage. The active flying capacitor voltage balancing controller becomes slightly unstable near the zero-crossing of the inductor current as the impact of inductor current ripple begins to dominate the impact of the average inductor current, as discussed in [50].

Fig. 5.7 illustrates the switch node voltages of both the buck and FCML bridges; the difference between these two voltages is applied across the buck-boost inductor. The inductor current ripple deviates significantly from the traditionally observed triangular current ripple due to the flying capacitor voltage ripple, a phenomenon investigated in [77].

Fig. 5.8 provides the switch voltage stress for the switches within the FCML bridge leg across several line cycles. During the displayed time frame, the converter output power reference is stepped from 440 W to 110 W. Due to the decreased output power and decreased inductor current, the flying capacitor voltage ripple and switch voltage stress both decrease after the output power is stepped down.

Fig. 5.9 shows the power drawn from the dc source and delivered to the grid across several line cycles and an output power reference step. Via control of just the buck-boost inductor current, the output grid current and power is relatively well regulated to track a $\sin$ and $\sin^2$ waveform respectively. The “notch” in the grid power at the lower power operating point occur when the inductor current crosses zero, destabilizing the active flying capacitor voltage balancer.

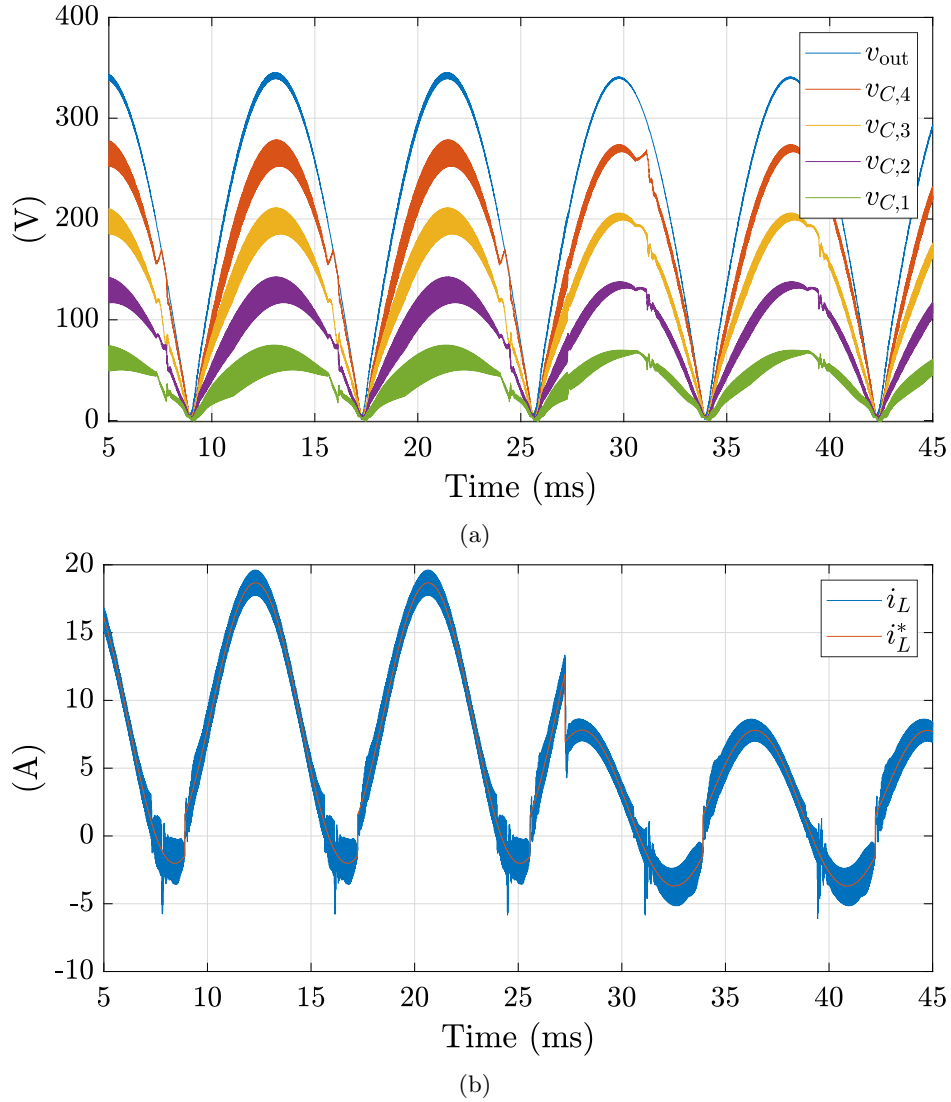


Figure 5.6: Simulation results of the non-inverting FCML-based buck-boost solar micro-inverter. The converter's average output power reference is stepped from 440 W to 110 W.

5.4 Chapter Remarks

This chapter presented an application extension to the buck-type PFC rectifiers investigated in previous chapters, a single-stage buck-boost micro-inverter for solar module-level power electronics. The controller for this application especially focused on the reactive power flow induced by the flying and output capacitors. The continuously modulated buck-boost converter analyzed is able to achieve fully active power delivered to the grid by deriving a feed-forward inductor current reference.

There are several open areas of investigation for practical hardware realization of this work. First, the unfold which converts the $|v_{ac}|$ output of the converter to the bipolar

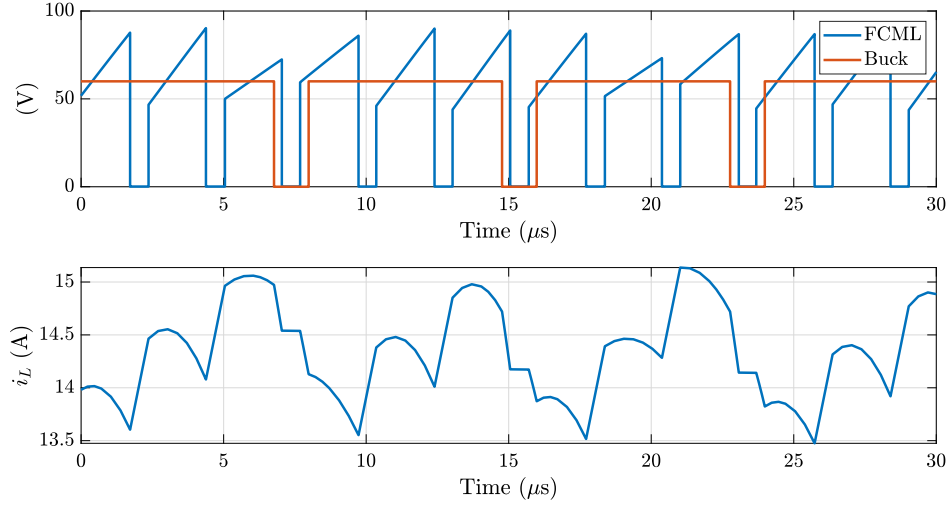


Figure 5.7: Simulated buck bridge switch node voltage v_{buck} and FCML bridge switch node voltage v_{FCML} and inductor current i_L . At this operating point, the converter is processing 440 W near the peak of the line cycle.

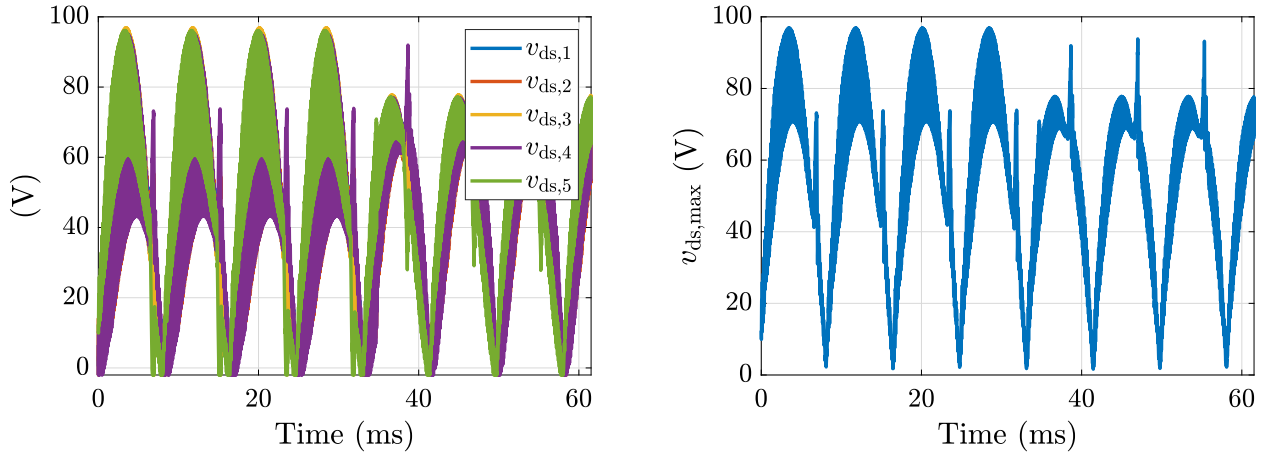


Figure 5.8: (a) FCML bridge switch v_{ds} stress across several line cycles. (b) The maximum FCML bridge switch v_{ds} stress. Partway through this simulation, the converter average output power is reduced, reducing the flying capacitor voltage ripple and switch voltage stress.

grid voltage. For unity power factor PFC converters, an unfolded is often a fine circuit choice, however when inverting into non unity power factor loads as a micro-inverter may be required to do, control of the unfolded circuit presents difficulty. Work in [78], [79] utilized PWM of the unfolded transistors to assist in the grid zero-crossing, however evaluating and implementing such a control scheme must still be done.

The twice-line frequency active power delivered to the grid and the reactive power drawn by the flying and output capacitors are buffered at the low voltage, photovoltaic node. This is problematic as electrolytic capacitors at this voltage rating have significantly lower energy densities and energy buffering capabilities compared to higher voltage capacitors [7],

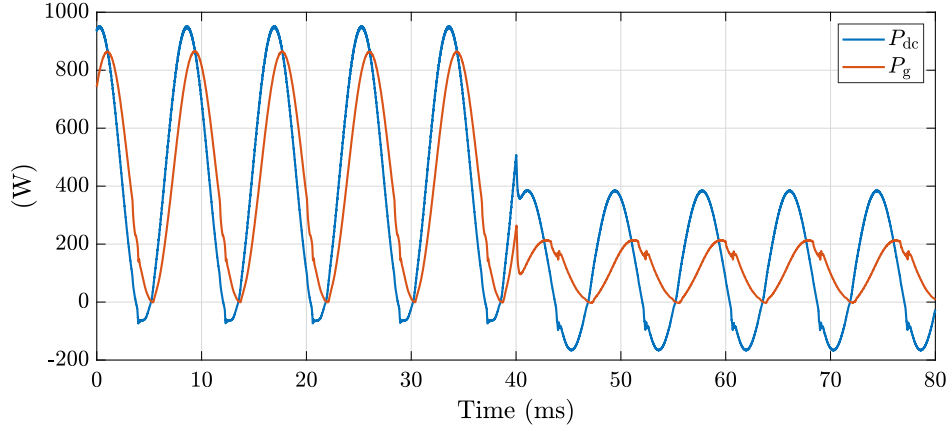


Figure 5.9: Power drawn from dc bus P_{dc} and power delivered to the grid P_g . The derived reactive power compensation is able to ensure that active, twice-line-frequency varying power is delivered to the grid. To achieve this power flow, the dc source must process significant reactive power to charge and discharge the flying and output capacitors within the converter.

[80]. Alternative converter structures which buffer the twice-line frequency active power and reactive power drawn by the flying and output capacitors may be necessary to achieve high system efficiency and density.

Finally, alternative topologies and modulation schemes could be considered to implement the FCML-based buck-boost micro-inverter. Rather than continuously switching both the buck and FCML bridges, an alternative modulation scheme could consider operating only one of the two bridges with PWM at a time. This approach would likely improve conversion efficiency through a reduction in switching losses and inductor current, however the controller would have to contend with discontinuous modulation as the converter transitions from one switching scheme to another.

Chapter 6

Design and Implementation of a Three-Phase Eight-Level Flying Capacitor Multilevel Rectifier for Future Data Center Power Delivery

Portions of this chapter are adapted in part or in whole from [81].

6.1 Introduction

Global capacity for AI-focused data centers are expected to rise at an annual rate of 20%, nearly quadrupling by the end of the decade [82]. Increased site power demand and rising thermal design powers of modern CPU/GPU/xPUs [83] are motivating the design of racks which consume significantly more power, with current designs surpassing 100 kW [84], and 1 MW racks being proposed [85], [86]. This is forcing a departure from traditional 48 V rack power delivery utilizing single-phase rectifiers [87], as cabling losses and weight would be excessive. To improve the site efficiency and increase rack power levels, future data centers are expected to use 800 V as the rack distribution voltage [85], [86], [88]. At these voltage levels, the common 650 V power semiconductor (Si or GaN) cannot be used in conventional topologies, necessitating alternative approaches to achieve high efficiency and small size. One such topology that has demonstrated superior performance is the flying capacitor multi-level (FCML) converter [1]. In this work, we propose the use of a high-level count, eight-level FCML converter design, and overcome practical and industry-relevant challenges. Specifically, the design presented in this work emphasizes EMI filter design, advanced three-phase modulation schemes for the FCML converter, and high efficiency gate drive power delivery.

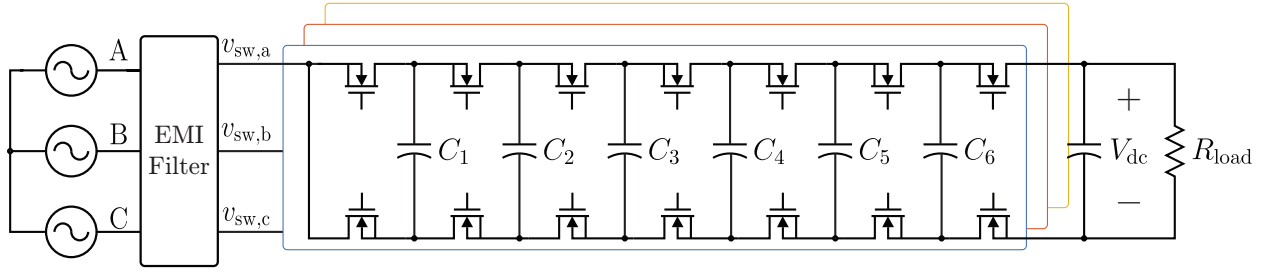


Figure 6.1: Three-phase eight-level FCML ac/dc converter schematic. The FCML converter enables the utilization of low voltage semiconductors and reduced magnetic stress to achieve the efficiency and power density goals of next generation data center power delivery. The implemented EMI filter is illustrated in Fig. 6.3(a).

6.2 Three-Phase Flying Capacitor Multilevel Rectifier

This work focuses on the design, optimization, and practical realization of a three-phase FCML rectifier aimed at the power level, efficiency, and power density required for future data center power delivery architectures. Fig. 3.2 shows a schematic drawing of the designed three-phase, eight-level FCML rectifier. Compared to previous high-performance single-phase prototypes [3], [89], this work leverages the inductor current ripple reduction properties of three-phase systems. Although three single-phase inverters could be combined to form a valid three-phase inverter/rectifier (as was done in [90], [91]), the ac-side filter inductors must store increased energy as this architecture does not effectively leverage the common-mode voltage of three-phase systems.

6.2.1 Modulation Considerations

Center-aligned PWM is a powerful technique to reduce inductor energy storage requirements in three-phase converters (e.g., motor drive inverters [92]). This modulation scheme results in the center of all three switch node voltage pulses occurring at the same time. Center-aligned PWM synthesizes a neutral point voltage which enables an effective doubling in the inductor current ripple frequency compared to the switching frequency. One common implementation to achieve center-aligned PWM utilizes triangle PWM carriers with the carriers aligned in time.

In an FCML converter, the time at which the center of the switch node voltage pulse occurs varies with duty cycle with respect to the PWM carriers. To achieve center-aligned v_{sw} pulses throughout the entire line cycle, the phase shifts of the PS-PWM carriers of phase B and phase C relative to phase A cannot be constant and must vary with the duty cycle [93], [94]. To achieve the switch node voltage alignment, two sets of PS-PWM carriers are used for the phase B and C FCML converters. The first set of carriers is fully aligned with those of phase A while the second set is phase shifted by $2\pi/(2(N-1))$ rad. The second set of carriers for phase B is utilized if its duty cycle region is different from that of phase A. The duty cycle regions are calculated according to the procedure outlined in [94]. The

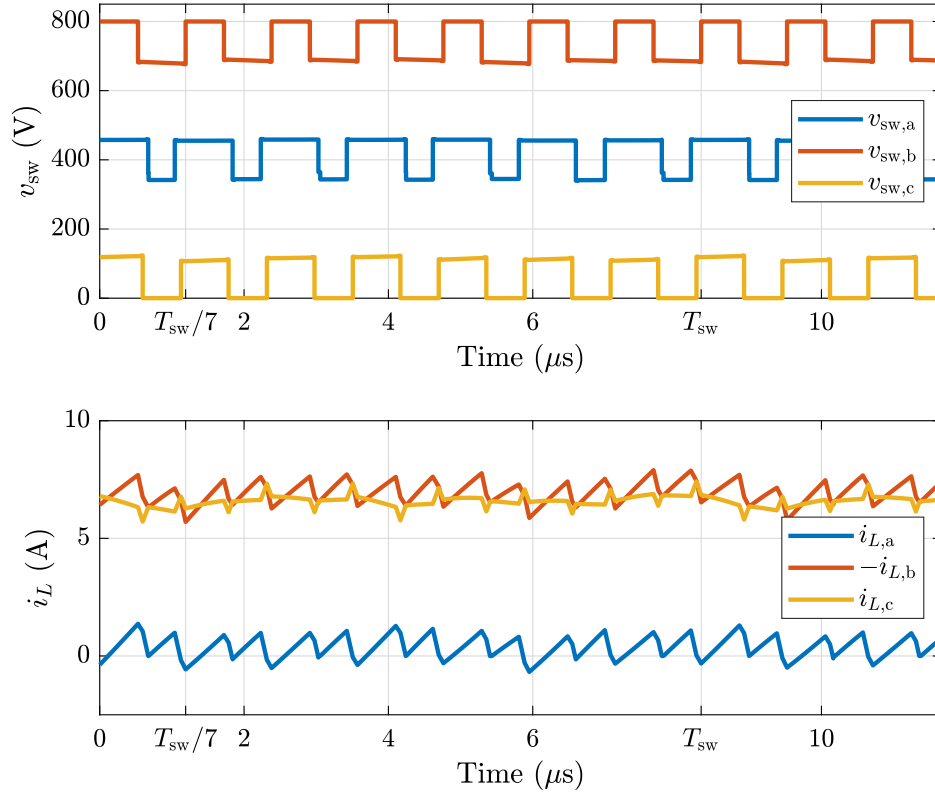


Figure 6.2: Simulated switch node voltages v_{sw} and inductor currents i_L . The v_{sw} pulses are center-aligned and the inductor currents i_L have a ripple component at $2(N-1)f_{sw}$. The converter supplied $5.5 \text{ A}_{\text{rms}}$ to a 50Ω wye-connected resistive load from an 800 V dc source.

same process is used for determining which sets of carriers to use for phase C. Fig. 6.2 shows simulated switch node voltages v_{sw} and inductor currents i_L for the eight-level FCML rectifier investigated in this work. As can be seen, the switch node pulses are center-aligned and the inductor ripple frequency is increased, most clearly seen in $i_{L,a}$.

Space vector modulation (SVM) [95] is widely used for both increasing the synthesizable ac voltage amplitude (i.e., extending the linear modulation range), reducing the line current distortion, and reducing the inductor current ripple. This increase in modulation depth is enabled by a decrease in the deviation in duty cycle from 50% by injecting appropriate zero voltage vectors [92]. In an FCML converter, this decrease in the extrema of the duty cycle increases the flying capacitor voltage ripple. The flying capacitor voltage ripple is proportional to both the time when the capacitor is charging or discharging and the inductor current. The flying capacitor charging or discharging time Δt is given by

$$\Delta t = \begin{cases} DT_{sw} & 0 < D < \frac{1}{N-1} \\ (1-D)T_{sw} & D > \frac{N-2}{N-1} \\ T_{sw}/(N-1) & \text{otherwise} \end{cases} \quad (6.1)$$

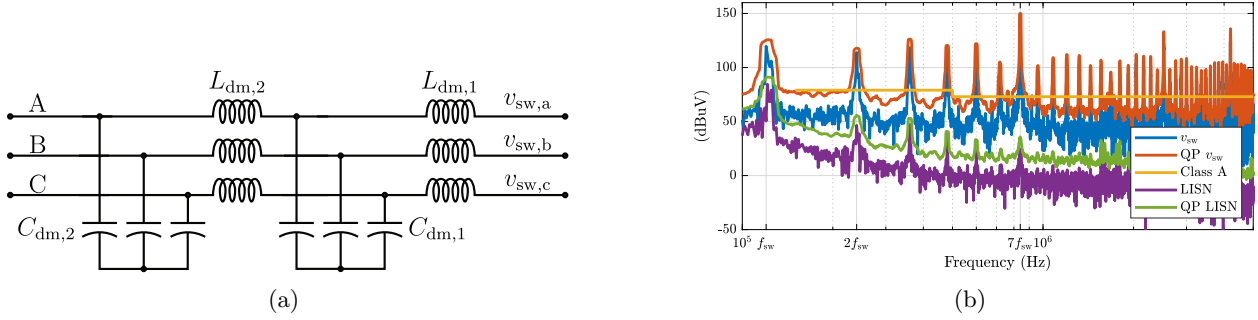


Figure 6.3: (a) Two-stage differential mode EMI filter schematic designed to meet the CISPR 32 Class A standard. Component values are provided in Table 6.1. (b) Simulated spectra of the switch node voltage v_{sw} and the voltage measured across the 50 Ω LISN resistor. Traces QP v_{sw} and QP LISN are conservative estimates of the quasi-peak measurements.

where N is the number of voltage levels apparent in the switch node voltage. Since SVM reduces the extrema of the duty cycle, the flying capacitor (dis)charging time is increased at the peak of the line current and the flying capacitor voltage ripple is increased. SVM thus allows a decrease in inductor size at the cost of increased flying capacitor voltage ripple.

6.2.2 EMI Filter Design

The conducted emissions of grid-connected rectifiers are regulated by standards such as CISPR 32 [85]. This work presents the design of a differential mode filter which meets the relevant standards with significant margin. The differential mode filter can be viewed as a passive network which must attenuate the harmonics of the switch node voltage v_{sw} to a level acceptable as measured by the receiver resistor as part of a line impedance stabilization network (LISN). If the converter switching frequency f_{sw} is chosen to be sufficiently below the minimum frequency of interest (for CISPR 32, 150 kHz), the harmonics of f_{sw} , rather than f_{sw} itself, must be attenuated, resulting in reduced filter attenuation requirements and volume. Ideally, the lowest frequency contained within the switch node voltage of an FCML converter is $(N - 1)f_{sw}$. However, if the flying capacitor voltage ripple and flying capacitor voltage imbalance are considered, the harmonics from $2f_{sw}$ to $(N - 2)f_{sw}$ must similarly be attenuated [77]. In this work, a switching frequency of 120 kHz was selected to prevent the sideband of the switching frequency from appearing in the CISPR measurement band which begins at 150 kHz. At the nominal output power of 24 kW, the simulated emissions at $2f_{sw}$ (240 kHz) would be 121 dB μ V while the emissions at $(N - 1)f_{sw}$ (840 kHz) would be 150 dB μ V. To meet the CISPR Class A limit with 12 dB of margin, the filter must achieve 54 dB of attenuation at 240 kHz and 89 dB of attenuation at 840 kHz. Assuming a two-stage filter design, this 240 kHz attenuation requirement determines the filter attenuation specification as a typical second-order passive filter designed to attenuate the $(N - 1)f_{sw}$ harmonic would not have sufficient attenuation at $2f_{sw}$ to meet the limit with sufficient margin, a departure from the finding in [96]. Fig. 6.3 shows the implemented EMI filter

topology and simulation results. Traces QP v_{sw} and QP LISN are conservative estimates of the quasi-peak measurements typically regulated by standards such as CISPR 32 by accounting for the resolution bandwidth of the EMC test receiver [97]. The implemented filter is a two-stage design, as depicted in Fig. 6.3(a), and the filter component values are provided in Table 6.1. To minimize filter volume, both components are chosen to be of the same value (i.e., $L_{dm,1} = L_{dm,2}$ and $C_{dm,1} = C_{dm,2}$) [98]. C_{dm} was chosen such that 10° of phase displacement due to the filter would occur at 10% of the nominal output power [99]. The corner frequency of this two-stage filter must be

$$f_{\text{corner}} = 2f_{\text{sw}}(A)^{1/4}, \quad (6.2)$$

where A is the (linear) desired attenuation as the attenuation increases at a rate of 80 dB/decade beyond the corner frequency of the filters. The differential filter inductance to achieve this corner frequency is then

$$L_{dm} = \frac{1}{(2\pi f_{\text{corner}})^2 C_{dm}}. \quad (6.3)$$

6.2.3 Performance Characteristics

Design of the FCML converter components is critical to achieving a high performance converter prototype. This section analyzes both the primary loss mechanisms of the converter and the impact of increased flying capacitor voltage ripple on efficiency and power density. Fig. 6.4(a) shows the analytical low-side transistor losses over one grid period for one of the three phases. The transistor overlap losses were calculated according to the procedure in [100]. Recent work [89] has shown that operating the flying capacitors with significant voltage ripple can result in designs with improved power density without excessive efficiency penalties. To achieve both large flying capacitor voltage ripple and utilization of the high performing 200 V EPC GaN devices, an eight-level design was selected. Fig. 6.4(b) shows the calculated transistor $v_{ds,\text{stress}}$ as a result of the flying capacitor voltage ripple. For switches connected to two flying capacitors, $v_{ds,\text{stress}}$ is the difference in adjacent flying capacitor voltages. For the final two switch pairs, $v_{ds,\text{stress},1} = v_{C,1}$ while $v_{ds,\text{stress},7} = V_{dc} - v_{C,6}$. This stress accounts for the flying capacitor small-signal capacitance de-rating with respect to voltage and the charging/discharging time across the line cycle. Due to utilizing space vector modulation, the peak $v_{ds,\text{stress}}$ occurs at the peak of the line cycle.

Fig. 6.5 provides the simulated efficiency and loss breakdown for the proposed converter, when the converter operates as an inverter driving a wye-connected resistive load. The converter attains a simulated peak efficiency of 99.2% and a full-load efficiency of 99.1% at an output power of 13.5 kW and 25 kW respectively. At the full load operating point, the losses per device are 4.9 W, the primary limit for the converter's output power. The core losses of the inductors within the EMI filter and the semiconductor losses were calculated according to the manufacturer-provided models.

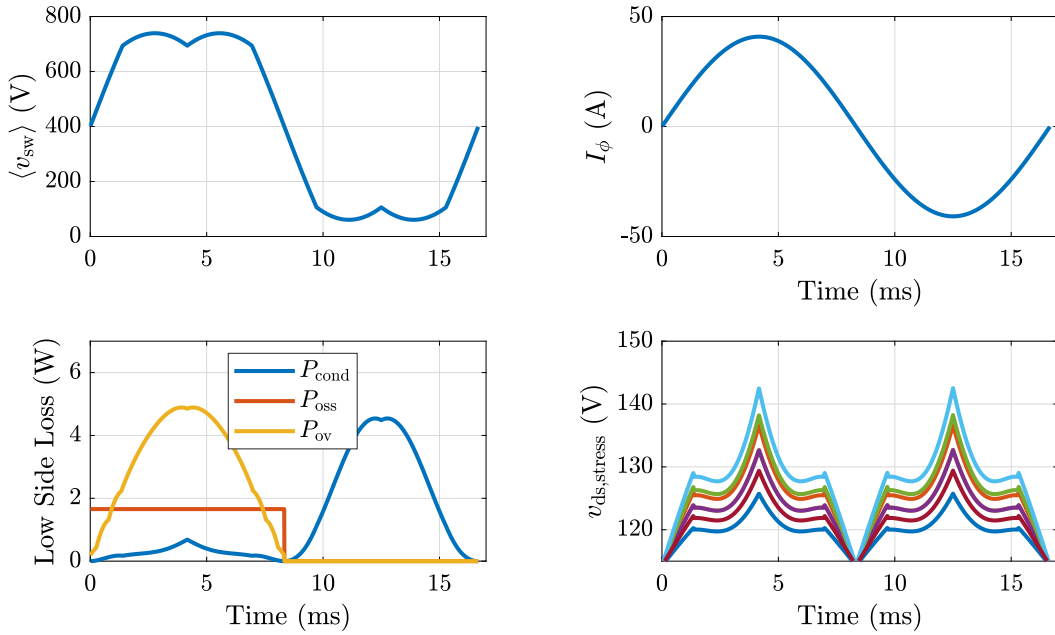


Figure 6.4: Analytical average switch node voltage, phase current, low side transistor losses, and transistor voltage stress for one phase. The converter is connected to a 480 V_{rms} line-to-line grid, processing $P_{out} = 8$ kW per phase at $f_{sw} = 120$ kHz. Switching losses are broken down into overlap losses P_{ov} and switch output capacitance hard-switching loss P_{oss} . This design operates the flying capacitors with significant voltage ripple to improve power density while maintaining sufficient transistor voltage stress margin.

6.2.4 Controller Design

Power factor correction (PFC) control is accomplished with a conventional multi-loop controller in the direct-quadrature (dq) domain [92], shown in Fig. 6.6. The outer, slower dc bus voltage controller commands a d-axis current reference while the q-axis reference current is zero to achieve unity power factor operation. A three-phase synchronously rotating reference frame PLL [101], [102] is used to obtain the grid angle.

A small dead time (0.3% of the switching period) is inserted between switching events of the same switching cell to prevent shoot through. This dead time, however, induces a 5th harmonic ripple in the line current [103] creating a disturbance the controller must reject. To reduce the THD of the line current, an adaptive feedforward Cancellation (AFC) controller is implemented [91], [104]. The AFC controller provides a large gain at the 6th harmonic (360 Hz), enabling the controller to reject the periodic dead time disturbance and other harmonics of this disturbance.

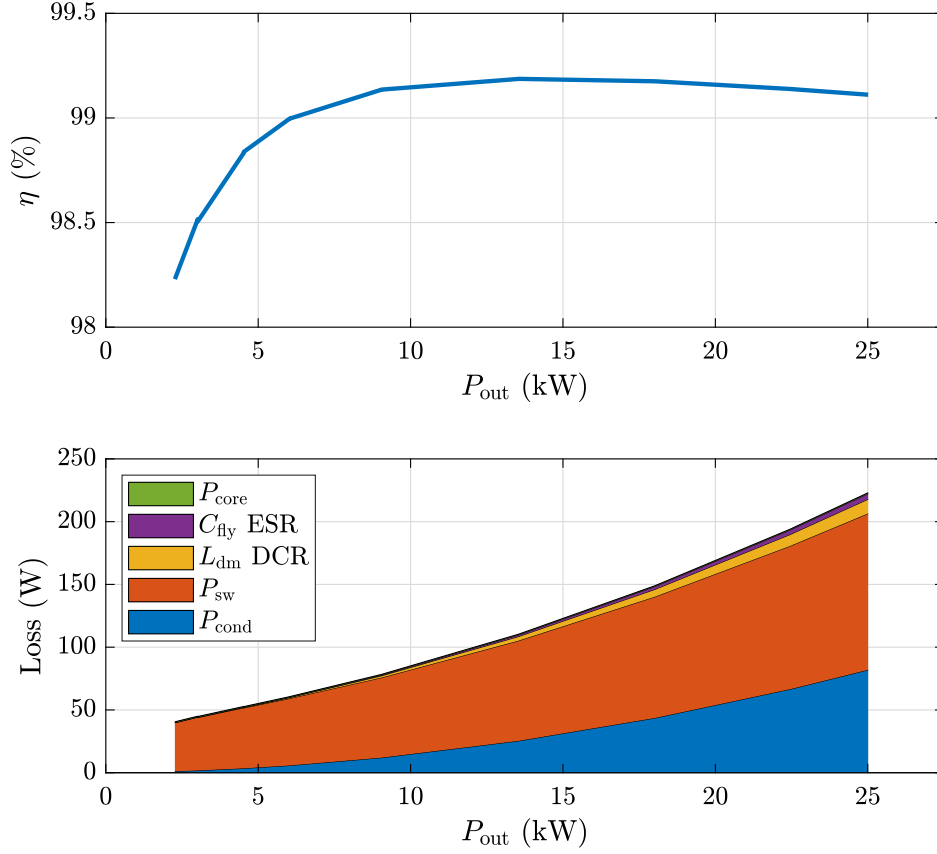


Figure 6.5: Simulated efficiency and breakdown of the primary loss mechanisms. The eight-level FCML rectifier operates from a 800 V dc voltage to create a 480 V_{rms} line-to-line grid across a three-phase, wye-connected resistive load. The simulated peak efficiency is 99.2% at an output power of 13.5 kW while the full load efficiency is 99.1% at an output power of 25 kW.

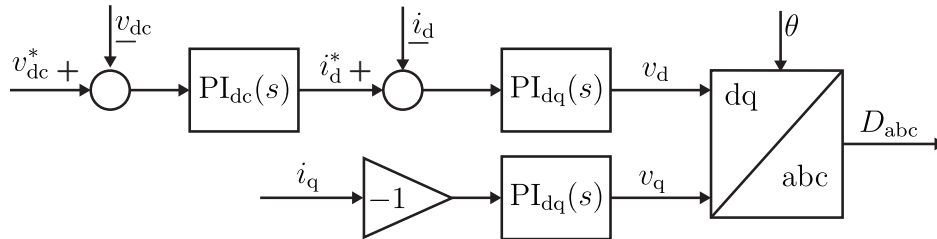


Figure 6.6: Power factor correction (PFC) multi-loop controller structure. A three-phase PLL (not shown) is used to obtain the grid angle from the measured grid voltage.

6.3 Experimental Results

A three-phase eight-level FCML converter prototype was designed and fabricated. Fig. 6.7 provides annotated photographs of the top and bottom of the hardware prototype. Relevant component parameters are provided in Table 6.1. N_s denotes the number of capacitors

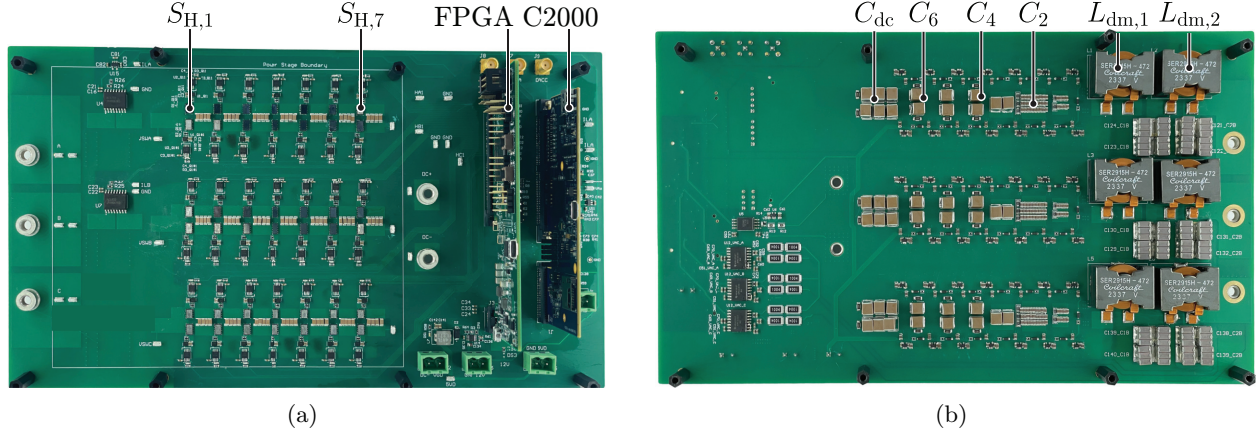


Figure 6.7: Photograph of the implemented hardware prototype. The PCB area is $11'' \times 6.3''$ while the power stage area is $6.45'' \times 5.54''$. The height of the power stage is $0.72''$. When operated at the design output power of $P_{out} = 25 \text{ kW}$, the prototype achieves a power stage power density of 60.24 kW/dm^3 .

Table 6.1: Component List

Component	Description	Part Number
Power Semi.	200 V, $3.5 \text{ m}\Omega$	EPC2304
Gate Driver	5 V, 7 A source, 5 A sink	LMG1025
Dig. Isolator	2.5 kV_{rms} , 150 Mbps	IL710
$L_{dm,1}$ & $L_{dm,2}$	$4.7 \mu\text{H}$, $I_{sat} = 48 \text{ A}$	SER2915H-472KL
$C_{dm,1}$ & $C_{dm,2}$	$4 \times 300 \text{ nF}$	CAA573C0G2J304J640LH
C_{dc}	$N_s = 2$, $N_p = 9$	C5750X6S2W225K250KAF
$C_{fly,decoupling}$	$4 \times 10 \text{ nF}$	C1206C103KFRAC7800
C_1	$4.7 \mu\text{F}$, $N_s = 2$, $N_p = 8$	C2012X5R2A475K125AC
C_2	$4.7 \mu\text{F}$, $N_s = 3$, $N_p = 18$	C2012X5R2A475K125AC
C_3	$2.2 \mu\text{F}$, $N_s = 1$, $N_p = 12$	C5750X6S2W225K250KA
C_4	$2.2 \mu\text{F}$, $N_s = 2$, $N_p = 6$	C5750X6S2W225K250KA
C_5	$2.2 \mu\text{F}$, $N_s = 2$, $N_p = 6$	C5750X6S2W225K250KA
C_6	$2.2 \mu\text{F}$, $N_s = 2$, $N_p = 6$	C5750X6S2W225K250KA

connected in series and N_p the number connected in parallel. To create the dense flying capacitor array, series combinations of 100 V MLCC capacitors were used for capacitors C_1 and C_3 while series combinations of 450 V capacitors were used for C_3 through C_6 and C_{dc} . Each switch pair is operated at a switching frequency of $f_{sw} = 120 \text{ kHz}$. Space vector modulation [95] was implemented by adding a common-mode component which varied at 360 Hz to all three duty cycles [92].

Gate drive power was generated with a cascaded bootstrap network [105] with a bootstrap

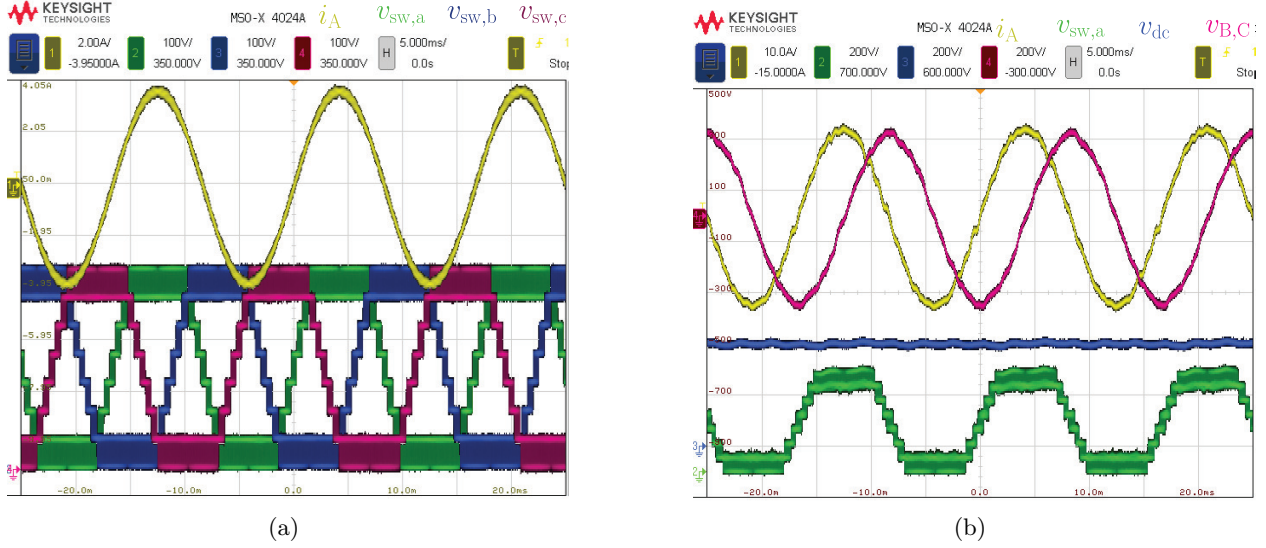


Figure 6.8: (a) Measured phase A current and switch node voltages when operated as an inverter with $V_{dc} = 387$ V. The symmetry apparent in the switch node voltages indicates that the flying capacitor voltages are at their balanced values. (b) Operation as a PFC rectifier with $V_{dc} = 393.5$ V and $I_{dc} = 12$ A for an output power of $P_{dc} = 4.73$ kW and an efficiency of $\eta = 98.75\%$. The current THD is 2.86%.

supply voltage of 15 V. Given a minimum duty cycle of 5% and a gate charge of $Q_g = 25$ nC [106], the diode forward current is $I_F = Q_g / (DT_{sw}) = 60$ mA, assuming the cascaded bootstrap switched-capacitor network operates in the slow switching limit. At this forward current, the utilized Schottky diodes exhibit an approximate 0.7 V drop. The total voltage drop of the chain of diodes in the cascaded bootstrap scheme resulted in $13 \cdot 0.7$ V = 9.1 V of total diode drops. Each gate drive IC is fed through an LDO that obtains its power from the corresponding bootstrap capacitor. Allotting 500 mV of headroom to the LDO at the end of the cascaded bootstrap chain results in a 14.6 V minimum gate drive voltage. Digital isolators were used to provide source-referenced signals to the gate drivers.

A TI C2000 F28379D DSP samples the grid voltages, inductor currents, and dc bus voltage, then computes the desired duty cycles according to the control law described in Fig. 6.6. The DSP commands an Altera 10M50DA FPGA over a SPI communication link to generate the 42 PWM signals. The power stage volume is 0.415 dm³ resulting in a power stage power density of 60.24 kW/dm³ for the design output power of $P_{out} = 25$ kW.

The prototype was tested as an inverter up to a dc voltage of 700 V and an ac line-to-line voltage of 415.2 V_{rms}. The inverter was connected to a three-phase wye-connected resistive load. The converter was operated up to an output power of $P_{out} = 5.06$ kW achieving a conversion efficiency of $\eta = 98.5\%$ as measured by a Yokogawa WT3000 power analyzer. Converter waveforms while operating as an inverter are provided in Fig. 6.8(a), showcasing the smooth sinusoidal output current with low THD. Moreover, the discrete and evenly spaced switching waveforms for the three phases indicates excellent flying capacitor voltage balancing. Fig. 6.8(b) illustrates operation as a PFC rectifier connected to a 238 V_{rms} line-

to-line grid. The ac voltage was provided by a three-phase variable transformer connected in series with a three-phase, wye-to-wye transformer. The converter powered a constant current electronic load with $I_{dc} = 12$ A for an output power of 4.75 kW. At this operating point, the converter efficiency was 98.75% and the current THD was 2.86% over a frequency range from dc to 3 kHz. The gate drive power loss was 2.65 W, reducing the conversion efficiency including gate drive loss to 98.73%. Equipment limitations prevented evaluation of the hardware prototype at the nominal full power rating.

6.4 Chapter Remarks

Innovations in data center computation and cooling are enabling significant increases in data center rack power consumption. To maintain high efficiency rack power delivery, architectures will require high rack voltages and high-performance three-phase rectifiers. This chapter detailed the design and implementation of a three-phase, eight-level FCML rectifier to achieve high performance ac/dc conversion. The FCML converter's utilization of low voltage semiconductors and capacitive energy storage enables efficient and power dense rectifiers. This work detailed the EMI filter design, converter modulation, and gate drive power delivery to achieve practical high level count FCML rectifiers, showcasing high efficiency (98.73%) at an output power of 4.75 kW while achieving power factor correction with a current THD of 2.86%. A hardware prototype was constructed to validate the proposed converter.

Chapter 7

Design and Analysis of a High Step-Down Ratio Capacitively-Isolated Flying Capacitor Multilevel Resonant Converter

Portions of this chapter are adapted in part or in whole from [107].

7.1 Introduction

High-performance, high step-down ratio isolated dc-dc converters are critical to applications such as data center power delivery, consumer electronics charging, and LED lighting [88], [108], [109], [110]. Fig. 7.1 shows a typical two-stage solution for isolated rectifiers used in these applications where, to achieve the target output voltage and galvanic isolation, a high step-down ratio dc-dc converter is required. Although transformers are typically utilized to both create an isolation barrier and provide voltage conversion, they can dominate the loss and volume of converter realizations and can be difficult to miniaturize [111]. This work investigates capacitive-isolation as an alternative architecture to achieve high-performance dc-dc converters.

One key design constraint for capacitively-isolated converters is the selection of both the isolation capacitance value and capacitor type. Prior work featuring capacitive isolation has often utilized excessively large isolation capacitance and/or did not utilize class Y safety capacitors which would be required in many practical systems where human safety must be considered [112], [113], [114], [115]. Here, we use the limit of maximum permissible touch current to quantitatively constrain the maximum capacitance of capacitively-isolated converters.

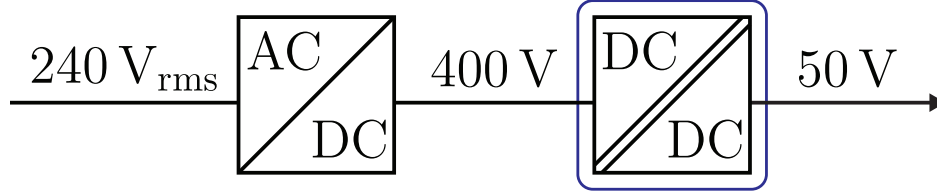


Figure 7.1: Schematic of a two-stage isolated rectifier with typical voltages labeled. In applications such as data center power delivery and consumer electronics charging, both galvanic isolation and a large step-down ratio are required of the dc-dc converter. The dc-dc stage is the focus of this work.

This work develops a hardware prototype which utilizes both appropriately designed class Y safety capacitors and a flying capacitor multilevel (FCML) bridge leg to create a high-step-down ratio capacitively-isolated resonant dc-dc converter. In addition to employing low-voltage, high figure-of-merit switches, the switch-node voltage of an FCML bridge leg is at a higher frequency and lower amplitude compared to a two-level converter. The reduced amplitude of the switch node voltage makes it possible to implement a high step-down ratio capacitively-isolated dc-dc converter in a single stage while the effect of frequency multiplication allows the design to operate efficiently at high frequencies. Frequency multiplication is especially useful in this application as the total isolation capacitance is limited due to safety constraints, which favors designs which can operate at high frequencies.

7.2 Capacitive Isolation as an Alternative to Transformer Isolation

Transformers often dominate converter volume, weight, and losses in highly optimized isolated dc-dc converters (e.g., [27], [116], [117]). Additionally, the power-handling capability of transformers and inductors scales poorly to smaller volumes [111], making miniaturization difficult. As an alternative approach, this work investigates an isolation capacitor network which can achieve the same safety objectives of transformer-based solutions. Capacitive isolation can thus mitigate a design's reliance on heavy and lossy magnetics and is likely to scale favorably to miniaturized, lower power applications.

To utilize capacitive-isolation as an alternative for transformer-based solutions, the quantitative metrics associated with isolation must be evaluated. UL Standard 60950 [118] provides guidelines on evaluating the safety of mains connected equipment by specifying the maximum allowed touch current, determined by connecting a measuring network, shown schematically in Fig. 7.2(a) and (b), to the unit under test. The touch current is determined according to $i_{TC} = v_{TC}/500\ \Omega$, where v_{TC} is the output of the measuring network. Given a limit of $i_{TC,max} = 3.5\text{ mA}_{rms}$ [118], the corresponding $v_{TC,max} = 1.75\text{ V}_{rms}$. In applications where v_{TC} is non-sinusoidal, the peak rather than the rms value may be evaluated. In this case, $v_{TC,max} = 2.475\text{ V}$.

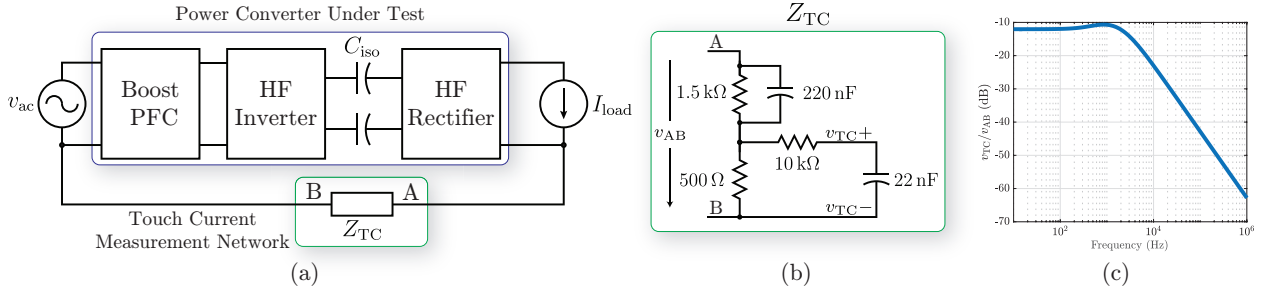


Figure 7.2: (a) Single phase power factor correction (PFC) rectifier schematic employing capacitive isolation connected to touch current measuring network Z_{TC} [118]. Nodes A and B which are the input to Z_{TC} are explicitly labeled. (b) Touch current measurement network Z_{TC} . The touch current magnitude is determined by $i_{TC} = v_{TC}/500\Omega$. (c) Magnitude of v_{TC}/v_{AB} vs. frequency. Note the low pass nature of Z_{TC} .

7.2.1 Choice of Isolation Capacitor

Fig. 7.2(c) provides a plot of the magnitude of the transfer function v_{TC}/v_{AB} , which can be used to characterize Z_{TC} . Components of v_{TC} near the line frequency are attenuated only by the resistor divider while high frequency components are attenuated also by the capacitors within Z_{TC} . At the 60 Hz line frequency, the capacitors in Z_{TC} are approximately open circuits and $v_{TC} \approx v_{AB}/4$. Given $v_{TC,max} = 2.475$ V, the maximum permissible v_{AB} is 9.9 V. The full bridge rectifier structure shown in Fig. 7.3(a) applies a non-sinusoidal low-frequency voltage across v_{TC} [119]. When $v_{ac} < 0$, the circuit is configured according to Fig. 7.3(b). During this half of the line-cycle, there is no low frequency voltage impressed on Z_{TC} and thus $v_{TC} = 0$. During $v_{ac} > 0$, however, the grid voltage appears in series with Z_{TC} and the isolation capacitors C_{iso} , shown in Fig. 7.3(c). Thus the peak value of v_{AB} may be found by analyzing the voltage divider formed by the resistors in Z_{TC} (approximately 2 kΩ) and the isolation capacitors C_{iso} :

$$V_{AB,pk} = \sqrt{2}V_{ac,rms} \frac{2 \times 10^3}{\sqrt{(2 \times 10^3)^2 + (\omega_g 2C_{iso})^{-2}}}. \quad (7.1)$$

For $V_{ac} = 277$ V_{rms} and $v_{AB,max} = 9.9$ V, the maximum $C_{iso} = 16.76$ nF. Fig. 7.3(d) shows simulated results of both v_{TC} and v_{AB} . Note that despite the relatively large amplitude of voltage applied to Z_{TC} , the network attenuates the high frequency component of v_{AB} and only the low frequency component remains. As predicted by (7.1), with $C_{iso} = 11.88$ nF, $v_{TC,pk} = 1.51$ V.

For the power factor correction (PFC) rectifier system considered in Fig. 7.2(a), the specific rectifier topology impacts the voltage impressed upon the touch current measurement network. Bridgeless rectifier topologies such as the totem-pole bridgeless boost or the dual boost rectifier [120] will apply different stresses to the isolation capacitors compared to a the conventional full bridge boost rectifier shown in Fig. 7.3. The impact of these alternative rectifier structures on the constraint of maximum isolation capacitance is an open point of investigation for future work.

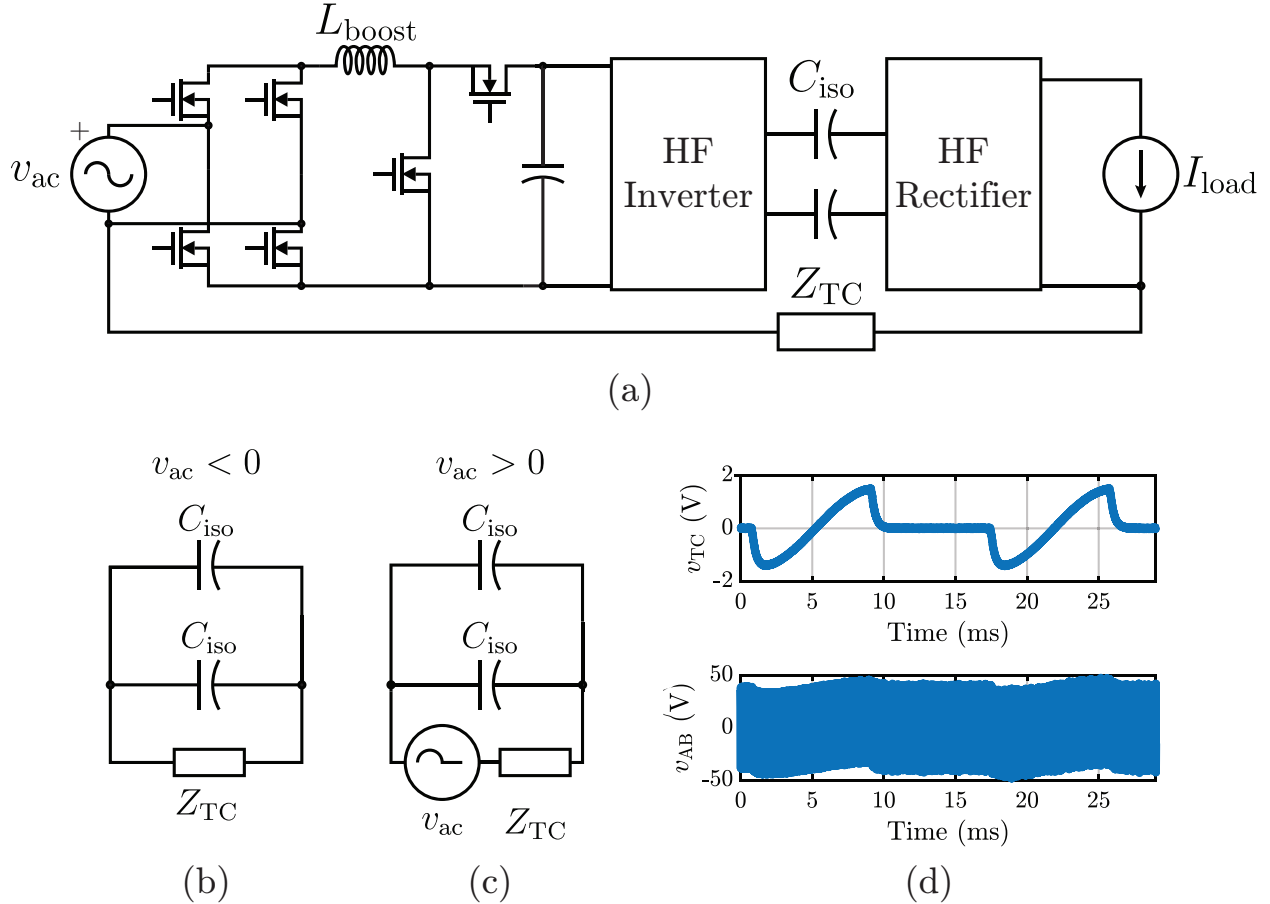


Figure 7.3: (a) Schematic illustrating connection of touch current measurement network Z_{TC} to capacitively isolated rectifier with full bridge rectifier boost PFC converter. Equivalent low frequency touch current common mode circuit when (b) $v_{ac} < 0$ and (c) $v_{ac} > 0$ [119]. (d) Simulated v_{TC} with $C_{iso} = 11.88 \text{ nF}$ and $V_{ac} = 240 \text{ V}_{rms}$. v_{TC} has an RMS value of 0.72 V_{rms} over a 60 Hz period with an absolute maximum value of 1.51 V . A non-sinusoidal v_{TC} voltage is created by the full bridge grid-tied rectifier.

7.3 Achieving Voltage Conversion with the FCML Converter

Without the turns ratio of a transformer to assist in achieving voltage conversion, capacitively-isolated converters must use alternative techniques to achieve high step-down ratios. One approach to achieve a high step-down ratio is to configure multiple low step-down ratio converters in input-series output-parallel (ISOP) configuration [114], [121], [122], [123]. One drawback of this approach is that the allotment of isolation capacitance must be distributed to each converter cell. This distribution of isolation capacitance forces each cell to operate at a higher frequency or employ multiple larger resonant inductances compared to a single-cell solution, both of which would likely compromise power density and efficiency [111].

The flying capacitor multilevel (FCML) converter [1] is a hybrid switched capacitor con-

verter that naturally performs voltage conversion by creating a switching node voltage which toggles between two fractions of the supply voltage, avoiding the aforementioned drawbacks of an ISOP capacitively-isolated structure. In an FCML bridge leg, the switch node voltage v_{sw} switches between voltage levels separated by $V_{in}/(N-1)$ where N is the number of levels in the FCML bridge leg. In addition to the amplitude of v_{sw} being reduced compared to a two-level half bridge, the frequency of v_{sw} is at an effective frequency $f_{eff} = (N-1)f_{sw}$. A schematic of the proposed capacitively-isolated dc-dc converter utilizing an FCML bridge leg is provided in Fig. 7.4(a). These features of innate voltage step-down and apparent frequency multiplication observed at the switching node voltage v_{sw} [1] make the FCML bridge leg a promising circuit to utilize in conjunction with a capacitively-isolated resonant tank.

The FCML converter additionally distributes the voltage stress applied to the switches such that low voltage, high figure of merit switches can be utilized compared to a two-level converter [9]. However, these benefits of reduced switch node voltage amplitude and period and switch voltage stress are achieved only if the flying capacitor voltages maintain a “balanced” distribution of $v_{C,k} = k \cdot V_{in}/(N-1)$, where the integer k ranges from 1 to $N-2$. Previous analyses (e.g., [13], [20]) have investigated the mechanisms by which this balanced flying capacitor voltage distribution is achieved. In short, typically the FCML converter is operated with symmetric phase shifted PWM (PS-PWM), where all high-side switches are driven with the same duty cycle and switching signals are evenly phase shifted throughout the switching period. This modulation scheme is shown in Fig. 7.4(b). When the FCML converter is operated with symmetric PS-PWM, imbalanced flying capacitor voltages induce harmonics in the switch node voltage v_{sw} at frequencies from f_{sw} to $(N-2)f_{sw}$. These v_{sw} harmonics induce currents and losses which drive the flying capacitor voltages to the balanced distribution.

The capacitively isolated dc-dc converter investigated in this work deviates from the typical FCML converter configuration in that the FCML bridge leg drives a series resonant circuit with an average current of zero and a dominant fundamental harmonic component at $(N-1)f_{sw}$. Through simulations and experiments of the proposed converter, the flying capacitor voltages balanced sufficiently well. The authors believe similar balancing mechanisms exist when the FCML bridge leg is operated in this manner however, a full investigation of flying capacitor voltage balancing in this configuration remains a point of investigation for future work.

7.3.1 ZVS Analysis

In order to operate at high frequency, soft switching of the power transistors is important to mitigate switching-related losses and operate at high efficiency. When operating the FCML converter with symmetric PS-PWM, when a high-side transistor $S_{H,k}$ turns ON, v_{sw} goes from a lower voltage level to a higher voltage level. For example, when operating a four-level FCML converter at a duty cycle of 50%, when an $S_{H,k}$ transistor turns ON, v_{sw} rises from $V_{in}/3$ to $2V_{in}/3$. Conversely, when an $S_{L,k}$ switch turns ON, v_{sw} falls from $2V_{in}/3$ to $V_{in}/3$. If an FCML bridge-leg is connected to a resonant tank which has an inductive impedance

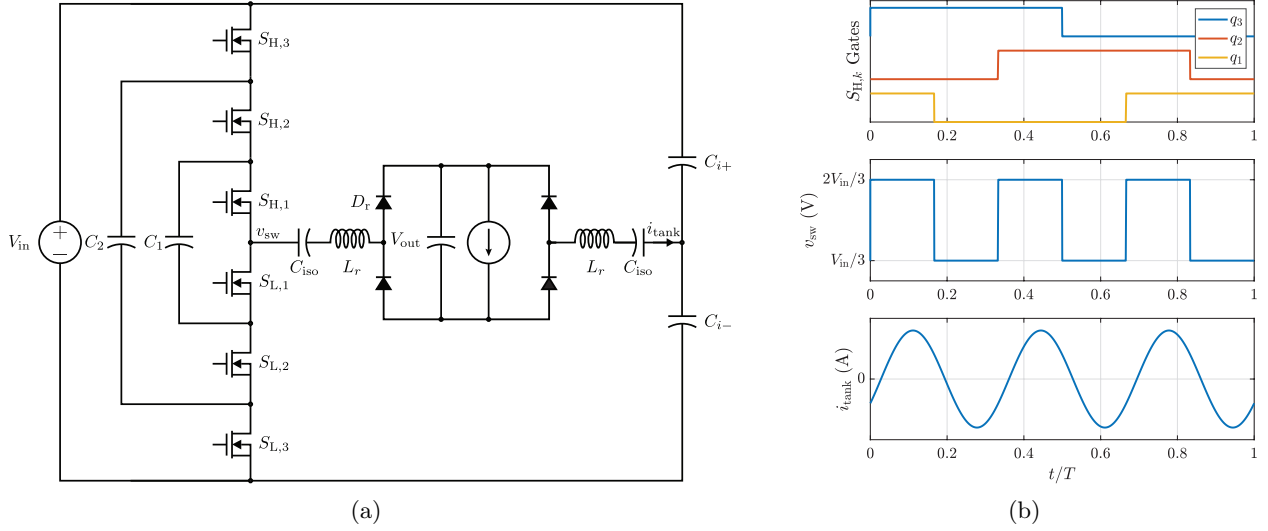


Figure 7.4: (a) Schematic of the capacitively-isolated four-level FCML series resonant dc-dc converter investigated in this work. Capacitors C_{iso} form the isolation barrier and are class Y safety capacitors. (b) Gating signals applied to $S_{H,k}$, switch node voltage v_{sw} , and resonant tank current i_{tank} when the FCML bridge leg is connected to a tank impedance which is inductive at $f_{eff} = 3f_{sw}$.

at the effective switching frequency $f_{eff} = (N - 1)f_{sw}$, the tank current i_{tank} will be of the correct polarity to softly commute the relevant transistor output capacitances and ZVS will be achieved. This property is conceptually shown in Fig. 7.4(b), where i_{tank} lags v_{sw} by 30° . As with conventional two-level converters, the energy stored by the resonant tank inductances must be sufficient to discharge the transistor output capacitances. Additionally, sufficient dead-time between complementary switching events must be allotted to achieve ZVS. Assuming the flying capacitors voltages are at the balanced state of $v_{C,1} = V_{in}/3$ and $v_{C,2} = 2 \cdot V_{in}/3$, when a switching event occurs, the tank current must satisfy the inequality $L_r I_{tank}^2 \geq Q_{oss} V_{in}/3$ where Q_{oss} is the charge required to raise the device voltage from 0 to $V_{dc}/3$ to achieve soft charging of the switch output capacitance [124].

7.3.2 Resonant Tank Design

Although alternative resonant tank structures could be employed (e.g., those enumerated in [125]), this work utilized a series resonant structure. To achieve the desired voltage conversion ratio of 8:1, the effective switch node frequency must be higher than the resonant frequency as the four-level FCML achieves a conversion ratio of 6:1 and the remaining voltage conversion must be performed by the inductive impedance of the series resonant tank.

Assuming C_{iso} is chosen to be as large as possible (i.e., close to the touch current-informed limit), selection of L_r impacts both the resonant frequency and peak energy storage of the series resonant tank. Designs with larger L_r exhibit a reduced tank resonant frequency and are thus able to reduce switching and other ac-related losses. However, this increased inductor energy storage forces either physically larger inductors to achieve tolerable inductor quality

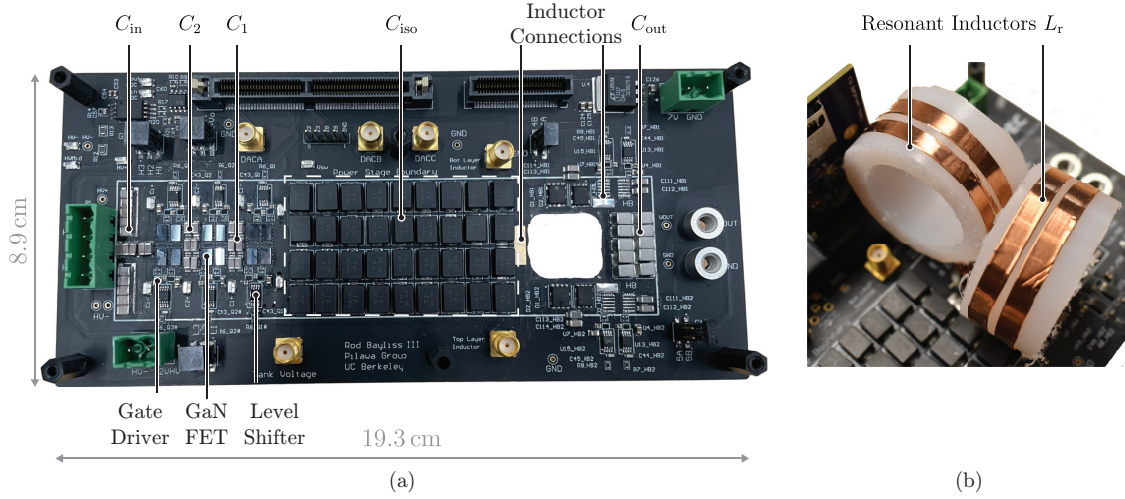


Figure 7.5: Capacitively-isolated FCML converter dc-dc hardware prototype. (a) Top-down view of board without inductors mounted and (b) resonant inductors mounted on the hardware prototype.

factors [126], [127] or increased loss. Conversely, designs which utilize smaller resonant inductances must operate at higher frequencies, suffering increased switching and ac-related losses but have reduced resonant tank energy storage and may be able to employ physically smaller and/or lower loss inductors. Designs with small resonant inductances also must operate with a wider switching frequency range with respect to load as the tank quality factor is reduced [128].

7.4 Experimental Results

A hardware prototype utilizing class Y safety capacitors was constructed to validate the capacitively-isolated FCML converter concept. An annotated photograph of the prototype is provided in Fig. 7.5 while a list of relevant power stage components is provided in Table 7.1. The resonant inductors L_r were each constructed using 2 turns of 4 mil thick copper foil on a PTFE cylinder with a diameter of 4.15 cm and a height of 2 cm. The board has a total area $19.3\text{ cm} \times 8.9\text{ cm}$ with a power stage area of $15.2\text{ cm} \times 3.9\text{ cm}$. Excluding the resonant inductors, the height of the power stage is 9 mm. Finally, the volume of the isolation capacitors C_{iso} is 14.52 cm^3 while the resonant inductors L_r occupy a (component) volume of 53.5 cm^3 . The gate drive voltages for the power-stage transistors were generated through a cascaded bootstrap network with low dropout regulators (PN: LT1117) [105], [129]. Each paralleled transistor was driven by a single gate driver and PWM level shifting from the C2000 F28379 DSP was accomplished with digital isolators (PN: IL710). Variable switching frequency control was used to regulate the output voltage as the load varies. As with other series resonant converters, the FCML converter switching frequency is reduced as the load current is increased.

Fig. 7.6 provides measured waveforms of the converter operating at a heavy load when

Table 7.1: Component List

Component	Description	Part Number
$S_{L,k}$ & $S_{H,k}$	$2 \times 200\text{V}$, $7.2\text{ m}\Omega$	EPC2307
Gate Driver	5 V , 7 A source, 5 A sink	LMG1020
C_1 & C_2	$12 \times 15\text{ nF}$	C3216C0G2W153J160AA
C_{iso}	$36 \times 330\text{ pF}$, $305\text{ V}_{\text{ac}}/1.5\text{ kV}_{\text{dc}}$	EVA86Q7UTF331KB01K
D_r	100 V , 30 A	STPS30H100DJF
$C_{i,+}$ & $C_{i,-}$	$30 \times 33\text{ nF}$	C3225C0G2W333J250AA
C_{out}	$20 \times 100\text{ nF}$	C4532C0G2A104J320KA
L_r	255 nH	N.A.

operating at an input voltage $V_{\text{in}} = 380\text{ V}$ and output voltage $V_{\text{out}} = 47\text{ V}$ for an approximate 8 : 1 voltage conversion ratio. The waveforms in Fig. 7.6 were taken when the converter was operating at an output current of $I_{\text{out}} = 13.3\text{ A}$ corresponding to an output power of $P_{\text{out}} = 622\text{ W}$. Of note are the smooth switch node transitions in Fig. 7.6(b), which indicate that the converter is operated under zero-voltage switching (ZVS). The tank current i_{tank} was measured with a Rogowski coil (PEM CWT). Fig. 7.7 shows the measured v_{gs} and v_{ds} of $S_{L,3}$ while the converter operated at a lower voltage point of $V_{\text{in}} = 30\text{ V}$. As can be seen, the switch drain voltage falls before the gate voltage rises, indicating that ZVS is achieved. Similar $v_{\text{gs}} - v_{\text{ds}}$ waveforms were observed for all six transistors at this operating point. As investigated in Section 7.3.1, the FCML bridge leg is able to achieve ZVS for all switch transitions if the bridge leg is connected to a resonant tank which is inductive at the $f_{\text{eff}} = (N - 1)f_{\text{sw}}$.

Fig. 7.8 provides the efficiency of the converter when operating at $V_{\text{in}} = 380\text{ V}$ and $V_{\text{out}} = 47\text{ V}$ and Fig. 7.9 provides thermal images of the converter operating at an output power of $P_{\text{out}} = 622\text{ W}$ under forced air cooling. The converter efficiency is limited due to the asynchronous diode rectification and the relatively low quality factor of the constructed resonant inductors. A small-signal inductor resistance measurement made with the Keysight E49990A Impedance Analyzer indicated $R_{\text{ac}} \approx 111\text{ m}\Omega$ at the heavy load tank frequency of 3.5 MHz .

7.5 Chapter Remarks

This chapter presented a capacitively-isolated high step-down dc-dc converter employing practical class Y safety capacitors. Capacitive-isolation offers an alternative technique to achieve galvanic isolation without reliance on transformers, which are difficult to miniaturize. This work analyzed the maximum permissible isolation capacitance C_{iso} to enable designs which adhere to the UL-60950 touch current standard. For a typical grid voltage of $V_{\text{ac}} =$

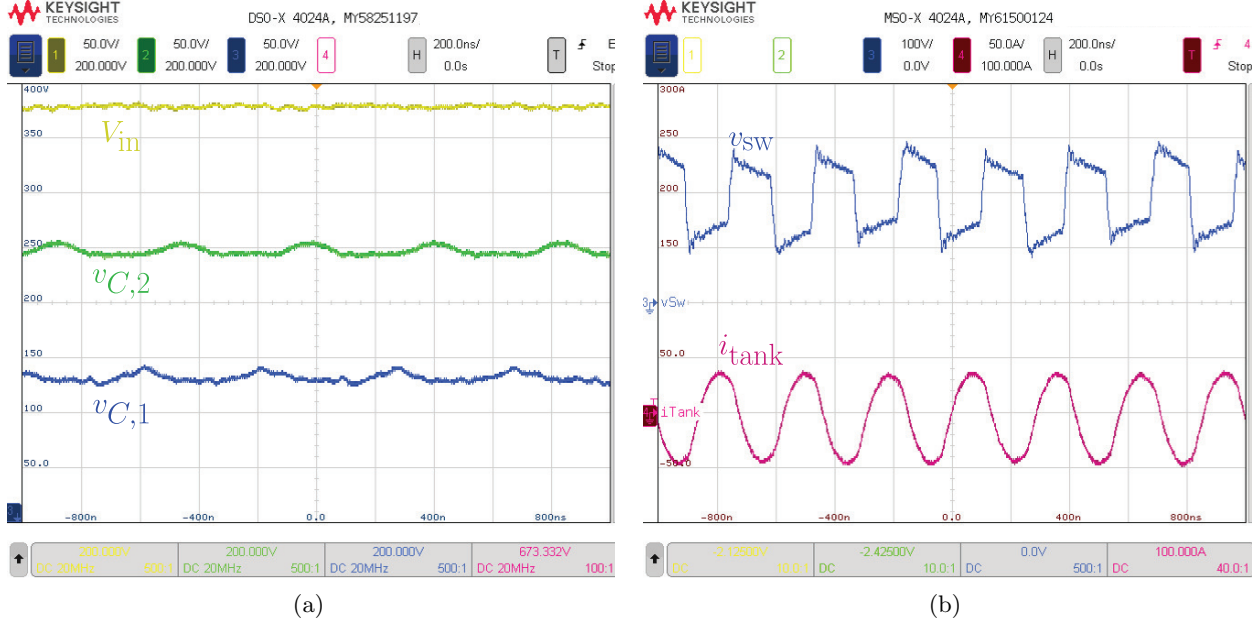


Figure 7.6: (a) Measured flying capacitor voltages and input voltage. (b) Measured switch node voltage v_{sw} and tank current i_{tank} . Relevant converter operational parameters are as follows: $V_{in} = 380$ V, $V_{out} = 47$ V, $I_{out} = 13.3$ A, and $f_{sw} = 1.16$ MHz.

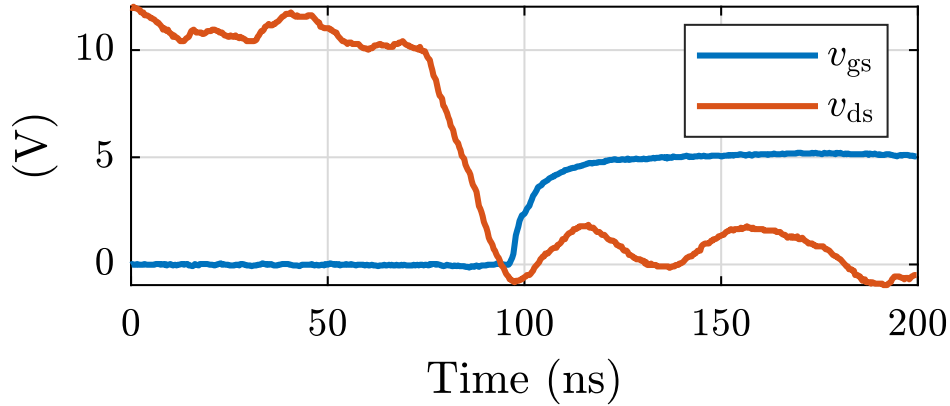


Figure 7.7: Measured v_{gs} and v_{ds} for $S_{L,3}$ while the converter was at a lower voltage operating point of $V_{in} = 30$ V, $I_{load} = 6.2$ A, and $f_{sw} = 1.85$ MHz.

$277 V_{rms}$, the maximum isolation capacitance is limited to 16.76 nF. To achieve a high-performance high voltage step-down ratio dc-dc converter, an FCML bridge leg was utilized, leveraging the benefits of switch node voltage amplitude reduction, switching frequency multiplication, and low voltage semiconductors. If the resonant tank is designed to be inductive at the effective switching frequency $f_{eff} = (N - 1)f_{sw}$, ZVS of all switches within the FCML converter can be achieved, further enabling efficient operation at high frequency. To the authors' knowledge, this work presented the first capacitively-isolated, high step-down ratio dc-dc converter using practical class Y capacitors without relying on an ISOP structure.

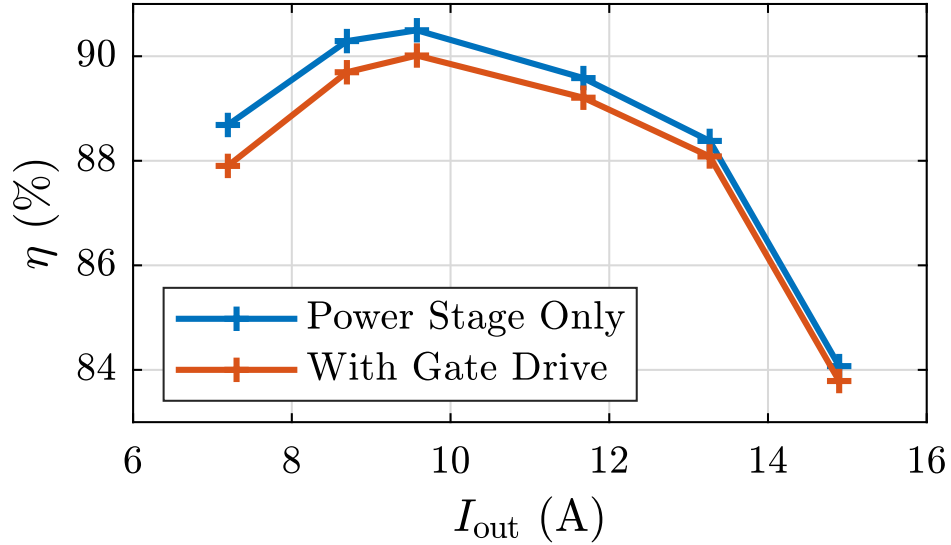


Figure 7.8: Measured converter efficiency with $V_{in} = 380$ V, $V_{out} = 47$ V. Converter efficiency was measured with a Keysight PA2201A Power Analyzer.

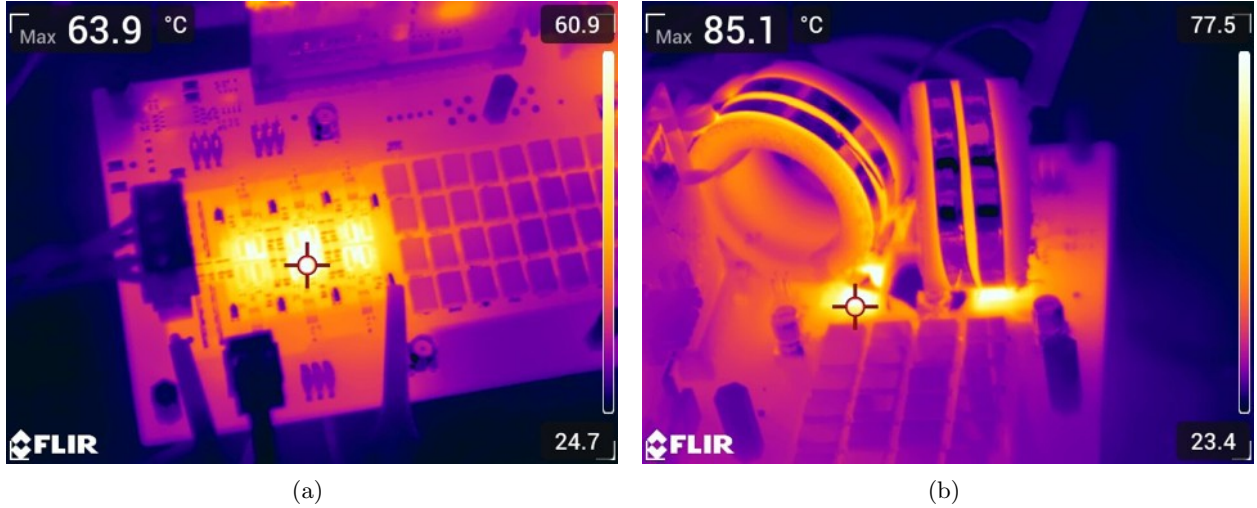


Figure 7.9: Thermal images of (a) FCML bridge leg FETs and isolation capacitors and (b) resonant tank inductors and output diodes. Images were captured using a FLIR T540. For these photos, the converter was at an operating point of $V_{in} = 380$ V, $V_{out} = 47$ V, and $P_{out} = 622$ W. A fan pointed down on the converter from above provided forced air cooling.

A hardware prototype was constructed and tested generating an isolated 47 V from an input of 380 V. Finally, understanding the mechanisms by which the flying capacitor voltages balance within this unconventional topology is of interest.

Chapter 8

Series-Stacked Buffer for Resonance Suppression in Multi-Motor Vehicles

8.1 Introduction

This chapter investigates electric vehicles composed of multiple drive units connected to a common dc bus (e.g., the vehicle's high voltage battery). To mitigate harness losses and electromagnetic interference, each drive unit should be packaged with sufficient input capacitance C_{in} such that the drive unit only draws dc current from the high voltage bus. However, due to the non-idealities of the harnesses which connect the drive unit to the battery and the typically large inductance associated with the battery pack, the ideally dc system of the battery bus to which all drive units are connected can result in one with significant high frequency currents flowing along the dc bus.

This chapter investigates the utilization of active filters to *locally* suppress the emission of harmful harmonics such that these harmonics do not propagate onto the dc bus and disturb other equipment. Given the high bandwidth requirements and potentially large (reactive) power to be processed by this filter, we investigate the use of the series-stacked buffer [130], [131] as an implementation for this active filter.

8.2 Input Current Harmonics

Several works have investigated the properties of the input current of a three phase inverter i_{inv} [132], [133], [134]. Fig. 8.1(a) shows a schematic of a three phase inverter connected to a dc bus with non-trivial harness impedance Z_{in} . Fig 8.1(b) schematically shows a decomposition of i_{inv} into its constituent harmonics. Thus a three phase inverter can be modeled by several current sources in parallel with coefficients α_i that depend on the operating point of the machine. That is, as the modulation index of the inverter changes, the coefficients α_i will vary in a nonlinear manner. Additionally, the machine's torque is roughly linear with

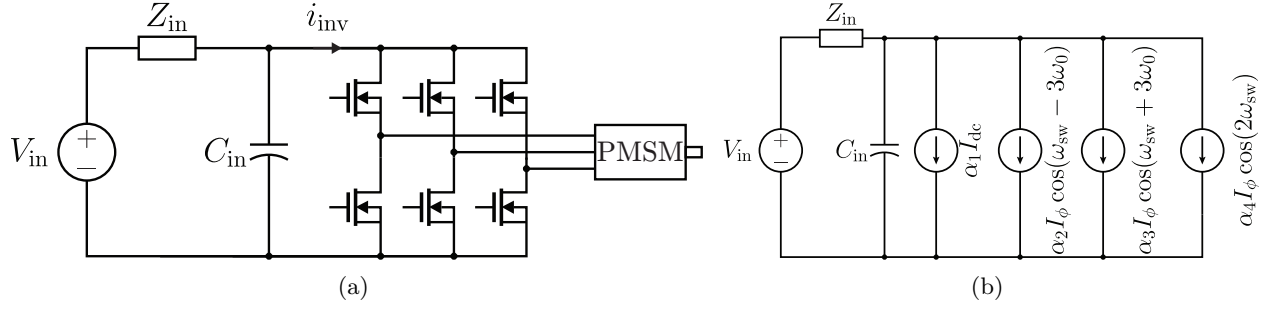


Figure 8.1: (a) Three-phase motor drive connected to a dc bus with non-zero harness impedance Z_{in} and permanent magnet synchronous machine (PMSM). (b) Current source decomposition model of the inverter input current i_{inv} .

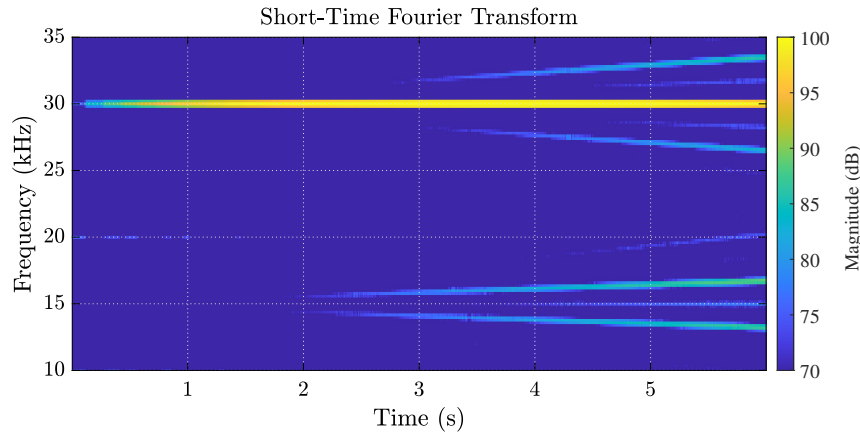


Figure 8.2: Short-Time Fourier Transform of inverter input current i_{inv} . The machine is controlled to output a constant torque while its speed is externally controlled to increase at a constant rate from 0 to 3500 RPM. The inverter operates at a constant $f_{sw} = 15$ kHz. Note that as the machine speed increases, the magnitude of the sidebands of f_{sw} increase while the frequencies depart from f_{sw} .

phase current magnitude I_ϕ and the speed of the machine impacts the frequency of several harmonics, namely the sidebands of the switching frequency $\omega_{sw} \pm 3\omega_0$.

Shown in Fig. 8.2 is a Short-Time Fourier Transform of an exemplar i_{inv} . The machine is externally accelerated at a constant speed while the inverter is controlled to output a constant torque (and thus maintain a constant I_ϕ). The inverter in this example operates at a constant switching frequency of 15 kHz. As the machine accelerates, the modulation index of the inverter must increase and the coefficients α_2 and α_3 , which correspond to the harmonics $\omega_{sw} \pm \omega_0$, increase. This increase in modulation depth results in these harmonics becoming more pronounced as the machine approaches the final speed in this simulation. Additionally, since the frequencies of these harmonics depend on the machine electrical speed ω_0 , the spectrogram possesses a dovetail pattern. Overall, both the amplitudes and the frequencies of the harmonics composing i_{inv} change dynamically.

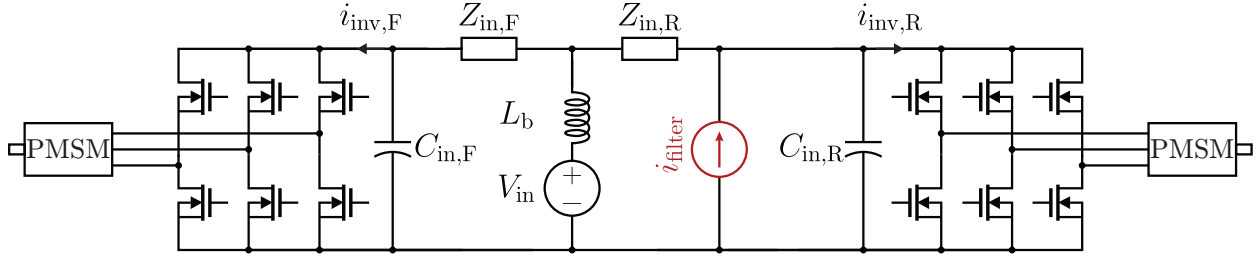


Figure 8.3: Two-motor electrical schematic of vehicle with non-trivial harness impedance $Z_{in,F}$ and $Z_{in,R}$ and battery impedance L_b . Shown in red is the proposed active filter i_{filter} which ideally operates as a current source anti-phase to the harmonics of $i_{inv,R}$.

8.3 Multi-Drive Systems

Electric vehicle designers seeking the absolute maximum in performance often turn to multi-drive architectures. By actively driving both axles, significant gains in acceleration, braking, energy recovery, and handling can be obtained. Although many of these benefits can be gained by driving each axle with a single machine, three motor vehicles (one in the front and two in the rear) and four motor vehicles (to actively drive each wheel) have been deployed in commercial products.

Fig. 8.3 shows a simplified electrical schematic of a two motor drive system. The front and rear inverters are coupled to a common dc bus through the battery. Ideally the voltages across the input capacitors $C_{in,F}$ and $C_{in,R}$ are constant and only dc currents flow through the harnesses $Z_{in,F}$ and $Z_{in,R}$. However, the non-idealities explicitly drawn as L_b , $Z_{in,F}$ and $Z_{in,R}$ can disturb this dc-coupled scenario. Due to the energy storage and peak power requirements of production electric vehicles, the physical size of the battery pack must be made to be quite large. This physical property manifests itself in the electrical domain as a relatively large inductance (on the order of several μH). Thus although at dc the battery pack presents itself as a relatively low impedance voltage source, at higher frequencies this inherent inductance prevents high frequency currents from flowing into the pack.

The parasitic which can have the most disastrous effect is that of the harness impedance Z_{in} . These impedances are primarily inductive and can range from 100s of nH with resistive components on the order of $\text{m}\Omega$. This harness inductance can resonate with the input capacitance of the inverter, resulting in unnecessary loss and emissions as input currents of one inverter flow through this resonating inductance onto the other. To illustrate this phenomenon, Fig. 8.4 plots the magnitude of the impedance seen at the dc port of the rear inverter. The circuit parameters used to extract this impedance are provided in Table 8.1. Both $Z_{in,F}$ and $Z_{in,R}$ are composed of a series combination of L_{in} and R_{in} . Of particular interest is the parallel resonance that appears at $\approx 18\text{ kHz}$. If the inverter operates at a switching frequency of 20 kHz and the machine spins at an electrical frequency of 667 Hz , the $i_{inv,R}$ harmonic of $\omega_{sw} - 3\omega_0$ will excite this resonance.

Although these resonances can be mitigated through an alternate parameter selection (i.e., a difference selection of Z_{in} and C_{in} may resonate at a non-problematic frequency),

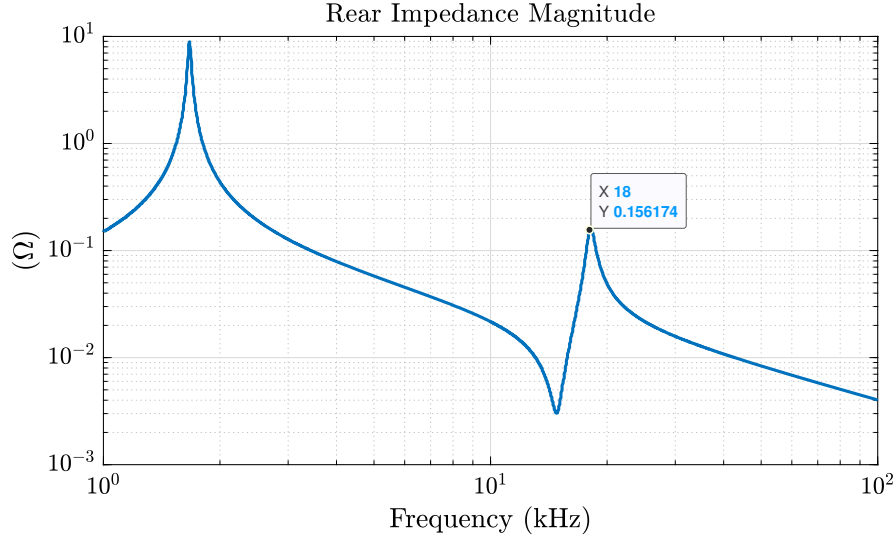


Figure 8.4: Rear harness impedance magnitude as seen from the port across the terminals of $C_{in,R}$. Note both the series resonance and parallel resonance associated with this system. The parallel resonance at 18 kHz is particularly problematic as harmonics of $i_{inv,R}$ can excite this resonance, inducing unnecessary emissions and loss.

this work investigates the use of active filters to avoid the excitation of these resonances altogether.

8.4 Active Filters for Mitigating System Resonance

One technique to mitigate harmful emissions is to utilize active filters local to the drive inverter, shown schematically as the red current source in Fig. 8.3. If the filter is implemented correctly, the harmonics generated by the inverter will be perfectly cancelled by the active filter and not propagate to the rest of the bus. Many high performance vehicles operate at large dc voltages, approaching $V_{dc} = 1$ kV. Thus filter topologies which do not require a separate converter utilizing high voltage (e.g., 1.25 kV) switches and do not require a high power converter power processing requirement are beneficial.

8.4.1 Series-Stacked Buffer

One such topology which enables the utilization of low voltage (relative to the system dc bus) switches and processes a fraction of the buffered power through the filter's power converter is the series stacked buffer [130], [131]. An schematic drawing of a drive inverter paired with a resonance-cancelling series stacked buffer (SSB) is shown in Fig. 8.5.

The SSB has found prominent use in line-frequency buffering applications [130], [131] where fully passive buffer solutions (e.g., through an electrolytic capacitor bank) are untenable from a size and efficiency perspective. In this application, the utilization of lower-voltage

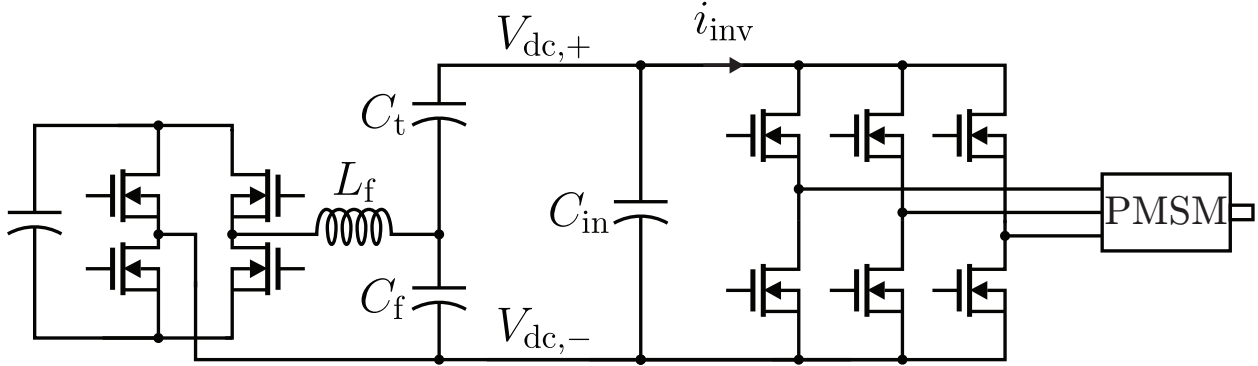


Figure 8.5: Schematic of motor drive inverter co-packaged with series-stacked buffer.

switches and the benefit of the power converter within the SSB only processing a fraction of the buffered power were found to have an outsized performance impact.

Although the use of the SSB as an active filter benefits from these same merits, one key difference in the motor drive active filter space compared to line-frequency buffers is the requirement of the filter to cancel harmonics of varying amplitudes and frequencies as mentioned in Section 8.2. For example, a drive inverter supplier may want their product to be used in a wide variety of end applications where the resonant frequencies of the dc-bus network are unknown. In this situation, having an active filter which is able to continuously monitor and cancel all problematic harmonics would allow the drive inverter to be used without worry of exciting these resonances.

8.4.2 SSB Operation

One technique to control the series stacked buffer is to regulate a voltage across the main energy processing capacitor C_t . If this voltage is able to be controlled, the current through the SSB branch is determined. $V_{dc} = v_{C_t} + v_{C_f}$ and if V_{dc} has relatively low ripple, by controlling v_{C_f} , $v_{C_t} = V_{dc} - v_{C_f}$. In sinusoidal steady state we can thus force a branch current of $i_C = \omega C v$ where ω is the desired angular frequency.

$$i_{C_t} = C_t \dot{v}_{C_t} \rightarrow i_{C_t} = \omega C_t v_{C_t} \quad (8.1)$$

$$v_{C_t} = \frac{i_{C_t}}{\omega C_t} \quad (8.2)$$

Thus given a desired SSB current i_{C_t} and frequency ω , the SSB controller generates an ac voltage across v_{C_f} anti-phase to the desired v_{C_t} voltage.

8.4.3 Control and Electrical Requirements

Although the high-level control objective of generating the desired voltage in an open-loop manner seems simple, there are several complications which warrant further investigation.

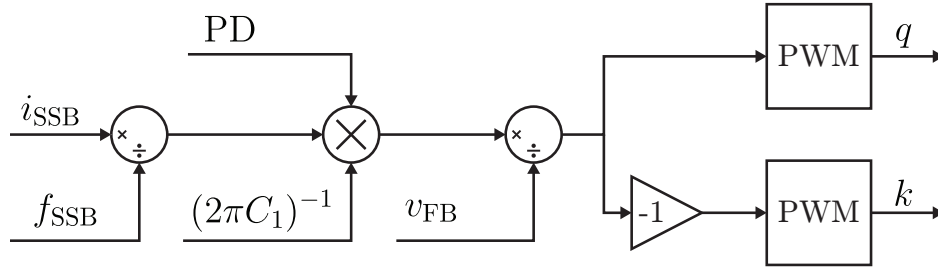


Figure 8.6: Series-stacked buffer control block diagram. Inputs to the controller are the desired current waveform i_{SSB} and frequency f_{SSB} of the waveform. Gating signals for the SSB full bridge are the output of the controller.

Given that the desired frequencies to be generated are relatively high (on the order of tens of kilohertz), there is a strong desire to minimize the passive components in the buffer C_t , C_f , and L_f . As a first order constraint, the resonant frequency of these elements ($\omega_{res} = \sqrt{L_f(C_f + C_t)^{-1}}$) must be larger than the highest desired frequency of current to be injected. This constraint of high frequency operation is directly in conflict with the dual objective of minimizing the power the SSB converter has to process and keeping buffer power losses low. Attempting to reduce L_f leads to increased ripple current and related losses and current distortion or an increase in switching losses to keep the ripple current at a reasonable level. Reducing C_t requires higher voltages to be generated by the SSB full bridge for the same branch current and frequency (see (8.2)) forcing more power to be processed by the SSB power converter as V_{SSB} must be increased.

This work investigates two solutions to the aforementioned constraints. First, unipolar modulation scheme was utilized to reduce the energy processing requirements on L_f [131]. Unipolar modulation effectively doubles the frequency of the ripple current in L_f for the same SSB switching frequency and reduces the voltage applied across L_f by using three level ($\pm V_{SSB}$ and 0) rather than two level ($\pm V_{SSB}$) voltage excitation.

Second, this work implemented pre-distortion of the duty cycle reference to compensate for gain of resonant tank. Although the resonant frequency of the SSB elements ω_{res} is larger than the desired frequency to be generated, the transfer function from the full bridge voltage to v_{C_t} exhibits resonant peaking at frequencies below ω_{res} . Given the open-loop voltage control nature of this work, the error induced by this resonance made the buffer unable to perfectly cancel the harmonics generated by the inverter. The desired duty cycle generated by (8.2) is attenuated by a factor Λ (labeled SSBPD in Fig. 8.6) according to the gain of the transfer function:

$$\Lambda = \sqrt{(1 - \omega^2 L_f C_f)^2 + (\omega R C_f)^2}. \quad (8.3)$$

The block diagram of the implemented control signal chain is shown in Fig. 8.6.

The 18kHz component of the inverter input current $i_{inv,R}$ was generated via a Fourier Transform. By adjusting the amplitude of a sine and cosine at 18kHz and summing these

Table 8.1: Circuit Parameters

Component	Description
C_f	$0.1 \mu\text{F}$
L_f	$5 \mu\text{H}$
C_t	$10 \mu\text{F}$
$C_{\text{in},F}$	$200 \mu\text{F}$
$C_{\text{in},R}$	$373.89 \mu\text{F}$
L_b	$15 \mu\text{H}$
L_{in}	300 nH
R_{in}	$0.5 \text{ m}\Omega$
$f_{\text{sw},\text{inv}}$	15 kHz
$f_{\text{sw},\text{SSB}}$	500 kHz

quadrature components, a signal with the desired gain and phase was generated. This signal was then further phase shifted by 270° (180° to account for the phase shift from v_{C_f} to v_{C_t} and 90° from v_{C_t} to i_{C_t}) to generate the desired SSB full bridge voltage. Future work should utilize feedforward knowledge of the inverter input current (e.g., as derived from [132] or [134]) to eliminate this requirement of sensing i_{inv} and taking its Fourier transform in a real time fashion.

Finally, one last non-ideality is the limited efficiency of the SSB branch. All three capacitors in the SSB and the full bridge dissipate power even though ideally fully reactive power flows in this branch. Several works [130], [131] have demonstrated techniques to modify the full bridge modulation to compensate for this dissipated power and maintain a constant V_{SSB} . This work did not implement these loss compensation methods and simply powered the SSB full bridge with a voltage source $V_{\text{SSB}} = 50 \text{ V}$.

8.5 Results

These concepts were validated in a PLECS simulation configured according to the schematics of Fig. 8.3 and 8.5. Simulation parameters are provided in Tables 8.1. The parameters for the machine (modeled after an Emrax 348 MV) are provided in Table 8.2. Both machines are controlled externally to spin at a constant speed of 4000 RPM, corresponding to an electrical frequency of 667 Hz. The rear machine produces a constant $I_q = 300 \text{ A}$ and $I_d = 0$ while the front machine produces a constant $I_{dq} = 0 \text{ A}$. Note that as evidenced by Fig. 8.4, there is a resonance in the harnesses of the system at 18 kHz which the rear inverter will excite with the $\omega_{\text{sw}} - 3\omega_0$ sideband.

Shown in Fig. 8.7 are the relevant system voltages and currents showcasing the effectiveness of the SSB resonance suppressor. At $t = 0.25 \text{ s}$, the SSB current reference is stepped

Table 8.2: Machine Parameters

Component	Description
L_d & L_q	$180 \mu\text{H}$
R_s	$12.3 \text{ m}\Omega$
λ	0.118 Wb
Pole Pairs	10

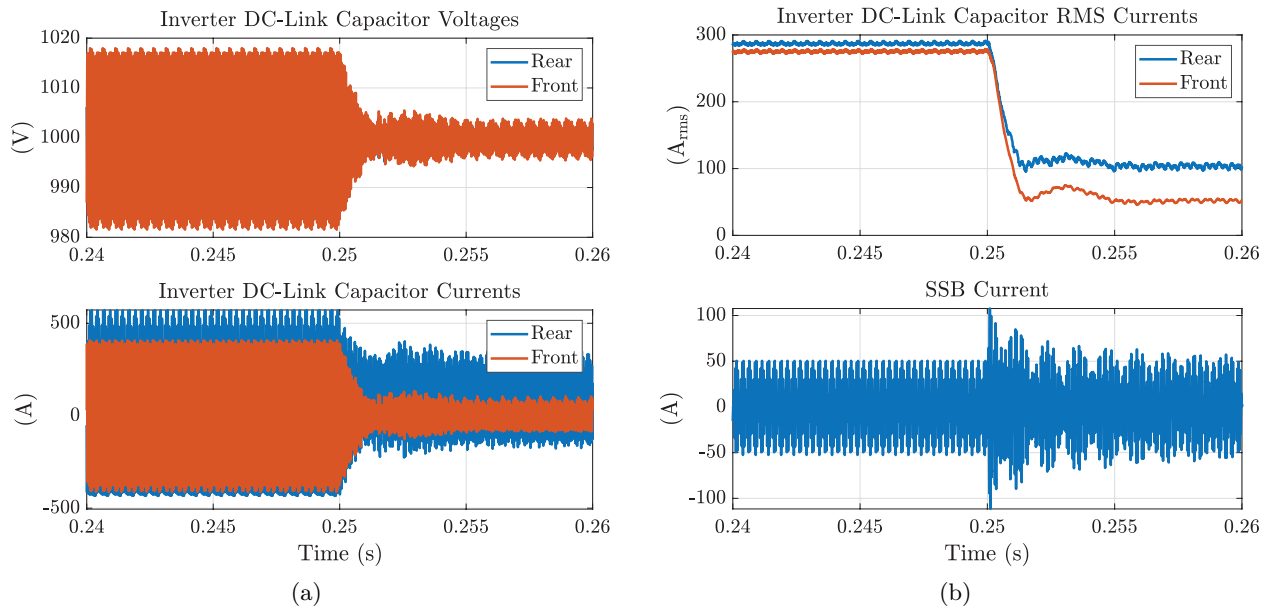


Figure 8.7: Relevant system variables in steady state operation before and after the series-stacked buffer is activated at $t = 0.25$ s. Of note is the extreme reduction in the rms currents of both inverter capacitances. The rms current of the front inverter capacitor $C_{\text{in,F}}$ reduces from $274 A_{\text{rms}}$ to $51 A_{\text{rms}}$ after the SSB is activated while the rms current of the rear inverter input capacitor $C_{\text{in,R}}$ decays from $290 A_{\text{rms}}$ to $101 A_{\text{rms}}$

from 0 to a current which is anti-phase with the 18 kHz harmonic of i_{inv} .

Before the SSB is activated, the 18 kHz system resonance is excited and both inverter capacitor voltages exhibit significant voltage ripple. Note that even though the front inverter is not producing any phase current, its capacitor is exposed to significant rms currents and voltage ripple. Fig. 8.8(a) shows a zoomed in view of relevant system parameters and high quality factor resonance can be clearly observed.

Note also the current present in the SSB branch (i.e., the current flowing through v_{C_t}). Since the SSB is directly in parallel with the main inverter dc-link capacitance, it also is exposed to the parallel resonance of the system despite the fact that $C_t || C_f \ll C_{\text{in,R}}$.

After the SSB is activated, the $i_{\text{inv,R}}$ harmonic which excited the system resonance is cancelled and the resonance is significantly suppressed. Fig. 8.7 shows how both the peak-

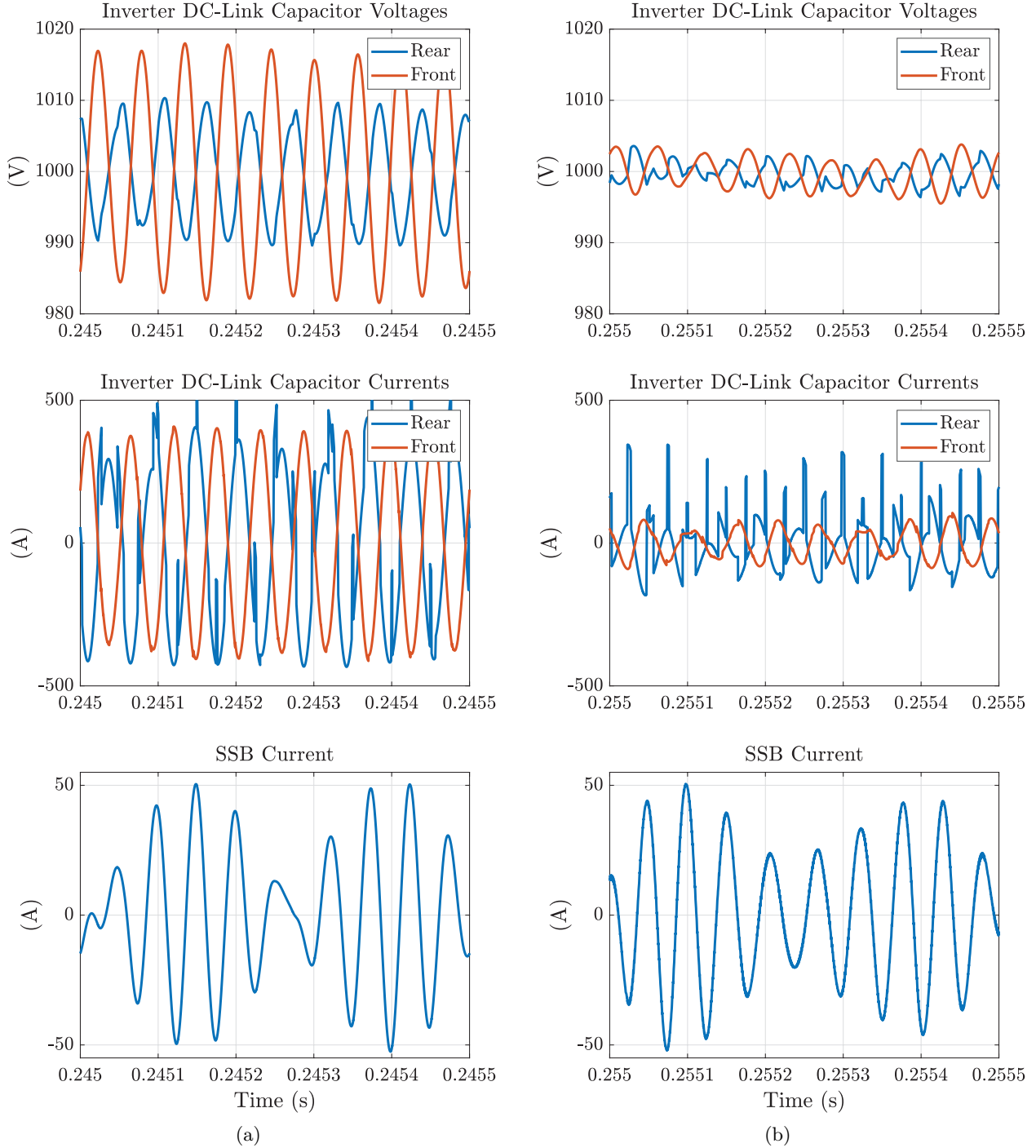


Figure 8.8: Zoomed in view of system variables (a) before and (b) after the SSB is activated. Note the relatively high quality factor resonance observable in the oscillation of the two inverter input capacitances.

to-peak voltages and rms currents of *both* inverter capacitors are significantly reduced due to the resonance suppression. Interestingly, the SSB current magnitude does not increase

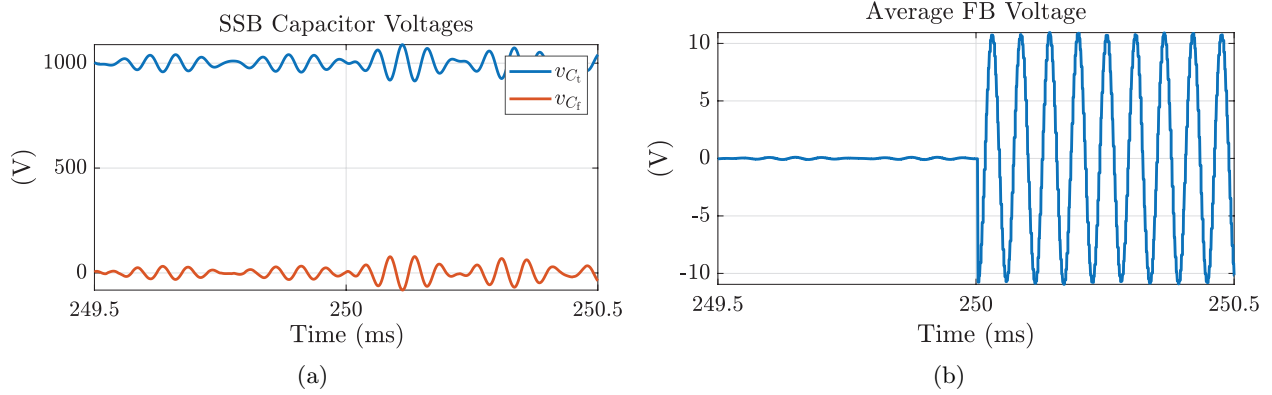


Figure 8.9: Relevant voltages within the series-stacked buffer. At $t = 250$ ms, the series-stacked buffer reference current is stepped from zero to the desired value. As a result, the average of the full-bridge switch-node voltage begins oscillating at the desired frequency.

drastically after the controller is enabled.

The magnitude of the SSB current i_{filter} is nearly matched to the 18 kHz harmonic of $i_{\text{inv,R}}$ at 30.6 A_{pk}. Given that $V_{\text{SSB}} = 50$ V, this implies the apparent processed by the SSB power converter is around 1 kW. This relatively small magnitude of power is impressive given the machine is outputting a mechanical power of 219 kW, indicated the merit of partial power processing is being fulfilled. Additionally, another practical benefit of mitigating the system resonance is the reduction in capacitor and harness losses. After the SSB is activated, the rms current of the front inverter capacitor $C_{\text{in,F}}$ reduces from 274 A_{rms} to 51 A_{rms} while the rms current of the rear inverter input capacitor $C_{\text{in,R}}$ decays from 290 A_{rms} to 101 A_{rms}. These rms current reductions are coupled to reduction in capacitor losses and conduction losses in the harnesses.

Fig. 8.9 shows the voltages within the SSB before and after the filter controller is enabled. Even though the full bridge voltage before $t = 250$ ms is approximately zero, both C_t and C_f oscillate as they participate in the system resonance. Note also the multi-tone nature of the harmonics generated by the inverter as predicted by the Fourier decomposition of i_{inv} . After the controller is activated, the average full bridge voltage takes on the desired sinusoidal characteristic and the SSB begins to draw the desired current from the dc bus and cancel the harmonics of $i_{\text{inv,R}}$.

8.6 Chapter Remarks

This chapter analyzed the Fourier decomposition of the input current of a three-phase inverter and the adverse impacts these currents can have on multi-drive vehicles. It was identified resonances between the inverter input capacitances and harness inductances can be excited by harmonics of the inverter input current. Although these resonances may be able to be suppressed through passive means (alternative harness or input capacitor selec-

tion), this work investigated the use of active filters to suppress resonances regardless of the design of the dc-bus network. The series-stacked buffer architecture was explored due to its benefits of partial power processing, large control bandwidth, and utilization of low voltage switches. Through appropriate control, the series-stacked buffer based active filter was able to effectively suppress system resonances in a realistic electric vehicle model. Future work includes utilizing feed-forward information derived from the inverter operating point to inform the SSB reference current, a more detailed design analysis for selecting SSB parameters (e.g., L_f , C_f , $f_{sw,SSB}$, etc.), and volume and efficiency estimates of the SSB versus a system without an active filter.

Chapter 9

Summary and Conclusions

9.1 Thesis Summary

This thesis investigated several key aspects relating to the dynamics and control of the flying capacitor multilevel (FCML) converter. Knowledge of the flying capacitor voltage dynamics and the ability to control these voltages are key roadblocks inhibiting industrial FCML converter adoption.

Chapter 2 investigated the impact of the switch output capacitance C_{oss} on the dynamics of the flying capacitor voltages. The hard-switched charge flow through the C_{oss} induced during switch commutation events acts to distribute charge between the flying capacitors within the FCML converter. Additionally, this C_{oss} -induced charge flow was found to have a negative-feedback effect where flying capacitor voltage imbalance induces higher quantities of charge flow through the C_{oss} to aid in the balancing of the flying capacitor voltages. The C_{oss} -induced charge flow has heightened significance at operating points of the FCML converter where traditional natural flying capacitor voltage balancing models are unable to predict the flying capacitor voltage distribution.

Chapters 3 and 4 investigated a rectifier architecture for step-down grid-tied applications, a buck-type PFC architecture. This architecture has the potential to significantly improve system efficiency and power density by performing the power conversion task in a single stage rather than two cascaded power conversion stages. To utilize the FCML converter within such an architecture, the flying capacitor voltages must track fractions of the rectified grid voltage to maintain flying capacitor voltage balance and minimization of switch voltage stress. Chapter 3 detailed a control structure to actively control the flying capacitor voltages and the inductor current to mitigate switch voltage stress and attain high power factor input current.

Chapter 4 investigated a topological variant of the converter investigated in Chapter 3, the input inductor FCML buck-type PFC converter to further improve converter performance. The input inductor topology beneficially has an input current shaped by an inductor current rather than the switched current present in the output inductor topology of Chapter 3. The

converter dynamics are very similar to that of the output inductor buck-type FCML PFC and a similar active flying capacitor voltage balancer and inductor current controller were developed. The resulting hardware prototype achieved a power density approximately double and a loss approximately half that of high-performance two-stage prototypes.

Chapter 5 discussed an application extension of the buck-type rectifiers of Chapters 3 and 4, a solar panel micro-inverter. The buck-boost converter investigated in this chapter enables an increase in grid current quality due to continuous modulation of the converter and grid current. The impact of the reactive power consumption of the flying and output capacitors on the inductor current reference and apparent power processed was analyzed, architecture providing insight into the efficiency penalty to be paid by processing significant reactive energy through the converter.

Chapter 6 explored several practical considerations involved with creating a high performance three-phase FCML rectifier. The large flying capacitor voltage ripple in the converter enabled a high density converter realization. However, these large voltage ripples create increased steady-state flying capacitor voltage imbalance and lower-order harmonics in the switch node voltage which must be attenuated by the grid-side conducted EMI filter.

Chapter 7 investigated a capacitively-isolated dc/dc converter utilizing an FCML converter to achieve a large step-down ratio. The FCML bridge leg reduces the voltage amplitude applied to the series resonant tank in the converter, achieving the majority of the step-down ratio required of the application. Notably, by operating the series resonant tank above its resonance frequency, where the effective switch node frequency f_{eff} is larger than the tank resonant frequency f_0 , the inductive tank impedance creates an inductive current which is able to soft switch all six transistors within the four-level FCML bridge leg.

Chapter 8 discussed active EMI filter structures for multi-motor electric drive systems. To avoid exciting system resonances, a series-stacked-buffer [2] placed in shunt with one of the motor drive inverters actively injects harmonic currents anti-phase with the drive inverter. As the drive inverter current harmonics change in both amplitude and frequency across the vehicle drive cycle, the active filter can significantly outperform passive filtering circuits. The series-stacked-buffer architecture reduces both the energy penalty and voltage stress of the active filter by utilizing low voltage semiconductor switches.

The appendices include captures of the software and firmware developed in this work along with schematics and layout captures of the implemented hardware prototypes.

9.2 Recommendations for Future Work

9.2.1 Quantification of FCML Flying Capacitor Imbalance

The switch output capacitance C_{oss} within an FCML converter aids flying capacitor voltage balance in a lossy manner. Therefore, attempts to add external capacitors in parallel with the semiconductor switches to try and enforce flying capacitor voltage balance will likely not be a high performance solution as converter efficiency would suffer. Determining “how much” C_{oss}

is necessary in the presence of other mechanisms which work to drive the flying capacitors to a state of imbalance is an interesting avenue for future research. For example, given some knowledge on the gate driver skew, input capacitor voltage ripple, or switch resistance asymmetry, several key mechanisms known to create flying capacitor voltage imbalance [16], how much C_{oss} would be sufficient to counteract these mechanisms and achieve a tolerable flying capacitor voltage distribution?

9.2.2 Startup, Shutdown, and Fault Handling for FCML Buck-Type PFCs.

The buck-type PFC converters investigated in Chapters 3 and 4 were tested in a relatively well-controlled laboratory environment with ac power supplies creating the grid voltage. Practical considerations on how to execute both the startup and shutdown of the converter in the buck-type PFC application is an intriguing area of future research.

Previous work [6], [135] has investigated and implemented both start up and shut down circuits for an FCML converter operating as a dc/dc converter in a battery-connected system with stringent shutdown time requirements. The buck-type PFC converter, in comparison, must charge and discharge the input and flying capacitors significantly across each line cycle.

9.2.3 Input Inductor Current Ripple Steering and Capacitor Voltage Ripple

As discussed by in [136], the inductors within a Ćuk converter can be coupled to “steer” the input or output current ripple to the other port, resulting in zero switching ripple being present at the port. This ripple steering property is achieved due to the coupled magnetic structure leveraging the voltage applied to its windings. The Ćuk topology enforces switched inductor winding voltages which are equivalent, assuming the converter has a negligible coupling capacitor voltage ripple. The input inductor topology is a member of the same switching cell family as the Ćuk converter as [64] discussed and also enforces equal switched inductor voltages.

To recap the findings from [136], current ripple steering is able to be achieved if the coupling coefficient (or equivalently, the magnetic circuit model parameters) of the coupled inductor in the Ćuk converter is chosen correctly. Referring to the magnetic circuit model of Fig. 9.1 if both ports of the transformer have the same (switched) voltages across them, and if the leakage inductance of one port is designed to be zero (shown in Fig. 9.1 (b)), the leakage inductance of the other port will have zero switching voltages across it, zero di/dt and thus no switching current ripple.

The circuit model shown in Fig. 9.1 (b) is equivalent to the following inductance matrix

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_M \\ L_M & L_M \end{bmatrix}. \quad (9.1)$$

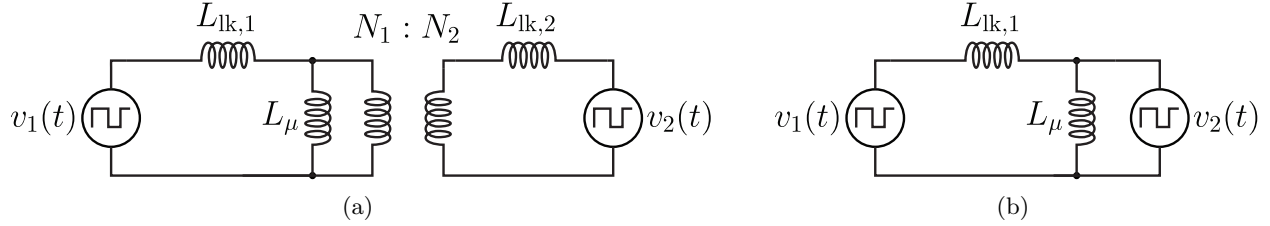


Figure 9.1: (a) T-model of an arbitrary coupled magnetic structure. If N_1 and N_2 are chosen to be the physical number of turns of each winding, the model has three-independent parameters $L_{lk,1}$, $L_{lk,2}$, and L_μ to model an inductance matrix $\mathbf{L}$. (b) Equivalent circuit if $L_{lk,2}$ is designed to be 0 and there are identical numbers of turns on both windings.

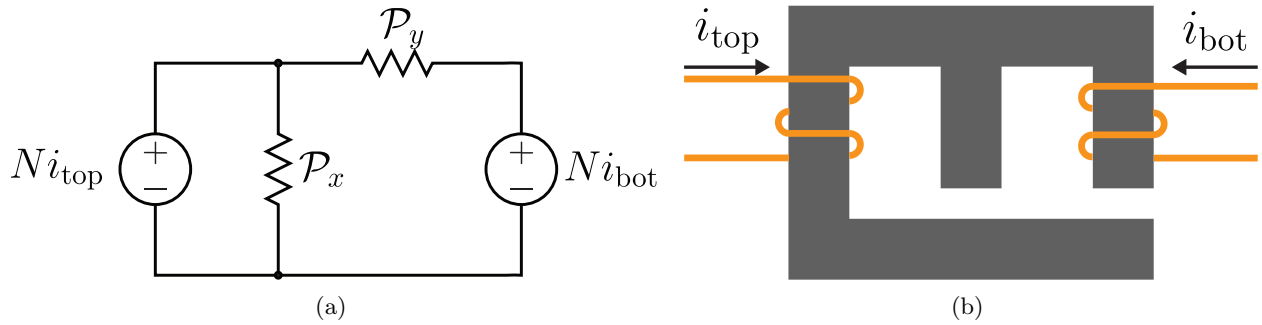


Figure 9.2: (a) Magnetic circuit model which achieves the desired inductance matrix description expressed in (9.2). Magnetic permeances $\mathcal{P}_x$ and $\mathcal{P}_y$ (the inverse of reluctances $\mathcal{R}_x$ and $\mathcal{R}_y$) can be chosen to achieve desired current ripple and input capacitor voltage ripple suppression. (b) Magnetic structure which achieves the desired magnetic circuit model shown in (a).

One realization of this inductance matrix is provided in Fig. 9.2(a). The inductance matrix for this structure can be derived as

$$\mathbf{L} = N^2 \begin{bmatrix} \mathcal{P}_x & \mathcal{P}_y \\ \mathcal{P}_y & \mathcal{P}_y \end{bmatrix}. \quad (9.2)$$

Fig. 9.2(b) shows an example magnetic structure realization which achieves the magnetic circuit model of Fig. 9.2(a). The gaps of the two legs can be adjusted to achieve desired permeances $\mathcal{P}_x$ and $\mathcal{P}_y$.

The analysis justifying the ripple steering investigated in [136] works well when the capacitor voltage ripple is relatively minor, a difficult requirement to achieve in a buck-type PFC application. That is, the voltage ripple on the (floating) input capacitor in the input inductor topology causes the instantaneous winding voltages to deviate. For the buck-type PFC application, it is difficult to suppress this voltage ripple to arbitrarily small values for several reasons. First, the capacitor ripple is at the switching frequency f_{sw} rather than the effective switching frequency $(N - 1)f_{sw}$, implying the capacitor is unable to access the frequency multiplication properties of the FCML converter. Second, the input capacitance cannot be grown excessively large as the input capacitor must track $V_{pk}|\sin(\omega t)|$ where V_{pk} is the peak of the grid voltage. Larger choices of C_F result in larger reactive power flow and

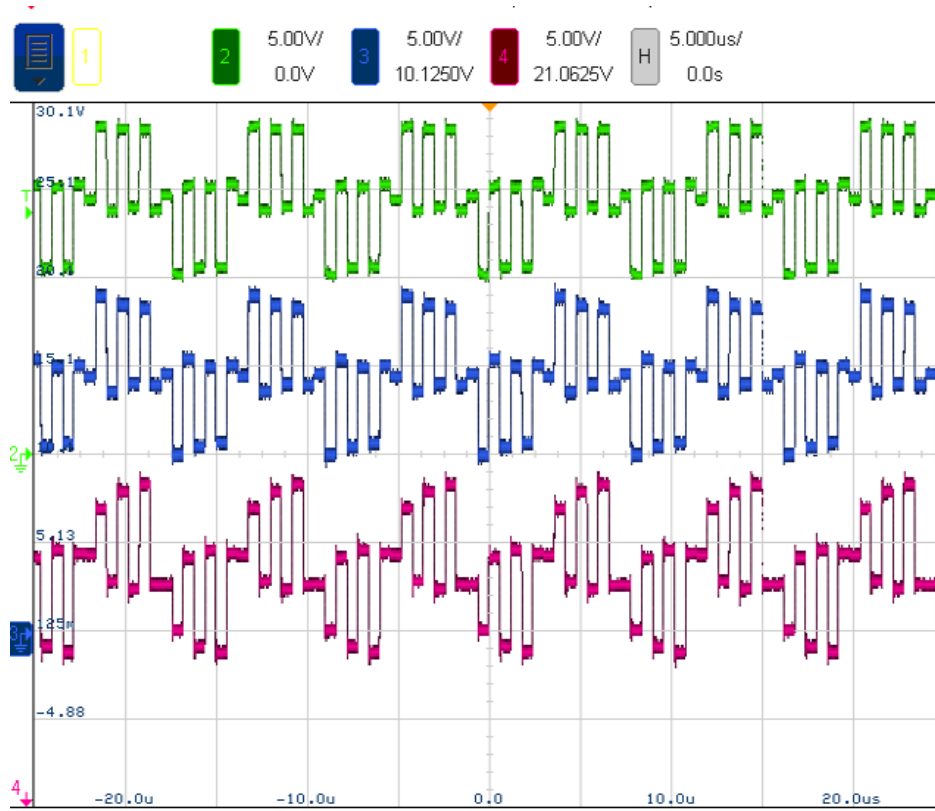


Figure 9.3: Measured switch node voltages of the three-phase FCML prototype of Chapter 6 during a fault condition. One of the 42 transistors in the hardware prototype failed short. Due to the grid-side filter configuration, this transistor failure causes flying capacitor voltage imbalance in all three phases.

a larger apparent power processed by the converter, similar to the impact investigated in Chapter 5. Thus there is much potential for investigation on the tradeoffs and impact of the coupled inductor approach given these capacitor ripple constraints.

9.2.4 Three-Phase FCML Converter Flying Capacitor Ripple and EMI Filter

Chapter 6 investigated the EMI filter implications of a three-phase FCML converter operated with significant flying capacitor voltage ripple and center-alignment of the switch node voltage pulses. This latter property enabled a significant reduction in inductor current filtering effort as the inductor current ripple frequency is further doubled to $2(N - 1)f_{sw}$ compared to a single-phase ac/dc or dc/dc FCML. This benefit, however, is achieved as the neutral point of the filter capacitors is floating (i.e., not referenced to either the positive or negative pole of the dc bus). This floating filter structure couples the three FCML phases together in a way that three single-phase FCML rectifiers with dc bus referenced grid-side filters would not.

Explicit investigation of the reliability/performance benefits of this filter structure should be investigated. For example, if one of the switches in one of the FCML undergoes a failure, all three phases will be subjected to flying capacitor voltage imbalance and potential cascading failures. Fig. 9.3 shows the measured switch node voltages for the prototype discussed in Chapter 6 during a fault condition. As a result of one of the switches within one of the phases having its drain-source terminals shorted, the flying capacitor voltages in all three phases are unable to balance. This propagation of switch failure does not occur in filter structures with the EMI filter referenced to the dc bus as this reference point decouples the separate phases.

Finally, the converter developed in Chapter 6 utilized significant flying capacitor voltage ripple to improve the converter power density. Although the increased capacitor voltage ripple improves the transient speed of natural flying capacitor voltage balancing, it compromises the steady-state flying capacitor voltage distribution. Quantification of the imbalance mechanisms and magnitude associated with increased flying capacitor voltage ripple is an interesting area of future investigation.

9.2.5 Micro-Inverter Optimization and Control

Alternative control architectures and auxiliary circuitry for the FCML-based micro-inverter presented in Chapter 5 remain an open area of investigation. In addition to the startup and shutdown challenges faced by the buck-type PFC of Chapters 3 and 4, the micro-inverter must also operate during nighttime or low-light conditions where the dc bus voltage can not necessarily be relied upon. Circuits and controllers which are able to maintain flying capacitor voltage balance and/or minimize switch voltage stress during these operating conditions will be critical.

Chapter 5 presented a feedforward based approach for deriving the inductor current reference where the desired power drawn from the dc source and the quiescent operating point informed the inductor current reference. As a result, the grid current is not strictly controlled. A feedback based approach where the grid current is sensed and a feedback controller (in conjunction with other controllers) sets the inductor current reference could be utilized instead. A grid current feedback-based approach was pursued for the buck-type inverter demonstrated in [78], [79] where the grid current controller sets the output capacitor voltage reference and the output capacitor voltage controller sets the inductor current reference. This approach comes with complexity of stabilizing multiple nested control loops with a relatively small frequency separation between the different loops. However, in the presence of necessary EMI filters in series with the buck-boost converter and the grid, impacting the inductor current to grid current dynamics, such a grid current controller may be necessary.

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Appendix A

MATLAB Code for Simulating C_{oss}

```

1  clearvars
2  colormap_MAT = get(gca,'ColorOrder');
3
4  %% Simulate 5 Level D = 0.5
5  L_o = 10e-6; %output filter inductance [H]
6  R_L = 34e-3+1.8e-3*11+4e-3; %resistance lumped into inductor [Ohms] Inductor DCR + 4
   ↪ switching FETs + 7 always on FETs + current sense resistors
7  R_L = R_L*6 ;
8  C_o = 20*2.2e-6; %Output capacitance
9  f_sw = 120e3;%switching frequency [Hz]
10 T = 1/f_sw; %period [s]
11 C_1 = 4*2.2e-6; %Fly cap capacitance [F]
12 C_2 = C_1;
13 C_3 = C_1;
14
15 Li = 1e-6; %Input impedance inductance [H]
16 RLi = 0.1; %Input impedance resistance [Ohms]
17 Ci = 30e-7; %Input capacitance [F]
18 C_oss = 3.5e-9;
19 R_o = 1; %Output resistance [Ohms]
20 sim_time = 50e-3;
21 num_iter = floor(sim_time/T*4); %number of iterations of a (fundamental) switching
   ↪ period
22 state_time = .25*T; %Time spent in each switching state
23 time_stamps = state_time*1e3*(0:num_iter-1); %time indices [ms]
24
25 x(:,1) = [zeros(4,1);30;60;0];
26 x2(:,1) = [zeros(4,1);30;60;0];
27
28 coss_tracker = [0;0;0];
29
30 %Leading carrier A matrices
31 A_S1 = [zeros(1,3),-1/C_1,zeros(1,3);zeros(1,7);zeros(1,3),1/C_3,zeros(1,3);1/L_o,0,-1/
   ↪ L_o,-R_L/L_o,-1/L_o,1/L_o,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,3),-1/Ci,0,0,
   ↪ 1/Ci;zeros(1,5),-1/Li,-RLi/Li];

```

```

32 A_S2 = [zeros(1,7);zeros(1,3),1/C_2,zeros(1,3);zeros(1,7);0,-1/L_o,0,-R_L/L_o,-1/L_o,1/
↪ L_o,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,3),-1/C_i,0,0,1/C_i;zeros(1,5),-1/Li,
↪ -RLi/Li];
33 A_S3 = [zeros(1,3),1/C_1,zeros(1,3);zeros(1,7);zeros(1,3),-1/C_3,zeros(1,3);-1/L_o,0,1/
↪ L_o,-R_L/L_o,-1/L_o,0,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/C_i;zeros(1,5)
↪ ),-1/Li,-RLi/Li];
34 A_S4 = [zeros(1,7);zeros(1,3),-1/C_2,zeros(1,3);zeros(1,7);0,1/L_o,0,-R_L/L_o,-1/L_o,0,
↪ 0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/C_i;zeros(1,5),-1/Li,-RLi/Li];
35 %Lagging carrier A matrices
36 % A_S1 = [zeros(1,3),-1/C_1,0;zeros(1,5);zeros(1,3),1/C_3,0;1/L_o,0,-1/L_o,-R_L/L_o,-1/
↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
37 % A_S2 = [zeros(1,5);zeros(1,3),-1/C_2,0;zeros(1,5);0,1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
↪ ),1/C_o,-1/(R_o*C_o)];
38 % A_S3 = [zeros(1,3),1/C_1,0;zeros(1,5);zeros(1,3),-1/C_3,0;-1/L_o,0,1/L_o,-R_L/L_o,-1/
↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
39 % A_S4 = [zeros(1,5);zeros(1,3),1/C_2,0;zeros(1,5);0,-1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
↪ ),1/C_o,-1/(R_o*C_o)];
40
41 AS1_matexp = expm(A_S1*state_time);
42 AS1_int = integral(@(t) expm(A_S1.*(t)),0,state_time, 'ArrayValued', true);
43 AS2_matexp = expm(A_S2*state_time);
44 AS2_int = integral(@(t) expm(A_S2.*(t)),0,state_time, 'ArrayValued', true);
45 AS3_matexp = expm(A_S3*state_time);
46 AS3_int = integral(@(t) expm(A_S3.*(t)),0,state_time, 'ArrayValued', true);
47 AS4_matexp = expm(A_S4*state_time);
48 AS4_int = integral(@(t) expm(A_S4.*(t)),0,state_time, 'ArrayValued', true);
49 %Leading carrier B matrices
50 B_S1 = [zeros(6,1);1/Li];
51 B_S2 = [zeros(6,1);1/Li];
52 B_S3 = [zeros(6,1);1/Li];
53 B_S4 = [zeros(6,1);1/Li];
54 %Lagging carrier B matrices
55 % B_S1 = [zeros(3,1);1/L_o;0];
56 % B_S4 = [zeros(3,1);1/L_o;0];
57
58 i = 2:num_iter;
59 V_in = [5,max(5,5+25*(1-exp(-(i-500)/454.5)))]];
60
61 for i = 1:4:num_iter-4
62     % Leading carrier arrangement
63     % x(:,i) = [x(1,i)*C_1/(C_1+C_oss);x(2,i)+C_3*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(x(3,i)
↪ )-x(2,i));x(3,i)+C_2*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(x(2,i)-x(3,i));x(4:5,i)];
↪ %Lagging carrier q3 turns off q1 turns on
64     coss_tracker(:,i) = x(1:3,i);
65     x(:,i) = [x(1,i)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i)-x(1,i));x(2,i)+C_1*C_o
↪ ss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i)-x(2,i));C_3/(C_3+C_oss)*(x(3,i)+C_oss/C_3*
↪ V_in(i));x(4:7,i)]; %leading carrier q2 turns off q4 turns on, leading carrier
66     coss_tracker(:,i) = x(1:3,i)-coss_tracker(:,i);
67     if(x(1,i)<-2) %Diode clamp lowest capacitor voltage
68         x(1,i) = -2;

```

```

69     end
70     if(x(2,i)-x(3,i)>2) %Diode clamp middle cell
71 %       x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
72       x(2,i) = (C_2*(x(2,i)-2) + C_3*x(3,i))/(C_2+C_3) + 2; %N. Brooks clamping
       ⇨ equaiton
73       x(3,i) = x(2,i)-2;
74     end
75
76     x(:,i+1) = AS1_matexp*x(:,i)+AS1_int*B_S1*V_in(i);
77
78     if(x(1,i+1)<-2) %Diode clamp lowest capacitor voltage
79       x(1,i+1) = -2;
80     end
81     if(x(2,i+1)-x(3,i+1)>2) %Diode clamp middle cell
82 %       x(2,i+1) = (C_2*x(2,i+1)+C_3*(x(3,i+1)+2))/(C_2+C_3);
83       x(2,i+1) = (C_2*(x(2,i+1)-2) + C_3*x(3,i+1))/(C_2+C_3) + 2; %N. Brooks clamping
       ⇨ equaiton
84       x(3,i+1) = x(2,i+1)-2;
85     end
86
87 %   x(:,i+1) = [x(1,i+1)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+1)-x(1,i+1));x(2,i+
⇨ 1)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+1)-x(2,i+1));C_3/(C_3+C_oss)*(x(3,i+1
⇨ )+C_oss/C_3*V_in(i+1));x(4:5,i+1)]; %Lagging carrier q4 turns off q2 turns on
88     coss_tracker(:,i+1) = x(1:3,i+1);
89     x(:,i+1) = [x(1,i+1)*C_1/(C_1+C_oss);x(2,i+1)+C_3*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(
⇨ x(3,i+1)-x(2,i+1));x(3,i+1)+C_2*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(x(2,i+1)-x(3,i
⇨ +1));x(4:7,i+1)]; %Leading carrier q1 turns off q3 turns on
90     coss_tracker(:,i+1) = x(1:3,i+1)-coss_tracker(:,i+1);
91
92     x(:,i+2) = AS2_matexp*x(:,i+1)+AS2_int*B_S2*V_in(i+1); %include integral for leading
⇨ carrier, exclude for lagging carrier
93
94     if(x(1,i+2)<-2) %Diode clamp lowest capacitor voltage
95       x(1,i+2) = -2;
96     end
97     if(x(2,i+2)-x(3,i+2)>2) %Diode clamp middle cell
98 %       x(2,i+2) = (C_2*x(2,i+2)+C_3*(x(3,i+2)+2))/(C_2+C_3);
99       x(2,i+2) = (C_2*(x(2,i+2)-2) + C_3*x(3,i+2))/(C_2+C_3) + 2; %N. Brooks clamping
       ⇨ equaiton
100       x(3,i+2) = x(2,i+2)-2;
101     end
102     coss_tracker(:,i+2) = x(1:3,i+2);
103 %   x(:,i+2) = [x(1,i+2)*C_1/(C_1+C_oss);x(2,i+2)+C_3*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*
⇨ (x(3,i+2)-x(2,i+2));x(3,i+2)+C_2*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(x(2,i+2)-x(3,i+2)
⇨ );x(4:5,i+2)]; %Lagging carrier q1 turns off q3 turns on
104     x(:,i+2) = [x(1,i+2)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+2)-x(1,i+2));x(2,i+
⇨ 2)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+2)-x(2,i+2));C_3/(C_3+C_oss)*(x(3
⇨ ,i+2)+C_oss/C_3*V_in(i+2));x(4:7,i+2)]; %Leading carrier q4 turns off q2 turns
⇨ on
105     coss_tracker(:,i+2) = x(1:3,i+2)-coss_tracker(1:3,i+2);

```

```

106 x(:,i+3) = AS3_matexp*x(:,i+2)+AS3_int*B_S3*V_in(i+2);
107
108 if(x(1,i+3)<-2) %Diode clamp lowest capacitor voltage
109     x(1,i+3) = -2;
110 end
111 if(x(2,i+3)-x(3,i+3)>2) %Diode clamp middle cell
112 %     x(2,i+3) = (C_2*x(2,i+3)+C_3*(x(3,i+3)+2))/(C_2+C_3);
113 x(2,i+3) = (C_2*(x(2,i+3)-2) + C_3*x(3,i+3))/(C_2+C_3) + 2; %N. Brooks clamping
    ↪ equaiton
114 x(3,i+3) = x(2,i+3)-2;
115 end
116
117 coss_tracker(:,i+3) = x(1:3,i+3);
118 % x(:,i+3) = [x(1,i+3)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+3)-x(1,i+3));x(2,i+
    ↪ 3)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+3)-x(2,i+3));C_3/(C_3+C_oss)*(x(3,i+
    ↪ 3)+C_oss/C_3*V_in(i+3));x(4:5,i+3)]; %Lagging carrier q2 turns off q4 turns on
119 x(:,i+3) = [x(1,i+3)*C_1/(C_1+C_oss);x(2,i+3)+C_3*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(
    ↪ x(3,i+3)-x(2,i+3));x(3,i+3)+C_2*C_oss/(C_3*C_2+C_oss*(C_3+C_2))*(x(2,i+3)-x(3,i+
    ↪ 3));x(4:7,i+3)]; %Leading carrier q3 turns off q1 turns onx_t_3_n =
    ↪ AS3_matexp*x_t_2_p;
120 coss_tracker(:,i+3) = x(1:3,i+3)-coss_tracker(:,i+3);
121 x(:,i+4) = AS4_matexp*x(:,i+3)+AS4_int*B_S4*V_in(i+3);
122 if(x(1,i+4)<-2) %Diode clamp lowest capacitor voltage
123     x(1,i+4) = -2;
124 end
125 if(x(2,i+4)-x(3,i+4)>2) %Diode clamp middle cell
126 %     x(2,i+4) = (C_2*x(2,i+4)+C_3*(x(3,i+4)+2))/(C_2+C_3);
127 x(2,i+4) = (C_2*(x(2,i+4)-2) + C_3*x(3,i+4))/(C_2+C_3) + 2; %N. Brooks clamping
    ↪ equaiton
128 x(3,i+4) = x(2,i+4)-2;
129 end
130
131 x2(:,i+1) = AS1_matexp*x2(:,i)+AS1_int*B_S1*V_in(i);
132
133 if(x2(1,i+1)<-2)
134     x2(1,i+1) = -2;
135 end
136
137 x2(:,i+2) = AS2_matexp*x2(:,i+1)+AS2_int*B_S2*V_in(i+1);
138
139 if(x2(1,i+2)<-2)
140     x2(1,i+2) = -2;
141 end
142 x2(:,i+3) = AS3_matexp*x2(:,i+2)+AS3_int*B_S3*V_in(i+2);
143 if(x2(1,i+3)<-2)
144     x2(1,i+3) = -2;
145 end
146 x2(:,i+4) = AS4_matexp*x2(:,i+3)+AS4_int*B_S4*V_in(i+3);
147 if(x2(1,4)<-2)
148     x2(1,4) = -2;

```

```

149     end
150     if(mod(i-1,5000)==0)
151         fprintf('Iteration Number %d/%d\r\n',i,num_iter)
152         fprintf('Simulation Time %.2f [ms]\r\n',1e3*i*T/4)
153     end
154 end
155
156 time_stamps = time_stamps(1:size(x,2));
157 V_in = V_in(1:length(time_stamps));
158
159 coss_tracker_filt(1,:) = filter(1/4*ones(1,4),1,cooss_tracker(1,:));
160 coss_tracker_filt(2,:) = filter(1/4*ones(1,4),1,cooss_tracker(2,:));
161 coss_tracker_filt(3,:) = filter(1/4*ones(1,4),1,cooss_tracker(3,:));
162 disp('Done Simulating D = 0.5 Leading Carrier Arrangement')
163
164 x_5 = x;
165 x2_5 = x2;
166 %% Plot D = 0.5
167
168 figure(1)
169
170 plot(time_stamps,V_in,'color',hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth',1)
171 hold on
172 plot(time_stamps,x(1,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth',1)%,'Li
    ↪ neStyle','--','Color','#D95319')
173 plot(time_stamps,x(2,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth',1)
174 plot(time_stamps,x(3,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth',1)
175 hold off
176 % legend('Experiment  $V_L \text{ } \textit{v}_{in}$ ', 'Experiment  $V_L \text{ } \textit{v}_{c1}$ ', 'Experiment
    ↪  $V_L \text{ } \textit{v}_{c2}$ ', 'Experiment  $V_L \text{ } \textit{v}_{c3}$ ', 'MATLAB  $V_L \text{ } \textit{v}_{in}$ ', 'MATLAB
    ↪  $v_{c1}$ ', 'MATLAB  $v_{c2}$ ', 'MATLAB  $v_{c3}$ ')
177 grid on
178 xlabel('Time [ms]')
179 ylabel('Voltages [V]')
180 set(gcf, 'Renderer', 'painters');
181 legend('$V_{in}$','$v_{c1}$','$v_{c2}$','$v_{c3}$')
182 title('D = 0.5 With  $C_{oss}$ ')
183 xlim([0 50])
184
185
186 set_figure_style(2)
187 figure(2)
188 plot(time_stamps,V_in,'color',hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth',1)
189 hold on
190 plot(time_stamps,x2(1,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth',1)
191 plot(time_stamps,x2(2,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth',1)
192 plot(time_stamps,x2(3,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth',1)
193 hold off
194 grid on
195 xlabel('Time [ms]')

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```

196 set(gcf, 'Renderer', 'painters');
197 legend('$$V_{in}$$', '$$v_{c1}$$', '$$v_{c2}$$', '$$v_{c3}$$')
198 title('D=0.5 Without $$C_{oss}$$')
199 set_figure_style(2)
200
201 time_stamps_Coss = time_stamps(1:length(coss_tracker));
202 figure(3)
203 subplot(3,1,1)
204 plot(time_stamps_Coss, coss_tracker_filt(1,:)*1e3)
205 ylabel(' [mV] ')
206 grid on
207 title('$$v_{c1}$$ Voltage Change due to $$C_{oss}$$')%, 'Moving Average Filtered')
208 subplot(3,1,2)
209 plot(time_stamps_Coss, coss_tracker_filt(2,:)*1e3)
210 grid on
211 ylabel(' [mV] ')
212 title('$$v_{c2}$$ Voltage Change due to $$C_{oss}$$')%, 'Moving Average Filtered')
213 subplot(3,1,3)
214 plot(time_stamps_Coss, coss_tracker_filt(3,:)*1e3)
215 grid on
216 ylabel(' [mV] ')
217 xlabel('Time [ms]')
218 title('$$v_{c3}$$ Voltage Change due to $$C_{oss}$$')%, 'Moving Average Filtered')
219 set_figure_style(2)
220
221 figure(4)
222 subplot(2,1,1)
223 plot(time_stamps, x(6,:), time_stamps, x(5,:))
224 ylabel(' [V] ')
225 legend('Input Capacitor', 'Output Capacitor')
226 grid on
227 title('Cap Voltages')
228 subplot(2,1,2)
229 plot(time_stamps, x(4,:), time_stamps, x(7,:))
230 title('Inductor Currents')
231 legend('Output Current', 'Input Current')
232 grid on
233 ylabel(' [A] ')
234 xlabel('Time [ms]')
235 set_figure_style(2)
236 %% 5-Level at D = 0.251 Leading PSPWM
237 L_o = 10e-6; %output filter inductance [H]
238 R_L = 34e-3+1.8e-3*11+4e-3; %resistance lumped into inductor [Ohms] Inductor DCR + 4
    ↪ switching FETs + 7 always on FETs + current sense resistors
239 R_L = R_L*6 ;
240 C_o = 20*2.2e-6; %Output capacitance
241 f_sw = 120e3; %switching frequency [Hz]
242 T = 1/f_sw; %period [s]
243 C_1 = 5e-6; %Fly cap capacitance [F]
244 C_2 = C_1;

```



```

245 C_3 = C_1;
246
247 C_oss = 3.5e-9;
248 R_o = 2; %Output resistance [Ohms]
249
250 Li = 1e-6; %Input impedance inductance [H]
251 RLi = 0.1; %Input impedance resistance [Ohms]
252 Ci = 42.5e-6; %Input capacitance [F]
253 Qi = 1/RLi*sqrt(Li/Ci); %Input network Q
254 Zi = sqrt(Li/Ci); %Input network characteristic impedance
255
256 sim_time = 80e-3;
257 num_iter = floor(sim_time/T*8); %number of iterations of a (fundamental) switching
    ⇨ period
258 state_time_1 = T*(.251-.25); %Time spent in each switching state
259 state_time_2 = T*(.5-.251);
260 time_stamps_25 = [];
261 for i = 0:sim_time*1e5*1.2-1
262
263     time_stamps_25 = [time_stamps_25,i*T,i*T+.01*T,i*T+T/4,i*T+.251*T,i*T+T/2,i*T+.51*T]
        ⇨ ,i*T+3*T/4,i*T+.751*T];
264 end
265 time_stamps_25 = 1e3*time_stamps_25; %converter indices to ms rather than s
266 x(:,1) = [zeros(7,1)];
267 x2(:,1) = x(:,1);
268
269 coss_tracker_25 = [0;0;0];
270 %Leading carrier A matrices
271 A_S1 = [zeros(1,7);zeros(1,3),-1/C_2,zeros(1,3);zeros(1,7);0,1/L_o,0,-R_L/L_o,-1/L_o,0,]
    ⇨ 0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/Ci;zeros(1,5),-1/Li,-RLi/Li];
272 A_S2 = [zeros(1,3),-1/C_1,zeros(1,3);zeros(2,7);1/L_o,0,0,-R_L/L_o,-1/L_o,0,0;zeros(1,3)
    ⇨ ),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/Ci;zeros(1,5),-1/Li,-RLi/Li];
273 A_S3 = [zeros(1,3),-1/C_1,zeros(1,3);zeros(1,7);zeros(1,3),1/C_3,zeros(1,3);1/L_o,0,-1/
    ⇨ L_o,-R_L/L_o,-1/L_o,1/L_o,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,3),-1/Ci,0,0,]
    ⇨ 1/Ci;zeros(1,5),-1/Li,-RLi/Li];
274 A_S4 = [zeros(2,7);zeros(1,3),1/C_3,zeros(1,3);0,0,-1/L_o,-R_L/L_o,-1/L_o,1/L_o,0;zeros
    ⇨ (1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,3),-1/Ci,0,0,1/Ci;zeros(1,5),-1/Li,-RLi/Li];
275 A_S5 = [zeros(1,7);zeros(1,3),1/C_2,zeros(1,3);zeros(1,7);0,-1/L_o,0,-R_L/L_o,-1/L_o,1/
    ⇨ L_o,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,3),-1/Ci,0,1/Ci,0;zeros(1,5),-1/Li,]
    ⇨ -RLi/Li];
276 A_S6 = [zeros(1,7);zeros(1,3),1/C_2,zeros(1,3);zeros(1,3),-1/C_3,zeros(1,3);0,-1/L_o,1/
    ⇨ L_o,-R_L/L_o,-1/L_o,0,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/Ci;zeros(1,5)
    ⇨ ),-1/Li,-RLi/Li];
277 A_S7 = [zeros(1,3),1/C_1,zeros(1,3);zeros(1,7);zeros(1,3),-1/C_3,zeros(1,3);-1/L_o,0,1/
    ⇨ L_o,-R_L/L_o,-1/L_o,0,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/Ci;zeros(1,5)
    ⇨ ),-1/Li,-RLi/Li];
278 A_S8 = [zeros(1,3),1/C_1,zeros(1,3);zeros(1,3),-1/C_2,zeros(1,3);zeros(1,7);-1/L_o,1/L_
    ⇨ o,0,-R_L/L_o,-1/L_o,0,0;zeros(1,3),1/C_o,-1/(R_o*C_o),0,0;zeros(1,6),1/Ci;zeros(1,5)
    ⇨ ),-1/Li,-RLi/Li];
279 %Lagging carrier A matrices

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280 % A_S1 = [zeros(1,3),-1/C_1,0;zeros(1,5);zeros(1,3),1/C_3,0;1/L_o,0,-1/L_o,-R_L/L_o,-1/
↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
281 % A_S2 = [zeros(1,5);zeros(1,3),-1/C_2,0;zeros(1,5);0,1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
↪ ,1/C_o,-1/(R_o*C_o)];
282 % A_S3 = [zeros(1,3),1/C_1,0;zeros(1,5);zeros(1,3),-1/C_3,0;-1/L_o,0,1/L_o,-R_L/L_o,-1/
↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
283 % A_S4 = [zeros(1,5);zeros(1,3),1/C_2,0;zeros(1,5);0,-1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
↪ ,1/C_o,-1/(R_o*C_o)];
284
285 AS1_matexp = expm(A_S1*state_time_1);
286 AS1_int = integral(@(t) expm(A_S1.*(t)),0,state_time_1, 'ArrayValued', true);
287 AS2_matexp = expm(A_S2*state_time_2);
288 AS2_int = integral(@(t) expm(A_S2.*(t)),0,state_time_2, 'ArrayValued', true);
289 AS3_matexp = expm(A_S3*state_time_1);
290 AS3_int = integral(@(t) expm(A_S3.*(t)),0,state_time_1, 'ArrayValued', true);
291 AS4_matexp = expm(A_S4*state_time_2);
292 AS4_int = integral(@(t) expm(A_S4.*(t)),0,state_time_2, 'ArrayValued', true);
293 AS5_matexp = expm(A_S5*state_time_1);
294 AS5_int = integral(@(t) expm(A_S5.*(t)),0,state_time_1, 'ArrayValued', true);
295 AS6_matexp = expm(A_S6*state_time_2);
296 AS6_int = integral(@(t) expm(A_S6.*(t)),0,state_time_2, 'ArrayValued', true);
297 AS7_matexp = expm(A_S7*state_time_1);
298 AS7_int = integral(@(t) expm(A_S7.*(t)),0,state_time_1, 'ArrayValued', true);
299 AS8_matexp = expm(A_S8*state_time_2);
300 AS8_int = integral(@(t) expm(A_S8.*(t)),0,state_time_2, 'ArrayValued', true);
301 %Leading carrier B matrices
302 B = [zeros(6,1);1/Li];
303 %Lagging carrier B matrices
304 % B_S1 = [zeros(3,1);1/L_o;0];
305 % B_S4 = [zeros(3,1);1/L_o;0];
306
307 i = 2:num_iter;
308 V_in = [5,max(5,5+45*(1-exp(-(i-500)/454.5)))]];
309
310 for i = 1:8:num_iter-8
311     % Leading carrier arrangement
312     coss_tracker_25(:,i) = x(1:3,i);
313     x(:,i) = [x(1,i)*C_1/(C_1+C_oss);x(2:7,i)]; %q1 turns on, leading carrier
314     coss_tracker_25(:,i) = x(1:3,i)-coss_tracker_25(:,i);
315     if(x(1,i)<-2) %Diode clamp lowest capacitor voltage
316         x(1,i) = -2;
317     end
318     if(x(2,i)-x(3,i)>2) %Diode clamp middle cell
319 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
320         x(2,i) = (C_2*(x(2,i)-2) + C_3*x(3,i))/(C_2+C_3) + 2; %N. Brooks clamping
↪ equation
321         x(3,i) = x(2,i)-2;
322     end
323
324     x(:,i+1) = AS1_matexp*x(:,i)+AS1_int*B*V_in(i);

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325
326     if(x(1,i+1)<-2) %Diode clamp lowest capacitor voltage
327         x(1,i+1) = -2;
328     end
329     if(x(2,i+1)-x(3,i+1)>2) %Diode clamp middle cell
330 %         x(2,i+1) = (C_2*x(2,i+1)+C_3*(x(3,i+1)+2))/(C_2+C_3);
331         x(2,i+1) = (C_2*(x(2,i+1)-2) + C_3*x(3,i+1))/(C_2+C_3) + 2; %N. Brooks clamping
            ↪ equaiton
332         x(3,i+1) = x(2,i+1)-2;
333     end
334     coss_tracker_25(:,i+1) = x(1:3,i+1);
335     x(:,i+1) = [x(1,i+1)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+1)-x(1,i+1));x(2,i+1)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+1)-x(2,i+1));x(3:7,i+1)];%q2 turns
            ↪ off, leading carrier
336     coss_tracker_25(:,i+1) = x(1:3,i+1)-coss_tracker_25(:,i+1);
337     x(:,i+2) = AS2_matexp*x(:,i+1)+AS2_int*B*V_in(i+1);
338
339     if(x(1,i+2)<-2) %Diode clamp lowest capacitor voltage
340         x(1,i+2) = -2;
341     end
342     if(x(2,i+2)-x(3,i+2)>2) %Diode clamp middle cell
343 %         x(2,i+2) = (C_2*x(2,i+2)+C_3*(x(3,i+2)+2))/(C_2+C_3);
344         x(2,i+2) = (C_2*(x(2,i+2)-2) + C_3*x(3,i+2))/(C_2+C_3) + 2; %N. Brooks clamping
            ↪ equaiton
345         x(3,i+2) = x(2,i+2)-2;
346     end
347
348     coss_tracker_25(:,i+2) = x(1:3,i+2);
349     x(:,i+2) = [x(1:2,i+2);x(3,i+2)+Ci*C_oss/(Ci*C_3+C_oss*(C_3+Ci))*(x(6,i+2)-x(3,i+2));
            ↪ );x(4:5,i+2);x(6,i+2)+C_3*C_oss/(C_3+Ci+C_oss*(C_3+Ci))*(x(3,i+2)-x(6,i+2));x(7,
            ↪ i+2)];%q4 turns on
350     coss_tracker_25(:,i+2) = x(1:3,i+2)-coss_tracker_25(:,i+2);
351
352     x(:,i+3) = AS3_matexp*x(:,i+2)+AS3_int*B*V_in(i+2);
353
354     if(x(1,i+3)<-2) %Diode clamp lowest capacitor voltage
355         x(1,i+3) = -2;
356     end
357     if(x(2,i+3)-x(3,i+3)>2) %Diode clamp middle cell
358 %         x(2,i+3) = (C_2*x(2,i+3)+C_3*(x(3,i+3)+2))/(C_2+C_3);
359         x(2,i+3) = (C_2*(x(2,i+3)-2) + C_3*x(3,i+3))/(C_2+C_3) + 2; %N. Brooks clamping
            ↪ equaiton
360         x(3,i+3) = x(2,i+3)-2;
361     end
362
363     coss_tracker_25(:,i+3) = x(1:3,i+3);
364     x(:,i+3) = [x(1,i+3)*C_1/(C_1+C_oss);x(2:7,i+3)];%q1 turns off
365     coss_tracker_25(:,i+3) = x(1:3,i+3)-coss_tracker_25(:,i+3);
366
367     x(:,i+4) = AS4_matexp*x(:,i+3)+AS4_int*B*V_in(i+3);

```

```

368
369     if(x(1,i+4)<-2) %Diode clamp lowest capacitor voltage
370         x(1,i+4) = -2;
371     end
372     if(x(2,i+4)-x(3,i+4)>2) %Diode clamp middle cell
373 %         x(2,i+4) = (C_2*x(2,i+4)+C_3*(x(3,i+4)+2))/(C_2+C_3);
374         x(2,i+4) = (C_2*(x(2,i+4)-2) + C_3*x(3,i+4))/(C_2+C_3) + 2; %N. Brooks clamping
           ↪ equaiton
375         x(3,i+4) = x(2,i+4)-2;
376     end
377
378     coss_tracker_25(:,i+4) = x(1:3,i+4);
379     x(:,i+4) =
           ↪ [x(1,i+4);x(2,i+4)+C_3*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(3,i+4)-x(2,i+4));x(3,
           ↪ i+4)+C_2*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(2,i+4)-x(3,i+4));x(4:7,i+4)];%q3
           ↪ turns on
380     coss_tracker_25(:,i+4) = x(1:3,i+4)-coss_tracker_25(:,i+4);
381
382
383     x(:,i+5) = AS5_matexp*x(:,i+4)+AS5_int*B*V_in(i+4);
384
385     coss_tracker_25(:,i+5) = x(1:3,i+5);
386     x(:,i+5) = [x(1:2,i+5);x(3,i+5)+Ci*C_oss/(Ci*C_3+C_oss*(C_3+Ci))*(x(6,i+5)-x(3,i+5)
           ↪ );x(4:5,i+5);x(6,i+5)+C_3*C_oss/(C_3*Ci+C_oss*(C_3+Ci))*(x(3,i+5)-x(6,i+5));x(7
           ↪ ,i+5)];%q4 turns off
387     coss_tracker_25(:,i+5) = x(1:3,i+5)-coss_tracker_25(:,i+5);
388     x(:,i+6) = AS6_matexp*x(:,i+5)+AS6_int*B*V_in(i+5);
389     coss_tracker_25(:,i+6) = x(1:3,i+6);
390     x(:,i+6) = [x(1,i+6)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+6)-x(1,i+6));x(2,i+
           ↪ 6)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+6)-x(2,i+6));x(3:7,i+6)];%q2 turns
           ↪ on
391     coss_tracker_25(:,i+6) = x(1:3,i+6)-coss_tracker_25(:,i+6);
392     x(:,i+7) = AS7_matexp*x(:,i+6)+AS7_int*B*V_in(i+6);
393     coss_tracker_25(:,i+7) = x(1:3,i+7);
394     x(:,i+7) =
           ↪ [x(1,i+7);x(2,i+7)+C_3*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(3,i+7)-x(2,i+7));x(3,
           ↪ i+7)+C_2*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(2,i+7)-x(3,i+7));x(4:7,i+7)];%q3
           ↪ turns off
395     coss_tracker_25(:,i+7) = x(1:3,i+7)-coss_tracker_25(:,i+7);
396     x(:,i+8) = AS8_matexp*x(:,i+7)+AS8_int*B*V_in(i+7);
397
398     x2(:,i+1) = AS1_matexp*x2(:,i)+AS1_int*B*V_in(i);
399     if(x2(1,i+1)<-2) %Diode clamp lowest capacitor voltage
400         x2(1,i+1) = -2;
401     end
402     if(x2(2,i+1)-x2(3,i+1)>2) %Diode clamp middle cell
403 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
404         x2(2,i+1) = (C_2*(x2(2,i+1)-2) + C_3*x2(3,i+1))/(C_2+C_3) + 2; %N. Brooks
           ↪ clamping equaiton
405         x2(3,i+1) = x2(2,i+1)-2;

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```

406     end
407     x2(:,i+2) = AS2_matexp*x2(:,i+1)+AS2_int*B*V_in(i+1);
408     if(x2(1,i+2)<-2) %Diode clamp lowest capacitor voltage
409         x2(1,i+2) = -2;
410     end
411     if(x2(2,i+2)-x2(3,i+2)>2) %Diode clamp middle cell
412 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
413         x2(2,i+2) = (C_2*(x2(2,i+2)-2) + C_3*x2(3,i+2))/(C_2+C_3) + 2; %N. Brooks
414         ↪ clamping equaiton
415         x2(3,i+2) = x2(2,i+2)-2;
416     end
417     x2(:,i+3) = AS3_matexp*x2(:,i+2)+AS3_int*B*V_in(i+2);
418
419     if(x2(1,i+3)<-2) %Diode clamp lowest capacitor voltage
420         x2(1,i+3) = -2;
421     end
422     if(x2(2,i+3)-x2(3,i+3)>2) %Diode clamp middle cell
423 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
424         x2(2,i+3) = (C_2*(x2(2,i+3)-2) + C_3*x2(3,i+3))/(C_2+C_3) + 2; %N. Brooks
425         ↪ clamping equaiton
426         x2(3,i+3) = x2(2,i+3)-2;
427     end
428     x2(:,i+4) = AS4_matexp*x2(:,i+3)+AS4_int*B*V_in(i+3);
429
430     if(x2(1,i+4)<-2) %Diode clamp lowest capacitor voltage
431         x2(1,i+4) = -2;
432     end
433     if(x2(2,i+4)-x2(3,i+4)>2) %Diode clamp middle cell
434 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
435         x2(2,i+4) = (C_2*(x2(2,i+4)-2) + C_3*x2(3,i+4))/(C_2+C_3) + 2; %N. Brooks
436         ↪ clamping equaiton
437         x2(3,i+4) = x2(2,i+4)-2;
438     end
439     x2(:,i+5) = AS5_matexp*x2(:,i+4)+AS5_int*B*V_in(i+4);
440
441     if(x2(1,i+5)<-2) %Diode clamp lowest capacitor voltage
442         x2(1,i+5) = -2;
443     end
444     if(x2(2,i+5)-x2(3,i+5)>2) %Diode clamp middle cell
445 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
446         x2(2,i+5) = (C_2*(x2(2,i+5)-2) + C_3*x2(3,i+5))/(C_2+C_3) + 2; %N. Brooks
447         ↪ clamping equaiton
448         x2(3,i+5) = x2(2,i+5)-2;
449     end
450     x2(:,i+6) = AS6_matexp*x2(:,i+5)+AS6_int*B*V_in(i+5);
451     if(x2(1,i+6)<-2) %Diode clamp lowest capacitor voltage
452         x2(1,i+6) = -2;

```

```

452     end
453     if(x2(2,i+6)-x2(3,i+6)>2) %Diode clamp middle cell
454 %       x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
455       x2(2,i+6) = (C_2*(x2(2,i+6)-2) + C_3*x2(3,i+6))/(C_2+C_3) + 2; %N. Brooks
         ↪ clamping equaiton
456       x2(3,i+6) = x2(2,i+6)-2;
457     end
458     x2(:,i+7) = AS7_matexp*x2(:,i+6)+AS7_int*B*V_in(i+6);
459     if(x2(1,i+7)<-2) %Diode clamp lowest capacitor voltage
460       x2(1,i+7) = -2;
461     end
462     if(x2(2,i+7)-x2(3,i+7)>2) %Diode clamp middle cell
463 %       x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
464       x2(2,i+7) = (C_2*(x2(2,i+7)-2) + C_3*x2(3,i+7))/(C_2+C_3) + 2; %N. Brooks
         ↪ clamping equaiton
465       x2(3,i+7) = x2(2,i+7)-2;
466     end
467     x2(:,i+8) = AS8_matexp*x2(:,i+7)+AS8_int*B*V_in(i+7);
468     if(x2(1,i+8)<-2) %Diode clamp lowest capacitor voltage
469       x2(1,i+8) = -2;
470     end
471     if(x2(2,i+8)-x2(3,i+8)>2) %Diode clamp middle cell
472 %       x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
473       x2(2,i+8) = (C_2*(x2(2,i+8)-2) + C_3*x2(3,i+8))/(C_2+C_3) + 2; %N. Brooks
         ↪ clamping equaiton
474       x2(3,i+8) = x2(2,i+8)-2;
475     end
476
477     if(mod(i-1,5000)==0)
478       fprintf('Iteration Number %d/%d\r\n',i,num_iter)
479 %       fprintf('Simulation Time %0.2f [ms]\r\n',1e3*i*T/4)
480     end
481 end
482
483 time_stamps_25 = time_stamps_25(1:size(x,2));
484 V_in = V_in(1:length(time_stamps_25));
485 disp('Done Simulating D = 0.25 Leading Carrier Arrangement')
486 % Plot D = 0.25
487
488 figure(5)
489 plot(time_stamps_25,V_in,'color',hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth',1)
490 hold on
491 plot(time_stamps_25,x(1,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth',1)%,
         ↪ 'LineStyle','--', 'Color', '#D95319')
492 plot(time_stamps_25,x(2,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth',1)
493 plot(time_stamps_25,x(3,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth',1)
494 hold off
495 grid on
496 xlabel('Time [ms]')
497 ylabel('Voltages [V]')

```

```

498 set(gcf, 'Renderer', 'painters');
499 legend('$$V_{in}$$', '$$v_{c1}$$', '$$v_{c2}$$', '$$v_{c3}$$')
500 title('D = 0.25 With $$C_{oss}$$')
501 xlim([0 80])
502 set_figure_style(2)
503
504 figure(6)
505 plot(time_stamps_25, V_in, 'color', hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth', 1)
506 hold on
507 plot(time_stamps_25, x2(1,:), 'color', hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth', 1) %]
   ⇨ , 'LineStyle', '--', 'Color', '#D95319')
508 plot(time_stamps_25, x2(2,:), 'color', hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth', 1)
509 plot(time_stamps_25, x2(3,:), 'color', hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth', 1)
510 hold off
511 grid on
512 xlabel('Time [ms]')
513 ylabel('Voltages [V]')
514 set(gcf, 'Renderer', 'painters');
515 legend('$$V_{in}$$', '$$v_{c1}$$', '$$v_{c2}$$', '$$v_{c3}$$')
516 title('D = 0.25 Without $$C_{oss}$$')
517 xlim([0 80])
518 set_figure_style(2)
519
520 figure(8)
521 subplot(2,1,1)
522 plot(time_stamps_25, x(6,:), time_stamps_25, x2(6,:))
523 ylabel('[V]')
524 legend('With $$C_{oss}$$', 'Without $$C_{oss}$$')
525 grid on
526 title('Input Cap')
527 subplot(2,1,2)
528 plot(time_stamps_25, x2(4,:), time_stamps_25, x2(7,:))
529 title('Inductor Currents')
530 legend('Output Current', 'Input Current')
531 grid on
532 ylabel('[A]')
533 xlabel('Time [ms]')
534 set_figure_style(2)
535
536
537 vc_ss = 0.5*(max(x(1:3, sim_time*1e6-15e3:sim_time*1e6-10e3), [], 2)+min(x(1:3, sim_time*1e
   ⇨ 6-15e3:sim_time*1e6-10e3), [], 2));
538 vc2_ss = 0.5*(max(x2(1:3, sim_time*1e6-15e3:sim_time*1e6-10e3), [], 2)+min(x2(1:3, sim_time
   ⇨ *1e6-15e3:sim_time*1e6-10e3), [], 2));
539 vc_ss_e = vc_ss-[1/4;1/2;3/4]*V_in(10e3);
540 vc_ss_e_pct = vc_ss_e*100./([1/4;1/2;3/4]*V_in(10e3));
541 vc2_ss_e = vc2_ss-[1/4;1/2;3/4]*V_in(10e3);
542 vc2_ss_e_pct = vc2_ss_e*100./([1/4;1/2;3/4]*V_in(10e3));
543
544 fprintf('Input Network Characteristic Impedance: %0.2d [\x03A9] and Q: %0.2d Cin: %0.2d
   ⇨ [\x03BC F]\r\n', Zi, Qi, Ci*1e6)

```

```

545 fprintf('Output Current %0.2d [A]\r\n',mean(x(4,14e3:14.5e3),2))
546 fprintf('No Coss SS error\t\t With Coss SS error \r\n')
547 fprintf('\x0394Vc1/Vc1nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(1),vc_ss_e_pct(1))
548 fprintf('\x0394Vc2/Vc2nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(2),vc_ss_e_pct(2))
549 fprintf('\x0394Vc3/Vc3nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(3),vc_ss_e_pct(3))
550 disp(vc_ss);
551 disp(vc2_ss);
552 disp(max(x(4,sim_time*1e6-15e3:sim_time*1e6-10e3)));
553 disp(max(x2(4,sim_time*1e6-15e3:sim_time*1e6-10e3)))
554
555 %% 5-Level at D = 0.4 Leading PSPWM no output cap
556 L_o = 10e-6; %output filter inductance [H]
557 R_L = 34e-3+4*16e-3; %resistance lumped into inductor [Ohms] Inductor DCR + 4 switching
    ↪ FETs + 7 always on FETs + current sense resistors
558 R_L = R_L*6 ;
559
560 f_sw = 120e3; %switching frequency [Hz]
561 T = 1/f_sw; %period [s]
562 C_1 = 10e-6; %Fly cap capacitance [F]
563 C_2 = C_1;
564 C_3 = C_1;
565
566 C_oss = 600e-12;
567 V_in = 50;
568 V_out = 0.4*V_in;
569 I_out = 4;
570 R_o = V_out/I_out; %Output resistance [Ohms]
571
572 Li = 1e-6; %Input impedance inductance [H]
573 RLi = 0.1; %Input impedance resistance [Ohms]
574 Ci = 13e-6; %Input capacitance [F]
575 Qi = 1/RLi*sqrt(Li/Ci); %Input network Q
576 Zi = sqrt(Li/Ci); %Input network characteristic impedance
577
578 sim_time = 80e-3;
579 num_iter = floor(sim_time/T*8); %number of iterations of a (fundamental) switching
    ↪ period
580 state_time_1 = T*(.6/4); %Time spent in each switching state; V_sw = .5V_in
581 state_time_2 = T*(.4/4); %time spent in v_sw = .25V_in
582 time_stamps_25 = [];
583 for i = 0:sim_time*1e5*1.2-1
584
585     time_stamps_25 = [time_stamps_25,i*T,i*T+.15*T,i*T+T/4,i*T+.4*T,i*T+T/2,i*T+.65*T,i_
        ↪ *T+3*T/4,i*T+.9*T];
586 end
587 time_stamps_25 = 1e3*time_stamps_25; %converter indices to ms rather than s
588
589
590 % x = zeros(5,num_iter); %vector of state variables [v_c; i_L; v_o];
591 x = x(1:6,:);

```



```

592 x2 = x2(1:6,:);
593 x(:,1) = [zeros(6,1)];
594 % x2 = zeros(5,num_iter); %vector of state variables [v_c; i_L; v_o];
595 x2(:,1) = x(:,1);
596 % syms C_1 C_2 C_3 C_o L_o R_L
597
598 coss_tracker_25 = [0;0;0];
599 %Leading carrier A matrices
600 A_S1 = [zeros(1,6);zeros(1,3),-1/C_2,zeros(1,2);zeros(1,6);0,1/L_o,0,-(R_L+R_o)/L_o,0,0]
        ↪ ;zeros(1,5),1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
601 A_S2 = [zeros(1,3),-1/C_1,0,0;zeros(2,6);1/L_o,0,0,-(R_L+R_o)/L_o,0,0;zeros(1,5),1/C_i;z
        ↪ eros(1,4),-1/L_i,-RLi/Li];
602 A_S3 = [zeros(1,3),-1/C_1,0,0;zeros(1,6);zeros(1,3),1/C_3,0,0;1/L_o,0,-1/L_o,-(R_L+R_o)
        ↪ /L_o,1/L_o,0;zeros(1,3),-1/C_i,0,1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
603 A_S4 = [zeros(2,6);zeros(1,3),1/C_3,0,0;0,0,-1/L_o,-(R_L+R_o)/L_o,1/L_o,0;zeros(1,3),-1
        ↪ /C_i,0,1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
604 A_S5 = [zeros(1,6);zeros(1,3),1/C_2,0,0;zeros(1,6);0,-1/L_o,0,-(R_L+R_o)/L_o,1/L_o,0;ze
        ↪ ros(1,3),-1/C_i,0,1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
605 A_S6 = [zeros(1,6);zeros(1,3),1/C_2,0,0;zeros(1,3),-1/C_3,0,0;0,-1/L_o,1/L_o,-(R_L+R_o)
        ↪ /L_o,0,0;zeros(1,5),1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
606 A_S7 = [zeros(1,3),1/C_1,0,0;zeros(1,6);zeros(1,3),-1/C_3,0,0;-1/L_o,0,1/L_o,-(R_L+R_o)
        ↪ /L_o,0,0;zeros(1,5),1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
607 A_S8 = [zeros(1,3),1/C_1,0,0;zeros(1,3),-1/C_2,0,0;zeros(1,6);-1/L_o,1/L_o,0,-(R_L+R_o)
        ↪ /L_o,0,0;zeros(1,5),1/C_i;zeros(1,4),-1/L_i,-RLi/Li];
608 %Lagging carrier A matrices
609 % A_S1 = [zeros(1,3),-1/C_1,0;zeros(1,5);zeros(1,3),1/C_3,0;1/L_o,0,-1/L_o,-R_L/L_o,-1/
        ↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
610 % A_S2 = [zeros(1,5);zeros(1,3),-1/C_2,0;zeros(1,5);0,1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
        ↪ ],1/C_o,-1/(R_o*C_o)];
611 % A_S3 = [zeros(1,3),1/C_1,0;zeros(1,5);zeros(1,3),-1/C_3,0;-1/L_o,0,1/L_o,-R_L/L_o,-1/
        ↪ L_o;zeros(1,3),1/C_o,-1/(R_o*C_o)];
612 % A_S4 = [zeros(1,5);zeros(1,3),1/C_2,0;zeros(1,5);0,-1/L_o,0,-R_L/L_o,-1/L_o;zeros(1,3)
        ↪ ],1/C_o,-1/(R_o*C_o)];
613
614 AS1_matexp = expm(A_S1*state_time_1);
615 AS1_int = integral(@(t) expm(A_S1.*(t)),0,state_time_1, 'ArrayValued', true);
616 AS2_matexp = expm(A_S2*state_time_2);
617 AS2_int = integral(@(t) expm(A_S2.*(t)),0,state_time_2, 'ArrayValued', true);
618 AS3_matexp = expm(A_S3*state_time_1);
619 AS3_int = integral(@(t) expm(A_S3.*(t)),0,state_time_1, 'ArrayValued', true);
620 AS4_matexp = expm(A_S4*state_time_2);
621 AS4_int = integral(@(t) expm(A_S4.*(t)),0,state_time_2, 'ArrayValued', true);
622 AS5_matexp = expm(A_S5*state_time_1);
623 AS5_int = integral(@(t) expm(A_S5.*(t)),0,state_time_1, 'ArrayValued', true);
624 AS6_matexp = expm(A_S6*state_time_2);
625 AS6_int = integral(@(t) expm(A_S6.*(t)),0,state_time_2, 'ArrayValued', true);
626 AS7_matexp = expm(A_S7*state_time_1);
627 AS7_int = integral(@(t) expm(A_S7.*(t)),0,state_time_1, 'ArrayValued', true);
628 AS8_matexp = expm(A_S8*state_time_2);
629 AS8_int = integral(@(t) expm(A_S8.*(t)),0,state_time_2, 'ArrayValued', true);

```

```

630 %Leading carrier B matrices
631 B = [zeros(5,1);1/Li];
632 %Lagging carrier B matrices
633 % B_S1 = [zeros(3,1);1/L_o;0];
634 % B_S4 = [zeros(3,1);1/L_o;0];
635
636 i = 2:num_iter;
637 V_in = [5,max(5,5+45*(1-exp(-(i-500)/454.5)))]];
638
639 for i = 1:8:num_iter-8
640     % Leading carrier arrangement
641     coss_tracker_25(:,i) = x(1:3,i);
642     x(:,i) = [x(1,i)*C_1/(C_1+C_oss);x(2:6,i)]; %q1 turns on, leading carrier
643     coss_tracker_25(:,i) = x(1:3,i)-coss_tracker_25(:,i);
644     if(x(1,i)<-2) %Diode clamp lowest capacitor voltage
645         x(1,i) = -2;
646     end
647     if(x(2,i)-x(3,i)>2) %Diode clamp middle cell
648         % x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
649         x(2,i) = (C_2*(x(2,i)-2) + C_3*x(3,i))/(C_2+C_3) + 2; %N. Brooks clamping
        ↪ equaiton
650         x(3,i) = x(2,i)-2;
651     end
652
653     x(:,i+1) = AS1_matexp*x(:,i)+AS1_int*B*V_in(i);
654
655     if(x(1,i+1)<-2) %Diode clamp lowest capacitor voltage
656         x(1,i+1) = -2;
657     end
658     if(x(2,i+1)-x(3,i+1)>2) %Diode clamp middle cell
659         % x(2,i+1) = (C_2*x(2,i+1)+C_3*(x(3,i+1)+2))/(C_2+C_3);
660         x(2,i+1) = (C_2*(x(2,i+1)-2) + C_3*x(3,i+1))/(C_2+C_3) + 2; %N. Brooks clamping
        ↪ equaiton
661         x(3,i+1) = x(2,i+1)-2;
662     end
663     coss_tracker_25(:,i+1) = x(1:3,i+1);
664     x(:,i+1) = [x(1,i+1)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+1)-x(1,i+1));x(2,i+1)+
        ↪ 1)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+1)-x(2,i+1));x(3:6,i+1)];%q2 turns
        ↪ off, leading carrier
665     coss_tracker_25(:,i+1) = x(1:3,i+1)-coss_tracker_25(:,i+1);
666     x(:,i+2) = AS2_matexp*x(:,i+1)+AS2_int*B*V_in(i+1);
667
668     if(x(1,i+2)<-2) %Diode clamp lowest capacitor voltage
669         x(1,i+2) = -2;
670     end
671     if(x(2,i+2)-x(3,i+2)>2) %Diode clamp middle cell
672         % x(2,i+2) = (C_2*x(2,i+2)+C_3*(x(3,i+2)+2))/(C_2+C_3);
673         x(2,i+2) = (C_2*(x(2,i+2)-2) + C_3*x(3,i+2))/(C_2+C_3) + 2; %N. Brooks clamping
        ↪ equaiton
674         x(3,i+2) = x(2,i+2)-2;

```

```

675     end
676
677     coss_tracker_25(:,i+2) = x(1:3,i+2);
678     x(:,i+2) =
        ↪ [x(1:2,i+2);x(3,i+2)+Ci*C_oss/(Ci*C_3+C_oss*(C_3+Ci))*(x(5,i+2)-x(3,i+2));x(4,i
        ↪ +2);x(5,i+2)+C_3*C_oss/(C_3*Ci+C_oss*(C_3+Ci))*(x(3,i+2)-x(5,i+2));x(6,i+2)];%q4
        ↪ turns on
679     coss_tracker_25(:,i+2) = x(1:3,i+2)-coss_tracker_25(:,i+2);
680
681     x(:,i+3) = AS3_matexp*x(:,i+2)+AS3_int*B*V_in(i+2);
682
683     if(x(1,i+3)<-2) %Diode clamp lowest capacitor voltage
684         x(1,i+3) = -2;
685     end
686     if(x(2,i+3)-x(3,i+3)>2) %Diode clamp middle cell
687 %         x(2,i+3) = (C_2*x(2,i+3)+C_3*(x(3,i+3)+2))/(C_2+C_3);
688         x(2,i+3) = (C_2*(x(2,i+3)-2) + C_3*x(3,i+3))/(C_2+C_3) + 2; %N. Brooks clamping
        ↪ equaiton
689         x(3,i+3) = x(2,i+3)-2;
690     end
691
692     coss_tracker_25(:,i+3) = x(1:3,i+3);
693     x(:,i+3) = [x(1,i+3)*C_1/(C_1+C_oss);x(2:6,i+3)];%q1 turns off
694     coss_tracker_25(:,i+3) = x(1:3,i+3)-coss_tracker_25(:,i+3);
695
696     x(:,i+4) = AS4_matexp*x(:,i+3)+AS4_int*B*V_in(i+3);
697
698     if(x(1,i+4)<-2) %Diode clamp lowest capacitor voltage
699         x(1,i+4) = -2;
700     end
701     if(x(2,i+4)-x(3,i+4)>2) %Diode clamp middle cell
702 %         x(2,i+4) = (C_2*x(2,i+4)+C_3*(x(3,i+4)+2))/(C_2+C_3);
703         x(2,i+4) = (C_2*(x(2,i+4)-2) + C_3*x(3,i+4))/(C_2+C_3) + 2; %N. Brooks clamping
        ↪ equaiton
704         x(3,i+4) = x(2,i+4)-2;
705     end
706
707     coss_tracker_25(:,i+4) = x(1:3,i+4);
708     x(:,i+4) =
        ↪ [x(1,i+4);x(2,i+4)+C_3*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(3,i+4)-x(2,i+4));x(3,
        ↪ i+4)+C_2*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(2,i+4)-x(3,i+4));x(4:6,i+4)];%q3
        ↪ turns on
709     coss_tracker_25(:,i+4) = x(1:3,i+4)-coss_tracker_25(:,i+4);
710
711
712     x(:,i+5) = AS5_matexp*x(:,i+4)+AS5_int*B*V_in(i+4);
713
714     coss_tracker_25(:,i+5) = x(1:3,i+5);
715     x(:,i+5) =
        ↪ [x(1:2,i+5);x(3,i+5)+Ci*C_oss/(Ci*C_3+C_oss*(C_3+Ci))*(x(5,i+5)-x(3,i+5));x(4,i
        ↪ +5);x(5,i+5)+C_3*C_oss/(C_3*Ci+C_oss*(C_3+Ci))*(x(3,i+5)-x(5,i+5));x(6,i+5)];%q4
        ↪ turns off

```

```

716     coss_tracker_25(:,i+5) = x(1:3,i+5)-coss_tracker_25(:,i+5);
717     x(:,i+6) = AS6_matexp*x(:,i+5)+AS6_int*B*V_in(i+5);
718     coss_tracker_25(:,i+6) = x(1:3,i+6);
719     x(:,i+6) = [x(1,i+6)+C_2*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(2,i+6)-x(1,i+6));x(2,i+
    ↪ 6)+C_1*C_oss/(C_1*C_2+C_oss*(C_1+C_2))*(x(1,i+6)-x(2,i+6));x(3:6,i+6)];%q2 turns
    ↪ on
720     coss_tracker_25(:,i+6) = x(1:3,i+6)-coss_tracker_25(:,i+6);
721     x(:,i+7) = AS7_matexp*x(:,i+6)+AS7_int*B*V_in(i+6);
722     coss_tracker_25(:,i+7) = x(1:3,i+7);
723     x(:,i+7) =
    ↪ [x(1,i+7);x(2,i+7)+C_3*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(3,i+7)-x(2,i+7));x(3,
    ↪ i+7)+C_2*C_oss/(C_2*C_3+C_oss*(C_2+C_3))*(x(2,i+7)-x(3,i+7));x(4:6,i+7)];%q3
    ↪ turns off
724     coss_tracker_25(:,i+7) = x(1:3,i+7)-coss_tracker_25(:,i+7);
725     x(:,i+8) = AS8_matexp*x(:,i+7)+AS8_int*B*V_in(i+7);
726
727     x2(:,i+1) = AS1_matexp*x2(:,i)+AS1_int*B*V_in(i);
728     if(x2(1,i+1)<-2) %Diode clamp lowest capacitor voltage
729         x2(1,i+1) = -2;
730     end
731     if(x2(2,i+1)-x2(3,i+1)>2) %Diode clamp middle cell
732 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
733         x2(2,i+1) = (C_2*(x2(2,i+1)-2) + C_3*x2(3,i+1))/(C_2+C_3) + 2; %N. Brooks
    ↪ clamping equaiton
734         x2(3,i+1) = x2(2,i+1)-2;
735     end
736     x2(:,i+2) = AS2_matexp*x2(:,i+1)+AS2_int*B*V_in(i+1);
737     if(x2(1,i+2)<-2) %Diode clamp lowest capacitor voltage
738         x2(1,i+2) = -2;
739     end
740     if(x2(2,i+2)-x2(3,i+2)>2) %Diode clamp middle cell
741 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
742         x2(2,i+2) = (C_2*(x2(2,i+2)-2) + C_3*x2(3,i+2))/(C_2+C_3) + 2; %N. Brooks
    ↪ clamping equaiton
743         x2(3,i+2) = x2(2,i+2)-2;
744     end
745
746     x2(:,i+3) = AS3_matexp*x2(:,i+2)+AS3_int*B*V_in(i+2);
747
748     if(x2(1,i+3)<-2) %Diode clamp lowest capacitor voltage
749         x2(1,i+3) = -2;
750     end
751     if(x2(2,i+3)-x2(3,i+3)>2) %Diode clamp middle cell
752 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
753         x2(2,i+3) = (C_2*(x2(2,i+3)-2) + C_3*x2(3,i+3))/(C_2+C_3) + 2; %N. Brooks
    ↪ clamping equaiton
754         x2(3,i+3) = x2(2,i+3)-2;
755     end
756
757     x2(:,i+4) = AS4_matexp*x2(:,i+3)+AS4_int*B*V_in(i+3);

```

```

758
759     if(x2(1,i+4)<-2) %Diode clamp lowest capacitor voltage
760         x2(1,i+4) = -2;
761     end
762     if(x2(2,i+4)-x2(3,i+4)>2) %Diode clamp middle cell
763 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
764         x2(2,i+4) = (C_2*(x2(2,i+4)-2) + C_3*x2(3,i+4))/(C_2+C_3) + 2; %N. Brooks
           ⇨ clamping equaiton
765         x2(3,i+4) = x2(2,i+4)-2;
766     end
767
768     x2(:,i+5) = AS5_matexp*x2(:,i+4)+AS5_int*B*V_in(i+4);
769
770     if(x2(1,i+5)<-2) %Diode clamp lowest capacitor voltage
771         x2(1,i+5) = -2;
772     end
773     if(x2(2,i+5)-x2(3,i+5)>2) %Diode clamp middle cell
774 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
775         x2(2,i+5) = (C_2*(x2(2,i+5)-2) + C_3*x2(3,i+5))/(C_2+C_3) + 2; %N. Brooks
           ⇨ clamping equaiton
776         x2(3,i+5) = x2(2,i+5)-2;
777     end
778     x2(:,i+6) = AS6_matexp*x2(:,i+5)+AS6_int*B*V_in(i+5);
779     if(x2(1,i+6)<-2) %Diode clamp lowest capacitor voltage
780         x2(1,i+6) = -2;
781     end
782     if(x2(2,i+6)-x2(3,i+6)>2) %Diode clamp middle cell
783 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
784         x2(2,i+6) = (C_2*(x2(2,i+6)-2) + C_3*x2(3,i+6))/(C_2+C_3) + 2; %N. Brooks
           ⇨ clamping equaiton
785         x2(3,i+6) = x2(2,i+6)-2;
786     end
787     x2(:,i+7) = AS7_matexp*x2(:,i+6)+AS7_int*B*V_in(i+6);
788     if(x2(1,i+7)<-2) %Diode clamp lowest capacitor voltage
789         x2(1,i+7) = -2;
790     end
791     if(x2(2,i+7)-x2(3,i+7)>2) %Diode clamp middle cell
792 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
793         x2(2,i+7) = (C_2*(x2(2,i+7)-2) + C_3*x2(3,i+7))/(C_2+C_3) + 2; %N. Brooks
           ⇨ clamping equaiton
794         x2(3,i+7) = x2(2,i+7)-2;
795     end
796     x2(:,i+8) = AS8_matexp*x2(:,i+7)+AS8_int*B*V_in(i+7);
797     if(x2(1,i+8)<-2) %Diode clamp lowest capacitor voltage
798         x2(1,i+8) = -2;
799     end
800     if(x2(2,i+8)-x2(3,i+8)>2) %Diode clamp middle cell
801 %         x(2,i) = (C_2*x(2,i)+C_3*(x(3,i)+2))/(C_2+C_3);
802         x2(2,i+8) = (C_2*(x2(2,i+8)-2) + C_3*x2(3,i+8))/(C_2+C_3) + 2; %N. Brooks
           ⇨ clamping equaiton

```

```

803     x2(3,i++8) = x2(2,i+8)-2;
804 end
805
806 if(mod(i-1,5000)==0)
807     fprintf('Iteration Number %d/%d\r\n',i,num_iter)
808 %     fprintf('Simulation Time %0.2f [ms]\r\n',1e3*i*T/4)
809 end
810 end
811
812 time_stamps_25 = time_stamps_25(1:size(x,2));
813 V_in = V_in(1:length(time_stamps_25));
814
815 coss_tracker_25_filt(1,:) = filter(1/8*ones(1,8),1,cooss_tracker_25(1,:));
816 coss_tracker_25_filt(2,:) = filter(1/8*ones(1,8),1,cooss_tracker_25(2,:));
817 coss_tracker_25_filt(3,:) = filter(1/8*ones(1,8),1,cooss_tracker_25(3,:));
818 disp('Done Simulating D = 0.4 Leading Carrier Arrangement')
819 %% Plot D = 0.4
820
821 figure(9)
822 plot(time_stamps_25,V_in,'color',hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth',1)
823 hold on
824 plot(time_stamps_25,x(1,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth',1)% ,
↪ 'LineStyle','--', 'Color', '#D95319')
825 plot(time_stamps_25,x(2,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth',1)
826 plot(time_stamps_25,x(3,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth',1)
827 hold off
828 grid on
829 xlabel('Time [ms]')
830 ylabel('Voltages [V]')
831 set(gcf, 'Renderer', 'painters');
832 legend('$$V_{in}$$', '$$v_{c1}$$', '$$v_{c2}$$', '$$v_{c3}$$')
833 title('D = 0.4 With $$C_{oss}$$')
834 xlim([0 80])
835 set_figure_style(2)
836
837 figure(10)
838 plot(time_stamps_25,V_in,'color',hsl2rgb(rgb2hsl(colormap_MAT(1,:))), 'LineWidth',1)
839 hold on
840 plot(time_stamps_25,x2(1,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(2,:))), 'LineWidth',1)% ,
↪ 'LineStyle','--', 'Color', '#D95319')
841 plot(time_stamps_25,x2(2,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(3,:))), 'LineWidth',1)
842 plot(time_stamps_25,x2(3,:), 'color',hsl2rgb(rgb2hsl(colormap_MAT(4,:))), 'LineWidth',1)
843 hold off
844 grid on
845 xlabel('Time [ms]')
846 ylabel('Voltages [V]')
847 set(gcf, 'Renderer', 'painters');
848 legend('$$V_{in}$$', '$$v_{c1}$$', '$$v_{c2}$$', '$$v_{c3}$$')
849 title('D = 0.4 Without $$C_{oss}$$')
850 xlim([0 80])

```

```

851 set_figure_style(2)
852
853 figure(12)
854 subplot(2,1,1)
855 plot(time_stamps_25,x(5,:),time_stamps_25,x2(5,:))
856 ylabel(' [V] ')
857 legend('With $$C_{oss}$$','Without $$C_{oss}$$')
858 grid on
859 title('Input Cap')
860 subplot(2,1,2)
861 plot(time_stamps_25,x(4,:),time_stamps_25,x(6,:))
862 title('Inductor Currents')
863 legend('Output Current','Input Current')
864 grid on
865 ylabel(' [A] ')
866 xlabel('Time [ms]')
867 set_figure_style(2)
868
869
870 vc_ss = 0.5*(max(x(1:3,sim_time*1e6-15e3:sim_time*1e6-10e3),[],2)+min(x(1:3,sim_time*1e
    ↪ 6-15e3:sim_time*1e6-10e3),[],2));
871 vc2_ss = 0.5*(max(x2(1:3,sim_time*1e6-15e3:sim_time*1e6-10e3),[],2)+min(x2(1:3,sim_time
    ↪ *1e6-15e3:sim_time*1e6-10e3),[],2));
872 vc_ss_e = vc_ss-[1/4;1/2;3/4]*V_in(10e3);
873 vc_ss_e_pct = vc_ss_e*100./([1/4;1/2;3/4]*V_in(10e3));
874 vc2_ss_e = vc2_ss-[1/4;1/2;3/4]*V_in(10e3);
875 vc2_ss_e_pct = vc2_ss_e*100./([1/4;1/2;3/4]*V_in(10e3));
876
877 fprintf('D = 0.4')
878 fprintf('Input Network Characteristic Impdeance: %0.2d [\x03A9] and Q: %0.2d Cin: %0.2d
    ↪ [\x03BC F]\r\n',Zi,Qi,Ci*1e6)
879 fprintf('Output Current %0.2d [A]\r\n',mean(x(4,14e3:14.5e3),2))
880 fprintf('No Coss SS error\t\t With Coss SS error \r\n')
881 fprintf('\x0394Vc1/Vc1nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(1),vc_ss_e_pct(1))
882 fprintf('\x0394Vc2/Vc2nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(2),vc_ss_e_pct(2))
883 fprintf('\x0394Vc3/Vc3nom: %0.2d[%%]\t\t %0.2d[%%]\r\n',vc2_ss_e_pct(3),vc_ss_e_pct(3))
884 disp(vc_ss);
885 disp(vc2_ss);
886 disp(max(x(4,sim_time*1e6-15e3:sim_time*1e6-10e3)));
887 disp(max(x2(4,sim_time*1e6-15e3:sim_time*1e6-10e3)))

```

Appendix B

Buck-Type PFC TI C2000 C-code

Firmware was written for Texas Instruments F28379D Microcontroller mounted on the TMD-SCNCD28379D controlCARD™.

```

1  #include "main.h"
2
3
4  uint32_t pwmHandle[6] = {EPWM2_BASE, EPWM3_BASE, EPWM4_BASE, EPWM5_BASE, EPWM6_BASE,
   ↪  EPWM1_BASE};
5  uint32_t adcHandle[4] = {ADCA_BASE, ADCB_BASE, ADCC_BASE, ADCD_BASE};
6  __interrupt void epwm2_isr(void); //Update at Q5's counter update
7
8  uint16_t TBPRD = 500; //100 kHz
9
10 int execute_ctrl = 0;
11 int main(void){
12     // Initialize device clock and peripherals
13     Device_init();
14     // Disable pin locks and enable internal pullups.
15     Device_initGPIO();
16     // Clear all interrupts and initialize PIE vector table:
17     // Initialize the PIE control registers to their default state.
18     // The default state is all PIE interrupts disabled and flags
19     // are cleared.
20     Interrupt_initModule();
21
22     // Initialize the PIE vector table with pointers to the shell Interrupt
23     // Service Routines (ISR).
24     // This will populate the entire table, even if the interrupt
25     // is not used in this example. This is useful for debug purposes.
26     Interrupt_initVectorTable();
27
28     Interrupt_register(INT_EPWM2, epwm2_isr);
29     //Interrupt_register(INT_EPWM1, epwm1_isr);
30     //Interrupt_register(INT_ADCA1, adca1_isr);
31

```



```

32     configureGPIO();
33     configureEPWM();
34     configureADC();
35     configureDAC();
36     //configureSPI();
37     //Interrupt_register(INT_SPIA_TX, &spiaTxFIFOISR);
38
39     SysCtl_enablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
40
41     // Clear spurious flags
42     EPWM_clearEventTriggerInterruptFlag(EPWM2_BASE);
43     //EPWM_clearEventTriggerInterruptFlag(EPWM1_BASE);
44     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP3);
45     //Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP6);
46     //EPWM_clearADCTriggerFlag(EPWM1_BASE, EPWM_SOC_A);
47     //ADC_clearInterruptStatus(adcHandle[0], ADC_INT_NUMBER1);
48     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP1);
49
50     // Enable CPU INT3 which is connected to EPWM1-3 INT:
51     Interrupt_enableInCPU(INTERRUPT_CPU_INT3);
52     Interrupt_enableInCPU(INTERRUPT_CPU_INT1);
53     //Interrupt_enableInCPU(INTERRUPT_CPU_INT6); //MCBSPB RX INT
54     init_ctrl_gain();
55
56     // Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
57     GPIO_writePin(PWMHA, 0);
58     GPIO_writePin(PWMLB, 1);
59     GPIO_writePin(PWMHB, 0);
60     GPIO_writePin(PWMLA, 1);
61     EPWM_setCounterCompareValue(EPWM1_BASE, EPWM_COUNTER_COMPARE_A, 0);
62     EPWM_setCounterCompareValue(EPWM2_BASE, EPWM_COUNTER_COMPARE_A, 0);
63     EPWM_setCounterCompareValue(EPWM3_BASE, EPWM_COUNTER_COMPARE_A, 0);
64     EPWM_setCounterCompareValue(EPWM4_BASE, EPWM_COUNTER_COMPARE_A, 0);
65     EPWM_setCounterCompareValue(EPWM5_BASE, EPWM_COUNTER_COMPARE_A, 0);
66     EPWM_setCounterCompareValue(EPWM6_BASE, EPWM_COUNTER_COMPARE_A, 0);
67     Interrupt_enable(INT_EPWM2);
68     //Interrupt_enable(INT_EPWM1);
69     //SM_changeState(&INITIAL_STATE);
70     //
71     // Enable global Interrupts and higher priority real-time debug events:
72     //
73     EINT; //Enable Global interrupt INTM
74     ERTM; //Enable Global realtime interrupt DBGM
75     while(1){
76     }
77 }
78 __interrupt void epwm2_isr(void){
79 //__interrupt void epwm1_isr(void){
80     // Toggle GPIO
81     GPIO_writePin(27, 1);

```

```

82     sample_system();
83     if(execute_ctrl){
84         execute_controller();
85     }
86     EPWM_clearEventTriggerInterruptFlag(EPWM2_BASE);
87     // Acknowledge this interrupt to receive more interrupts from group 3
88     Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP3);
89     GPIO_writePin(27, 0);
90     return;
91 }
92
93 void configureGPIO(void){
94     //PWM1A maps to Q5H
95     GPIO_setMasterCore(0, GPIO_CORE_CPU1);
96     GPIO_setPinConfig(GPIO_0_EPWM1A);
97     GPIO_setPadConfig(0, GPIO_PIN_TYPE_STD);
98     //PWM1B maps to Q5L
99     GPIO_setMasterCore(1, GPIO_CORE_CPU1);
100    GPIO_setPinConfig(GPIO_1_EPWM1B);
101    GPIO_setPadConfig(1, GPIO_PIN_TYPE_STD);
102    //PWM2A maps to Q5H
103    //IGNORE PWM2A maps to Q4H
104    GPIO_setMasterCore(2, GPIO_CORE_CPU1);
105    GPIO_setPinConfig(GPIO_2_EPWM2A);
106    GPIO_setPadConfig(2, GPIO_PIN_TYPE_STD);
107    //PWM2B maps to Q5L
108    //IGNORE PWM2B maps to Q4L
109    GPIO_setMasterCore(3, GPIO_CORE_CPU1);
110    GPIO_setPinConfig(GPIO_3_EPWM2B);
111    GPIO_setPadConfig(3, GPIO_PIN_TYPE_STD);
112    //PWM3A maps to Q4H
113    //IGNORE PWM3A maps to Q3H
114    GPIO_setMasterCore(4, GPIO_CORE_CPU1);
115    GPIO_setPinConfig(GPIO_4_EPWM3A);
116    GPIO_setPadConfig(4, GPIO_PIN_TYPE_STD);
117    //PWM3B maps to Q4L
118    //IGNORE PWM3B maps to Q3L
119    GPIO_setMasterCore(5, GPIO_CORE_CPU1);
120    GPIO_setPinConfig(GPIO_5_EPWM3B);
121    GPIO_setPadConfig(5, GPIO_PIN_TYPE_STD);
122    //PWM4A maps to Q3H
123    //IGNORE PWM4A maps to Q2H
124    GPIO_setMasterCore(6, GPIO_CORE_CPU1);
125    GPIO_setPinConfig(GPIO_6_EPWM4A);
126    GPIO_setPadConfig(6, GPIO_PIN_TYPE_STD);
127    //PWM4B maps to Q3L
128    //IGNORE PWM4B maps to Q2L
129    GPIO_setMasterCore(7, GPIO_CORE_CPU1);
130    GPIO_setPinConfig(GPIO_7_EPWM4B);
131    GPIO_setPadConfig(7, GPIO_PIN_TYPE_STD);

```

```

132     //PWM5A maps to Q2H
133     //IGNORE PWM5A maps to Q1H
134     GPIO_setMasterCore(8, GPIO_CORE_CPU1);
135     GPIO_setPinConfig(GPIO_8_EPWM5A);
136     GPIO_setPadConfig(8, GPIO_PIN_TYPE_STD);
137     //PWM5B maps to Q2L
138     //IGNORE PWM5B maps to Q1L
139     GPIO_setMasterCore(9, GPIO_CORE_CPU1);
140     GPIO_setPinConfig(GPIO_9_EPWM5B);
141     GPIO_setPadConfig(9, GPIO_PIN_TYPE_STD);
142     //PWM6A maps to Q1H
143     GPIO_setMasterCore(10, GPIO_CORE_CPU1);
144     GPIO_setPinConfig(GPIO_10_EPWM6A);
145     GPIO_setPadConfig(10, GPIO_PIN_TYPE_STD);
146     //PWM6B maps to Q1L
147     GPIO_setMasterCore(11, GPIO_CORE_CPU1);
148     GPIO_setPinConfig(GPIO_11_EPWM6B);
149     GPIO_setPadConfig(11, GPIO_PIN_TYPE_STD);
150     // Debugging pin
151     GPIO_setMasterCore(27, GPIO_CORE_CPU1);
152     GPIO_setPinConfig(GPIO_27_GPIO27);
153     GPIO_setPadConfig(27, GPIO_PIN_TYPE_STD);
154     GPIO_setDirectionMode(27, GPIO_DIR_MODE_OUT);
155     // Rectifier GPIOs
156     //PWM HA
157     GPIO_setMasterCore(22, GPIO_CORE_CPU1);
158     GPIO_setPinConfig(GPIO_22_GPIO22);
159     GPIO_setPadConfig(22, GPIO_PIN_TYPE_STD);
160     GPIO_setDirectionMode(22, GPIO_DIR_MODE_OUT);
161     //PWM LA
162     GPIO_setMasterCore(23, GPIO_CORE_CPU1);
163     GPIO_setPinConfig(GPIO_23_GPIO23);
164     GPIO_setPadConfig(23, GPIO_PIN_TYPE_STD);
165     GPIO_setDirectionMode(23, GPIO_DIR_MODE_OUT);
166     //PWM HB
167     GPIO_setMasterCore(28, GPIO_CORE_CPU1);
168     GPIO_setPinConfig(GPIO_28_GPIO28);
169     GPIO_setPadConfig(28, GPIO_PIN_TYPE_STD);
170     GPIO_setDirectionMode(28, GPIO_DIR_MODE_OUT);
171     //PWM LB
172     GPIO_setMasterCore(29, GPIO_CORE_CPU1);
173     GPIO_setPinConfig(GPIO_29_GPIO29);
174     GPIO_setPadConfig(29, GPIO_PIN_TYPE_STD);
175     GPIO_setDirectionMode(29, GPIO_DIR_MODE_OUT);
176     return;
177 }
178
179 void configureEPWM(void){
180     uint16_t base;
181     for(base = 0; base<6; base++){

```

```

182     EPWM_setClockPrescaler(pwmHandle[base], EPWM_CLOCK_DIVIDER_1,
    ↪ EPWM_HSCLOCK_DIVIDER_1);
183     EPWM_setTimeBasePeriod(pwmHandle[base], TBPRD); //TPWM =
    ↪ 2(TBPRD)(TBCLK), TBCLK = 10 ns -> 100 kHz
184     EPWM_setPhaseShift(pwmHandle[base], (uint16_t)
    ↪ (TBPRD-(float)TBPRD*0.2f*base)); //Symmetric PS-PWM with Q5 centered
    ↪ at t=0
185     EPWM_setTimeBaseCounter(pwmHandle[base], (uint16_t)
    ↪ (TBPRD-(float)TBPRD*0.2f*base)); //Symmetric PS-PWM with Q5 centered
    ↪ at t=0
186     EPWM_setTimeBaseCounterMode(pwmHandle[base], EPWM_COUNTER_MODE_UP_DOWN);
187
188     EPWM_setActionQualifierShadowLoadMode(pwmHandle[base],
    ↪ EPWM_ACTION_QUALIFIER_A, EPWM_AQ_LOAD_ON_CNTR_ZERO);
189     EPWM_setActionQualifierShadowLoadMode(pwmHandle[base],
    ↪ EPWM_ACTION_QUALIFIER_B, EPWM_AQ_LOAD_ON_CNTR_ZERO);
190     EPWM_setActionQualifierActionComplete(pwmHandle[base],
    ↪ EPWM_AQ_OUTPUT_A,
    ↪ (EPWM_ActionQualifierEventAction)(EPWM_AQ_OUTPUT_LOW_UP_CMPA |
    ↪ EPWM_AQ_OUTPUT_HIGH_DOWN_CMPA));
191     EPWM_setDeadBandDelayMode(pwmHandle[base], EPWM_DB_RED, true);
192     EPWM_setDeadBandDelayMode(pwmHandle[base], EPWM_DB_FED, true);
193     EPWM_setDeadBandDelayPolarity(pwmHandle[base], EPWM_DB_FED,
    ↪ EPWM_DB_POLARITY_ACTIVE_LOW);
194     EPWM_setRisingEdgeDelayCount(pwmHandle[base], 5); //50 ns of deadtime
195     EPWM_setFallingEdgeDelayCount(pwmHandle[base], 5);
196     EPWM_setCounterCompareShadowLoadMode(pwmHandle[base], EPWM_COUNTER_COMPA,
    ↪ RE_A, EPWM_COMP_LOAD_ON_CNTR_PERIOD);
197     EPWM_setCounterCompareShadowLoadMode(pwmHandle[base], EPWM_COUNTER_COMPA,
    ↪ RE_B, EPWM_COMP_LOAD_ON_CNTR_PERIOD);
198     EPWM_setTripZoneAction(pwmHandle[base], EPWM_TZ_ACTION_EVENT_TZA,
    ↪ EPWM_TZ_ACTION_LOW);
199
200     EPWM_setCounterCompareValue(pwmHandle[base], EPWM_COUNTER_COMPARE_A, 0);
201     EPWM_setCounterCompareValue(pwmHandle[base], EPWM_COUNTER_COMPARE_B,
    ↪ TBPRD*0.5f);
202
203 }
204
205 EPWM_disablePhaseShiftLoad(EPWM1_BASE);
206 EPWM_setSyncOutPulseMode(EPWM1_BASE, EPWM_SYNC_OUT_PULSE_ON_COUNTER_ZERO);
207 SysCtl_setSyncInputConfig(SYSCTL_SYNC_IN_EPWM4, SYSCTL_SYNC_IN_SRC_EPWM1SYNCOUT);
208
209     EPWM_setInterruptSource(EPWM2_BASE, EPWM_INT_TBCTR_ZERO);
210     EPWM_setInterruptEventCount(EPWM2_BASE, 1); // trigger interrupt every event
211     EPWM_enableInterrupt(EPWM2_BASE);
212
213     EPWM_setSyncOutPulseMode(EPWM2_BASE, EPWM_SYNC_OUT_PULSE_ON_EPWMxSYNCIN);
214     EPWM_enablePhaseShiftLoad(EPWM2_BASE);
215     EPWM_setPhaseShift(EPWM2_BASE, 0);

```

```

216     EPWM_setTimeBaseCounter(EPWM2_BASE,0);
217     EPWM_setCountModeAfterSync(EPWM2_BASE, EPWM_COUNT_MODE_UP_AFTER_SYNC);
218     for(base = 1; base < 3; base++){
219         if(base == 1)
220             EPWM_setSyncOutPulseMode(pwmHandle[base],
221                                     ↪ EPWM_SYNC_OUT_PULSE_ON_EPWMxSYNCIN);
222     EPWM_enablePhaseShiftLoad(pwmHandle[base]);
223     EPWM_setPhaseShift(pwmHandle[base],
224                       ↪ (uint16_t)((float)TBPRD*2*0.2f*base)); //Symmetric PS-PWM with Q5
225                       ↪ centered at t=0
226     EPWM_setTimeBaseCounter(pwmHandle[base],
227                       ↪ (uint16_t)((float)TBPRD*2*0.2f*base)); //Symmetric PS-PWM with Q5
228                       ↪ centered at t=0
229     EPWM_setCountModeAfterSync(pwmHandle[base], EPWM_COUNT_MODE_DOWN_AFTER_SYNC);
230 }
231
232     for(base = 3; base<5; base++){
233         EPWM_setSyncOutPulseMode(pwmHandle[base],
234                                 ↪ EPWM_SYNC_OUT_PULSE_ON_EPWMxSYNCIN);
235     EPWM_enablePhaseShiftLoad(pwmHandle[base]);
236     EPWM_setPhaseShift(pwmHandle[base],
237                       ↪ (uint16_t)((float)TBPRD*0.2f*4-(float)TBPRD*2*0.2f*(base-3)));
238                       ↪ //Symmetric PS-PWM with Q5 centered at t=0
239     EPWM_setTimeBaseCounter(pwmHandle[base],
240                       ↪ (uint16_t)((float)TBPRD*0.2f*4-(float)TBPRD*2*0.2f*(base-3)));
241                       ↪ //Symmetric PS-PWM with Q5 centered at t=0
242     EPWM_setCountModeAfterSync(pwmHandle[base],
243                               ↪ EPWM_COUNT_MODE_UP_AFTER_SYNC);
244 }
245
246     return;
247 }
248
249 void configureDAC(void){
250     DAC_setReferenceVoltage(DACA_BASE, DAC_REF_ADC_VREFHI);
251     DAC_setShadowValue(DACA_BASE, 0);
252     DAC_enableOutput(DACA_BASE);
253     DEVICE_DELAY_US(10); // Delay for buffered DAC to power up
254
255     DAC_setReferenceVoltage(DACC_BASE, DAC_REF_ADC_VREFHI);
256     DAC_setShadowValue(DACC_BASE, 0);
257     DAC_enableOutput(DACC_BASE);
258     DEVICE_DELAY_US(10); // Delay for buffered DAC to power up
259     return;
260 }
261
262 void configureADC(void){
263     //Analog Connections
264     //Vline A1
265     //Iin ADCIN15
266     //vc4 D4

```

```

255      //vc3 D3
256      //vc2 D2
257      //vc1 D1
258      //PREVIOUSLY
259      //vc4 D5
260      //vc3 D4
261      //vc2 D3
262      //vc1 D2
263      //iL C2
264      //vin B2
265      //vout D0
266
267      uint16_t base;
268      for(base = 0; base < 4; base++){
269          // Set 12-bit single ended conversion mode
270          ADC_setMode(adCHandle[base], ADC_RESOLUTION_12BIT, ADC_MODE_SINGLE_ENDED);
271          // Set main clock scaling factor (100MHz max clock for the ADC module)
272          ADC_setPrescaler(adCHandle[base], ADC_CLK_DIV_4_0);
273          // set the ADC interrupt pulse generation to end of conversion
274          ADC_setInterruptPulseMode(adCHandle[base], ADC_PULSE_END_OF_CONV);
275          // enable the ADC
276          ADC_enableConverter(adCHandle[base]);
277          // set priority of SOC's
278          ADC_setSOCPriority(adCHandle[base], ADC_PRI_ALL_HIPRI);
279      }
280      // delay to allow ADCs to power up
281      DEVICE_DELAY_US(1500U);
282
283      ADC_setupSOC(ADCA_BASE,ADC_SOC_NUMBER0,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN15,14); //Iin
284      ↪ SOC
285      ADC_setupSOC(ADCA_BASE,ADC_SOC_NUMBER1,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN1,300);
286      ↪ //Vline SOC
287      //ADC_setupSOC(ADCA_BASE,ADC_SOC_NUMBER1,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN1,14);
288      ↪ //Vline SOC
289
290      ADC_setupSOC(ADCB_BASE,ADC_SOC_NUMBER0,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN2,14); //Vin
291      ↪ SOC
292
293      ADC_setupSOC(ADCC_BASE,ADC_SOC_NUMBER0,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN2,14); //iL
294      ↪ SOC
295
296      ADC_setupSOC(ADCD_BASE,ADC_SOC_NUMBER0,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN1,14); //vc1
297      ADC_setupSOC(ADCD_BASE,ADC_SOC_NUMBER1,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN2,14); //vc2
298      ADC_setupSOC(ADCD_BASE,ADC_SOC_NUMBER2,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN3,14); //vc3
299      ADC_setupSOC(ADCD_BASE,ADC_SOC_NUMBER3,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN4,14); //vc4
300      ADC_setupSOC(ADCD_BASE,ADC_SOC_NUMBER4,ADC_TRIGGER_SW_ONLY,ADC_CH_ADCIN0,14); //vout
301
302      //end of conversion of ADCA causes a new SOC (continuous conversion)
303      ADC_setInterruptSOCTrigger(ADCA_BASE,ADC_SOC_NUMBER0,ADC_INT_SOC_TRIGGER_ADCINT1);
304      ADC_setInterruptSOCTrigger(ADCA_BASE,ADC_SOC_NUMBER1,ADC_INT_SOC_TRIGGER_ADCINT1);

```

```

300 //end of conversion of ADCB causes a new SOC (continuous conversion)
301 ADC_setInterruptSOCTrigger(ADCB_BASE,ADC_SOC_NUMBER0,ADC_INT_SOC_TRIGGER_ADCINT1);
302
303 //ADC_setInterruptSOCTrigger(ADCC_BASE,ADC_SOC_NUMBER0,ADC_INT_SOC_TRIGGER_ADCINT1);
304
305 ADC_setInterruptSOCTrigger(ADCD_BASE,ADC_SOC_NUMBER0,ADC_INT_SOC_TRIGGER_ADCINT1);
306 ↪ //ADCD_INT1 triggers SOC 0
307 ADC_setInterruptSOCTrigger(ADCD_BASE,ADC_SOC_NUMBER1,ADC_INT_SOC_TRIGGER_ADCINT1);
308 ↪ //ADCD_INT1 triggers SOC 1
309 ADC_setInterruptSOCTrigger(ADCD_BASE,ADC_SOC_NUMBER2,ADC_INT_SOC_TRIGGER_ADCINT1);
310 ↪ 1); //ADCD_INT1 triggers SOC 2
311 ADC_setInterruptSOCTrigger(ADCD_BASE,ADC_SOC_NUMBER3,ADC_INT_SOC_TRIGGER_ADCINT1);
312 ↪ //ADCD_INT1 triggers SOC 3
313 ADC_setInterruptSOCTrigger(ADCD_BASE,ADC_SOC_NUMBER4,ADC_INT_SOC_TRIGGER_ADCINT1);
314 ↪ //ADCD_INT1 triggers SOC 4
315
316 //EOC pulses continue to be generated regardless of flag bit
317 ADC_enableContinuousMode(ADCA_BASE,ADC_INT_NUMBER1);
318 ADC_enableContinuousMode(ADCB_BASE,ADC_INT_NUMBER1);
319 //ADC_enableContinuousMode(ADCC_BASE,ADC_INT_NUMBER1);
320 ADC_enableContinuousMode(ADCD_BASE,ADC_INT_NUMBER1);
321
322 //EOC triggers ADC interrupt
323 ADC_setInterruptSource(ADCA_BASE, ADC_INT_NUMBER1, ADC_SOC_NUMBER1);
324 ADC_setInterruptSource(ADCB_BASE, ADC_INT_NUMBER1, ADC_SOC_NUMBER0);
325 ADC_setInterruptSource(ADCC_BASE, ADC_INT_NUMBER1, ADC_SOC_NUMBER0);
326 ADC_setInterruptSource(ADCD_BASE, ADC_INT_NUMBER1, ADC_SOC_NUMBER4); //ADC SOC 4
327 ↪ finishing triggers ADCD_INT1
328
329 ADC_enableInterrupt(ADCA_BASE, ADC_INT_NUMBER1);
330 ADC_enableInterrupt(ADCB_BASE, ADC_INT_NUMBER1);
331 ADC_enableInterrupt(ADCC_BASE, ADC_INT_NUMBER1);
332 ADC_enableInterrupt(ADCD_BASE, ADC_INT_NUMBER1);
333
334 ADC_forceSOC(ADCA_BASE,ADC_SOC_NUMBER1);
335 ADC_forceSOC(ADCB_BASE,ADC_SOC_NUMBER0);
336 //ADC_forceSOC(ADCC_BASE,ADC_SOC_NUMBER0);
337 ADC_forceSOC(ADCD_BASE,ADC_SOC_NUMBER4);
338 return;
339 }

```

```

1 #include "controller.h"
2
3 float Lo = 10e-6f;
4 //float Lo = 6.8e-6f;
5 float PI = 3.1415926535897932f;
6 float N = 6;
7 float C1 = 6.6e-6f;

```

```

8  float C2 = 8.8e-6f;
9  float C3 = 11e-6f;
10 float C4 = 13.2e-6f;
11 float Cin = 16*2.2e-6f;
12 float RL = 12e-3f+10e-3f+5e-3f;
13
14 float pcap = 3e3f;
15 float pL = 20e3f; //Inductor current dynamic [rad/sec]
16 float Ts = 10e-6f; //Switching/control period
17
18 float Cbuf = 9*18e-3f;//54e-3f;//18e-3*3
19 float Cout = 39.6e-6f;//2.2e-6*10
20 float Rout = 4;//1.6f;//2.66f;
21 float vo_wbw;
22 float vout_kp;
23 float vout_ki;
24
25 float Delta_d[4] = {0,0,0,0};
26 float D[5] = {0,0,0,0,0};
27 float d5 = 0;
28 float vc1, vc2, vc3, vc4;
29 float vc1_raw, vc2_raw, vc3_raw, vc4_raw;
30
31 float vc1e, vc2e, vc3e, vc4e; //Fly cap errors
32 float iin;
33 float iL, iL_ref, iL_K;
34 float iL_raw, iin_raw;
35 float iL_error, iL_error_sum, iL_error_sum_old, iL_PI_out;
36
37 float vin_raw, vout_raw;
38 float vin, vout, vout_error;
39 float vout_error_sum_old, vout_error_sum;
40
41 int Cfly_interpolation = 1; //Flag to turn on interpolation of the C(v) curve for the
   ↔ fly caps
42 int Cin_comp = 0; //flag to enable Cin displacement current term
43 int active_balance = 1; //Flag to turn on active balancing
44
45 float IL_MAX = 15; //Saturate inductor current reference
46
47 uint16_t vc1_ADC, vc2_ADC, vc3_ADC, vc4_ADC;
48 uint16_t vin_ADC, vout_ADC;
49 uint16_t iL_ADC, iin_ADC;
50
51 uint16_t vg_ADC;
52
53 float vg_raw, vg_filt;
54 float vg_offset = 1.5f;
55 float vg_max = 0;
56 float vg_min = 0;

```



```

57 float vg_offset;
58
59 float fgrid = 60;
60 float vo_fbw = 1;
61 float wn;
62
63 float vout_ref = 6;
64
65 int i, base; //for loop counting variables
66
67 float v_filt, i_filt;
68
69 float Cin_eff;
70
71 int disable_PWM = 0;
72 int dcdc = 0; //flag to enable acdc
73
74 float I_mult = 1; //0.25;
75
76 int doubleLoop = 1;
77 float wc = 6.28f*2e3f;
78 float Kp;
79 float Ki;
80
81 float KpPLL, Ti, KiPLL; //PLL Constants
82 float theta, omega, vp, qvp, vd, vq, MagV, vdSum, vdSumOld, MagVRaw; //PLL Variables
83 float vgAbs; //Cleaned up grid voltage
84 float sg, cg; //sin(theta) & cos(theta)
85 int vout_ctrler_flag;
86 int ramp_down=0;
87
88 float dd_sat = 2.5e-2f;
89
90 float u_PI;
91
92 float vFiltf3 = 5e3;
93 float iFiltf3 = 20e3;
94 float vY, iY;
95
96 float vg_scale = 95e-3;
97 float vgOff = 2037;
98 int autoVRef = 1;
99 float kdc = 0.01f; //PLL dc offset gain
100 float PLLdcInt=0;
101 float PLLdc=0;
102 void init_ctrl_gain(void){
103     vo_wbw = 2*PI*vo_fbw; //Bandwidth of output voltage loop [rad/s]
104     vout_kp = vo_wbw*(Cout+Cbuf);
105     vout_ki = vo_wbw*vout_kp/5;
106     Cin_eff = Cin+1.2*C1;

```

```

107
108     wn = 2*PI*fgrid;
109
110     KpPLL = 9.2/3*fgrid;
111     Ti = 3/fgrid*(1/__sqrt(2))*(1/__sqrt(2))/2.3;
112     KiPLL = KpPLL/Ti;
113     vp = 1;
114
115     Kp = wc*Lo;
116     Ki = wc*Kp/5;
117
118     vY = 1-__cos(2*PI*vFiltf3*Ts);
119     v_filt = -vY+__sqrt(vY*vY+2*vY);
120
121     iY = 1-__cos(2*PI*iFiltf3*Ts);
122     i_filt = -iY+__sqrt(iY*iY+2*iY);
123 }
124
125 void sample_system(void){
126     ADC_forceSOC(ADCC_BASE,ADC_SOC_NUMBER0);
127     while(ADC_getInterruptStatus(ADCC_BASE, ADC_INT_NUMBER1) == false){}
128     ADC_clearInterruptStatus(ADCC_BASE, ADC_INT_NUMBER1);
129
130     vc1_ADC = ADC_readResult(ADCRESULT_BASE,ADC_SOC_NUMBER0);
131     vc2_ADC = ADC_readResult(ADCRESULT_BASE,ADC_SOC_NUMBER1);
132     vc3_ADC = ADC_readResult(ADCRESULT_BASE,ADC_SOC_NUMBER2);
133     vc4_ADC = ADC_readResult(ADCRESULT_BASE,ADC_SOC_NUMBER3);
134
135     vin_ADC = ADC_readResult(ADCBRESULT_BASE,ADC_SOC_NUMBER0);
136     vout_ADC = ADC_readResult(ADCRESULT_BASE,ADC_SOC_NUMBER4);
137
138     iL_ADC = ADC_readResult(ADCCRESULT_BASE,ADC_SOC_NUMBER0);
139     iin_ADC = ADC_readResult(ADCARESULT_BASE,ADC_SOC_NUMBER0);
140
141     vg_ADC = ADC_readResult(ADCARESULT_BASE,ADC_SOC_NUMBER1);
142
143     //convert counts into voltages
144     vc1_raw = (float) vc1_ADC*3/4096*134.3333f; //Assuming 1.24M top resistor in
    ↪ resistor divider
145     vc2_raw = (float) vc2_ADC*3/4096*134.3333f;
146     vc3_raw = (float) vc3_ADC*3/4096*134.3333f;
147     vc4_raw = (float) vc4_ADC*3/4096*134.3333f;
148     vin_raw = (float) vin_ADC*3/4096*134.3333f;
149     vout_raw = (float) vout_ADC*3/4096*134.3333f;
150     iL_raw = (float) ((float) iL_ADC*3/4096-1.25f)*10; //Gain of 20 LT1999 5 mOhm
    ↪ current shunt
151     iin_raw = (float) ((float) iin_ADC*3/4096-1.25f)*50; //Gain of 10 LT1999 2 mOhm
    ↪ current shunt
152     vg_raw = ((float) vg_ADC-vgOff)*vg_scale;
153     //PLL

```

```

154     PLLdcInt += Ts*kdc*(vg_raw-vp-PLLdc);
155     if(PLLdcInt>.1)
156         PLLdcInt = .1;
157     if(PLLdcInt<-.1)
158         PLLdcInt = -.1;
159     PLLdc=PLLdcInt*omega;
160     //vp += Ts*omega*(SQRT2*(vg_raw-vp-PLLdc)-qvp);
161     vp += Ts*omega*(SQRT2*(vg_raw-vp-PLLdc)-qvp);
162     qvp += Ts*omega*vp;
163     vd = vp*__cos(theta)+qvp*__sin(theta);
164     vq = qvp*__cos(theta)-vp*__sin(theta);
165     MagVRaw = __sqrt(vd*vd+vq*vq);
166     vd = vd/MagVRaw;
167     vdSumOld = vdSum;
168     vdSum += vd*Ts;
169     omega = KpPLL*vd+KiPLL*vdSum;
170
171     if(omega>500){
172         omega = 500;
173         if(vd>0)
174             vdSum = vdSumOld;
175     }
176     else if(omega<300){
177         omega = 300;
178         if(vd<0)
179             vdSum = vdSumOld;
180     }
181
182     theta += omega*Ts;
183     if(theta>6.28f)
184         theta = 0;
185     sg = __sin(theta);
186     cg = __cos(theta);
187     MagV = MagV*(1-1e-5)+MagVRaw*1e-5;
188     vgAbs = fabsf(MagV*sg);
189     //DAC_setShadowValue(DACC_BASE, 2048+vp/20.0f*2048);
190     //exponentially filter incoming signals
191     vc1 = vc1*(1-v_filt)+v_filt*vc1_raw;
192     vc2 = vc2*(1-v_filt)+v_filt*vc2_raw;
193     vc3 = vc3*(1-v_filt)+v_filt*vc3_raw;
194     vc4 = vc4*(1-v_filt)+v_filt*vc4_raw;
195     vin = vin*(1-v_filt)+v_filt*vin_raw;
196     vout = vout*(1-v_filt)+v_filt*vout_raw;
197     iL = iL*(1-i_filt)+i_filt*iL_raw;
198     iin = iin*(1-i_filt)+i_filt*iin_raw;
199 }
200
201 void execute_controller(void){
202     if ((vgAbs<vout) || (dcdc && vg_filt<vout && vg_filt>-vout )){
203         //if ((MagV*vSOGI[0]<vout && vSOGI[0]>-vout) || (dcdc && vg_filt<vout &&
204         ↪ vg_filt>-vout )) && 0){

```

```

204         disable_PWM = 1;
205         for(base = 0; base<5; base++){
206             EPWM_forceTripZoneEvent(pwmHandle[base],EPWM_TZ_FORCE_EVENT_OST
                ↪ );
207         }
208         GPIO_writePin(PWMHA, 0);
209         GPIO_writePin(PWMLB, 1);
210         GPIO_writePin(PWMHB, 0);
211         GPIO_writePin(PWMLA, 1);
212         //Reset integrators on zero-crossing
213         iL_error_sum = 0;
214         vout_ctrler_flag = 1;
215     }
216     else
217         disable_PWM = 0;
218     if(disable_PWM == 0){
219         if(sg > 0 || (dcdc && vg_filt>0)){
220             GPIO_writePin(PWMHA, 1);
221             GPIO_writePin(PWMLB, 0);
222             GPIO_writePin(PWMHB, 0);
223             GPIO_writePin(PWMLA, 1);
224         }
225         else{
226             GPIO_writePin(PWMHB, 1);
227             GPIO_writePin(PWMLA, 0);
228             GPIO_writePin(PWMHA, 0);
229             GPIO_writePin(PWMLB, 1);
230         }
231         if (ramp_down && vout_ref > 6.25)
232             vout_ref -= 5e-6; //ramps down the output voltage at 0.5
                ↪ V/sec
233         else if(autoVRef)
234             vout_ref = MagV*0.2828f;
235         if (vout_ctrler_flag){ //Update the vout controller every half cycle
236             vout_error = vout_ref-vout;
237             vout_error_sum_old = vout_error_sum;
238             vout_error_sum += vout_error/120.0f;
239             vout_ctrler_flag = 0;
240         }
241         if(dcdc)
242             iL_ref = vout_error*vout_kp+vout_error_sum*vout_ki;
243         else{
244             iL_K = vout_error*vout_kp+vout_error_sum*vout_ki;
245             iL_ref = iL_K*sg*sg;
246             if(Cin_comp)
247                 iL_ref += wn*Cin_eff/vout_ref*MagV*MagV*sg*cg;
248         }
249         if (iL_ref > IL_MAX){
250             iL_ref = IL_MAX; //Saturate
251             if(vout_error > 0)

```

```

252         vout_error_sum = vout_error_sum_old; //Conditional
           ↪ Integration
253     }else if (iL_ref < -1){
254         iL_ref = -1; //Saturate
255         if(vout_error < 0)
256             vout_error_sum = vout_error_sum_old; //Conditional
           ↪ Integration
257     }
258     vc1e = vin/(N-1)-vc1;
259     vc2e = 2*vin/(N-1)-vc2;
260     vc3e = 3*vin/(N-1)-vc3;
261     vc4e = 4*vin/(N-1)-vc4;
262     if(Cfly_interpolation){ //Update C given present capacitance voltage
263         C1 = 4*(-1e-8f*vc1+2e-6f);
264         C2 = 4*(-1e-8f*vc2+2e-6f);
265         C3 = 4*(-1e-8f*vc3+2e-6f);
266         C4 = 4*(-1e-8f*vc4+2e-6f);
267     }
268     iL_error = iL_ref-iL;
269     iL_error_sum_old = iL_error_sum;
270     iL_error_sum += iL_error*Ts;
271     if(doubleLoop)
272         iL_PI_out = iL_error/I_mult + I_mult*pL*iL_error_sum;
273     else
274         u_PI = iL_error*Kp + iL_error_sum*Ki;
275
276     if(doubleLoop){
277         if(iL_PI_out > IL_MAX){
278             iL_PI_out = IL_MAX; //Saturate
279             if(iL_error > 0)
280                 iL_error_sum = iL_error_sum_old; //conditional
           ↪ integration
281         } else if(iL_PI_out < -IL_MAX){
282             iL_PI_out = -IL_MAX; //Saturate
283             if(iL_error < 0)
284                 iL_error_sum = iL_error_sum_old; //conditional
           ↪ integration
285         }
286     } else{
287         if(u_PI > vgAbs){
288             u_PI = vgAbs; //Saturate
289             if(iL_error > 0)
290                 iL_error_sum = iL_error_sum_old; //conditional
           ↪ integration
291         }
292         if(u_PI < -vout){
293             u_PI = -vout; //Saturate
294             if(iL_error < 0)
295                 iL_error_sum = iL_error_sum_old; //conditional
           ↪ integration

```

```

296     }
297 }
298 if (iL_ref!=0 && active_balance){
299     Delta_d[0] = C1*pcap/iL_ref*vc1e;
300     Delta_d[1] = C2*pcap/iL_ref*vc2e;
301     Delta_d[2] = C3*pcap/iL_ref*vc3e;
302     Delta_d[3] = C4*pcap/iL_ref*vc4e;
303     for(i = 0;i<4;i++){
304         Delta_d[i] = (Delta_d[i] > dd_sat) ? dd_sat :
305             ↪ Delta_d[i];
306         Delta_d[i] = (Delta_d[i] < -dd_sat) ? -dd_sat :
307             ↪ Delta_d[i];
308     }
309     if(dcdc)
310         D[4] = ((iL_PI_out-iL)*Lo*pL+vout)/vin+1/(N-1)*(Delta_d[
311             ↪ 0]+Delta_d[1]*2+Delta_d[2]*3+Delta_d[3]*4);
312         ↪
313     else{
314         if(doubleLoop)
315             D[4] = ((iL_PI_out-iL)*Lo*pL+vout)/vgAbs+1/(N-1)
316             ↪ *(Delta_d[0]+Delta_d[1]*2+Delta_d[2]*3+Del
317             ↪ ta_d[3]*4);
318         else
319             D[4] = (u_PI+vout)/vgAbs+1/(N-1)*(Delta_d[0]+De
320             ↪ lta_d[1]*2+Delta_d[2]*3+Delta_d[3]*4);
321             ↪
322     }
323     //D[4] = (iL_PI_out-iL)*Lo*pL/vin+vout/vin+iL_ref*RL/vin+1/(N-1)
324     ↪ *(Delta_d[0]+Delta_d[1]*2+Delta_d[2]*3+Delta_d[3]*4);
325     ↪
326 }
327 else{
328     if(dcdc){
329         if(doubleLoop)
330             D[4] = ((iL_PI_out-iL)*Lo*pL+vout)/vin;
331         else
332             D[4] = (u_PI+vout)/vin;
333     }else{
334         if(doubleLoop)
335             D[4] = ((iL_PI_out-iL)*Lo*pL+vout)/vgAbs;
336         else
337             D[4] = (u_PI+vout)/vgAbs;
338     }
339     Delta_d[0] = 0;
340     Delta_d[1] = 0;
341     Delta_d[2] = 0;
342     Delta_d[3] = 0;
343 }
344 D[3] = D[4] - Delta_d[3];
345 D[2] = D[3] - Delta_d[2];

```

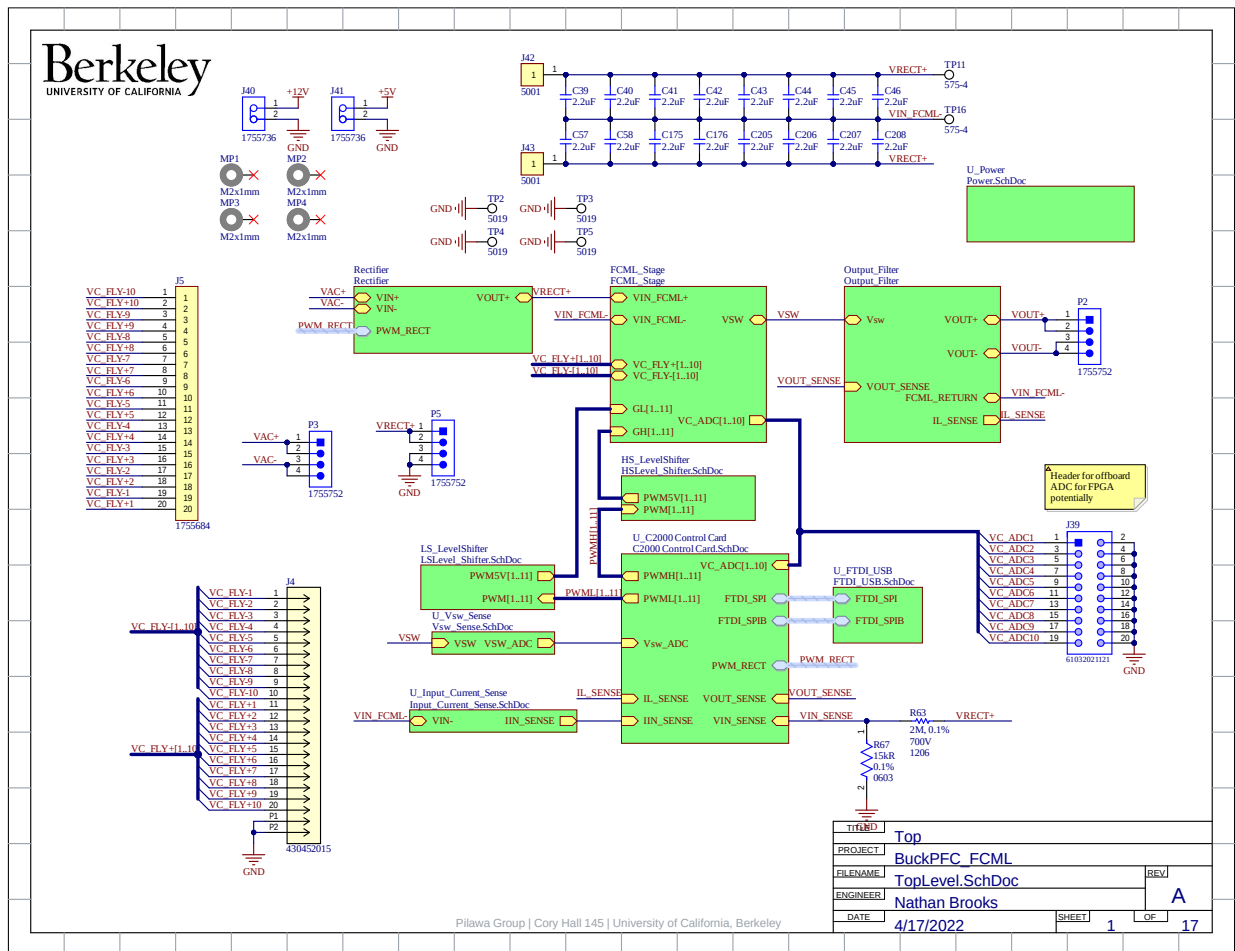
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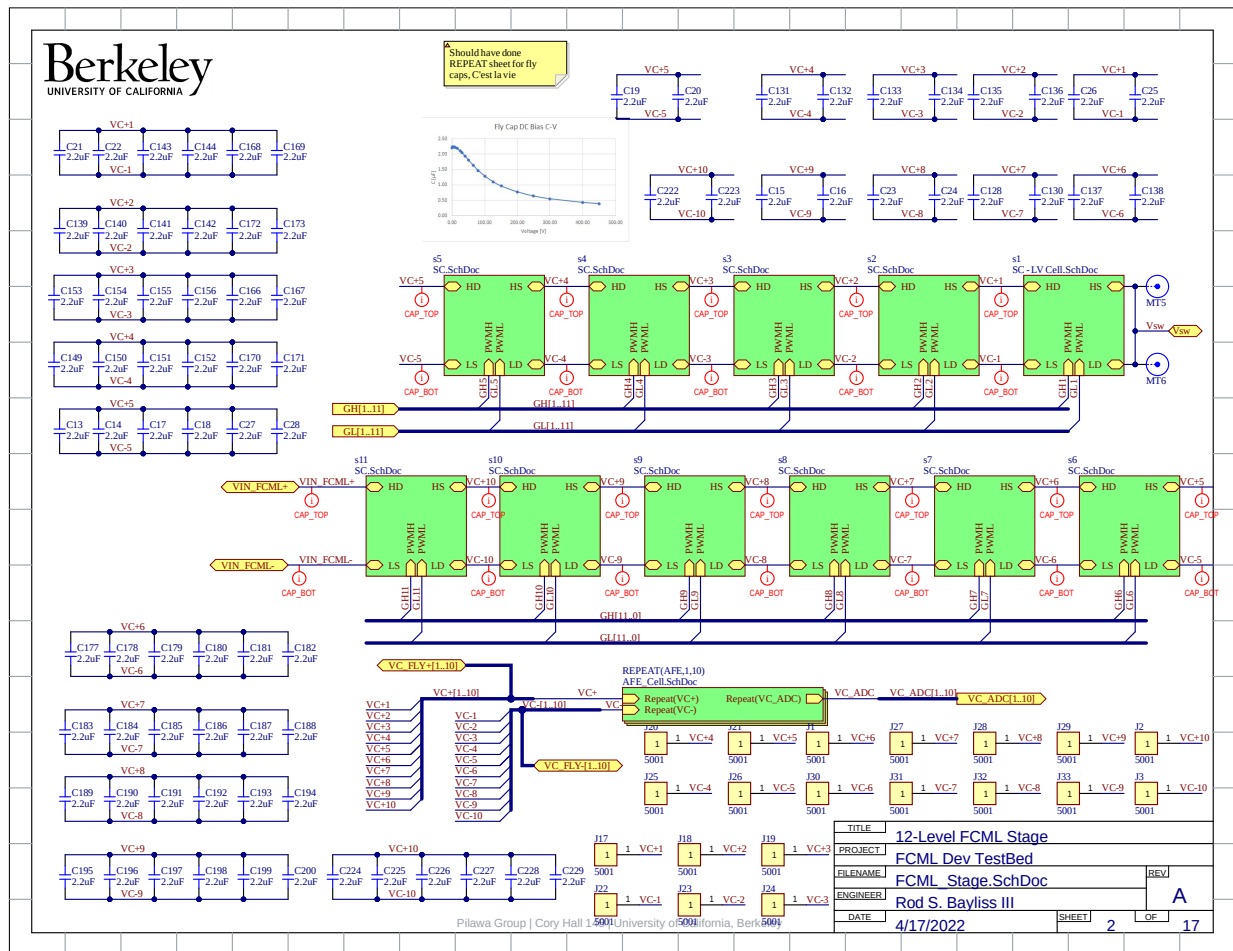
336         D[1] = D[2] - Delta_d[1];
337         D[0] = D[1] - Delta_d[0];
338         for(i = 0;i<5;i++){//Saturate duties
339             D[i] = (D[i] > 1) ? 1 : D[i];
340             D[i] = (D[i] < 0) ? 0 : D[i];
341         }
342         EPWM_setCounterCompareValue(EPWM1_BASE,EPWM_COUNTER_COMPARE_A,(uint16_t)
↪      ) (D[4]*TBPRD));
343         EPWM_setCounterCompareValue(EPWM2_BASE,EPWM_COUNTER_COMPARE_A,(uint16_t)
↪      ) (D[3]*TBPRD));
344         EPWM_setCounterCompareValue(EPWM3_BASE,EPWM_COUNTER_COMPARE_A,(uint16_t)
↪      ) (D[2]*TBPRD));
345         EPWM_setCounterCompareValue(EPWM4_BASE,EPWM_COUNTER_COMPARE_A,(uint16_t)
↪      ) (D[1]*TBPRD));
346         EPWM_setCounterCompareValue(EPWM5_BASE,EPWM_COUNTER_COMPARE_A,(uint16_t)
↪      ) (D[0]*TBPRD));
347         if(EPWM_getTripZoneFlagStatus(pwmHandle[0])!=0) {
348             for(base = 0; base<5; base++){
349                 EPWM_clearTripZoneFlag(pwmHandle[base],
↪      EPWM_TZ_FLAG_OST);
350             }
351         }
352     }
353 }

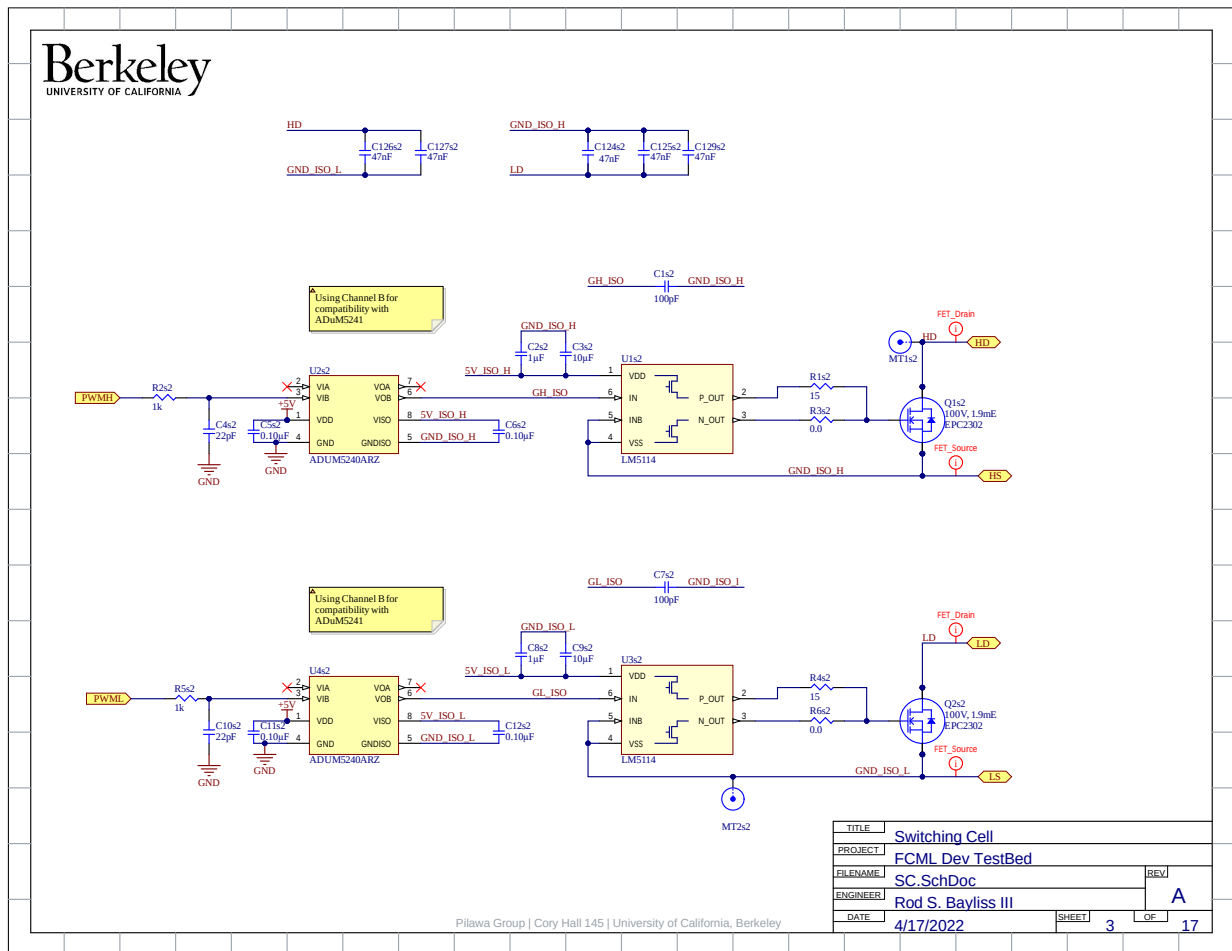
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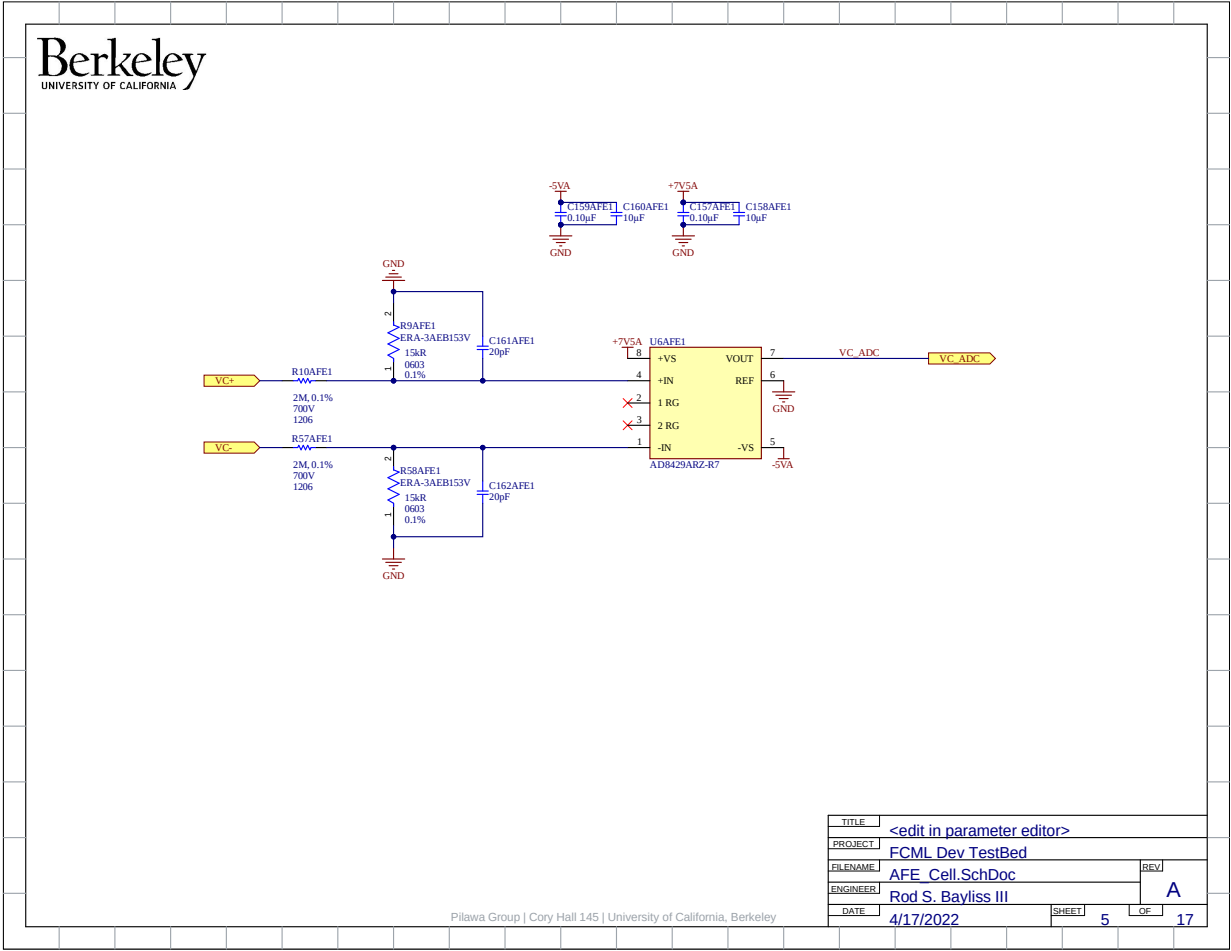
Appendix C

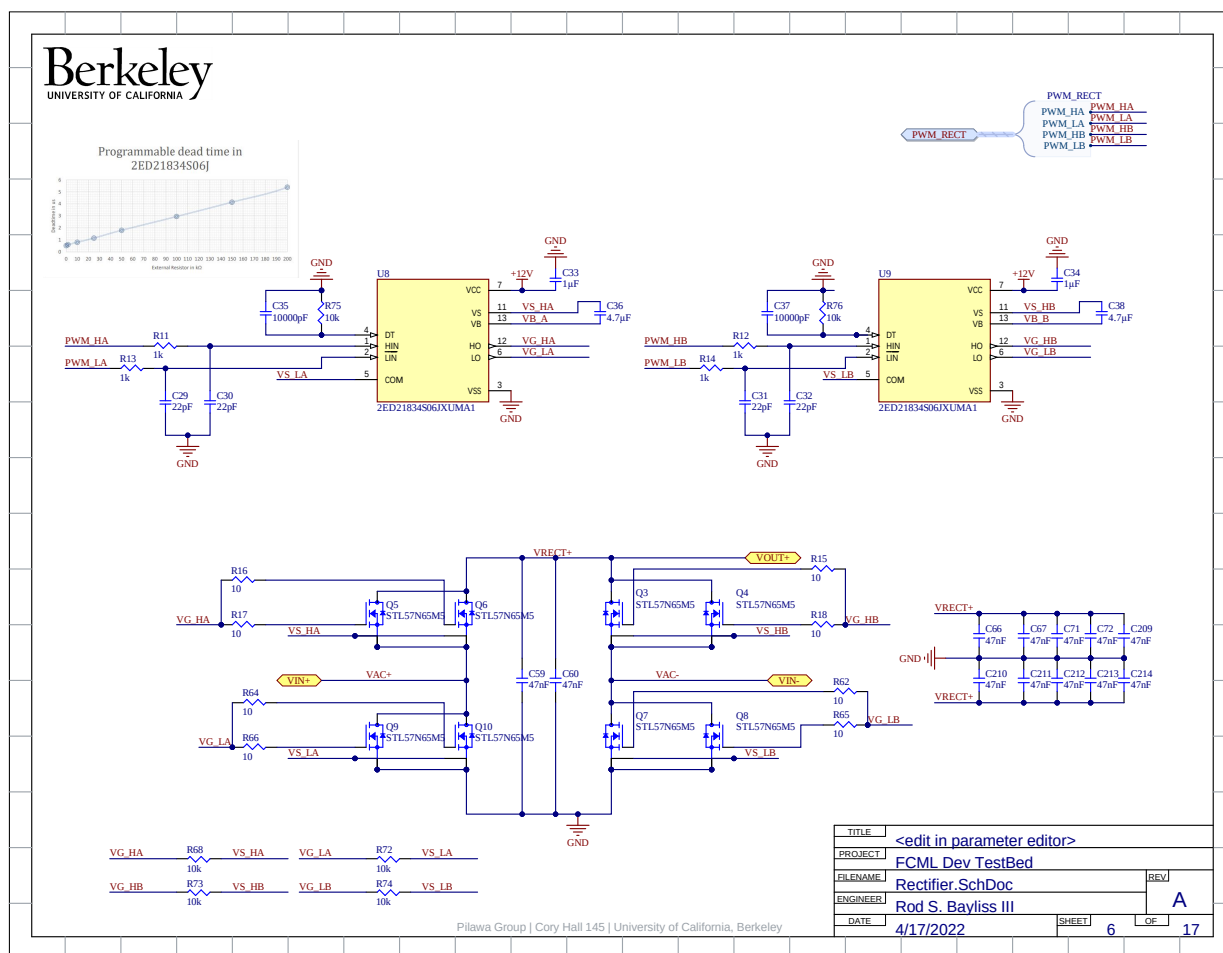
12-Level FCML Converter Schematics

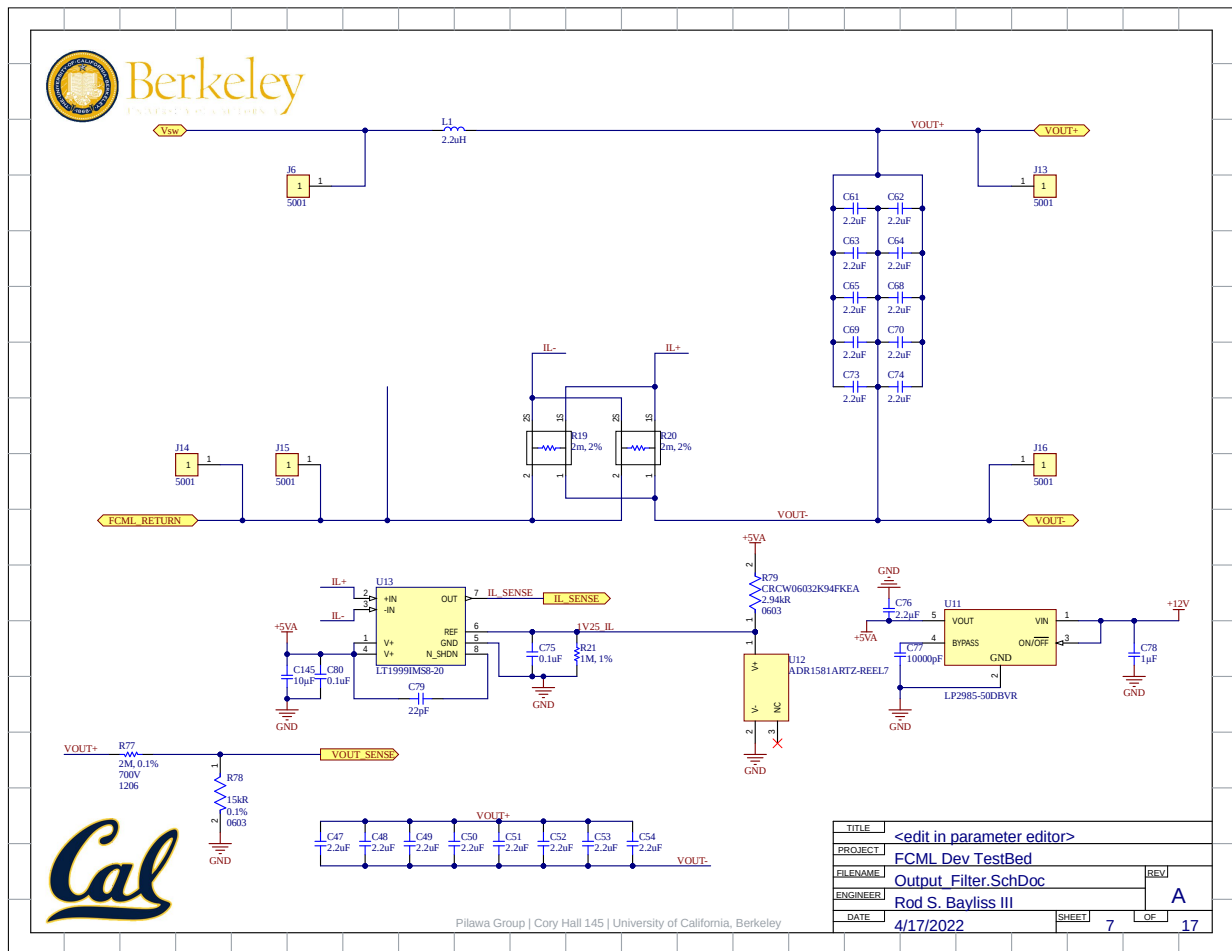


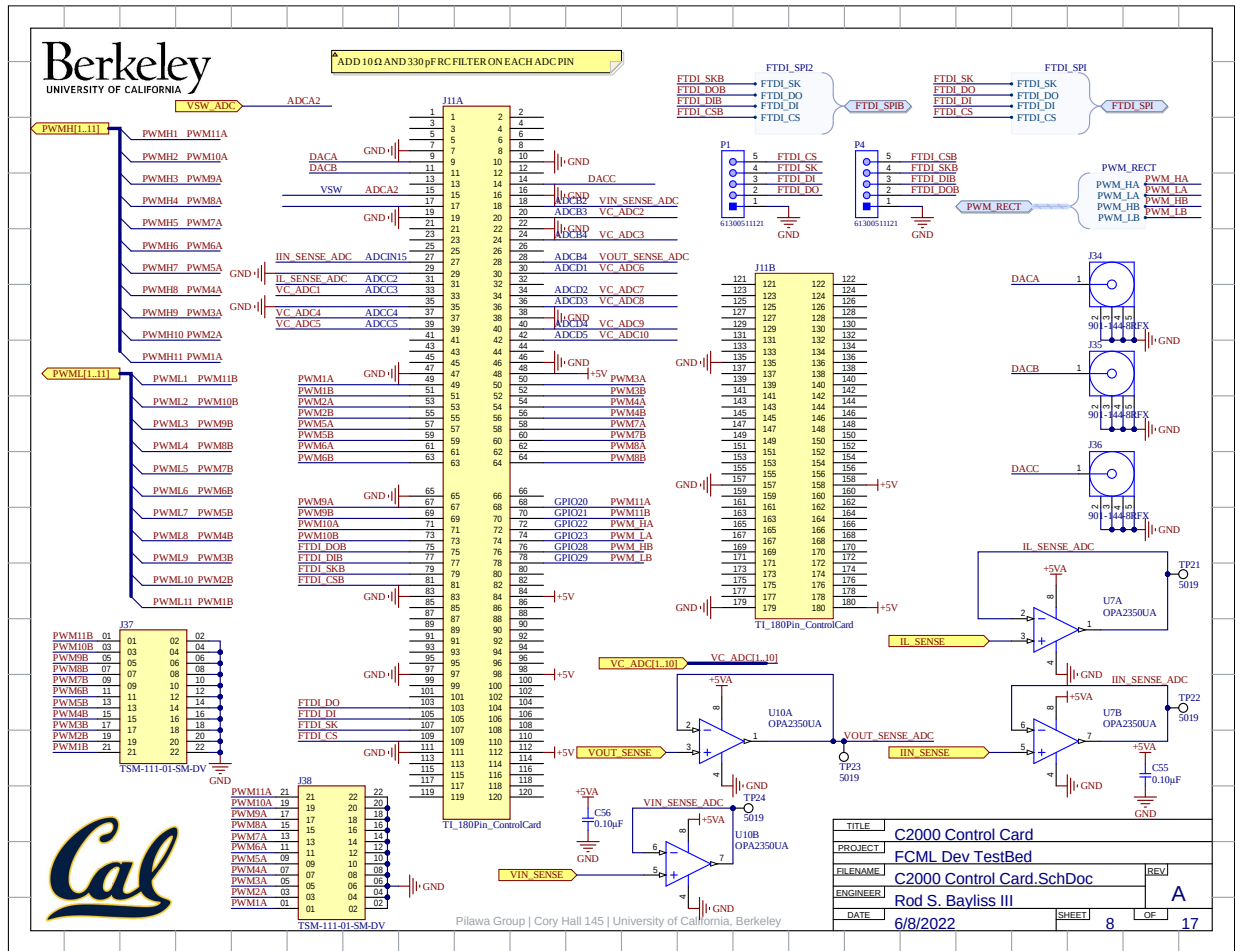


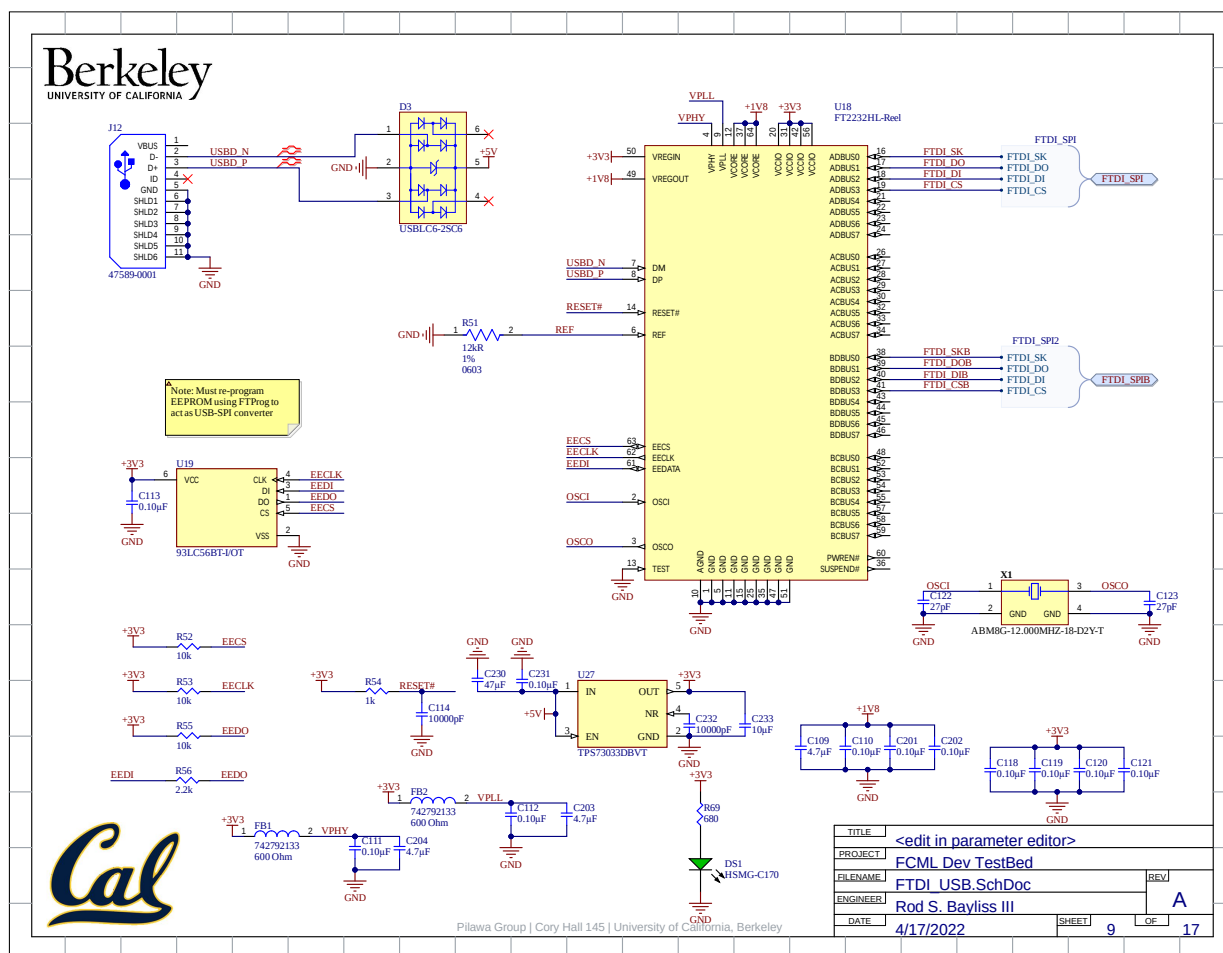


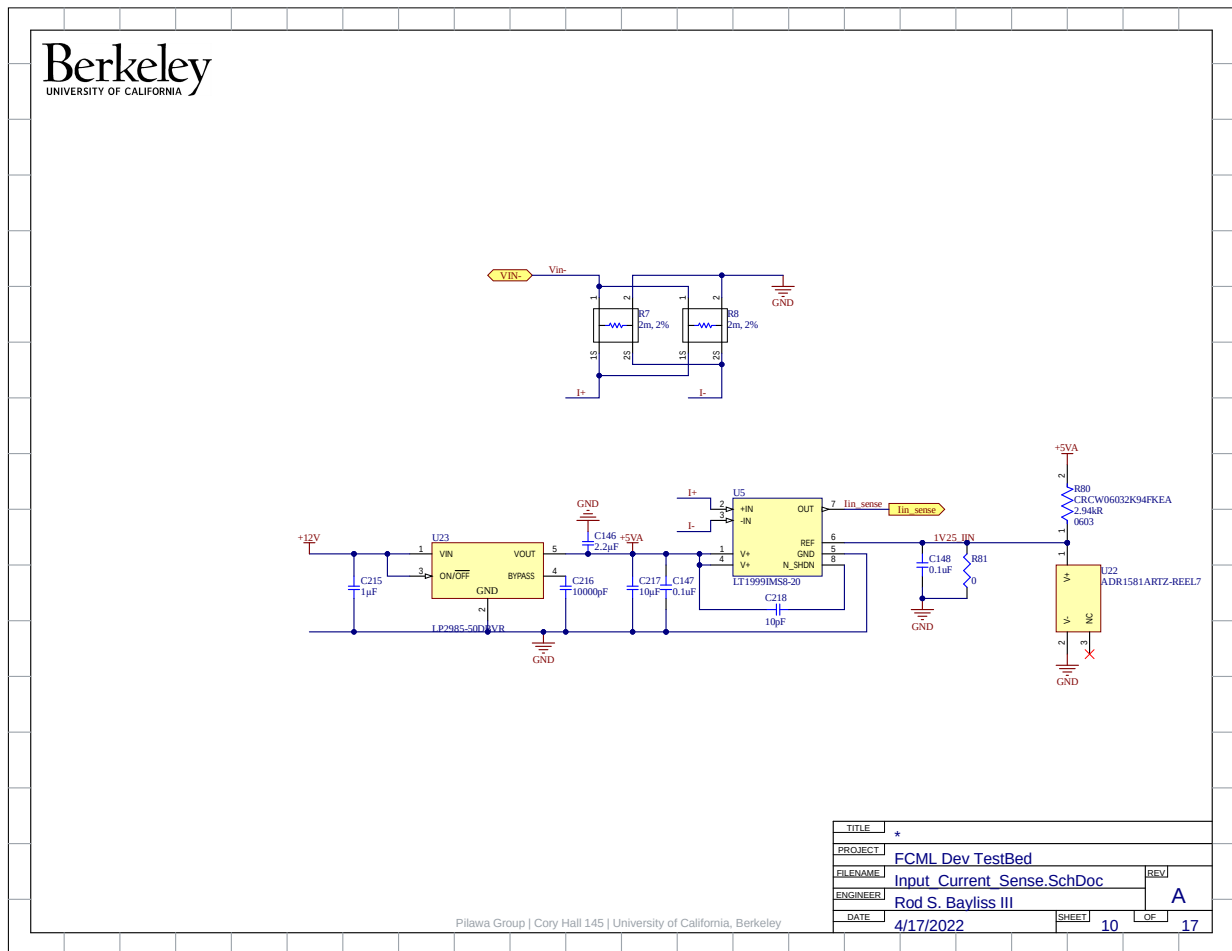


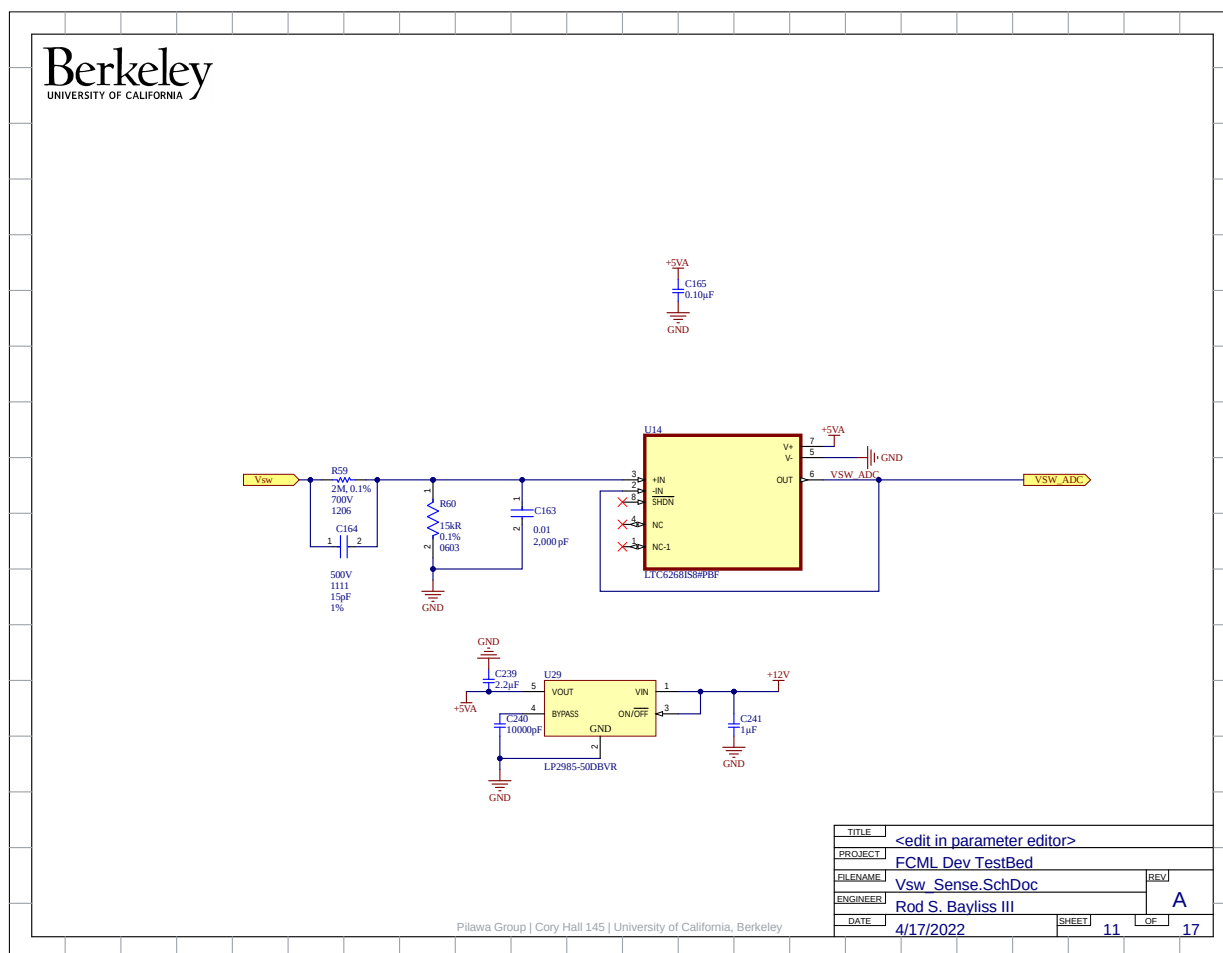


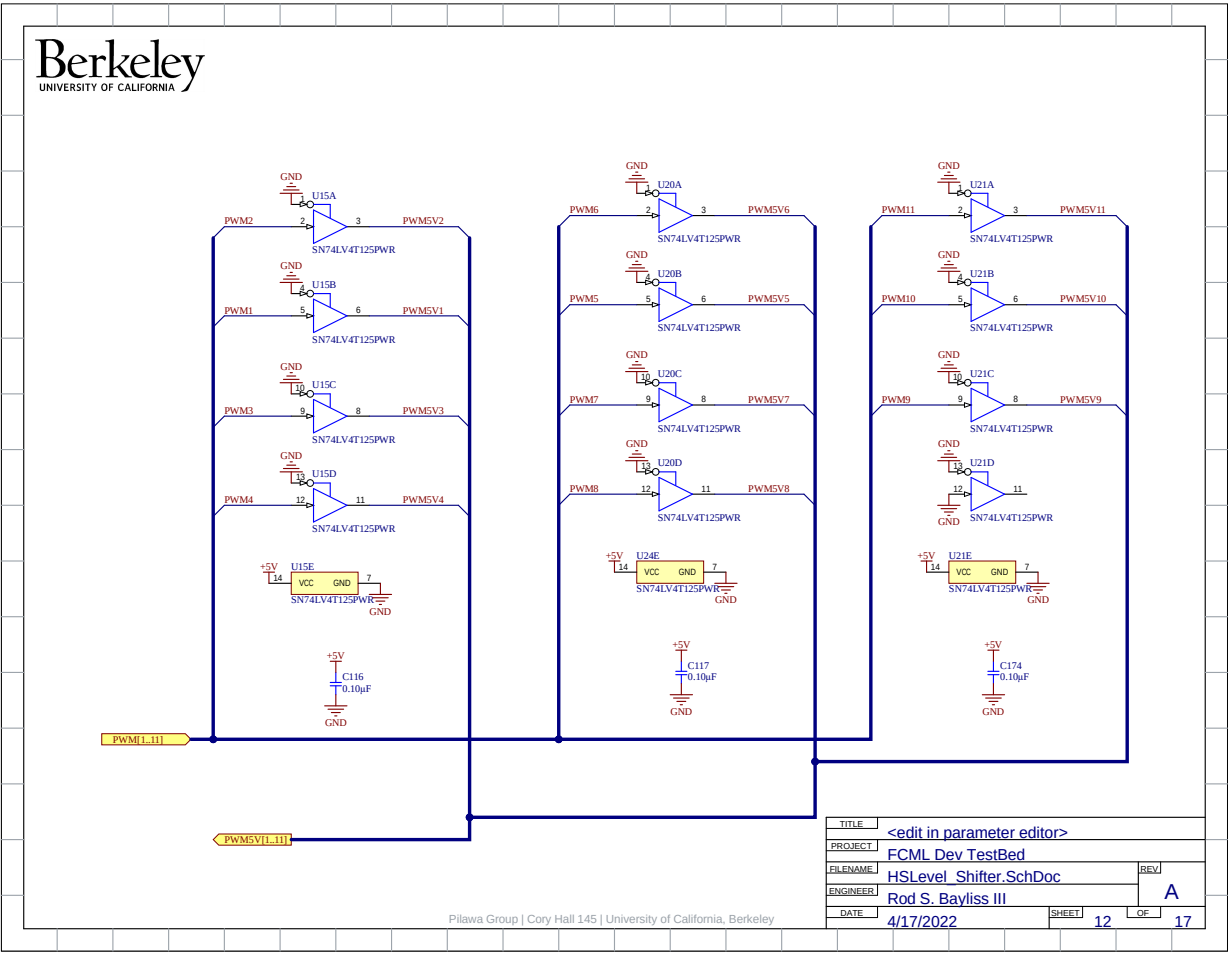


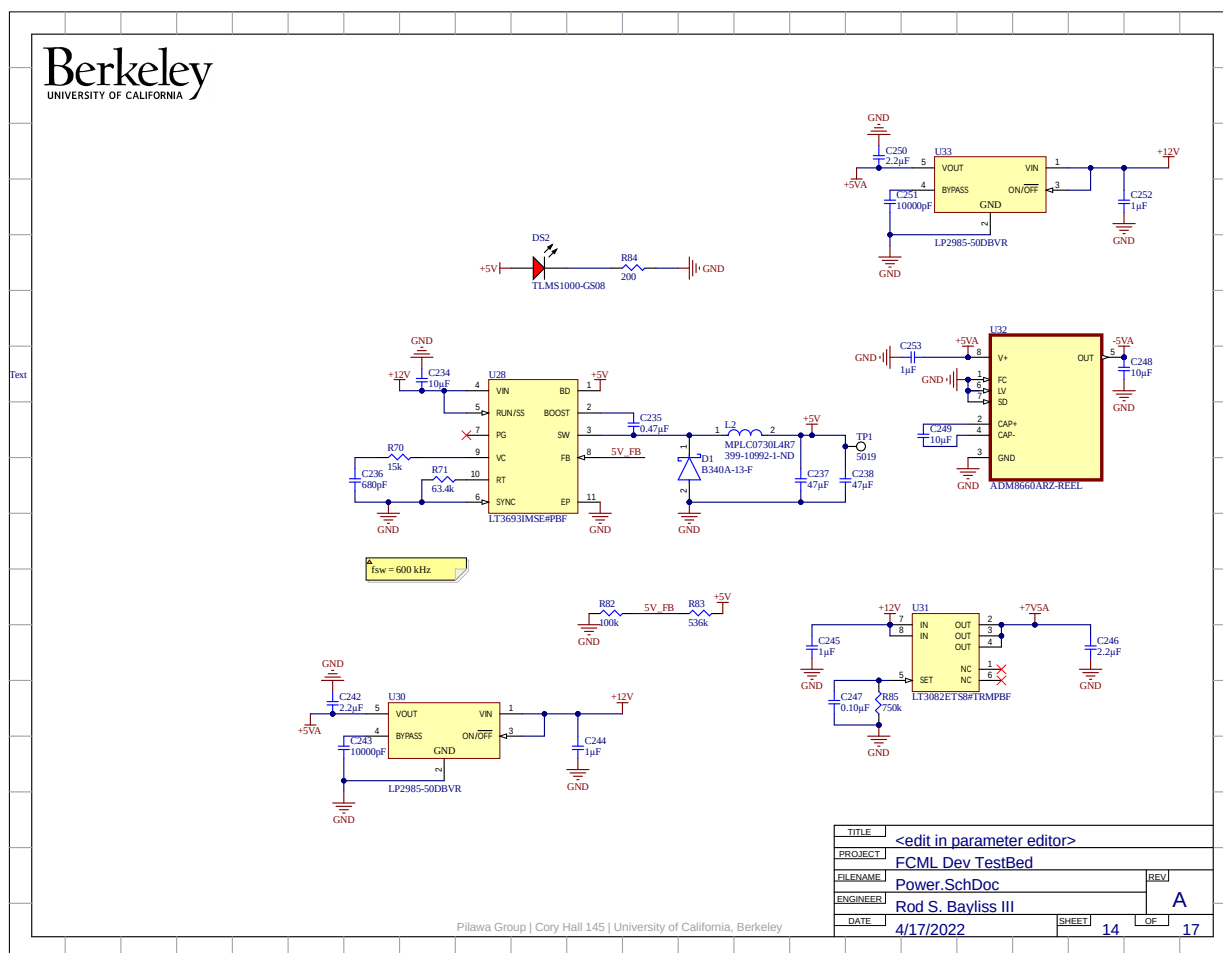


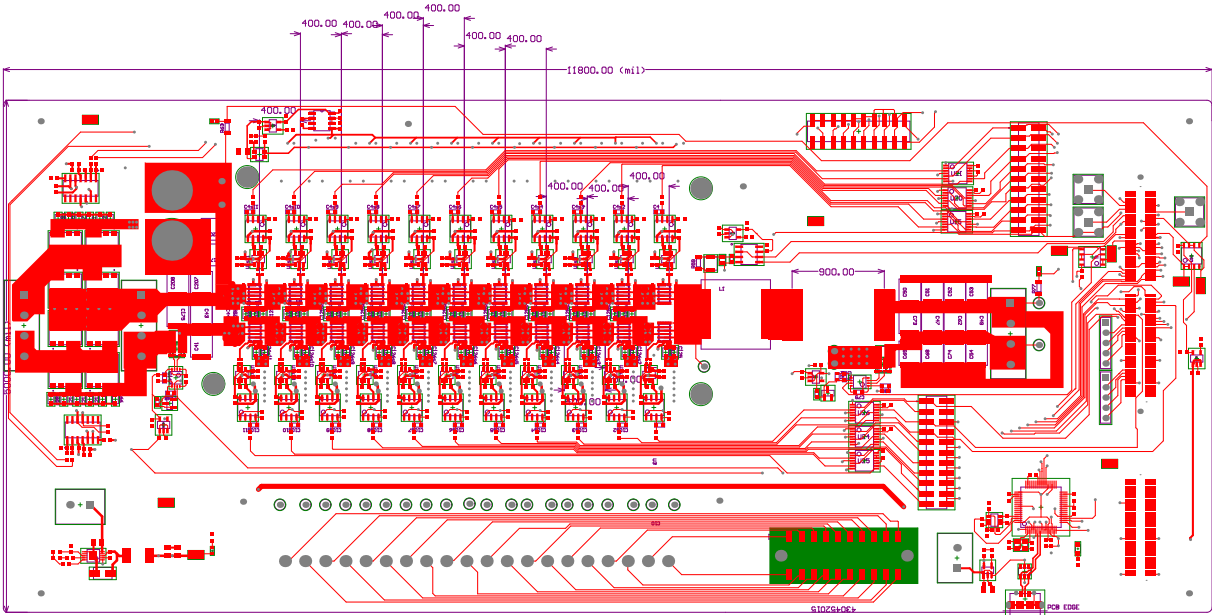


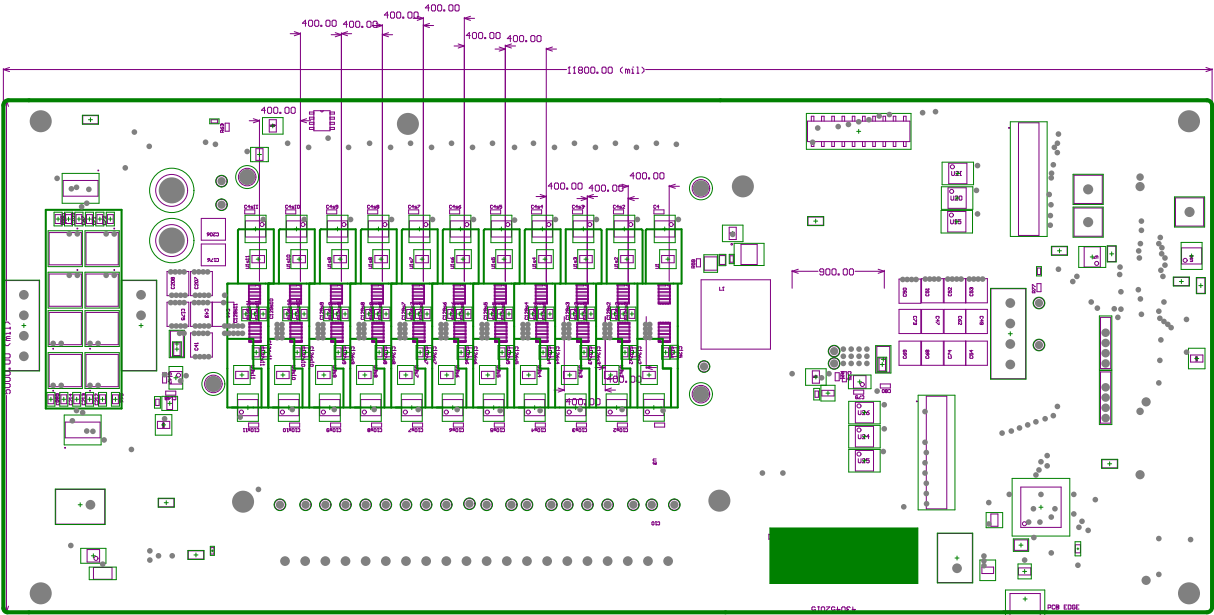


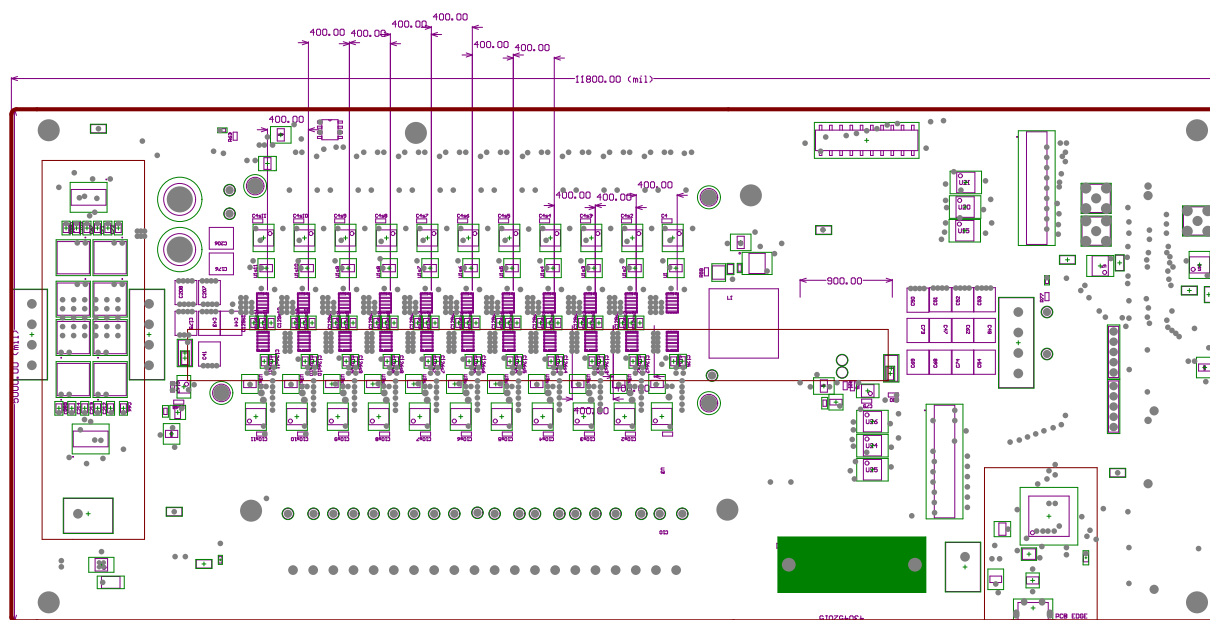


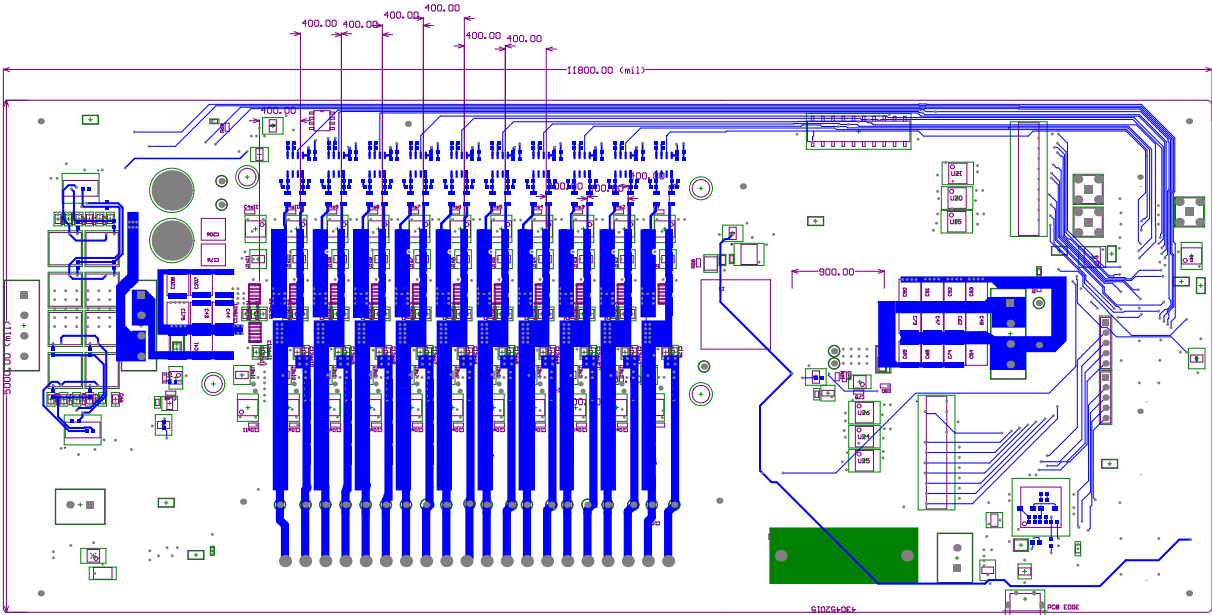


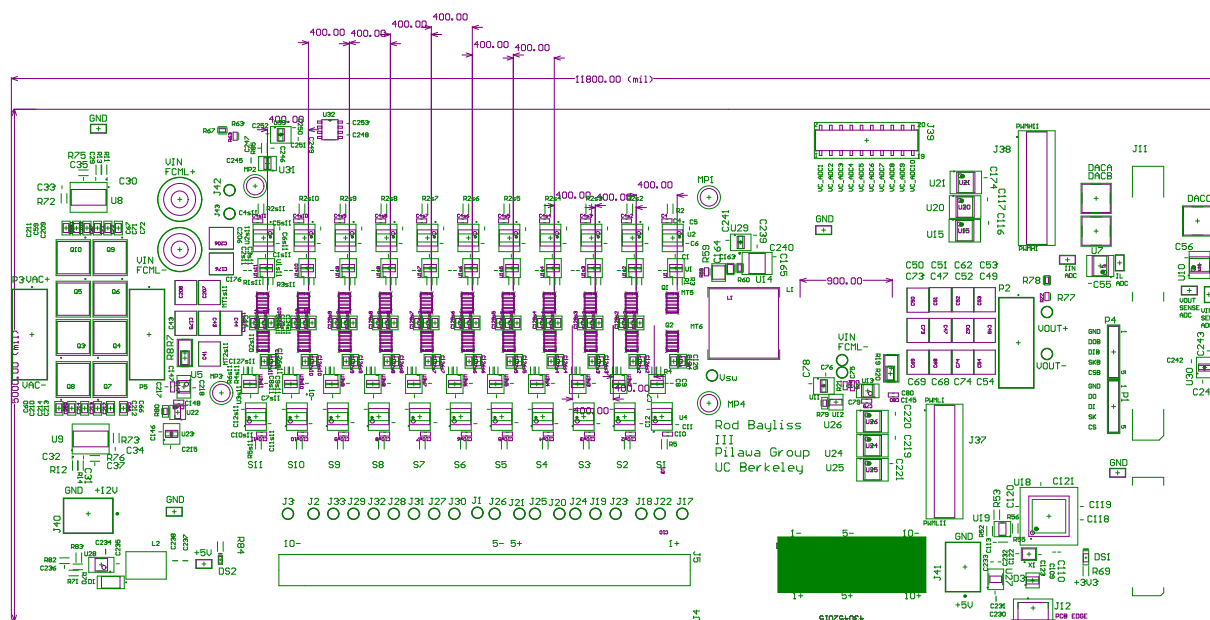


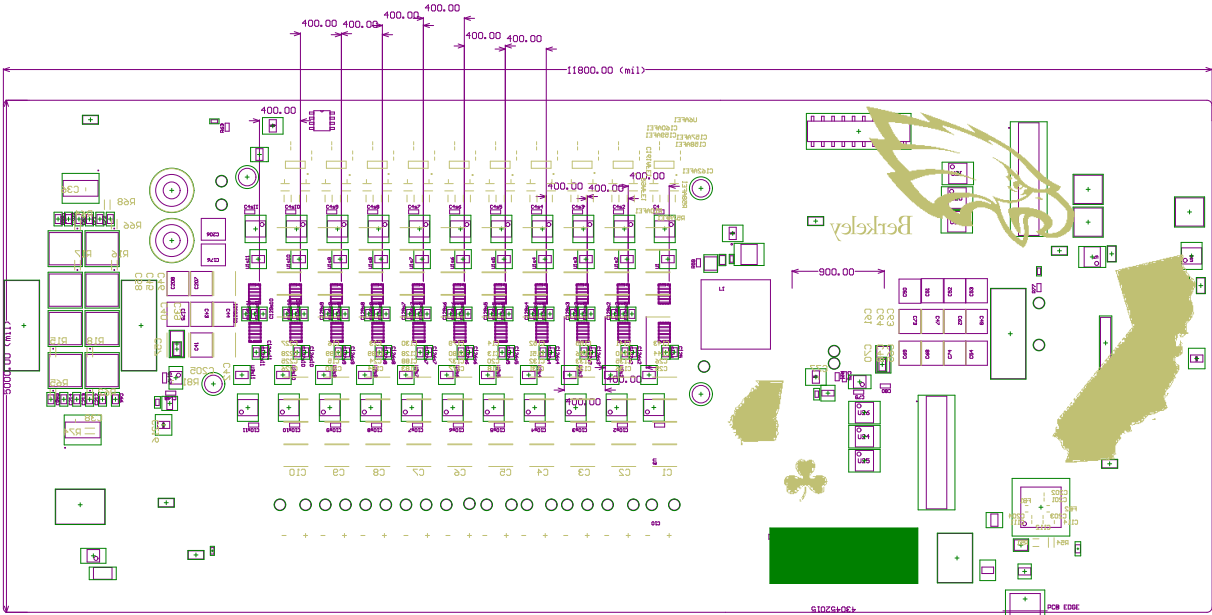








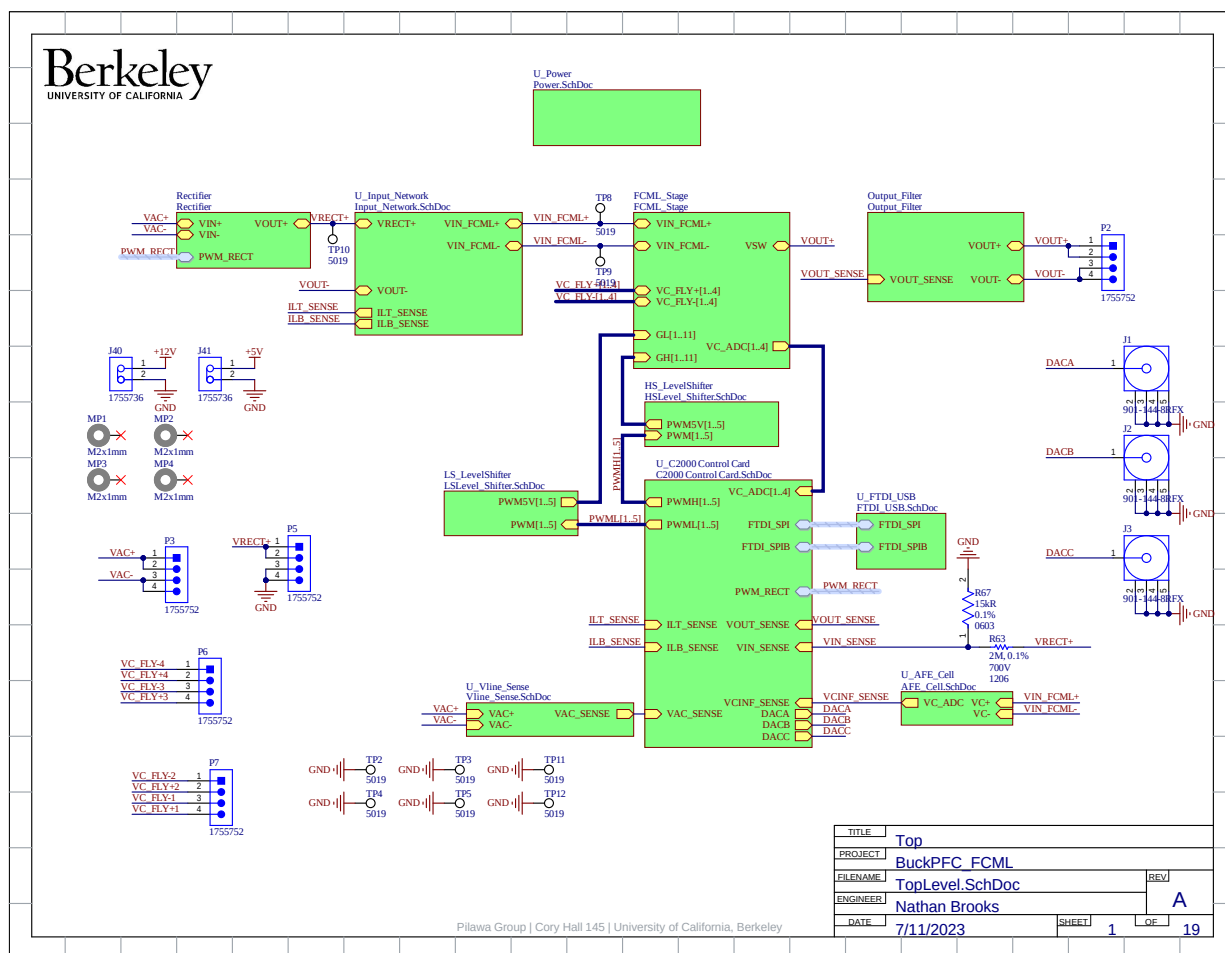




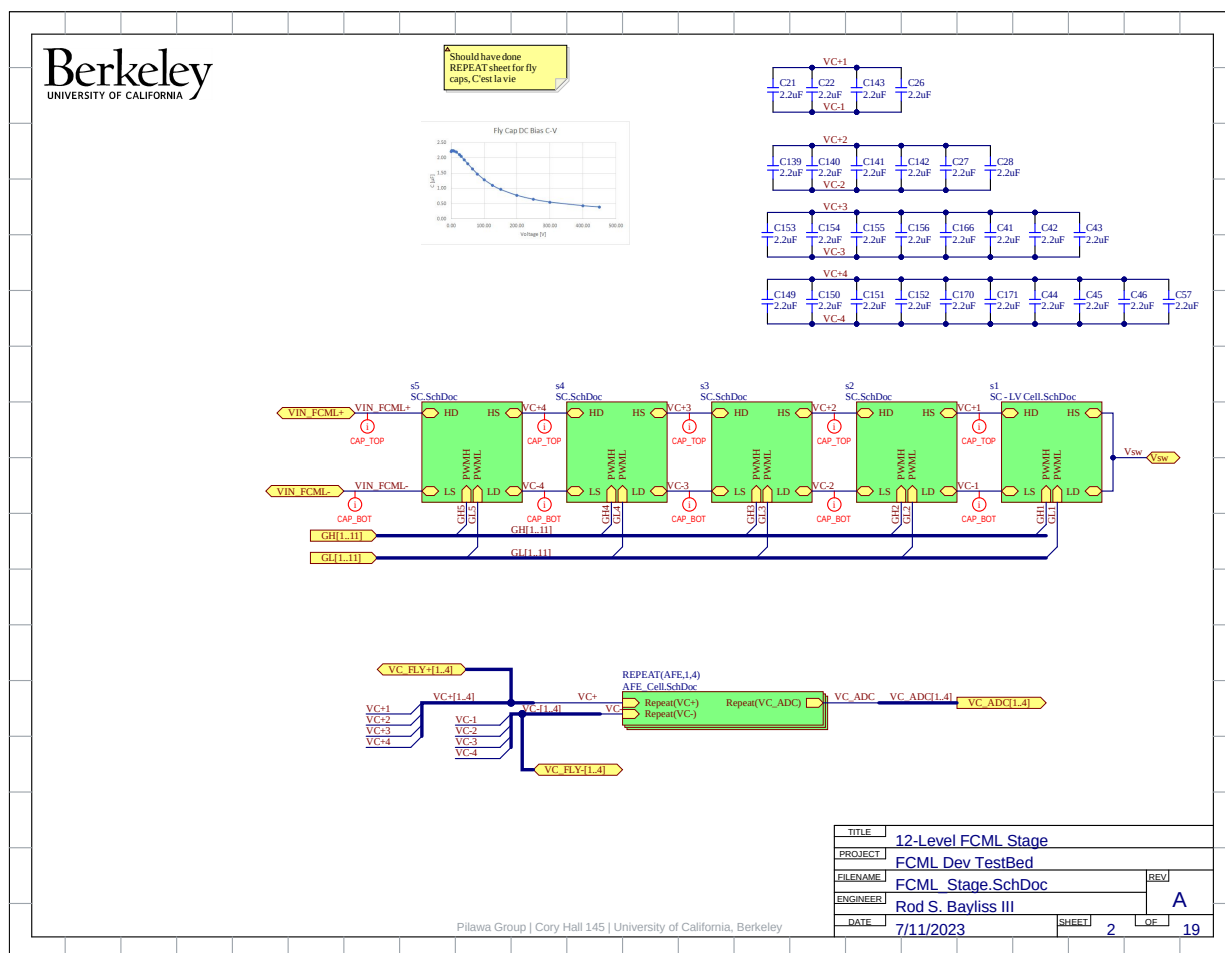
Appendix D

Input Inductor Buck-Type FCML PFC Converter Schematics

180

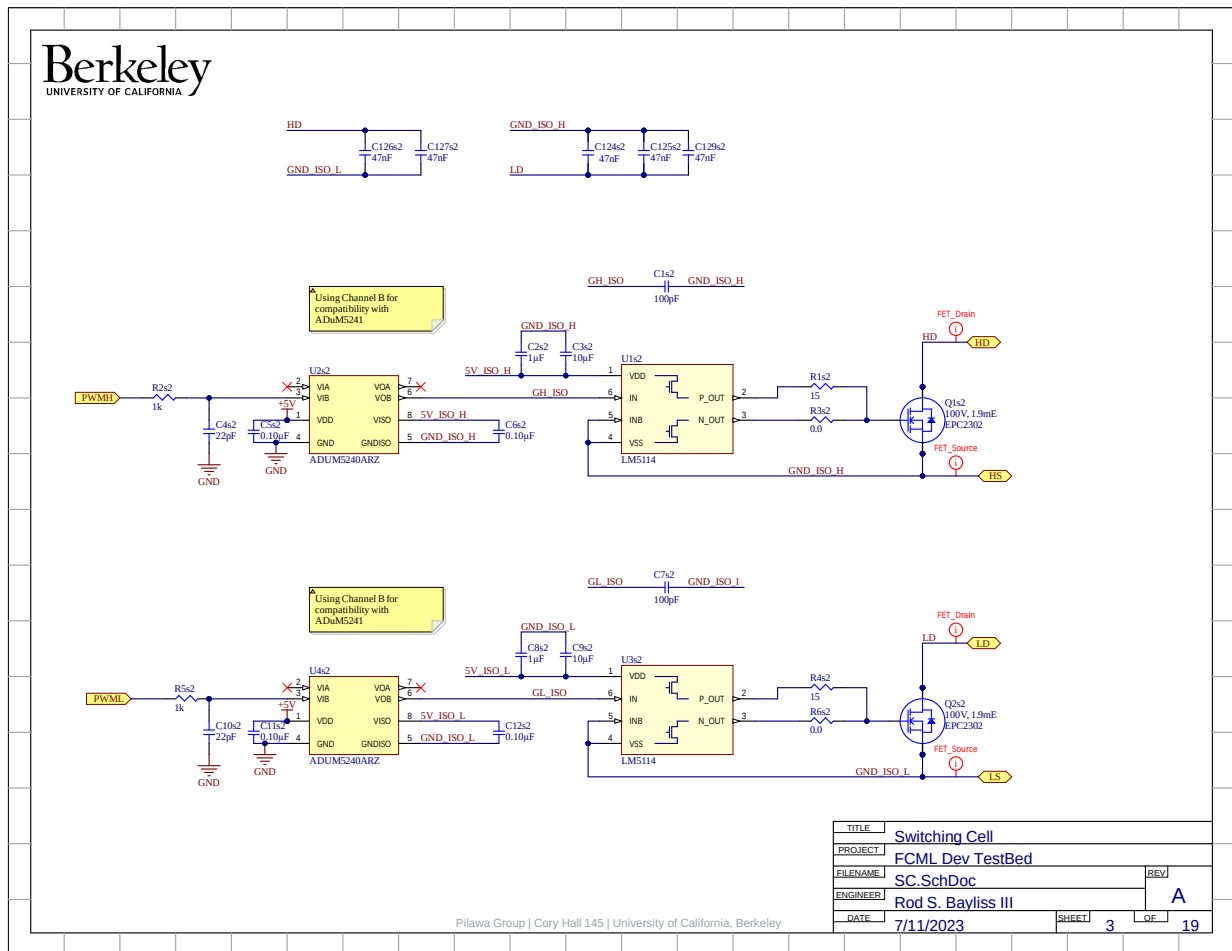


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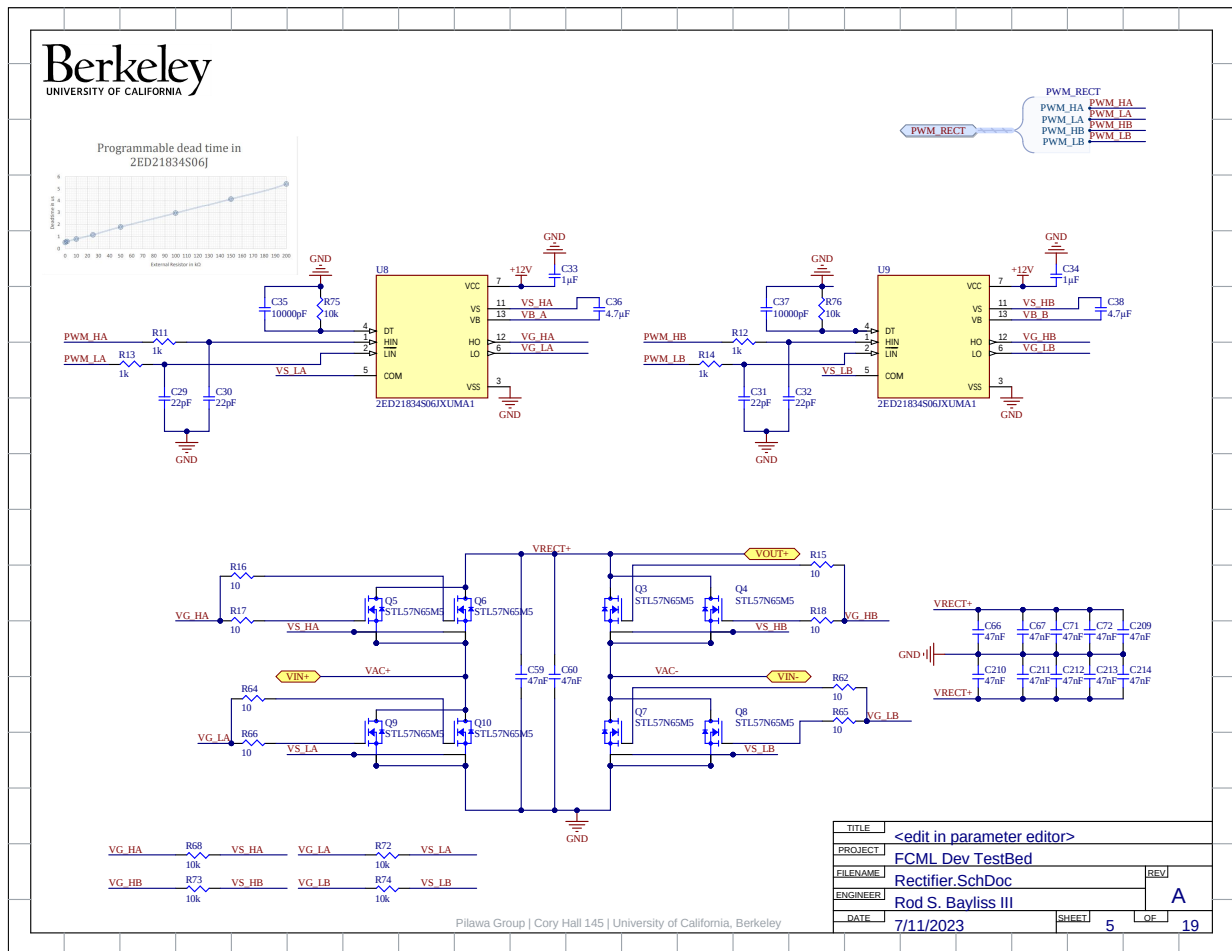


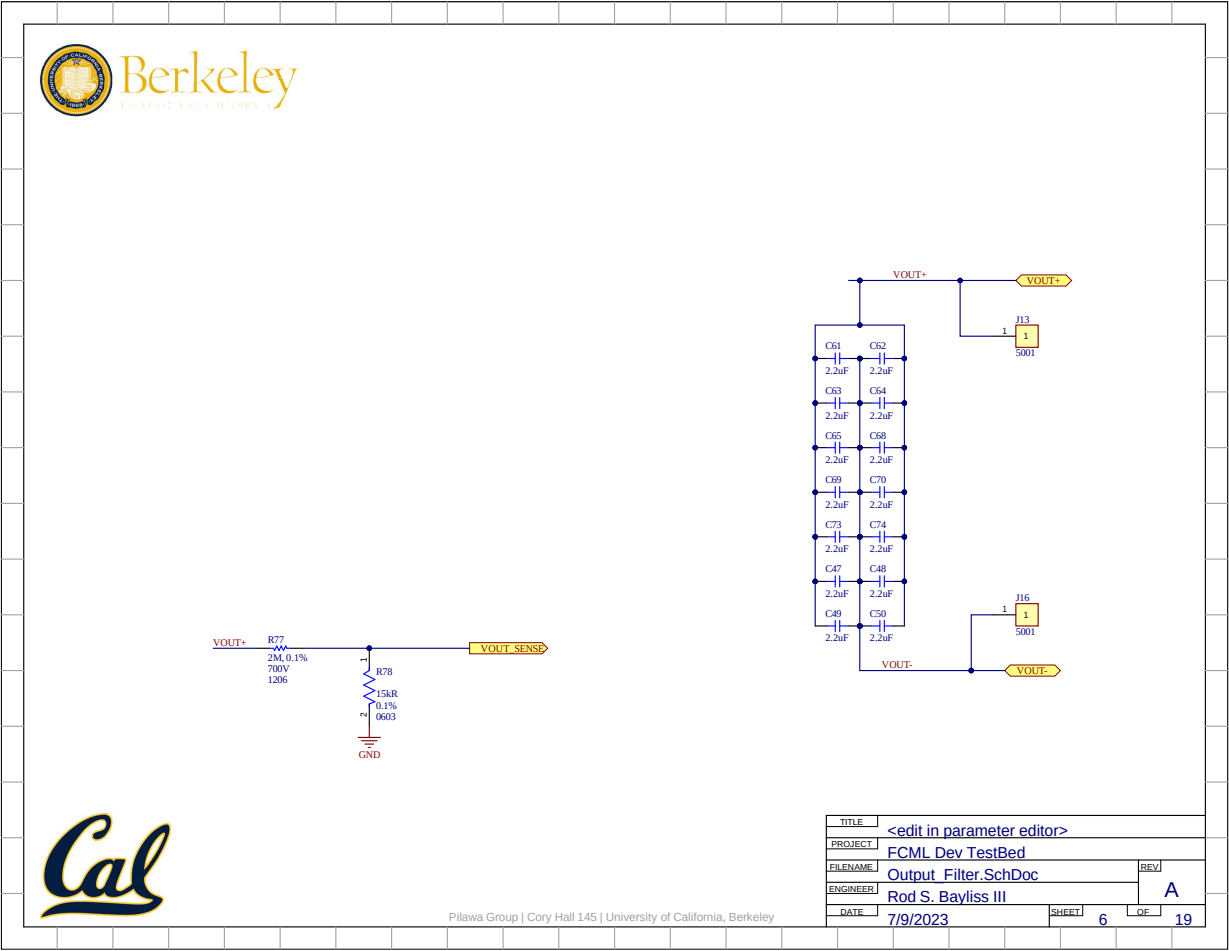
APPENDIX D. INPUT INDUCTOR BUCK-TYPE FCML PFC CONVERTER SCHEMATICS

182



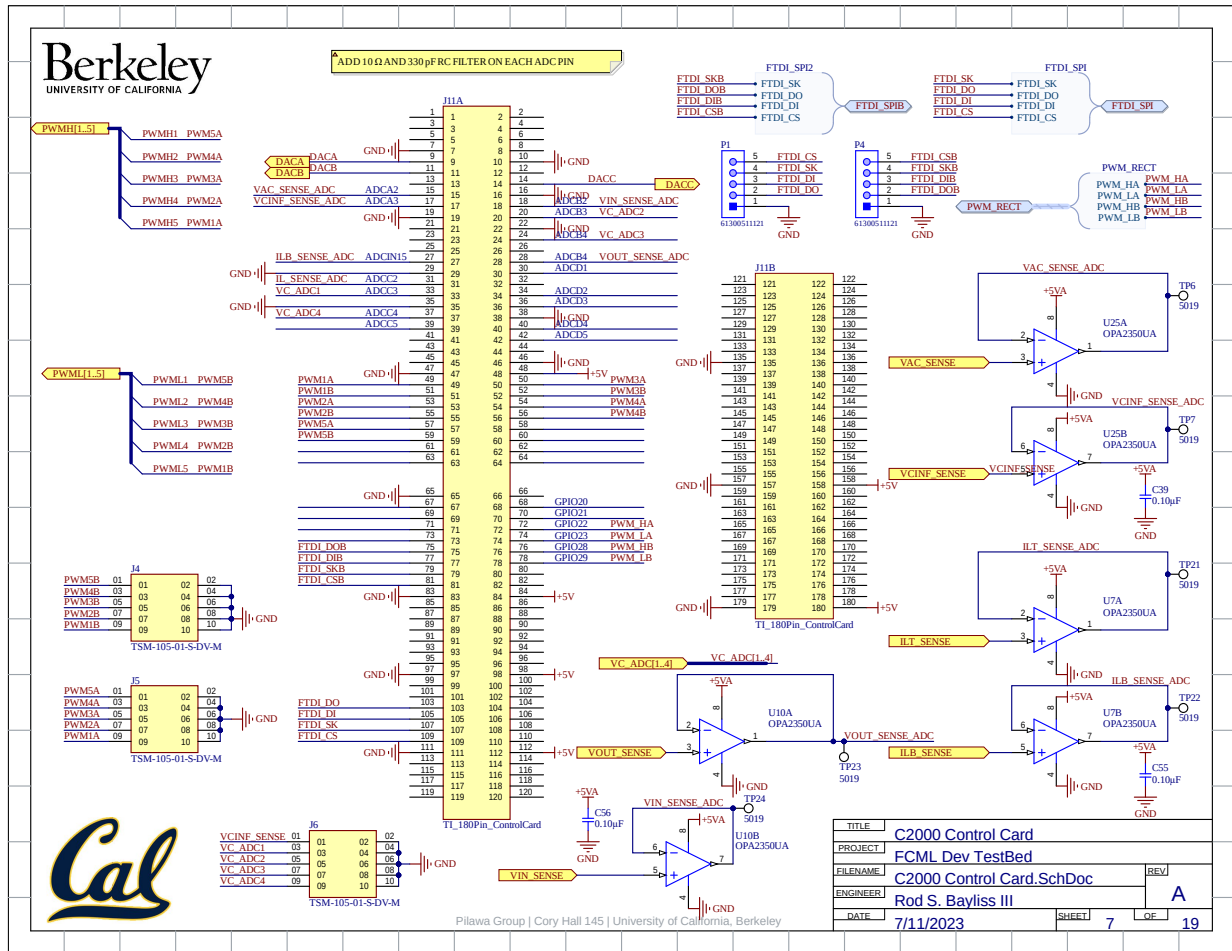
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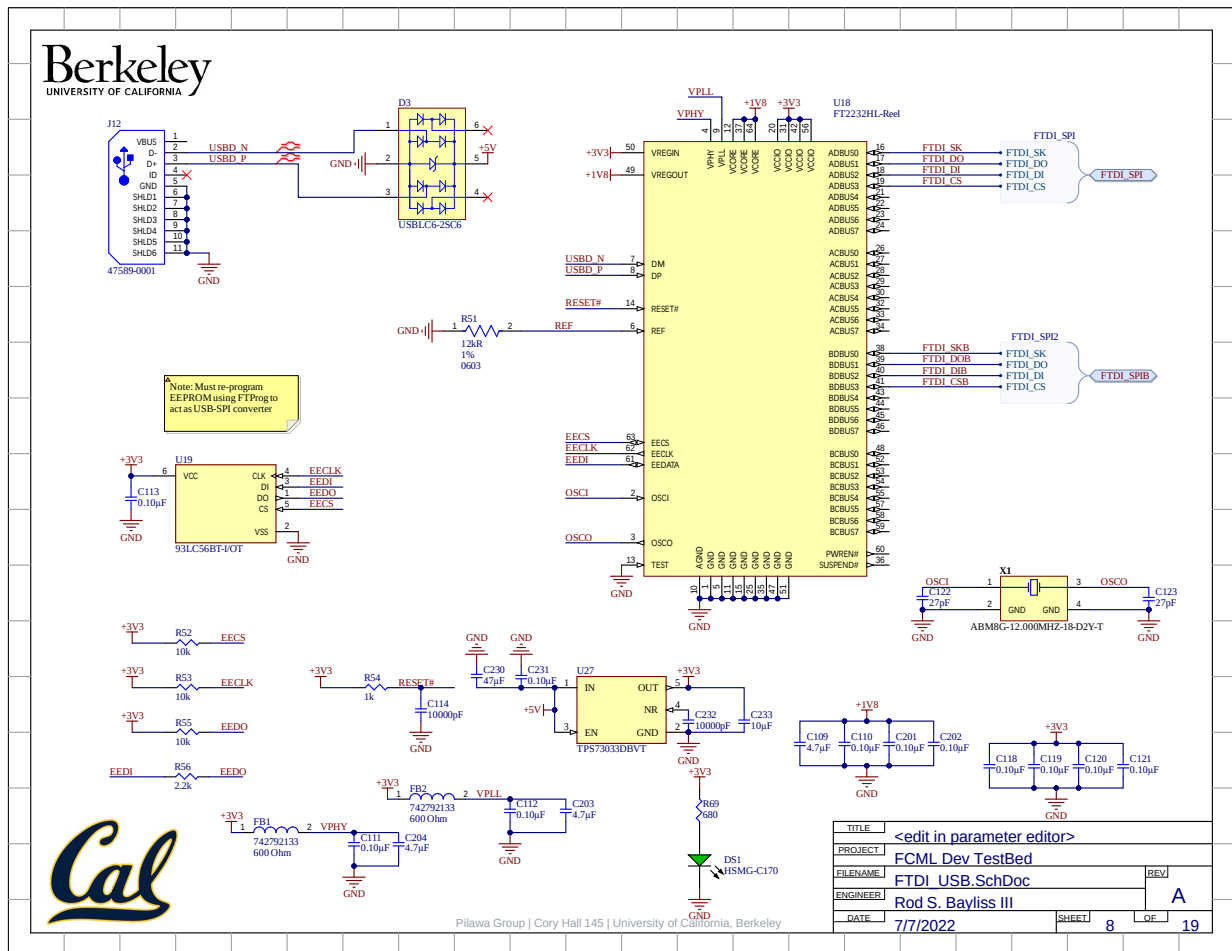


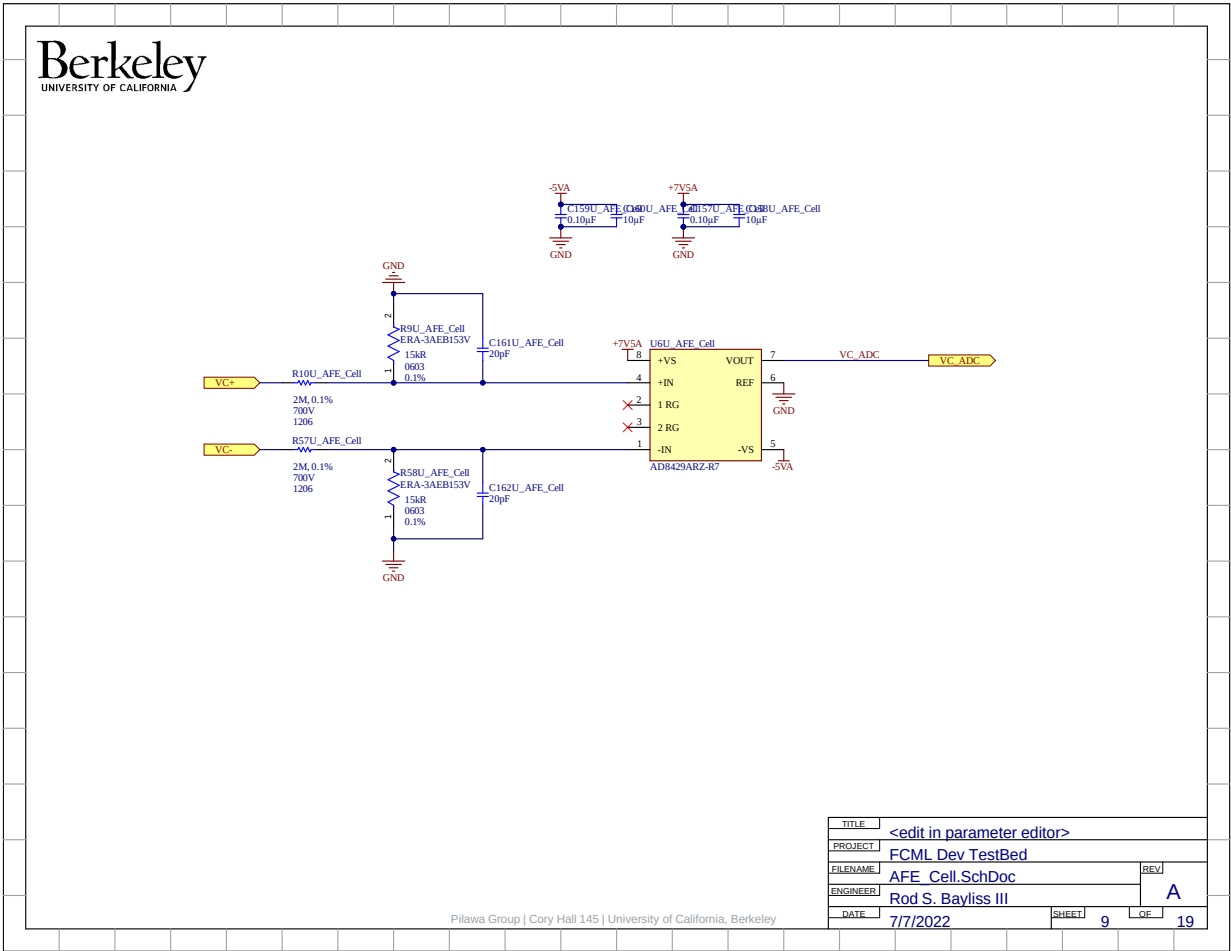
APPENDIX D. INPUT INDUCTOR BUCK-TYPE FCML PFC CONVERTER SCHEMATICS

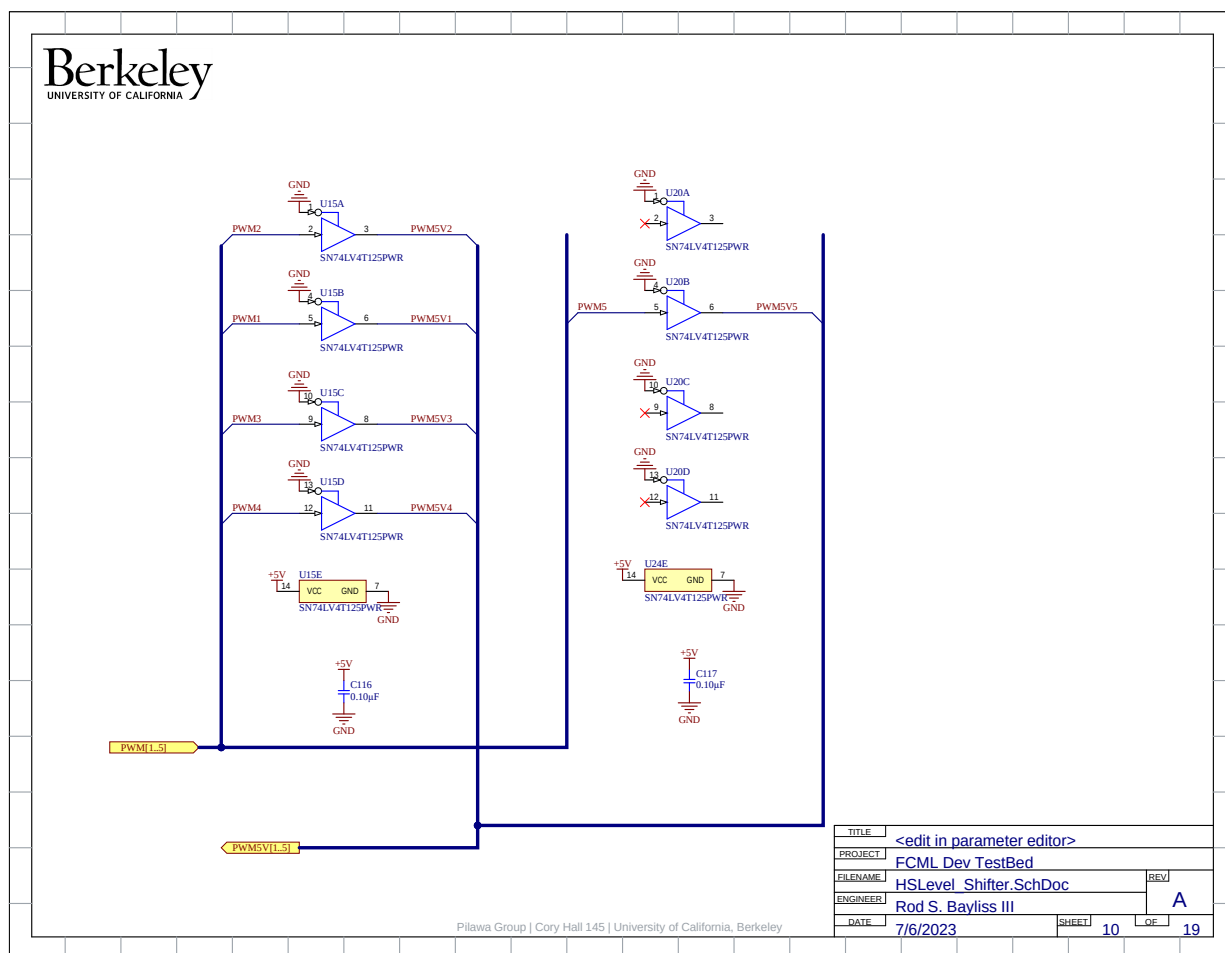
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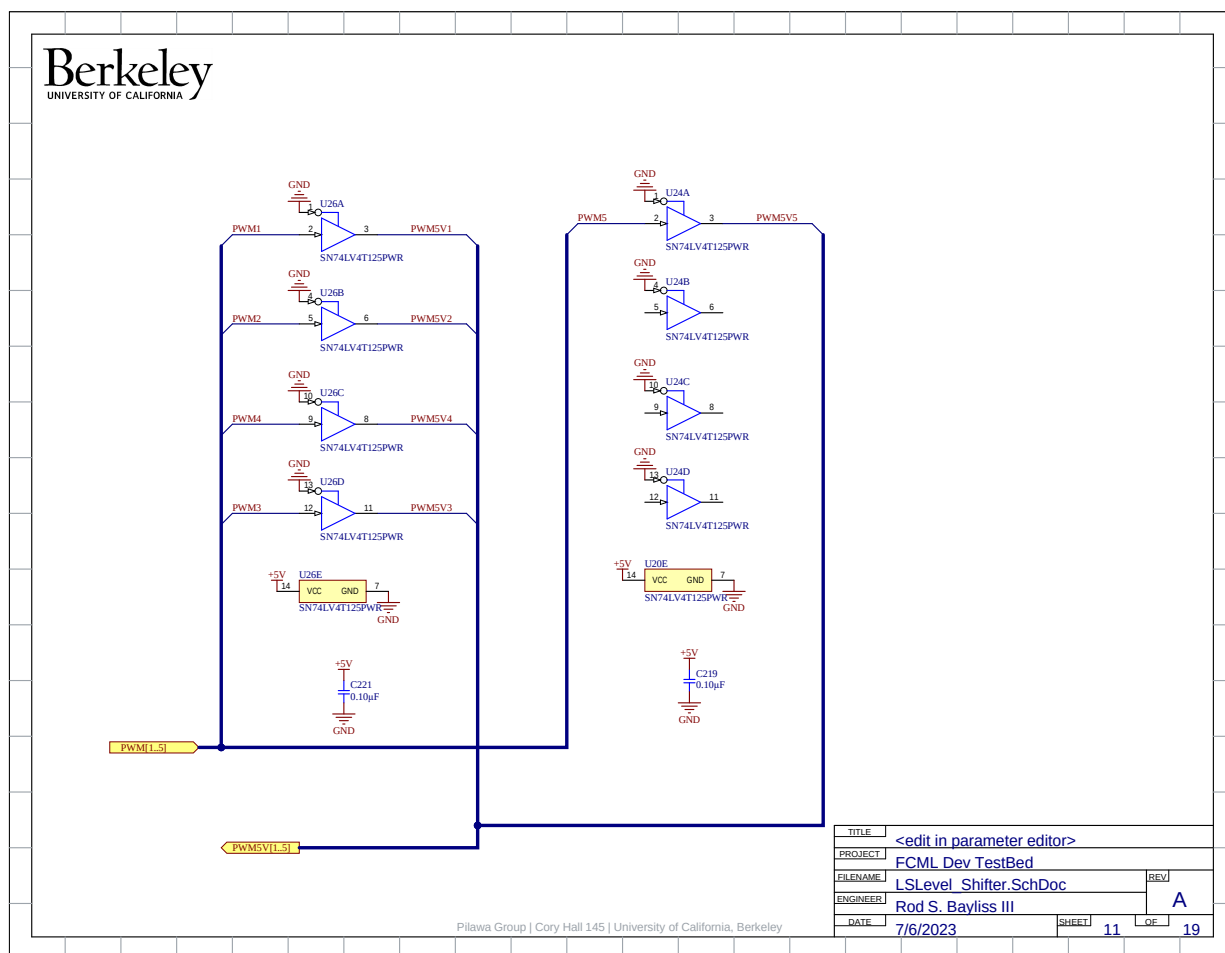


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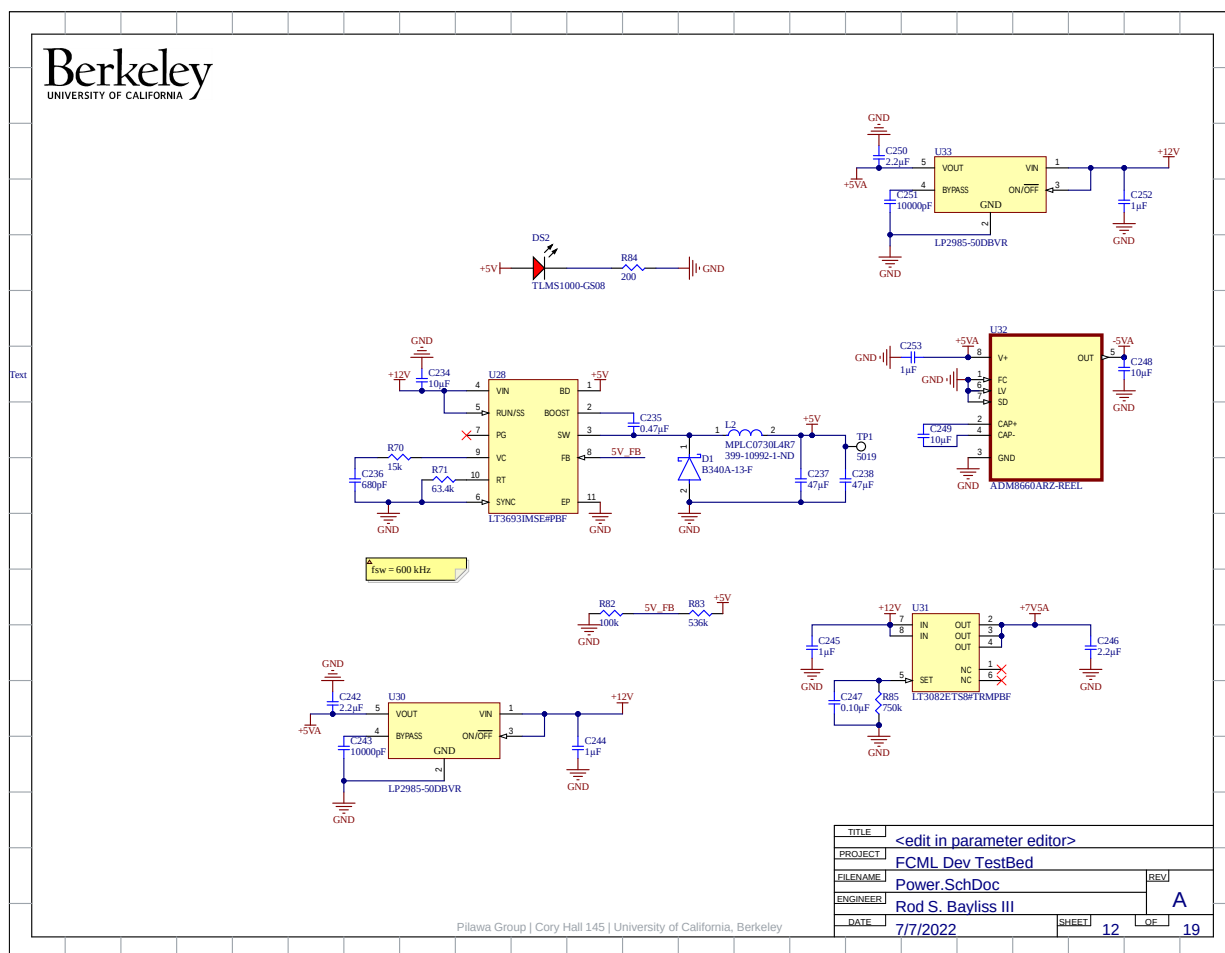




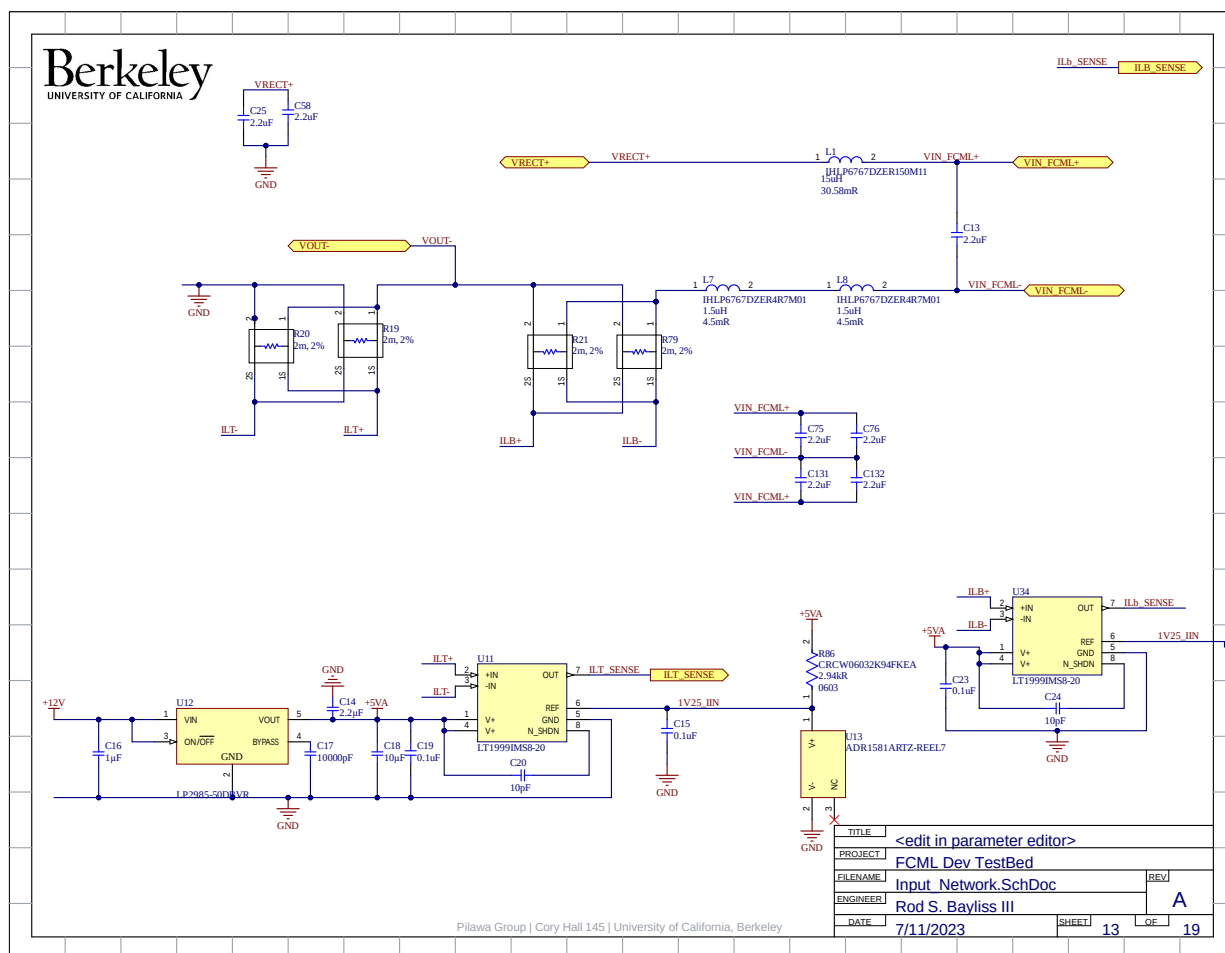


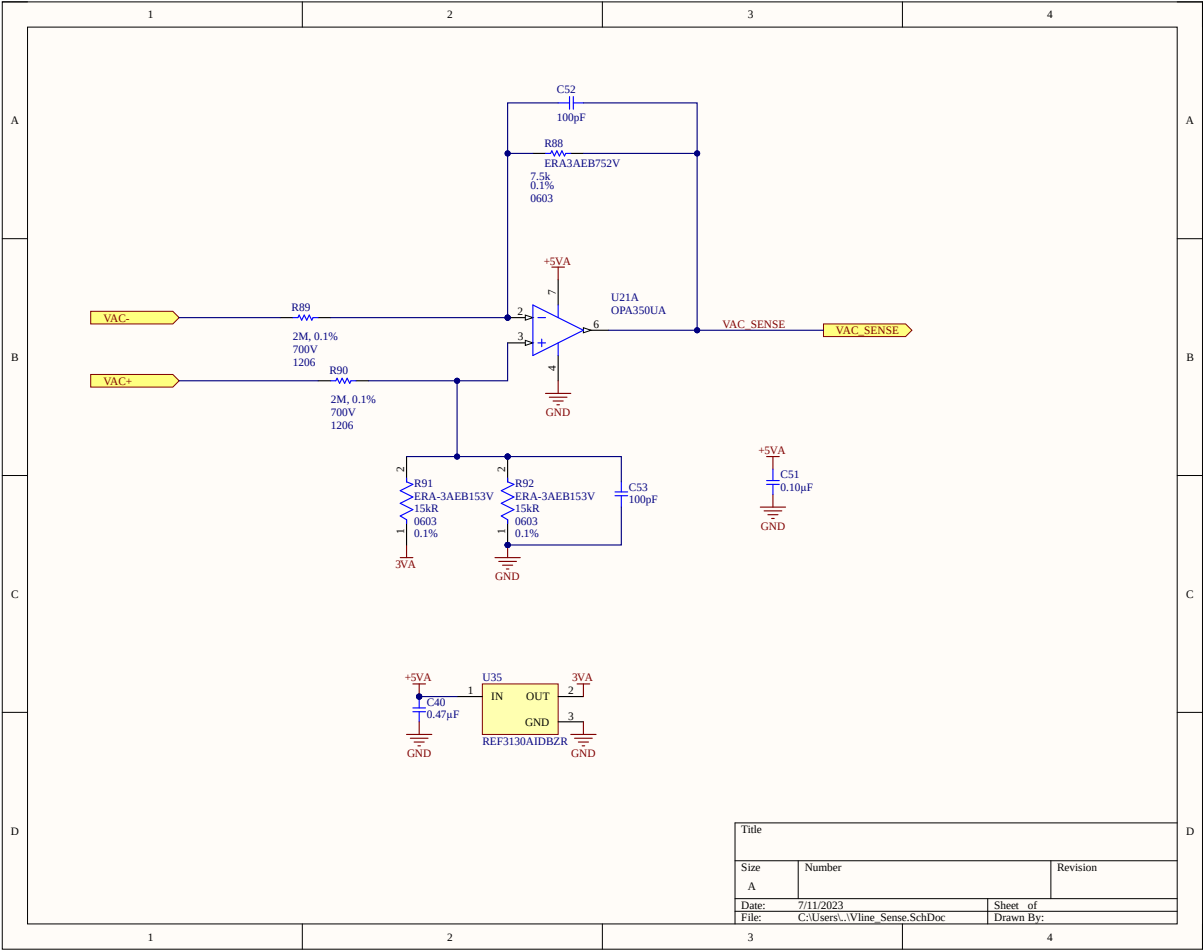


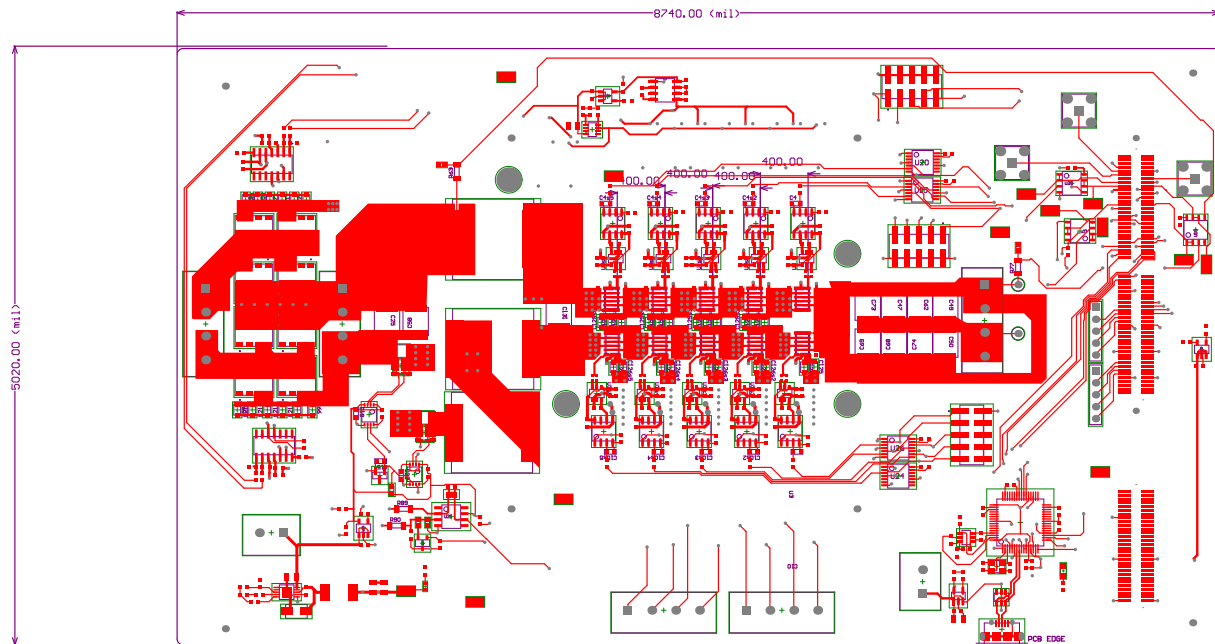
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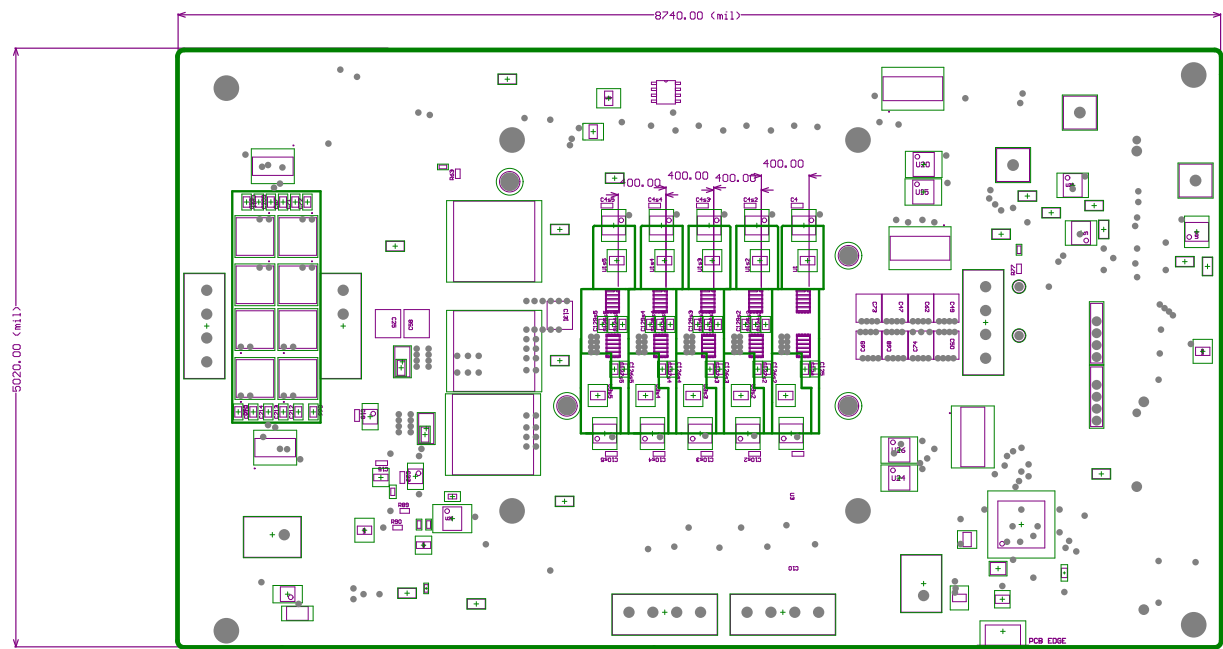


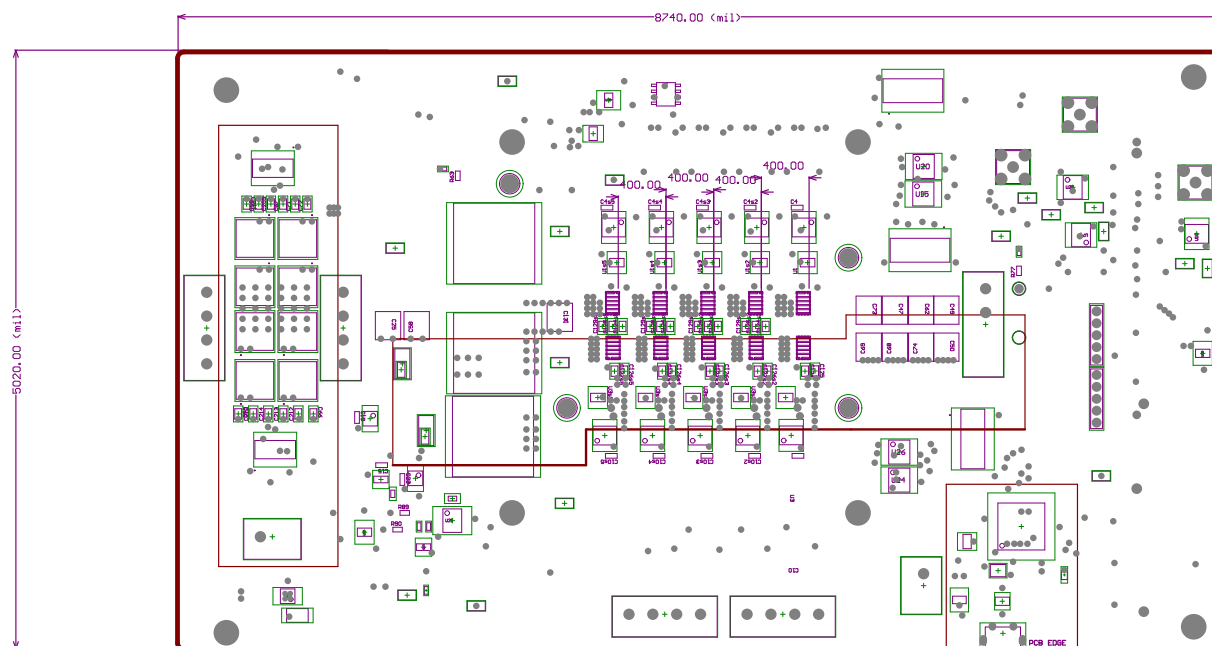
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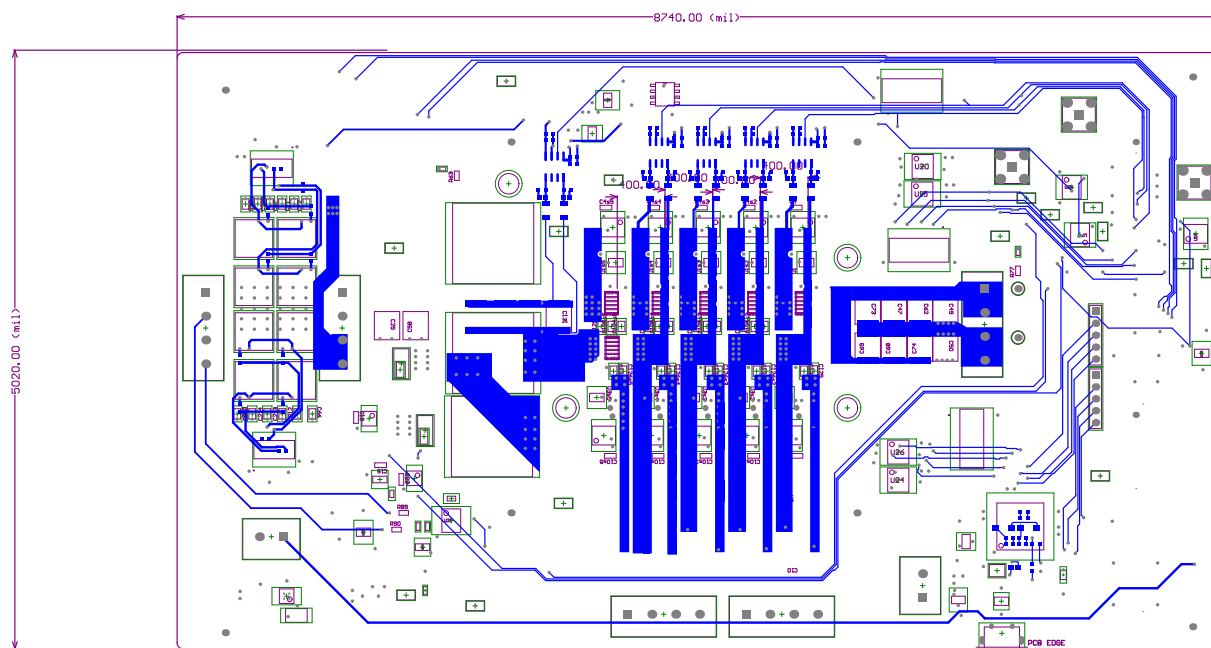






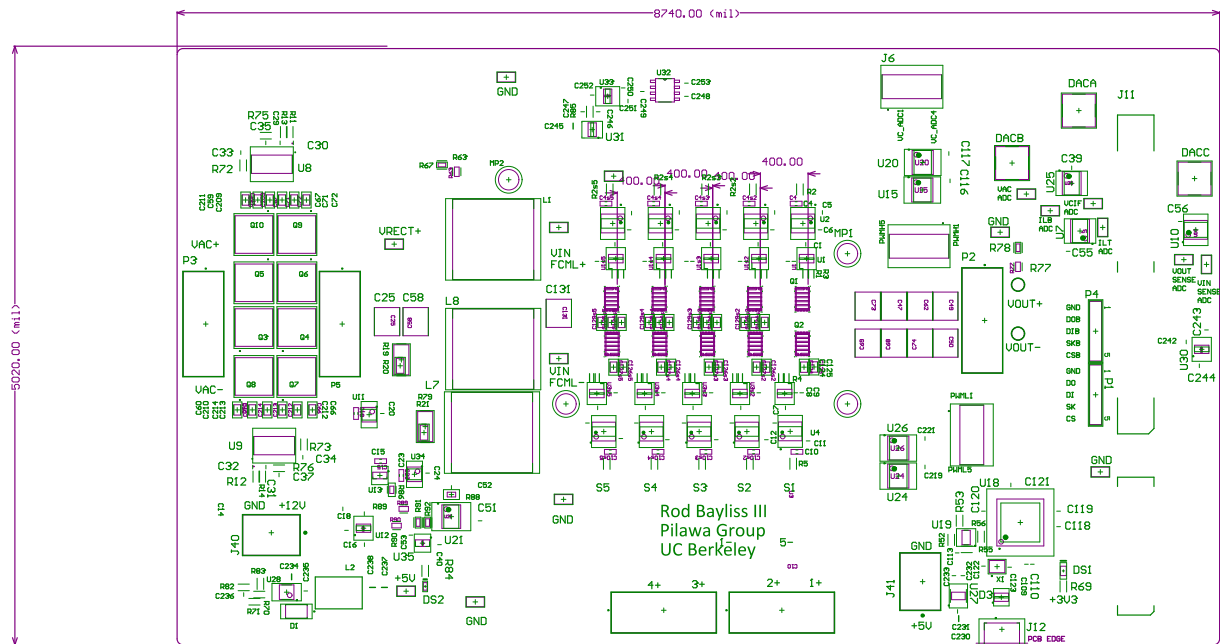


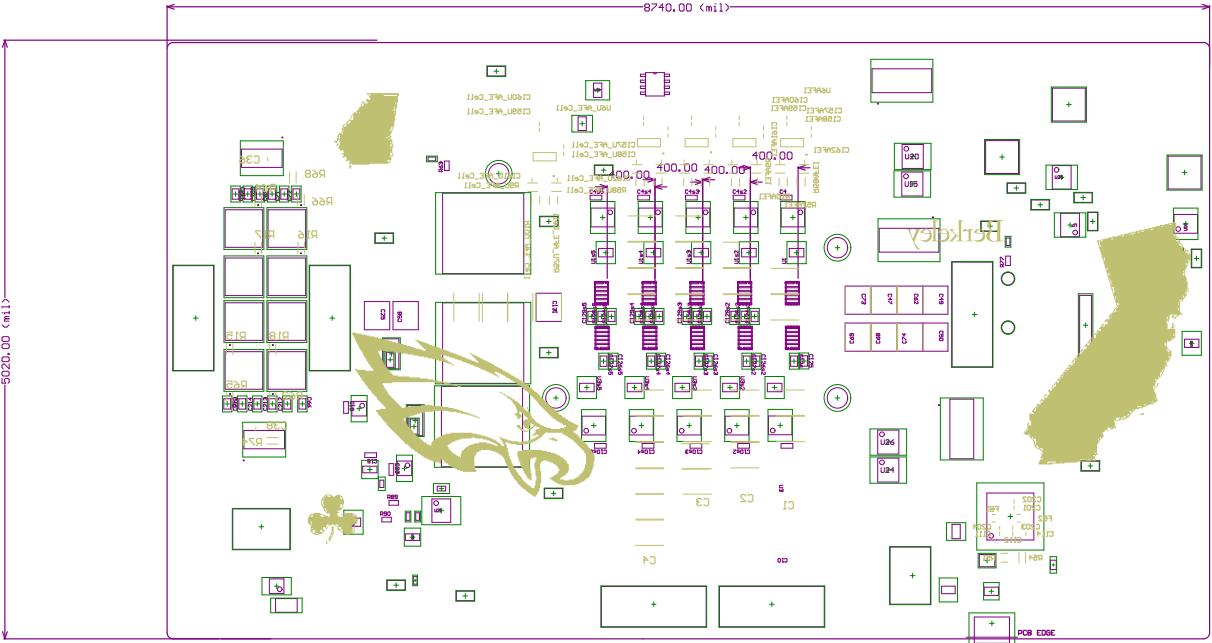




APPENDIX D. INPUT INDUCTOR BUCK-TYPE FCML PFC CONVERTER SCHEMATICS

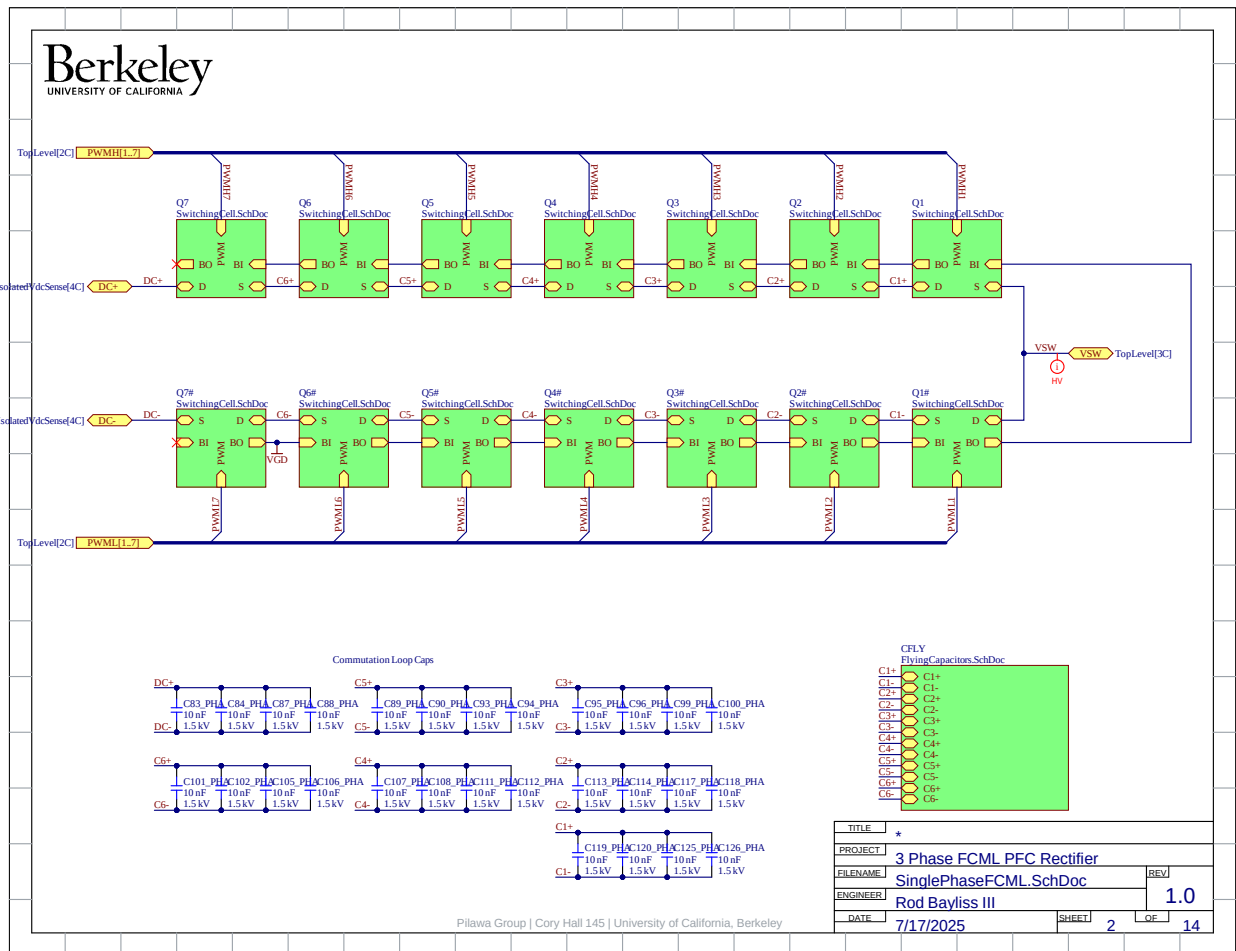
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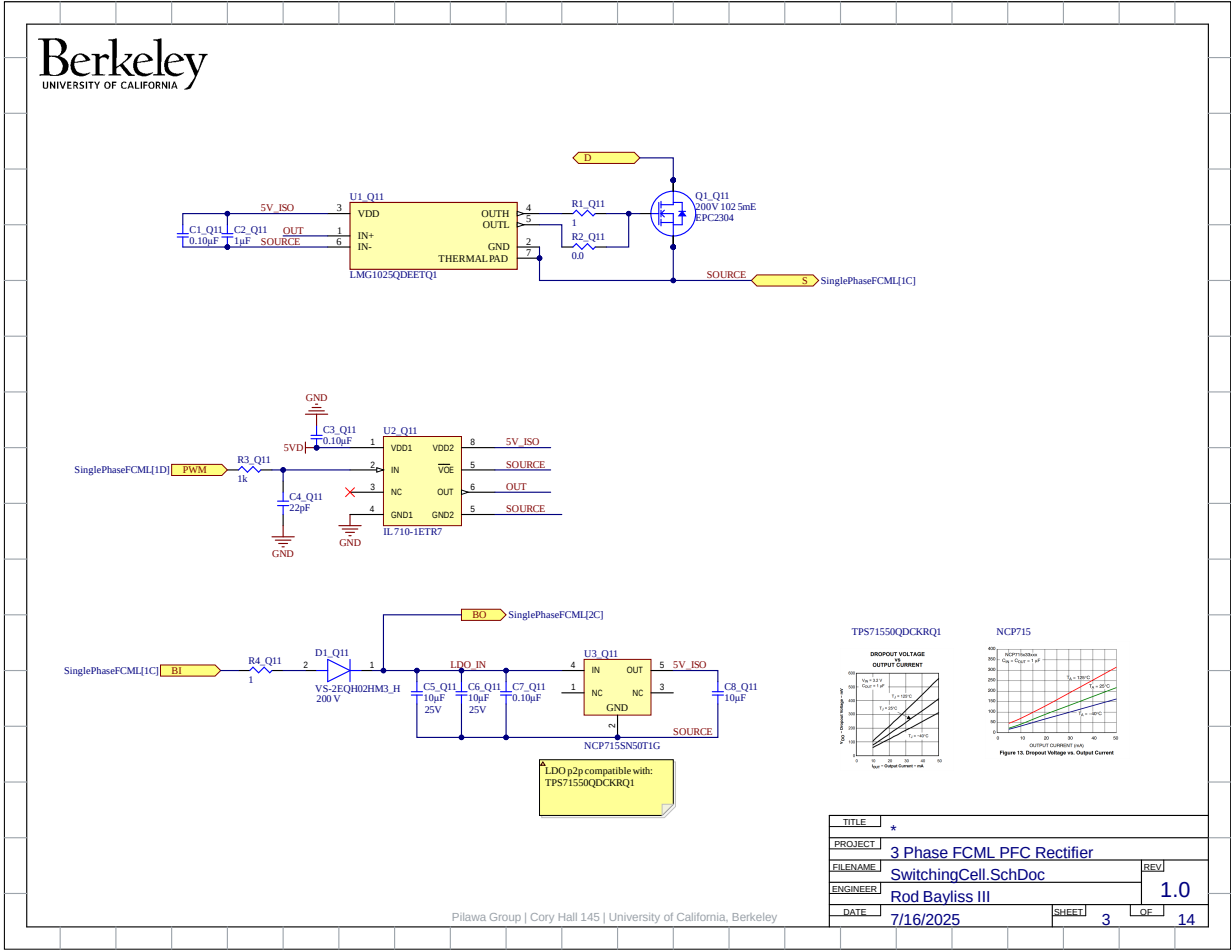


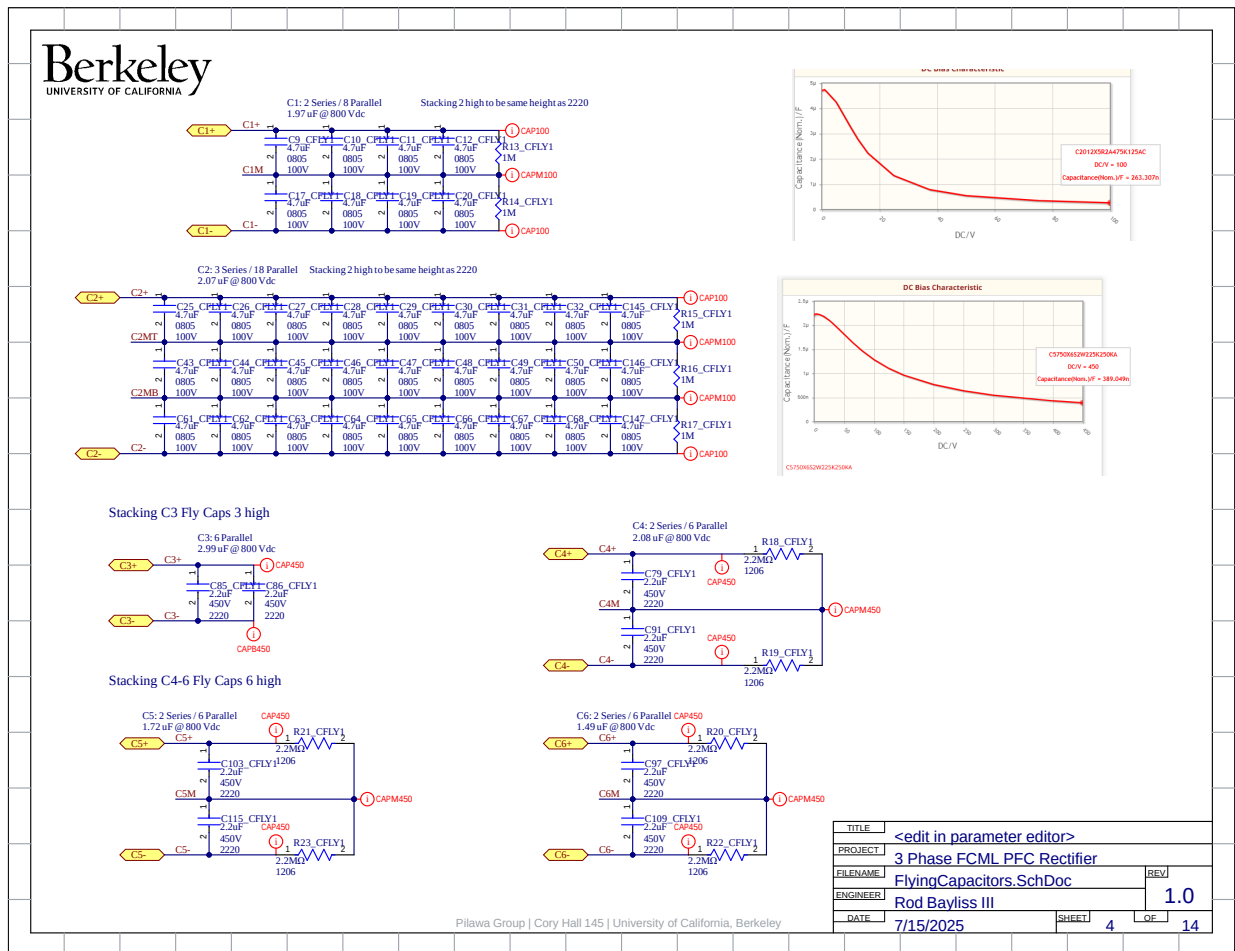


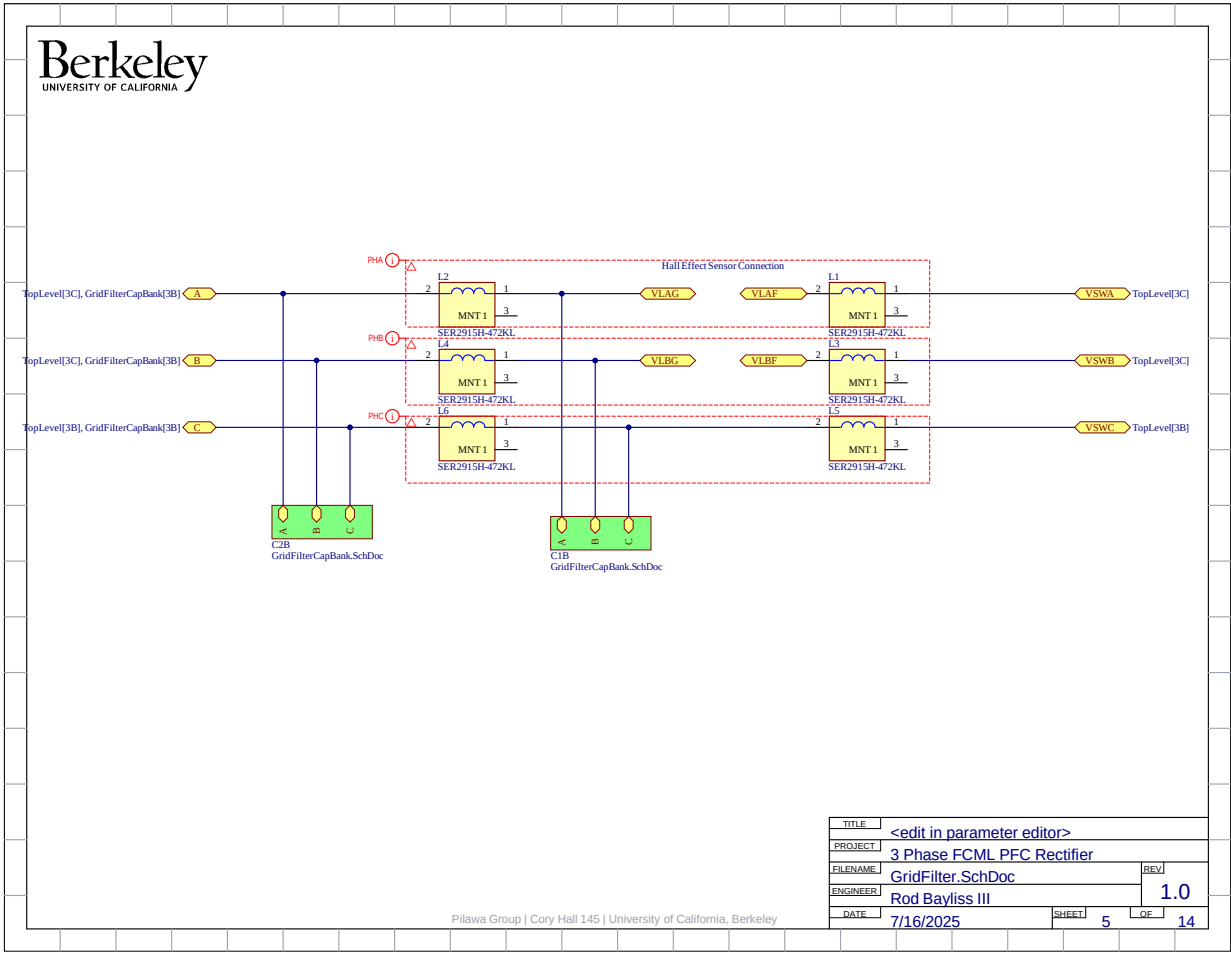
Appendix E

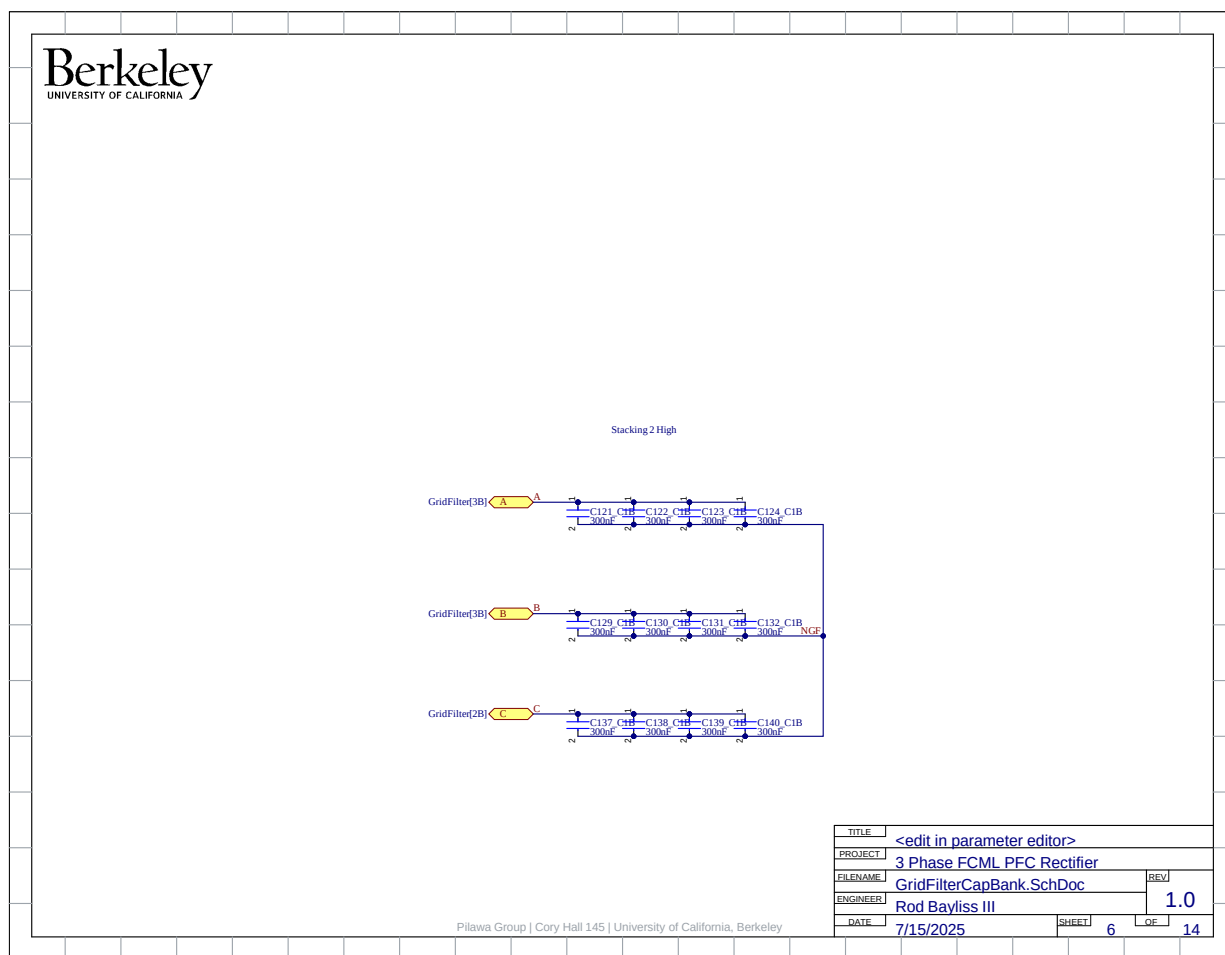
Three-Phase Eight-Level FCML Rectifier Schematics

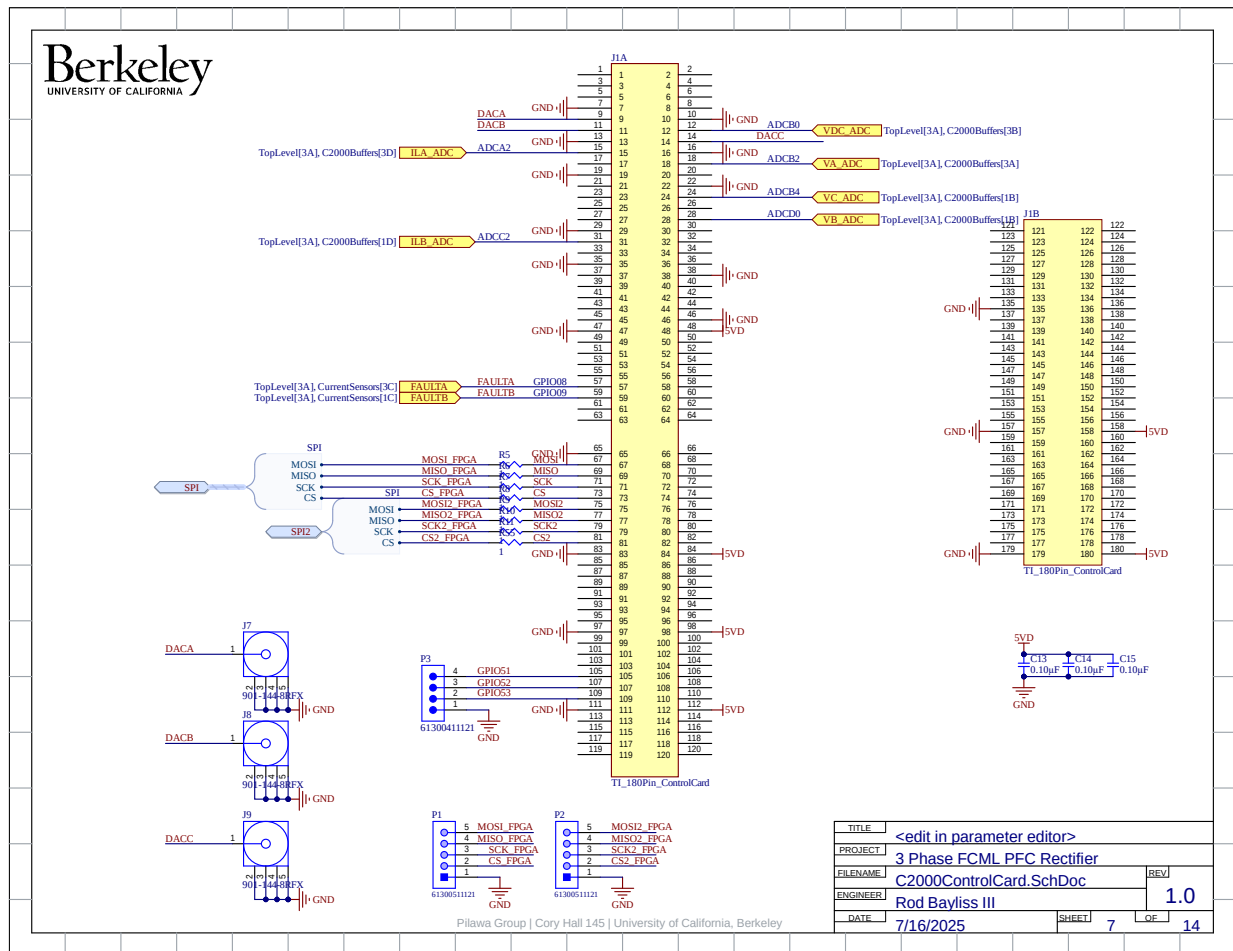


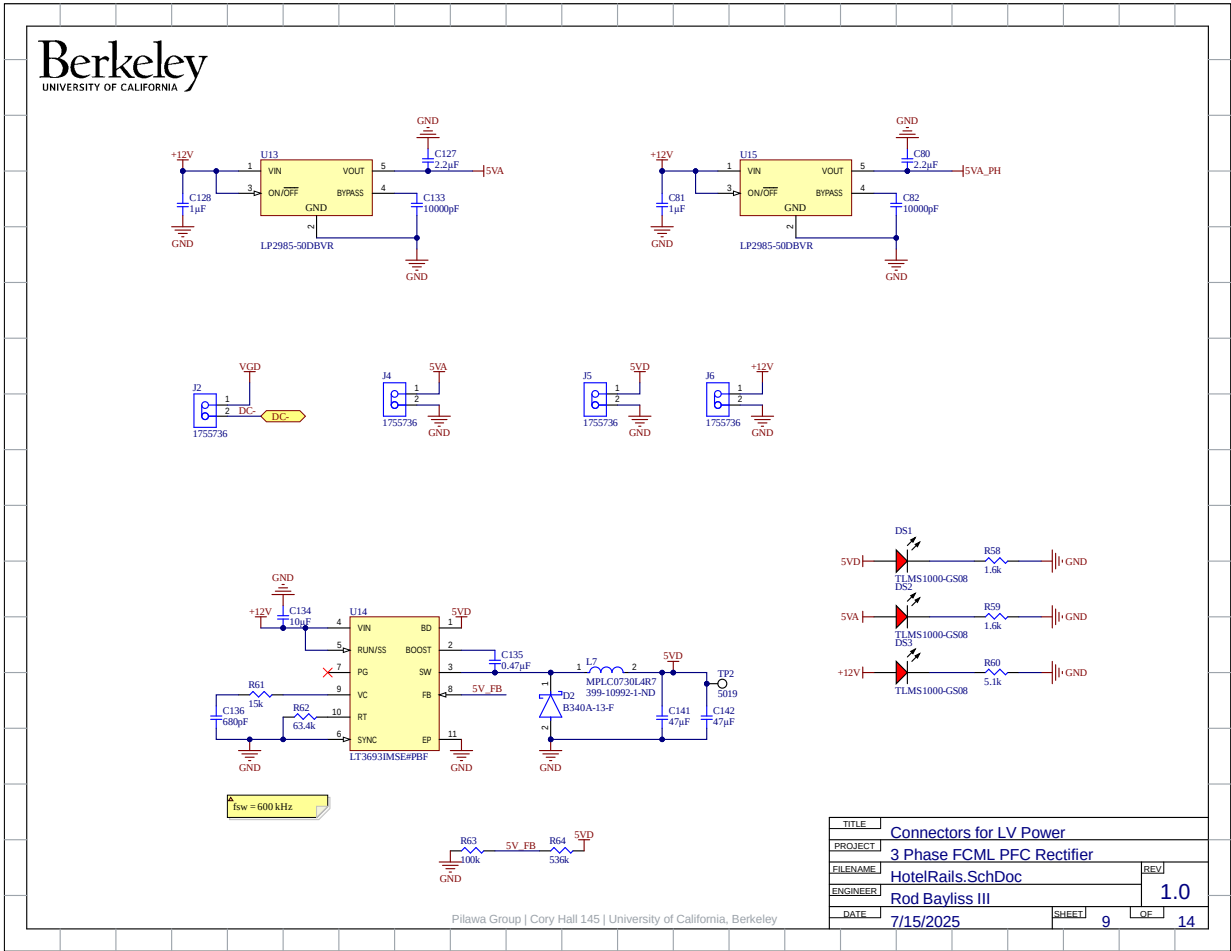


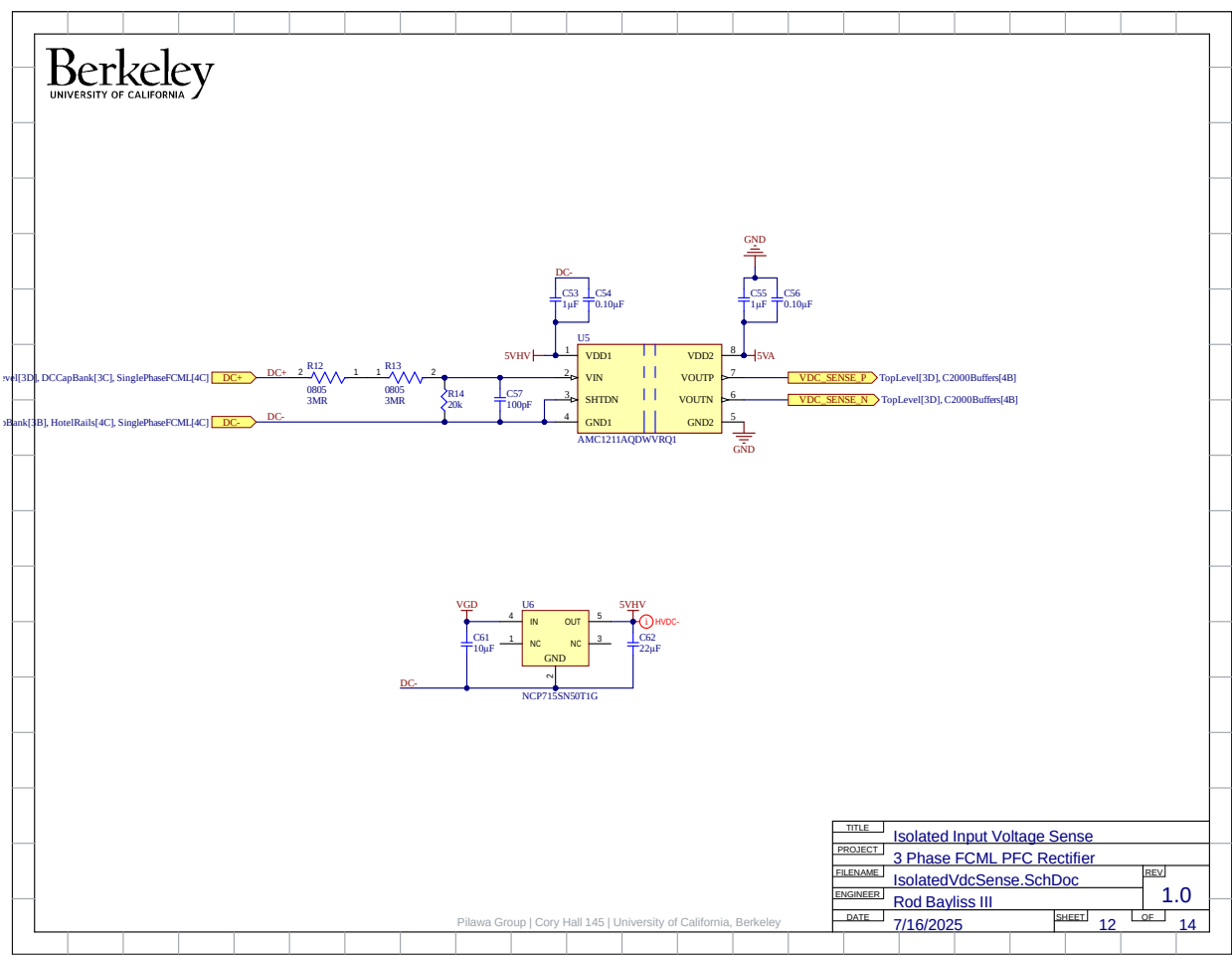


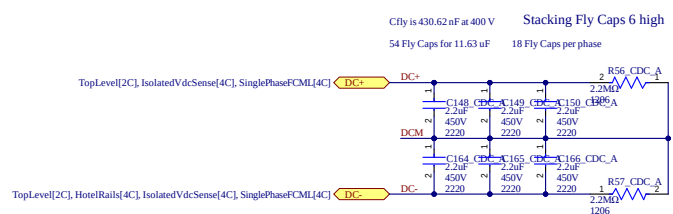




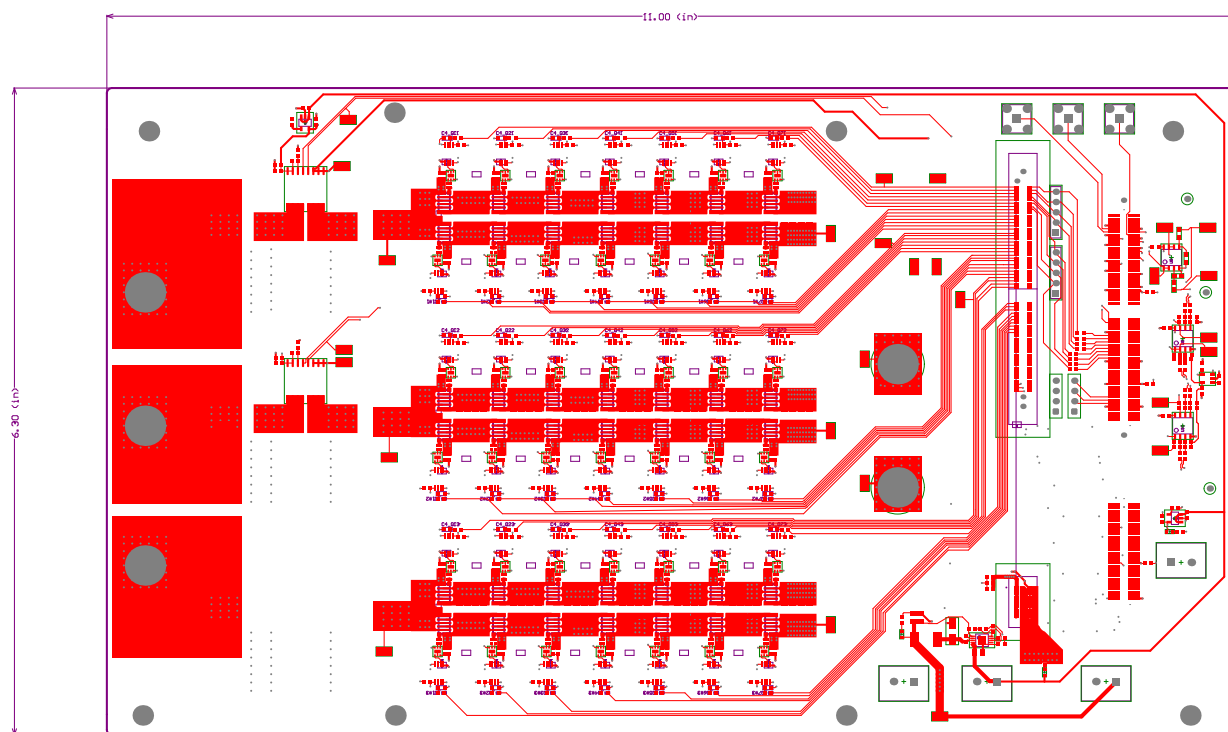


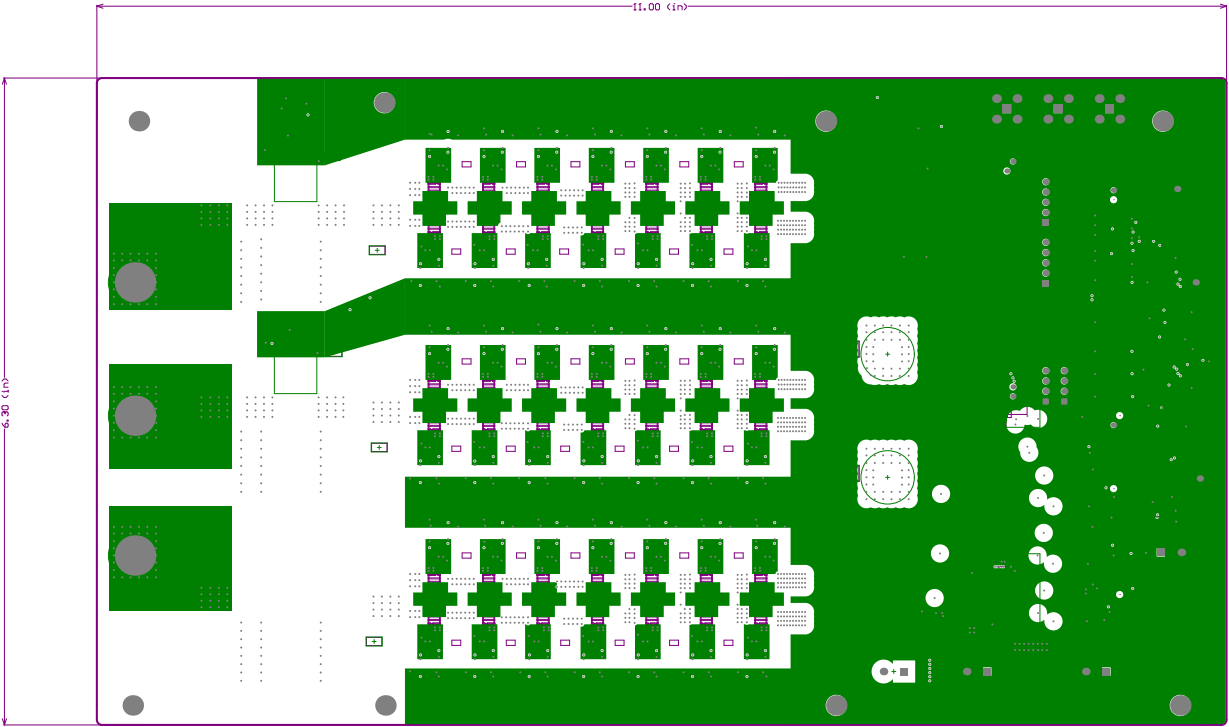


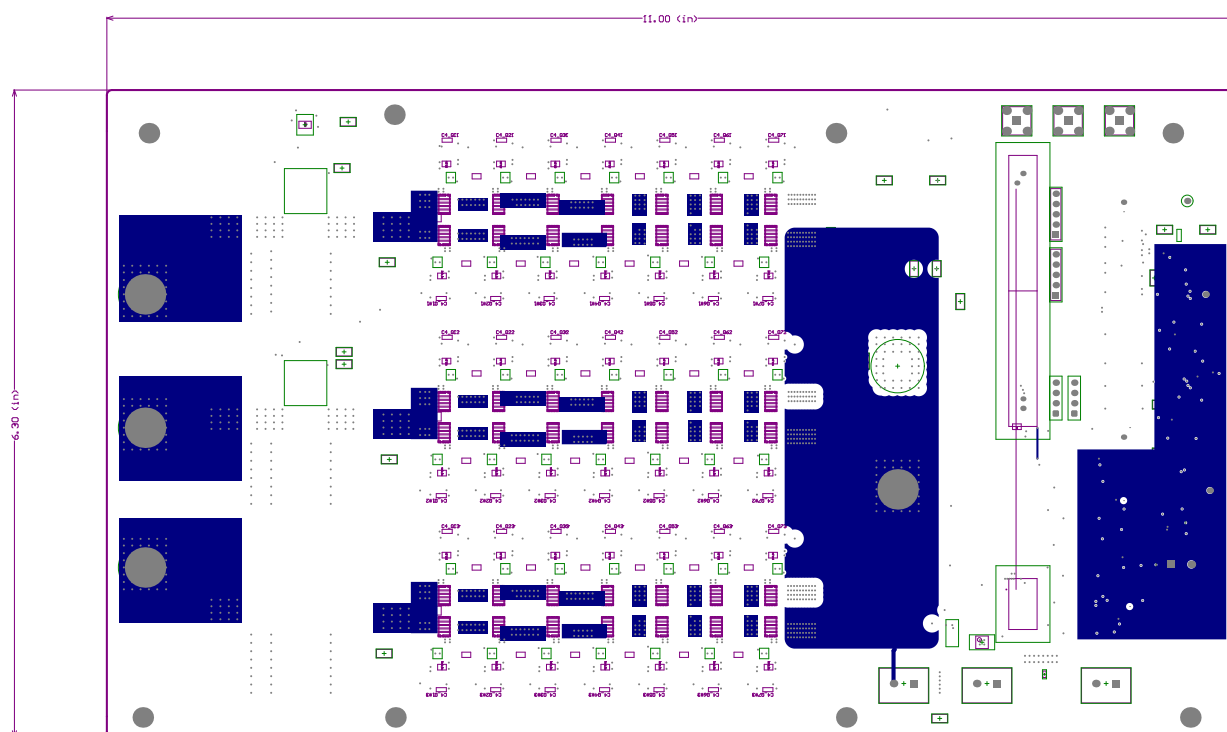


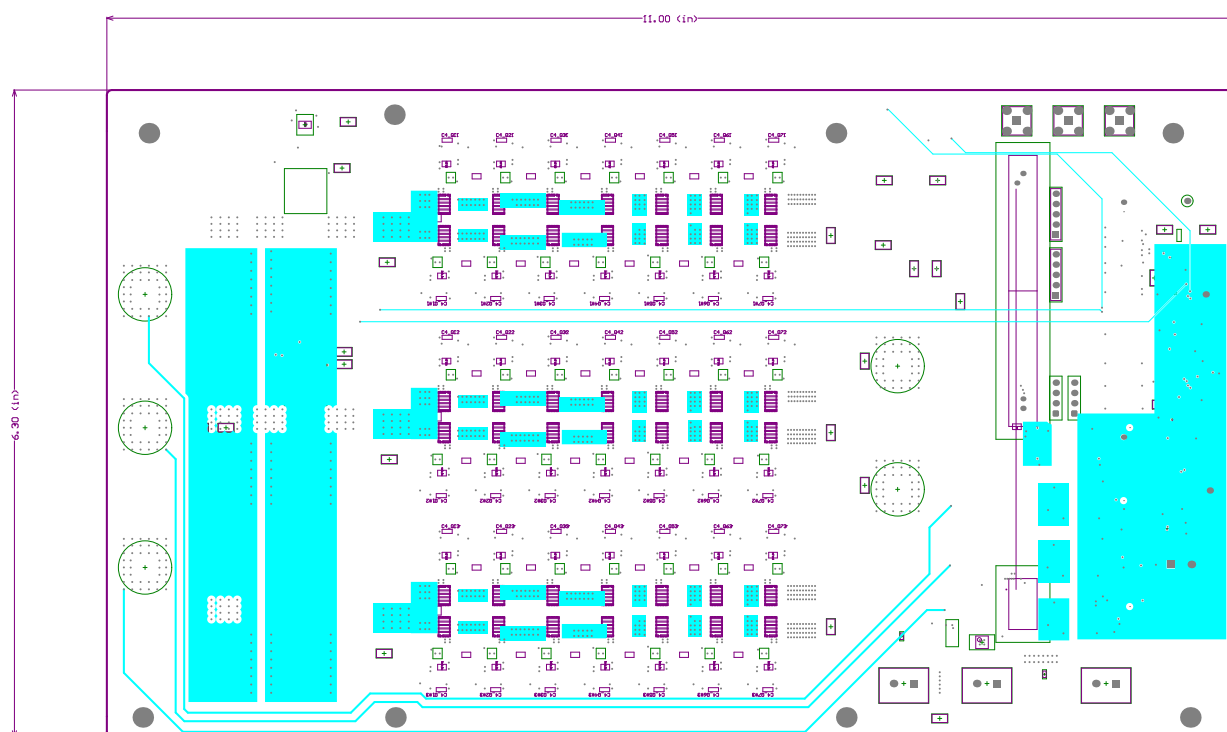


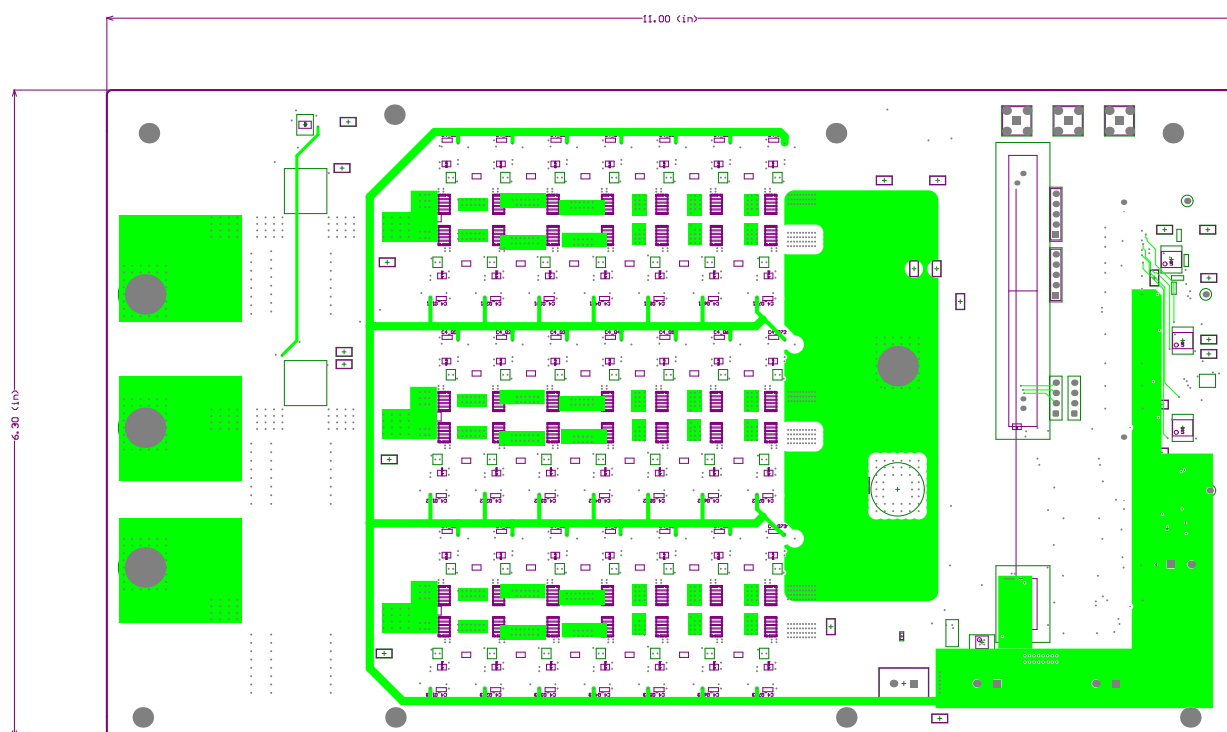
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ENGINEER	Rod Bayliss III		
DATE	7/15/2025	SHEET	14 OF 14

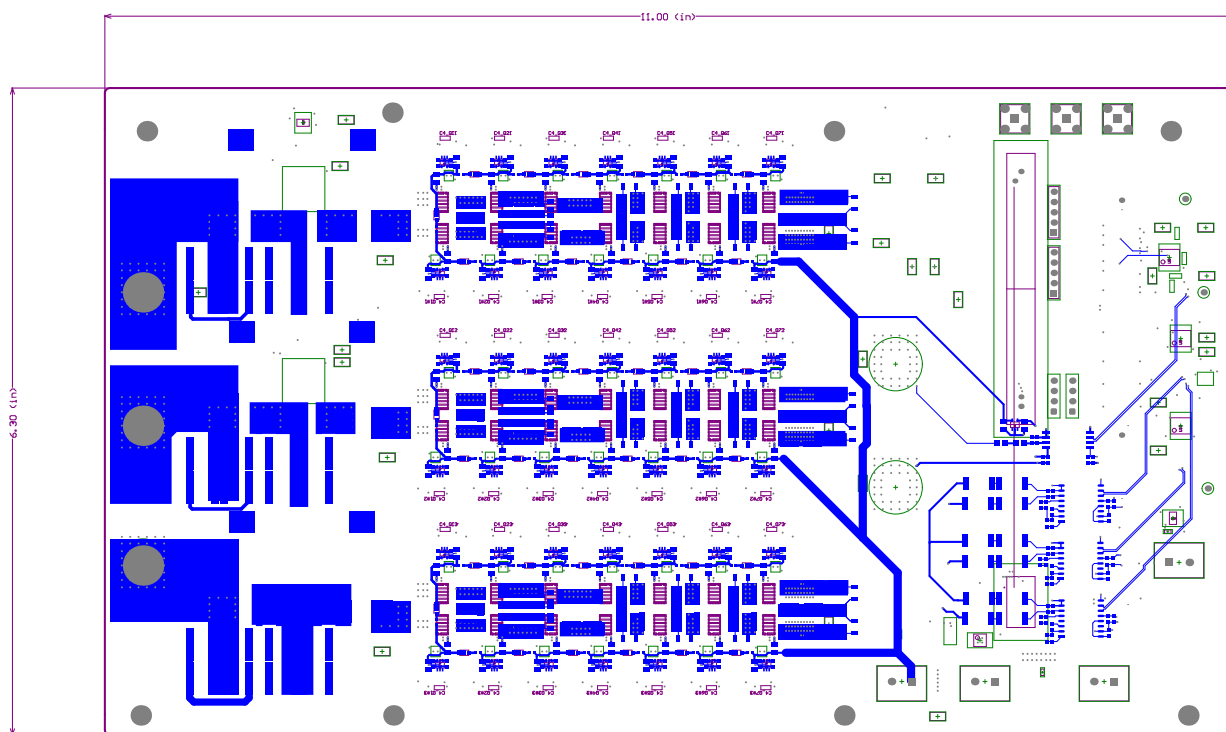




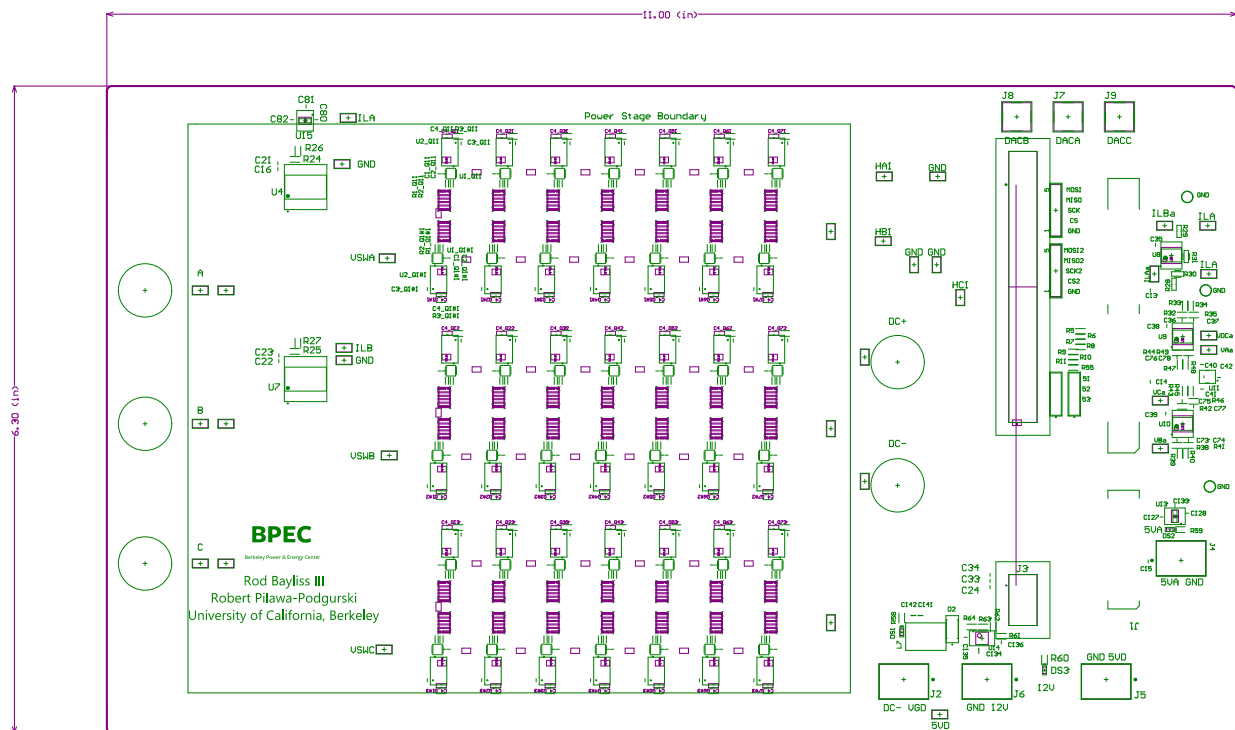


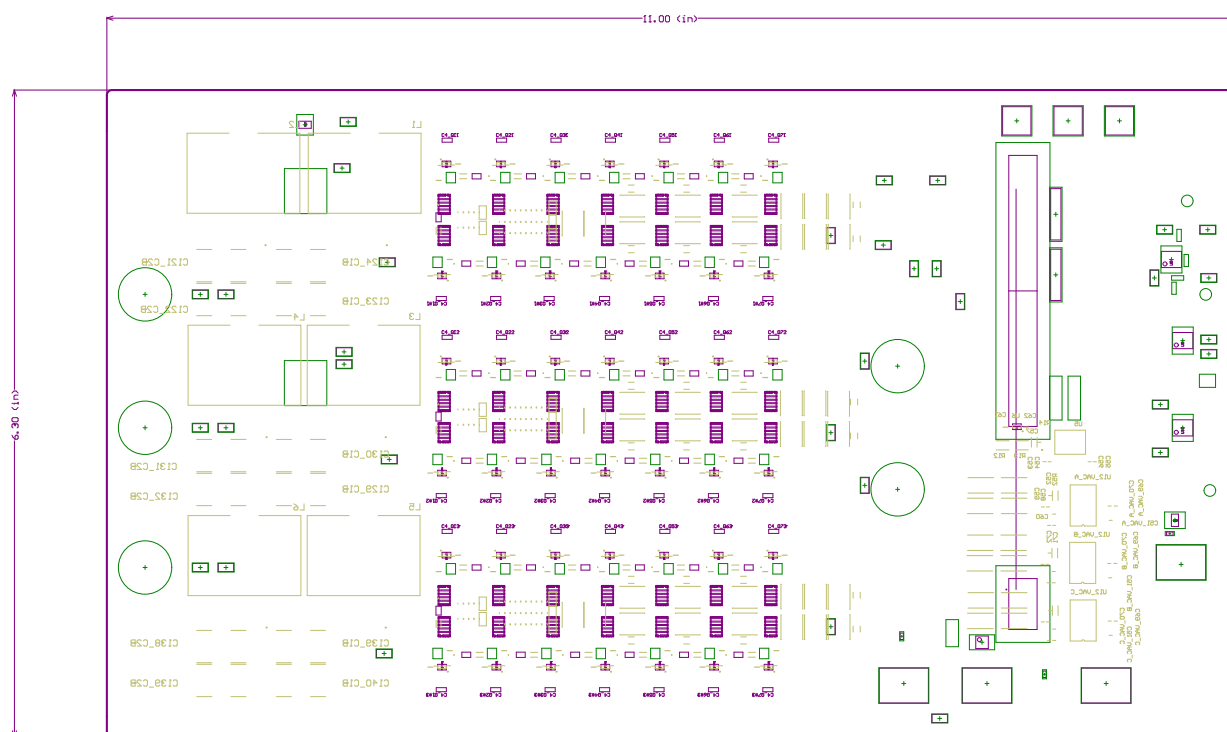






APPENDIX E. THREE-PHASE EIGHT-LEVEL FCML RECTIFIER SCHEMATICS 220





Appendix F

Capacitively-Isolated FCML DC/DC Schematics

