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UNIVERSITY OF CALIFORNIA, SAN DIEGO

**Packaged X-band Phased-Arrays and High Data-Rate Switching Matrices in
Advanced CMOS Processes**

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Donghyup Shin

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor James Buckwalter
Professor William S. Hodgkiss
Professor Brian Keating
Professor Lawrence E. Larson

2013

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The dissertation of Donghyup Shin is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2013

DEDICATION

To my wife and daughter, and to my parents.

TABLE OF CONTENTS

Signature Page	iii
Dedication	iv
Table of Contents	v
List of Figures	vii
List of Tables	xii
Acknowledgements	xiii
Vita	xv
Abstract of the Dissertation	xvii
Chapter 1 Introduction	1
1.1 Phased-Arrays	1
1.2 Integrated Circuit Packaging	4
1.3 Switching Matrices	5
1.4 Dissertation Overview	8
Chapter 2 Packaged X-band Phased-Array Receiver in 0.13- μ m CMOS . . .	10
2.1 Introduction	10
2.2 Design	11
2.3 On-Chip Measurements	20
2.4 Chip-On-Board Packaging: Simulations and Measurements .	26
2.5 Conclusion	34
2.6 Acknowledgment	34
Chapter 3 Packaged X-band Phased-Array Transmitter in 0.13- μ m CMOS . .	35
3.1 Introduction	35
3.2 Design	36
3.2.1 Block Diagram and Technology	36
3.2.2 Active 1:4 Divider	39
3.2.3 Active Phase Shifter	39
3.2.4 Power Amplifier	43
3.2.5 Input and Output Baluns	43
3.2.6 Bias and Control	48
3.3 Measurements	50
3.3.1 S-Parameter Measurements: Small Signal	50
3.3.2 S-Parameter Measurements: Large Signal	50

	3.3.3 Spectral Regrowth and EVM	53
	3.3.4 On-Chip Coupling	54
	3.4 Packaging	54
	3.5 Conclusion	64
	3.6 Acknowledgment	64
Chapter 4	12 Gbps 4x4 Switching Matrices in 0.13- μ m CMOS	67
	4.1 Introduction	67
	4.2 Design	68
	4.3 Measurements	75
	4.4 Conclusion	77
	4.5 Acknowledgment	82
Chapter 5	Scalable High Data-Rate Switching Matrices in 45nm CMOS . . .	83
	5.1 Introduction	83
	5.2 Design	84
	5.2.1 Scalable Architecture	84
	5.2.2 Passive Switch Design	88
	5.2.3 Bandwidth Extension using Inductive-Peaking Amplifier	92
	5.3 Measurements	96
	5.4 Conclusion	104
	5.5 Acknowledgment	105
Chapter 6	Conclusion	106
Appendix A	2 $\times$ 2 and 4 $\times$ 4 CMOS Switching Matrices for 0.01–12 GHz Applications	108
	A.1 Introduction	108
	A.2 2 $\times$ 2 and 4 $\times$ 4 Switching Matrix: Design	109
	A.3 Implementation	113
	A.4 Measurements	113
	A.5 Conclusion	116
Bibliography		117

LIST OF FIGURES

Figure 1.1:	Antenna array and electromagnetic wave from angle θ . All-RF architecture shown.	2
Figure 1.2:	Block diagram of $N \times N$ switching matrix in cross-point architecture.	6
Figure 1.3:	Switching matrix application in a beam-link system.	6
Figure 1.4:	Conceptual block diagram of a reconfigurable RF frontend.	7
Figure 2.1:	Block diagram of the 4-element high-linearity phased-array chip.	12
Figure 2.2:	Topology comparison for X-band phased-array receiver. Topology #3 results in the best power consumption for specific gain/NF/linearity combination.	12
Figure 2.3:	Circuit diagrams of (a) LNA, VGA and (b) switched LC phase shifters.	13
Figure 2.4:	Simulated insertion loss and phase difference of the switched LC phase shifters.	14
Figure 2.5:	The IBM8RF metal stack and a $50\ \Omega$ CPW transmission line in the top metal layers.	16
Figure 2.6:	Comparison of S_{22} for the cascode and common-source amplifiers under different phase shifter settings.	16
Figure 2.7:	(a) Layout, circuit model and (b) simulated S-parameters of the 4:1 Wilkinson combiner (port 5 is the output port).	17
Figure 2.8:	Chip microphotographs of the (a) 4-element and (b) single-element phased-array receivers.	19
Figure 2.9:	Simulation setup and coupling for different on-chip decoupling capacitors.	20
Figure 2.10:	Measured and simulated return loss.	21
Figure 2.11:	Measured and simulated gain, insertion phase and relative phase difference without using the VGA or 11° bit.	22
Figure 2.12:	Measured and simulated average noise figure over 16 phase states.	23
Figure 2.13:	Measured and simulated IP_{1dB} and IIP_3 . The P_{1dB} and IP_3 are within ± 0.25 dB for all 16 phase states.	23
Figure 2.14:	Measured and simulated gain and associated <i>rms</i> gain and phase error with the VGA and the 11° bit.	24
Figure 2.15:	Measured on-chip coupling between different input ports (see Fig. A.4 for port definition).	24
Figure 2.16:	(a) Top view and cross-section of the chip-on-board packaging method, and (b) equivalent circuit diagram including all simulation blocks.	25
Figure 2.17:	Simulation setup and resulting S-parameters vs. L_{GND1} ($L_{GND2} = 40$ pH). The amplitude and phase change in channel 1 vs. the phase state of channel 2 is also shown.	27

Figure 2.18:	Bondwire and printed-circuit-board simulation using HFSS for (a) 400 μm and (b) 800 μm -pitch feedlines with a grounded stub between the bondwires.	28
Figure 2.19:	(a) Photograph of packaged phased-array chip, (b) input and output matching networks, and (c) simulated S-parameters of the printed-circuit-board distribution network ($S_{51} \cong -0.6$ dB and $S_{11} < -10$ dB at 8.5-10.5 dB).	29
Figure 2.20:	Measured and simulated S-parameters for the chip-on-board phased-array. The S_{11} , S_{55} and S_{51} are average values over all phase states.	30
Figure 2.21:	(a) Vectorial representation of the channel-to-channel coupling, and measured and simulated amplitude and phase error of channel 1 when the phase state of (b) channel 2 and (c) channel 4 is changed in the chip-on-board phased array.	31
Figure 3.1:	Block diagram of 4-element phased-array transmitter.	37
Figure 3.2:	Metal stack-up of IBM8RF 0.13- μm CMOS process.	37
Figure 3.3:	Circuit schematic of a single channel: (a) active 1:4 divider and (b) phase shifter and power amplifier.	38
Figure 3.4:	Simulated power gain and output power, and normalized phase vs. input power of active divider at 9.0 GHz.	40
Figure 3.5:	Simulated I/Q phase and amplitude error of the all-pass network.	40
Figure 3.6:	Simulated (a) i_I and i_Q at 22.5° phase state, and (b) phase vs. input power defined at the QAF input port.	41
Figure 3.7:	Measured and simulated power amplifier (a) gain, and (b) output power, PAE, and phase distortion vs. input power.	44
Figure 3.8:	Measured and simulated power amplifier output power P_{SAT} , P_{1dB} , and PAE vs. frequency.	45
Figure 3.9:	Measured and simulated power amplifier second and third harmonic components vs. input power at 9.0 GHz.	45
Figure 3.10:	(a) Input and output baluns with wideband matching network and (b) simulated frequency response.	46
Figure 3.11:	Microphotograph of X-band 4-element phased-array transmitter chip (2.9 $\times$ 3.0 mm ²).	47
Figure 3.12:	Measured and simulated small-signal (a) input and output reflection coefficient, (b) gain, (c) phase response and (d) differential phase response (normalized to 0°) for 16 phase states. VGA and trim-bit were used to reduce the <i>rms</i> gain and phase error.	49
Figure 3.13:	Polar diagram showing measured phase and gain at 9.0 GHz.	51
Figure 3.14:	Measured (a) output P_{1dB} and P_{SAT} , and (b) phase vs. input power at 9.0 GHz. VGA set at maximum gain state.	51
Figure 3.15:	Measured large-signal (a) gain, (b) phase response and (c) differential phase response (normalized to 0°) for 16 phase states. VGA set at maximum gain state.	52

Figure 3.16:	Measured output spectrum for (a) QPSK and (b) BPSK modulation at different output power levels.	54
Figure 3.17:	Measured EVM for (a) QPSK and (b) BPSK vs. input power at 8.7 GHz.	55
Figure 3.18:	Measured QPSK (a) 10 MSym/s and (b) 20 MSym/s constellation vs. output power at 8.7 GHz.	56
Figure 3.19:	Cross-section of QFN package ($6 \times 6 \text{ mm}^2$) and chip-on-board on a Rogers RT5880 substrate	56
Figure 3.20:	(a) 3-D EM simulation setups of the silicon chip, baluns and bondwires in a package using HFSS, and (b) the resulting S-parameters.	58
Figure 3.21:	Bonding diagram of X-band phased-array transmitter chip in a QFN package.	59
Figure 3.22:	Circuit environment of the packaged phased-array transmitter including silicon chip, package 3-D EM simulation, and on-board matching/distribution network with bondwire inductances.	59
Figure 3.23:	Photograph of the (a) packaged X-band phased-array transmitter on a Rogers RT5880 substrate and (b) close-in view of QFN and chip-on-board.	60
Figure 3.24:	Measured (a) reflection coefficients and (b) average gain of 16 phase states and (b) P_{SAT} compared to the on-chip measurement of QFN and CoB packaged X-band phased-array transmitter.	62
Figure 3.25:	(a) Vectorial representation of channel-to-channel coupling, and (b) measured <i>rms</i> gain and phase error of channel 1 when changing the phase states of channel 2, 3, and 4 in a QFN and CoB package. . . .	63
Figure 4.1:	Schematic of a 4×4 switch matrix. The resistors at the end of each line are optional and allow for a matched load if an input port is not switched to an output port.	69
Figure 4.2:	IBM8HP metal stack-up. The CPW line is built in the top three layers.	69
Figure 4.3:	The 4×4 switch unit-cell with the series-shunt-series switch, (b) details of the CPW cross-over, and (c) cross-over isolation using full electromagnetic simulations.	70
Figure 4.4:	Simulated figure of merit (FOM) for a $0.13 \text{ }\mu\text{m}$ deep n-well CMOS transistor in a series configuration with $V_{GS}=1.5 \text{ V}$	70
Figure 4.5:	Series-shunt-series switch: (a) circuit diagram and (b) cross-section.	71
Figure 4.6:	(a) Circuit diagram for an input-to-output interconnection, and (b) simulated insertion loss and isolation vs. series switch width.	73
Figure 4.7:	Microphotograph of the 4×4 switch matrix. The chip size is $1.4 \times 1.5 \text{ mm}^2$	74
Figure 4.8:	Measured and simulated (a) S_{nn} ($n=1-8$) and (b) insertion gain for the two different 4×4 switching matrices.	76
Figure 4.9:	Measured and simulated isolation for the two different 4×4 switching matrices.	78

Figure 4.10:	Measured and simulated large signal performance: (a) Input P_{1dB} and IP_3 , and (b) insertion gain and isolation vs. input power. Measurements are done on the 4×4 switch matrix without termination resistors.	79
Figure 4.11:	(a) Measured and simulated group delay for the shortest (S_{21}) to longest (S_{87}) path. (b) Measured eye diagrams for different data rates.	80
Figure 5.1:	Block diagram of switch matrices of (a) cross-point architecture and (b) multiplexer-based architecture.	84
Figure 5.2:	Block diagrams and simplified small-signal model of all-passive switching matrices (a) with and (b) without isolation switches. . . .	85
Figure 5.3:	Simulated 3-dB bandwidth vs. N (number of input and output channels) of switching matrices with and without isolation switches. . .	86
Figure 5.4:	Block diagram of (a) all-passive and (b) passive-active switching matrices.	87
Figure 5.5:	(a) Metal stack-up and (b) cross-section of IBM 45-nm SOI CMOS (12S0) technology.	89
Figure 5.6:	Layout structure of unit switching cell and 2×2 cell, and simulated isolation between ports of 2×2 cell.	91
Figure 5.7:	Optimization of 2×2 switching cell	93
Figure 5.8:	Simulated insertion loss and isolation of a unit cell and 2×2 cell. . .	93
Figure 5.9:	3-dB bandwidth of switch matrices of different scales with and without isolation switches	94
Figure 5.10:	Simulated (a) normalized gain and (b) normalized group delay vs. frequency for 2×2 cell alone, buffer alone, and 2×2 cell and buffer together.	95
Figure 5.11:	Microphotograph of (a) all-passive and (b) passive-active 4×4 switch matrices. The chip sizes are both $1.4 \times 1.4 \text{ mm}^2$	97
Figure 5.12:	Measured and simulated return loss, insertion gain, isolation and group delay of (a) all-passive and (b) passive-active 4×4 switch matrix.	98
Figure 5.12:	Measured and simulated return loss, insertion gain, isolation and group delay of (a) all-passive and (b) passive-active 4×4 switch matrix. (cont.)	99
Figure 5.13:	Measured and simulated input P_{1dB} of 4×4 switch matrices.	100
Figure 5.14:	Measured eye diagrams of (a) all-passive and (b) passive-active 4×4 switch matrices for PRBS input signals of different data-rates. . . .	101
Figure 5.15:	Comparison of eye diagrams of out of THRU pattern and switching matrices.	102
Figure 5.16:	Measured RMS jitter for THRU pattern, and (a) all-passive and (b) passive/active 4×4 switch matrices.	103
Figure A.1:	Schematic of 2×2 switching matrix.	109

Figure A.2:	(a) Circuit model of series-shunt-series cell and (b) simulated insertion loss, isolation and reflection coefficient of a series-shunt-series cell at 12 GHz versus series FET width.	110
Figure A.3:	Block diagram of 4×4 switching matrix.	111
Figure A.4:	Micro-photograph of (a) 2×2 and (b) 4×4 switching matrix.	112
Figure A.5:	Measured (solid) and simulated (dashed) insertion loss, return loss, and isolation of 2×2 switching matrix.	114
Figure A.6:	Measured (solid) and simulated (dashed) insertion loss, return loss, and isolation of 4×4 switching matrix.	115

LIST OF TABLES

Table 2.1:	Performance Comparison of Silicon Phased Array Receivers	33
Table 3.1:	Vector Modulator I/Q DC Current Level	39
Table 3.2:	Summary of the Performance	65
Table 4.1:	Performance Comparison of Switch Matrices	81

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- Donghyup Shin and G. M. Rebeiz, "Low-Power Low-Noise 0.13- μ m CMOS X-Band Phased Array Receivers," in *IEEE MTT-S Int. Microw. Symp.*, Anaheim, CA, May 2010.

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- Donghyup Shin, C. Y. Kim, D. Kang, and G. M. Rebeiz, "A 4-Element X-Band CMOS Phased-Array RFIC in a QFN Package," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Montreal, Canada, June 2012, pp. 1–3.
- Donghyup Shin, C. Kim, D. Kang, and G. M. Rebeiz, "A High-Power Packaged Four-Element X-band Phased-Array Transmitter in 0.13- μ m CMOS for Radar and Communication Systems," *IEEE Trans. Microw. Theory Tech* (in review).

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- Donghyup Shin and G. M. Rebeiz, "A 32-Gbps 4×4 Passive Cross-Point Switch in 45-nm SOI CMOS," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, June 2013.

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Donghyup Shin, D. Kang, and G. M. Rebeiz, “A 0.01-8 GHz (12.5 Gbps) 4×4 CMOS Switch Matrix,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 2, pp. 381–386, Feb. 2012.

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Donghyup Shin and G. M. Rebeiz, “Low-Power Low-Noise 0.13- μm CMOS X-Band Phased Array Receivers,” in *IEEE MTT-S Int. Microw. Symp.*, Anaheim, CA, May 2010.

Donghyup Shin and G. M. Rebeiz, “ 2×2 and 4×4 CMOS Switching Matrices for 0.01-12 GHz Applications,” in *Compound Semiconductor Integrated Circuit Symp. (CSICS)*, Greensboro, NC, Oct. 2009.

ABSTRACT OF THE DISSERTATION

Packaged X-band Phased-Arrays and High Data-Rate Switching Matrices in Advanced CMOS Processes

by

Donghyup Shin

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Gabriel M. Rebeiz, Chair

This thesis explores two areas in RF integrated circuits. The first area of work is X-band phased-array design in CMOS technology. A receiver and a transmitter chip is designed, fabricated, measured on-wafer, and then packaged on printed-circuit boards using chip-on-board technique and in QFN modules to verify the reliable operation of silicon chip after packaging. The high-linearity four-element phased-array receiver for 9-10 GHz application is built using 0.13- μm CMOS process with a single-ended design, and it results in a measured gain of 10 dB, an input P_{1dB} 12.5 dBm, and a noise figure of 3.4 dB at 9.5 GHz. An *rms* gain error of 0.4 dB and phase error of 8° are obtained at 9-10 GHz using an integrated variable gain amplifier and an 11° phase trim bit.

The 4-element X-band transmitter chip is also developed in 0.13- μm CMOS

technology. The design contains an active 1:4 power divider, active 5-bit phase shifters (lowest bit is used as a trim bit), 4-bit gain control (to reduce the *rms* gain error), and power amplifiers capable of delivering a P_{SAT} of 13.5 dBm per channel at 8.5-10.5 GHz. The chip can be used in the linear mode for communication systems and in the saturated mode for FMCW radar systems. Packaging based on chip-on-board and QFN modules have been implemented, and both show a very small nearest neighbor coupling of $\sim$ -30 dB at 8-10 GHz, limited by bond-wire coupling.

The second area of work is the switching matrices for high data-rate networking. Two generation of design is implemented and the first-generation is the 0.01–8-GHz 4×4 switch matrix in 0.13- μ m CMOS technology. A deep n-well series-shunt-series switch is chosen as the switching core, and the transistor sizes are optimized for low insertion loss and high isolation up to 8 GHz. A full electromagnetic analysis is performed on the switching core to result in a compact design with high isolation. The 4×4 switch matrix shows a measured insertion loss of 2.0–3.3 dB and an isolation of 50–44 dB at 2–8 GHz with near-zero power consumption. The measured input P_{1dB} and IP_3 are 8-10 and 26-30 dBm at 0.5-8 GHz. The switching matrix has very low dispersion with 6-ps group-delay variation and can switch a 12.5-Gb/s signal with a bit error rate of $<10^{-12}$.

The second-generation switching matrix is implemented using IBM 45-nm SOI CMOS process, which offers advanced switch performance. The design is focused on the optical/digital wideband signal networking, and therefore optimization is done to maximize the bandwidth and minimize the added jitter after switching. A cross-point architecture with passive CMOS switch is used to achieve switching with near-zero power consumption. Scalability of all-passive design is maximized by introducing isolation switches placed after every 2×2 switching cells. An inductive-peaking buffers are used on passive-active design in order to further increase the bandwidth of the matrix. The measured 3-dB bandwidth of all-passive and passive-active design are 20-25 GHz and >26.5 GHz (measurement limit), with very low group delay variation of ± 5 and ± 2 psec, respectively. The eye-diagram measurement shows that all-passive design can transfer signals up to 30-Gbps and passive-active design can achieve up to 44-Gbps of data-rate. The scalability of passive-active design ensures constant 3-dB bandwidth up to more than 12×12 matrix.

Chapter 1

Introduction

1.1 Phased-Arrays

A phased-array is an array of antennas with appropriate phase delays on each element, and provides beamforming and electronic beam-steering. Compared to a mechanical steering antenna, phased-arrays offer very fast (almost instantaneous) beam-steering with higher accuracy and can quickly detect signals from multiple directions. Also, power-combining of multiple elements results in higher signal power and improved signal-to-noise ratio (SNR) compared to the single element due to coherently added signal power and incoherently added noise power [1–3].

The beam-forming and steering is achieved by a constructive interference between the electromagnetic waves from a desired direction and destructive interference from other directions. Fig. 1.1 shows a exemplary 8-element phased-array receiver with an incident wave from an angle θ . Due to the finite distance between antenna elements d , the received signals at the antennas have phase differences of

$$\Delta\phi = kd \cos \theta \quad (1.1)$$

between adjacent elements, where k is the wavenumber ($2\pi/\lambda$). Therefore, the combined signal will have the maximum constructive interference when the antenna elements have a progressive phase delay of $kd \cos \theta$. In other words, when the antenna elements have a progressive phase delay of ϕ , the phased array steers the beam to

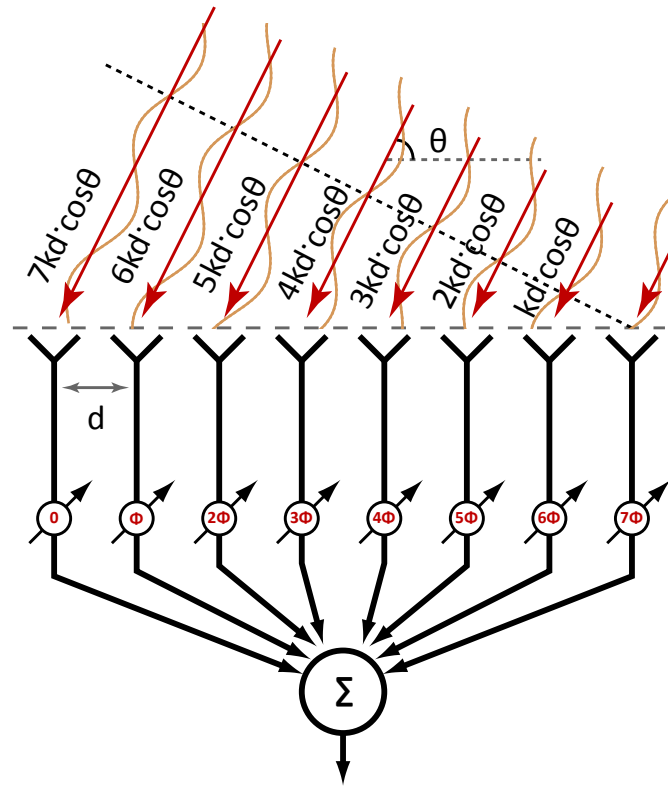


Figure 1.1: Antenna array and electromagnetic wave from angle θ . All-RF architecture shown.

$$\theta = \cos^{-1} \frac{\Delta\phi}{kd} \quad (1.2)$$

This can also be explained using an antenna-array radiation patterns. Under the far-field radiation assumption, the radiation pattern of an array antenna can be derived as a single antenna element pattern (element factor, EF) multiplied by an array factor (AF), which is represented as

$$AF = \frac{\sin(\frac{N}{2} \frac{2\pi}{\lambda} d \cos \theta + \phi)}{\sin(\frac{1}{2} \frac{2\pi}{\lambda} d \cos \theta + \phi)} \quad (1.3)$$

where N is the number of elements, d is the distance between elements, λ is the wavelength of the incident wave, θ is the incident angle, and ϕ is the progressive phase delay between each elements.

Since the original development by Nobel Laureate Karl Ferdinand Braun in 1905 [4], phased-arrays have been widely adopted in communication systems and radar applications. In defense system, large-scale phased arrays for missile/target detection are now common in naval ships and aircrafts, and aircraft landing assistance systems also use phased-arrays for detection of objects in multiple directions. For scientific research, phased-arrays are also applied for astronomical observation, weather detection, and air quality monitoring with higher resolution. Currently, the application area encompasses not only communications, but also in pipe flaw detection, medical imaging, RFID, etc.

The phase delay in each element can be realized using a true time-delay (TTD) unit or a phase shifter. It can be done in RF, LO, IF, or digital domain and each architecture has its own advantages and disadvantages. However, RF phase-shifting architecture is the most widely used because of its simplicity and relaxed linearity requirement on the mixer. In the All-RF architecture, signals are combined after phase-shifting at each element and spatial filtering is done before the mixer input. Therefore, interferer from non-desired direction is suppressed and the linearity requirement of the mixer is relaxed.

Before silicon technology, the phased-array implementation was done using GaAs discrete components assembled together on a multi-layer board and connected to antennas. This is heavy, bulky, and expensive for large-scale production. Silicon technology offers an opportunity of compact design and integration of multi-functions, and

leads to a lower-cost production. Phased-arrays in silicon technology has been an active research area, and there are successful implementations of all-RF architecture in various frequency bands [5–12]. IF/LO and digital beam-forming (DBF) architectures were also demonstrated using CMOS and SiGe technology [13–15]. The silicon phased-arrays packaged and assembled together with antenna arrays, or with on-chip antenna can be designed such that the packaging loss is minimized [14, 16].

1.2 Integrated Circuit Packaging

Silicon IC designs require a low cost package to make an interface to the exterior devices/equipment for real applications. The packaging techniques has been rapidly evolved over several decades together with the silicon technology. However, the performance degradation is inevitable due to the parasitic effects especially for high-frequency applications. Therefore, IC designers must take into consideration the packaging effects for a successful implementation. IC packaging includes chip mounting on printed-circuit boards (PCB) and encapsulation. Within various types of chip-mounting techniques (flip-chip, quilt-packaging, etc), wirebonding is most popular and cost-efficient. The bondwire creates an inductive path from the PCB lead to the silicon chip pad, with a typical inductance of 1 nH/mm. Flip-chip techniques reduce the inductance, but it is not as cost-efficient as wirebonding except for very high volumes. The added wirebond inductance distorts the impedance matching, which increases the reflection and the loss at the chip-to-board interface. This requires an on-board matching network or a wideband capacitive matching at the silicon chip. The more detrimental effect of the bondwire inductance is between the on-chip ground and the package ground. After packaging, the reference ground plane is the package ground, and the on-chip ground becomes (a bit) floating as a result of this ground inductance. This creates gain reduction, instability, and crosstalk between the multiple RF ports on the silicon chip, especially for single-ended design, and the effect worsens as the inductance gets higher. Differential circuits are less susceptible to the ground inductance due to the common-mode rejection, but CMRR is reduced as a result of the ground inductance and this may affect the circuit performance.

Encapsulation offers electrical, thermal, and mechanical protection of the silicon chip. For phased-arrays, mechanical protection is especially important because the PCB with the antenna array is usually much larger than the silicon chip, and the board can easily bent, damaging the bondwires. There are numerous encapsulations available, and quad flat no-lead (QFN) package is a good candidate for RFIC chips because of its reduced inductance due to its absence of lead legs. Also, QFN is cost efficient and easily attached to the board with excellent thermal property [17]. The problem induced from the encapsulation is the increased capacitance between the pads and wirebonds as a result of mold compound which is filled inside the package. This capacitive coupling between the leads can reduce the isolation between the RF ports.

The packaging parasitics can be modeled as inductors and capacitors, but the values vary depending on how they are packaged. Therefore, in order to successfully estimate the packaging effect, 3-D modeling using electromagnetic solvers (e.g., HFSS [18]) are required especially for high frequency circuits.

1.3 Switching Matrices

Switching matrices (also known as crossbar switch, cross-point switch, or matrix switch) are multiple input - multiple output switches widely used in communication and automated measurement systems. Switching matrices have been used from primitive telephone networks to digital data networking in local and wide area networks (LAN and WAN). As the area of network becomes wider, demand for high-speed digital switching matrices is getting higher. Digital packet switching is also required on smaller domains includes servers, routers, storage system/device, multi-core processors, etc.

Switching matrices are also used in satellite systems to maximize the bandwidth utilization and reduce the system redundancy. Figure 1.3 presents an example of a satellite application such as a beam-link system [21]. The receiver takes multiple signals from different locations and switch them to the intended spots. The switching matrix provides the flexibility to direct the subchannels to the desired downlink beam. Also, the switching matrix can be used to take the input signals at different frequency band and switch them to the desired baseband circuitry so that the system requires fewer number

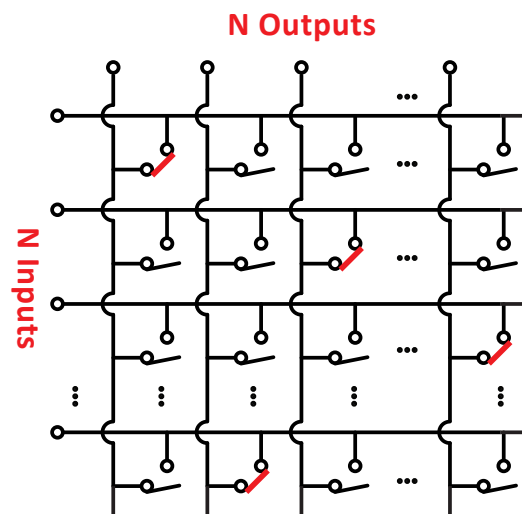


Figure 1.2: Block diagram of $N \times N$ switching matrix in cross-point architecture.

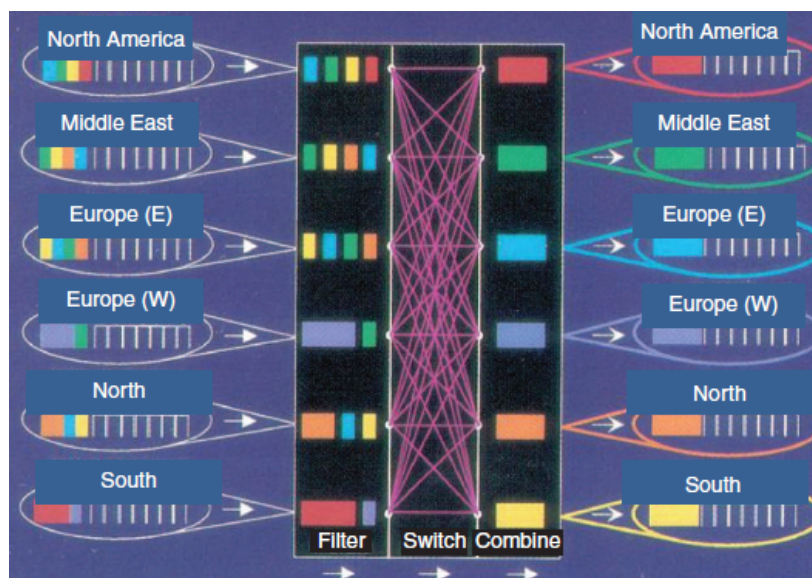


Figure 1.3: Switching matrix application in a beam-link system.

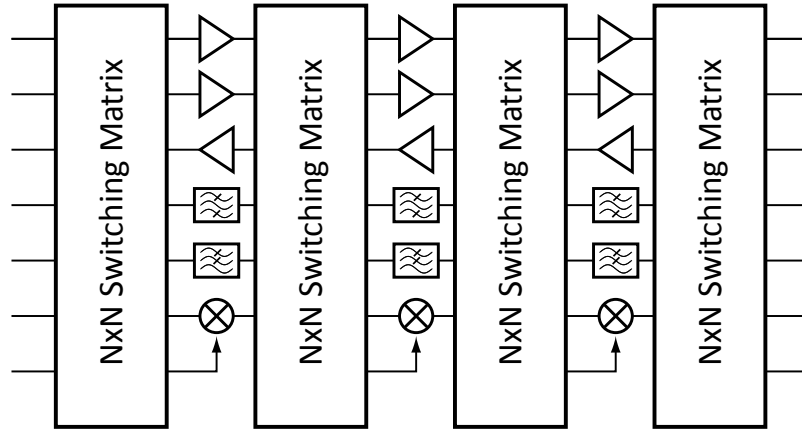


Figure 1.4: Conceptual block diagram of a reconfigurable RF frontend.

of back-end circuitry.

A reconfigurable RF frontend is another field of application of switching matrices which is under research [22]. An example of reconfigurable frontend architecture is shown on Fig. 1.4, which comprises switching matrices and any RF building blocks such as a matching network, LNA, PA, mixer, and filters. The switching matrices are programmed such that the injected RF signal can be fed to any desired building block, and as a result the reconfigurable RF frontend can process signal of multiple frequency bands and standards.

In silicon technology, numerous techniques have been proposed on switching matrices especially for optical/digital signal networking [23–33]. Note that rather than a cross-point architecture, multiplexer-based design, which is composed of multiple multiplexers, clock, and buffers, have been the dominant architecture. This is because the cross-point architecture is believed to have limitation on the scalability and switching speed due to its large capacitive loading. However, significant DC power consumption is the weakness of MUX-based designs. As CMOS technology advances, the loading capacitance of CMOS switches is getting smaller, and by applying circuit techniques and careful electromagnetic modeling, the CMOS cross-point architecture is also proved possible for high-speed switching matrix.

1.4 Dissertation Overview

This dissertation presents phased-array RFICs designed with emphasis on packaging effects, and high data-rate CMOS switching matrices. First, an X-band phased-array receiver and transmitter chip are implemented on 0.13- μm CMOS and packaged on printed-circuit board using chip-on-board technique and in QFN (quad flat no-lead) modules. The package effect is intensively analyzed using 3-D electromagnetic solvers (HFSS, Sonnet, and ADS Momentum) and agrees well with measurements. The high data-rate switching matrices are based on a cross-point architecture using passive CMOS switches to reduce the DC power consumption. The design is focused on higher data-rate (i.e. higher bandwidth), and the highest data-rate of >40 Gbps is achieved by using advanced SOI CMOS process and active buffers to boost the bandwidth.

Chapter 2 demonstrates the design of a 4-element X-band phased-array receiver using 0.13- μm CMOS and explores the simulated and measured effect of packaging on duroid substrate using bondwires. Since the design is intended for a hand-held communication device, tight specification on power-consumption, linearity, noise figure are required, and therefore, the all-RF architecture, passive phase-shifters/power-combiner, and gain-loss alternating scheme are chosen. Packaging effects from the bondwire inductance and on-package structure are fully analyzed to ensure that coupling between the channels is low enough for a phased-array operation.

Chapter 3 presents an X-band phased-array transmitter design using 0.13- μm CMOS. CMOS power amplifiers can generate moderately high power from each channel (± 13 dBm) and the phased-array chip is demonstrated in linear-mode in back-off power levels, and in saturated-mode, to ensure operation both in communication system using complex modulation (e.g. BPSK and QPSK) and in radar systems. Again, the silicon chip is packaged on a printed circuit board using chip-on-board technique and QFN packages, and the effect of package is analyzed in detail.

Chapter 4 presents the first generation of 4×4 CMOS switching matrices which can cover up to 12-Gbps data-rate of digital signal transfer. The design is based on a high frequency RF switch design approach and the wideband nature shows the possibility of high data-rate optical/digital networking circuit using passive CMOS switches.

The switching matrix work continues in chapter 5, which demonstrates two

designs of high data-rate switching matrices using an advanced CMOS process. The all-passive design achieves 30 Gbps data-rate with near-zero power consumption. The active-passive version, which applies bandwidth boosting by using bandwidth enhancement buffers, can achieve >40 Gbps operation. Scalability of the design is emphasized to ensure implementation of larger scale matrix with low degradation of performance.

Chapter 6 concludes the thesis. In addition, appendix A presents a 0-12 GHz 4×4 switching matrix using multiple 2×2 switches. Series-shunt-series switches with deep n-well and deep trenches are employed to result in a high isolation of >30 dB up to 12 GHz.

Chapter 2

Packaged X-band Phased-Array Receiver in 0.13- μm CMOS

2.1 Introduction

Silicon phased arrays with single and multiple elements on a single chip have been demonstrated at X/Ku-band using SiGe and CMOS technologies [7, 34–38]. The advantages of the *All-RF* architecture are its simplicity, system-level linearity, low power consumption (no mixer, no LO drivers, no LO distribution), and the use of a single high-performance receiver at the sum port of the phased array. The RF phase shifters are typically implemented either using vector modulators, switched LC-networks or switched transmission lines [8, 39, 40]. For multiple elements, on-chip lumped-element Wilkinson combiners are used to provide high linearity and zero power consumption [41].

This paper presents an improved X-band phased array with high linearity, low noise figure and low DC power consumption. The topology is based on alternating gain and phase shifter blocks, which shows the best dc power consumption, NF, and linearity combination. Cascode amplifiers are used throughout the chip for added isolation between the switched LC phase shifters, which is essential when using large transistors with higher bias current (needed for linearity improvement). Also, variable gain amplifiers are used to correct for the gain change at different phase states and for aperture amplitude tapering (Fig. 2.1).

The packaging of the silicon chip is also discussed in detail, with particular emphasis on the coupling between the channels which can be high in single-ended systems due to the packaging inductances. The on-chip V_{DD} decoupling capacitors and the ground bond-wire inductance are first taken into account, and their effect on the channel coupling is modeled in detail. Then, the mutual coupling between the input bondwires and the resulting channel-to-channel coupling is modeled using HFSS and Cadence. Finally, the silicon chip is packaged using chip-on-board techniques, and the measurements are compared with simulations. It is seen that excellent agreement is obtained using accurate EM and circuit modeling.

2.2 Design

The required performance from the chip are a gain of 11 dB per channel, an input P_{1dB} of -12 dBm (input IP_3 of -3 dBm), and a NF less than 3.5 dB at 9-9.5 GHz. This would allow the 4-element chip to be used together with a GaAs LNA front-end with 12 dB gain and 0.5 dB NF and result in a total system gain of 23 dB, and input P_{1dB} of -24 dBm (input IP_3 of -15 dBm) and an overall NF of 0.8 dB. The combined receiver would be competitive for point-to-point communications in high interference environments.

Fig. 2.2 presents three different circuit configurations for the X-band phased-array receiver under the assumption that the system requires a gain of 13 dB with IP_{1dB} of -13 dBm, and the phase shifters are based on passive CMOS switches which have a high linearity ($IIP_3 > 23$ dBm) and a P_{1dB} of 10–17 dBm [43]. The first design is based on a GaAs MMIC architecture with the LNA in front and the phase shifter at the back. While this results in the lowest noise figure, it also results in the highest power consumption due to the high P_{1dB} required at the output of the CMOS amplifier. The second design divides the amplifier into two units, one at the input and one at the output of the phase shifter. While this results in the best power consumption, it also results in a high NF of 4.4 dB and is not acceptable. The third design alternates amplifiers and phase shifter blocks in succession. In this case, the amplifier gain and its associated output P_{1dB} can be relatively low, which results in low power consumption and a NF of 3.3 dB. The alternating gain/phase-shifter approach is used and results in approximately

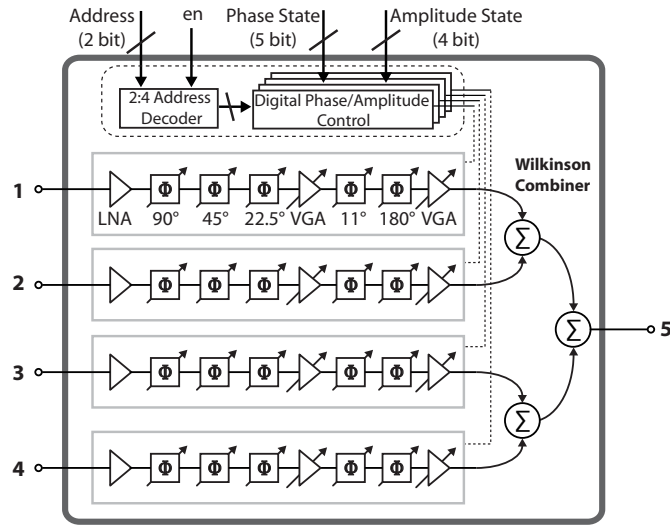


Figure 2.1: Block diagram of the 4-element high-linearity phased-array chip.

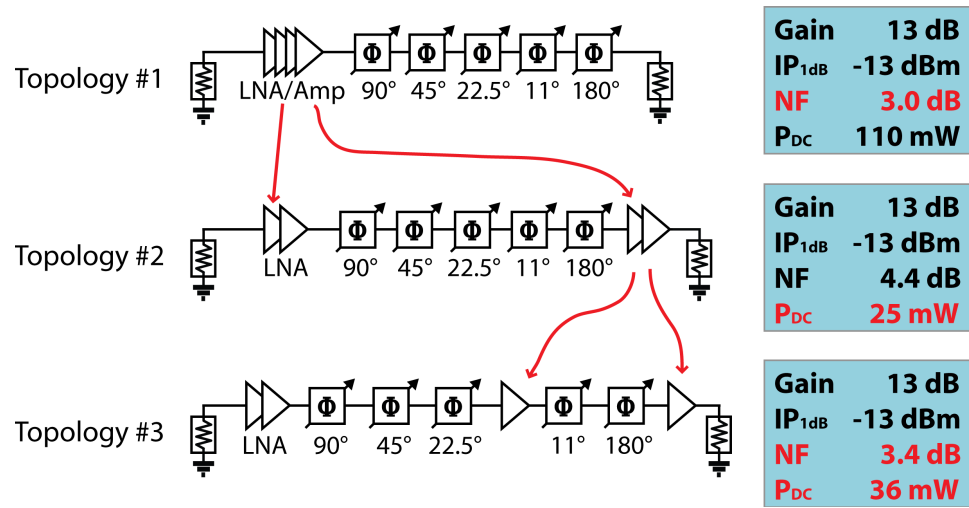


Figure 2.2: Topology comparison for X-band phased-array receiver. Topology #3 results in the best power consumption for specific gain/NF/linearity combination.

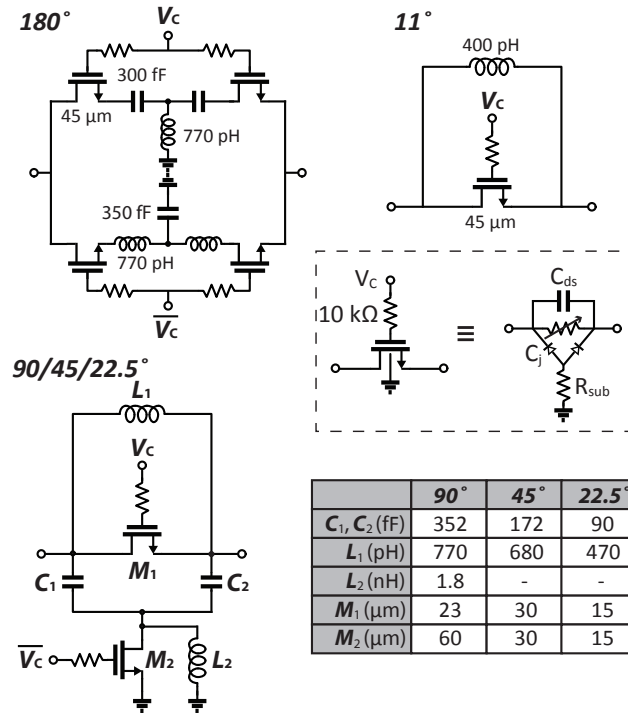
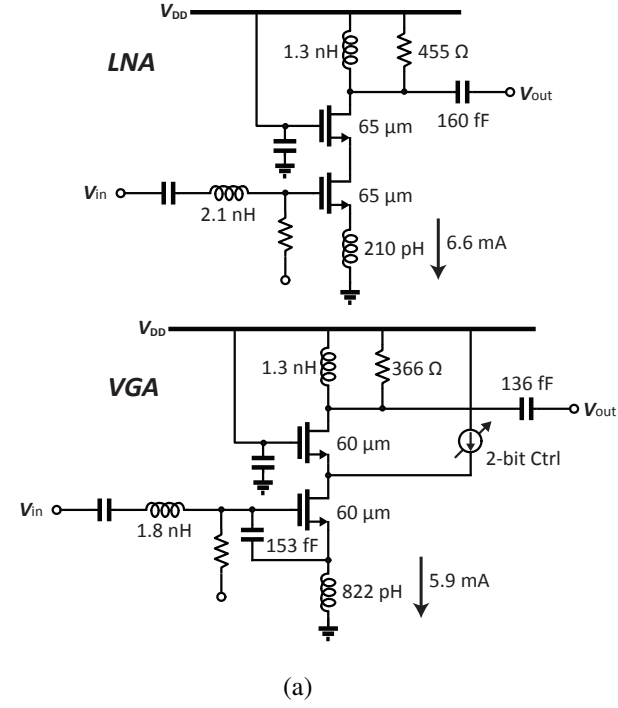


Figure 2.3: Circuit diagrams of (a) LNA, VGA and (b) switched LC phase shifters.

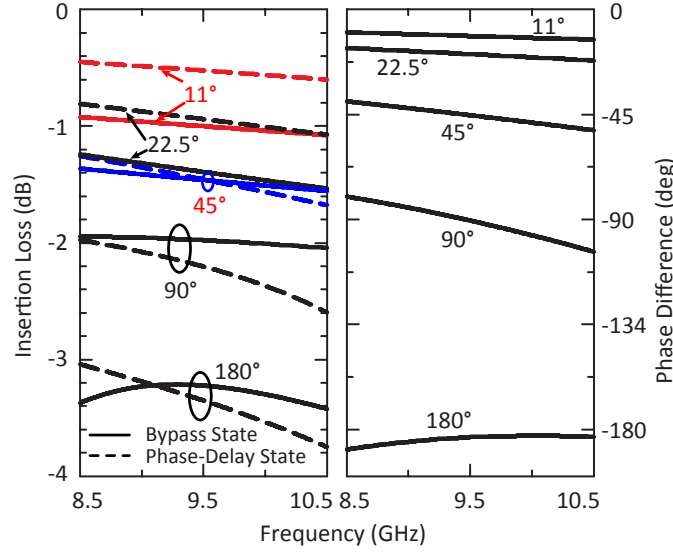


Figure 2.4: Simulated insertion loss and phase difference of the switched LC phase shifters.

30 % the power consumption than the traditional design based on an amplifier followed by a passive phase-shifter but at a slight increase in the noise figure.

For this work, a low cost 0.13 μm CMOS technology is used with an f_T of 100 GHz at a bias current of 0.1 mA/ μm (IBM8RF) and a $\text{NF}_{\min}$ of 0.8 dB at 10 GHz. The first stage is a cascode-based LNA with a simulated gain and NF of 13.4 dB and 1.95 dB, respectively, at 9.5 GHz, an input P_{1dB} of -10.3 dBm, and a power consumption of 7.2 mA from 1.8 V supply including the bias circuitry (Fig. 2.3(a)). The input and output impedances are designed to be 50 Ω so as to be impedance matched to the phase-shifter cells, and the simulated S_{11} and S_{22} are < -10 dB at 8.5-10.5 GHz (< -15 dB at 9-10 GHz).

Two 50 Ω variable gain amplifiers (VGAs) are also designed each with a 2-bit gain control of 0.8-4.0 dB (in 0.8-1.1 dB steps) at 9.5 GHz, a NF of 4.5-6.0 dB and a power consumption of 11.6 mW (Fig. 2.3(a)). The amplifiers show a low phase variation vs. gain state, around $\pm 5^\circ$ at 9.5 GHz, and compensate for the phase shifter gain variation with enough gain control to allow for an additional 4.5 dB taper on the phased array aperture. The first VGA is designed with an input P_{1dB} of -0.9 dBm so as to handle the output power of the LNA (after the 4 dB loss in the 90/45/22° phase shifter cells) and

its gain is limited to 4.0 dB for low DC power consumption. A high linearity is achieved using a large source inductor (822 pH). Also, a gate-to-source loading capacitance of 153 fF helps in the impedance matching by reducing the effect of the 822 pH at the gate node, at the expense of a slightly reduced gain [44]. The second VGA has nearly the same power levels after passing by the 180/11° phase shifter cells and therefore, the same circuit is used.

The 22.5°, 45° and 90° phase shifter cells are based on switched LC-networks that are commonly used in GaAs circuits [40]. These phase shifters have been designed before using CMOS transistors at Ka-band frequencies [8] and are summarized in Figs. 4.1 and 2.4. The LC values and transistor sizes are therefore optimized using Cadence so as to result in a minimum variation in the insertion loss vs. phase shifter state - too wide of a transistor results in high loss due to capacitive coupling, while too narrow of a transistor results in high loss due to R_{on} . The 180° cell is a high-pass/low-pass design, requires the use of two SPDT switches, that are 45 μ m transistors, and results in an insertion loss of 3.3 dB at 9-10 GHz. The 11° phase shifter cell is designed without the shunt transistor and inductor and results in good performance at X-band due to the small amount of phase shift. Note that the 180° cell results in a constant phase shift vs. frequency while the 90/45/22° cells result in a linear phase shift vs. frequency (Fig. 2.4). The 9-10 GHz bandwidth is low enough that this is not a problem, and the 11° cell is placed so as to “trim” the array for minimum *rms* phase error (see Section III).

In the above circuits, the transmission-lines are grounded CPW with dimensions of 10/14/10 μ m and a loss of 0.2 dB/mm at 9.5 GHz ($\epsilon_{eff}=4.1$, $Q=9.5$ at 9-10 GHz) (Fig. 2.5). The inductors are simulated using Sonnet [45] and have a Q of ~ 15 at 9-10 GHz. The capacitors are implemented using the library MIM capacitors with a $Q > 20$ at 10 GHz. Also, the phase shifters cells are optimized first alone in Sonnet, and then together (90/45/22° for example) in Sonnet and Cadence in order to ensure low electromagnetic coupling between the individual cells and a wideband impedance match. In general, all inductors are placed with at least a 70 μ m edge-to-edge spacing so as to ensure low mutual coupling.

The cascode amplifiers are essential for the high-linearity design and show a substantial improvement in the wideband receiver S-parameters as compared to single-

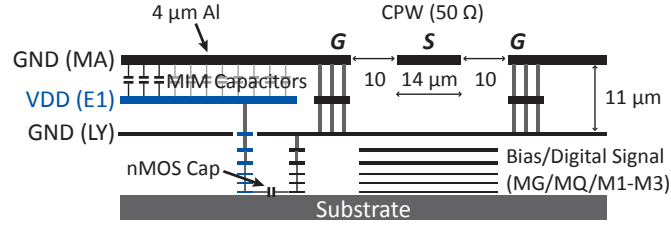


Figure 2.5: The IBM8RF metal stack and a 50 Ω CPW transmission line in the top metal layers.

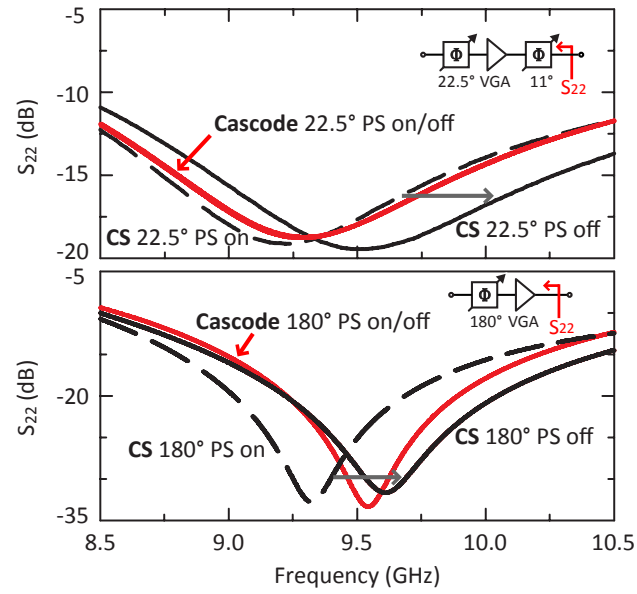


Figure 2.6: Comparison of S_{22} for the cascode and common-source amplifiers under different phase shifter settings.

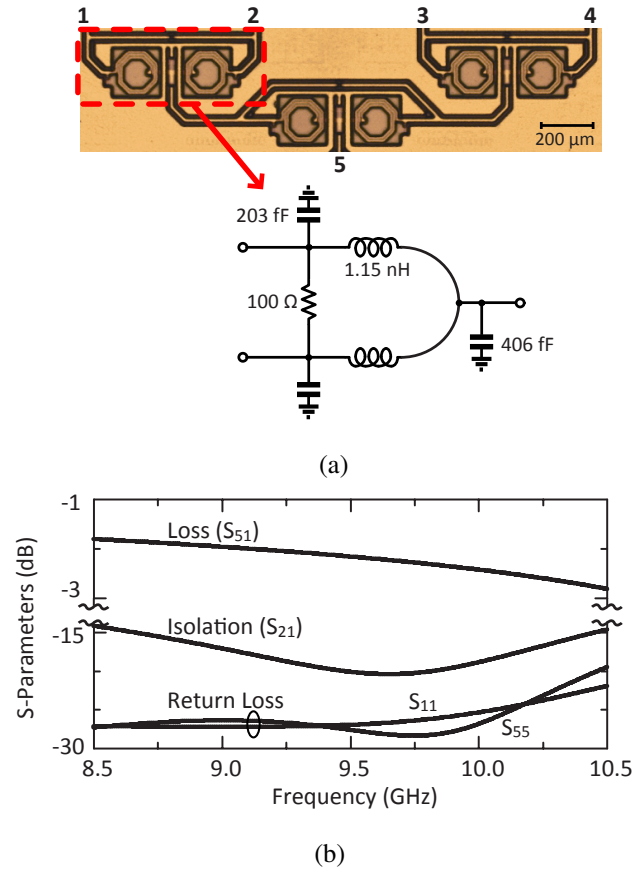


Figure 2.7: (a) Layout, circuit model and (b) simulated S-parameters of the 4:1 Wilkinson combiner (port 5 is the output port).

stage common-source amplifiers [42]. This is due to the high isolation in the cascode amplifier ($S_{12}=-36$ dB at 9-10 GHz) vs. the low isolation encountered in a common-source amplifier ($S_{12}=-13$ dB at 9-10 GHz). Fig. 2.6 presents the simulated S-parameter of the first VGA with the 22.5° and 11° cells, and of the second VGA with the 180° cell. It is seen that the 8.5-10.5 GHz S-parameters with the cascode design are more stable vs. phase-state than with the common-source design. The cascode amplifier does consume more power, but results in better overall performance and less *rms* gain error.

A passive combining network is required due to the high output P_{1dB} from the 4-element array (+3 dBm with no combining loss). The Wilkinson combiner is shown in Fig. 2.7 and is based on LC components with an interconnecting $100\ \Omega$ resistor and a simulated loss of 1.0 dB at 9.5 GHz. The overall loss of the 4:1 combiner is 2.1 dB at 9.5 GHz including the $50\ \Omega$ CPW interconnect loss (0.26 mm). The isolation is >17 dB and the input and output impedance match is <-25 dB at 9-10 GHz.

Since this is a single-ended design, the phased array channels are placed $>190\ \mu\text{m}$ from each other ($550\ \mu\text{m}$ center-to-center), and the area between the channels is filled with V_{DD} decoupling capacitors. To ensure excellent V_{DD} grounding, a total of 110 pF is used between V_{DD} and the on-chip ground for each channel, where the capacitors are a combination of 680 fF MIM capacitor and 1 pF nMOS capacitors with a Q of 7 at 10 GHz (this results in an R_S of $2\ \Omega$ and added stability). Also, continuous metal trenches are used between the channels and these connect the top ground metal layer to substrate contacts. The address lines, latches and biasing circuits are all routed underneath the LY ground layer and have no effect on the RF performance.

The simulated performance of the entire chain, including the Wilkinson combiner loss, show an average gain of 10.3 dB at 9.5 GHz with an *rms* gain error of <0.4 dB and a noise figure of 3.4 ± 0.2 dB at 9-9.5 GHz. The 4-bit phase performance has an *rms* phase error of $<10^\circ$ at 8.6-10.8 GHz, and it can be further improved with the use of the 11° bit. Excellent input and output match are achieved due to the cascode design. The input P_{1dB} is -13 dBm at 9.5 GHz (IIP₃ of -5 dBm). The 4-element chip consumes 144 mW, including the biasing circuits, and is $2.5 \times 2.9\ \text{mm}^2$ (Fig. 2.8(a)). A single channel was also built with a power consumption of 36 mW and is $2.5 \times 0.75\ \text{mm}^2$ (Fig. 2.8(b)).

The on-chip coupling between the phased array channels can be modeled using

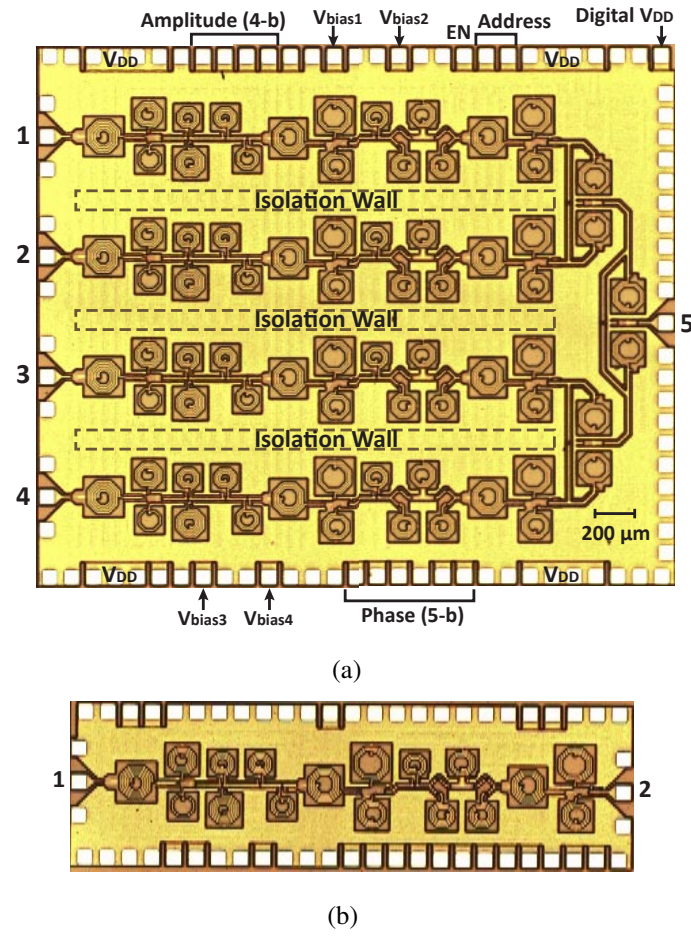


Figure 2.8: Chip microphotographs of the (a) 4-element and (b) single-element phased-array receivers.

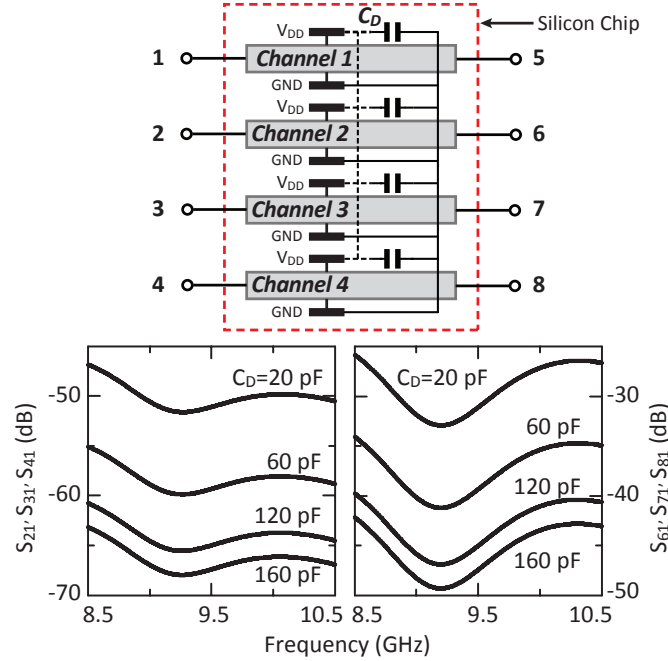


Figure 2.9: Simulation setup and coupling for different on-chip decoupling capacitors.

the simplified circuit shown in Fig. 2.9. There are two important coupling mechanisms: the forward coupling S_{61} , S_{71} and S_{81} results in amplitude and phase error in the path of channel 1 due to phase settings in channels 2, 3, 4 [34], [46], and the backward coupling S_{21} , S_{31} , S_{41} , which has minimal effect if the antenna ports are well matched. However, if the backward coupling is high and the antennas are not well matched (-10 dB) or open-circuited (worst-case test condition), then the power coupled to port 2, for example, can reflect back to the chip, be amplified by channel 2, and add again to S_{51} causing additional amplitude and phase error. Fig. 2.9 shows that a V_{DD} to ground capacitance of 20-100 pF per channel is enough to ensure a very low on-chip coupling and virtually no additional *rms* amplitude and phase errors.

2.3 On-Chip Measurements

The NF is measured on a single channel with a gain of 12.2 dB and is 3.4 ± 0.1 dB at 9.5 GHz over the 16 phase states (< 3.5 dB average at 9.0-9.8 GHz) (Fig. 2.12). The expected NF of a channel in a 4-element array and including the 2.1 dB Wilkinson

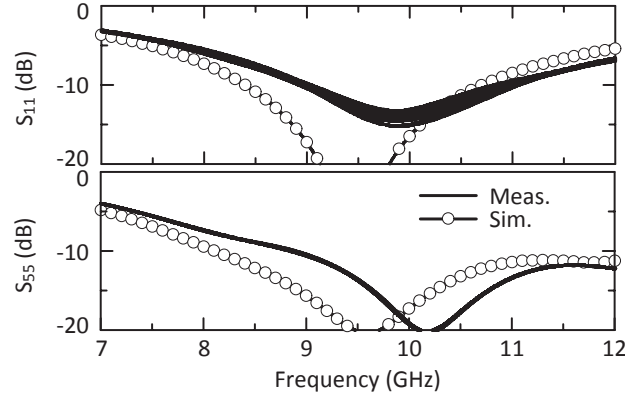


Figure 2.10: Measured and simulated return loss.

combiner loss is 3.47 dB at 9.5 GHz. The measured IP_{1dB} and IIP_3 are -12.5 dBm and -4.1 dBm at 9.5 GHz and agree well with simulations (Fig. 2.13). The measured output P_{1dB} and IP_3 in the 4-channel array are -3.5 and +6 dBm at 9.5 GHz and include the Wilkinson network loss.

The S-parameters can be further improved with the use of gain and phase control and result in an *rms* gain error of <0.5 dB at 8.8-11 GHz (minimum of 0.22 dB at 9.5 GHz) and an *rms* phase error of $<6^\circ$ at 9.2-10.1 GHz (Fig. 2.14). This is achieved at the expense of an average gain reduction to 9.9 dB (4-channel array) and an average NF increase to 3.75 dB (single channel) at 9.5 GHz (< 3.85 dB from 8.8-9.8 GHz).

The measured on-chip coupling between the different channels is first done using S-parameters and is < -35 dB at 9-10 GHz, which is limited mostly by CPW probe-to-probe coupling (Fig. 2.15). In this measurement, two CPW probes are placed on the input ports of the 4-element chip and the S-parameters are measured with the other ports left open-circuited.

The S-parameters of channel 1 are then measured when the phase of channels 2, 3, and 4 are changed from $0-337^\circ$. In this case, the input ports of channels 2, 3, and 4 are left open-circuited, which results in a worse-case condition for testing [46]. The measurements show $< \pm 0.15$ dB and $< \pm 1^\circ$ change in the gain and phase of channel 1 for all phase settings of channel 2, 3 and 4 (not shown for brevity), and result in negligible error. The measurements indicate that for all practical purposes, this is an excellent high-linearity, low-noise figure on-chip phased array. However, the chip performance

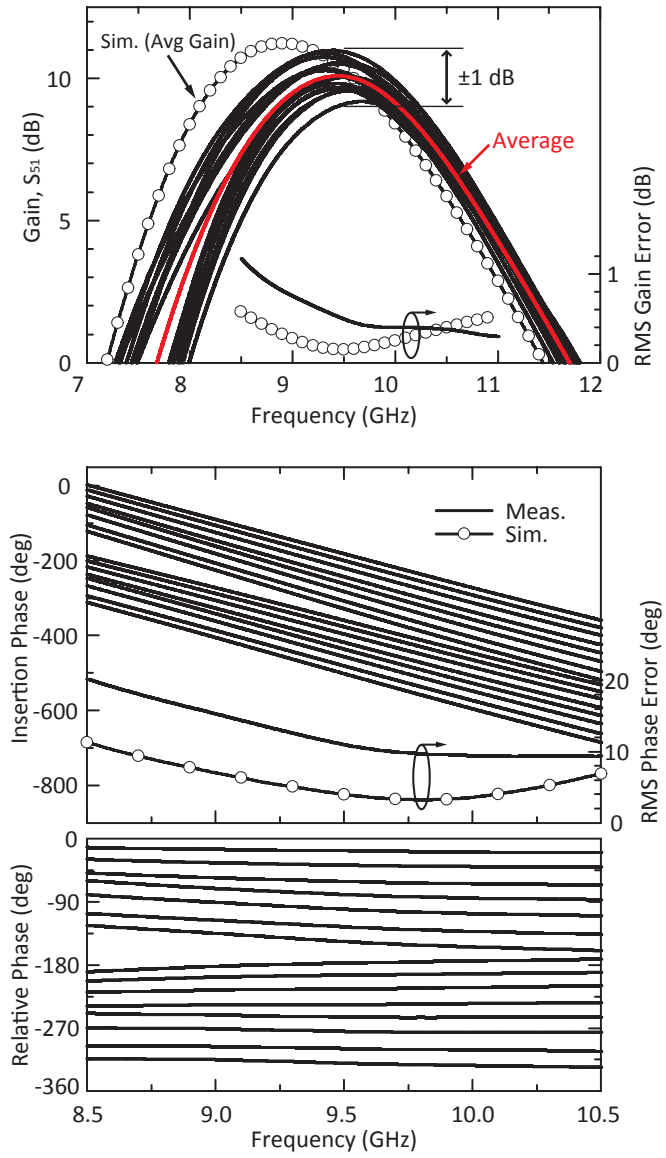


Figure 2.11: Measured and simulated gain, insertion phase and relative phase difference without using the VGA or 11° bit.

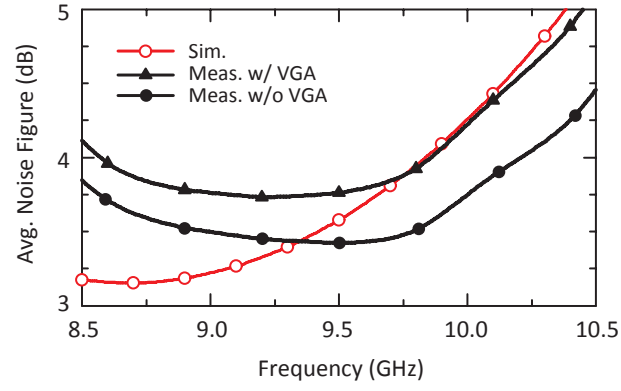


Figure 2.12: Measured and simulated average noise figure over 16 phase states.

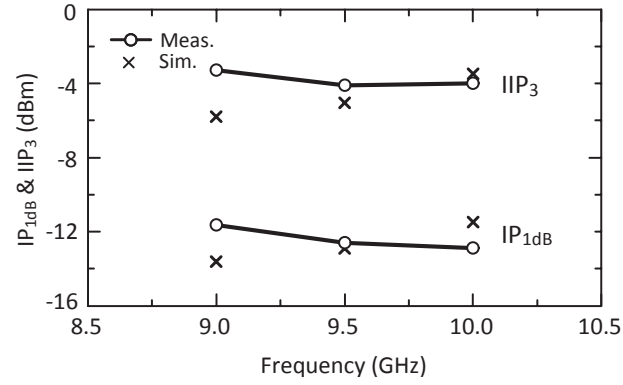


Figure 2.13: Measured and simulated IP_{1dB} and IIP_3 . The P_{1dB} and IP_3 are within ± 0.25 dB for all 16 phase states.

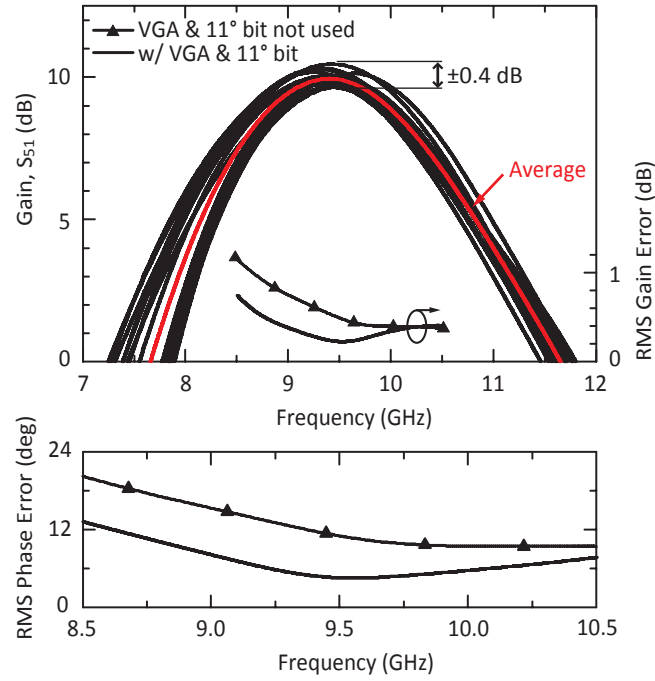


Figure 2.14: Measured and simulated gain and associated *rms* gain and phase error with the VGA and the 11° bit.

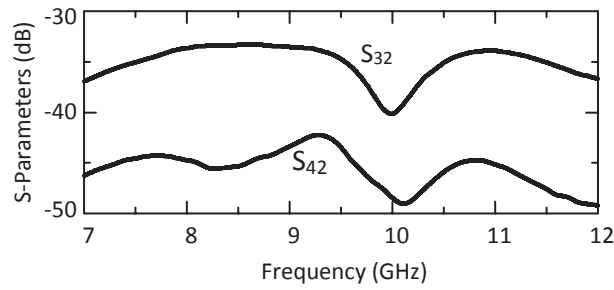


Figure 2.15: Measured on-chip coupling between different input ports (see Fig. A.4 for port definition).

degrades with chip-on-board packaging, and this is investigated in the following section.

2.4 Chip-On-Board Packaging: Simulations and Measurements

The phased-array chip is placed on an RF board with a grounded pedestal and bonded as shown in Fig. 2.16. The substrate is Rogers RT5880 with $\epsilon_r=2.2$, $t=10$ mils and a loss of ~ 0.1 dB/cm at 8.5-10.5 GHz for a $50\ \Omega$ microstrip line (0.8 mm width). In this case, due to the presence of on-chip RF currents on the V_{DD} and ground planes, a large number of short RF-ground bondwires (“down-bonds”) are used in order to ensure a low ground inductance between the chip and the system-level ground plane. Also, 4 different V_{DD} pins are used, each with its own 100 pF off-chip de-coupling capacitors that are placed very close to the chip in order to also ensure V_{DD} grounding. A closer look reveals two inductances between the chip and the system-level ground: L_{GND1} between the chip and the grounded pedestal (plane A), and L_{GND2} between the grounded pedestal and the main system-level ground (where the antenna and sum ports are referenced). EM simulations done using HFSS [18] and Sonnet indicate that L_{GND2} is 25-40 pH depending on the substrate thickness and number and spacing of the via holes. L_{GND1} , on the other hand, is hard to model exactly and is best done using a full HFSS model including the 4 input RF lines (see below). Still, a good assumption is 50-150 pH for a large number of down-bonds.

Fig. 2.17 presents the coupling simulations using the simplified inductance model for $L_{GND1}=50\text{-}150$ pH and $L_{GND2}=40$ pH. The simulations show a forward coupling ($S_{6/1}$) of -15 dB, which is an increase over the on-chip results with $C_D=110$ pF. Knowing that $S_{5/1}$ is +13 dB at 9-9.5 GHz, the overall coupling between the channels is therefore -28 dB. This results in an amplitude and phase error of ± 0.25 dB and $\pm 2^\circ$, respectively, in channel 1 when the phase of channel 2 is changed from 0 to -337° (Fig. 2.17). This model concentrates all the inductance in one node (and is not distributed along the chip and different RF ports) and could be considered as the worst-case condition for coupling estimation, but is important to have as a benchmark.

The coupling between the input bondwires and transmission-lines was not taken

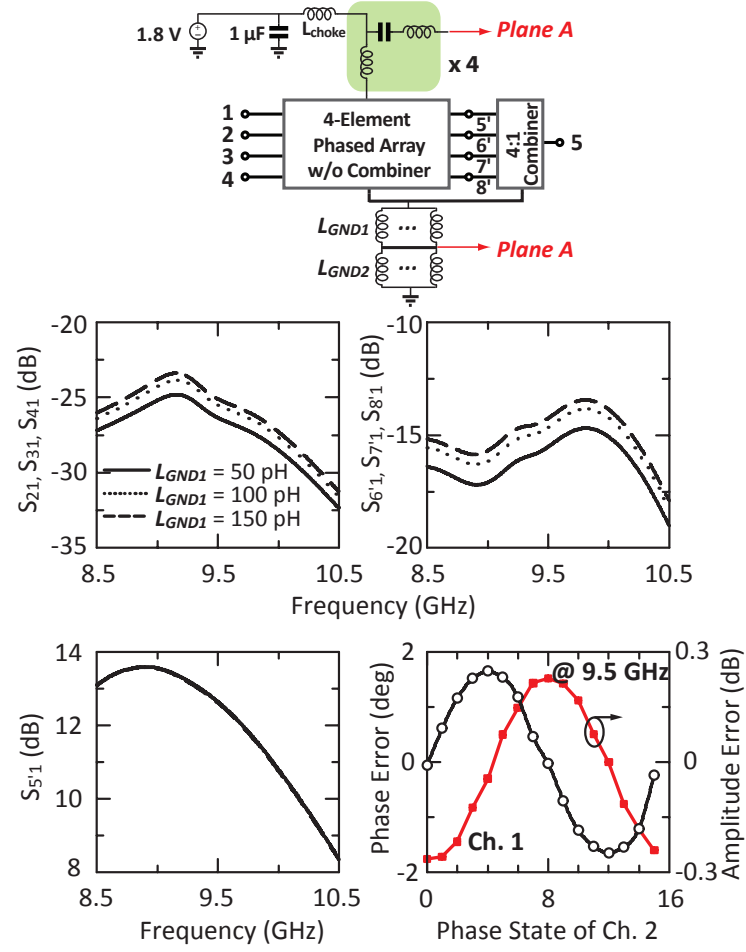


Figure 2.17: Simulation setup and resulting S-parameters vs. L_{GND1} ($L_{GND2} = 40$ pH). The amplitude and phase change in channel 1 vs. the phase state of channel 2 is also shown.

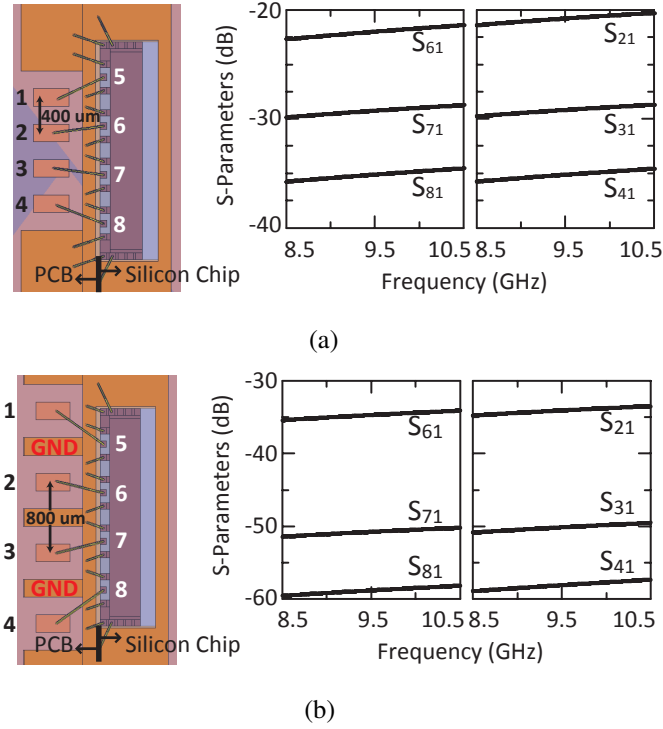


Figure 2.18: Bondwire and printed-circuit-board simulation using HFSS for (a) 400 μm and (b) 800 μm -pitch feedlines with a grounded stub between the bondwires.

into account in the above simulations, and this can be simulated using HFSS for the input and output ports (Fig. 2.18). In this case, the simulation is referenced to the global system ground (antenna ports) and the inductance from plane A to the system ground is automatically taken into account. Fig. 2.18 presents the results for two different designs, a pitch of 400 μm (200 line, 200 μm gap), and a pitch of 800 μm (200 μm line, 200 μm gap, 200 μm grounded stub, 200 μm gap). It is seen that the coupling between the channels due to the bondwires alone is $S_{61} = -21$ dB at 9-10 GHz for a 400 μm pitch, but it can be reduced to -35 dB with the use of a grounded stub between the different input ports. In both cases, the non-adjacent coupling due to the input bondwires is < -30 dB.

The input and output ports also need to be matched since the RF-port bond-wire inductance is ~ 0.8 nH (Fig. 2.19). A simple matching network can be achieved using a high-impedance line ($Z_0 = 94 \Omega$, $l = 130^\circ$ at 9.5 GHz) and results in $S_{11} < -10$ dB at 8.7-10.0 GHz at the antenna ports. It is also important to model the coupling between the

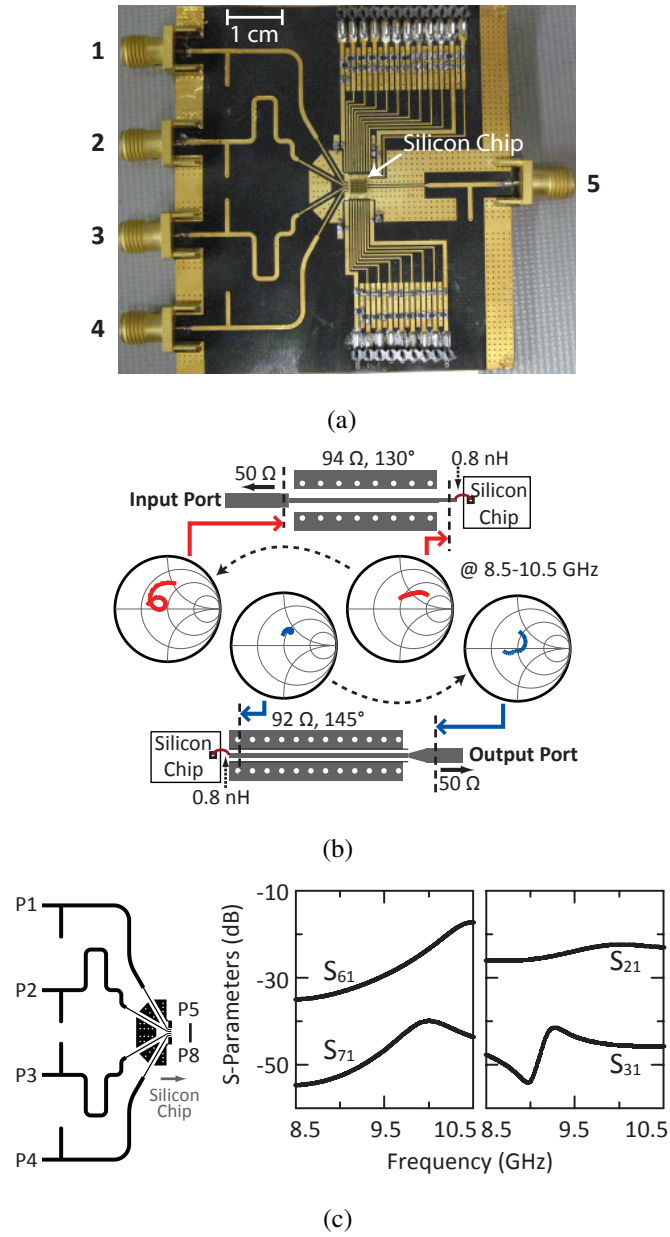


Figure 2.19: (a) Photograph of packaged phased-array chip, (b) input and output matching networks, and (c) simulated S-parameters of the printed-circuit-board distribution network ($S_{51} \cong -0.6$ dB and $S_{11} < -10$ dB at 8.5-10.5 dB).

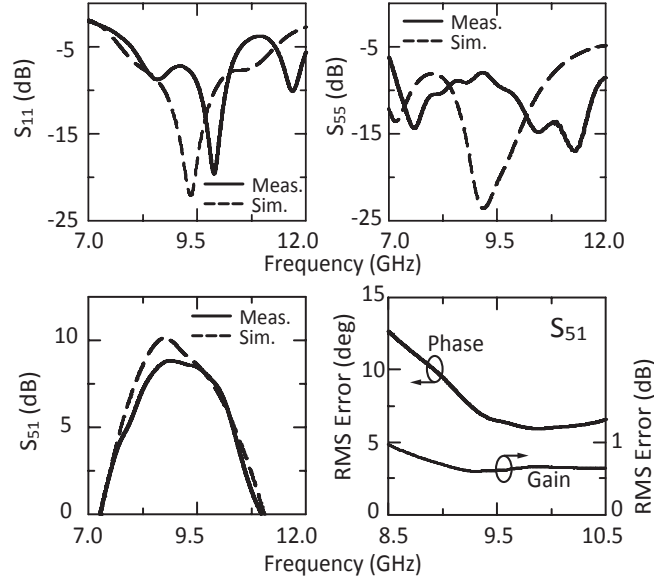


Figure 2.20: Measured and simulated S-parameters for the chip-on-board phased-array. The S_{11} , S_{55} and S_{51} are average values over all phase states.

transmission-lines on the Teflon substrate since they are quite close to each other around the chip. This is easily done using ADS Momentum [47], and the estimated coupling (S_{61}) is < -30 dB at 9-10 GHz between adjacent channels. The packaged chip can then be simulated using the model of Fig. 2.16(b), which includes all the known coupling effects.

The phased array chip was assembled with the 4 feedlines placed at a pitch of 400 μm (200 line, 200 μm gap) in order to study the effect of the bond-wire coupling (Fig. 2.19). The measured average channel gain agrees well with simulation and is 8.5 dB at 9.5 GHz and include board and connector losses (Fig. 2.20). The measured *rms* gain and phase error are similar to the on-chip results. The measured S_{11} and S_{55} are mostly due to connector imperfections (the SMA connectors were measured separately and result in -10 dB reflection at 10 GHz).

The coupling measurements are done by changing the phase of channels 2 and 4 while measuring the performance of channel 1 (S_{51}) at a fixed phase state (Fig. 2.21). The coupling between the channels, $C=B/A$, is fitted using the vector method of Fig. 2.21(a) and is -19 dB between channels 1 and 2, and -31 dB between channels 1 and 4. The error in S_{51} is determined by the RF bondwire coupling for the near-channel

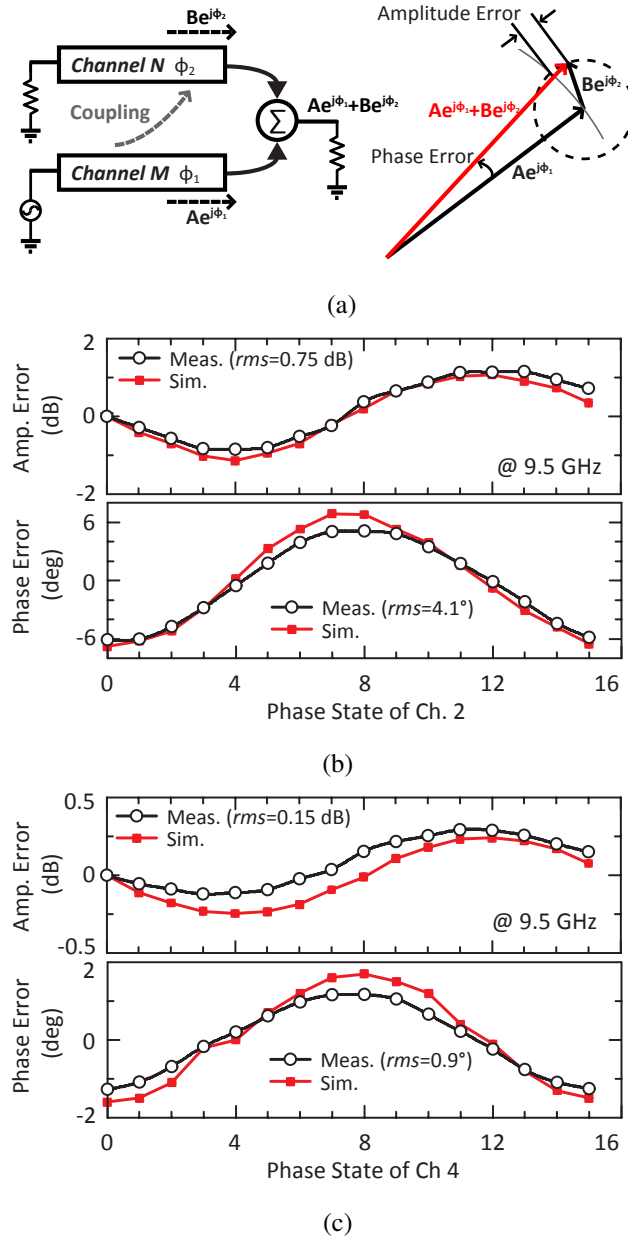


Figure 2.21: (a) Vectorial representation of the channel-to-channel coupling, and measured and simulated amplitude and phase error of channel 1 when the phase state of (b) channel 2 and (c) channel 4 is changed in the chip-on-board phased array.

(channel 2) and by the chip-to-ground inductance ($L_{GND1}=50$ pH and $L_{GND2}=40$ pH) for the far-channel (channel 4). If a pitch of $800\text{ }\mu\text{m}$ ($200\text{ }\mu\text{m}$ line, $200\text{ }\mu\text{m}$ gap, $200\text{ }\mu\text{m}$ grounded stub, $200\text{ }\mu\text{m}$ gap) was used for the feedlines, then the coupling for all channels would be as that of channel 4 since the bondwire coupling would be negligible. The results of Fig. 2.21(c) agree with the simulations of Fig. 2.17.

Table 1 presents a comparison of this work with other chips in the X/Ku-band range. It is evident that [42] shows lower power consumption and better NF than this work, but has 3 dB worse linearity. The design in [48] consumes a lot of power but is a very wideband design (6-18 GHz) and is based on a vector modulator approach. The lowest power consumption is demonstrated in [36] using a high-performance SiGe technology, a 2-bit phase shifter and a reduced NF requirement.

Table 2.1: Performance Comparison of Silicon Phased Array Receivers

	This Work	[35]	[36]	[37]	[38]	[42]	[48]
Technology	0.13 μm CMOS	0.12 μm BiCMOS	0.12 μm BiCMOS	0.18 μm CMOS	0.5 μm SiGe	0.13 μm CMOS	0.18 μm BiCMOS
Frequency (GHz)	9.5	9.3	9.4	12.1	11.5	9.5	12
3-dB Bandwidth (GHz)	2	1.8	2	—	2	1.8	7.7
Phase Bits	4-5	5	3	4	4	4	5
No. of Channels	4	1	2	1	1	4	1
Gain (dB)	10.1	11.0	10.5	3.5	3.7	11.5	20
RMS Gain Error (dB)	0.2	0.2	0.2	0.3	0.2	0.5	0.7
RMS Phase Error (deg)	4.5	7	—	2.6	—	8	4
Noise Figure (dB)	3.4	4.1	5.0	—	4.4	3.2	4.1
$\text{IP}_{1\text{dB}}$ (dBm)	-12.5	—	—	—	-27	-16.5	-18.5
IIP_3 (dBm)	-4	-13	-1.5	—	-17	-6.5	—
Power Consumption (mW) Total / per channel	144 / 36	33 / 33	8 / 4	26 / 26	53 / 53	76 / 19	62 / 62
Chip Area (mm^2)	2.5×2.9	3.8×3.5	3.0×2.0	1.9×0.9	1.9×0.8	2.4×3.0	1.2×0.75

2.5 Conclusion

A high-linearity, 4-element X-band phased array was demonstrated using 0.13 μm CMOS technology. A single-ended design was used and results in very low on-chip coupling. The phased-array chip was then mounted on a Teflon substrate using bond-wires. Simulations and measurements show that with high isolation bond-wire design, the channel-to-channel coupling ($\sim$ -31 dB at 9.5 GHz) is determined by the overall ground inductance, and results in $\sim$ 0.15 dB and 0.9° of additional *rms* amplitude and phase error. This work shows that one can use chip-on-board packaging for X-band silicon phased arrays with a large number of input channels.

2.6 Acknowledgment

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- Donghyup Shin and G. M. Rebeiz, "Low-Power Low-Noise 0.13- μm CMOS X-Band Phased Array Receivers," in *IEEE MTT-S Int. Microw. Symp.*, Anaheim, CA, May 2010.

Chapter 3

Packaged X-band Phased-Array Transmitter in 0.13- μm CMOS

3.1 Introduction

Silicon phased-array RFICs, based on SiGe and CMOS technologies, have been well demonstrated at X/*Ku*-band using the *All-RF* beamforming approach, both in the receive, transmit and transmit/receive modes [5, 7, 34–38, 49–51]. As is well known, SiGe and CMOS offer multiple RF front-ends on a single chip, together with all the necessary digital control electronics, which results in a space savings per unit cell as compared to a GaAs solution [52]. This allows for the construction of compact X/*Ku*-band phased-arrays using standard printed-circuit board techniques at a great reduction in cost and increase in reliability, either using chip-on-board or QFN packaging techniques [5, 49, 53–55].

This paper presents an X-band 4-element phased-array chip built using 0.13- μm CMOS technology and with moderately high power levels from each channel (~ 13 dBm). The chip is intended for dual operation: A radar mode at 9-9.5 GHz for FMCW perimeter detection and a communication mode at 8.2-8.7 GHz for BPSK and QPSK satellite systems. The chip is therefore characterized at saturated power levels for the radar mode, and also, at P_{1dB} and associated backoff power levels in a communications mode where attention is placed to distortion versus power levels. The 4-element chip

has been packaged using chip-on-board and using QFN solutions. The mutual coupling between the bond-wires are taken into account together with the passive baluns on the CMOS IC, and the resulting channel-to-channel coupling simulation is done using Ansoft-HFSS [18]. A comparison is presented between the two solutions in terms of isolation between the channels and ground inductance effects. To our knowledge, this is the first demonstration of a packaged phased-array transmitter chip for radar and communication systems.

3.2 Design

3.2.1 Block Diagram and Technology

Fig. 5.4 presents the block diagram of the 4-element transmit phased-array chip. The circuit design is differential, but baluns are used at the input and output ports since single-ended ports are compatible with microstrip or CPW circuits on the printed-circuit board. Two independent power supplies are used on the chip: The input power divider and buffer amplifier are driven using a 2 V supply, while the active phase shifter and output power amplifier are driven using a 3 V supply. Also, two different 3 V power supply lines are used, each driving a 2-element subarray so as to reduce the coupling between the elements and also to reduce the current draw from the supply pins.

The chip is built in a low-cost 0.13- μm CMOS technology with an f_T of 100 GHz and $\text{NF}_{\min}$ of 0.8 dB at a bias current density of 0.1 mA/ μm (IBM8RF) and with 8 metal layers (Fig. 3.2). Differential transmission-lines are implemented in a grounded coplanar waveguide (G-CPW) configuration with dimensions of 10/8/8/8/10 μm and a simulated loss of 0.22 dB/mm at 9 GHz. Note that the IBM8RF process allows for 11 μm of oxide between the MA and the LY layer, which results in relatively wide and low-loss differential lines.

All inductors and transmission-line connections are simulated using 2.5-D electromagnetic solver (Sonnet [45]) and have Q of 12-15 at 9-10 GHz depending on the design. The capacitors are implemented using the library metal-insulator-metal (MIM) capacitors.

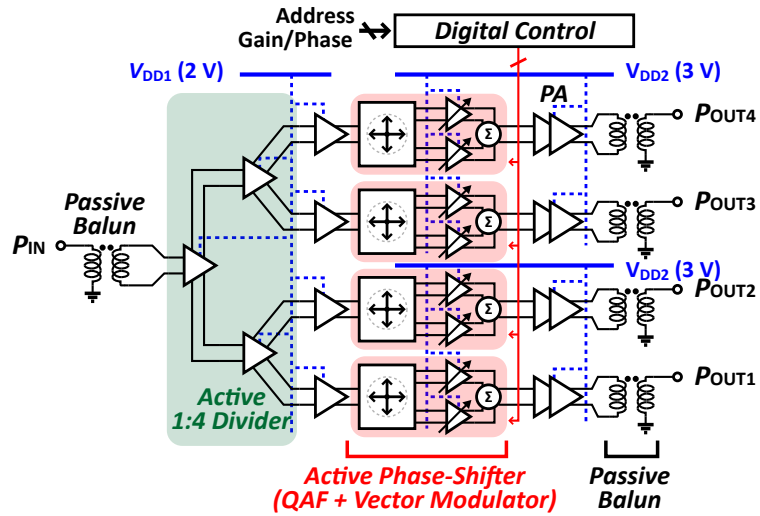


Figure 3.1: Block diagram of 4-element phased-array transmitter.

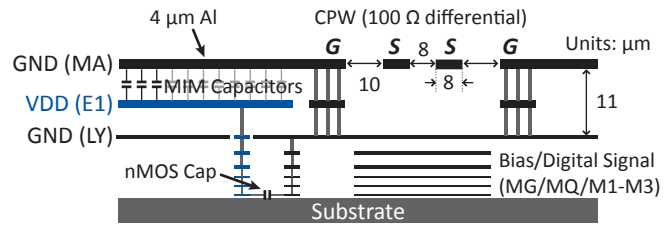


Figure 3.2: Metal stack-up of IBM8RF 0.13- μm CMOS process.

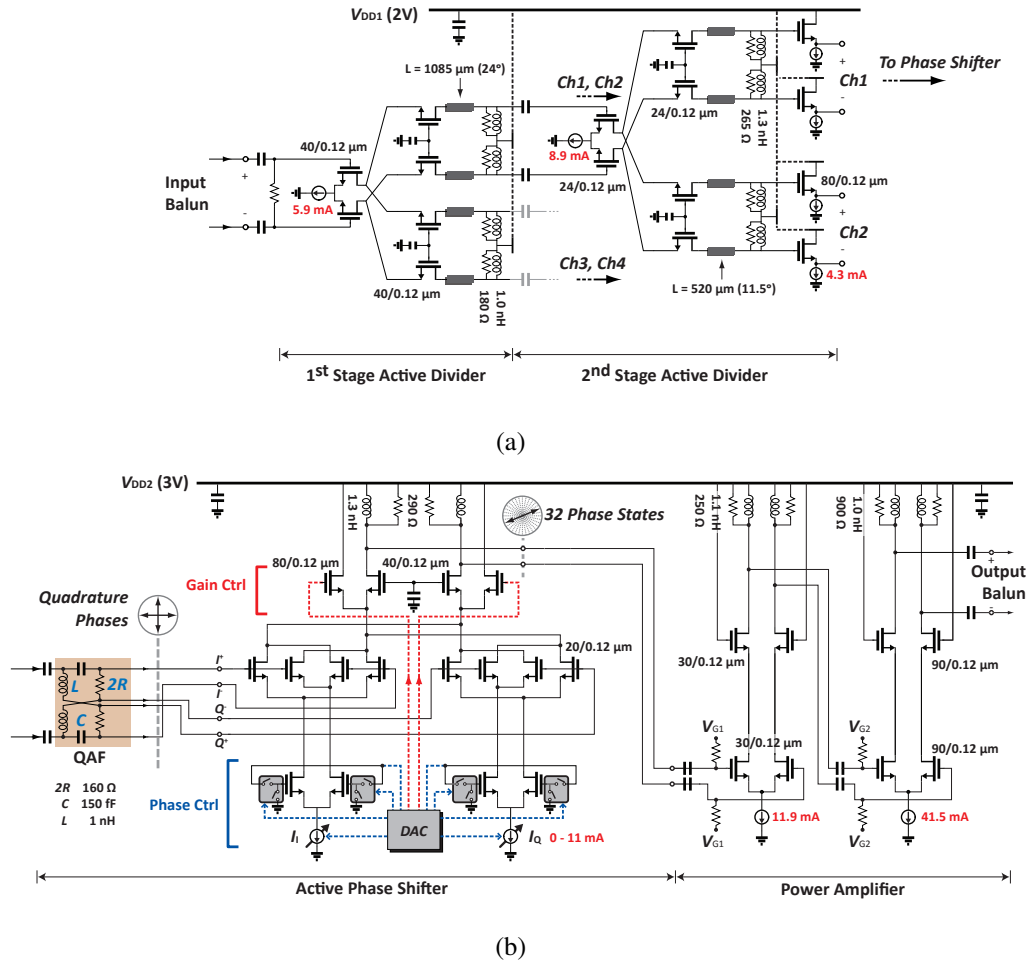


Figure 3.3: Circuit schematic of a single channel: (a) active 1:4 divider and (b) phase shifter and power amplifier.

Table 3.1: Vector Modulator I/Q DC Current Level

	I_I (mA)	I_Q (mA)
0 °	10.7	0
22.5 °	9.8	1.0
45 °	5.5	5.5
67.5 °	1.0	9.8
90 °	0	10.7

3.2.2 Active 1:4 Divider

An active 1:4 divider is used after the input balun and is based on a 2-stage cascode divider with LR loads for wideband operation (Fig. 3.3(a)). The input stage should be capable of handling ~ 0 dBm of input power (-1.7 dBm after the balun), and is biased at 5.9 mA. The second stage feeds a source follower amplifier with an output impedance of 54Ω so as to drive the low-impedance quadrature all-pass filter network (QAF [39]). The active 1:4 divider consumes 25 mA and has an electronic gain of 1.5 dB at 9 GHz, where the gain is defined as the power in the 54Ω load (differential) at the output of a source follower divided by the available power at the single-ended port from a 50Ω source. The simulated output power and phase vs. input power is shown in Fig. 3.4 with an input P_{1dB} of -5 dBm, limited mostly by the first-stage active divider. Still, the 1:4 divider can deliver -2 dBm at the QAF (350 mV_{peak}) for an input power of 0 dBm, and with low phase distortion ($\sim 2^\circ$).

3.2.3 Active Phase Shifter

The QAF is designed for a $Z_o = \sqrt{L/C} = 80 \Omega$ (differential) with $L = 1.0 \text{ nH}$, $C = 150 \text{ fF}$ and $R = 80 \Omega$ and provides a very wideband quadrature with $< \pm 3^\circ$ phase variation at 6-10.5 GHz including the effect of the capacitance loading of the vector modulator stage ($C_{Load} = 30 \text{ fF}$). The simulated QAF voltage gain is 1.5 dB including

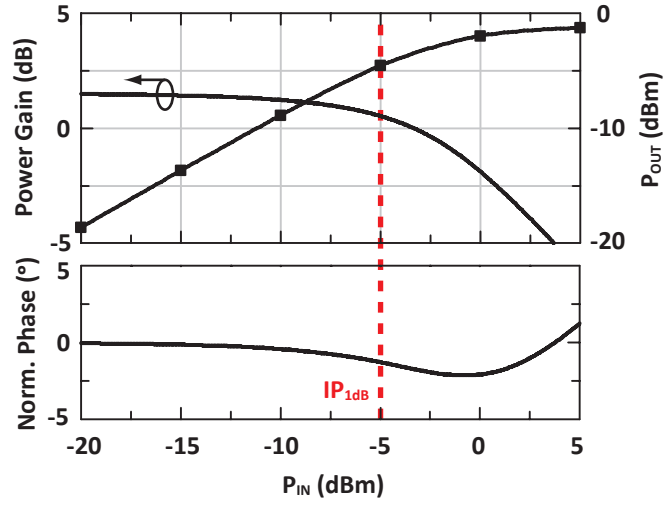


Figure 3.4: Simulated power gain and output power, and normalized phase vs. input power of active divider at 9.0 GHz.

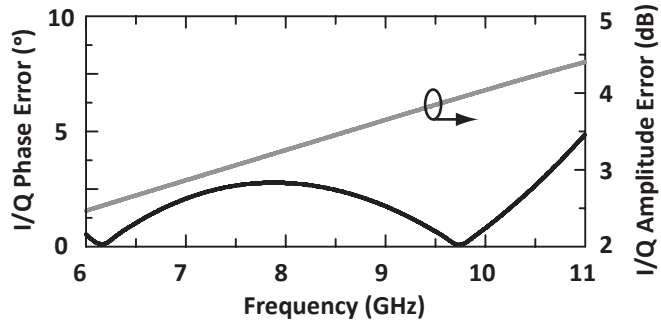


Figure 3.5: Simulated I/Q phase and amplitude error of the all-pass network.

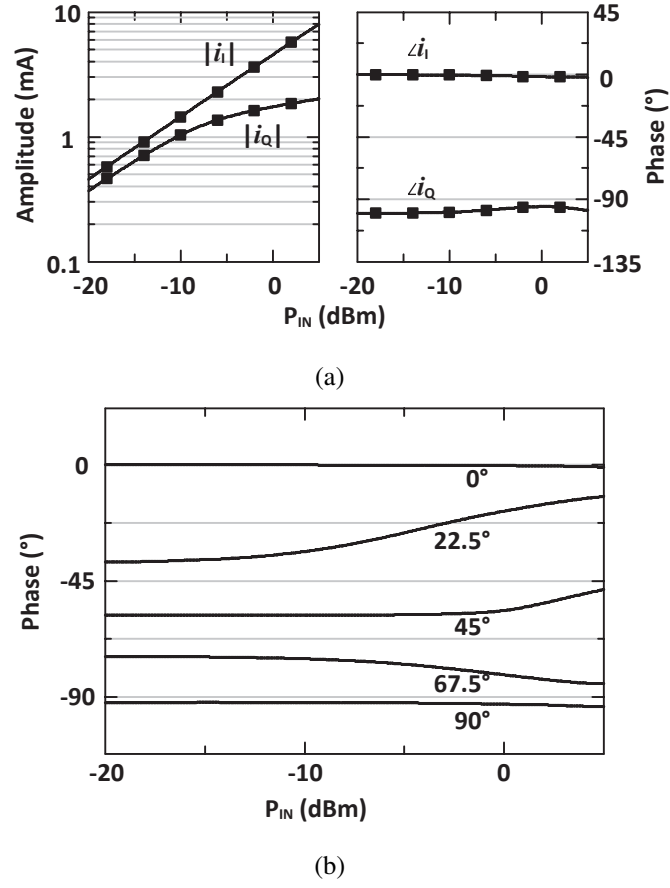


Figure 3.6: Simulated (a) i_I and i_Q at 22.5° phase state, and (b) phase vs. input power defined at the QAF input port.

the capacitive load, and with < 3.6 dB error between the I and Q outputs at 9 GHz (Fig. 3.5). A lower amplitude error can be designed using a QAF with $Z_O = 40 \Omega$ but at the expense of lower gain (or higher current) in the active divider.

The QAF feeds a vector modulator phase shifter with integrated gain control and wideband RL loads (Fig. 3.3(b)). The switches at the bottom select between the I+ and I- quadrants (and Q+ and Q- quadrants), and the gain of the I and Q paths is controlled using a 5-bit DAC. The requirements are a 4-bit phase shifter, but an additional bit is used as a trim bit to improve the *rms* phase error (if needed). The DAC currents are optimized to take into account the interconnect parasitic effects (modeled using Sonnet), and are listed in Table 4.1 for 0, 22.5, 45, 67.5 and 90°. In addition, a 5 dB gain control stage is placed on top of the phase shifter using a current steering mode. This gain stage also uses a 3-bit control voltage from the DAC and is employed to reduce the *rms* gain error in the phase shifter. Note that this gain control method is useful for a 0-5 dB range due to current starving effect in the main RF path transistor.

The phase shifter consumes 11.5 mA of current from a 3 V supply and has a simulated voltage gain of 5.6 dB, an input P_{1dB} of 6.7 dBm and a noise figure of 12 dB (gain values can change by ± 1.5 dB vs. phase state). However, since this chip will be operated under high drive powers, it is important to study the gain and phase distortion vs. input power. The gain follows the usual compression curve, but the phase starts to distort at an input power of > -10 dBm for 22.5°, 45°, and 67.5° phase states (Fig. 3.6(b)). This is because compression begins for different input power levels for the I- and Q-path transconductance stages. For the 22.5° phase state, the linearity of Q-path transconductance stage is much smaller than I-path due to the lower DC bias current ($I_I = 9.8$ mA, $I_Q = 1$ mA). As a result, the amplitude mismatch between the I/Q ac currents combined at the load (i_I and i_Q) increases at higher input power even though the power is less than IP_{1dB} (Fig. 3.6(a)), and hence an output phase error occurs.

Still, for radar operation operating at P_{SAT} , the input power of the active phase shifter is -2 dBm from the 1:4 active divider and the resulting phase distortion at different phase states are $< 15^\circ$, which can be calibrated out using the additional trim bit in the DAC (see Section 3.3.2).

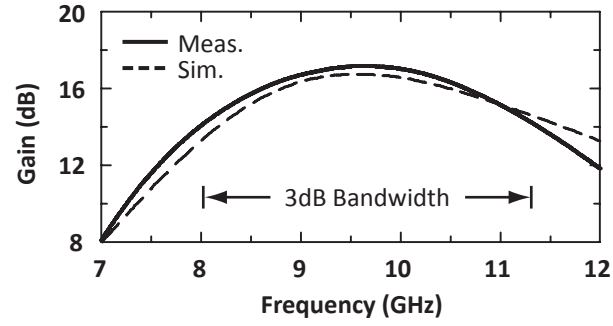
3.2.4 Power Amplifier

The power amplifier (PA) is a two-stage cascode design with a total bias current of 53.4 mA from a 3 V supply. The bias conditions of the first and second stages are optimized as class A and class AB, respectively. Since this is a relatively high-power amplifier with $P_{SAT}=15$ dBm, the selection of the transistors and their layout is essential for proper operation. In this design, transistors with $W/L = 30/0.12$ μm and $90/0.12$ μm for the first and second stage, and the interconnects are modeled using Sonnet. The inductors are designed with 9 μm wide line for improved Q (~ 14 at 9.5 GHz) and the layout is entirely symmetrical with top and bottom inductors. Also, the edge-to-edge separation between the first and second stage inductors is >100 μm which ensures a coupling of <-30 dB. The simulated small-signal gain is 17 dB at 9.5 GHz with differential output impedance of 100 Ω .

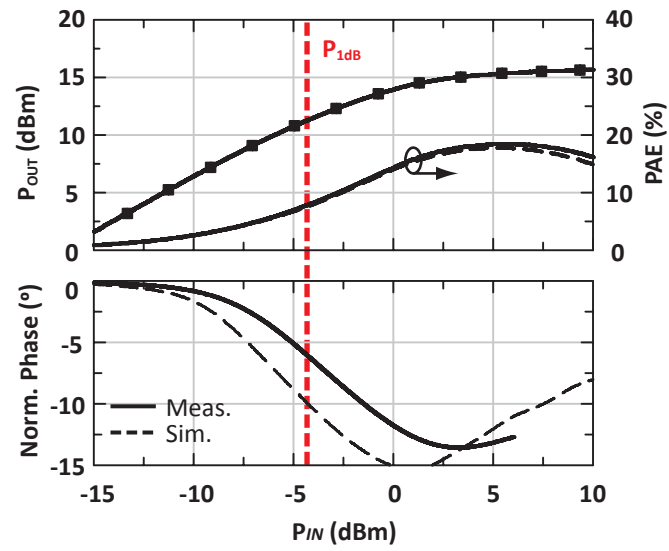
The measurements on the PA are presented here for completeness and since they do not fit in the phased-array measurement section. The power amplifier was tested on an individual breakout chip with the input and output balun losses deimbedded. Measurements indicate a gain of ~ 17 dB with a 3-dB bandwidth of 8.1-11.3 GHz (Fig. 3.7(a)). The measured OP_{1dB} and P_{SAT} are 11 dBm and 15.5 dBm, respectively, at 9.5 GHz and with a peak PAE of 19% (Figs. 3.7(b) and 3.8). Note that there is an AM to PM distortion of -5° and -12° at the P_{1dB} and P_{SAT} powers, respectively, and again, this can be calibrated out for radar application (see Section 3.3.2). Finally, the measured output 2^{nd} and 3^{rd} harmonic levels are at -32 dBc and -60 dBc for P_{SAT} power levels (note that this include the output balun filtering effect) (Fig. 3.9). All measurements are in good agreement with simulations for the PA breakout, and compete well with X-band results [56].

3.2.5 Input and Output Baluns

The input and output baluns are built using vertical magnetic coupling between the top two metal layers (MA and E1) (Fig. 3.10). The balun also act as ESD circuits since they provide a wideband short-circuit to ground at low frequencies. An additional LC matching network (C_1 and L_3 for input balun, and C_3 and L_3 for output balun) is



(a)



(b)

Figure 3.7: Measured and simulated power amplifier (a) gain, and (b) output power, PAE, and phase distortion vs. input power.

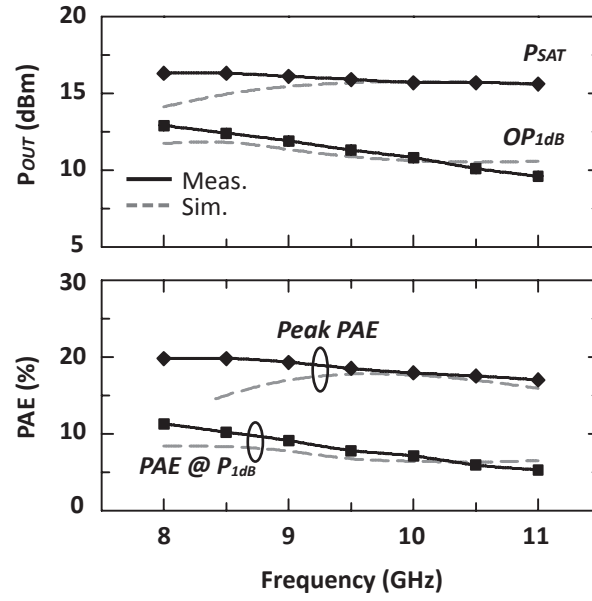


Figure 3.8: Measured and simulated power amplifier output power P_{SAT} , P_{1dB} , and PAE vs. frequency.

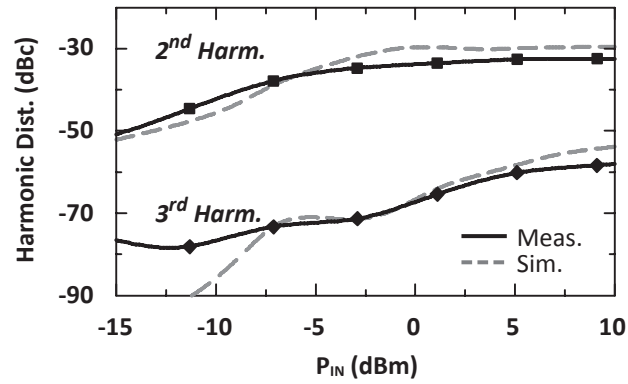


Figure 3.9: Measured and simulated power amplifier second and third harmonic components vs. input power at 9.0 GHz.

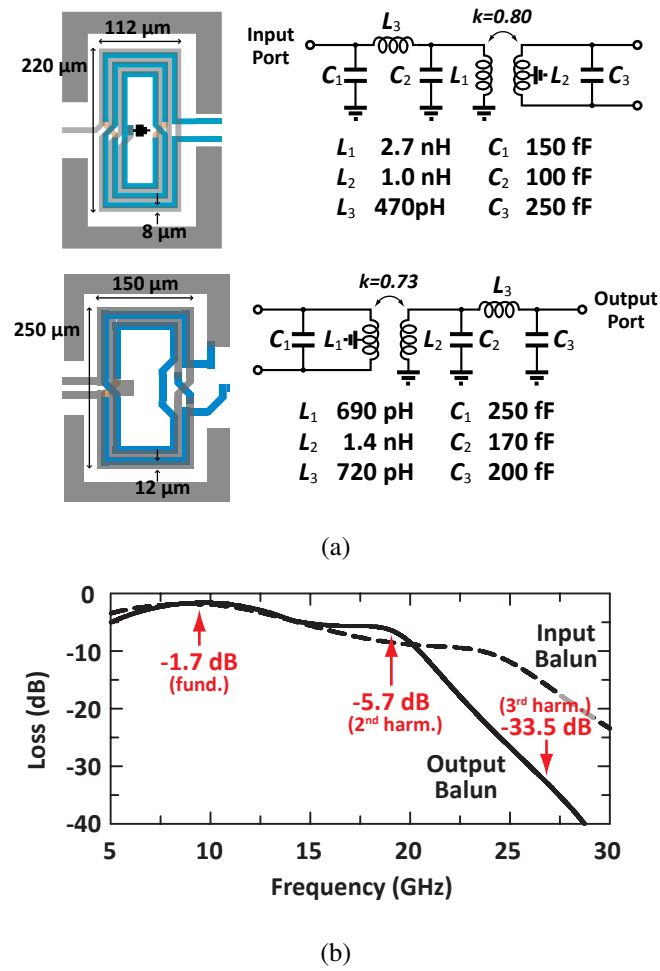


Figure 3.10: (a) Input and output baluns with wideband matching network and (b) simulated frequency response.

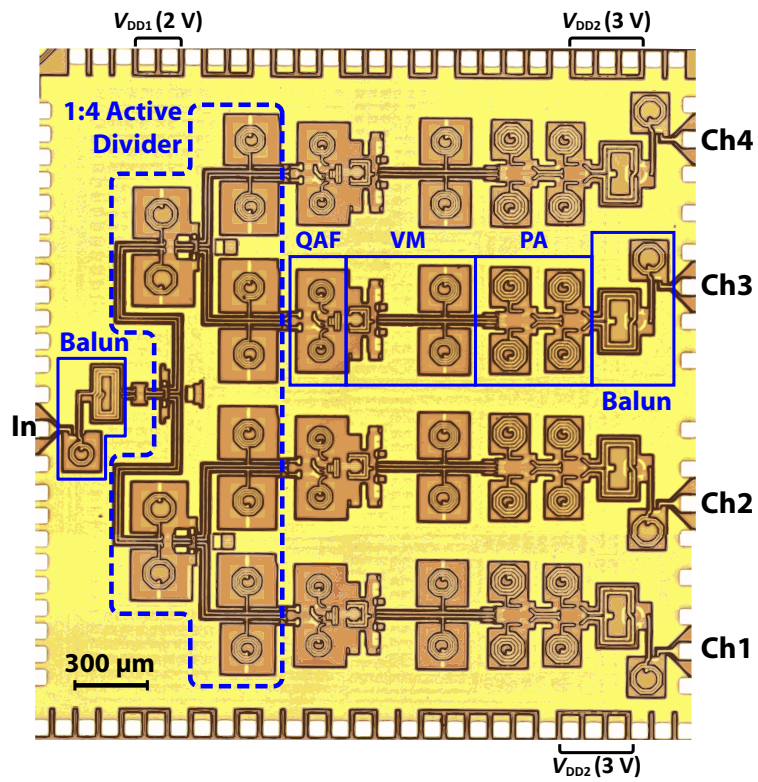


Figure 3.11: Microphotograph of X-band 4-element phased-array transmitter chip ($2.9 \times 3.0 \text{ mm}^2$).

used to provide very wideband input and output impedance matching so as to result in easy bondwire attachment and PCB matching circuits. The simulated losses of the input and output baluns are 1.7-1.8 dB at 7-11 GHz with a differential impedance of 100 Ω . Note that the output balun also provides substantial filtering at the 2nd (-5.7 dB) and 3rd (-33.5 dB) harmonic frequencies.

3.2.6 Bias and Control

The layout is done in a symmetrical fashion and every differential stage contains a top and bottom inductor for the RL loads (Fig. A.4). This design was preferred over differential inductors due to symmetry. The chip size is 2.9×3.0 mm² and consumes 79 mA (2 V) and 237 mA (3 V), for a total power consumption of 870 mW. The 3 V supplies pins are at the top and bottom of the chip to reduce the IR drop to the power amplifiers and for added isolation between channels 1 and 2, and 3 and 4. The V_{DD} plane covers most of the available chip area using E1 metal layer which is placed between MA and LY ground planes. High density MIM capacitors (2 fF/ μm^2) are used for supply decoupling and the total capacitance of ~200 pF is distributed over the chip area.

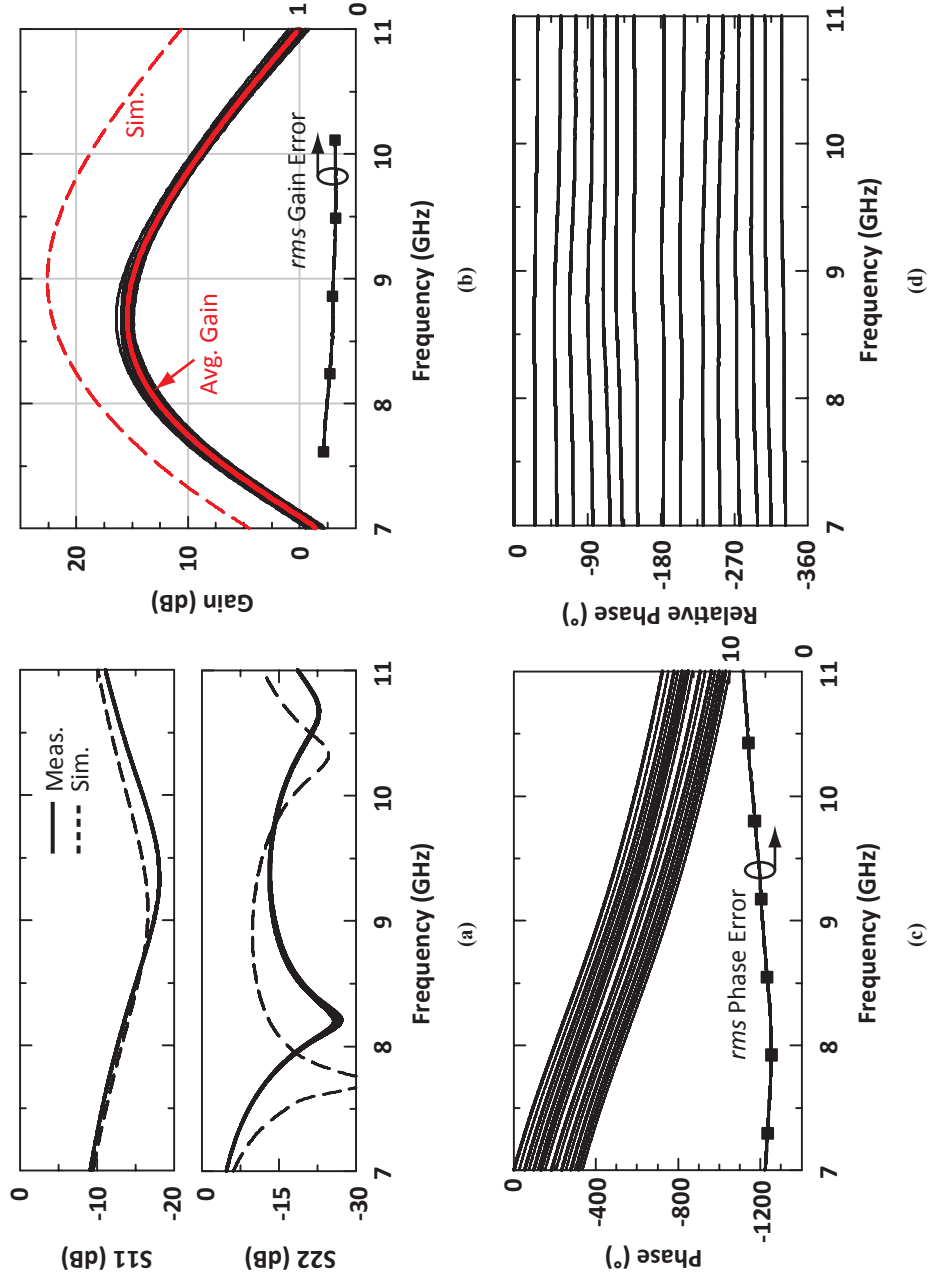


Figure 3.12: Measured and simulated small-signal (a) input and output reflection coefficient, (b) gain, (c) phase response and (d) differential phase response (normalized to 0°) for 16 phase states. VGA and trim-bit were used to reduce the *rms* gain and phase error.

The chip is controlled using a parallel interface. Each channel stores the phase and amplitude data on a 7-bit (4 for phase and 3 for amplitude) register, and a 2-to-4 address decoder allocates the address to each register by an enabling clock signal. The digital signal routing is done using M2 or M3 and are shielded by M1 and MQ ground planes to isolate the digital switching noise from the analog path.

3.3 Measurements

3.3.1 S-Parameter Measurements: Small Signal

All measurements are done on-chip with ground-signal-ground (GSG) probes and a short-open-load-thru (SOLT) calibration to the probe tips. The bias voltages are supplied using a DC bias probe on the north and south side of the chip. No oscillations have been recorded from DC-40 GHz, either at the RF probes or the DC probes. The chip was biased at 2 V, 79 mA, and at 3 V, 237 mA for all measurements below.

Fig. 3.12 presents the measured and simulated S-parameters under small signal conditions. The measured S_{11} and S_{22} is < -10 dB from 7.5-11 GHz. The measured gain peak shifted from 9.0 GHz to 8.7 GHz, and we believe that this is due to the transmission-line sections inside the 1:4 cascode divider stage (between the cascode stage and RL load). The 3-dB bandwidth is 7.9-9.6 GHz with a gain of 15.5 dB at 8.7 GHz which is suitable for both communication and radar applications. The four channels showed nearly identical response ($< \pm 0.5$ dB) and therefore only one channel is shown. The amplitude and phase trim bits were used in the vector modulator in order to get a very low *rms* gain and phase error, as shown in Fig. 3.12, and with no phase cross-overs. The measured gain and phase at 9.0 GHz on a polar circle is also shown (Fig. 3.13). Overall, except for the gain reduction, the measurements agreed well with simulations.

3.3.2 S-Parameter Measurements: Large Signal

The measured output power vs. input power are shown in Fig. 3.14(a) with a best P_{1dB} and P_{SAT} of 8.8 dBm and 13.6 dBm, respectively, at 9.0 GHz. This is expected

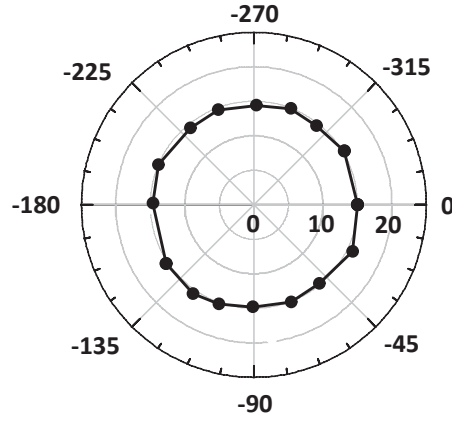
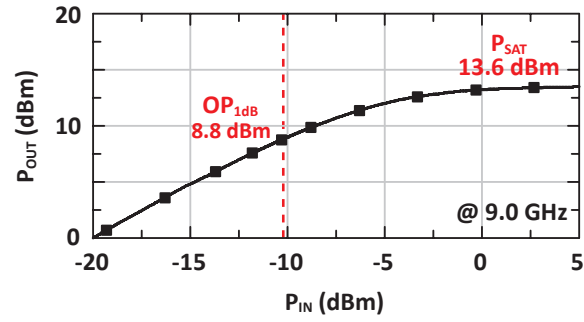
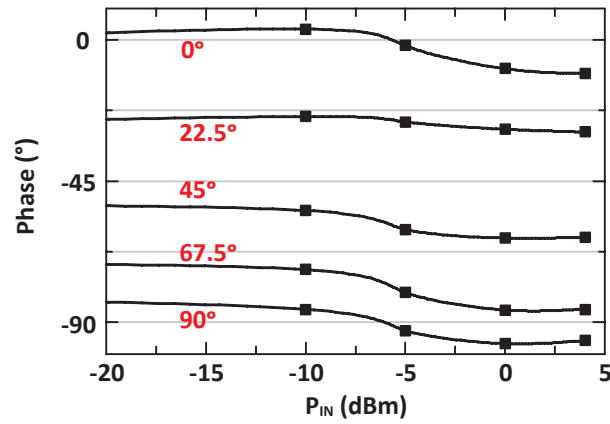


Figure 3.13: Polar diagram showing measured phase and gain at 9.0 GHz.



(a)



(b)

Figure 3.14: Measured (a) output P_{1dB} and P_{SAT} , and (b) phase vs. input power at 9.0 GHz. VGA set at maximum gain state.

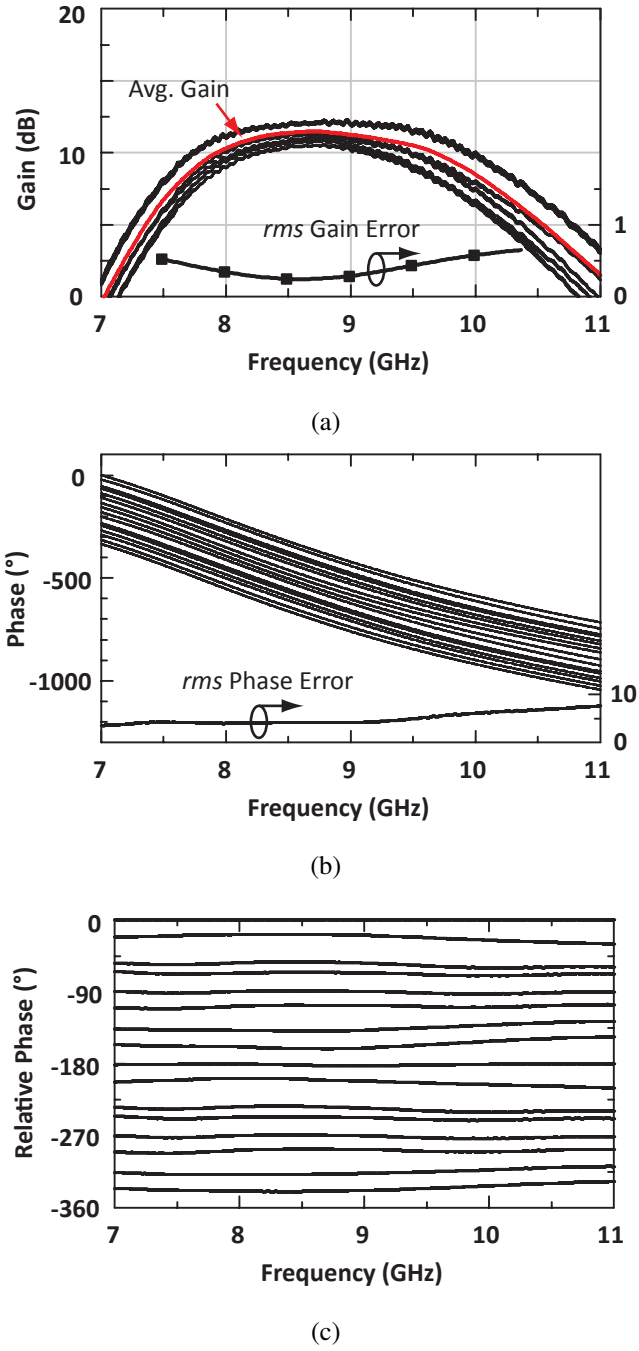


Figure 3.15: Measured large-signal (a) gain, (b) phase response and (c) differential phase response (normalized to 0°) for 16 phase states. VGA set at maximum gain state.

knowing that the output balun and GSG pad loss is ~ 2 dB and the power amplifier delivers a P_{SAT} of 15.5 dBm. These values are achieved at the phase state with the highest gain, and the average P_{1dB} and P_{SAT} over all phase states are ~ 0.7 - 0.8 dB lower. The measured phase distortion vs. power level is shown in Fig. 3.14(b). Note that this overall phase distortion takes into account the 1:4 active divider, phase shifter and the power amplifier AM to PM distortion components. This distortion can be calibrated out vs. input power and has virtually no effect on the radar operation.

The measured S-parameters of a single channel at $P_{OUT} = 12$ - 13 dBm is shown in Fig. 3.15. In this case and due to the gain compression, the VGA is not used. The average gain is ~ 11.5 dB (4 dB compression from the small signal values) with a peak-to-peak variation of 1.5 dB vs. all phase states and an *rms* gain error of 0.5 dB. The *rms* phase error is ~ 4 - 5° at 8.5-9.5 GHz, which is much lower than the 4-bit requirement. There are also no cross-overs in the phase shifts. The chip is therefore suitable for radar applications at 8.5-9.5 GHz with very low *rms* gain and phase errors, even under P_{SAT} conditions.

3.3.3 Spectral Regrowth and EVM

Fig. 3.16 presents the measured spectral regrowth at 8.7 GHz vs. different output levels for 20 MSym/s QPSK and BPSK modulation. It is seen that an output power of up to 4-5 dBm (OP_{1dB} -4 dB) results in very little spectral regrowth as expected. This is done at an input power of ~ -12 dBm, and the 1:4 active divider and the phase shifter both have virtually no phase distortion. At close to P_{SAT} , the spectral regrowth is not acceptable for communication systems. The measured EVM is 2-2.5% up to an output power of 5 dBm, and then increases rapidly at higher P_{SAT} values, as expected (Fig. 3.17). The I/Q constellation for a 20 MSym/s is shown and is near ideal up to 5 dBm (Fig. 3.18). The EVM values are 0.5-0.6% higher than measurements done on a PA breakout alone, indicating that the phase shifter and 1:4 active divider are contributing a small amount of additional error.

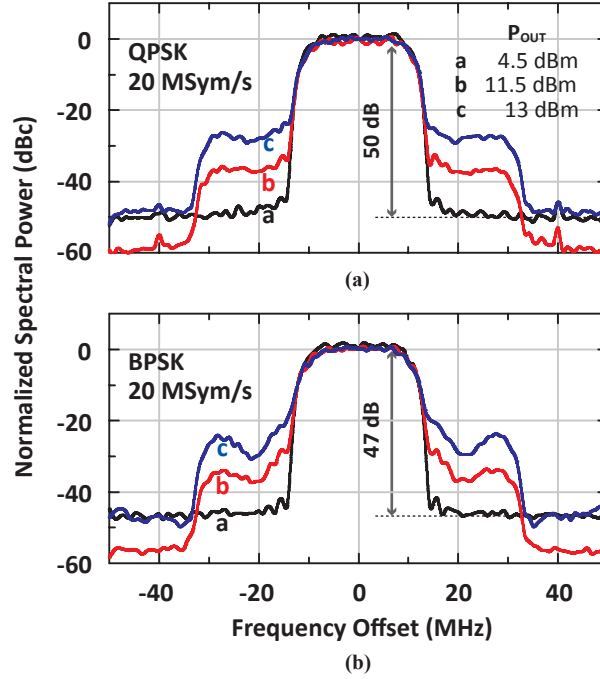


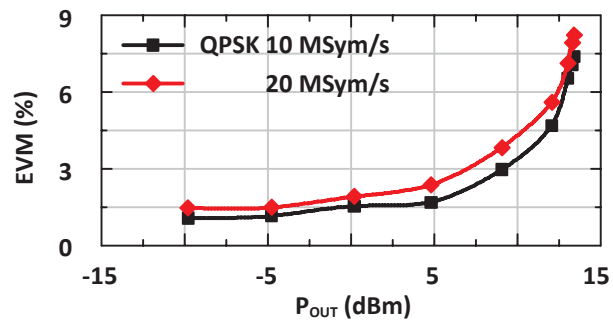
Figure 3.16: Measured output spectrum for (a) QPSK and (b) BPSK modulation at different output power levels.

3.3.4 On-Chip Coupling

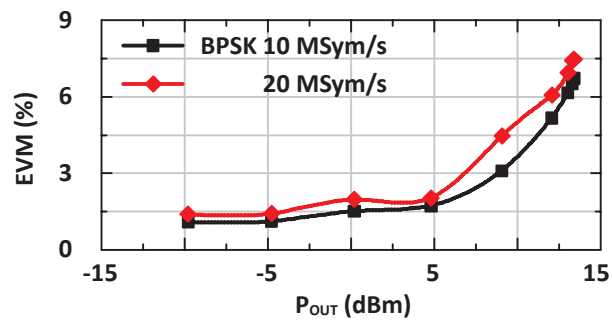
The coupling between the channels was measured according to [46] and is < -42 dB for neighboring channels at 7-11 GHz. This is due to the differential nature of the chip, and such low levels have been measured before on similar multi-channel chips [7, 34]. The coupling increases when the chip is placed in a package due to bondwire and ground inductance, and this is presented in Section IV.

3.4 Packaging

The 4-element chip was packaged in a chip-on-board (CoB) implementation and in a 6×6 mm² QFN package with a standard 0.5 mm pitch lead frame (Fig. 3.19). Both are assembled on a Rogers RT5880 printed-circuit board (PCB) with $\epsilon_r=2.2$ and $t=10$ mils with a large ground pad underneath the chip or QFN pedestal. A mold compound of $\epsilon_r=4.2$, $\tan\delta=0.015$ is used inside the QFN, but the CoB implementation does not use any glob-top material over it. Bondwires with 1-mil diameter are used to connect the



(a)



(b)

Figure 3.17: Measured EVM for (a) QPSK and (b) BPSK vs. input power at 8.7 GHz.

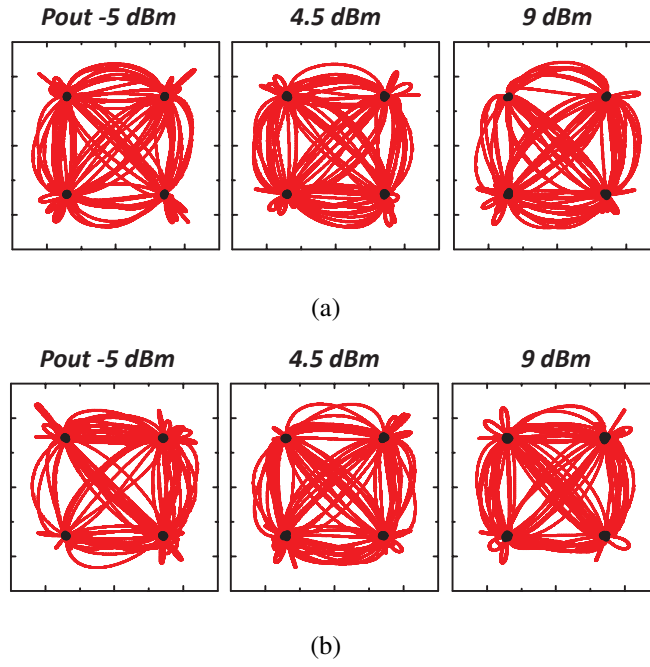


Figure 3.18: Measured QPSK (a) 10 MSym/s and (b) 20 MSym/s constellation vs. output power at 8.7 GHz.

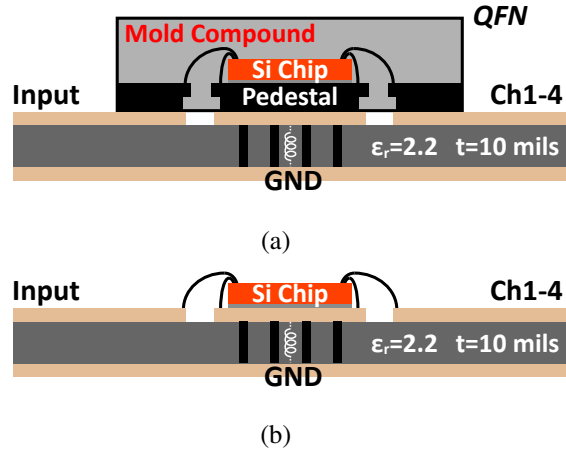


Figure 3.19: Cross-section of QFN package (6×6 mm²) and chip-on-board on a Rogers RT5880 substrate

CMOS chip to the board or inside the QFN package.

The electromagnetic coupling environment between the 4 CMOS RFIC output ports is shown in Fig. 3.20 for the CoB and QFN implementations. The on-chip transformers on the silicon chip, bond-wires, QFN pedestals, and transmission-lines and surrounding vias are all placed into Ansoft-HFSS and modeled together. Ports 1,2,3,4 are differential on the silicon chip, while Ports 5,6,7,8 are single-ended on the PC board. Note that grounded CPW lines are used around the chip to raise the ground plane to the top PCB surface and reduce the ground plane inductance. A maximum channel-to-channel coupling of < -34 dB and < -29 dB is achieved for the CoB and QFN implementations at 9 GHz (Fig. 3.20(b)). For the QFN implementation, and due to the relatively long signal and bondwires used, two ground bond-wires are needed between the signal ports in order to get high isolation, and this is the primary reason why a 6×6 mm² QFN package is used (instead of a 5×5 mm² package) (Fig. 3.21). The simulated insertion loss is < -1.3 dB at 7.5-9.5 GHz due primarily to the balun loss. However, this is lower than the simulated loss of the balun itself as shown in Fig. 3.10(b) due to the discretization of HFSS for such a large electromagnetic problem (finer discretization is used when simulating the balun alone).

The electromagnetic model also results in the S_{NN} at all ports and a matching network is then placed on the PC board for a 50 ohm impedance match. However, in the QFN case, the capacitance of the lead frame bond pad presents a near perfect compensation of the bond-wire inductance at X-band (~ 0.7 nH), and a matching circuit is not needed on the PC board. For the CoB case, a simple capacitive matching network is used. Similar impedance matching is done at the input port (not shown).

The circuit environment with packaging effect is shown in Fig. 3.22. In this case, the CMOS Cadence library models are used for all circuit components except for the input and output transformers. These are now embedded in the EM transition model, and an 8-port S-parameter matrix is used to account for the baluns and the bondwire/package coupling effects. This model also takes into account the additional ground inductance at the balun grounds which affects the coupling between the ports. A similar procedure is done on the input port, but in this case, it is just a two port S-matrix for impedance matching, and no coupling is present. Additionally, power supply inductance and ground

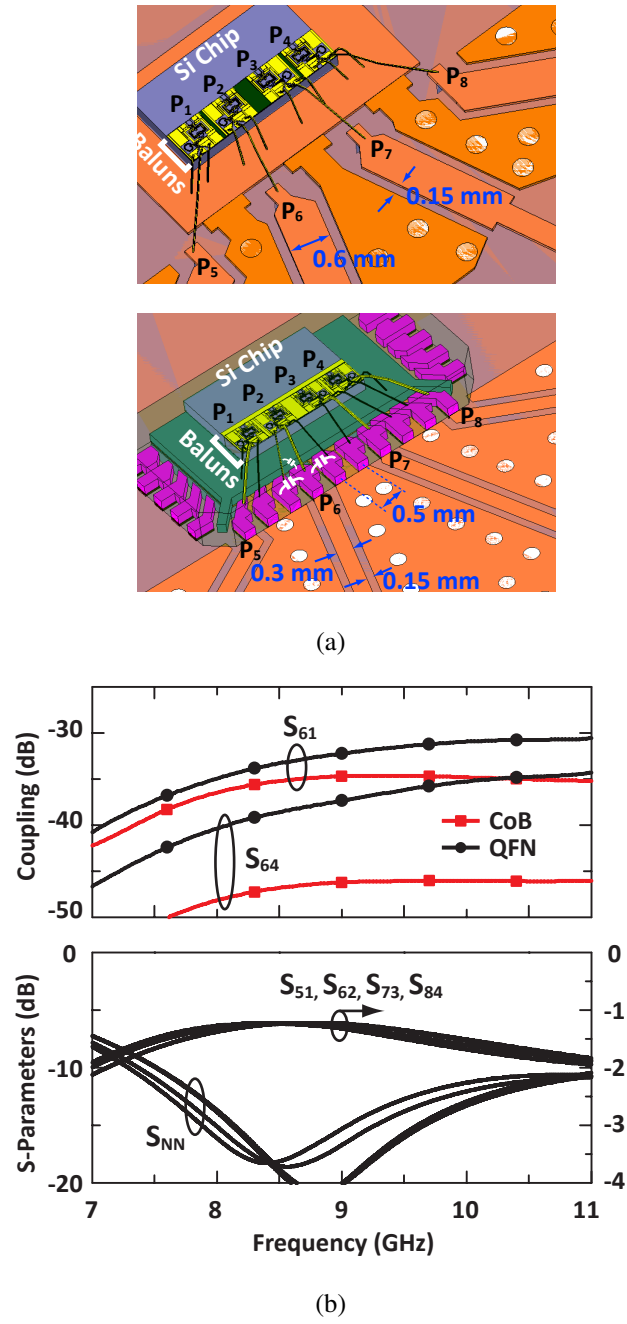


Figure 3.20: (a) 3-D EM simulation setups of the silicon chip, baluns and bond-wires in a package using HFSS, and (b) the resulting S-parameters.

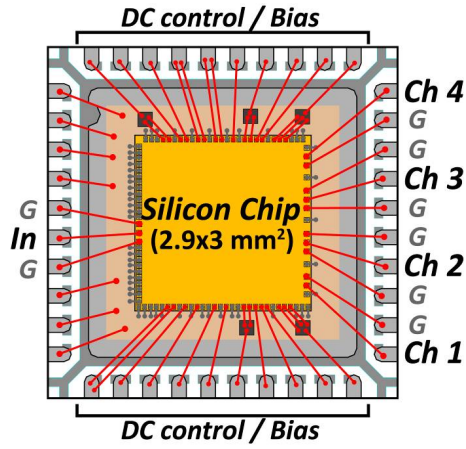


Figure 3.21: Bonding diagram of X-band phased-array transmitter chip in a QFN package.

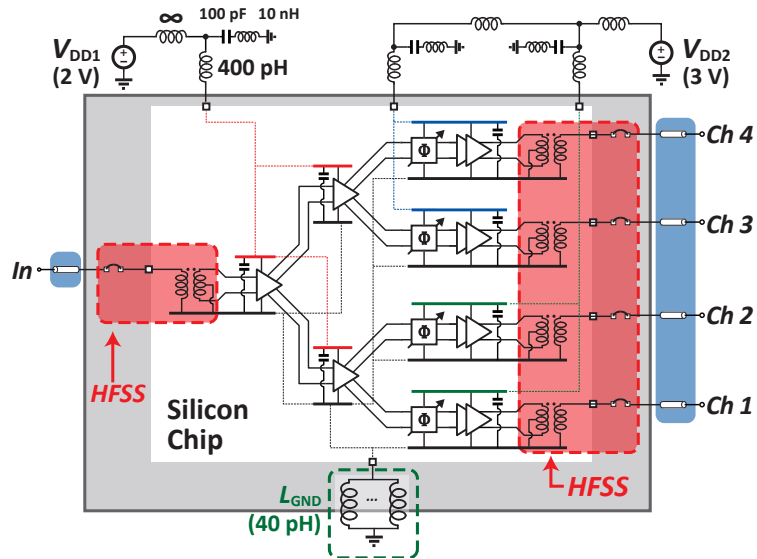
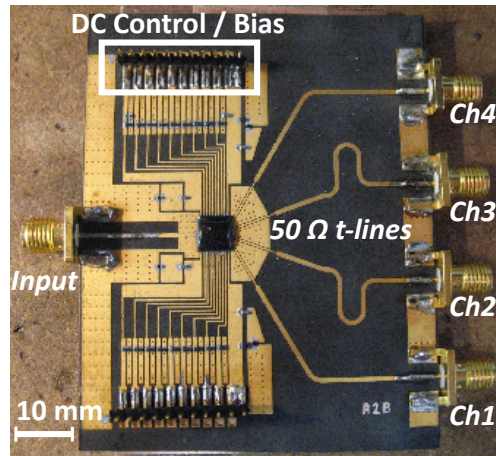
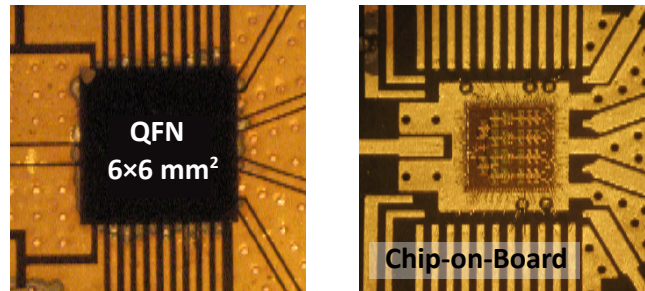


Figure 3.22: Circuit environment of the packaged phased-array transmitter including silicon chip, package 3-D EM simulation, and on-board matching/distribution network with bondwire inductances.



(a)



(b)

Figure 3.23: Photograph of the (a) packaged X-band phased-array transmitter on a Rogers RT5880 substrate and (b) close-in view of QFN and chip-on-board.

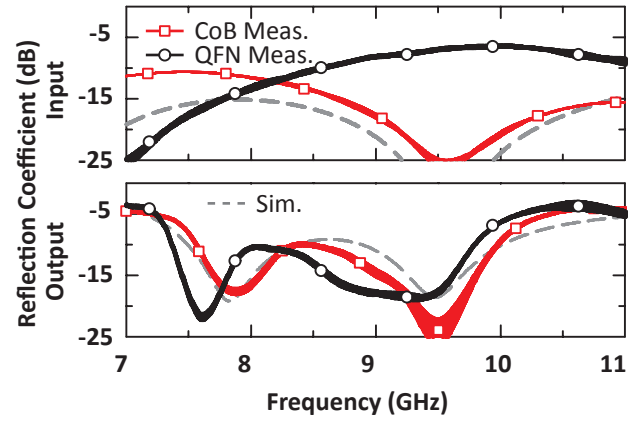
inductance are also taken due to the packaging effects. Simulations on the entire chip with ground inductance show no packaging detrimental effect (same S-parameters as Section 3.3.1) due to the differential circuits used. Therefore, the main effect of the packaging is the electromagnetic coupling between the elements.

The CoB and QFN implementations are shown in Fig. 3.23 together with the entire board. Note the grounded-CPW environment around the chip with transitions to four equiphase microstrip lines. The additional loss referenced to the SMA connectors is ~1.4 dB at 9 GHz (2×0.5 dB SMA connector loss and 0.4 dB microstrip line loss). The measured S-parameters referenced to the SMA connectors are shown in Fig. 3.24 for the CoB and QFN implementations. It is seen that the channels are well balanced (average gain shown for 16 phase states for each channel) and that the CoB results in slightly higher gain than the QFN implementation. Also, there is ~2 dB drop in the CoB gain as compared to the average gain of a chip measured with GSG probes which is close to the expected value of ~1.4 dB. The QFN package showed an additional drop in gain, partly due to the high S_{11} of 8.5-10.5 GHz (-10 to -7 dB). It is not clear why the QFN gain difference is much higher than expected at 9-11 GHz.

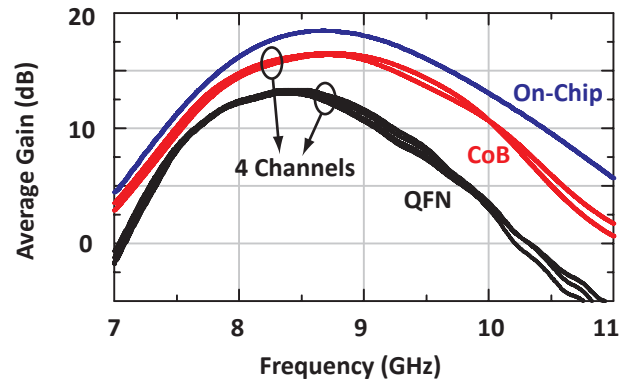
The measured output P_{SAT} is also shown in Fig. 3.24(c) and is 2.0-2.5 dB lower than the GSG probe measurements for the CoB and QFN implementations. Still, this chip delivers 11 dBm of power per channel at the output of the SMA connectors (13 dBm on-chip), which is the highest so-far from a CMOS chip at X-band frequencies.

The coupling between the channels was determined by measuring the output of channel 1 at a fixed phase setting and changing the phase of channels 2, 3, 4 from 0-360° (one channel at a time) [46]. This results in an amplitude and phase modulation in channel 1 bounded by $(1+c)$ and $(1-c)$ in amplitude and $\pm \tan^{-1}(c)$ in phase, and can be represented as an *rms* gain and phase error in channel 1. For $c=0.018$ -0.036 (-35 dB to -29 dB), the equivalent *rms* gain and phase error is 0.1-0.2 dB and 1-2°, respectively (Fig. 3.25(a)).

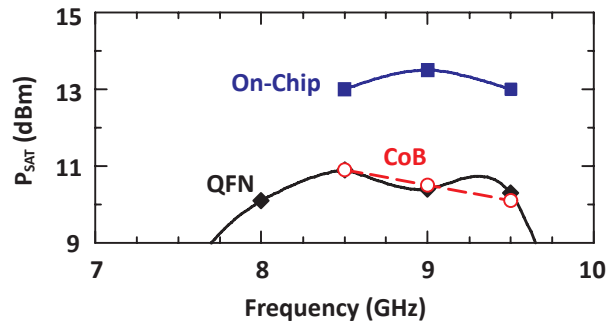
Fig. 3.25(b) presents the measured *rms* gain and phase error vs. frequency for channel 1 when the phase of channels 2,3,4 are changed. Both the CoB and QFN resulted in nearly the same coupling for channel 2 and the QFN results are shown. As expected, the maximum coupling occurs between channels 1 and 2, with an *rms* gain



(a)



(b)



(c)

Figure 3.24: Measured (a) reflection coefficients and (b) average gain of 16 phase states and (b) P_{SAT} compared to the on-chip measurement of QFN and CoB packaged X-band phased-array transmitter.

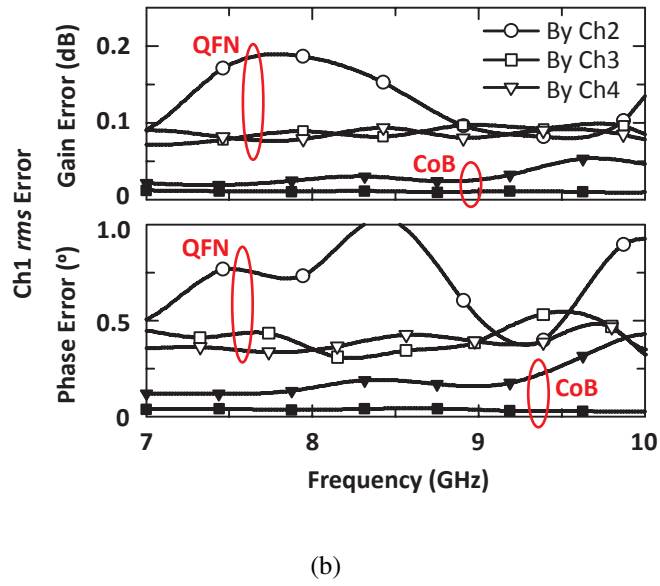
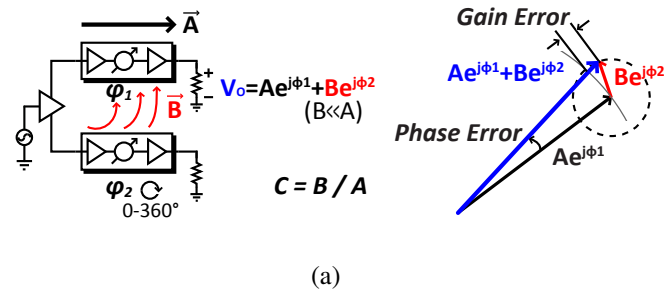


Figure 3.25: (a) Vectorial representation of channel-to-channel coupling, and (b) measured *rms* gain and phase error of channel 1 when changing the phase states of channel 2, 3, and 4 in a QFN and CoB package.

error of <0.2 dB and $\sim 1^\circ$ at ~ 8 GHz. This is equivalent to a peak coupling of -29 to -30 dB as expected from simulations. Note that QFN channels 3 and 4 show a wideband coupling characteristic of -35 dB which may be due to V_{DD} coupling and to the silicon RFIC/package/PC board ground inductance. For the CoB, channels 3 and 4 result in a wideband coupling characteristics of -45 dB (rms gain and phase error <0.05 dB and $<0.5^\circ$.) showing the reduced ground and V_{DD} inductance of this implementation.

3.5 Conclusion

This paper presented a 4-element high-power phased-array transmitter capable of operation in a communication or a radar mode. It is found that the vector modulator phase shifter and the power amplifier result in phase distortion vs. power but these can be calibrated out in radar mode operation. For communication systems, it is best to operate below the output P_{1dB} level for complex constellations. The chip has been packaged using CoB and QFN techniques, and the CoB results in higher ultimate isolation between the channels (-45 dB) as opposed to the QFN (-35 dB). However, both result in nearly the same isolation between the neighboring channels (~ -30 dB) which is primarily limited by bond-wire coupling. This work shows that complex phased-arrays with multiple channels can be packaged in low-cost QFN packages for X-band applications.

3.6 Acknowledgment

This work was supported by the Army Research Laboratories under the X-band Radar and SATCOM program, Alfred Hung and Ed Viveiros, Program Monitors.

This chapter is mostly a reprint of:

- Donghyup Shin, C. Y. Kim, D. Kang, and G. M. Rebeiz, "A 4-Element X-Band CMOS Phased-Array RFIC in a QFN Package," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Montreal, Canada, June 2012, pp. 1–3.
- Donghyup Shin, C. Kim, D. Kang, and G. M. Rebeiz, "A High-Power Packaged Four-Element X-band Phased-Array Transmitter in 0.13- μ m

Table 3.2: Summary of the Performance

Technology	IBM8RF CMOS	0.13- μ m
Frequency Band	7.9–9.6 GHz	
Supply Voltage	2.0/3.0 V (analog), 1.5 V (digital)	
Power Consumption	870 mW	
Chip Area	2.9 $\times$ 3.0 mm ²	
Phase Resolution	4-bit (+ trim-bit)	
Gain Control	5 dB (3-bit)	
Peak Average Gain	15.5 dB (Linear-mode) 11.5 dB (Saturated-mode)	
<i>rms</i> Gain Error	< 0.5 dB (calibrated)	
<i>rms</i> Phase Error	< 6° (calibrated)	
Max. Output Power (P_{SAT})	13.6 dBm (On-Chip) 11.0 dBm (QFN, CoB)	
Coupling between Channels	<-41 dB (On-Chip) <-29 dB (QFN, CoB)	

CMOS for Radar and Communication Systems,” *IEEE Trans. Microw. Theory Tech* (in review).

Chapter 4

12 Gbps 4x4 Switching Matrices in 0.13- μ m CMOS

4.1 Introduction

Switch matrices are used in reconfigurable communication systems, optical networks, and automated test equipment, and they are generally based on low-loss metal-contact relays (for ATE and satellite communications), active III-V and SiGe technologies (data networks), or pin diodes (communication systems) [57–61]. RF MEMS switches have been proposed to replace the switching matrices in ATE or communication systems due to their much longer life, smaller size and excellent isolation, and several switch matrices were demonstrated at DC-12 GHz with low loss [62–65]. However, advances in CMOS electronics, especially at the 130 nm to 65 nm nodes, allow for high-performance transistors that can be used in low-loss/high-isolation switching matrices. For example, SP4T switches have been demonstrated at 0.01-67 GHz with low loss [?].

This paper presents a high isolation 0.01-8 GHz 4×4 switch matrix in CMOS technology. The 4×4 switch does not consume any power and can be used in the receive section of complex multiband communication systems [22] or as a crossbar switch for data networks [57,58,61,64]. Note that traditional crossbar switches are based on active cascode-transistor switches and consume a lot of DC power, while this implementation

is entirely passive. A high isolation switching cell is first presented and optimized, and is then implemented in the 4×4 switch matrix. The design is scalable to higher number of ports and to wider bandwidths using advanced CMOS nodes.

4.2 Design

Fig. 4.1 presents a block diagram of two versions of the 4×4 switch matrix. In the first design, the 4 inputs ports are connected to any one of the 4 output ports by selecting the appropriate switches. In the second design, the input ports (and output ports) may be terminated by a matched load and not connected to any port, and this is achieved using a switched load at the end of the transmission line. Both are quite common in switching matrices depending on the application. In both designs, the unit switching cell is based on a series-shunt-series switch and is connected in a 4×4 grid across the input and output. The series-shunt-series switch results in high isolation, an open circuit on both ports, and does not load (or short) input/output ports when not engaged.

There are two important design considerations for the 4×4 switch matrix: 1) A high-isolation transmission-line cross-over and 2) a low-loss switch. The $50\ \Omega$ transmission-line is implemented as a coplanar-waveguide (CPW) configuration in the silicon metal-backend (IBM8HP but only the $0.13\ \mu\text{m}$ CMOS part is used for the transistors) with dimensions of $11/12/11\ \mu\text{m}$ and a simulated loss of $0.07\text{-}0.22\ \text{dB/mm}$ at $1\text{-}8\ \text{GHz}$ (Fig. 4.2). The CPW cross-over is implemented using the AM and LY metals, and has a simulated isolation of $> 46\ \text{dB}$ up to $8\ \text{GHz}$ with negligible insertion loss (Fig. 4.3). A high isolation is possible due to the narrow CPW line width and relatively large dielectric spacing between the lines ($4\ \mu\text{m}$).

The IBM8HP deep n-well switch is used to reduce the loss arising from the substrate contact resistance, which results in an excellent figure of merit ($\text{FOM} = R_{ON}C_{OFF}$) (Fig. 4.4). A deep n-well increases effective substrate resistance and minimizes the capacitance between the body and substrate without latch-up problems. The transistor body and n-well are tied to ground and V_{DD} , respectively, using $R = 20\ \text{k}\Omega$ to eliminate any RF leakage (Fig. A.2(a)). Fig. 4.4 presents the simulated R_{ON} , C_{OFF} and FOM for

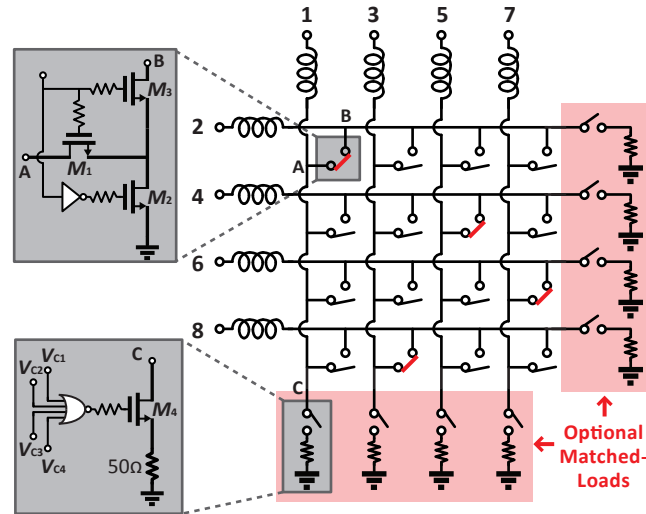


Figure 4.1: Schematic of a 4×4 switch matrix. The resistors at the end of each line are optional and allow for a matched load if an input port is not switched to an output port.

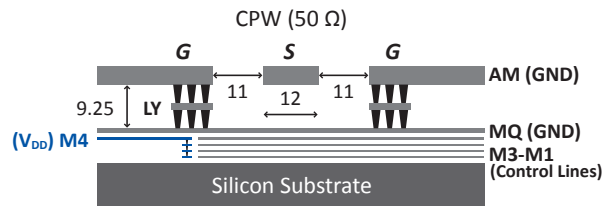


Figure 4.2: IBM8HP metal stack-up. The CPW line is built in the top three layers.

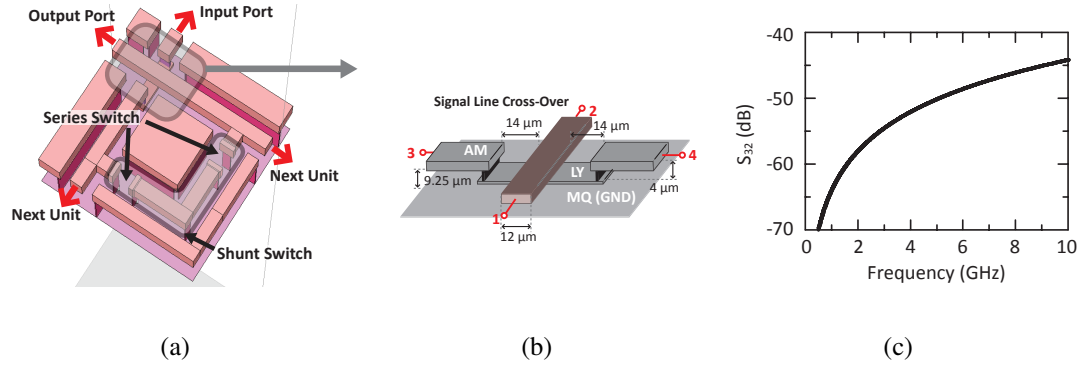


Figure 4.3: The 4×4 switch unit-cell with the series-shunt-series switch, (b) details of the CPW cross-over, and (c) cross-over isolation using full electromagnetic simulations.

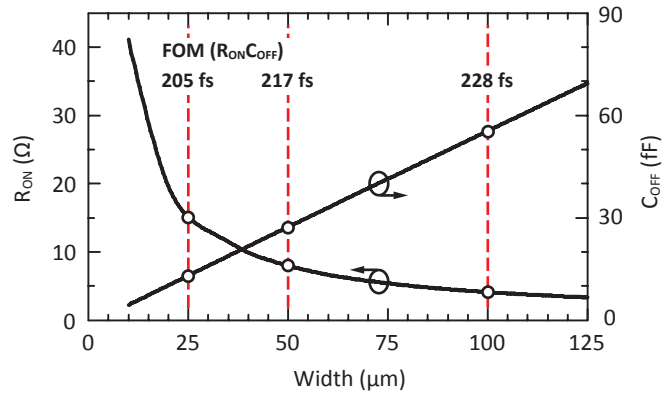
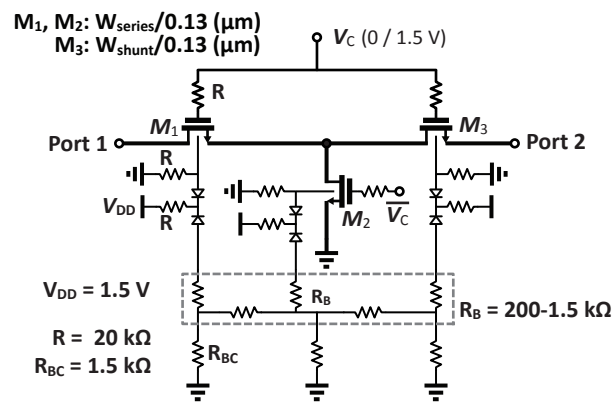
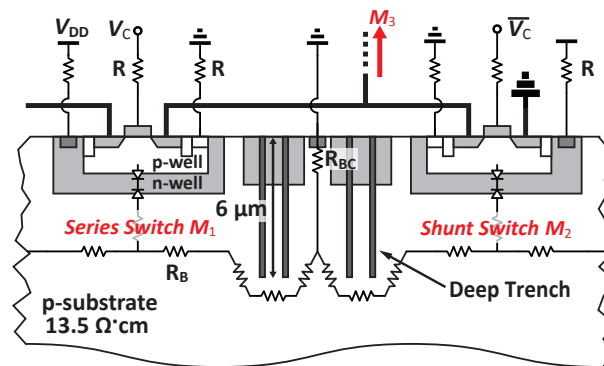


Figure 4.4: Simulated figure of merit (FOM) for a 0.13 μm deep n-well CMOS transistor in a series configuration with $V_{GS}=1.5$ V.



(a)



(b)

Figure 4.5: Series-shunt-series switch: (a) circuit diagram and (b) cross-section.

the deep n-well switch with widths of 25, 50 and 100 μm . The FOM is 217 fs for a 50 μm switch and is competitive with GaAs devices [60], [66, 67].

A Sonnet [45] model of the series-shunt-series switch cell is also shown in Fig. 4.3(a). Note that the series transistors are located close to the transmission-lines in order to minimize the off-state capacitance (i.e., no open stub connected to the transmission line). Also, a ground island is placed in the middle of the switch and is connected to the MQ layer for added isolation. The shunt transistor is connected to the MQ layer at its source terminal and results in a very low inductance to ground. The transmission-lines, cross-overs, and via connections are simulated in Sonnet with internal ports for the transistor switches. This switch cell is then placed in Cadence and the 4×4 switch matrix is optimized by varying the series transistor size.

The series-shunt-series switch is first optimized with 50 Ω ports using the IBM transistor model. Fig. 4.6(b) presents the simulated insertion loss and isolation with a shunt transistor width of 50 μm . The switches are surrounded by deep trenches which enhances the isolation between adjacent switches (Fig. 4.5(b)). A series transistor size of 50-150 μm results in an insertion loss of 1.7-1.0 dB and an isolation of ~ 43 dB at 6 GHz. A parametric study vs. the shunt transistor size indicates that a 50 μm wide transistor is the best compromise between high isolation (100 μm wide transistor is better but with higher insertion loss) and low insertion loss (25 μm wide transistor is better but with lower isolation).

The series-shunt-series transistor is not used in a stand-alone 50 Ω circuit but in a distributed 4×4 switch matrix. When an input port is connected to an output port using a series-shunt-series switch in the “pass” state, three switches are still connected to the transmission-line each in the “isolation” state and with their own loading capacitance. These “isolation” switches add to the overall 4×4 switch matrix loss by shunting some of the RF current to ground, and therefore, the series switches must be as small as possible. On the other hand, the series switches must be as large as possible to result in a low insertion loss in the “pass” state. A compromise is therefore required for the series transistor size. The insertion loss and isolation are simulated including the matching inductor ($L=838$ pH, $Q=5.0-15.8$ at 1-8 GHz) and the effect of C_{OFF} and R_{ON} (Fig. 4.6). A 70 μm series transistor results in the best compromise between insertion loss

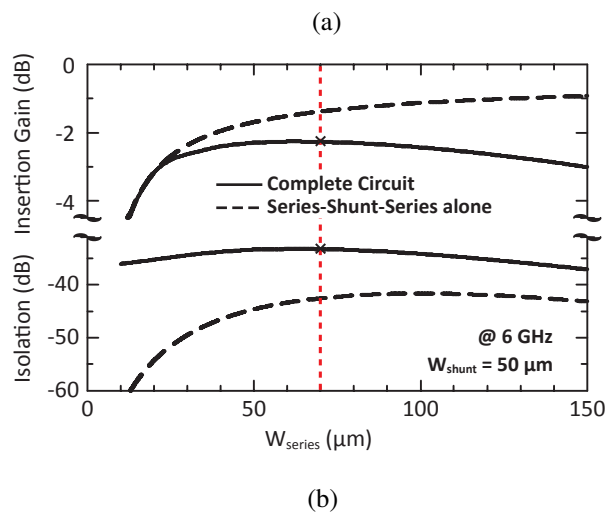
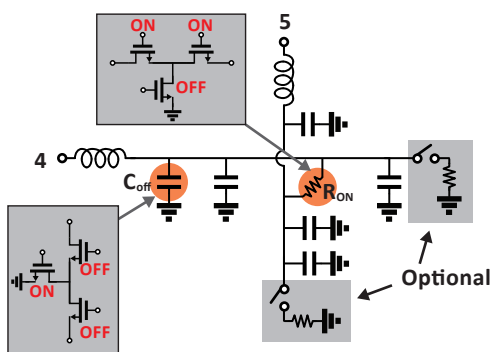


Figure 4.6: (a) Circuit diagram for an input-to-output interconnection, and (b) simulated insertion loss and isolation vs. series switch width.

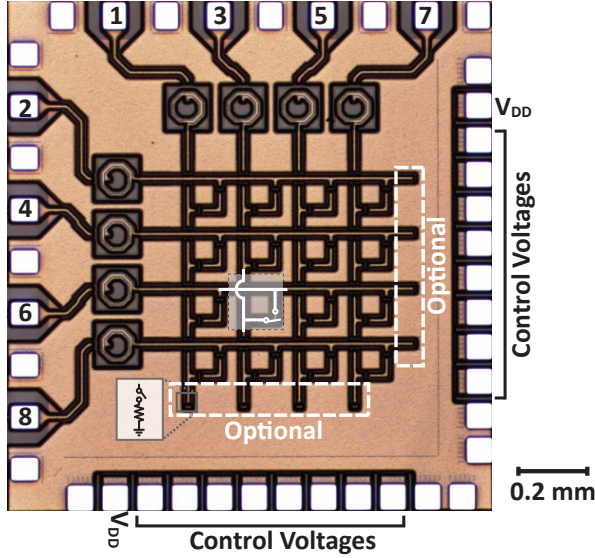


Figure 4.7: Microphotograph of the 4×4 switch matrix. The chip size is $1.4 \times 1.5 \text{ mm}^2$.

and isolation. A matching inductance is required at the input and output ports in order to compensate the capacitive loading on the line and create a low-pass LC matching network.

Design #1 (Fig. 4.1 with no matched load) results in an insertion loss of 1.4-3.3 dB with an isolation of 58-36 dB at 1-8 GHz. Design #2 (Fig. 4.1) is optimized using the same technique, and a $15 \text{ }\mu\text{m}$ series transistor with a matched load is placed at the end of each transmission line. This series transistor is connected to a $50 \text{ }\Omega$ load and can greatly increase the insertion loss if a large width is chosen. The simulated insertion loss and isolation are 1.4-3.7 dB and 58-37 dB at 1-8 GHz when the ports are connected to each other.

The simulated input P_{1dB} and IP_3 for both designs are 9-8 dBm and 27-28 dBm, respectively, at 1-8 GHz. The slight P_{1dB} drops with frequency due to the LC matching network which acts as a voltage transformer and increases the effective RF voltage at the series-shunt-series switch.

4.3 Measurements

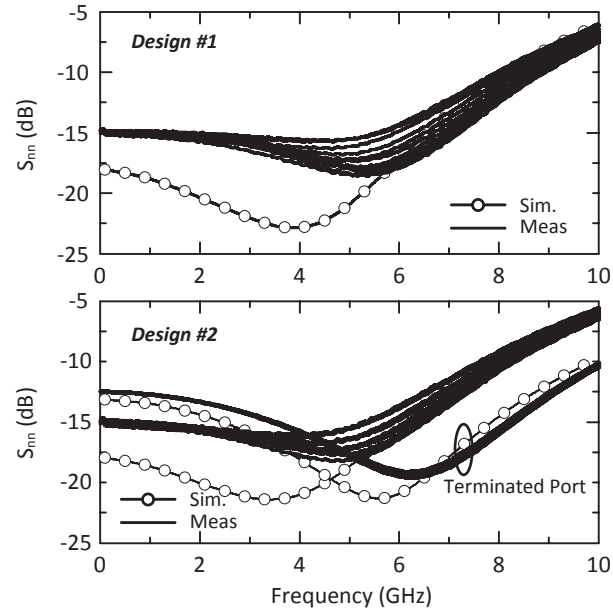
The 4×4 switch matrix is shown in Fig. A.4. Two chips were fabricated, one with the switched load (Design #2) and one without the switched load (Design #1 - not shown since it is very similar to Fig. A.4 except for the end section). The control voltages are 1.5 V with near zero current consumption. Measurements are done on-wafer using GSG probes and an SOLT calibration, and this places the reference planes at the probe tips.

Fig. 4.8 presents the measured reflection coefficient and insertion gain vs. different switch matrix configurations. The lowest loss is achieved when ports 1 and 2 are switched together, while the highest loss is achieved when ports 7 and 8 are switched together. The measured insertion loss is ~ 0.5 dB higher than simulation due to inaccuracy in the switch resistance model. At 8 GHz, the insertion loss is 3.3 ± 0.3 dB for all switching combinations (Design #1). As expected, Design #2 results in a slightly larger insertion loss due to the switched-loads at the end of the transmission-lines. The insertion loss at 3 GHz is 2.2-2.3 dB for both designs.

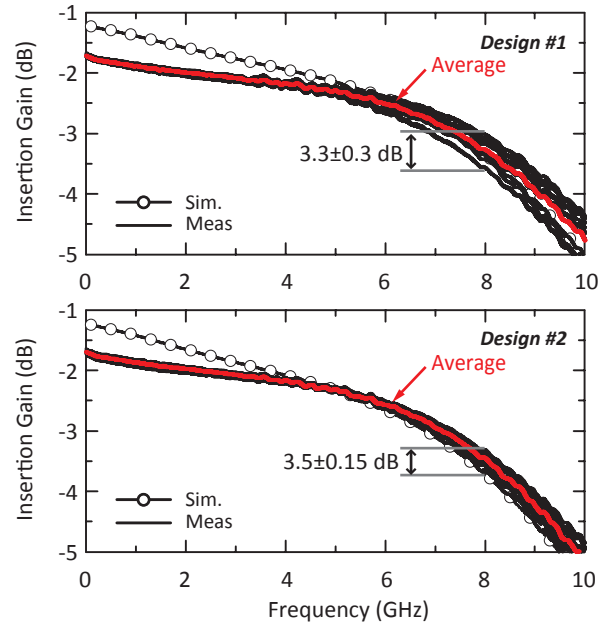
The measured isolation is also presented over a large number of switch configurations and is better than 46 dB up to 8 GHz (Fig. 4.9). The discrepancy above 3 GHz is due to a non-accurate IBM switch model (R_B and R_{BC} are layout dependent and hard to model). For Design #2, measurements are also presented when an input port is terminated and the isolation between this input port and all the output ports is obtained. Note that the isolation is virtually identical for all measured switch configurations showing the repeatability of the series-shunt-series switch and the ground inductance.

The CMOS switches do not handle a lot of RF power since self-biasing occurs at the gate when the switch is in the off-state position and this can turn the switch to the on-state (or slightly bias the channel thus changing the switch characteristics). The measured input P_{1dB} is 9-10 dBm and the measured input IP_3 is 28-30 dBm and both agree well with simulations (Fig. 4.10(a)). These values are acceptable for many communication systems (receive port only) or $N \times M$ switching systems. The switch matrix maintains a very high isolation for all input powers, and this is due to the series-shunt-series design (Fig. 4.10(b), also see [68] for more details).

The 4×4 switch matrix was also tested when used for networking systems since



(a)



(b)

Figure 4.8: Measured and simulated (a) S_{nn} ($n=1-8$) and (b) insertion gain for the two different 4×4 switching matrices.

it has a group delay variation of < 6 ps up to 8 GHz (Fig. 4.11(a)). A 3-12.5 Gbps ASK non-return-to-zero signal was used with a power of 1.5 dBm at the input port, and the signal was switched to different output ports. The measured output eye diagram is shown in Fig. 5.14, and the BER was $< 10^{-12}$ up to 12.5 Gbps for the “insertion loss state” with a measured *rms* jitter of 4 ± 0.5 ps. The 4×4 switch isolation is so high that the tester could not lock or measure a BER for the isolated ports.

4.4 Conclusion

This work presented a 0.01-8 GHz 4×4 CMOS switch matrix with low insertion loss and high isolation. The CMOS switch matrix consumes ~ 0 mW, has high linearity and adequate power handling for receive systems and backplane switching networks. The switch matrix can be scaled to a larger number of ports and higher frequencies using advanced CMOS nodes. For example, the switch FOM in the IBM 45 nm CMOS SOI technology is 75 fs and would allow for low-loss 8×8 switch matrices operating up to 40 Gbps together with equalizers and retimers on the same chip [69–72]. Furthermore, the designs can be extended to differential circuits which are less sensitive to ground inductance and are compatible with backplane data networks.

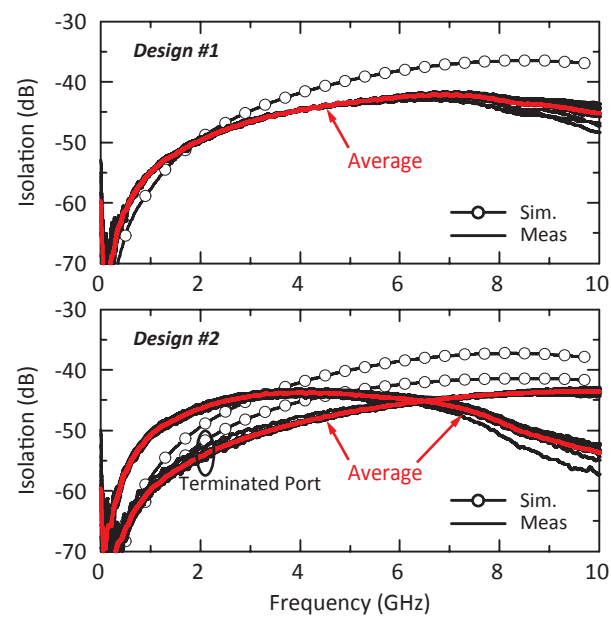


Figure 4.9: Measured and simulated isolation for the two different 4×4 switching matrices.

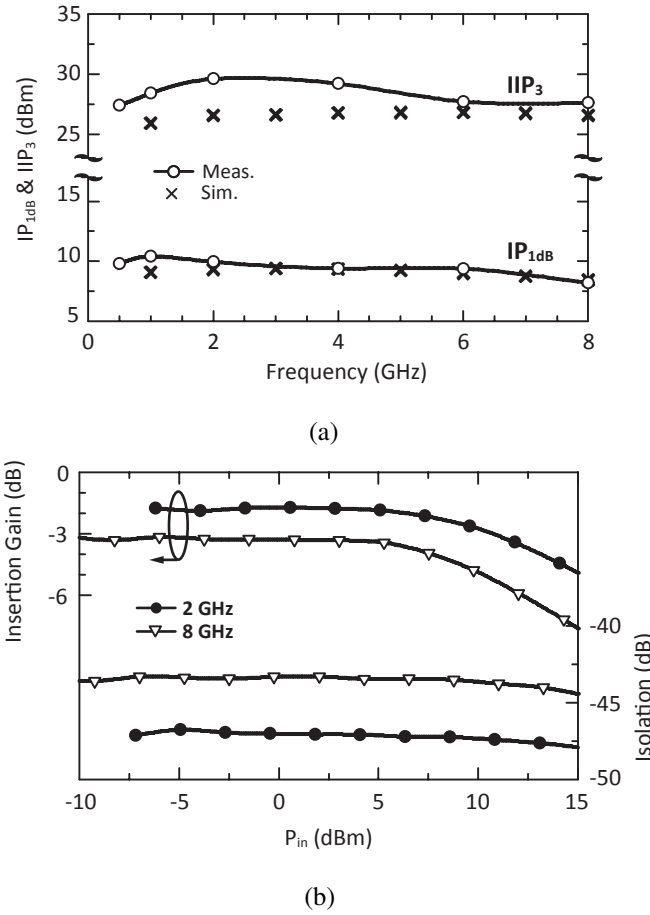
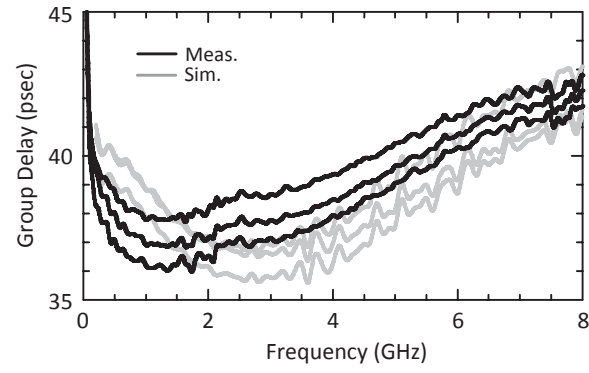
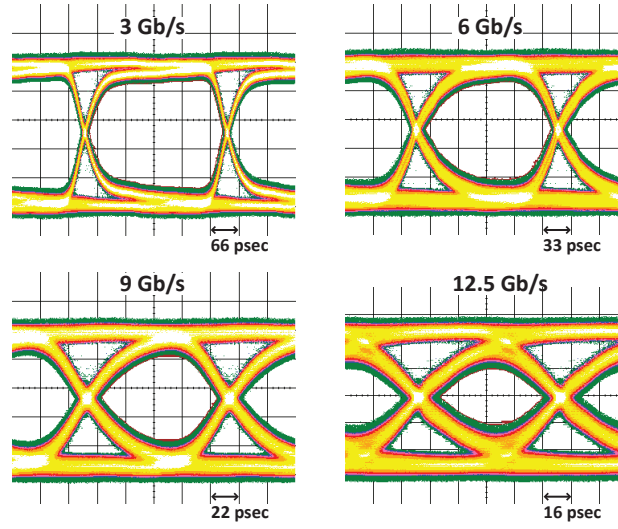


Figure 4.10: Measured and simulated large signal performance: (a) Input P_{1dB} and IP_3 , and (b) insertion gain and isolation vs. input power. Measurements are done on the 4x4 switch matrix without termination resistors.



(a)



(b)

Figure 4.11: (a) Measured and simulated group delay for the shortest (S_{21}) to longest (S_{87}) path. (b) Measured eye diagrams for different data rates.

Table 4.1: Performance Comparison of Switch Matrices

	This Work	[57]	[58]	[61]	[62]	[63]	[64]
Technology	0.13 μm CMOS	AlGaAs/ GaAs HBT	GaAs HBT	InP HBT	MEMS on LTCC	MEMS	MEMS
Frequency (GHz)	0.01-8	–	–	–	0.01-7	0.01-13.5	0.01-20
Data Rate (Gbps)	12.5	10	10	25	–	–	–
Isolation (dB)	>44	>40	>23	>10	>55	>45	>25
Insertion Loss (dB)	<3.3	–	–	-5	<1.5	<2.2	<2
Topology	4 $\times$ 4	16 $\times$ 16	16 $\times$ 16	2 $\times$ 2	4 $\times$ 4	3 $\times$ 3	3 $\times$ 3
Power Consumption (W)	$\sim$ 0	11.3	10.5	0.24	$\sim$ 0	$\sim$ 0	$\sim$ 0
Dimension (mm ²)	1.4 $\times$ 1.5	6.0 $\times$ 6.6	7.1 $\times$ 6.4	1.1 $\times$ 1.1	15.0 $\times$ 15.7	22 $\times$ 16	2.6 $\times$ 2.6

4.5 Acknowledgment

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This chapter is mostly a reprint of:

- Donghyup Shin, D. Kang, and G. M. Rebeiz, “A 0.01-8 GHz (12.5 Gbps) 4×4 CMOS Switch Matrix,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 2, pp. 381–386, Feb. 2012.

Chapter 5

Scalable High Data-Rate Switching Matrices in 45nm CMOS

5.1 Introduction

Switch matrices are multiple-input/multiple-output non-blocking switches commonly used in various communication systems including satellite communication [73–75], multiband reconfigurable RF front-end, and digital/optical data communications [23–32, 57, 58], and also in automated measurement system [76]. Switch matrices provide signal routing thereby reducing the system redundancy and maximizing the bandwidth utilization. Many different technologies are being used or proposed for different applications starting from coaxial switches [76], RF microelectromechanical systems (MEMS) switches [73, 74] to silicon integrated circuits using CMOS and HBT's [23–32, 57, 58, 75]. These various applications share common requirements: 1) high fidelity of data transmission, 2) reasonable switching speed, and 3) high isolation between ports. In [77], we have demonstrated that passive 0.13- μm CMOS switches can be used for high data-rate networking with high isolation and near-zero power consumption. This paper presents switching matrices with very high data-rate with low power consumption and emphasis on scalability using 45-nm SOI CMOS technology. An all-passive design maximizes the 3-dB bandwidth using only passive switches. The bandwidth can further be increased by having active buffers to compensate for the switch

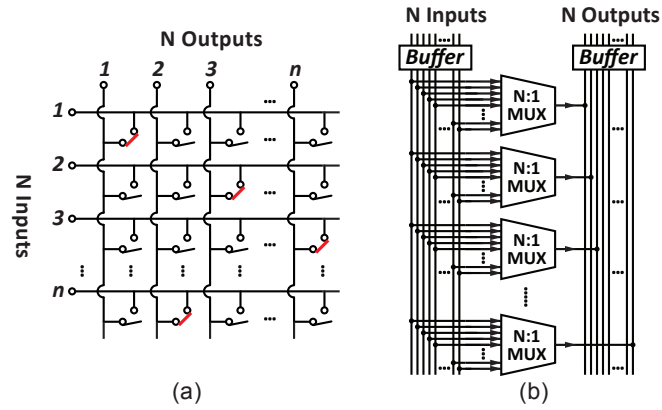


Figure 5.1: Block diagram of switch matrices of (a) cross-point architecture and (b) multiplexer-based architecture.

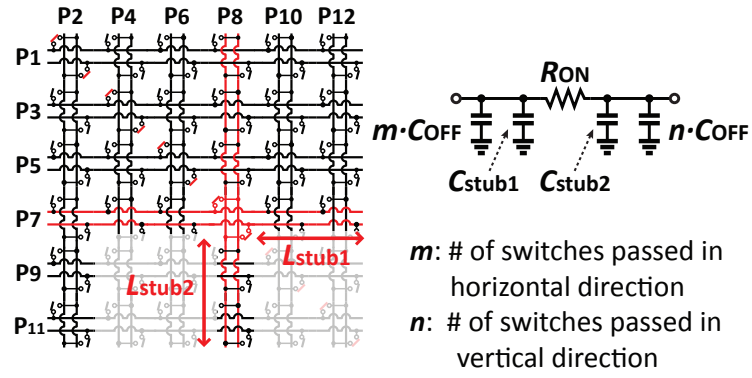
loss and boost the bandwidth even more (passive-active design). The designs are optimized to achieve high-speed digital signal networking operation under consideration on signal integrity and scalability.

5.2 Design

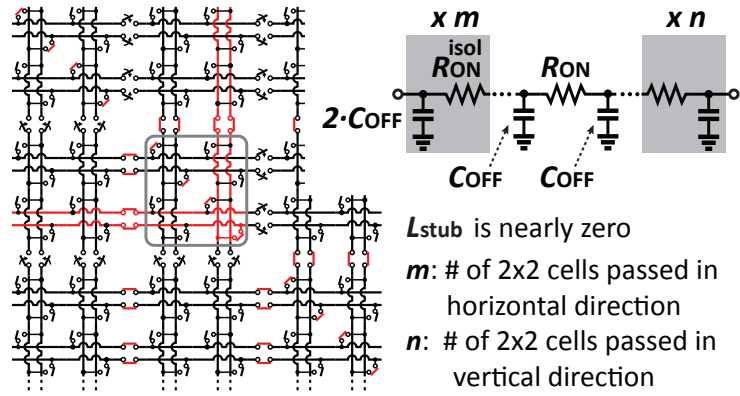
5.2.1 Scalable Architecture

Fig. 5.1 compares the two architectures in switching matrix designs: cross-point and multiplexer-based architecture. Current-mode logic (CML) multiplexer-based architecture uses multiple of $N:1$ multiplexers connecting each input port to the desired output port. Most of the commercial switching matrices today are based on the multiplexer-based architecture because it provides fast switching and regeneration of signal waveform. However, it consumes significant DC power. In contrast, the cross-point architecture is composed of multiple overlapped vertical and horizontal transmission lines and switches placed at every cross-points. The switches at the cross-points can either isolate the vertical and horizontal lines (isolation-state) or connect them to each other (pass-state). It has advantage of low power consumption by using passive switches and its simple structure offers very easy scalability of the matrix design.

Scalability of a passive cross-point architecture is limited by the shunt capaci-



(a)



(b)

Figure 5.2: Block diagrams and simplified small-signal model of all-passive switching matrices (a) with and (b) without isolation switches.

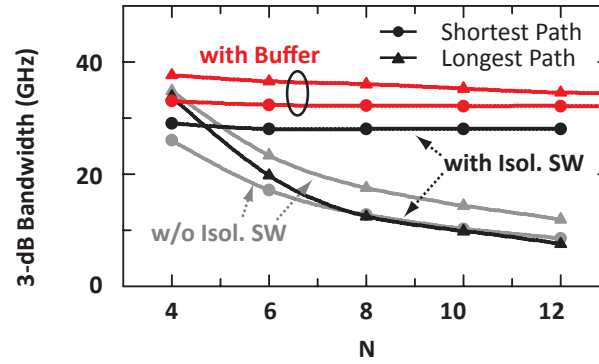


Figure 5.3: Simulated 3-dB bandwidth vs. N (number of input and output channels) of switching matrices with and without isolation switches.

tances loaded to the signal line as N (number of input and output channels) increases. Shunt capacitance comes from the off-state switches that are passed by the signal line and, more importantly, the transmission lines which are not connected to the output ports. They effectively become short open-stubs, which add significant capacitance as N and their lengths increase. Fig. 5.2(a) shows the simplified model of a passive switch matrix when P7-P8 are connected ($m = n = 3$). L_{stub1} and L_{stub2} are the lengths of transmission-lines with open end, which create effective capacitances of $C_{stub} = \tan(\beta L_{stub})/wZ_O$ and increases abruptly as L_{stub} increases. This capacitance creates a dominant pole for the switching matrices with $N \geq 4$ and as a result, the 3-dB bandwidth drops rapidly as N is larger than 4 (Fig. 5.3). For this reason, the shortest path (P1 to P2) becomes the limiting path for 3-dB bandwidth and the longest path has higher bandwidth because it has the shortest L_{stub} .

The bandwidth limitation of the shortest path can be overcome by using an isolation switch after each 2×2 cell as shown in Figs. 5.2(b) and 5.4. After unit switching cell is turned on and becomes a “pass-state” (horizontal and vertical lines connected), the isolation switch following this unit cell is turned off such that the open-ended transmission line after the “pass-state” switch becomes very short irrespective of the size of the switching matrix, i.e. C_{stub} becomes very small. As a result, overall frequency response is dominated by the pass-state switch inside the unit cell and the 3-dB bandwidth remains almost constant even when N increases to 12. However, the longest path is limiting the bandwidth because C_{OFF} (capacitance of unit switching cell in isolation-state)

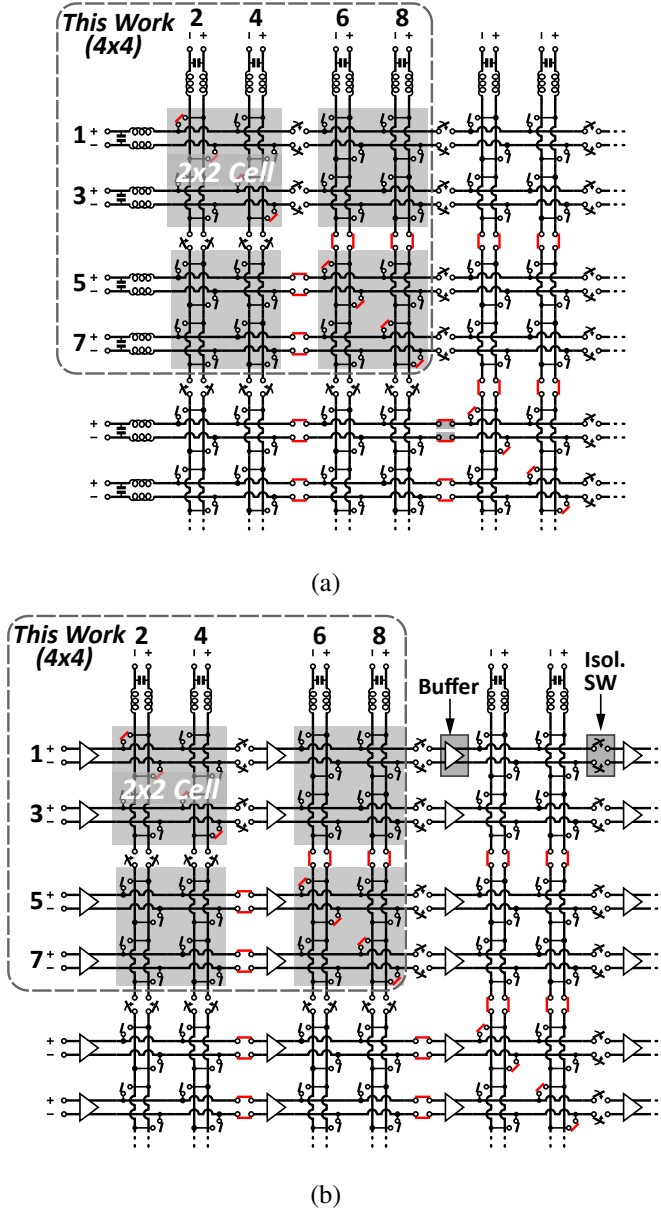


Figure 5.4: Block diagram of (a) all-passive and (b) passive-active switching matrices.

and R_{ON}^{isol} (on-state resistance of isolation switch) are accumulated and 3-dB bandwidth shrinks as N becomes very large. The all-passive design using isolation switches can maintain > 20 GHz up to 6×6 switching matrix.

In order to improve the bandwidth limitation of passive switch and also to maintain the scalability even when N is very large, active buffers can be used. Moreover, broadband buffers using inductive-peaking can increase the overall bandwidth by compensating for the gain drop of passive switches at high frequency. In order to maintain the scalable design, active buffers are placed before every 2×2 cells such that a (buffer)–(2×2 -cell)–(isolation-switch) comprises a unit that are duplicated over the matrix with proper bias and control lines (Fig. 5.4). Simulated result shows that active-passive design can achieve > 30 GHz 3-dB bandwidth and maintains scalability even when N is > 12 (Fig. 5.3).

5.2.2 Passive Switch Design

The IBM 45-nm SOI CMOS process provides advanced switch performance for high frequency operation. The 45-nm floating-body NFET switch provides very low FOM (Ron·Coff) of ~ 80 fsec. In SOI process, buried-oxide (BOX) layer is placed underneath the active layer. Since the bottom of source and drain touches the BOX layer, junction area capacitance between source (or drain) and substrate is not present. Instead, capacitance through the BOX layer (C_{BOX}) is present, but it is much smaller than junction capacitance, and as a result, transistors are effectively isolated from the low-resistivity ($13.5 \Omega\cdot\text{cm}$) silicon substrate [69]. Therefore, the substrate resistance network which degrades the insertion loss and isolation of switch is no longer effective in the SOI CMOS process. The backend provides 11 metal layers (10 coppers and one aluminum top metal) which offers differential grounded coplanar-waveguide (G-CPW) of 100Ω characteristic impedance (Z_{diff}) from $22/10/8/10/22 \mu\text{m}$ geometry. However, differential 100Ω lines are only used for connecting the RF pads to the active area because they occupy a large space.

Crosstalk between channels is minimized in the unit switching cell by designing the crosspoint layout and switch configuration to get the maximum isolation. As shown from Fig. 5.6, a differential line crossover is implemented using top two metal layers

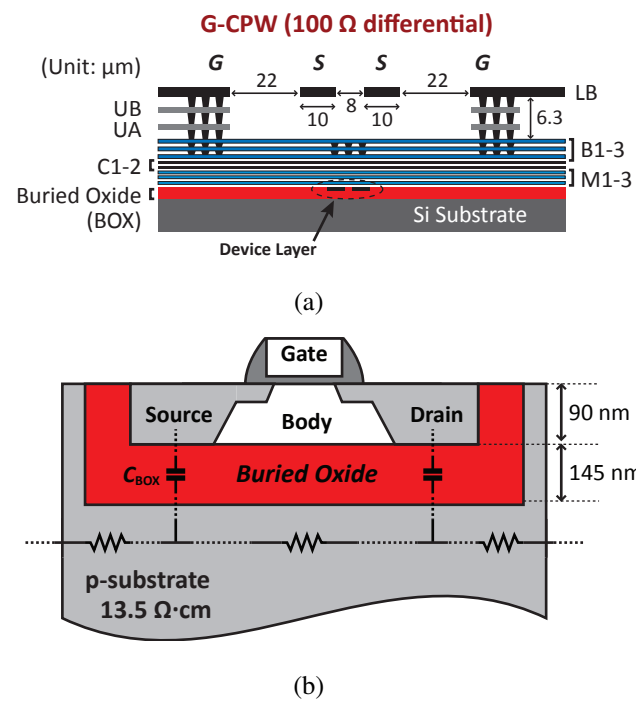


Figure 5.5: (a) Metal stack-up and (b) cross-section of IBM 45-nm SOI CMOS (12S0) technology.

(LB and UA) which has $4.25\ \mu\text{m}$ distance between each other. A full electromagnetic simulation is done using Sonnet [45] and differential-mode ensures a high isolation of $>60\ \text{dB}$ up to $60\ \text{GHz}$. Stacked ground plane on B3 and B2 layer covers the area underneath and isolates the interconnects between CMOS switches from vertical and horizontal lines. A series-shunt-series switch is used as a unit switching cell instead of a series switch in order to provide high isolation with a small penalty of $\sim 1\ \text{dB}$ higher loss at $30\ \text{GHz}$. The interconnects between NFET switches are laid out carefully to minimize the imbalance between (+) and (-) t-lines. The shunt switch remains small ($7\ \mu\text{m}$) to minimize the shunt capacitance when the unit switching cell is in pass-state. All CMOS switches are connected to a $20\ \text{k}\Omega$ resistor at the gate to make the gate node floating and hence improve the linearity. Also, an inverter is integrated in a unit switching cell to turn on/off the shunt switch in an opposite polarity of series switches.

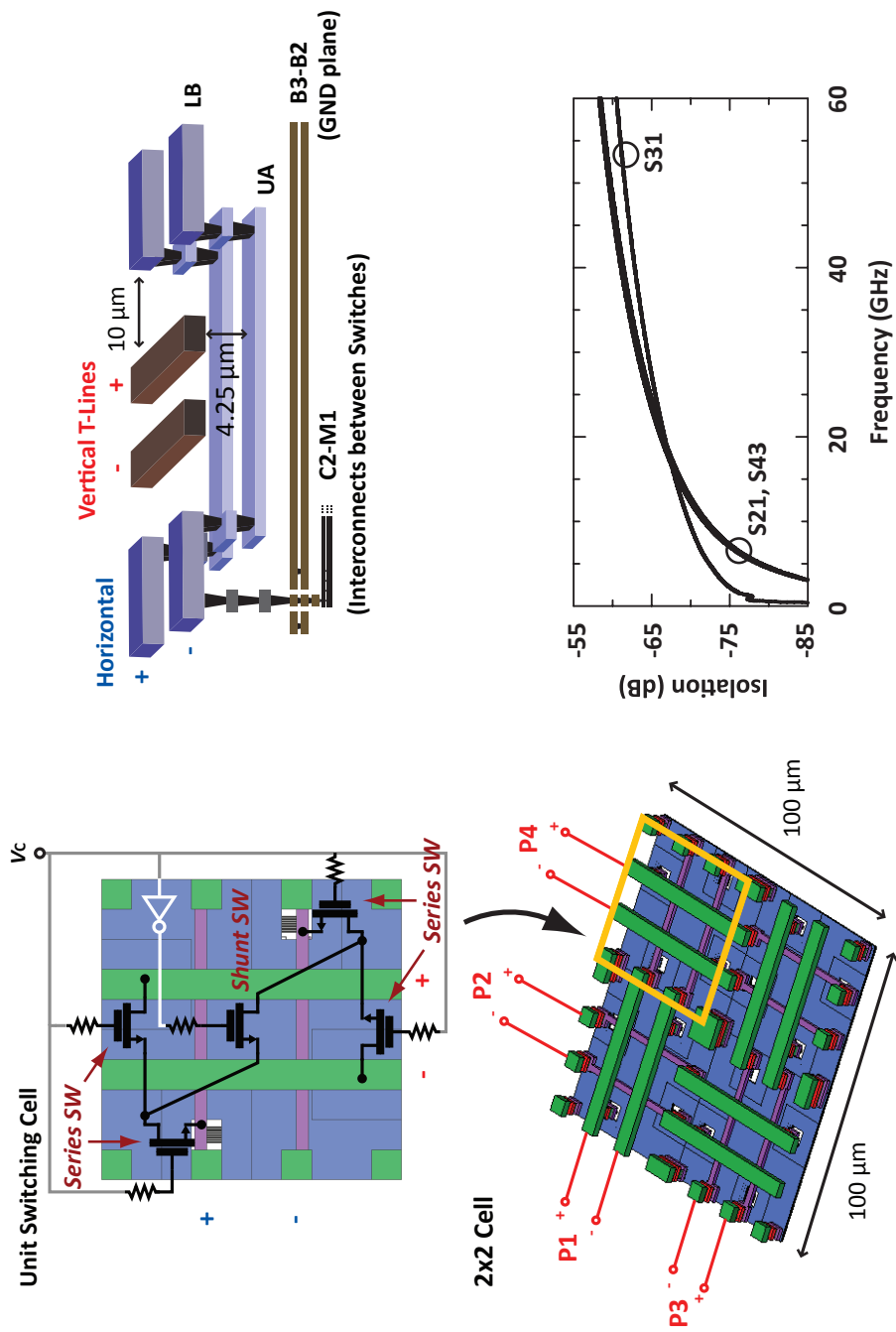


Figure 5.6: Layout structure of unit switching cell and 2×2 cell, and simulated isolation between ports of 2×2 cell.

A small dimension of a 2×2 cell is preferred in order to minimize the open-stub effect described on Section 5.2.1. $100 \times 100 \text{ } \mu\text{m}^2$ ensures both low open-stub effect and high isolation ($>55 \text{ dB}$ up to 60 GHz) between any two adjacent channels (Fig. 5.6). A parametric sweep of series switch width on simulation of 2×2 switching cell (W_{series}) is done at 20 GHz over insertion loss, isolation, and 3-dB bandwidth of a unit switching cell, and the optimum value of $40 \text{ } \mu\text{m}$ is chosen for the maximum 3-dB bandwidth (Fig. 5.7).

A 2×2 switch simulation including all the interconnect layout effects shows a 3-dB bandwidth $>24 \text{ GHz}$ and an isolation $>40 \text{ dB}$ up to 40 GHz (Fig. 5.8). Although a DC loss of 1.8 dB is shown it can be compensated by active buffers.

5.2.3 Bandwidth Extension using Inductive-Peaking Amplifier

Inductive peaking amplifiers can achieve a high bandwidth with low DC power consumption compared to distributed amplifiers [78–81]. An inductor is placed in parallel with output capacitance of transistor to provide a zero in load that compensates for the decreasing impedance at higher frequency (shunt peaking), or in series to separate the poles coming from the device output capacitance and from the following stage (series peaking). These two techniques can also be used at the same time (shunt-series peaking) to maximize the bandwidth enhancement ratio (BWER), which is the ratio of 3-dB bandwidth of the inductively compensated design to that of uncompensated case ($w_u = 1/RC$). BWER is determined by $m = L/R^2C$, which is the ratio of time constant of RL network (L/R) and RC network (RC) [79].

In order for the amplifier to be used in the matrix, it must 1) compensate for the higher loss of passive switches at the higher frequency, 2) not increase the group delay variation (GDV), and 3) be placed before every 2×2 cell so that scalability of the matrix design is maintained. The GDV is also an important factor on the broadband design since it dominates the timing jitter. Therefore, since a maximum BWER design introduces added GDV, the buffer design has to be optimized to get a large BWER and low group delay variation at the same time. The voltage gain of the amplifier can remain small ($<2 \text{ dB}$) only to compensate for the loss of switches. Fig. 5.9 shows the schematic of the buffer which consists of a common-source stage with shunt-peaking

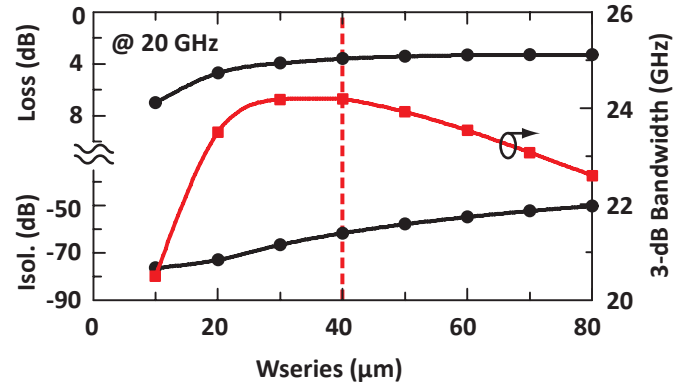


Figure 5.7: Optimization of 2x2 switching cell

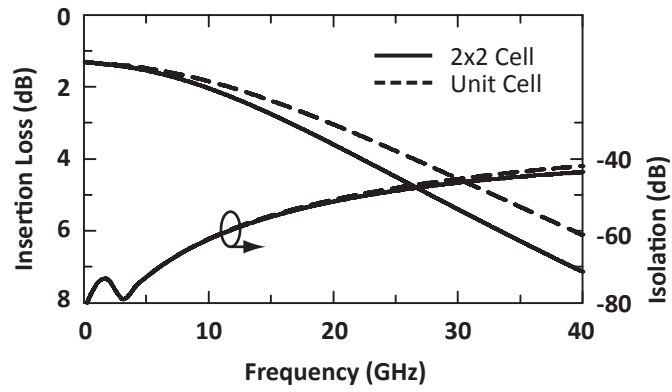


Figure 5.8: Simulated insertion loss and isolation of a unit cell and 2×2 cell.

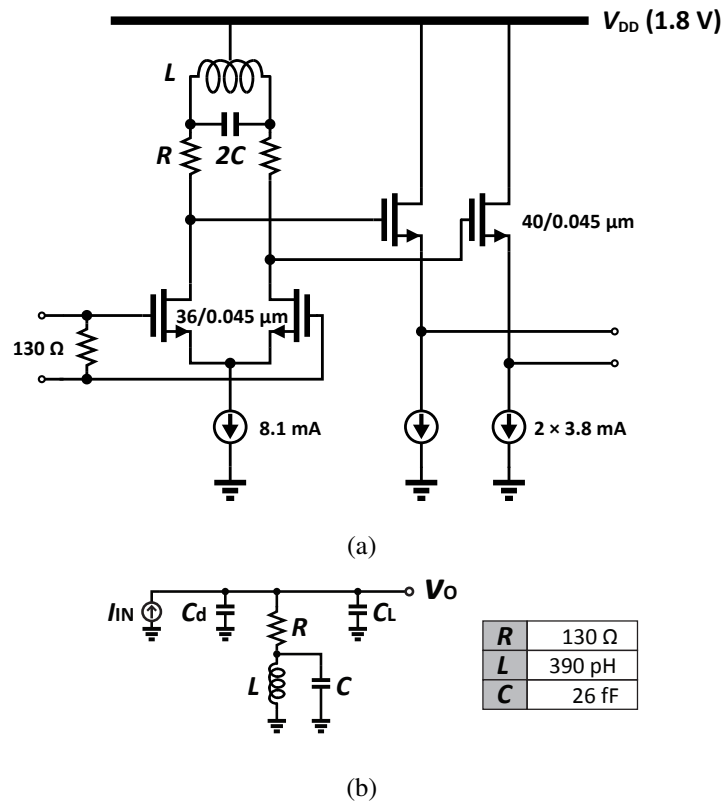
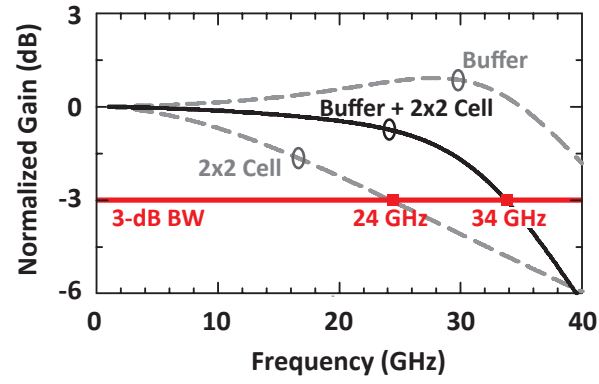
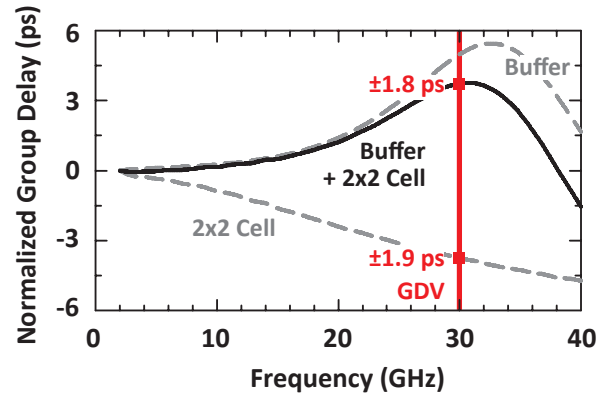


Figure 5.9: 3-dB bandwidth of switch matrices of different scales with and without isolation switches



(a)



(b)

Figure 5.10: Simulated (a) normalized gain and (b) normalized group delay vs. frequency for 2×2 cell alone, buffer alone, and 2×2 cell and buffer together.

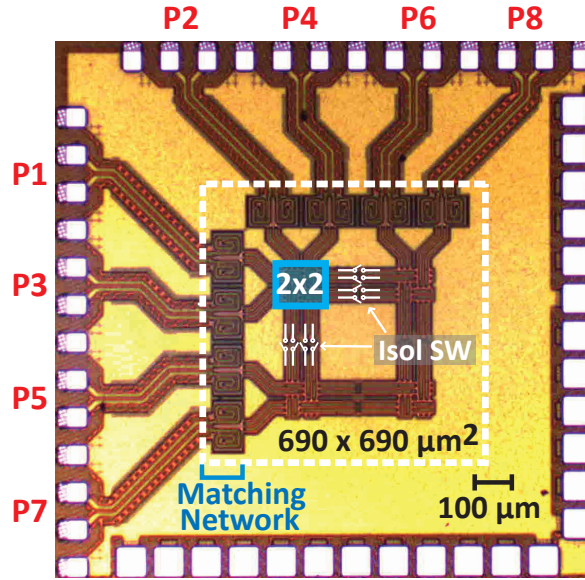
load and a source-follower stage. Source-follower stage is needed to provide a low output impedance and to level shift the buffer output node voltage because all circuit nodes are DC-coupled. The first stage dominates the frequency response since the source-follower creates a very high frequency pole far away from the dominant pole, and Fig. 5.9(b) presents the simplified small-signal model of the first-stage. Values of R and L decide the DC gain and a zero frequency, and also a small capacitor C is inserted in parallel with inductor L such that it creates an extra pole and a zero frequency and makes flatter gain response. A flatter response is preferred because otherwise when the signal passes by multiple buffers the overall response will result in an excessive peaking. In other words, the gain peaking of a buffer has to be large enough to compensate for the gain drop when a pass-state switch follows and small enough not to create a large peaking when isolation-state switch follows.

The R , L , and C values of $80\ \Omega$, $390\ \text{pH}$, and $26\ \text{fF}$ was chosen after optimization of gain and GDV when a buffer and a 2×2 cell are connected together (Fig. 5.10). The simulation results in a staggered response that extends the 3-dB bandwidth by 42 % ($24\ \text{GHz}$ to $34\ \text{GHz}$) and maintains the small group-delay variation of $<\pm 2\ \text{psec}$.

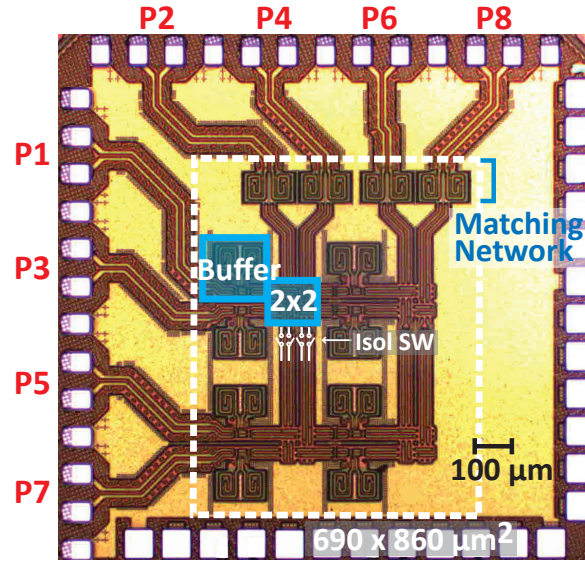
5.3 Measurements

Fig. 5.11 shows the microphotograph of two designs of 4×4 switching matrices: all-passive and passive-active designs. The chip dimensions of both designs are $1.4\times 1.4\ \text{mm}^2$. Note that the dimension is expanded to fit the dimension of $100\ \mu\text{m}$ -pitch GSSG differential pads. The active region is only $0.7\times 0.9\ \text{mm}^2$ and rest of the area is occupied by the transmission lines connecting the active region to the RF pads.

On-chip S-parameter measurement was done using Agilent N5242A PNA-X 4-port network analyzer which enables true differential measurement up to $26.5\ \text{GHz}$. Ground-signal-signal-ground (GSSG) RF probes were used at the input and output, and a short-open-load-thru (SOLT) calibration was done to place the reference planes to the probe tips. A parallel control signals of $1.0/0\ \text{V}$ for each unit cells are injected from the east and south DC pads. All-passive design includes passive switches and digital circuits, and hence consumes near-zero DC power. Passive-active design includes eight

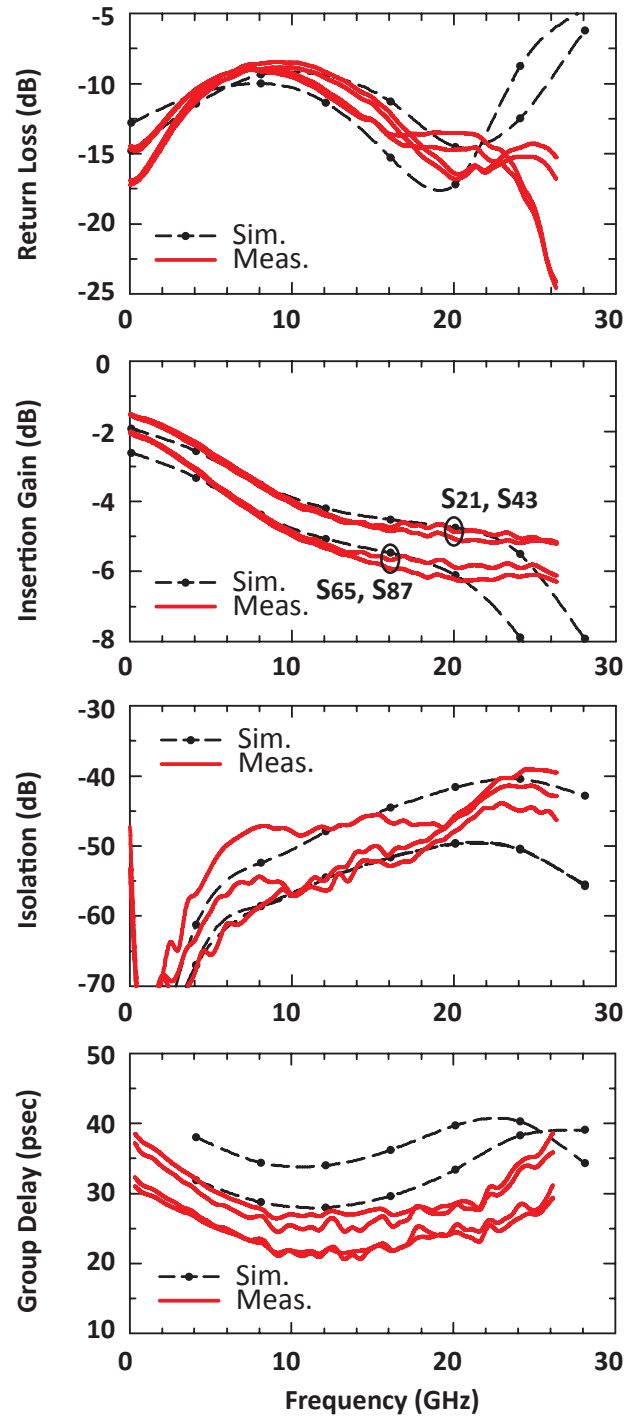


(a)



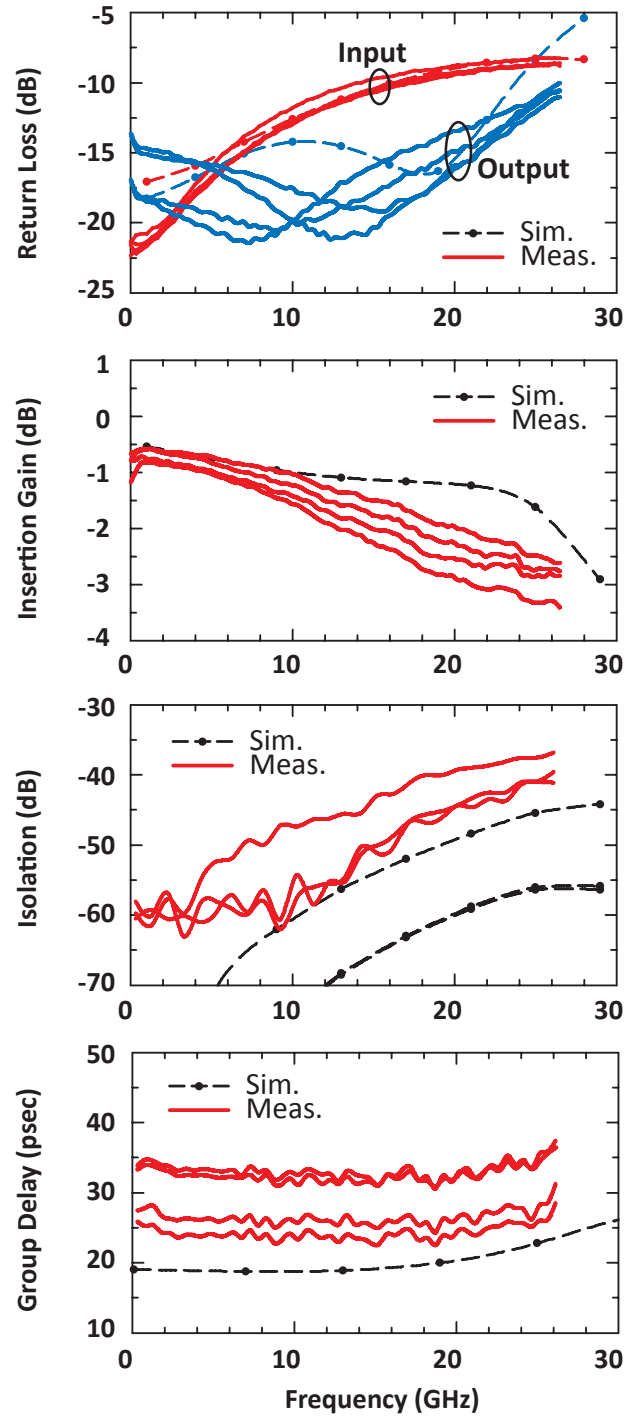
(b)

Figure 5.11: Microphotograph of (a) all-passive and (b) passive-active 4×4 switch matrices. The chip sizes are both $1.4 \times 1.4 \text{ mm}^2$



(a)

Figure 5.12: Measured and simulated return loss, insertion gain, isolation and group delay of (a) all-passive and (b) passive-active 4×4 switch matrix.



(a)

Figure 5.12: Measured and simulated return loss, insertion gain, isolation and group delay of (a) all-passive and (b) passive-active 4×4 switch matrix. (cont.)

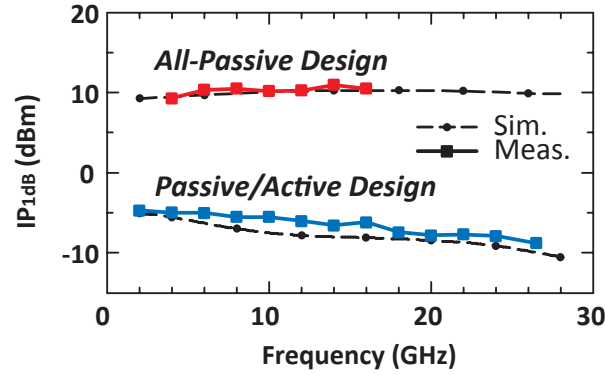
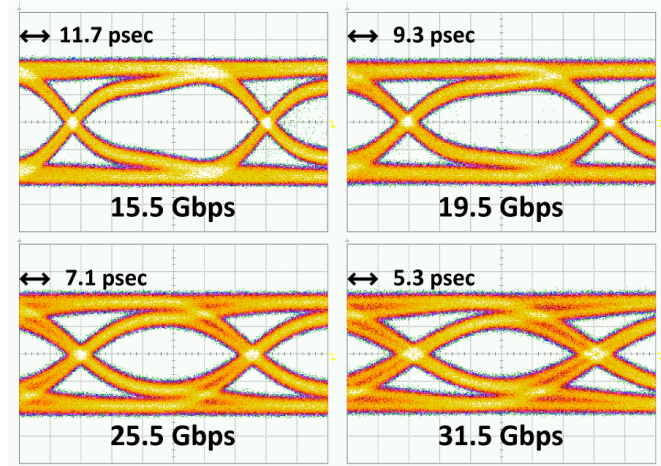


Figure 5.13: Measured and simulated input P_{1dB} of 4×4 switch matrices.

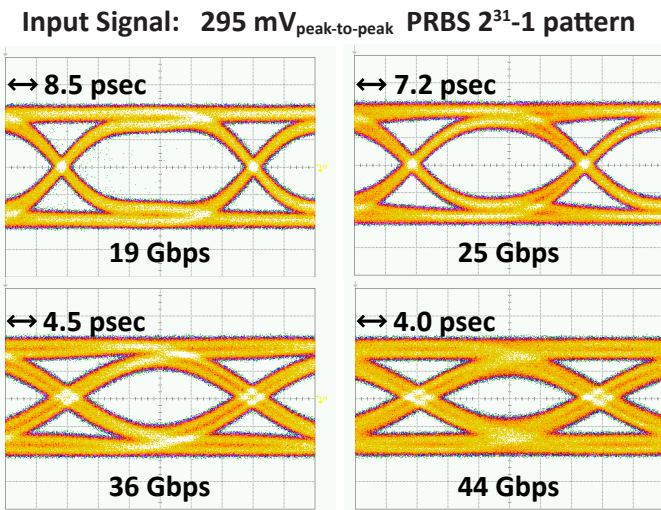
active buffers which are placed after every 2×2 cells. Each active buffer consumes 15.7 mA from 1.8 V supply. Therefore, the total dc power consumption of a passive-active 4×4 switching matrix is 241 mW.

Fig. 5.12 presents the measured and simulated S-parameters of two designs of 4×4 switching matrix. The return loss is less than 8 dB up to 26.5 GHz at both input and output for both of the designs. The insertion losses shown are S_{21} , S_{43} , S_{65} and S_{87} when P1-P2, P3-P4, P5-P6, and P7-P8 are connected. The insertion loss of all-passive design is 5-6 dB at 20 GHz depending on the signal path. There are differences between S_{21} , S_{43} and S_{65} , S_{87} because isolation switch adds ~ 1 dB of loss. The 3-dB bandwidth is 20-25 GHz, which enables ~ 30 Gbps of signal transmission. The passive-active design results in the insertion loss of 2.0–2.9 dB at 20 GHz for four different paths and the 3-dB bandwidth is more than 26.5 GHz (32 GHz in simulation) as a result of active buffers. The measured gain is approximately 1 dB lower than simulation at 20 GHz due to inaccurate modeling of CMOS switch in high frequency.

The isolation plots are presenting the S_{41} , S_{61} and S_{81} when P1-P2, P3-P4, P5-P6, and P7-P8 are connected, which shows the measured isolation more than 38 dB up to 26.5 GHz for both designs. However, since it is not possible to terminate port 2 with 50Ω load when measuring the isolation at ports 4, 6, or 8, the isolation measurement shows some ripple as a result of reflection from the open circuit port. This effect and an inaccurate switch model account for the discrepancy between simulation and measurement.



(a)



(b)

Figure 5.14: Measured eye diagrams of (a) all-passive and (b) passive-active 4×4 switch matrices for PRBS input signals of different data-rates.

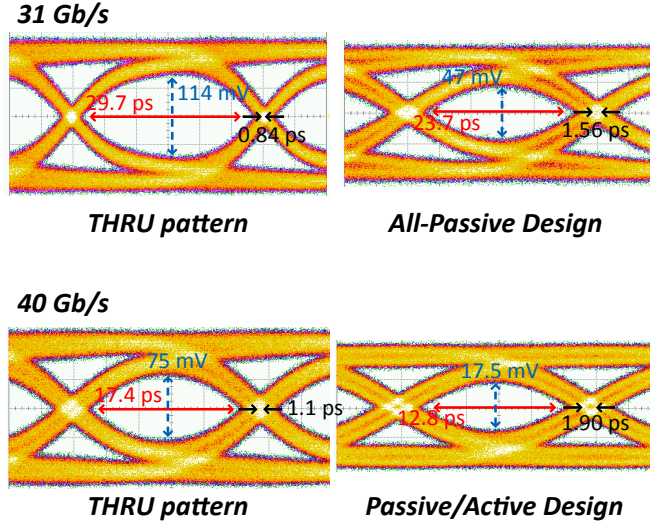
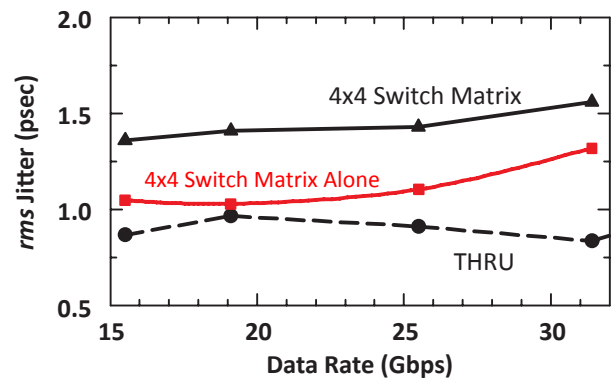


Figure 5.15: Comparison of eye diagrams of out of THRU pattern and switching matrices.

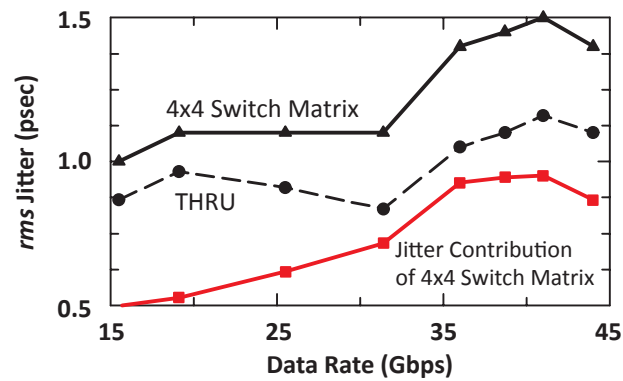
The measured group delay of all-passive design is 20-30 psec (± 5 psec) from DC to 26.5 GHz. For passive-active design, active buffers also help reducing the group delay variation as described on Section 5.2.3. The resulting group delay variation is less than ± 2 psec regardless of the signal path which is enough to transfer 40 Gbps signal with low horizontal variation in the eye diagram.

The P_{1dB} of the matrix is measured to show the large-signal characteristic (Fig. 5.13). The all-passive design shows the measured P_{1dB} of ~ 10 dBm up to 18 GHz. It is limited by the power-handling of SOI CMOS switches. The P_{1dB} of passive-active design is limited by the buffer which has IP_{1dB} of ~ -6 dBm at 20 GHz. The measured IP_{1dB} of the passive-active 4×4 switching matrix is -5 to -9 dBm from 2 to 26.5 GHz. The power handling gets smaller as the frequency goes higher as a result of higher voltage swing at the inductor load of the shunt-peaking buffer.

In order to verify the signal integrity of the signal passing through the switch matrix, the eye diagram of 4×4 switching matrix is tested using an Agilent 86100A DCA wide-bandwidth sampling oscilloscope. A differential 19-44 Gb/s pseudo-random binary sequence (PRBS) pattern of $2^{31}-1$ is generated from a Centellax TG1P4A pulse pattern generator with an input peak-to-peak voltage of 295 mV. The input voltage swing is adjusted by coaxial attenuator not to inject power-level beyond power-handling capa-



(a)



(b)

Figure 5.16: Measured RMS jitter for THRU pattern, and (a) all-passive and (b) passive/active 4×4 switch matrices.

bility of the DUT. The measured eye diagram shows good eye openings for all-passive design up to 31.5 Gbps. Passive-active design achieves good openings up to 44 Gbps as a result of higher bandwidth (Fig. 5.14). Passive-active design shows also cleaner (lower jitter) eye diagrams than all-passive design which seems to be as a result of lower group delay variation of passive-active design.

The digital sampling scope shows the jitter components from the measured eye diagram but these values are not from the DUT alone. The measurement setup requires bias-tees at the input and output of the switching matrix and attenuators at the input to adjust the input power. These additional components and RF cables between DUT and measurement instrument generate jitter by reflections and frequency cut-offs. In order to quantify the jitter contribution of the 4×4 matrix alone, a THRU pattern from GGB CS-5 calibration substrate is probed and tested on the same measurement setup. Then the measured pattern will be the smallest jitter that can be measured for the given system. As shown from Fig. 5.15, for 40 Gbps signal from pattern generator, THRU pattern result in *rms* jitter of 1.1 psec, whereas passive-active switching matrix shows more noisy eyes and *rms* jitter of 1.9 psec. Assuming that the jitter from the system and matrix is uncorrelated, the RMS jitter contribution of the 4×4 switch matrix is less than 0.9 psec. 5.16 shows the estimated *rms* jitter component of 4×4 switching matrix alone, which is less than 1.0 psec up to 44 Gbps.

5.4 Conclusion

This paper presented all-passive and passive-active 4×4 switching matrices using advanced 45-nm SOI CMOS. A cross-point architecture with passive CMOS switch was used to achieve switching with near-zero power consumption. Scalability of all-passive design is maximized by introducing isolation switches placed after every 2×2 switching cells. A inductive-peaking buffers are used on passive-active design in order to further increase the bandwidth of the matrix. The eye-diagram measurement shows that all-passive design can route signals up to 30-Gbps of data-rate and passive-active design can achieve up to 44-Gbps. The scalability of passive-active design maintains constant 3-dB bandwidth up to more than 12×12 matrix. This design is expected to be

a good candidate to replace the existing multiplexer-based switching matrices for low power design.

5.5 Acknowledgment

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- Donghyup Shin and G. M. Rebeiz, “A Scalable Low Power >40 -Gb/s 4×4 Switch Matrix in 45-nm CMOS,” to be submitted to *IEEE J. Solid-State Circuits*.
- Donghyup Shin and G. M. Rebeiz, “A 32-Gbps 4×4 Passive Cross-Point Switch in 45-nm SOI CMOS,” in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, June 2013.

Chapter 6

Conclusion

This thesis presented packaged X-band phased-array transmitter and receiver, and high data-rate switching matrices using advanced CMOS processes. CMOS integrated circuit of 9-10 GHz phased-array receiver and transmitter was designed and measured. In addition, packaging of the phased-array chips on teflon board was demonstrated and characterized intensively, especially on the coupling between channels. Also, CMOS switching matrices for high data-rate using cross-point architecture which consumes very low dc power was implemented.

In chapter 2, a high-linearity, 4-element X-band phased array was demonstrated using 0.13 μm CMOS technology. A single-ended design was used and optimized architecture results in low power consumption, and low noise figure. The measured on-chip coupling is very low (< -40 dB) and does not degrade the performance of phased-array operation. The phased-array chip was then mounted on a Teflon substrate using bond-wires. Simulations and measurements show that with high isolation bond-wire design, the channel-to-channel coupling (~ -31 dB at 9.5 GHz) is determined by the overall ground inductance, and results in ~ 0.15 dB and 0.9° of additional *rms* amplitude and phase error. This work shows that one can use chip-on-board packaging for X-band silicon phased arrays with a large number of input channels.

Chapter 3 presented a 4-element high-power phased-array transmitter capable of operation in a communication or a radar mode. It is found that the vector modulator phase shifter and the power amplifier result in phase distortion vs. power but these can be calibrated out in radar mode operation. For communication systems, it is best to operate

below the output P_{1dB} level for complex constellations. The chip has been packaged using chip-on-board (CoB) and QFN techniques, and the CoB results in higher ultimate isolation between the channels (-45 dB) as opposed to the QFN (-35 dB). However, both result in nearly the same isolation between the neighboring channels ($\sim$ -30 dB) which is primarily limited by bond-wire coupling. This work shows that complex phased-arrays with multiple channels can be packaged in low-cost QFN packages for X-band applications.

Chapter 4 presented a 0.01-8 GHz 4×4 CMOS switch matrix with low insertion loss and high isolation. The CMOS switch matrix consumes $\sim$ 0 mW, has high linearity and adequate power handling for receive systems and backplane switching networks. The switch matrix can be scaled to a larger number of ports and higher frequencies using advanced CMOS nodes. Furthermore, the designs can be extended to differential circuits which are less sensitive to ground inductance and are compatible with backplane data networks. This work showed a possibility of high data-rate switching matrix using passive CMOS switches.

Chapter 5 presented all-passive and passive-active 4×4 switching matrices using advanced 45-nm SOI CMOS. A cross-point architecture with passive CMOS switch was used to achieve switching with near-zero power consumption. Scalability of all-passive design is maximized by introducing isolation switches placed after every 2×2 switching cells. An inductive-peaking buffers are used on passive-active design in order to further increase the bandwidth of the matrix. The eye-diagram measurement shows that all-passive design can route signals up to 30-Gbps of data-rate and passive-active design can achieve up to 44-Gbps. The scalability of passive-active design maintains constant 3-dB bandwidth up to more than 12×12 matrix. This design is expected to be a good candidate to replace the existing multiplexer-based switching matrices for low power designs.

Appendix A

2×2 and 4×4 CMOS Switching Matrices for 0.01–12 GHz Applications

A.1 Introduction

Switching matrices are an important circuit block in satellite communications, reconfigurable radios and base stations, and are commonly implemented using mechanical relays. The relays provide very low loss high linearity and power handling, and therefore, can be used after the RF power amplifiers. However, this results in a large system and with limited lifetime since the mechanical relays typically have a lifetime of 10⁵-10⁶ cycles.

This paper explores the use of CMOS switches as high performance switching matrices. In this application, the CMOS switches are placed before the power amplifiers (in the transmit mode) and after the low noise amplifiers (in the receive mode). In this case, the isolation and linearity of the CMOS switch matrix are of utmost importance, followed by a reasonable insertion loss and power handling capabilities. It is seen that complex switching matrices can be built using standard 0.13 μm CMOS for 0.01-12 GHz applications and with good performance.

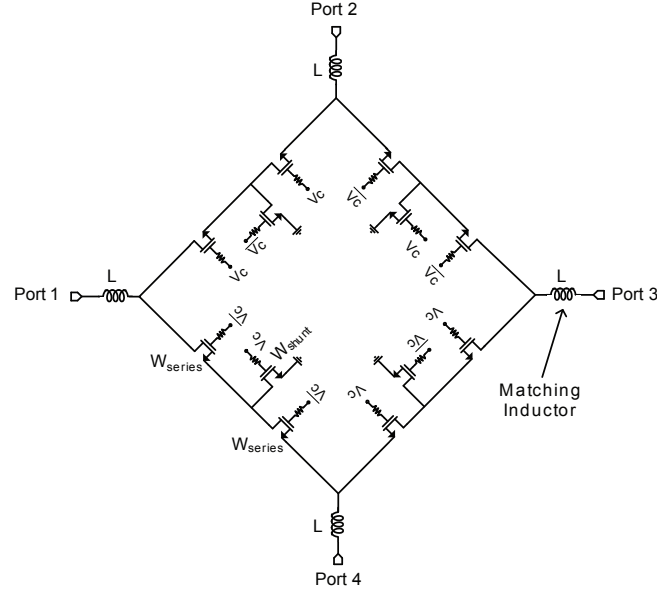


Figure A.1: Schematic of 2×2 switching matrix.

A.2 2×2 and 4×4 Switching Matrix: Design

Fig. A.1 presents the layout of a 0.01-12 GHz 2×2 switching matrix, commonly called a transfer matrix or a double-pole-double-throw switch (DPDT). In this case, ports 1 and 3 are connected to ports 2 and 4 or ports 4 and 2, depending on the control voltage. In order to get wideband performance and high isolation, a series-shunt-series design is placed in every path. Also, inductors are used at the 4 RF ports in order to result in a wideband match to 12 GHz.

The transistors are based on the deep n-well technology which enables the minimization of the capacitance between the body and the substrate without any latch-up problems. The transistor body and n-well are tied to ground and V_{DD} , respectively, using $R_w = 20 \text{ k}\Omega$ to eliminate any RF leakage. A high substrate resistance of $1 \text{ k}\Omega$ is used to reduce the RF loss through the junction capacitances, C_J . The high R_{SUB} is realized by adopting very small substrate contacts ($0.8 \times 0.8 \text{ }\mu\text{m}^2$) close to the nMOS transistor. The transistors are surrounded with deep trenches that isolate the transistor active area from the substrate. The deep trench has a depth of $6 \text{ }\mu\text{m}$, and increases the resistance between the junctions of two nMOS transistors, thus also improving the isolation between the ports.

Figure 10 is a graph showing the relationship between Series FET width (um) and Insertion Loss (dB) and Isolation & Return Loss (dB). The x-axis represents Series FET width (um) from 100 to 300. The left y-axis represents Insertion Loss (dB) from -1.5 to -0.6. The right y-axis represents Isolation & Return Loss (dB) from -15 to -35. Three curves are plotted: Return Loss (solid line, decreasing from -0.6 to -0.7 dB), Isolation (dashed line, increasing from -1.5 to -0.9 dB), and Insertion Loss (dash-dot line, increasing from -1.2 to -0.8 dB). Arrows indicate the direction of increasing width for each curve. A note specifies @ 12 GHz, $W_{\text{shunt}} = 110 \mu\text{m}$.

Figure A.2: (a) Circuit model of series-shunt-series cell and (b) simulated insertion loss, isolation and reflection coefficient of a series-shunt-series cell at 12 GHz versus series FET width.

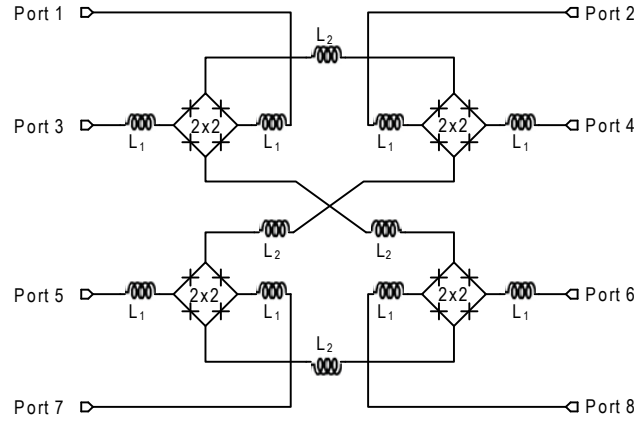


Figure A.3: Block diagram of 4×4 switching matrix.

An optimization was done in order to determine the best transistor sizes. Fig. A.2(a) shows the full model of the series-shunt-series cell together with all the parasitic capacitances and resistances. Fig. A.2(b) presents the insertion loss, isolation and reflection coefficient as a function of the series transistor width. This was done for several shunt transistors, and Fig. A.2(b) is for a shunt transistor width of $110 \mu\text{m}$. The simulation in Fig. A.2 is done at 12 GHz. As expected, increasing the series transistor width results in a better insertion loss but at the expense of worse isolation and matching. Also, the substrate resistance is not well known and increasing the series transistor width results in additional losses due to power loss in the substrate (coupled to the substrate resistance through the device capacitance).

A final design consisting of series and shunt transistors of width 130 and $110 \mu\text{m}$, respectively, was chosen. This, together with 270 pH matching inductors at the RF ports ($Q=11$ at 12 GHz) results in an insertion loss of < 2.5 dB at 12 GHz, an isolation > 30 dB at 12 GHz excellent match (< -13 dB at 12 GHz). The 4×4 switching matrix is based on the 2×2 cell as shown in Fig. A.3, and with several additional matching inductors. The series and shunt transistors are the same width as before ($W_{\text{Series}}=130 \mu\text{m}$, $W_{\text{Shunt}}=110 \mu\text{m}$), and the matching inductors are optimized to result in a wideband match to 12 GHz with $L_1=270$ pH ($Q=11$ at 12 GHz) and $L_2=540$ pH ($Q=16$ at 12 GHz). The simulated insertion loss, isolation and reflection coefficient of the 4×4 switching matrix are 4.5, 35, 15 dB, respectively, at 12 GHz. Again, part of the insertion loss is due to the transistor substrate resistance (see Fig. A.2(b)).

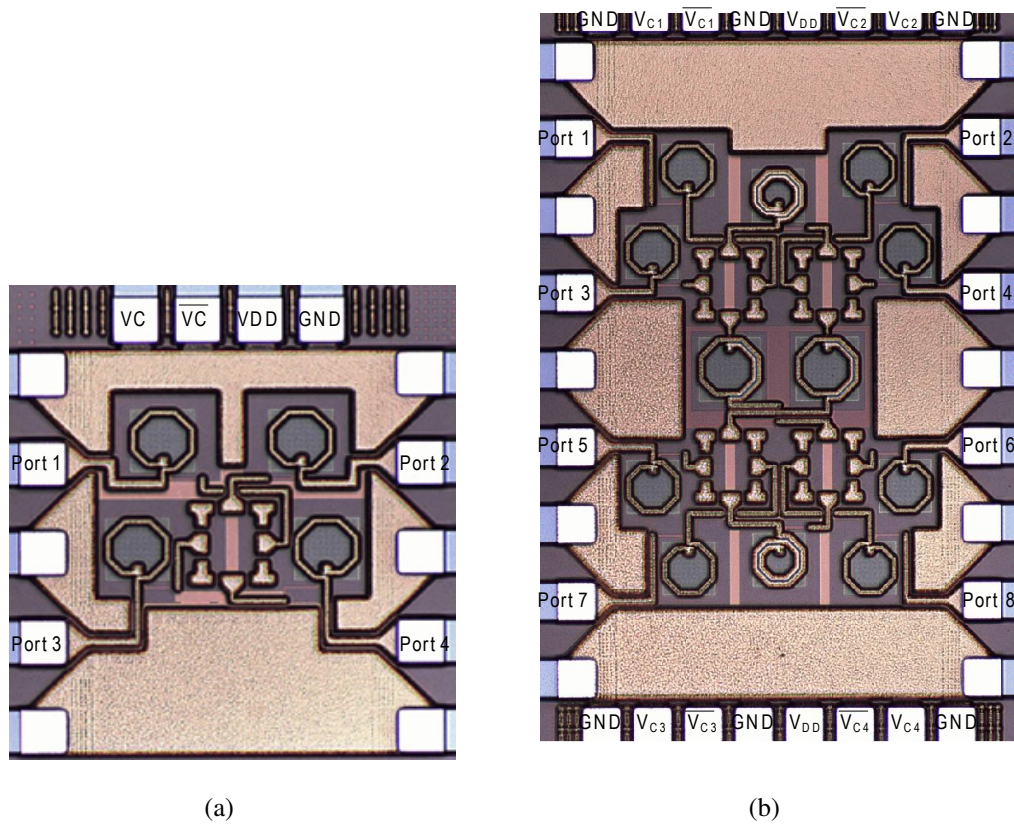


Figure A.4: Micro-photograph of (a) 2×2 and (b) 4×4 switching matrix.

A.3 Implementation

The 2×2 and 4×4 switching matrices chip are implemented in the IBM 8RF process with 7 metal layers. This process has $0.13 \mu\text{m}$ CMOS transistors (f_T of 90–100 GHz). Grounded CPW transmission lines are used with dimensions of $11/12/11 \mu\text{m}$ for 50Ω and with an estimated loss of 0.18 dB/mm at 10 GHz. Standard IBM transistor cells and resistor models (for gate biasing) are used, and full electromagnetic modeling is done on the transmission-lines using Sonnet [45]. The input and output CPW pads are designed to be 50Ω and are included in the simulations.

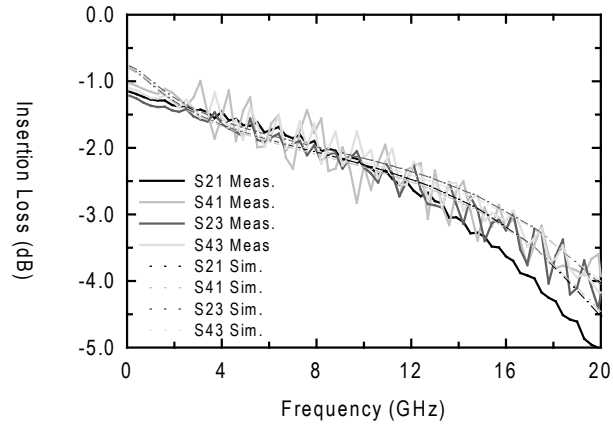
The IBM model does not include accurate substrate resistance values which depend on the transistor layout, substrate contracts and deep trench isolation. These values were obtained using fitting with the measured data. The fabricated 2×2 and 4×4 switching matrices occupy 0.66 and 1.44 mm^2 , respectively, including pads. The chips do not consume any current and operate from a 1.5 V supply (Fig. A.4).

A.4 Measurements

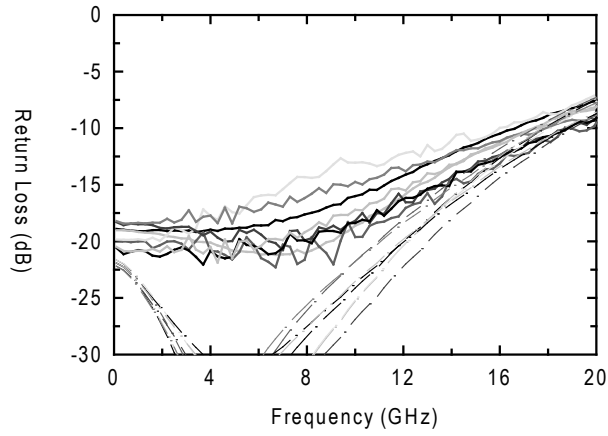
The measured S-parameters of the 2×2 switching matrix are presented in Fig. A.5. Measurements are done on-chip after a probe-tip SOLT calibration, and include the CPW input and output pad losses. The channels are well balanced and show an insertion loss and an isolation of $< 2.5 \text{ dB}$ and $> 38 \text{ dB}$ up to 12 GHz, and agree well with simulations. The measured S_{NN} is $< -15 \text{ dB}$ up to 12 GHz, but the simulated dip in S_{NN} at 4-8 GHz is not seen. This could be due to the finite substrate size and additional parasitic inductance.

The measured S-parameters of the 4×4 switching matrix are presented in Fig. A.6. In this case, two out of the four ports at the input and output are terminated with a GSGSG probe, while the other ports are left open-circuited. This has no effect on the insertion loss or matching due to the high isolation of the 2×2 switching matrix cell, but does have a minor effect on the measured isolation, especially at high frequencies.

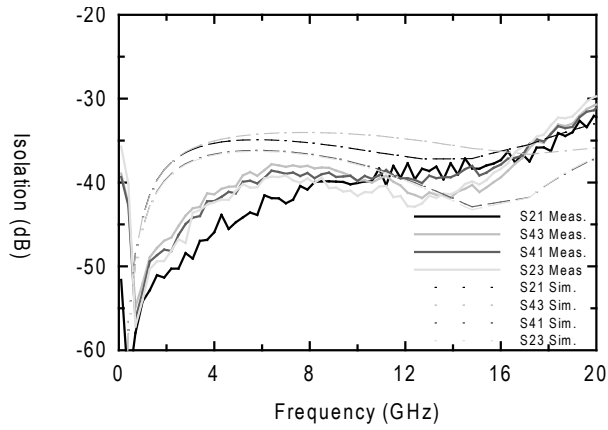
The measured insertion loss is $4.0 \text{ dB} \pm 0.3 \text{ dB}$ over many different port combinations and agrees well with simulations. The measured S_{NN} for port 3 when connected to ports 2, 4, 6, 8 are also shown. In general, S_{NN} is $< -12 \text{ dB}$ up to 12 GHz for any



(a)

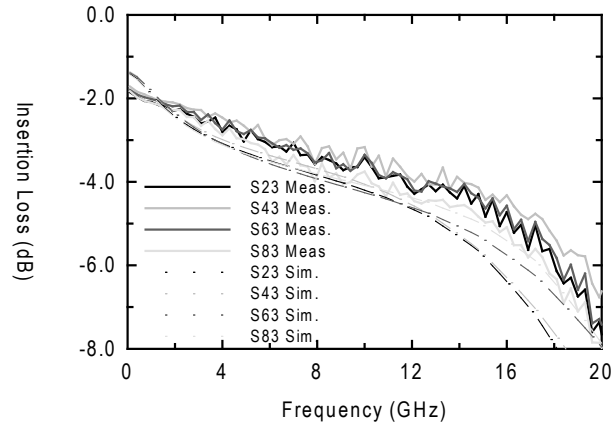


(b)

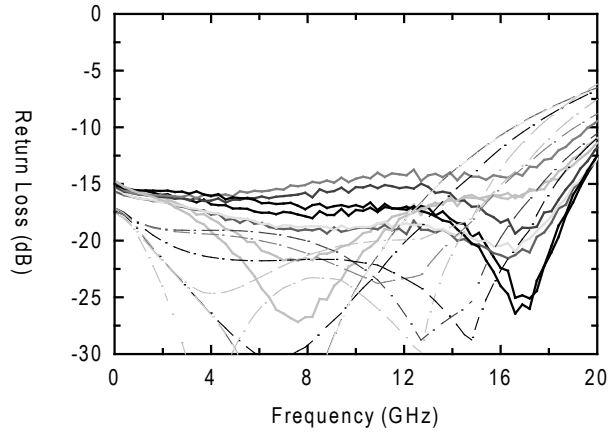


(c)

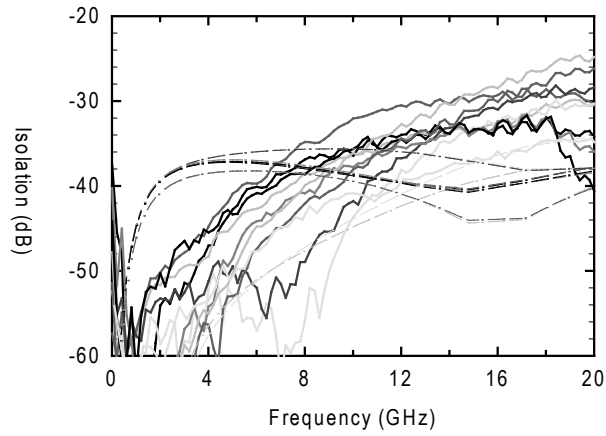
Figure A.5: Measured (solid) and simulated (dashed) insertion loss, return loss, and isolation of 2×2 switching matrix.



(a)



(b)



(c)

Figure A.6: Measured (solid) and simulated (dashed) insertion loss, return loss, and isolation of 4×4 switching matrix.

connection between the input and output ports, with some being < -15 dB over the entire frequency range. The measured isolation is shown in Fig. A.6 and is 35 ± 5 dB at 12 GHz. The variation is due to the non-terminated ports, coupling through the on-chip inductors, and coupling through the substrates. This is currently being investigated.

Finally, P_{1dB} and IP_3 measurements were done at 2, 6 and 12 GHz, and resulted in a P_{1dB} and IP_3 of 11 ± 1 dBm and 31 ± 1 dBm, respectively. This is similar to other series-shunt implementation in this technology.

A.5 Conclusion

This paper showed that 2×2 and 4×4 switching matrices are viable in CMOS switching networks and result in relatively low insertion loss and very high isolation up to 12 GHz. The 4×4 switching matrix can be improved in the future with further optimization.

A.6 Acknowledgment

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