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Experimental Evidence for the Impact of Copper Microstructure on Residual Stress of Through Silicon Via

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Three-dimensional integrated circuits (3DIC) with Cu through silicon vias (TSVs) offer improved system performance beyond front-end-of-line scaling. However, the residual thermal stress imparted by TSVs on the surrounding silicon raises reliability concerns. This stress is dependent upon the mechanical properties of Cu, which are dependent on its underlying microstructure owing to the metal's anisotropic modulus. Smaller TSVs magnify this microstructural effect due to the increased grain-to-via diameter ratio. Here, we experimentally quantify the impact of Cu-microstructure on the TSV-induced residual stress within silicon. A 3- μm TSV array was annealed at 400°C for 60 min, and the residual stress in the surrounding Si was imaged with Raman spectroscopy at room temperature. The Cu surface microstructure was characterized with electron backscatter diffraction (EBSD) to deduce the microstructure dependent elastic modulus. Mean Si residual stress increased with the out-of-plane elastic modulus of Cu, which varies by $2\times$ with the grain structure, and the microstructural influence diminishes with increasing distance from the TSV. Together, these findings provide direct experimental evidence linking copper microstructure to the residual stress within the Si near a TSV, an effect that becomes increasingly prominent with the continued TSV scaling.

I. INTRODUCTION

The demand for high efficiency and low energy cost in applications such as artificial intelligence and high performance computing continues the push for higher performing modern microelectronics¹. However, with the shrinkage of transistor size towards the atomic scale, limits both physical and economic have slowed front end of line (FEOL) scaling¹. Innovation beyond the FEOL are needed to accelerate the post-Moore era. Three-dimensional integrated circuits (3DIC) provide a promising path, as it improves system performance on the package level without further scaling in FEOL².

A through silicon via (TSV) is a vertical metal interconnect embedded into the Si itself. For 3DIC, TSVs are crucial, enabling vertical signal transmission and power delivery through Si dies. This boosts system performance by increasing interconnect density and reducing latency by shortening the signal path. TSVs also allow heterogeneous integration of separately manufactured known-good dies (KGDs) that reduce footprint and improve cost efficiency². The pursuit for ultra high bandwidth in advanced memory applications and high-density interconnect in backside power delivery continue to drive the further scaling of TSV size to 1 μm and below³.

Despite the benefits TSVs provide, thermomechanical reliability issues arising from coefficient of thermal expansion (CTE) mismatch is an inherent challenge of the heterogeneous system^{4,5}. TSVs are multi-layer structures made of a metal pillar (usually Cu) embedded into

Si and surrounded by adhesion layer, anti-diffusion barrier, and dielectric insulator^{6,7}. The CTE of Cu is six times that of Si, however. Thermal stresses ultimately causing structural failure can, therefore, develop both during the fabrication and operation of 3DICs employing TSVs^{2,8,9}. Moreover, thermal stress affects Si's mobility and thus circuit performance owing to the semiconductor's piezoresponse¹⁰. It is, therefore, vital to understand the characteristics governing the TSV-induced stress so that designs and processes can be developed mitigating the impact of the inherent CTE mismatch.

For larger TSVs ($\geq 10\mu\text{m}$), stress can be well described with isotropic models^{11–17}, where the mechanical properties of Cu are assumed to be independent of its microstructure. An isotropic response of the metal core, in turn, results in identical stress profiles from one TSV to the other. Despite the highly anisotropic properties of single crystal copper¹⁸, the isotropic assumption is valid for large-sized TSVs because at this scale each TSV possesses hundreds of randomly-oriented grains. The large-ensemble of randomness “adds up” to a quasi-isotropic response¹⁹. However, as size of TSV scales down, Cu grain size becomes comparable to the TSV diameter²⁰. When this occurs, there are no longer enough grains to “average out” all directional dependence from the anisotropic response intrinsic to the material²¹. With the continued scaling of TSV, the grain structure of Cu will have, therefore, a more pronounced impact on the TSV-induced thermal stress.

The anisotropic behavior of Cu TSVs have been previously investigated both experimentally and computationally underscoring how variation in the Cu-microstructure could impact the stress induced by the TSVs^{19,21–29}. Electron backscatter diffraction (EBSD), for example,

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images the Cu grain structure within the TSVs providing a foothold linking microstructure to variations in mechanical properties^{23,24}. Nanoindentation, meanwhile, has directly quantified the microstructure dependent change in elastic modulus within the cross section of the Cu within a TSV.²⁸ This knowledge has been leveraged computationally to assess the implications of this microstructural dependence on the thermal stress within the TSV and the surrounding silicon. Finite element analysis (FEM)^{22,26}, phase field method^{21,25}, technology computer-aided design (TCAD)²⁸, and crystal plasticity finite element (CPFE) method²⁷, have each been used to assess the thermomechanical response of polycrystalline Cu TSV, consistently demonstrating the non-trivial impact of Cu-microstructure on thermal stress.

Even as Cu-microstructure is known as a direct determinant of the thermomechanical response direct experimental measurements linking silicon stress to the copper microstructure remains lacking. Recognizing this, we experimentally studied the impact of Cu-microstructure in a TSV on the resulting residual stress within the surrounding silicon. Practically, a 3- μm diameter TSV sample was annealed at 400°C for 1-hour, and residual stress within the surrounding Si was imaged with Raman spectroscopy at room temperature. The resulting stress images within the silicon were compared to the variation in effective elastic modulus of the polycrystalline Cu-cores deduced from the microstructure imaged with EBSD. By correlating Raman-imaged TSV stress with Cu grain structure, we provide direct experimental evidence highlighting the impact of Cu-microstructure on TSV-induced thermal stress in silicon showing a direct correlation between silicon stress and the effective out-of-plane modulus of Cu.

II. MATERIALS AND METHODS

TSV arrays with a diameter of 3 μm , a height of 21 μm , and pitches ranging from 6 μm to 12 μm were fabricated on a $1 \times 1 \text{ cm}^2$ Si substrate with a thickness of 525 μm . The TSV array was first patterned with photolithography and etched with deep reactive ion etching (DRIE). A 15-nm SiO_2 insulator was then deposited with plasma enhanced atomic layer deposition (PEALD), followed by physical vapor deposition (PVD) sputtering of 100-nm Ta barrier and 300-nm Cu seed. The deep trench was then filled with electroplated copper. Chemical mechanical polishing (CMP) was performed to remove the excessive copper on the top surface and reveal the Si/ SiO_2 substrate. The detailed fabrication process flow and process optimization can be found in our previous paper^{30,31}. Figure 1 shows both top views of polished TSV arrays accompanied by a scanning electron microscope (SEM) image of TSV cross sections prepared using a focused ion beam (FIB).

The TSV arrays were then thermally annealed at 400°C for one hour in a high-temperature furnace purged

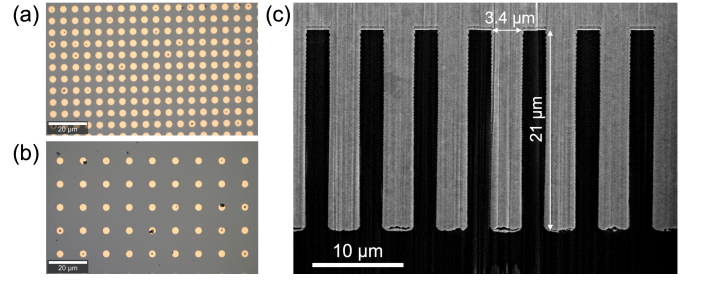


FIG. 1. Fabricated 3- μm Cu TSV array. Optical microscope images of polished top surface of TSV arrays with (a) a 6- μm pitch and (b) a 12- μm pitch. (c) SEM/FIB image of TSV cross section with a opening of 3.4 μm and a height of 21 μm .

with forming gas (98% nitrogen and 2% hydrogen). Another CMP step was performed after annealing to remove Cu-protrusion and improve the smoothness of the top Cu surface, enabling high-quality characterization of Cu-microstructure with EBSD. The grain structure of TSV array was then imaged on the top surface with electron beams at 20 kV and 0.4 nA and a step size of 150 nm.

Microstructural data obtained with EBSD was post-processed with AZtec Crystal software, which reduced the noise and provided pixel-level determination of grain orientation (see Figure 2a). In practice, the pixels of copper were segmented into grains with a misorientation criterion of $<10^\circ$ by a Python script (see Figure 2b). The elasticity matrix of each grain was then determined by its crystal orientation using an algorithm adopted from the study of Zhang et al.²³. With the elastic modulus of each grain determined, the effective elastic modulus of each Cu core was evaluated by volume-weighted average derived from the individual Cu grains' elasticity matrix, using Hill's averaging method³².

$$C_{\text{mean}} = \frac{1}{2} \left(\sum f_i C_i + \left(\sum f_i S_i \right)^{-1} \right) \quad (1)$$

where C_{mean} is the average stiffness matrix of the Cu core, C_i and S_i are the stiffness matrix and the compliance matrix of i -th grain, and f_i is i -th grain's volume fraction estimated using equivalent grain diameter. Figure 2c shows the histogram of effective out-of-plane Young's modulus deduced from the EBSD analysis for 187 separate TSVs, where a variation of 2x is observed spanning from 80 GPa to 160 GPa.

Residual stress within the Si surrounding the TSV array was quantified with Raman spectroscopy at room temperature. The scan was performed in a WiTec alpha300R system with in a backscattering arrangement. A 532-nm laser was focused to a diffraction limited spot size on the top surface of Si with a $100\times/0.9$ objective at a laser flux of $<10 \text{ mW}/\mu\text{m}^2$ to minimize the laser self-heating. Image scans were performed by rastering laser on the sample at a step size of 300 nm with a piezo-stage. Day-to-day variation of stress-free Si shift was calibrated by daily examination of Raman shift on

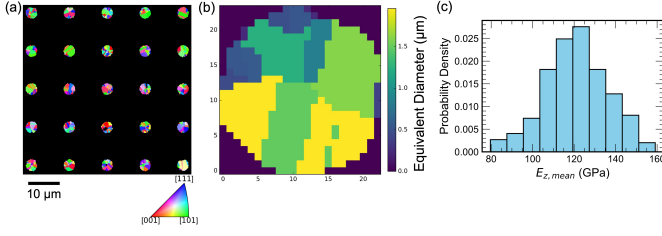


FIG. 2. Microstructure of Cu TSV and evaluation of elasticity matrix. (a) Inverse pole figure (IPF) of a 5×5 TSV array shows the crystal orientation. (b) Pixels on Cu are segmented into grains with a misorientation criterion of $< 10^\circ$ with most exhibiting a an equivalent diameter of $\sim 1 \mu\text{m}$. (c) Histogram of 187 TSVs indicates the variability of z -directional Young's modulus.

a bare Si sample, and drift of laser wavelength in long-duration scans (>10 hours) was corrected by tracking measured changes of the same location with time. Biaxial stress (σ) on Si (001) was calculated by a standard formula linking the measured Raman shift (ω) to the reference position (ω_0) on the stress-free reference sample via $\sigma = (\omega - \omega_0)/D$, where $D = -3.6 \text{ cm}^{-1}/\text{GPa}$ is a known calibration coefficient^{33,34}. A biaxial stress assumption is applied to evaluate the average residual stress around copper TSV near the Si surface, and the correlation between Raman shift and stress level was validated in previous studies^{33,34}. The details of system setup and calibration can be found in our previous work²⁰.

III. RESULTS AND DISCUSSION

The stress and microstructure of a 10×5 TSV array with a pitch of $12 \mu\text{m}$ was investigated using a combination of Raman and EBSD imaging to link how the Cu-microstructure impacts the mechanical state of the silicon. Figure 3a shows a combined microstructure-stress map, where Cu crystal orientation is represented with colors assigned via the inverse pole figure (IPF) and Raman-measured stress is depicted with a yellow-orange-brown color scale. Although the geometry of TSV remained consistent throughout the array, the profile, as well as the magnitude of stress within the Si, varies considerably from one TSV to the other. Conventional isotropic models¹¹ predict TSV stress merely based on geometric factors and homogeneous mechanical properties. Therefore, those models fail to explain the observed TSV-to-TSV difference, and additional contributing factors, such as microstructure, must be accounted for.

Figures 3b and 3c provide enlarged views of two TSVs with the same geometry but distinct microstructures, where one of them contains more than 10 grains and the other is closer to single crystal for the top portion of the TSV measured by EBSD. Comparing their stress fields, the more polycrystalline TSV (Figure 3b) exhibits lobes of both tensile and compressive stress within the Si. The

heterogeneous Cu-microstructure leads to a varied stress within the Si. The more uniform microstructure of Figure 3c, in contrast, leads to a more uniform tensile stress profile in the Si. Taken together, the characteristics of stress fields are consistent with that of Cu-microstructure influencing both the magnitude and distribution of the stress in the silicon. Cu-microstructure alters the effective moduli of TSV and, therefore the magnitude of Si-stress. Therefore, we conclude that the TSV-to-TSV variation of residual stress within the silicon is due to the distinct microstructure of the individual metallic cores.

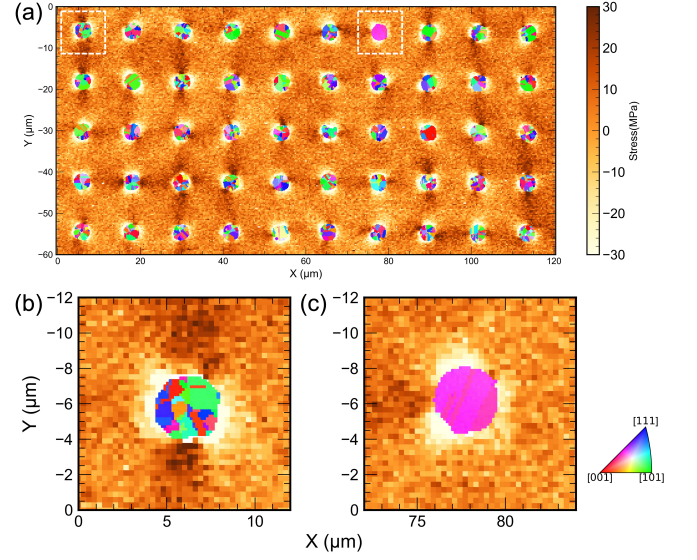


FIG. 3. Microstructure and residual stress of a Cu TSV array with $12 \mu\text{m}$ pitch. (a) Mixed stress and crystal orientation map. Crystal orientation of Cu is denoted with IPF colors, and level of Si biaxial stress is plotted in a yellow-orange-brown scale. Detailed views of TSVs (b) possesses more than 10 grains and (c) dominated by single grain. The enlarged regions in (b) and (c) are denoted with dotted boxes surrounding their location in the original map of (a).

To support this conclusion, the correlation between microstructure and the magnitude of the residual stress within the silicon was investigated. To do so, coordinates of a given TSV center were first determined. A ring-shaped band was then defined by two concentric circles each centered with the copper core of a TSV having a width (i.e., distance between two concentric circles) fixed at $1 \mu\text{m}$, an example of which is shown in Figure 4. The mean stress within the silicon surrounding a TSV was then calculated by calculating the average stress of all pixels within this band. The average stress could then be compared to the average effective modulus of the grain in the out of plane direct (E_z). To further assess the spatial extent of the Cu-microstructure's influence on the Si, the location of this band was also varied by altering the magnitude of the inner and outer radii while keeping their difference constant at $1 \mu\text{m}$. By specifying the location of the band with the average radius (r) of in-

ner and outer circle—corresponding to the distance from the center of band to that of TSV—the spatial extent of Cu-microstructure on Si stress was investigated.

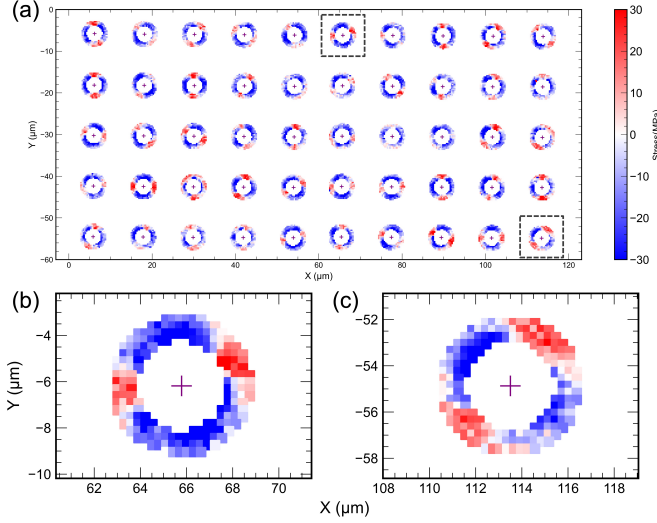


FIG. 4. Calculation of mean residual stress of TSV. (a) Pixels are segmented into ring-shaped bands with a distance of $r = 2.5 \mu\text{m}$ to the center of adjacent TSV and a width of $1 \mu\text{m}$. TSV centers are denoted with purple crosses. (b, c) Enlarged view of stress bands of two TSVs. The location of the enlarged regions within the array are denoted with dotted boxes in the original map of (a).

The magnitude of stress in the silicon correlates with the effective modulus of the Cu in the TSV and thus its microstructure. Shown in Figure 5, the correlation between stress and effective Young’s modulus of Cu is evaluated at two different distances, namely $r = 2.5 \mu\text{m}$ and $r = 4.5 \mu\text{m}$ from the TSV core. At $r = 2.5 \mu\text{m}$, the inner circle of the band is located close to the Si-Cu interface, and a pronounced positive correlation is observed between z -directional elastic modulus and mean stress of TSV (see Figure 5a). A p -value of $p < 10^{-4}$ is obtained with linear regression, proving the statistical significance of the correlation.

The positive relationship between stress and z -directional modulus can be explained by microstructure-dictated minimization of elastic strain energy. Elastic strain energy scales with directional elastic modulus (E) and elastic strain (ϵ). The elastic strain energy in the out-of-plane direction can be expressed as $U_z \sim E_z \epsilon_z^2$. With a larger z -directional modulus, the minimization of strain energy during thermal processes tends to decrease deformation in z direction. Meanwhile, a larger E_z corresponds to smaller elastic moduli in the x and y directions, allowing larger in-plane strains. Consequently, Cu TSVs with larger E_z tend to undergo larger in-plane expansions, squeezing more significantly against surrounding Si and leading to a higher level of Si stress. The correlation between the grain-dictated elastic modulus and stress demonstrates the important role of microstructure

in predicting residual stress of $3\text{-}\mu\text{m}$ TSVs. As the size of TSVs continues shrinking, combined grain-diameter analysis is needed to further understand the thermomechanical response of scaled TSVs²⁰.

The influence of the metal microstructure decays with distance away from the TSV underscoring how scaling will heighten the importance of this effect as via spacing approaches the zone affected by the microstructure. Qualitatively, the spatial decay of the microstructural influence on Si-stress is seen by comparing the correlation with effective modulus at a distance of $r = 4.5 \mu\text{m}$ and $r = 2.5 \mu\text{m}$ from the core. Even as both show a positive correlation with effective modulus, the effect is demonstrably weaker further away from the TSV core (compare Figures 5a and b). To quantify the spatial decay of the microstructural influence on Si-stress, a linear regression was performed to fit stress (σ) as a function of z -directional modulus (E_z) as a function of distance from the Cu-core. The resulting fitted slopes (i.e., $\partial\sigma/\partial E_z$), representing the sensitivity of the Si-stress to the Cu-microstructure, are plotted in Figure 5c. The magnitude of TSV-induced stress in Si decreases in an inverse parabolic manner¹¹ with distance, leading to a reduction in the sensitivity by a factor of 2 at a distance approximately equal to the TSV-radius. Effectively, the anisotropic characteristics of stress field diminish as it is being developed in the less-anisotropic Si substrate³⁵. This is a natural consequence of Saint-Venant’s principle.

IV. CONCLUSIONS

The impact of Cu-microstructure on the thermomechanical residual stress of TSVs with a diameter of $3 \mu\text{m}$ was investigated by comparing Raman stress imaging and EBSD grain characterization. Stress measured in the silicon near the TSV increases with the magnitude of the out-of-plane elastic modulus of copper determined by the Cu-microstructure. This positive correlation is explained with minimization of elastic strain energy. The observed microstructural dependence of Si-stress diminishes with distance from the Cu-core, having a decay length on the order of the TSV diameter. Together, this study experimentally demonstrates the impact of Cu-microstructure on residual stress in the silicon surrounding TSVs and highlights how this effect will likely become more prominent as the diameter and spacing between vias continues to decrease role with the continued scaling needed for advanced 3DIC.

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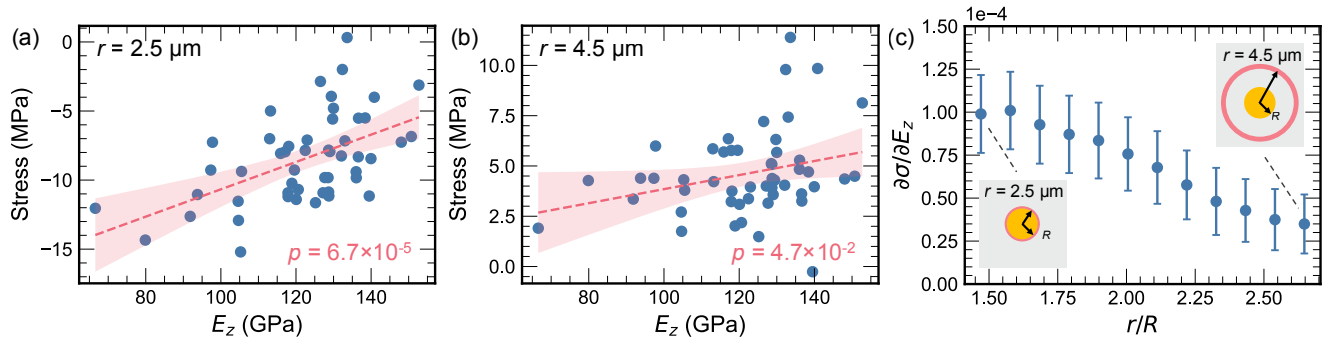


FIG. 5. Dependence of residual stress (σ) on z -directional elastic modulus (E_z) at varying distances from the TSV center. Residual stress as a function of z -directional elastic modulus at (a) $r = 2.5 \mu\text{m}$ and (b) $r = 4.5 \mu\text{m}$. A significant positive correlation is observed in the region close to TSV ($r = 2.5 \mu\text{m}$), whereas the trend becomes less prominent at a larger distance ($r = 4.5 \mu\text{m}$). Confidence of correlation is examined with linear regression. The blue dots represent experimental data and the red dotted line denotes the linear fit. The 95% confidence interval are plotted as red bands. (c) The fitting slope ($\partial\sigma/\partial E_z$) quantifies the sensitivity of residual stress to the Cu-microstructure near the TSV. The fitted slope decreases with increasing distance from the TSV center, indicating a diminishing influence of Cu-microstructure on residual stress. The distance from TSV center (r) is normalized with radius of TSV (R).

his feedback and input. Fabrication of TSV was performed at Birck Nanotechnology Center, Purdue University. Electron microscopy was performed using instrumentation in the Purdue Electron Microscopy Center (RRID:SCR.022687).

VI. DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

VII. CONFLICT OF INTEREST

The authors declare no conflict of interest.

VIII. REFERENCES

- ¹H.-S. P. Wong, "The End of the Road for 2D Scaling of Silicon CMOS and the Future of Device Technology," in *2018 76th Device Research Conference (DRC)*, pp. 1–2.
- ²J. H. Lau, "Recent Advances and Trends in Advanced Packaging," **12**, 228–252.
- ³S. B. Samavedam, J. Ryckaert, E. Beyne, K. Ronse, N. Horiguchi, Z. Tokei, I. Radu, M. G. Bardon, M. H. Na, A. Spessot, and S. Biesemans, "Future Logic Scaling: Towards Atomic Channels and Deconstructed Chips," in *2020 IEEE International Electron Devices Meeting (IEDM)*, pp. 1.1.1–1.1.10.
- ⁴H. Kim, J. Y. Hwang, S. E. Kim, Y.-C. Joo, and H. Jang, "Thermomechanical Challenges of 2.5-D Packaging: A Review of Warpage and Interconnect Reliability," **13**, 1624–1641.
- ⁵Y. Li, P. Chen, F. Qin, T. An, Y. Dai, M. Zhang, and Y. Jin, "Constitutive modelling of annealing behavior in through silicon vias-copper," **179**, 111359.
- ⁶T. Wei, J. Cai, Q. Wang, Z. Liu, Y. Li, T. Wang, and D. Wang, "Copper filling process for small diameter, high aspect ratio Through Silicon Via (TSV)," in *2012 13th International Conference on Electronic Packaging Technology & High Density Packaging*, pp. 483–487.
- ⁷T. Wei, Q. Wang, Z. Liu, Y. Li, D. Wang, T. Wang, and J. Cai, "A 3D integration testing vehicle with TSV interconnects," in *2012 14th International Conference on Electronic Materials and Packaging (EMAP)*, pp. 1–5.
- ⁸M. Zhang, F. Qin, S. Chen, Y. Dai, Y. Jin, P. Chen, T. An, and Y. Gong, "Holding time effect on mechanical properties and protrusion behaviors of through silicon via copper under various annealing processes," **158**, 107353 ().
- ⁹M. Zhang, F. Qin, S. Chen, Y. Dai, Y. Jin, P. Chen, T. An, and Y. Gong, "Effect of Capped Cu Layer on Protrusion Behaviors of Through Silicon via Copper (TSV-Cu) Under Double Annealing Conditions: Comparative Study," **23**, 89–98 ().
- ¹⁰M.-Y. Tsai, P.-S. Huang, C.-Y. Huang, H. Jao, B. Huang, B. Wu, Y.-Y. Lin, W. Liao, J. Huang, L. Huang, S. Shih, and J. P. Lin, "Investigation on Cu TSV-Induced KOZ in Silicon Chips: Simulations and Experiments," **60**, 2331–2337.
- ¹¹M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim, "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC," **57**, 107–115.
- ¹²S.-K. Ryu, K.-H. Lu, X. Zhang, J.-H. Im, P. S. Ho, and R. Huang, "Impact of Near-Surface Thermal Stresses on Interfacial Reliability of Through-Silicon Vias for 3-D Interconnects," **11**, 35–43.
- ¹³P. Saettler, M. Hecker, M. Boettcher, C. Rudolph, and K. J. Wolter, " μ -Raman spectroscopy and FE-modeling for TSV-Stress-characterization," *Materials for Advanced Metallization* **2014**, **137**, 105–110.
- ¹⁴C. Selvanayagam, X. Zhang, R. Rajoo, and D. Pinjala, "Modeling Stress in Silicon With TSVs and Its Effect on Mobility," **1**, 1328–1335.
- ¹⁵A. Udupa, G. Subbarayan, and C.-K. Koh, "Analytical estimates of stress around a doubly periodic arrangement of through-silicon vias," *Reliability of Micro-Interconnects in 3D IC Packages*, **53**, 63–69.
- ¹⁶D. Vogel, E. Auerswald, J. Auersperg, P. Bayat, R. D. Rodriguez, D. R. T. Zahn, S. Rzepka, and B. Michel, "Stress analyses of high spatial resolution on TSV and BEoL structures," *SI: ESREF* **2014**, **54**, 1963–1968.
- ¹⁷Z. Wang, G. Ye, X. Li, S. Xue, and L. Gong, "Thermal-Mechanical Performance Analysis and Structure Optimization of the TSV in 3-D IC," **11**, 822–831.

- ¹⁸A. Basavalingappa and J. R. Lloyd, "Effect of Microstructure and Anisotropy of Copper on Reliability in Nanoscale Interconnects," **17**, 69–79.
- ¹⁹A. P. Karmarkar, X. Xu, K.-B. Yeap, and E. Zschech, "Copper Anisotropy Effects in Three-Dimensional Integrated Circuits Using Through-Silicon Vias," **12**, 225–232.
- ²⁰S. Lyu, T. Beechem, and T. Wei, "Scaling effects on the microstructure and thermomechanical response of through silicon vias (TSVs)," **137**, 085101 ().
- ²¹S. B. Liang, C. B. Ke, C. Wei, M. B. Zhou, and X. P. Zhang, "Study of the Influence of Elastic Anisotropy of Cu on Thermo-Mechanical Behavior and Cu Protrusion of Through Silicon Vias Using Combined Phase Field and Finite Element Methods," **19**, 322–332 ().
- ²²Z. Fan, X. Chen, Y. Liu, Y. Jiang, and Y.-a. Zhang, "Effects of anisotropy on the reliability of TSV microstructure," 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2020, **114**, 113745.
- ²³Y. Zhang, C. Sheng, S. Wang, T. Liu, Z. Gao, and S. Liu, "Influence of Inhomogeneous Anisotropic Copper Grains in TSV on the Thermo-Mechanical Behaviors in the Annealing Process," **14**, 601–610 ().
- ²⁴P. Saettler, K. Meier, and K.-J. Wolter, "Considering copper anisotropy for advanced TSV-modeling," in *Proceedings of the 2011 34th International Spring Seminar on Electronics Technology (ISSE)*, pp. 419–423.
- ²⁵J. Liang, M. Ning, C. Ding, T. Liu, Z. Dai, and H. Qin, "The effect of silicon anisotropy on the thermal stress of TSV structure of 3D packaging chip under thermal cyclic loads," in *2021 22nd International Conference on Electronic Packaging Technology (ICEPT)*, pp. 1–4.
- ²⁶Z. Wu, Z. Huang, P. P. Conway, and Y. Ma, "Effect of microstructure on thermal-mechanical stress in 3D copper TSV structures," in *2011 IEEE 13th Electronics Packaging Technology Conference*, pp. 450–454.
- ²⁷M. Lei, Y. Wang, X. Yang, and Y. Yao, "Microstructure evolution and mechanical behavior of copper through-silicon via structure under thermal cyclic loading," **136**, 114730.
- ²⁸K. B. Yeap, E. Zschech, U. D. Hangen, T. Wyrobek, L. W. Kong, A. Karmakar, X. Xu, and I. Panchenko, "Elastic anisotropy of Cu and its impact on stress management for 3D IC: Nanoindentation and TCAD simulation study," **27**, 339–348.
- ²⁹Y. Dai, M. Zhang, F. Qin, P. Chen, and T. An, "Effect of silicon anisotropy on interfacial fracture for three dimensional through-silicon-via (TSV) under thermal loading," **209**, 274–300.
- ³⁰S. Lyu, T. Beechem, and T. Wei, "Reliability and Microstructure Characterization of Through-Silicon Vias (TSV) at Different Aspect Ratios Using EBSD-Raman Spectroscopy," in *2025 IEEE 75th Electronic Components and Technology Conference (ECTC)*, pp. 380–385.
- ³¹S. Lyu, T. E. Beechem, and T. Wei, "Thermo-Mechanical Reliability Analysis and Raman Spectroscopy Characterization of Sub-micron Through Silicon Vias (TSVs) for Backside Power Delivery in 3D Interconnects," in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*, pp. 834–841.
- ³²R. Hill, "Constitutive inequalities for isotropic elastic solids under finite strain," **314**, 457–472.
- ³³T. Beechem, L. Yates, and S. Graham, "Invited Review Article: Error and uncertainty in Raman thermal conductivity measurements," **86**, 041101.
- ³⁴T. Beechem, S. Graham, S. P. Kearney, L. M. Phinney, and J. R. Serrano, "Invited Article: Simultaneous mapping of temperature and stress in microdevices using micro-Raman spectroscopy," **78**, 061301.
- ³⁵D. H. Chung and W. R. Buessem, "The Elastic Anisotropy of Crystals," **38**, 2010–2012.