UNIVERSITY OF CALIFORNIA

Los Angeles

Nanowire Optoelectronics at Infrared: Modeling, Epitaxy, and Devices

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Dingkun Ren

2018

ABSTRACT OF THE DISSERTATION

Nanowire Optoelectronics at Infrared: Modeling, Epitaxy, and Devices

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Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2018

Professor Diana L. Huffaker, Chair

Bottom-up semiconductor nanowires and their arrays have been frequently highlighted as building blocks for next-generation optoelectronic devices. Compared with planar thin films, vertical nanowires have unique properties, namely three-dimensional (3-D) geometries with high surface-to-volume ratios, small junction area, and heteroepitaxy. These capabilities lead to the designs of high-performance, integrated, and compact device platforms. Intrinsically, there is no fundamental difference in the semiconductor device physics or material characteristics between nanowires and traditional planar thin films. However, the relationship between the 3-D nanowire geometries and the material properties introduces unique aspects of carrier dynamics. Studying these dynamics is critical to exploring the rich electrical properties underlying the material characterizations and guiding the design of nanowire optoelectronic devices.

In this dissertation, we provide new insight into nanowire optoelectronics at infrared by investigating nanowire modeling, epitaxy, and devices. Since carrier dynamics in nanowires are much more complicated than those in thin films, we combine optical and electrical simulations to develop a more powerful scheme of 3-D modeling, allowing us to comprehensively interpret and understand the temporal and spatial motion of carriers in nanowires. Equipped with this simulation capability, we are able to propose novel device structures for infrared photodetection with better performance than their planar device counterparts. With these new insight as well as nanowire designs obtained from modeling, we then tackle the heteroepitaxy of nanowires on lattice mismatched substrates by selective-area metal-organic chemical vapor deposition and demonstrate the growth capability of high-quality materials within the 2 – 5 μm wavelength spectrum. Finally, we demonstrate an uncooled nanowire-based device platform for photodetection at short-wavelength infrared and mid-wavelength infrared. These three points of focus in this dissertation–modeling, epitaxy, and devices–are closely intertwined, and together provide a holistic picture of 3-D nanowire performance. We believe the presented theoretical and experimental work will stimulate more validating studies of nanowire optoelectronics at infrared to further reveal the inherent carrier dynamics of nanowires and develop more sophisticated nanowire optoelectronic devices.

This dissertation of Dingkun Ren is approved.

Benjamin S. Williams

Chee-Wei Wong

Mark S. Goorsky

Diana L. Huffaker, Committee Chair

University of California, Los Angeles

2018

This dissertation is dedicated to my family.

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Acknowledgements

I would first like to thank my committee chair and advisor Diana L. Huffaker for the tremendous support and guidance over the course of my Ph.D. years at UCLA. I also appreciate Prof. Benjamin S. Williams for his constant support and guidance on many aspects of my research. I would like to thank all my committee for the guidance and suggestions contributed to the completion of this dissertation.

I would like to thank Alan C. Farrell, Adam C. Scofield, Baolai Liang, Pradeep Senanayake, Andrew Pan, and Benjamin A. Burnett for mentoring me and leading me into the research of nanotechnology. I would also like to say thank you to Bor-Chau Juang, Hyunseok Kim, Zixuan Rong, Wook-Jae Lee, Mukul Debnath, Ting-Yuan Chang, Khalifa M. Azizur-Rahman, Andrew Chen, Siddharth Somasundaram for their great support as colleagues and as friends.

I am grateful to the technical support from the staff of the UCLA Nanoelectronics Research Facility as well as the Integrated Systems Nanofabrication Cleanroom (ISNC), Electron Imaging Center for NanoMachines (EICN), and Nano & Pico Characterization Lab (NPC) in the California NanoSystems Institute (CNSI). I would also like to thank the staff at the Office of Graduate Student Affairs, Deeona Columbia, Mandy Smith, Ryo Arreola, Julio Vega Romero, for always being there for students in need. I would like to acknowledge the financial support from the National Science Foundation (NSF), Air Force Office of Scientific Research (AFOSR), the United Sates Department of Defense (DoD), and Sêr Cymru National Research Network in Advanced Engineering and Materials.

Finally, I would like to thank the selfless support from my family for their endless love and encouragement along the way.

Vita

EDUCATION

Ph.D. candidate	University of California, Los Angeles Electrical Engineering	2013 - 2018
M.S.	University of California, Los Angeles Electrical Engineering	2011 - 2013
B.E.	Tianjin University Mechanical Engineering	2007 - 2011
	University of Glasgow (exchange) Electronics and Electrical Engineering	2010 - 2011

HONORS

Member of the Optical Society (OSA)	2017
Member of the Materials Research Society (MRS)	2016
Member of SPIE	2015

PUBLICATIONS

1. **D. Ren**, A. C. Scofield, A. C. Farrell, Z. Rong, M. A. Haddad, R. B. Laghumavarapu, B. Liang, and D. L. Huffaker, "Exploring time-resolved photoluminescence for nanowires using a three-dimensional computational transient model," *Nanoscale*, 10, 7792, 2018.
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9. A. C. Farrell*, X. Meng*, **D. Ren***, H. Kim, P. Senanayake, N. Y. Hseih, Z. Rong, T.-Y. Chang, K. M. Azizur-Rahman, and D. L. Huffaker, "InGaAs-GaAs nanowire avalanche photodiodes toward single photon detection in free-running mode," (*ACS Nano*, *under review*, **co-first authors*)
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12. **D. Ren**, Khalifa M. Azizur-Rahman, Z. Rong, B.-C. Juang, S. Somasundaram, M. Shahili, A. C. Farrell, B. S. Williams, and D. L. Huffaker, "Developing uncooled InAsSb nanowire photodetector arrays with Al_2O_3 passivation for photodetection at mid-wavelength infrared," (*in preparation*)

CONFERENCE ORAL PRESENTATIONS

1. D. L. Huffaker, D. Ren, Khalifa M. Azizur-Rahman, and H. Kim, "Selective-area nanowire photodetectors for mid-wavelength detection and single photon detection," SPIE Optics + Photonics 2018, San Diego, USA, 2018. (***Invited***)
2. D. Ren, A. C. Farrell, X. Meng, M. Cao, and D. L. Huffaker, "Feasibility of room-temperature mid-wavelength infrared photodetector using InAsSb nanostructured photoabsorbers," SPIE Photonics West 2018, San Francisco, USA, 2018. (***Invited***)
3. D. L. Huffaker, M. Jarrahi, D. Ren, Z. Rong, H. Kim, and D. Turan, "Plasmonic nanowire optical to terahertz converter operation at telecom wavelengths," SPIE Photonics West 2018, San Francisco, USA, 2018. (***Invited***)
4. D. L. Huffaker, D. Ren, A. C. Farrell, and X. Meng, "Infrared photodetectors by selective-area nanowires," 2017 Materials Research Society Spring, Phoenix, USA, 2017. (***Invited***)

TEACHING EXPERIENCE

EE 170C – Photonic Sensors and Solar Cells (upper division undergrad) 2016-2018
(Instructor: Prof. Benjamin S. Williams)

EE 123A – Fundamentals of Solid-State I & II 2012-2015
(Instructor: Prof. Diana L. Huffaker)

PIC 10A – Introduction to Programming 2012
(Instructor: Prof. Keith Ouellette)

REVIEW SERVICE

Ad hoc reviewer for various journals including: Applied Physics Letters, Journal of Applied Physics, Scientific Reports, Optics Letters, Optics Express, Optical Materials Express, Applied Optics, Nanoscale Research Letters, Micro & Nano Letters.

Ad hoc reviewer for conference: 17th IEEE International Conference on Nanotechnology.

1. Introduction

Bottom-up semiconductor nanowires and their arrays have been frequently highlighted as building blocks for next-generation optoelectronic devices. Compared with planar thin films, vertical nanowires have unique properties, namely three-dimensional (3-D) geometries with high surface-to-volume ratios, small junction area, and heteroepitaxy. These capabilities lead to the designs of high-performance, integrated, and compact device platforms. Intrinsically, there is no fundamental difference in the semiconductor device physics or material characteristics between nanowires and traditional planar thin films. However, the relationship between the 3-D nanowire geometries and the material properties introduces unique aspects of carrier dynamics (Fig. 1.1). Studying these dynamics is critical to exploring the rich electrical properties underlying the material characterizations and guiding the design of nanowire optoelectronic devices.

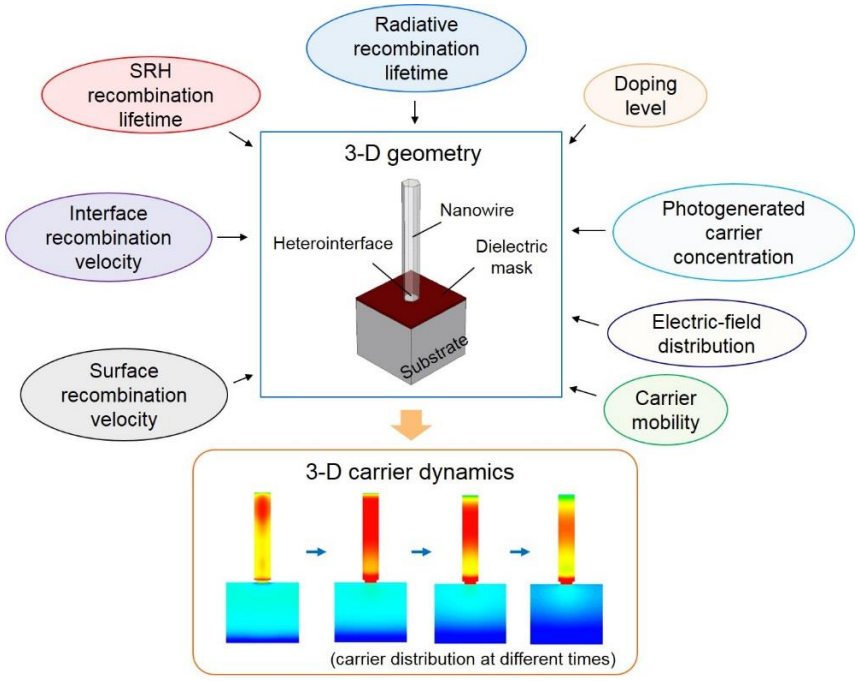

Figure 1-1 Correlation between 3-D geometry, material properties, and carrier dynamics for nanowires.

In this dissertation, we provide new insight into nanowire optoelectronics at infrared by investigating nanowire modeling, epitaxy, and devices (Fig. 1-2). Since carrier dynamics in nanowires are much more complicated than those in thin films, we combine optical and electrical simulations to develop a more powerful scheme of 3-D modeling, allowing us to comprehensively interpret and understand the temporal and spatial motion of carriers in nanowires. Equipped with this simulation capability, we are able to propose novel device structures for infrared photodetection with better performance than their planar device counterparts. With these new

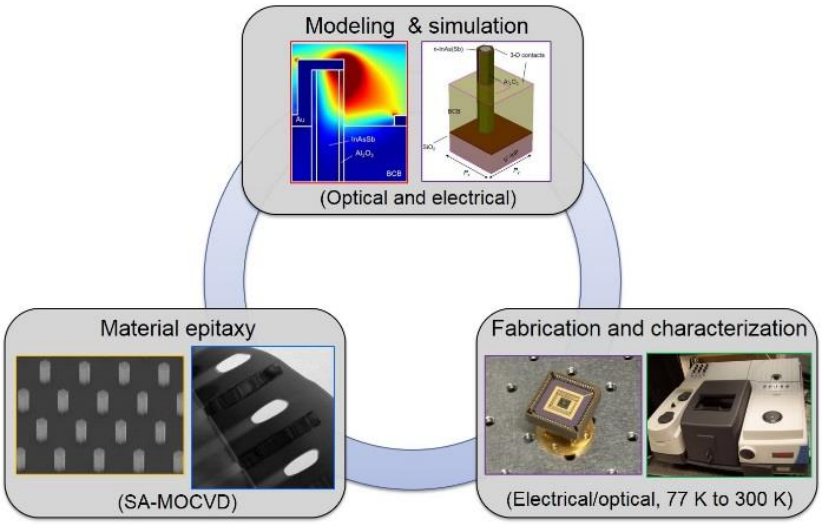

Figure 1-2 Illustration showing the scope of this study.

insight as well as nanowire designs obtained from modeling, we then tackle the heteroepitaxy of nanowires on lattice mismatched substrates by selective-area metal-organic chemical vapor deposition (SA-MOCVD) and demonstrate the growth capability of high-quality materials within the 2 – 5 μm wavelength spectrum. Finally, we demonstrate an uncooled nanowire-based device platform for photodetection at short-wavelength infrared (SWIR) and mid-wavelength infrared (MWIR). These three points of focus in this dissertation–modeling, epitaxy, and devices–are closely intertwined, and together provide a holistic picture of 3-D nanowire performance. The modeling and simulation provide a fundamental understanding of the material and device

characterizations as well as a blueprint for nanowire-based optical devices. Meanwhile, the epitaxy discusses the logistics of growing the nanowires, while the devices provide the final fabrication and characterizations, along with real-world understanding of how these photodetectors work. The experimental work also provides insight into the physics underlying the nanostructures and determine the next course of action in the simulation study. This cycle of simulation, epitaxy, and devices is repeated over itself, with the experimental and theoretical study mutually affecting each other. This strategy will be clearly presented throughout the entire dissertation.

Within this dissertation, we will discuss several studies that focus on several different factors that affect nanowire optical device performance. Chapter 2 focuses on developing an optoelectronic transient model and photoresponse model, allowing us to investigate carrier lifetimes, specifically how they are affected by material properties, and how they affect responsivity and detectivity. Chapter 3 then studies the growth of nanowires and inserts by SA-MOCVD, which enables hybrid integration of small bandgap photoabsorbers on large bandgap material. Chapter 4 then performs an initial demonstration of SWIR/MWIR nanowire photodetectors with *p*-*n* heterojunctions to show significant suppression of surface recombination and dark current, paving the way to accomplish room-temperature operation of detectors with higher detectivities. Finally, Chapter 5 concludes with future studies that would ultimately realize room-temperature nanowire photodetectors for photodetection at MWIR.

2. Nanowire Optoelectronic Computational Models

2.1 Overview

Due to the unique three-dimensional (3-D) geometries of nanowires—i.e., large surface-to-volume ratios and smaller cross-sections at the nanowire-substrate interfaces— their carrier dynamics are much more complicated than those of thin films. Therefore, analytical solutions cannot be found for these nanostructures and a more comprehensive scheme of 3-D modeling is necessary to interpret their intrinsic carrier dynamics.[1] To date, most modeling studies for nanowires have focused on electromagnetic properties (e.g. optical modes and optical absorption). However, very few studies have combined optical and electrical simulations together to probe the temporal and spatial carrier motions within nanowires. In this chapter, we present a comprehensive nanowire optoelectronic transient model and photoresponse model, allowing us to investigate carrier lifetimes and their fundamental correlations with material properties, as well as responsivities and detectivities for nanowire-based optical devices for photodetection (i.e., photodetectors). We believe this work can stimulate further experimental and theoretical work and unveil the real strength of 3-D computational models for exploring carrier dynamics in nanowires and nanostructured materials.

The first part of this chapter will overview the procedures for 3-D computational transient and photoresponse modeling. The second part focuses on the detailed applications of these models: (1) the transient model for time-revolved photoluminescence (TRPL) to concurrently extract multiple material properties for nanowires; (2) the transient model to investigate the correlation between carrier lifetime and surface recombination velocity for nanowires; (3) the photoresponse

model to explore the ideal responsivities and detectivities for nanowire-based photodetectors; and (4) the photoresponse model to study the generation of ultrafast current pulses by nanowire photoabsorbers.

2.1.1 3-D computational transient model

The 3-D computational transient model of the nanowire structure is set up in Synopsys Sentaurus TCAD based on the finite-element method (FEM) to mimic a TRPL measurement process. The output of the simulation is the nanowire's temporal optical emission in response to a laser pulse, caused by band-to-band radiative recombination. A diagram of the simulation process composed of three major steps is shown in Fig. 2-1. First, we construct a unit cell composed of a nanowire, dielectric mask, substrate, and ambient air. The dimensions of the nanowire, height and diameter, can be determined from either scanning electron microscope (SEM) or cross-sectional transmission electron microscopy (TEM) measurements. Then, we compute the optical generation (in units of $cm^{-3}\,s^{-1}$) in the nanowire using normally incident light by finite-difference time-domain (FDTD). Next, by combining the Poisson equation, current-density equation, and continuity equation in the transient model with the temporal optical generation, we calculate the temporal band-to-band radiative recombination in a nanowire segment. For a 3-D geometry, the radiative recombination rate (in units of $cm^{-3}\,s^{-1}$) has a high dependency on position due to a nonuniform distribution of carriers and can be expressed as

$$R(x,y,z,t) = B[n(x,y,z,t)p(x,y,z,t) - n_0(x,y,z,t)p_0(x,y,z,t)] \tag{2.1}$$

where n and p are local carrier densities of electrons and holes respectively (in units of cm^{-3}), B is the radiative recombination coefficient (in units of $cm^3\,s^{-1}$), and t is the time (in units of s). Thus,

the actual time-dependent radiative recombination (in units of s^{-1}), or the intensity of photoluminescence emission, from nanowire segments can be calculated as

$$I = \int R(x, y, z, t) dV \tag{2.2}$$

where I is the intensity of optical emission and V is the overall volume of nanowire segments.

The numerical simulator offers the critical benefit of being able to compute Poisson equations in 3-D structures and solve carrier concentrations in steady states at different points in time. This allows us to directly probe temporal and spatial carrier motion. To represent an optical excitation from a pulsed laser source, the incident light is set as a Gaussian function with full width at half maximum (FWHM) in a picosecond level. This is based on the calibrated specifications of our TRPL characterization setup using an NKT SuperK EXTREME continuum laser. Finally, carrier lifetime τ (in units of ns) is extracted by fitting to an exponential equation with a single decay $\exp(-t/\tau)$. We computationally map the spatial and temporal carrier distributions in nanowire segments to reveal the underlying carrier dynamics. Note that we use a low excitation condition in simulations and thus the lifetime τ was minority carrier lifetime.

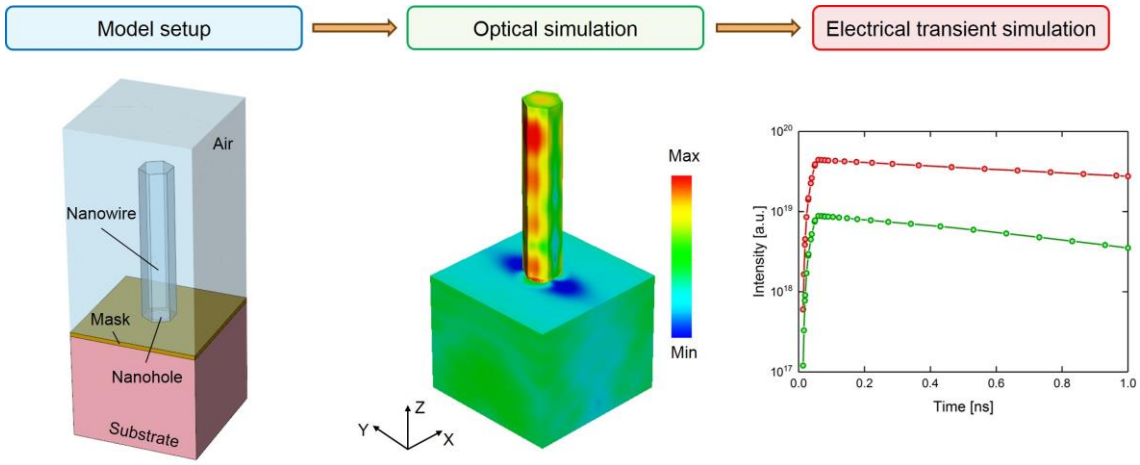

Figure 2-1 Schematic diagram for TRPL simulation process. The three major steps include: (1) model setup, (2) optical simulation (FDTD and FEM), and (3) electrical transient simulation (FEM).

2.1.2 3-D computational photoresponse model

Similar to the TRPL simulations, the model for the current response is also based on Synopsys Sentauras TCAD. The difference is that we now focus on the output photocurrent instead of the radiative recombination. A diagram of the simulation process composed of the three major steps is shown in Fig. 2-2. First, we solve the optical profiles of a unit cell by Lumerical FDTD. Next, we translate the electric field profiles in FDTD rectangular nodes into the FEM tetrahedral nodes generated by Sentaurus using MATLAB. Note that the nanowire structures drawn in the two simulators need to be identical. Then, we couple the generated optical generation profiles (from electric distribution) to the drift-diffusion equation as well as the continuity equation and calculate the output current as a function of reverse. Finally, we extract the actual photocurrent (I_{ph}) and calculate responsivities and detectivities based on the analytical equations. Further description of the photoresponse modeling will be presented in the Section 2.4.

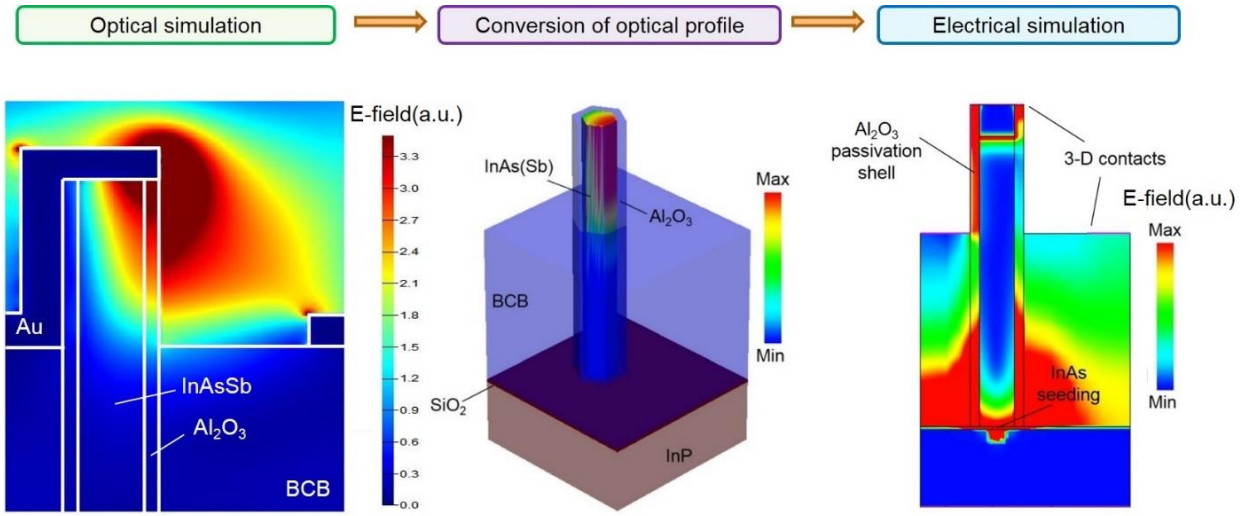

Figure 2-2 Schematic diagram of photoresponse simulation steps. Three major steps are involved: (1) optical simulation (FDTD), (2) conversion of optical profile (from FDTD to FEM), and (3) electrical photoresponse simulation (FEM). InAsSb nanowire photodetectors are used as an example.

2.2 Transient model – extracting multiple material properties

2.2.1 Introduction

Although TRPL is traditionally used to measure carrier lifetimes and infer recombination mechanisms, we believe that the rich physics underlying TRPL can be harnessed to also explore multiple material properties that reflect the complex carrier dynamics in III-V nanowires with nanowire-substrate heterointerfaces. This is because the overall carrier lifetime is influenced by the carrier dynamics resulting from multiple mechanisms. In other words, the lifetime and material properties of a nanowire are related, but not in a simple one-to-one correlation (mainly because of the 3-D carrier motion). Changing only one of these mechanisms is experimentally impractical. As a result, we use the 3-D TRPL transient model and take a simulation approach to investigate the correlation between lifetime and material properties.

To validate the model and demonstrate the concept, we investigate *p*-type GaAs nanowires grown on silicon substrates. Without losing generality, we consider three important material properties: mobility (μ), Shockley-Read-Hall (SRH) recombination lifetime (τ_{SRH}), and nanowire-substrate heterointerface recombination velocity (S_n). We measure the minority carrier (electron) lifetime (τ_n) of *p*-type GaAs nanowires by TRPL and perform numerical simulations to fit the measured TRPL curves. By tuning the material properties of the GaAs nanowire segments and the GaAs seeding layers, we study the impact of those properties on τ_n and further identify their lifetime characteristics. Finally, we tabulate the values of material properties based on the simulation results and interpret the carrier dynamics by mapping the spatial electron distribution as a function of time.

2.2.2 Experimental setup

We first perform a series of growths of Zn-doped GaAs nanowires on lightly boron-doped Si (111) wafers by selective-area metal-organic chemical deposition (SA-MOCVD). The lattice mismatch between GaAs and Si is about 4.1%, and electrons are the minority carriers. The diameter and pitch of the nanoholes are 80 nm and 800 nm, respectively, defined by electron-beam lithography (EBL). The arrays have dimensions of 50 μm × 50 μm, much larger than the laser spot size. Prior to the growth of the nanowire segment, a thin GaAs seeding layer is introduced as a buffer to achieve high vertical yield and high uniformity across the nanowire array. To vary the GaAs-Si heterointerface material quality, five different growth temperatures for the seeding layers (T_{Seed})—450°C, 550°C, 600°C, 625°C, and 650°C—are used, while the nanowire growth temperature remains fixed at 730°C. The nanowires are passivated *in-situ* by a lattice-matched AlGaAs shell followed by a thin GaAs shell to reduce surface recombination at the semiconductor-to-air interface. We have labelled these five samples according to different seeding layer growth temperatures: Sample A (450°C), Sample B (550°C), Sample C (600°C), Sample D (625°C), and Sample E (650°C).

Next, the minority (electron) carrier lifetimes (τ_n) of Samples A to E for band-to-band recombination (875 nm) are carried out by TRPL at room temperature (300 K) using a pulsed laser operated at 633 nm with a repetition rate of 40 MHz and a pulse width of 30 ps. The lifetimes are taken on the as-grown nanowire arrays. The laser power density is calibrated to 178 W/cm^2. Note that the laser pump power is set relatively low to keep a low injection level for carriers. As shown in later discussion (in Fig. 2-9), the density of excess electrons is about 1×10^{16} – 1×10^{17} cm^{-3}, so filling the traps is unlikely. The measured TRPL curves are shown in Fig. 2-3, and the extracted τ_{n} as a function of T_{Seed} is summarized in the inset. To obtain τ_{n}, the TRPL curves between 0.4 ns and

1.4 ns are fitted by a single exponential decay expressed as exp(-t/τ). The calculated τ_n of Samples A, B, C, D, and E are 0.52 ns, 0.84 ns, 1.25 ns, 0.73 ns, and 0.60 ns, respectively.

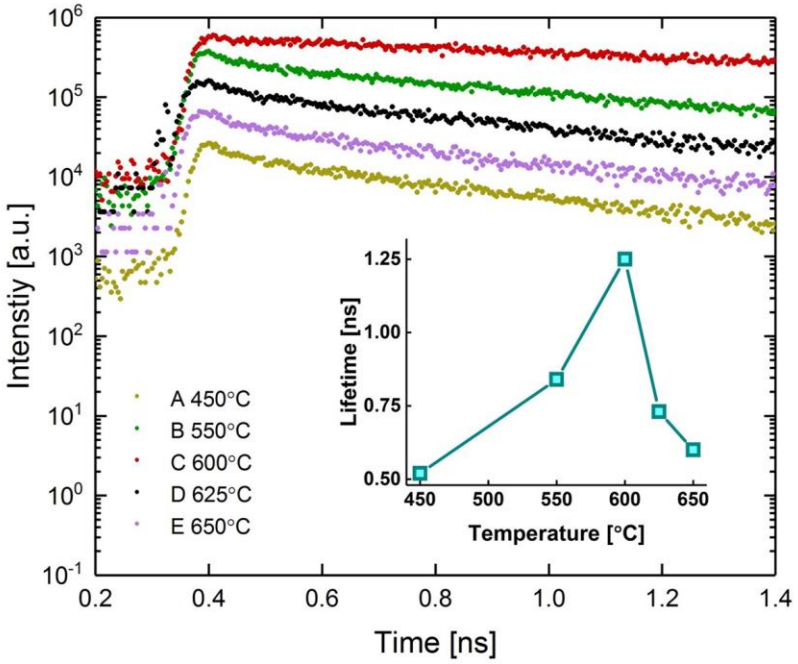

Figure 2-3 The TRPL curves of Samples A, B, C, D, and E at 300 K. The seeding layer growth temperatures of these three samples are 450°C, 550°C, 600°C, 620°C and 650°C, respectively. All the extracted lifetimes of Samples A to E are provided in the inset.

2.2.3 Model setup

Recall that the entire simulation started with the construction of a 3-D model based on actual nanowire dimensions. Thus, we first measure the dimensions—height and diameter—of Samples A through E by SEM, and investigate the cross-sections of the nanowires by TEM. A 30°-tilted SEM image of a GaAs nanowire array Sample C (600°C) is shown in Fig. 2-4(a). Clearly, Samples B through D show high vertical yield (nearly 100% for Samples B and C and over 85% for Sample D), similar to that of the un-doped GaAs nanowires grown by SA-MOCVD.[2] In contrast, Samples A and E show a much lower vertical yield with some randomly located irregular polycrystalline structures and tilted nanowires. The average height and diameter of the

vertical nanowires are 740 nm and 135 nm respectively. All samples show a good uniformity, with a variation of no more than 6 nm. Sample C (600°C) is prepared for TEM analysis by focusing ion beam (FIB) milling, and a FEI T12 TEM is operated in bright field to study the GaAs-Si heterointerface regions and the GaAs nanowire segments, as shown in Fig. 2-4(b). Crystal defects, specifically zinc-blende (ZB)–wurtzite (WZ) polytypisms and stacking faults, are observed, which is expected in patterned SAE growth of III-V nanowires. Interestingly, the seeding layer growth is initiated beneath the SiN_x growth mask, and a trapezoid-shaped GaAs crystalline structure is formed with a thickness of 6 – 7 nm. Thus, the growth beneath the mask is included in the 3-D model. As shown in a previous study for InGaAs nanowire growth on Si with GaAs stub,[3] the GaAs seeding layer is expected to fill up to the top of the SiN_x mask.

A cross-sectional schematic diagram of the 3-D model composed of a GaAs nanowire and Si substrate is illustrated in Fig. 2-4(c), along with a close-up look of the seeding layer segment and the GaAs-Si heterointerface. The dimensions characterized by TEM are labelled. No threading dislocations or antiphase domains (APDs) are found at GaAs-Si heterointerfaces. To simplify the simulation structure, we make several assumptions. First, the nanohole and trapezoid-shaped segments are fully covered by the GaAs seed, and their geometries are appoximated as cylindrical, which are similar to the GaAs stubs shown in a previous work.[3] Second, since the thickness of the AlGaAs passivation layer is only ~ 5 – 10 nm, it is not included in the schematics. Instead, we simplify its structure by introducing surface recombination velocity at GaAs-air interfaces on six (110) sidewalls of GaAs nanowires. The energy-band diagram as well as the quasi-Fermi level of the segment along the GaAs-Si heterointerface is schematically shown in Fig. 2-4(c), and the interface states, i.e., traps, that result in nonradiative recombination are illustrated.

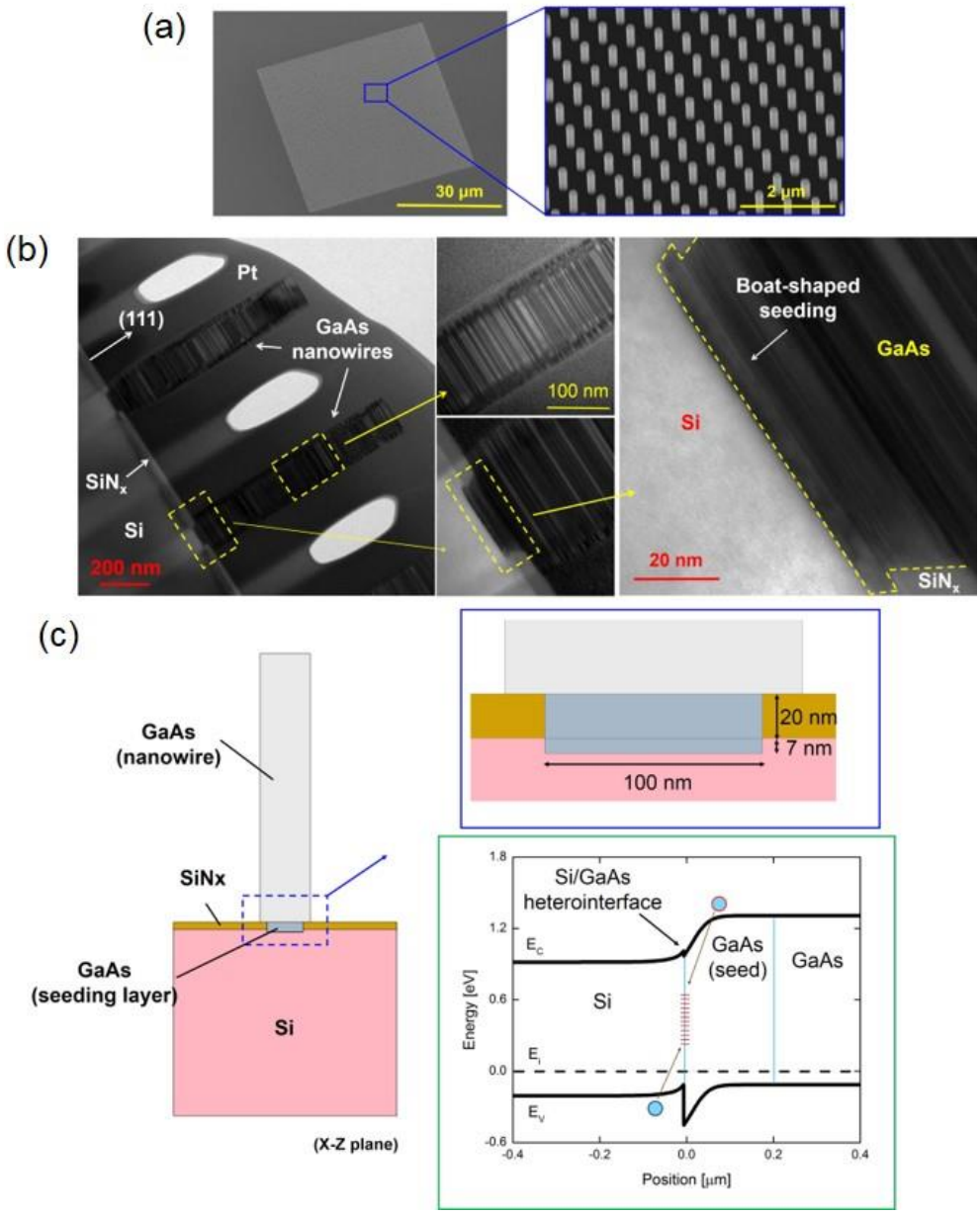

Figure 2-4 (a) An as-grown 50 µm × 50 µm array with extremely high uniformity. The GaAs seeding layer was grown at 600°C. The close-up image of the nanowire array is shown on the right. (b) Cross-sectional TEM image of GaAs nanowires with GaAs seeding layer grown at 600 °C. The two zoom-in images in the center show the nanowire segment and the trapezoid-shaped seeding layer. Further close-up detail of GaAs-Si interface is shown in the image on the right. (c) *Z*-normal cross-section of the 3-D model showing a close-up of the GaAs seeding layer and an energy-band diagram of the GaAs-Si heterointerface. The interface states are illustrated.

2.2.4 Optical simulation

After building the 3-D geometry, we move on to the optical simulation. To precisely replicate the TRPL measurement in the experiment, we define the optical wavelength as 633 nm and the optical power density as 178 W/cm^2. Periodic boundary conditions are used in the X and Y directions, while a perfectly matched layers absorbing boundary are used in the Z direction. Fig. 2-5 shows the simulated optical generation along the cross-section of a nanowire. The optical absorption in the Si substrate is much less compared with GaAs segments due to its smaller absorption coefficient. Note that the photogenerated carriers are mostly concentrated at the top and bottom regions of the nanowire as well as the area near the GaAs-Si heterointerface. This can be explained by the increased electric field intensities at those locations due to incident light coupling to the HE_{11} guided mode on resonance.[4]

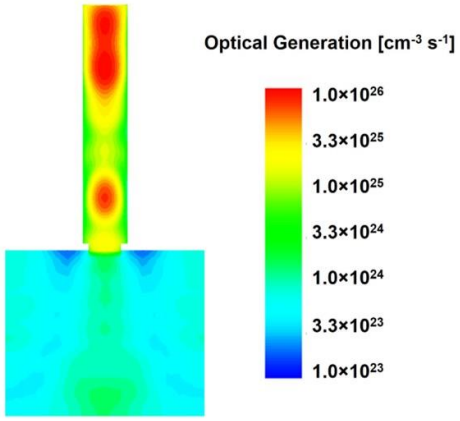

Figure 2-5 FDTD simulation showing optical generation under top illumination at 633 nm with an incident power of 178 W/cm^2.

2.2.5 Electrical transient simulation and material parameters

The last step is to perform transient simulations of band-to-band radiative recombination of GaAs segments (including GaAs seeding layers) at 875 nm by coupling drift-diffusion and continuity equations with optical generation profile solved using FDTD. Since the repetition rate

of laser pulse is 40 MHz, far beyond the time required for the system to revert to equilibrium, we only simulate one cycle of TRPL. To reproduce a transient process, we treat the temporal profile of the 'laser beam' as a Gaussian distribution — the pulse peaks at 60 ps and the pulse width is defined as 30 ps.

As mentioned above, three types of material properties are included in the model: mobility (μ), SRH recombination lifetime (τ_{SRH}), and surface recombination velocity (S_n) at the interface. Therefore, there are five variables in total: the electron mobility of the nanowire (μ_{n_wire}) and the seeding layer (μ_{n_seed}), the SRH recombination lifetime of the nanowire (τ_{SRH_wire}) and the seeding layer (τ_{SRH_seed}), and surface recombination velocity (S_{n_hetero}) at GaAs-Si heterointerface. The material properties of Samples B to D will be determined later by fitting to the experimental TRPL curves in Fig. 2-3. Samples A and E are not included in the transient simulations due to their low vertical yield, where the optical periodic boundary conditions no longer apply. The randomly located irregular polycrystalline structures and tilted nanowires are attributed to the formation of multiple types of nucleation during seeding layer growth.[5] Therefore, it is fair to expect that the material quality of seeding layers grown at different temperatures varied. Additionally, crystal defects are clearly observed by TEM, and thus the electron mobility of these GaAs nanowires is expected to be much lower than that of thin-film GaAs or VLS GaAs nanowires due to stronger scattering.

Based on an initutive understanding of material properties and their qualities, we set the values of each material property as follows to fit TRPL curves: (1) electron mobility of nanowire μ_{n_wire} 10 – 500 $cm^2/(V \cdot s)$, (2) electron mobility of seeding layer μ_{n_seed} 0.5 – 10.0 $cm^2/(V \cdot s)$, (3) SRH recombination lifetime of nanowire τ_{SRH_wire} 1.0 – 5.0 ns, (4) SRH recombination lifetime of seeding layer τ_{SRH_seed} 0.1 – 1.0 ns, and (5) surface recombination velocity at the nanowire-

substrate heterointerface S_{n_hetero} 1.0×10^{0} – 1.0×10^{6} cm/s. Note that the nonradiative SRH recombination lifetime is considered as a variable, while a constant bulk radiative recombination coefficient of 2.0×10^{-10} cm^3/s is applied to both the nanowire and the seeding layer segments. Additionally, Auger recombination is not significant due to a low incident laser power. Based on bulk values, the hole mobility (μ_p), i.e., the mobility of the majority carrier, is set as 10 times less than the electron mobility (μ_n) (a default setting). The surface recombination velocity at the nanowire-air interface (S_{n_air}), i.e., at the GaAs-AlGaAs heterointerface, is fixed at 1.0×10^{3} cm/s, based on the suggested values in some published studies.[6,7] All other material parameters are set as default values offered by the material database in the simulator.

2.2.6 Minority carrier lifetimes from TRPL measurements

Compared with the reported studies of intrinsic GaAs nanowires on Si,[8,9] the Zn-doped GaAs with a 600°C seeding layer (Sample C) shows a comparable minority carrier lifetime (τ_n) of 1.25 ns. Clearly, τ_n is largely affected by the seeding growth temperature (T_{Seed}), as shown in the inset of Fig. 2-3. Here, we note a rapid decrease of τ_n from 1.25 ns to a much lower value less than 1 ns while T_{Seed} is away from 600°C, which might be due to an increase of local defect density inside the GaAs seeding layer or at the GaAs-Si heterointerface. As expected, τ_n has a positive correlation with the vertical yield of nanowires because τ_n of individual irregular polycrystalline structures are expected to be shorter. Further, it is found that although the growth yield and uniformity of Samples B and C are comparable, the carrier lifetimes are much different. Thus, we suspect that the quality of GaAs seeding layers have an impact on the material properties of the upper GaAs segments – which is a fair assumption for heteroepitaxy. This fact, in turn, supports our core arguement that the measured lifetime is a convolution of multiple recombination machnisms which cannot be simply deconvolved without detailed analysis of 3-D carrier dynamics.

In the transient simulations, we take this aspect into account by varying the properties of seeding layers and nanowire segments simaultanouly.

2.2.7 Impact of material properties on carrier lifetime

To study the impact of material properties on carrier lifetime, we first investigate the contributions from nanowire electron mobility μ_{n_wire} (10 – 500 $cm^2/(V \cdot s)$) as well as surface recombination velocity at the GaAs-Si heterointerface S_{n_hetero} (1.0×10^0 – 1.0×10^6 cm/s) while τ_{SRH_wire} (5 ns) and τ_{SRH_seed} (1 ns) are kept fixed. Since the GaAs seeding layer is grown at a much lower temperature, we expect that the material quality of the seed to be much different from that of the nanowire, which is similar to the case for thin-film low-temperature GaAs (LT-GaAs). For starters, we assume μ_{n_seed} (1 – 50 $cm^2/(V \cdot s)$) is one tenth of μ_{n_wire} (10 – 500 $cm^2/(V \cdot s)$). Fig. 2-6(a) shows a contour plot of τ_n as a function of μ_{n_wire} and S_{n_hetero}, which is also marked by three contour lines at 0.84 ns, 1.25 ns, and 0.73 ns, corresponding to the measured τ_n of Samples B through D, respectively. Note that by only changing S_{n_hetero}, τ_n cannot vary from 0.73 ns to 1.25 ns. This significantly suggests that other material properties apart from S_{n_hetero} must be concurrently changed while the seeding layer growth temperature is altered. More simulated τ_n corresponding to other material properties will be given in the later discussion.

The variation of τ_n due to electron mobilities is remarkable – the value spans from 0.029 ns to 2.042 ns with S_{n_hetero} of 1.0×10^0 cm/s while it varies from 0.027 ns to 1.876 ns with S_{n_hetero} of 1.0×10^6 cm/s. It is observed that the change of τ_n exhibits more significant dependency on electron mobility than on surface recombination velocity at the heterointerface. With larger mobility, the diffusion of electrons will be enhanced, which can be explained by the Eisntein relation $D_n = \mu_n k_B T$, where D_n is the diffusivity of electrons, k_B is the Boltzmann constant, and T is the lattice temperature. Due to the large surface-to-volume ratio of nanowires, the carriers are

likely to recombine at the nanowire sidewalls before diffusing to the GaAs-Si heterointerfaces, and thus the nonradiative recombination at the GaAs-Si heterointerfaces is not a dominant contributor to carrier dynamics. Nonetheless, this might not be the case if the aspect ratio of the nanowire, i.e., the ratio of height to diameter, is lower, or the diameter of nanohole is larger, leading to a higher probabilty for carriers reaching the heterinterface . Fig. 2-6(b) illustrates the simulated TRPL curves, i.e., radiative recombination of GaAs as a function of time, with a constant S_{n_hetero} of 1.0×10^{0} cm/s and a series of μ_{n_wire} from 10 $cm^2/(V\cdot s)$ to 75 $cm^2/(V\cdot s)$. The intensity of emission reaches a maximum at 60 ps and then starts to decay along with carrier diffusion and recombination. The overall τ_n varies from 2.04 ns to 0.55 ns, which reveals the large impact of electron mobility on carrier recombination. Note that the change in τ_n is almost neligible while S_{n_hetero} varies within $1.0\times10^{0} - 1.0\times10^{3}$ cm/s, only becoming noticeable with larger S_{n_hetero}, suggesting that nonradiative recombination at heterointerfaces is dominant compared to recombination at other surfaces.

So far, we have fixed τ_{SRH_wire} at 5 ns and τ_{SRH_seed} at 1 ns, which would presumably be high for GaAs nanowires grown on Si substrates. Interestingly, we find that τ_n can be as low as tens of ps with high carrier mobility and significant carrier diffusion. Therefore, observing a short carrier lifetime in nanowires does not necessarily mean that the actual radiative/nonradiative lifetimes are short or material properties are imperfect—the impacts of carrier mobility, nonradiative recombination at surfaces, as well as 3-D geometry (surface-to-volume ratio) must be taken into account, and can only be deconvolved using a computatiaonal 3-D model. Based on the results given in Fig. 2-6, it is fair to assume that the simulated τ_n with S_{n_hetero} of 1.0×10^{0} cm/s sets the upper limit, and the actual τ_n would be shorter due to smaller values of actual τ_{SRH_wire} and τ_{SRH_seed}. Since μ_{n_wire} yields a mobility of 10 – 75 $cm^2/(V\cdot s)$ (more likely toward 10 $cm^2/(V\cdot s)$), we fix the value at 25 $cm^2/(V\cdot s)$ in the next step, which is close to a reported carrier mobility of 31 $cm^2/(V\cdot s)$

for *p*-type GaAs nanowires.[10] Indeed, we raise a concern in a previous section that the quality of seeding layers might affect the material properties of GaAs nanowires, meaning that μ_{n_wire} might not be a constant in Samples B to D. Still, we intentionally keep μ_{n_wire} fixed for the remaining simulations for the following reasons. First, the carrier mobility of III-V nanowires is predominantly determined by the density of polytypisms and stacking faults, which is found to be related to the growth temperature for selective-area GaAs nanowires. Since the nanowire segements are grown at the same temperature (730°C),[11] it is reasonable to assume the carrier mobility remains the same as well. Second, it is computationally easier to fix μ_{n_wire} in order to unveil the correlations between τ_n and other materail peroperties.

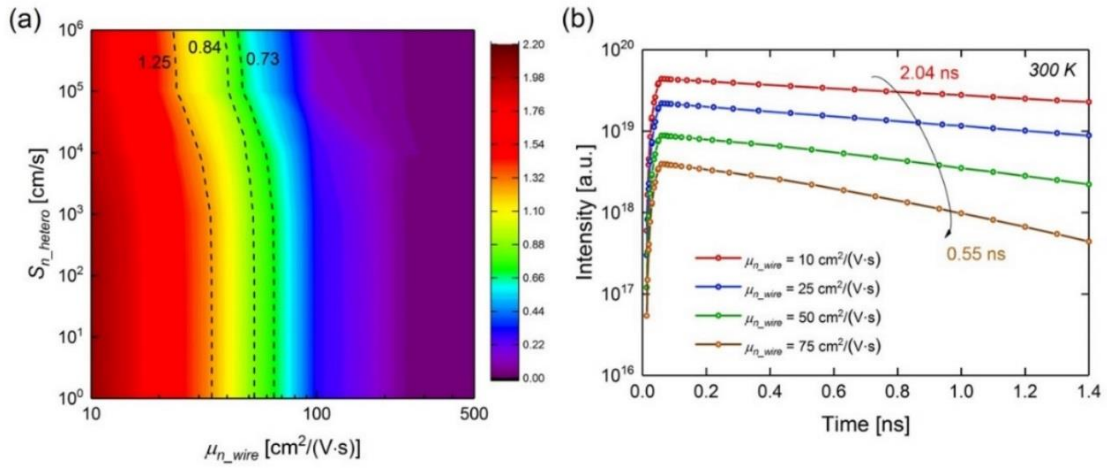

Figure 2-6 Determining electron mobility of GaAs nanowire μ_{n_wire}. (a) Contour plot of simulated minority carrier lifetime τ_n as a function of μ_{n_wire} (10 – 500 cm^2/(V·s)) and S_{n_hetero} (10^0 – 10^6 cm/s) for selective-area GaAs nanowires on Si for minority carrier lifetime simulation. Three contour lines correspond to the measured lifetime of Samples B to D: 0.73 ns, 1.25 ns, and 0.84 ns, respectively. (b) Simulated TRPL spectra at room temperature with different μ_{wire} of 10 cm^2/(V·s), 25 cm^2/(V·s), 50 cm^2/(V·s), and 75 cm^2/(V·s), which correspond to τ_n of 2.04 ns, 1.47 ns, 0.89 ns, and 0.55 ns, respectively. The values of other material properties used in the simulation are as follows: μ_{n_seed} = 0.1× μ_{n_wire}, τ_{SRH_wire} = 5 ns, and τ_{SRH_seed} = 1 ns.

Next, we vary four other material properties: τ_{SRH_wire} (1 – 5 ns), τ_{SRH_seed} (0.1 – 1.0 ns), S_{n_hetero} (1.0×10^0 – 1.0×10^6 cm/s), and μ_{n_seed} (0.5 – 10 $cm^2/(V\cdot s)$). Fig. 2-7(a) shows four 3-D contour plots of τ_n as a function of τ_{SRH_wire}, τ_{SRH_seed}, and S_{n_hetero} with a constant μ_{n_seed} of 0.5 $cm^2/(V\cdot s)$, 1.0 $cm^2/(V\cdot s)$, 5.0 $cm^2/(V\cdot s)$, and 10.0 $cm^2/(V\cdot s)$, respectively. Similar to the previous case, increasing μ_{n_seed} results in a decrease of τ_n, suggesting that carriers tend to diffuse a longer distance to the GaAs-Si heterointerface and then recombine. As for SRH recombination, τ_{SRH_wire} has a larger impact on τ_n than τ_{SRH_seed}, which is because the nanowire segment carries more minority carriers due to its larger spatial volume than the seeding layer. As for S_{n_hetero}, it barely affects τ_n while it is smaller than 1.0×10^4 cm/s; however, its impact on τ_n becomes more significant when the value is larger than 1.0×10^4 cm/s.

To further investigate the correlation between τ_n and material properties, we resummarize the lifetime information from each coutour plot in Fig. 2-7(a) and replot it in box charts, as shown in Fig. 2-7(b). Each box (shown in green) in Fig. 2-7(b) presents a range of τ_n while altering τ_{SRH_seed} (1 – 5 ns) and S_{n_hetero} (1.0×10^0 – 1.0×10^6 cm/s) and keeping τ_{SRH_wire} and μ_{n_seed} fixed. In other words, the box offers estimated values of τ_n for different growth conditions of the GaAs seeding layer and the GaAs-Si heterointerface. Moreover, each box chart is labeled with three dashed lines, showing the boundaries of measured τ_n, i.e., 1.25 ns, 0.84 ns, and 0.73 ns, of Samples B to D. Clearly, with decreasing μ_{n_seed}, τ_n is more sensitive to the local nonradiative recombination in seeding layers and nanowire segments due to a less significant diffusion of carriers. Additionally, with longer τ_{SRH_wire}, it is more likely that electrons in the nanowire segments can diffuse into the seeding layer before being recombined – the overall τ_n exhibits more dependency on material properties of the seeding layer. Thus, we once again conclude that τ_n is not positively correlated to

the material quality of either seeding layer or nanowire segment. Without determining the carrier mobility, it is illogical to attribute measured lifetime to any recombination mechanisms.

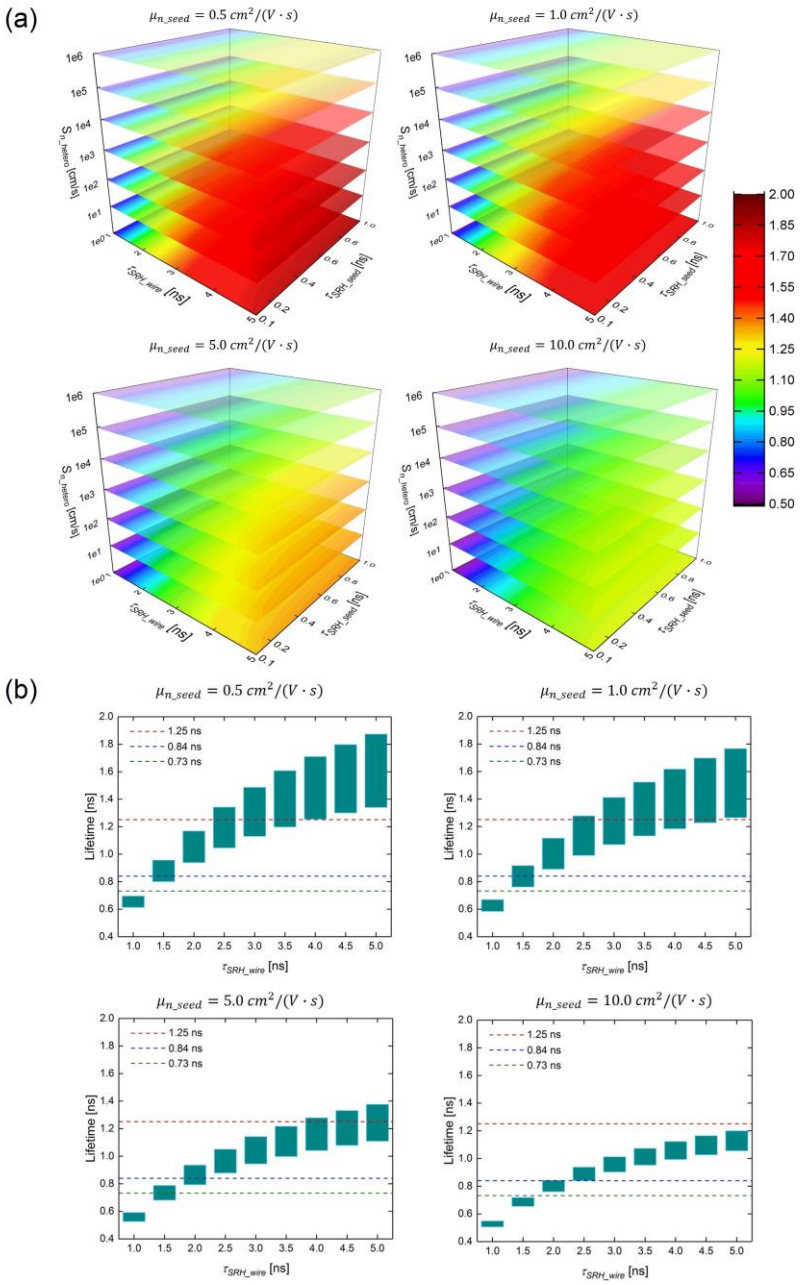

Figure 2-7 The correlation between minority carrier lifetime τ_n and other four material properties μ_{n_seed}, τ_{SRH_wire}, τ_{SRH_seed}, and S_{n_hetero}. (a) 3-D contour plots of simulated τ_n as a function of τ_{SRH_wire} (1 – 5 ns), τ_{SRH_seed} (0.1 – 1 ns), and S_{n_hetero} (10^0 – 10^6 cm/s). The electron mobility of seeding layer μ_{n_seed} is fixed for each plot. (b) Box charts summarizing all values of τ_n as a function of τ_{SRH_wire} based on (a).

We further note that no single box in those four charts is able to cover a full range of τ_n from 0.73 ns to 1.25 ns, meaning that τ_n cannot be varied from 0.73 ns to 1.25 ns by changing either τ_{SRH_seed} or S_{n_hetero}. In other words, the variation of lifetime between Samples B to D cannot be simply attribued to a difference in GaAs-Si heterointerface quality – other material properties contribute as well. It is highly possible that the quality of the GaAs seeding layer has a significant impact on the upper GaAs segment—the material quality of the nanowire is concurrently degraded while the growth temperature of the seeding layer is lower or higher than 600°C. Although the growth conditions, i.e., growth temperature, growth time, and gas flows, of nanowire segments for Samples A to E are consistent, local defects might be introduced at the seed-nanowire interface and then affect the growth quality of nanowire segments, which eventually causes a difference in nonradiative recombination mechansim in nanowire segments. Note that the seeding layer acts as a buffer layer between the lattice mismatched GaAs nanowires and Si substrates. It is well known that the quality of this buffer layer affects the quality of the material grown atop in thin-film epitaxy (e.g. GaAs grown on Si(001))[12-14] – the same should apply to nanowires.

2.2.8 Final fitting of material properties

Equipped with the insights into recombination machnisms of carriers, we now perform a numerical analysis to estimate reasonable values of τ_{SRH_wire}, τ_{SRH_seed}, S_{n_hetero} and μ_{n_seed}. As shown in Fig. 2-7(b), with μ_{n_seed} = 10.0 cm^2/(V·s), τ_n cannot be over 1.25 ns, indicating that the actual mobililty of all those samples should be lower. To cover a span of τ_n from 0.73 ns to 1.25 ns, the ranges of τ_{SRH_wire} should be within 1.2 ns and 2.3 ns, 1.4 and 2.5 ns, or 1.4 and 4.0 ns for μ_{n_seed} = 0.5 cm^2/(V·s), 1.0 cm^2/(V·s), or 5.0 cm^2/(V·s), respectively. We expect that the material quality of both the nanowire and seeding segments of Sample C is the best among all samples. Thus, it is desired that the line of 1.25 ns crosses the top portion of the box where τ_{SRH_seed} is high and S_{n_hetero}

is low, while the bottom boundary of 0.73 ns intersects the bottom part of the box. It is more likely that μ_{n_seed} is less than 5.0 $cm^2/(V \cdot s)$, because we expect that the change of τ_{SRH_wire} resulting from the seeding layer growth temperature is significant and might be around 1 ns or so.

Based on these assumptions, we suggest values for each material property, as listed in Table 2-1. Fig. 2-8 illustrates the simulated TRPL curves that fit experiments (in Fig. 2-3) by using suggested values listed in Table 2-1. It is clear that the measured τ_n shows a strong dependancy on not only one but several recombination mechanisms. Since the carrier mobilities and radiative recombination rate are kept fixed for Samples B to D, we can safely assume that the radiative recombination lifetimes of those samples are approximately the same. As a result, the major recombination mechanisms that lead to the change of τ_n are all attributed to nonradiative recombinations due to trap/defect states at GaAs-Si heterointerfaces and AlGaAs-GaAs surfaces, and within nanowire. Further, the probabliliby of carriers being recombined also depends on the actual 3-D geometry of nanowire. Thus, we demonstrate here that the lifetime and material properties of a 3-D nanowire are certainly intercorrelated instead of in a simple one-to-one correlation.

Sample	T_{Seed} **(°C)**	τ_n **(ns)**	μ_{n_wire} **($cm^2/(V \cdot s)$)**	μ_{n_seed} **($cm^2/(V \cdot s)$)**	τ_{SRH_wire} **(ns)**	τ_{SRH_seed} **(ns)**	S_n **(cm/s)**
B	550	0.84	25	1	1.5	0.2	1.0×10^4
C	600	1.25	25	1	2.5	0.3	1.0×10^2
D	625	0.73	25	1	1.4	0.1	1.0×10^5

Table 2-1 Suggested fitting values of material properties for Sample B, Sample C, and Sample D with seeding layers grown at different temperatures.

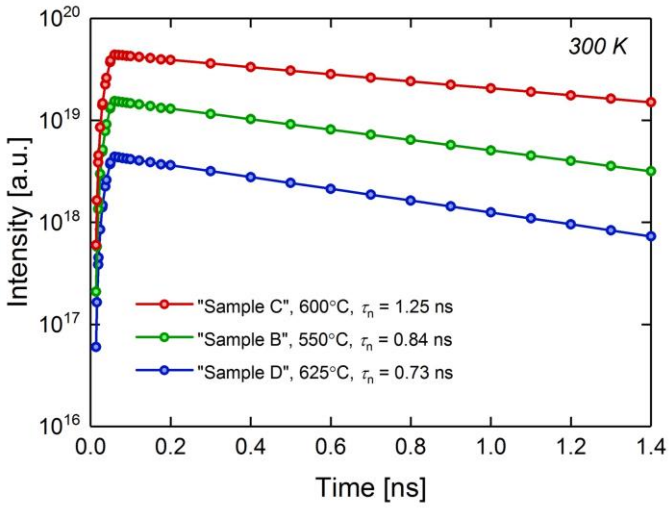

Figure 2-8 Simulated TRPL spectra at room temperature with fitting values listed in Table 2-1.

2.2.9 3-D carrier dynamics

The temporal and spatial information of electron distribution provides a further insight into carrier motions and the recombination mechnisms of 3-D nanostructures. Thus, our final step is to show the capability of mapping real-time carrier dynamics using the 3-D transient model. The simulated spatial distributions of electrons at different points of time, i.e., 30 ps, 60 ps, 100 ps, 300 ps, 600 ps, and 1000 ps, for Samples B through D are illustrated in Fig. 2-9. At the intial stage, the density of photogenerated minority carriers keeps increasing when the samples are exposed under laser pulses from 10 ps to 60 ps. Then, from 60 ps to 1000 ps, electrons in the nanowire segments start to diffuse either toward the top or downward to the GaAs-Si heterointerfaces, while the density of electrons decreases due to nonradiative recombination within the nanowires or at the interfaces. Similarly, electrons in the Si substrate diffuse toward Si-SiN_x and GaAs-Si interfaces and are then recombined. It is obvious that, starting from 100 ps, the electron density inside the nanowire of Sample C is larger than that of Samples B and D, which is due to a longer τ_{SRH}. We also note that the electron density close to the GaAs-Si heterointerface decreases with increasing S_n from Sample C to Samples B and D. Due to the intrinsic large surface-to-volume ratio for

nanowires, τ_n would be largely affected by aspects of the nanowire itself rather than the nanowire-subtrate heterointerface, unless the recombination in the GaAs seeding layer or at the GaAs-Si heterointerface is dominant, which would surpass the recombination along the nanowire sidewalls. Another possible approach to make recombination at the GaAs-Si heterointerface more significant is to properly design the patterns of nanowire array or nanowire dimensions, which would result in optical generation mostly close to the heterointerfaces.

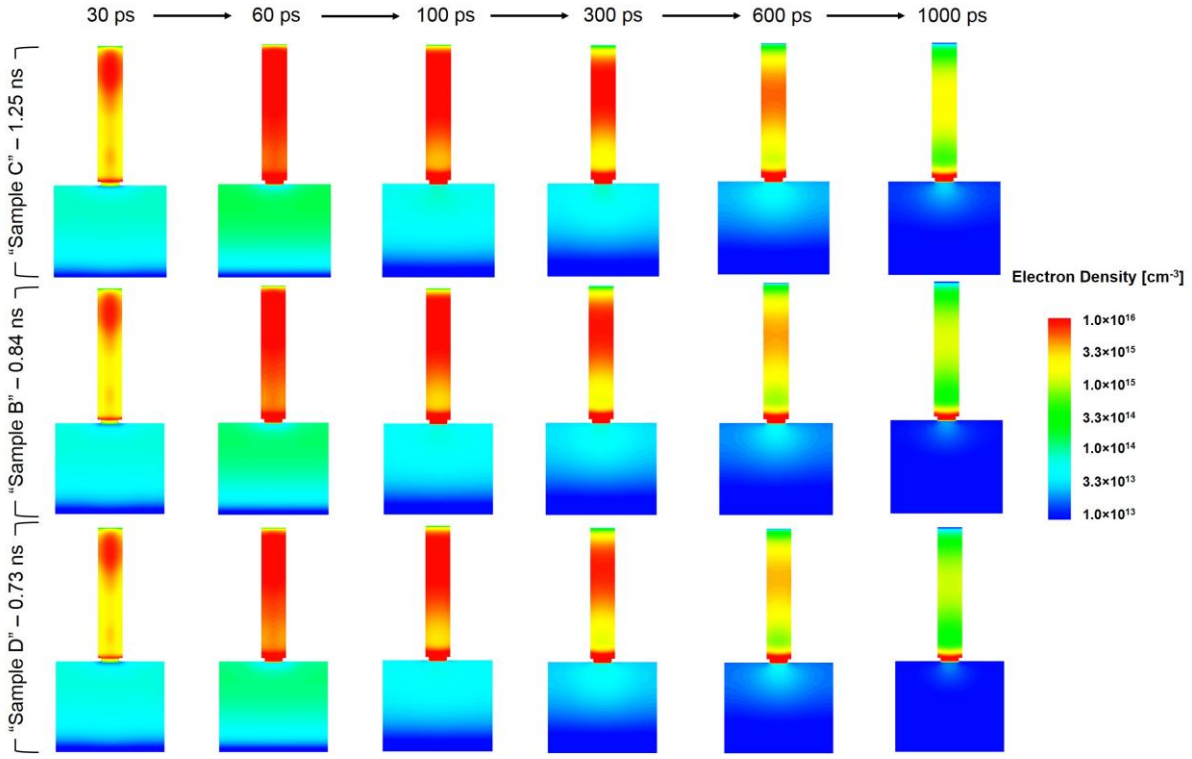

Figure 2-9 Simulated spatial distribution of electrons at different times – 30 ps, 60 ps, 100 ps, 300 ps, 600 ps, and 1000 ps, respectively.

2.2.10 Summary

We investigated the feasibility of unveiling carrier dynamics of 3-D nanostructures using TRPL measurements combined with a 3-D computational transient model. Our goal, as emphasized throughout the study, is to provide a theoretical foundation to concurrently extract multiple material properties by fitting measured TRPL curves. The motivation for the numerical

model is that the 3-D geometries of nanostructures result in more complicated mechanisms of carrier recombination than those in thin films and analytical solutions cannot be simply found. Without losing generality, we considered three material properties as variables, i.e., carrier mobility, SRH nonradiative recombination lifetime, and surface recombination velocity at heterointerfaces. To validate the model, we grew *p*-type GaAs nanowires on *p*-type Si by SA-MOCVD, and then fit the TRPL curves by tuning material properties. We observed that the seeding layers grown at different temperatures resulted in different material properties for nanowires, seeding layers, and GaAs-Si heterointerfaces. Finally, we suggested fitting values for material properties based on a complete set of transient simulations, and further interpreted the carrier dynamics by mapping spatial and temporal electron distributions. We believe the presented theoretical and experimental work will stimulate more validating studies to reveal the inherent capability of TRPL for fundamental research on nanowires and nanostructured materials.

2.3 Transient model – correlation of carrier lifetime and surface recombination velocity

2.3.1 Introduction

The performance of nanowire-based devices is predominantly affected by nonradiative recombination on their surfaces, or sidewalls, due to large surface-to-volume ratios. Nonradiative recombination centers on surfaces, i.e., surface states (or dangling bonds), which are caused by the interruption to the crystal periodicity, leading to higher levels of threshold current and dark current for emitters and detectors, respectively. Such dark current is disadvantageous for energy-efficient and high-temperature operation of emitters and detectors. Thus, it is crucial to quantify the surface

property of nanowires in order to explore the impact of surface states on carrier dynamics and guide the design of nanoscale devices.

Typically, the property of surface recombination is interpreted as surface recombination velocity, in units of cm/s. One technique commonly used to extract the surface recombination velocity of nanowires is to correlate its value with minority carrier lifetime measured by time-resolved photoluminescence (TRPL). This relation is given by a conventional analytical equation expressed as[15]

$$\frac{1}{\tau_{TRPL}} = \frac{1}{\tau_{Bulk}} + \frac{4v_S}{d} \tag{2.3}$$

where τ_{TRPL} is the carrier lifetime measured by TRPL, τ_{Bulk} is the carrier lifetime of the bulk nanowire, v_{S} is the surface recombination velocity at nanowire-air or nanowire-passivation interfaces, and d is the nanowire diameter. This analytical approach has been reported in a broad range of studies on nanowire surface properties, including relaxed and strained GaN nanowires without passivation,[16] Si nanowires coated by amorphous silicon (a-Si),[17] GaAs nanowires covered by *in-situ* AlGaAs layers,[18,19] InGaAs nanopillars passivated by $(NH_4)_2S/SiO_2$ films,[20] and InP nanowires passivated by Al_2O_3/PO_x.[21] However, looking back at the original publication that shows the derivation of Eq. 2.3, we note that the equation is valid only in the condition that the nanowire is an infinitely long cylinder.[15,22] Yet, this is not the case for an actual nanowire, which is hexagonal (terminated by six (0-11) facets) with a certain finite height (or length). Therefore, we surmise that Eq. 2.3 might not accurately solve for nanowire v_{S} and that a comprehensive 3-D computation is required to provide a more accurate analysis.

Here, we have revisited the correlation between carrier lifetime (τ_{TRPL}) and surface recombination velocity (v_{S}) by reproducing TRPL measurements and numerically solving carrier

drift-diffusion with our 3-D transient model. We simulate three cases—first using GaAs nanowires, second with InGaAs nanowires, and the third with InGaAs layer inserts embedded in GaAs nanowires, all of which are on GaAs substrate to encompass common nanowire structures. The first case considers nanowire structures where there are no potential barriers between any junctions to confine minority carriers. The latter two cases are general situations where minority carriers are confined within nanowires as a result of certain energy-band alignments. Our resultant simulations show that the correlation is convoluted, and is determined not only by recombination on surface but also by nanowire geometry, energy-band alignment, and spatial carrier diffusion in 3-D. The first part of this work concerns the validation of our 3-D transient model for nanowire surface recombination by replicating experimental TRPL characterizations of $(NH_4)_2S/SiO_2$ passivated InGaAs/InP nanopillars reported in a previous study.[20] Next, equipped with the modeling capability and the fundamental insight we gain from the first step, we analyze the impact of v_S on τ_{TRPL} in the three cases. If the aforementioned conventional analytical correlation stands, the extracted surface recombination velocity (v_S') from the simulated (or measured) τ_{TRPL} based on the relation in Eq. 2.1 should be equal to v_S set in the transient model. However, we observe that v_S' differs from v_S in most situations with decreasing v_S or increasing d, which indicates that surface recombination velocities derived by Eq. 2.1 are an overestimate. We believe that the complex carrier dynamics in 3-D geometries are responsible for such overestimation. With such structures, the conventional analytical approach is of limited use, and a more comprehensive computation in 3-D can provide more accurate analysis.

2.3.2 Model setup

A unit cell of nanowire arrays is first built to include a single nanowire, a dielectric growth mask (SiO_2), a growth substrate (GaAs), and ambient air. However, a growth mask may not be

necessary in the model if the nanowire growth is self-assembled instead of selective-area. Fig. 2-10 shows the schematics of the three abovementioned nanowire structures—GaAs nanowire, InGaAs nanowire, and InGaAs insert embedded in GaAs nanowire. Then, optical generation (in units of cm^{-3} s^{-1}) is computed using finite-difference time-domain (FDTD) with periodic boundaries along the X and Y directions and perfectly matched layer absorbing boundaries are specified above and below the nanowire unit cell in the Z direction. Next, the drift-diffusion and continuity equations are solved, and band-to-band radiative recombination of (In)GaAs segments is computed as a function of time to obtain temporal TRPL curves. Finally, τ_{TRPL} is extracted from the simulated TRPL curve by fitting an exponential equation with a single decay of $\exp(-t/\tau_{TRPL})$.

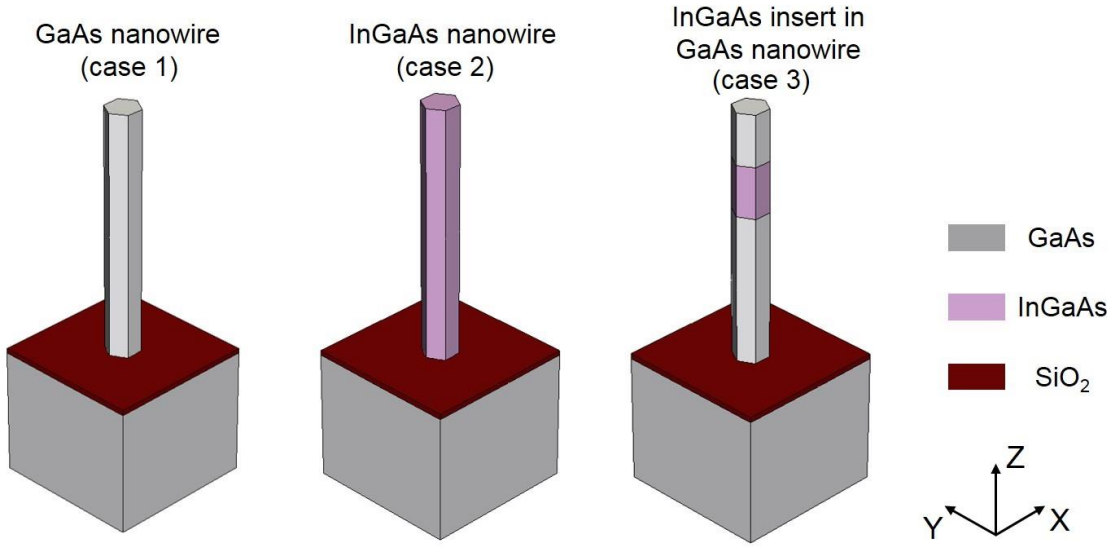

Figure 2-10 Schematic diagrams of three nanowire structures used in the simulations: GaAs nanowire, InGaAs nanowire, and InGaAs insert embedded in GaAs nanowire. All nanowires are on GaAs substrates. For each structure, only a unit cell is shown.

2.3.3 Parameter settings

The temperature is set at 300 K. When reconstructing unit cells of nanowires, we fix the pitch at 600 nm and height at 1 μm for all cases and vary the nanowire diameter (d) at 80 nm, 100

nm, 120 nm, 140 nm, and 180 nm. The thickness of the SiO_2 mask is set to 20 nm (this thickness value may vary depending on the growth structure or material). The indium composition of the InGaAs bulk nanowire and insert is set to 0.13, causing an optical emission peak at 1 μm, which is below the cutoff wavelength of the silicon single-photon avalanche diodes (SPADs). In addition, the lattice mismatch between $In_{0.13}Ga_{0.87}As$ and GaAs is not sufficient to generate any local defects in nanowires.[23] To simplify the structure, we assume that the diameter of a nanohole is the same as that of a nanowire, and we exclude from the model any passivation layer that covers the nanowire surfaces. Instead, v_S is introduced at nanowire-air or nanowire-passivation interfaces on six (110) sidewalls (as discussed later).

In optical simulation, the power intensity of normal incidence is kept fixed at a low level of 10 W/cm^2, which gives a low injection condition. We use a 635 nm wavelength to excite GaAs nanowires and a 965 nm wavelength to excite InGaAs nanowires or inserts. The laser source at 965 nm, beyond the cutoff of GaAs, allows optical generation to occur only in InGaAs segments. Then, the 3-D optical generation profiles are coupled into the electrical transient simulations. A FWHM of 30 ps is set to time-dependent optical generation, and the entire simulation period is set to 10.0 ns, which provides a fair amount of time to observe TRPL decays (or carrier decays) in each case. To investigate the impact of surface recombination on carrier lifetime, only one of the material properties, v_S, is considered a variable, ranging from 1.0×10^1 cm/s to 1.0×10^4 cm/s (1.0×10^1 cm/s, 3.0×10^1 cm/s, 1.0×10^2 cm/s, 3.0×10^2 cm/s, 1.0×10^3 cm/s, 3.0×10^4 cm/s, and 1.0×10^4 cm/s). Some of the material properties of (In)GaAs segments are (1) electron mobility at 1000 cm^2/(V·s),[24-27] (2) hole mobility at 100 cm^2/(V·s),[24-27] (3) Shockley-Read-Hall (SRH) nonradiative recombination lifetime (for bulk nanowires) at 100 ns,[28] and (4) radiative recombination coefficient at 2.0×10^{-10} cm^3/s.[28] Note that at the level of mobility given above, the

diffusion length of either electron or hole is much longer than the nanowire diameter. All other properties used in the simulations are taken from the material database of the numerical simulator.

2.3.4 Extraction of surface recombination velocity

For each case, there are in total 35 computed TRPL curves and their corresponding carrier lifetimes from resultant transient simulations (five values of d and seven values of v_S). At this moment, we treat v_S as the actual surface recombination velocity at nanowire-air or nanowire-passivation interfaces for an as-grown nanowire sample. To analytically obtain the surface recombination velocity, we fit v_S by using Eq. 2.3 to then estimate its value based on the relation shown below:

$$\tau_{TRPL}{}^{-1} = \left(\frac{4}{d}\right) v_S{}' + \tau_{Bulk}{}^{-1} \tag{2.4}$$

Note that we use v_S' to indicate that the value was an experimentally fitted number based on the conventional analytical model. This, then, is the entire process of transient simulation for TRPL measurements, and the model can be easily adjusted and modified for any nanowire structure. One assumption we make in the simulation is that all nanowire unit cells are identical. This is reasonable if the nanowire growth is uniform, but may not hold for non-uniform self-assembled growths with or without catalysts. In such cases, some corrections would be required to modify the model. For instance, a larger unit cell can be used to include multiple nanowires of varying geometrical parameters to approximate a non-uniform array.

2.3.5 Model validation

To demonstrate the rationality of our transient model for nanowire surface recombination, we validate it by replicating the TRPL characterizations in a surface passivation study by the Fiore's group.[20] They demonstrate a strong suppression of surface recombination of InGaAs/InP

nanopillars by using $(NH_4)_2S/SiO_2$ as passivation for InGaAs layers, where TRPL characterizations are performed on a series of nanopillars with different diameters. The best surface recombination velocity fitted by Eq. 2.4 is reported to be 260 cm/s. We reconstruct the same structures using our transient model, and obtain a surface recombination velocity of 242 cm/s, which is very close to the measured value.

2.3.6 The case of GaAs nanowires on GaAs substrates

We first investigate the correlation between τ_{TRPL} and v_S for bulk GaAs nanowires on GaAs substrates. Again, this case produces nanowire growth structures without potential barriers between any junctions to confine minority carriers. Fig. 2-11(a) provides a 3-D map of the optical generation profile at 635 nm for a periodic GaAs nanowire array, where the nanowire pitch and diameter are 600 nm and 120 nm, respectively. Clearly, a large portion of the incident light is concentrated within the nanowires. This is because optical resonant-guided modes that couple normally incident light into periodic 3-D structures lead to an enhancement of the local electromagnetic field intensity.[29,30] Thus, it is fair to assume that the motion of photogenerated carriers is predominantly affected by the nanowire properties. Fig. 2-11(b) illustrates cross-sectional optical generation profiles of unit cells of GaAs nanowires with respect to different diameters, spanning from 80 nm to 180 nm. Note that the photogenerated carriers are not uniformly distributed—there are several "hot spots" inside the nanowires. This will result in an abrupt decay of the TRPL curve at the beginning due to a rapid separation of electrons and holes (an exception is when electron mobility and hole mobility are close). A similar mechanism is discussed in a study on thin-film CdTe solar cells, where the first part of decay in a biexponential TRPL curve is attributed to rapid carrier separation.[31]

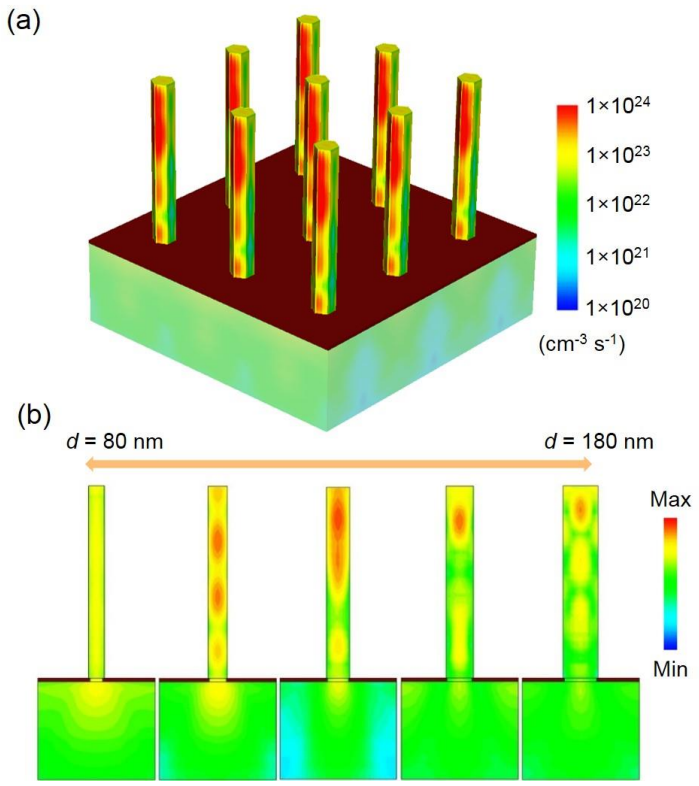

Figure 2-11 (a) 3-D optical generation profile of a periodic nanowire array. The nanowire diameter is 120 nm. (b) Cross-sectional optical generation profiles of GaAs nanowires with diameters (each 20 nm smaller than the next) spanning from 80 nm to 180 nm.

Next, we move on to the electrical simulations. Fig. 2-12 displays the simulated carrier lifetimes and TRPL curves for GaAs nanowires. The top-left contour plot shows the correlation between carrier lifetimes and two nanowire properties: v_S and d. The carrier lifetime is also expressed by three contour lines at 0.70 ns, 0.80 ns, and 0.90 ns. Four subplots show simulated TRPL curves by fixing v_S at 1×10^1 cm/s, 1×10^2 cm/s, 1×10^3 cm/s, and 1×10^4 cm/s. Since all TRPL curves behave as single exponential decays, we extract their corresponding τ_{TRPL} by fitting $\exp(-t/\tau_{TRPL})$ from 2 ns to 5 ns (the curves from 5 ns to 10 ns are not shown). τ_{TRPL}, which is theoretically predicted, can be no more than 1 ns in any case. Furthermore, as v_S decreases, d exhibits a more significant impact on τ_{TRPL}, while surface recombination becomes the dominant factor in the regime where v_S is greater than 1×10^3 cm/s.

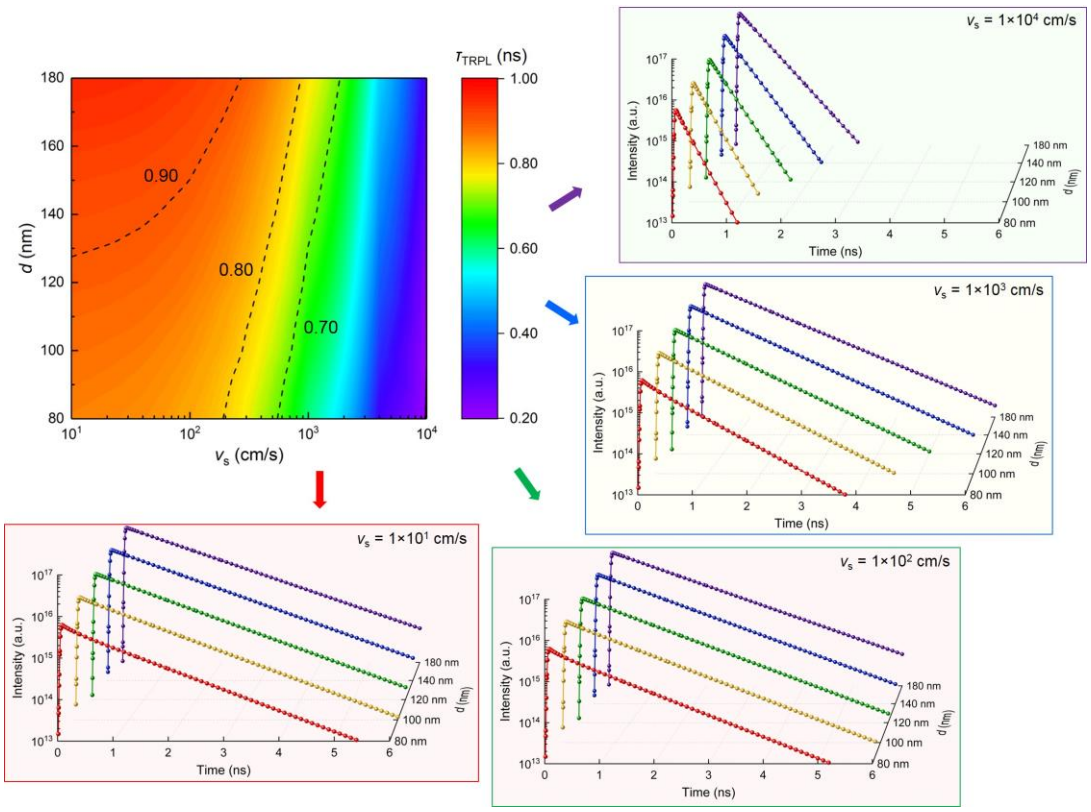

Figure 2-12 Simulated carrier lifetime and TRPL curves for GaAs nanowires on GaAs substrates as a function of surface recombination velocity and nanowire diameter. The contour plot displays a summary of the distribution of τ_{TRPL}, where the three contour lines correspond to the lifetimes of 0.70 ns, 0.80 ns, and 0.90 ns. Four subplots show simulated TRPL curves for fixed v_S of 1×10^1 cm/s, 1×10^2 cm/s, 1×10^3 cm/s, and 1×10^4 cm/s.

In an attempt to understand the underlying physics of carrier behaviors, it is crucial to first recognize that a large portion of carriers are more likely to gradually diffuse from nanowire segments into substrates when there are no potential barriers at the nanowire-substrate interfaces for minority carriers. In other words, carriers are unlikely to recombine on surfaces while the entire system is "open". This helps explain why the experimentally measured τ_{TRPL} for GaAs nanowires grown on GaAs is within a picosecond or nanosecond, regardless of nanowire diameter or surface passivation condition, even when the overall carrier lifetime is short (in spite of a low $v_S < 1\times10^2$ or so).[18,19,32] However, it is still possible to obtain a longer τ_{TRPL} when (1) the nonradiative SRH

recombination lifetime of the bulk GaAs nanowires is long, (2) the carrier mobility is low (or the diffusion length is small), (3) *d* is large, and (4) the TRPL signals are mixed with optical emission from the substrate. With decreasing *d*, the carrier diffusion into substrates is less significant, since more carriers recombine on nanowire surfaces due to high nanowire surface to volume ratio.

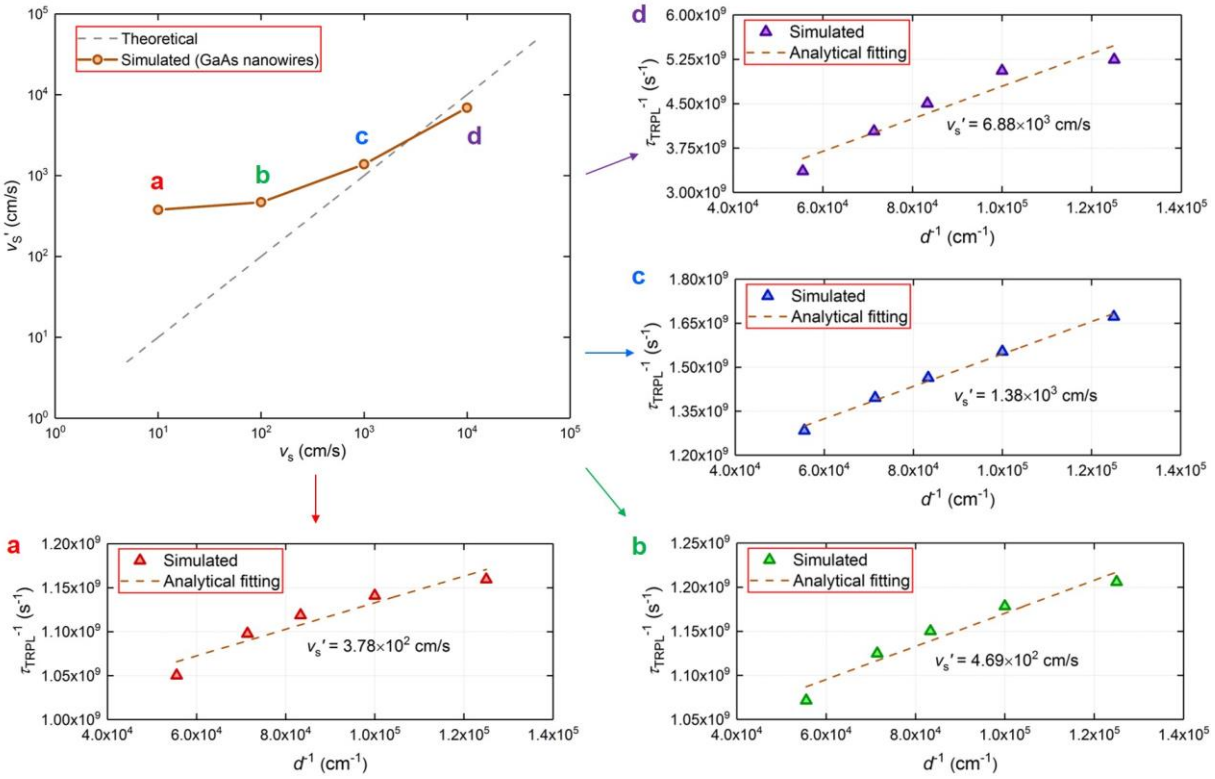

Figure 2-13 Extracted surface recombination velocity (v_S') versus actual surface recombination velocity (v_S), where v_S represents the value used in the simulations (or the actual surface property) and v_S' is the fitted value using the analytical argument given in Eq. 2.4. The dashed line in the top-left plot shows an ideal relation between v_S' and v_S. The fitted surface recombination velocities v_S' for v_S = 1×10^1 cm/s to 1×10^4 cm/s are depicted in subplots a – d: where v_S' = 3.78×10^2 cm/s, 4.69×10^2 cm/s, 1.38×10^3 cm/s, and 6.88×10^2 cm/s, respectively.

After obtaining carrier lifetimes, we start to examine the rationality of the conventional analytical model for nanowire surface recombination velocity, or Eq. 2.3. Again, v_S is the surface recombination velocity we insert into the transient simulations, and thus it can be considered the

"actual" recombination property at nanowire-air or nanowire-passivation interfaces. To analytically extract v_S' using Eq. 2.4, we plot the simulated τ_{TRPL}^{-1} as a function of d^{-1} by fixing v_S at 1×10^1 cm/s, 1×10^2 cm/s, 1×10^3 cm/s, and 1×10^4 cm/s, as shown in subplots a, b, c, and d, respectively, in Fig. 2-13. The fitted values of v_S' for those four values of v_S are 3.78×10^2 cm/s, 4.69×10^2 cm/s, 1.38×10^3 cm/s, and 6.88×10^2 cm/s, respectively. We then summarize the values of v_S and v_S', as illustrated in the top-left plot in Fig. 2-13, where the dashed grey line gives an ideal relation between v_S and v_S' ($v_S = v_S'$). v_S' becomes much larger than v_S when v_S is smaller than 1×10^3 cm/s, suggesting that surface recombination velocities are overestimated by Eq. 2.4 in that regime.

Recall that Eq. 2.3 (or Eq. 2.4) was analytically derived based on the assumption that the nanowire is an infinitely long cylinder. Looking back at the literature, we find that Eq. 2.3 was first derived to calculate the carrier concentration of InGaAs quantum dots by using two-dimensional continuity and boundary conditions.[15,22] However, these boundary conditions are not appropriate for the case of nanowires. More importantly, the traditional analytical argument does not consider carrier diffusion into substrates when there are no potential barriers at nanowire-substrate interfaces. Such rapid diffusion will lead to a significant loss of photogenerated carriers inside nanowire segments. As a result, the entire radiative recombination rate shown in Eq. 2.4, or the intensity of the optical emission, suffers from an abrupt decay, and presumably v_S' becomes small. In addition, with decreasing v_S, v_S' moves further away from v_S because most carriers will tend to diffuse into substrates instead of being recombined on surfaces, resulting in a less significant surface recombination.

To provide further insight into carrier dynamics and recombination mechanisms, we map the temporal and spatial distribution of minority carriers, or holes, across an entire unit cell of

GaAs nanowire. Fig. 2-14 shows the simulated electron distribution for $v_S = 1\times10^2$ cm/s and 1×10^4 cm/s at different times, namely 10 ps, 30 ps, 50 ps, 70 ps, 100 ps, 500 ps, and 1000 ps.

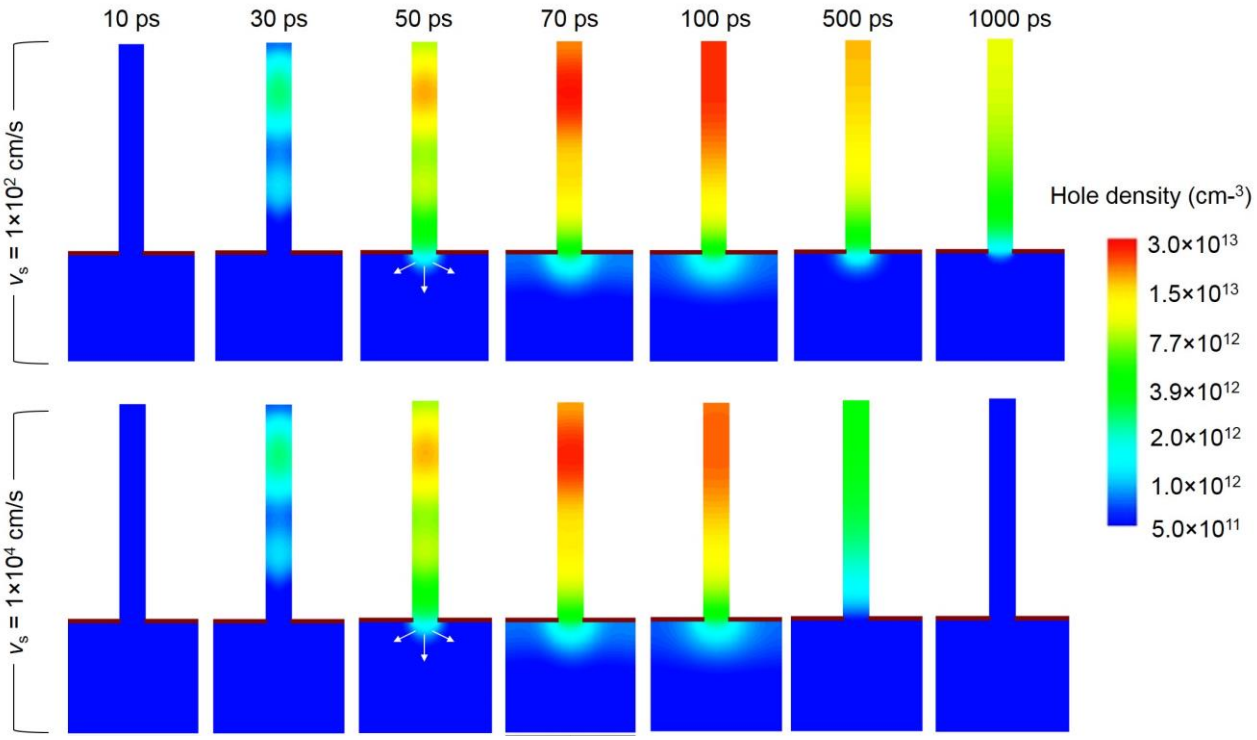

Figure 2-14 Simulated spatial distribution of minority carriers, or holes, in GaAs nanowires for $v_S = 1\times10^2$ cm/s and 1×10^4 cm/s at different points of time: 10 ps, 30 ps, 50 ps, 70 ps, 100 ps, 500 ps, and 1000 ps, respectively. The nanowire diameter is 120 nm. The white arrows indicate the carrier diffusion.

At the beginning, from 0 ps to 70 ps, the density of photogenerated minority carriers increases when the laser pulse (Gaussian) arrives. Then, starting from 70 ps, holes in the nanowire segments rapidly diffuse to the sidewalls and substrates. Similar numbers of carriers diffuse into the substrates, while the holes are recombined faster with increasing v_S. This concurs with our previous observation that with increasing v_S, the decay of TRPL intensity is mostly determined by the surface recombination. In another situation where the surface recombination is dominant, since the surface to volume ratio of nanowires is high, the optical absorption is mostly confined in the

nanowire segments. In short, if the actual 3-D nanowire geometry is not fully considered, the v_S' will be overestimated.

2.3.7 The case of InGaAs nanowires and inserts on GaAs substrates

Turning now to InGaAs nanowires and InGaAs inserts, we first look at the optical generation in both cases, as shown in Fig. 2-15(a). Since the excitation wavelength (965 nm) is beyond the cutoff wavelength of GaAs, all carriers are generated inside InGaAs segments. Note that InGaAs-GaAs forms a type-I heterojunction, as illustrated in Fig. 2-15(a), and thus photogenerated carriers are mostly confined without diffusing away. Indeed, the diffusion would still occur due to thermionic emission; however, the fraction of carriers are much less than those in the GaAs nanowires discussed in the previous case. Similarly, we analytically extract v_S' using Eq. 2.4 for v_S ranging from 1×10^1 cm/s to 1×10^4 cm/s, as shown in Fig. 2-15(b). Remarkably, the discrepancy between v_S and v_S' is much less. Such a difference is attributable to the recombination on the top and bottom surfaces of InGaAs segments, i.e., the top InGaAs-air interfaces and bottom InGaAs-GaAs (substrate) heterointerfaces in the case of InGaAs bulk nanowires, and both the top and bottom InGaAs-GaAs heterointerfaces in the case of InGaAs inserts.

Since the lattice mismatch between $In_{0.13}Ga_{0.87}As$ and GaAs is small, the surface recombination velocity at heterointerfaces would be much smaller than that at semiconductor-air interfaces. As a result, the conventional analytical model becomes more accurate. Still, when v_S is smaller than 1×10^2 cm/s, v_S' will be slightly overestimated. Fig. 2-15(c) shows contour plots of computed τ_{TRPL} for both cases. Compared with the distribution of τ_{TRPL} for GaAs nanowires shown in Fig. 2-13(a), the ones given in Fig. 2-15(c) show less dependence on d, indicating, again, that the carrier diffusion into substrates and the surface recombination on top or bottom surfaces are less significant.

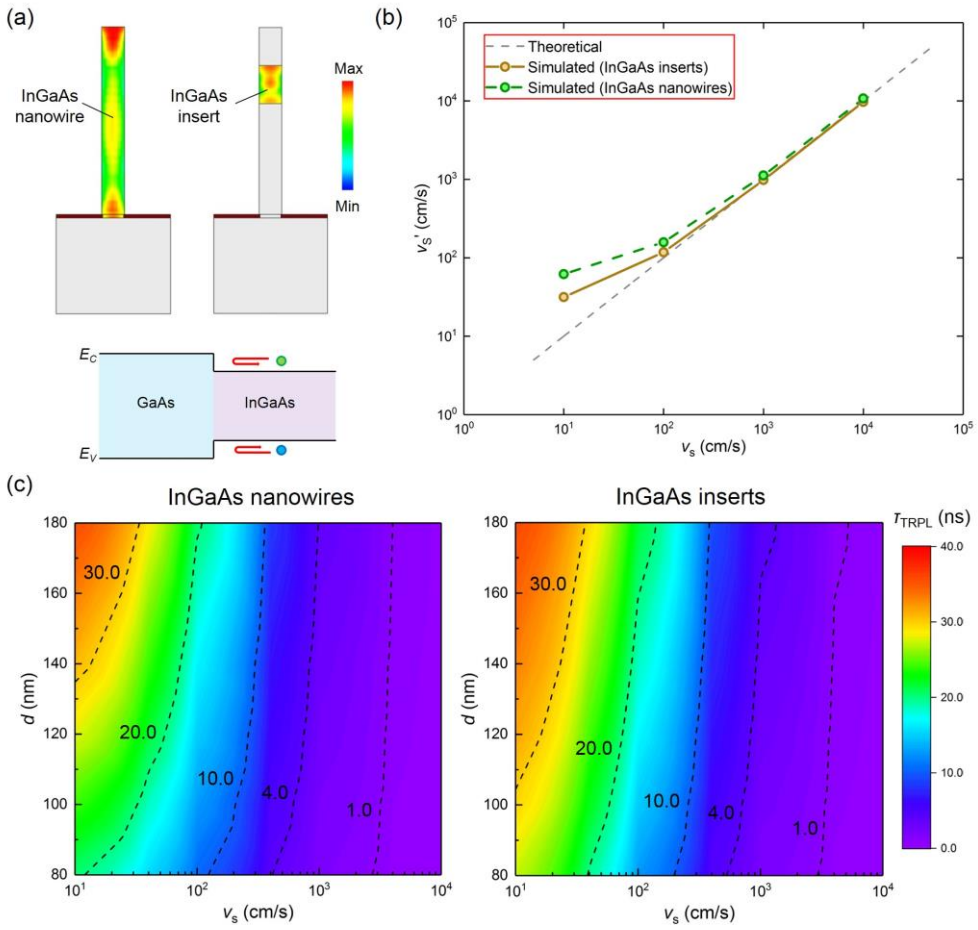

Figure 2-15 The resultant simulations for the case of InGaAs nanowires and the case of InGaAs inserts. (a) Cross-sectional optical generation profiles of unit cells for both cases with a nanowire diameter of 120 nm. The schematics on the bottom show the energy-band alignment (type-I) of a InGaAs-GaAs heterojunction, where carriers are confined in the InGaAs segment. (b) Extracted surface recombination velocity (v_S') versus actual surface recombination velocity (v_S). (c) Contour plots of simulated carrier lifetimes for InGaAs nanowires and InGaAs inserts, respectively, as a function of v_S and d, where the five contour lines correspond to the lifetimes of 1.0 ns, 4.0 ns, 10.0 ns, 20.0 ns, and 30.0 ns.

2.3.8 Conditions of reasonable applicability of the analytical model

Equipped with a comprehensive understanding of the correlation between τ_{TRPL} and v_S, we can critique the applicability of the conventional analytical model. In most cases, unfortunately, a fair conclusion cannot be made about the quality of nanowire surfaces without a complete analysis

of the carrier dynamics in 3-D by considering the actual geometry of the nanowire. We suggest that it is more reasonable to analytically solve v_S for thin films, since they can be simply considered as 1-D slices by assuming that the in-plane areas are infinite. In other words, setting electrical boundary conditions in 1-D is more straightforward. However for 3-D nanowire structures we summarize several conditions for the reasonable applicability of the analytical model presented in Eq. 2.3 (or Eq. 2.4) : (1) the nanowire aspect ratio (L/D) is extremely high so as to assume it "infinitely" long; (2) the minority carriers can be mostly confined within the nanowire segment resulting from certain energy-band alignments; (3) the carrier diffusion into substrates is not adequate; (4) the recombination at both the top and bottom interfaces of the nanowire segment is much less significant than the surface recombination on the sidewalls; and (5) the diffusion length of the minority carriers is much longer than the nanowire diameter, and therefore the carriers can reach surfaces before being recombined by other bulk nonradiative mechanisms. Thus, it is critical to carefully consider these prerequisites before implementing the analytical model to solve surface recombination velocities for nanowires. Indeed, Eq. 2.3 (or Eq. 2.4) can obtain an approximate upper limit of surface recombination velocity, or in other words, the worst-case scenario of the surface recombination.

2.3.9 Summary

We applied a 3-D transient model to numerically thoroughly investigate the correlation between carrier lifetime and surface recombination velocity for nanowire time-resolved photoluminescence characterizations. We questioned the conventional analytical model that is widely implemented to interpret such correlation. The conclusion is rather straightforward: with the analytical model, the extracted surface recombination velocity is normally overestimated, and this flaw can be corrected by performing complete 3-D transient modeling. To arrive at this insight,

we made three common nanowire structures—a GaAs nanowire, an InGaAs nanowire, and an InGaAs insert in GaAs nanowire—and then computationally explored the impact of surface recombination velocity on carrier lifetime. We found, based on the resultant simulations, that the actual correlation was convoluted and determined by not only surface recombination but also by nanowire geometry, energy-band alignment at the heterointerface, and spatial carrier diffusion in 3-D nanostructures.

2.4 Photoresponse model for responsivity and detectivity

2.4.1 Introduction

Semiconductor nanowires are frequently highlighted as promising building blocks for next-generation photodetectors. Their unique properties, namely small junction area and heteroepitaxy of different bandgap materials, are advantageous for significantly suppressing dark current from generation-recombination and minority carriers. This capability can lead to a higher signal-to-noise ratio (SNR) and pave the way to accomplish room-temperature operation of small bandgap detectors with higher detectivities.[33] Here, we investigate the theoretical responsivity and detectivity for nanowire photodetection at short-wavelength infrared (SWIR) and mid-wavelength infrared (MWIR) using our 3-D computational photoresponse model. Note that this model can be easily applied to any type of nanostructured photodetectors in any wavelength spectrum. The nanowire photodetector array is composed of selective-area *n*-type InAs(Sb) nanowire photoabsorbers grown on *p*-type InP substrates and 3-D plasmonic gratings.[34,35] The resultant simulations show a remarkable reduction of dark current with high optical absorption in nanowires through excitation of surface plasmonic waves at metal-nanowire interfaces. Furthermore, we compare the computed responsivity and detectivity with the performance of the best planar InAs

photovoltaic *p-i-n* photodiodes. Our modeling work shows that, through sophisticated optical and electrical designs, nanowire-based photodetectors can demonstrate equivalent or better performance than their planar device counterparts for photodetection at SWIR and MWIR.

2.4.2 Model setup

A unit cell of nanowire arrays is first constructed to include a single InAs(Sb) nanowire, a dielectric growth mask (SiO_2), a growth substrate (InP), a benzocyclobutene (BCB) layer, a metallic grating, and ambient air. To better discuss the feasibility of room-temperature operation of nanowire photodetectors at SWIR and MWIR, we replicate the measured characteristics of InAs photovoltaic diodes and compare the figure of merits, i.e., responsivity and detectivity, with those of nanowire photodetectors. Fig. 2-16 shows the schematics of the nanowire photodetector and the planar thin-film InAs *p-i-n* photodiode.[33,36]

The optical absorption is solved in Lumerical FDTD. A 1 – 4 μm wavelength spectrum is selected, and the refractive index *n* and the extinction coefficient *k* of InAs(Sb) is obtained from a previously reported study.[37] Periodic boundary conditions are set at *x* and *y* directions, while perfectly matched layer (PML) boundary conditions are applied above and below the nanowire array (*z*-direction). The nanowire diameter is set as 210 nm, while the nanowire pitch P_x and P_y are both set to 1300 nm. The thickness of the Al_2O_3 passivation layer is 60 nm. To simulate absorption of unpolarized light, we take note of the asymmetry of the nanowire photodetector on *x* and *y* directions and set the incident light source to 45°-polarized, which contains both *x*-polarized and *y*-polarized components.

Then, the simulated electric profiles from 1 – 4 μm (in FDTD mesh grids) are incorporated into the finite-element mesh (FEM) grids so that it can be imported into the electrical simulator (Synopsys Sentaurus TCAD) to determine the photocurrent. The FEM grids are previously

generated in TCAD, based on the exact same dimensions of the optically simulated structure (without the metallic gratings, which are replaced by the electrical boundary conditions as shown in Fig. 2-16). Note that the electric profiles at different wavelengths solved by the optical simulator are based on a unique optical input power (in arbitrary units). Additionally, the drift-diffusion and continuity equations are solved, allowing for the dark and optical current to be extracted. Unlike the transient model, we set the optical generation "ON" during the entire simulation. Finally, since the TCAD numerical simulator cannot compute current at 0 V, we use 0.0001V to represent the photovoltaic mode.

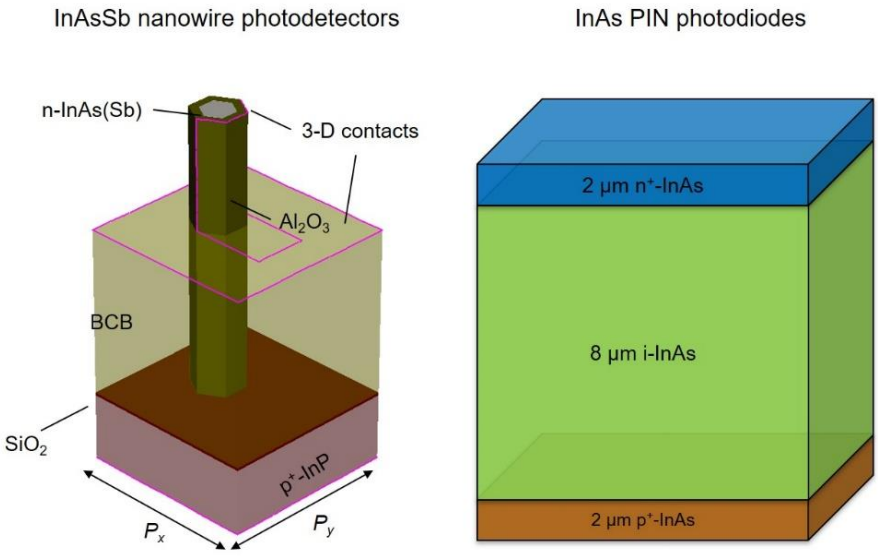

Figure 2-16 Schematics of the 3-D InAsSb nanowire photodetectors and the planar InAs photodiodes. P_x and P_y indicate the pitches of nanowires on x and y directions, respectively. The structure of InAs photodiodes follows a reported study.[36]

2.4.3 Parameter settings

All the simulations are performed at 300 K. To study the theoretical, or ideal, responsivity and detectivity of the nanowire photodiodes, we use the material properties of thin-film InAs for InAsSb nanowires. Note that the bandgap of InAs nanowires grown by catalyst-free selective-area

mode is at about 0.477 – 0.496 eV, much different from the zinc-blende InAs bandgap of 0.364 eV at 300 K. It is mainly due to a high-density of rotational twins, i.e., crystal phase switches between zinc-blende and wurtzite, which is commonly observed in InAs nanowires grown by selective-area growth mode.[38,39] Therefore, we intentionally add antimony into InAs to form $InAs_{0.95}Sb_{0.05}$, which has the same bandgap as that of thin-film InAs.

Table 2-2 shows a list of material parameters applied in the model including doping levels, electron and hole mobilities, Shockley-Read-Hall (SRH) recombination lifetimes, and more. Those parameters are obtained by fitting the dark I-V curve of the InAs *p-i-n* diode with a mesa size of 400 μm, and the values are reasonably comparable to the results from previous references. All other material parameters are taken from the material database of the numerical simulator. In this study, the non-radiative recombination on surfaces of both photodetectors is not included in the electrical simulations.

	Material parameters	**Values**
Nanowire photodetector	InP substrate doping level	3.0×10^{18}
Thin-film photodiode	n^+-InAs	1.0×10^{18}
	i-InAs	7.0×10^{14}
	p^+-InAs	1.0×10^{18}
Both devices	InAs(Sb) electron mobility	11000 $cm^2/(V\cdot s)$
	InAs(Sb) hole mobility	250 $cm^2/(V\cdot s)$
	InAs(Sb) SRH lifetime	3 μs

Table 2-2 Summary of material parameters used in the electrical simulations.

2.4.4 Calculation of responsivity and detectivity

The responsivity of the nanowire photodetector is given by

$$\sigma(\lambda) = \frac{I_{ph}(\lambda)}{P(\lambda)} = \frac{I_{ph}(\lambda)}{\int G(x,y,z,\lambda)dV/\alpha(\lambda)} \tag{2.4}$$

where I_{ph} is the output photocurrent ($I_{ph} = I_{total} - I_{dark}$), P is the input power, G is the optical generation rate for a specific incident light wavelength in units of cm^{-3} s^{-1}, and α is wavelength dependent optical absorption. To obtain the total input power at a certain wavelength, we integrate G over the InAsSb region and then divide the integral sum by α. In this case, we only need to calculate the input power once, because the power is kept fixed in the optical simulations by FDTD for the entire wavelength regime.

Then, we estimate the detectivity (D^*) through a well-known equation expressed as

$$D^* = \frac{\sqrt{AB}}{NEP} = \frac{\sigma\sqrt{AB}}{\sqrt{2qI_{dark}B + 4kTB/R}} \approx \frac{\sigma\sqrt{AB}}{\sqrt{2qI_{dark}B}} = \frac{\sigma}{\sqrt{2qJ_{dark}}} \tag{2.5}$$

where A is the detector area (the area of a unit cell in our case), B is the bandwidth, σ is the responsivity, I_{dark} is the dark current, and R is the load resistance. We assume the detector works in the quantum regime (not limited by Johnson or thermal noise), and therefore neglect the Johnson noise in Eq. 2.5. For typical SWIR and MWIR detectors, decreasing dark current means to reduce the volume of the absorption layer, which also results in a decreased responsivity (σ). An unfortunate outcome of this approach is that it may lead to an even lower detectivity, especially if the loss of responsivity is significant. However, in the case of nanowire-based InAsSb-InP photodiodes, the dark current is drastically reduced due to much lower saturation current and generation-recombination current. Meanwhile, the optical absorption is enhanced by surface

plasmon wave resonance, excited by metallic gratings, and so it is possible to reduce dark current without sacrificing the optical absorption.

2.4.5 Model validation

To demonstrate the validity of our photoresponse model for nanowire-based photodetectors, we simulate the responsivity of a thin-film InAs PIN photodiode in photovoltaic mode. As shown in Fig. 2-16, the InAs *p*-*i*-*n* photodiode is composed of a n^+-InAs layer (1×10^{18} cm^{-3}, 2 μm), a *i*-InAs layer (7×10^{14} cm^{-3}, 2 μm), and a p^+-InAs layer (1×10^{18} cm^{-3}, 2 μm). The reported responsivity at 2 μm is about 0.75 A/W for a 400 μm mesa, where the effect of surface recombination is minimized. Similarly, we compute the optical generation profile, or electric field profile, by FDTD, and then electrically solve the photocurrent. With an input power of 2×10^{-10} W, the calculated photocurrent is 1.69×10^{-10} A, which yields a responsivity of 0.85 A/W, very close to the experimentally measured value of 0.75 A/W.

2.4.6 Performance of nanowire photodetectors

We investigate the theoretical performance of nanowire InAsSb-InP photodiodes with three types of doping profiles, as shown in Fig. 2-17. While the doping profiles of Structures 1 and 2 are constant across the entire nanowire segments, Structure 3 has a non-uniform profile, resulting in a local electric field near the top of the nanowire. Structure 3 is expected to have the highest responsivity among the three devices since the surface plasmon mode is tightly confined at the nanowire tip, and the photocarriers (electrons) can be quickly swept to the 3-D contacts. The dark current of Structure 2 (with the highest *n*-type doping level) is also expected to be the lowest because it has the smallest depletion region, and consequently, the least amount of diffusion from the minority carriers.

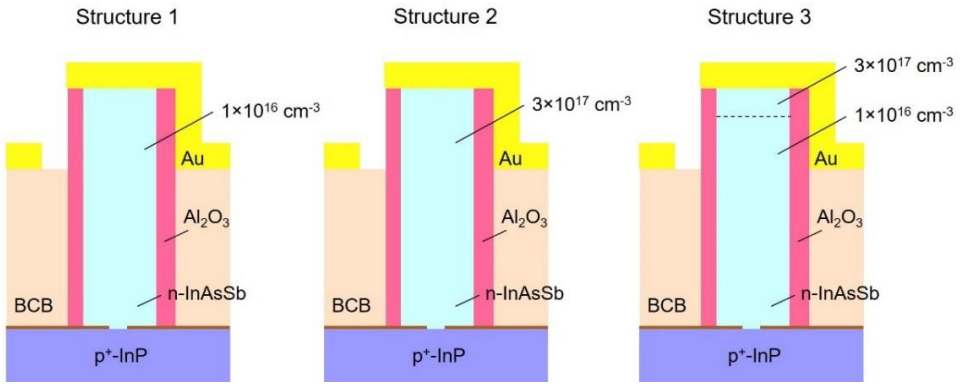

Figure 2-17 Schematics of the 3-D InAsSb nanowire photodiodes with three different doping profiles investigated by the simulations.

Note that the Al_2O_3 passivation layers fully cover the nanowire sidewalls, and only the top facets are exposed to form the contacts. These structures are advantageous over the previously reported nanowire photodetectors with InP passivation layers because: (1) the high bandgap oxide passivation layers can fully avoid depletion of top nanowire segments by the metal contacts under applied bias; (2) the Al_2O_3 deposition by atomic layer deposition (ALD) as an *ex-situ* passivation approach is more robust and controllable than the *in-situ* passivation technique; (3) the thickness of Al_2O_3 layer can be accurately controlled by deposition time, and thus is much easier to grow a thicker shell (~ 30 – 60 nm) without formation of dislocations at interfaces; and (4) the "effective" thickness of nanowire can be enhanced by forming a thick Al_2O_3 shell, resulting in greater modal confinement and higher optical absorption. More discussion of Al_2O_3 passivation will be provided in Chapter 4.

Fig. 2-18(a) illustrates the *x*-polarized and *y*-polarized electric profiles at 3 μm. Clearly, the optical mode inside the top nanowire segment is entirely isolated from the interface with ambient air, and thus the impact of surface recombination on photocurrent, or responsivity, is much lower. Fig. 2-18(b) displays a comparison of optical absorption between nanowire photodetectors and thin-film InAs photodiodes. Clearly, thin-film devices offer a much higher optical absorption

(~ 70%) across the entire spectrum (except the regime close to the bandgap cut-off) due to their thick absorbers (T ~ 14 μm). In contrast, the absorption of nanowires mostly relies on the excited surface plasmon wave on the exposed nanowire top segments (~ 1 μm). At the plasmonic peaks, the absorption of nanowire detectors can reach up to ~ 15%, roughly 4 – 5 times less than that of thin-film devices. By assuming the same internal quantum efficiency (IQE) for both types of photodiodes, we estimate that the responsivities of nanowire devices will be lower.

Fig. 2-19 shows the resultant simulations of the spectral response (i.e., responsivity *vs.* wavelength) and detectivities of the above three structures and thin-film InAs *p-i-n* photodiode in photovoltaic mode, or at 0.0001 V. As expected, the responsivities of nanowire devices are lower than those of thin-film devices. Structure 3 shows the highest responsivity among all designs, indicating that the local electric field near the top nanowire facets assists the drift of photocarriers to the 3-D contacts. Note that the multiple spectral response peaks in Fig. 2.19 (a) result from the multiple surface plasmonic peaks shown in the absorption spectra in Fig. 2.18 (b).

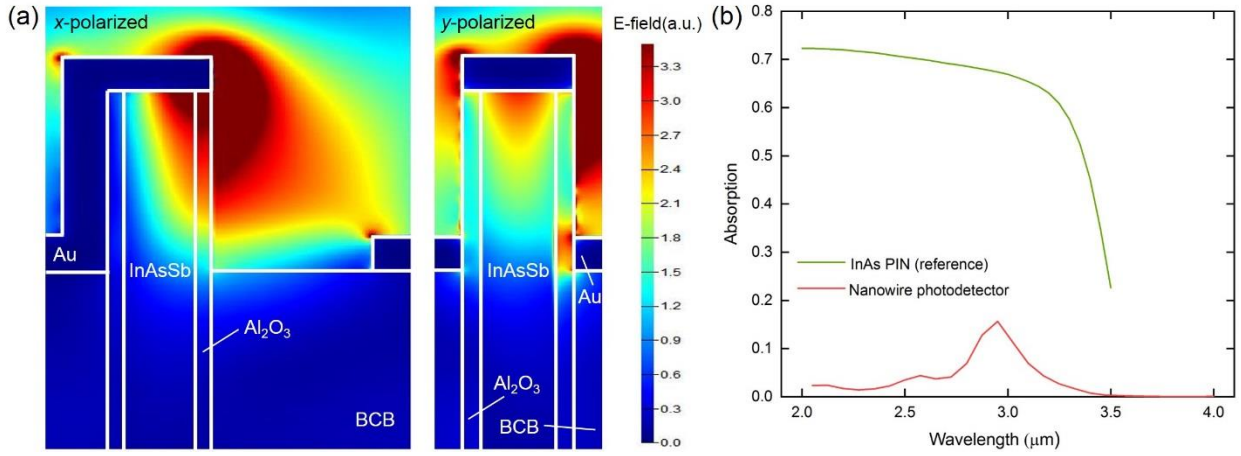

Figure 2-18 (a) Cross-sectional electric field profiles of *x*- and *y*- polarization for InAs nanowire photodiode. (b) Simulated optical absorption of InAs *p-i-n* photodiode and InAsSb nanowire photodiode.

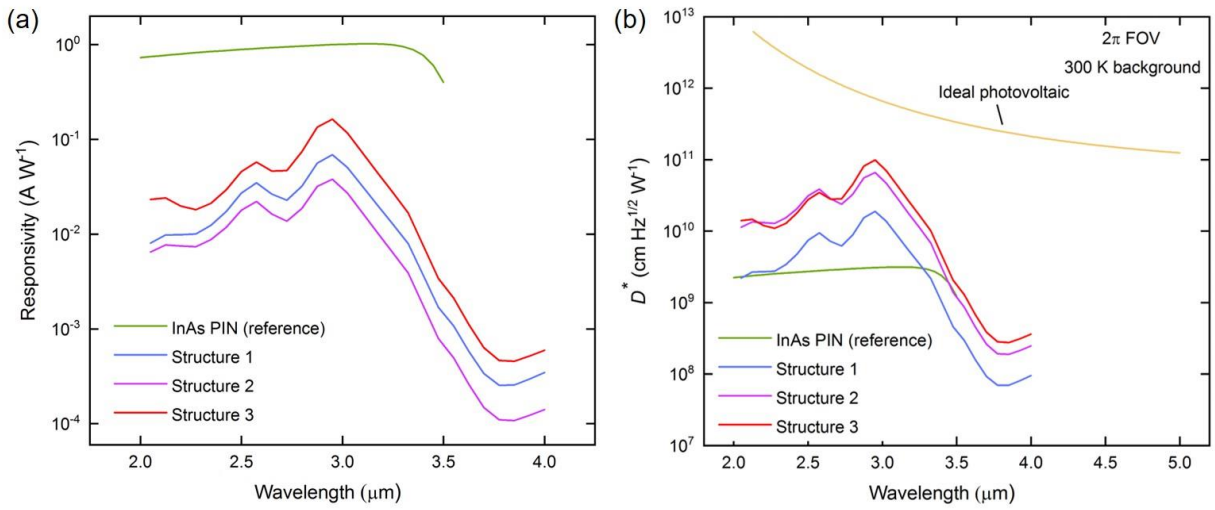

Figure 2-19 Simulated room-temperature device performance of nanowire-based InAsSb-InP photodiodes with Al_2O_3 passivation layers. Structures 1 – 3 correspond to the device schematics illustrated in Fig. 2-17.

Now we consider the simulated detectivities. Remarkably, the room-temperature detectivities of InAsSb nanowire photodiodes can achieve over 1×10^{10} cm $Hz^{1/2}W^{-1}$ up to 3.3 μm wavelength light for Structure 2 and Structure 3, higher than the values reported from any commercial or research MWIR photodetectors at 300 K to date (Fig. 2-19 (b)). Although the responsivity of Structure 2 is lower than that of Structure 3, the dark current of the former design is lower due to less saturation current. Moreover, the dark current of Structure 1 is about 5-6 times higher than that of Structure 3, resulting in a lower detectivity; however, it still shows better performance than the thin-film device for wavelengths up to 3.3 μm. Indeed, with further device structure optimization of InAsSb based nanowire photodetector, the detectivity can be enhanced further and cover the entire mid-wavelength spectrum.

2.4.7 Summary

We developed a 3-D computational model to numerically investigate the responsivities and detectivities of nanowire photodetectors at SWIR and MWIR and compare the performance with

planar thin-film InAs photodiodes. Such nanowire photodetectors were composed of *n*-type $InAs_{0.95}Sb_{0.05}$ nanowire photoabsorbers grown on *p*-type InP substrates and metallic gratings. For the nanowire InAsSb-InP photodiodes, the dark current was largely suppressed, due to a much smaller photoabsorber volume and reduced saturation current from minority carrier diffusion, while the optical absorption was plasmonically enhanced by metallic gratings. The resultant simulations show a room-temperature detectivity of over 1.0×10^{10} cm $Hz^{1/2}W^{-1}$ for wavelengths up to 3.3 μm, at least one-order higher than that of any commercial or research diodes in this wavelength regime. Our work shows that, through sophisticated optical and electrical designs, nanowire-based photodetectors can demonstrate better performance than their thin-film device counterparts for infrared photodetection.

2.5 Photoresponse model for ultrafast current pulse

2.5.1 Introduction

This model combines the transient model together with the photoresponse model to simulate the output current corresponding to an input ultrafast laser pulse (femtosecond laser). We take a nanowire photoabsorber array as an example, which is composed of self-assembled metal nanostructures as 3-D plasmonic gratings.[34,35] Most of the incident optical photons can be confined within nanoscale distances from the metallic gratings. As a result, the majority of the photocarriers inside the nanowires are routed to the gratings in sub-picosecond time to contribute to efficient and ultrafast current pulses. The nanoscale photoabsorbers promise ultrafast current generation, which can be potentially used to realize energy-efficient optical-to-terahertz converters and thus circumvent the need for short carrier lifetime semiconductor substrates.[40] Furthermore, such

optical-to-terahertz converters can be fully-integrated into a compact and low-cost device scheme for enabling practical terahertz imaging and sensing architectures used in large scales.

2.5.2 Plasmonic nanowire photoabsorber

Plasmonic nanowire photoabsorbers are one of the most crucial building blocks of the proposed transformative terahertz emitter concept. Fig. 2-20(a) shows an exemplary plasmonic nanowire photoabsorber unit comprised of an InAs nanowire grown on a Si substrate and optimized for photo-absorption at a 1550 nm pump wavelength. Benzocyclobutene (BCB) is used as a dielectric spacer to separate the top and bottom metal contact and control the exposed nanowire height.

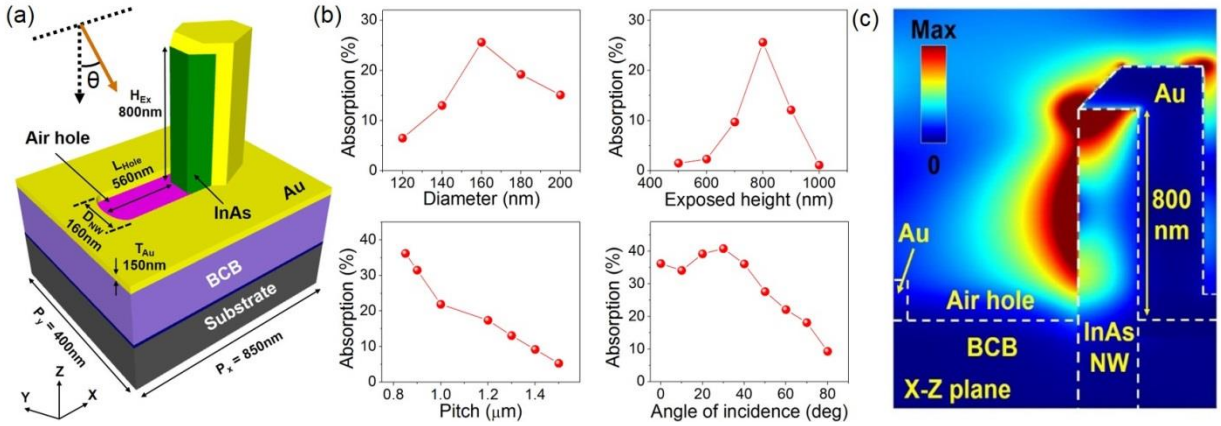

Figure 2-20 (a) Optimized dimensions for an InAs nanowire photoabsorber at 1550 nm optical wavelength. (b) Optical absorption as a function of absorber dimensions (nanowire diameter (D_{NW}), exposed nanowire height (H_{Ex}), and pitch of the array (P)) and angle of the optical pump beam (θ). (c) Electric-field profile of the excited surface plasmon wave at a 1550 nm pump wavelength for an x-polarized beam and an incident angle of 30°.

Multiple parameters were finely tuned to optimize the optical absorption including: (1) the nanowire diameter (D_{NW}), (2) the exposed nanowire height (H_{ex}), (3) the nanowire array pitch (P_x and P_y), (4) the length of the air hole (L_{Hole}), (5) the thickness of the gold layer (T_{Au}), (6) the

incident angle of the optical pump beam (θ), and (7) the polarization of the optical pump beam. Our initial analysis from FDTD simulations (Lumerical FDTD Solutions) estimate a remarkable photo-absorption of over 40% at a 1550 nm optical pump wavelength using the dimensions shown in Fig. 2-20(a) and at a pump incident angle of 30°. Fig. 2-20(b) shows how different geometrical parameters impact photo-absorption in the designed nanowire photoabsorber. The excited surface plasmon waves are tightly confined at the exposed nanowire tips, as shown in the electric-field profile in Fig. 2-20(c). It should be noted that the effect of the substrate on the optical mode is negligible.

2.5.3 Current response

To analyze the induced photocurrent, we incorporate the 3-D optical generation rate profile into the inside of a single nanowire photoabsorber in a TCAD simulation (Sentaurus) as shown in Fig. 2-21(a) by using the 3-D optical field profile calculated by FDTD. Next, we compute the transient response to an optical pump beam from a femtosecond laser with a pulse width of 50 fs FWHM and an average power of 16 μW (peak power of 4.5 W), and a beam diameter of 15 μm (illuminating ~ 500 nanowires). Fig. 2-21(b) shows a comparison of the induced photocurrent by *n*-type and *p*-type InAs nanowires with doping concentrations ranging from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}. The simulation results clearly indicate that the nanoscale transport path of the photo-generated carriers to the metal contact offers an ultrafast photocurrent response with less than a 100 fs FWHM. Moreover, the simulation results show that the induced photocurrent can be increased significantly by using higher doping levels, as a higher doping level results in a larger gradient of carriers and a more rapid acceleration of carriers toward the 3-D metal contacts. Note that the doping dependence on InAs mobility has already been considered. Again, since no bias is applied to the photoabsorbers (in photovoltaic mode), the dark current is zero, and the carrier

transport mainly relies on diffusion. As shown in Fig. 2-21(c), the hole density reaches its maximum value at a time of ~ 230 fs after the laser peak arrives, and then it starts to decrease mostly due to carrier diffusion near the contacts.

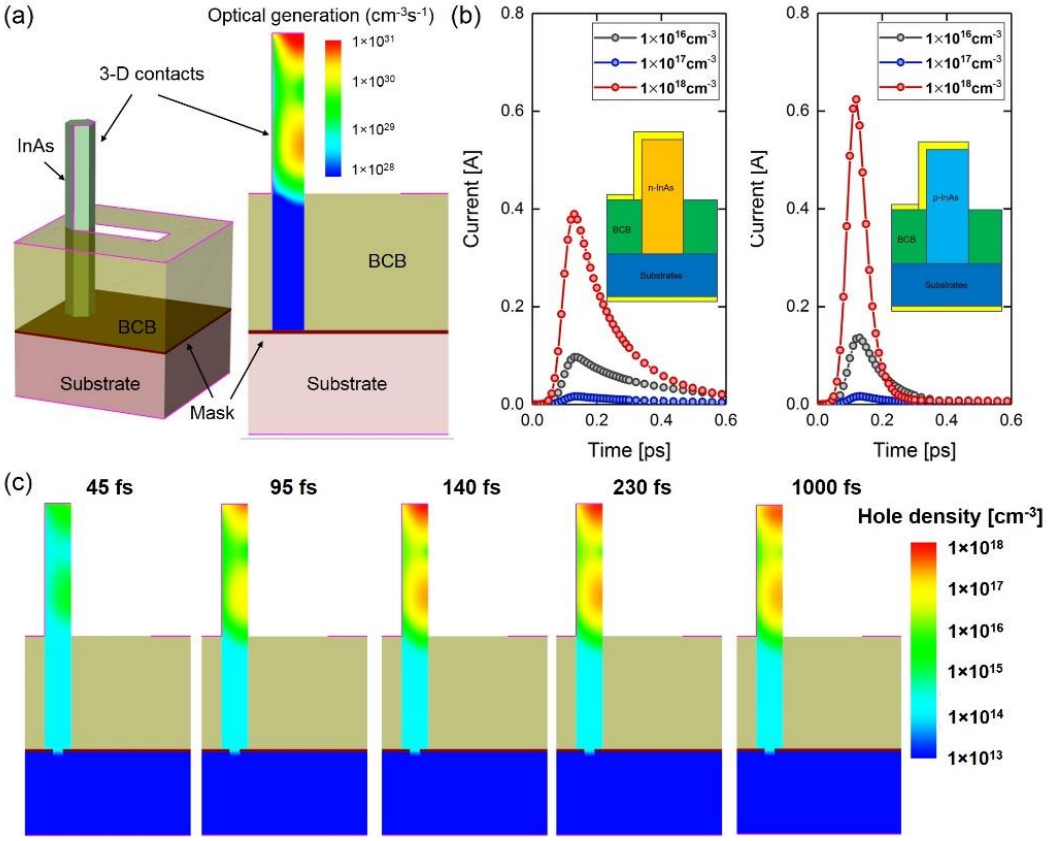

Figure 2-21 (a) The profile of the optical generation rate inside the designed nanowire photoabsorber in response to a pump beam from a femtosecond laser with a pulse width of 50 fs FWHM, a repetition rate of 50 MHz, an average power of 16 μW (peak power of 4.5 W), and a beam diameter of 15 μm (illuminating ~ 500 nanowires) at the peak optical intensity. (b) The induced photocurrent for *n*-type and *p*-type nanowires, at a fixed diameter of 160 nm, with doping levels ranging from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}. (c) The hole distribution as a function of time for an *n*-type nanowire at $1\times10^{18}cm^{-3}$ doping.

2.5.4 Summary

We developed a photoresponse model for ultrafast current pulse to investigate the current response of an innovative terahertz emitter based on plasmonic nanowire light absorbers that

enabled unprecedented conversion efficiencies from optical beam to terahertz radiation. By utilizing a compound semiconductor nanowire array integrated with plasmonic gratings, we confined most of the incident optical photons within nanoscale distances from the plasmonic grating. As a result, majority of the photo-generated carriers inside the nanowires were routed to the plasmonic grating within a picosecond to contribute to efficient terahertz generation. Such a platform based on nanoscale photoabsorbers is promising to enhance the optical-to-terahertz conversion efficiency and bandwidth of terahertz emitters at telecommunication optical wavelengths. It also allows for monolithic integration on Si or InP substrates, offering a compact and low-cost device scheme.

3. Nanowire epitaxy for optoelectronics at 2 – 5 μm

3.1 Overview

III-V semiconductor photonic devices operating at wavelengths longer than 2 μm have received increasing attention due to the variety of applications in the short-wavelength infrared (SWIR) and mid-wavelength infrared (MWIR). In this wavelength regime, InAs and its ternaries – arsenic-rich (As-rich) InAsP, As-rich InAsSb, and indium-rich (In-rich) InGaAs – are able to serve as building blocks for interband and intersubband optical devices. To fabricate those, a fundamental challenge is the epitaxy of lattice mismatched active regions on well-studied substrates, such as Si, InP and GaAs. Compared with thin film growth, a unique property of bottom-up nanowires is that elastic deformation can occur at a heterogeneous interface; this reduces planar defects such as threading dislocations and misfit dislocations, which allows growth of heterostructures with larger lattice mismatches. Although integration of III-V nanowires on Si is of particular interest for telecommunications, for many other applications requiring longer wavelength, including 2 – 3 μm lasers and detectors, the low cost of the substrate is offset by the poor device performance. In these cases, InP is the ideal substrate because: (1) lattice mismatches can be minimized (~ 3.2% for InAs, on InP, ~ 7.2% for InAs on GaAs, and ~ 11.6% for InAs on Si), and (2) critical thickness, i.e., maximum thickness of a lattice-mismatched layer without generating defects, of an As-rich InAs-based ternary layer on InP becomes infinite with a nanowire diameter up to 100 – 120 nm.[23] Therefore, development of growth capability for InAs(P)(Sb) nanowires on InP substrates is significant, and furthermore, it can offer opportunities for hybrid integration as well.

Heteroepitaxy of vertical InAs nanowires on InP as well as Si substrates has been previously reported.[41-48] As for ternaries, growth of As-rich InAsP nanowires has been mostly achieved on InAs substrates using gold-catalyzed (Au-catalyzed) vapor-liquid-solid (VLS) by chemical-beam epitaxy (CBE), and photoconductive current of single nanowire at about 2 μm has been observed.[49,50] Growth of self-catalyzed phosphorus-rich (P-rich) InAsP has been reported on both InP (111)B and Si.[51,52] Only one study shows the morphology of As-rich InAsP nanowires on InP (111)B; however, no further material characterization has been provided.[53] High-yield and high-uniformity selective-area growth of InAsSb nanowires with a high antimony composition of 0.149 have been successfully grown on InAs (111)B as well.[54] Intensive studies have been performed to develop near-infrared emitters with InP/In-rich InAsP heterostructures on InP (111)A or (111)B substrates, which are grown by Au-catalyst or indium catalyst-assisted VLS, and catalyst-free selective-area epitaxy (SAE) using both molecular-beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD).[55-62] Additionally, only one study has shown the growth of In-rich InGaAs nanowires on InP (111)B with indium composition as high as 0.9, estimated by photoluminescence (PL) measurement.[63] In short, for heteroepitaxy of InAs-based nanowires on InP substrates, material studies to date have been limited.

In this study, we develop the growth technique for InAs(P)(Sb) nanowires on InP (111)B substrates by catalyst-free selective-area metal-organic chemical vapor deposition (SA-MOCVD). The first part of this chapter presents the demonstration of arsenic-rich $InAs_{1-x}P_x$ ($0 \leq x \leq 0.33$) nanowire arrays grown on InP (111)B substrates. It is shown that by introducing a thin InAs seeding layer prior to the growth of the nanowire, extremely high vertical yield is achieved by eliminating rotational twins between (111)A and (111)B crystal orientations. InAsP nanowire arrays show strong emission by PL at room temperature, spanning a wavelength range of 1.9 – 2.6

μm. The second part of this chapter will show high vertical yield $InAs_{1-x}Sb_x$ ($0 < x \leq 0.18$) nanowire arrays grown on InP (111)B substrates by the same growth mode. High antimony composition is achieved by pulsing the arsenic flow to reduce the effective arsenic partial pressure while keeping the antimony partial pressure fixed. This increases the antimony vapor phase composition while allowing the antimony partial pressure to be kept low enough to avoid antimony condensation on the growth mask. InAsSb nanowire arrays show strong emission by photoluminescence at 77 K, covering a wavelength range of 3.7 – 5.1 μm. In the third part of this chapter, we report on the growth of high yield InAs and InAsSb inserts embedded in InAsP nanowires grown on InP (111)B substrates. It is observed that the growth of the inserts with high aspect ratios can be achieved by properly tuning the V/III ratio. Nanowire arrays with InAs(Sb) inserts exhibit strong photoluminescence at 77 K from interband transitions, spanning a wavelength range of 2.30–3.70 μm. In addition, we electrically extract the conduction band offsets (CBOs) of InAs-InAsP heterojunctions from characteristics on InAsP single-barrier devices.

3.2 Growth of InAsP nanowires

3.2.1 Introduction

For SA-MOCVD, growth of vertical InAs nanowires can be easily performed on InAs (111)B substrates; however, InP nanowires tend to grow along (111)A instead of (111)B on InP (111)B substrates, which is completely opposite to the growth by catalyst-assisted VLS mode where the growth direction is (111)B. Therefore, the key challenge for growth of InAsP is to overcome the bidirectional property of InP nanowires. To solve this problem, we propose a thin InAs seeding layer as a transition between substrates and $InAs_{1-x}P_x$ nanowires to control the growth direction. High uniformity and high yield of nanowire array have been achieved, and strong PL

emission of InAsP nanowires has been obtained at phosphorus compositions between 0.12 and 0.33. Here, we argue that such seeding-layer-assisted growth mode can also serve as a universal solution for the growth of all types of InAs-based ternary nanowires on InP (111)B.

3.2.2 Experimental section

The substrate is a Zn-doped 2-inch on-axis InP (111)B wafer. A 20 nm silicon dioxide (SiO_2) film is deposited on the substrate and patterned by electron-beam lithography (EBL). The designed diameter and pitch of nanoholes are 40 nm and 600 nm, respectively, and the dimension of individual arrays is 100 μm × 100 μm. The growth of nanowires is accomplished using a low-pressure (60 Torr) Emcore D-75 MOCVD reactor with hydrogen (H_2) as the carrier gas. The precursors are trimethylindium (TMIn), tertiarybutylarsine (TBAs), and tertiarybutylphosphine (TBP). A schematic of the growth sequence is illustrated in Fig. 3-1(a). In the first step of the growth sequence, the sample temperature is directly ramped to 590°C and holds for 8 minutes in order to fully remove the surface native oxide by thermal deoxidation in a H_2 atmosphere. Then, the temperature is ramped down to 575°C, and InAs seeding layer is grown for 30 seconds with a gas flow of TMIn at 4.54×10^{-2} sccm and TBAs at 1.45×10^{0} sccm (V/III ratio of 32). Next, the temperature is decreased to the designed growth temperature for nanowires. The growth of vertical InAsP nanowire is carried out at a V/III ratio of 32, and the growth temperature varies between 545°C and 575°C. In this step, the gas flow of TMIn is fixed at 4.54×10^{-2} sccm, while the gas flow of TBAs and TBP is changed to achieve increasing vapor phase of phosphorus from 0.70 to 0.95, labelled as x_v (x_v = [TBP]/([TBAs]+[TBP])). The growth is terminated by shutting off group-III, and the temperature is ramped down under TBP or TBAs overpressure, which us implemented to study surface properties of InAsP nanowires. Fig. 3-1(b) shows a scanning electron microscope (SEM) image of a 100 μm × 100 μm array, and a close-look of high-uniform vertical As-rich

InAsP nanowires. Similarly, the growth of InAs is carried out at 575°C with V/III ratio of 8. In order to demonstrate the compatibility of InAs seeding layer with other As-rich ternaries, growth of InAsSb nanowires is also performed at 530°C with V/III ratio of 4.2 and antimony vapor-phase of 0.6. Additionally, the temperatures discussed in this work refer to the readings on the pyrometer.

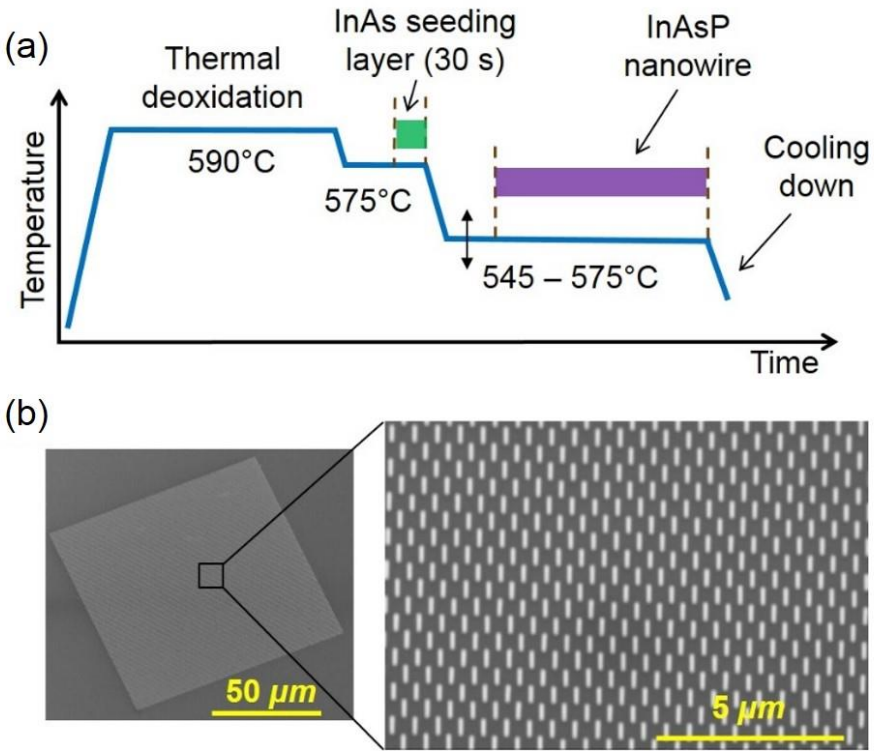

Figure 3-1 (a) The schematics of growth sequence for InAsP nanowires. The temperature and growth time are not to scale. (b) 30°-tilted SEM images of a 100 × 100 μm^2 as-grown InAsP nanowire array.

The height and diameter of InAsP nanowires are measured using SEM. A solid-state red laser at 671 nm is used as the pumping source for PL characterization, and the output optical signal is detected by a liquid-nitrogen cooled InSb detector in a Nicholet 6700 Fourier-transform infrared (FTIR) spectrometer. Finally, a FEI Titan transmission electron microscope (TEM) is used to obtain phosphorus composition from single InAsP nanowires by energy-dispersive x-ray spectroscopy (EDX).

3.2.3 As-rich InAsP nanowires

Due to the lattice-mismatch of 3.2% between InAs and InP, epitaxial growth of As-rich InAsP nanowires on InP substrates is not straightforward. Previously, growth on InAs (111)B substrates with Au-catalyst has been reported,[49,50] while growth by catalyst-free SAE has been successfully achieved at 590°C. The same dielectric mask in 20 nm thickness is used for both InAs and InP substrates. To keep the same surface temperature for InAsP on InP substrates, it is assumed that the pyrometer temperature should be reduced because of the higher thermal conductivity of InP over InAs. Therefore, we first attempt to directly grow on InP substrates with $x_V = 0.90$ at 545° – 575° C with interval of 10° C. No significant difference of geometry of as-grown structures is observed between those four samples. Figs. 3-2(a) and (b) show the growth at 555°C and 565°C where nanoholes are fully covered by irregular parasitic disks, tripods, and 'rocks' without any single hexagonal vertical nanowire. Such results are similar to the reported study of intrinsic InP grown on InP (111)B where nanoholes are mostly covered by tripods, except that the relative ratio of disks to tripods is much higher for InAsP growth than InP.[55] We assume that the irregular growth does not result from improper growth temperature or other growth conditions (such as III-V ratio) because (1) a 45°C temperature difference has been used to compensate thermal conductivity difference of substrates, and (2) tripods can be grown under current growth conditions. Thus, it is highly possible the nucleation in nanoholes are not formed properly. In the second trial, an extra InAs seeding layer is introduced prior to nanowire growth, and both disk- and tripod-shaped structures are fully eliminated, as shown in Figs. 3-2(c) and (d). Vertical growth is clearly observed with extreme high vertical yield close to 100% – only a few irregular polycrystalline rock-shaped islands are formed over 27,000 nanowires on a 100 × 100 μm^2 array.

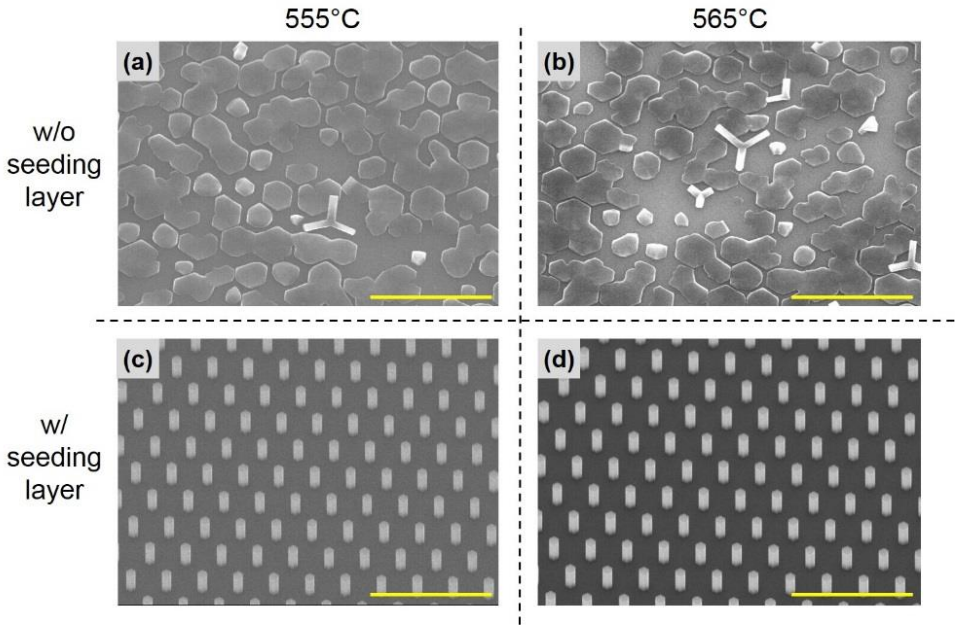

Figure 3-2 30°-tilted SEM images of InAsP NW growth (a) at 555°C without InAs seeding layer, (b) at 565°C without InAs seeding layer, (c) at 555°C with InAs seeding layer, and (d) at 565°C with InAs.

Here, we propose an explanation of the growth mechanism of the three major geometries observed by SEM – vertical wire, disk, and tripod – as shown in Fig. 3-3, where disk is considered as a mixed phase between vertical growth and tripod growth. Similar to the growth of InP nanowires on InP (111)B, a trapezoidal island tends to grow at the initial stage inside a nanohole due to competing growth between (111)A and (111)B directions.[55] It is well-known that the growth of InP nanowires by SAE is more favourable along (111)A.[55,64,65] When rotational twins are formed on (111)A along the edges of islands, the chemical bonds will be separated from the top (111)B surface, and therefore inclined wires are grown along three equivalent (111)A directions.[55] Note that tripods have been formed with a 180º rotation as shown in Fig. 3-3(b). This is because stacking faults are introduced along (111)B during island growth before twin boundaries along (111)A are formed, resulting in a crystal axis rotation of 60º and three additional (111)A directions. Interestingly, we observe much more irregular disk-like growth than tripod-like, which is opposite

to the growth of binary InP nanowires. The hypothesis is that the trapezoidal island and twin boundaries are still formed at the beginning of the growth; however, since the growth of As-rich InAsP might not be favourable along (111)A, other twin boundaries can be formed on sidewalls and adatoms diffused from the mask would attach to those boundaries. Thus, the bottom part of wires starts to grow towards the mask and merge with growth segments from neighbouring nanoholes, as shown in Fig. 3-3(b). Again, we suggest the disk-like growth does not result from the improper growth conditions, but from inappropriate initial nucleation inside nanohole. Note that a high x_v of 0.90 was used, and the actual vapor phase inside nanohole might be even higher to some extent. Thus, it would be very easy to form islands on the top surface of InP (111)B substrates, same as InP growth.

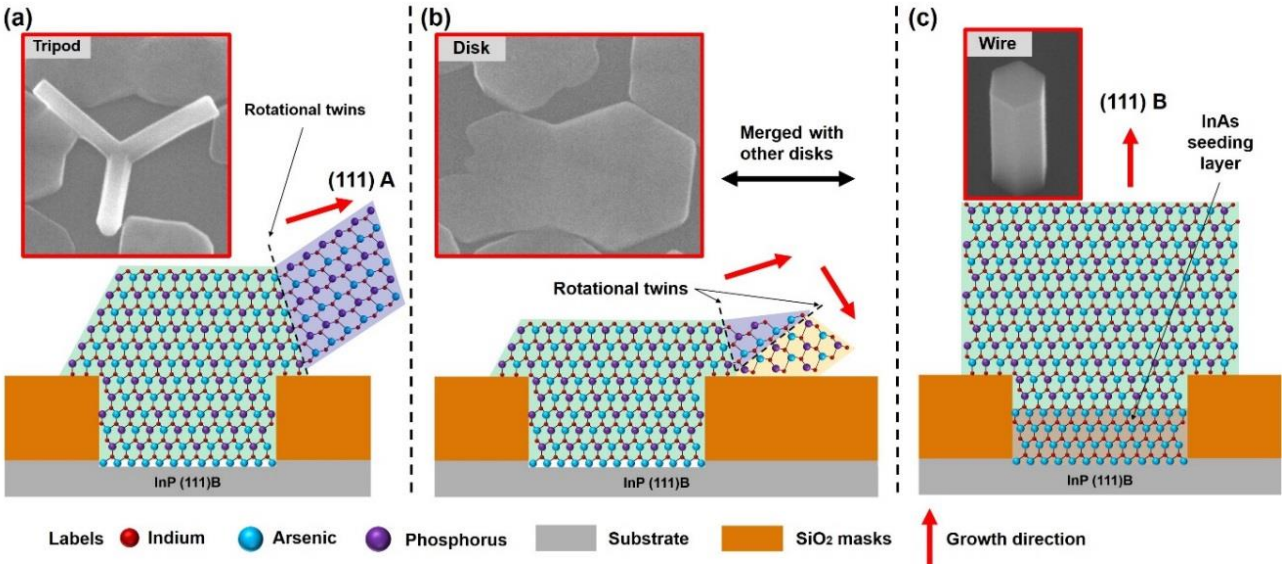

Figure 3-3 Two-dimensional schematics of three geometries formed from nanoholes: (a) tripod, (b) merged parasitic disk, and (c) vertical wire. The insets show a closer look of SEM images for each. Crystal orientations, twin boundaries, and grown structures during different growth periods are labeled and highlighted.

The solution, seemingly, is to reconstruct the substrate surface to avoid the growth of trapezoidal islands. We then introduce a thin InAs seeding layer as a buffer prior to nanowire growth to create As-terminated (111)B surface, as shown in Fig. 3-3(c). The current surface

properties are then similar to InAs (111)B substrates on which InAsP vertical nanowires are successfully grown. For growth of the seeding layer, a V/III ratio of 32 is used to reduce the growth rate for better uniformity (which is based on our previous experience for growth of InAs nanowires on InAs (111)B substrates). Since InAs vertical growth can be easily performed along (111)B at temperatures over 580°C, trapezoidal islands on InP (111)B are fully eliminated. Meanwhile, the tensile strain at InAs-InP heterointerface can be elastically released along the sidewalls of nanoholes and the threading/misfit dislocation can be minimized, which is extremely difficult for planar InAs epitaxy on InP substrates.

3.2.4 Growth temperature

We find the growth temperature has a significant impact on the aspect ratio of $InAs_{1-x}P_x$ nanowires with different phosphorus compositions. In this work, we define the aspect ratio as the ratio of nanowire height to the diameter. We perform several growths covering a temperature range from 545°C to 575°C for x_v of 0.90 and 0.95, as shown in Fig. 3-4(a), which correspond to a solid phase composition of x_s = 0.21 and 0.33, respectively (detailed characterization of phosphorus composition will be discussed later). The change of nanowire dimensions, i.e., diameter and height, are summarized in Fig. 3-4(b), and the change of aspect ratios are illustrated in Fig. 3-4(c). With x_v = 0.90, the aspect ratio first increases and then decreases with an increase of temperature. Meanwhile, with x_v = 0.95, the aspect ratio monotonically decreases for decreasing temperature. Therefore, we conclude that the growth is not primarily surface kinetically limited or mass-transport limited, but somewhere in between. For the case of x_v = 0.90, as the growth temperature is increased in a low temperature regime, the axial growth rate is increased because the top (111)B surface is more activated and the adatom diffusion length along nanowire sidewalls is longer. In contrast, with increasing growth temperature in a high temperature regime, the desorption of

indium and phosphorus atoms on (111) surface would become more significant,[66] while the surface bonds on (110) facets would be more activated where desorption of atoms is not dominant. Thus, the axial growth rate is suppressed, and the lateral growth rate keeps increasing. Additionally, as shown in Fig. 3-4(c), the temperature-dependent aspect ratio for x_v = 0.90 reveals an inverse u-shape characteristic; however, no maximized aspect ratio has been observed for x_v = 0.95 between 545°C and 575°C – it is possible that the actual axial growth rate for x_v = 0.95 would become lower at temperatures lower than 545°C, meaning that the peak of aspect ratio would occur in the temperature regime 545 – 555 °C. A similar temperature-dependent trend of axial growth rate has been reported for selective-area growth of InAs nanowires on InAs substrates (x_v = 0.00) (Fig. 3 in ref. 30; however, the change of axial growth rate as a function of temperature is not explained).[66] We believe that the same explanation for morphology change of InAsP nanowires can be applied to the growth of InAs nanowires in ref. 30. Therefore, it is expected to observe the similar inverse u-shape aspect ratios with peaks at the temperature higher than 560°C for x_v = 0.70 and x_v = 0.80.

Note that at the lowest temperature 545°C for x_v = 0.95, the tips of some nanowires are irregularly polygonal instead of hexagonal. This could possibly be due to the lower temperature at which growth along the lateral direction is kinetically limited, i.e., not thermally activated, contributing to non-uniform growth rate along six (110) directions. Thus, the temperatures over a range of 545°C to 555°C are considered as the optimized regime for x_v =0.90 and 0.95. Note that the growth temperature of InP on InP (111)B, *i.e.* x_s = 1.00, was reported at 660°C,[55] the same as InP on InP (111)A.[65] It is interesting that the growth temperature of $InAs_{1-x}P_x$ is then not positively correlated with phosphorus composition. Although the temperature data of $InAs_{1-x}P_x$ ($0.4 \leq x < 1.0$) nanowires by catalyst-free SAE have not been reported in literatures, it is highly possible that there would be a bowing relation between the optimized temperature and phosphorus composition.

Seemingly, in order to access phosphorus composition over 0.40, the growth temperature might need to be increased while much lower molar flow of TBAs is required.

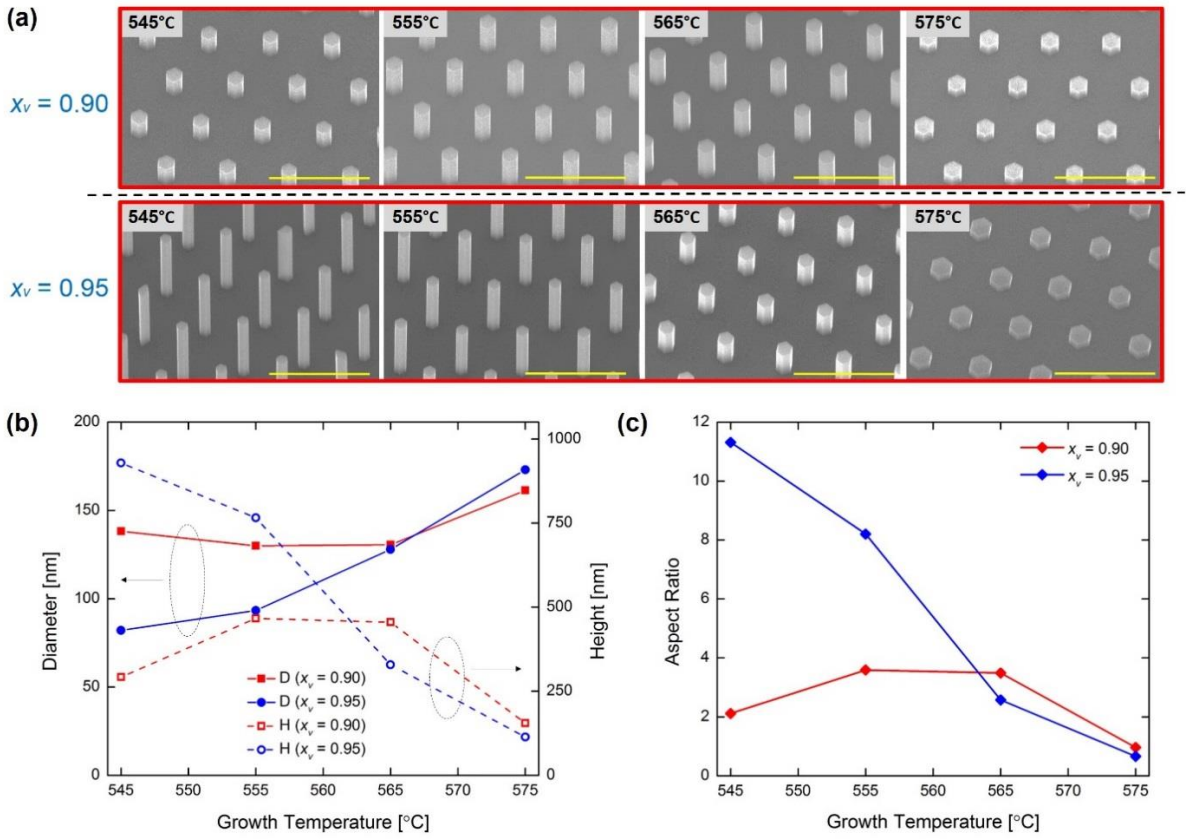

Figure 3-4 (a) 30° tilted SEM images of InAsP on InP (111)B for x_v = 0.90 and x_v = 0.95. The growth temperatures: 545 °C, 555 °C, 565 °C, and 575 °C. The scale bar for all images is 1 µm. (b) InAsP nanowire diameter and height for x_v = 0.90 and x_v = 0.95. (c) Aspect ratio (height divided by diameter) of InAsP nanowires for x_v = 0.90 and x_v = 0.95.

3.2.5 Material characterization

PL characterization of As-rich InAsP nanowires, serving as a significant study for material properties, has still not been reported in the literature. Thus, we perform PL measurements on four samples grown by different phosphorus vapor phase x_v – 0.70, 0.80, 0.90, and 0.95. In this study, the growth time is fixed at 10 minutes and the growth temperature is kept at 555°C to maintain a constant growth condition. To determine the corresponding phosphorus solid phase x_s of those

samples, the nanowires are mechanically removed onto copper grids, and the compositions are extracted by EDX point-scan. The measured x_s is given as follows: $x_s = 0.12$ ($x_v = 0.70$), $x_s = 0.15$ ($x_v = 0.80$), $x_s = 0.21$ ($x_v = 0.90$), and $x_s = 0.33$ ($x_v = 0.95$). In addition, the EDX line-scan is performed as well to demonstrate the uniformity of phosphorus across entire nanowires. The normalized PL spectra measured at room-temperature (300 K) are illustrated in solid lines, as shown in Fig. 3-5(a), and the reference signal from a n-type InAs substrate is depicted as well in dash line. The emission intensity from InAsP arrays is much stronger than InAs arrays (emission from InAs arrays is too weak to resolve), which we believe is due to a reduction of surface state density by introducing phosphorus. It can be further confirmed by two previous studies where As-rich InAsP is used as passivation layer to enhance optical emission from InAs nanowires,[67] and unpassivated P-rich InAsP nanowires show strong PL signals at room temperature as well.[52] As opposed to the spectra for InAsP grown on InAs substrates, there is no interference signal from InP substrates (~ 1.34 eV at 300 K).

To further study optical property and bandgap E_g of InAsP nanowires, temperature-dependent PL over a range of 77 K to 300 K is performed for the InAsP array with $x_s = 0.21$ ($x_v = 0.90$). As shown in Fig. 3-5(b), the peak emission energy as a function of temperature, corrected by $k_BT/2$, is fitted using material parameters from planar $Ga_xIn_{1-x}As_yP_{1-y}$ with single-phase zinc-blende (ZB) crystal structure,[68] giving an approximate phosphorus solid phase of 0.223. The bowing parameter used to fit the bandgap $E_g(InAs_{1-x}P_x)$ is 0.078 eV. The FWHM as a function of temperature is shown in Fig. 3-5(b) as well, and it increases almost linearly with temperature, which is a characteristic of linewidth broadening due to non-radiative phonon scattering, similar to thin film epitaxy of binary or ternary materials.

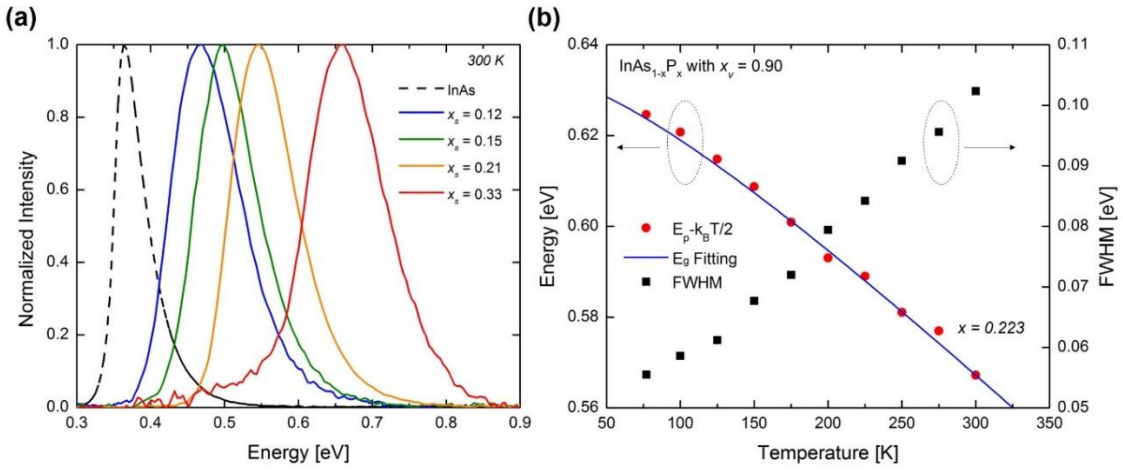

Figure 3-5 (a) Room-temperature PL spectra of four InAsP nanowire arrays with different phosphorus solid phase – 0.12, 0.15,0.21, and 0.33. A reference emission spectrum from a n-type InAs substrate is given as well. (b) Temperature-dependent emission peaks (left) FWHM (right) of InAsP arrays with phosphorus vapor phase of 0.90. The fitted temperature-dependent energy gap is plotted in solid line, giving an estimated solid phase of 0.223.

It is noted that the phosphorus composition of this sample obtained by PL is slightly higher than the one by EDX. Thus, it is possible that the nanowires might be in multi-phase, i.e., a mixture of ZB and wurtzite (WZ). To get further insight of crystal structure, we compare our result with a previous study in which E_g of WZ As-rich InAsP segments in InAs nanowires is determined by photocurrent measurement at 5 K.[69] Based on the fitting shown in Fig. 3-5(b), we first estimate E_g of InAsP nanowires with x_s = 0.21 at 5 K as 0.633 eV. From the fit in *ref.* 69, E_g of ZB $InAs_{0.79}P_{0.21}$ is ~ 0.60 eV, E_g of WZ $InAs_{0.79}P_{0.21}$ is ~ 0.72 eV.[69] Since the approximated E_g 0.633 eV is located in between and closer to the theoretical E_g of ZB structure, we suggest that as-grown InAsP nanowires are mostly composed of ZB segments.

Thermodynamics is another significant aspect of III-V ternary growth. The relationship between vapor phase and solid phase of phosphorus is typically not a one-to-one ratio, and it depends on chemical reactions and their activities, decomposition efficiency of precursors at

certain temperature, partial pressure of inlet gases, V/III ratio and so on.[70,71] Note that the growth temperature and V/III ratio are fixed in this study. It is predicted from thermodynamics model of InAsP that the phosphorus solid phase has an abrupt increase when x_v is over 0.80, as shown in Fig. 3-6.[71]

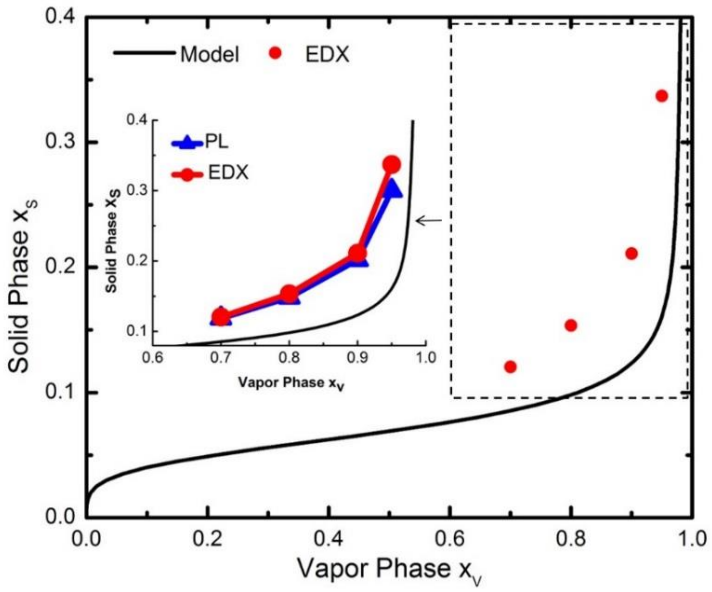

Figure 3-6 Thermodynamics of InAsP nanowire growth. The relation of vapor phase and solid phase for thin film InAsP is given in the solid line. A comparison of phosphorus solid phase determined by EDX and estimated by PL is shown in the inset.

Here, we perform the first study of thermodynamics mapping of InAsP nanowires grown by selective-area. The solid phase determined by EDX and estimated by PL are both projected onto the plot of thermodynamics. As shown in the inset of Fig. 3-6, phosphorus compositions are very close in both cases, with only about 10% difference at x_v of 0.95. This is because that the crystal phase of as-grown InAsP nanowires with all those phosphorus compositions is mostly ZB. As expected, the solid phase in nanowires will not precisely follow the model. It can be explained that the thermodynamics model is based on two-dimensional thin film growth, while nanowire growth

involves gas flow from all three dimensions e.g. adatoms diffused from the top of nanowires as well as the bottom through dielectric mask.

3.2.6 Overpressure

Generally, phosphorus overpressure is required during chamber cooling in order to prevent the desorption of phosphorus from the nanowires. Thanks to a much lower growth temperature of As-rich InAsP nanowire compared with growth of InP, the desorption of phosphorus during chamber cooling is not so significant, and therefore either group-V precursor, TBP or TBAs, is able to hold as-grown structures. Interestingly, we find the PL spectra from two unpassivated InAsP nanowire arrays that were grown under exact same conditions but with different overpressure materials are remarkably different. The optical signal from a sample with TBAs overpressure is too weak to resolve compared with TBP overpressure, as shown in Fig. 3-7(a). Since overpressure is the only variable in those two growths and the nanowire geometries are almost identical, the degradation of emission with TBAs overpressure must result from the change of InAsP nanowire surface condition. It has been reported that over 350°C arsenic exchanges with phosphorus on InP (001) surface, forming an InAs film in three monolayers.[72] In addition, it is well-known that the surface state density of InAs nanowire is high and can reach a level of 10^{14} ($cm^{-2}eV^{-1}$)[39,73]. Thus, it seems likely the same mechanism occurs in InAsP nanowire growth, as illustrated in Fig. 3-7(b). During PL measurements, most of the excited carriers diffuse to the InAs-like surface and decay by non-radiative recombination. In order to prove this, we put the sample with TBAs overpressure back into the reactor and regrew a thin InP passivation layer, as shown in Fig. 3-7(c). As expected, enhanced optical emission is observed, meaning that the surface state density was reduced by passivation. The red-shift of energy peak can be explained by phosphorus

desorption on the surface forming a more InAsP-like well region, and thus with a large band-gap passivation layer, the excited carriers were trapped and then recombined.

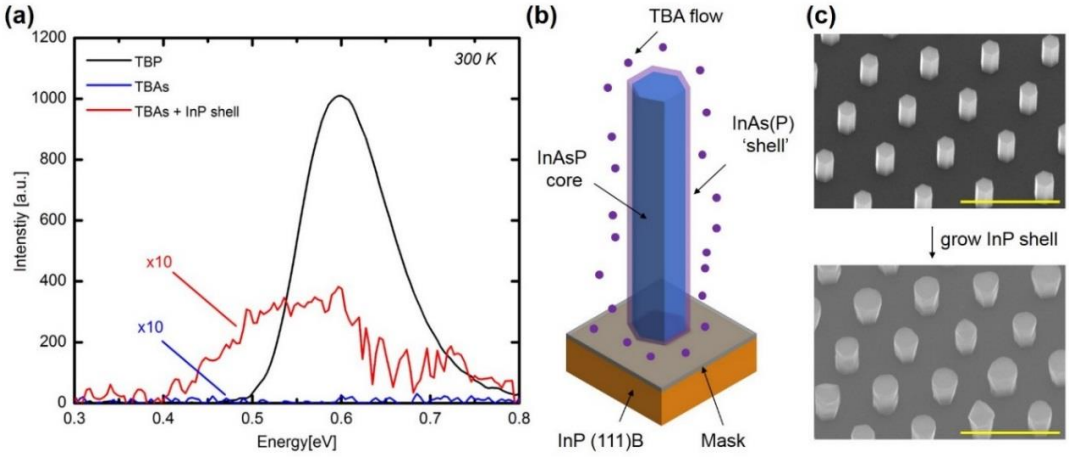

Figure 3-7 (a) Room-temperature PL measurement of InAsP samples with TBP or TBAs overpressure and regrown sample. The vapor phase of phosphorus is 0.90. (b) The schematic illustration to show the formation of a thin InAs(P) shell under TBA overpressure. (c) SEM images before and after regrowth of passivation layer. The scale bar is 1 μm.

3.2.7 Summary

We grew As-rich InAsP nanowires on InP (111)B substrates with lattice-mismatch between 2.6% – 3.2%. An InAs seeding layer was introduced to form a transition between substrate and nanowires, resulting in full elimination of trapezoidal islands at the initial stage of growth. PL characterization was carried out and thermodynamics of phosphorus incorporation was studied by EDX. Growth temperature was investigated as well, showing a bowing relation between target phosphorus composition and optimized temperature. Furthermore, we found TBP overpressure was preferred during chamber cooling to avoid exchange between arsenic and phosphorus. We believe that this study provides a promising approach to integrate As-rich InAs-based ternary nanowires on InP (111)B substrates.

3.3 Growth of InAsSb nanowires

3.3.1 Introduction

In this section, we report the first demonstration of $InAs_{1-x}Sb_x$ ($0 < x \leq 0.18$) nanowires grown on InP (111)B. To achieve InAsSb nanowire growth with high antimony composition, a high antimony flow is required. A key growth challenge is to minimize the antimony condensation on substrates or growth masks. To solve this problem, we propose a pulsed-arsenic growth technique to decrease the effective flow of arsenic, and thus to keep the partial pressure of antimony at a low level.[54] High uniform and high yield of nanowire array have been achieved, and the peak energy PL emission has been obtained at a range from 3.77 μm to 5.08 μm. We believe even higher antimony composition can be achieved by properly tuning the growth parameters with the proposed growth technique.

3.3.2 Experimental section

InAsSb nanowires are grown on Zn-doped InP (111)B substrates using SA-MOCVD. A 20 nm SiO_2 film is deposited on the substrate as a growth mask, and then patterned by EBL. The pitch and diameter of nanoholes are 400 nm and 40 nm, respectively, and the dimension of individual nanowire arrays is 100 μm × 100 μm. The precursors are trimethylindium (TMIn), tertiarybutylarsine (TBAs), and trisdimethylaminoantimony (TDMASb). A similar growth sequence has been previously discussed. Prior to the nanowire growth, the sample is annealed at 590°C for 8 minutes in order to fully remove the surface native oxide. Then, the temperature is ramped down to 555°C, and a thin layer of InAs is grown for 30 seconds with a gas flow of TMIn at 8.51×10^{-7} mole/min and TBAs at 2.74×10^{-5} mole/min (V/III ratio of 32). Next, the temperature is ramped down to 500 – 530°C to perform nanowire growth. In this step, the growth of InAsSb is carried out using the pulsed-TBAs growth technique, as illustrated in Fig. 3-8. The flow of TMIn

and TDMASb is constantly on, while the flow of TBAs is kept at 1.98×10^{-6} mole/min (the system limit) and modulated in an "on-off" fashion. As shown in Fig. 3-8, the duty cycle of TBAs flow is defined as t_1/T, where t_1 is the "on" time of TBAs flow in a single period and T is the period. A duty cycle of 0.14 (or 0.10) is implemented, corresponding to an antimony vapor phase $[x_v]_{Sb}$ of 0.84 (or 0.89), which is defined as $[x_v]_{Sb}$ = [TDMASb]/([TBAs]+[TDMASb]). The growth parameters are summarized in Table 3-1. Note that the vertical growth of InAsSb nanowire is carried out at a V/III ratio of 2.07, close to the value used in the growth on InAs (111)B substrates.[54] Finally, the growth is terminated by shutting off group-III, and the temperature was ramped down under TBAs overpressure.

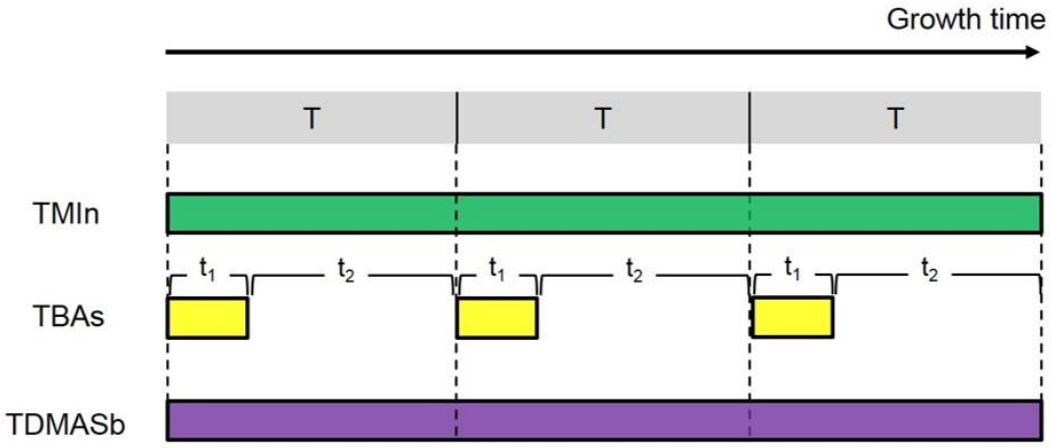

Figure 3-8 The schematics showing the pulsed-TBAs growth technique. T stands for the time of a single period; t_1 and t_2 are the "on" and "off" time of TBAs flow in one period, respectively.

Growth parameter	Scheme 1	Scheme 2
On time (s)	1	1
Off time (s)	6	9
Duty cycle	0.14	0.10
$[x_v]_{Sb}$	0.84	0.89

Table 3-1 Two schemes of pulsed-arsenic growth technique.

3.3.3 InAsSb nanowires with pulsed-arsenic

The selective-area growth of $InAs_{1-x}Sb_x$ ($0 < x \leq 0.149$) has been successfully performed on InAs (111)B with a $[x_v]_{Sb}$ of 0.60 and a V/III ratio of 2.05.[54] The longest peak emission wavelength, however, is 4.1 μm. Thus, higher antimony composition is required to cover the full MWIR (3 – 5 μm) spectrum. Normally, the antimony composition can be increased by increasing vapor phase $[x_v]_{Sb}$, decreasing temperature, or decreasing V/III ratio. Since V/III ratio > 2 is necessary to achieve uniform nanowire morphology, and excess antimony flow would contribute to antimony condensation on SiO_2 growth mask near patterned nanoholes, the only approach is to increase $[x_v]_{Sb}$ while V/III should be kept at the lowest level 2.07, which is currently used for selective-area InAsSb nanowire growth in all our study. However, we are unable to reach $[x_v]_{Sb}$ > 0.60 while simultaneously maintaining the same indium flow due to the system limit of the TBAs flow rate at 1.98×10^{-6} mole/min imposed by the MOCVD mass flow controller (MFC).

One possibility to overcome this limit is to use a smaller pitch for the pattern nanohole array, which would allow the incorporation of excess antimony during growth. Another approach is to reduce the effective arsenic flow by modulating arsenic flow in an "on-off" fashion, i.e., pulsed-arsenic growth technique. The former method is limited by proximity effect during EBL if the pitch is too small, causing over-exposure of electron-beam resist (ZEP520A, ZEONREX® Electronic Chemicals). Therefore, we take the second approach by growing InAsSb nanowires with two schemes of the pulsed-arsenic growth technique, as shown in Table 3-1. In the first scheme, the arsenic flow is switched on for 1 second and off for 6 second, giving a duty cycle of 0.14, while in the latter case, the arsenic flow is set with a longer "off" time of 9 second in a 10-second period, giving a duty cycle of 0.10. In both schemes, the TBAs flow is maintained at minimum, i.e., 1.98×10^{-6} mole/min with a constant V/III ratio of 2.07. Therefore, the effective

TBAs flows in both schemes are largely reduced, and determined by the duty cycles, i.e., $[TBAs]_{eff}$ = [TBAs] × t_1/T. As a result, we successfully increase the effective $[x_v]_{Sb}$ up to 0.84 and 0.89, respectively, by using those growth schemes.

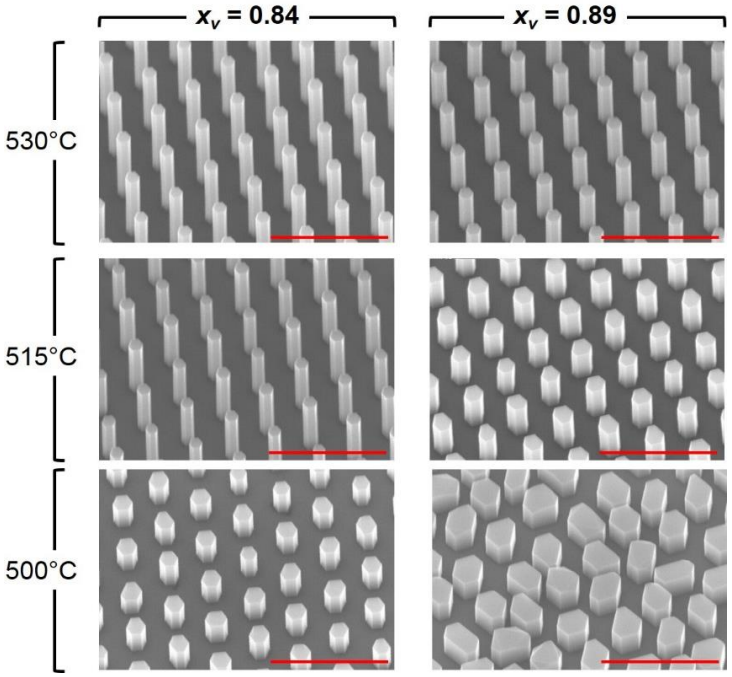

Figure 3-9 SEM images showing the morphology of InAsSb nanowires grown on InP (111)B substrates (six samples in total). Two different antimony vapor phase $[x_v]_{Sb}$ – 0.84 and 0.89. Three different growth temperatures – 530°C, 515°C, and 500°C. The scale bar: 1 μm.

The morphology of as-grown InAsSb nanowire arrays with two schemes is shown in Fig. 3-9. Three different growth temperatures are used – 530°C, 515°C, and 500°C. No condensation from excess antimony has been observed inside arrays. Equipped with the new growth technique, it is promising to achieve even higher antimony composition by freely tuning the duty cycle and the flow of TDMASb. It is expected that with the increase of $[x_v]_{Sb}$ and decrease of growth temperature, the antimony composition will be increased. Note that the aspect ratio (the ratio between nanowire height and diameter) becomes smaller with increasing antimony composition, which is due to the suppression of antimony adatom diffusion at high antimony flow.[74]

3.3.4 Optical characterization

PL characterization of InAsSb nanowires is performed at 77 K on the six samples, as shown in Fig. 3-10. The measured spectra are normalized and plotted in solid dots, and the fitted Gaussian spectra are depicted in solid lines. Fig. 3-11 summarizes the peak emission energies as a function of growth temperatures for $[x_v]_{Sb}$ = 0.84 and 0.89. Remarkably, we observe that the emission of InAsSb has been increased up to 5.08 μm, corresponding to an antimony composition of 0.18,[54,75] which is the highest achieved by selective-area InAsSb nanowire growth so far. Note that the optical signal tends to become weaker with increasing peak wavelength (i.e., increasing antimony composition). It might be due to the increase of surface state density. Further study is required to understand the relation between antimony composition and surface recombination mechanism.

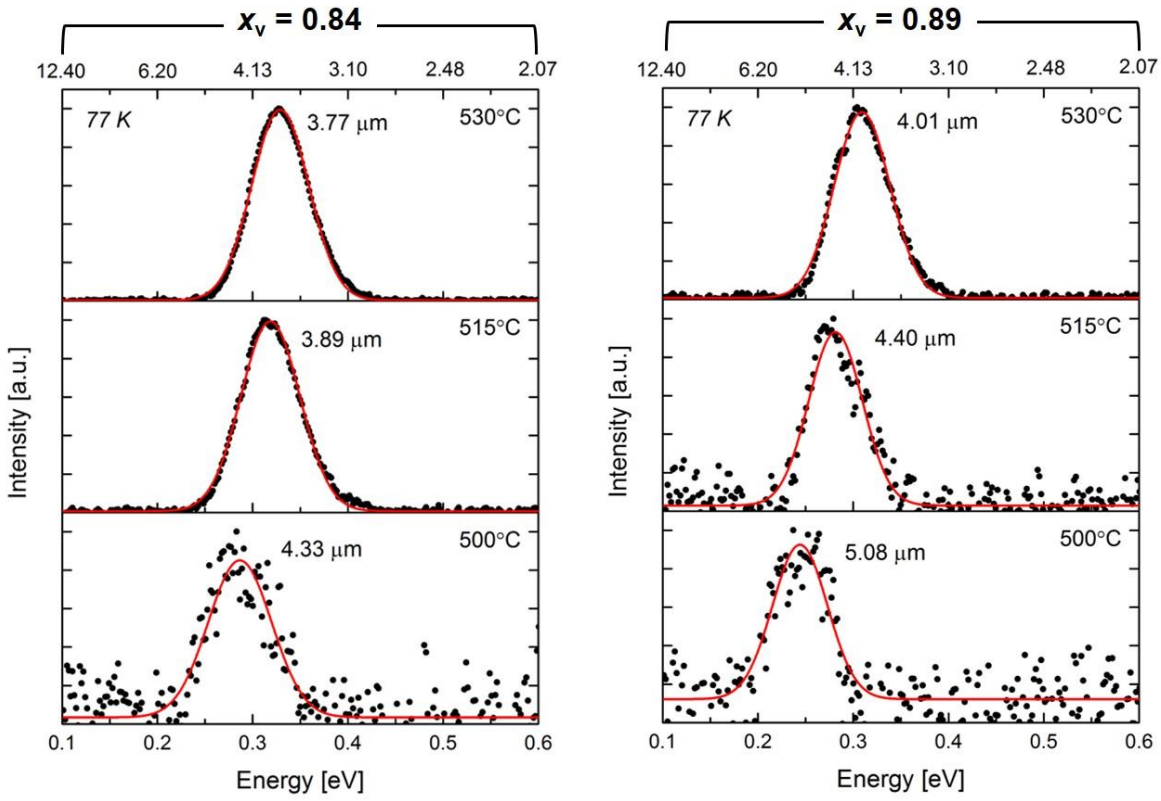

Figure 3-10 PL spectra at 77K of six InAsSb nanowire samples (shown in Fig. 3-9). The measured spectra are shown in black solid dots, and the fitted Gaussian spectra are depicted in red solid lines.

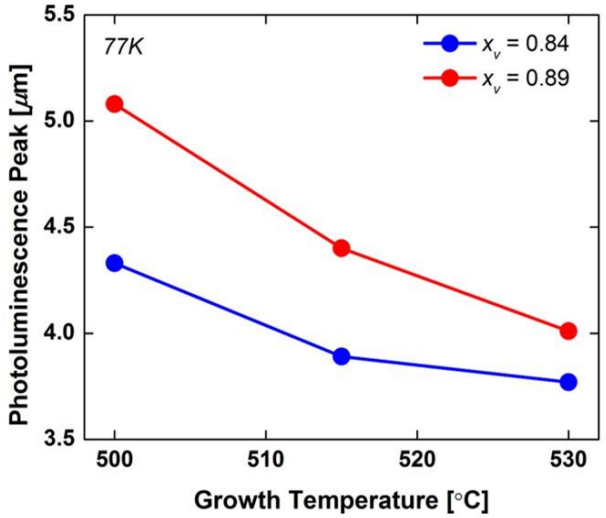

Figure 3-11 Emission peaks of PL spectra as a function of growth temperature.

3.3.5 Summary

We grew $InAs_{1-x}Sb_x$ ($0 < x \leq 0.18$) nanowires on InP (111)B substrates with PL emission up 5.08 μm at 77 K. A new growth technique with pulsed-arsenic was implemented to successfully reduce effective arsenic flow and increase antimony vapor phase. No antimony condensation was observed inside nanowire arrays. We believe that this study provides a promising approach to integrate InAsSb nanowires into InP substrates for MWIR photodetectors.

3.4 Growth of InAs(Sb) inserts and InAsP barriers

3.4.1 Introduction

To date, there has been significant effort to develop thin-film optical materials on InP substrates, allowing direct epitaxy of high-performance optical devices on well-studied substrates at a reduced cost compared to InAs substrates. Those optical devices include, but are not limited to, extended InGaAs interband photodetectors,[76] InGaAs-InAlAs (type-I) quantum-well infrared photodetectors,[77] and InGaAs-GaAsSb(Bi) (type-II) multi-quantum well lasers and

photodetectors.[78-81] Another material system based on arsenic-rich InAs(Sb)-InAsP type-I heterojunctions with compressively strained InAs(Sb) layers serves as a potential candidate as well for interband optical devices with minimized Auger recombination.[82,83] However, thin film epitaxy of InAs(Sb)-InAsP heterostructures, especially with high antimony or phosphorus composition, is challenging due to lattice mismatches, which might result in planar defects. Alternatively, heteroepitaxy with large lattice mismatch can be achieved by the bottom-up growth of vertical freestanding nanowires due to elastic deformation occurring at heterogeneous interfaces.[84,85]

Growth of thin film InAs(Sb)-InAsP multi-quantum well and superlattices has been previously reported for the applications of lasers and light-emitting diodes up to 6 μm, available in the literature.[82,83,86-88] On the other hand, growth of InAs-In(As)P heterostructures in nanowires has been achieved by chemical beam epitaxy to realize quasi one-dimensional potential barriers as well as quantum devices such as resonant tunneling diodes and single-electron transistors.[89,90] Unfortunately, all those heterostructures mentioned above are grown on InAs substrates, and no study in nanowires regarding optical properties of InAs(Sb) in this material system has been shown.

In this study, we provide a detailed study of high yield axial InAs(Sb) inserts in InAsP nanowires grown on InP substrates by SA-MOCVD. Interestingly, we find that the aspect ratio of insert segments can be freely controlled by the V/III ratio during growth. Strong optical emission over 2.3 μm has been obtained from nanowire arrays with InAs(Sb) inserts at cryogenic temperature. We further examine InAs-InAsP heterointerfaces by SEM and EDX. Additionally, we electrically extract the conduction band offsets (CBOs) of InAs-InAsP heterostructures. These results establish an experimental foundation for engineering interband transitions and enabling hybrid integration for nanoscale optical devices.

3.4.2 Experimental section

InAs and InAsSb inserts in InAsP nanowire are grown on Zn-doped InP (111)B substrate using SA-MOCVD. Note that for SA-MOCVD, growth of vertical arsenic-rich InAs(P)(Sb) nanowires is more favorable along (111)B instead of (111)A. A schematic diagram of the nanowire structure with an insert is illustrated in Fig. 3-12(a). To achieve high vertical yield on InP (111)B, a thin layer of InAs was introduced prior to nanowire growth. Here, the major steps of the process are given. A 20 nm SiO_2 film is first deposited on the substrate as a growth mask, and then patterned with nanoholes by EBL. The substrate is subsequently exposed by reactive ion etching of the SiO_2 mask. The diameter and pitch of the nanoholes are 40 nm and 600 nm, respectively. The group III precursor is trimethylindium [TMIn], and the group V precursors were tertiarybutylphosphine [TBP], tertiarybutylarsine [TBAs], and trisdimethylaminoantimony [TDMASb]. Before nanowire growth is initialized, all samples are annealed at a temperature of 590°C for 10 minutes to fully remove the surface native oxide. The temperature is then decreased to the growth temperature at 550°C. Growth of InAs inserts is carried out at a V/III ratio between 16 and 48, while for the growth of InAsSb inserts, the V/III ratio is kept fixed at 4. A 2-sec growth interruption with H_2 purge is used as the switching sequence for all heterointerfaces. An antimony vapor phase, i.e., [TDMASb]/([TDMASb]+ [TBAs]), of 0.6 is used for InAsSb inserts. Finally, the growth is terminated by shutting off TMIn, and the chamber is cooled down under TBP overpressure. Note that we intentionally induce slight overgrowth in the lateral direction during growth of the upper InAsP segment as a passivation layer for the inserts. Fig. 3-12(b) shows a SEM image of a close-up look of a highly-uniform InAsP nanowire array with InAs inserts. Additionally, InAsP barriers are grown in InAs nanowires on InAs (111)B substrates using a similar growth sequence given above.

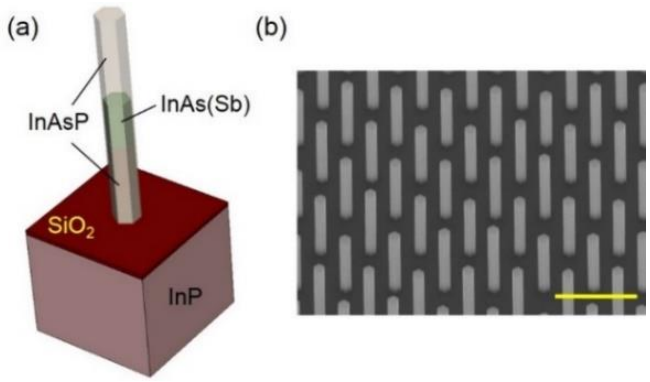

Figure 3-12 (a) Schematics of InAs(Sb) inserts in InAsP nanowires grown on InP (111)B. (b) A close-up look of nanowire array with InAs inserts. The scale bar is 1 μm.

The height and diameter of nanowires are characterized using SEM. PL measurement at cryogenic temperature (77 K) is carried out by a solid-state red laser at 671 nm as the pumping source (normal incidence, polarization ratio > 100:1) and a liquid-nitrogen cooled InSb detector in a Nicholet 6700 FTIR spectrometer. The incident laser power and the spot size on samples are calibrated as 2 mW and 50 μm, respectively. In addition, a step-scan mode with a resolution of 32 cm^{-1} is used for FTIR. The InAs inserts and InAsP barriers are further examined by scanning transmission electron microscope (STEM) and EDX. To prepare the STEM/EDX samples, nanowires are mechanically moved onto the grids with carbon films. The InAsP single-barrier devices are fabricated using a standard process. Temperature-dependent current-voltage (I-V) characteristics is performed from 77 K to 300 K and the CBOs are extracted by Arrhenius plots.

3.4.3 InAs inserts

Purely axial growth of small bandgap inserts is desired for nanowires because any overgrowth in the lateral directions may form a shunt path for carriers through the spacing between segments. Thus, the first part of the study concerns the growth condition to achieve a high aspect ratio, i.e., nanowire height divided by nanowire diameter, with enhanced axial growth and eliminated lateral growth. Interestingly, we observe that by tuning V/III ratio the aspect ratio can

be freely controlled. As shown in Fig. 3-13(a), three different V/III ratios of 16, 32, and 48 are applied to 30-sec growth of InAs inserts on top of InAsP bottom segments, which results in very different nanowire dimensions. The changes of height and diameter after InAs growth are characterized by SEM and summarized in Fig. 3-13(b), and the calculated aspect ratio as a function of V/III ratio is shown in the inset.

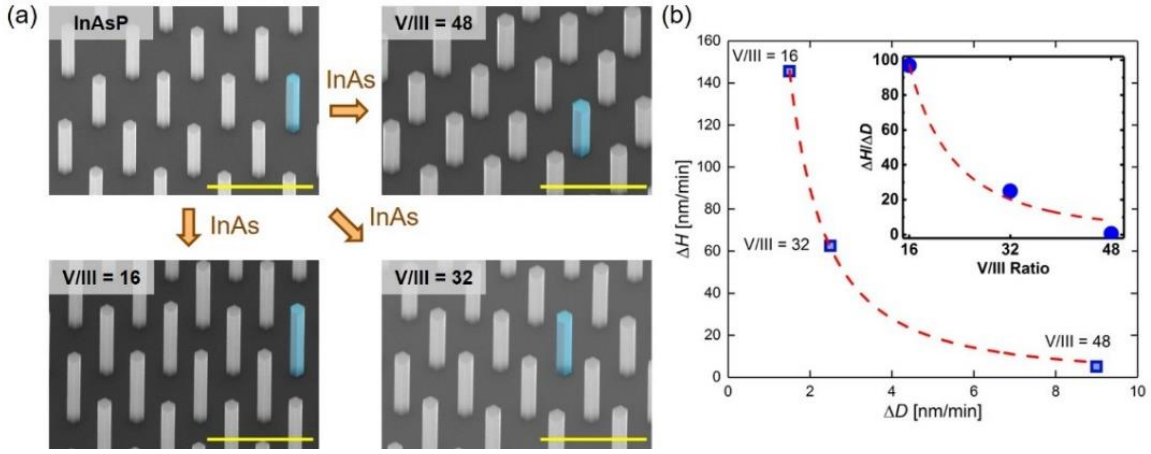

Figure 3-13 (a) SEM images of InAs segments grown on InAsP bottom segments using different V/III ratios of 16, 32, and 48. The scale bar is 1 μm. (b) The average change of nanowire height ΔH as a function of the average change of nanowire diameter ΔD after the growth of InAs inserts. The inset shows the aspect ratio of InAs growth as a function of V/III ratio.

The results are remarkable – an aspect ratio of nearly 100 is achieved using a V/III ratio of 16, meaning that growth of a 100 nm axial InAs insert only results in a lateral overgrowth of about four monolayers on nanowire sidewalls. The increase of aspect ratio with decreasing V/III ratio can be explained by a lower activation energy at the InAs-InAsP interface due to precursor pyrolysis or interpreted by an enhanced diffusion length of indium adatoms on SiO_2 growth mask due to less phosphorus.[91-93]

PL characterization of InAsP/InAs/InAsP heterostructures (shown in Fig. 3-12(a)) is carried out at cryogenic temperature (77 K), as shown in Fig. 3-14(a). The growth time of InAs inserts is

varied from 5 to 30 seconds. The emission peak at lower energy is attributed to the emission from InAs inserts, shaded in blue, which spans a wavelength range of 2.31 – 2.57 μm, while the peak at a higher energy results from InAsP segments. Spectrum fitting is accomplished by using only two Gaussian functions, suggesting interband transitions are the dominant form of emission for all segments. The peak energy of InAs inserts as a function of growth time is displayed in Fig. 3-14(b). We observe that the peak energy of InAsP segments is almost constant between 0.630 and 0.635 eV, while the peak energy of InAs inserts shifts towards higher energy with decreasing growth time. The phosphorus composition is estimated to be 0.23 and 0.24 based on our previous growth study of InAsP nanowires on InP substrates.[10] The peak shift of InAs inserts might result from phosphorus inter-diffusion at InAs-InAsP heterointerfaces, or the quantized well-like structure of InAs. Additionally, it is noted that the emission peak of InAs inserts grown for 30 seconds is at 0.483 eV, much different from the ZB InAs bandgap of 0.415 eV at 77 K. It is mainly due to a high-density of rotational twins, i.e. crystal phase switches between ZB and WZ, which is commonly observed in InAs nanowires grown by selective-area growth mode.[38,39]

Having determined the peak energy, we study the surface passivation for InAs inserts. As mentioned earlier, top InAsP segments are intentionally grown laterally to realize passivation layers with larger bandgap. It is known that by introducing phosphorus into InAs the surface state density can be largely suppressed.[86,94,95] Here, we compare the PL emission from two nanowire arrays with 30-sec and 60-sec InAsP top segments while the growth time of InAs inserts is kept fixed at 30 seconds. The measured PL spectra are depicted in Fig. 3-14(c). As expected, the emission from inserts is enhanced by a factor of seven with no shift of InAs peak energy. Thus, it is evident that the increased emission results from a reduction of surface state density at nanowire surface.

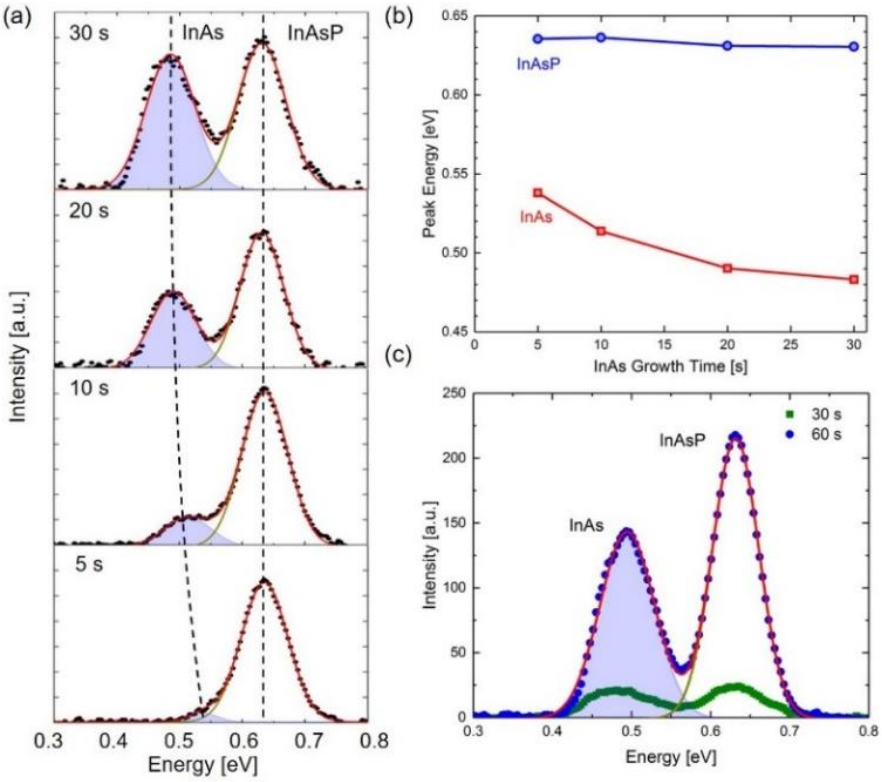

Figure 3-14 (a) PL (77 K) of nanowire arrays with InAs inserts. The growth time of inserts is varied from 5 to 30 seconds. (b) A summary of peak energy as a function of growth time of InAs inserts. (c) Optical emission of nanowire arrays where the InAsP top segments are grown for 30 and 60 seconds.

Fig. 3-15 shows STEM/EDX characterization of a single nanowire with a 60-sec InAs insert. The insert is clearly shown in the highlighted region with an estimated width of 150 nm. In this study, we use a 2-sec H_2 purging scheme during growth interruptions between segments as the source gas switching procedure. The duration of H_2 purging is critical – the residual arsenic or phosphorus adatoms need to be fully removed to avoid being incorporated into the next growth segment. This is normally known as the "memory effect" for As/P material systems.[96,97] One potential solution is to optimize the switching sequence of As/P by extending the time of H_2 purging scheme to fully remove any residual arsenic or phosphorus adatoms on dielectric growth masks. Since the EDX measurement was performed on an as-grown nanowire (no thinning), the

scan resolution is insufficient to accurately assess the abruptness of the heterointerface and so further study will be necessary.

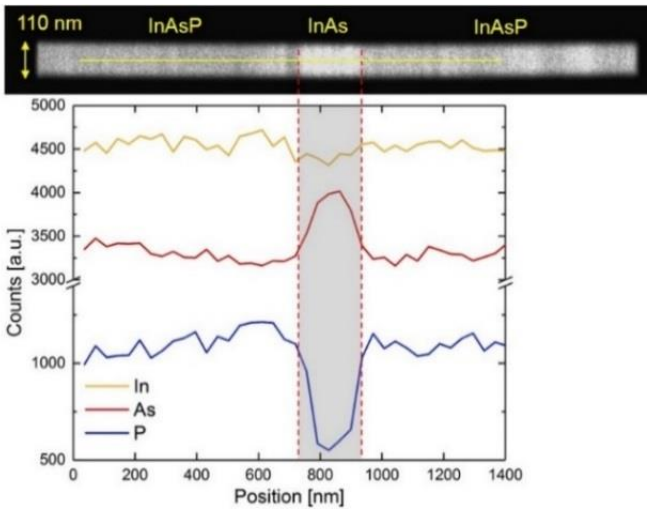

Figure 3-15 STEM and EDX line-scan of a single nanowire with a 60-sec InAs insert.

3.4.4 InAsSb inserts

We now perform a study of InAsSb inserts in InAsP nanowires. Growth of purely axial InAsSb inserts is achieved using a V/III ratio of 4, as shown in Fig. 3-16(a). The axial growth rate of InAsSb is determined to be 282 nm/min. Similar to the previous growth of InAs inserts, the top InAsP segments are used as high bandgap passivation layers. We perform 77 K PL measurements of as-grown samples of InAsSb/InAsP and InAsP/InAsSb/InAsP, as shown in Figs. 3-16(b) and (c), respectively. In Fig. 3-16(b), the emission peak of InAsSb, shaded in blue, is at 0.390 eV, i.e., 3.12 μm. It is not surprising that there is no InAsP emission in the spectrum and the signal from InAsSb nanowires is weak. First, an exchange of arsenic and phosphorus on nanowire surface occurs during InAsSb growth, resulting in an arsenide-like surface with high density of surface states for the bottom InAsP segments. Second, the weak InAsSb emission is due to a high surface state density as well. By adding the top InAsP segments, inserts and bottom InAsP segments are

properly passivated, and thus, the emission from both inserts and InAsP segments are dramatically enhanced, as shown in Fig. 3-16(c).

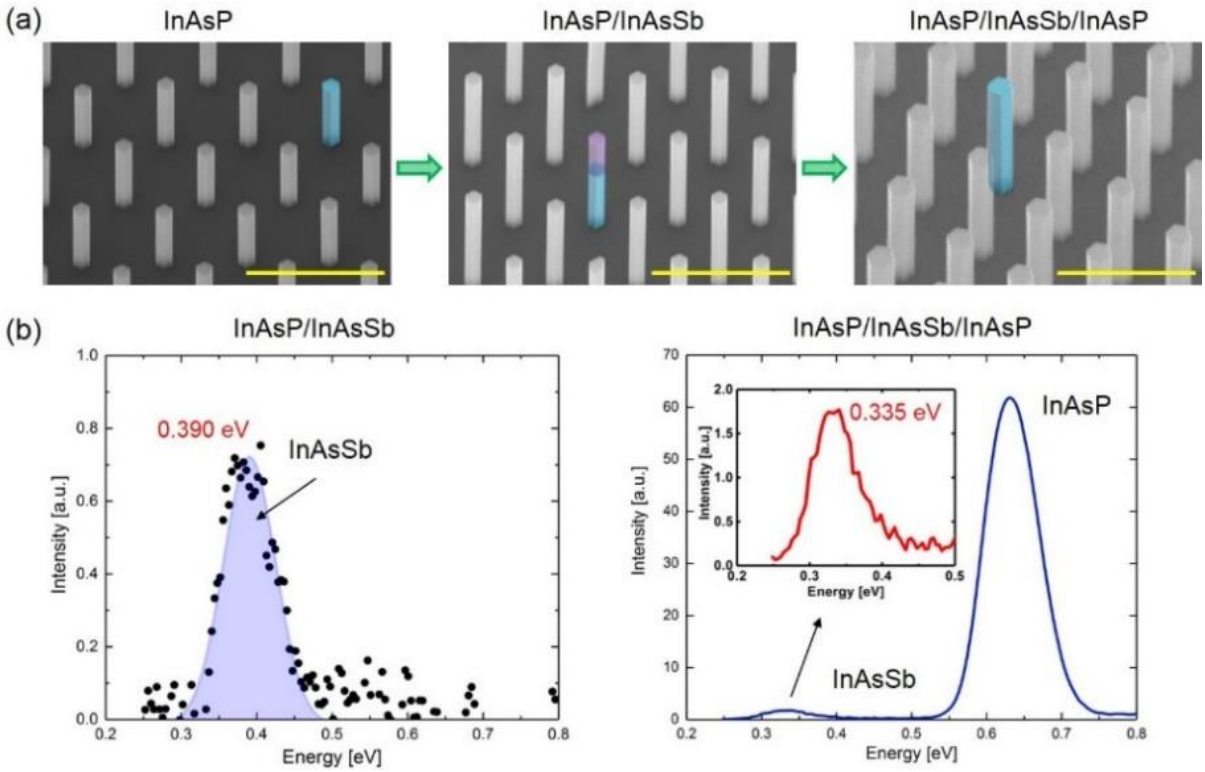

Figure 3-16 (a) SEM images of growth process of InAsSb inserts. (b) PL characterization (77 K) of InAsP/InAsSb and InAsP/InAsSb/InAsP heterostructures, respectively. The inset shows a close-up look of emission from InAsSb inserts.

We note that the peak energy of InAsSb is shifted from 0.390 eV to a lower energy of 0.335 eV (3.70 μm), which results from a relaxation of Fermi-level pinning at the surface of InAsSb inserts. The antimony composition is estimated to be between 0.08 and 0.10 based on previous growth studies of InAsSb nanowires.[54] Additionally, the full-width half-max (FWHM) of the InAsSb peak is 73.7 meV, higher than the value obtained from InAsSb bulk nanowires, which is about 45.0 meV.[54] This might be due to a nonuniform antimony composition across the insert segment.

3.4.5 InAsP barriers

Equipped with the growth capability of InAs-InAsP heterostructures, we move forward to determine CBOs of those type-I heterojunctions. The device structure is designed as InAs (conducting layer)/InAsP (barrier)/InAs (conducting layer). where the current is limited by thermionic emission of electrons (InAs is unintentionally doped as n-type). The current can be simply described as

$$I \propto T^2 exp[-q\emptyset(V)/kT] \tag{3.1}$$

where T is the temperature, and $q\Phi(V)$ is CBO as a function of applied bias.

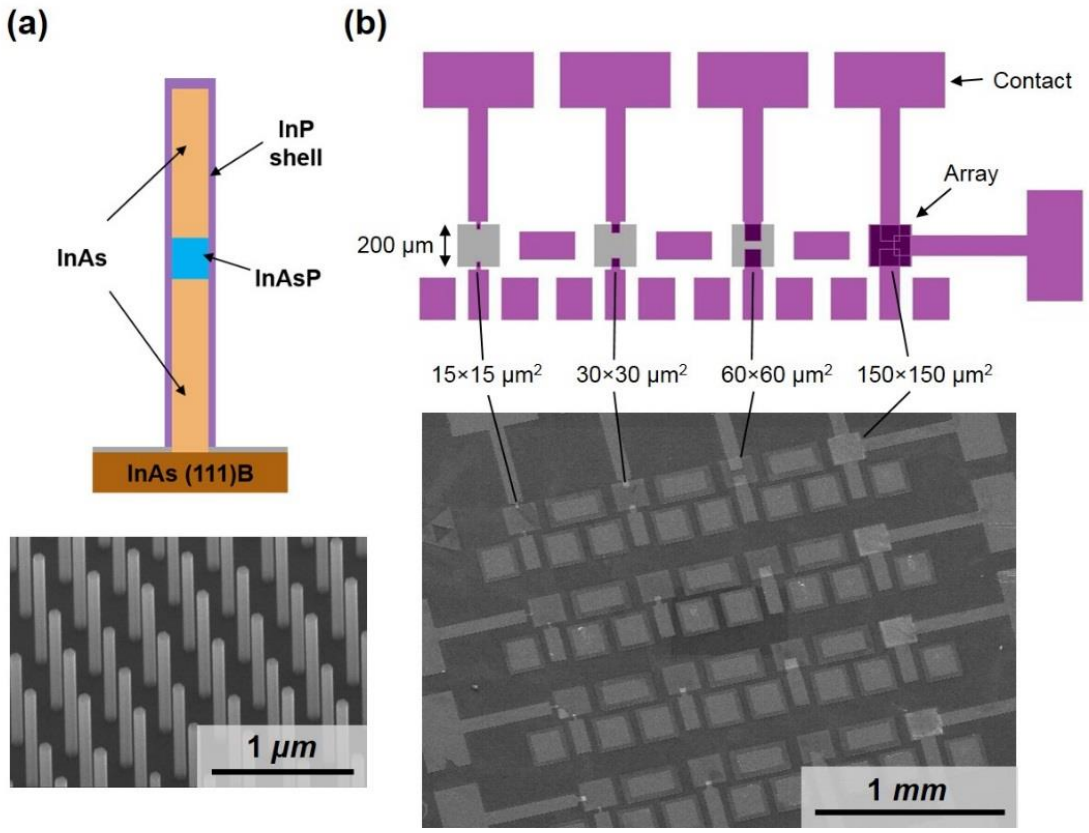

Figure 3-17 (a) Schematics of InAsP single-barrier devices and SEM image of one as-grown nanowire array. (b) The schematics of area-dependent metal contact (top). The bottom image shows the nanowire arrays after fabrication with patterned Cr/Cu top and bottom contacts.

In order to determine CBOs of InAs-InAsP, we perform the growth of single InAsP barriers in InAs nanowires and then electrically extract the values by Arrhenius plots. The schematics of growth structure is shown on the top of Fig. 3-17(a), where the InP layer acts as surface passivation shell. The size of nanowire array is 150 × 150 μm^2. The SEM image on the bottom of Fig. 3-17(a) shows one of as-grown nanowire arrays. The growth rate of InAsP barriers is carefully calibrated by multiple growths of InAsP layers on InAs nanowires. In addition, to study the area-dependent property of devices, we design metal contacts (top) with four different areas – 15 μm × 15 μm, 30 μm × 30 μm, 60 μm × 60 μm, and 150 μm × 150 μm, as illustrated in Fig. 3-17(b). The SEM image of fabricated devices is shown in Fig. 3-17(b) as well.

To extract CBOs, the I-V characteristics are carried out at temperatures from 77 K to 300 K on three arrays with contact areas of 30 μm × 30 μm, 60 μm × 60 μm, and 150 μm × 150 μm, as shown in Fig. 3-18(a) (the electrical measurement is not repeatable for devices with 15 × 15 μm^2 contacts). Note that the current density is normalized by the top contact area. It is clearly observed that the current densities are very close in all cases, indicating high growth uniformity across the samples. The CBOs (in units of meV) as a function of applied bias are illustrated in Fig. 3-18(b) at bias of -0.5 to 0.5 V. Note that the CBO increases with decreasing bias due to the decrease of energy difference between Fermi-level and conduction band of InAsP barrier. Finally, the zero-bias CBOs can be estimated as the measured barrier height at a small bias, which would be -0.05 or 0.05 V. We note that the extracted zero-bias CBOs are slightly different between devices with different contact areas (128 meV, 136 meV, and 106 meV, respectively), which might be explained as: (1) the CBOs of InAs-InAsP heterostructures across the entire 150 × 150 μm^2 array are not constant due to the variation of phosphorus composition of InAsP, which might be caused by the nonuniform flow of TBP, or (2) the fitting error of band offsets.

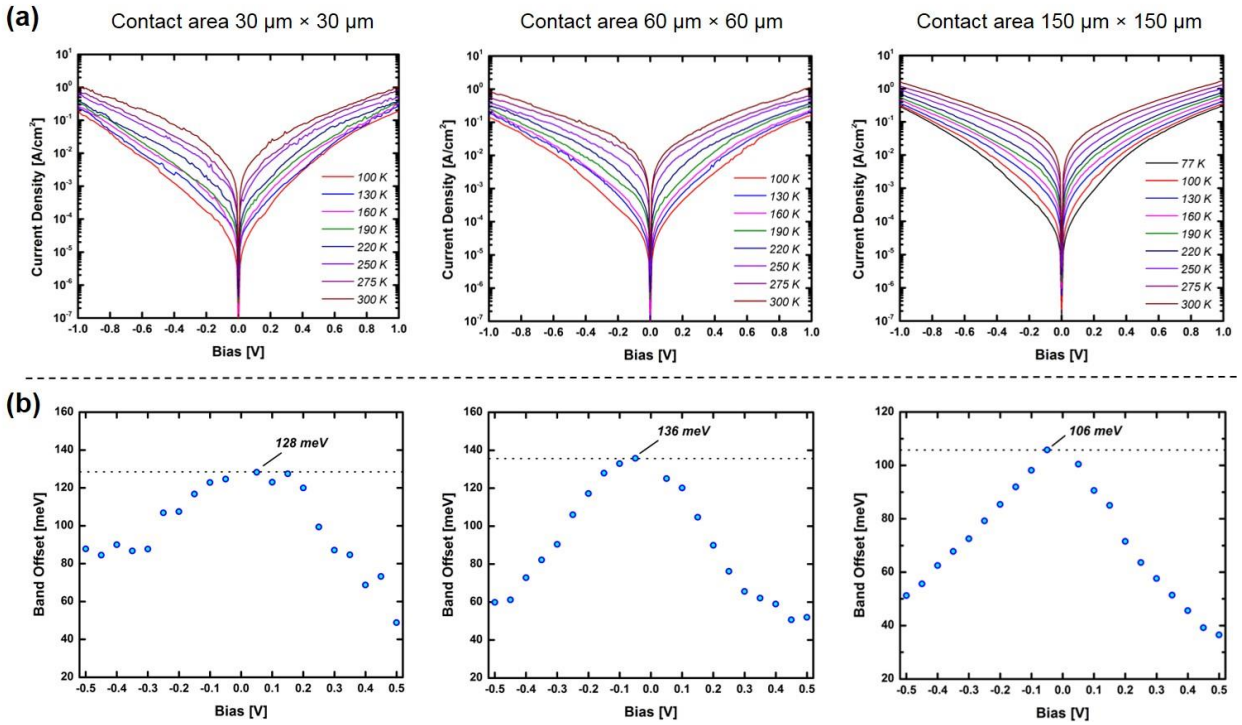

Figure 3-18 Characteristics of InAsP single-barrier devices with three different contact areas – 30 × 30 μm^2, 60 × 60 μm^2, and 150 × 150 μm^2. (a) The temperature-dependent I-V characteristics. (b) Extracted CBOs as a function of applied bias and extrapolated zero-bias band offsets.

To correlate the measured CBOs with the phosphorus compositions, we perform energy-EDX along nanowire cross-section thinned by focused ion beam (FIB). Fig. 3-19(a) shows a cross-section SEM image of fabricated single-barrier device with a 150 × 150 μm^2 top contact. The STEM images of nanowire cross-section are shown in Fig. 3-19(b), where the routine of EDX line scan is marked. The phosphorus count as a function of position is shown in Fig. 3-19(c). The width of potential barrier is then estimated as 100 nm, and the peak of spectrum gives a phosphorus composition of 0.21, which corresponds to bandgap energy of 0.550 eV at 300 K. Thus, the theoretical CBO can be estimated as

$$CBO(eV) = \left(E_g^{InAsP} - E_g^{InAs}\right) \times 0.65 = 0.121\ eV \tag{3.2}$$

Note that the actual CBO would be lower because the bandgap of InAs nanowire with multi-phase crystal structures, i.e., mixture of ZB and WZ, is higher than 0.364 eV. Thus, the measured CBO of this sample is close to the estimated value by EDX. However, the phosphorus count shows a triangular profile with a transition width of around 40 nm. This can be explained by the following reasons: (1) the inter-diffusion of phosphorus is significant, and (2) the resolution of EDX measurement is not high enough and limited by the scattering from thick sample.

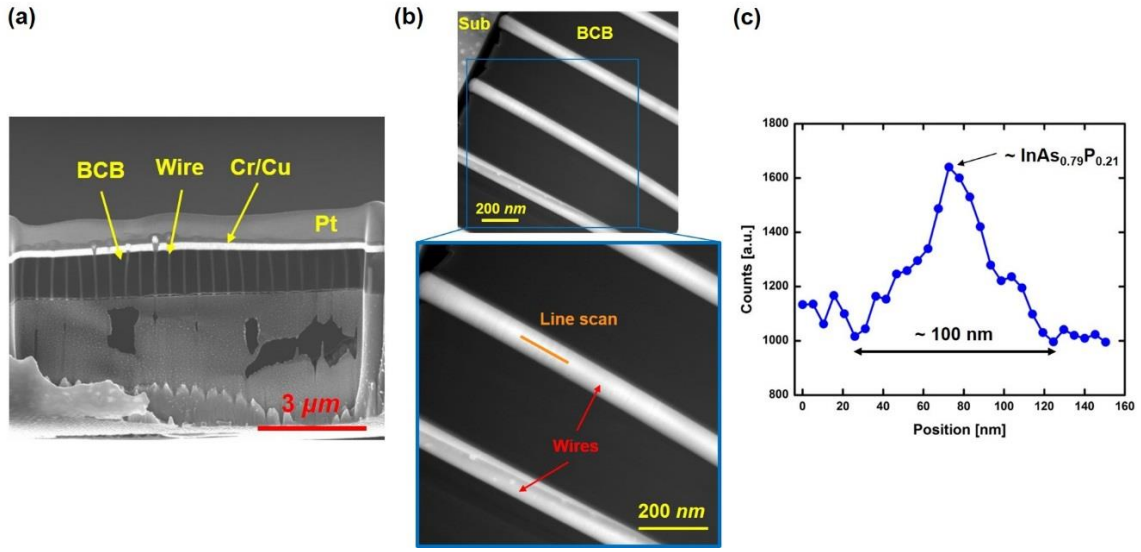

Figure 3-19 (a) The cross-section of fabricated single-barrier devices with a 150 × 150 μm^2 top contact. (b) STEM images of nanowires. The position for EDX line scan is marked. (c) The count of phosphorus as a function of position. The barrier width is estimated as 100 nm, and the peak shows a phosphorus composition of 0.21.

3.4.6 Summary

We grew InAs and InAsSb inserts in InAsP nanowires on InP (111)B substrates as well as InAsP barriers in InAs nanowires by SA-MOCVD. We observed optical emission of InAs(Sb) inserts spanning a wavelength range from 2.31 – 3.70 μm from interband transition by PL characterization. The growth of InAs inserts was further examined by STEM/EDX. It is worth

noting that by choosing a proper V/III ratio, we achieved the growth of inserts with high aspect ratio. In addition, we fabricated InAsP single-barrier devices and electrical extracted the CBOs of InAs-InAsP heterojunctions yielding 106 – 136 meV. The phosphorus composition and the heterointerface quality was further investigated by the line-scan EDX. We believe that this study provides a new material system based on InAs(Sb)-InAsP heterostructures for interband and intersubband optoelectronics.

4. Nanowire optoelectronic devices based on InAs(Sb)

4.1 Overview

III-V photodetectors operating at short-wavelength infrared (SWIR, 1.4 – 3 μm) and mid-wavelength infrared (MWIR, 3 – 5 μm) are sensors of choice for a broad range of demanding applications such as remote sensing, deep space imaging, and spectroscopy. These detectors require high detectivity and low noise; however, their room-temperature operation commonly suffers from low signal-to-noise ratio (SNR) due to high dark current from generation-recombination (G-R) and minority carrier diffusion. A promising alternative approach is to develop device with bottom-up vertical III-V nanowires to circumvent the drawbacks of traditional planar detectors and achieve better device performance for photodetection in these wavelength regimes. Their unique properties, namely small junction area and heteroepitaxy of small bandgap photoabsorbers on large bandgap materials, are advantageous for significantly suppressing dark current. This is because (1) the volume of nanoscale photoabsorbers is small due to the small fill factor, and (2) the density of minority carriers from large bandgap materials is much smaller than that of small bandgap materials. Additionally, elastic deformation, which is prohibited in thin-film growth techniques with large lattice mismatches, at the heterointerfaces can fully eliminate threading dislocations and minimize point dislocations.

One ideal scheme of making SWIR or MWIR photodetectors is to integrate small bandgap nanowire photoabsorbers onto large bandgap substrates to form *p*-*n* heterojunctions. In this case, the dark current is predominantly determined by the nanowire's heterointerface quality and the nanowire-air (or nanowire-passivation) surface quality in the depletion region. Therefore, in order

to show the potential of nanowire-based photodetectors at SWIR and MWIR, it is crucial to demonstrate the quality of heterojunctions and develop surface passivation techniques that yields lower dark current than their planar device counterparts. We believe this study paves the way for room-temperature operation and high detectivity in next-generation photodetectors at SWIR and MWIR.

This chapter is divided into two major sections showing the development of InAs(Sb) nanowire photodetectors. These devices are fabricated with self-aligned plasmonic gratings to largely enhance optical absorption by exciting surface plasmons and tightly confining photogenerated carriers at nanowire tips. The first part shows the demonstration of InAs nanowire photodetectors at SWIR composed of vertically oriented selective-area InAs nanowire photoabsorber arrays on InP substrates, forming InAs-InP heterojunctions. We measure a rectification ratio greater than 300 at room temperature, which indicates a desirable diode performance. The dark current density, normalized to the area of nanowire heterojunctions, is 130 mA/cm^2 at a temperature of 300 K and a reverse bias of 0.5 V, making it comparable to the state-of-the-art bulk InAs *p-i-n* photodiodes. An analysis of the Arrhenius plot of the dark current at reverse bias yields an activation energy of 175 meV from 190 K to 300 K, suggesting that the Shockley-Read-Hall (SRH) nonradiative current is the primary contributor to the dark current. By using three-dimensional electrical simulations, we determine that the SRH nonradiative current originates from the acceptor-like surface traps at the nanowire-passivation heterointerfaces. The spectral response at room temperature is also measured, with a clear photodetection signature observed at wavelengths up to 2.5 μm. The second part presents the demonstration of uncooled InAsSb nanowire photodetectors at MWIR composed of vertical selective-area InAsSb nanowire photoabsorber arrays on large bandgap InP substrate with nanoscale plasmonic gratings. The non-radiative recombination at InAsSb nanowire surfaces is significantly suppressed by introducing *ex-situ* conformal Al_2O_3 passivation shells, and an extremely low surface recombination velocity in the order of 10^3 cm/s is estimated by transient simulations. Furthermore,

room-temperature emission from InAsSb nanowires is achieved, spanning the entire MWIR regime from 3 μm to 5 μm. A dry-etching process is developed to expose only the top nanowire facets for metal contacts with sidewalls fully covered by Al_2O_3 shells, allowing for a higher internal quantum efficiency. Based on those techniques, we fabricate nanowire photodetectors with optimized pitch and diameter, and show room-temperature spectral response with MWIR detection signatures at 3.4 μm.

4.2 InAs nanowire photodetectors

4.2.1 Introduction

Great progress has been made recently for direct integration of vertical SWIR nanowire photoabsorbers on large bandgap materials. Examples of some pioneering studies include (1) single *n*-InAs nanowire on *p*-Si for photodetection at 1470 nm;[98] (2) *n*-InAs nanowire arrays on *p*-Si for wavelengths spanning up to 3 μm;[99] (3) *n*-InAs nanowire arrays on *n*-Si for a wavelength range covering 1.4 – 3.0 μm;[100] (4) unintentionally doped *n*-InAsSb nanowires on *p*-InAs (grown on GaAs substrate), giving a photoresponse up to 3.5 μm;[101] and (5) InAsSb *p*-*i*-*n* nanowire arrays on *p*-Si offering photoresponse up to ~3 μm.[102] However, a thorough analysis of the G-R mechanisms at reverse bias and a cross-comparison of its dark current with those of planar devices has not yet been performed. Note that the dark current in a 3-D nanowire−substrate *p*-*n* diode with a heterointerface is predominantly determined by the heterointerface quality and the nanowire-air (or nanowire-passivation) interface quality around the nanowire depletion region. Therefore, the carrier dynamics in nanowires are more complicated than in planar devices,[1,103] which needs to be thoroughly considered when developing high-performance nanowire-based optoelectronic devices.

In this work, we present the electrical and optical properties of an InAs-InP heterojunction nanowire photodetector at SWIR, which is composed of vertically oriented, *n*-InAs nanowire

photoabsorber arrays grown on *p*-InP substrates with selective area epitaxy. The nanowires are passivated with *in-situ* InP shell layers (~ 5 nm) to reduce nonradiative recombination centers on the surfaces.[39] These InAs-InP photodiodes with *p-n* heterojunctions exhibit a room-temperature rectification ratio greater than 300 and photodetection at wavelengths up to 2.5 μm. To compare the dark current of our devices with the state-of-the-art InAs *p-i-n* diodes, we normalize the measured dark current values to the active area of the InAs-InP nanowire heterojunctions, rather than the area of the nanowire array.[27] We observe nearly identical dark current density. To further understand the dark current mechanism, we apply a 3-D computational model to fit temperature-dependent current-voltage (I-V) curves and extract heterointerface and surface properties. The resultant simulations indicate that the suppression of dark current, via reduction of absorption volume and implementation of *p-n* heterojunctions, was offset by an increase in surface leakage current on the nanowire sidewalls. Finally, we show the feasibility of achieving high detectivity by using the nanowire InAs-InP heterojunction platform to break the trade-off between high responsivity and low dark current. This study provides an understanding of dark current for small bandgap selective-area nanowires, and paves the way to integrate these nanostructured photoabsorbers on large bandgap substrates for high-performance photodetectors at SWIR.

4.2.2 Nanowire epitaxy and fabrication

The nanowires are grown by SA-MOCVD. The substrate is a Zn-doped 2-inch on-axis InP (111)B wafer. We choose InP as the large bandgap substrate because it is feasible to achieve dislocation-free InAs-InP heterointerface for nanowire diameters up to 100 – 120 nm due to its modest lattice mismatch of 3.2%.[23] InAs-Si or InAs-GaAs heterojunctions suffer larger mismatches of 11.6% and 7.2% respectively. A 2-D triangular lattice with nanohole diameter of 40 nm and pitch of 400 nm is patterned on a ~20 nm SiO_2 mask layer, atop an InP substrate, to

promote selective area InAs nanowire growth. The overall size of the nanowire array is 100 μm × 100 μm, containing a total of 72,000 nanowires. The gaseous precursors during MOCVD growth are trimethylindium (TMIn), tertiarybutylarsine (TBAs), and tertiarybutylphosphine (TBP). Prior to the growth of the InAs nanowire segment (V/III ratio of 8), a thin InAs seeding layer (V/III ratio of 32) is introduced as a buffer to assist nucleation along the (111)B orientation and avoid formation of any twin boundaries along the (111)A orientation.[85,104] InAs nanowires are unintentionally *n*-doped and are *in-situ* passivated by InP shells (intrinsic, thickness of ~ 5 nm, V/III ratio of 8) to reduce nonradiative surface recombination centers on the nanowire sidewalls.[39] The as-grown nanowires have a diameter of 100 nm (without the InP passivation shells) and a height of 1.4 μm. A SEM image of the nanowire array with high vertical yield and high uniformity is shown in Fig. 4-1(a).

Following the growth, the nanowires are planarized using benzocyclobutene (BCB), an electrically insulating filler medium between the nanowires that supports the top contact and isolates it from the bottom. Vias to the InP substrate are defined by photolithography. The BCB film is then cured at 250°C for 60 minutes and an Au (20 nm)/Zn (20 nm)/Au (200 nm) film is deposited on the substrate to define the bottom p-contact. Then, the BCB film is etched back using reactive ion etching process to expose ~400 nm of the nanowire tip, followed by a 15-second selective HCl:H_2O (1:2) chemical etch of the InP passivation shells for top metal contacts. Next, a Cr (10 nm)/Au (150 nm) film is deposited atop the nanowire tips at a tilt angle of ~45° to form plasmonic gratings that would strongly couple incident light on surface plasmon resonance. Schematics of the device structure are illustrated in Fig. 4-1(b) and a SEM image of the self-aligned plasmonic couplers are shown in Fig. 4-1(c). The spectral response measurement is then conducted

by packaging the fabricated InAs photodetector array on a 68-pin leadless chip carrier through wire bonding, as shown in Fig. 4-1(d).

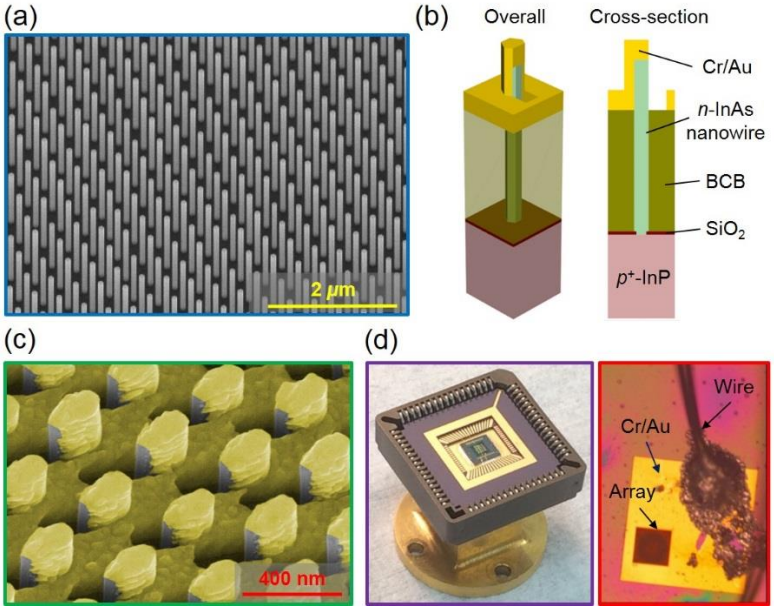

Figure 4-1 (a) As-grown InAs nanowire arrays on InP (111)B substrate. (b) Schematics of the unit cell of an InAs nanowire photodetector (InP passivation layer is not shown). (c) Close-up view of plasmonic gratings. (d) Wire-bonded photodetector device sample (left). (d) Close-up view of the wire-bonded nanowire array (right). The size of the array is 100 μm × 100 μm.

4.2.3 Diode analysis

Temperature-dependent I-V characterization of the device from 100 K to 300 K are carried out using a Lakeshore PS-100 cryogenic probe station, as shown in Fig. 4-2(a). We observe a rectification ratio greater than 300 at 300 K and greater than 2000 at 100 K (at 1 V, both forward and reverse biased). We then compare the dark current level of our devices with that of planar InAs *p-i-n* photodiodes (working in photovoltaic mode at room temperature, grown by either MOCVD or molecular beam epitaxy) as a means for quantifying the dark current of our device.[36,105,106] For planar photodiodes, the dark current level is quantified as dark current density, $J_{Dark\_J} = I_{Dark}/A_J$, where I_{Dark} is the measured dark current and A_J is the area of the etched homojunction or

heterojunction mesa. However, nanowire photodiodes with nanowire-substrate *p*-*n* heterojunctions do not have an easily defined device (or effective) area A_{Eff}, which poses a challenge in efficiently comparing nanowire and planar devices.[27] As a result, to make a fair comparison, we normalize the dark current to the junction area of the *n*-InAs/*p*-InP photodiodes instead. Since the depletion regions extend from the bottom nanowire segments, the total junction area is the sum of the area of all x-y cross-sections of the nanowires. In other words, $A_J = N \times A_{NW}$, where N is the total number of nanowires in an array and A_{NW} is the x-y cross-sectional area of a single nanowire.

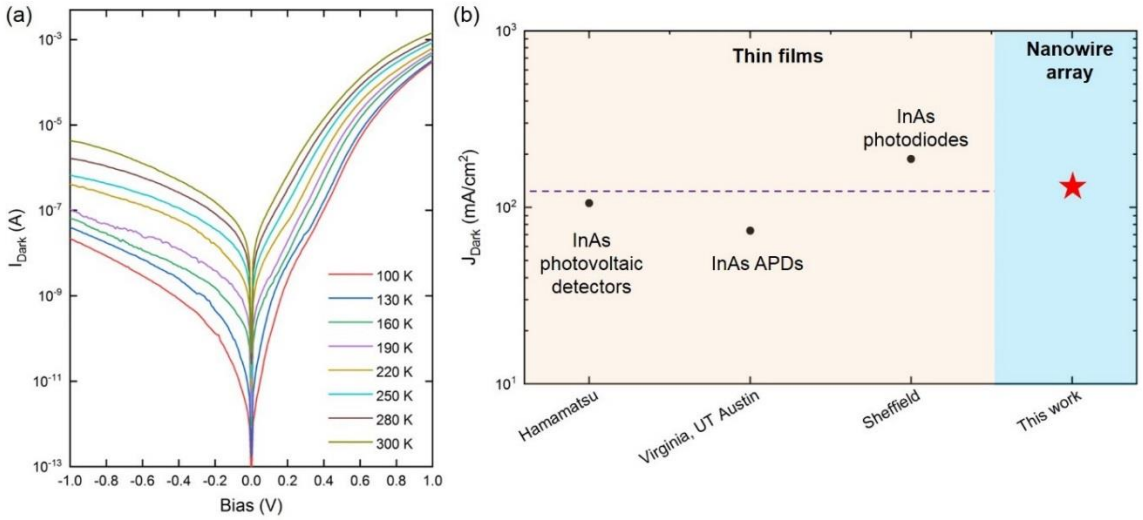

Figure 4-2 (a) Temperature-dependent I-V characteristics of InAs-InP photodiodes with nanowire-substrate *p*-*n* heterojunctions. (b) Comparison of room-temperature dark current density at a reverse bias of 0.5 V between the nanowire photodetector and the best commercial or research InAs homojunctions. The model of Hamamatsu uncooled InAs photovoltaic detector is P10090-01. The dark current of the InAs nanowire array is normalized by the junction area of the *n*-InAs/*p*-InP heterointerfaces (i.e., *n*-InAs nanowire cross-section A_J), not by the area of nanowire array (A_{Eff}).

As mentioned earlier, the photodetector array is composed of 72000 nanowires, and the average diameter (edge-to-edge, without InP passivation layers) of each nanowire is 100 nm (± 5 nm). With this information, we calculate the dark current density J_{Dark_J} of our nanowire array at

300 K and a reverse bias of 0.5 V to be about 130 mA/cm^2. Then, we compare our calculated J_{Dark_J} with that of the best commercial and research InAs *p-i-n* photodetectors, including photovoltaic detectors, avalanche photodetectors, and photodiodes, in similar characterization conditions (at 300 K and at a reverse bias of 0.5 V), as shown in Fig. 4-2(b).[36,105,106] Note that we simply use the mesa area as A_J when calculating the dark current density for the compared planar devices. The average J_{Dark_J} of the abovementioned planar devices is 123 mA/cm^2, marginally lower than the dark current level of our *n*-InAs/*p*-InP photodiodes.

Here, we provide further analysis to better understand the source of the dark current level of the InAs nanowire photodiodes. There are two critical factors that enable low dark current density: (1) significant suppression of minority carrier diffusion, and (2) high quality of InAs-InP heterointerfaces. The first factor can be simply interpreted by the saturation current density equation for a heterojunction given by[107]

$$J_0 \equiv q\left(\frac{D_{p1}}{L_{p1}N_{D1}}n_{i1}^2 + \frac{D_{n2}}{L_{n2}N_{A2}}n_{i2}^2\right), \tag{4.1}$$

where D is the diffusivity of the minority carriers, L is the diffusion length, N is the impurity concentration, n_i is the intrinsic carrier concentration, and the subscripts 1 and 2 refer to two different materials. For the InAs nanowire photodiodes, materials 1 and 2 are *n*-type InAs and *p*-type InP respectively. Our approach is to achieve low J_0 by reducing n_{i1} by significantly reducing *n*-type volume (InAs nanowire) and n_{i2} using a large bandgap substrate, i.e., InP instead of InAs. Regarding the second factor, nanowire heteroepitaxy allows for a dislocation-free heterointerface, as the diameter of the nanoholes is only 40 nm. The thin-film heteroepitaxy technique, on the other hand, cannot achieve such heterointerface, as the large lattice mismatch and difference in thermal expansion coefficient between the two materials will inevitably cause the formation of high-density threading dislocations and point dislocations. Note that since the heterointerfaces are

located within the active *p-n* junctions, any local defects within the heterointerfaces can contribute to nonradiative recombination and leakage current, which significantly degrade the photodetector performance.

Based on the explanation in the previous paragraph, we expect that J_{Dark_J} of the nanowire device should be even lower than the values reported for thin-film InAs *p-i-n* devices.[36,105,106] Note that the bandgap of InAs nanowires is 0.442 eV, different from the bulk zinc-blende (ZB) InAs bandgap of 0.365 eV at 300 K (further discussion on the significance of this will be provided in the next section). Thus, the intrinsic carrier concentration of the InAs nanowires, given by n_{i1} in Eq. 4.1, is lower than that of ZB InAs, and therefore is expected to have less contribution to the dark current. We note that the dark current of the nanowire device (at 300 K) shows a strong dependence on the applied voltage when reverse biased, having a two-order increase from 0.1 V to 1.0 V. At such low biases, field sensitive current generation mechanisms such as trap-assisted tunneling and avalanching are not likely to be the contributors to the dark current. Rather, the increase in dark current can be attributed to the surface leakage on the nanowire sidewalls between the InAs nanowire cores and InP passivation shells. With increasing reverse bias, the heterojunction extends further into the InAs nanowire segments, meaning that a larger surface area will be depleted and further contribute to the dark current. This is not surprising because the performance of nanowire-based devices is predominantly affected by the surface leakage due to the large surface-to-volume ratios of the nanowires.

To determine whether the surface leakage can account for the bias-dependent increase of dark current, we perform further analysis of temperature-dependent I-V curves by extracting the activation energy at reverse biases of 0.2 V, 0.5 V, and 1.0 V and temperatures from 170 K to 300 K using the following exponential relationship

$$I_{Dark} \propto T^{3/2} \exp\left(\frac{-E_A}{k_B T}\right) \tag{4.2}$$

where I_{Dark} is the dark current, T is the temperature, E_A is activation energy, and k_B is the Boltzmann constant. The resultant activation energies for the given temperature and bias values are consistently between 0.173 eV and 0.175 eV, as shown in Fig. 4-3. Typically, the Fermi-level of a bare InAs nanowire without surface passivation is pinned above its conduction band due to its large surface state density. However, by adding InP passivation layers, the Fermi level lowers toward the midgap (hovering about 0.046 – 0.048 eV above it), indicating a significant reduction of surface states.

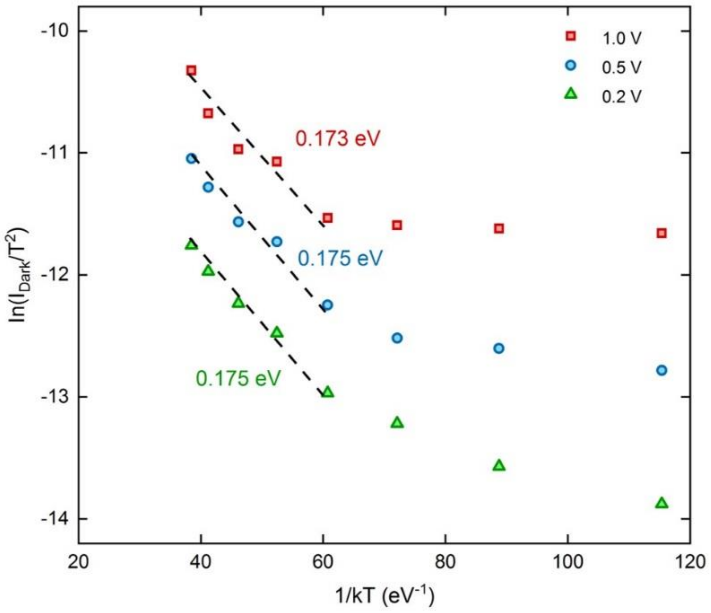

Figure 4-3 Arrhenius plot of the measured current at reverse biases of 0.2 V, 0.5 V, and 1.0 V. Extracted values of activation energy are labeled.

To further quantify I_{Dark} of InAs nanowire photodiodes, we perform 3-D electrical simulation (in Synopsys Sentaurus TCAD) to fit the I-V curves (in Fig. 4-2(a)) and extract InAs nanowire surface properties. To achieve this, we simulate a unit cell of a nanowire array that comprises of two InAs nanowires (with InP passivation shells for each), a dielectric growth mask

(SiO_2), a growth substrate (InP), and ambient air, as schematically shown in Fig. 4-4(a). The dimensions of the simulated nanowires are defined from measuring the dimensions of the actual nanowires from the SEM measurements. Note that the 3-D metal top contacts are defined on the exposed nanowire segments to mimic the actual fabricated device with plasmonic gratings. In the electrical model, the effects of Shockley-Read-Hall (SRH) nonradiative recombination are introduced into the nanowire-passivation (*n*-InAs/*i*-InP) interface, the nanowire-substrate (*n*-InAs/*p*-InP) interface, and the nanowire-air interface. The local trap capture and emission model (surface trap model) is applied to the InAs-InP nanowire-passivation heterointerfaces, described by the equation[107]

$$R_{Trap} = \frac{N_t v_{th}^p v_{th}^n \sigma_p \sigma_n (np - n_i^2)}{v_{th}^p \sigma_p (p + p_1) + v_{th}^n \sigma_n (n + n_1)} \tag{4.3}$$

with

$$p_1 = n_i exp\left(\frac{-E_t}{k_B T}\right) \tag{4.4}$$

and

$$n_1 = n_i exp\left(\frac{E_t}{k_B T}\right) \tag{4.5}$$

where N_t is the trap density (in cm^{-2}), v_{th} is the thermal velocity (in cm s^{-1}), σ is the trap cross section (in cm^2), and E_t is the trap energy, or the energy difference between the trap state and midgap state (in eV). In the simulations, E_t is kept fixed at 0.75 eV while N_t varies as a fitting parameter. The carrier traps are specified as acceptor-like surface traps (neutral when unoccupied and negtively charged when occupied by electrons). For nanowire-substrate (*n*-InAs/*p*-InP), nanowire-air (*n*-InAs/vacuum) and nanowire-mask (*n*-InAs/SiO_2) interfaces, we introduce surface recombination velocities instead of trap states to reproduce the nonradiative recombination

mechanisms, as shown in previous studies for heterointerfaces.[1] Finally, the simulated dark current of one unit cell is multiplied by 36000 (the number of unit cells within the 100 μm × 100 μm nanowire array) to find the total dark current produced by the nanowire array.

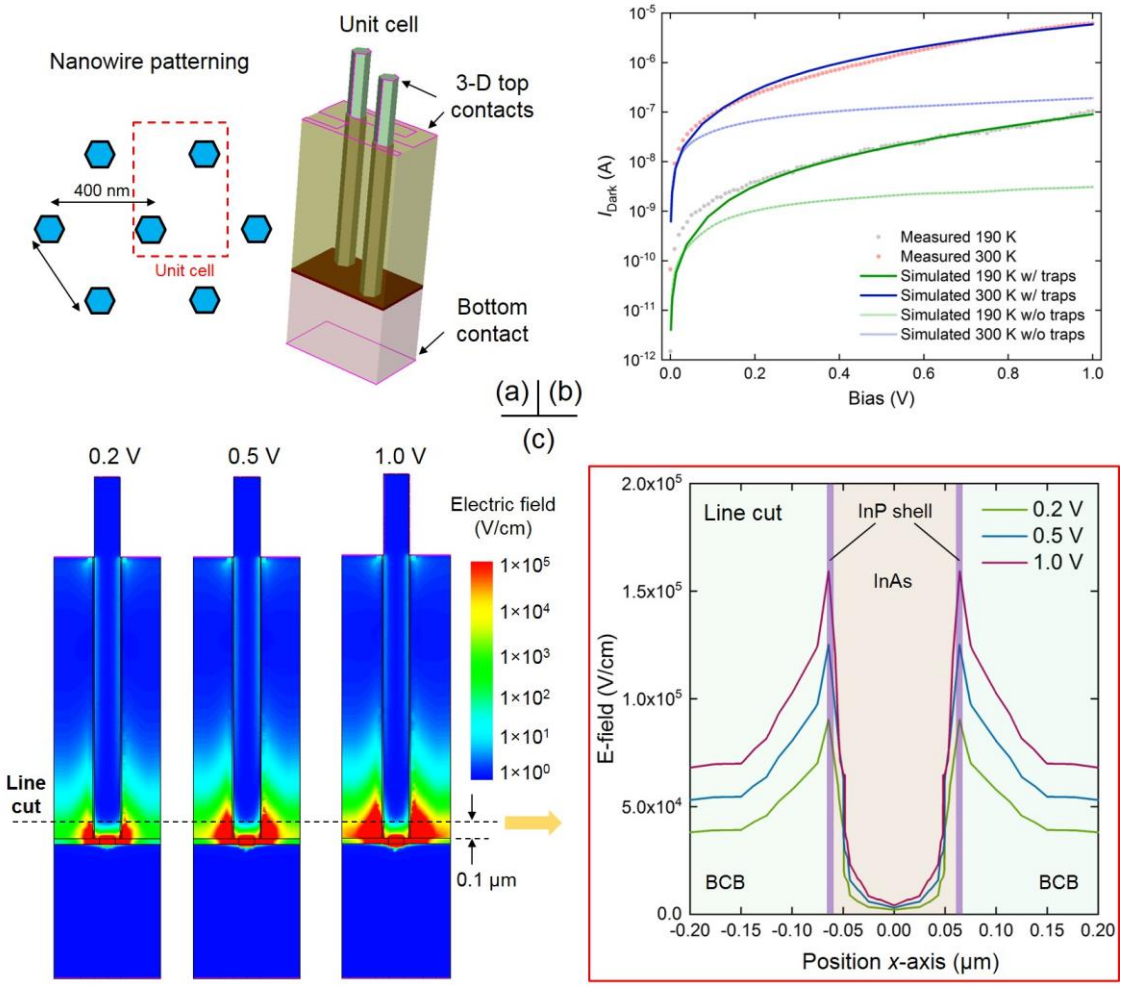

Figure 4-4 (a) Schematics of a unit cell in the electrical model. (b) Comparison of simulated and measured dark current (reverse biased) at 190 K and 300 K, both with and without the surface trap model. (c) Left: cross-sectional mapping of simulated electric field distributions at reverse biases of 0.2 V, 0.5 V, and 1.0 V. Right: line cut of electric field profiles along the *x*-axis (region labeled in (c)).

Fig. 4-4(b) shows the simulated I-V curves at 190 K and 300 K with and without the surface trap model. The fitted N_t at the nanowire-passivation (InAs-InP) heterointerfaces is 2×10^{12} cm^2. It becomes immediately clear that the simulated dark current of nanowires with surface traps has a

strong dependence on bias. Without surface traps, the dark current is mostly attributed to the minority carrier diffusion and depletion layer G-R. Note that the simulated dark current without surface traps is almost constant at higher biases (> 0.2 V) because the contribution from saturation current (i.e. minority carrier diffusion from *n*-InAs nanowires) is much greater than from generation-recombination within depletion regions. Fig. 4-4(c) shows cross-sectional views of the electric field profiles at reverse biases of 0.2 V, 0.5 V, and 1.0 V, along with a line cut along the *x*-axis near the bottom of the nanowire. Initially, the electric field is confined between the nanohole and the bottom segment of BCB. As the bias is increased, the depletion region edge extends upwards toward the middle of the nanowire segment and BCB layer. During this process, the electric field at nanowire-passivation heterointerfaces builds up, resulting in larger drift velocity of dark carriers towards the sidewalls. Note that the high field region (where the electric field is greater than 4×10^4 V/cm) in the nanowire segment is relatively small, meaning that avalanching is unlikely to occur.

4.2.4 Optical characterizations

PL of as-grown InAs nanowires with InP passivation layers is carried out by a solid-state red laser at 671 nm and a liquid-nitrogen cooled InSb detector in a Thermo Scientific Nicolet 6700 FTIR spectrometer. Spectral response of the wire-bonded detector array is measured using an infrared source in the FTIR spectrometer, an attached Thermo Scientific Nicolet Continuum microscope (equipped with a liquid-nitrogen cooled MCT-A detector and a Nexus detector interface box), and a Stanford SR570 preamplifier.

Fig. 4-5(a) shows room-temperature PL emission of the InAs nanowire photodiode array (before device fabrication) and simulated optical absorption of the fabricated device. PL emission is clearly observed, which suggests that a significant reduction of surface state density of InAs

nanowires was achieved by introducing large bandgap phosphorus-based *in-situ* passivation layers.[85] Detailed studies of In(As)P passivation on InAs nanowires have been previously reported, showing significant enhancement of PL emission at different temperatures.[67,108-110] In addition, we also observe in a previous study that the PL emission from InAs(Sb) inserts in InAsP nanowires was drastically enhanced when *in-situ* InAsP passivation layers were implemented.[111] It is well known that by introducing phosphorus into InAs, the surface state density can be largely suppressed (a strong room-temperature PL emission from arsenic-rich InAsP nanowires is shown in this study). Note that the measured optical emission peak at 2.8 μm indicates a calculated bandgap of 0.442 eV, which differs from the theoretical ZB InAs bandgap of 0.364 eV (all values are at 300 K). This is primarily due to a high density of rotational twins, i.e., crystal phase switches between ZB and wurtzite (WZ), which is more commonly observed in InAs nanowires grown by selective-area vapor-solid (VS) growth technique.[39,111] Such high density is not as common in nanowires grown by gold-catalyst vapor-liquid-solid (VLS) growth mode without intentional switching of growth conditions for InAs(ZB)-InAs(WZ) heterostructures.[112-114] As for the simulated optical absorption, the fundamental mode of surface plasmon (SP_{01}) is excited at 1.5 μm. Since the nanowire pattern (pitch of 400 nm) and nanowire diameter (diameter of 100 nm) were not optimized for resonant surface plasmon enhanced absorption in SWIR, the absorption becomes lower than 2 % beyond 2.0 μm due to the diffraction limit.[101] In other words, the cutoff of the photoresponse is expected to be limited by the diffraction limit, rather than the bandgap of InAs nanowires near 2.5 μm. In future works, a larger nanowire pitch could be applied to excite surface plasmon resonance over 2.0 μm for a higher optical absorption and quantum efficiency.

Fig. 4-5(b) shows shows the calibrated responsivity of the InAs nanowire photodiode array at 300 K (at a reverse bias of 0.5 V), with photodetection achieved at wavelengths up to 2.5 μm.

The inset depicts the calculated external quantum efficiency (EQE). To the best of our knowledge, this is the first reported room-temperature responsivity over 2 μm for InAs nanowire photodetectors. Note that the calibrated responsivity and EQE are relatively low compared to the planar InAs *p*-*i*-*n* diodes. In addition, the spectral response at 0 V is too weak to be resolved. The low responsivity, or EQE, is due to the exclusive generation of photogenerated carriers within the top segments of the nanowires near the plasmonic gratings. This first leads to a loss of these carriers through nonradiative recombination at the nanowire-passivation (InAs-InP) heterointerfaces due to a high density of surface trap states. Secondly, since the entire nanowires are unintentionally *n*-doped and no junctions are formed at nanowire tips, there is no electric field to properly drift the photogenerated carriers to the 3-D contacts. This currently limits the operation of our nanowire photodiode in photovoltaic mode. Therefore, introducing a highly doped *n*-type region at the nanowire tips can potentially enhance the responsivity of our structure in PV mode.

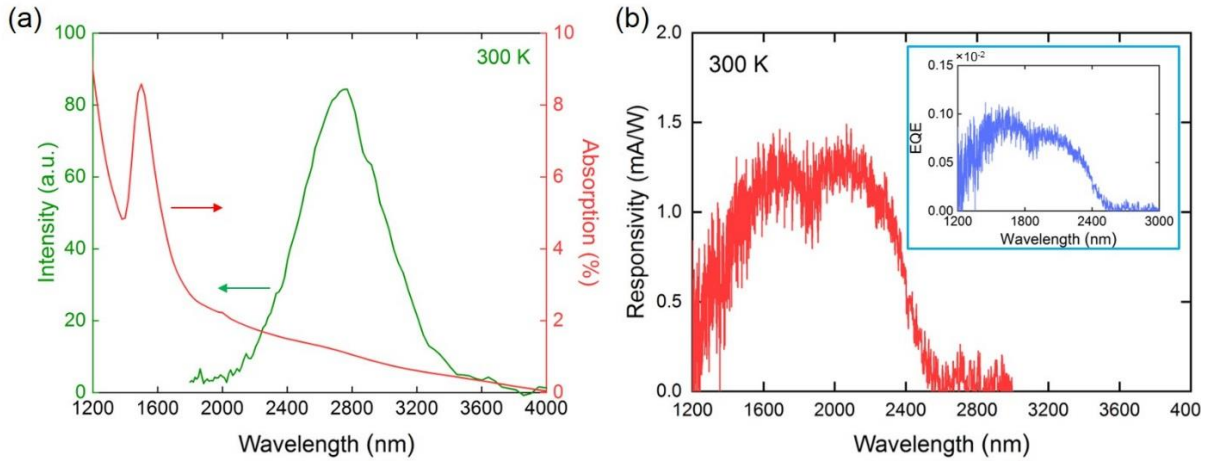

Figure 4-5 Optical characterizations of *n*-InAs/*p*-InP photodiode at 300 K. (a) PL of as-grown InAs-nanowires with InP passivation layers (left *x*-axis) and simulated optical absorption (right *y*-axis). (b) Spectral response of the InAs photodetector at reverse bias of 0.5 V, indicating photodetection signature at SWIR up to 2.5 μm. The inset shows the calculated EQE in fractions.

The calculated detectivity (D^*) at a reverse bias of 0.5 V is shown in Fig. 4-6, which is calculated based on the responsivity spectrum shown in in Fig. 4-5(b) and the following well-known equation (assuming that the nanowire photodiode works in a quantum-limited regime)

$$D^* \approx \frac{R}{\sqrt{2qJ_{Dark\_Eff}}} \tag{4.6}$$

where R is the responsivity, $J_{\text{Dark\_Eff}}$ is the dark current density, and q is the electron charge. Note that the interpretation of $J_{\text{Dark\_Eff}}$ here differs from that of the aforementioned dark current density $J_{\text{Dark\_J}}$. Here, $J_{\text{Dark\_Eff}} = I_{\text{Dark}}/A_{\text{Eff}}$, where A_{Eff} represents the area of the nanowire array (100 μm × 100 μm). The peak detectivity at SWIR is close to 2.5×10^7 cm·Hz$^{1/2}$/W, which is two orders lower than that of commercial InAs *p-i-n* photodiodes (photovoltaic ~ 0 V). This lower level of detectivity is mainly due to a lower quantum efficiency (i.e. optical absorption and internal quantum efficiency) and can be further increased by improving passivation quality and tuning the geometrical structure of the nanowire device to enhance absorption via surface plasmon resonance.[101,115]

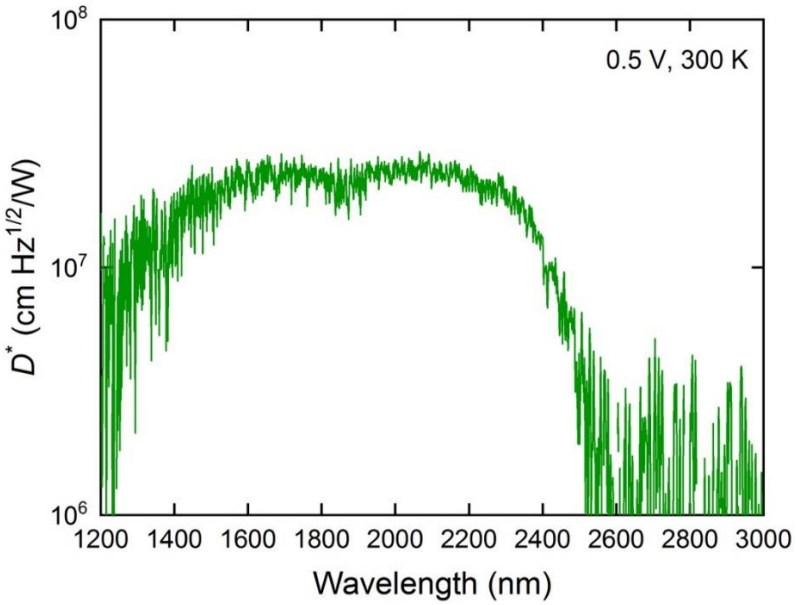

Figure 4-6 Detectivity (D^*) spectrum of n-InAs/p-InP photodiode at 300 K (at reverse bias of 0.5 V).

4.2.5 Toward high-detectivity InAs-InP heterojunction photodiodes

The purpose of this work is to show that the nanowire platform with nanoscale photoabsorbers and InAs-InP heterojunctions can provide certain performance improvements for D^*. There exists a fundamental limit to achieve higher D^* due to the trade-off between high responsivity and low dark current in planar devices, as shown in Eq. 6. To improve D^*, it is common to lower $J_{Dark\_Eff}^{1/2}$ by reducing photoabsorption volume. However, this leads to a lower R, which in turn results in a lower D^*. Thus, one solution is to ensure that the reduction in $J_{Dark\_Eff}^{1/2}$ is greater than the reduction in R, an idea which can potentially be achieved by using the nanowire platform. This is because the reduction in $J_{Dark\_Eff}^{1/2}$ of the presented device platform is accomplished through a reduction of the fill factor to reduce the generation-recombination as well as through a usage of InAs-InP heterojunctions to significantly reduce the number of minority carriers. To prove this concept, we studied the dark current of InAs-InP heterojunction nanowire photodetector. We show a nearly identical dark current density (normalized to the nanowire cross-sections) with a fill-factor of about 4%, suggesting a 5-fold decrease of $J_{Dark\_Eff}^{1/2}$. Despite the decrease in dark current, there are several critical challenges that must be addressed to achieve a higher D^* in nanowire photodetector. First, it is necessary to develop a better surface passivation because of the high trap density currently observed at InAs-InP (nanowire-passivation) interfaces. Based on the simulations shown in Figure 4b, it is possible to reduce J_{Dark_Eff} by one order, i.e., a 3-fold decrease of $J_{Dark\_Eff}^{1/2}$. Thus, an over 15-fold decrease of $J_{Dark\_Eff}^{1/2}$ is expected. Second, the nanowire pattern and the plasmonic grating can be optimized to maximize the optical absorption at SWIR. Fortunately, it is a simple matter to address, as the absorption can be tuned by varying the nanowire pitch and nanowire diameter and increased to larger than 10% at 1064 nm.[101,115] Third, the internal quantum efficiency can be improved by introducing a highly doped layer atop

the InAs nanowire segment, creating an intrinsic electric field that would sweep the carriers to the contact. In this case, it is possible to resolve the spectral response in PV mode. As a result, although the absorption of planar InAs *p*-*i*-*n* photodiodes is close to 70%, which is roughly 7 times higher than the absorption of the proposed nanowire-based InAs photodetectors, the nanowire-based InAs photodetectors can still potentially achieve 15-fold reduction in $J_{\text{Dark\_Eff}}^{1/2}$, effectively breaking the trade-off between high R and low $J_{\text{Dark\_Eff}}$.

4.2.6 Summary

We developed InAs nanowire photodiodes on InP substrates for photodetection at SWIR. The photodiodes were comprised of nanostructured photoabsorbers and *n*-InAs/*p*-InP (nanowire-substrate) *p*-*n* heterojunctions. I-V characteristics showed a rectification ratio of over two orders at room temperature, suggesting a desirable diode performance. The dark current density at a reverse bias of 0.5 V, normalized to the junction area, was comparable to that of the best commercial or research InAs *p*-*i*-*n* photodiodes. This is because the dark current of *n*-InAs/*p*-InP photodiodes was drastically suppressed by decreased photoabsorber volume, which reduced minority carrier diffusion from *p*-type materials, and passivation with *in-situ* InP shells. In addition, the electrical simulations showed that the bias dependent performance was strongly influenced by the surface leakage on nanowire sidewalls. Finally, the spectral response at room temperature was measured, showing a clear photodetection signature at SWIR. We also discussed the feasibility of achieving high D^* by using the nanowire InAs-InP heterojunction platform to break the trade-off between high responsivity and low dark current. Further work can be carried out to improve nanowire surface quality and optimize optical design for higher detectivity at room temperature. This work paves the way to integrate nanostructured photoabsorbers at SWIR on

large bandgap substrates to achieve comparable detection performance metrics as their planar counterparts.

4.3 InAsSb nanowire photodetectors

4.3.1 Introduction

Previously in the Section 2.4, we have demonstrated, through simulation, the promise of InAsSb nanowire-based photodetectors to achieve one to two orders higher detectivity at room temperature than planar InAs and HgCdTe *p*-*i*-*n* photodiodes in photovoltaic mode. In this section, we will show some initial studies to approach room-temperature photodetection at MWIR. It is critical to use InAsSb nanowires as photobabsorbers instead of InAs nanowires, because the cut-off bandgap wavelength of InAs nanowires grown by catalyst-free selective-area growth technique is less than 3 μm due to intermixing of ZB and WZ crystal phases. By introducing antimony, the cut-off wavelength can extend further into the MWIR regime.

To date, a few studies on InAsSb nanowires as photodetectors have been reported. Examples of some pioneering works include (1) *n*-InAsSb nanowires on *p*-InAs giving photoresponse up to 3.5 μm (227 K);[101] (2) InAsSb *p*-*i*-*n* nanowires on *p*-Si showing a photodetection signature up to ~3 μm (300 K);[102] (3) unintentionally doped InAsSb nanowires on *n*-InAs offering spectral response between 3 – 5 μm (5 K).[116] However, no uncooled nanowire detector has been reported to show clear photodetection signatures over 3 μm. Additionally, more studies have shown growth of high-quality InAsSb nanowires with different antimony compositions. However, improving their optical properties remains a challenge, as there has been no reported room-temperature PL emission from those nanowires at MWIR. This is mainly

because of the significant non-radiative recombination at InAsSb nanowire surfaces – it is well known that the surface state density of the arsenic-rich InAsSb is high. Since the performance of nanowire-based devices is predominantly affected by the surface quality due to their large surface-to-volume ratios, it is critical to develop a high-quality surface passivation to improve IQE of InAsSb nanowire photodetectors for room-temperature photodetection at MWIR.

In this work, we demonstrate uncooled InAsSb photodetector arrays on InP substrates for photodetection at MWIR, grown by SA-MOCVD. We first develop the surface passivation for InAsSb nanowires using conformal Al_2O_3 layers by atomic-layer deposition (ALD). The *in-situ* InP passivation layer is not suitable for InAsSb nanowires because of the lattice mismatch between InAs(Sb) and InP and the noticeable surface recombination at InAs-InP (nanowire-shell) heterointerfaces shown in the Section 4.2.3. Note that the nanowires are grown on the patterns that are optimized for photodetection at MWIR. A 10- to 50-fold increase in the intensity of PL emission from InAsSb nanowire arrays is observed at 77 K by introducing $(NH_4)_2S/Al_2O_3$ passivation. An extremely low surface recombination velocity in the order of 10^3 cm/s is estimated by 3-D transient simulations of the PL process. Furthermore, room-temperature emission from InAsSb nanowire arrays is achieved, spanning the entire MWIR regime from 3 μm to 5 μm. Second, we design the dry etching process for passivated InAsSb nanowires to expose only the top nanowire facets for metal contacts with sidewalls fully covered by Al_2O_3 shells. No degradation of nanowire surface quality is observed after dry etching, indicating its compatibility with standard nanowire fabrication process. We finally show the characterizations of fabricated InAsSb photodetector arrays, including reflectance of plasmonic gratings and room-temperature spectral response with MWIR detection signatures at 3.4 μm. Our work paves the way toward realizing

uncooled focal plane arrays at MWIR on low-cost substrates for highly compact and fully integrated detection platforms.

4.3.2 Optimization of optical design

The physics of self-assembled plasmonic grating is described elsewhere. Different from photodetection at near-infrared, SPP-BW modes at MWIR requires a much larger pitch (*P*) of nanowires, which can be intuitively explained by the equation below

$$\lambda_{ij} = \frac{P}{\sqrt{i^2 + j^2}} Re\left\{\left[\frac{\varepsilon_m \varepsilon_d}{\varepsilon_m + \varepsilon_d}\right]^{1/2}\right\} \tag{4.6}$$

where λ is the resonance wavelength of SPP-BW; p is the pitch of nanowires, or nanoholes; integers, *i* and *j*, correspond to the order of the plasmonic grating wavevector (which defined the surface plasmon mode); ε_m is the dielectric constant of the metal, ε_d is the dielectric constant of the dielectric, or the effective medium underneath the gratings. We investigate the optical absorption of $InAs_{0.93}Sb_{0.07}$ nanowire arrays for three different pitches – 1300 nm, 1600 nm, and 1900 nm.

Fig. 4-7 shows the simulated optical absorption under *x*-polarized incident light spanning 2.0 – 4.0 μm. Clearly, two 'modes' are observed – the first one is located within 2.0 – 2.8 μm, while the second one is beyond 2.8 μm. The first mode can be attribute to the localized surface plasmon (LSP) resonance mode and coincides with waveguide mode resonances (ref. Aziz), and the second mode presents the SPP-BW SP_{01}, far beyond the diffraction limit. From the optical design, we select 1300 nm as the pitch of nanowire, because the plasmonic modes overlap with MWIR between 3 – 4 μm and show promising optical absorption. More importantly, it is easier to realize the growth of InAsSb nanowires with smaller nanowire pitches, due to better incorporation of antimony into nanowires. This is because the vapor pressure of antimony precursor (TDMASb)

is low and it can easily lead to condensation of antimony on the growth mask or on nanowire sidewalls if the nanoholes are far apart from each other (discussed later).

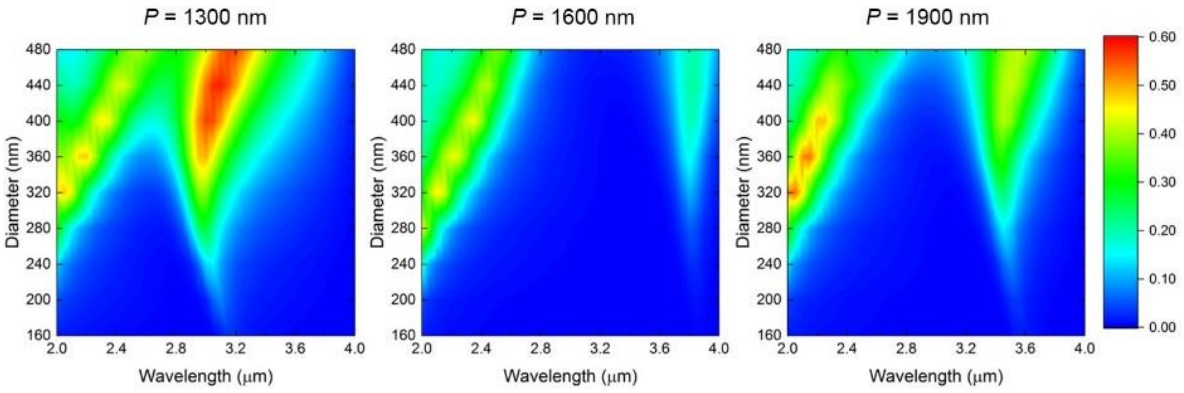

Figure 4-7 Simulated optical absorption under *x*-polarized incident light for nanowire arrays with three different pitches – 1300 nm, 1600 nm, and 1900 nm.

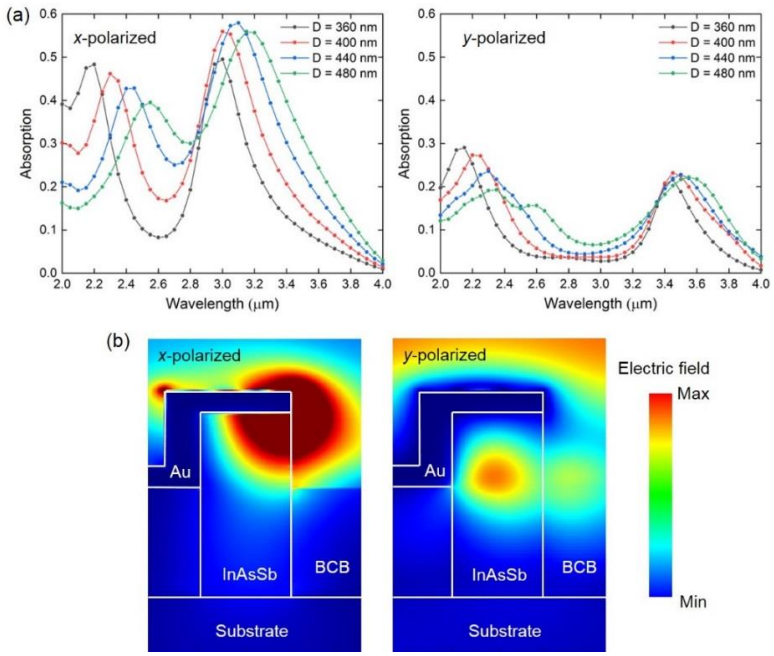

Figure 4-8 Simulated optical absorption under both *x*- and *y*-polarized incident light with fixed nanowire pitch at 1300 nm. The nanowire diameters are 360 nm, 400 nm, 440 nm, and 480 nm. (b) Cross-sectional electric field profiles of *x*- and *y*- polarization.

Fig. 4-8(a) shows the simulated optical absorption with varied nanowire diameters under both *x*- and *y*-polarized incident light. *P* is kept fixed at 1300 nm, and four values of nanowire

diameter are used – 360 nm, 400 nm, 440 nm, and 480 nm. Under *y*-polarized excitation, the plasmonic peak at MWIR shows a strong correlation with the nanowire diameter. Fig. 4-8(b) illustrates the cross-sectional electric field (E-field) profiles for both *x*- and *y*-polarized incident light. For *x*-polarization, the E-Field profile maxima is closer to tip and exposed nanowire edges, while for *y*-polarization, the E-Field profile maxima is located within the center of nanowire.

4.3.3 Nanowire epitaxy

The InAsSb nanowires are grown by SA-MOCVD on InP (111)B substrates. The diameter and pitch of nanoholes are designed as 40 nm and 1300 nm, respectively. The size of nanowire array is 200 μm × 200 μm, containing approximately a total number of 23716 nanowires. The precursors are trimethylindium (TMIn), tertiarybutylarsine (TBAs), and trisdimethylaminoantimony (TDMASb). We use a similar growth technique, the pulsed-arsenic, for InAsSb nanowires as discussed in the Section 4.3.3. A thin InAs seeding layer (V/III ratio of 32) is first introduced, followed by the growth of InAsSb nanowires (V/III ratio of 2). No *ex-situ* passivation is applied – all samples will be used to develop *in-situ* passivation.

Compared to the previous growth shown in the Section 4.3.3 (P = 400 nm), the growth on nanohole pattern with larger nanowire pitch (P = 1300 nm) is significantly difficult. The low vapor pressure of antimony at growth temperatures (500 – 530°C) can easily lead to condensation of antimony on the nanowire sidewall or on the substrate if the thermodynamics are not carefully controlled. It has been found that a V/III ratio of 2 is desired to achieve high vertical yield and effective antimony incorporation. A lower V/III ratio leads to a lower vertical growth rate, while a higher V/III ratio results in less antimony incorporation and excess antimony adatoms. Thus, there is a clear restriction on the usable range of V/III ratios for the growth of InAsSb nanowires. Furthermore, as the nanowire pitch is increased from 400 nm to 1300 nm, each nanohole shares

about 10 times more antimony adatoms that diffuse from the substrate ($n \approx 1300^2/400^2$). This gives a one-order increase of effective flow ($[\text{TDMASb}]_{\text{eff}}$) and partial pressure ($[p_{\text{Sb}}]$). Since it is critical to keep a low $[p_{\text{Sb}}]$ to avoid condensation, the only approach is to maintain a low flow rate. However, we are limited by the minimum TDMASb and TBAs molar flow rates (labelled as $[\text{TDMASb}]_{\text{m}}$ and $[\text{TBAs}]_{\text{m}}$) given by our mass flow controllers (MFCs) in the MOCVD system.

Several attempts have been made to grow InAsSb nanowires on nanoholes with large pitch 1300 nm at different temperatures (500 – 530°C), as shown in Fig. 4-9. The growth giving non-hexagonal nanowires results from excessive $[\text{TDMASb}]_{\text{m}}$. We note that $[\text{TDMASb}]_{\text{m}}$ cannot exceed 1.4×10^2 sccm (the dashed line shown in Fig. 4-9), regardless of the amount of $[\text{TDMASb}]_{\text{eff}}$ tuned by the duty cycle in the pulsed-arsenic technique; below that, the growth of irregular nanowires occurs. Thus, the maximum vapor phase of [TDMASb] available is 0.64.

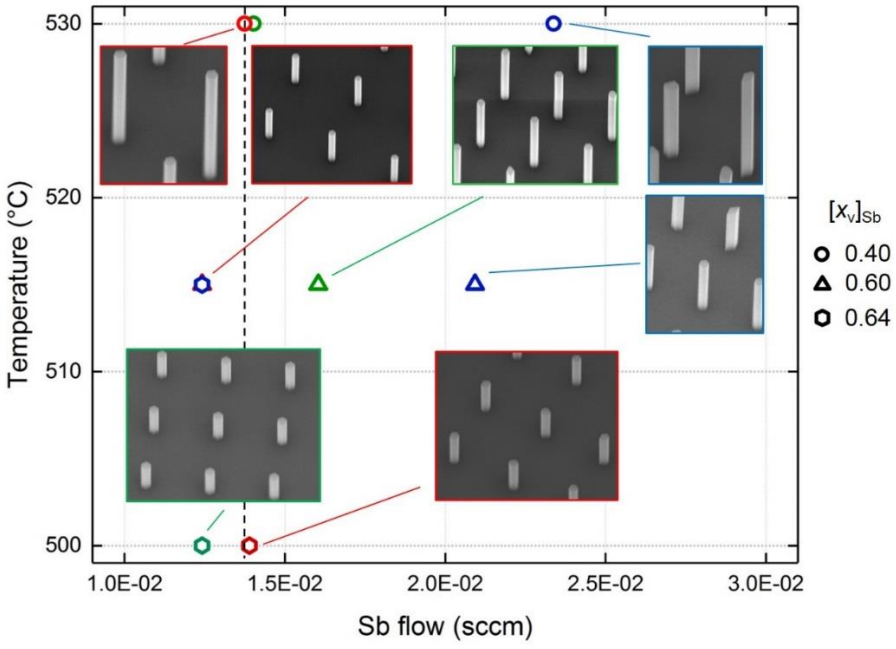

Figure 4-9 Growth of InAsSb nanowires on patterned nanoholes with P = 1300 nm. X-axis shows the actual gas flow of TDMASb, and Y-axis presents the growth temperature. The dashed line indicates the maximum TDMASb flow without introducing irregular nanowire growth.

4.3.4 Surface passivation – Al_2O_3

In order to achieve uncool nanowire detectors at MWIR, it is critical to develop a robust and controllable passivation technique. To date, there has been no report to show room-temperature optical signatures spanning the entire MWIR spectrum (3 – 5 μm) due to unsatisfied performance of surface passivation. Here, we develop an *ex-situ* passivation technique based on Al_2O_3 thin films by ALD. The *ex-situ* passivation is more desirable for InAsSb nanowire material system. First, the only lattice matched materials to arsenic-rich InAsSb are based on GaSb and AlSb; however, none of them offers sufficient valance band offset for hole carriers. Second, In(As)P shells can be used as passivation layers; however, the large lattice mismatch leads to increased surface leakage current and also the surface strain bends the nanowires. Conversely, the *ex-situ* passivation technique is more reliable because the thickness of passivation layer can be freely controlled by the deposition time in ALD. In addition, the etching selectivity of oxides to III-V compound semiconductors is high, and thus oxide on the nanowire tips can be selectively removed for metal contacts while nanowire sidewalls are left fully covered (shown later in the device fabrication).

The *ex-situ* passivation process is carefully designed. The samples with as-grown InAsSb nanowire arrays were taken out from the purge box and then submerged in a $(NH_4)_2S$ solution for 5 minutes, i.e., sulfuration. The dilution ratio was $(NH_4)_2S:H_2O$ = 1:10. Finally, the samples were blow-dried by nitrogen (no rinsing with deionized water) and quickly transferred into the ALD system. A 60 nm thick thermal Al_2O_3 layer was deposited at 200°C. The deposition rate was calibrated as 1.1 Å/cycle. The precursors were trimethylaluminum (TMAl) and vapored water (H_2O). Scanning electron microscopy (SEM) images of InAsSb nanowires before and after Al_2O_3 coating are shown in Fig. 4-10. It is clearly observed that the nanowires are conformally coated by the Al_2O_3 layers, indicating that the deposition process is controllable.

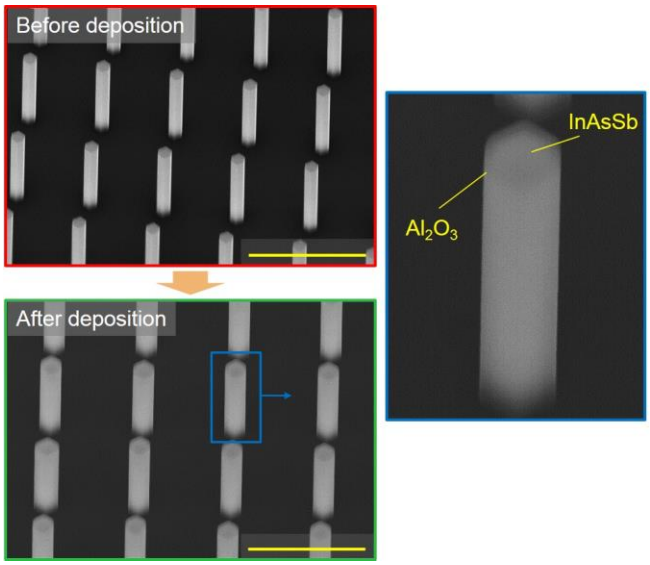

Figure 4-10 SEM images of InAsSb nanowires before and after a 60 nm Al_2O_3 deposition. The scale bar is 2 μm. The image on the right side shows a close-up look of a single nanowire conformally coated by an Al_2O_3 layer.

Then, we performed PL characterization to examine the quality of surface passivation by comparing the intensities of PL emission from nanowire arrays with and without Al_2O_3 layers. No room-temperature PL emission from unpassivated InAsSb nanowires was observed. The measurement was carried out by a solid-state red laser at 671 nm and a liquid-nitrogen cooled InSb detector in a Thermo Scientific Nicolet 6700 Fourier-transform infrared (FTIR) spectrometer. For the PL measurement, we intentionally tested three nanowire arrays (Samples A to C) with different nanowire dimensions, i.e., diameter (D_{NW}) and height (H_{NW}), which give different surface-to-volume ratios. Since the carrier motion in 3-D nanowire structures is complicated and closely correlated to their geometries, it is interesting to investigate the dependency of PL emission on nanowire dimensions and understand the comprehensive 3-D carrier dynamics. Fig. 4-11 shows the SEM images of those three nanowire samples (without Al_2O_3 passivation) and the PL emission before and after the passivation process was performed. It is clearly evident that the PL intensity in passivated nanowires are drastically enhanced by a factor of 10 to 50 times compared to non-

passivated nanowires, which demonstrates a high quality of surface passivation. Furthermore, it is noted that the Al_2O_3 shells introduce compressive strains on the bulk InAsSb nanowires, causing a blue-shift of PL emission peaks, which cannot be avoided in the passivation process. Interestingly, the enhancement of PL intensity is inversely correlated to the nanowire diameter. Sample B has the nanowire in the smallest diameter (151 nm) shows the most significant increase of PL emission with 52-fold, while Sample C gives a 17-fold increase. This is because the non-radiative recombination of the photogenerated carriers on surfaces is more significant in nanowires with smaller diameter, since the probability of those carriers diffusing to the surfaces is higher.

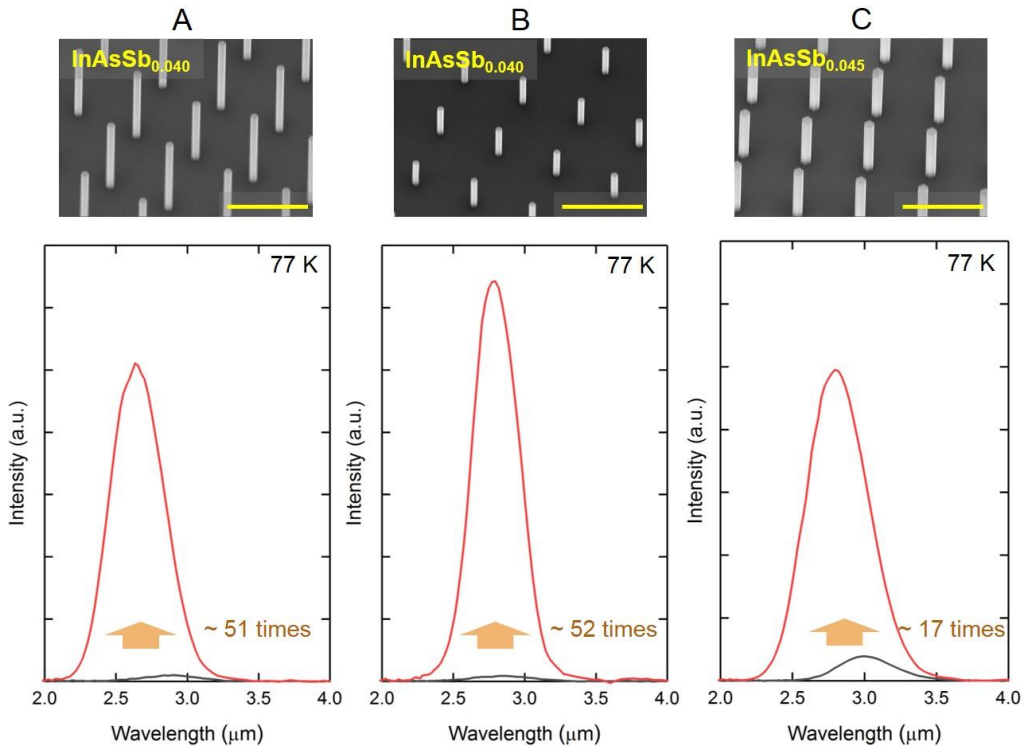

Figure 4-11 Samples A – C to examine passivation quality of thin-film Al_2O_3. SEM images show the InAsSb nanowire dimensions before Al_2O_3 deposition: (1) Sample A – D_{NW} =173 nm, H_{NW} = 4728 nm; (2) Sample B – D_{NW} =151 nm, H_{NW} = 2120 nm; (3) Sample C – D_{NW} =220 nm, H_{NW} = 2152 nm; The scale bar is 2 μm. The bottom PL-plots show a comparison of the low-temperature (77 K) PL emission of InAsSb nanowires with and without passivation layers. The enhancement ratios are labelled.

One interesting study is to correlate the increase of PL emission to the improvement of surface recombination velocity (in units of cm/s), which is a critical parameter to quantify the surface quality. Typically, the surface recombination velocity of nanowires is extracted by time-resolved photoluminescence (TRPL), as shown in many pioneering studies. However, we believe that the rich information underlying PL measurement can be still harnessed to unveil the surface dynamics. The basic idea is as follows. We assumed the surface recombination velocity of non-passivated nanowires as v_S ($1\times10^1 - 1\times10^6$ cm/s) and that of passivated nanowires as v_S' ($1\times10^1 - 1\times10^6$ cm/s). We applied a 3-D computational transient model to compute the radiative recombination over nanowire segment at steady-state with constant light injection. The enhancement of "PL" of nanowires with passivation layers, can be calculated as

$$R = I_2/I_1 \tag{4.7}$$

where R is the ratio or the factor of enhancement; I_1 and I_2 is the simulated radiative recombination rates, or "PL intensities" of nanowires with and without passivation layers, respectively. Unlike previous transient models, we used a step function instead of a Gaussian function to represent the incoming continuous-wave (CW) laser. The radiative recombination coefficient of InAsSb at 77 K was set as 1.2×10^{-9} $cm^3\cdot s^{-1}$.

Fig. 4-12 shows the resultant simulations of the enhancement ratio R and its correlation with v_S and v_S'. The schematics of simulation structures are shown in the upper-left corner of Fig. 4-12. Each point on the contour plot represents a certain combination of v_S and v_S', i.e., the quality of non-passivated and passivated surface. The contour line is a set of points which gives the same R. We can interpret the contour plots by observing Sample B as an example. All points, i.e., combinations of (v_S, v_S'), on the contour lines can give the same PL enhancement of 52. If v_S is between $8\times10^4 - 1\times10^5$ cm/s, the corresponding v_S' is between $1\times10^1 - 1\times10^3$ cm/s, meaning that

the surface recombination velocity is suppressed by 100 – 8000 times with Al_2O_3 passivation. Similarly, if v_S is between 8×10^5 – 1×10^6 cm/s, a possible range of v_S' is between 2×10^4 – 3×10^4 cm/s, suggesting a decrease of surface recombination velocity by a factor of 30 – 40 with Al_2O_3 passivation. Although the exact value of v_S is unknown, we can certainly suggest that it is between 8×10^4 – 1×10^6 cm/s. A surface recombination of $(5.0\pm0.2)\times10^4$ cm/s is previously reported for unpassivated InAs in InAs/GaSb type-II superlattices, and then v_S of unpassivated InAs(Sb) nanowire can estimated to be within the order of 10^4 cm/s. Thus, we conclude that for Sample B, v_S is between 8×10^4 – 1×10^5 cm/s and v_S' is between 1×10^1 – 1×10^3 cm/s.

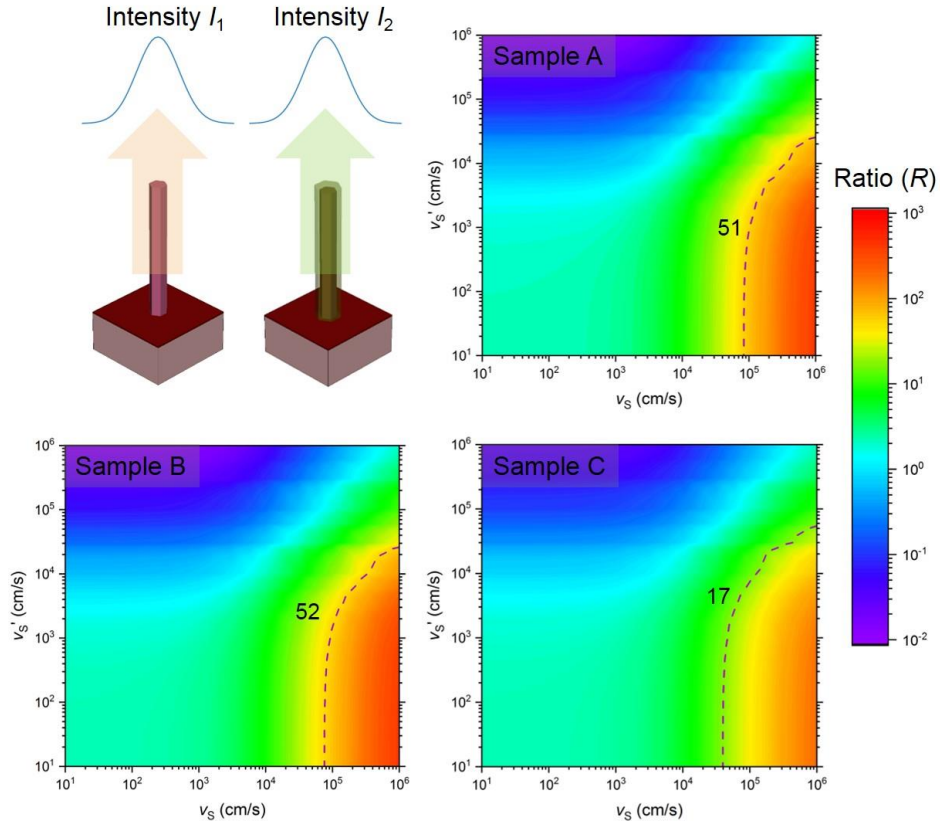

Figure 4-12 Schematics diagram at the upper-left corner shows the structures of unpassivated and passivated nanowires used in the transient simulations. Three contour plots show the simulated PL enhancement ratios corresponding to different combinations of (v_S, v_S'). The measured ratios R are labelled along with the contour lines.

Now, if we look at the other two Samples A and C. The enhancement ratio R of Sample A is 51, similar to that of Sample B, as shown in the bottom-left corner of Fig. 4-12. Their two contour lines almost overlap with each other, and thus the actual values of v_S and v_S' of Samples A and B are the same. As for Sample C, the ratio R is 17, much lower than those of Samples A and B. Even so, we note that the intersections of the contour line with the x-axis and y-axis for Sample B is 4×10^4 cm/s and 5×10^4 cm/s, respectively, within the same orders for the other two cases. The smaller R results from a smaller surface-to-volume ratio of Sample C due to its larger diameter. Consequently, the effect of surface recombination on the photogenerated carriers is not as sensitive as that for Samples A and B. In other words, a smaller R does not necessarily mean that the surface quality is low. This is a unique property for nanowires – their 3-D geometries must be taken into account and can only be deconvolved using a 3-D computatiaonal model. It might be fair to assume that the surface quality of passivated nanowires of Samples A – C is the same. If so, v_S of Sample C is about 4×10^4 – 5×10^4 cm/s, which is slightly lower than that of Samples A and B. Note that $[x]_{Sb}$ of Sample C is 0.045, slightly higher than that of Samples A and B. Thus, there might be a dependency of surface recombination velocity of unpassivated InAsSb nanowire surface on $[x]_{Sb}$.

To examine the optical property at room temperature for InAsSb nanowires, we applied the same $(NH_4)_2S/Al_2O_3$ passivation technique to InAsSb nanowires with different $[x]_{Sb}$ ranging from 0.02 to 0.18. Some of the nanowire samples were previously grown with nanowire pitch of 400 nm ($[x]_{Sb} > 0.07$). The thickness of Al_2O_3 shell was kept fixed at 60 nm. Room-temperature PL emission from InAsSb nanowires is shown in Fig. 4-13, spanning the entire MWIR regime, which indicates high-quality of surface passivation. This shows promise to achieve room-temperature photodetection at MWIR. The dips in the PL spectra of InAsSb nanowires with higher $[x]_{Sb}$ result from CO_2 absorption, and the cutoff of spectra at 5 μm comes from the InSb detector.

Note that since the PL emission peaks of passivated InAsSb nanowires show blue-shifts, they cannot be directly use to estimate $[x]_{Sb}$.

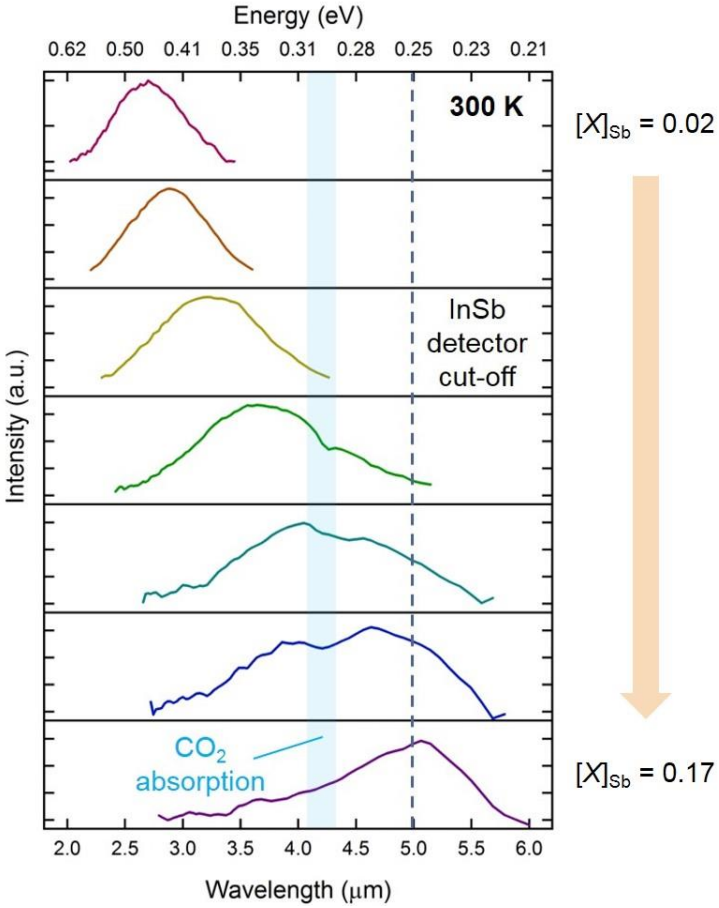

Figure 4-13 Room-temperature PL characterization of InAsSb nanowires passivated by $(NH_4)_2S/Al_2O_3$. The antimony composition $[x]_{Sb}$ ranges from 0.02 to 0.17.

After demonstrating the passivation technique, we developed the fabrication process of Al_2O_3 compatible to our standard nanowire device fabrication. The goal was to only expose the top facets of nanowires while keeping their sidewalls coated by selectively removing Al_2O_3 shells. This is because photogenerated carriers of nanowire photodetectors with self-aligned plasmonic gratings are tightly confined in the top nanowire segments, and well-passivated surfaces can reduce nonradiative recombination and enhance responsivity. Different from III-V semiconductor shells formed by *in-situ* passivation, e.g. In(Ga)(As)P and AlGaAs, oxide based shells show high

selectivity to core materials, i.e., nanowires, in wet etching or dry etching. Another advantage of using oxide shells is that the top small bandgap materials for optical absorption are not depleted by the 3-D contacts, i.e., plasmonic gratings, which is commonly observed in our previous nanowire photodetectors.

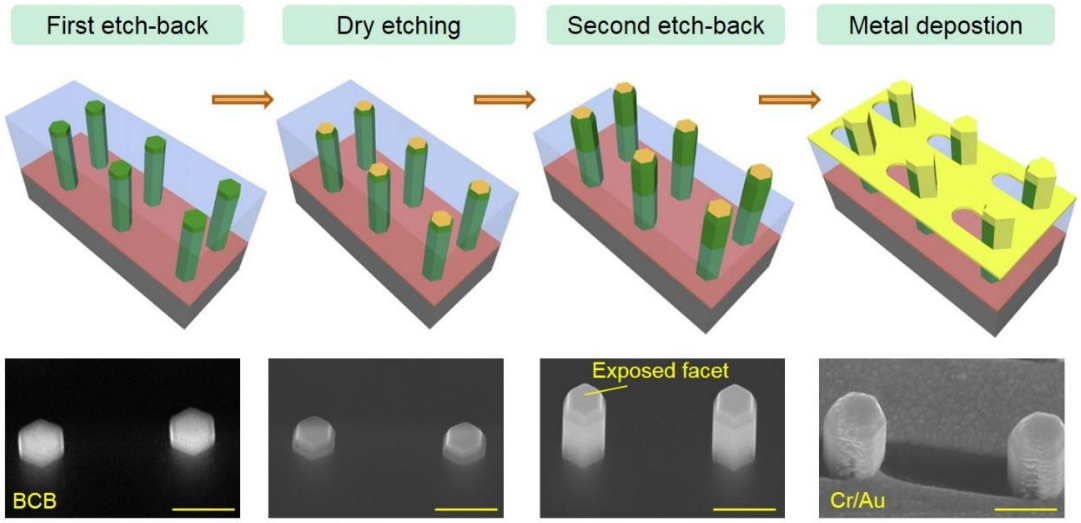

Figure 4-14 Nanowire fabrication process with Al_2O_3 passivation shells. Four major steps are shown. Dry etching process is carefully designed to expose only top nanowire facets with sidewalls entirely covered by the Al_2O_3 layer. The scale bar is 500 nm.

The schematic diagram of the fabrication process is shown in the top part of Fig. 4-14. In this study, we tested two different strategies: (1) wet etching by buffered oxide etch (BOE), and (2) dry etching by reactive ion etching (RIE) using CHF_3 and Ar plasmas. We first performed the wet etching process and realized the process is not controllable (Fig. 4-15). During the wet etching process, the BOE solution tended to penetrate between the BCB layer and Al_2O_3 layer and etched Al_2O_3 underneath the exposed portion. As a result, gaps were created around nanowire circumference and became larger during the second etch-back process. This is not desirable because those gaps will affect the quality of tilted metal deposition. Thereafter, we examined the

dry etching strategy, as shown in the lower part of Fig. 4-14. Remarkably, the entire nanowires were capped by Al_2O_3 shells where only the top facets were exposed, showing "pencil" shaped nanowire segments. The etching process was precisely controlled by using a very slow etch rate 1.0 – 1.5 nm/min, leading to a total etching time of 50 – 60 minutes. The calibrated selectivity of Al_2O_3 to BCB was between 1:4 and 1:5. No gaps along the nanowire circumference were observed before and after the shell etching or the second etch-back. To test whether or not the passivation was degraded after the entire dry etching process, we selected one InAsSb nanowire sample and fully remove the BCB layer after the shell etching. We then performed PL characterization (77 K) on one nanowire array and compare its PL emission with the one measured right after the Al_2O_3 deposition. All measurement conditions were kept fixed. No degradation of PL signal was observed; instead, the PL emission was even stronger, suggesting an enhanced light out-coupling efficiency due to the tapered nanowire tips with Al_2O_3 shells. Therefore, we conclude that the etching scheme displays excellent compatibility with our standard nanowire device fabrication process and shows the thermal stability at least up to 250°C (the temperature used for BCB curing). It is worth mentioning that no degradation of Al_2O_3 has been found after one month, suggesting a reasonable long-term stability for device processing.

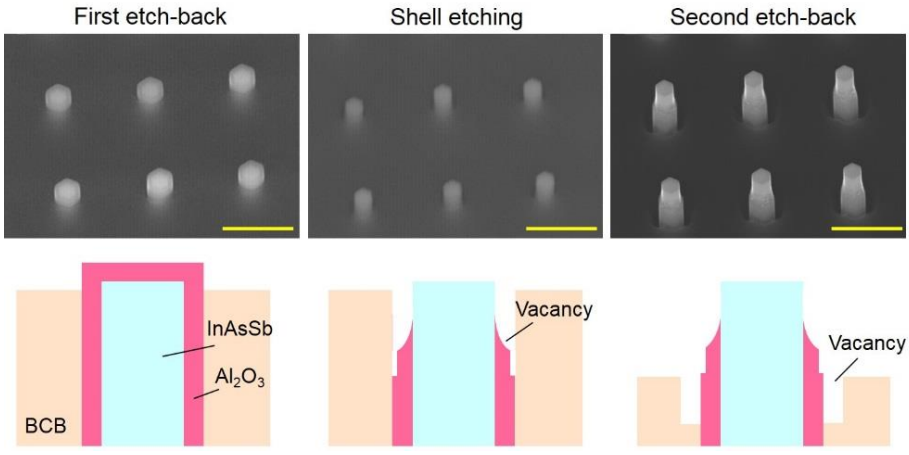

Figure 4-15 Exposing nanowire top segments by wet etching of Al_2O_3 shells. The scale bar is 1 μm.

4.3.5 Uncooled InAsSb nanowire photodetectors

The Samples E and F ($InAs_{0.955}Sb_{0.045}$) are fabricated by following the modified fabrication process for Al_2O_3-passivated InAsSb nanowires. The size of nanowire array is 200 μm × 200 μm and the nanowire pitch is 1300 nm. The nanowires dimensions are given: (1) Sample E – D_{NW} = 150 nm, H_{NW} = 2260 nm, and (2) Sample E – D_{NW} = 220 nm, H_{NW} = 1740 nm. In addition, the thickness of oxide shell is 60 nm and the exposed nanowire height after etch-back is 1000 nm. Room-temperature DC current-voltage (I-V) characteristics under dark and illumination are measured using a probe station (Signatone 1160 series), a semiconductor parameter analyzer (Agilent 4156C), and a fiber-coupled 1064nm laser (Orbits Lightwave Ethernal SlowLight). The calibrated laser spot size is about 100 μm by a planar GaSb *p-i-n* with mesas in different sizes.

Fig. 4-16 shows SEM images and device characterizations of Samples E and F. The incident power at 1064 nm is 12 mW. We immediately note that the dark current levels are high and the rectification ratios are low by compared with the I-V characteristics of InAs nanowire photodiodes shown in the Section 4.2.3. The dark current density (normalized to the nanowire cross-sectional area) at reverse bias of 0.5 V is 2.85×10^3 mA/cm^2 and 2.48×10^5 mA/cm^2 for Sample E and F, respectively, much higher than 130 mA/cm^2 given by the InAs nanowire photodiodes. Recall that the diameter of InAs nanowires is 100 nm. Seemingly, there is a strong dependency of the dark current on the nanowire diameter. Here, we list three possible sources of dark current: (1) InAsSb-Al_2O_3 interfaces; (2) InAs (seeding)-InP interfaces; and (3) InAs(Sb)-SiO_2 (mask) interfaces. Since a low surface recombination velocity of Al_2O_3-passivated InAsSb nanowires has been demonstrated in the previous Section 4.3.4, the first possibility is not likely to be the case. In addition, the size of nanoholes are kept fixed at 40 nm and a similar condition is applied to the growth of seeding layer for Samples E and F (a slight change of gas flow is made while the V/III

ratio is fixed at 32), the InAs-InP heterointerfaces should be of good quality. Thus, we suspect that the significant leakage results from the large area InAsSb-SiO_2 interface, i.e., the excessive overgrowth on the lateral direction. One potential solution is to selectively remove the SiO_2 growth mask and passivate the entire nanowire and nanohole segments by Al_2O_3 to reduce the surface effect. Note that this process requires a nanowire growth using nanoholes with larger diameter (~80 nm or higher) to avoid "peeling-off" of nanowires during nanowire sulfuration due to the hydrophobic effect.

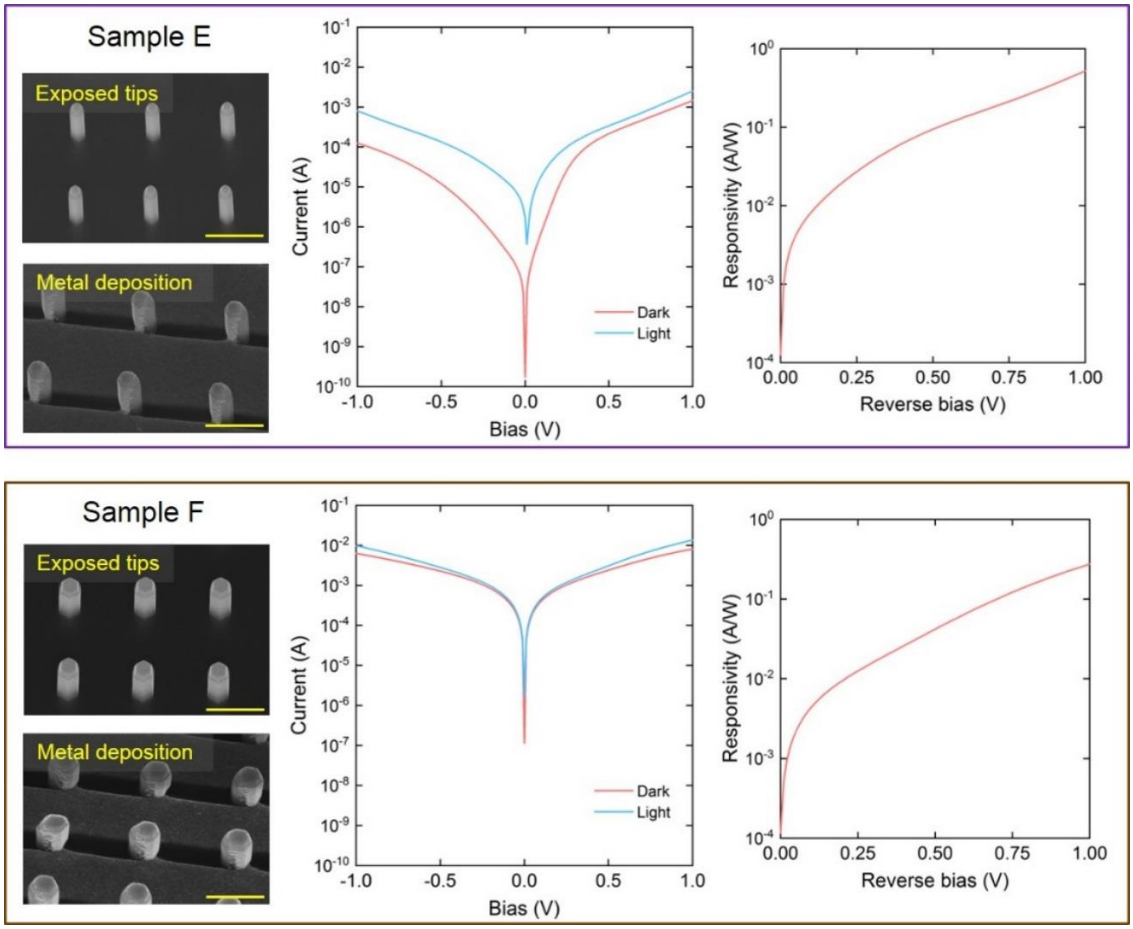

Figure 4-16 Device characterizations (under dark and illumination) at room temperature for Samples E and F. The nanowire top facets are selectively removed, as shown in the SEM images.

Instead, the optical property is more promising. The responsivities at 1064 nm at reverse bias of 0.5 V are 0.042 A/W and 0.094 A/W for Sample E and F, respectively, which are drastically

improved by a factor of 40 – 90 compared with that of InAs nanowire photodiodes (giving 0.001 A/W at the same bias). Clearly, this indicates a significant reduction of surface recombination by capping the exposed nanowire tips by the Al_2O_3 shells – photocarriers can be efficiently drifted to the contacts without recombining at nanowire-air interfaces. As discussed in the Section 4.2.4, the responsivity can be further increased by introducing a highly *n*-doped segment at the nanowire tip to locally generate electric field.

Last but not least, reflectance measurement and spectral response is performed on Sample F using Nicolet 6700 Fourier-transform infrared (FTIR) spectrometer and an attached Thermo Scientific Nicolet Continuum microscope with a liquid-nitrogen cooled MCT-A detector. Fig. 4-17 shows the normalized absorbance plus transmittance, i.e. 1 - reflectance, of Samples E and F from 1 – 5 μm under a broadband infrared source. Three peaks are observed between 1.3 – 1.5 μm, 2.0 – 2.2 μm, and 3.5 – 3.6 μm, clearly indicating the resonance peaks of SPP-BW modes. This clearly indicates the ability to obtain room-temperature photoresponse signatures at MWIR.

Fig. 4-17(a) depicts the normalized absorbance plus transmittance, i.e. 1 - reflectance, from 1.5 to 5.0 μm under a broadband infrared source. The inset shows the top view of the fabricated array. Two peaks are observed ~2.0 μm and ~3.5 μm, clearly indicating the resonance peaks of surface plasmon resonance excited by the 3-D plasmonic grating. This clearly indicates the absorption signatures at short-wavelength infrared (SWIR) and MWIR, which are achieved by using large nanowire pitch of 1300 nm and large nanowire diameter over 200 nm. Fig. 4-17(b) shows room-temperature spectral response at reverse bias of 0.5 V from 1.5 to 5.0 μm. Note that the photocurrent spectrum is not normalized. Two detection peaks are clearly observed – one at ~2.0 μm and ~3.4 μm, corresponding to the absorption signatures in Fig. 4-17(a). Thanks to the low v_S given by the Al_2O_3 passivation, a portion of photocarriers can be drifted to the 3-D contacts

without recombining at nanowire surfaces. The spectral response in photovoltaic mode, i.e., 0 V, is too noisy to resolve. Since the InAsSb nanowires are unintentionally *n*-doped and the doping level is uniform, there is no additional electric field at nanowire tips where photogenerated carriers are located and thus, IQE is low at 0 V. Additionally, the detectivity (D^*) of this device is expected to be low due to high leakage current at reverse bias. We suspect that the significant leakage results from the large area InAsSb-SiO_2 interface, i.e., the excessive overgrowth on the lateral direction. A strong dependency of the dark current on the nanowire diameter is observed. One potential solution is to selectively remove the SiO_2 growth mask after nanowire growth and passivate the entire nanowires and nanohole segments by Al_2O_3 to reduce the nonradiative recombination at InAsSb-SiO_2 interface. Note that this process requires a nanowire growth using nanoholes with larger diameter (~80 nm or higher) to avoid "peeling-off" of nanowires during nanowire sulfuration due to the hydrophobic effect.

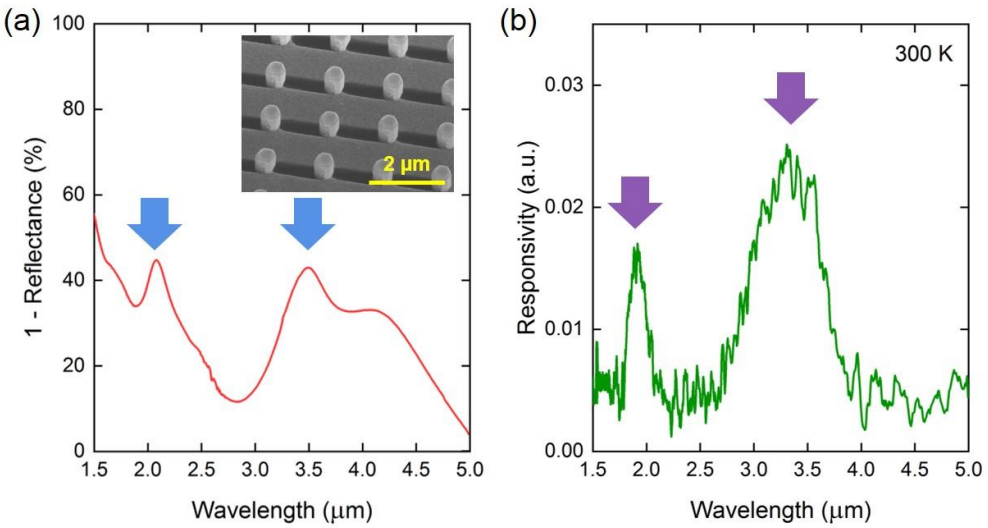

Figure 4-17 (a) Reflectance measurement. The *y*-axis is one minus reflectance, giving the sum of absorbance and transmittance. The inset shows the top view of the fabricated nanowire array. (b) Spectral response measurement at room temperature (not normalized). The arrays highlight the peaks observed in both reflectance and spectral response measurement.

4.3.6 Summary

We demonstrated InAsSb nanowire photodetectors on InP substrate to approach room-temperature photodetection at MWIR. The photodetectors were comprised of nanostructured photoabsorbers, *n*-InAsSb/*p*-InP (nanowire-substrate) *p*-*n* heterojunctions, and 3-D plasmonic gratings. We first developed an *ex-situ* passivation technique using $(NH_4)_2S/Al_2O_3$ to reduce the non-radiative recombination at InAsSb nanowire surfaces. A significant suppression of surface recombination velocity was observed and PL emission from InAsSb nanowires at room temperature was achieved, spanning the entire MWIR spectrum. Next, we developed a fabrication process based on dry etching to expose nanowire top facets with sidewalls fully covered by the Al_2O_3 shells. This process was proved to be compatible with the standard fabrication process of vertical nanowires. Last but not least, we performed device characterization on the fabricated InAsSb photodetectors and observed room-temperature photodetection at 3.4 μm. The result matched the absorption signatures obtained by the reflectance measurement. Our work provides a foundation for achieving uncooled nanowire photodetectors with high detectivity for photodetection at MWIR or even longer wavelengths.

5. Conclusions and Future Prospects

5.1 Conclusions

This dissertation has shown a comprehensive study of selective-area nanowires based on optical and electrical modeling, heteroepitaxy, and device fabrication and characterizations. First, we developed several comprehensive models to investigate: (1) the carrier dynamics of 3-D nanowires using TRPL measurements; (2) the correlation between carrier lifetime and surface recombination velocity; (3) the responsivity and detectivity of the proposed nanowire photodetectors at short and mid wavelength infrared (SWIR and MWIR); and (4) ultrafast current response in nanoscale photoabsorbers. Second, we achieved high-uniform and high vertical yield of InAs(P)(Sb) nanowire growth on InP (111)B substrate. The nanowire structures analyzed were: (1) bulk InAsP nanowires; (2) bulk InAsSb nanowires; and (3) InAs(Sb) inserts. We also electrically characterized the conduction band offset of the InAs-InAsP heterojunction. Third, we studied InAs(Sb) nanowire photodiodes on InP substrates at SWIR/MWIR. The dark current density of InAs nanowire photodiode, normalized to the junction area, was comparable to that of the best commercial or research InAs *p-i-n* photodiodes due to a significant reduction of minority carrier diffusion and generation-recombination. In addition, an *ex-situ* passivation technique using $(NH_4)_2S/Al_2O_3$ was developed, which greatly suppressed nonradiative recombination on InAsSb nanowire surface. We believe the presented theoretical and experimental work will stimulate more validating studies of nanowire optoelectronics at infrared to further reveal the inherent carrier dynamics of nanowires, develop more sophisticated optical and electrical designs, and demonstrate better device performance.

5.2 Future prospects

Beyond the studies in this dissertation, we propose a device scheme based on separate absorption and multiplication avalanche photodetector (SAM-APD) for photodetection at MWIR for future study. SAM-APDs have proven to be a robust means of increasing signal-to-noise ratio through internal gain. Realizing room-temperature SAM-APDs at MWIR on standard III-V substrates can advance the technology for high-resolution, high-speed, and low-noise focal plane arrays. However, no commercial MWIR SAM-APDs have been effective due to high saturation current, generation-recombination current, and tunneling current from small bandgap III-V materials. The ideal structure for a MWIR SAM-APDs is the integration of a small bandgap absorber onto a large bandgap multiplication region. The proposed nanowire MWIR SAM-APDs are composed of InAsSb absorbers, large bandgap InP *p-i-n* multiplication regions, and In(As)P graded layers, as shown in Fig. 5-1. *Ex-situ* Al_2O_3 shells would be perfect passivation layers for InAsSb absorbers. The absorption peaks of the surface plasmon can be freely tuned via the geometry of metal photonic crystal grating, which can be further lithographically controlled for individual pixels. We predict that the detectivity (D^*) at room temperature can reach around 1×10^9 – 1×10^{10} cm $Hz^{1/2}W^{-1}$ across the entire MWIR regime.

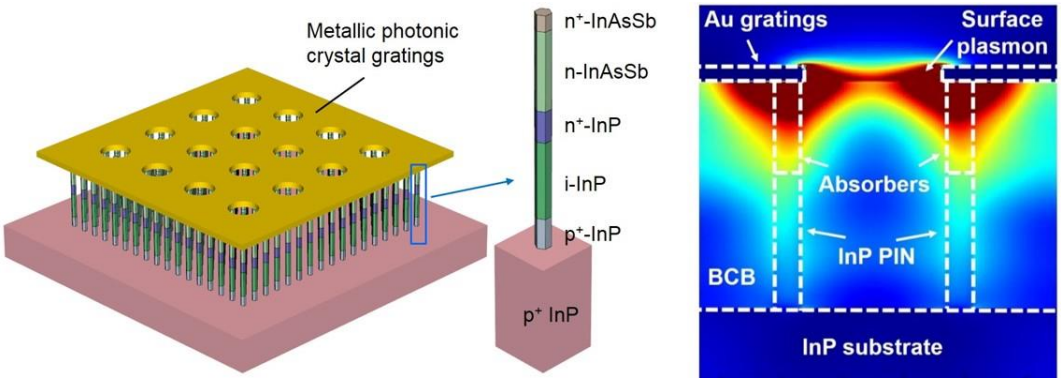

Figure 5-1 Proposed nanowire SAM-APD device scheme for photodetection at MWIR.

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