The Electronics System for the LBNL Positron Emission Mammography (PEM) Camera

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***Abstract*--We describe the electronics for a high performance Positron Emission Mammography (PEM) camera. It is based on the electronics for a human brain PET camera (the Siemens/CTI HRRT), modified to use a detector module that incorporates a photodiode (PD) array. An ASIC services the PD array, amplifying its signal and identifying the crystal of interaction. Another ASIC services the photomultiplier tube (PMT), measuring its output and providing a timing signal. field programmable gate arrays (FPGAs) and lookup RAMs are used to apply crystal by crystal correction factors and measure the energy deposit and the interaction depth (based on the PD/PMT ratio). Additional FPGAs provide event multiplexing, derandomization, coincidence detection, and real-time rebinning. Embedded PC/104 microprocessors provide communication, real-time control, and configure the system. Extensive use of FPGAs make the overall design extremely flexible, allowing many different functions (or design modifications) to be realized without hardware changes. Incorporation of extensive onboard diagnostics, implemented in the FPGAs, is required by the very high level of integration and density achieved by this system.**

I. Introduction

We have designed a Positron Emission Mammography (PEM) camera [1] based on a detector module that uses a photomultiplier tube (PMT) and PIN photodiode array (PD) to read out an array of 64 optically isolated LSO crystals [2, 3]. The PMT provides timing information (7 bits) and location of the module, the PD array identifies the crystal of interaction (12 bits), the sum of the PD and PMT signals provide an estimate of the total energy deposit (8 bits), and the ratio of the PD and PMT signals estimates the interaction depth (3 bits). This module design requires the front-end electronics to perform a significant amount of real-time processing in order to form a "singles" event word.

The camera consists of four planar banks of detector modules arranged in a rectangular array surrounding (and adjacent to) the patient's breast, with each bank containing between nine and fifteen detector modules. Each bank of detectors is placed in time coincidence with each of the other three detector banks, and no interplane septa are used.

The septaless design and close proximity to the patient yield very high solid angle coverage and so imply high event rates. This requires that the time to process each annihilation photon be minimized (our goal is <1 μs) and that the coincidence processing rate be high (our goal is 10 MHz). To meet these electronics challenges, we have constructed a system based on the Siemens/CTI HRRT electronics [4, 5], but containing the significant modifications necessary for this unique configuration.

II. System Architecture

Fig. 1 shows a top level diagram of the electronics. Each of the four "detector heads" services a single bank of detector modules, collecting 24-bit "singles" event words that are forwarded to the coincidence processor. The "coincidence processor" identifies singles events that are in time coincidence among any pair of detector heads and forms 64-bit "coincidence" event words that are passed to the Pentium-based data acquisition computer via a fiber optic link to a Systran SLDC receiver. A "rebinner board" that converts (in real time) crystal-crystal addresses into sinogram space addresses can optionally be placed between the coincidence processor and the fiber optic readout board.

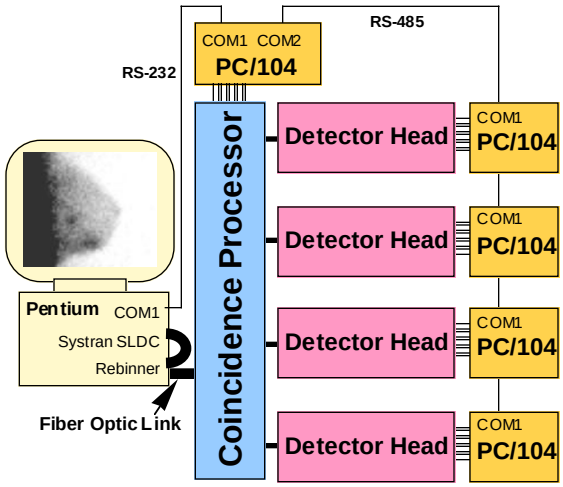

Fig. 1. Top level diagram of the electronics system. Each of the four detector heads collects "singles" events which are forwarded to the coincidence processor. Coincident events are then passed to the Pentium-based data acquisition computer via a fiber optic link to a Systran SLDC receiver. A rebinner board can optionally be placed between the coincidence processor and the fiber optic readout board.

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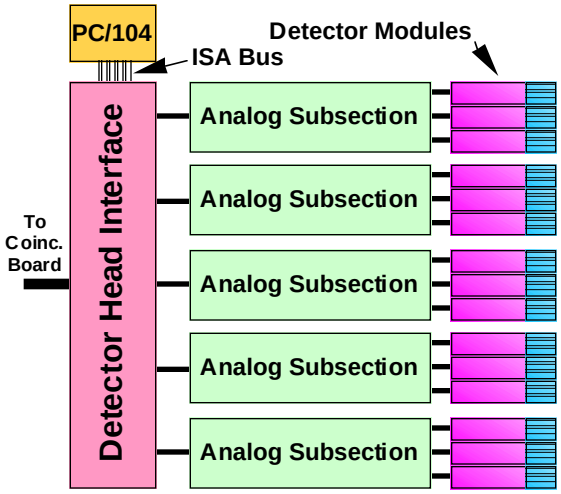

Fig. 2. Diagram of the Detector Head. Three detector modules are serviced by each analog subsection board. The singles event words generated by the analog subsection board are multiplexed by the detector head interface board, which also buffers communication with the PC/104 as well as system timing signals.

Control information is passed between the data acquisition computer and electronics via PC/104 embedded microprocessors. Commands and data are transferred between the COM1 port of the host and the COM1 port of the 486-based PC/104 that controls the coincidence processor using the RS-232 serial point-to-point protocol. Each command includes the numeric identifier of the PC/104 for which the command is intended, and should the command be intended for the coincidence processor board, the PC/104 will act upon the command, passing information to/from that board via the PC/104's ISA bus. If it is not intended for that board, the coincidence PC/104 echoes the command on its COM2 port, relaying it (using the RS-485 serial bus protocol) to all four 386-based PC/104s that service the detector heads. Like before, each of detector head PC/104s examines the numeric identifier of the command, and if the command is meant for that detector head, information is again passed to/from the detector head electronics via the PC/104's ISA bus.

Fig. 2 shows a block diagram of an individual detector head, which processes signals from a single bank of up to 15 detector modules. Groups of three adjacent detector modules are controlled and independently read out by a single "analog subsection" board, whose output is up to three singles event words each SYNC cycle (defined below). A "detector head interface board" provides mechanical support for the analog subsection boards and multiplexes the singles event words, passing up to four singles event words to the coincidence processor board each SYNC cycle. The detector head interface board also communicates directly with the PC/104, passing signals from it to the analog subsection boards when necessary.

System timing signals are generated on the coincidence board and routed to the analog subsection boards via the detector head interface boards. The system clock has a 16 ns period and a synchronization pulse SYNC is generated every 16 clock pulses (*i.e.* with a 256 ns period). In general, each stage of the electronics transfers information to the next stage

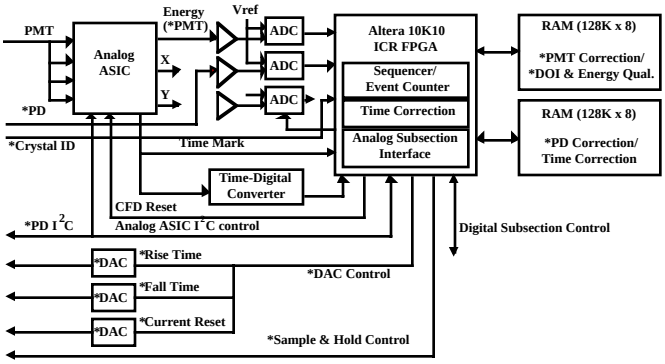

Fig. 3. Diagram of the Analog Subsection Board. Signals unique to the LBNL (as opposed to CTI) version are proceeded with an asterisk (*).

on each cycle of this synchronization pulse. System-wide clock skew and jitter are minimized by keeping clock traces the same length and regenerating the clock pulses with skew adjustment chips.

III. Individual Circuit Boards

A. *Flexible Circuit Board*

The photodiode array for each detector module is controlled by a custom ASIC that amplifies the input signals from each channel (*i.e.* pixel) in the array, identifies the channel with the largest amplitude, and provides as output the (analog) amplitude of this largest signal and the (digital) address of that channel [6]. The ASIC must also be provided with power, ground, and a number of control signals (both analog and digital). This ASIC is mounted "chip-on-board" to a "rigid-flex" circuit board. The size of the rigid area of the board is 1" square that matches the photodiode array, which it is soldered to. This allows the leads that connect the photodiode pixels to the ASIC inputs to be of minimum length, which reduces electronic noise. Several surface mount bypass capacitors are also mounted in this area. The flexible portion of this board is a 0.008" thick Kapton "tail," 1" wide by 18" long. This portion acts as a cable that connects the ASIC to the next level of electronics, but is thin enough to fit between adjacent photomultiplier tubes, minimizing the dead space between detector modules.

B. *Analog Subsection Board*

The outputs of three detector modules are processed by a variant of the analog subsection board for the CTI / Siemens HRRT [4]. Fig. 3 shows the block diagram of a single channel the analog subsection board for this design. The main physical components are identical, namely the ASIC controlling the PMT, the timing circuit, flash ADC's for digitizing the various analog input signals, and an FPGA (field-programmable gate array) coupled to 256 kB of RAM in order to perform the event processing. The main difference in the physical components is the connection to the ASIC for the PD (and removal of the inputs from 3 PMTs).

Processing of the photomultiplier tube signal is performed by a custom ASIC that provides a (digital) timing pulse and the (analog) amplitude of the signal observed by the PMT [7]. While this ASIC was designed to service the 4 PMTs in

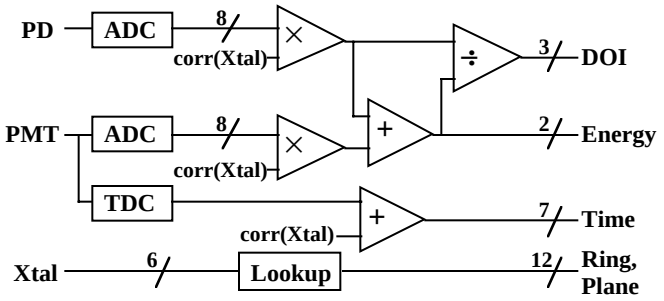

Fig. 4. Diagram of the algorithm performed by the FPGA / RAM combination when in data taking mode.

a block detector module, it is well suited to servicing a single PMT by utilizing only the "Energy" outputs of the ASIC (which sum the 4 PMT inputs).

The 7-bit time-to-digital converter is implemented by passing the timing pulse generated by the PMT ASIC through a 10 tap, 20 ns delay line. The first eight outputs from the delay line are latched on the rising edge of the next 16 ns period clock, indicating the phase of the timing pulse with respect to the 16 ns clock in 2 ns increments. The remaining four bits are obtained by counting 16 ns clock signals in the FPGA. The 256 ns TDC range corresponds to the time between SYNC pulses.

Most of the event processing is performed by the Altera 10K10 FPGA and RAM. As the detectors used by the HRRT and this camera are significantly different, the processing algorithms that are loaded into the FPGA (and the RAM contents) are also quite different. For example, the crystal address is read directly from the PD ASIC rather than being computed from block detector logic. Rather than comparing the deposited energy to a channel dependent window and determining a 1-bit interaction depth based on scintillation decay time, channel by channel gain corrections are applied to the PD and PMT signals and the corrected values summed and ratioed (via RAM lookup) to determine total energy and a 3-bit interaction depth respectively. An example of the algorithms loaded into the FPGA are shown in Fig. 4.

While all three channels of an analog subsection board operate independently while taking data, there are connections that couple the three FPGAs. These connections are used to load data (*e.g.* the contents of the RAM or the setup parameters for the PD and PMT ASICs) into each channel by daisy-chaining the FPGAs, treating each FPGA as part of a shift register, and transferring data using a serial protocol (controlled by the detector head interface). This method is also used to obtain periodic status information from each module, such as the count rate each 100 ms.

Equations are downloaded into the FPGAs via the detector head interface. Identical equations are sent to each channel, but a separate chip select (and download complete) line for each channel allows the user to target the equations to an arbitrary combination of channels. It takes one second to download the equations, limited by the processing time and clock speed of the 386-based PC/104. The download time can be sped up by an order of magnitude using a Pentium-based PC/104, as is now implemented in the HRRT system.

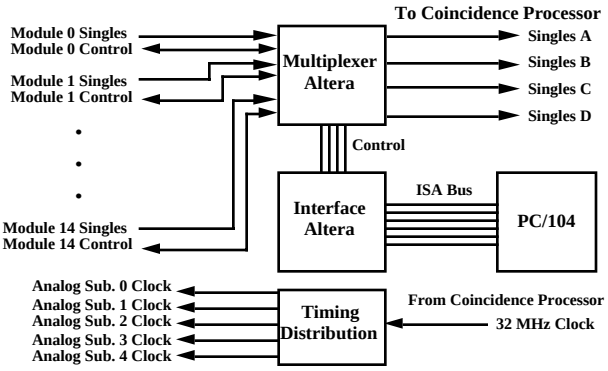

Fig. 5. Diagram of the Detector Head Interface board.

Use of FPGAs (and RAM) allows the electronics to be very flexible and reduces the amount of circuitry necessary. For example, the system can be placed in calibration mode, whereby the full ADC data from the PD and PMT ADCs can be passed to the detector head interface rather than the normal singles event word, or specialized diagnostics and debugging functions (*e.g.* test pulsing) can be performed. One can even do coincident event detection between two detector modules within the board using the connections between FPGAs.

C. Detector Head Interface Board

A diagram of the detector head interface (DHI) board is shown in Fig. 5. Its main purpose is to multiplex the 24-bit singles event words from the analog subsection boards. This board is conceptually identical to that used by the HRRT [4], but services a maximum of 15 (rather than 117) detector modules. Up to 15 singles events can be presented to the detector head interface board every SYNC cycle, but a maximum of four events per SYNC cycle can be transferred to the coincidence processor. Simulation suggests that very few events are lost by this multiplexing — the event rate at which the DHI begins to lose data (approaching 10 MHz) corresponds to a rate at which the front end detector modules have considerable losses due to dead time.

The multiplexing function is performed by an Altera 10K20 FPGA that also provides the fan-out for the analog subsection board communication and control signals. An Altera 10K10 FPGA provides an interface to the PC/104 microprocessor's ISA bus. The PC/104 CPU runs DOS, has 24 MB of FLASH EEPROM available for storage, and can perform relatively complex tasks. For example, all of the equations to be downloaded into the FPGAs and all the data to be loaded into the analog subsection RAM is stored on this local disk, as is the code that performs these downloads and extensive diagnostic / testing software. The PC/104 also performs near real-time control functions such as insertion of tag words.

D. Coincidence Processor Board

Coincidence events are detected and processed using the HRRT Coincidence Controller board, whose block diagram is shown in Fig. 6. As with the detector head interface, an embedded PC/104 microprocessor coupled to an Altera 10K10 FPGA provides communication with the host computer, provides real-time control, and loads equations

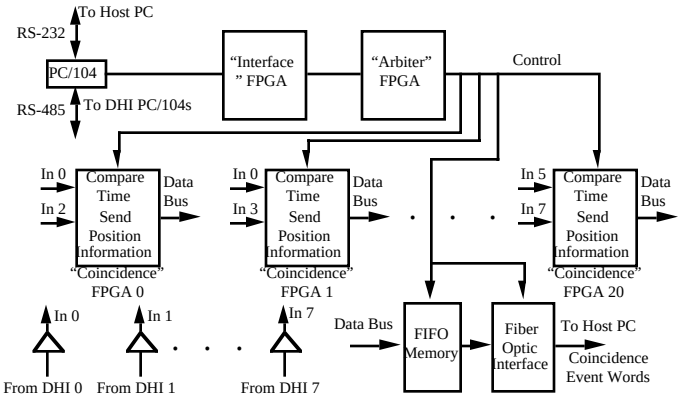

Fig. 6. Diagram of the Coincidence Processor board.

into the coincidence processing Altera 10K30 FPGAs. Singles data from up to eight detector heads are input to the board and time correlation performed. A single FPGA handles time coincidence between any two DHI connections (module pairs), formats the ensuing 64-bit coincidence event word, and places the event word into a FIFO memory. In the HRRT, each detector head is placed in coincidence with all other detector heads except for the two adjacent heads (and itself), giving 20 module pairs that are processed by 20 Altera data processing FPGAs. For the PEM camera, there are only four detector heads that must all be in coincidence — achieved by using alternating DHI inputs to the HRRT coincidence controller. Alternatively, equations corresponding to "pass-through" mode can be loaded into the coincidence FPGAs. In this mode, which is used for calibration, debugging, etc., singles events are passed unaltered (and without demanding time coincidence with another singles event) through the coincidence FPGAs. A final arbiter Altera 10K20 FPGA controls the passing of the coincidence event word to an optical fiber readout that can send up to four 64-bit coincidence event words to the host computer every 256 ns, giving a board throughput of 15.625 million events per second, which is more than adequate for the PEM application. The output of this fiber optic cable can be read directly by the host PC (via a Systran SLDC PCI plug-in board) in list mode.

E. Rebinner Board

The inclusion of 3 bits of depth of interaction information per "Singles" event (and thus 6 bits per coincident event) yields a larger number of lines of response (LORs) than is practical to histogram. As many of these LORs are either redundant (exactly overlap or nearly overlap in space), the number of effective LORs can be reduced significantly by combining these redundant LORs. This can be done by passing the coincident data through a real-time rebinner board before it is read into the PC memory. This board rearranges the data into a format more suitable for histogramming. The board also plugs into an ISA slot in the host computer and has fiber optic inputs and outputs. The design of the system and the board permit the rebinner to be optionally inserted into the fiber optic data stream between the coincidence board and the Systran SLDC receiver. This board is currently used by both the CTI/Siemens HRRT and PET/SPECT.

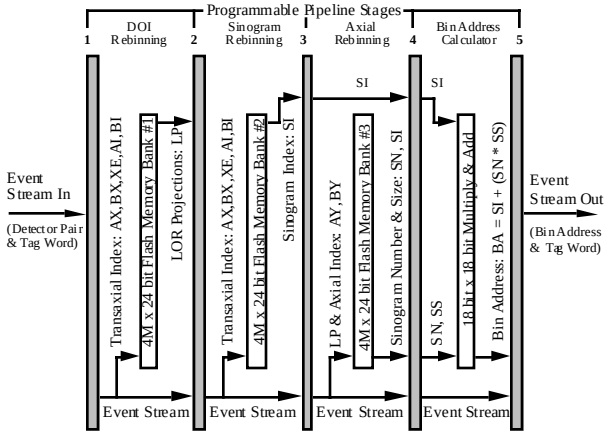

Fig. 7. Diagram of the Rebinner board. Data flow is from left to right.

A fiber-optic 1Gigabaud Fiber Channel interface receives the 64 bit (detector pair index) packets and transmits the 32 bit (projection space index) packets in real time. Rebinning occurs at a sustained rate of 8 to 10 MHz. For command, control and configuration programming, this rebinner card connects to either the ISA bus or the PC/104 bus and is designed for PC compatibility. Internally, the rebinner uses PLD and flash memory technology to perform the rebinning function in a rapid fashion. Fig. 7 shows a block diagram of the circuit. The circuit is made up of 5 programmable pipeline stages serving 4 processing banks. The first 3 banks are comprised of flash memory to implement functional look-up tables. Each of the 3 banks of flash memory is a 4 M x 24 bit array. The fourth bank is an algebraic calculator with an 18x18 integer multiplier and 36 bit adder. These 4 processing banks operate simultaneously and each completes in 100 ns. Such speed permits 10 M event-packet per second pipelining. The circuit is implemented with FPGAs to allow this complex circuit to be realized in a small physical space with a large degree of flexibility.

Fig. 8 illustrates an example of the processing performed by the rebinner board. Given the crystal indices and interaction depths, rebinner bank #2 produces the x,y coordinates of the interaction points (xa,ya) and (xb,yb), as well as the nearest neighbor sinogram indexes, sa and ro, for mapping into projection space. The sinogram index is the primary output produced by bank #2. Complete definitions of the coordinate definitions can be found in the PETLINK™ guideline

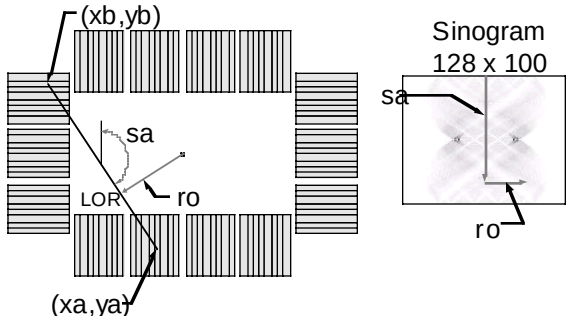

Fig. 8. Functionality of rebinner bank #2. The main purpose is to convert crystal indices (shown in "detector space" on the left side of the figure) into x,y coordinates and sinogram indexes (sa,ro), shown in "sinogram space" at the right.

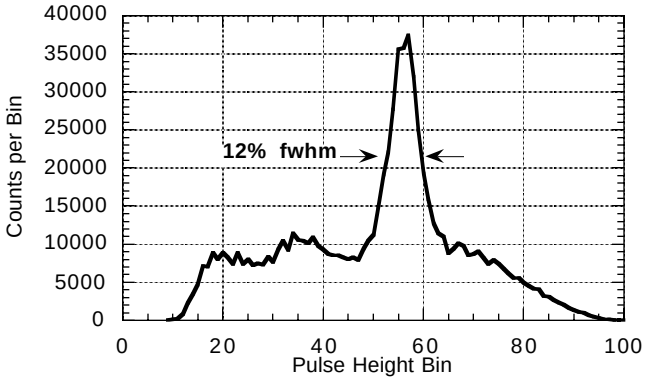

Fig. 9. 511 keV photopeak obtained with the electronics.

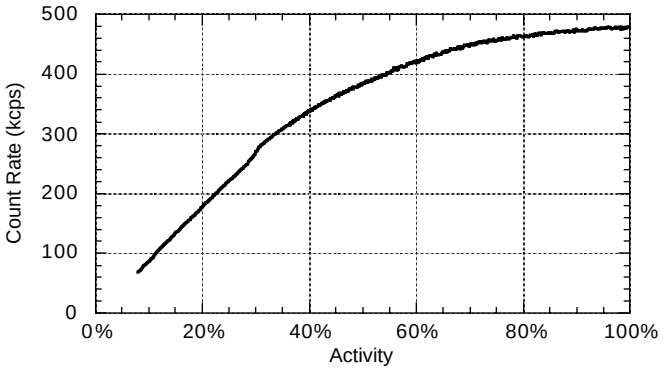

Fig. 10. Observed count rate as a function of activity.

document and other documents available on-line [8].

IV. Performance Measurement

The electronics described has been fabricated and tested, and its performance meets the design goals. Fig. 9 shows a pulse height spectrum obtained by exciting a single detector module (that contained only a photomultiplier tube, and so did not have depth of interaction measurement ability). The output from this detector module was digitized by the analog subsection board, passed through the detector head interface and coincidence processor boards, and read out in list mode by the data acquisition PC (*i.e.* it went through the entire processing chain with the exception of the rebinner board). A 511 keV photopeak with 12% fwhm is clearly seen over the background caused by the naturally abundant ^{176}Lu in the LSO scintillator crystal.

The rate capability of a single channel of the analog subsection board (and portions of the rest of the electronics) is tested by exciting a detector module with a 20 mCi ^{13}N source placed in close proximity to the detector, then observing the measured count rate as a function of time. Since the goal is to observe the processing dead time (as opposed to imaging performance), triggers are accepted as events even if their energy is not consistent with a 511 keV energy deposit. The data are shown in Fig. 10, and are well fit by a paralyzing dead time of 0.75 µs, although a non-paralyzing dead time of 1.2 µs also yields a reasonably good fit. The dead time limited maximum event rate is 480 kHz.

The rate capability of the remainder of the system (*i.e.* detector head interface, coincidence processor, and fiber optic readout) is difficult to verify, as the system is designed for the detectors to saturate before these portions exhibit significant dead time. Simulation suggests that this is the case, and the coincidence processor board and fiber optic readout were used to evaluate the count rate performance of the HRRT [9]. The data presented in that paper demonstrate coincidence event rates (Trues + Scatter + 2*Randoms) of 7 MHz (limited by the amount of activity placed in the field of view), which is approximately half of the expected maximum rate.

V. Acknowledgment

This work was supported in part by the This work was supported in part by the Director, Office of Science, Office of Biological and Environmental Research, Medical Science Division of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098, and in part by the National Institutes of Health, National Cancer Institute under grant No. R01-CA67911, and National Institutes of Health, National Heart, Lung, and Blood Institute under grant No. P01-HL25840.. Reference to a company or product name does not imply approval or recommendation by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

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