Title
Coupling Two-Dimensional Materials with Solid-State Ionics for Programmable Electronics

Author
Lee, Sungjoon

Publication Date
2019

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

Coupling Two-Dimensional Materials with Solid-State Ionics for Programmable Electronics

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Sungjoon Lee

2019

ABSTRACT OF THE DISSERTATION

Coupling Two-dimensional Materials with Solid-State Ionics for Programmable Electronics

by

Sungjoon Lee

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2019

Professor Yu Huang, Chair

Diodes and transistors represent the fundamental device building blocks for modern semiconductor electronics. Two-dimensional (2D) semiconductors have drawn considerable recent interest for their atomically thin channel and electrostatically tunable device characteristics. However, unlike three-dimensional (3D) semiconductors in which the selective impurity doping can be readily used for controlling the charge carrier type/concentration and realizing functional diodes and transistors, the impurity doping in 2D semiconductors has been challenging due to the limited physical space in the atomically thin lattice for incorporating impurity dopants. To date, the carrier type is usually determined by its intrinsic defects of a given 2D semiconductor and hardly tunable for specific device functions. The creation of diodes or complementary transistor circuits is typically achieved

by physical assembly of two distinct 2D semiconductors with intrinsically opposite carrier types. In this dissertation, the development of novel solid-state ionic doping approaches is reported and investigated with which a new class of programmable devices are created to enable 2D diodes, transistors and complementary inverters with tunable carrier type and device polarity. In the first part, by using organic-inorganic halide perovskite materials (methylammonium lead iodide, $CH_3NH_3PbI_3$) as a solid-state ionic doping agent, a 2D field-effect transistor can be transformed to reversibly switchable diodes and transistors. The perovskite layer not only provides effective doping effects to semiconductor channels, but also greatly enhances the optical absorption of the 2D transistors. In the next chapter, superionic silver iodide (AgI) is employed as a solid-state ionic dopant to show that few-layer WSe_2 field-effect transistors can be reversibly transformed into transistors with switchable polarity or diodes with near-unity ideality factors which stably operate at room temperature. Furthermore, complementary logic gates including inverter, NAND and NOR gates are constructed by integrating innately identical transistors. Lastly, it is demonstrated that programmed functions can be erased by thermal or irradiation excitation in a triggerable manner, creating a transient electronic system attractive for protecting vital information.

The dissertation of Sungjoon Lee is approved.

Ali Mosleh

Yong Chen

Xiangfeng Duan

Yu Huang, Committee Chair

University of California, Los Angeles

2019

Dedicated

To

my parents, Seunghoon and Miae,

my brother, Sungwook,

whose loving spirit sustains me still

and

my wife, Inyoung,

without whom my life is incomplete.

TABLE OF CONTENTS

LIST OF FIGURES

Chapter 2. Electrostatic Doping Effects of Organohalide Perovskite on Two-Dimensional Semiconductor

Chapter 3. Electrostatic Doping Effects of Silver Iodide on Two-Dimensional Semiconductor

Chapter 4. Programmable Devices for Transient Electronics

LIST OF TABLES

ACKNOWLEDGEMENTS

It has been a great privilege to be a graduate student in the Department of Materials Science and Engineering at University of California, Los Angeles. The past five years has been the most important and, without any doubt, was a turning point in my life. I would like to take this opportunity to express my appreciation to many people who have made these years beautiful memory.

Foremost, I would like to express my sincere gratitude to my advisors, Professor Yu Huang and Professor Xiangfeng Duan, for their invaluable guidance on my research. I have always been impressed by their profound knowledge and keen insight to find scientific obstacles important but easy to miss. Their passion in science and education is incomparable that leads a great success as both scientists and mentors, which I admire and emulate. I respect their constant enthusiasm for exploring new challenges, and persistence in coming up with insane ideas and making them right. It has been a great privilege to join their research group and learn from such creative, enthusiastic and inexhaustible minds. I also would like to thank the members on my thesis committee, Professor Ali Mosleh and Professor Yong Chen, for reading my thesis and providing talented comments and sharp insight. They have been of great help on my oral qualification exam and final dissertation.

I have enjoyed working with an outstanding group of highly motivated minds. In particular, Dr. Hung-Chieh Cheng taught me many experimental details in electronics and optoelectronics, and helped me a lot in many aspects in both research and life to quickly adapt to the new environment when I first came here, for which I have been always grateful. I admire Dr. Yuan Liu for his outstanding research capability and free mind. Dr. Zhaoyang Lin has always been a source of rich experience in research. Dr. Jian Guo and Dr. Yiliu Wang are good friends of mine and we

together went through many tough things in the lab. Dr. Yun-Chiao Huang is a very nice person who helped me quite much in my life here and future career plan. Hyunpil Boo, Chungseok Choi, Dr. Enbo Zhu, Dr. Hao Wu, Dr. Zipeng Zhao, Dr. Chen Wang, Dr. Hui-Ying Shiu and Dr. Mengning Ding introduced me to the group and unselfishly helped me with my research projects.

I am pleased to share daily working routine with a long list of previous and current members of Huang and Duan group. Their willingness to help has made difficult problems a lot easier. Many thanks to Dr. Huilong Fei, Dr. Chuancheng Jia, Dr. Zheng Fan, Jin Huang, Peiqi Wang, Dr. Chen Peng, Zhihong Huang, Dr. Mufan Li, Dr. Ben Papandrea, Dr. Boris Volosskiy, Dr. Hongtao Sun, Ziying Feng, Michelle Flores, Bocheng Cao, Chengzhang Wan, Guangyan Zhong and Daniel Baumann, for many help and discussion once in a while. I also would like to thank my UCLA friends Dr. Jin-Wook Lee, Christopher Sungeun Choi, Dr. You-Seung Rim, Dr. Sang-Hoon Bae, Dr. Tae-Hee Han and Dr. Sheng-Yung Chang from whom I have learned the great passion and sincere attitude toward research.

Last but not least, I could not thank enough to my parents, my brother, my family and my wife for their continuous support and unconditional love. I could not have achieved what I have today without them. It is to them this humble dissertation is dedicated.

VITA

2006 – 2013	Bachelor of Science in Materials Science and Engineering Seoul National University, Seoul, South Korea
2014 – 2019	Graduate Student Researcher Department of Materials Science and Engineering University of California, Los Angeles

Chapter 1. Introduction and Objectives

Diodes and transistors are essential to modern electronics and optoelectronics. As the evolution of silicon-based transistors is approaching its technological limits[1], considerable efforts have been devoted worldwide to seeking alternative materials[2] and technologies[3] in order to extend the range of silicon electronics and their functions. The emerging two-dimensional (2D) materials, including graphene and transition-metal dichalcogenides (TMDs), feature an atomically thin geometry[4] with superior immunity to short-channel effects[5] along with other unique attributes such as high flexibility[6, 7], exceptional mechanical strength[8], excellent transparency[9] and broad spectrum tunability[10-13]. However, unlike three-dimensional (3D) semiconductors in which the carrier type and carrier concentration can be easily controlled by impurity doping for realizing functional devices[14], it has been a continual challenge to rationally control the carrier type in 2D semiconductors due to the inherent difficulties in incorporating sufficient impurity dopants in the atomically thin lattices without seriously degrading their structural[15] and electronic properties[16].

To date, the carrier type of a given 2D semiconductor is often determined by its intrinsic defects with limited tunability[17, 18]. Therefore, creating diodes[19-21] or complementary transistor circuits[22] is usually built by heterogeneously combining two distinct 2D semiconductors with intrinsically opposite carrier types or by applying an external electric field to electrostatically tune the carrier transport in split-gate field-effect transistor (FET)[23-26]. Although the split-gate configurations somewhat address the poor tunability of 2D semiconductors, the introduction of additional terminals greatly complicates device design, particularly at the circuit level, and the requirement of a continuous voltage supply due to its high volatility also complicates its practical implementation.

Recently, ionic liquid[27-29] or ionic gel[30] induced doping has been applied to 2D semiconductors to create diodes[31, 32]. In this configuration, split gates are no longer needed to realize a diode, but, instead, the positive and negative ions in ionic liquids can electrostatically modulate the carrier density in devices. However, ionic liquids or gel polymer electrolytes can only be applied to the entire sample and are fundamentally incompatible with solid-state electronic device applications. Moreover, such ionic liquid-induced diodes can only be non-volatile at cryogenic temperatures by freezing the ion motion[31], which still does not resolve the volatility issue for split-gate induced doping.

In this dissertation, to achieve highly controllable, non-invasive and stable doping to 2D semiconductors, a new class of electrostatic doping approach is developed and investigated thereby creating programmable, erasable and reprogrammable 2D diodes, transistors and complementary logic gates. Solid-state ionic conductors, in which electric current is delivered by charged atoms[33], are selected as unique candidates for electrostatic dopants. To couple solid-state ionic materials with inorganic 2D semiconductors and enable the out-of-the-box device functions, a few significant challenges must be addressed. First, it needs to hold established device structures in fully solid-state conditions for better compatibility with conventional electronics. Second, thermal stability must be secured. The programmed device should be able to robustly function at room temperature. Third, once set up, it should retain the desired functions without continuing manipulation (or supply additional voltage). Lastly, the ability to erase and reprogram the device function could enable unconventional transient electronics. In this context, two solid-state ionic materials, organic-inorganic halide perovskite (methylammonium lead iodide, $CH_3NH_3PbI_3$) and superionic silver iodide (AgI), are selected as electrostatic doping agents for 2D semiconductors.

References

1. Lundstrom, M., Moore's law forever? *Science* **2003**, 299, 210-211.

2. Wilk, G. D.; Wallace, R. M.; Anthony, J., High-κ gate dielectrics: Current status and materials properties considerations. *Journal of applied physics* **2001**, 89, 5243-5275.

3. Huang, X.; Lee, W.-C.; Kuo, C.; Hisamoto, D.; Chang, L.; Kedzierski, J.; Anderson, E.; Takeuchi, H.; Choi, Y.-K.; Asano, K., Sub-50 nm P-channel FinFET. *IEEE Transactions on Electron Devices* **2001**, 48, 880-886.

4. Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L.-J.; Loh, K. P.; Zhang, H., The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nature chemistry* **2013**, 5, 263.

5. Liu, H.; Neal, A. T.; Ye, P. D., Channel length scaling of MoS2 MOSFETs. *ACS nano* **2012**, 6, 8563-8569.

6. Vu, Q. A.; Kim, H.; Nguyen, V. L.; Won, U. Y.; Adhikari, S.; Kim, K.; Lee, Y. H.; Yu, W. J., A High-On/Off-Ratio Floating-Gate Memristor Array on a Flexible Substrate via CVD-Grown Large-Area 2D Layer Stacking. *Advanced Materials* **2017**, 29, 1703363.

7. Seo, J.-W. T.; Zhu, J.; Sangwan, V. K.; Secor, E. B.; Wallace, S. G.; Hersam, M. C., Fully Inkjet-Printed, Mechanically Flexible MoS2 Nanosheet Photodetectors. *ACS applied materials & interfaces* **2019**.

8. Lee, C.; Wei, X.; Kysar, J. W.; Hone, J., Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene. *Science* **2008**, 321, 385-388.

9. Li, X.; Zhu, Y.; Cai, W.; Borysiak, M.; Han, B.; Chen, D.; Piner, R. D.; Colombo, L.; Ruoff, R. S., Transfer of large-area graphene films for high-performance transparent conductive electrodes. *Nano letters* **2009**, 9, 4359-4363.

10. Novoselov, K.; Mishchenko, A.; Carvalho, A.; Neto, A. C., 2D materials and van der Waals heterostructures. *Science* **2016**, 353, aac9439.

11. Amani, M.; Lien, D.-H.; Kiriya, D.; Xiao, J.; Azcatl, A.; Noh, J.; Madhvapathy, S. R.; Addou, R.; Santosh, K.; Dubey, M.; Cho, K.; Wallace, R. M.; Lee, S.-C.; He, J.-H.; Ager, J. W., III; Zhang, X.; Yablonovitch, E.; Javey, A., Near-unity photoluminescence quantum yield in MoS2. *Science* **2015**, 350, 1065-1068.

12. Yan, X.; Liu, C.; Li, C.; Bao, W.; Ding, S.; Zhang, D. W.; Zhou, P., Tunable SnSe2/WSe2 heterostructure tunneling field effect transistor. *Small* **2017**, 13, 1701478.

13. Zeng, J.; Liang, S.-J.; Gao, A.; Wang, Y.; Pan, C.; Wu, C.; Liu, E.; Zhang, L.; Cao, T.; Liu, X.; Fu, Y.; Wang, Y.; Watanabe, K.; Taniguchi, T.; Lu, H.; Miao, F., Gate-tunable weak antilocalization in a few-layer InSe. *Physical Review B* **2018**, 98, 125414.

14. Mayer, J. W. In *Ion implantation in semiconductors*, 1973 International Electron Devices Meeting, IEEE: 1973; pp 3-5.

15. Zhang, K.; Feng, S.; Wang, J.; Azcatl, A.; Lu, N.; Addou, R.; Wang, N.; Zhou, C.; Lerach, J.; Bojan, V.; Kim, M. J.; Chen, L.-Q.; Wallace, R. M.; Terrones, M.; Zhu, J.; Robinson, J. A., Manganese doping of monolayer MoS2: the substrate is critical. *Nano letters* **2015**, 15, 6586-6591.

16. Chen, C.-H.; Wu, C.-L.; Pu, J.; Chiu, M.-H.; Kumar, P.; Takenobu, T.; Li, L.-J., Hole mobility enhancement and p-doping in monolayer WSe2 by gold decoration. *2D Materials* **2014**, 1, 034001.

17. Zhou, W.; Zou, X.; Najmaei, S.; Liu, Z.; Shi, Y.; Kong, J.; Lou, J.; Ajayan, P. M.; Yakobson, B. I.; Idrobo, J.-C., Intrinsic structural defects in monolayer molybdenum disulfide. *Nano letters* **2013**, 13, 2615-2622.

18. Singh, A.; Singh, A. K., Origin of n-type conductivity of monolayer MoS2. *Physical Review B* **2019**, 99, 121201.

19. Wang, F.; Wang, Z.; Xu, K.; Wang, F.; Wang, Q.; Huang, Y.; Yin, L.; He, J., Tunable GaTe-MoS2 van der Waals p–n junctions with novel optoelectronic performance. *Nano letters* **2015**, 15, 7558-7566.

20. Cheng, R.; Li, D.; Zhou, H.; Wang, C.; Yin, A.; Jiang, S.; Liu, Y.; Chen, Y.; Huang, Y.; Duan, X., Electroluminescence and photocurrent generation from atomically sharp WSe2/MoS2 heterojunction p–n diodes. *Nano letters* **2014**, 14, 5590-5597.

21. Deng, Y.; Luo, Z.; Conrad, N. J.; Liu, H.; Gong, Y.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Xu, X.; Ye, P. D., Black phosphorus–monolayer MoS2 van der Waals heterojunction p–n diode. *ACS nano* **2014**, 8, 8292-8299.

22. Jeon, P. J.; Kim, J. S.; Lim, J. Y.; Cho, Y.; Pezeshki, A.; Lee, H. S.; Yu, S.; Min, S.-W.; Im, S., Low power consumption complementary inverters with n-MoS2 and p-WSe2 dichalcogenide nanosheets on glass for logic and light-emitting diode circuits. *ACS applied materials & interfaces* **2015**, 7, 22333-22340.

23. Resta, G. V.; Balaji, Y.; Lin, D.; Radu, I. P.; Catthoor, F.; Gaillardon, P.-E.; De Micheli, G., Doping-free complementary logic gates enabled by two-dimensional polarity-controllable transistors. *ACS nano* **2018**, 12, 7039-7047.

24. Baugher, B. W.; Churchill, H. O.; Yang, Y.; Jarillo-Herrero, P., Optoelectronic devices based on electrically tunable p–n diodes in a monolayer dichalcogenide. *Nature nanotechnology* **2014**, 9, 262.

25. Li, D.; Chen, M.; Sun, Z.; Yu, P.; Liu, Z.; Ajayan, P. M.; Zhang, Z., Two-dimensional non-volatile programmable p–n junctions. *Nature nanotechnology* **2017**, 12, 901.

26. Pospischil, A.; Furchi, M. M.; Mueller, T., Solar-energy conversion and light emission in an atomic monolayer pn diode. *Nature nanotechnology* **2014**, 9, 257-261.

27. Perera, M. M.; Lin, M.-W.; Chuang, H.-J.; Chamlagain, B. P.; Wang, C.; Tan, X.; Cheng, M. M.-C.; Tománek, D.; Zhou, Z., Improved carrier mobility in few-layer MoS2 field-effect transistors with ionic-liquid gating. *ACS nano* **2013**, 7, 4449-4458.

28. Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y., Ambipolar MoS2 thin flake transistors. *Nano letters* **2012**, 12, 1136-1140.

29. Zhang, Y.; Ye, J.; Yomogida, Y.; Takenobu, T.; Iwasa, Y., Formation of a stable p–n junction in a liquid-gated MoS2 ambipolar transistor. *Nano letters* **2013**, 13, 3023-3028.

30. Allain, A.; Kis, A., Electron and hole mobilities in single-layer WSe2. *ACS nano* **2014**, 8, 7180-7185.

31. Zhang, Y.; Oka, T.; Suzuki, R.; Ye, J.; Iwasa, Y., Electrically switchable chiral light-emitting transistor. *Science* **2014**, 344, 725-728.

32. Pu, J.; Fujimoto, T.; Ohasi, Y.; Kimura, S.; Chen, C. H.; Li, L. J.; Sakanoue, T.; Takenobu, T., A versatile and simple approach to generate light emission in semiconductors mediated by electric double layers. *Advanced Materials* **2017**, 29, 1606918.

33. Farrington, G. C., Solid ionic conductors. *Sensors and Actuators* **1981**, 1, 329-346.

Chapter 2. Electrostatic Doping Effects of Organic-Inorganic Perovskite on Two-Dimensional Semiconductors

2.1. Introduction

Electrostatic doping has been widely used in low-dimensional materials, including carbon nanotube, graphene and atomically thin TMDs[1-12]. The traditional doping method involving insertion of alien atoms may damage the lattice of these materials and affect the carrier transport in low-dimensional materials. A well-adopted method to control the carrier density and the dominant type of carrier is by applying an electric field to semiconducting channel materials in FETs with split-gates embedded and floated within gate dielectrics. With field-effect induced doping, the fundamental junction properties can be examined and reconfigured without both physical and chemical modification of low-dimensional materials. Even though the split-gate designs provide a well-controlled junction and effective carrier doping, such devices usually require complicated fabrication process and operating procedure. Recently, ionic liquid induced doping has been applied to single-layer WSe_2 to create p-n junction, which allows circularly polarized emission to be generated due to strong spin-valley coupling[2, 8]. In this configuration, split gates are no longer needed to realize a p-n junction, instead, the positive and negative ions in ionic liquid can electrostatically modulate the carrier density in WSe_2 FETs. By electrically poling the ionic liquid at room temperature, the positive and negative ion accumulate at two ends of the device and induce n-type and p-type regions in WSe_2, thus creating a p-n junction. Such a p-n junction can be further stabilized at low temperature by freezing the ion motion to keep the status of the device[2, 8]. However, the ionic liquid can only be applied to entire sample and its liquid form is less convenient to solid-state electronic device applications. Here a novel electrostatic doping strategy for 2D materials is proposed in which organic-inorganic halide perovskite (methylammonium lead

iodide, $CH_3NH_3PbI_3$) is employed as a solid-state ionic conductor to facilitate the electrostatic doping and the formation of switchable diodes and transistors on 2D semiconductor FETs through solid-state electrical poling process. Moreover, unlike ionic liquid, the well-defined shape of ionic solid offers a local control of the doping in 2D semiconductors, enabling diverse designs of solid-state electronic and optoelectronic devices.

Recently, methylammonium lead iodide perovskite ($CH_3NH_3PbI_3$) has attracted intensive interests for its potential for solar cell applications[13-24]. On the other hand, this type of perovskite is an ionic solid composed of organic cations, metal cations and halide anions. It has been reported that the ion migration in the perovskite may occur under applied electric field, which is also considered as one of the origins causing large hysteresis in voltage-dependent photocurrent[25-29]. For example, a switchable photovoltaic effect was reported from $CH_3NH_3PbI_3$ solar cell[30]. They have created a switchable p-i-n junction on $CH_3NH_3PbI_3$ both in lateral and vertical directions by poling the perovskite materials with electric fields, resulting in the observation of both switchable open-circuit voltage (V_{OC}) and short-circuit current (J_{SC}). It is suggested that the migration of positively charged ions and negatively charged ions could induce n-type and p-type regions in the perovskite, respectively. Such ion migration could eventually lead to ion accumulation under applied electric field similar to the effect with ionic liquid[2, 8]. Although ion migration is undesired and considered one main challenge that contributes to the insufficient stability in perovskite devices, the disadvantage can be turned into advantage in a different point of view. In this chapter, the heterostructure of two different kinds of materials, $CH_3NH_3PbI_3$ and TMDs, is introduced to investigate the ionic doping effect on TMDs by $CH_3NH_3PbI_3$ perovskite[18, 31]. Electronic properties of 2D semiconductor channels could be locally modified either to n-type and p-type regions by $CH_3NH_3PbI_3$ perovskite serving as a non-covalent doping agent. With well-defined geometry of

the perovskite ionic solid, the semiconductor channel of the FETs can be partially modified. The resulting functional heterostructures which enables the extension of design capability can be created. Such controllable doping effect can also be used to enhance optoelectronic properties of TMD-based devices or even create a switchable p-n junction, thereby facilitating the extraction of photo-generated carriers due to strong built-in electric field.

2.2. Experimental section

Preparation of 2D materials

Graphene was originally obtained by micromechanical exfoliation of layer after layer from naturally occurring graphite[32]. This strategy has also been applied to many other 2D materials such as WSe_2 and h-BN that are found in 3D stacked forms, from both naturally occurring minerals and artificially synthesized bulk crystals (Figure 1). Typically, this mechanical exfoliation approach yields the highest-quality material, which is ideally suited for fundamental studies.

van der Waals heterostructure assembly

Once the atomically thin layers are attained from the mechanical exfoliation, it is necessary to assemble them into the desired stacking order to create the desired van der Waals heterostructure. A microscope stage equipped with micromanipulators is crucial in both wet and dry transfer methods to properly align the micrometer-scale flakes. The first step of assembly is mechanical exfoliation of a 2D bulk material onto an existing substrate. A second 2D material can then be dry exfoliated using a sacrificial polymer such as poly(methyl methacrylate) (PMMA) or poly(propylene carbonate)) (PPC). The flake with the polymer is then transferred onto a

transparent stamp (e.g. poly(dimethyl siloxane) (PDMS)) that is positioned using the micromanipulators into the desired location and orientation (with respect to the first flake) under the objective lens, and lowered down until the two flakes make contact to form the van der Waals heterostructure. Although the polymer can be directly dissolved to achieve the desired two-layer structure, residue left on top of the surface hinders further stacking, which is only useful for simple two-layer structures or as the last stacked layer. To achieve complex multilayer stacking without polymer residue between individual layers, more advanced peel-off and pick-up methods have been developed[33]. A major advantage of these alignment transfer techniques is their independence from the materials being transferred, as long as they are stable and robust enough to endure the process. Using this exfoliation and restacking approach, complex van der Waals heterostructure are easily created with atomically sharp interfaces[34]. It is conceivable that air-sensitive (e.g. black phosphorus) could be transferred using this approach in inert environments.

Preparation of precursor of $CH_3NH_3PbI_3$: lead iodide (PbI_2)

$CH_3NH_3PbI_3$ can be converted from layered lead iodide (PbI_2). During the conversion, the crystal structure of PbI_2 undergoes the structural rearrangement as the organic cations are inserted into the interstice of corner sharing PbI_6 octahedra[35]. PbI_2 thin flake was obtained by mechanical exfoliation of the bulk PbI_2 crystal. To obtain the bulk PbI_2 crystal, commercial PbI_2 powder of 0.4 g in 100 ml deionized water at 100 ℃. The solution is fully stirred at 100 ℃ and slowly cooled down to room temperature. Due to much lower solubility of PbI_2 in water at room temperature, the crystal starts precipitating and growing during the cooling down process. Once the solution reached to room temperature, the solution was poured into a crystallizing dish and its clear solution was removed by pipette. Then, the precipitated crystals were further dried in oven.

Fabrication of PbI_2/WSe_2 FETs

To fabricate WSe_2 field-effect transistors, single-layer of WSe_2 samples were first exfoliated on an oxygen plasma treated 300 nm SiO_2/Si substrate. The device pattern is defined by electron-beam lithography, followed by pattern development in IPA/water (7:3 volume ratio) and Au deposition (30 nm) in an electron-beam evaporator for defining contact electrodes of WSe_2 FETs. On the other hand, for the FETs in which a pair of graphene flakes are used as drain and source contacts, the graphene flakes are laminated on WSe_2 followed by PbI_2 transfer. In this case, Cr/Au (20 nm/80 nm) are adopted for the contact with graphene electrodes and the PMMA/metal is lifted off in chloroform for 10 minutes. Using conventional adhesive tape method, thinner PbI_2 crystals (several nanometer to single layer) can be easily obtained from the resulted bulk crystals due to its inherent layered structural characteristic.

$CH_3NH_3PbI_3$ vapor conversion from precursor PbI_2

After PbI_2 transfer process, the PMMA polymer medium is dissolved in chloroform for 10 minutes. The PbI_2 sitting on a prepared WSe_2 can further be converted into $CH_3NH_3PbI_3$ using vapor phase intercalation process[35]. In the conversion process, the sample was placed at the downstream of a quartz furnace tube in which a sapphire boat contained CH_3NH_3I powder near the center of tube furnace. By heating up to 130 ℃, the CH_3NH_3I vapor carried by argon gas was brought to the sample sitting at the downstream. The reaction time could take around 1 to 3 hours for the PbI_2 to be fully converted into $CH_3NH_3PbI_3$. A sample before and after conversion process showed a stark color change (Figure 2). The photoluminescence (PL) spectrum taken from an identical spot shows the advent of the clear peak at 760 nm after conversion, demonstrating a successful conversion to $CH_3NH_3PbI_3$ (ref. [18]) (Figure 3). To ensure the stability of the devices,

another separately prepared hexagonal boron nitride (h-BN) is used to cover the entire area of perovskite after conversion process.

Device characterization

The electrical and low temperature measurements were both carried out in commercial probe station (Lakeshore, TTP4) equipped with a 532 nm wide-field laser (Coherent, 532-100). The electrical measurement was conducted with precision source/measurement unit (Agilent, B2902A). The photoluminescence spectra were taken with a commercial confocal micro-Raman system (Horiba LABHR) excited by Ar-ion laser (488 nm) with an excitation power ~3.8 μW. The photocurrent map was conducted in the same system by monitoring the current under the irradiation of focused laser (488 nm, < 300 nW) while moving the stage within a specified area. The AFM images were taken from Bruker Dimension 5000 Icon scanning probe microscope.

2.3. Results and discussion

Thermal stability of h-BN encapsulated $CH_3NH_3PbI_3$

$CH_3NH_3PbI_3$ perovskite has attracted considerable interest for its high-efficiency, low-cost solar cells, but is currently plagued by its poor environmental and thermal stability. To aid the development of robust devices, we investigated the microscopic degradation pathways of $CH_3NH_3PbI_3$ microplates[36]. We employed h-BN thin flakes as the encapsulation layer on $CH_3NH_3PbI_3$ surface and fabricated a h-BN/$CH_3NH_3PbI_3$/h-BN heterostructure (Figure 4a-c). We conducted in situ characterization of the h-BN/$CH_3NH_3PbI_3$/h-BN heterostructure in vacuum at 358 K. We demonstrated that encapsulated h-BN showed considerably improved thermal stability.

In particular, no obvious structural change is observed after 30 min of continuous heating at 358 K (Figure 5), in stark contrast to the rapid emergence of the trigonal phase within 1 min and the complete transformation to trigonal PbI_2 within 7 min of the same thermal treatment for the non-encapsulated tetragonal perovskites[37].

As-fabricated doping effect of $CH_3NH_3PbI_3$ on WSe_2 FETs

To elucidate the doping effect introduced by ionic solid, FETs based on single-layer WSe_2 were adopted due to their ambipolarity which could facilitate the observation of both n-type and p-type doping effect. To investigate the ion doping effect and delineate the contribution from WSe_2 and $CH_3NH_3PbI_3$, we have fabricated FETs with $CH_3NH_3PbI_3/WSe_2$ stacked structure, and $CH_3NH_3PbI_3$ with h-BN encapsulation, respectively (Figure 6b). Additionally, the same WSe_2 FET itself was also studied for comparison before integration with $CH_3NH_3PbI_3$ (Figure 6a). Electrical transport studies of the pristine WSe_2 FET showed a typical ambipolarity with slight p-doping (Figure 7a). After $CH_3NH_3PbI_3$ integration (Figure 6c), the $CH_3NH_3PbI_3/WSe_2$ FETs showed strong p-type doping effect with the drain-source current increased by 2-5 orders of magnitude (Figure 7c). It is important to note that the current in $CH_3NH_3PbI_3$ semiconductor channel (without WSe_2) is essentially at the baseline of our measurement resolution, which 4-5 orders of magnitude smaller than that in the $CH_3NH_3PbI_3/WSe_2$ FETs, which implies that the $CH_3NH_3PbI_3$ itself does not directly contribute to charge transport but only serves as a doping agent to dramatically increase carrier density and conductivity in WSe_2. By comparing the device current measured under illumination and dark conditions in transfer curves (I_{DS}-V_{DS} at V_{DS} = 5 V), we obtained photocurrent ($I_{ph} = I_{light} - I_{dark}$) for both the $CH_3NH_3PbI_3$ ($I_{ph,perov}$) FET and the $CH_3NH_3PbI_3/WSe_2$ ($I_{ph,hybrid}$) FET (Figure 7, b and c). We found that $I_{ph,hybrid}$ is more than 4 orders of magnitude larger than $I_{ph,perov}$ at V_G = -40 V, and more than 3 orders of magnitude larger when

V_G = 40 V, implying that the $CH_3NH_3PbI_3/WSe_2$ channel can be much more efficient that $CH_3NH_3PbI_3$ itself in terms of photo-carrier extraction.

Partial ionic doping effect on $CH_3NH_3PbI_3/MoS_2$ FETs

Unlike ionic liquid doping, the solid-state ionic conductors allow more flexible designs for solid-state electronic devices. For example, by partially covering the channel in MoS_2 FET with $CH_3NH_3PbI_3$, it is possible to partially modify the electronic properties of MoS_2 channel (intrinsically n-type semiconductor), and turn it into p-type characteristics thereby creating p-n junction like device. To contrast the doping effect by $CH_3NH_3PbI_3$, we fabricate a single-layer MoS_2 FET on a (3-aminopropyl)triethoxysilane (APTES) treated SiO_2/Si substrate which provides extra n-doping to MoS_2 device. The bare singl-layer MoS_2 FET was initially highly n-doped by APTES-treated substrate as shown in the transfer curve with a rather negative threshold voltage beyond -60 V (Figure 8c). A layer of $CH_3NH_3PbI_3$ was then integrated with prepared MoS_2 FET and partially covered the MoS_2 semiconductor channel (Figure 8b). With $CH_3NH_3PbI_3$ integration, the device showed a drastic reduction in drain-source current with the threshold shift back to nearly 0 V, which can be attributed to partial p-doping induced by $CH_3NH_3PbI_3$ at room temperature (Figure 8c). It is noted that this is consistent with the observation from WSe_2 FET. With partially p-doped region, the single-layer MoS_2 FET showed an apparent diode behavior (Figure 9d). The positively biased condition (V_{DS} = 5 V) has a larger ON-current and gate response than the negatively biased one (V_{DS} = -5 V) (Figure 9c). This can be attributed to the difference of channel conductivity in these two distinct regions ($CH_3NH_3PbI_3/MoS_2$ and bare MoS_2). Under positive bias voltage, the device current was controlled by the injected electrons from B electrode (grounded) to A electrode (Figure 9a). At the junction of bare MoS_2 and $CH_3NH_3PbI_3/MoS_2$, the electron is injected from the intrinsic region to the doped region of MoS_2 in which the intrinsic part can easily

be modulated by gate electric field, thus the output current can be modulated by changing the gate voltages (Figure 9c and d). On the other hand, under negatively biased voltage, the output current was controlled by electron injection from the p-doped region to the intrinsic part of MoS_2. Due to less available carriers and ionic screening effect induced by $CH_3NH_3PbI_3$ in p-doped region, the output current is much smaller and less affected by the gate modulation, therefore asymmetric output characteristics were both observed (Figure 9c and d). In this case, we showed that ionic solid provides a more flexible way to dope the semiconductor channel of 2D materials than ionic liquid, which could also facilitate the design of 2D material-based electronic applications.

Gate-controlled ionic doping effect on $CH_3NH_3PbI_3/WSe_2$ FETs

The above studies clearly demonstrate the ionic doping can easily tailor the charge transport properties in 2D semiconductors. It is thus possible to use an applied voltage to control the ion migration, and selectively accumulate either positive or negative charges at the interface of $CH_3NH_3PbI_3$ and 2D semiconductor channel. We have examined the possibility to directly create a carrier type-switchable FET in $CH_3NH_3PbI_3/WSe_2$ FETs. As an ionic solid with migrating ion species, the ions in $CH_3NH_3PbI_3$ can be polarized with electric field, thereby facilitating conceivable ion migration which could induce n-type or p-type doping in underlying materials such as WSe_2 through accumulation of positively or negatively charged ions, respectively. To facilitate a type-switchable doping effect of $CH_3NH_3PbI_3$, $CH_3NH_3PbI_3/WSe_2$ FETs were fabricated on a APTES-treated SiO_2/Si substrate which provides n-doping to the WSe_2 channel. The transfer curve of the as-fabricated $CH_3NH_3PbI_3/WSe_2$ FET showed p-type characteristics under dark condition at 77 K (Figure 10b). To examine the poling effect, a large back-gate bias voltage was applied against initial non-poling status. To facilitate ion migration in $CH_3NH_3PbI_3$ layer, the substrate was heated up to 400 K. After 5 minutes of electrical poling at 400 K, the

substrate was cooled down to 77 K. The back-gate bias voltage was continuously applied during this cooling process to ensure that the ion migration is suppressed at low temperature thereby the frozen ions stay in place. During the negative poling process (V_G = -60 V), the positive ions are supposed to migrate to the interface between $CH_3NH_3PbI_3$ and WSe_2, while negative ions should move away from the interface (Figure 10a). After negative poling, the transfer curve switched from p-type to n-type, showing that a completely opposite type of carrier dominates in the $CH_3NH_3PbI_3/WSe_2$ semiconductor channel (Figure 10b). To highlight the controllability of this vertically poled doping effect, a positive back-gate bias voltage (V_G = +60 V) has been applied to the same device following the identical poling procedure as we previously performed with the negative poling. The results indicate that the type of majority carrier returned from n-type to its original p-type characteristics after the positive vertical poling process. This gate bias voltage-induced switching behavior has demonstrated that the carrier type of semiconductor in $CH_3NH_3PbI_3/WSe_2$ FETs could be controlled by the reversible ion migration in $CH_3NH_3PbI_3$ perovskite.

Drain-controlled ionic doping effect on $CH_3NH_3PbI_3/WSe_2$ FETs

Taking a step further, in this session, a switchable p-n junction in $CH_3NH_3PbI_3/WSe_2$ FETs has been examined based on the knowledge from the gate-controlled doping effect (Figure 10). Similar to vertical poling process, mobile ions in $CH_3NH_3PbI_3$ perovskite can be polarized by electric field (here, not gate but drain-source voltage), thereby facilitating ion migration which could result in doping effect on underlying 2D semiconducting channel through ion accumulation on both ends.

Transfer and output curves of pristine single-layer WSe_2 FETs show that the device is in OFF-state and no current was detected even under light excitation (Figure 11). At $V_G = 0$ V, the single-layer WSe_2 FET was in OFF-state where no output current was observed even under light excitation (Figure 11b). A 6-μm long channel of the $CH_3NH_3PbI_3/WSe_2$ FET with h-BN top encapsulation was fabricated (Figure 12a). The output curves show an asymmetric behavior as well as a small open-circuit voltage (V_{OC}) ~ 30 mV under 532-nm laser excitation (Figure 12b). This initial polarity might be due to a slight poling effect by an applied voltage at the A electrode with the B electrode (grounded) during transfer curve measurement. To highlight the effect of mobile ion poling, negative ions are supposed to migrate to B electrode while the positive ions should migrate to A electrode (Figure 13a). After negative poling process, the output curves showed a completely opposite diode behavior compared to original condition in which the turn-on voltage becomes negative (Figure 13b). In addition, V_{OC} = -0.78 V was extracted under 532-nm laser excitation from the output curve, which represents the highest V_{OC} ever achieved in single-layer WSe_2 or other 2D semiconductor-based p-n junction devices.

To examine the controllability of this p-n junction formation, we have applied a positive bias voltage (V_{DS} = +10 V) to the same device at 400 K followed by the same cool down process as we previously used for negative poling (Figure 14a). The output characteristics indicated that V_{OC} is switched to +0.75 V under 532-nm laser illumination, which is very close to the previous result (-0.78 V) achieved by the negative poling process (Figure 14b). Such highly consistent and switchable diode behaviors demonstrate that the polarity of the $CH_3NH_3PbI_3/WSe_2$ diode is indeed governed by the controllable ion migration.

To elucidate the photocurrent contribution in the $CH_3NH_3PbI_3/WSe_2$ FET-based diode, we have examined the poling effect in both the $CH_3NH_3PbI_3/WSe_2$ device and the $CH_3NH_3PbI_3$ only

device. During poling process, the voltage was continuously applied to both A and C electrodes with the B electrode grounded. It is noted that the $CH_3NH_3PbI_3/WSe_2$ diode showed prominent rectification behavior under dark and laser excitation conditions in the output characteristics, while the $CH_3NH_3PbI_3$ only device showed negligible current and diode behavior under dark condition (Figure 15, a and b). This has demonstrated that the device current and diode behavior are mainly contributed by the WSe_2 channel instead of the $CH_3NH_3PbI_3$. The $CH_3NH_3PbI_3$ here is acting more like a sensitizer and a tunable doping agent rather than a conducting channel.

Optoelectronic property of $CH_3NH_3PbI_3/WSe_2$ diodes

In order to estimate the performance of the $CH_3NH_3PbI_3/WSe_2$ FETs, the time-domain photocurrent with zero bias voltage was measured (Figure 16, a and b). A zero-biased photocurrent, $I_{ph,hybrid}$ ~83.3 pA was obtained. Moreover, the external quantum efficiency (EQE) was further extracted by the formula:

$$\mathrm{EQE} = \left(\frac{I_{\mathrm{ph,hybrid}}}{P_{\mathrm{laser}}}\right)\left(\frac{hc}{e\lambda}\right) \quad (1)$$

where P_{laser} is the total effective power of incident photons, h, c and e are Planck's constant, the speed of light and electron charge, respectively. The extracted EQE of 84.3% at 532 nm is much higher than previously reported EQE of 0.2% at 522 nm in WSe_2 FET with split-gate defined p-n junction. Such strong enhancement could be due to strong optical absorption and long minority carrier diffusion distance in $CH_3NH_3PbI_3$, which can ensure the photo-generated carriers to reach the n-type region and p-type region in the atomically thin WSe_2 p-n junctions thereby enhancing the photoresponse of WSe_2.

Enhanced performance in graphene-contacted $CH_3NH_3PbI_3/WSe_2$ device

The above studies have clearly demonstrated that a switchable p-n junction can be created by selectively poling the $CH_3NH_3PbI_3$ layer. However, a single metal contact does not normally make optimized contacts to both n-type and p-type WSe_2 at the same time, thus one of the contacts could always be non-ideal and form a Schottky barrier to compromise the p-n diode effect. Therefore, to create a switchable junction with optimized diode characteristics, it is desired to have a tunable contact that can make excellent contacts to both n-type and p-type materials. Graphene has been recently demonstrated to be a promising contact material for MoS_2 FETs due to its tunable work functions which eliminate the contact barrier between graphene and MoS_2 as the device is in the ON state[38]. To further improve the performance of $CH_3NH_3PbI_3/WSe_2$ diode, we have investigated the device performance by using graphene as tunable electrical contacts. Unlike metal-based electrode, the work function of graphene can be tuned by not only gate bias voltage but also accumulated ions during the poling process, resulting in gate-tunable and preferable p-type (n-type) electrical contacts for p-type (n-type) region of WSe_2 channel.

The graphene-contacted device showed similar switchable p-n junction formation to the metal-contacted devices after the poling process (Figure 17, a and b). The device showed much larger gate tenability than the metal-contacted device, which may be due to effective work function modulation in graphene (Figure 19, a and b). In addition, the I_{DS}-V_{DS} curves under laser excitation exhibit a wide gate-tunable V_{OC} from 30 mV to 1.08 V after positive poling process (Figure 18a). On the other hand, the negatively poled device also showed a tunable V_{OC} from 0 to -0.96 V along with a widely tunable EQE from 2.7 to 91.3% (Figure 18b), demonstrating that the tunable graphene contact compared to metal electrodes allows more efficient extraction of photo-generated carriers as well as offering more tenability to better optoelectronic properties of the devices. It is important to note that the V_{OC} of ~1.0 V represents the highest V_{OC} ever achieved in WSe_2 or 2D

semiconductor, highlighting the excellent diode characteristics achieved in such ion-doped p-n junctions.

Room temperature volatility of programmed functions driven by $CH_3NH_3PbI_3$ ionic solids

In order to understand performance stability of the programmed p-n junction, the temperature of the sample was raised to 298 K, 350 K and 400 K. The measured V_{OC} decreased from -0.80 V (at 77 K) to -0.50 V (at 298 K), -0.35 V (at 350 K) and -0.30 V (at 400 K), indicating that the mobile ions in $CH_3NH_3PbI_3$ tend to be redistributed at high temperature and eliminate the internal electric field established at the junction (Figure 20). Moreover, this volatility was consistent with FET after the positive poling process which is a diode with opposite polarity. The V_{OC} dropped from +0.75 V to +0.60 V after heating up the sample stage to room temperature (Figure 21), which is similar to what we observed in the negatively poling (V_{OC} = -0.50 V at 298 K).

2.4. Conclusion

The $CH_3NH_3PbI_3/WSe_2$ FETs have been demonstrated to have an enhanced photoresponse because of greatly improved optical absorption with $CH_3NH_3PbI_3$ absorber. We have further employed $CH_3NH_3PbI_3$ as an efficient p-doping agent on MoS_2 and a controllable doping source on WSe_2 as well as demonstrating either a type-switchable FET or a switchable diode in the $CH_3NH_3PbI_3/WSe_2$ device by vertical or lateral electrical poling process, respectively. In the diode, it delivered a large V_{OC} up to 0.78 V with an EQE of 84.29% at 532 nm. Moreover, the hybrid device with graphene as electrical contact showed improved and gate-tunable optoelectronic properties with a V_{OC} up to 1.08 V under 532-nm laser excitation. Lastly, a widely tunable EQE from 2.7 to 91.3% has been achieved. With the ionic solid induced doping in 2D materials, we

could explore more intriguing electronic and optoelectronic properties of 2D materials with a much simpler device design as well as the enhanced optoelectronic properties with an ionic light absorber or emitter.

2.5. Figures and legends

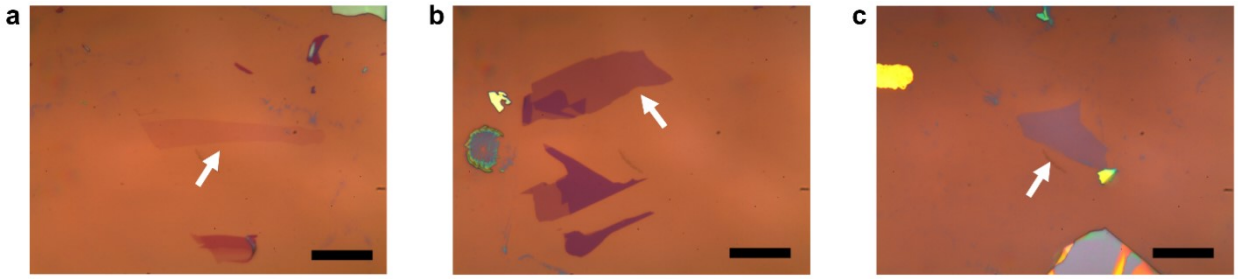

Figure 1. Preparation of 2D materials on SiO_2/Si wafer by mechanical exfoliation. **a**, graphene flake exfoliated from bulk graphite. **b**, exfoliated tungsten diselenide (WSe_2) flake. **c**, exfoliated hexagonal boron nitride (h-BN) flake. Scale bar, 20 μm.

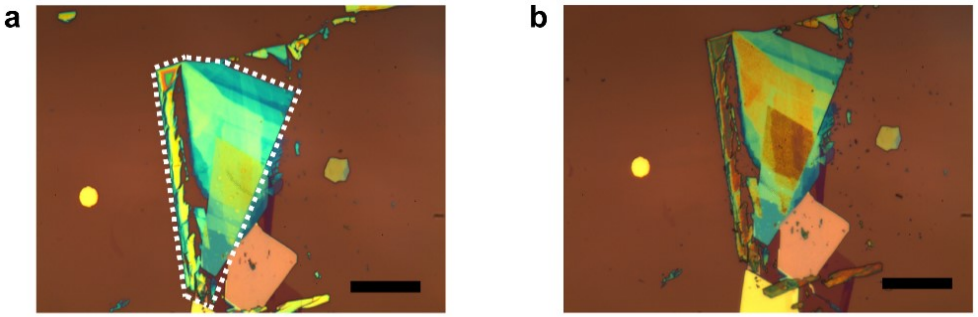

Figure 2. Optical images of vapor conversion from PbI_2 to $CH_3NH_3PbI_3$. **a**, The PbI_2 flake (inside white dotted line) was transferred on top of the prepared 2D materials. **b**, The PbI_2 flake was converted into $CH_3NH_3PbI_3$. Scale bar, 20 μm.

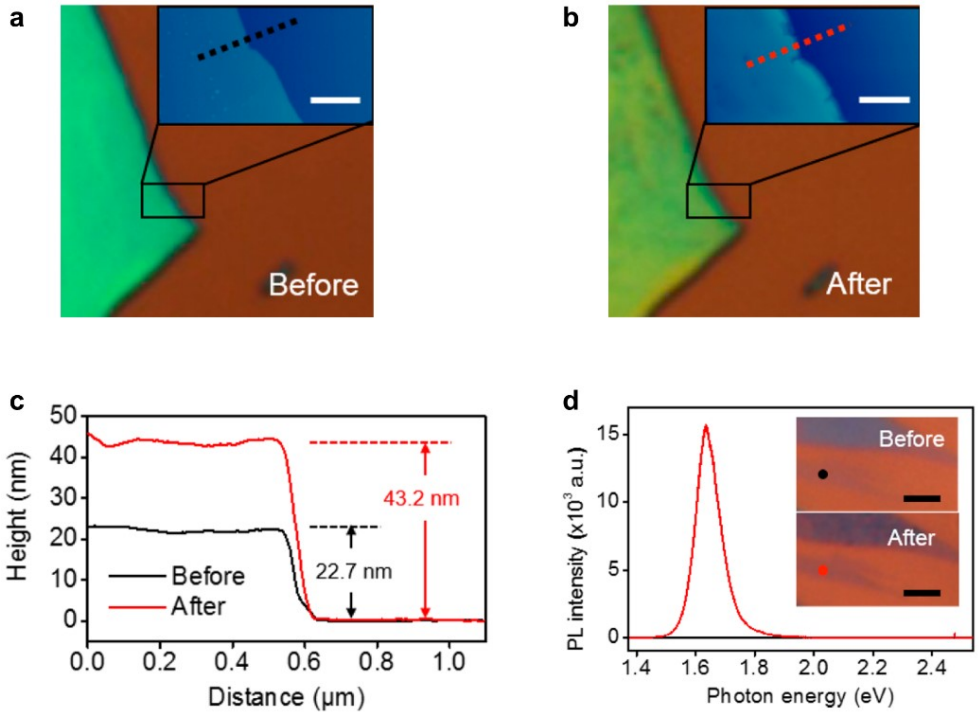

Figure 3. Conversion of exfoliated PbI_2 flake into $CH_3NH_3PbI_3$. a,**b**, The optical images of an exfoliated PbI_2 flake before and after conversion process. Inset: Atomic force microscopy (AFM) images of the area marked by black boxes in the optical images. Scale bar, 500 nm. **c**, The sectional height profile extracted from black and red dotted lines from the insets of (**a**) and (**b**), showing increased thickness of the identical sample after the vapor conversion. **d**, Photoluminescence (PL) spectra taken from black and red spots shown in insets (optical images). A prominent emission peak at 1.63 eV was observed after the conversion demonstrating that PbI_2 was completely converted to $CH_3NH_3PbI_3$.

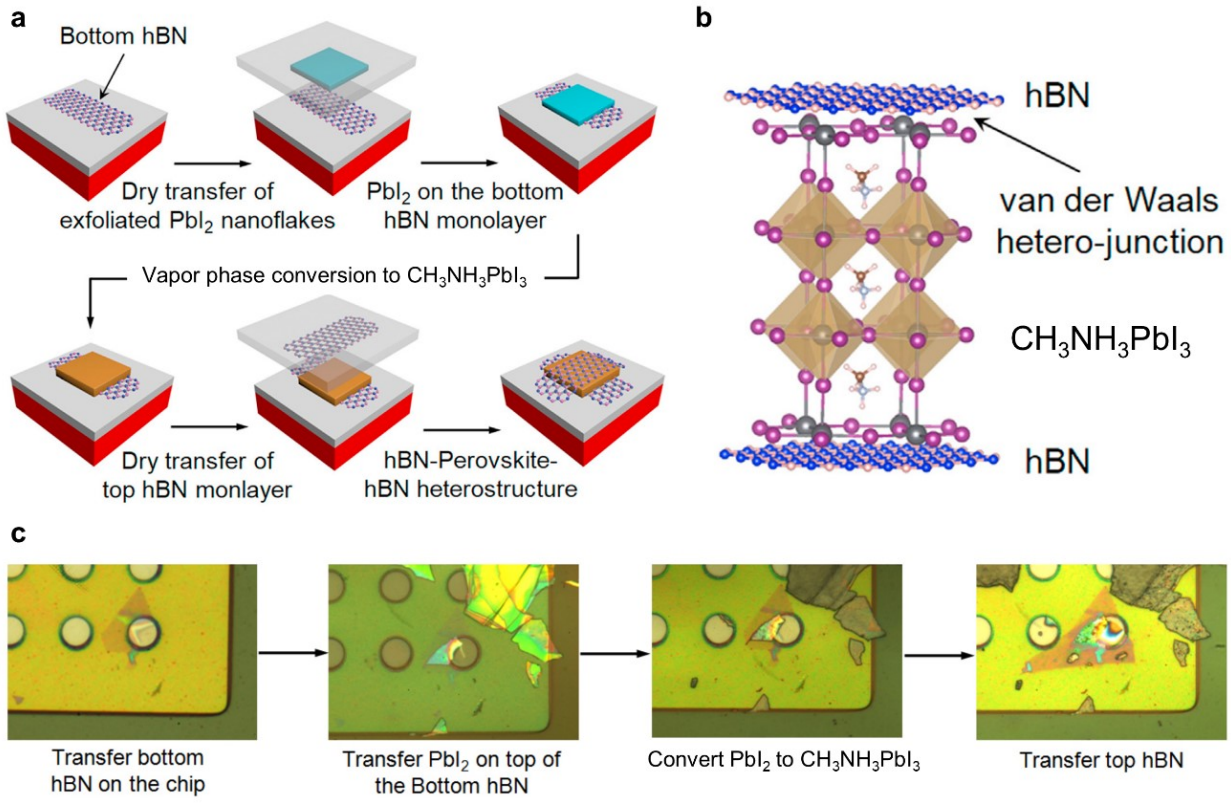

Figure 4. h-BN/$CH_3NH_3PbI_3$/h-BN heterostructure and fabrication process. a, Schematic illustrations of fabrication process of the heterostructure. **b**, Schematic illustration of h-BN/$CH_3NH_3PbI_3$/h-BN heterostructure. **c**, Optical image of the heterostructure on *in situ* TEM grid (silicon nitride).

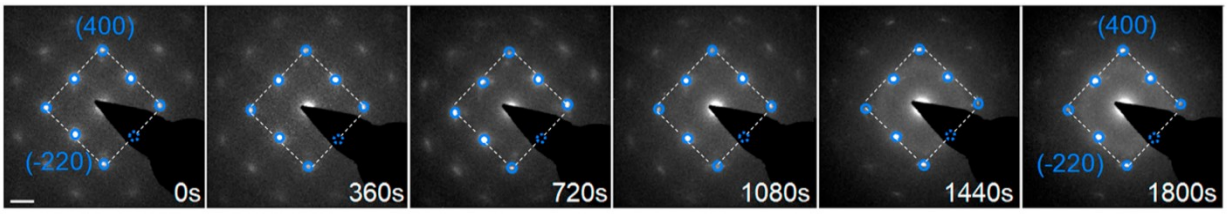

Figure 5. *in situ* TEM measurements of $CH_3NH_3PbI_3$ with h-BN surface protection. $CH_3NH_3PbI_3$ with h-BN surface protection showed robust thermal stability. The thermal energy (85 ℃ in vacuum) has not affected the crystalline structure of the $CH_3NH_3PbI_3$ in 30 min of heating. Scale bar, 2 nm^{-1}.

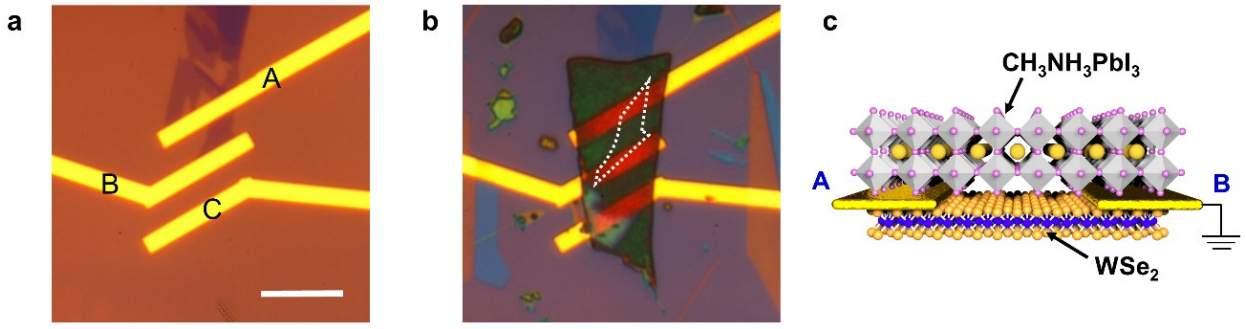

Figure 6. Structural configurations of single-layer WSe_2, $CH_3NH_3PbI_3$ and $CH_3NH_3PbI_3/WSe_2$ FETs. a, Optical image of as-fabricated single-layer WSe_2 FET device. A, C electrodes were used for drain electrode and B electrode was used for source electrode which was grounded. Scale bar, 10 μm. **b**, Optical image taken after $CH_3NH_3PbI_3$ integration and h-BN encapsulation. The white dashed lines frame the position of single-layer WSe_2. **c**, Schematic illustration of a $CH_3NH_3PbI_3/WSe_2$ FET.

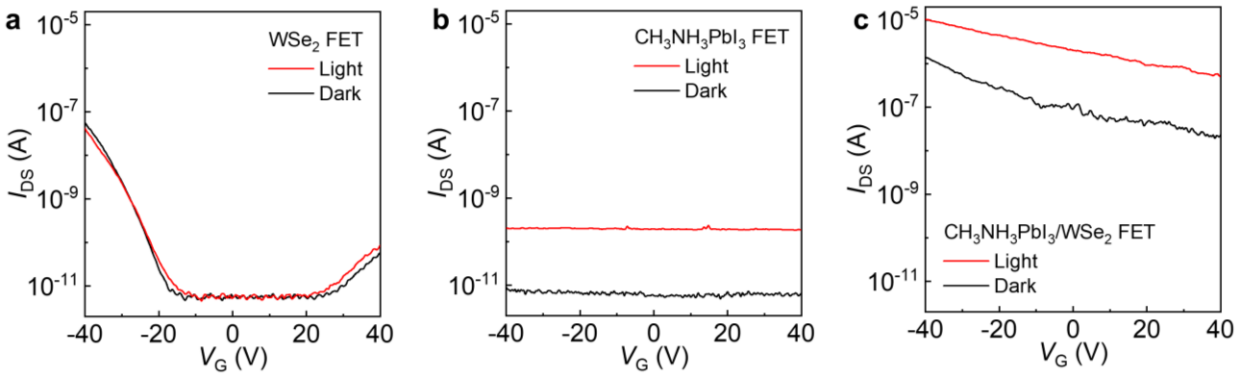

Figure 7. Device properties of single-layer WSe_2, $CH_3NH_3PbI_3$ and $CH_3NH_3PbI_3/WSe_2$ FETs. **a**, Transfer characteristics of WSe_2 only FET measured under light illumination and dark. **b**, Transfer characteristics of $CH_3NH_3PbI_3$ only FET measured under light illumination and dark. **c**, Transfer characteristics of $CH_3NH_3PbI_3/WSe_2$ FET measured under light illumination and dark. All the measurements were conducted under V_{DS} = 5 V.

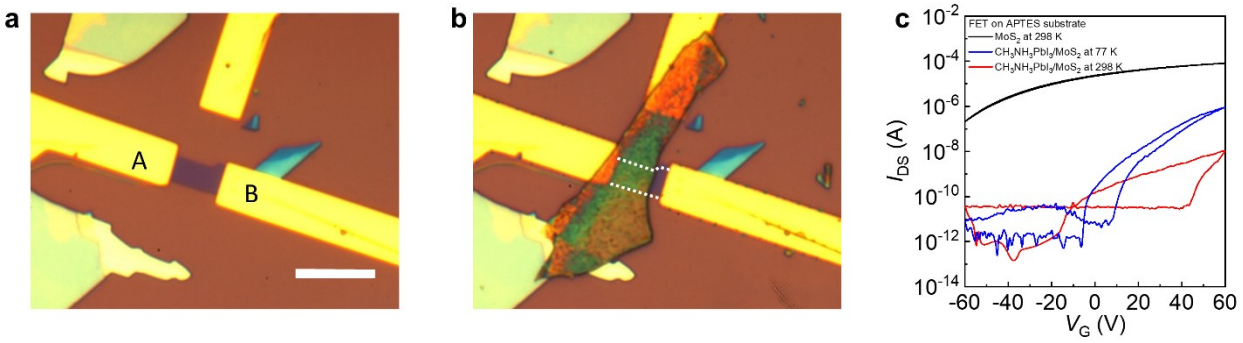

Figure 8. Doping effect of $CH_3NH_3PbI_3$ in a $CH_3NH_3PbI_3/MoS_2$ device. a,**b**, Optical images of a single-layer MoS_2 FET (**a**) and the FET with $CH_3NH_3PbI_3$ on top (**b**). Scale bar, 10 μm. **c**, Logarithmic plot of transfer characteristics measured at room temperature (black and red lines) and low temperature (blue line).

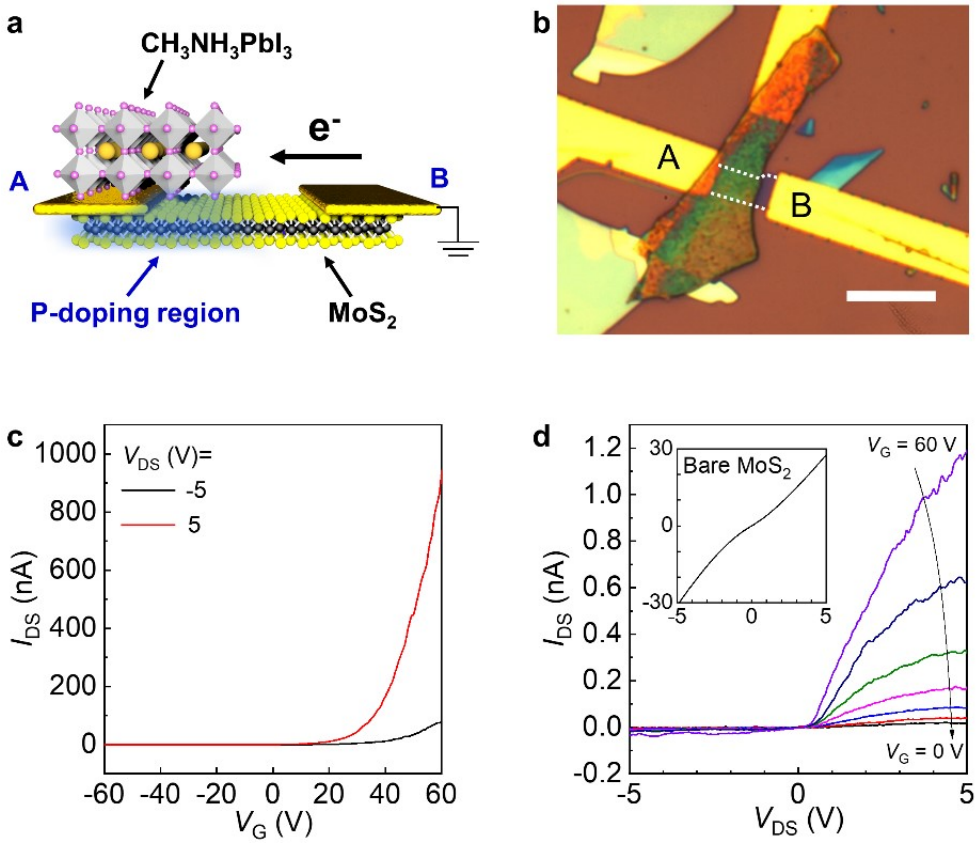

Figure 9. Device properties of a partially doped MoS_2 FET. a, Schematic illustration of a partially doped MoS_2 FET. A electrode was used as drain electrode and B electrode was used as source electrode which was grounded. **b**, Optical image of a single-layer MoS_2 FET partially covered by a $CH_3NH_3PbI_3$ flake. A electrode was used as drain electrode and B electrode was used as source electrode. Scale bar, 10 μm. **c**, Negatively (V_{DS} = -5 V) and positively (V_{DS} = 5 V) biased transfer curves measured under dark condition at 77 K. **d**, Output characteristics measured at room temperature, showing larger gate tunability at positive bias voltages ($0 \leq V_G \leq 60$ V). Inset: the diode-like characteristics in (**d**) showed distinct contrast compared to the same device without $CH_3NH_3PbI_3$ measured before integration.

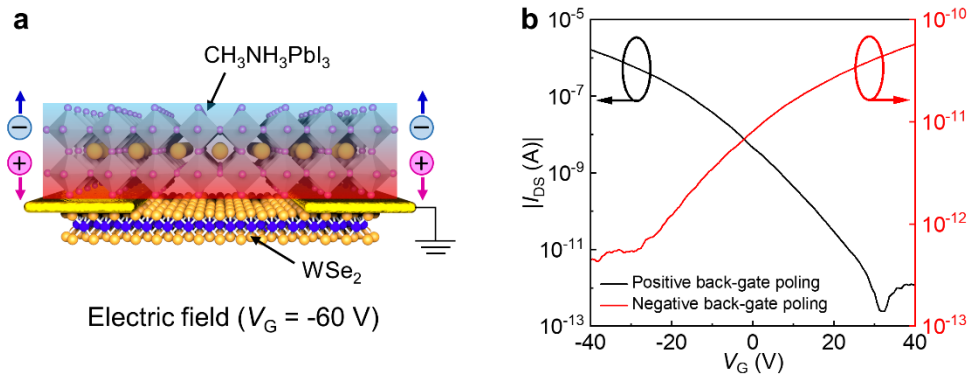

Figure 10. Gate-controlled ionic doping in $CH_3NH_3PbI_3/WSe_2$ FET. a, Schematic illustration of vertical negative poling process in a $CH_3NH_3PbI_3/WSe_2$ FET. **b**, Transfer curves after positive (black line) and negative (red line) back-gate poling process measured at V_{DS} = 5 V. All the curves were measured under dark condition at 77 K.

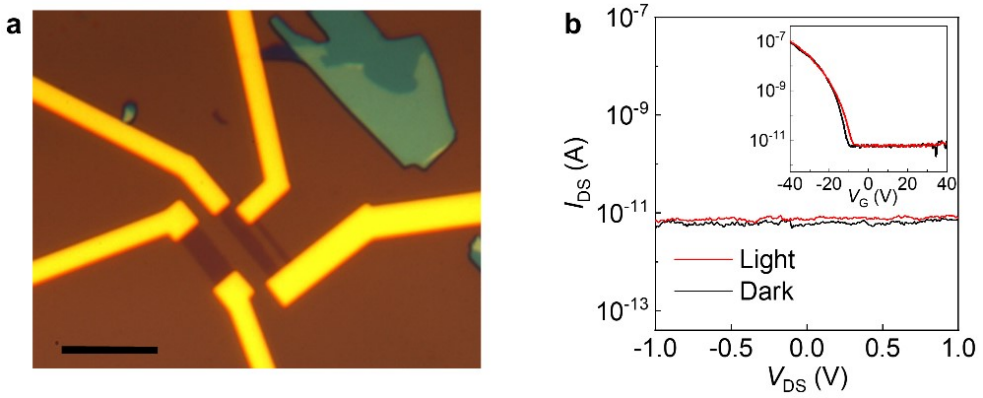

Figure 11. Device properties of a single-layer WSe_2 FET before $CH_3NH_3PbI_3$ integration. a, Optical image of a single-layer WSe_2 FET. **b**, Output characteristics of the device shown in (**a**) measured under light illumination (red line) and dark (black line). Inset: Transfer characteristics of the corresponding device.

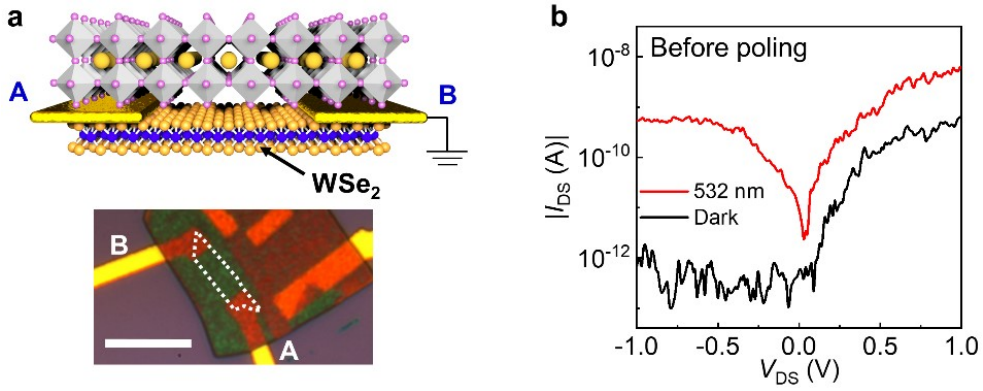

Figure 12. Characteristics of as-fabricated $CH_3NH_3PbI_3/WSe_2$ FET. a, Schematic illustration and optical image of $CH_3NH_3PbI_3/WSe_2$ FETs. Scale bar, 10 μm. **b**, Output characteristics of the FET before poling process measured under 532-nm laser illumination and dark conditions. All the measurements were measured at 77 K after poling processes.

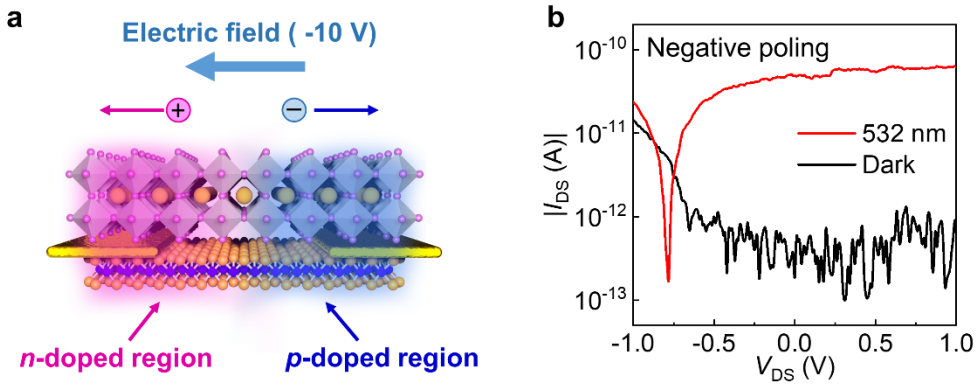

Figure 13. Negatively poled $CH_3NH_3PbI_3/WSe_2$ FET-based diode. a, Schematic illustration of non-uniform negative poling process. During the application of negative bias voltage, cations in the $CH_3NH_3PbI_3$ flake are supposed to be accumulated near the biased electrode. **b**, Output characteristics of the FET after the negative poling process measured under 532-nm laser illumination and dark conditions. All the measurements were conducted at 77 K.

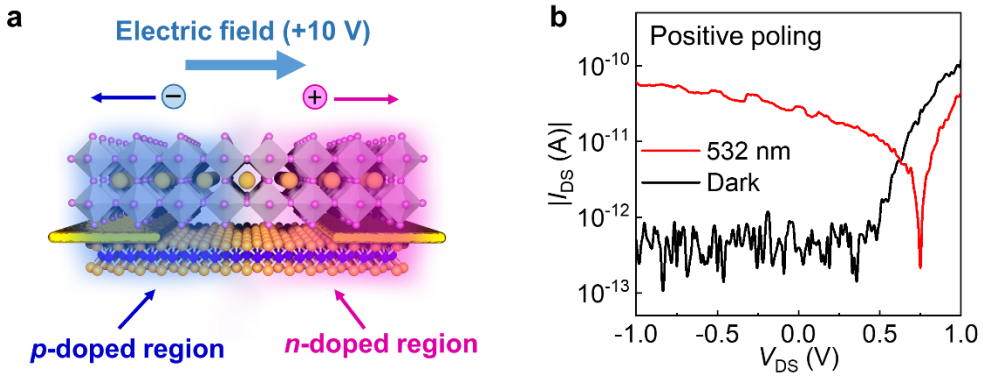

Figure 14. Positively poled $CH_3NH_3PbI_3/WSe_2$ FET-based diode. a, Schematic illustration of non-uniform positive poling process. During the application of positive bias voltage, cations in the $CH_3NH_3PbI_3$ flake are supposed to be pushed away and accumulated near the grounded electrode. **b**, Output characteristics of the FET after the positive poling process measured under 532-nm laser illumination and dark conditions, demonstrating that previous negative V_{OC} was changed to positive one. All the measurements were conducted at 77 K.

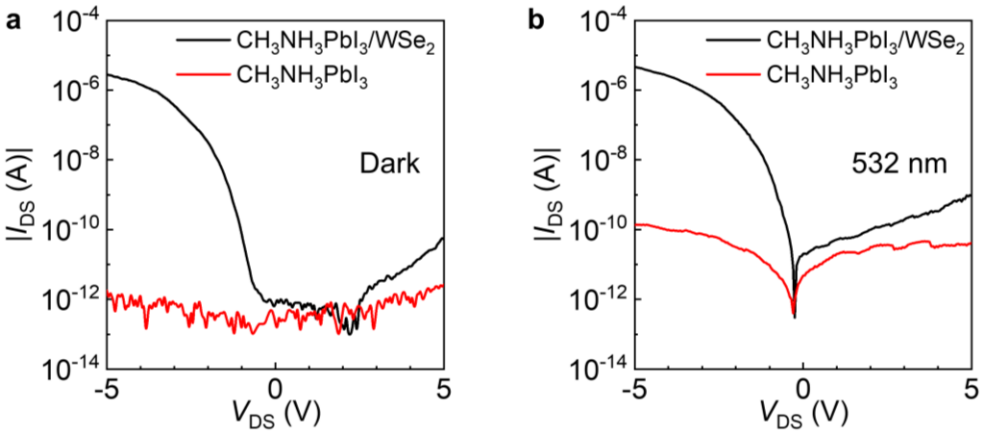

Figure 15. Comparison between the negatively poled $CH_3NH_3PbI_3/WSe_2$ FET and $CH_3NH_3PbI_3$ only FET. a, Output characteristics of $CH_3NH_3PbI_3/WSe_2$ FET and $CH_3NH_3PbI_3$ FET measured after negative poling process under dark condition. **b**, Output characteristics of $CH_3NH_3PbI_3/WSe_2$ FET and $CH_3NH_3PbI_3$ FET measured after negative poling process under 532-nm laser illumination. The diode behaviors were prominent with WSe_2 layer.

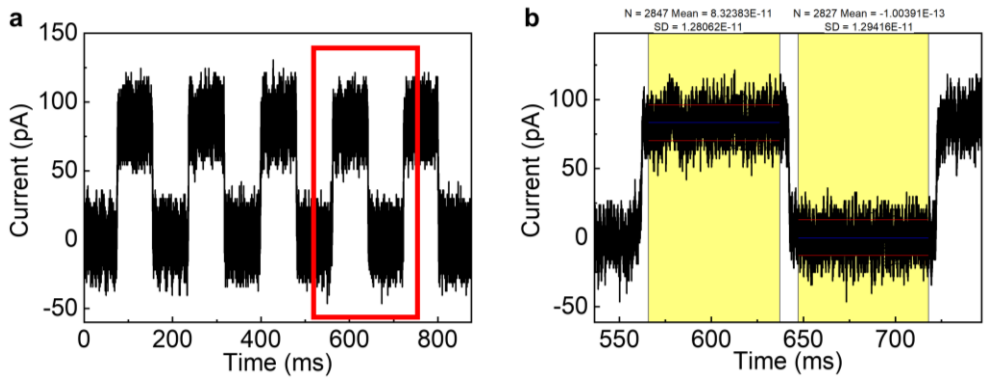

Figure 16. Time-domain photoresponse of $CH_3NH_3PbI_3/WSe_2$ FET after negative poling process (V_{DS} = -10 V). a, Time-domain photoresponse was measured with 532-nm laser illumination with a chopping frequency of 7 Hz. **b**, Photocurrent change at the time scale in the red box in (**a**), which was estimated from the mean value of the current steps during ON and OFF states under V_{DS} = 0 V.

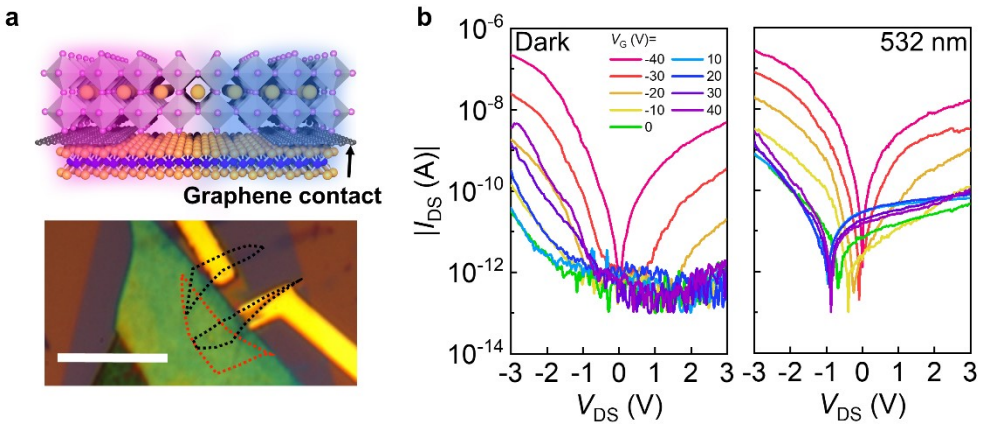

Figure 17. Gate tunable and switchable p-n junction in graphene-contacted $CH_3NH_3PbI_3/WSe_2$ FET. a, Schematic illustration and optical image of a graphene-contacted $CH_3NH_3PbI_3/WSe_2$ FET. The black and red dashed lines frame the position of graphene and WSe_2, respectively. Scale bar, 10 μm. **b**, Semi-logarithmic plot of gate-dependent output curves measured after negative poling process under dark (left panel) and 532-nm laser illumination (right panel) at 77 K.

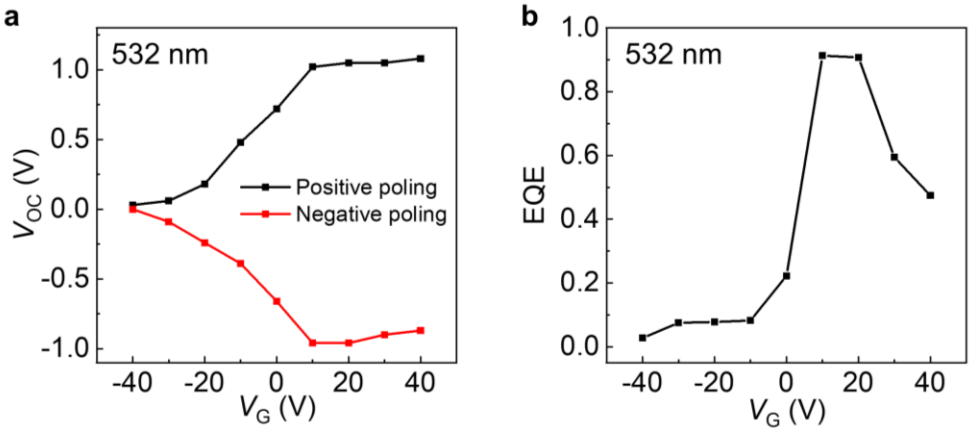

Figure 18. Optoelectronic properties of gate tunable graphene-contacted $CH_3NH_3PbI_3/WSe_2$ FET. a, Open-circuit voltage (V_{OC}) extracted from the I_{DS}-V_{DS} curves of the diode measured after

positive (black) and negative (red) poling process. **b**, External quantum efficiency (EQE) extracted from the gate-dependent short circuit current (I_{SC}) measured under 532-nm laser illumination after negative poling process.

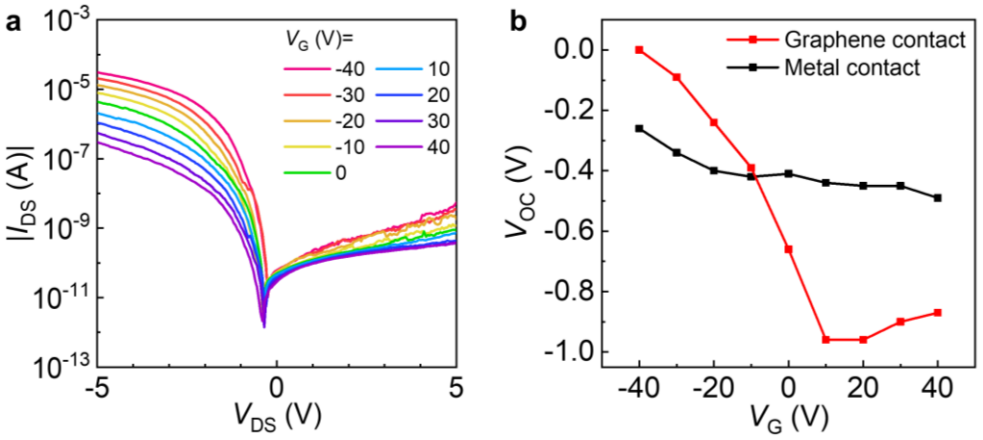

Figure 19. Enhanced gate-tunable photovoltaic effect with graphene contacts. a, Gate-dependent output curves of a negatively poled $CH_3NH_3PbI_3$ with Cr/Au metal contacts. **b**, Comparison of gate-dependent V_{OC} in the negatively poled $CH_3NH_3PbI_3$ diode with metal contact (black line) and graphene contact (red line).

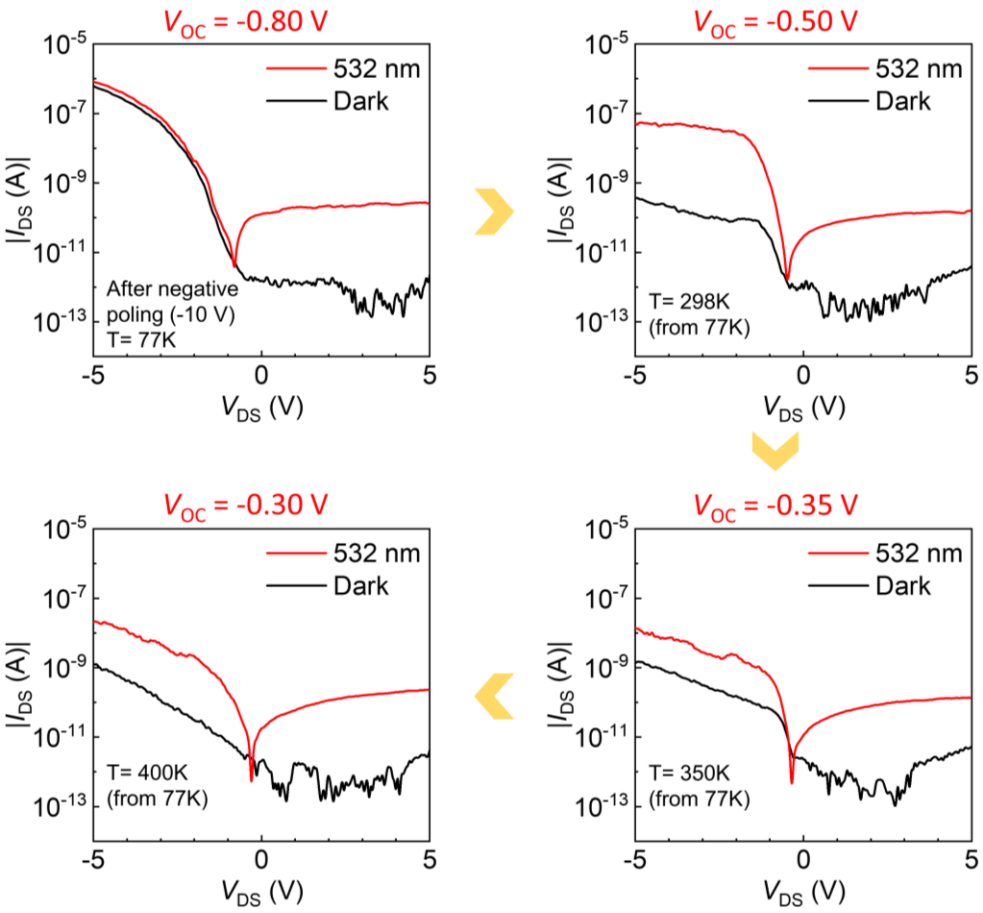

Figure 20. Thermal stability of the negatively poled $CH_3NH_3PbI_3/WSe_2$ FET-based diode. Output characteristics of a negatively poled $CH_3NH_3PbI_3/WSe_2$ diode were measured under 532-nm laser illumination and dark conditions. As the temperature of sample stage increased from 77 K to 400 K, the open-circuit voltage (V_{OC}) decreased from -0.80 V to -0.30 V. The sequential process steps are indicated by yellow arrows.

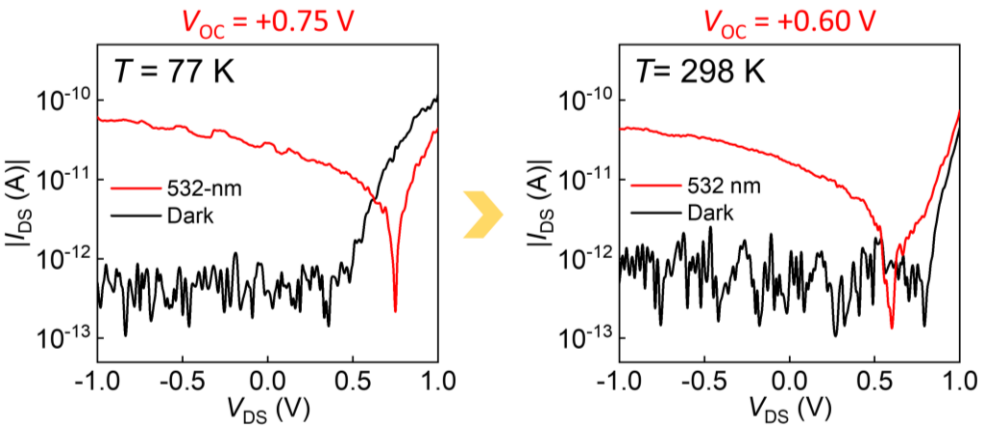

Figure 21. Thermal stability of programmed functions of the positively poled $CH_3NH_3PbI_3/WSe_2$ FET-based diode. The V_{OC} decreased from 0.75 V (at 77 K) to 0.60 V (at 298 K). The sequential process steps are indicated by yellow arrows.

2.6. References

1. Baugher, B. W. H.; Churchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P., Optoelectronic devices based on electrically tunable p-n diodes in a monolayer dichalcogenide. *Nature Nanotechnology* **2014**, 9, 262-267.

2. Zhang, Y. J.; Ye, J. T.; Yomogida, Y.; Takenobu, T.; Iwasa, Y., Formation of a Stable p–n Junction in a Liquid-Gated MoS2 Ambipolar Transistor. *Nano Letters* **2013**, 13, 3023-3028.

3. Ross, J. S.; Klement, P.; Jones, A. M.; Ghimire, N. J.; Yan, J.; Mandrus, D. G.; Taniguchi, T.; Watanabe, K.; Kitamura, K.; Yao, W.; Cobden, D. H.; Xu, X., Electrically tunable excitonic light-emitting diodes based on monolayer WSe2 p-n junctions. *Nature Nanotechnology* **2014**, 9, 268-272.

4. Pospischil, A.; Furchi, M. M.; Mueller, T., Solar-energy conversion and light emission in an atomic monolayer p-n diode. *Nature Nanotechnology* **2014**, 9, 257-261.

5. Williams, J. R.; DiCarlo, L.; Marcus, C. M., Quantum Hall Effect in a Gate-Controlled p-n Junction of Graphene. *Science* **2007**, 317, 638.

6. Choi, J.-H.; Lee, G.-H.; Park, S.; Jeong, D.; Lee, J.-O.; Sim, H. S.; Doh, Y.-J.; Lee, H.-J., Complete gate control of supercurrent in graphene p–n junctions. *Nature Communications* **2013**, 4, 2525.

7. Gabor, N. M.; Zhong, Z.; Bosnick, K.; Park, J.; McEuen, P. L., Extremely Efficient Multiple Electron-Hole Pair Generation in Carbon Nanotube Photodiodes. *Science* **2009**, 325, 1367.

8. Zhang, Y. J.; Oka, T.; Suzuki, R.; Ye, J. T.; Iwasa, Y., Electrically Switchable Chiral Light-Emitting Transistor. *Science* **2014**, 344, 725.

9. Mueller, T.; Kinoshita, M.; Steiner, M.; Perebeinos, V.; Bol, A. A.; Farmer, D. B.; Avouris, P., Efficient narrow-band light emission from a single carbon nanotube p-n diode. *Nature Nanotechnology* **2010**, 5, 27-31.

10. Sundaram, R. S.; Engel, M.; Lombardo, A.; Krupke, R.; Ferrari, A. C.; Avouris, P.; Steiner, M., Electroluminescence in Single Layer MoS2. *Nano Letters* **2013**, 13, 1416-1421.

11. Gabor, N. M.; Song, J. C. W.; Ma, Q.; Nair, N. L.; Taychatanapat, T.; Watanabe, K.; Taniguchi, T.; Levitov, L. S.; Jarillo-Herrero, P., Hot Carrier–Assisted Intrinsic Photoresponse in Graphene. *Science* **2011**, 334, 648.

12. Bae, S.-H.; Kahya, O.; Sharma, B. K.; Kwon, J.; Cho, H. J.; Ozyilmaz, B.; Ahn, J.-H., Graphene-P (VDF-TrFE) multilayer film for flexible applications. *ACS nano* **2013**, 7, 3130-3138.

13. Dong, Q.; Fang, Y.; Shao, Y.; Mulligan, P.; Qiu, J.; Cao, L.; Huang, J., Electron-hole diffusion lengths > 175 μm in solution-grown CH3NH3PbI3 single crystals. *Science* **2015**, 347, 967.

14. De Wolf, S.; Holovsky, J.; Moon, S.-J.; Löper, P.; Niesen, B.; Ledinsky, M.; Haug, F.-J.; Yum, J.-H.; Ballif, C., Organometallic Halide Perovskites: Sharp Optical Absorption Edge and Its Relation to Photovoltaic Performance. *The Journal of Physical Chemistry Letters* **2014**, 5, 1035-1039.

15. Lee, M. M.; Teuscher, J.; Miyasaka, T.; Murakami, T. N.; Snaith, H. J., Efficient Hybrid Solar Cells Based on Meso-Superstructured Organometal Halide Perovskites. *Science* **2012**, 338, 643.

16. Stranks, S. D.; Eperon, G. E.; Grancini, G.; Menelaou, C.; Alcocer, M. J. P.; Leijtens, T.; Herz, L. M.; Petrozza, A.; Snaith, H. J., Electron-Hole Diffusion Lengths Exceeding 1 Micrometer in an Organometal Trihalide Perovskite Absorber. *Science* **2013**, 342, 341.

17. Yang, W. S.; Noh, J. H.; Jeon, N. J.; Kim, Y. C.; Ryu, S.; Seo, J.; Seok, S. I., High-performance photovoltaic perovskite layers fabricated through intramolecular exchange. *Science* **2015**, 348, 1234.

18. Cheng, H.-C.; Wang, G.; Li, D.; He, Q.; Yin, A.; Liu, Y.; Wu, H.; Ding, M.; Huang, Y.; Duan, X., van der Waals Heterojunction Devices Based on Organohalide Perovskites and Two-Dimensional Materials. *Nano Letters* **2016**, 16, 367-373.

19. Jeon, N. J.; Noh, J. H.; Yang, W. S.; Kim, Y. C.; Ryu, S.; Seo, J.; Seok, S. I., Compositional engineering of perovskite materials for high-performance solar cells. *Nature* **2015**, 517, 476-480.

20. Son, D.-Y.; Lee, J.-W.; Choi, Y. J.; Jang, I.-H.; Lee, S.; Yoo, P. J.; Shin, H.; Ahn, N.; Choi, M.; Kim, D., Self-formed grain boundary healing layer for highly efficient CH3 NH3 PbI3 perovskite solar cells. *Nature Energy* **2016**, 1, 16081.

21. Dou, L.; Yang, Y.; You, J.; Hong, Z.; Chang, W.-H.; Li, G.; Yang, Y., Solution-processed hybrid perovskite photodetectors with high detectivity. *Nature Communications* **2014**, 5, 5404.

22. Cho, H.; Jeong, S.-H.; Park, M.-H.; Kim, Y.-H.; Wolf, C.; Lee, C.-L.; Heo, J. H.; Sadhanala, A.; Myoung, N.; Yoo, S.; Im, S. H.; Friend, R. H.; Lee, T.-W., Overcoming the electroluminescence efficiency limitations of perovskite light-emitting diodes. *Science* **2015**, 350, 1222.

23. Veldhuis, S. A.; Boix, P. P.; Yantara, N.; Li, M.; Sum, T. C.; Mathews, N.; Mhaisalkar, S. G., Perovskite Materials for Light-Emitting Diodes and Lasers. *Advanced Materials* **2016**, 28, 6804-6834.

24. Brenner, T. M.; Egger, D. A.; Kronik, L.; Hodes, G.; Cahen, D., Hybrid organic—inorganic perovskites: low-cost semiconductors with intriguing charge-transport properties. *Nature Reviews Materials* **2016**, 1, 15007.

25. Miyano, K.; Yanagida, M.; Tripathi, N.; Shirai, Y., Hysteresis, Stability, and Ion Migration in Lead Halide Perovskite Photovoltaics. *The Journal of Physical Chemistry Letters* **2016**, 7, 2240-2245.

26. Levine, I.; Nayak, P. K.; Wang, J. T.-W.; Sakai, N.; Van Reenen, S.; Brenner, T. M.; Mukhopadhyay, S.; Snaith, H. J.; Hodes, G.; Cahen, D., Interface-Dependent Ion Migration/Accumulation Controls Hysteresis in MAPbI3 Solar Cells. *The Journal of Physical Chemistry C* **2016**, 120, 16399-16411.

27. Li, C.; Tscheuschner, S.; Paulus, F.; Hopkinson, P. E.; Kießling, J.; Köhler, A.; Vaynzof, Y.; Huettner, S., Iodine Migration and its Effect on Hysteresis in Perovskite Solar Cells. *Advanced Materials* **2016**, 28, 2446-2454.

28. Eames, C.; Frost, J. M.; Barnes, P. R. F.; O'Regan, B. C.; Walsh, A.; Islam, M. S., Ionic transport in hybrid lead iodide perovskite solar cells. *Nature Communications* **2015**, 6, 7497.

29. Meloni, S.; Moehl, T.; Tress, W.; Franckevičius, M.; Saliba, M.; Lee, Y. H.; Gao, P.; Nazeeruddin, M. K.; Zakeeruddin, S. M.; Rothlisberger, U.; Graetzel, M., Ionic polarization-induced current–voltage hysteresis in CH3NH3PbX3 perovskite solar cells. *Nature Communications* **2016**, 7, 10334.

30. Xiao, Z.; Yuan, Y.; Shao, Y.; Wang, Q.; Dong, Q.; Bi, C.; Sharma, P.; Gruverman, A.; Huang, J., Giant switchable photovoltaic effect in organometal trihalide perovskite devices. *Nature materials* **2015**, 14, 193.

31. Wang, G.; Li, D.; Cheng, H.-C.; Li, Y.; Chen, C.-Y.; Yin, A.; Zhao, Z.; Lin, Z.; Wu, H.; He, Q.; Ding, M.; Liu, Y.; Huang, Y.; Duan, X., Wafer-scale growth of large arrays of perovskite microplate crystals for functional electronics and optoelectronics. *Science Advances* **2015**, 1.

32. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A., Electric field effect in atomically thin carbon films. *science* **2004**, 306, 666-669.

33. Withers, F.; Del Pozo-Zamudio, O.; Mishchenko, A.; Rooney, A.; Gholinia, A.; Watanabe, K.; Taniguchi, T.; Haigh, S.; Geim, A.; Tartakovskii, A., Light-emitting diodes by band-structure engineering in van der Waals heterostructures. *Nature materials* **2015**, 14, 301.

34. Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X., Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature* **2018**, 1.

35. Jain, S. M.; Philippe, B.; Johansson, E. M.; Park, B.-w.; Rensmo, H.; Edvinsson, T.; Boschloo, G., Vapor phase conversion of PbI 2 to CH 3 NH 3 PbI 3: spectroscopic evidence for formation of an intermediate phase. *Journal of Materials Chemistry A* **2016**, 4, 2630-2642.

36. Fan, Z.; Xiao, H.; Wang, Y.; Zhao, Z.; Lin, Z.; Cheng, H.-C.; Lee, S.-J.; Wang, G.; Feng, Z.; Goddard III, W. A., Layer-by-layer degradation of methylammonium lead tri-iodide perovskite microplates. *Joule* **2017**, 1, 548-562.

37. Wang, Q.; Chen, B.; Liu, Y.; Deng, Y.; Bai, Y.; Dong, Q.; Huang, J., Scaling behavior of moisture-induced grain degradation in polycrystalline hybrid perovskite thin films. *Energy & Environmental Science* **2017**, 10, 516-522.

38. Liu, Y.; Wu, H.; Cheng, H.-C.; Yang, S.; Zhu, E.; He, Q.; Ding, M.; Li, D.; Guo, J.; Weiss, N. O., Toward barrier free contact to molybdenum disulfide using graphene electrodes. *Nano letters* **2015**, 15, 3030-3034.

Chapter 3. Electrostatic Doping Effects of Silver Iodide on Two-Dimensional Semiconductor

3.1. Introduction

In previous chapter, we showed that positive and negative ions in the organic-inorganic hybrid perovskite ($CH_3NH_3PbI_3$) can electrostatically modulate the carrier density in ambipolar WSe_2 devices to realize a diode. Although somewhat enhancing compatibility with solid-state electronic device applications, such solid-state perovskite-induced diodes can only be non-volatile at cryogenic temperature by freezing the ion motion, which still does not resolve the volatility issue for split-gate induced doping (Figure 20 and Figure 21).

In general, to enable programmable and stable operating logic functions, three critical factors must be considered: (i) the temperature used for programming device functions; (ii) the operating temperature; and (iii) functional stability at the operating temperature. Furthermore, for integrated circuit (IC) applications, the typical operating condition and thermal budget of the ICs should also be considered. According to the guideline from the Intel's CPU product[1], most CPUs experience an operating temperature under 100 ˚C (typically 45 to 70 ˚C during normal operation). For programming temperature, although most ICs have a typical front-end of line (FEOL) processing tolerance of 550 ˚C (ref. [2]) and back-end of line (BEOL) processing tolerance of 440 ˚C (ref. [3]), the maximum programming temperature is limited by the glass transition temperature T_g of the typical commercial plastic package (~175 ˚C) (ref. [4]).

Because of these temperature constraints, the devices need to be programmed below 175 ˚C (ref. [2-4]) and also retain the programmed functions at temperature up to 100 ˚C (ref. [1]). This requires a large change in ionic conductance within a rather narrow temperature window (100-175 ˚C) to ensure efficient programming and stable operation. This combination is difficult to achieve with

ionic liquids/solids in which the ion movement is governed by thermal activation process, following the Arrhenius relationship:

$$\sigma_{\text{ion}} = \text{A}e^{-E_a/\text{k}_\text{B}T} \quad (1)$$

where σ_{ion} is the ionic conductivity, A is the pre-exponential factor, E_a is the activation energy, k_B is the Boltzmann constant and T is the absolute temperature. With Arrhenius behavior, the ionic conductance in ionic liquids/solids is fundamentally determined by the activation energy and temperature. Thus, the values are either too low to allow sufficient programmability at a reasonable temperature (due to large activation energy) or too high to ensure stable operation of the programmed function at room temperature. It is thus fundamentally challenging to use conventional ionic liquids/solids to simultaneously achieve the programmability and operation stability within the narrow temperature window identified here. In this regard, no previous approaches (mobile ion in glass, typical superionics or ionic liquids) can satisfy these requirements for typical IC operation conditions (Figure 22) as detailed below.

The mobile Na^+ in soda-lime glass

Soda-lime glass is one of the typical ionic solids which has an ion activation energy $E_a = 1.654$ eV (ref. [5]) and shows very low ionic conductivity even at the maximum thermal budget of typical back-end packaging (175 ˚C) (Figure 22, green line). Such a low ionic conductivity would require impractically long times for programming the desired logic functions. To achieve the ionic conductivity comparable to superionic AgI at 147 ˚C (~1 S/cm), the soda-lime glass needs to be heated to 935 ˚C (ΔT = 910 ˚C) far above thermal budget of plastic packaging (maximum 175 ˚C) (ref. [4]) or even the typical FEOL processing tolerance (maximum 550 ˚C) (ref. [2]) and BEOL processing tolerance (maximum 400 ˚C) (ref. [3]).

LaF_3 and diethylmethyl(2-methoxyethyl)ammonium bis(trifluoromethylsulfonyl)imide (DEME-TFSI)

Typical superionic solids (e.g. LaF_3) and ionic liquids (e.g. DEME-TFSI) often possess too high of an ionic conductance[6-8] to maintain an ionic doping layer without the constant presence of an electric field at reasonable operating conditions (Figure 22, black and blue line). Additionally, because of their low activation energy (0.1-0.5 eV), it is fundamentally challenging to achieve a sufficient ionic conductance ratio within the required temperature window. For example, the ionic conductivity of LaF_3 at 160 ˚C (~4.35 S/cm) is only ~50 times higher than that of room temperature (~0.09 S/cm) (ref. [9]) (Figure 22). Based on the Arrhenius equation, to achieve the ionic conductance ratio $>10^3$, superionic LaF_3 needs to be heated from room temperature to about 369 ˚C (ΔT = 344 ˚C) far above the maximum thermal budget of typical plastic-encapsulated devices (175 ˚C). It is also noted that the conductance ratio of 10^5 is practically not achievable since LaF_3 will melt before achieving ~10^4 S/cm.

To bypass such limitations, superionic solids with a sharp solid-state phase transition are attractive candidates for achieving a large change in ionic conductance within the narrow temperature window that is necessary to obtain efficient programmability at moderate temperature and operational stability at room temperature. Unlike ionic liquids, the superionic solids offer a local control of the doping on 2D materials that is critical for diverse designs for solid-state electronics. Among superionic solids, silver iodide (AgI) is particularly desirable for its unique superionic phase transition behavior[10]. At room temperature, it adopts a beta-polymorph (β-AgI) and behaviors as an insulating dielectric. Upon reaching 147 ˚C, it transits into the alpha-polymorph (α-AgI), also known as the superionic conduction phase, with a sharp increase in ionic conductance by $>10^3$ (ref. [10]). Overall, an ionic conductance ratio greater than five-order of

magnitude can be achieved from room temperature to switching temperature at 147 ˚C. Such a solid-state superionic phase transition and the associated sharp change in ionic conductance, occurring in the right temperature window, is well suited for ensuring the efficient programmability and stable operation of the programmed functions.

In this chapter, we mainly focus on a solid-state non-volatile doping approach to 2D semiconductors adopting the phase transition of superionic AgI. The atomically thin 2D semiconductor channel ensures efficient coupling with superionics to induce dynamically switchable, non-volatile n-type or p-type doping, producing a new class of reversibly programmable devices that can function as transistor or diodes with tunable carrier type and device polarity. We constructed functional 2D complementary logic gates including inverters, NAND and NOR gates, demonstrating a promising pathway to 2D complementary logic circuits.

3.2. Experimental section

Fabrication of WSe_2 field-effect transistor

The sacrificial SiO_2/Si wafers were first cleaned with oxygen plasma for 5 minutes. A pair of few-layer graphene flakes, a single-/few-layer WSe_2 flake, and a few-layer h-BN flake were mechanically exfoliated on top of the pre-cleaned SiO_2/Si wafer. Another few-layer h-BN flake for the top h-BN dielectric were mechanically exfoliated on poly(methylmethacrylate) (PMMA) layer which was located on top of a polydimethylsiloxane (PDMS) stamp. The h-BN on the PMMA/PDMS stamp was used to sequentially pick up the prepared graphene and WSe_2 flakes. The resulting h-BN/graphene-WSe_2-graphene stack on the PMMA/PDMS stamp was then transferred to the few-layer h-BN prepared on the SiO_2/Si wafer to construct the final h-

BN/graphene-WSe_2-graphene/h-BN stack. The PMMA windows for electrodes were defined through standard electron-beam lithography on the previously transferred PMMA layer. The samples were then immersed in IPA/water (7:3) solution for 40 seconds, followed by reactive ion etching with CF_4/O_2 (100/20 mTorr; 200 W) for 20 seconds (Technics MicroRIE 800). Cr/Au (20/50 nm) metals made edge-contact with the graphene flakes by high-vacuum electron-beam evaporator.

Fabrication and transfer process of AgI microplate

We first prepared a series of 50-nm thick Ag metal microplates on SiO_2/Si substrate with an atomically flat surface by using standard electron-beam lithography and high-vacuum electron-beam evaporation. Iodine vapor conversion process was executed by placing the Ag microplates into a sealed glass vial where 0.1 g of solid iodine was contained. The Ag microplates were iodized in the dark at room temperature and under ambient pressure for 24 hours (Figure 23). To avoid possible Ag oxidation, the whole conversion steps were conducted in a nitrogen-filled glove box with low oxygen level lower than 0.1 ppm.

Next, a hexamethyldisilazane (HMDS) layer was applied to functionalize the entire wafer. The wafer was placed with HMDS in a sealed glass container at 120 ˚C inside oven for 10 minutes. After taken out from the oven, the wafer was cooled down for 10 minutes, followed by isopropyl alcohol (IPA) rinse. PMMA layer was then spin-coated on the whole wafer. The PMMA layer with the AgI microplates can thus be physically peeled off together from the substrate using a PDMS stamp. The AgI microplates on the PMMA/PDMS stamp were then transferred and laminated on the channel of the prefabricated WSe_2 FETs.

Device poling process and characterization

To facilitate ion migration in AgI microplates, the devices were placed on the heating stage of the commercial probe station (Lakeshore, TTP4) and heated to 425 K. After 10 minutes of applying potentials either by V_{DS} or V_{BG}, the devices were cooled down to room temperature (300 K). The magnitude of the applied potentials for uniform poling by V_{BG} was 60 V. For non-uniform poling by V_{DS}, 1 V/μm was applied along with channel lengths. The poling potentials were continuously applied during cooling process to ensure that Ag^+ mobility is suppressed below the superionic transition point (420 K) of AgI, thereby the poled Ag^+ are fixed in desired locations. Both back-gate and drain-source poling processes and electrical measurements were carried out in the probe station equipped with 532-nm wide field laser (Coherent, 532-100). The electrical measurement data were obtained by a precision source/measure unit (Agilent, B2902A) and a computer-controlled analogue-to-digital converter. The structural analyses of Ag and AgI were carried out by X-ray diffraction (XRD) with Panalytical X'Pert Pro X-ray. Electrochemical impedance spectroscopy was measured using a Bio-Logic VMP-3 Potentiostat. AC impedance was measured using a 10 mV amplitude in the frequency range between 1 MHz and 100 mHz. Pasted silver electrodes were used to make contacts. Ionic conductivity measurements were carried out from 25 to 160 °C to observe a phase transition from the β-AgI to the α-AgI phase. The cross-sectional structure of AgI/WSe_2 FET was prepared by focused ion beam (FIB) with NOVA 600 SEM/FIB System, and characterized by transmission electron microscopy (TEM) with Titan S/TEM.

3.3. Results and discussion

Characterization of AgI/WSe_2 FETs

To elucidate the doping effect induced by AgI, WSe_2 is selected as a model system for its excellent electronic properties[11] and intrinsic ambipolarity[12] for better visualization of both the p- and n-type doping effects. Graphene with tunable work functions is used as the source drain contacts to ensure low barrier contacts for either p- or n-doped WSe_2 channels[13]. Because the direct deposition of Ag atoms involves bombardment of high-energy atomic clusters that could alter underlying WSe_2 characteristics (Figure 24), we utilized physical lamination (or *van der Waals* integration)[14] of a AgI microplate to ensure proper device function (Figure 25). Specifically, AgI microplates were first fabricated on a sacrificial substrate by a standard lithography and Ag deposition process, followed by a vapor phase iodine conversion process[15]. The crystallographic structure of the formed AgI microplates was characterized by X-ray diffraction (XRD) and confirmed the complete transformation of Ag into AgI (Figure 26). The AgI microplates were then mechanically peeled from the substrate and physically laminated onto a WSe_2 FET with a pair of graphene electrodes on top of highly doped (p^{++}) silicon covered with 290-nm SiO_2.

The graphene-WSe_2-graphene FET was encapsulated within few-layer hexagonal boron nitride (h-BN). Top h-BN served as a protective layer for integration of AgI on top. With direct deposition of Ag on a WSe_2 semiconductor channel followed by iodine vapor conversion, the output current of WSe_2 FET cannot be measured, which might be attributed to possible damage on the channel during AgI crystallization of Ag atoms planted by high energy of electron beam evaporation (Figure 27).

Moreover, the top h-BN prevents WSe_2 from directly reacting with AgI after lamination (Figure 28)[16] while the bottom h-BN minimizes scattering effects[17, 18] from the trapping states on SiO_2 surface. This results in an overall device structure of: AgI/h-BN/graphene-WSe_2-graphene/h-BN on a SiO_2/Si substrate with a pair of graphene flakes forming electrical contacts with the WSe_2

channel (Figure 29a). The channel length of a typical device was about 6 μm and covered with AgI microplate (Figure 29b). The cross-sectional transmission electron microscopy (TEM) image of the transferred AgI/WSe_2 FET junction showed atomically sharp and clean interface with no apparent defects or disorder (Figure 29c)[19]. Measurements of the temperature-dependent ionic conductivity of the fabricated AgI microplate clearly showed a sharp increase of ionic conductivity by nearly three orders of magnitude upon reaching 147 ˚C (Figure 22 and Figure 30)[10], clearly demonstrating a robust superionic phase transition.

Type-switchable WSe_2 FETs programmed by silver iodide

Next, we examined the feasibility of creating carrier type-switchable FETs by applying vertical poling through the back-gate terminal. The programmability of our AgI/WSe_2 devices is achieved by exploiting the unique superionic phase transition in AgI. In the superionic conduction phase, Ag^+ can be polarized with a negative gate electric field[20]. The Ag^+ selectively accumulate near the WSe_2 interface and become immobilized at a temperature below 147 ˚C (ref. [10]). The accumulated Ag^+ induce an electrostatic field to increase electron concentration in WSe_2 (ref. [21]), producing an n-channel FET (Figure 31a). In contrast, a positive poling voltage produces an Ag^+-deficient interface, resulting in a hole doping effect and a p-channel FET (Figure 31b). The transfer curve (I_{DS}-V_{BG}) of the as-fabricated AgI/WSe_2 FET showed clear ambipolar characteristics with the charge neutral point close to zero gate voltage, which is similar to that of WSe_2 FET (Figure 32a). This behavior suggests there is minimal extrinsic doping in the fully encapsulated devices[17].

As expected, the transfer curve was shifted from ambipolar to n-type behavior after the negative back-gate poling process (Figure 32b, red line), confirming that electrons become the dominant carrier type with an on/off current ratio exceeding 10^5. It is important to note that, by

being physically isolated by the upper h-BN dielectric (Figure 29c), the AgI microplate does not directly contribute to the charge transport of the FET but only provides the electrostatic doping effect to modulate the dominant carrier type and concentration.

To highlight the ability to control the doping effect, the identical device underwent a positive back-gate poling process against the previous n-programmed state. The transfer curve showed that the majority carrier type completely switched to holes (Figure 32b). This experiment demonstrates that a carrier type-switchable transistor can be realized by reversible Ag^+ migration in AgI crystal through vertical poling. The standard output characteristics (I_{DS}-V_{DS}) further confirmed n-type (Figure 32c) and p-type (Figure 32d) transistor characteristics after negative and positive vertical poling processes, respectively. It is also noted that single-layer WSe_2 devices showed similar behavior with that of the few-layer devices (Figure 33, a and b), demonstrating that there is no apparent distinction in the doping effects either on single- or few-layer WSe_2. The qualitatively similar gate tunability in single- or few-layer 2D transistors has been consistently observed in previous literature[22].

Polarity-switchable WSe_2 diodes programmed by AgI microplate

Beyond uniform doping in the semiconducting channel by vertical potentials, non-uniform doping can be achievable through lateral electric fields[20]. In this case, the drain-source electrodes are used to polarize the superionic solid. The migration of Ag^+ in the superionic conduction phase is facilitated by the drain-source potential (V_{DS}), which creates a charge imbalance along the channel length. The resulting ionic profile provides opposite doping effects at both ends of the underlying WSe_2 channel[23]. During a positive lateral poling process, Ag^+ are accumulated near the grounded electrode (Figure 34a). In this process, one side of the channel near the biased electrode experiences a net negative electrostatic potential, achieving p-type doping, while the opposite side

close to the grounded electrode experiences a net positive potential and becomes electron doped. Together, this process produces a forward biased p-n diode. Furthermore, negative V_{DS} poling produces a forward biased n-p diode (Figure 34b). After the positive lateral poling process, rectifying output characteristics showed a positive turn-on voltage and high output current above the turn-on voltage (Figure 35a)[24]. To emphasize the switchable doping effect, the lateral poling process was repeated on the identical device, but with negative V_{DS}. The resulting diode exhibited the rectification behavior with opposite polarity, showing a negative turn-on voltage and high output current in the negative bias regime (Figure 35b)[24].

The experimental output curves of both diodes were fitted to the Shockley equation for quantitative analyses[25, 26]. For a diode, the current dependence can be written as:

$$I = I_S \cdot \left[\exp\left(\frac{V - I \cdot R_S}{n \cdot V_T}\right) - 1\right] + \left(\frac{V - I \cdot R_S}{R_{SH}}\right) \quad (2)$$

where the pre-exponential factor I_S is the reverse saturation current and $V_T = k_B T/q$ defines the thermal voltage; the Boltzmann constant is k_B, temperature is T and the electron charge is q. The empirical parameters n, R_S and R_{SH} are introduced in the Shockley equation to fit the experimental data; these are the ideality factor n, series resistance R_S and shunt resistance R_{SH}. The extracted ideality factors were n = 1.19 with R_S = 5.4 MΩ and n = 1.20 with R_S = 7.2 MΩ for positively (Figure 36a) and negatively poled diodes (Figure 36b), respectively, with the rectification ratio of 10^5 for both diodes. Compared to the previously reported values from TMD-based diodes[22, 24, 27-30], the ideality factors obtained here are among the closest to that of an ideal diode (n = 1) (Table 1). Such consistent ideality factors between positively and negatively poled diodes demonstrate that, regardless of the poling directions, the device retained its rectifying performance and the rectifying behavior resulted from the dynamic poling process rather than intrinsic non-

asymmetrical contacts. The small differences in the R_S values are most likely due to the contact and series resistance of the atomically thin channel[31]. Moreover, we note that the current outputs from the diodes showed apparent gate-tunability (Figure 35, a and b)[28]. Interestingly, the positive gate potentials promoted the charge transport for both types of diodes, which could be attributed to less efficient doping (or large contact barrier) by AgI for the n-doped WSe_2 channel. This behavior suggests that the n-doped side may be dominating the on-state resistance.

These programmed diodes can also function as effective photodiodes. With 532-nm wide field laser illumination, a positively poled photodiode delivered an open-circuit voltage (V_{OC}) of +0.52 V (Figure 37a). After the negative lateral poling process, the photodiode showed a V_{OC} of -0.41 V (Figure 37b), demonstrating that the polarity is programmable by the poling process.

Stability of programmed function

To further support the room-temperature stability of programmed functions, retention performance of the diode was also investigated (Figure 38). The output currents measured at certain periods of time after programming showed the stable rectification behavior over the experimental time scale, suggesting that the large ionic conductance switch associated with the sharp superionic phase transition in AgI effectively addresses volatility issue in typical ionic dopants to ensure highly stable operation at room temperature.

Application: Logic gates

Our findings show that coupling of 2D semiconductors and the superionic conductor, AgI, offers programmable FETs with non-volatile characteristics for either p- or n-type dopants depending on the direction of potentials. Such switchable FETs allow a flexible integration of multiple transistors to create complex logic functions with a single type of devices through proper

ion manipulation. We demonstrated a digital logic inverter by connecting two innately identical FETs (Figure 39a) and poling them with opposite gate potentials to create p- and n-type transistors with enhancement-mode characteristics (Figure 40). The digital logic inverters showed the voltage transfer characteristics with consistent logic inversion function (Figure 39, a and b). The voltage gain (~2.8) we obtained was clearly larger than unity, sufficient for integrated logic circuits with multiple cascaded inverters. We also tested more complicated logic functions achieved by connecting 4 identical AgI/WSe_2 FETs, configuring either a logic NAND or NOR gate depending on how each FET is poled: 2 FETs as NMOS and 2 FETs as PMOS. The NAND logic functions were successfully observed from $V_{IN,A}$, $V_{IN,B}$ and V_{OUT} (Figure 41, a and b)[32]. Furthermore, the logic NAND gate can be reconfigured into a logic NOR gate by poling the FETs in the opposite direction and exchanging V_{DD} with GND (Figure 42, a and b).

Scalability to smaller dimension

Together, by integrating switchable superionic solids with atomically thin 2D semiconductors, our design allows independent programming with minimum crosstalk to make logic integration possible. Additionally, the scalability to smaller dimension is important for modern electronic devices. The Debye screening length in the solid-state superionic conductor should represent the ultimate limit of the scalability, which is dependent upon the dielectric constant and the concentration of charge carriers in the material[33]. Since most typical superionic conductors (e.g. α-AgI) feature high concentration of mobile ions and high dielectric constant, the Debye length is usually rather small (~1 nm) (ref. [34, 35]). On the other hand, the state-of-the-art extreme ultraviolet (EUV) lithography in the semiconductor industry may produce structures down to 5 nm (ref. [36]). Therefore, the Debye length (~1 nm) that limits the doping profile for 2D materials is likely not the dictating factor in scaling to the smaller dimension.

3.4. Conclusion

This study not only addresses the current technological challenges in controlling the carrier doping in 2D semiconductors, but also opens a pathway to a new generation of devices that can be dynamically programmed, stably operated at room temperature, erased or reprogrammed with distinct functions on demand (Table 2). This integration of switchable superionic solid with 2D semiconductors could also lead to a new direction for future electronics by taking full advantage of atomically thin 2D materials and superionics to achieve efficient coupling between electron transport and ionic transport, which could enable novel devices for unconventional computing, information storage and advanced solid-state neuromorphic circuits[37].

3.5. Figures, tables and legends

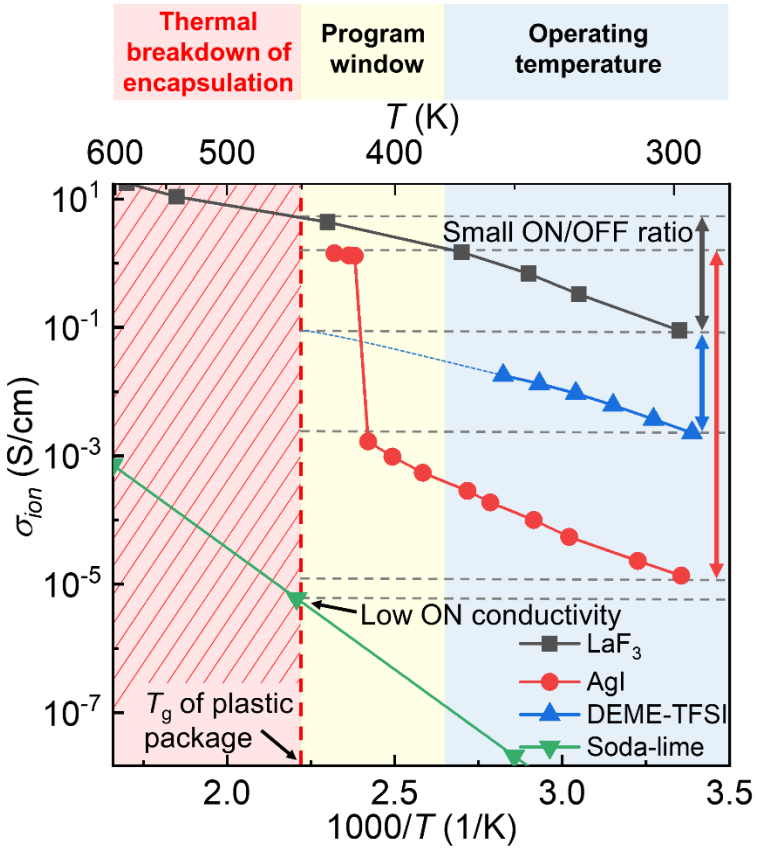

Figure 22. Comparison of ionic conductivity of AgI, LaF_3 (ref. [9]), DEME-TFSI (ref. [38]), and soda-lime glass[5] for programmable logic functions. According to the guideline from the Intel's CPU product[1], most CPUs experience an operating temperature under 100 ˚C (typically 45 to 70 ˚C during normal operation). The maximum programming temperature is limited by the glass transition temperature T_g of the typical commercial plastic package (~175 ˚C) (ref. [4]). With these temperature constraints, the devices need to be programmed below 175 ˚C and stably operate at temperature up to 100 ˚C. This requires a large ionic conductance switching within a rather narrow temperature window (100-175 ˚C) to ensure efficient program and stable operation. The ionic conduction in superionic solid (LaF_3), ionic liquid (DEME-TFSI) or soda-lime glass is typically governed by thermal activation and the Arrhenius law, and it is fundamentally challenging to

achieve a sufficiently large switch of the ionic conductance within a narrow enough temperature window (100-175 ˚C). The ionic conductance of these materials is either too high to allow stable operation at room temperature or too low to allow efficient program within the thermal budget of typical ICs. In contrast, the AgI features a unique solid-state superionic phase transition at 147 ˚C with a very sharp large ionic conductance switch that is critical for efficient programming at a moderate temperature and stable logic operation at room temperature.

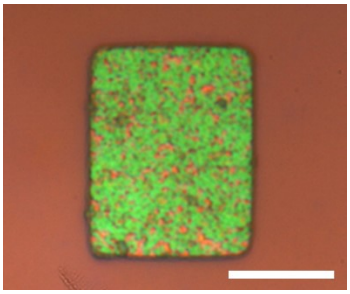

Figure 23. Optical image of a AgI microplate. After evaporation of 50-nm Ag on SiO_2/Si, the sample was converted to AgI with iodine vapor. Scale bar, 10 μm.

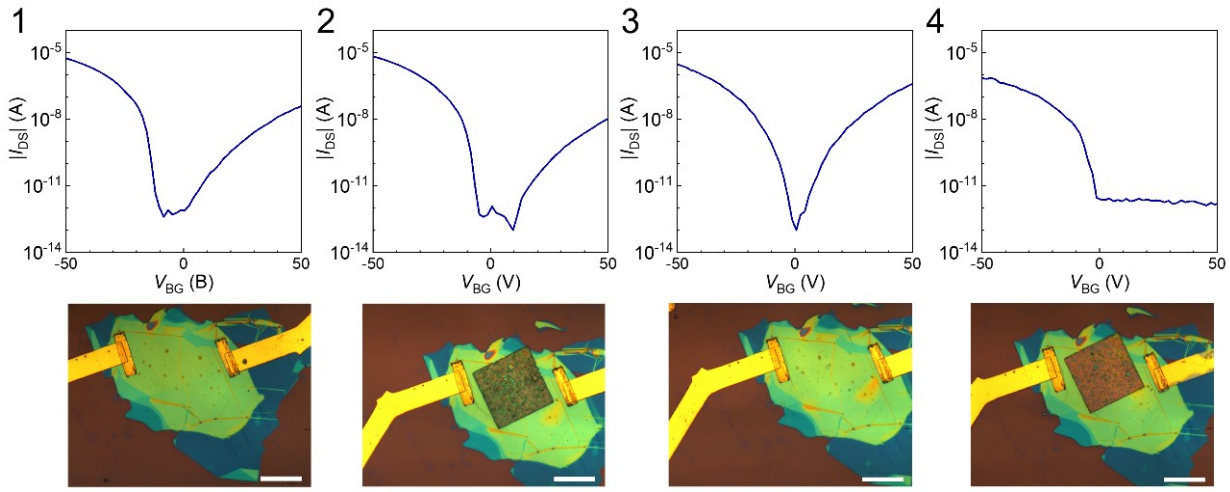

Figure 24. Sequential transfer characteristics of AgI/WSe_2 FET with van der Waals integration and direct deposition of AgI. I_{DS}-V_{BG} transfer curves and corresponding optical images of WSe_2 FET (1), WSe_2 FET with van der Waals-laminated AgI (2), WSe_2 FET after the removal of the previously laminated AgI (3), and WSe_2 FET with deposited AgI by electron-beam evaporator (4). All the measurements were conducted at room temperature in dark. WSe_2 FET without AgI microplate showed clear ambipolar behavior. AgI microplate was then laminated on the WSe_2 FET by using van der Waals integration. The resulting AgI/WSe_2 FET remained its ambipolarity. After the removal of the AgI, the transfer curve of WSe_2 FET showed minimal changes from its initial ambipolarity. Ag metal was then deposited on the identical location of the previously laminated AgI by using high-vacuum electron-beam evaporator, followed by vapor phase iodine conversion process. The resulting AgI/WSe_2 FET did not possess the innate ambipolar, but showed p-type characteristics, demonstrating that typical metal deposition processes could alter intrinsic properties of underlying 2D materials (scale bar, 20 μm).

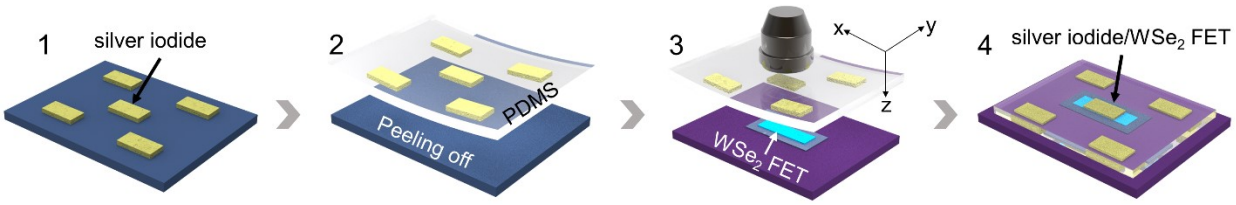

Figure 25. Schematic illustrations of *van der Waals* integration of AgI. The sequential process of AgI/WSe_2 FET fabrication by *van der Waals* integration is shown by AgI on sacrificial SiO_2/Si substrate (1), peeling-off (2), alignment to a target (3) and lamination on WSe_2 FET (4).

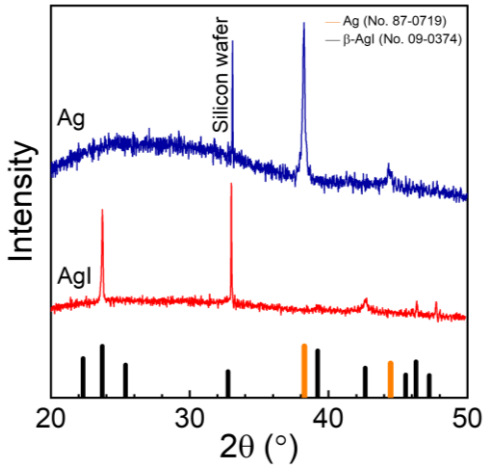

Figure 26. X-ray diffraction (XRD) patterns of the fabricated Ag and AgI. XRD patterns of AgI thin film (red) showed multiple peaks with no strong Ag peak at around 38˚, whereas the peak appeared in the Ag pattern (blue) suggesting the complete conversion from Ag to AgI. JCPDS data of Ag (No. 87-0719) (orange) and β-AgI (No. 09-0374) (black) are presented for comparison at the bottom of the plot. All the measurements were conducted at room temperature in dark.

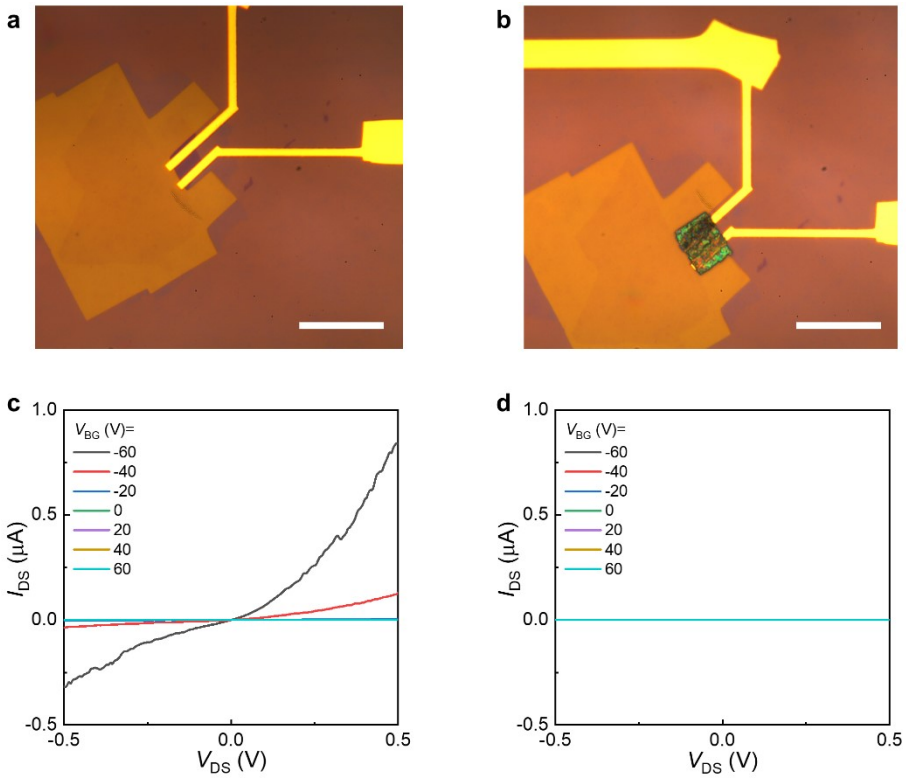

Figure 27. Deposition and conversion of AgI directly on WSe_2 semiconductor channel without top h-BN protective layer. a, Optical image of WSe_2 FET without AgI layer. **b**, Optical image of AgI/WSe_2 FET in which AgI was directly deposited on prepared WSe_2 FET. **c**, Output characteristics of as-fabricated WSe_2 FET on SiO_2/Si substrate shown in (**a**), showing p-doped behavior. **d**, Output characteristic of the AgI/WSe_2 FET shown in (**b**), showing no output current after direct deposition and conversion of AgI top layer. Scale bar, 10 μm.

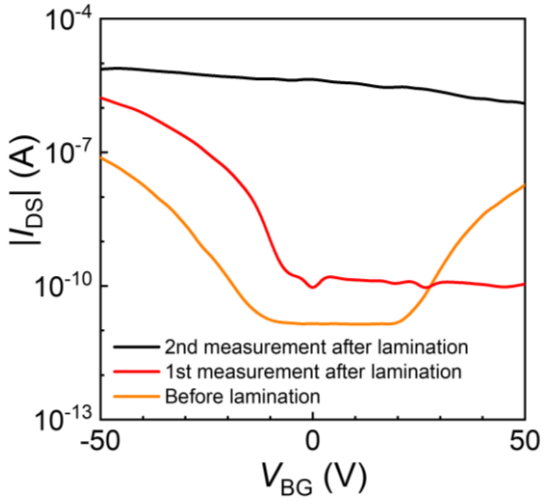

Figure 28. Encapsulation effect by the top h-BN dielectric. I_{DS}-V_{BG} transfer characteristics of WSe_2 FET without top h-BN dielectric (graphene-WSe_2-graphene/h-BN) (orange), AgI/WSe_2 FET without top h-BN dielectric (AgI/graphene-WSe_2-graphene/h-BN) on the 1st measurement (red), and on the 2nd measurement (black), collected right after the 1st measurement. The WSe_2 FET without top h-BN dielectric and AgI microplate showed clear ambipolarity. After lamination of AgI microplate on the WSe_2 channel, the transfer curves of the AgI/WSe_2 FET were shifted to p-type characteristics with an increase in current by more than one order of the magnitude. Compared to the top h-BN encapsulated AgI/WSe_2 FET, the direct contact between AgI and WSe_2 could induce irreversible chemical reactions and alter the intrinsic properties of WSe_2. All the measurements were conducted under V_{DS} = 1 V at room temperature in dark.

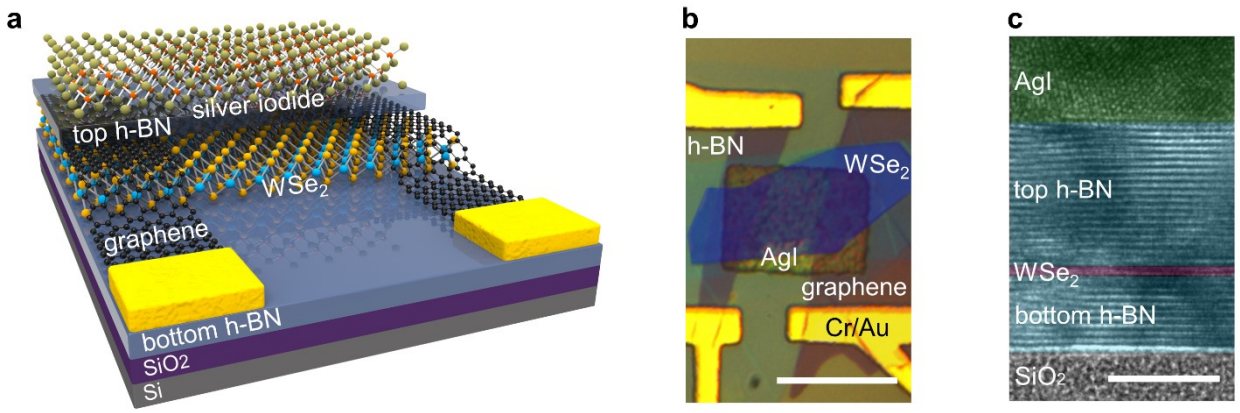

Figure 29. Illustrations of the WSe_2 FET integrated with a AgI microplate. a, Schematic illustration of the AgI/h-BN/graphene-WSe_2-graphene/h-BN device structure on a SiO_2/Si substrate. **b**, False-colored microscope image of the device. Scale bar, 10 μm. **c**, False-colored cross-sectional TEM image of the transferred AgI microplate on top of the channel of WSe_2 FET encapsulated in h-BN dielectrics. Scale bar, 5 nm.

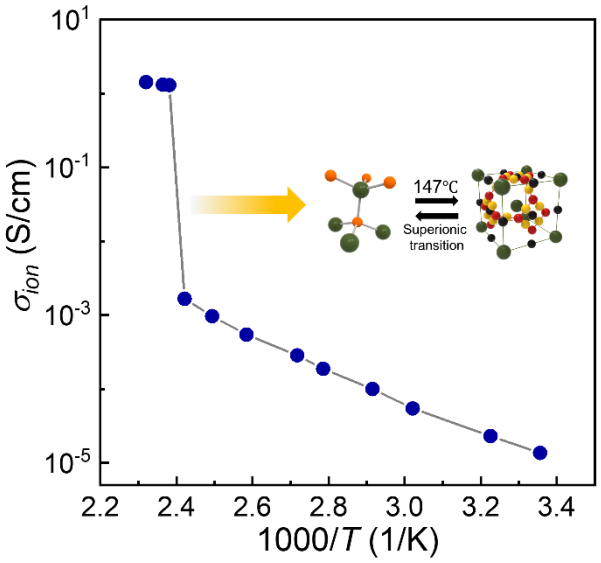

Figure 30. Temperature-dependent ionic conductivity of the fabricated AgI. Ionic conductivity (σ_{ion}) of the fabricated AgI was measured with increasing temperatures. Upon

reaching the superionic transition point (420 K), the ionic conductivity showed a sharp increase by about three orders of magnitude. Compared to other ionic conductors with gradual conductivity increase as temperature reaches their melting point, the sharp transition of AgI is essential for stably operating devices with programmable characteristics.

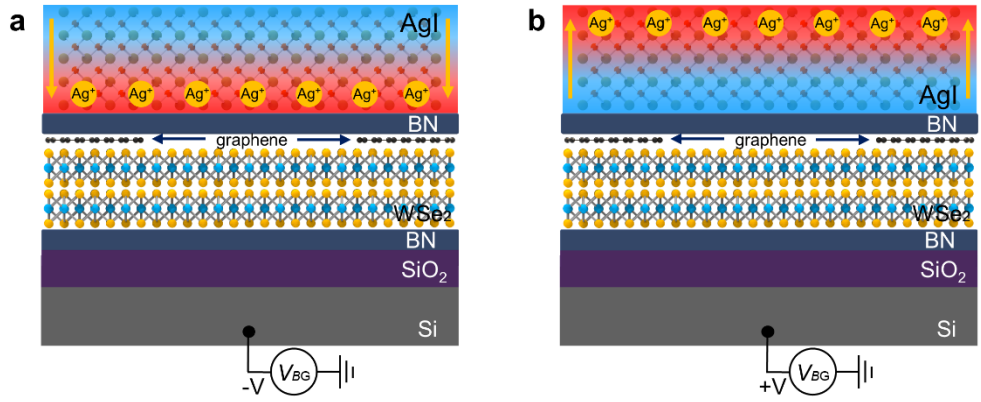

Figure 31. Gate-terminal poling process and resulting uniform doping effects. a, Schematic illustrations of negative back-gate poling process that enriches a net positive potential (Ag^+ rich) at AgI/h-BN interface thereby the positive electrostatic fields driven by Ag^+ induce n-doping effect on underlying WSe_2 semiconductor layer. **b**, Schematic illustrations of positive back-gate poling process that enriches a net negative potential (Ag^+ deficient) at AgI/h-BN interface thereby the negative electrostatic fields driven by I^- induce p-doping effect on underlying WSe_2 semiconductor layer.

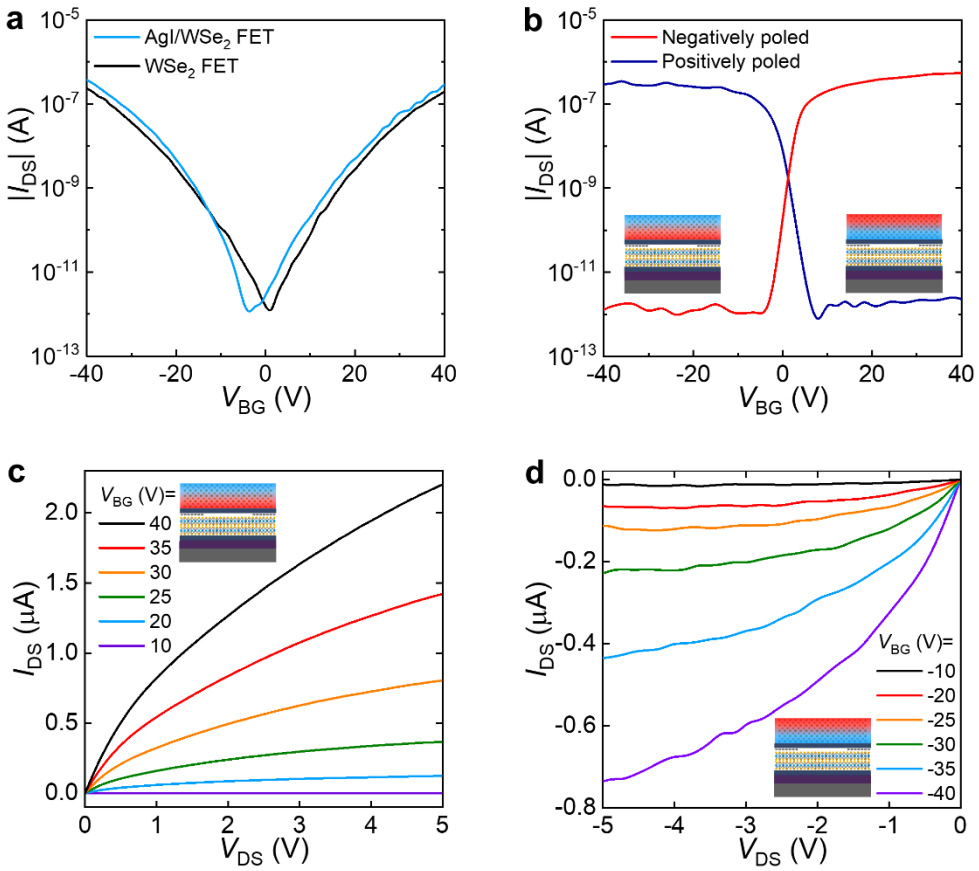

Figure 32. Uniform doping effects and resulting type-switchable WSe_2 FETs programmed by AgI. a, I_{DS}-V_{DS} transfer curves of the WSe_2 FET before (black line) and after (blue line) AgI lamination. **b**, I_{DS}-V_{BG} transfer curves after vertical poling process with negative (V_{BG} = -60 V, red line) and positive (V_{BG} = +60 V, blue line) back-gate voltages. Inset: Schematic illustrations of resulting ionic charge distribution. **c**, I_{DS}-V_{DS} curves after negative back-gate poling process, showing n-channel FET characteristics. Inset: Schematic illustration of resulting ionic charge distribution. **d**, I_{DS}-V_{DS} curves after positive back-gate poling process, showing p-channel FET characteristics. Inset: Schematic illustration of resulting ionic charge distribution. All the measurements were conducted at room temperature in dark.

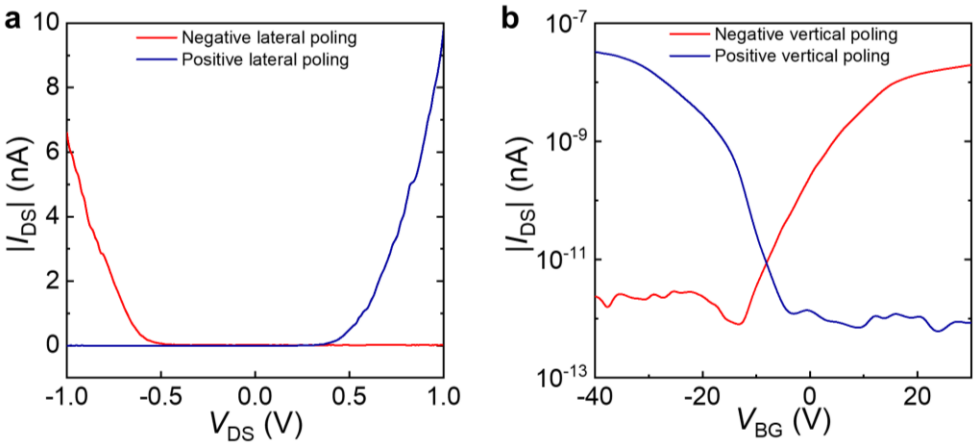

Figure 33. Single-layer WSe_2 devices programmed by AgI. a, I_{DS}-V_{DS} output curves after lateral poling process with negative (red line) and positive (blue line) drain-source voltages. **b**, I_{DS}-V_{BG} transfer curves after vertical poling process with negative (red line) and positive (blue line) back-gate voltages. All the measurements were conducted at room temperature in dark.

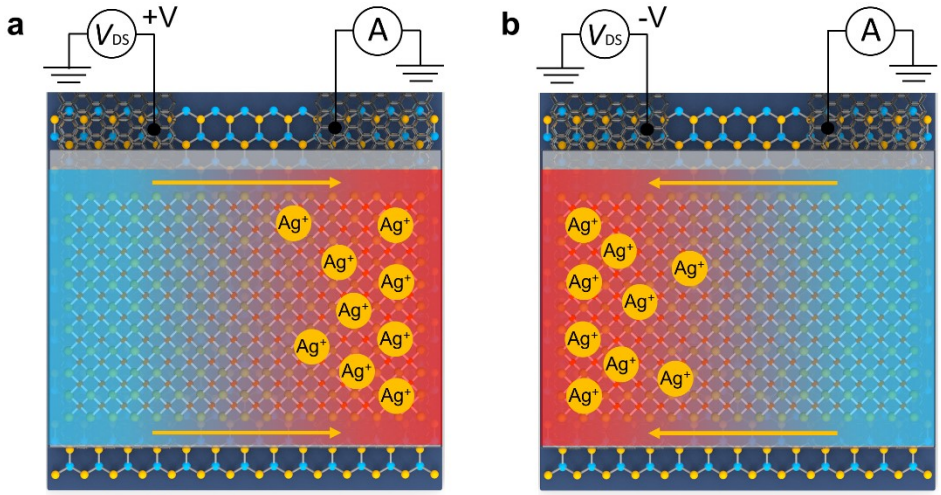

Figure 34. Drain/Source terminal poling process and resulting non-uniform doping effects. a, Schematic illustrations of negative drain-terminal poling process that enriches a net positive potential (Ag^+ rich) at AgI/h-BN interface near grounded source electrode thereby the positive

electrostatic fields driven by Ag^+ induce n-doping effect on the underlying WSe_2 semiconductor layer. On the other side near the biased drain electrode, a net negative potential (Ag^+ deficient) induces p-doping effect to the underlying WSe_2 semiconductor layer. **b**, Schematic illustrations of positive drain-terminal poling process that enriches a net positive potential (Ag^+ rich) at AgI/h-BN interface near biased drain electrode thereby the positive electrostatic fields driven by Ag^+ induce n-doping effect on the underlying WSe_2 semiconductor layer. On the other side near the grounded source electrode, a net positive potential (Ag^+ rich) induces n-doping effect to the underlying WSe_2 semiconductor layer.

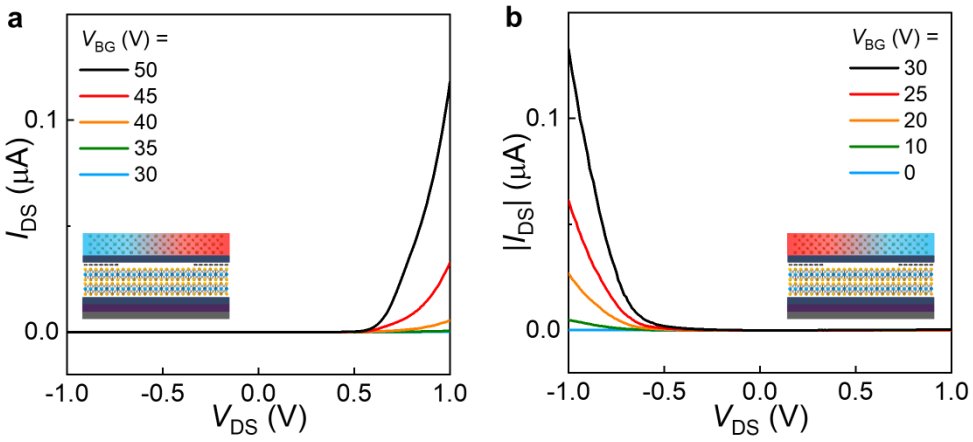

Figure 35. Non-uniform doping effect and the resulting polarity-switchable WSe_2 diode programmed by AgI. a, Output characteristics of the AgI/WSe_2 FET after lateral non-uniform poling process with positive V_{DS} = 1 V/μm. Inset: Schematic illustration of resulting ionic charge profile. **b**, Output characteristics of the AgI/WSe_2 FET after lateral non-uniform poling process with negative V_{DS} = -1 V/μm. Inset: Schematic illustration of resulting ionic charge profile.

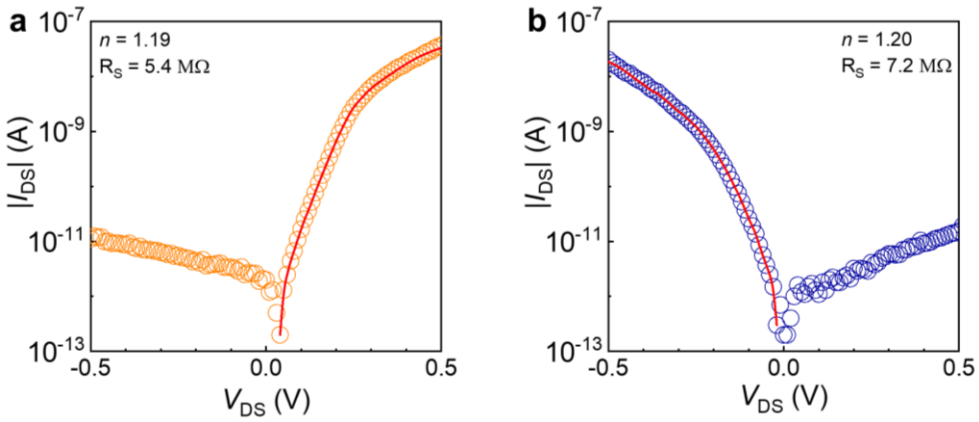

Figure 36. Derivation of diode ideality factors by fitting the measured data with Shockley equation. a,**b**, Semi-logarithmic plots of I_{DS}-V_{DS} output curves with the Shockley equation fittings of positively poled (**a**) and negatively poled (**b**) diodes represented by data points (open circles) and fitted curves (red).

Table 1. Comparison of the ideality factors of 2D-TMD semiconductor-based diodes. Data are from this work and references. N/A, not applicable/reported.

Device Structure	Feature			
	2D materials	Thickness	Ideality factor (*n*)	Reference
AgI-coupled	**WSe_2**	**few-layer**	**1.19**	**Present work**
Stacked heterojunction	GaTe/MoS_2	few-/few-layer	**1.75**	27
	WSe_2/MoS_2	1-/few-layer	**1.20-1.30**	28
	BP/MoS_2	few-/1-layer	**2.70**	30
	MoS_2/WSe_2	few-/few-layer	N/A	39
Split-gated	WSe_2	few-layer	N/A	32
	WSe_2	1-layer	**1.90**	24
	WSe_2	1-layer	**1.83**	22
	WSe_2	1-layer	**2.60**	29
Ionic liquid -gated	MoS_2	bi-/few-layer	N/A	21
	WSe_2	1-layer	**N/A**	23
	MoS_2	1-layer	N/A	40
	MoS_2	1-layer	N/A	41
Gel polymer -gated	WSe_2	1-layer	N/A	42

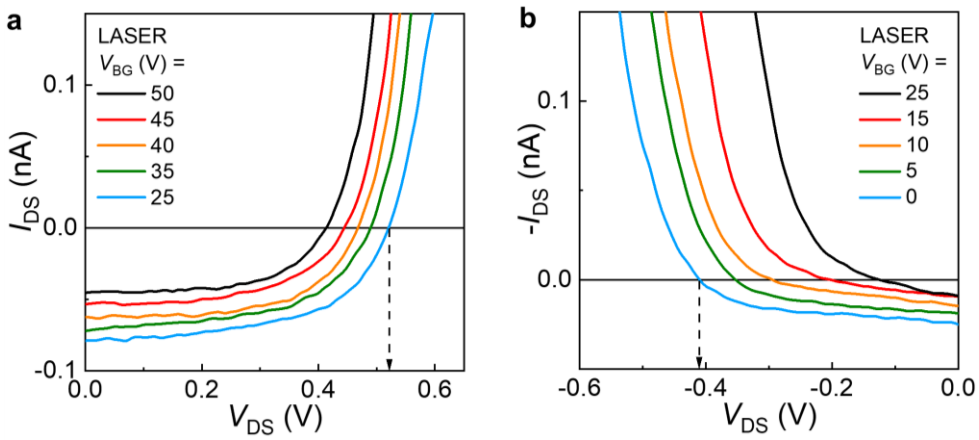

Figure 37. WSe_2 photodiodes programmed by AgI. a, I_{DS}-V_{DS} curves of the WSe_2 diode after lateral poling process with positive V_{DS}. **b**, I_{DS}-V_{DS} curves of the WSe_2 diode after lateral poling process with negative V_{DS}. All the measurements were conducted under 532-nm laser illumination (20 W/m^2) at room temperature.

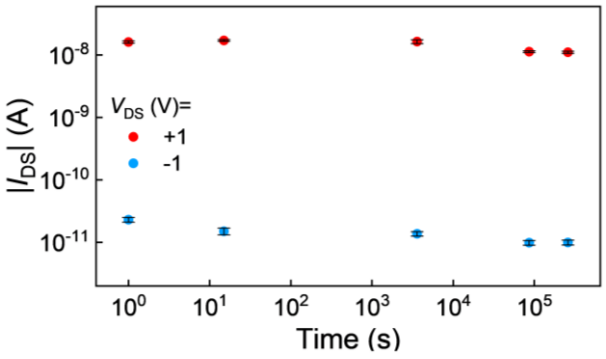

Figure 38. Retention performance of the WSe_2 diode programmed by AgI. Steady-state forward current (red circle) and reverse current (blue circle) of the positively poled AgI/WSe_2 diode were measured at the certain periods of time after programming. The output currents showed the stable status within experimental time scale (72 hours). All the measurements were conducted at room temperature in dark.

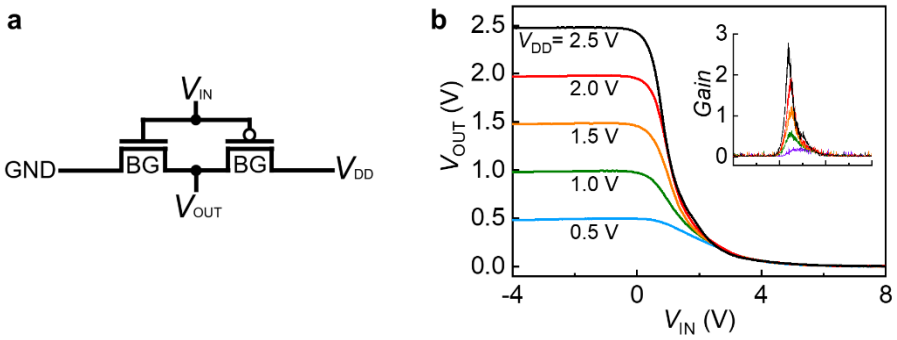

Figure 39. Logic digital inverter integrated by two identical AgI/WSe_2 FETs. a, Circuit diagram of the inverter integrated with two AgI/WSe_2 FETs. **b**, Transfer characteristics of the inverter operated at power supply V_{DD} = 0.5, 1.0, 1.5, 2.0 and 2.5 V. Inset: Output signal gain of the inverter extracted from the plot. All the measurements were conducted at room temperature.

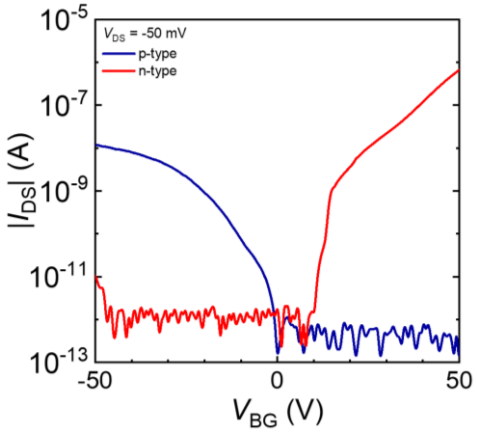

Figure 40. I_{DS}-V_{BG} curves of NMOS and PMOS for logic gates. Transfer curves of AgI/WSe_2 FETs after negative (for NMOS) (red) and positive (for PMOS) (blue) uniform poling process, showing enhancement-mode characteristics. All the measurements were conducted at room temperature in dark.

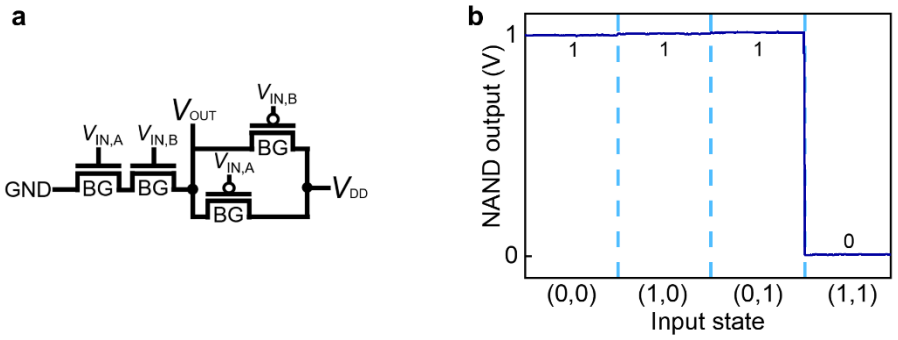

Figure 41. Logic NAND gate integrated by four identical AgI/WSe_2 FETs. a, Circuit diagram of NAND gate. **b**, Output voltage of logic NAND gate, at four typical input states, separated by blue dashed vertical lines, with a power supply of V_{DD} = 1 V. GND, ground; BG, back gate; '0', low binary output state; '1', high binary output state. All the measurements were conducted at room temperature.

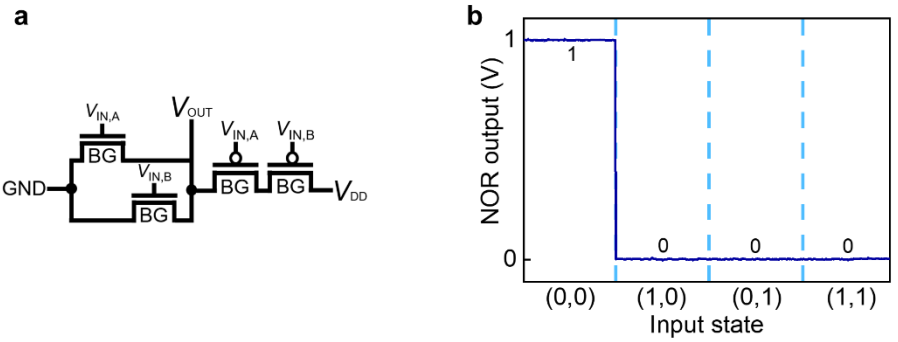

Figure 42. Logic NOR gate integrated by four identical AgI/WSe2 FETs. a, Circuit diagram of NOR gate. **b**, Output voltage of logic NOR gate, at four typical input states, separated by blue dashed vertical lines, with a power supply of V_{DD} = 1 V. GND, ground; BG, back gate; '0', low binary output state; '1', high binary output state. All the measurements were conducted at room temperature.

Table 2. Comparison of functional features among 2D-TMD devices.

Features	Device structure				
	AgI-coupled	Stacked heterojunction	Split-gated	Semi-split -gated	Ionic liquid -gated
Complete transistor-type switching (programmability)	Yes	No	Yes	No (partial)	Yes
Complete diode-polarity switching (programmability)	Yes	No	Yes	No (partial)	Yes
Non-volatile programmed functions without bias	Yes	Yes	No	Yes	Yes
Non-volatile programmed functions at room temperature	Yes	Yes	Yes	Yes	No
Solid-state compatibility	Yes	Yes	Yes	Yes	No
References	Present work	27, 28, 30, 39	24, 29, 32	22	21, 23, 40, 41

3.6. References

1. Intel Intel® Core™ Processors Technical Resources. https://www.intel.com/content/www/us/en/products/docs/processors/core/core-technical-resources.html.

2. Luryi, S.; Xu, J.; Zaslavsky, A., *Future trends in microelectronics*. Wiley Online Library: **1999**.

3. Li, L.; Zhu, Z.; Wang, T.; Currivan-Incorvia, J. A.; Yoon, A.; Wong, H.-S. P., BEOL compatible graphene/Cu with improved electromigration lifetime for future interconnects. *2016 IEEE International Electron Devices Meeting (IEDM)* **2016**, 9.5. 1-9.5. 4.

4. Saito, T.; Nishimura, Y.; Momose, F.; Hirao, A.; Morozumi, A.; Tamai, Y.; Mochizuki, E.; Takahashi, Y., High reliability packaging technologies for 175deg. C continuous operation in IGBT module. *2015 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)* **2015**, 791-794.

5. Dutta, A.; Sinha, T.; Jena, P.; Adak, S., Ac conductivity and dielectric relaxation in ionically conducting soda–lime–silicate glasses. *Journal of Non-Crystalline Solids* **2008**, 354, 3952-3957.

6. Kleitz, M.; Kennedy, J.; Vashishta, P.; Mundy, J.; Shenoy, G., Fast ion transport in solids. *Noth Holland: Elsevier* **1979**, pp. 683-686.

7. Shahi, K., Transport studies on superionic conductors. *physica status solidi (a)* **1977**, 41, 11-44.

8. Lau, J.; DeBlock, R. H.; Butts, D. M.; Ashby, D. S.; Choi, C. S.; Dunn, B. S., Sulfide solid electrolytes for lithium battery applications. *Advanced Energy Materials* **2018**, 8, 1800933.

9. Sinitsyn, V.; Lips, O.; Privalov, A.; Fujara, F.; Murin, I., Transport properties of LaF3 fast ionic conductor studied by field gradient NMR and impedance spectroscopy. *Journal of Physics and Chemistry of Solids* **2003**, 64, 1201-1205.

10. Agrawal, R.; Gupta, R., Superionic solid: composite electrolyte phase–an overview. *Journal of materials science* **1999**, 34, 1131-1162.

11. Podzorov, V.; Gershenson, M.; Kloc, C.; Zeis, R.; Bucher, E., High-mobility field-effect transistors based on transition metal dichalcogenides. *Applied Physics Letters* **2004**, 84, 3301-3303.

12. Chuang, H.-J.; Tan, X.; Ghimire, N. J.; Perera, M. M.; Chamlagain, B.; Cheng, M. M.-C.; Yan, J.; Mandrus, D.; Tománek, D.; Zhou, Z., High mobility WSe2 p-and n-type field-effect transistors contacted by highly doped graphene for low-resistance contacts. *Nano letters* **2014**, 14, 3594-3601.

13. Liu, Y.; Wu, H.; Cheng, H.-C.; Yang, S.; Zhu, E.; He, Q.; Ding, M.; Li, D.; Guo, J.; Weiss, N. O., Toward barrier free contact to molybdenum disulfide using graphene electrodes. *Nano letters* **2015**, 15, 3030-3034.

14. Cheng, R.; Bai, J.; Liao, L.; Zhou, H.; Chen, Y.; Liu, L.; Lin, Y.-C.; Jiang, S.; Huang, Y.; Duan, X., High-frequency self-aligned graphene transistors with transferred gate stacks. *Proceedings of the National Academy of Sciences* **2012**, 109, 11588-11592.

15. Cha, J.-H.; Jung, D.-Y., Air-Stable Transparent Silver Iodide–Copper Iodide Heterojunction Diode. *ACS applied materials & interfaces* **2017**, 9, 43807-43813.

16. Wang, J. I.-J.; Yang, Y.; Chen, Y.-A.; Watanabe, K.; Taniguchi, T.; Churchill, H. O.; Jarillo-Herrero, P., Electronic transport of encapsulated graphene and WSe2 devices fabricated by pick-up of prepatterned hBN. *Nano letters* **2015**, 15, 1898-1903.

17. Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J., Boron nitride substrates for high-quality graphene electronics. *Nature nanotechnology* **2010**, 5, 722.

18. He, D.; Qiao, J.; Zhang, L.; Wang, J.; Lan, T.; Qian, J.; Li, Y.; Shi, Y.; Chai, Y.; Lan, W.; Ono, L. K.; Qi, Y.; Xu, J.-B.; Ji, W.; Wang, X., Ultrahigh mobility and efficient charge injection in monolayer organic thin-film transistors on boron nitride. *Science advances* **2017**, 3, e1701186.

19. Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X., Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature* **2018**, 557, 696.

20. Kharkats, Y. I., Fast ion transport in solids induced by an electric field. *Solid State Ionics* **1981**, 2, 301-308.

21. Perera, M. M.; Lin, M.-W.; Chuang, H.-J.; Chamlagain, B. P.; Wang, C.; Tan, X.; Cheng, M. M.-C.; Tománek, D.; Zhou, Z., Improved carrier mobility in few-layer MoS2 field-effect transistors with ionic-liquid gating. *ACS nano* **2013**, 7, 4449-4458.

22. Li, D.; Chen, M.; Sun, Z.; Yu, P.; Liu, Z.; Ajayan, P. M.; Zhang, Z., Two-dimensional non-volatile programmable p–n junctions. *Nature nanotechnology* **2017**, 12, 901.

23. Zhang, Y.; Oka, T.; Suzuki, R.; Ye, J.; Iwasa, Y., Electrically switchable chiral light-emitting transistor. *Science* **2014**, 344, 725-728.

24. Baugher, B. W.; Churchill, H. O.; Yang, Y.; Jarillo-Herrero, P., Optoelectronic devices based on electrically tunable p–n diodes in a monolayer dichalcogenide. *Nature nanotechnology* **2014**, 9, 262.

25. Shockley, W., *Electrons and holes in semiconductors: with applications to transistor electronics*. van Nostrand New York: **1950**.

26. Schubert, E., *Light-emitting diodes*. New York Cambridge: **2006**.

27. Wang, F.; Wang, Z.; Xu, K.; Wang, F.; Wang, Q.; Huang, Y.; Yin, L.; He, J., Tunable GaTe-MoS2 van der Waals p–n junctions with novel optoelectronic performance. *Nano letters* **2015**, 15, 7558-7566.

28. Cheng, R.; Li, D.; Zhou, H.; Wang, C.; Yin, A.; Jiang, S.; Liu, Y.; Chen, Y.; Huang, Y.; Duan, X., Electroluminescence and photocurrent generation from atomically sharp WSe2/MoS2 heterojunction p–n diodes. *Nano letters* **2014**, 14, 5590-5597.

29. Pospischil, A.; Furchi, M. M.; Mueller, T., Solar-energy conversion and light emission in an atomic monolayer pn diode. *Nature nanotechnology* **2014**, 9, 257-261.

30. Deng, Y.; Luo, Z.; Conrad, N. J.; Liu, H.; Gong, Y.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Xu, X.; Ye, P. D., Black phosphorus–monolayer MoS2 van der Waals heterojunction p–n diode. *ACS nano* **2014**, 8, 8292-8299.

31. Sze, S. M.; Ng, K. K., *Physics of semiconductor devices*. John Wiley & Sons: **2006**.

32. Resta, G. V.; Balaji, Y.; Lin, D.; Radu, I. P.; Catthoor, F.; Gaillardon, P.-E.; De Micheli, G., Doping-free complementary logic gates enabled by two-dimensional polarity-controllable transistors. *ACS nano* **2018**, 12, 7039-7047.

33. Debye, P.; Huckel, E., Phys. Z. **1923**, pp. 185-305.

34. Stegmaier, S.; Voss, J.; Reuter, K.; Luntz, A. C., Li+ defects in a solid-state Li ion battery: theoretical insights with a Li3OCl electrolyte. *Chemistry of Materials* **2017**, 29, 4330-4340.

35. Kvist, A.; Tärneberg, R., Self-diffusion of silver ions in the cubic high temperature modification of silver iodide. *Zeitschrift für Naturforschung A* **1970**, 25, 257-259.

36. Anandtech Samsung Completes Development of 5nm EUV Process Technology. https://www.anandtech.com/show/14231/samsung-completes-development-of-5-nm-euv-process-technology.

37. Fuller, E. J.; Keene, S. T.; Melianas, A.; Wang, Z.; Agarwal, S.; Li, Y.; Tuchman, Y.; James, C. D.; Marinella, M. J.; Yang, J. J.; Salleo, A.; Talin, A. A., Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing. *Science* **2019**, eaaw5581.

38. Sato, T.; Morinaga, T.; Marukane, S.; Narutomi, T.; Igarashi, T.; Kawano, Y.; Ohno, K.; Fukuda, T.; Tsujii, Y., Novel Solid-State Polymer Electrolyte of Colloidal Crystal Decorated with Ionic-Liquid Polymer Brush. *Advanced Materials* **2011**, 23, 4868-4872.

39. Jeon, P. J.; Kim, J. S.; Lim, J. Y.; Cho, Y.; Pezeshki, A.; Lee, H. S.; Yu, S.; Min, S.-W.; Im, S., Low power consumption complementary inverters with n-MoS2 and p-WSe2 dichalcogenide nanosheets on glass for logic and light-emitting diode circuits. *ACS applied materials & interfaces* **2015**, 7, 22333-22340.

40. Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y., Ambipolar MoS2 thin flake transistors. *Nano letters* **2012**, 12, 1136-1140.

41. Zhang, Y.; Ye, J.; Yomogida, Y.; Takenobu, T.; Iwasa, Y., Formation of a stable p–n junction in a liquid-gated MoS2 ambipolar transistor. *Nano letters* **2013**, 13, 3023-3028.

42. Allain, A.; Kis, A., Electron and hole mobilities in single-layer WSe2. *ACS nano* **2014**, 8, 7180-7185.

CHAPTER 4. Programmable Devices for Transient Electronics

4.1. Introduction

Transient electronics is an emerging technology, which refers to fully functional and complete electronic system that can be made non-functional and/or physically destroyed on demand or when prearranged conditions are met[1]. An electronic system that dysfunctions itself at the termination stage is a precious resource for the protection of the vital information contained in the system[2]. The idea of building transience into critical electronic system is not new but calls for new thinking[1, 3]. In electronic industry where a next generation of electronic systems has been to make them more durable, an 'excellent' system requires the components that have long life spans more than a century. Thus, a new development paradigm is needed to manage the transient electronic technology. One way to accomplish transience is to develop transient version of each electronic component and combine them to build up electronic systems. Notable recent examples are electronic circuits fabricated on water soluble organic substrate with dissolvable metals[4], in which transience was made possible under water. On the other hand, more highly integrated and complex technologies related to active components, such as transistors and diodes, are more difficult to make transient while being reliable during operation. It is possible to fabricate transient versions of active components by introducing defects in semiconductor crystals which shorten its service life. Alternatively, current durable components can be replaced to less durable ones. However, both approaches have limitation in device performance and are hard to replace the current active components in integrated circuits. The best expected active components in near terms, therefore, should be made both with critical parts that are made transient and commercial-off-the-shelf performance.

In this chapter, we showed that the programmed functions of solid-state superionic-induced doping can be erased by environmental cues such as temperature or ultraviolet (UV) irradiation, thus defining a new type of transient electronics that can be nonfunctional on demand.

4.2. Experimental section

We have investigated the transient properties of the AgI/WSe_2 FET under different environmental conditions. Thermal excitation and UV irradiation were used to demonstrate the ability of the FET to function as a transient electronic device (Figure 43).

Transience triggered by temperature

To activate the transience of the device, a AgI/WSe_2 FET device was first non-uniformly poled to program the positively poled diode (Figure 35a). After stabilization of programmed function at room temperature, the FET-based photodiode was illuminated under 532-nm laser to measure V_{OC} at increasing temperatures from 300 K to 430 K.

Transience activated by UV

To observe the transience of the device, the prepared positively poled diode was illuminated by 254-nm UV lamp for specific time period. After each exposure to UV, the output characteristics of the diode were measured to observe the change in the reverse biased output currents ($V_{DS} < 0$ V).

4.3. Results and discussion

The V_{OC} of the positively poled diode remained stable with increasing temperature. Upon reaching the superionic transition temperature, the V_{OC} rapidly dropped to zero (Figure 44 and Figure 45). The lost built-in potential is attributed to the high mobility of Ag^+ in the superionic state (Figure 22)[5], thereby losing its imbalanced ionic distribution which is necessary for creating lateral p- and n- regions to form p-n diodes.

We also showed that the diode function can be erased by weak UV irradiation with 245-nm lamp (5 W/m^2). After the positive lateral poling, the diode was exposed to the UV lamp at room temperature. As the exposure time increases, the device lost its rectifying characteristics as a rapid increase occurred in the reverse current (Figure 46). This response could be attributed to the reduction of ionic silver to metallic silver induced by irradiation[6]. The temperature or UV dependent decrease in device functionality demonstrates that AgI/WSe_2 FET could be a potential candidate for transient electronic applications[2].

4.4. Conclusion

The controllable removal of device functions upon specific external trigger could portend a new generation of devices that are dynamically programmed, stably operated at room temperature, and then erased or reprogrammed with distinct functions. The prospect of such transient electronics are of considerable interest for protecting sensitive information contained in various electronic systems.

4.5. Figures and legends

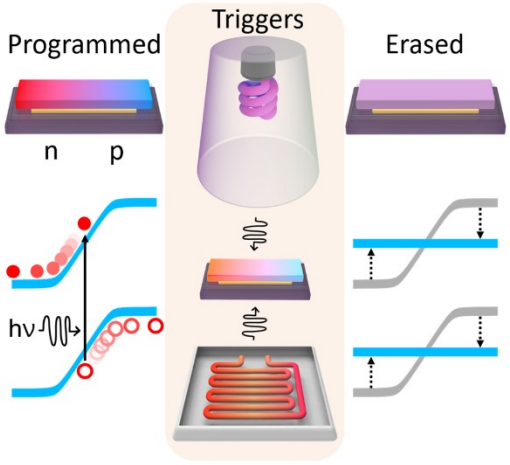

Figure 43. Transient electronics. Schematic illustrations of how transience of AgI/WSe_2 diodes is being activated by external triggers. The programmed diode (left) loses its built-in potential (right) either by UV irradiation (top center) or thermal excitation (bottom center).

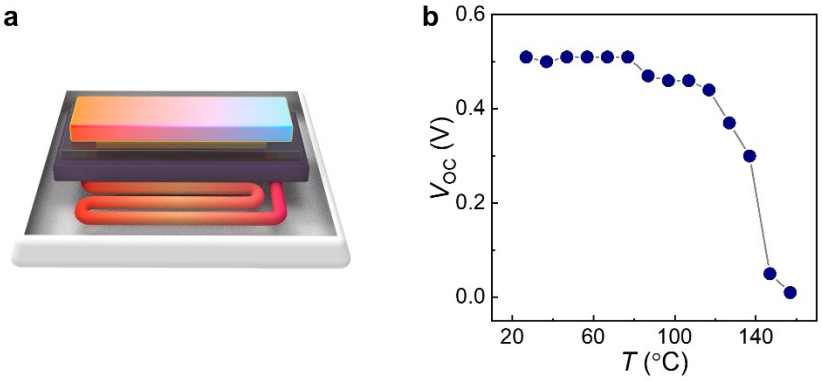

Figure 44. Temperature-triggerable transient property of the AgI/WSe_2 diode. a, Schematic illustration of the diode on heating plate on which the temperature of the AgI/WSe_2 diode can be controlled. **b**, The change of V_{OC} with increasing temperatures showed a sudden drop upon reaching the superionic transition temperature of AgI.

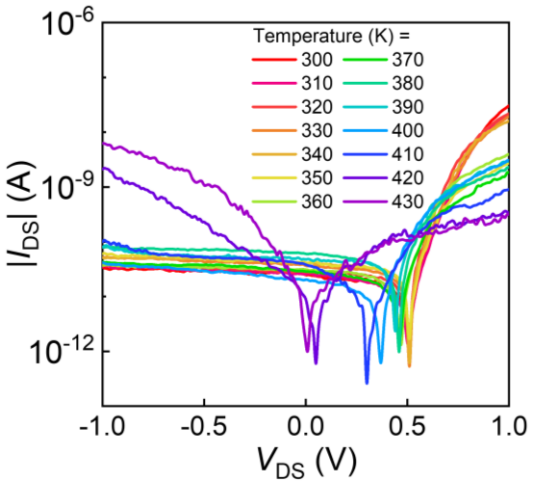

Figure 45. Thermal transience of the positively poled AgI/WSe_2 photodiode. Semi-logarithmic plot of I_{DS}-V_{DS} output curves of the positively poled photodiode with increasing temperature from 300 to 430 K (10 K step) under 532-nm laser illumination. The V_{OC}s were maintained at around 0.5 V at temperature between 300 K and 410 K but showed a sharp decrease above 420 K. Beyond this point, the photodiodes lost its built-in potentials, suggesting a rapid ion movement in the superionic phase to reach an equilibrium.

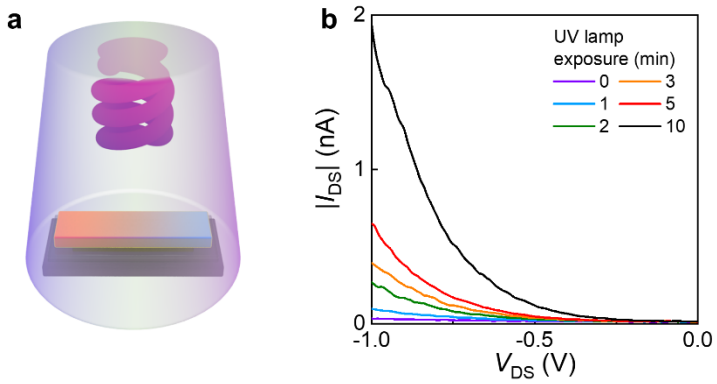

Figure 46. Ultraviolet-triggerable transient property of the AgI/WSe_2 diode. a, Schematic illustration of the diode under 254-nm UV lamp (5 W/m^2). **b**, The reverse output current of the positively poled diode increased over time under the lamp, indicating a loss of its rectifying behavior. All the measurements were conducted at room temperature.

4.6. References

1. Hwang, S.-W.; Tao, H.; Kim, D.-H.; Cheng, H.; Song, J.-K.; Rill, E.; Brenckle, M. A.; Panilaitis, B.; Won, S. M.; Kim, Y.-S.; Song, Y. M.; Yu, K. J.; Ameen, A.; Li, R.; Su, Y.; Yang, M.; Kaplan, D. L.; Zakin, M. R.; Slepian, M. J.; Huang, Y.; Omenetto, F. G.; Rogers, J. A., A Physically Transient Form of Silicon Electronics. *Science* **2012**, 337, 1640-1644.

2. Bayraktaroglu, B. *Transient Electronics Categorization*; AFRL-RY-WP-TR-2017-0169; U.S. Air Force Research Laboratory: **2017**.

3. Lei, T.; Guan, M.; Liu, J.; Lin, H.-C.; Pfattner, R.; Shaw, L.; McGuire, A. F.; Huang, T.-C.; Shao, L.; Cheng, K.-T.; Tok, J. B.-H.; Bao, Z., Biocompatible and totally disintegrable semiconducting polymer for ultrathin and ultralightweight transient electronics. *Proceedings of the National Academy of Sciences* **2017**, 114, 5107-5112.

4. Yin, L.; Cheng, H.; Mao, S.; Haasch, R.; Liu, Y.; Xie, X.; Hwang, S.-W.; Jain, H.; Kang, S.-K.; Su, Y.; Li, R.; Huang, Y.; Rogers, J. A., Dissolvable Metals for Transient Electronics. *Advanced Functional Materials* **2014**, 24, 645-658.

5. Agrawal, R.; Gupta, R., Superionic solid: composite electrolyte phase–an overview. *Journal of materials science* **1999**, 34, 1131-1162.

6. Reynolds, S.; Hume, W. M.; Vonnegut, B.; Schaefer, V. J., Effect of sunlight on the action of silver iodide particles as sublimation nuclei. *Bulletin of the American Meteorological Society* **1951**, 32, 47-47.

Chapter 5. Conclusion

Here I have presented a novel solid-state electrostatic doping approach to control the carrier concentration of 2D semiconductors. With this doping method, electronic properties of 2D semiconductors can be effectively tuned without degradation of their intrinsically excellent carrier transport and atomically thin 2D semiconductor crystal lattice. To demonstrate the solid-state ionic doping method, $CH_3NH_3PbI_3$ perovskite microplates have used to electrostatically dope 2D semiconductors such as single-/few-layer WSe_2 and MoS_2. The $CH_3NH_3PbI_3$ perovskite microplates were laminated on top of WSe_2 and MoS_2 semicondutor channels by which the FETs showed large p-doping effects compared to those of the FETs without the perovskite microplates. This $CH_3NH_3PbI_3$ perovskite is also well-known for low activation energy of its mobile ion components, which makes it possible to build up the charge distribution along with channel length or channel thickness inside the perovskite microplate by applying electrical poling voltages through drain terminal or back-gate terminal, respectively. After uniform poling process, an ambipolar $CH_3NH_3PbI_3$/WSe FET was reversibly switched either to n- or p-channel FETs dependent on electrical poling directions, demonstrating that mobile ions and their accumulation can electrostatically convert the major carrier type of the FETs. Moreover, with non-uniform poling process, an ambipolar $CH_3NH_3PbI_3$/WSe FET became polarity switchable diodes, which delivered a large V_{OC} up to 0.78 V. Because of the excellent optoelectronic properties of the $CH_3NH_3PbI_3$ perovskite doping agent, the device can also become a photodiode, showing EQE of 84.29% at 532 nm. Furthermore, the performance of the device can be improved by adopting Fermi-level tunable graphene as drain/source electrodes with which the device showed an enhanced V_{OC} up to 1.08 V under 532-nm laser excitation and a widely tunable EQE from 2.7 to 91.3%.

Based on the solid-state $CH_3NH_3PbI_3$ perovskite doping study, a superionic solid with a sharp solid-state phase transition was considered as an attractive candidate for achieving non-volatility of programmed functions at room temperature. Among superionic solids, AgI is particularly desirable for its unique superionic phase transition behavior where it transits from dielectric β-AgI into conductive α-AgI upon reaching 147 ˚C also known as superionic conduction phase with a sharp increase in ionic conductance by three orders of magnitude. After uniform poling process on an ambipolar AgI/WSe_2 FET, the transfer curves were reversibly shifted from ambipolar to n- or p-type behaviors dependent on the sign of back-gate voltages, confirming that the dominant carrier type of WSe_2 semiconductor channel can be effectively changed by the accumulation of mobile ions at the AgI/h-BN interface. Moreover, non-uniform doping can be achievable through drain/source electric fields to become polarity switchable diodes. These programmed diodes can also function as effective photodiodes with a V_{OC} up to 0.52 V. Unlike other ionic dopants including the $CH_3NH_3PbI_3$ perovskite and ionic liquids, the retention performance of the diode showed outstanding operational stability at room temperature. The output currents measured at certain periods of time after programming showed the stable recitification behavior at room temerpature over the experimnetal time scale, suggesting that the large ionic conductance switch associated with the sharp superionic phase transition in AgI effectively addresses volatility issue. Our findings also demonstrated that multiple ambipolar AgI/WSe_2 FETs can be combined to fabricate complementary logic gates including inverter, NAND and NOR gates. Lastly, the programmed diode function can be erased by weak UV irradiation. The diodes lost its rectification characteristics as the reduction of ionic silver to metallic silver induce by the irradiation. These controllable removal of device functions upon specific environmental triggers are of considerable interest for protecting vital information in electronic systems.