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Interference Mitigation Techniques for Communication Systems

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Interference Mitigation Techniques for Communication Systems

By

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Abstract

Interference Mitigation Techniques for Communication Systems

Wireless communication systems have been growing at a very fast rate over the last few decades. This growth has been fueled by development of cellular technologies such as 4G LTE/5G, and machine to machine communication. Growth is expected to continue especially in the machine to machine sector with the rise of Internet of Thing (IoT) in consumer electronics. Even though the number of connected devices has grown, the Radio Frequency Spectrum has not. This has resulted in a massive overcrowding of the radio frequency spectrum. Overcrowding can create massive interference in communication links and put receivers into saturation. High levels of harmonics and intermodulation distortion are generated in saturation. In this state receivers performance degrades significantly. Some of this interference is unintentional, and some could be caused by nefarious parties. Much research has been done in order to mitigate the problems caused by interference. Transceivers that utilize interference mitigation circuits tend to be more robust in heavily congested radio frequency spectrum.

In this work three different approaches are presented in dealing with in-band and out of band types of interference.

The first work reports a novel design of RF signal processing module for direct sequence spread-spectrum (DSSS) communications to effectively suppress in-band radio interference. RF signal processing can flexibly achieve DSSS spreading gain without having to modify the conventional narrowband radios. Our new design leverages low power GaN switches to spread and despread RF signals efficiently while rejecting narrowband interference at the receiver. GaN devices enable the circuitry to have high 1dB compression point of 38dBm and third-order intercept point over 48dBm. The receiver correlator also spreads incoming interference, so the system is able to perform in the presence of strong blockers. The demonstrated module is shown to suppress narrow in-band interference up to $27dB$. A unique design feature of this RF signal processing module is the use of an innovative non-coherent chip synchronization scheme for DSSS at RF that traditionally

requires baseband signal processing. The proposed design can be used in full or half duplex system. In full duplex there is additional benefit of transmitter to receiver leakage suppression that the proposed system can achieve.

Interference that fall outside the band of interest is typically taken care of by filters. Filtering can be done in digital and analog domain. Conventional analog filter have a fixed center frequency and bandwidth which can't be tuned. Modern communication system need filters that are reconfigurable in frequency and bandwidth. This work reports a tunable, high power N=4 N-Path filter. Majority of published works utilize a standard CMOS process for implantation which has power handling limitation. The N-Path filter in this work takes a heterogeneous approach to architecture design. The N-path core was designed in a GaN process, which allows for high power handling. The four phase none-overlapping clock is generated in a CMOS process. An intermediate GaN Level shifter for driving the GaN switched in N-Path core is also shown. The work also demonstrated the PCB integration methodology of the heterogeneous filter. The measurement show that the filter can be tuned from 1-1.3GHz in center frequency which simulation showing that the architecture should be able be tuned from .5GHz to 1.5GHz. Also it was demonstrated that the 3dB bandwidth is tunable from 5MHz to 20MHz. Simulation show that this heterogeneous architecture has a 1dB compression point of 18.8dBm

A full duplex system which can transmit and receive in the same frequency and time space has been of great interest since the advent of wireless communication. However, the full duplex architecture adoption is limited due to the self interference problem in where a transmitter is a strong in-band jammer to it's own receiver. In this work two independent methods for dealing with self interference are demonstrated. The first method uses tap-delays to couple off signal from the transmitter path, invert the phase with some added delay and inject it right before the LNA in the receiver path. This method was designed to have four taps. Each tap has individual amplitude and phase control. The system was designed to be modular in order to study the cancellation effects at critical points. The measured results show that an additional 20dB of isolation can be achieved over a 63MHz bandwidth, and over 30dB over 30MHz bandwidth

The second method is to use orthogonal coding in time domain to achieve deep self interference cancelling by clever selection of timing offset between the transmitter and receiver code. This type of cancellation only applies to systems that use analog correlators which are shown in the first part of this work. By doing partial timing offset, energy can be redistributed in the frequency spectrum creating bands with smaller energy concentration. There are specific timing offsets between transmitter and receiver codes that will yield a nulling effect in the receive filters pass-band. This will remove more transmitters energy than what the code originally was designed for in digital domain. Also, since the spreading sequence in the transmitter and receiver are using the same clock we can use this to find a good nulling offset, and then move the transmitter and receiver codes in tandem to recover the correct timing offset. This work demonstrated that over 50dB of isolation can be achieved by the use of this method.

Chapter 1

Introduction

1.1 Background

Wireless communication systems at radio frequency (RF) are essential to both commercial and defense applications. In the last few decades there has been a massive growth in number of devices that can emit electromagnetic radiation for the sole purpose of communication. It can be seen from the frequency allocation chart (Fig.1.1) made by National Telecommunications and Information Administration (NTIA) [1], that the electromagnetic spectrum has become extremely crowded. Due to this crowding, wireless transceivers are becoming more and more susceptible to interference. Most of the current interference is unintentional. An example of this would be two communication devices contesting for the same frequency and time space, or energy leakage from one user to another. Some of this problem can be partially mitigated by setting clear guidelines and rules on how to operate in the electromagnetic spectrum. In United State, the rules and regulation for the electromagnetic spectrum are set by National Telecommunications and Information Administration (NTIA) for military purpose, and by FCC for civilian. However, there is some interference that could be inflicted for nefarious purposes. Usually this is seen in military scenarios where a adversary intentionally tries to disrupt communication links.

Figure 1.1: United States Radio Spectrum Frequency Allocations Chart from NTIA [1]

1.2 Types of Interference

1.2.1 Co-Channel Interference

In Co-Channel Interference (CCI) many devices are attempting to operate in the same defined frequency space at the same time. The example of this type of interference is clearly seen in cellular mobile communication. A mobile phone network is typical comprised of base station that operate within a predefined geographic region that are called "cells". Each cell has specified frequency that it operates in, and when users enter the cell space they have to operate on the same frequency. However, due to limited frequency allocation for mobile provides, frequencies are typically reused in non adjacent cells. Due to poor planning, overcrowding, and natural conditions, there could be situation that users in one cell will receive the signal from different cell operating in the same frequency.

1.2.2 Adjacent channel Interference

Adjacent channel inference (ACI) is caused by transmitter leaking energy into a receiver that is operating in an adjacent frequency. For optimal efficiency power amplifiers are designed to operate in very non-linear regions and close to saturation points. These

operation requirements create energy emission in adjacent frequencies that a receiver could operate in. Channel filters are utilized to suppress out of band emission, but sometime they do a poor job in doing so.

1.2.3 Intentional Jammer Interference

Intentional emission of electromagnetic interference for the sole purpose to disrupt communication (aka jammer) can also be a concern for receivers. This occurs when a jammer transmitter output a lot of electromagnetic energy into a frequency space that a known receiver is operating in. Typical users don't have to worry about this kind of inference as there are laws that prohibit this type of behavior. However, this is of create concern in military setting. In military scenarios, communication links are vital for successfully operations. An adversary could flood the communication channels with large amount of electromagnetic energy that could desensitize or even saturate vital receivers, thus completely disrupting the communication link.

1.2.4 Self Interference

Self Interference (SI) is a phenomenon that occurs in transceiver that are operating in full duplex mode. In full duplex mode a transceiver is transmitting into the same time and frequency space that its own RX channel is receiving. Full duplex operation have been sought after for years because total throughput can be increased, collisions are avoided, and the communication link is bidirectional in time, and frequency domains Due to proximity of transceivers transmitter (TX) and receiver (RX) channels large amounts of energy from the transmitter will leak into the receiver. The leaked signal will reduce the sensitive of the receiver and if the leakage is large enough, completely saturate it. In order for full duplex to be a viable transceiver architecture, at least 110dB of isolation is needed between TX and RX [2].

1.3 Mitigation Strategy

1.3.1 Conventional Filtering

Some of the aforementioned interference is taken care of by conventional filtering. These filters are really good at taking care of interference that is outside the band of operation.

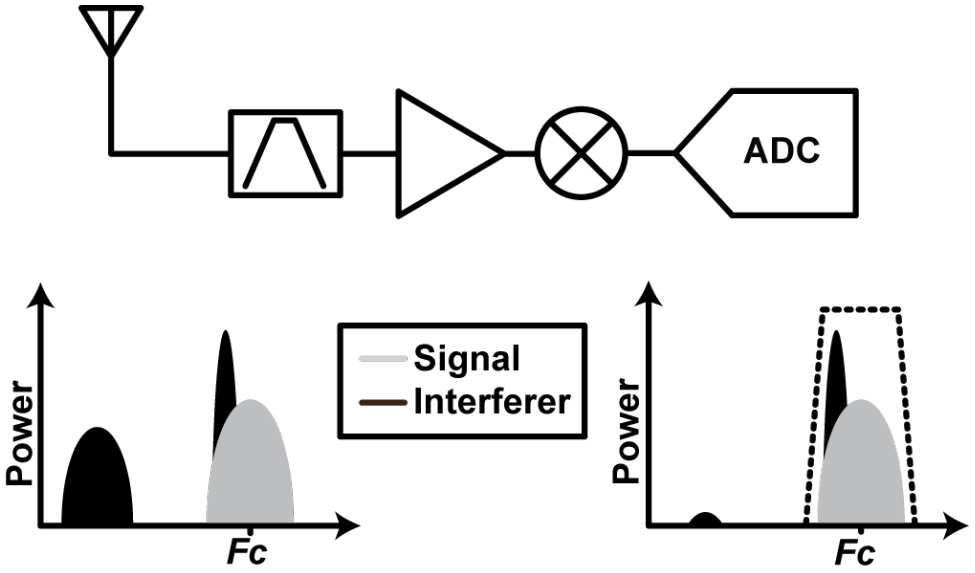


Figure 1.2: Representation of interference in the receiver chain. Out-of-band interference is filtered, but in-band interference cannot be suppressed with this approach.

Unfortunately they are useless against interference the lies directly in the band of operation. Figure 1.2 shows how the in-band and out of band interference pass through a conventional filter.

1.3.2 Frequency Hopping Spread Spectrum

One of the possible mitigation technique is to use Frequency hopping spread spectrum (FHSS). This method takes a narrow band signal and changes (hops) to a different center frequency or channels. The range of frequencies that a signal can hop to should be much larger the signal bandwidth, so that in fact the total operational bandwidth is large. From the perspective of the jammer, it either has to spread its energy to cover the whole hopping band or just focus it on a few channels. If jammer spreads to cover all the possible hopping channels then total received energy from the jammer is minimized by the number of hops. An advantage of FHSS type architecture is when a jammer is fully concentrated in a few channels, and if those channels are known, then they can be avoided.

Mousavis [3] has demonstrated successfully a 47MHop/s FHSS system at RF frequencies. The system operates in a 60MHz band which is subdivided into 100 channels that are .6Mhz wide. It was shown that with a hopping speed of 47MHops and a signal band-

width of 470kHz, 20dB of processing gain can be archived. The system utilizes a digital oscillator generator to create all the required frequency hops. The system was built using TSMCs 65nm process. The issue with using FHSS approach is that timing recovery is becomes extremely difficult, and only a few modulation schemes can work with it. There is also a max limit users that can occupy the spreaded bandwidth which is set by number of channels one can hop to. Also, for narrow band jammer avoidance, a complex spectrum sensing technique must be utilized

1.3.3 Direct Sequence Spread Spectrum

Direct Sequence Spread Spectrum (DSSS) is a method of directly multiplying the narrow band transmitted signal by a spreading sequence that has a much larger bandwidth. This has the effect of spreading the transmitted signal to a much larger bandwidths. DSSS communication, such as code-division multiple access (CDMA) is a highly effective in providing substantial spreading gain against interference with bandwidth similar to signals of interest. Conventional spread spectrum scheme is realized at the digital base-band, leaving the RF front-end still vulnerable to high-power in-band interference signals. For strong interference mitigation this technique must be realized in RF domain. Works from Agrawal. [4], Mousavi. [5], and AlShammary. [6, 7] have all show DSSS at RF frequencies. They all utilize N-Path filter realized in CMOS technology to do interference suppression. DSSS is cleverly implement in the N-Path filter by delaying or progressing all the phases of the clock with a spreading sequence. Due the low breakdown voltage of CMOS technologies, N-Path filters will always have a lower power handling ability, and thus make them unattractive for transceivers front-end. AlShammary [6, 7] did demonstrate a "chopper" stacked FET switch that can handle up to 30dBm of power, but due to the large amount of FETS used in the stack, the insertion losses are very high which is also undesirable.

1.4 This Work

The work presented here discusses different approaches for interference mitigation that fall in-band and out of band. The proposed solutions are implemented at system level. First techniques used DSSS at RF to deal with incoming strong in-band interference

leveraging GaN high power handling capabilities. Second, a system level GaN N-Path filter that is designed for high power handling is demonstrated. Third, a clever timing offset selection between transmitters and receivers orthogonal spreading codes to achieves self interference nulling.

1.4.1 In-Band Interference Mitigation

1.4.1.1 Strong In-band Interference

A novel RF system design for mitigating in-band interference is presented. Similar to the conventional CDMA systems, the proposed system relies on encoding the transmitted signals with orthogonal pseudo-random codes/sequences to allow co-existence of multiple users and the elimination of in-band interference. We hence name the proposed system "RF-CDMA" system. Unlike a conventional CDMA system, the encoding and subsequent decoding/correlation of the signals are carried out directly at the RF frequency. As such, in-band interference is eliminated before hitting the sensitive receiver front-end. Compared to similar works [4–7], the proposed system utilizes high-power handling GaN RF switches as the fundamental building block of the correlators, thus allowing exceptional system power handling capabilities. The work also demonstrate a non-coherent timing recovery algorithm that find code alignment offset that achieves maximum correlation between two users in analog domain.

1.4.1.2 Self Interference

For transceiver systems that are designed to operate in simultaneous transmit and receive (STAR) or full-duplex mode, signals from transmitter can desensitize own receiver due to the large leaked power level. In Chapter 8 two different approaches that deal with self interference are investigated.

The first approach uses traditional method of tapping off a small amount of the transmitter signal, inverting it and injecting it back into the receiver. The idea is that this approach can negatively match the amplitude and delay of the leaked paths and cancel them out at the input into the receiver in order to protect it.

The second approach uses a novel code domain alignment technique to shape the frequency spectrum in order to minimize the self interference energy that fall in band of

the receive filter. This is done by selectively aligning the orthogonal codes between own TX and RX to achieve desired spectrum shaping.

Both of the approaches are implemented and demonstrated individually. Since the two approaches for self interference mitigation are mutually exclusive, the two are put together to demonstrate their combined cancellation of leaked transmitter to receiver power.

1.4.2 Out-Band Interference Mitigation

1.4.2.1 GaN N-Path Filter

In Chapter 7 a high power handling N-Path filter is presented. The filter design is heterogeneous system integration approach between GaN and CMOS technologies. Integration of CMOS and GaN capitalizes on GaN's high power handling capabilities, and CMOS digital clock generation. The N-Path utilizes GaN switch core with ability to switch between different capacitor banks in-order to change filters bandwidth. Also, different GaN driver circuitry is demonstrate in order to drive the GaN switches to appropriate voltage levels at fast speeds. A CMOS clock is demonstrated that is specifically designed to integrate with GaN. Lastly, different integration consideration are taken into account such as wire-bonding and PCB material layout in order to archive tight GaN-CMOS on PCB integration

Chapter 2

Concept of Spread Spectrum at RF

2.1 Direct Sequence Spread Spectrum at RF

In communication systems, interference signals can cause degradation to the desired signal. When the power of the interference signal is significantly larger than the desired signal and surpasses the point where gain starts to compress, the desired signal will no longer be receivable. Interference signals that fall outside the band of operation can be attenuated by the use of bandpass filters. Unfortunately, this method does not work for unwarranted signals that fall inside the passband. Figure 1.2 depicts these two situations.

Although there are different methods to deal with in-band interference, the most widely used method is to utilize spread spectrum schemes. In this method the message signal is stretched (spreaded) into a larger bandwidth with equal total power, and is reconstructed (de-spreadeded) accordingly in the receiver. Direct-sequence spread spectrum (DSSS) and Frequency hopping spread spectrum (FHSS) are some of the ways frequency bandwidth spreading can be done. DSSS is the most common of these schemes, and works as follows: at the transmitter, the message signal with bandwidth B_s modulates a periodic sequence (also known as spreading code) with bandwidth $B_c = B_s L$, where L is known as the spreading gain. The resulting signal has bandwidth $B = B_s + B_c$ and the total power initial initially concentrated in the B_s spectrum is spread to B. In a corresponding receiver, subject to interference, the same sequence is used to demodulate the incoming signal. This computes a correlation between transmitter and receiver sequences. After demodulation,

the transmitted signal is reconstructed into the original message and filtered to remove out-of-band components. Additionally, the in-band interferer has not been previously encoded, so its is modulated by the receiver sequence, and after the filter, its in-band power is reduced by a factor of L.

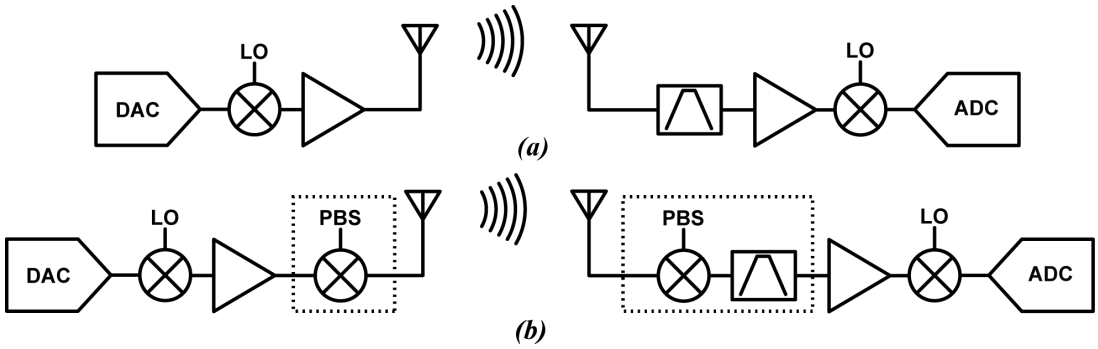


Figure 2.1: Comparison of transmitter and receiver architectures a) without and b) with Direct Sequence Spread Spectrum at RF

2.1.1 Digital Correlator

In a conventional DSSS system, shown in Figure 2.1a, both spreading and de-spreading are implemented at baseband frequencies in the digital domain. The spreading sequence $c[k]$ is commonly a binary code with polar signaling that changes at a rate $1/T_c$, where T_c is known as chip period. There are L chips within a symbol duration of T_s, and $L = T_s/T_c = B_c/B_s$. The message signal $s[n]$ is upsampled and modulates the spreading sequence, and the resulting modulated signal is

$$x[k] = s[k]c[k], \quad k \text{ in terms of } T_c. \tag{2.1}$$

The analog frontends of both DSSS transceivers need to handle the bandwidth $B = B_s + B_c$ of the spreaded signal $x[k]$. Digital approach works well with relatively low interference power and small bandwidths.

2.1.2 Analog Correlator

Problems start arising when the in-band interference power becomes too large, or when large processing gains are required leading to wideband spreading codes. In a typical receiver's architecture, the antenna is followed by an adjacent channel filter (ACF) and a

low noise amplifier (LNA), which usually has low compression point. When a interference signal is larger than the compression point of the LNA, no useful signal can be recovered because the LNA will be saturated. Another issue with the conventional method is that in order to fully achieve the desired processing gain for wideband signals, the hardware components need to operate over the full bandwidth B, which increases the complexity of all the component designs.

In this work an alternative method is proposed to conventional DSSS systems which is a analog implementation of DSSS directly in the RF domain. Specifically, the direct-sequence modulator is placed between a non-spreading transmitter and its antenna, and the demodulator is located between a corresponding receiver and its antenna, as depicted in Figure 2.1b. The RF direct-sequence modulator uses the RF signal $s_{\mathrm{RF}}(t)$ (commonly a QAM signal) to modulate an analog binary polar sequence $c(t)$, such that the modulated signal is

$$x(t) = s_{\mathrm{RF}}(t)c(t). \tag{2.2}$$

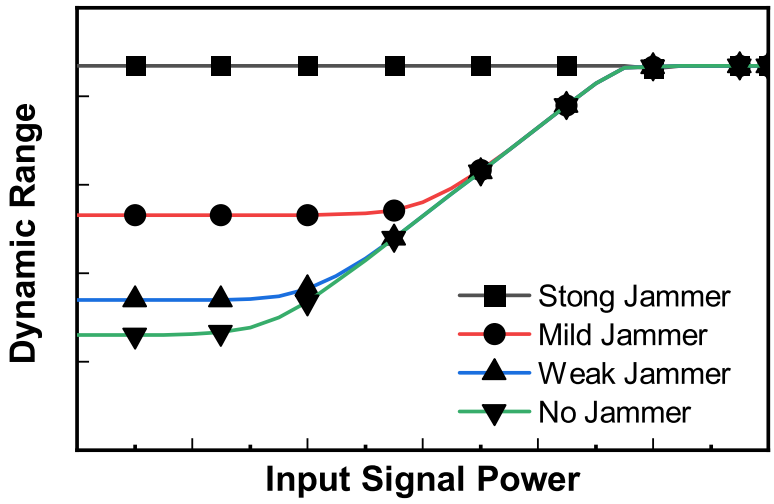
Under interference, the RF direct-sequence demodulator in the receiver acts before down converting the received signal, which is the sum of the transmitted signal $x(t)$ and an interferer $q(t)$):

$$r(t) = (s_{\mathrm{RF}}(t)c(t) + q(t))c(t) = s_{\mathrm{RF}}(t) + q(t)c(t). \tag{2.3}$$

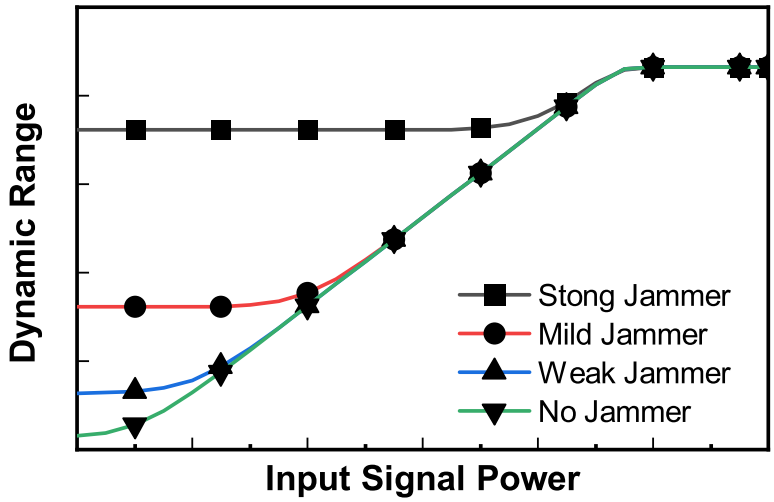
Thus, the signal is recovered in to a bandwidth of B_s and the interference signal is spreaded to a bandwidth of B_c. After the multiplication in the RF correlator, the $r(t)$ passes through a narrow bandpass filter that has a bandwidth of B_s. After this filter, the received signal $r(t)'$ contains the fully recovered S_{RF} and the interference signal that has decreases by a factor of B_s/B_c or $1/L$.

$$r(t)' = s_{\mathrm{RF}}(t) + q(t)/L. \tag{2.4}$$

RF DSSS approach overcomes the two aforementioned disadvantages of digital base-band implementations, by relaxing the design requirements of the hardware, and allowing larger interferer power before reaching saturation. One way to see the latter effect is to



(a)



(b)

Figure 2.2: Dynamic range of a receiver with DSSS and different interference conditions. (a) Conventional digital DSSS system showing dynamic range saturation with strong jammer. (b) RF DSSS system extending extended dynamic in the presence of the same strong jammer range.

study the dynamic range of the system under interference, for both digital and RF DSSS systems. System level simulations were performed in AWR's Visual System Simulator using ideal correlators and filters. The results are shown in Figure 2.2. There are two way

that the dynamic range of the system is improved. First, the power of the in-band jammer is reduced because it gets spread outside the receivers filter which buys the receiver more headroom on the upper end. The second way dynamic range is increased is by reducing the overall noise floor of the receiver by making the ADC bandwidth requirement smaller because despreading now happens in the analog domain and not the digital. Due to the narrowing of the ADC bandwidth, the lower end of the dynamic range is extended for input signal with no jammer and is shown in Figure 2.2b. Equation 2.5 show how the bandwidth affects the minimum detectable signal of the receiver, this is also know as receivers sensitivity.

$$P_{sen} = -174dB/Hz + Noise\,Figure + 10Log(Bandwidth) + Signal\,Noise\,Ratio \quad (2.5)$$

The simulation did use lossless correlators/filters that were added to the receivers front. In reality these components will have some loss, and will degrade receivers Noise Figure (NF). The reader should be aware that there is some trade off of using this method.

2.2 DSSS in full duplex systems

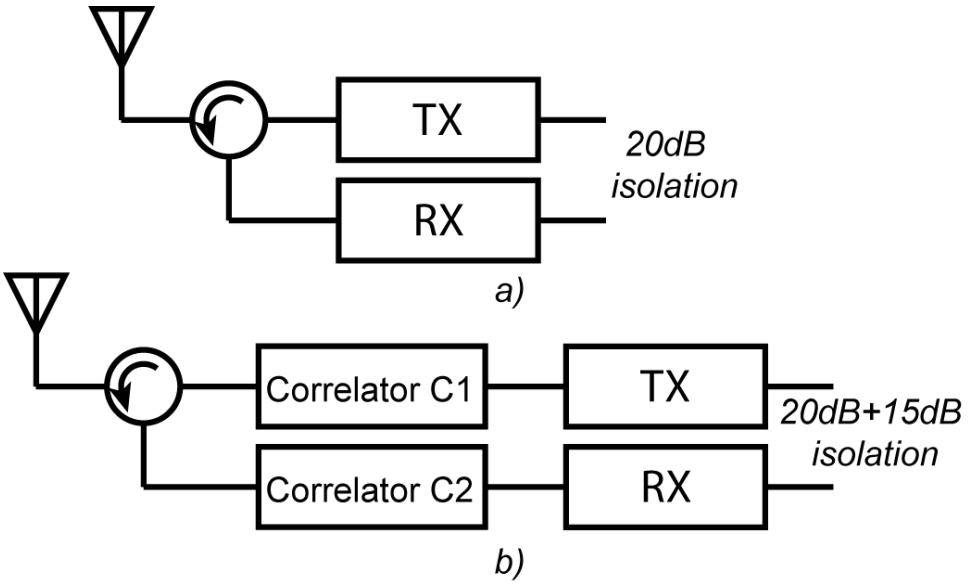


Figure 2.3: Full duplex systems a) typical full duplexes system that has 20dB of isolation from the circulator. b) show the full duplex system with the correlators that have orthogonal codes $C1(t)$ and $C2(t)$

A full duplex system also benefits from having correlators placed at front end of the transceiver chain. In a typical full duplex operation, large isolation is required between TX and RX (90dB+) in order to receive signals with reasonable fidelity. A circulator can provide around 20dB of TX to RX isolation Figure 2.3a and is insufficient thus places greater pressure to do cancellation at the backend. By placing correlators at the front of the TX and RX chain (Figure 2.3b), and choosing the codes between them to be orthogonal, additional cancellation can be achieved depending on the code length selection. Self interference cancellation requirement, to be done in digital domain, is greatly reduced by this method.

Chapter 3

System Design

3.1 Spreading Sequence Selection

The performance of a DSSS system is defined by the particular spreading sequence $c(t)$ that it uses. To properly de-spread the transmitted signal, the receiver direct-sequence demodulator needs to be synchronized with the transmitter so the application of the spreading sequence on the receiver matches in time with the transmitted sequence embedded in the received signal. If this does not happen and there is a timing offset, the quality of the de-spread signal decreases, due to its close relation to the correlation of the spreading sequence $c(t)$, which degrades with larger timing offsets [8].

Moreover, the channel can be shared by several simultaneous users, each one with its own spreading sequence to avoid system self-interference. Thus, the spreading sequences need the following key properties:

1. The autocorrelation of each sequence should resemble an impulse, i.e. it should have a single narrow peak, significantly larger than other values.

2. Two distinct sequences should have very low crosscorrelation regardless of timing offset.

There is no finite sequence that can achieve both perfect autocorrelation and cross-correlation, but there are known finite sequence families that can achieve either one or a tradeoff of both, such as maximum-length sequences, Gold sequences [9], Kasami sequences [10], Barker codes [11], and others. In particular, Walsh-Hadamard sequences

(used in CDMA systems) require full synchronization of all users to exploit orthogonality [12] and do not have a single narrow autocorrelation peak, and thus they are not suited as spreading codes for our system.

3.1.1 Maximally long Sequence

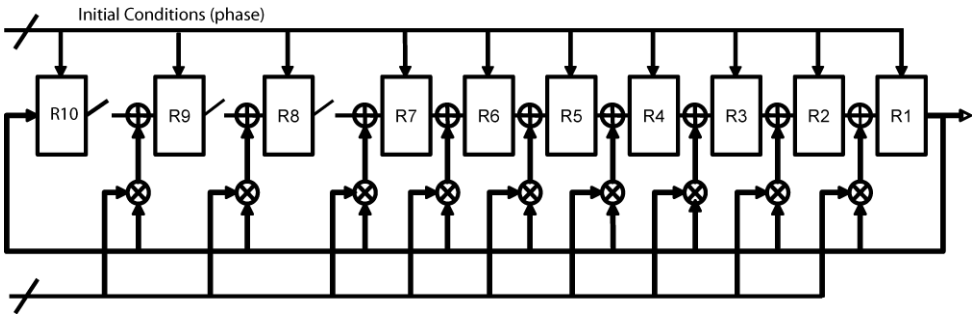


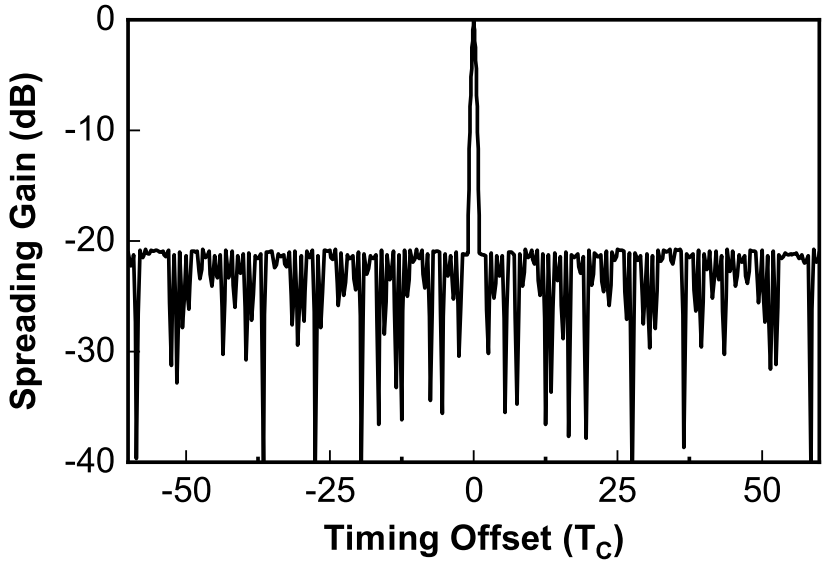
Figure 3.1: Linear feedback shift register structure that can generate maximal sequences of lengths $2^7 - 1$ through $2^{10} - 1$

To avoid the implementation of complex analog RF multipliers in the direct-sequence modulators, only polar binary codes will be considered (discarding families such as Zadoff-Chu sequences). Additionally, we require balanced codes (that have a similar number of positive and negative chips) to avoid DC components in the spreaded signal.

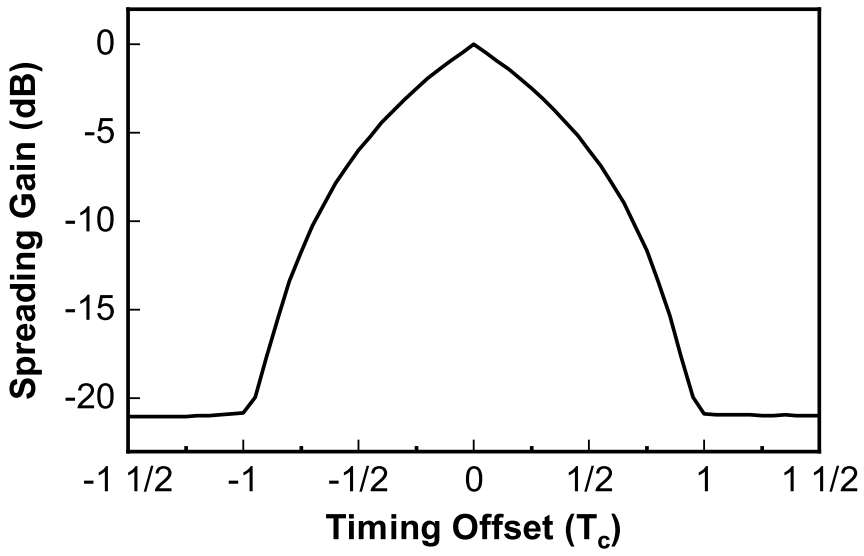
As an example, this work shows simulations using maximal-length sequences due to their impulse-like autocorrelation and low crosscorrelation. Maximal-length sequence can be generated by using a series of linear feedback shift registers (LSFR) shown in Figure 3.1. The LSFR shown can generate code lengths of $2^7 - 1$ through $2^{10} - 1$. Different feedback taps will generate different codes within a family, but not all codes that are generated are of maximal length. In particular, a sequence length of 127 chips is chosen to achieve at least 20dB of spreading gain. Figure 3.2 shows the simulated in-band energy across timing offsets, with respect to the in-band energy in perfect synchronization (0dB). In one chip time, the in-band energy is reduced by a factor of the sequence length L, and timing offsets larger than one chip show more than 20dB of attenuation across the board.

3.1.2 Gold Sequence

Unfortunately, maximal-length sequences do not allow for many concurrent signals be detected. There is a limit of how many preferred pairs can exist for a given code length [13].



(a)



(b)

Figure 3.2: Simulated in-band energy of the despreaded signal with respect to timing offsets, in multiples of chip time T_c. (a) Whole range of possible timing offsets in one symbol time. (b) Magnified version showing the single narrow peak in the in-band energy.

Therefore, we transitioned to Gold codes [14] to allow for a larger number of concurrent users to be detected with the expected interference rejection. Figure 3.3 shows how to generate Gold sequence of lengths $2^7 - 1$ through $2^{10} - 1$. Two LSFRs generate two

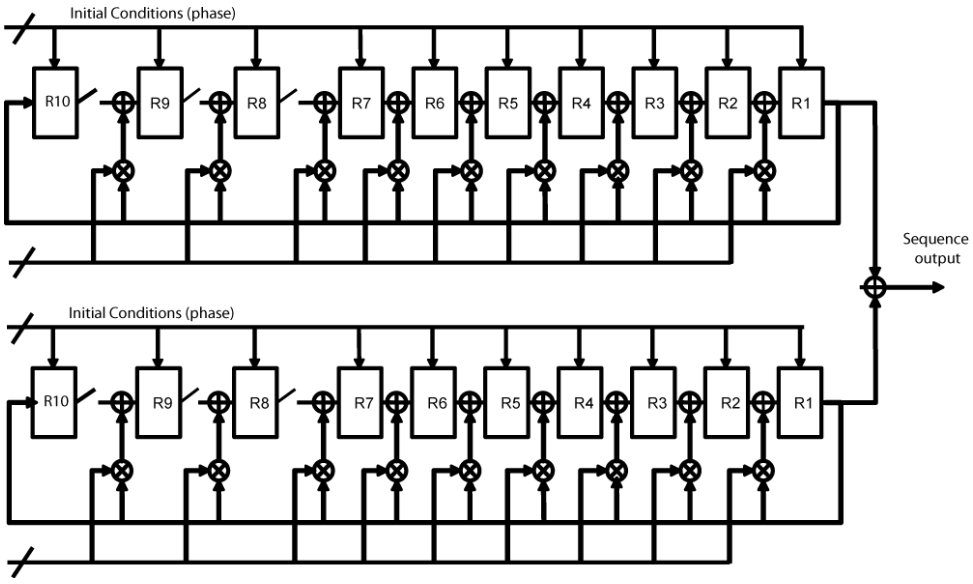


Figure 3.3: Two linear feedback shift registers that generate two different maximal sequences of lengths $2^7 - 1$ through $2^{10} - 1$ combined to make a Gold sequence

independent maximal-length sequences and are added together at the output to create a Gold sequence.

3.2 Timing recovery

As previously stated, the direct-sequence modulator and demodulator need to be synchronized to achieve the desired performance in terms of spreading and de-spreading. Thus, good timing synchronization is key to the performance of the system. In traditional receivers, timing recovery requires carrier recovery that often utilizes baseband pilot signals. Hence, typical timing synchronization relies on information from the receiver baseband information.

A standalone RF signal processing system requires to synchronize the direct-sequence correlators independently of baseband information. Therefore, the proposed system considers a non-coherent timing synchronization scheme based on the level of narrow-band signal energy after de-spreading. This approach further reinforces the use of spreading sequences with a single, narrow autocorrelation peak for code synchronization.

Figure 3.4 depicts a diagram of our proposed timing recovery algorithm. The flow chart for the algorithm can be also be seen in Figure 3.5. The key part of the algorithm

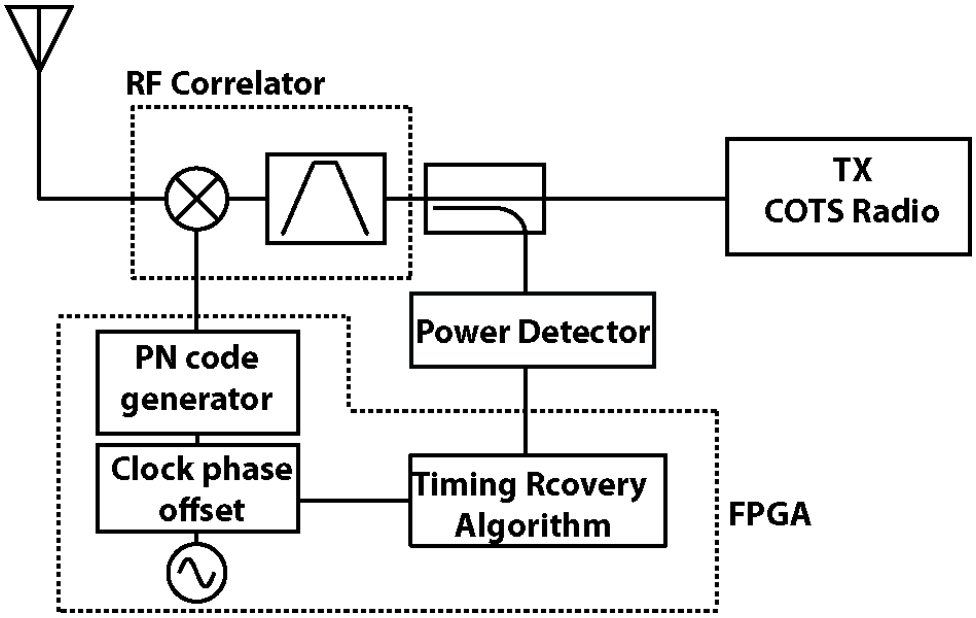


Figure 3.4: Non-coherent timing recovery algorithm for sequence synchronization at RF.

is the ability to do dynamic thresholding. When the algorithm start up initially, there is no baseline for the energies levels that will be received. To set the baseline, the algorithm first programs the receiver with a sequence $d(t)$ that is quasi-orthogonal to $c(t)$. This is used to de-spread the same received signal and to provide a baseline energy reference. This reference level will be stored. Next, the receiver switches to the true spreading sequence $c(t)$ to perform a time-domain search for correct timing, adjusting the offset of the receiver's $c(t)$ by discrete steps until the non-coherently received signal energy exceeds a dynamic threshold that is a function of the reference level. This detection algorithm helps reduce false alarms without having to accurately detect the signal power and interference level prior to timing estimation. The adjustment of timing is further improved by having multiple stages with different step sizes and thresholds, allowing for a finer synchronization and a faster overall response.

3.3 Transmitter spectral mask

The use of binary codes yields an effective rectangular pulse shaping for each chip time T_c, which has a power spectral density with shape $sinc^2$, known to have a small roll-off factor and significant bandwidth. This is problematic as the transmitted signal could

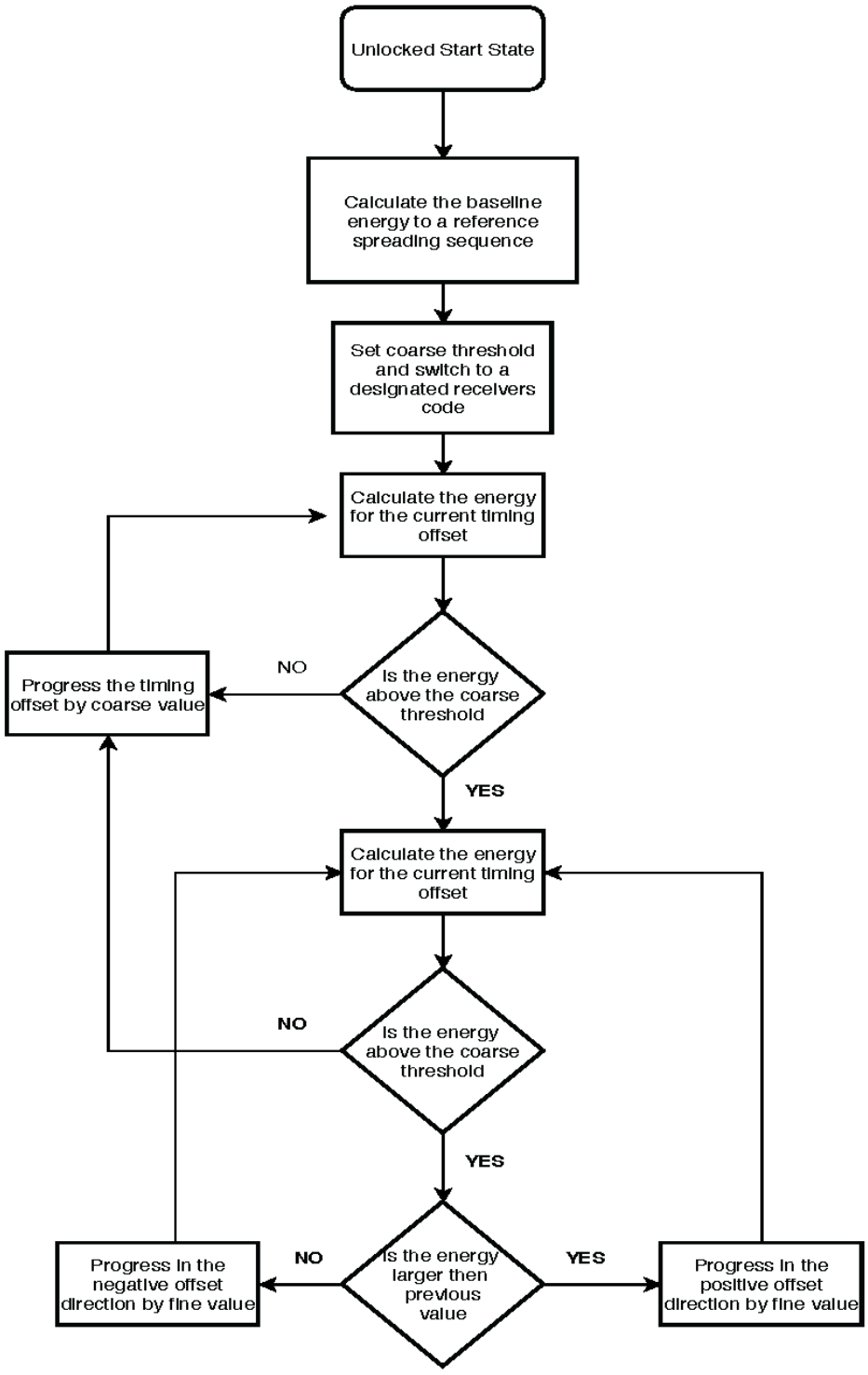


Figure 3.5: Algorithm flow chart for the timing recovery in RF Correlators. Algorithm shows dynamic thresholding, coarse stepping, and fine stepping.

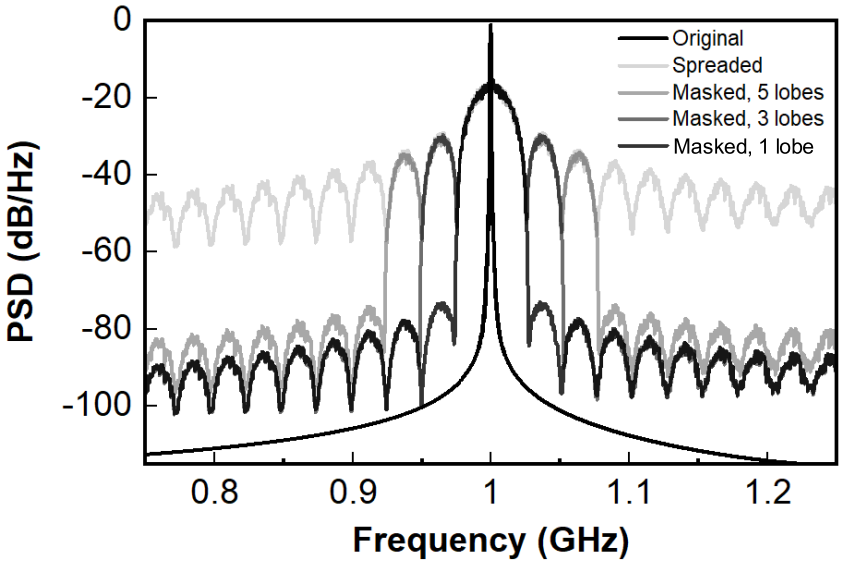


Figure 3.6: Transmitted signal using different spectral mask filters to reduce transmitted side lobes.

have a significant impact on systems operating in neighboring bands. To counter this, a spectral mask is applied to the spreaded signal at the transmitter using a bandpass filter, effectively discarding a large portion of out-of-band emissions. In this work simulations were performed of the system with different bandwidths of the spectral mask filter. In particular, and avoiding significant distortion of the transmitted spread signal, the tested bandwidths correspond to full lobes of the PSD of the spread signal. The $sinc^2$ PSD is centered at the carrier frequency and has nulls at every non-zero multiple of B_s. In particular, simulation used filters with bandwidth equal to B_s (main lobe), $2B_s$ (3 lobes) and $3B_s$ (5 lobes). The resulting narrowband energy at the input of the timing synchronization scheme is shown in Figure 3.6 for the different filters.

The fraction of signal energy after each tested filter and the resulting loss of spreading gain in the receiver are shown in Table 3.1. The main lobe by itself contains around 90% of the energy of the transmitted signal, which results in an attenuation of ∼0.44dB at the input of the timing synchronization scheme. Figure 3.7 shows the in-band energy over timing offsets, under the use of the spectral mask filters mentioned above.

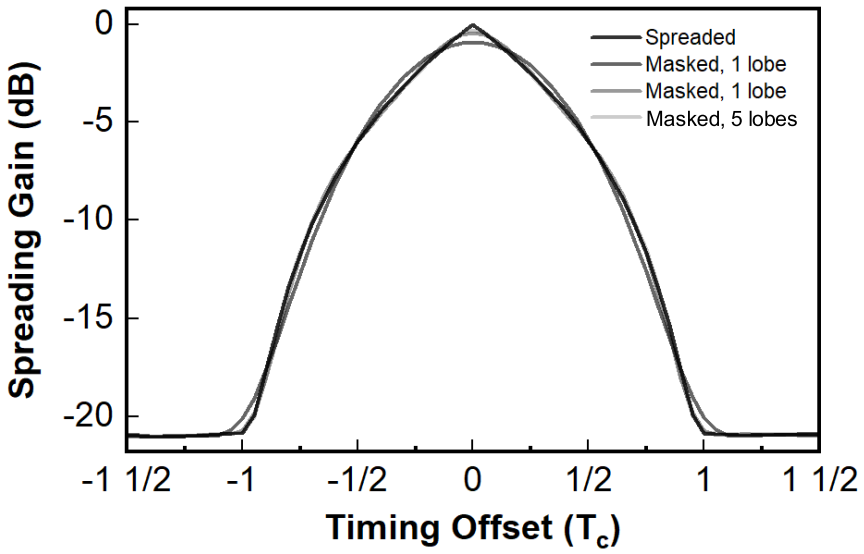


Figure 3.7: Simulation of in-band energy of the despreaded signal vs timing offset when using different spectral mask filters are applied. This shows that there is no significant difference between keeping all the energy or 1, 3, 5 of the spread lobes

Spectral Mask	1 lobe	3 lobes	5 lobes
Energy Loss	90.28%	94.99%	96.64%
	(-0.44dB)	(-0.22dB)	(-0.14dB)

Table 3.1: Energy loss of transmitted signals using spectral mask filters, with respect to transmission with no spectral mask.

3.4 Effect of Multipath

Wireless communications are subject to channel impairments, which are usually countered with several techniques in both analog and digital domain of the receiver. Nevertheless, in general, current receiver design places most of these corrections at the digital baseband domain.

For our standalone timing recovery algorithm, it needs to be robust against channel impairments with no baseband information. The algorithm cannot rely on channel gain estimates and it does not know if the channel presents significant multipath. To study the effect of multipath, we model a 2-path channel of the form

$$h(t) = \alpha_0\delta(t) + \alpha_1\delta(t-\tau), \quad \sqrt{|\alpha_0|^2 + |\alpha_1|^2} = 1, \tag{3.1}$$

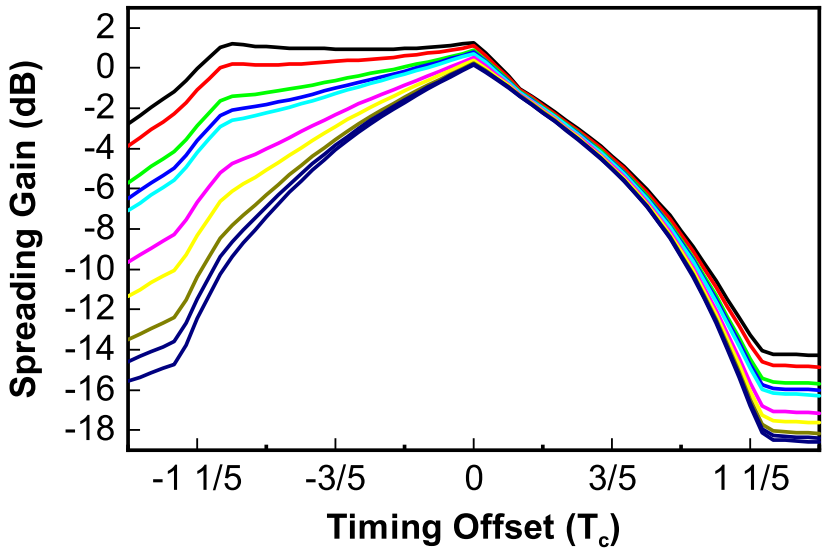


Figure 3.8: Simulated fist delay secondary path with variable gain, in multiples of chip time T_c.

where α_0 and α_1 are the path gains, and τ is the delay of the second path. With this model, there are two scenarios:

1. If the path delay satisfies $|\tau| \geq 2T_c$, the resulting inband energy will show 2 distinct peaks, each corresponding to one path of the channel. Depending on the path gains and the reference level, the timing recovery algorithm will lock onto a time offset corresponding to the first path that satisfies the dynamic threshold condition, and the other path will be severely attenuated at least by a factor of L thanks to the autocorrelation properties of the spreading sequence $c(t)$ (see Fig.3.2a).

2. On the other hand, if the path delay $|\tau| < 2T_c$, both inband energy peaks will overlap. Fig.3.9 shows this effect for $\tau \approx 1.03T_c$ and different path gain settings. The narrow peak of inband energy is increasingly distorted with increasing path gain α_1. However, the timing algorithm operates by a time-domain search with discrete steps, and as such it will observe only one of the edges of the distorted peak and activate the first thresholding stage. When the next threshold activates, the algorithm will still look for a local maximum value of the peak, regardless of the existence of other local or global maxima. Therefore, depending on the path gains,

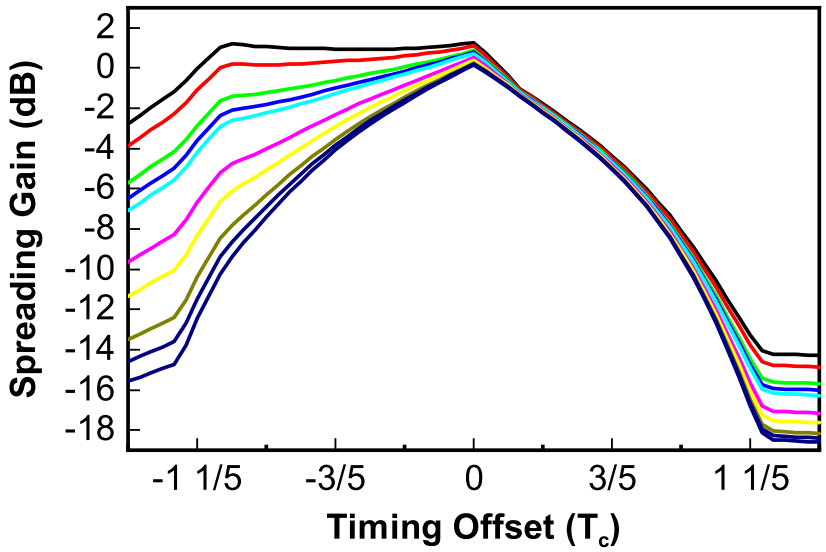


Figure 3.9: Simulated fist delay secondary path with variable gain, in multiples of chip time T_c.

it will lock on one of the paths with interference of the other. This interference will become significant if the path delay is close to the original path, e.g., in Fig.3.2b, for $|\tau| \leq 0.5T_c$ the attenuation is less than 8dB.

Overall, channel multipath will have a rather small effect on the timing recovery algorithm, and it will eventually recover the timing offset in one path only (the first one that is found that satisfies the dynamic threshold). Only in cases where the path delays are very small, the system performance might deteriorate, as the timing recovery may not be as precise, and the attenuated signal from the other path could degrade the quality of the recovered signal at baseband.

3.5 Analog Spread Spectrum Analysis

To understand how the RF correlator improves the dynamic range of a receiver, we model the non-linear behavior of the low-noise amplifier on the received signals. Usually, RF amplifiers are compressive in nature. In particular, a receiver's low noise amplifier can be modeled as a simple third order polynomial [15], i.e., for any given input signal $x(t)$, the

output of the amplifier $y(t)$ is given by

$$y(t) \approx \alpha x(t) + \beta x(t)^2 + \gamma x(t)^3. \tag{3.2}$$

First, assume that the input is a single-sinusoid jammer, which we model as

$$x_{\text{jam}}(t) = A\cos(\omega t), \tag{3.3}$$

and the corresponding output of the low-noise amplifier is

$$\begin{aligned} y_{\text{jam}}(t) \approx \frac{\beta A^2}{2} + \left(\alpha A + \frac{3\gamma A^3}{4}\right)\cos(\omega t) \\ + \frac{\beta A^2}{2}\cos(2\omega t) + \frac{\gamma A^3}{4}\cos(3\omega t). \end{aligned} \tag{3.4}$$

After removing the DC component and high order harmonics with conventional filtering, Eq.(3.4) states that the fundamental sinusoid of the output will exhibit compressive behavior if $\alpha\gamma < 0$. As the input amplitude A becomes significantly large, the gain of the fundamental will no longer be linear, and eventually the input amplitude A is so large that the amplifier will not exhibit any gain. This is called the *saturation point* of the amplifier.

Assume that for a given LNA the saturation point is reached when the amplitude of the jammer as defined in Eq.(3.4) is A_o. From this assumption, the amplitude of the fundamental component after amplification is

$$y(t)_{\text{fundamental}} = \left(\alpha A_o + \frac{3\gamma A_o^3}{4}\right)\cos(\omega t), \tag{3.5}$$

and, at the saturation point, no more amplification can be achieved, i.e. any desired input signal will not have any gain. If there is any wanted low power signal it will not be amplified due to the fact the signal will not have a gain.

Now consider a system that uses a correlation function and filter in the RF domain right before the LNA, as shown in Fig.2.1b. The same jammer signal with the amplitude A_o is applied to the input. The jammer will be multiplied by the spreading sequence $c(t)$ of length L chips, with each chip T_c seconds long. The output of the correlator becomes

$$y(t)_{\text{corr}} = c(t)A_o\cos(\omega_o t). \tag{3.6}$$

Since $c(t)$ is periodic. we use its Fourier series representation [16] and we can rewrite

$$y(t)_{\text{corr}} = \sum_{n=-\infty}^{\infty} D_n A_o \mathrm{e}^{jn\omega_s t} \cos(\omega_o t). \tag{3.7}$$

$$D_n = \frac{1}{T_s} \int_{T_s} c(t) \mathrm{e}^{-jn\omega_s t} dt \tag{3.8}$$

Where ω_s is the period of the spreading sequence $c(t)$ and ω_o is the center frequency of the receiver front-end. We also choose the chip time to be a fraction of a symbol time.

$$T_c = \frac{T_s}{L} = \frac{2\pi}{L\omega_s} = \frac{1}{Lf_s} \tag{3.9}$$

In frequency domain, this signal has been spread over a bandwidth of $B_c = 1/T_c = 1/LT_s$, and a large portion of its energy is relatively far from the center frequency. Signal $y(t)_{corr}$ can be expressed in frequency domain as

$$Y(f)_{\text{corr}} = \sum_{n=-\infty}^{\infty} D_n A_o \frac{2\pi}{2} (\delta(\omega - nL\omega_c - \omega_o) + \delta(\omega - nL\omega_c - \omega_o)) \tag{3.10}$$

Examining equation 3.10 we can see that the spectrum is just made of a train of weighted impulses centered around ω_o. We can think of this as spreading of original signal in frequency domain.

After spreading, we filter the incoming signal with a ideal bandpass filter. This filter is not possible real world implementation dude to the infinite delay. For this example we can assume that it is possible to implement these type of filters. The filter has complete out of band rejection. The frequency response of this filter is given by

$$H(f) = \text{rect}\left(\frac{f}{2f_{cH}}\right) - \text{rect}\left(\frac{f}{2f_{cL}}\right), \tag{3.11}$$

where the bandwidth of the filter is defined as $f_{cH} - f_{cL} = 1/T_s = L/T_c = \omega_s/2\pi$ and the center band of the filter $(f_{cH} + f_{cL})/2$ is also the center band of the receiver.

Because the bandwidth of filter is L times smaller the spread bandwidth, only the first impulse is kept. This means that first coefficient of the Fourier series is kept while all other become discarded.

$$D_0 = \frac{1}{T_s}\int_{T_s} c(t)\mathrm{e}^0 dt = \frac{1}{T_s}\int_{T_s} c(t)dt \tag{3.12}$$

Since the $c(t)$ sequence is selected to be pseudo random the integral over T_s will yield and Equation 3.12

$$D_0 = \frac{T_c}{T_s} = \frac{T_c}{L * T_c} = \frac{1}{L} \tag{3.13}$$

This means that the output of the filter becomes

$$Y(f)_{\text{filter}} = \frac{A_o}{L}\frac{2\pi}{2}(\delta(\omega - \omega_o) + \delta(\omega - \omega_o)) \tag{3.14}$$

Or in time domain

$$y(t)_{\text{filter}} = \frac{A_0}{L}\cos(\omega_o t). \tag{3.15}$$

This example clearly shows that the jammer is reduced by a factor of $1/L$ before it seen the LNA. The ratio of chip time and symbol time $L = T_s/T_c$ dictates how much of the jammer can be removed. In theory we can make this ratio very large and achieve very large removal of jammer signal. However in real application this is limited by how fast the multiplication can done.

3.6 Noise Figure Analysis for Analog Spread Spectrum

The method for analog spread spectrum method become unattractive for applications where noise figure (NF) is of great importance. The example was done with ideal correlator and ideal filter which have no loss. In reality these components will have loss. The downside of using this method to protect the LNA is that we will pay a price in noise figure (NF). In a receiver chain, LNA's are usually placed in front of transmitters to suppress the following components noise contribution. The cascaded noise figure of the receiver is give by Friis equation which comes from [17].

$$NF_{total} = 1 + (NF_{LNA} - 1) + \frac{NF_{Next_C MP} - 1}{A_{LNA}} + ... + \frac{NF_{N_{th}stage} - 1}{A_{LNA}...A_{N_{th}-1stage}} \tag{3.16}$$

From this equation we can see that gain of the LNA suppress all the following components NF contributions. This make the receivers LNA requirement to have the lowest noise figure possible while achieving maximum gain.

However, receivers that utilize the analog spread spectrum method will have a much higher NF. The reason is that implementation of the correlation function and integration will be passive with some loss. The benefit of having a high gain first will diminished significantly.

$$NF_{total\,RFCorr} = 1 + (NF_{RFCorrm} - 1) + \frac{NF_{LNA} - 1}{A_{RFCorr}} + ... + \frac{NF_{N_{th}stage} - 1}{A_{RFCorr}...A_{N_{th}-1stage}} \quad (3.17)$$

Analog spread spectrum clearly has clear implication in improving the dynamic range of receivers by removing large amount of in-band jammers, but at a cost of a larger NF. Carefully consideration needs to be taken when a low NF receiver architecture becomes critical.

Chapter 4

Circuit Design

4.1 Analog Correlation Function Implementation

4.1.1 Chopper

The RF correlator circuit can be implemented using two single pull double throw switches (SPDT). This is shown in Fig. 4.1. The input to the correlator is a differential signal with the output being cross coupled. This allows the phase of the signal to be encoded/decoded according to $c(t)$ spreading sequence. For each chip in the sequence one of the SPDT tran-

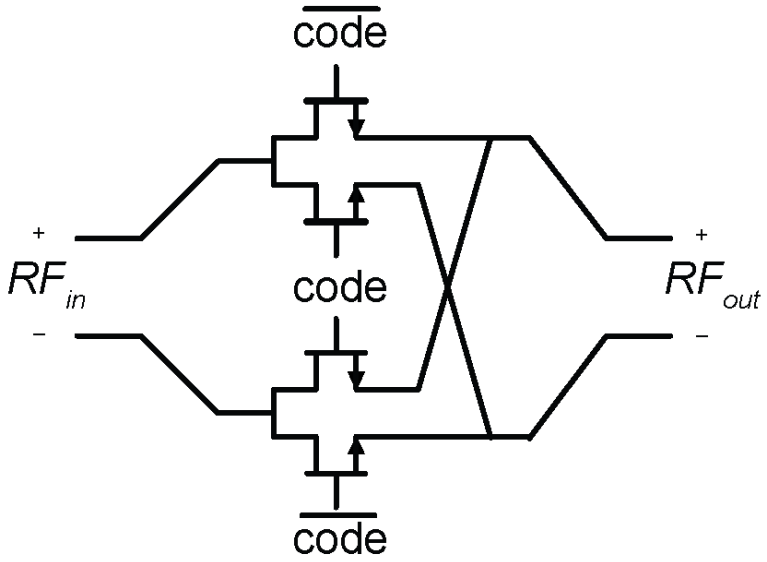


Figure 4.1: RF Correlator: Two single pull double throw switches connected differently with a cross coupled output.

sistors will be in the ON state and the other in the OFF state. This requires the spreading sequence to have two control voltages one regular $c(t)$ and the other complimentary $\overline{c(t)}$. When a particulate bit of the spreading sequence is $+1$ then RF_{out} is the same as RF_{in}, but when the bit is -1 then the output becomes crossed. This means that $-1 * RF_{in}$ occurs, which is an 180 degree phase shifted. This give us the ability to do binary multiplication at RF.

4.2 Switch Requirements

There are three criteria that govern the type of architecture that is used to design an RF correlator. They are low loss, power handling and speed.

RF correlators need to have low insertion loss since they will be placed right after the power amplifier in the transmitter chain and before the LNA in the receiver chain. Ideally the correlators should not dissipate any transmit power or contribute to the receivers overall noise figure (NF).

The large power requirement is set by the TX power amplifiers as well as the possible large in-band jammers. Since the RF correlator goes into place after the power amplifier and before the antenna, it needs to be able to handle the max output power of the PA.

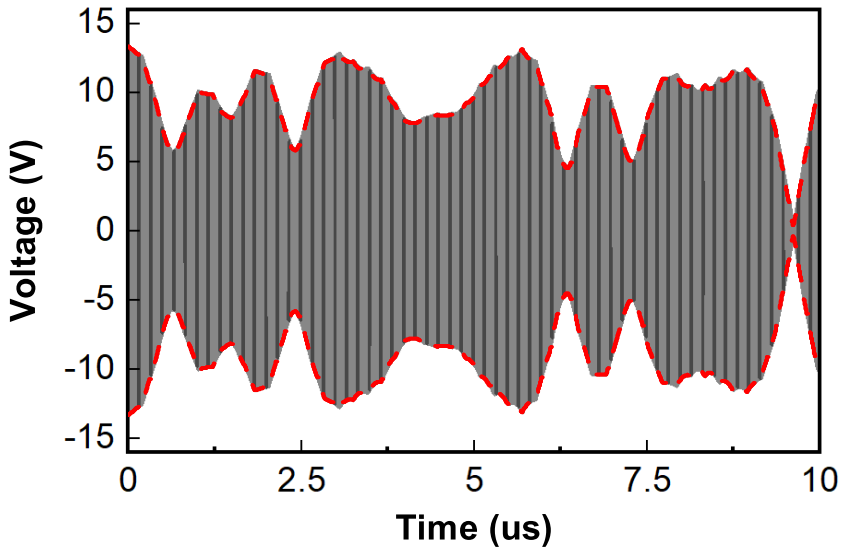


Figure 4.2: 30dBm 1GHz QPSK voltage waveform on a 50Ω load.

Figure 4.2 shows 30dBm QPSK voltage waveform. In the presence of these types of powers the RF correlator must be able to operate in the linear region. In a communication systems +30dBm of output power is typical. Some may question the need of a RF correlator in the TX chain when spreading can be done in digital domain before the DAC. However, there is a distinct benefit that a RF correlator provides, all components can stay relatively narrow band thus reducing the design requirement on the TX chain. Since a spreading factor of 10-100 is desired, all the components before or after the RF correlator can have 10-100x smaller bandwidth compared to what is being transmitted.

This brings us to the third design requirement which is switching speed. To ensure good signal fidelity the rise and fall time should be one tenth of a chip time. It can be seen in the RF correlator schematic in Figure. 4.1 that during a chip transition there will be some time that all switches are in a transition state. During this state all the transistors will be partially OFF or ON. This creates a temporary RF short at the RF output. This transition period needs to be minimized by selecting a faster switch.

These requirements are challenging to satisfy simultaneous, specifically the power handling and switching speed. The reason that power handling and switching speed can't be satisfied concurrently is they divaricate. A larger device will have high power handling, low insertion loss, and slow switching speed. While a smaller device will have a faster switching speed, low power handling, and larger insertion loss. Naturally, a process that has high power handling and can achieve fast switching speeds is highly desirable.

4.3 Switch Architectures

RF Switches are typically designed in a shunt or a series architectures.

4.3.1 Shunt Switch

Figure 4.3b shows a shunt RF switch. It consists of two $\lambda/4$ transmission lines with a FET transistor that are connected to ground in between them. When the control voltage is low then the transistor presents a high impedance to ground and is effectively disconnected from the transmission line. This is the on state of the switch. When the control voltage is high, the transistor pulls the middle node to ground or presents a short. From an RF

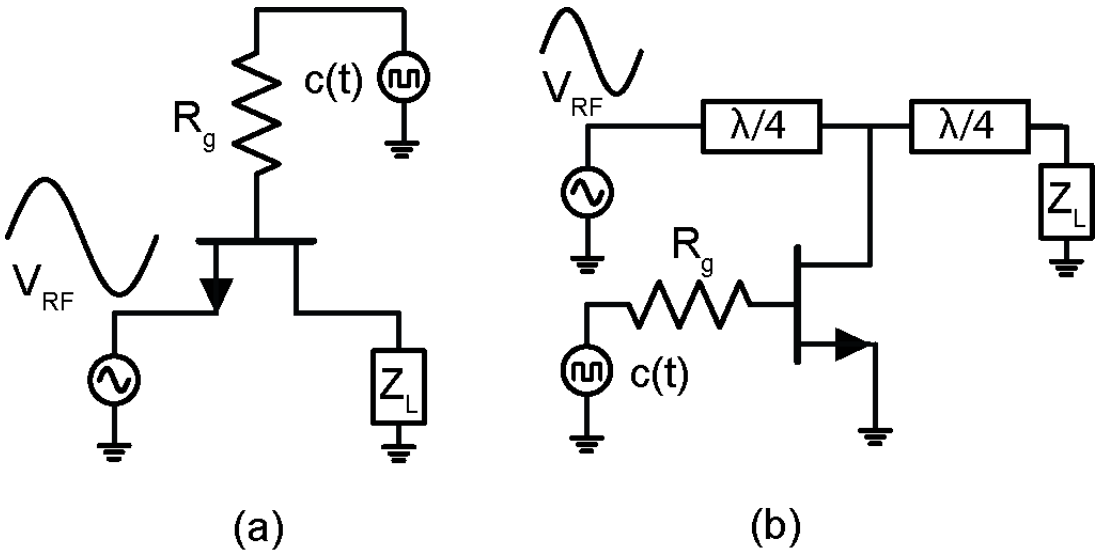


Figure 4.3: RF switch architectures, with resistor R_g at the gate to improve power handling. a) Series switch. b) Shunt switch.

signals prospective, a short will become a open $\lambda/4$ wavelength away. Shunt switches can handle larger powers compared to series switches [18]. The limitation of the shunt configuration is that the at low frequencies $\lambda/4$ becomes very large. Due to its large area requirement, shunt switch becomes unfeasible in integration application, and low frequency designs. Also, the $\lambda/4$ is designed to a specific frequency. When the frequency shifts away from center, the $\lambda/4$ it will not present a perfect open.

4.3.2 Series Switch

The switch shown in Figure 4.3a is placed in a series with the signal. Since FET transistors are symmetrical devices, it does not matter if they are drained or the source is input or output. When the control voltage is high the switch is on and presents a low impedance R_{on} to the signal. When the control voltage is low the switch presents a high impedance. The benefit of using a series switch is that it is easy to implement and its small form factor.

4.3.3 Series Shunt Series Switches

Another interesting switch is the combination of the two aforementioned architectures. Putting three transistors in a series-shunt-series configuration. This configuration can be

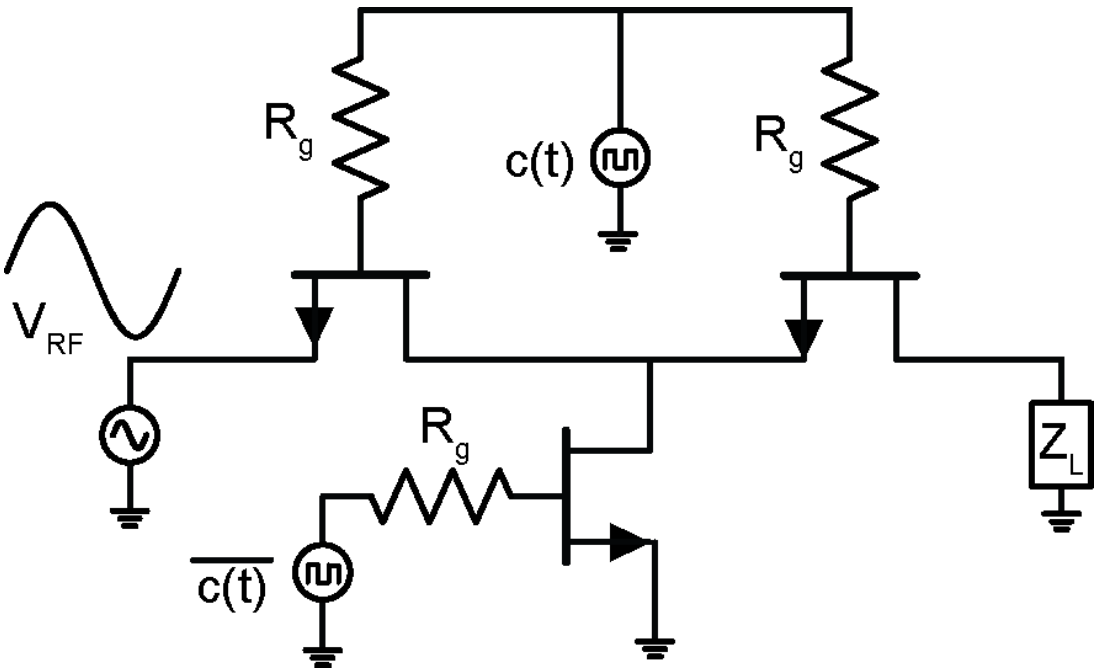


Figure 4.4: Series-Shunt-Series switch architecture

seen in Figure 4.4. The switch offers the same benefits of the shunt switch show in the previous section, but without the drawback of larger size. The two series transistors work as a standard switch in isolating input from output. The shunt transistor pulls the center node to ground when off state is desires. The drawback of this switch is that the layout becomes very complex, and the control voltage needs to have a complimentary variant.

4.4 Switch Technologies

4.4.1 CMOS and etc

RF switches can be implemented with different technologies, such as Microelectromechanical systems (MEMS), Phase-Change Material (PCM), and solid-state devices such as diodes or FETS. Although, MEMS have demonstrated very high power handling and low insertion loss, they are unable to switch very fast. PCM RF switches have recently come to fruition and have show excellent performance, but they still suffer from lack of switching speed and maximum number of cycles due to heating before the switch breaks down.

The bulk of RF switches are usually made in solid state technologies such as FET

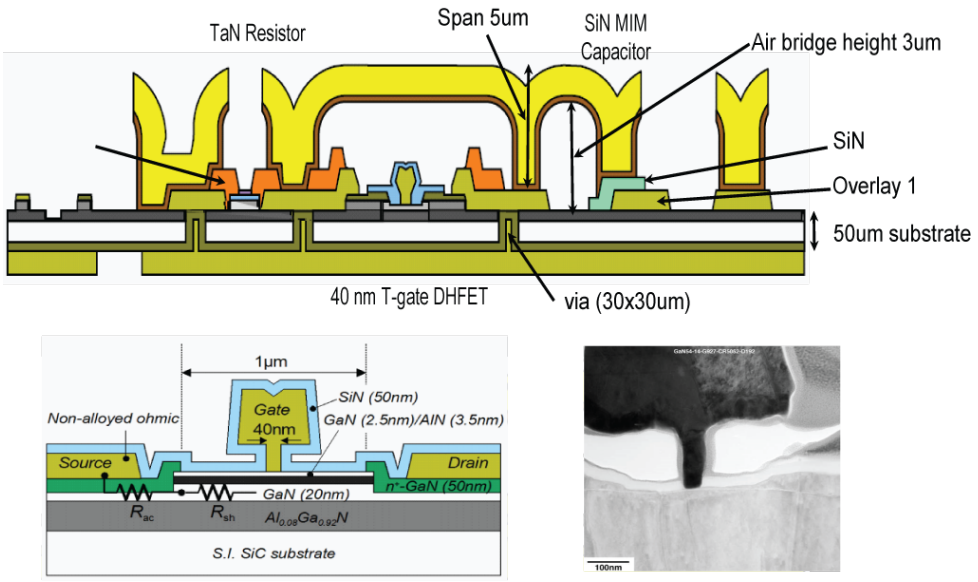


Figure 4.5: Cross section of HRL's T3 GaN Process

and p-i-n diode. These technologies have have been around for a very long time and have a proven track record of reliability, great power handling and speed performance. P-i-n diodes particularly have shown great performance with respect to power handling and switching speed. The downside of using p-i-n diodes has been their power consumption requirement due to on state DC current. They also require a complex DC biasing networks that needs to be added to the RF path, which potentially limits performance. FETs are the most widely used technology in construction of RF switches. Since RF switches can be build in the same technology as the RF front end components, a very tight integration can be achieved.

4.4.2 GaN

Each switch in this paper is implemented as a series transistor using HRL's GaN T-3 process. This is a 40-nm T-gate GaN DHFETs with f_T/f_{max} in excess of 200/400 GHz and breakdown voltage in excess of 55V. This process uses $Al_{0.25}Ga_{0.75}N/GaN/Al_{0.04}Ga_{0.96}$ double-heterojunction, grown by MBE [19–21]. The cross section for this process is shown in Figure 4.5. This process is able to achieve very low parasitic resistance and low gate capacitance which makes it suitable for fast switches. This is a depletion mode device technology. The RF signal passes from source to drain, and the gate is controlled by the

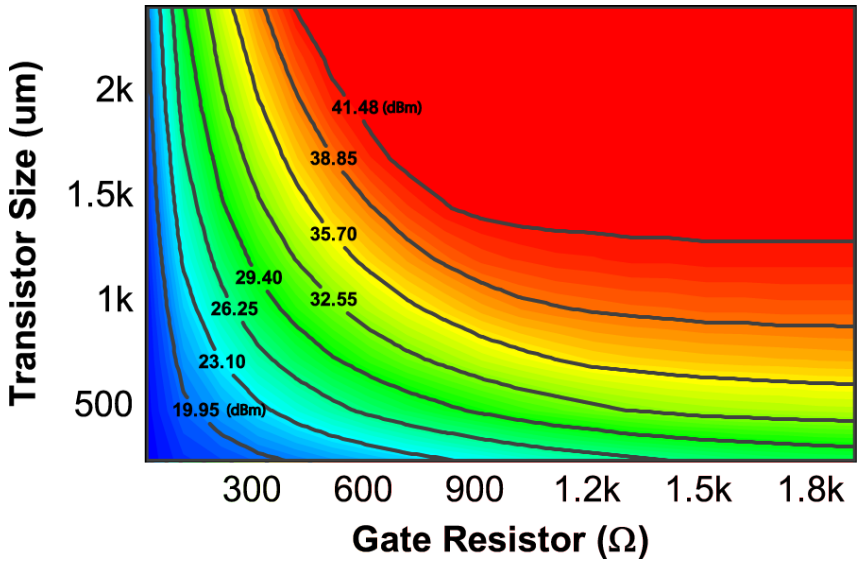
spreading sequence voltage. A positive 1V is needs to be applied to the gate to turn the switch ON and a voltage below -1V to turn it OFF. For power handling purposes this voltage was set to be -10V. A resistor R_g is added at the gate of every transistor switch to increase power handling (Fig.4.3). If there were no R_g at the gate of the transistor, then for large V_{RF} (which would be equal to V_{sw}) would cause the transistor to enter a nonlinear region and create distortion in the waveform. This can be mitigated by the addition of the R_g to the gate of the transistor. This causes a voltage division of V_{RF} on R_g and C_{in}:

$$V_{RF} = V_{sw} + V_g = I_{RF} \cdot (1/j\omega C_{in} + R_g). \tag{4.1}$$

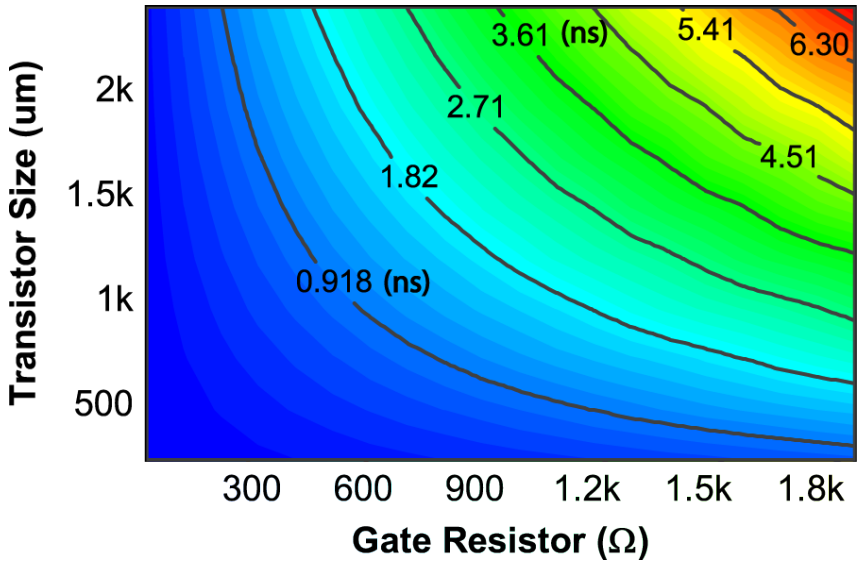
This equation shows the direct relationship between power handling and the combination of R_g and C_{in}. At the same time, they also are defined as an RC constant for the control voltage. Larger R_g or C_{in} will slow down the switching speed of the transistor essentially limiting the maximum processing gain that can be achieved. To have both high power handling and fast switching speed, a large R_g can be selected when using a process with very low C_{in}.

Contours in Figure.4.6 can be used as a guide to design RF switches in order to meet power and switching speed requirements. Figure.4.6a shows the 1dB compression point and figure.4.6b shows rise and fall time at the gate. These contours are dependent on different transistor and resistor sizes. They were generated using a scaled FET model and EPI resistor models from the HRL's T3 process.

A few observations can be see from the contours. In Figure. 4.6a it can be seen that a saturation point in power handling of more than 42dBm is achieved with transistor sizes larger than 1500um and resistor size larger than 900Ω. For these transistor and resistor sizes the rise and fall time is over 2ns. There is no benefit in choosing transistor and resistor sizes within this region of the contour.



(a) 1dBm Compression point of the transistor switch.



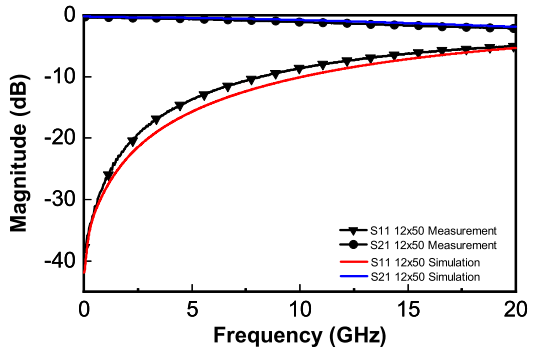
(b) Rise and Fall time of control voltage at the gate of the transistor in nanoseconds.

Figure 4.6: Contours for FET and resistor selection for specific power and switching speed a) 1dB compression point in dBm b) rise and fall time at the gate in ns

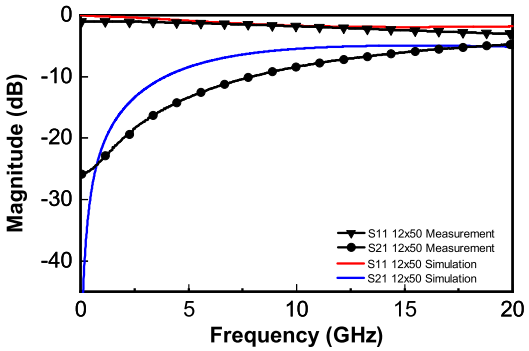
Chapter 5

Circuit Measurements

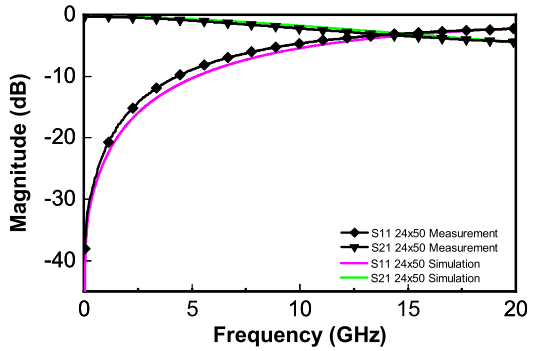
Using the contours in Figure 4.6, two different sizes of FETS are selected to fabricate the RF switches and the RF correlators. A 600um device with twelve fingers (12x50um) and a 1200um device (which is two 12x50um devices in parallel or 24x50um single devices). The 12x50um device was selected to be fast switching and the 24x50um to be larger power handling. The particular transistor sizes are predefined process parameters. To increase the size past the 12x50um, transistor devices are placed in parallel. The gate resistor is chosen to be $1k\Omega$. This choice gives a switch that has 1ns switching speed and a switch that has power handling close to 40dBm. The small signal S-Parameters measurement were done using Keysight PNAX N5247A with Infinity GSG probes and ISS 101-190 calibration standard. The calibration method is Line-Reflect-Reflect-Match (LRRM) with the reference plane located at the probe tip. The 1dB compression point measurements were done using a HP8360 RF source driving a 10W Spanwave PAS-00260-10 amplifier. An Anritsu 2438A was used to measure input and output power. The input was connected to the power meter using a 20dB coupler and the output was connected through a 30dB attenuator. Figure 5.1 show the comparison of the small signal s-parameters between measurement vs simulation for 12x50um and the 24x50um switches. There is very good agreement between what was simulated and what was measured, with the exception of the 12x50 off state. This deviation can be attributed to bad landing of the RF probes on the IC pads. The correlators are designed to work around 1GHz center frequency. When the gate voltage is set to 1V (switch is ON), at 1GHz the measured insertion loss



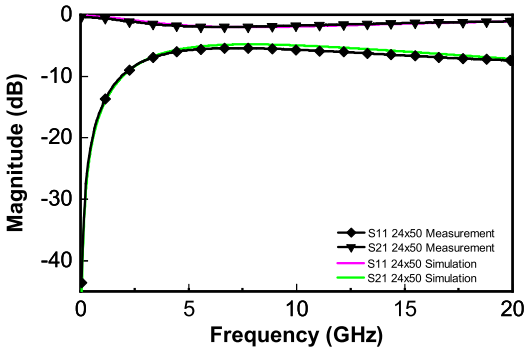
(a) S-Parameters for 12x50um Switch On



(b) S-Parameters for 12x50um Switch Off



(c) S-Parameters for 24x50um Switch On



(d) S-Parameters for 24x50um Switch Off

Figure 5.1: Comparison of simulated and measured small signal s-parameter for 12x50um and 24x50um switches with $1k\Omega$ resistor at the gate

of the 12x50um is -.41dB with the simulation showing -0.3dB. For the 24x50um switch, the measured insertion loss is $-0.32\,\mathrm{dB}$ with the simulation showing -0.305dB. Larger switches will have smaller R_{on} resistance so lower insertion loss is expected. When the gate voltage is set to -5V (switch is off), at 1GHz the isolation for 12x50um is measured to be -23.4dB a with the simulation showing -21.4dB. For the 24x50um the isolation is measured to be -14.7dB and -15.1dB simulated. The reason that isolation is poorer for the 24x50um vs the 12x50um device is because the former is larger so it has a larger parasitic C_{off} capacitance. The results show that both the 12x50um and the 24x50um make good switches, providing low insertion loss in the on state, and good isolation in the off state. Figure 5.2 shows the 1dB compression point for the two switches. The 12x50um compresses at 35dBm of input power and the 24x50um at 40dBm.

The third inter-modulation product was measured by injecting clean 997MHz and

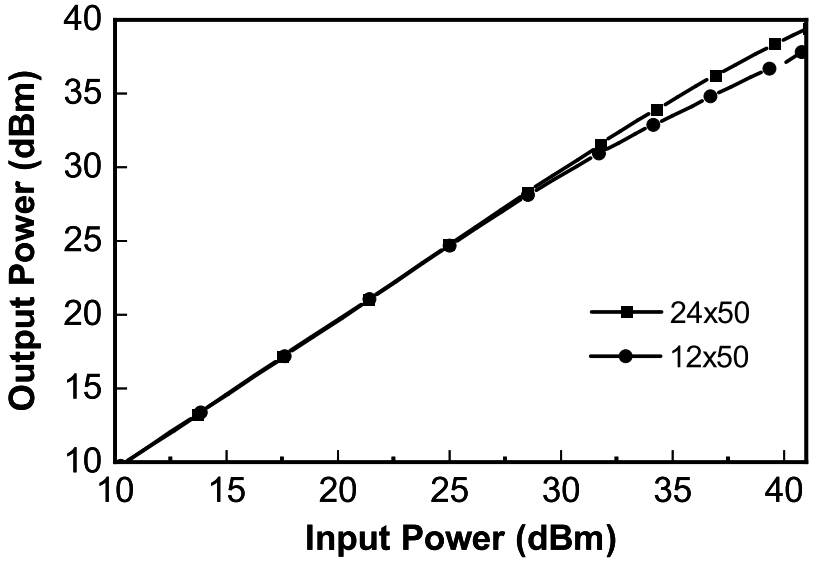


Figure 5.2: Gain compression of 12x50 and 2x12x50 devices in the ON state with respect to input power.

Table 5.1: Simulation vs Measurement of S-Parameters of different switches at 1GHz

	ON		OFF	
Switch Type	S11 (dB)	S21 (dB)	S11 (dB)	S21 (dB)
12x50um SW Sim	-28	-0.303	-0.19	-21.4
12x50um SW Meas	-26.5	-0.41	-1.0	-23.4
24x50um SW Sim	-23.3	-0.305	-0.32	-15.1
24x50um SW Meas	-21.5	-0.32	-0.56	-14.7

1003MHz CW signals with minimum spurious and noise floor. Two HP 8360 synthesizers were used with isolators, and a band pass filter to generate the two tones independently. A combiner is used to combine the two tones before injection into the switch. A Keysight N9030A PXA signal analyser was used to measure the intermodulation product at the output of the switches. A 16dB attenuator was used at the input of the N9030B signal analyser to insure adequate dynamic range and linear operation.

The measured OIP3 for the 12x50um switch was measured to be 48dBm and for the 24x50um 49dBm. No third order intermodulation simulation were performed. The reason for that is that the model for the GaN devices are very primitive and don't converge for

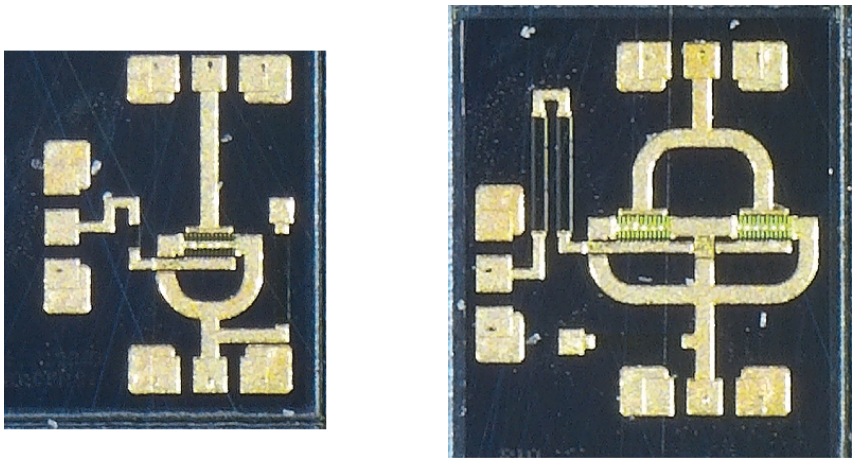


Figure 5.3: Die photos of the a) 24x50 and b) 12x50 GaN PHEMT switches.

very nonlinear simulation.

The simulated 90-10% rise and fall time for the 12x50um and 24x50um switch is .9ns and 1.7ns. This metric can only be derived from simulation. The reason for this is that the rise and fall time is defined at the node between the gate of the transistor and the added gate resistor. There is no way to measure this node without significantly altering the result.

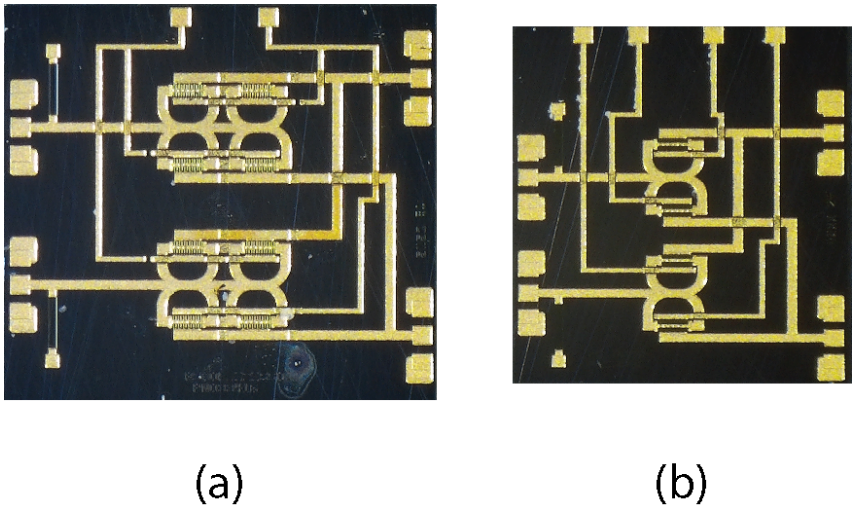


Figure 5.4: Die photos of the fabricated correlators.

The two 12x50 and 24x50 switches were used to construct the RF correlator ICs. A

single RF correlator schematic is shown in Figure 4.1. The pictures of the RF correlator dies is shown in Figure 5.4. The size of the 24x50um correlator was 2.2mm by 2mm, and the size of the 12x50um correlator was 1.7mm x 2mm. The measurement setup for the correlators was identical to the testing of the single switches.

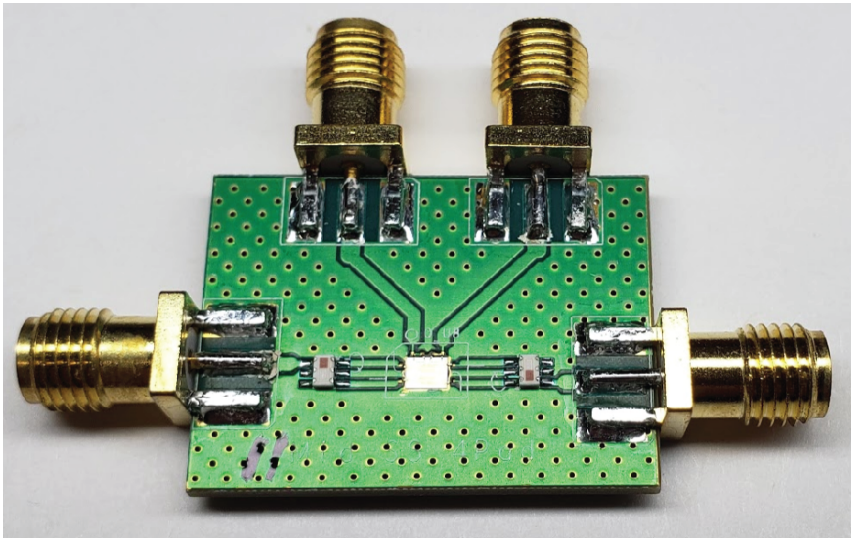


Figure 5.5: PCB of the RF correlator and the two input output baluns.

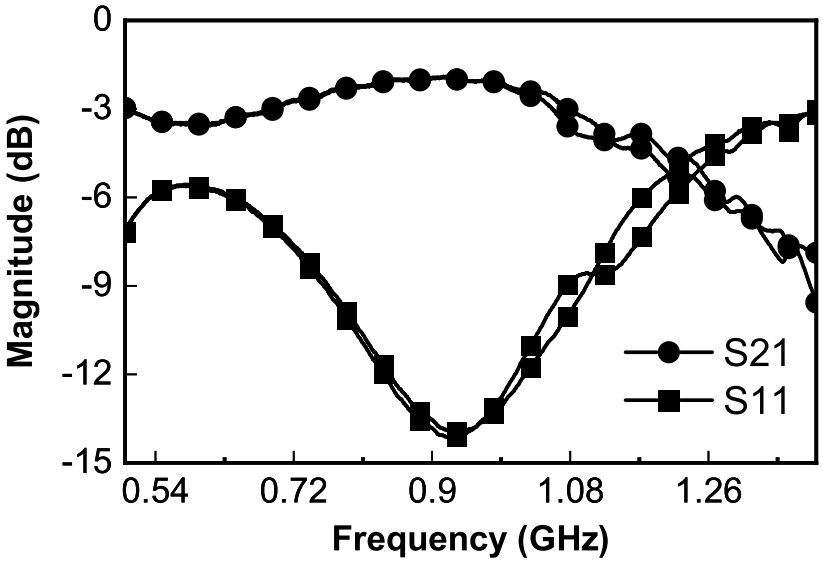


Figure 5.6: Small Signal S-parameter for RF Correlator PCB in for pass-through and cross state.

The simulated 90-10% rise and fall time for the RF correlators was 1.8ns the one using

the 12x50um switches and 3.4ns for the one using the 24x50um switches. The reason that the rise and fall time has increased is because there are two switches per control line of the correlator, which means that there is twice as much capacitance that needs to be driven. For system demonstration the smaller correlator was used as it has a smaller switching time. The reason for this choice is that the correlator, with the smaller switch, will allow for spreading sequences that are much wider in bandwidth. The cost of choosing this correlator is a slightly lower power handling.

For system testing and demonstration, the RF correlators were mounted and wire-bonded onto a custom FR4 PCB with two NCS4-102 Mini-Circuit baluns. The baluns were mounted on the input and output of the RF correlator to make it a single ended device. Figure 5.5 shows the picture of the RF correlator PCB. The reason for selection of these baluns is because the filter, used in the system demonstration, fall into their pass-band. Each balun contributes to the insertion loss of the correlator. Figure 5.6 shows the s-parameters for the pass-through and the cross states. The two port, small signal measurement was done using an Agilent E5071A network analyser, with a calibration done up to the cable ends. The pass-through and cross states were realized by setting the control voltages to 1V and -10V for one and then swapping them for the other. The input and output baluns are specified to have a 700-1000MHz operational bandwidth. Although the switch for the correlator can operate over a large band, the baluns will limit performance to a much smaller band. This is clearly seen from Figure 5.6. In the pass band of 900MHz, the insertion loss was around 2dB. Each one of the baluns contributes around .8dB of insertion loss while the rest coming from the RF correlator. There are some systems that can have fully differential front-end amplifiers and antennas, so baluns will not be necessary, and only the insertion loss of the RF correlator will be significant. Baluns will limit performance for codes that need to spread signals over large bandwidths. According to Figure 5.6 the 3dB bandwidth is set by the roll-off in the upper frequency which is at 1.15GHz. The implication of this is that no noticeable performance degradation will be seen for codes that spread up 400MHz bandwidths when centered around 850MHz, but for any larger bandwidth performance will start to degrade.

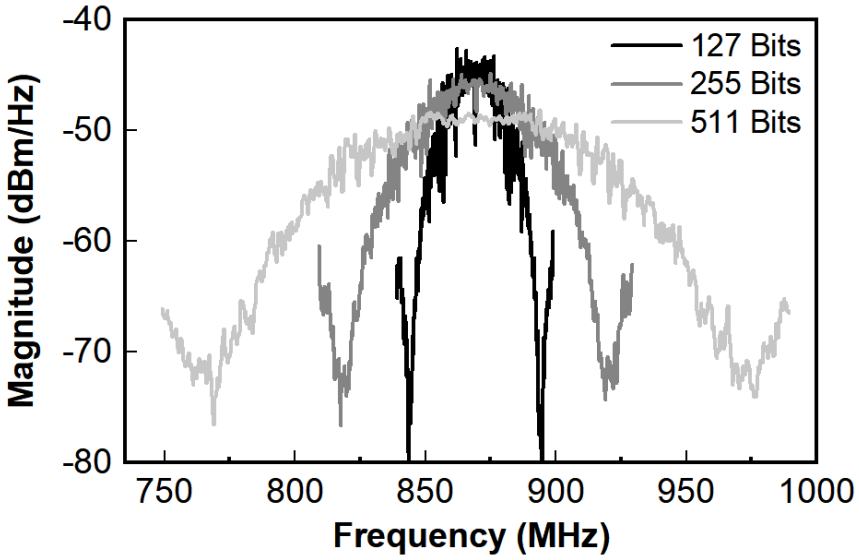


Figure 5.7: Frequency spectrum of the signal spreaded due to 127-bit, 255-bit and 511-bit spreading sequences.

Correlator's spread spectrum function was tested by inputting a CW signal from a HP8360 RF source and measuring the output using a Tektronix RSA406 spectrum analyzer. The control voltage was modulated using a Rigol 4102 function generator with a programmed spreading sequences. The control voltage was set to 1V for ON and -10V for OFF. Figure 5.7 shows the measured spread spectrum main lobes for 123-bit, 255-bit and 511-bit sequences. From this figure it can be seen that the doubling of the spreading sequence correspond to a doubling of bandwidth. The 123-bit sequence spread the signal to 25.4MHz, the 255-bit to 51MHz, and the 511-bit to 102.2MHz.It can be concluded from these results, that the correlator functions correctly. It spreading the input signal to the appropriate bandwidths that correspond to the spreading sequences. The small PCB modules will be used in the system demonstrations in the following chapters.

Chapter 6

System Demonstration

6.1 Surface Acoustic Wave Filters

This selection of the filter is very important for the system. It governs the center frequency location of the system as well as the spreading bandwidth requirement in order to achieve the desired processing gain B_c/B_s. Surface Acoustic Wave (SAW) Filters is a very popular filter technology for RF front-end. SAW filters offer a very narrow bandwidth, small form factors, and low cost. This work uses a TFS869 SAW filter from Vectron International was used. This filter has a center frequency of 869.21MHz and a 3dB bandwidth between 300kHz-200kHz.

6.2 Testbed

The requirement of the system was to achieve a minimum 20dB of processing gain, or 100x in spreading of the bandwidth. Given that the required code length for the system is a ratio of spreading and message bandwidth $L = T_s/T_c = B_c/B_s$, 100x spreading factor is needed with a minimum code length of 127 bit is required. In system testing code lengths of 127, 255 and 511 were used.

6.3 Correlator

Processing gain was measured by pacing two correlators back to back and applying the same spreading sequence to both. The input was a CW signal from a HP8360 RF source, and the output was measured using Tektronix RSA406 spectrum analyzer. The static

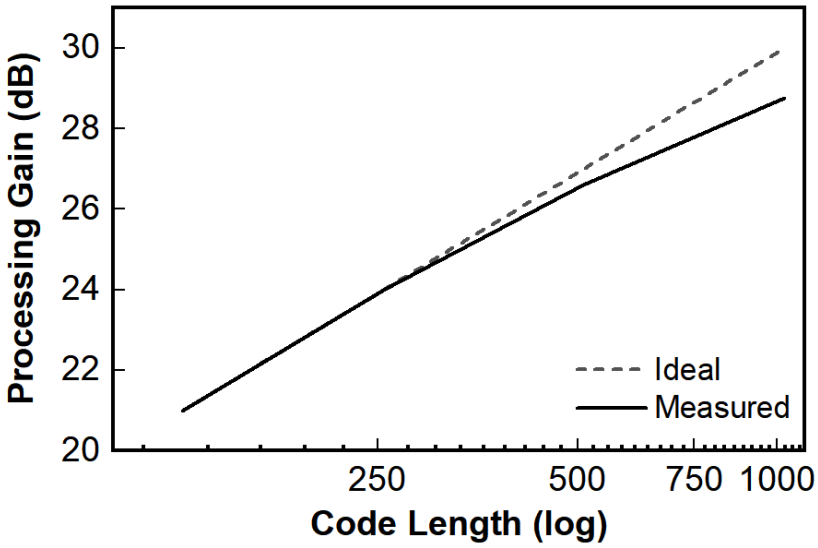


Figure 6.1: Theoretical and measured processing gain with respect to spreading sequence length.

losses were subtracted by measuring the setup with constant DC values on the control voltage. Fig. 6.1 shows processing gain for a CW signal being spread and then de-spread using different m-sequences. Chosen code lengths are 127, 255, 511 and 1023. For every doubling of code length a 3dB increase of processing gain is expected. For each particular code, loss in magnitude was subtracted from the ideal case. The 127-bit code achieves 21dB of processing gain while spreading the signal to 25.4MHz. The 255-bit code achieves 24 dB of processing gain, spread to 50.8 MHz, and the 511-bit code achieved approximately 27 dB of processing gain with 100.16 MHz bandwidth, and the 1023-bit achieved 28dB Due to limitations of the function generators that provide the codes for the correlators, codes larger than 1023 were not tested. In Figure 6.1 it is clearly seen that the processing gain is compressing with increased code lengths. The reason for this is that the switches are reaching their maximum design switching speed, and the signal quality of the source that is generating the spreading sequence is degrading. In the system measurements the correlator with the smaller switches of 12x50um was used. The switching speed for this correlator was 1.7ns. For the reasons explained above, the period of each chip in the spreading sequence $c(t)$ is faster than the $17ns$ of $58MHz$ and

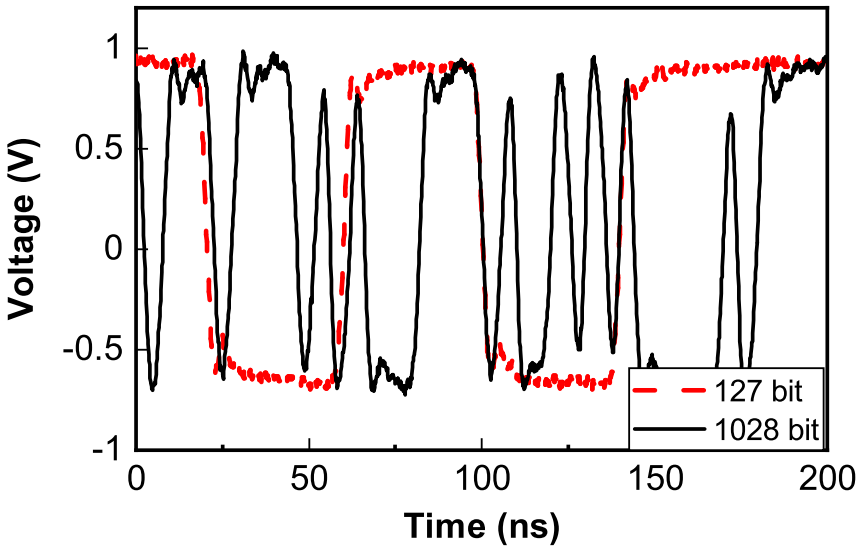


Figure 6.2: Voltage swing degradation going from a 127-bit to 1023-bit spreading sequences.

the transition period will start to play a bigger role and introduce more loss. The second reason that the processing gain compresses is that with each doubling of the code, the quality of the clock signal degrades due to the limitation of the source. It can be seen in Figure 6.2 that a slower 123-bit sequence has good transitions between high and low bits, but the 1023-bit sequence does not. For switches used in our correlator, no additional processing gain will be achieved if codes over 1023-bit in length are use. Faster switches are required if processing gain over 30dB is needed.

6.4 Antenna

The wireless operational center frequency was set by the pass band of the SAW filter. In this research this center frequency was located 869.21MHz. Also a wide band is needed due to the fact that the RF signal will be spread really wide. In order to accommodate spreading codes lengths such as 1024 bits and base-band bandwidth of $200kHz$ dictate a need for an antenna with a very wide bandwidth of $200kHz * 1023 * 2 = 408MHz$. Assuming that only the main lobe (Figure 3.3) is needed to be transmitted in order to completely reconstruct the signal on the receiver end, a bandwidth of 408MHz is required.

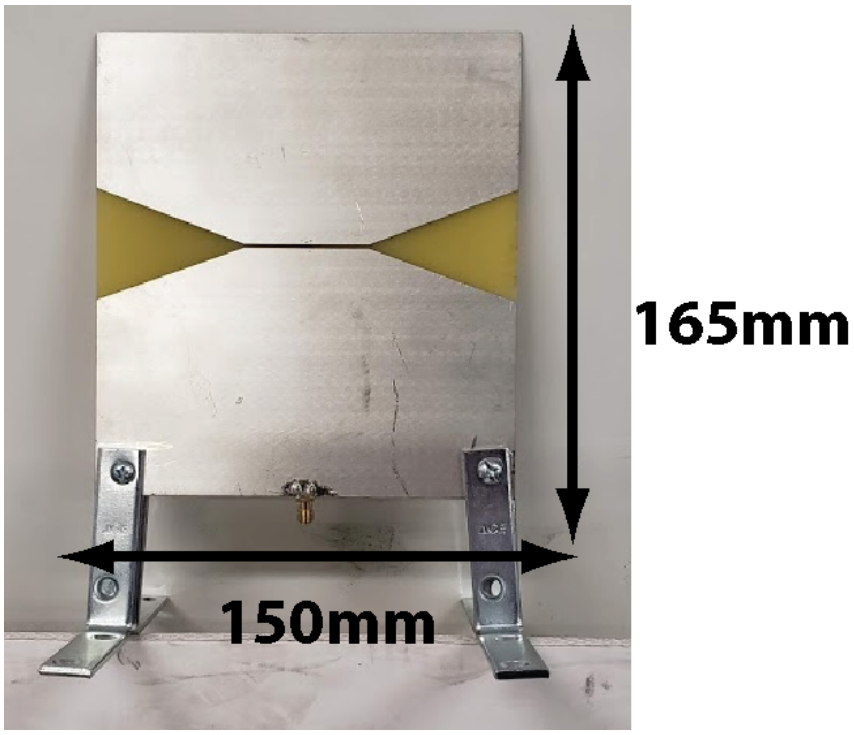


Figure 6.3: Picture of manufactured 150mm by 165mm bow tie antenna on FR4 substrate.

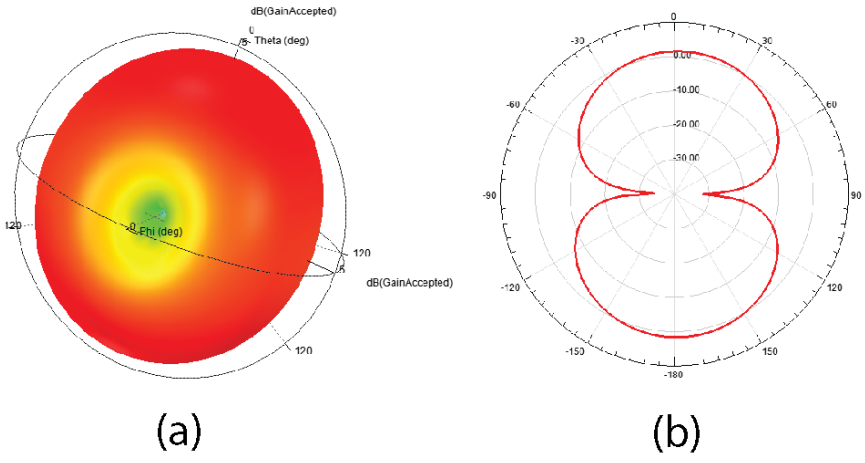


Figure 6.4: a) 3D simulated antenna radiation pattern b) Polar cross section antenna radiation pattern

There is also a requirement that the antennas need to be omnidirectional. The system will be used in communication systems such as handheld radios, the location of transmitters relative to the receiver needs to be arbitrary.

An inverted bow tie antenna design was chosen due to its wide band performance and its omnidirectional performance. The antennae was designed on 62mil FR4 substrate. The x dimension is 150mm and the y dimension is 165mm. A picture of the manufactured antenna is shown in Figure 6.3. Figure 6.4 shows the simulated pattern for the antenna, and very closely resemble that of a dipole antenna. Figure 6.5 shows a comparison between the simulated and measured bow tie antenna. According to this plot the antenna becomes mismatched around 700MHz, but remains well matched up into the higher frequencies. Due to the mismatch the occurs below $700MHz$, codes that spread to longer bandwidth are expected to have slightly degraded performances. In this research all codes larger than 255 bits do experience performance degradation because the lower side lobe gets attenuated.

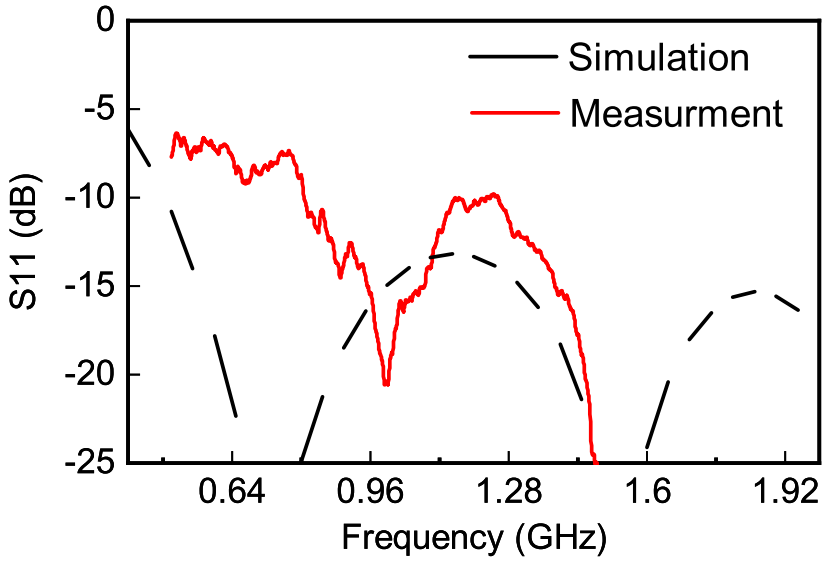


Figure 6.5: Comparison of 3d EM simulated antenna vs measured result.

6.5 System characterization

To demonstrate the functionality of the system, we perform a bench-top demonstration of the system as shown in Fig. 6.6 (a). Fig. 6.6 (b) shows a photo of the setup. We used an NI USRP 2901 as the transceiver to which our system is connected, and program a basic transmitter/receiver system that operates at a center frequency of 869 MHz (center frequency of the Vectron SAW filter), with a bandwidth of 200 kHz and QPSK modulation. The USRP is programmed using the LabVIEW Communications software. Two RIGOL 4102 function generators act as separate clocks for the GaN correlators, operating at 25.4 MHz with 127-bit spreading codes. The TX correlator and RX correlator are exact copies, implemented in separate boards for modularity and testing. An interferer can be injected using a power combiner between TX and RX. After the RX correlator, a narrow bandpass SAW filter TFS869 from Vectron rejects the out-of-band frequency components (discarding most of the spreaded jammer energy) and feeds the receiver of the USRP.

Figs. 6.6 (c)–(g) shows the spectrum of the transmitted signal (blue) and jammer (red) at the different stages of the system, denoted by the corresponding number in Fig. 6.6 (a).

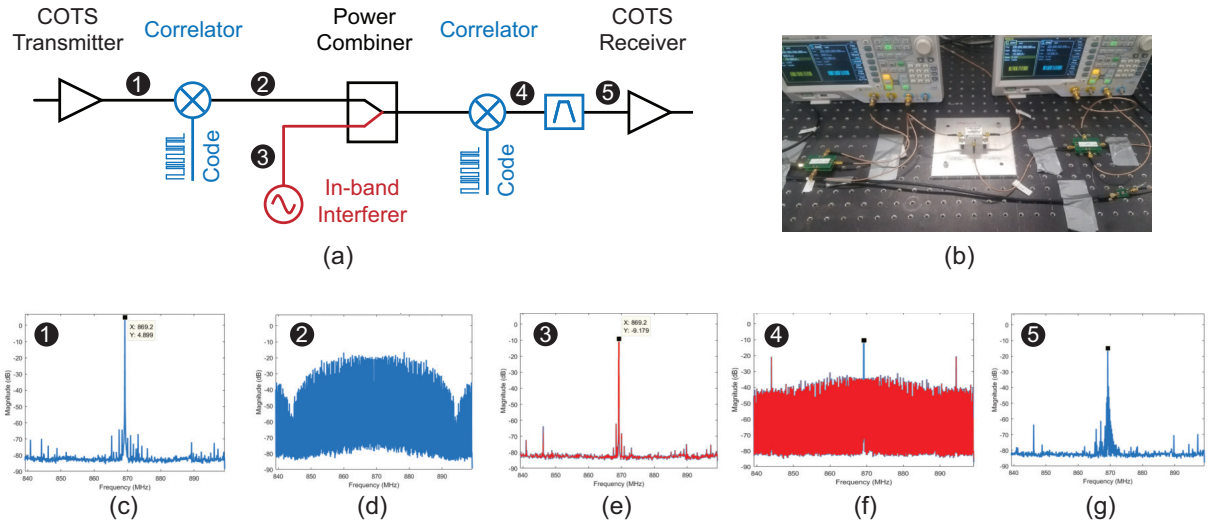


Figure 6.6: Wired system demonstration. (a) Block diagram of the system. (b) Wired system testbed. (c) Spectrum of the signal transmitted by the COTS device. (d) Spectrum of the signal after the TX correlator. (e) Spectrum of the narrow in-band jammer. (f) Spectrum of both the signal (blue) and jammer (red) after the RX correlator, which spreads the jammer and de-spreads the original signal when synchronization has been achieved. (g) Spectrum of both signal and jammer after bandpass filtering.

Measurements for both transmitted signal and jammer were performed independently with synchronized TX and RX correlators, and are shown to be superimposed in the plots for readability. The original transmitted signal [Fig. 6.6 (c)] is spread [Fig. 6.6 (d)], de-spread [Fig. 6.6 (f)] and filtered [Fig. 6.6 (g)], recovering the original signal up to insertion losses. The jammer [Fig. 6.6 (e)] is only spread by the RX correlator [Fig. 6.6 (f)], and after filtering its effect on the original signal is minimal.

6.5.1 Timing Recovery

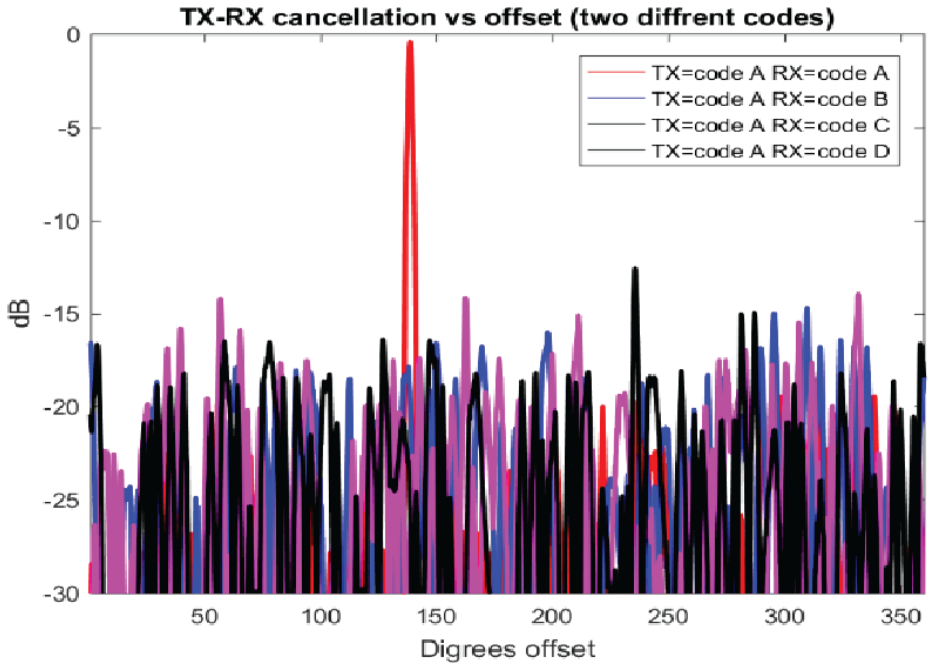


Figure 6.7: Received energy after the filter using one same and three different 123-bit spreading sequences in terms of partial T_c. offsets.

It was quickly realized that this system was very slow. The loop speed between analyzing the received signal and changing timing offset was measured in seconds. This meant that the total time to lock would take minutes rather than seconds. This method also had difficulty keeping the timing offset lock. The reason was due to the fact that the drift of internal oscillators in the clock sources is much faster than the loop speed. GPS disciplined oscillators needed to be used to minimize the effect to the drifting clocks. A new version to the timing recovery was implemented using a Xilinx Spratan-7 FPGA and a Analog Devices HMC1020 power detector. Figure 6.7 shows the measured energy in

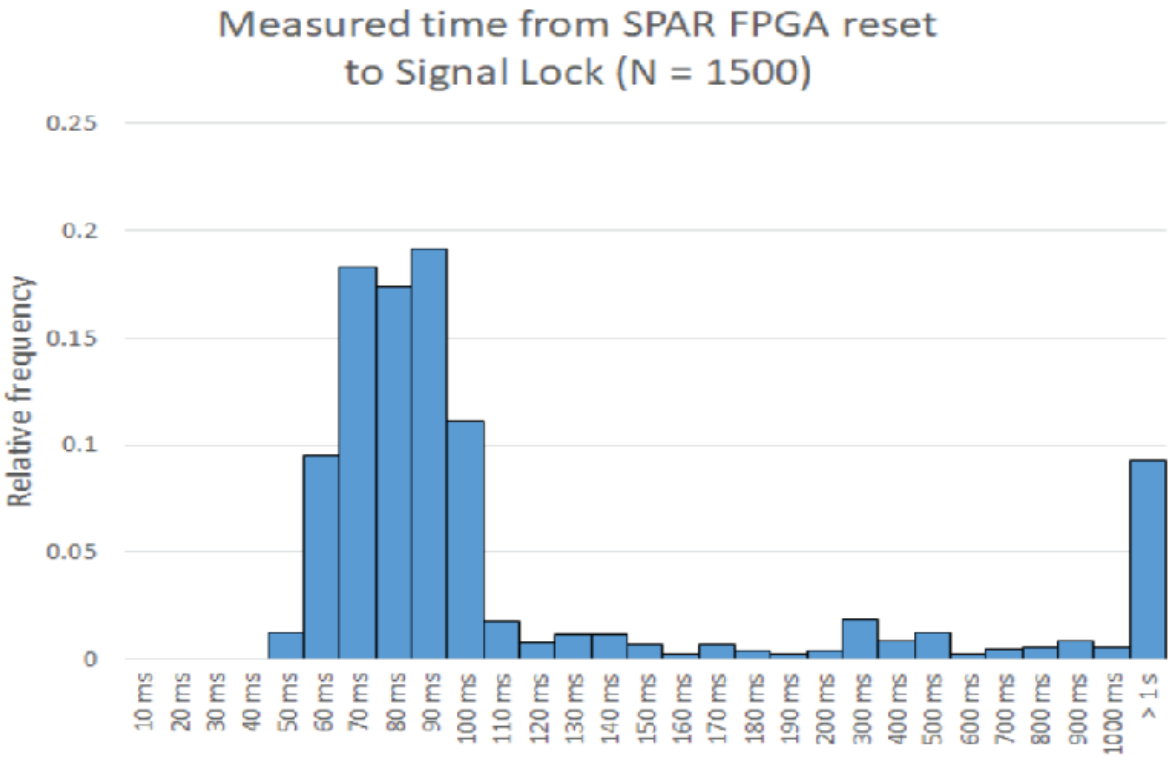


Figure 6.8: Statistical result for locking algorithm for 1500 runs

the receiver after the filter using one similar code as the transmitter and three different codes. The measurement was done by stepping through one tenth of a chip time for the full spreading sequence. It can be seen that there is only one unique peak with respect to all offset when the same sequence is used for spreading and de-spreading. The next largest peak is at-least 15dB lower no matter what sequence is used. This allowed us set the threshold to 15dB above the calculated number in order to avoid false locks. Each coarse offset was in terms of $1/3_{rd}$ of a chip time, and once the threshold is reached the locking algorithm would switch to a finer $1/10_{th}$ of a chip time steps. The "time to lock" for the timing offset algorithm were done using the bow tie antennas with the TX and RX placed one meter apart. Figure 6.8 shows a distribution of how long it takes to lock on to the correct timing offset. The measurement was performed 1500 times using the same spreading sequence in the TX and RX. On average the system would take 80ms to acquire lock. Less 10% of the measurement were not able to lock on to the offset. This error is attributed to the changing environment inside the lab.

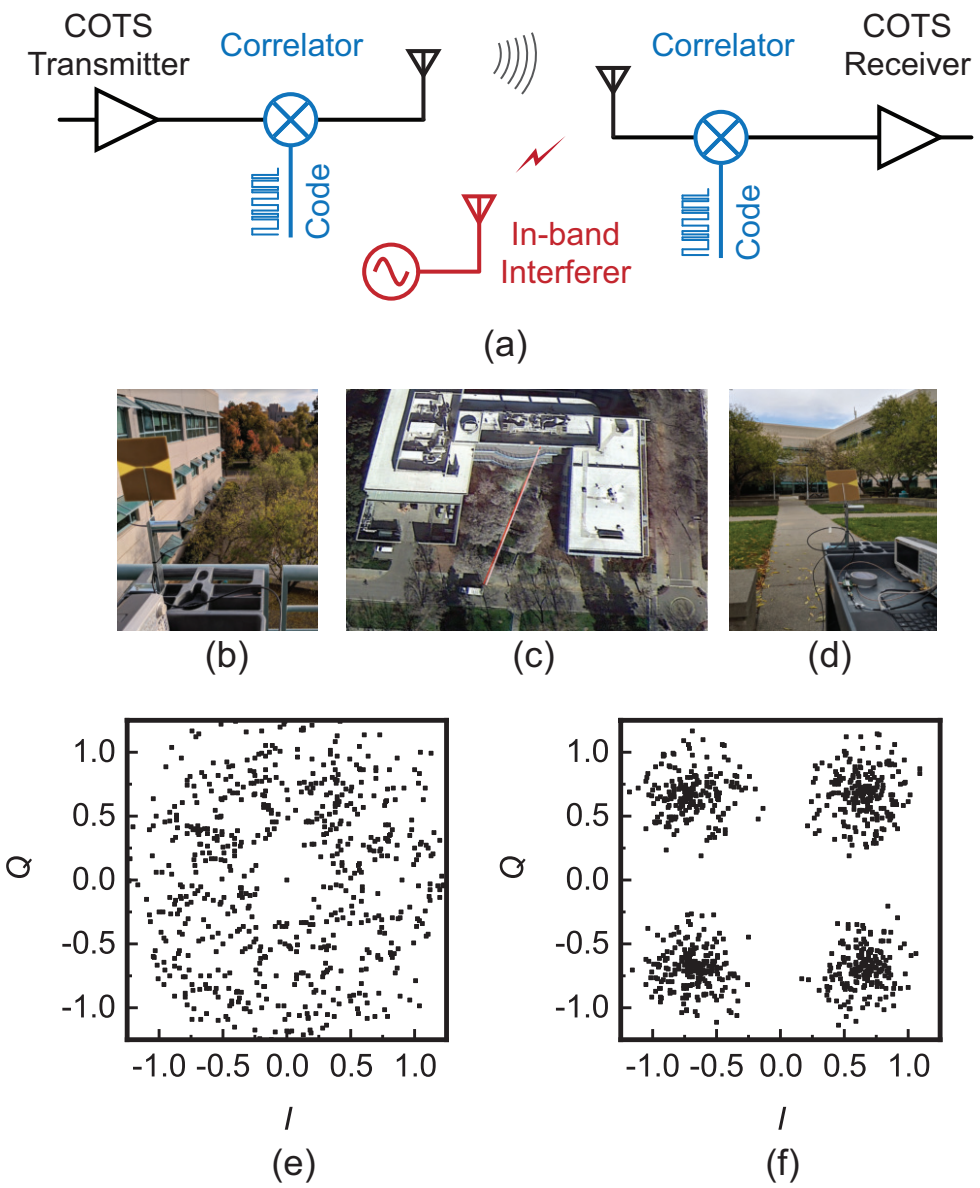


Figure 6.9: Wireless system demonstration. (a) Block diagram of the system. (b) Photo of TX in wireless setting. (c) Depiction of the wireless setting, with approximately 200ft. between TX and RX. (d) Photo of RX in wireless setting. (e) Received constellation under jamming conditions with no RF-CDMA system active. (f) Received constellation under jamming conditions with RF-CDMA active and synchronized systems.

6.6 Wireless testing

A demonstration of the effectiveness of the proposed system through in a more realistic wireless setting, as shown in Fig. 6.9. Fig. 6.9 (a) shows a block diagram of the demonstration setup. Fig. 6.9 (b)–(d) shows photos of the demonstration in action. The same

transmitter and receiver programs of the wired testbed are used in two separate USRP devices, operating on the same center frequency, bandwidth and modulation, and the function generators that provide the spreading codes use the same configuration described before. An Agilent E4432 RF signal generator was used to inject a narrowband interferer at 869MHz, which is the center frequency of the system.

Two experiments are done to show the effectiveness of the RF-CMDA correlators in terms of in-band interference mitigation. In the first experiment, a CW jammer that is -5-dB lower than the received RX signal power is injected to the receiver without turning on the RF-CDMA correlators. It can be seen in Fig. 6.9 (e) that the QPSK constellation diagram is completely destroyed. In the second experiment, an in-band interferer that is 25-dB higher than the received signal is wirelessly injected into the receiver, but this time with the RF-CDMA correlators turned on. It can be seen from Fig. 6.9 (f) that the QPSK constellation is restored. Although the constellation diagram still shows a rather high level of added amplitude and phase noise to the received signal, the effectiveness of the proposed RF-CDMA system is shown, considering the 30-dB difference in jamming power between the two experiments.

Chapter 7

GaN N-Path filter

7.1 Out of Band Interference

For wireless and wire-line electronics out-of-band interference has always been an issue. Especially in wireless communication, out-of-band interference has the potential to saturate or even damage electronics. Out-of-band interference can come from many sources. Since the inception of analog electronics, interference has always been dealt with by the use of filters to discriminate between different parts of the spectrum.

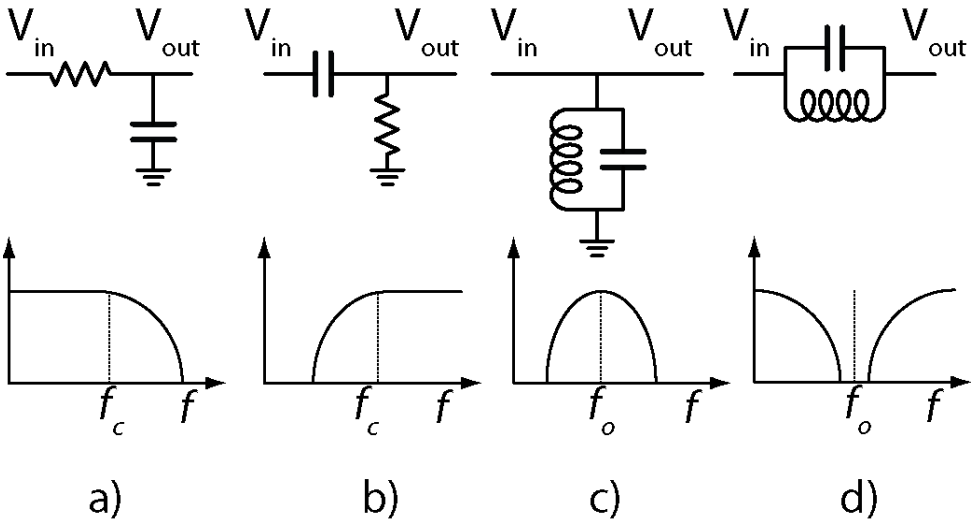


Figure 7.1: Types of filters and their frequency response a) Low-pass b)High-pass c) Band-pass d) Band-stop

7.2 Convectional filters

Convectional filters can take on many shapes and sizes. The simplest form in construction of filters is using lumped elements like resistors, capacitors and inductors. Figure 7.1 shows the most common lumped components configuration and the expected frequency response. These lumped components can be arranged in various ways to construct low, high, band-pass and band-stop filters. In analog domain, filters can be passive such as lumped components or active such as Op-amp filters [22]. In RF and mmWave domain the filters are typically made of transmission lines, and wave guides [23]. Also, due to advancements in data acquisition speeds, digital filters have become very prevalent in modern electronics, but this is outside the scope of this work. Due to the tight bandwidth requirements, modern transceivers use surface acoustic wave (SAW) [24] and bulk acoustic wave (BAW) filters.

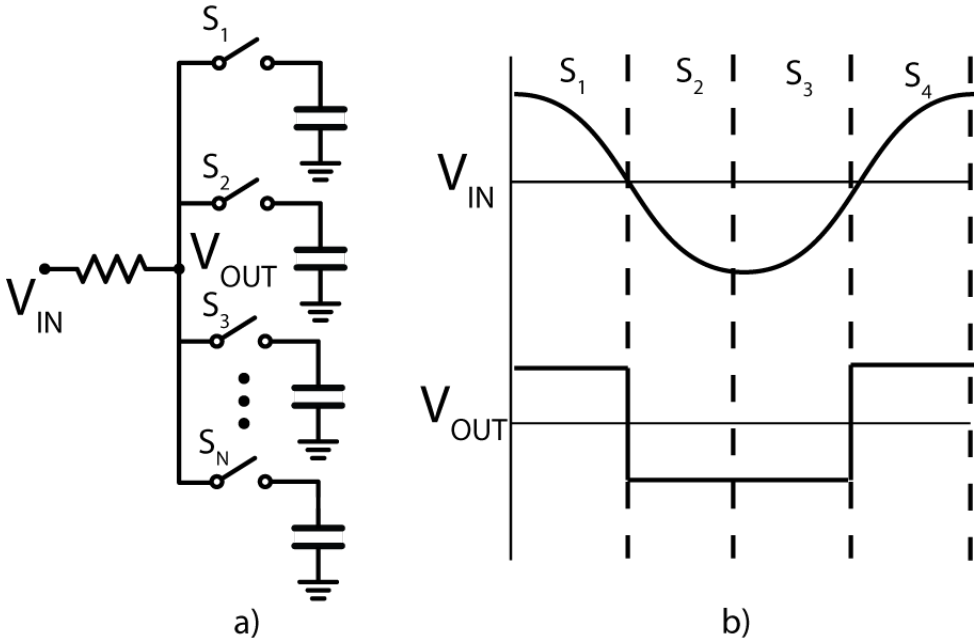


Figure 7.2: a) Simple single ended N-Path filter b) Input and output voltage for N-Path filter

7.3 Tunable filter

With the current advancements in technology, modern transceivers are expected to operate at multiple frequency bands. A good example of this is a modern cell-phone which houses

multi-generations of communication technologies such as EDGE, 3G, 4G LTE and 5G. Each of these wireless standards operates on a multitude of band/sub-band thus requiring a large quantity of filters [25]. With the requirement of making cell-phone transceivers small, dedicated filters can take up a lot of precious real estate. There has always been a desire, and even more so now, to have a filter that is tunable in frequency and bandwidth to cover all the bands of operation. There has been a lot of progress towards making filters that are tunable with respect to frequency and bandwidth [26–30]. Some of these works use a mechanical actuator, and other use a varactors to change capacitance. Typically the mechanical devices are bulky, and suffer from limited performance due to mechanical life span of the actuator. The varactor tuned filters are also performance limited due to the tuning limitation of the diode and power handling. Works in tunable SAW/BAW filters have also shown promising results [31–34], but there are limited in performance and tunability range.

7.4 N-Path filter

An alternative and increasingly popular tunable filter architecture is called the N-Path filter. This architecture is very compact, it utilizes commercially available IC fabrication process and can be tightly integrates in to IC systems. A simplified schematic of the filter is show in Figure 7.2 a). These types of filters use switched-capacitors also known as sample and hold circuits to down convert the RF signal, pass it through a low-pass filter created between input impedance R and capacitor C and up-convert back to RF. Another way to visualise this is to look at the input and output of the N-Path filter in analog domain. Figure 7.2 b) shows the V_{IN} and the V_{OUT} waveforms for N=4 N-Path filter. When a specific switch is on, the corresponding capacitor charges to the average voltage level. The output waveform is a discreet version of the input with the same frequency. If the input frequency is doubled then average voltage on the capacitors will be close to zero. From this example, it can be seen that the each switch needs to be ON for a period of T/N and that there should be no overlap between each switches on time.

The transfer function for the differential N-Path filter is shown in equations 7.1 and

7.2 which were originally derived in [35].

$$H_o(f) = \frac{N}{1+jf/f_{rc}} \times (D + \frac{1+exp(j\pi(1-2D)f/f_S}{2\pi f_{rc} f_S} \times (-\frac{epx(j2\pi Df/f_S) - exp(-2\pi Df_{rc}/f_S)}{exp(j\pi f/f_S) + exp(-2\pi Df_{rc}/f_S)} \times \frac{1}{1+jf/f_{rc}})) + (1-ND) \tag{7.1}$$

$$H_{N-path}(f) = \frac{R}{R+2R_{SW}} + \frac{R}{R+2R_{SW}} H_o(f) \tag{7.2}$$

In 7.1 D refers to the duty of the clock cycle, N refers to number of paths, $f_{rc} = 1/\pi RC$ is the cutoff frequency of RC filter where R is the input resistance and C is the chosen capacitor value and f_S is the center frequency of the filter. In equation 7.2 the switch loss which is represented by R_{SW} is taken in to account.

This type of filter has been demonstrated extensively in the sub-micron CMOS processes [36] [37] [38]. N-Path filters have been shown that they can effectively be used for DSSS at RF frequencies. [4–7, 39]. Most of them are built in the typical CMOS process which limits their power handling performance which is key in performing signal processing at RF frequencies.

7.5 GaN N-Path Filter

7.5.1 State of the Art

GaN has always been an attractive technology when it comes to high power handling requirement in RF frequencies. There have only been a few works done recently that use the GaN IC fabrication process to create N-path filter ICs [40] [41]. These works show a N-Path filter core (switches only) that is manufactured in a 250nm GaN process. It was able to achieve a tunability over 1.6GHz with a P1dB of 18dBm. These works rely on external drivers, and a external source to generate the four phase non-overlapping clock. From a system integration perspective this is a big drawback because this makes the overall N-Path filter very large. Although these works show that the core GaN N-Path

filter does not consume any power, one must include the power consumed by the drivers circuitry and the FPGA to generate the clocks.

7.5.2 This work

For this work a heterogeneous system integration approach is taken to achieve a high power handling N-Path filter.

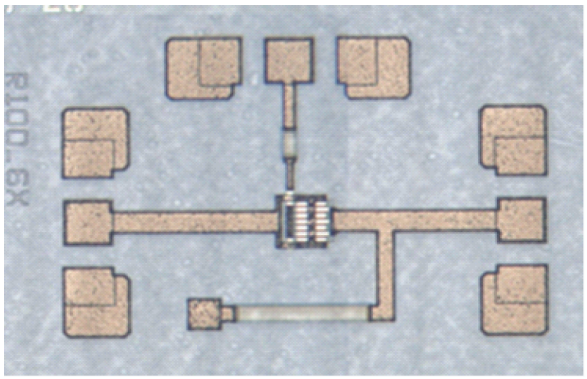
1. A N=4 N-Path filter core is designed and fabricated in HRL's T3 process.
2. A driver circuit is integrated into the GaN process in order to drive the GaN switches to correct voltage levels.
3. Stand-stand alone, four phase none over lapping clock, is designed in a standard CMOS process with intention to drive the GaN devices.
4. ICs are integrated at PCB level with consideration taken for effects such as wire-bonding.

This heterogeneous system approach gives the ability to create a high power handling N-Path filter with a relatively small footprint and reasonable power consumption. Different circuits and integration techniques are explored that can yield a N-Path filter with the current commercially available processes.

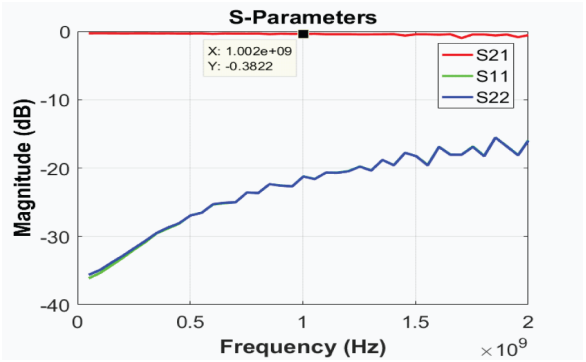
7.6 GaN N-Path core

7.6.1 GaN switch for filter

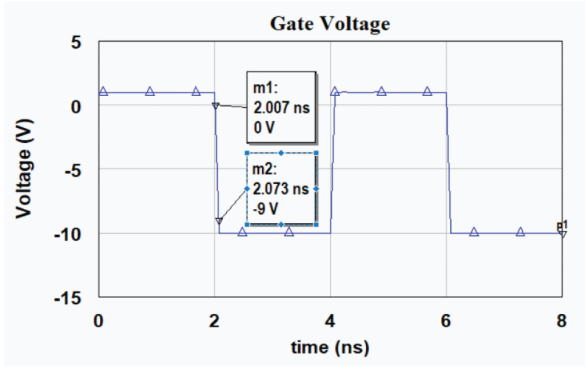
The key requirement for a N-Path filter is to have a fast switch. As shown in Figure 4.6 for HRL's T3 process the switches can be fast if power handling is sacrificed. The filter in this work was designed to operate in the $1GHz$ range this means that the switch need to transition from on to off in less than $1/10ns$. Using Figure 4.6 as a guide, the switch that was selected is a 6x50um device with no resistor at the gate. The single switch was fabricated for testing and the die is shown in Figure 7.3a. The small signal measurements in Figure 7.3b show that the switch is well matched up to $2GHz$ with no additional matching network and the insertion loss is less than .4dB. The time domain simulation



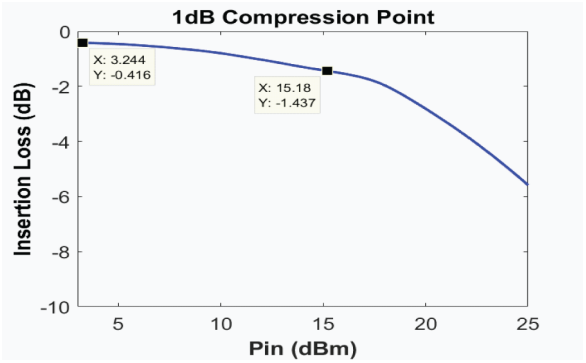
(a) Die photo of a single 6x50um switch with launchers



(b) Small signal measurement of single 6x50um switch



(c) Simulation of a 1GHz pulse on the gate of the switch



(d) 1dB compression point for the single 6x50um switch

Figure 7.3: Fast GaN switch used in the N-Path filter core

of the Gate control voltage is shown in Figure 7.3c. This shows that the $10\% - 90\%$ transition takes around $70ps$. This means that the device is more than sufficient to for N-Path filter application and meets the $100ps$ transition speed. The 1dB compression point for this switch is measures to be 15dBm of input power.

7.6.2 GaN N-Path filter core design

The schematic for the design filter is shown in Figure 7.4. The core switch of the filter was chosen to be a 6x50um device as it provides a good compromise between power handling and switching speed. In addition to having the center tunable center frequency, two different capacitor banks are added to change the bandwidth of the filter. The bandwidth of the filter is inversely proportional to the designed capacitor value C and intrinsic resistance of the transistor R_{on}. In order to achieve small bandwidths, larger capacitor values are required.

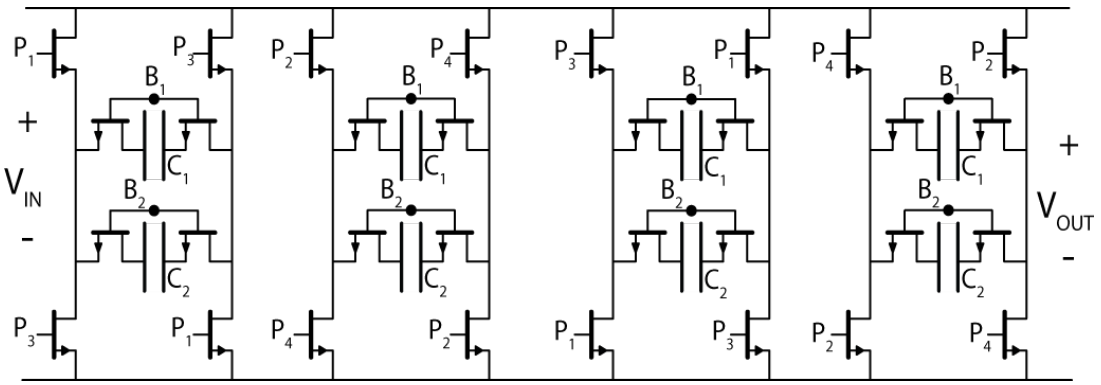


Figure 7.4: Schematic of N-Path filter core in GaN

$$\omega_{3dB} \propto 1/RC \tag{7.3}$$

The switches that engage the different capacitors are the same 6x50um devices. In order to have a tunable bandwidth, insertion loss will have to be increased. The reason for this is that there are four additional devices that are connected to each capacitor during each clock period. The largest manufacturable capacitor value in HRL's T3 process is 75pF which is 500um by 500um in size. This capacitor was used for the narrow band value. The second capacitor that was selected for the filter was the 15pF which is 200um by 200um in size.

The simulation results for the small signal are show in Figure 7.5. These results show three different simulation frequencies .8GHz, 1GHz, and 1.2GHz. Also, in the figure there are two colored curves that represent the two different capacitor banks. The blue curve is with the 75pF capacitance and the red curve is with the 15pF capacitance. The 15pF capacitor shows to have a 112MHz 3dB bandwidth with an insertion loss of -2.9dB at 1GHz center frequency. The 75pF capacitor has a 20MHz 3dB bandwidth and a insertion loss of 3.4dB at 1GHz center frequency. Figure 7.6 shows the simulated 1dB compression point of the filter at 18.8dBm.

7.7 GaN Driver

One of the most challenging things about using GaN switches is the ability to turn them on and off. Since GaN is a depletion mode device, a negative voltage is required to turn

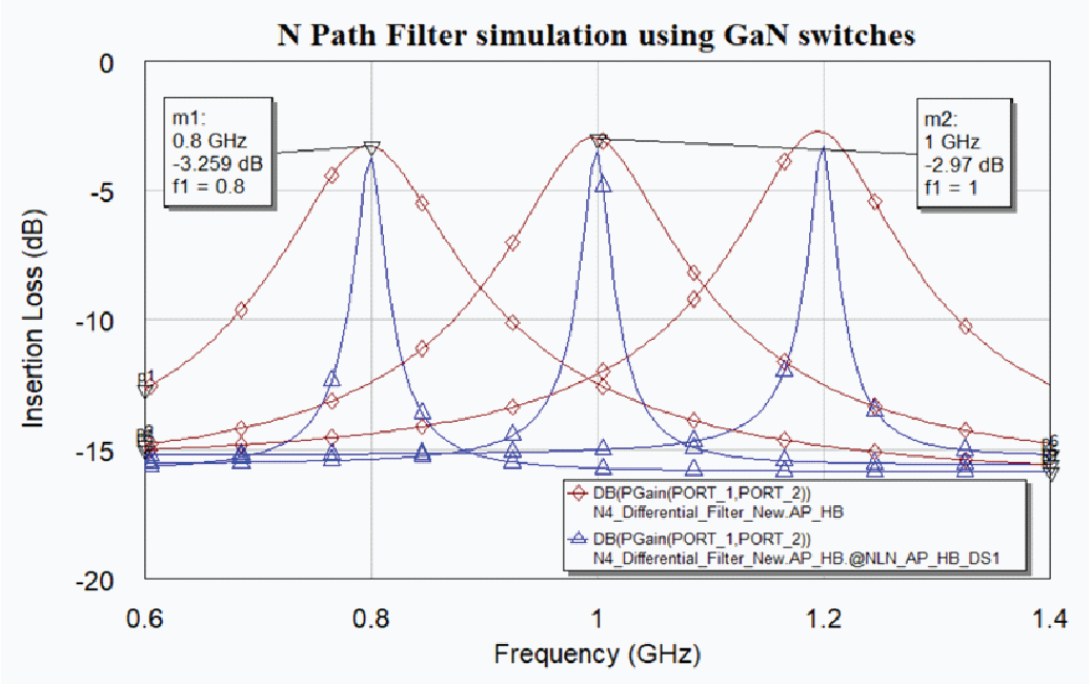


Figure 7.5: Simulated bandpass response of N-Path filter at .8, 1, 1.2GHz

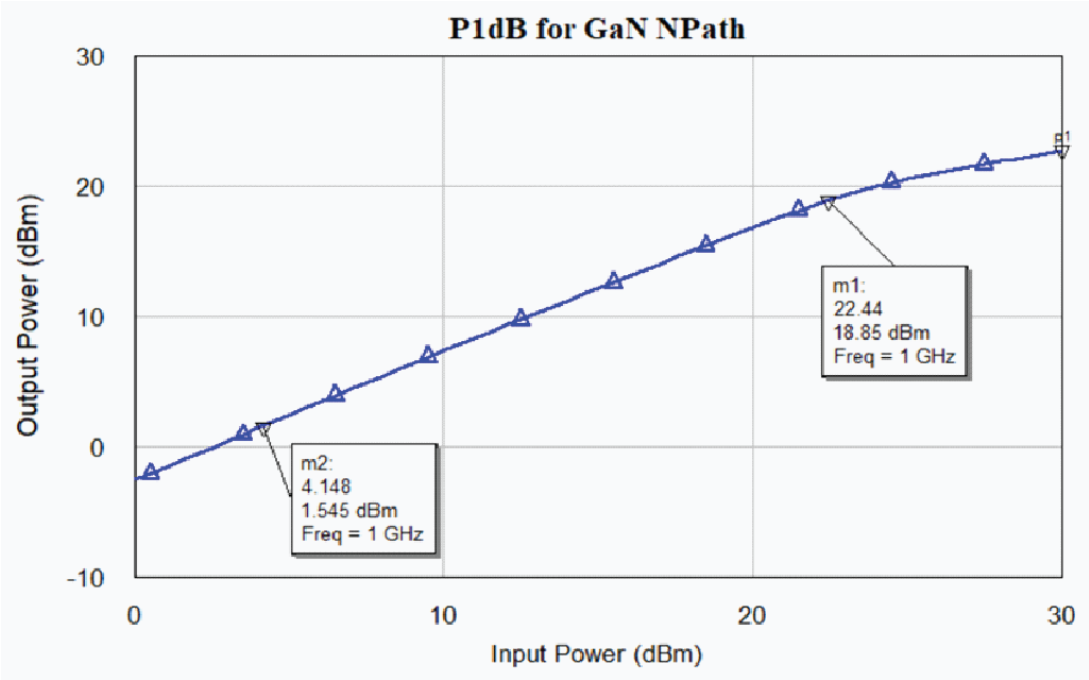


Figure 7.6: Simulated p1dB compression point of GaN N-path filter

it off, the voltage must be greater than zero to turn it on. For devices in HRL process the devices require +1V to turn on with a pinch-off at -1V. Also, to ensure that the device

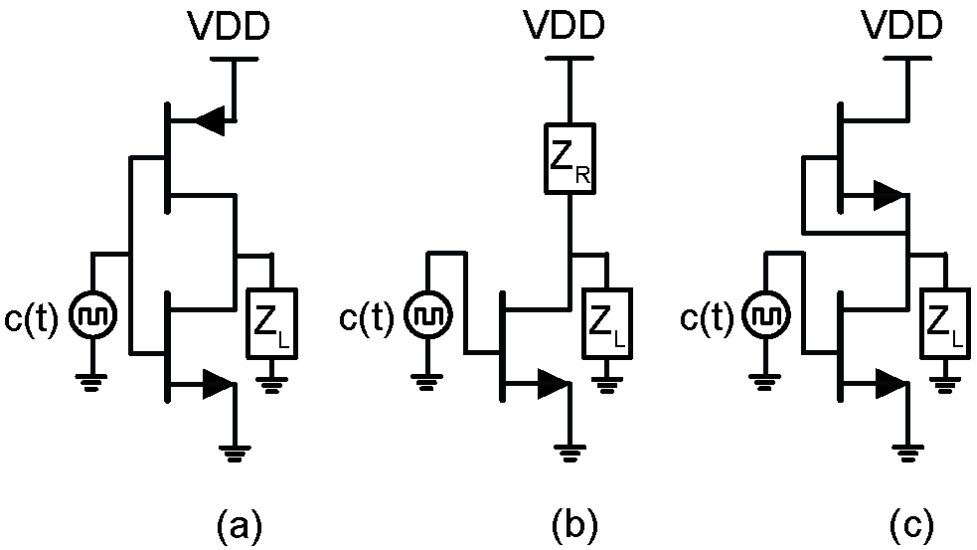


Figure 7.7: a) Typical CMOS inverter b) Pseudo-MOS inverter using a resistor for the pullup network. c) Pseudo-MOS inverter using a diode connected NMOS transistor in the pullup network

stays off during presence of large RF power, a negative voltage needs to be provided to the switch. A voltage of -3V will need to be applied to the gate to ensure that a RF signal power of 20dBm does not turn the device on.

7.7.1 Pseudo-MOS GaN Logic

For circuits that are built in a CMOS process, clock generation is not a problem due to the fact that they have complimentary devices. The input logic voltage levels are the same as output $V_{LOWin} = V_{LOWout}$ $V_{HIGHin} = V_{HIGHout}$. PMOS and NMOS can be used to construct inverters that can be used to generate and gate different clock signals. Currently, there are no complimentary FETs that exist in the GaN process that is fast enough to make a usefully inverter and where the logic voltage levels between input and output are not the same. There is research that is working towards making a PMOS devices in GaN process, but they are extremely complicated to build and are very slow [42]. There is a alternative way that a inverter can be created in a process that lacks a complimentary device. This is typically referred as a Pseudo-MOS inverter. In the early days of CMOS technology Pseudo-MOS was used to create fast inverters in theologies that lack a fast PMOS device [43].

In Figure 7.7 a) a traditional CMOS inverter is show that has a NMOS transistor in the pulldown network and a PMOS transistor in the pullup. The two transistors are properly sized to have a equal rise and fall transition time going between high and low logic levels. The same type of logic can be achieved if the top PMOS transistor is replaced with a resistive load Z_R as shown in Figure 7.7 b). When the bottom transistor is of the voltage on the Z_L is pulled up to VDD or high logic level. When the bottom transistor is turned on the voltage on Z_L is pulled low logic lever. The bottom NMOS and Z_R are sized to achieve the same rise and fall time. This resistive Pseudo-MOS inverter has the same logic functionality as a traditional inverter shown in Figure 7.7a), but has a much higher power consumption. In logic systems Z_L is typically capacitive, and for ideal/traditional inverter the power consumption is dictated by the frequency of charging and discharging the capacitve Z_L load. This is know as dynamic power consumption and is depicted in Equation 7.4, and is the only source of power dissipation.

$$P_{\text{avg}} = f_{\text{c(t)}} Z_{\text{L}} V_{\text{DD}} \tag{7.4}$$

However, the Pseudo-MOS device also has static power dissipation that occurs when the bottom device is on and there is DC current I_{DD} that goes through the Z_R load. This is depicted in Equation 7.5 and is added to the dynamic power consumption. This static power consumption can be significant if the V_{DD} is high and the total resistance of Z_R and the bottom NMOS are low.

Resistor are hard to implement in a IC process when compared to a transistor, but a diode connected transistor can be used to replicate a resistor with adequate accuracy. The circuit that is typically used for implementing the Pseudo-MOS devices is depicted in Figure 7.7 c). This makes for a compact circuit layout and the devices are more likely to be well matched to achieve a symmetric rise and fall time.

$$P_{\text{static}} = I_{\text{D}} V_{\text{DD}} \tag{7.5}$$

7.7.1.1 Pseudo-MOS simulation in GaN

The purposed GaN pseudo-MOS is shown in figure 7.8. This inverter is simulated in HRLs T3 GaN process. Transistors M1 and M2 are $12x50um$ devices. These device sizes

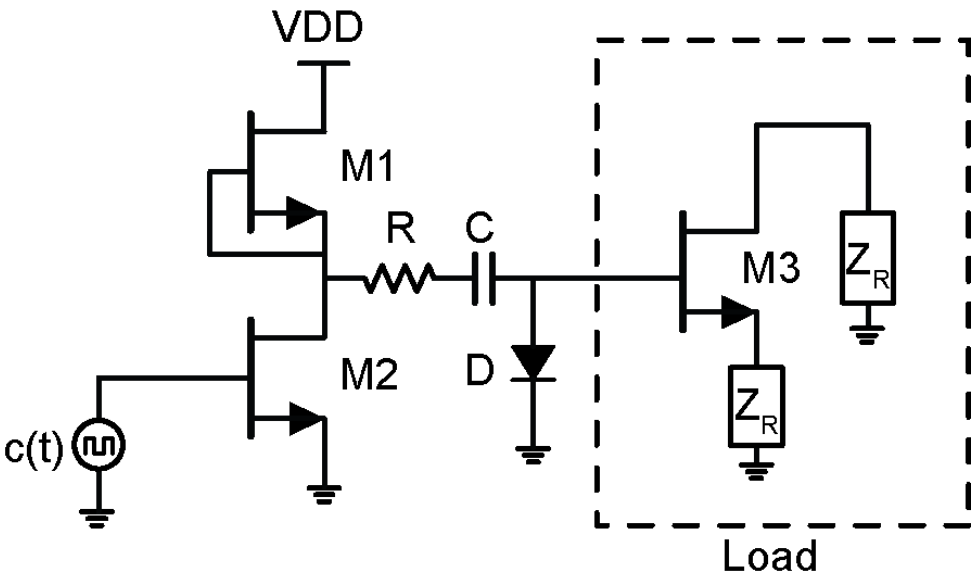


Figure 7.8: Proposed implementation of pseudo-MOS inverter in HRL GaN process

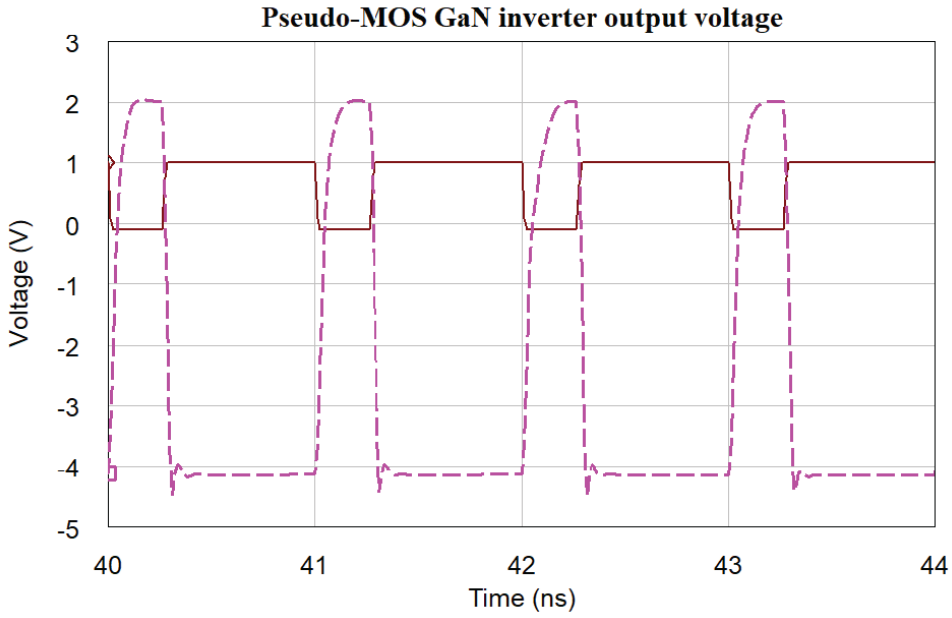


Figure 7.9: Input and output voltage of GaN inverter

give a good balance between rise and fall time and output current that is needed to drive a load. M3 and the two Z_R resistors simulate a captive load that the inverter will have to drive, i.e gates N-Path filter switches. The additional diode D is added to provide voltage clamping on the high end. This is due to the fact the gates in HRLs T3 process will get permanently damages if voltage greater than 2V is applied. Figure 7.9 shows the input

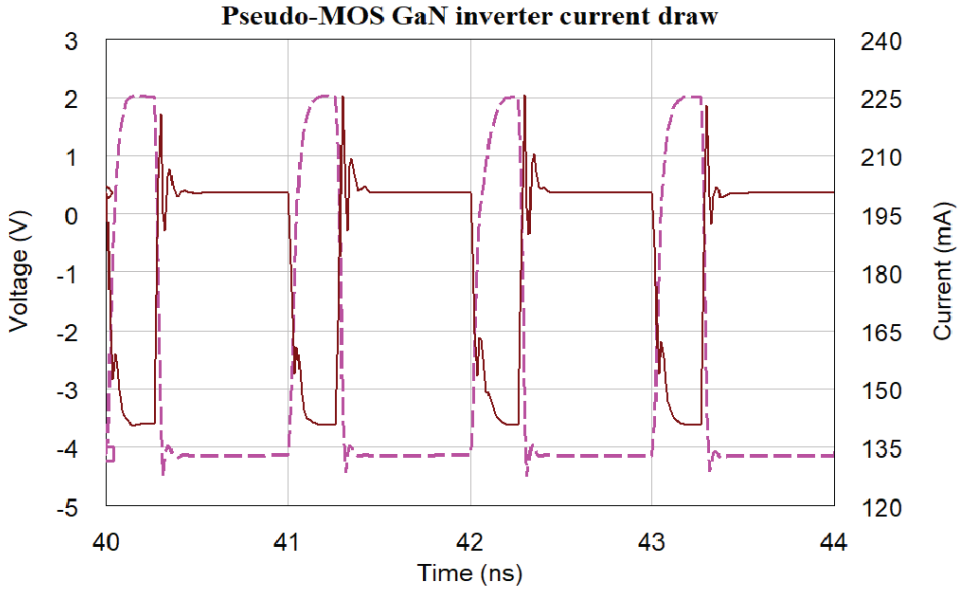


Figure 7.10: Current draw of GaN inverter overlayed with output voltage

(solid line curve) and the output (dashed line curve) voltages of the simulated inverter. The input waveform is a inverter version of a $1GHz$ square wave with a 25% duty cycle with a voltage of $1V_p$ (typical waveform for clocking N=4 N-Path filters). The output is the $1GHz$ square wave with a 25% duty cycle, but with V_{High} level of 2V and V_{Low} at -4V. The rising edge of the output wave is slightly longer than the falling, and this is due to the diode connected transistor in the pull up network not being full sized. This demonstrates that a fast inverter with voltage level shifting capabilities can be built in a GaN process.

However, there is a really big drawback to using a Pseudo-MOS inverter and that is power consumption. In Figure 7.10 dynamic current draw is show with output voltage overlaid. From this Figure it can be seen that even when the voltage is very low the current draw is over $130mA$, and when the voltage is high the current draw is close to $200mA$. Since we want VDD to be significantly larger then ground the power consumption with these currents is extremely large. Although, the max drain current for the HRL T3 process is close to 1.6A/mm, this power consumption level is not feasible for use with N-Path filter application [20]. If a N=4 N-path architecture is used then these inverters will be needed, which means that the power consumption just for the inverters will need

to be four times that of a single Pseudo-MOS inverter, which is very high. The power consumption of these inverters can be minimized in two ways and that is by making the transistors smaller which makes the Ron resistance larger thus reducing drain current, or make V_{DD} smaller. If the transistors is made smaller then the rise and fall time will increased due to the RC time constant that is created between the inverters R_{on} resistance and capacitance of the load transistor. N-Path filters require very fast clocks so reducing transistor size is not an option. Also, reducing supply voltage is not optimal because of the large negative voltage requirement for power handling.

7.7.2 Wide-band GaN Driver Circuit

As mentioned in the Pseudo-MOS section devices that are built in the GaN process are depletion mode. They typically have a large delta Voltage between on and off states. Connecting CMOS circuit directly to the N-Path gates will not turn them on/off fully. In order to have the filter switches turn on and off fully a driver circuit with a voltage translation is needed. One idea is to use a very wideband amplifier as a driver for the GaN switches in the N-Path filter. The clock generation will be in CMOS logic, and the driver and the N-Path filter will be in GaN process. The idea behind this is that the digital clock waveform is shown in figure 7.13 b) is periodic thus it has a Fourier series that are described by Equation 7.6. This can be reduced to Equation 7.7 for a pulse train with 25% duty cycle with. If all the harmonics for this series can be amplified then the resulting waveform is a scaled version of the original. Unfortunately, this is impossible as there is no amplifier that has wide enough band, but a good approximation can made with only first seven to ten harmonics.

$$V(t) = \frac{4A}{n\pi} + \sum_{n=1}^{\infty} \frac{2A}{n\pi} \sin\frac{n\pi\tau}{T} \cos\frac{2n\pi\tau}{T} \tag{7.6}$$

$$V(t) = \frac{4A}{n\pi} + \sum_{n=1}^{\infty^{n\neq even}} \frac{2A}{n\pi} \sin\frac{n\pi}{2} \cos\frac{2n\pi\tau}{T} \tag{7.7}$$

The proposed wideband amplifier is shown in Figure 7.11. It consists of two transistors M1 and M2, where transistor M2 is acting as an active load. M1 and M2 are chosen to be 2x25um devices, which is a good compromise between speed and current drive. The

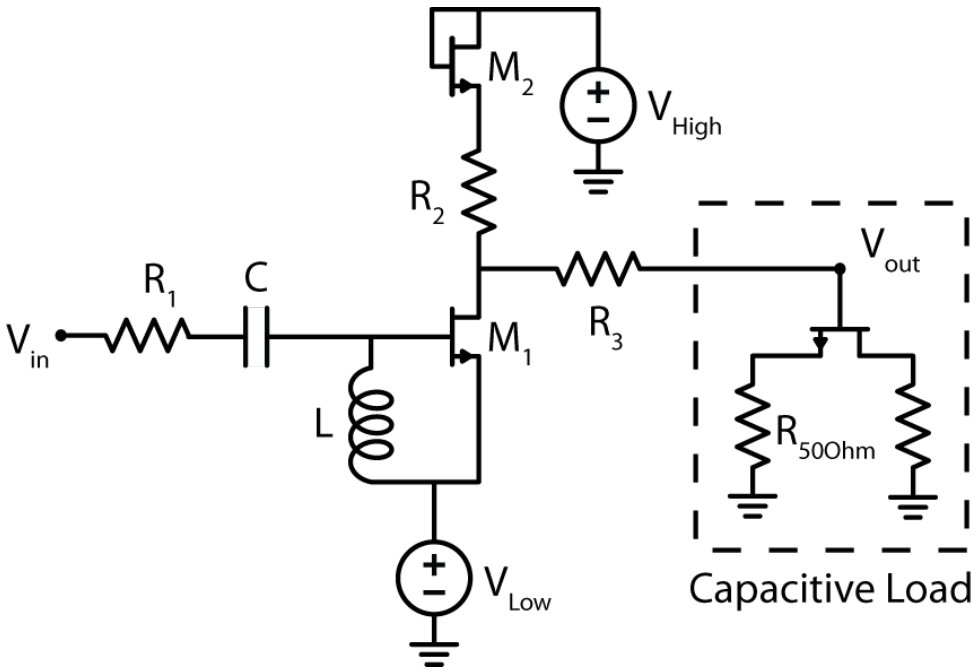


Figure 7.11: Schematic of the wideband GaN driver used to driver Gan switches with voltage level shifting

input capacitor is used for DC blocking between the CMOS IC and the GaN Driver. L is used to change the gain for different parts of the Fourier series harmonics. Resistors R1, R2, and R3 are used for matching in order to maximize the voltage gain on the load. The load for this driver is a gate of the transistor, this is to emulate the fact the this drive will be driving a GaN transistor switch. Because the requirement of the on/off voltage of the load transistor, the drain and source are biased at V_{High} and V_{Low}. Depending on what on/off voltages are needed, V_{High} and V_{Low} can be adjusted.

Time domain simulation results for this wideband driver-level shifter are shown in figure 7.12. This simulation shows the output voltage waveform when driven with a 2GHz square wave that is 1Vpp. The output voltage swing is from 1.5V to -5V. The current consummation for this driver is less than 40mA during the high phase of the wave form and less than 5mA during the low phase. Comparing this drivers current consumption to the Pseudo-MOS driver, this draws almost an order of magnitude less current.

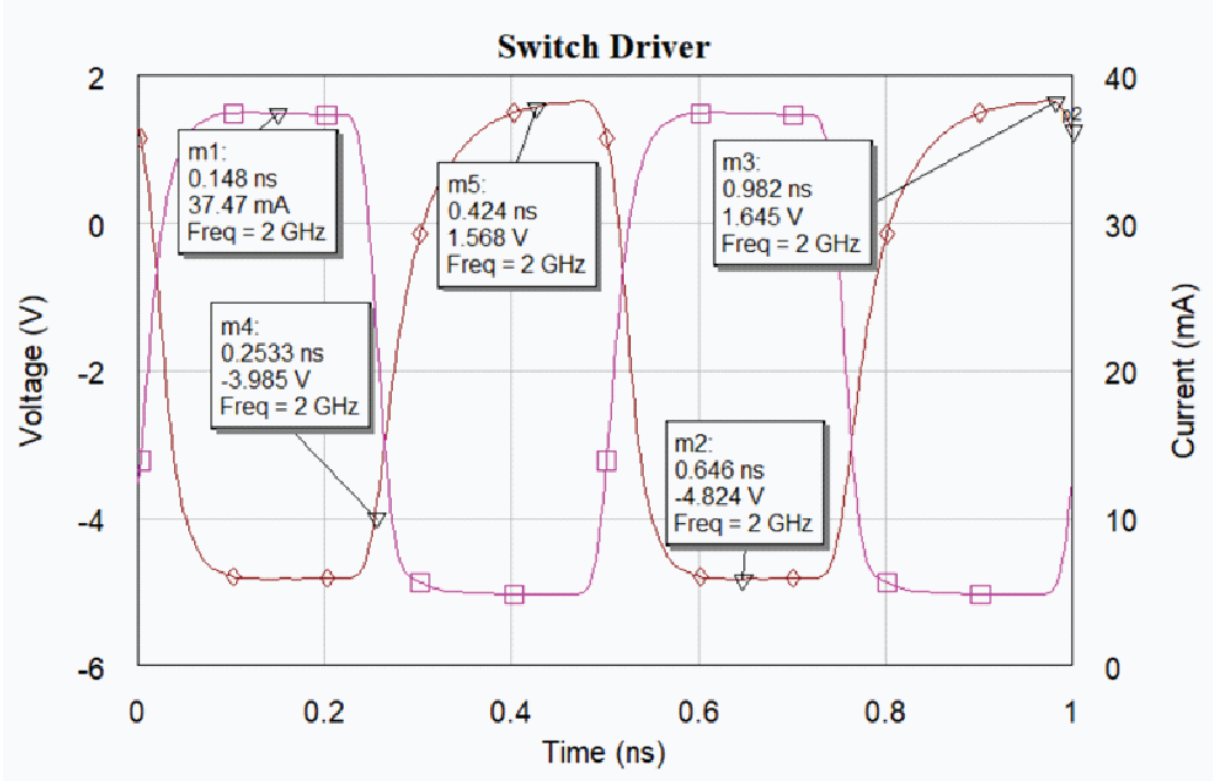


Figure 7.12: Output voltage of GaN driver and dynamic current draw

7.8 CMOS Clock generation

Since clock generation is not possible when using a GaN process, one idea is to use a standard CMOS process and use voltage level shifter to translate the CMOS output voltage to the GaN operating voltage levels. The overall architecture for the CMOS clock generation is shown in Figure 7.13. This design is very similar to the works shown by [39] but with a few changes. Fig 7.13 a) shows the internal clock generation network where CW is a sine wave with a frequency of $1/T_s$ and outputs a square clock CLK and its complimentary variant $\overline{CLK}$. The inverters in the chain are sized accordingly so that CLK and $\overline{CLK}$ have the save crossing point during transition. In Figure 7.13 b) the sub-circuit for the D-flip is shown. This consists of two transmission gates and two inverters. Figure 7.13 c) shows the high level schematic of the full clock circuit. The ring oscillator creates a 25% duty cycle waveform with a high period of T_s and outputs it on the node X. This waveform is passed through four D flip-flop chain. Each flip-flop delays the clock waveform by T_s consecutively at each latch point. The output of each flip-flop is taped off

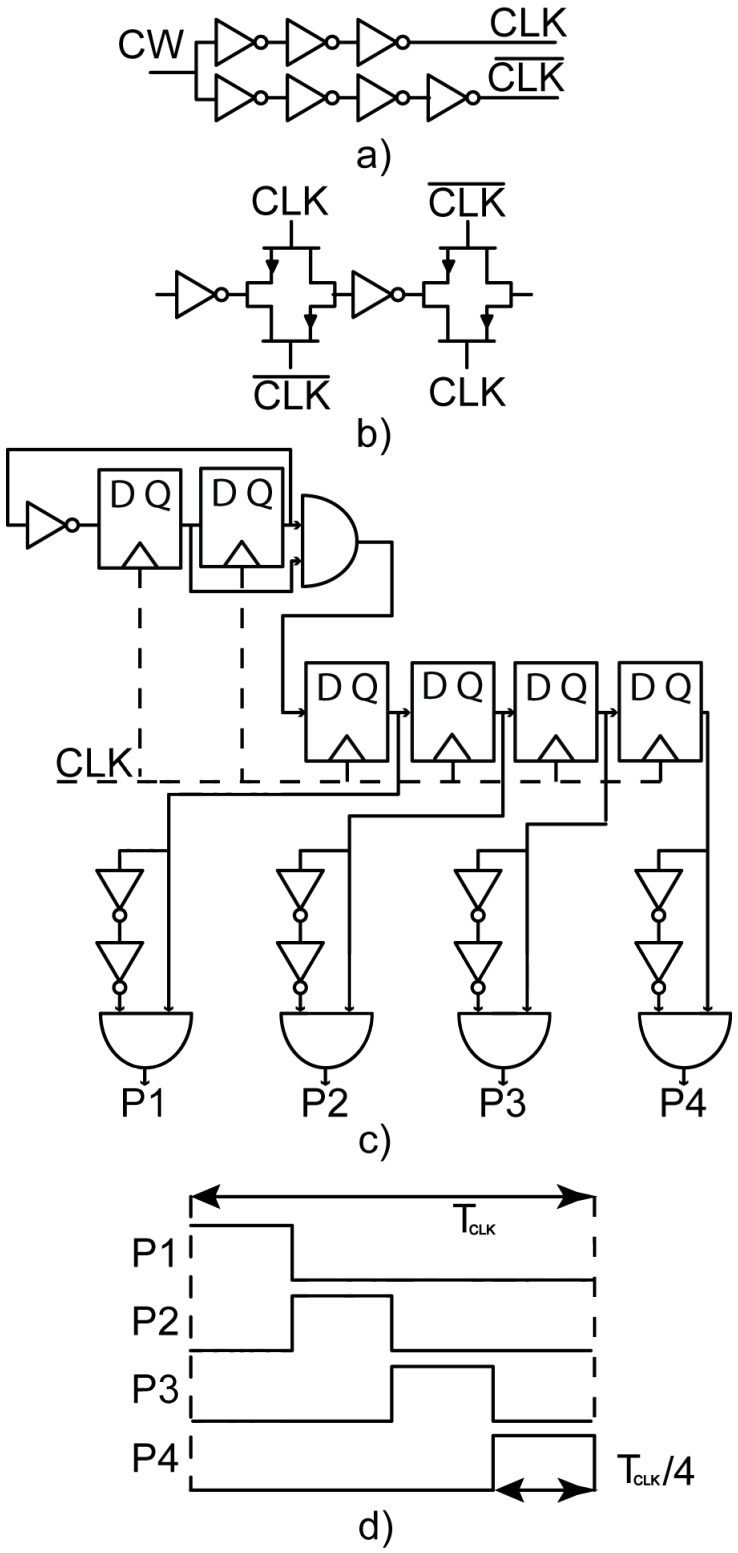


Figure 7.13: Schematic of the four phase none overlapping clock with 25% duty cycle designed in the CMOS process a) Differential Clock feed b) D-Flip Flop core c) Clock Generation circuit b) Ideal Four phase non overlapping clock

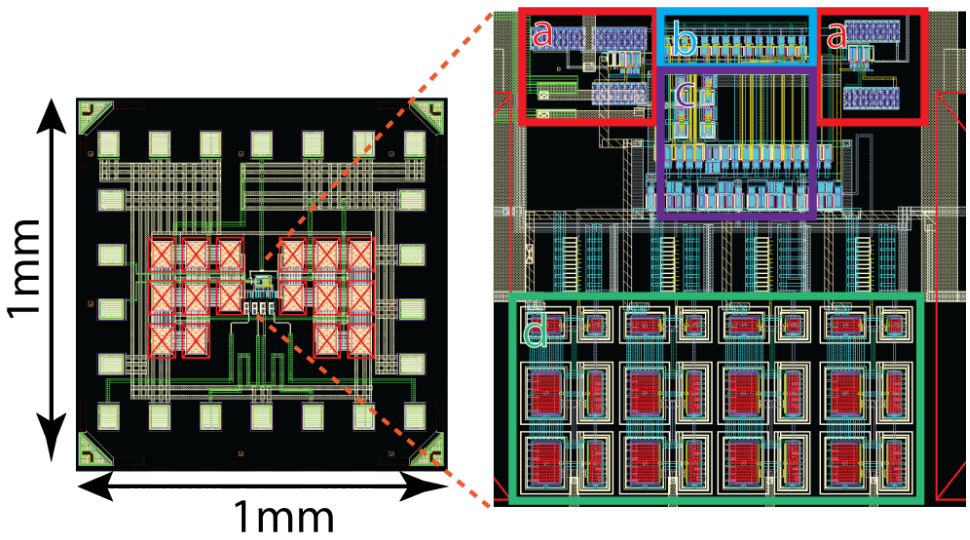


Figure 7.14: Layout of CMOC Clock IC in 65nm TSMC process

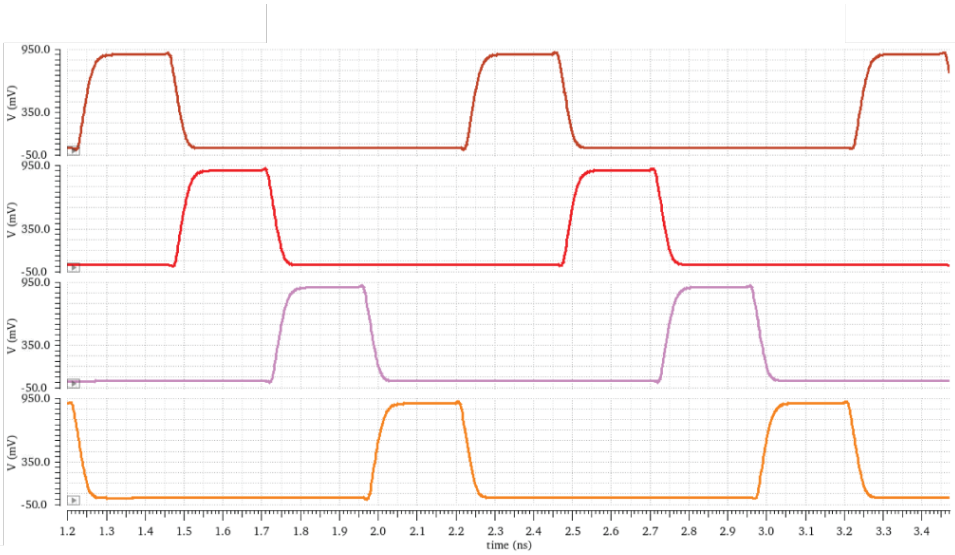


Figure 7.15: Simulated output of the CMOS four phase clock

to create the P_1', P_2', P_3', P_4' phases of the clock. Each of these phases of the clock pass through a dead time generation network which insures that there is no overlap between two consecutive phases of the clock. The expected, ideal waveform is shown in Figure 7.13 d).

For this work the TSMCs 65nm CMOS process was used to design the four phase none overlapping clock source. Figure 7.14 show the layout of the clock circuit. The total die

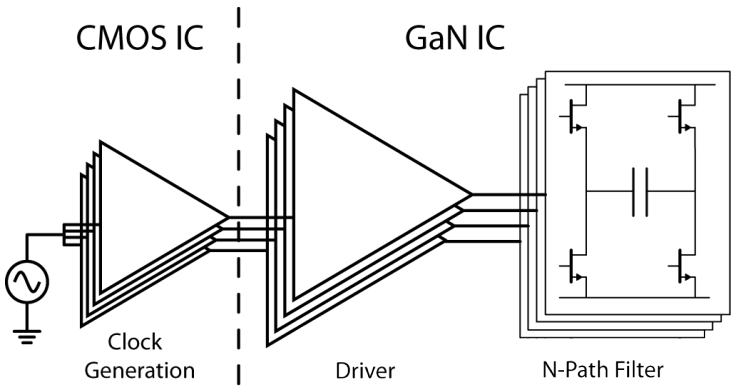


Figure 7.16: Architecture for CMOS, GaN N=4 N-Path filter integration

size is $1mm^2$ of which the core circuitry only takes up $0.01mm^2$ area. The rest of the IC area is taken up by the Input\Output pads and bypass capacitors. The simulated results of the four output clock are shown in Figure 7.15. All IC level parasitic capacitance and resistance, due to layout and routing, were extracted and included in the simulation. For simulation purposes, the load for the CMOS chip was a 500pf capacitor which emulates the gate of the GaN driver that this chip will drive. The simulation shows a good none overlapping in the four output phases. There is also no voltage ringing on the output node that typically happens when driving a reactive load.

7.9 Integration and Assembly

7.9.1 IC Integration

An architecture of the GaN/CMOS filter integration is shown in Figure 7.16. The dashed line in the middle represents the dividing boundary between the CMOS IC and the GaN IC. Since the driver and N-Path filter both need to be in the GaN process, they are integrated tightly on the same IC die. The picture of the die is shown in Figure 7.17.

7.9.2 PCB Integration

Having the clock generation circuit on a CMOS IC and the N-Path filter on GaN presents integration challenges.The clocks that are generated on the CMOS IC are fast and need to make it over to the GaN N-Path filter with reasonable integrity. There are a few ways that high speed IC can be integrated [44]. The most popular method is the use of

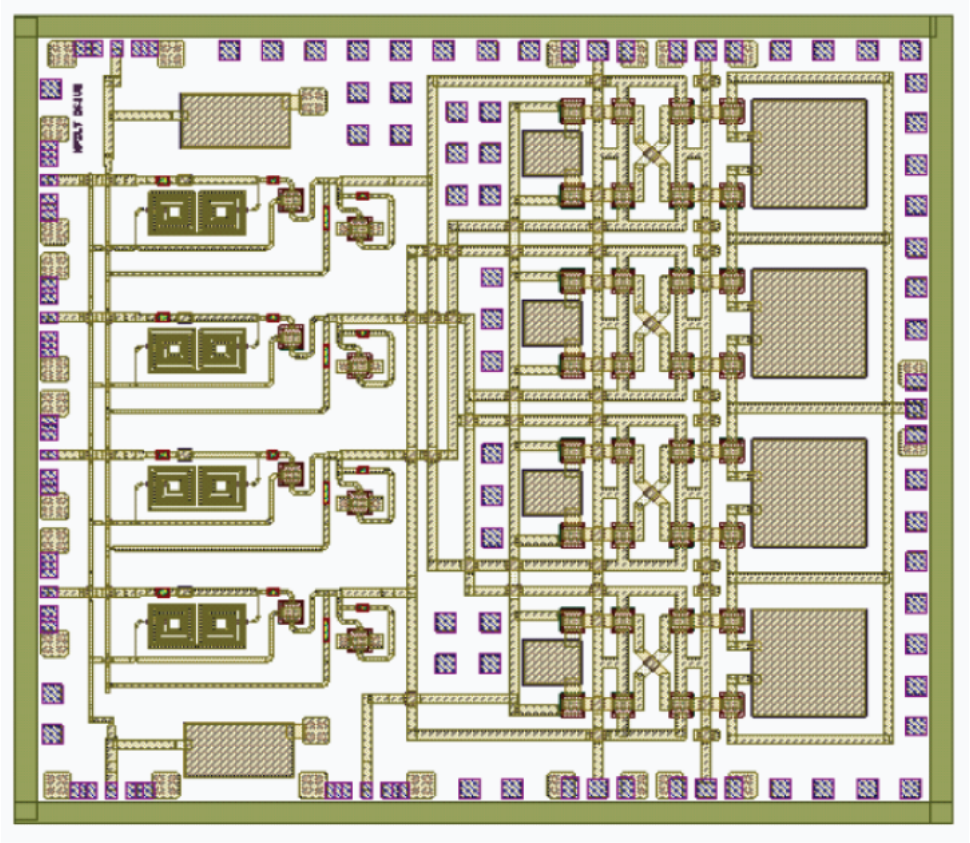


Figure 7.17: Layout of core N-Path filter with GaN driver

and interposer with flip-chip bonding or use of wire bonds. The interposer integration method can achieve tight integration with lower loss thus allowing for higher speed signals between IC [45], but this approach is expensive and takes a very long time to fabricate. An alternative is to use wire bonding method which is much cheaper and has a faster fabrication time. Figure 7.18 shows the difference between the two methods. Due to time and budget constraints the wire bonding method was chosen for integration of CMOS and GaN IC.

7.9.3 IC wire bond model for high speed

A simple way to model a wire bond connection is to use series L and R. This first order model is good for low frequencies and narrow band signals. When the signals become wideband, things like material and the type of wire needs to be considered for signal integrity purposes. There are two types of wires that are typically used in wire bonding,

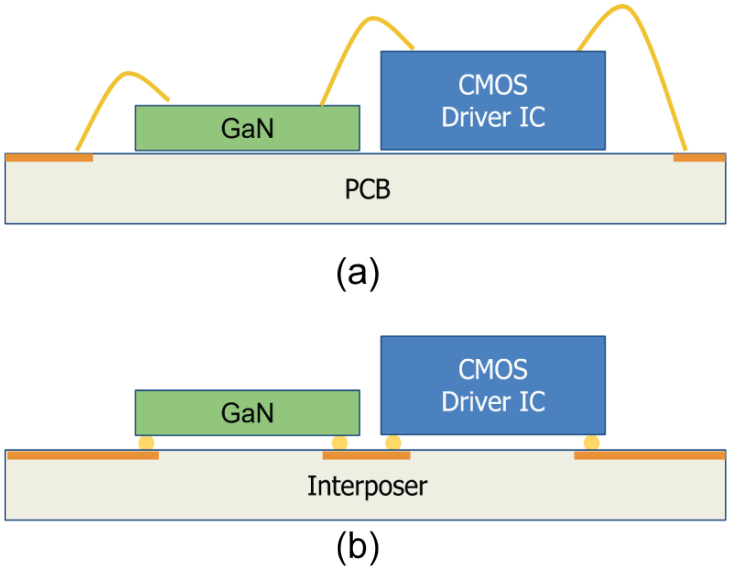


Figure 7.18: Two different IC integration methods a) On PCB using wire bonds b) On interposer using compression bonding

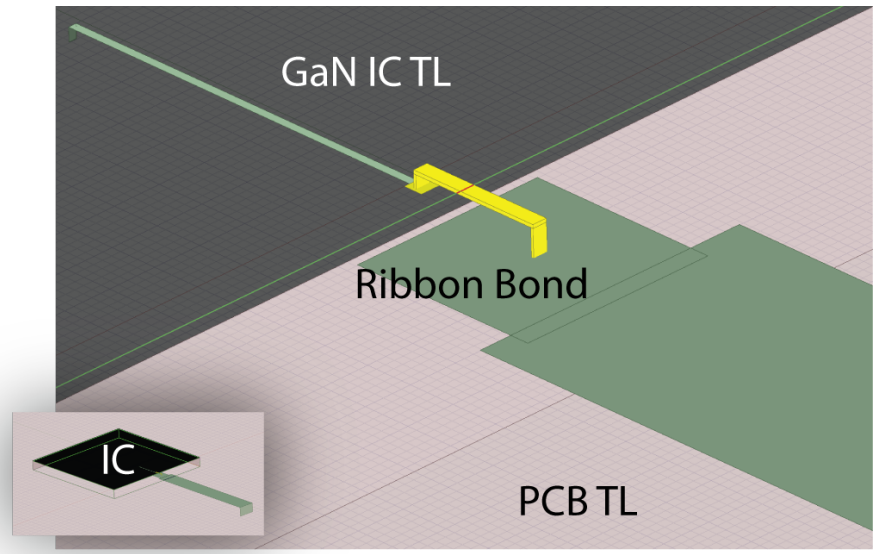
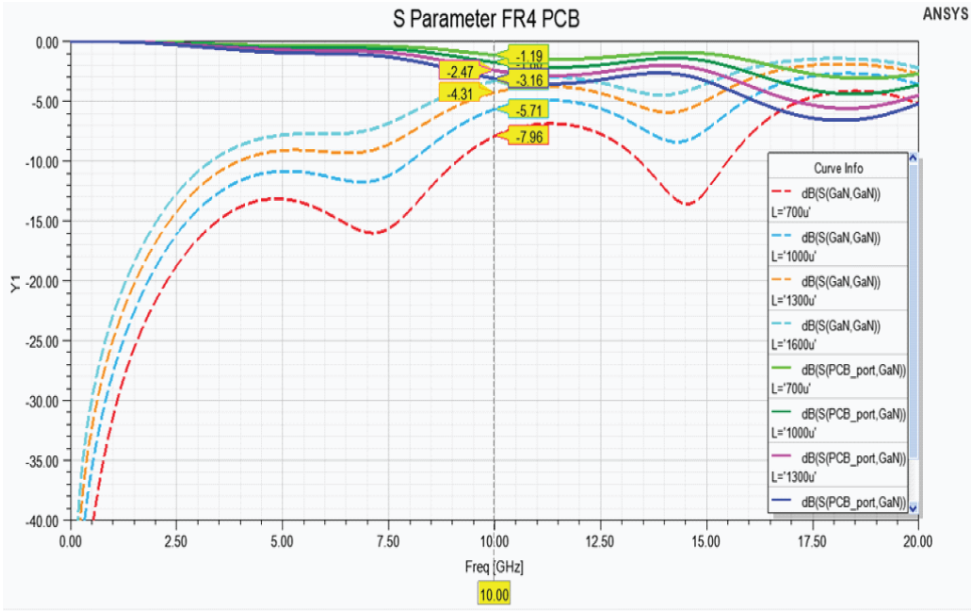
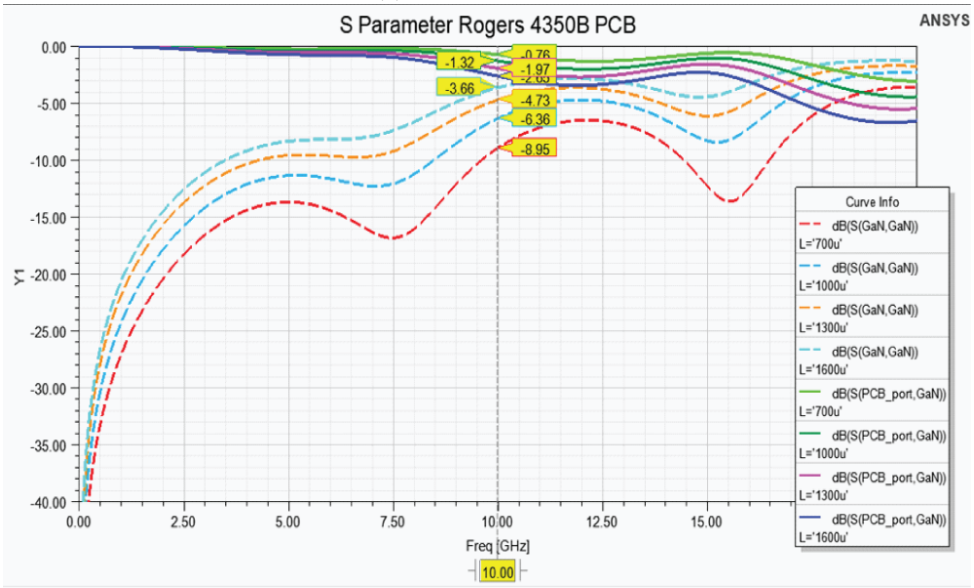


Figure 7.19: GaN IC Ribbon bond model in HFSS 3D EM solver

round and ribbon. It has been shown that ribbons and round wire can be both used for high frequency connections [46], [47], [48]. However material properties of the GaN IC and the PCB will have different effects on performance. A 3D EM simulation model was created to see how much effect different materials such as FR4 or Rogers 4350B have on



(a) FR4 PCB material



(b) Rogers 4350B PCB material

Figure 7.20: S-parameter simulation results of a gold ribbon-bond wire with different lengths

performance. The model consists of a 32mil PCB material with a 1.65mil copper trace that is 50Ohm. A gold ribbon bond wire lifts off the copper trace and lands on top of a SiC IC material that is 50um thickness. SiC is the base wafer that is used to construct GaN ICs. The IC is 10mm by 10mm in dimension. The ribbon landing pad on the IC is 100um by 100um which transitions to a 42um transmission 50ω line on the IC that runs for 2mm. A 50Ohm lumped port is placed at the end of the edges of PCB and IC transmission lines. A picture of this model can be seen in Figure 7.19. The simulation was ran with FR4 and Rogers 4350B substrates. FR4 PCB material is very cheap to manufacture especially when it comes to multiple layer PCBs, but has a poor performance at high frequency while Rogers 4350B substrate is specifically designed to be used up to 20GHz. The results of the simulation is shown in Figure 7.20 where the simulation was done up to 20GHz. In each simulation the ribbon bond-wire length varied from 850um to 1750um. From this simulation the results can be seen that for small bond-wires that are less then 900um, the insertion return loss is good up to 10GHz. Any length above that the return loss starts to degrade. One of the interesting observations is that FR4 PCB material has a slightly worse performance in comparison to Rogers with about 1dB of difference at $10GHz$. This is not a very significant difference and it indicates that both of the materials will work well. These results show that for a square 1GHz clock signal with 25% duty cycle, the first 10 harmonics will not experience significant attenuation because! of the wire bond as long as the bond length is kept below 900um in total length.

7.10 Measured results

The N-Path filter was assembled on custom two layer Rogers 4350B PCB board. The CMOS clock and the GaN N-Path were attached to the PCB with conductive silver epoxy. The designed N-Path filter is differential so two NCS4-102 Mini-Circuit baluns were used to convert a single ended input to differential and the differential output to single ended. These are the same baluns that were used in the correlator PCB with an average of .7dB of insertion loss per balun in the 1GHz pass band. All the wire bonding was done using 75mil ribbon bonds with care not to exceed 900um in total length. The

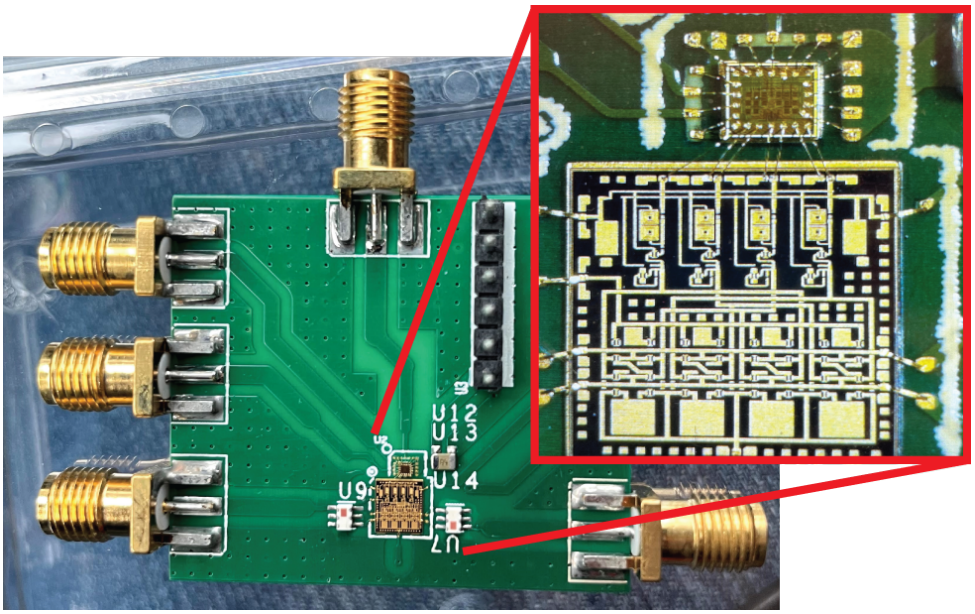


Figure 7.21: CMOS-GaN N-Path filter integrated on a Rogers 4350B PCB

assembled PCB is sown in Figure 7.21. The two port, small signal measurement was done using an Agilent E5071A network analyser, with a calibration done up to the cable ends. An HP8360 RF source was used to drive the clock frequency for the N-Path filter. The center frequency of the filter was 1/4 of the input clock frequency. To have the center frequency of 900MHz to 1.25GHz the input clock was swept from 3.6GHz to 5GHz. This measurement was repeated for the two different capacitor values switched in to the filter. The result for the large capacitor value is shown in Figure 7.22 and the result for the small capacitor is shown in Figure 7.23. There are a few interesting things that can be observed from these plots. The total DC power consumption for the GaN N-Path filter filter was 787mW. This included the 755mW for on chip GaN driver and the 32mW for the CMOS clock generation IC. In comparison to a full CMOS implementation which only uses 73mW total, this is 10 times times more. Although the large power consumption might be unattractive for applications that require low power, there are application that need large RF power handling at any cost. Power measurement were not done on the filter as the CMOS IC stopped working shortly after the small signal measurement was completed. This was due to the fact that the CMOS IC did not have any ESD protection on any of the IOs.

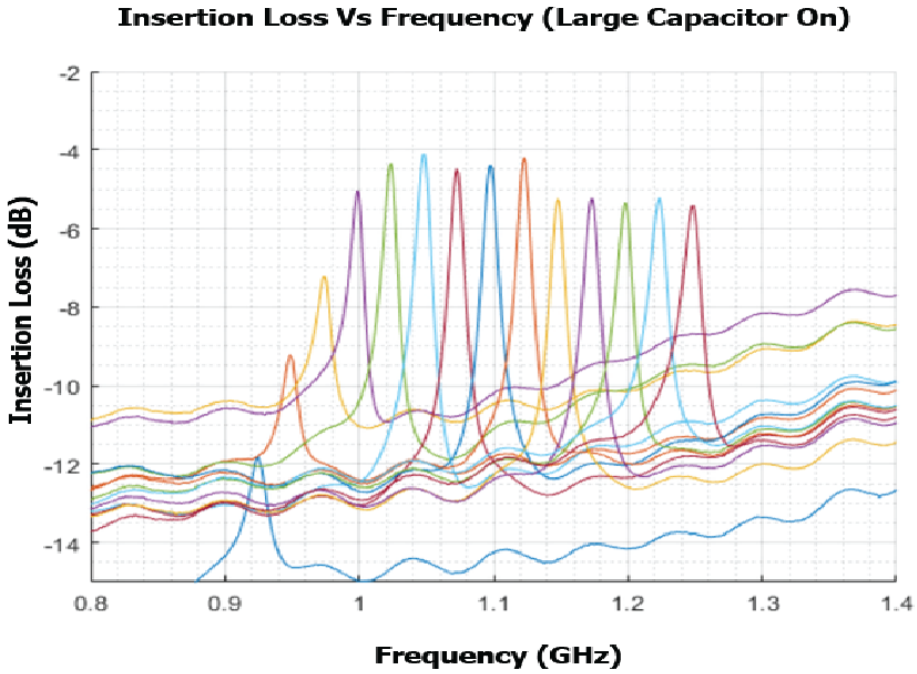


Figure 7.22: Measurement of GaN N-Path filter with CMOS clock, Large capacitor is engaged for narrower pass band

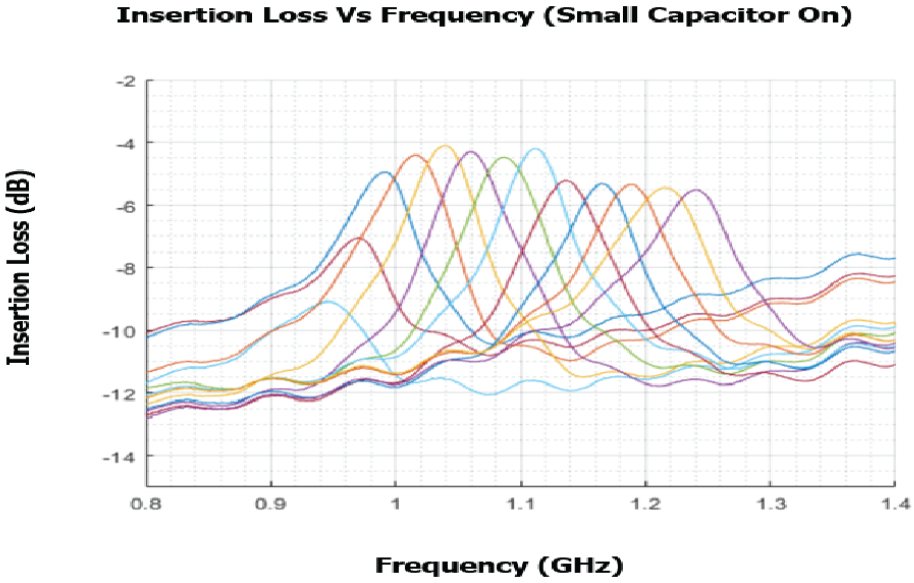


Figure 7.23: Measurement of GaN N-Path filter with CMOS clock, Large capacitor is engaged for wider pass band

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Table 7.1: N-Path Comparison

GaN N-Path filter comparison				
	This Work	[41]	[40]	[36]
Technology	40nm GaN	250nm GaN	400nm GaN	65nm CMOS
Tunable frequency range	.5-1.5GHz	.2-1.9GHz	50-300MHz	.1-1.4GHz
Tunable bandwidth	5 or 20MHz	NA	NA	NA
Out-of-band rejection	12dB† 8dB ‡	18dB	30-50dB	55dB
Insertion Loss	-3.3dB*	-2.5-5dB	-10dB	20dB
1dB Compression point	18.8dBm	18dBm	17dBm	8dBm
IIP3	>40dBm	37.5dBm	24.6dBm	23dBm
Clock generation	CMOS IC	External	External	On-Chip
DC power (mw)	787mW	NA	NA	50-73

* This insertion loss is de-embedded from the measurement as the circuit required a balun at the input and output

† Simulated

‡ Measured

Chapter 8

Self Interference Mitigation

Wireless communication systems have always strived to achieve better bandwidth efficiency, while at the same time mitigate interference. One of the holy grail of bandwidth efficiency is to operate transceivers in full duplex mode (FD), where the transmitter and receiver are occupying the same time and frequency space. These types of systems are also known as simultaneous transmit and receive (STAR) transceiver. FD is way more desirable over a typical transceiver that operate in half duplex (HD) because theoretically bandwidth efficiency is increased two fold. The main challenge for a STAR transceiver is its own transmitters power which becomes a large interference at the receiver. Typical

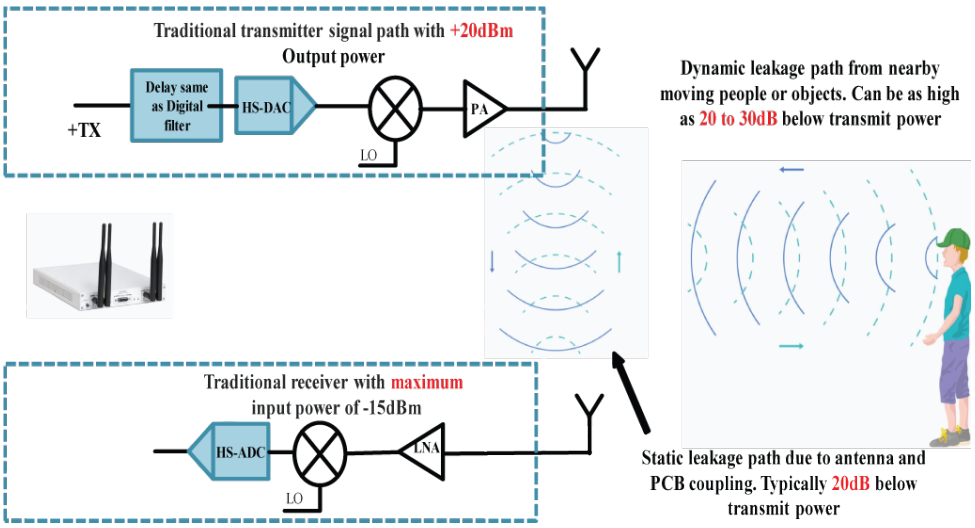


Figure 8.1: Self interference problem for transceivers that are operating in full duplex mode

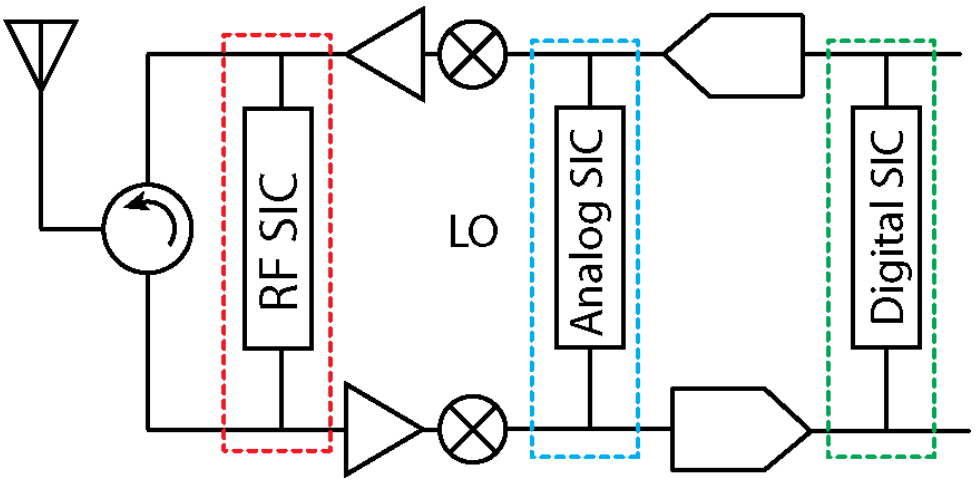


Figure 8.2: Self interference cancellation is typically done in a) RF b) Base-band and c) Digital domains

communication systems need to transmit 20-30dBm of power while at the same time the received power level is around -80 to -70dBm [49]. In the same transceiver the isolation between the transmit PA and the receivers LNA is 20-30dB. This means the during simultaneous operation large amounts of power will leak from the transmitter (TX) to receiver (RX) and can potential saturate analog components such as LNAs or ADCs. This type of power level difference between TX and RX makes full duplex architectures very challenging to say the least. Receivers are typically optimized to receive very low power levels and as such don't fair well in the presence of very large signals. Also the leaked TX signal is seen as noise from the point of the receiver. This has the effect of massively degrading the Signal to Noise (SNR) ratio. The challenge of STAR transceiver system can be seen in Figure 8.1. One way to look at the received signal is as a summation of the desired signal and addition of the summation all the undesired leaked/reflected self transmit signal.

$$R_{Signal\ at\ receiver}(t) = R_{Desired\ signal}(t) + \sum_{n=1}^{\infty} A_n R_{Own\ transmitter}(t - \theta_n) \tag{8.1}$$

8.1 Methods for Self Interference cancellation

To solve this issue, a lot of work has been done to remove or cancel the transmitter powers. Cancellation can be done in RF, analog and digital domains or a combination of the three as shown in Figure 8.2

8.1.1 Analog

8.1.1.1 TX RX antenna placement

The simplest way to achieve isolation between TX and RX is by clever placement/design of TX and RX antennas [50]. This method can archive 20-30dB of isolation between TX and RX channels. Down side of this method is that it only considers one leakage path and is limited to the 20-30dB of leakage suppression.

8.1.1.2 Circulators

Historically in RF domain, magnetic circulators have been used to provide isolation between TX and RF, but they are typically very large in size, and offer only 15-20dB of isolation for a single leakage path. There has been a lot of work on magnetic-less time-varying circulators [51]. These works show that a completely integrated circulators can be built in a tightly integrated process, be tunable, have 3% fractional bandwidth and handled well over 35dBm of input power. Although this work is very novel and notable, it alone is not sufficient enough to cancel out the self leakage power to the required level.

8.1.1.3 Taps

Lately there has been lot of work done in the use of tap-delay lines for self interference cancellation in analog domain [52] [53] [54]. The idea of this method is to tap off some power from the transmitter invert the amplitude, add proper delay and inject it into the receiver chain.

$$\begin{aligned} R_{Signal\ at\ receiver}(t) = R_{Desired\ signal}(t) + \sum_{n=1}^{\infty} A_n R_{Own\ transmitter}(t-\theta_n) \\ + \sum_{k=1} A_k R_{Tapped\ signal}(t-\theta_k) \end{aligned} \tag{8.2}$$

This can be done at RF before the LNA, and at baseband before the ADC. This method works well if the are only a few major leakage paths. A real challenge arises when there there are many multiples paths that need to be accounted for creating a need to many taps which might be impossible to implement in hardware.

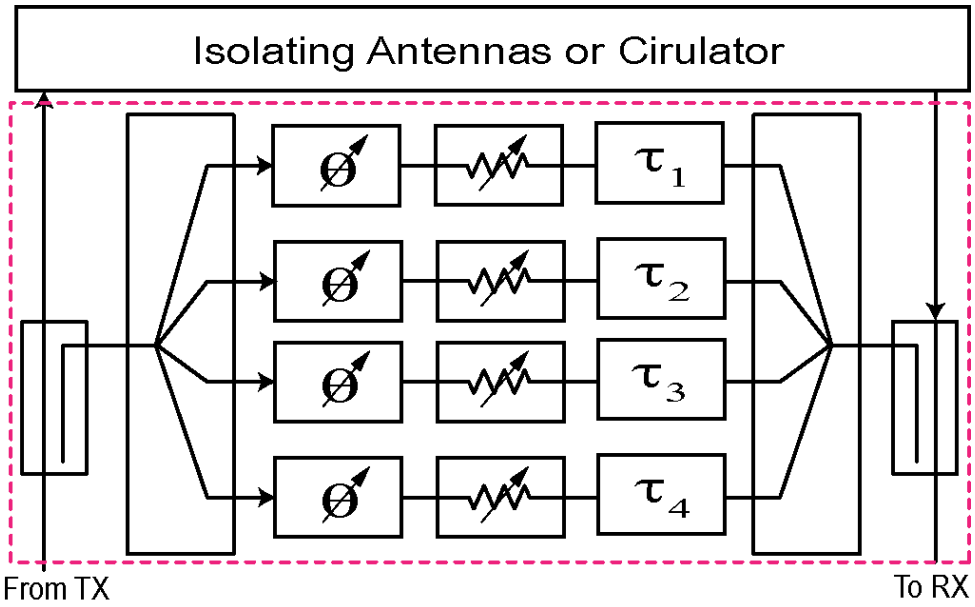


Figure 8.3: Block diagram of the self interference cancellation at RF using four taps with control over delay and amplitude

8.1.1.4 Code Domain

Another way to achieve self interference cancellation is to use code domain methods in analog domain as shown in previous section of this work. We can chose TX and RX to be multiplied by codes that are orthogonal to each other thus creating natural isolation between TX and RX. This method will be discussed in more detail later in this publication.

8.1.2 Digital

In parallel to the analog domain, there has been much work done ins doing self interference cancellation in the digital domain right after the ADC [55] [56] [57]. These methods use algorithms such as channels estimation, polynomial models, and neural networks to cancel out the leaked TX signal. These methods have shown that up to 60dB of cancellation is possible. In order to achieve the necessary level of self interference cancellation, digital methods will have a prominent role, but they can't be used by themselves. Digital methods can only archive cancellation on the back end with the assumption that the frond end receiver electronics are operating nominally and is not saturated.

8.2 Tap delay Self Inference cancellation before LNA

The approach taken by this work is to initially do cancellation in the RF domains by tapping of the power right after the power amplifier. The idea is to tap off from TX signal, right after the transmit correlators and inject it before the receive correlator on the RX side. A block diagram of the method is shown in Figure 8.3. To couple power in/out of the main lines, a Minicircuits bidirectional coupler BDCA1-6-11+ was used. This couples -6dB of power from the main TX line. Right after the coupler a Minicircuits SEPS-4-272+ splitter was used to split the signal into four different taps. Each tapped paths consisted of a Minicircuits JSPH-1000+ phase shifter and a Minicircuits SVA-2000+ voltage controlled variable attenuator. Four of the phase shift/attenuate PCBs are places in parallel after the four way splitter. The output of these four circuits goes directly into the same power splitter that is used on the input, but here it serves as a combiner with 6dB loss. Lastly, all the combined outputs are injected into the RX line via an identical coupler as the input. A fixed delay via different cable lengths is added to each tap to facilitate the different delays that a TX signal will experience by antenna. The system was designed to be completely modular. Each of the above mentioned components was placed on individual PCBs designed on FR4 material. The pictures of these PCB can be seen in Figure 8.5

8.2.1 Results

The modular was connected in accordance to Figure 8.4. Two port small signal measurement was done using an Agilent E5071A network analyzer, with a calibration done up to the cable ends. Port one was connected to TX and port two was connected to the RX. Four Rigol DL300 dc power supplies where used to power the attenuators and the phase shifters. A 36dB attenuator was connected on the output to emulate the initial isolation that two antennas or a circulator might provide. The result for the measurements are shown in Figure 8.6.

When the cancellation circuit is off, the leaked signal from TX to RX is -42dB (with most of the isolation coming from the 36dB attenuator). The other 6dB comes from the couplers and the coax wires. When the cancellation circuit is on 20dB of cancellation is

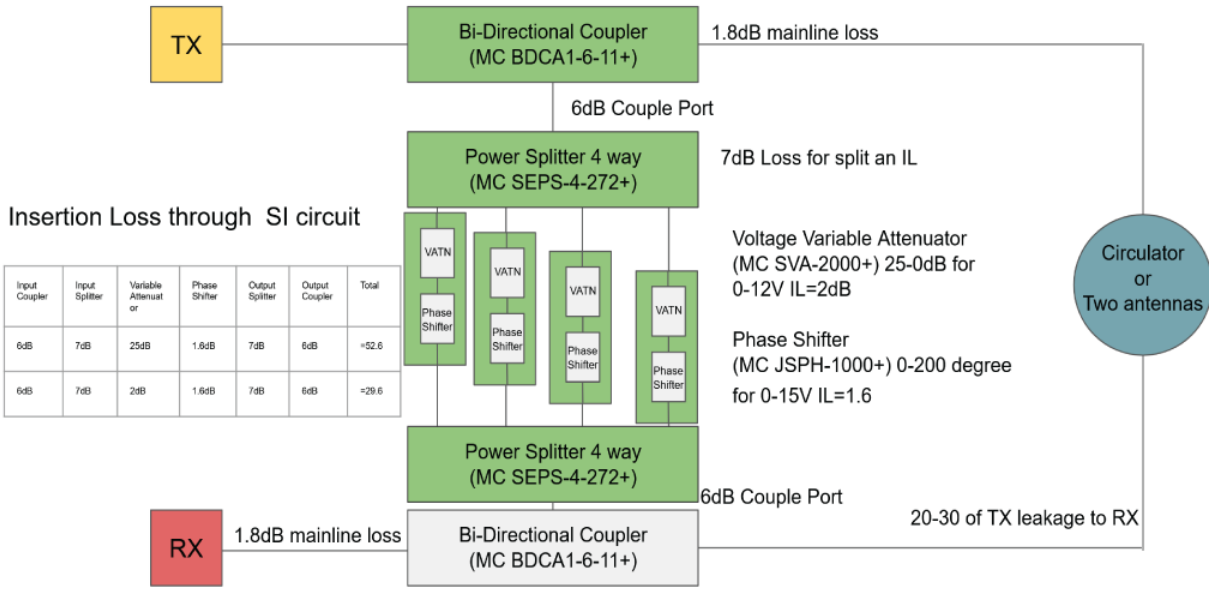


Figure 8.4: Modular Self interference cancellation circuit with four cancellation paths

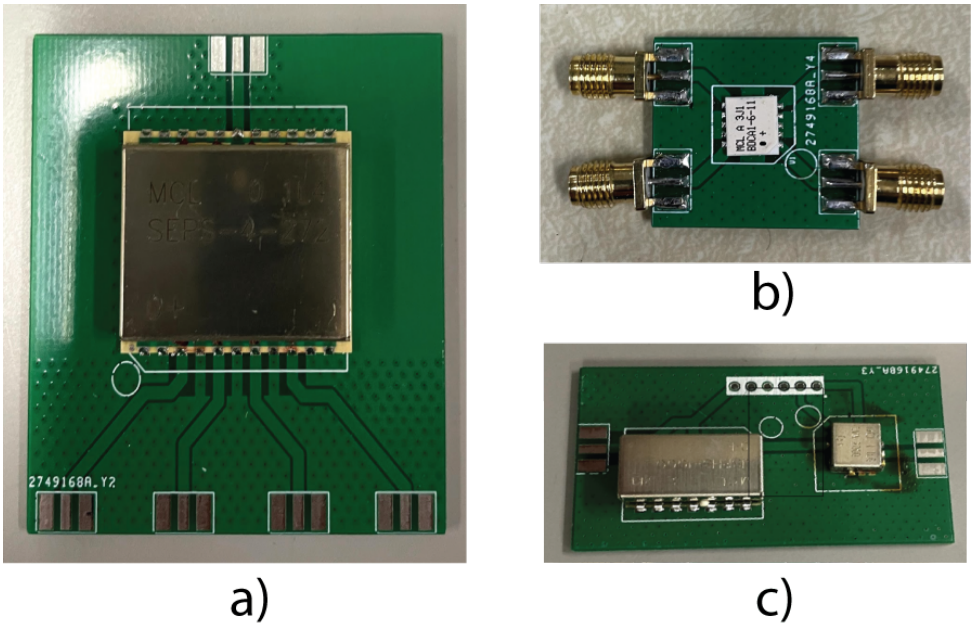


Figure 8.5: Modular PCB for Four tap self interference cancellation a)Four way splitter, b) Bidirectional coupler, c) Attenuator and phase shifter

provided over 63MHz of bandwidth, and 30dB of cancellation over 63MHz.

Although, this method does provide Self interference cancellation it is very much band limited. The band limitation is due to the number of delays that are possible with the

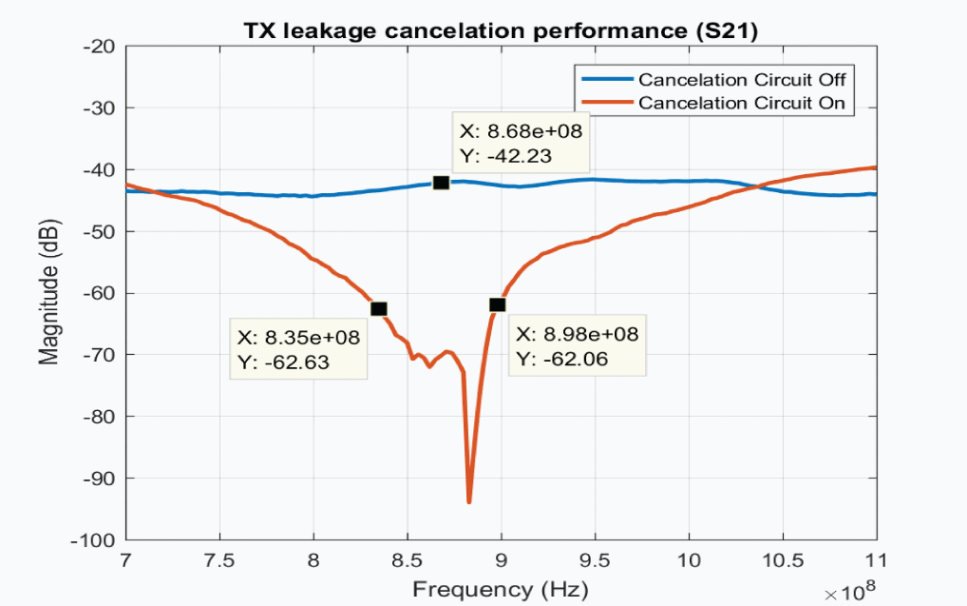


Figure 8.6: Measured results of modular four tap self interference circuit

current setup. In our approach the delay is set by the length of the coax lines. These fixed delays might not exactly correspond to the delay of the reflections. We can approximate the delays of all the major reflections, but once cancellation gets below 20dB all the minor reflections and the ones that are further out start coming into play. In our setup we only had four taps and a ideal attenuator to emulate an antenna or circulator, but this is insufficient for real systems. There are many possible points of reflections, such as SMA connectors, solder joints, antenna reflection, etc. This problem becomes even more challenging as soon at the TX signal leaves the antenna. The number of reflection points becomes infinite, as do the delays. Although, we have show that we can cancel out some of the primary leakage paths. However, in order to achieve good cancellation, all the leaked paths, and their delays need to be accounted for. Another challenge for these types of circuits is the resolution of the phase shifts and attenuators. For this experiment we used a voltage controlled attenuator, which gave a good resolution for coarse cancellation value. However to achieve cancellation above 40dB the control resolution was too sensitive. This means that there is an point when noise on the control line will limit the amount of possible cancellation.

8.3 Code domain Self Inference cancellation

In a system architecture, such as the one demonstrated in this work, one can exploit the fact the TX and RX correlators use different codes to spread and despread the signals 8.7. These codes can be chosen to be part of the same family and have excellent cross correlation properties. We have demonstrated in this work that for a fixed filter bandwidth, different spreading sequences lengths L that spread signals to bandwidths that are a multiples of the filters bandwidth, the energy that falls outside the bandpass filter will be removed. As shown in 3.5, after the bandpass filter the unwanted energy that is spread is attenuated by a factor of $1/L$ or $10log(1/L)$. For demonstration purposes we used a codes of lengths 127 and 255. These theoretically will yield $21dB$ and $24dB$ of isolation between TX and RX.

8.3.1 Code Domain Nulling effect in continuous time

During the testing of the aforementioned code domain self interference cancellation, it was observed that more or less cancellation can be achieved for particular offsets between the two codes. This can be clearly seen in Figure 6.7 where the energy is measured for a particular code correlation with itself and three other codes at different offsets. This can also be seen in the simulation of the auto-correlation of a single sequence in Figure 3.2a. Both simulation and measured results show that when the codes are aligned with specific factional chip times the lower bound of $1/L$ no longer applies and better cancellation can be achieved. This same phenomena was also observed in recent SIC works done by Hamza [58], but no explanation was given as to why this occurs.

8.4 Spectrum shaping

The theory as to why this occurs is that when the offset between chips is no longer limited to discrete multiple of chip times T_s and can take on arbitrary fraction of chip time, T_s/α where α is a real number, different frequency components are created. Depending on the alignment of the two spreading sequences $C(t)$ and $D(t+\tau)$ during the final multiplication process there could be a particular τ that will generate frequency content that is further away from the center frequency. We call this technique "spectrum shaping" because the

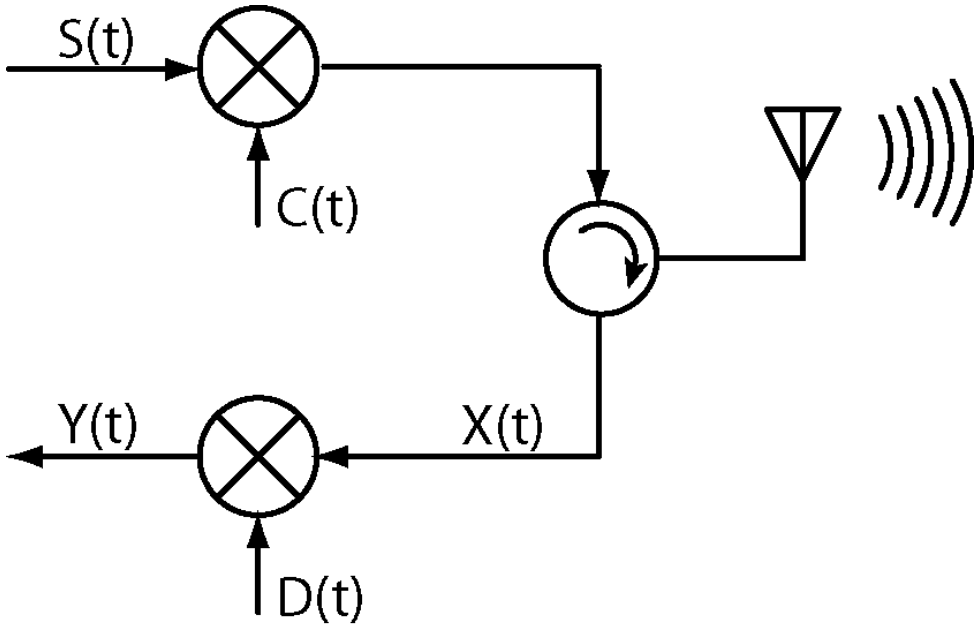


Figure 8.7: Diagram of transceiver equipped with code-domain self-interference cancellation. When $C(t)$ and $D(t)$ are periodic, quasi-orthogonal spreading codes with a specific time offset, $S(t)$ may be significantly attenuated in $Y(t)$.

spectrum of the signal can be shaped in such a way to minimize the amount of energy that will pass through the bandpass filter.

8.4.1 Theory of Operation

Consider transceiver that is designed to transmit signal $S(t)$ and receive signal $Y(t)$. Both the transmitter and receiver signals are band limited to B_s. The architecture of this type of transceiver is shown in Figure 8.7. The spreading code $C(t)$ in the transmitter branch can be described as

$$C(t) = \sum_{k=-\infty}^{\infty} c_0(t - kT_s), \tag{8.3}$$

$$c_0(t) = a[\ell]p(t - \ell T_c) \quad \ell = 1, 2, 3...L \tag{8.4}$$

$$p(t) = \sqcap\Big(\frac{t - T_c/2}{T_c}\Big), \tag{8.5}$$

This sequence $C(t)$ repeats over interval of T_s and c_0 is a pseudo random sequence of length L and every bit in the sequence takes a set time interval of T_s and $a[\ell]$ are integer coefficients taking form of 1 or -1 depending on the spreading sequences. Similarly, the

code $D(t)$ at the receiver branch is

$$D(t) = \sum_{k=-\infty}^{\infty} d_0(t - kT_s) \tag{8.6}$$

$$d_0(t) = b[\ell]p(t - \ell T_c) \quad \ell = 1, 2, 3...L \tag{8.7}$$

The crosscorrelation of the two spreading codes is give by

$$R[n] = \frac{1}{L} \sum_{\ell=0}^{L-1} a[\ell]b[\ell + n], \tag{8.8}$$

and because both spreading codes are (quasi) orthogonal,

$$\big|R[n]\big| \ll 1 \quad \forall n. \tag{8.9}$$

Typically, this correlation function is bounded on the lower end as the offset between the code is bounded by an integer value. For codes that are designed to have best autocorrelation such as m-sequence, this value is bounded to $1/L$.

$$|R[n]| \geq \frac{1}{L} \tag{8.10}$$

Now consider an arbitrary timing offset between transmitter and receiver codes. Dismissing the received signal, noise and distortion, but accounting for a timing offset τ between spreading codes, we can describe the received signal $Y(t)$ originating from $S(t)$ as

$$Y(t) = S(t)C(t)D(t - \tau), \tag{8.11}$$

where the offset τ is a real number that can take on any value. This offset can be assumed as a timing offset between the rectangular pulses p.

$$C(t)D(t - \tau) = \Bigg(\sum_{k=-\infty}^{\infty} a[\ell]p(t - \ell T_c - kT_s) \Bigg) \Bigg(\sum_{k=-\infty}^{\infty} b[\ell]p(t - \ell T_c - kT_s - \tau) \Bigg) \tag{8.12}$$
$$\ell = 1, 2, 3...L$$

Due to the introduced real number offset τ the crosscorrelation is no longer bounded to the lowest value of $1/L$. A good way to see this recast the chip time to account for the timing offset τ. Assume the new chip-time T_c' is defined as

$$T_c' = GCF(\frac{T_c - \tau}{T_c}, \frac{\tau}{T_c}) \tag{8.13}$$

We define i to the number of T_c' chips needed to make the original T_c chip time

$$i = T_c/T_c' \tag{8.14}$$

This would mean that we will need to define the length of the sequence to be iL in length.

$$\ell' = 1, 2, 3...iL \tag{8.15}$$

Now the crosscorrelation of the two spreading codes with the recast chip time and sequence is give by

$$R[n] = \frac{1}{iL} \sum_{\ell'=0}^{iL-1} a[\ell']b[\ell' + n] \tag{8.16}$$

Examining Equation 8.16 we can see that there is potential for this to take on a smaller value than the original crosscorelation with no τ timing offset. Also, we can see from Equation 8.16 that if $\tau = 0$ the Equation 8.16 will just simplify Equation 8.8

$$|R[n]| \begin{cases} \frac{1}{iL} & \text{if } \tau \neq 0 \\ \frac{1}{L} & \text{if } \tau = 0 \end{cases}$$

An alternative way to understand what is happening is examine $Y(t)$ signal in frequency domain. After the multiplication the offset shown in equation 8.12, and recasting of the chip time shown in equation 8.16 we can see the new chip time T_c' is smaller then T_c. This means that in frequency domain the $Y(t)$ with the timing offset τ will have a higher frequency content in comparison to $\tau = 0$.

Since τ can take on any arbitrary number there are many different possible offsets and each will have a different effect on SIC. The offsets that we are very interested in are the ones that will generate more high frequency content and reduce low frequency content. If a filter with a bandwidth of $1/127T_c$ is used as an integrator and the spectrum is reshaped there is a chance that the correlation will result in a value less than $1/L$.

8.5 Example

To see the derivation from the previous section a little more clearly, we will derive an example of how the spectrum shaping happens for a simple sequence. The two sequences

selected for this example do not have any special design and are purely selected by the author to illustrate the example of spectrum shaping.

Consider the two random sequences α shown in Figure 8.8a and β shown in Figure 8.8b. These simple sequences are considered to be periodic and each chip period is T_c and the whole chip period of $5T_c$. Figure 8.8c show when α is multiplied by β with no timing offset. Figure 8.8d shows when α is multiplied by β that is offset by 1/4 of T_c. For this particular example, to make the calculation simpler we can let $T_c = 1$ and the magnitude of each period be 1. These results are periodic so a Fourier series can be derived for them and can be expressed in exponential form shown in 8.17.

$$f(t) = \sum_{n=-\infty}^{\infty} D_n \exp(jnt2\pi/T_o) \tag{8.17}$$

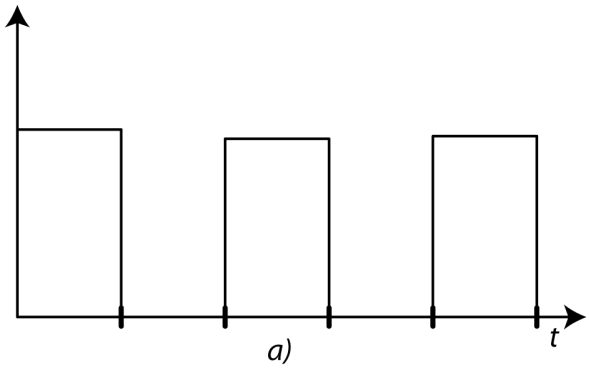
The coefficient for the resulting waveform $\alpha \times \beta$ with no offset shown in Equation 8.18 and its magnitude in Equation 8.19.

$$D_n = \frac{1}{5}\int_0^1 \exp(-jnt2\pi/T_o)dt \tag{8.18}$$

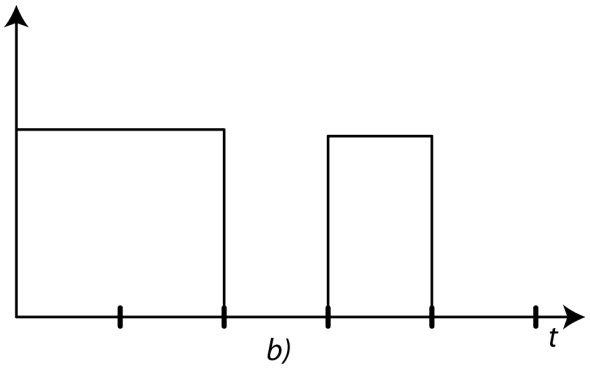
$$|D_n| = \frac{\sqrt{-2(cos(\frac{2n\pi}{5}) - 1}}{2|n|\pi} \tag{8.19}$$

The coefficient of the resulting waveform of $\alpha \times \beta(t - \frac{1}{4}T_o)$ with a quarter of a chip time offset is shown Equations 8.20 and its magnitude in Figure 8.21

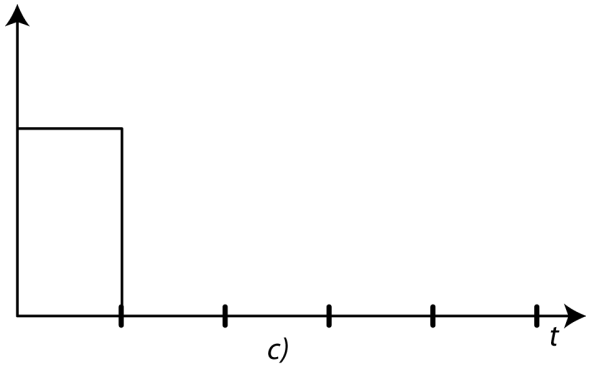
$$D_n = \frac{1}{5}\left(\int_{.25}^1 \exp(-jnt2\pi/T_o)dt + \int_2^{2.25} \exp(-jnt2\pi/T_o)dt + \int_4^{4.25} \exp(-jnt2\pi/T_o)dt \right) \tag{8.20}$$



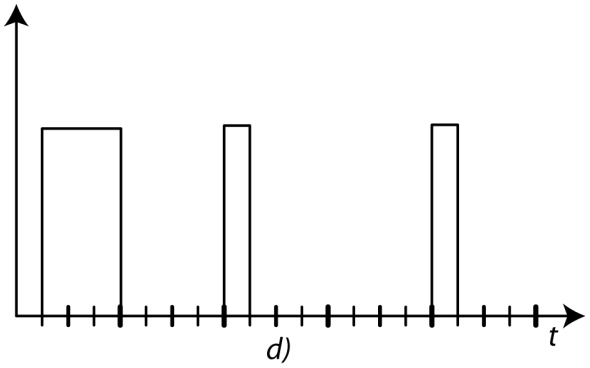
(a) Random sequence α of length 5



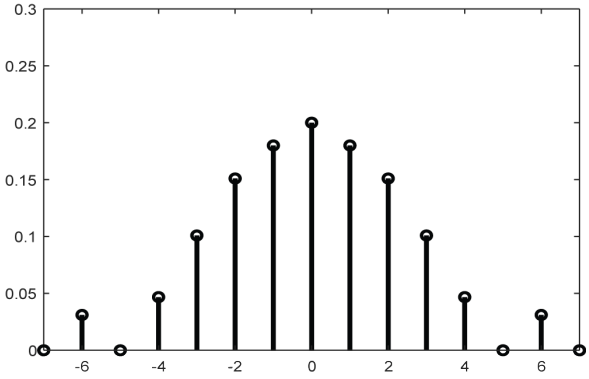
(b) Random sequence β of length 5



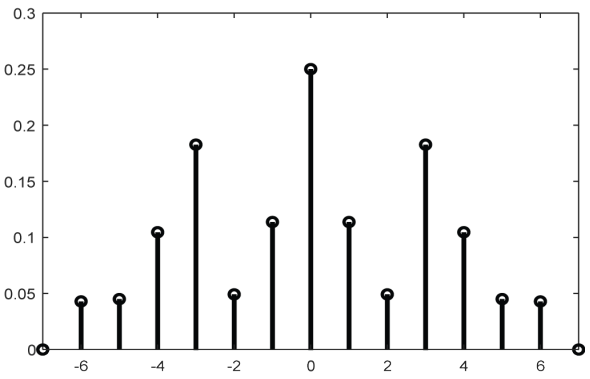
(c) Direct multiplication of α and β with no offset



(d) Direct multiplication of α and β with $1/4T_c$ offset



(e) Magnitude of the D_n spectrum with no offset



(f) Magnitude of the D_n spectrum with $1/4T_c$ offset

Figure 8.8: Comparison of multiplication of two different random sequences with no fractional offset and a fractional offset

$$
\begin{aligned}
|D_n| = (\sqrt{(} &- 2((cos(((3n\pi)/(2))) + cos(((9n\pi)/(10))) - cos(((4n\pi)/(5))) \\
&+ cos(((2n\pi)/(5))) - cos(((n\pi)/(10))))cos(((8n\pi)/(5))) + (sin(((3n\pi)/(2))) \\
&+ sin(((9n\pi)/(10))) - sin(((4n\pi)/(5))) + sin(((2n\pi)/(5))) \\
&- sin(((n\pi)/(10))))sin(((8n\pi)/(5))) - (cos(((9n\pi)/(10))) \\
&- cos(((4n\pi)/(5))) + cos(((2n\pi)/(5))) - cos(((n\pi)/(10))))cos(((3n\pi)/(2))) \\
&- (sin(((9n\pi)/(10))) - sin(((4n\pi)/(5))) + sin(((2n\pi)/(5))) \\
&- sin(((n\pi)/(10))))sin(((3n\pi)/(2))) + (cos(((4n\pi)/(5))) - cos(((2n\pi)/(5))) \\
&+ cos(((n\pi)/(10))))cos(((9n\pi)/(10))) + (sin(((4n\pi)/(5))) \\
&- sin(((2n\pi)/(5))) + sin(((n\pi)/(10))))sin(((9n\pi)/(10))) \\
&+ (cos(((2n\pi)/(5))) - cos(((n\pi)/(10))))cos(((4n\pi)/(5))) \\
&+ (sin(((2n\pi)/(5))) - sin(((n\pi)/(10))))sin(((4n\pi)/(5))) \\
&+ cos(((n\pi)/(10)))cos(((2n\pi)/(5))) + sin(((n\pi)/(10)))sin(((2n\pi)/(5))) - 3)) \\
&/(2abs(n)\pi))
\end{aligned}
\tag{8.21}
$$

For each of the results we can look at the Fourier series coefficients in order to understand what happens to the spectrum of each. The coefficients for this example are shown in Table 8.1, and the spectrum for the magnitude is shown in Figures 8.8e and 8.8f. Clearly, we can see that the waveform with the offset has more power as the offset generates a higher correlation. An interesting observation can be made by comparing the spectrum of the two resulting signals shown in Figures 8.8e and 8.8f. The shape of the spectrum is very different and although the fundamental component is slightly higher for the offset spectrum, overall the sum of the magnitude squared of the first three components for the offset will be smaller in comparison. If an ideal filter is placed to only pass through the first few harmonics, significant energy reduction can be achieved for codes that have partial offset. We call this spectrum shaping because by intentionally applying a timing offset we reshape the spectrum in order to yield less low frequency content and more high frequency.

Table 8.1: Comparison of Coefficients

Coefficient of Fourier series		
n_{th} Coefficient	No Offset	$1/4T_c$ Offset
Fundamental	.20	0.25
2nd Harmonic	.18	0.1137
3rd Harmonic	.151	.0492
4th Harmonic	.1009	.1827
5th Harmonic	.04677	.10459
6th Harmonic	0	.045
7th Harmonic	.0311	.04292

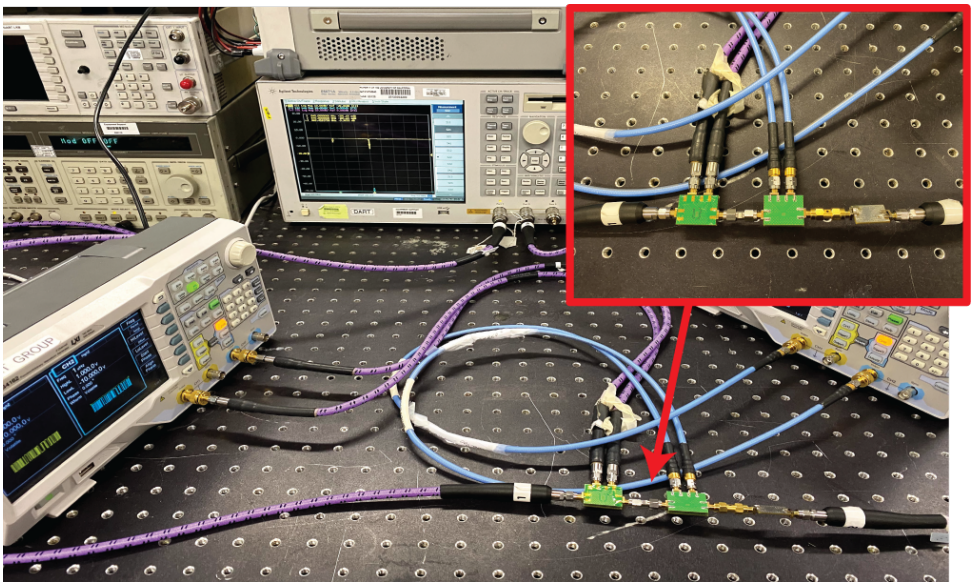


Figure 8.9: Bench top setup for SIC using correlator only

8.6 Experimental Results

8.6.1 Code domain cancellation only

To validate the code domain self interference cancellation, a test bench was constructed using two correlators and a SAW filter that were demonstrate in previous section. The two correlators were connected in a series with the SAW filter. The center frequency of the SAW filter is at 869MHz with a pass band bandwidth of 200kHz. Each of the correlators

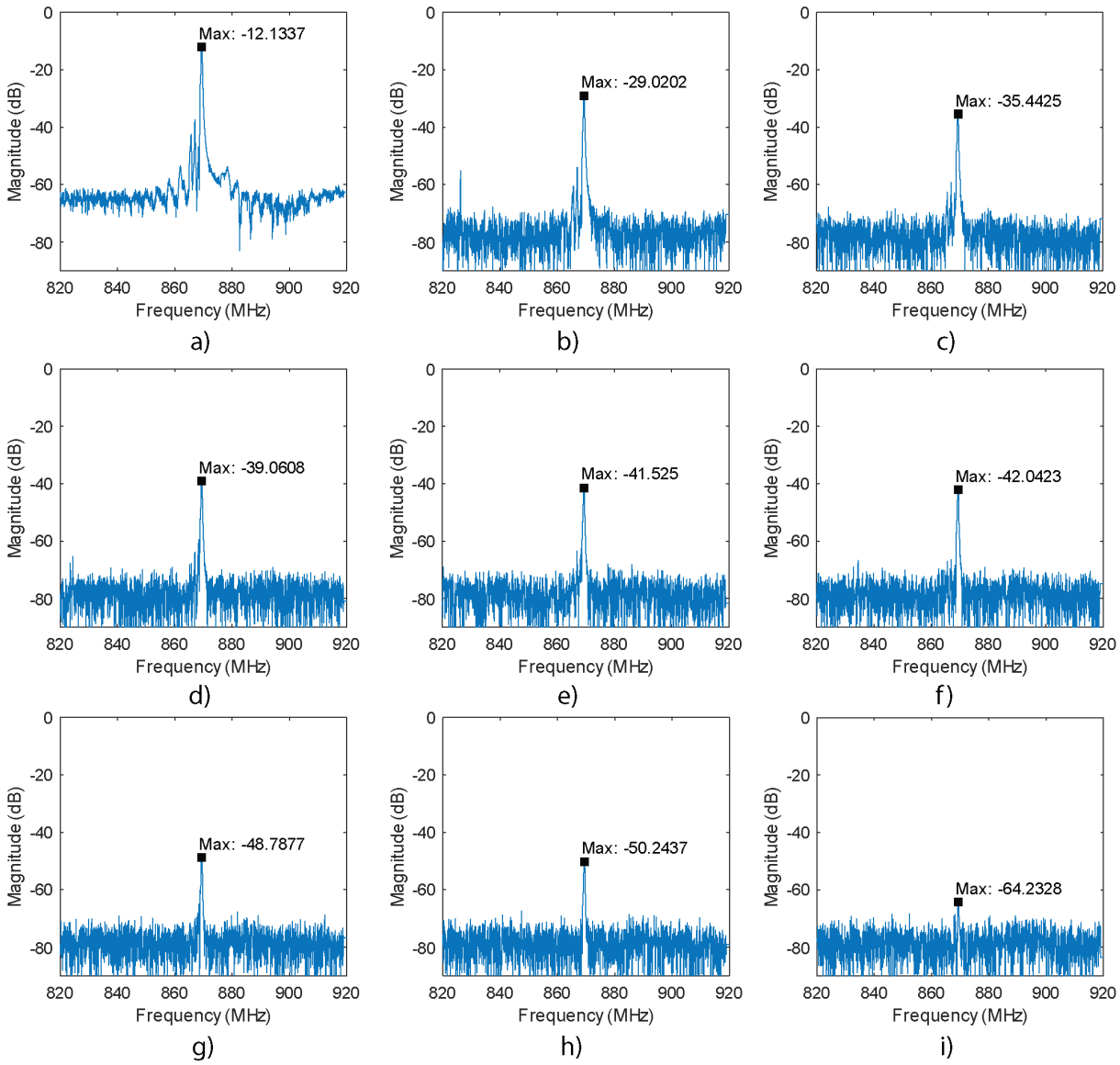


Figure 8.10: Results for the different offset between the two codes.

was driven be a Rigol 4102 arbitrary function generator. Each Rigol was programmed to output a 127bit m-sequence and have a chip time of $127 * 200kHz = 25.4MHz$. The two port S-Parameters were measured using Agilent E5071A network analyzer. The setup of this measurement is shown in Figure 8.9.

The measured results are show in Figure 8.10 and are also presented in Table 8.2 where the maximal insertion loss peak is tabulated. The baseline for the measurement of the correlators and the SAW filter is shown in Figure 8.10 a). This insertion loss of $-12dB$ is

Table 8.2: Insertion Loss of Different offsets between codes

Offset	Insertion Loss (dB)
Baseline	-12.12
1st Offset	-29.02
2nd Offset	-35.45
3rd Offset	-39.06
4th Offset	-41.52
5th Offset	-42.04
6th Offset	-48.78
7th Offset	-50.24
8th Offset	-64.23

coming from the static losses of the SAW filter and the correlator PCBs. Since the code length is 127bit the and the codes between TX and RX are quasi-orthogonal the expected minimal isolation is $10\log(127) = 21dB$, plus the static loss when the codes are perfectly aligned. The measurement was done by putting a random offset between the two codes. Eight different offset results are shown in 8.10 and Table 8.2. These measurement show a variety of possible isolation ranging from -29dB and going all the way down to -64dB.

8.6.2 Offset for Maximum Cancellation

The measured results reported in the previous section might not give the maximum cancellation that can be achieved between the two codes that were used. The goal of the experiment was to demonstrate that for a system that uses RF correlations systems (reported in Section 2.1) to suppress incoming jammers, the orthogonality between the TX and RX codes can be exploited to achieve self interference cancellation. With a carefully selected offset of τ between the two codes, a much larger cancellation can be achieved than what the original code was designed for. However, there is no straight way that τ can be calculated. Since the spreading sequences are random, different offsets of τ will also generate different results between two orthogonal codes even from the family. The only

way that the τ' offset that achieves maximum cancellation can be found is by performing an exhaustive search. This is a brute force method of finding the τ' offset, but once it is found, it will not change for that code pair. This τ' can be pre-computed in advance and looked up when a particular code pair is selected for use.

8.7 SIC circuit plus code domain cancellation

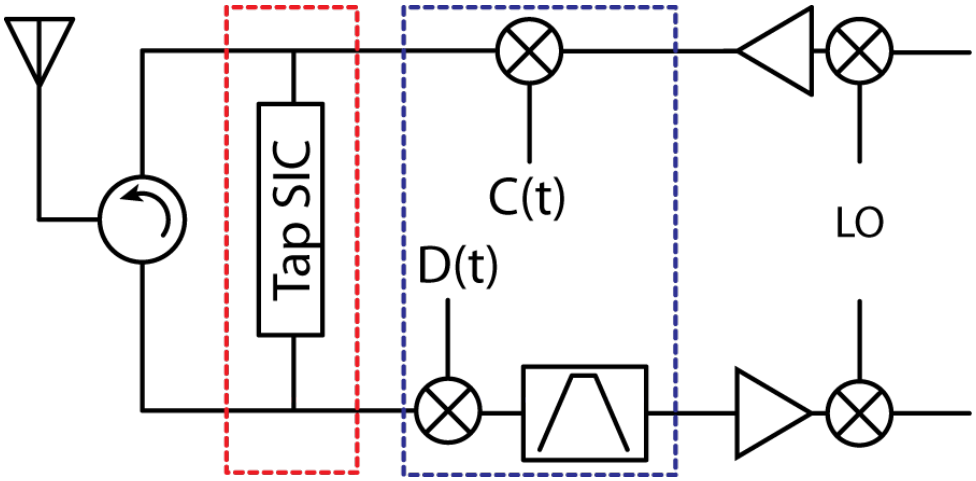


Figure 8.11: Block diagram of using both Tap-delay method cancellation and code domain cancellation

The two methods that were presented in the previous section can work independent of each other. Greater cancellation can be achieved if when they are used together. Block diagram of how the two methods can be integrated is shown in Figure 8.11. The experiment was done using two correlators used and the four tap self interference cancellation circuitry. The first correlator was added right after the TX signals and the second correlator was added right before the RX signal output. Two port small signal measurement was done using an Agilent E5071A network analyzer, with a calibration done up to the cable ends. Port one was connected to TX and port two was connected to the RX. Four Rigol DL300 dc power supplies were used to power the attenuators and the phase shifters. Each of the correlators was driven by a Rigol 4102 arbitrary function generator each being programmed with its own 127 bit spreading sequence. A 36dB attenuator was connected on the output to emulate the initial isolation that two antennas or a circulator might provide. The result for the measurements are shown in Figure 8.13.

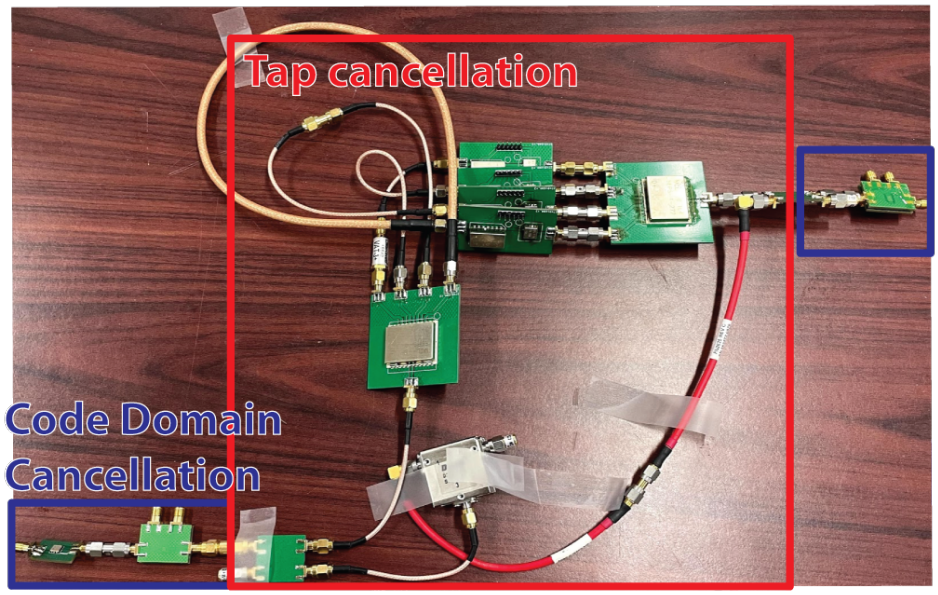


Figure 8.12: Bench top setup for SIC circuitry including code main cancelling circuitry

The measured results show that additional cancellation of 30dB can be achieved when a correlator is used. Granted the additional 30dB shown in Figure 8.13 also includes the static insertion loss of the added correlators which is around 5dB. Also, when different offsets are used the resulting spectrum changes from more flat cancellation as shown with an 200^o offset, to one that has many deep nulls like the 100^o offset. If a narrowband filter like the one used in previous section was attached right after the RX correlator the offset with the deep nulls would definitely provide much larger isolation. This clearly shows that for particular cases very large isolation can be achieved.

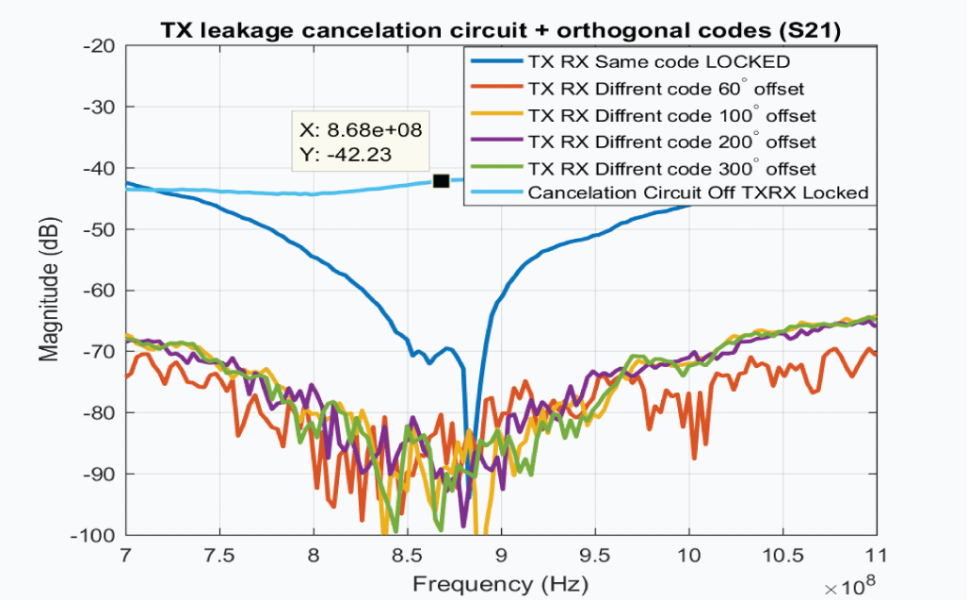


Figure 8.13: Measured results of modular four tap self interference circuit with the addition of analog correlator function

Chapter 9

Conclusion

The communication space how grown tremendously in the last few decades [59] [60]. This growth has been fueled by development of cellular technologies such as 4G LTE/5G, and machine to machine communication in internet of things (IoT) space. [61] [62]. This exponential growth has created challenges in sharing of the limited RF spectrum. Many users experience interference coming from unintentional or nefarious sources. This interference disrupt vital communication links. Much efforts has been dedicated to different interference mitigation strategies.

In this work three different approaches were presented in dealing with in-band and out of band types of interference.

9.1 Analog Spread Spectrum

In this section a novel direct sequence spread spectrum signal processing approach in analog domain was presented. This approach provides a mitigation strategy for interference signals that fall in the band of operation. A in-depth analysis of the analog direct sequence spread spectrum signal processing approach was also demonstrated. The system is based in GaN time domain correlators that spread (TX) and de-spread (RX) the signal. GaN devices enable the circuitry to have high P1dB compression point that is over 38dBm and IIP3 that is over 48dBm. The RX correlator spreads incoming interference, so the system is able to perform correctly even if blockers power is high. The demonstrated module is shown to suppress narrow in-band interference up to $27dB$ for a 200kHz signal bandwidth.

To achieve this suppression a Gold spreading sequence of 1027 bit was used. Additionally, the system includes a non-coherent timing recovery scheme, so no information from the baseband receiver is needed to synchronize the correlators. The algorithm has the ability to dynamically set the energy threshold lever when initially started. There are a few ideas that the author has for future research in this area. The signal bandwidth that was used for demonstration was only around 200kHz. To be a more compelling architecture, signal bandwidth will need to be increased. If the processing gain is to remain above 20dB then switching speed will need to be much faster while still maintaining high power handling. One idea is to use a resonant structure at the gate instead of a resistor. From the clocks perspective the resonant structure will be low impedance to archive fast switching, while from the perspective of the RF inputs it will be high impedance to maintain high power handling. Another area of possible improvement is the use of N-path filter to do the correlation function in analog domain on the receive side. There has been a few works that have demonstrated the use of phase encoding on N-Path clock to achieve spreading and de-spreading of signals [4] [5]. The GaN correlator PCB with the off chip clock generation has was demonstrated in this work. The next step is to include the phase encoding of the clock to achieve spreading and de-spreading. The simplest way that this could be done is by changing where the clock is tapped off in the ring oscillator shown in 7.13 by including some additional switches in the design.

9.2 GaN N-Path Filter

Interference that fall outside the band of interest is typically taken care of by filters. This can be done in digital and analog domain. Conventional filter have fixed center frequency and bandwidth which can't be tuned. In this work a tunable, high power N=4 N-Path filter is demonstrated. Majority of published works utilize a standard CMOS process for implantation which has power handling limitation. The N-Path filter in this work takes a heterogeneous approach to architecture design. The N-path core was designed in a GaN process, which allows for high power handling. The four phase not overlapping clock is generated in a CMOS process. An intermediate GaN Level shifter to driver the

GaN switched in N-Path core was also shown. The work also demonstrated the PCB integration methodology of the heterogeneous filter. The measurement show that the filter can be tuned from 1-1.3GHz in center frequency. Also it was demonstrated that the 3dB bandwidth is tunable from 5MHz to 20MHz. Simulation show that this heterogeneous architecture has a 1dB compression point of 18.8dBm

One of the potential improvement to this type of heterogeneous N-Path filter design is to have a much tighter integration by the use of an interposer. Due to cost constraints this method was not explored, but much better signal integrity will be achieved if the clock lines are smaller which is possible with interposer.

9.3 Self Interference cancellation

A full duplex system that can transmit and receive in the same frequency and time space has been of great interest since the advent of wireless communication. However, the full duplex architecture adoption is limited due to the self interference problem. This is where a transmitter is a strong in-band jammer to it's own receiver. In this work two independent methods for dealing with self interference were demonstrated. The first method uses tap-delay method to tap off power from the TX side, invert the signal with some added delay and inject it right before the LNA on the RX. This method was designed to have four taps. Each tap has individual amplitude and phase control. The system is modular in order to study the cancellation effects at critical points. Measured results show that an additional 20dB of isolation can be achieved over a 63MHz bandwidth, and over 30dB over 30MHz bandwidth using controlled loads. The challenge of doing this type of self interference cancellation is that there are many different paths that a leaked signal can take before it reaches the receiver. Each path will have a different delay and amplitude. To get good cancellation all these path will need to be account for. This sets a requirement of having many taps, which is not possible in a real system. This approach is also narrow band due to the fact that frequency delay spread is very hard to match. Each tap that does not have the correct delay and amplitude match starts to contribute to the leaked signal as it is a auxiliary path from TX to RX. The author sees this approach viable to very narrow

band application, but adoption for wideband systems will be challenging.

The second method show was the use orthogonal coding in time domain to achieve deep self interference cancelling. Clever selection of timing offset between the TX and RX code. This type of cancellation only applies to systems that use Analog correlators which were shown in the first part of this work. By doing partial timing offset the spreading energy is not uniformly distributed in the spreading bandwidth. There are some specific timing offsets that will yield a nulling effect in the filters pass-band. This will remove more transmitters energy than what the code originally was designed for. In future work this idea will be explored further to see if there are certain code families that give better nulling effects. Also, since the spreading sequence in the TX and RX are using the same clock we can use this to find a good nulling offset, and then move the TX and RX codes in tandem to recover the correct timing offset. In this work we have demonstrate that over 50dB of cancellation can be achieved by the use of this method.

This demonstration only focused on a few 127 bit Gold codes, but there could be code pairs that have wider rejection and deeper cancellation. Future work in this area could include exploring of longer codes, and different families of codes to see if better spectrum shaping can occur.

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