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High-Efficiency Sub-THz Transmitters

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Jeff Shih-Chieh Chien

Committee in charge:

Professor James Buckwalter, Chair
Professor Mark Rodwell
Professor Loai Salem
Professor Bongjin Kim

March 2023

The Dissertation of Jeff Shih-Chieh Chien is approved.

Professor Mark Rodwell

Professor Loai Salem

Professor Bongjin Kim

Professor James Buckwalter, Committee Chair

December 2022

High-Efficiency Sub-THz Transmitters

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by

Jeff Shih-Chieh Chien

To my family.

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Curriculum Vitæ

Jeff Shih-Chieh Chien

Education

- 2022 Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara.
- 2015 M.S. in Electrical Engineering, National Tsing-Hua University.
- 2014 B.S. in Electrical Engineering and Computer Science, National Tsing-Hua University.

Publications

1. **J. S. -C. Chien** and J. F. Buckwalter, "A 120-GHz, 1.58-mm² Multiplying Outphasing Transmitter in 22nm FDSOI," 2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2022, pp. 16-19.
2. **J. S. -C. Chien** and J. F. Buckwalter, "A Compact, 114-GHz, High-efficiency Power Amplifier in a 250-nm InP HBT Process," 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022, 2022, pp. 452-455.
3. **J. S. -C. Chien** and J. F. Buckwalter, "Compact, High-Isolation 110-140-GHz SPST and SPDT Switches Using a 250-nm InP HBT Process," 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022, 2022, pp. 152-155.
4. **J. S. -C. Chien** and J. F. Buckwalter, "A 111-149-GHz, Compact Power-combined Amplifier With 17.5-dBm P_{sat} , 16.5% PAE in 22-nm CMOS FD-SOI," ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC), 2022, pp. 453-456.
5. **J. S. -C. Chien** and J. F. Buckwalter, "A D-band, High Switching Speed, Differential Reflection-Type Phase Shifter in 250-nm InP HBT," 2022 17th European Microwave Integrated Circuits Conference (EuMIC), 2022, pp. 115-118.
6. **J. S. -C. Chien**, W. Lee and J. F. Buckwalter, "A 180-220-GHz, 12.7-dBm peak P_{sat} and 17.3% peak PAE Power Amplifier in 250-nm InP HBT," 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2022.
7. **J. S. -C. Chien** and J. F. Buckwalter, "A 110-120-GHz, 12.2% Efficiency, 16.2-dBm Output Power Multiplying Outphasing Transmitter in 22-nm FDSOI," 2022 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2022.
8. **J. S. -C. Chien** and J. F. Buckwalter, "Low Insertion Loss, Reflective-Load Switches Operating in D -Band and G -Band," in IEEE Transactions on Microwave Theory and Techniques, 2022.
9. **J. S. -C. Chien**, W. Lee and J. F. Buckwalter, "High-Efficiency 200-GHz Neutralized Common-Base Power Amplifiers in 250-nm InP HBT," submitted to IEEE Journal of Microwaves.
10. J. F. Buckwalter, **Jeff Chien**, et al., "Prospects for High-Efficiency Silicon and III-V Power Amplifiers and Transmitters in 100-300 GHz Bands," 2021 IEEE Custom Integrated Circuits Conference (CICC), 2021, pp. 1-7.

Abstract

High-Efficiency Sub-THz Transmitters

by

Jeff Shih-Chieh Chien

D-band (110-170 GHz) and G-band (140-220 GHz) phased array transceivers have gained more attention for automotive radar and beyond-5G communication systems in recent years due to the high resolution for imaging and wide available bandwidth for high data rate applications. The limited f_T/f_{max} of CMOS technologies, even with scaled devices places a significant circuit design challenge, for power amplifiers (PAs) and, moreover, transmitters since low efficiency is found not only in the PA but also high loss in mixers and multipliers in local oscillator (LO) path.

This dissertation describes the design methodology of high efficiency Sub-THz transmitter and building blocks in 22-nm FDSOI CMOS and InP HBT process. D-band Multi-way power combined PA in 22-nm FDSOI CMOS is discussed in Chapter 3. High efficiency D-band and G-band PA designs in InP HBT is described in Chapter 4. Chapter 5 describes D-band and G-band switches design in InP HBT. D-band high efficiency outphasing transmitter in 22-nm FDSOI CMOS is discussed in Chapter 6.

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Chapter 1

Introduction

With the continuous research and development of millimeter-wave (mm-wave) circuits and systems over more than 20 years, mm-wave products enter consumer electronics market in the past few years especially 5G applications. Fig. 1.1 shows an example of mm-wave phased-array module deployment in a iPhone which includes 5G modem, mm-wave IF chip and mm-wave RF beamformer chips as well as power management unit and antennas. Operating at 28/38-GHz frequency range, the targeted down link data rate for 5G mm-wave is over 10Gbps. To achieve even higher data rate, wider bandwidth and higher operating frequency are explored in recent years.

1.1 Shannon–Hartley Theorem

Shannon-Hartley theorem is a theorem describing the upper limit of data rate for channel with Gaussian noise and is written as

$$C = BW \times \log_2(1 + SNR) \approx BW \times \frac{SNR(dB)}{3} \quad (1.1)$$

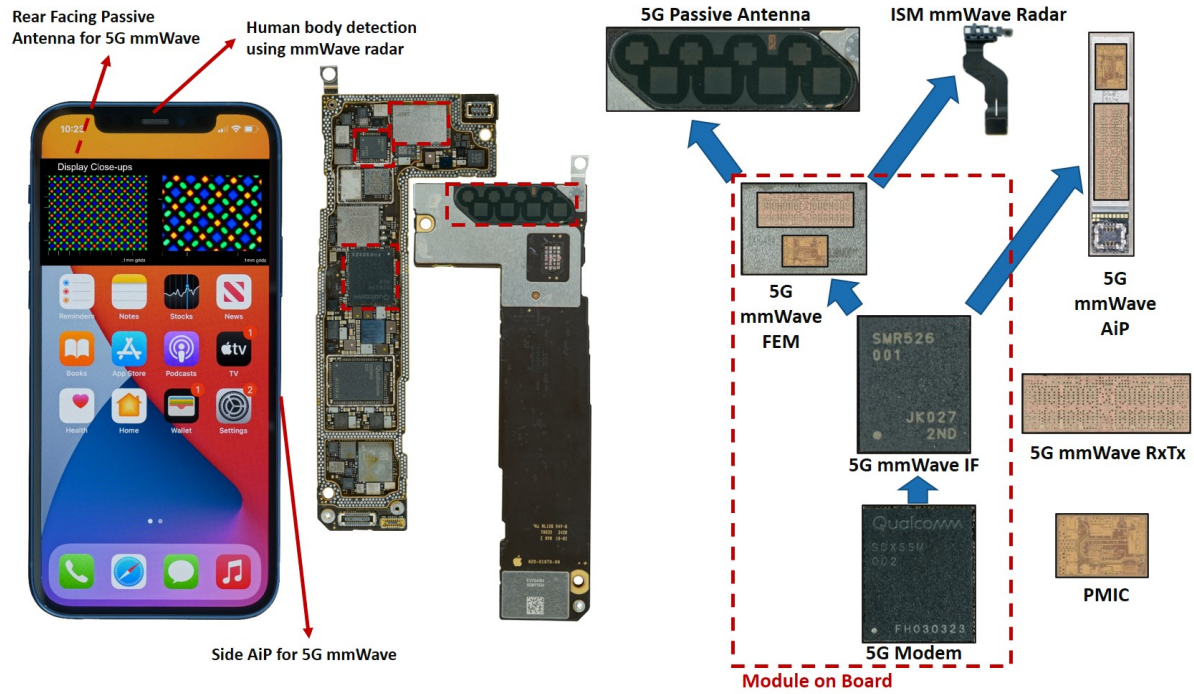


Figure 1.1: mm-wave phased array antenna module in iPhone 12.

(Source: <https://www.reverse-costing.com/teardown-notes/elaboration-iphone-12-5g-antennas/>)

where C is the channel capacity, BW is the channel bandwidth while SNR is the signal to noise ratio within the channel bandwidth. From equation 1.1, using more complex modulation scheme with high SNR or increasing bandwidth could provide higher channel capacity or higher data rate. Under limited bandwidth scenario such as 5G sub-6GHz or WiFi application, complex modulation scheme is preferred to improve data rate. However, high SNR imposes transmitter to operate in more linear region and therefore circuits are operated less efficiently. Also, data rate enhancement due to SNR improvement is less efficient compared to bandwidth improvement as observed in 1.1. Therefore, by moving the operating frequency toward mm-wave frequency with larger available bandwidth is a straight forward methodology for future communication system with higher data rate.

1.2 Phased-Array Systems

Friis transmission equation is used to calculate the free space path loss [1]:

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{C}{4\pi df} \right)^2 \quad (1.2)$$

where P_r is the received power at the receiver antenna, P_t is the transmitted power through the transmitter antenna, G_t is the transmitter antenna gain in the direction of receiver antenna and G_r is the receiver antenna gain in the direction of transmitter antenna. C is the speed of light, d is the distance between transmit and receive antenna while f is the operating frequency. From the equation, free space path loss is inverse proportional to f^2 . However, if antenna aperture $A_{eff} = C^2/4\pi f^2$ is considered, 1.2 becomes

$$\frac{P_r}{P_t} = G_t G_r A_{eff} \frac{1}{4\pi d^2} \quad (1.3)$$

The equation indicates the path loss is independent of frequency if same antenna aperture is considered. For instance, if there is an RX antenna designed at 28 GHz and we simply transform one big antenna to 140 GHz 5x5 antenna phased array occupying same area, we should obtain the same path loss in both cases. Furthermore, if we design both TX and RX into phased array at 140 GHz, the path loss will reduce 25 times compared to single TX and RX antennas at 28 GHz. Therefore it is beneficial to use phased array at mm-wave bands.

Phased array antenna spacing is usually designed with $\lambda/2$ [2] since smaller or larger spacing will impact beam width on the main-lobe as well as introducing grating lobes. As mentioned in [2] and [3], the chip size is hard to fit into the antenna spacing constraint moving from lower mm-wave toward higher mm-wave bands. More details will be discussed in the next section.

1.3 Challenges of Sub-THz Circuits Design

There are several challenges on RF amplifier implementation at upper mm-wave bands including area, gain, linearity, noise and efficiency. These challenges are originated from the limited f_T/f_{max} of available technologies. In a typical bulk/SOI CMOS process nowadays, f_{max} are around 300 GHz while SiGe BiCMOS could reach 500 GHz. InP so far holds the highest f_{max} numbers that could be over 1 THz [4]. In this dissertation, 22-nm FDSOI CMOS and 250-nm InP HBT process with f_{max} of 370 GHz and 700 GHz are used. The f_{max} number indicates our operating frequency is higher than $f_{max}/10$ and therefore maximum power gain below 20-dB for both technology could be expected. Low single stage power gain imposes design difficulty for power amplifier (PA) and low noise amplifier (LNA) designs. For PA design, the low gain single stage amplifier will cause huge efficiency drop comparing power-added efficiency (PAE) to drain efficiency (DE) as well as efficiency degradation due to power consumption from driver stages. Besides, PAs are most likely to be biased at class-A for sufficient gain at Sub-THz bands, maximum PAE point is normally located at several dB compression point. This makes the linear amplifier hard to operate at high efficiency region and higher output power PA is needed for large back-off to meet the EVM requirement. Similar to PA performance degradation, noise from latter stages will add more noise contribution toward the overall noise performance under low single stage gain.

One thing that we benefit from moving toward higher frequency is the reduced size of passive structures such as inductors, transformers and transmission lines. However, due to the reduced single stage gain, more gain stages are required to maintain the same amount of transmitter or receiver gain as lower mm-wave bands design. With antenna spacing scaling with frequency as shown in Table 1.1, the published works above around 70 GHz start to fail fitting in antenna spacing as revealed in paper [2] and [3].

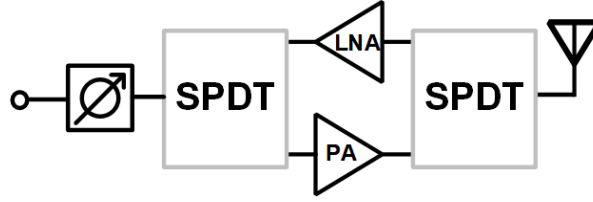


Figure 1.2: A single element in a RF beamformer.

The heat dissipation is another issue related to the shrinkage of antenna spacing. If single element transmitter with 17dBm output power and 20% efficiency is used to calculate DC power density, the scaling of DC power density is shown in Table 1.1. The results also indicate high efficiency is required to keep DC power density in a reasonable range.

Frequency (GHz)	Antenna Spacing (mm ²)	Power Density (W/cm ²)
28	5.36	0.87
38	3.95	1.6
60	2.5	4
120	1.25	16
220	0.68	54.1

Table 1.1: Antenna spacing and DC power density under different frequency.

Besides amplifier designs, transmit/receive module in a RF beamforming phased array system requires switches and phase shifters as shown in Fig. 1.2. Due to limited $R_{on}C_{off}$ performance of the available technologies, switches and phase shifters are lossy at sub-THz. This implies more gain stages are required for preventing the degradation of NF in receiver and efficiency in transmitter.

1.4 Thesis Objectives and Organization

In this thesis, exploration of sub-THz high efficient and compact power amplifier, low loss switches as well as high efficient D-band outphasing transmitter will be covered.

Chapter 2

mm-wave Transmitter System and Circuit Basics

2.1 mm-Wave Transmitter basics

Transmitter serves as a front-end system that transmits the signal toward antenna. In [5], the author summarized several topologies including direct-conversion transmitter as shown in Fig. 2.1 with modified LO path which normally including multipliers in sub-THz transmitters [6],[7]. IF I and Q signals are up-converted by two mixers with I and Q LO driving the LO ports. In this topology, LO is normally set the same frequency as RF while IF is centered at DC. The topology is widely used in cellular and connectivity RF systems but normally have to trade efficiency with linearity while the higher order modulation base-band signal is used.

The second transmitter topology is polar transmitter as shown in Fig. 2.2. Decomposing a point on constellation into magnitude and phase, mixer in direct conversion transmitter could be eliminated. Since only phase information is remained in the main RF path, all the circuit blocks could be operated in the nonlinear region with better

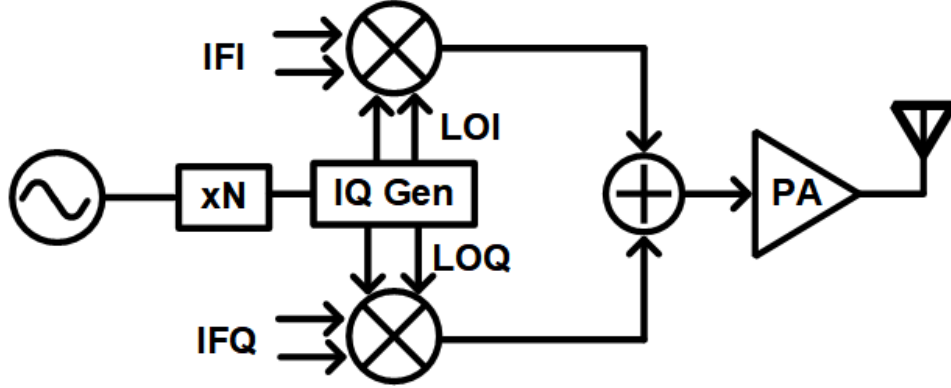


Figure 2.1: Direct-conversion Transmitter.

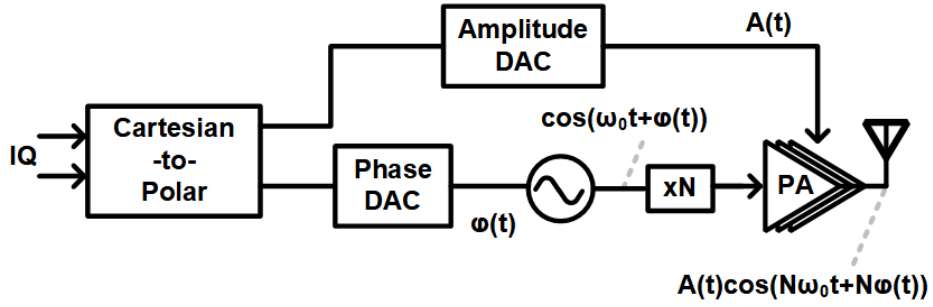


Figure 2.2: Polar Transmitter.

efficiency. However, the alignment between AM and PM paths is usually an issue and the base-band bandwidth is widened due to Cartesian to polar transmission.

The third transmitter topology is outphasing transmitter as shown in Fig. 2.3 [8]. Points on constellation are decomposed into two vectors with same magnitude and different phases. Similar to polar transmitter, all the circuit blocks could be operated in nonlinear region for better efficiency. Also, if Chireix power combiner is applied, back-off efficiency could also be improved compared to direct-conversion transmitter.

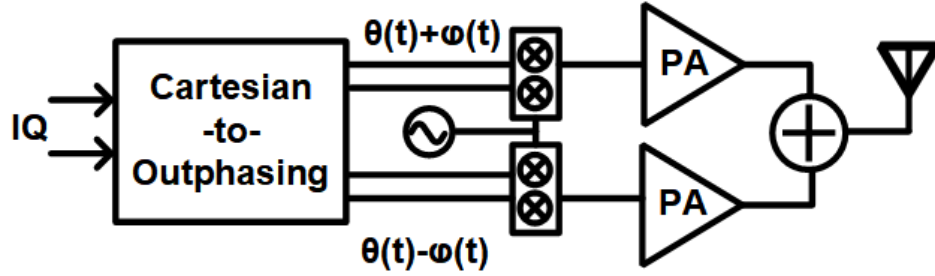


Figure 2.3: Outphasing Transmitter.

2.2 PA basics

The purpose of a PA is to amplify the up-converted signal to a desired signal level. Overall transmitter efficiency is also dominated by PA in high power transmitter. Several important indexes of PA are efficiency, output power and linearity. Among these indexes, power efficiency is one of the most important metrics of PA. It is an indication of how well a PA converts the given supplied power to the output power. If power efficiency is low, most of DC power is translated to heat and therefore the chip temperature will increase and cause the degradation of device performance or reduced transistors life time. Therefore, high efficiency PA not only improves the system performance but also its own reliability. There are three power efficiency definitions, drain efficiency $\eta_D = P_{out}/P_{DC}$, power added efficiency $\eta_{PAE} = (P_{out} - P_{in})/P_{DC}$, and total efficiency $\eta_{total} = P_{out}/(P_{DC} + P_{in})$. The relationship between drain efficiency and PAE is

$$\eta_{PAE} = \eta_D \left(1 - \frac{1}{G}\right) \quad (2.1)$$

where G is power gain of PA. The relationship between drain efficiency and total efficiency is

$$\eta_{total} = \frac{\eta_D}{\left(1 + \eta_D \frac{1}{G}\right)} \quad (2.2)$$

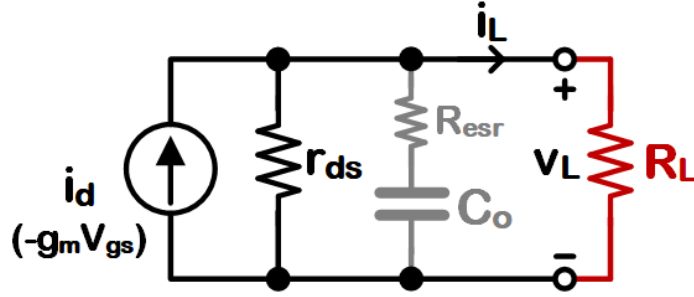


Figure 2.4: PA output modeled as ideal current source with parasitics.

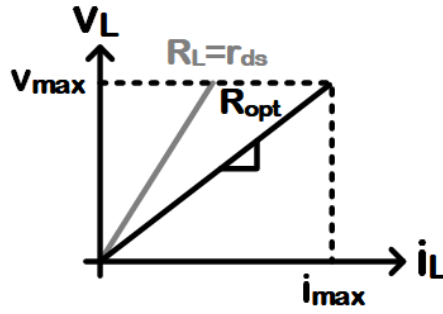


Figure 2.5: Load-line match.

It is more common to use PAE as an index for PA design while total efficiency is more common to be used in multiplier design.

Conjugate matching is usually used to achieve the maximum power transfer from microwave theory. However, it may not be the best impedance for output matching network in PA design. As shown in Fig. 2.4, the transistor output is modeled as a current source i_d , output resistance r_{ds} and output parasitic capacitance C_o . First of all, We ignore C_o and a better output power with R_{opt} than the conjugate matching r_{ds} in Fig. 2.5 is observed. The reason that conjugate matching is not the best for the output power is because this matching condition is based on the small-signal assumption without considering the voltage or current swing constraints of the transistor. If parasitic capacitance from the transistor C_o and its equivalent series resistor R_{esr} are put into

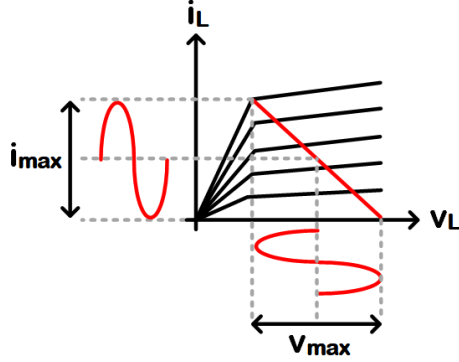


Figure 2.6: Load-line with resistive load only.

consideration, the power delivered from the current source is written as

$$P_{del} = \frac{1}{2} i_d^2 \frac{R_L r_{ds} (1 + j\omega R_{esr} C_o)}{R_L + r_{ds} + j\omega C_o [R_L r_{ds} + (R_L + r_{ds}) R_{esr}]} \quad (2.3)$$

Therefore, one pole and one zero could be obtained from 2.3 and written as

$$\omega_P = \frac{1}{(R_L // r_{ds} + R_{esr}) C_o}, \omega_Z = \frac{1}{R_{esr} C_o} \quad (2.4)$$

This indicates the power delivered from the current source drops with higher operating frequency. It's also worth mentioning when the large transistor is used at high frequency bands, the metal routing of devices normally adds on to higher R_{esr} and therefore the pole frequency is reduced. This relationship provides some insights on the reason why single power cell are normally with low power level and power combining or stacked technique are usually required for higher output power.

The load-line with voltage and current swing of pure resistive load is shown in Fig. 2.6. If output parasitic capacitance C_o is considered, load impedance drops while operating at high frequency as shown in Fig. 2.7. As a result, the impedance can no longer operate at V_{max} with reduced output power. To solve the problem, Shunt inductance is

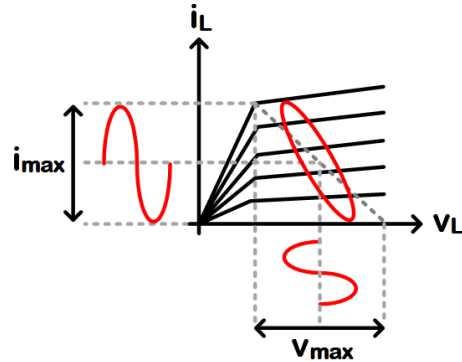


Figure 2.7: Load-line with resistive and capacitive load.

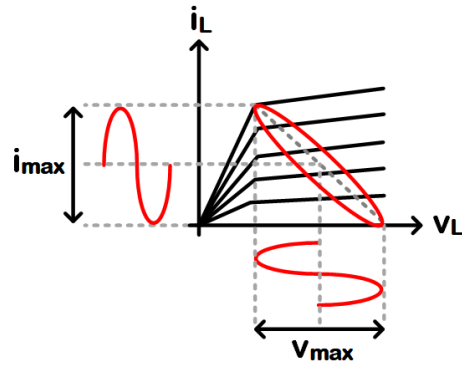


Figure 2.8: Load-line with resistive, capacitive and inductive tuning load.

normally added to resonate out the parasitic capacitance so that the load line can still at the optimal condition as shown in Fig. 2.8.

There are several classes of PA as discuss in [9]. Based on the conduction angles, continuous-mode PA are classified into Class-A, AB, B and C without harmonic termination. Class-J, Class-F and inverse Class-F are based on class-AB with different second or third harmonic impedance termination. Besides, switch-mode PA such as class-D and class-E are widely researched in lower GHz frequency range but less attractive for upper mm-wave band due to limited switching speed of available technologies. Considering the continuous-mode PA without harmonic engineering, the DC power and fundamental

power of PA [9] is written as

$$P_{dc} = V_{dc} \cdot \frac{I_{max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)} \quad (2.5)$$

$$P_{fund} = \frac{V_{dc}}{2} \cdot \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)} \quad (2.6)$$

where α is the conduction angle between 0 and 2π . Drain efficiency could be derived as

$$\eta_D = \frac{1}{2} \cdot \frac{\alpha - \sin(\alpha)}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}. \quad (2.7)$$

Combining equation 2.1 and 2.7 with considering knee voltage V_{knee} , PAE is re-written as

$$\eta_{PAE} = \frac{1}{2} \cdot \frac{\alpha - \sin(\alpha)}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \cdot \left(1 - \frac{1}{G}\right) \cdot \left(1 - \frac{V_{knee}}{V_{dc}}\right) \quad (2.8)$$

As discussed in [10], power gain is relevant to conduction angle and if PA is operating at MAG region, power gain is expressed as

$$G = \left(\frac{f_{max}}{f_0}\right)^2 \cdot \frac{(1 - \cos(\alpha/2))^2}{4} \quad (2.9)$$

and input and output matching loss are approximated as

$$L_{IMN} = \frac{\sqrt{(kQ)^2 + 1} - 1}{\sqrt{(kQ)^2 + 1} + 1}, L_{OMN} = \frac{Q_o}{Q_o + Q_t} \cdot \frac{1}{1 + \frac{|XC_o|}{R_L Q_o}} \quad (2.10)$$

where Q_o is quality factor of passive components while Q_t is impedance transformation quality factor. Combining equation 2.8, 2.9 and 2.10, PAE is re-written as

$$\eta_{PAE} = \frac{1}{2} \cdot \frac{\alpha - \sin(\alpha)}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \cdot \left(1 - \left(\frac{f_0}{f_{max}}\right)^2 \cdot \frac{4}{L_{IMN}(1 - \cos(\alpha/2))^2}\right) \cdot \left(1 - \frac{V_{knee}}{V_{dc}}\right) \cdot L_{OMN}. \quad (2.11)$$

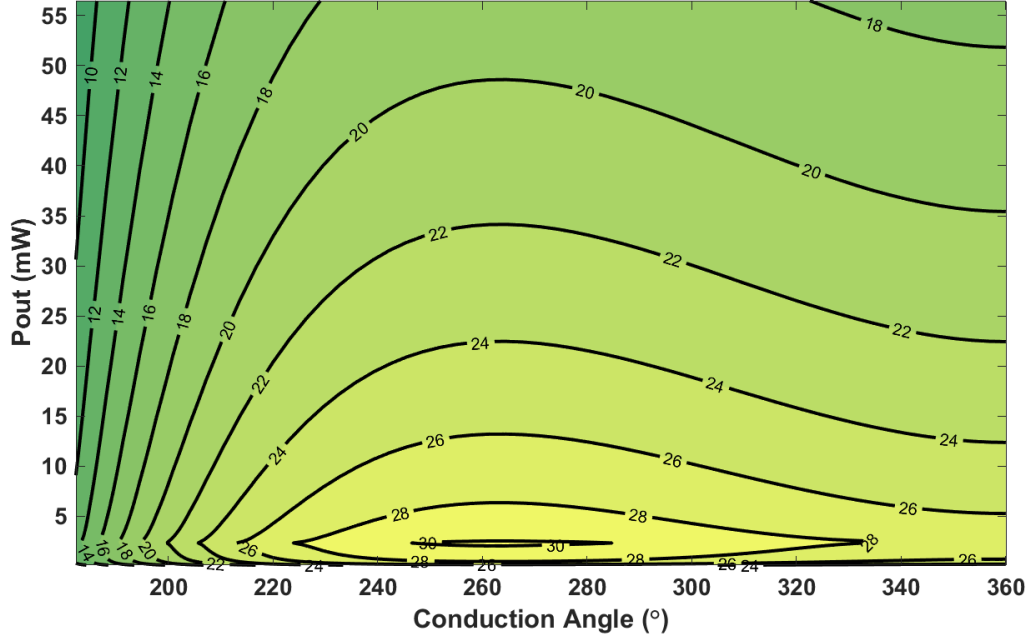


Figure 2.9: Calculated PAE contour with output power and conduction angles in 22-nm FDSOI CMOS at $f_0=140$ GHz.

Using parameters from Globalfoundries 22-nm FDSOI CMOS process with 350-GHz f_{max} and passive Q of 20, contours of PAE with sweep of conduction angles and output power at 140-GHz are plotted in Fig. 2.9. The optimal PAE is over 30% with 265° and 2.3 mW. Due to limited power gain and supply voltage (1V), the high PAE region is biased at class-AB and below 10 mW power level. Estimation of PAE in Teledyne 250-nm InP HBT with 700-GHz at 140-GHz f_{max} and passive Q of 20 is also plotted in Fig. 2.10 where the peak PAE over 44% is feasible with 195° and 15 mW. PAE in Teledyne 250-nm InP HBT at 220-GHz is also plotted in Fig. 2.11 where the peak PAE over 32% is observed with 240° and 10 mW. With the calculation and plots shown above, the selection of technologies with targeted output power and the bias design of PA is more clear. Besides, insight of whether using a single high power PA or power-combined PA could be observed. For instance, if a 140-GHz 17dBm PA is targeted in 22-nm FDSOI

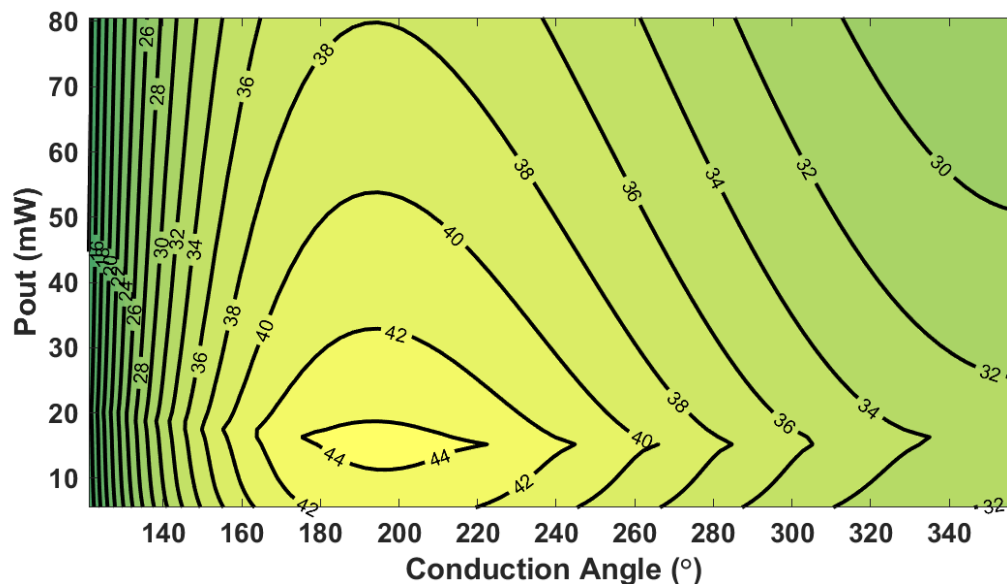


Figure 2.10: Calculated PAE contour with output power and conduction angles in 250-nm InP HBT at $f_0=140$ GHz.

process, the highest PAE from a single PA is about 19% from Fig. 2.9. However, if we use two 14.3 dBm and power combining with 0.3 dB loss, 20.5% PAE with same output power could be achieved.

2.3 Switch basics

Switches are widely used in cellular communication systems including Frequency-Division Duplexing for selecting bands and Time-Division Duplexing for switching between transmitter and receiver path. Switches are also used in several different systems such as SPST in an on-off keying transmitter as shown in Fig. 2.12 and SPDT switches in a Dicke receiver as shown in Fig. 2.13.

Series shunt topology is not uncommon in low frequency SPDTs as shown in Fig. 2.14. Number of stacked transistors is dependent on the power handling and the requirement for sub-6GHz application usually goes above 30 dBm. Due to limited $R_{on}C_{off}$ performance,

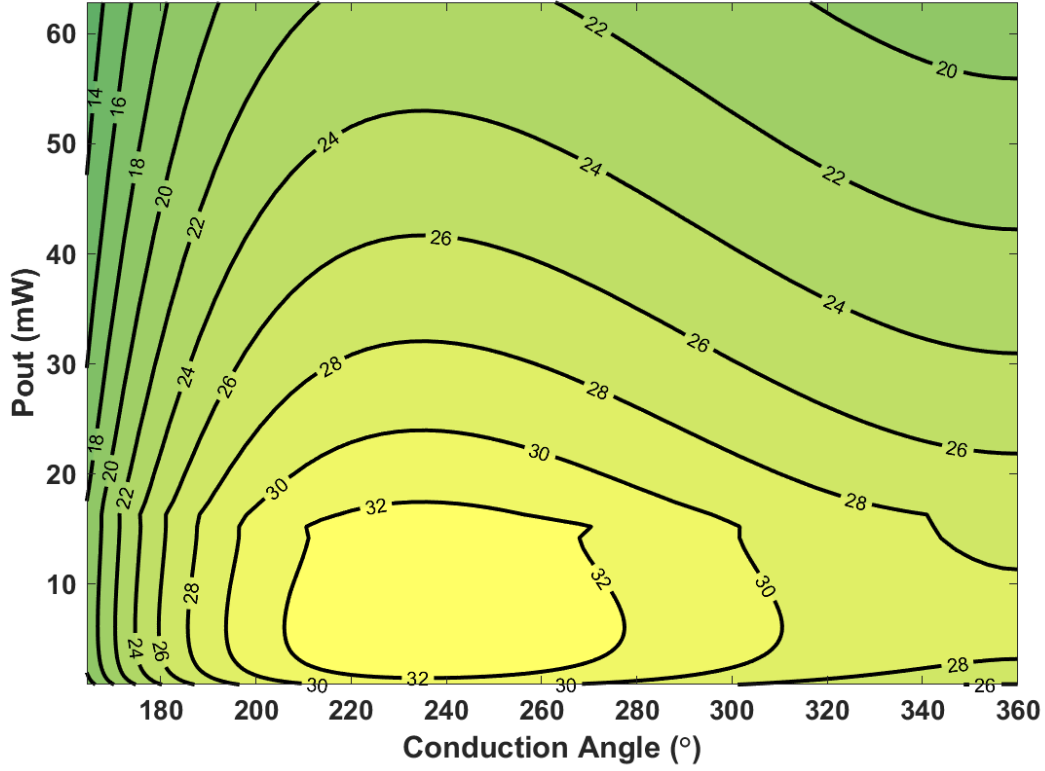


Figure 2.11: Calculated PAE contour with output power and conduction angles in 250-nm InP HBT at $f_0=220$ GHz.

Off-state of series path is not providing sufficient isolation at upper mm-wave bands. Therefore, shunt transistors with transmission line are usually adopted as shown in Fig. 2.15 [11] [12]. SPSTs in a SPDT should present low R_{ON} in the off-state as well as transform a low impedance to a high impedance through quarter-wavelength transmission lines at the input to prevent loading on-state path. High shunt impedance should be expected in the on-state path so that signals directly pass through by using short stub or shunt inductance to resonate out C_{OFF} from transistor switches. This approach is also adopted in HEMT devices [13] [14]. However, these switches not only require large area for two quarter-wavelength transmission line but also show limited performance due to R_{ONCOFF} of available processes. In [15], an SPDT is based on magnetically switchable

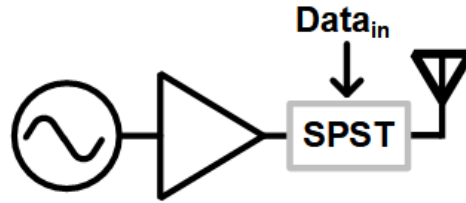


Figure 2.12: On-off keying transmitter.

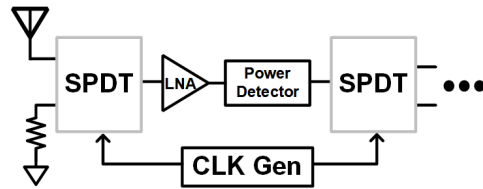


Figure 2.13: Dicke receiver.

artificial resonator is proposed at D-band to control the coupling factor between input and output short stubs as shown in Fig. 2.16. This eliminates the area penalty of quarter-wavelength transmission line, but the performance still suffers from $R_{on}C_{off}$ of the process.

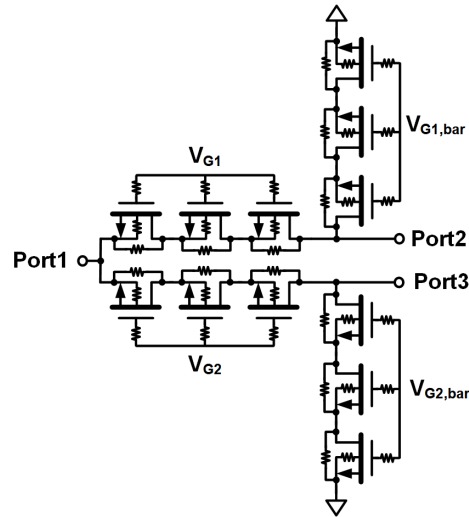


Figure 2.14: Series-shunt SPDT.

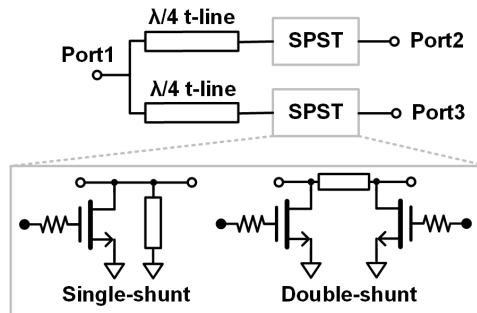


Figure 2.15: Conventional upper mm-wave bands SPDT.

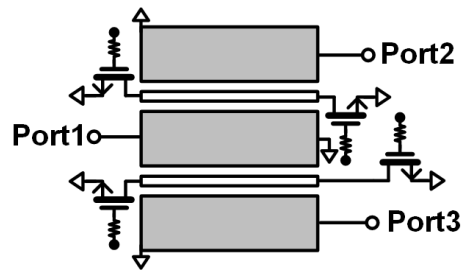


Figure 2.16: Artificial resonator SPDT.

Chapter 3

D-band PA in 22-nm FDSOI CMOS process

With low gain at D-band and low supply voltage in CMOS process, multiple stages and multi-way power combining in PA designs is required to reach over 17 dBm output power. Several D-band PA in silicon have been published in the past few years based on compact designs but with P_{sat} of only 15dBm [16] and 12.5dBm [17], respectively. In [18], the efficiency is limited. However, [19][20][21] demonstrate PAs with more than 50-mW P_{sat} , but the area also scales with power since multi-way power combiners and multiple transmission lines are used. In this Chapter, a compact 4-way-combined PA is introduced based on a multi-stage, pseudo-differential power cell with neutralization capacitance.

3.1 GlobalFoundries 22-nm FDSOI CMOS process

The f_T and f_{max} trend of CMOS process is shown in Fig. 3.1. As observed from the plots, process nodes at 40/45-nm and 28/22-nm show the most promising f_T and f_{max} . If

intensive digital or high speed mixed mode circuits are also considered in RF front-end, 28/22-nm is preferred for it's higher transistor density as well as lower switching power consumption. GF 22-nm FDSOI serves a good candidate for Sub-THz RF circuit design due to it's high f_T/f_{max} as summarized in Table. 3.1. The simulated results in the table shows over 400-GHz f_{max} in several devices in this process. SLVT with larger gate pitch (2XCPP) is chosen for PA designs to avoid electromigration issue while f_T/f_{max} is degraded due to longer gate routing as well as more parasitic capacitance. From the table, the device performance degradation due to metal stack is also observed. 22-nm FDSOI has 10 metal layers with 7 of them are thin metal layers while 3 of them are thick metal layers. The device model comparison with metal built up to first thin metal layer and fifth thin metal layer could also be found in Table. 3.1. The simulated results show huge degradation between these two models and this constrains the performance of circuit implementation while operating at sub-THz region.

Metal connection	RVT	LVT	SLVT(1XCPP)	SLVT(2XCPP)	SLVT(3XCPP)
M1(f_T/f_{max})(GHz)	334/450	341/438	333/457	324/434	313/417
C3(f_T/f_{max})(GHz)	298/371	300/358	297/364	264/331	241/289

Table 3.1: f_T and f_{max} of different devices in 22-nm FDSOI CMOS.

3.2 Power cell design in 22-nm FD-SOI CMOS

To address the metal interconnect issue mentioned in the last section, the transistor layout is optimized in the proposed design. The expressions for f_T and f_{max} are

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, f_{max} = \sqrt{\frac{f_T}{8\pi r_g C_{gd}}}. \quad (3.1)$$

Therefore, the gate-drain capacitance should be minimized for higher maximum avail-

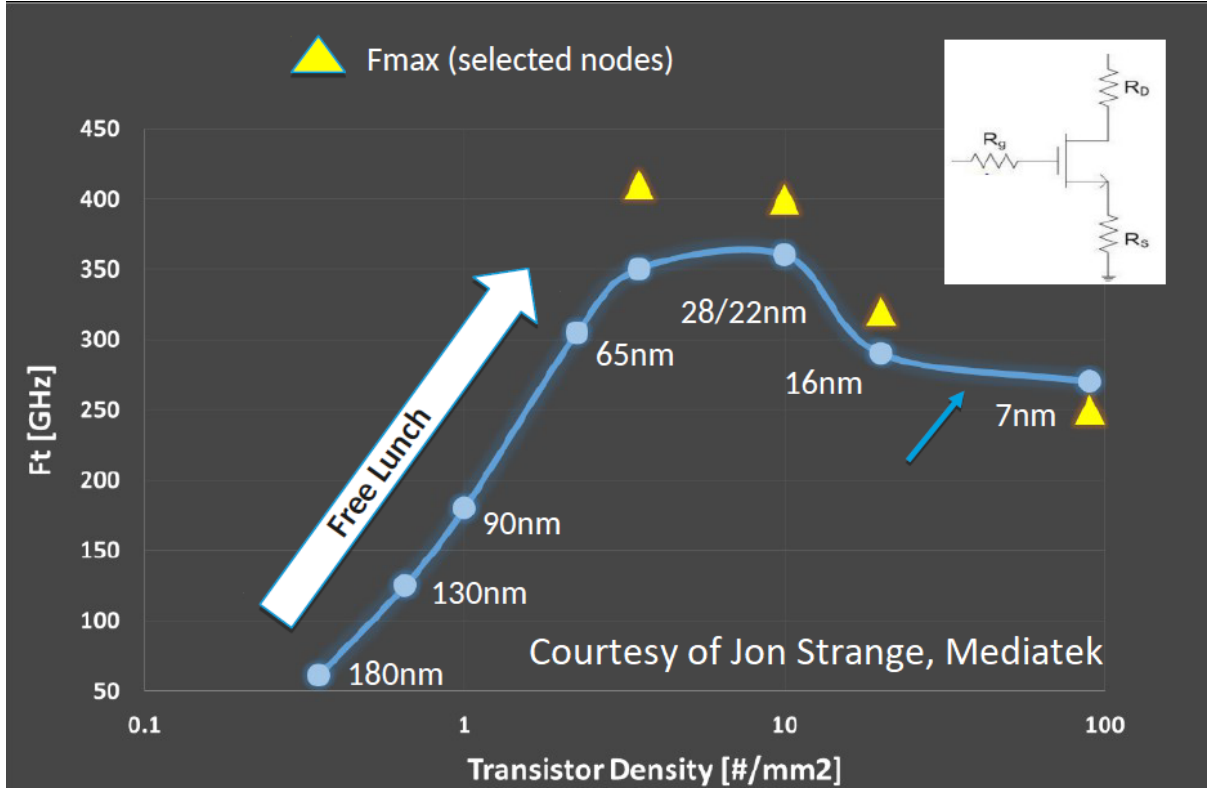


Figure 3.1: Trend of f_T and f_{max} in CMOS processes. (Source:Jon Strange, Mediatek.)

able gain. Although minimizing r_g and C_{gd} presents a trade-off, reducing C_{gd} is a priority since the neutralization capacitor (C_{neu}) will be added to both the input and output node in the differential power cell design. In most cases, C_{neu} is equal to C_{gd} for achieving best stability condition and, therefore, the total capacitance on the drain node will become

$$C_{d,total} = C_{db} + C_{ds} + 2C_{gd}. \quad (3.2)$$

The increase of the capacitance pushes the power and PAE contours of the transistor to a high voltage-standing-wave ratio on the Smith chart. This will also further deteriorate the output matching loss and bandwidth. With the above mentioned approach, a single transistor layout is shown in Fig. 3.2. Using the first metal as base, the source is connected to global ground using the second metal layer. This could not only reduce

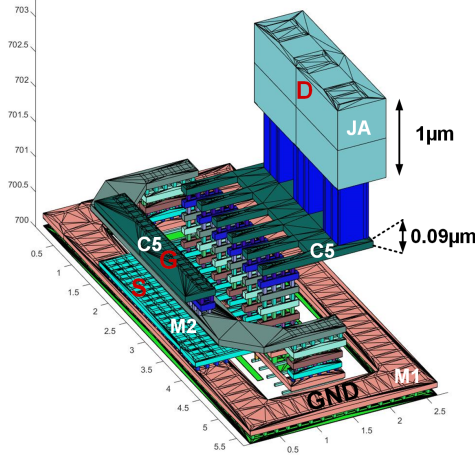


Figure 3.2: Single transistor layout.

the resistance to ground but also prevent the fringe capacitance with gate and drain. The gate is connected to the upper thin metal layer from C3 to C5 and only drain node is connected to the thick metal layer for reducing fringe capacitance between gate and drain. The simulated G_{max} comparison between different models are shown in Fig. 3.3. The optimized layout with M1 model provides higher f_{max} than the C3 model in PDK. Fig. 3.4 shows the simulated drain capacitance with different layout. 17% capacitance reduction is observed comparing the optimized layout to M3 model, which means lower output matching loss or higher output power could be achieved.

To further increase output power of a single PA path, pseudo-differential with 8-fold gate connections on each side is designed as shown in Fig. 3.5. To improve the small signal stability, two C_{neu} are added between two cells. The load-pull simulation of the proposed power cell layout with 6 dBm input power is shown in Fig. 3.6 and Fig. 3.7 with 33.6% peak PAE and 12.2 dBm output power at $Z_{opt} = 18 + j*32\Omega$. The simulated P_{sat} of this power cell is around 13.4 dBm under 1.1-V supply.

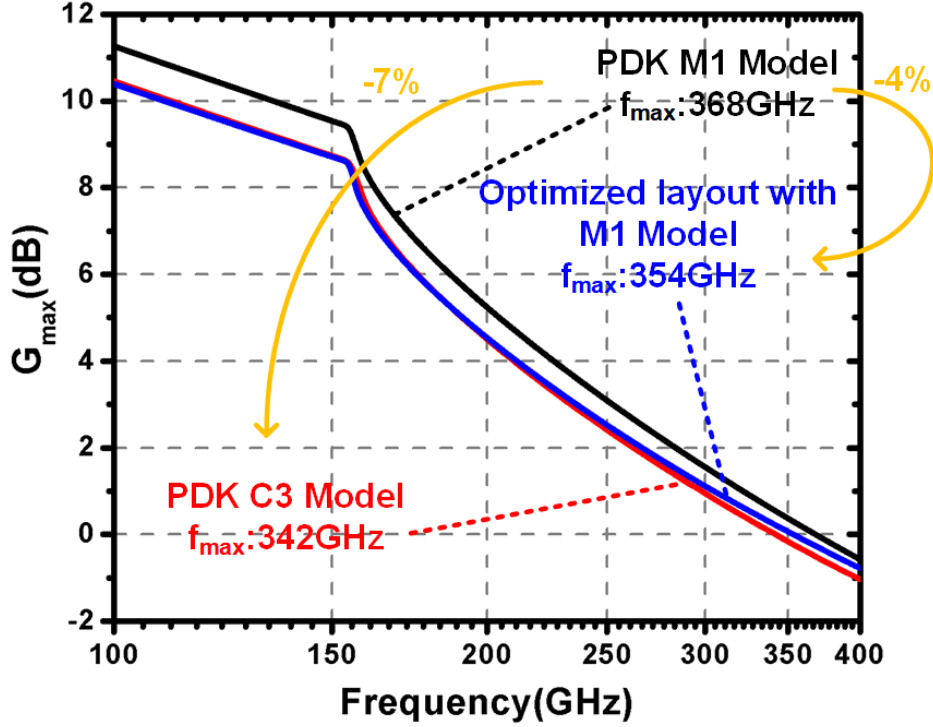


Figure 3.3: G_{max} comparison between different transistor layout.

3.3 Coupled-line balun and parallel power combiner design

The output balun plays an important role in mm-wave differential PA design. One popular implementation is based on transformer balun [16][17][20][21]. However, the loss of a transformer balun increases dramatically due to lower in-band quality factor as well as the drop of coupling factor since the shunt inductance required to resonate out the power cell capacitance reduces at high frequency and targeted output power. With the fixed metal stack, [16] proposed a high-k sandwiched transformer. However, the coupling factor is still limited to 0.73 and this constrains the minimum feasible loss at the output matching network.

In [22], the authors proposed a SQWL balun that achieves excellent insertion loss (IL)

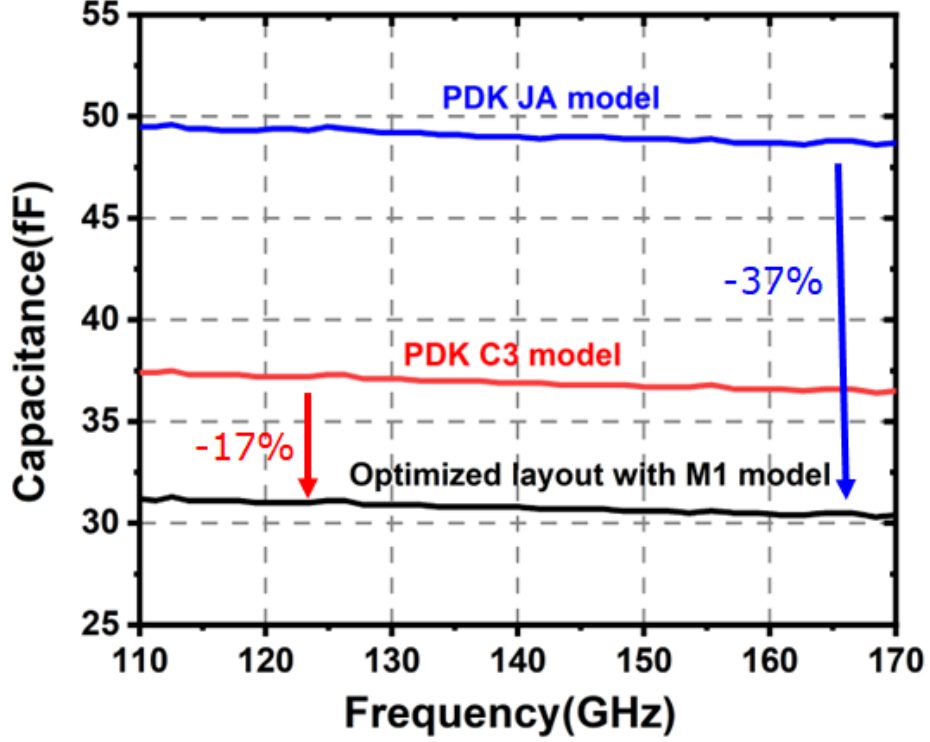


Figure 3.4: Drain capacitance comparison between different transistor layout.

with impedance transformation. However, the bottom transmission line of the SQWL balun needed to be far away from ground so that the desired impedance could be fulfilled. This makes the topology less compact and hard to incorporate with multi-way power combiner. Also, at high frequency, the finite quality factor of the bypass capacitor at two ends of bottom plates increases the loss of the whole balun.

Here, we propose the CLB as shown in Fig. 3.8. With the bended structure, the AC ground could be leveraged and supply voltage could be fed on left or right direction which makes multi-way power combining simpler. The simulated G_{max} of the proposed CLB is -0.51 dB as shown in Fig. 5, the equivalent inductance of two coils are 87.4pH and 82.4pH and the coupling factor is 0.82 at 140 GHz. To achieve higher output power,

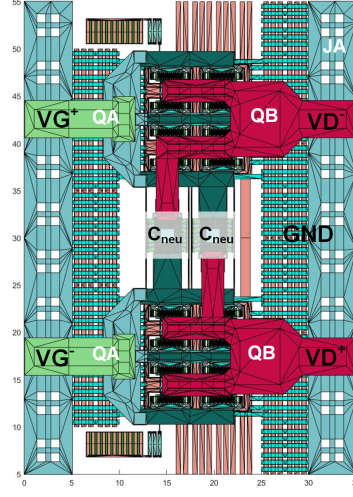


Figure 3.5: Differential power cell layout with 8 multipliers on each side.

4-way parallel power combiner is shown in Fig. 3.9. The design methodology follows

Step 1) Optimize the single path balun with the targeted P_{sat} and highest achievable PAE.

Step 2) Place two balun in parallel closely and figure out Z_{opt} that provides similar P_{sat} and PAE as Step1. The result in our implementation is $Z_{opt} = 17.1 + j*7.8\Omega$.

Step 3) Figure out the RF pad impedance Z_{pad} with pre-fill metal dummies.

Step 4) Figure out the transmission line impedance and length to match Z_{opt} and $2Z_{pad}$.

With the above mentioned steps, 4-way parallel power combiner is designed with simulated 1.2dB insertion loss including RF pad loss at 140 GHz.

3.4 Measurement results of four-way power combined PA

The proposed PA is implemented in a GlobalFoundries 22-nm CMOS FD-SOI technology and illustrated in the microphotograph in Fig. 3.10. The core area of the PA is $450\ \mu\text{m}$ by $250\ \mu\text{m}$ while the overall chip size limited by probe spacing is $620\ \mu\text{m}$ by $600\ \mu\text{m}$

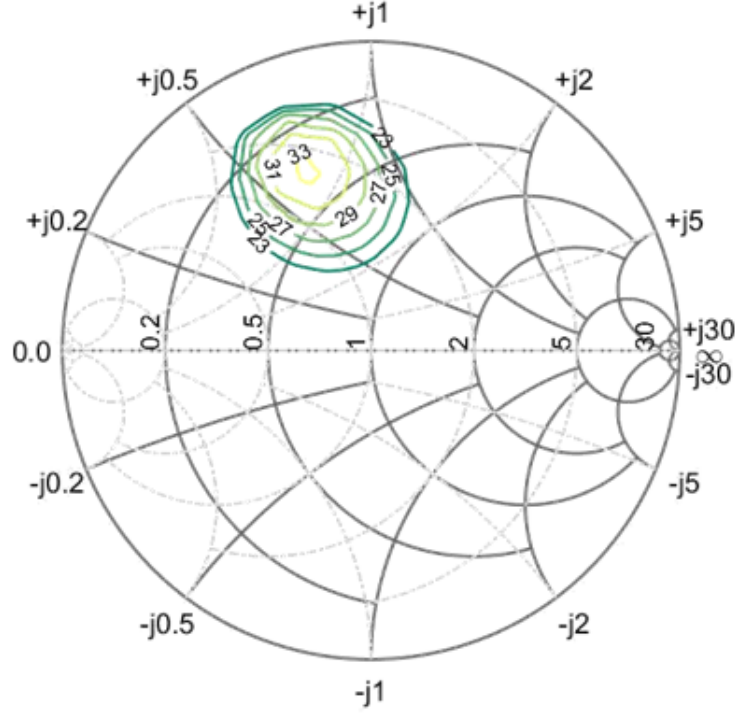


Figure 3.6: PAE contour of the proposed power cell.

μm . The PA gate is biased with 0.5 V and the collector supply is 1.1V.

The S-parameters and power measurement are performed with D-band (110-170 GHz) VDI frequency extenders and D-band 100- μm pitch waveguide probes. Calibration is done with CS-15 calibration substrate to the probe tip. The measured and simulated S-parameters are plotted in Fig. 3.11. The measured peak gain is 13.5 dB with 111-149 GHz 3-dB bandwidth. Power measurements are plotted at 140 GHz as shown in Fig. 3.12. The 16% peak PAE is measured at 15.7 dBm output power while still having 10-dB power gain at 140 GHz. The output power and PAE are also measured in Fig. 3.13 across the D-band. The measured peak PAE is 16.5% at 114 GHz and 17.5 dBm peak P_{sat} at 124 GHz. Table 1 summarizes the state-of-the-art D-band PAs in silicon for the

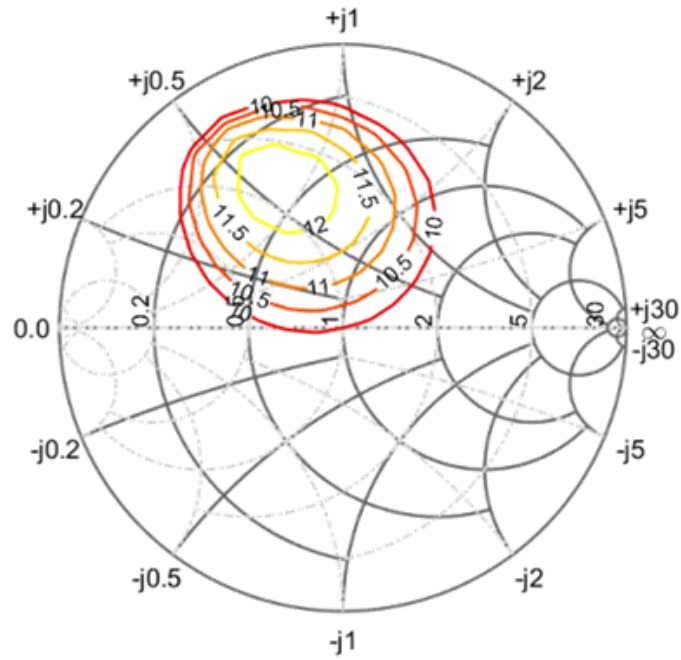


Figure 3.7: Power contour of the proposed power cell.

comparison of the presented work. The PA demonstrates the highest PAE in CMOS SOI while also demonstrating compact area and wideband operation.

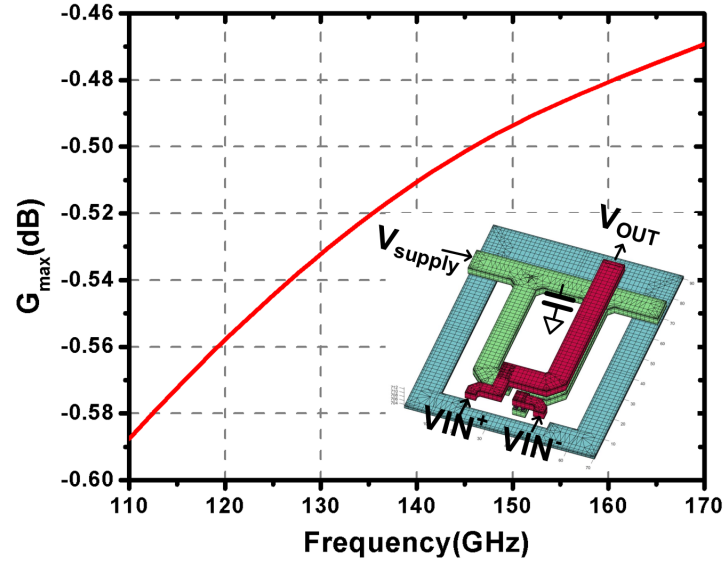
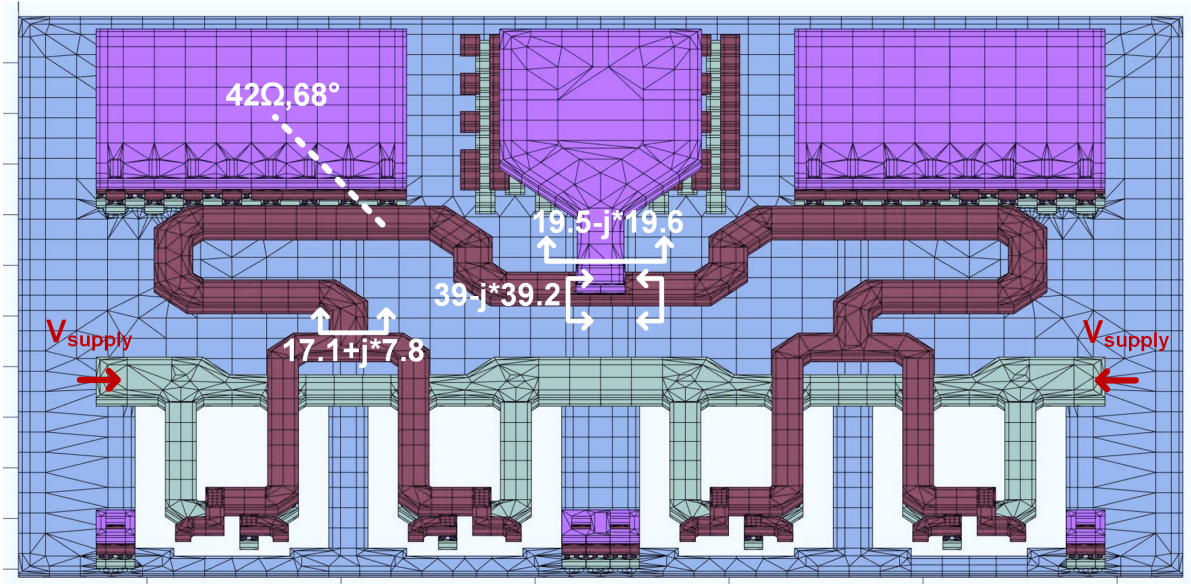
Figure 3.8: G_{max} of the proposed CLB.

Figure 3.9: Layout and impedances of four-way output combiner.

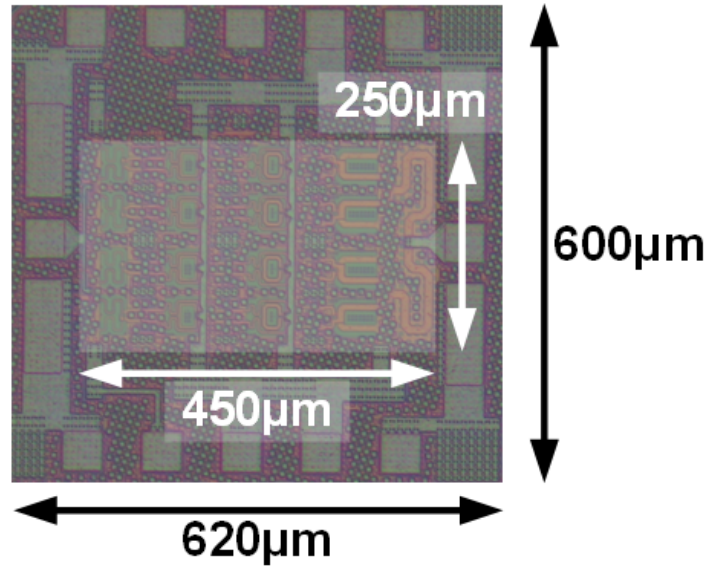


Figure 3.10: Die photograph of the fabricated four-way power combined PA in 22-nm FDSOI CMOS.

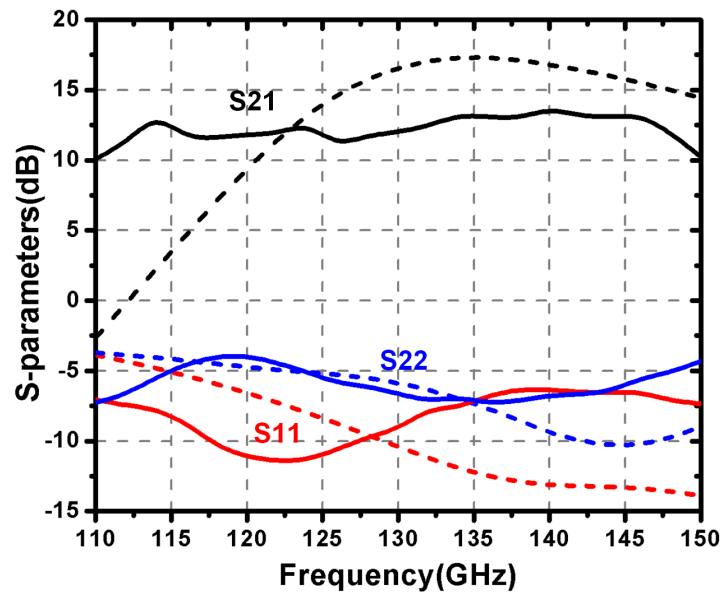


Figure 3.11: Measured (solid) and simulated (dashed) S-parameters.

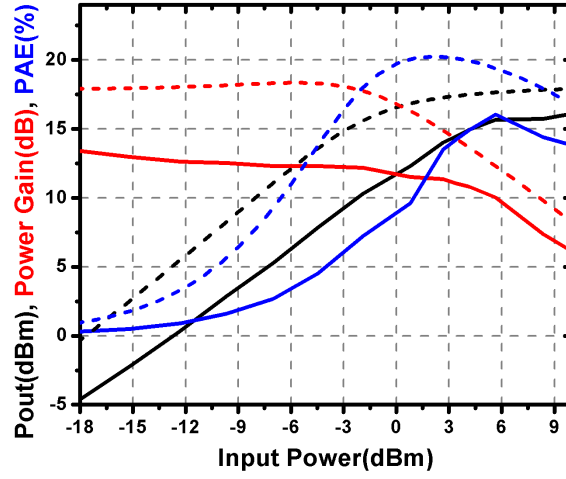


Figure 3.12: Measured (solid) and simulated (dashed) output power, power gain and PAE versus input power at 140 GHz.

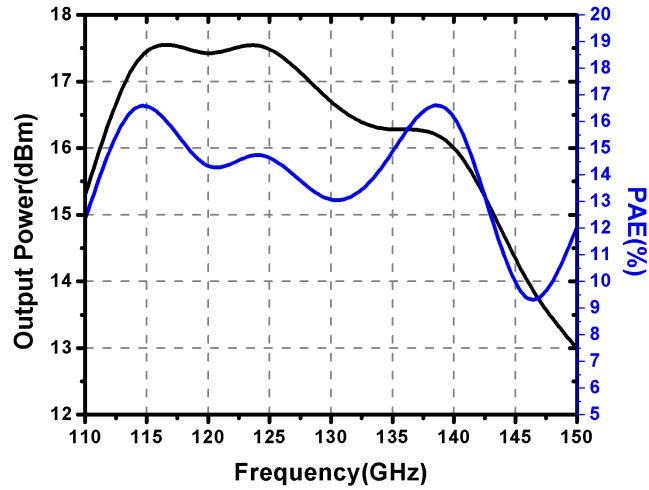


Figure 3.13: Measured output power and PAE over 110-150 GHz.

Chapter 4

D-band and G-band PA in 250-nm InP process

In Chapter 3 Fig. 3.1, the highest f_{max} from all available CMOS process is limited to around 400 GHz. This not only limits the achievable power gain but also constrains PAE of PA. To achieve better performance, InP is a better candidate for higher peak PAE if we compare calculated results in Fig. 2.9 and Fig. 2.10. In this section, InP PA designs in D- and G-band will be discussed.

4.1 110-128 GHz PA design

Several recent D-band InP PA designs have demonstrated high efficiency [23] and high power [24][25] using a 250nm InP HBT technology. However, chip area is often dominated by matching elements such as transmission line and this impacts the area available for front-end integration. Compact PAs are required for scalability of 2-dimensional phased arrays at D-band.

In particular, the implementation of the output matching and the combiner networks

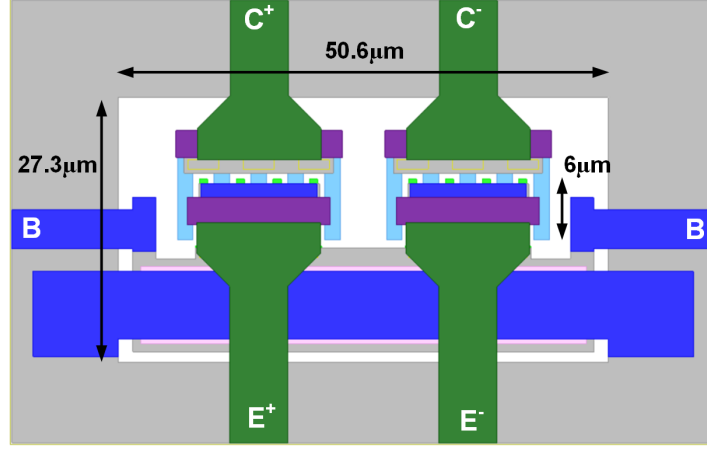


Figure 4.1: Footprint of differential $4 \times 6\mu\text{m}$ power cell.

has a significant impact on PA performance as the area of the matching network impacts the power density and the losses of the output matching network impact the maximum efficiency of the PA. Increases to higher frequency bands introduce higher losses in the combiners and matching networks in high power PA design but benefit from the reduction of the physical area. To address the power density issue, a CLB similar to CMOS design in Chapter 3 is used to occupy a small area and reduce the balun loss to achieve high efficiency.

Pseudo-differential design is attractive for high-power-density, millimeter-wave (mm-wave) PAs due to the virtual ground which avoids off-chip return currents and eliminates large on-chip bypass capacitors. Pseudo-differential stages also aid in power combining since the impedance seen from the transistor collector is halved compared to single-ended design if a 1:1 transformer is applied at the output. The loadline of the pseudo-differential transistors also reduces the loss in the output balun. In [23], the rationale of selecting CB over common-emitter (CE) is discussed and this work reaches a similar conclusion. As shown in Fig. 4.1, the power cell includes a pair of 4-finger 6- μm emitter length HBTs. The device geometry produces a loadline that is highly related to the matching loss [16],

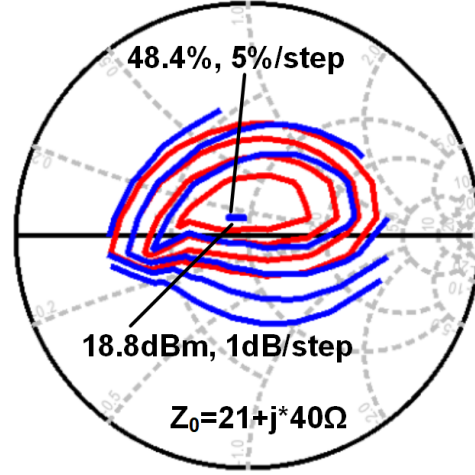


Figure 4.2: Simulated power contour (red) and PAE contour (blue) of differential $4 \times 6 \mu\text{m}$ power cell.

and we limit the output matching loss to 1dB to achieve high efficiency. The collector metals are shared between different fingers to obtain the minimum footprint and base voltage is fed either from the left-hand side or right-hand side. The base connections of each HBT are connected closely such that AC currents have a low-impedance path between the devices. Additionally, the DC connection for the base can be located symmetrically on either side of the pair of HBTs. Load-pull simulations of power cell are shown in Fig. 4.2. The differential equivalent output impedance shows $65\text{pH}/120\Omega$ is required with 18.8 dBm peak power and 48.5% peak PAE.

To reduce the size and improve loss of balun design, bended transmission line leveraging virtual ground similar to CMOS PA design in Chapter 3 is used. As shown in Fig. 4.3, the differential port (IN+ and IN-) is the stacked metal of metal2 and metal3 while the single-ended port (OUT) is on metal4. IN+ is directly connected to OUT while the signal from IN- is coupled from metal3 to metal4. The simulated G_{max} of this CLB is -0.67dB at 120GHz.

Fig. 4.4 shows the detailed schematic of the proposed pseudo differential CB PA. Additional matching network is added after CLB for matching to 50Ω and input balun is also

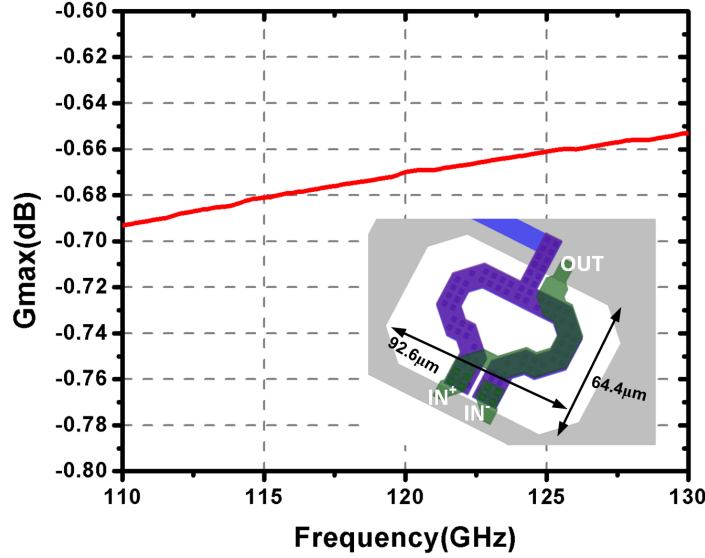


Figure 4.3: The layout of the proposed coupled line balun and the simulated G_{max} indicating 0.67 dB of loss at 120 GHz.

designed using similar structure as output balun. It is worth mentioning that although G_{max} of the proposed structure is better than -0.7 dB, the overall output matching loss is around 0.9 dB as shown in Fig. 4.5. Input matching contributes to equivalent 0.54 dB loss at the output due to the degradation of power gain.

The proposed PA is implemented in 250-nm InP HBT technology and illustrated in the microphotograph in Fig. 4.6. The core area of the PA is 250μm by 93μm while the overall chip size limited by probe spacing is 638μm by 433μm. The PA base is biased with 0.75V and the collector supply is 2.3 V.

The S-parameters and power measurement are performed with D-band (110-170 GHz) VDI frequency extenders and D-band 100μm pitch waveguide probes. Calibration is done with CS-15 calibration substrate to the probe tip. The measured and simulated S-parameters are plotted in Fig. 4.7. The S-parameters are measured with input power from frequency extender between 7.9dBm to 10.6dBm in the band of 110-140 GHz. The measured peak gain is 8.3dB with 110-128 GHz 3dB bandwidth. Power measurements

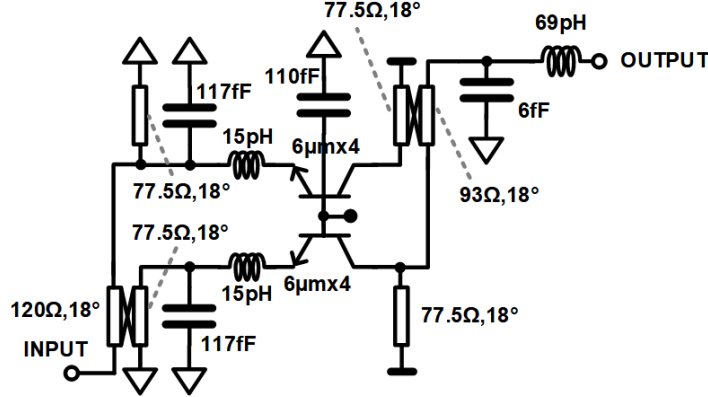


Figure 4.4: Schematic of the proposed single-stage D-band PA with 0.75 V base voltage and 2.3 V supply.

are plotted at 114 GHz as shown in Fig. 4.8. The 32.7% PAE is measured at 17.6 dBm output power while still having 8.5-dB power gain. Due to the limitation of input power from frequency extender, P1dB point was not measurable. Output power and PAE across frequencies are also measured in Fig. 4.9. The measured output power is over 16 dBm and PAE is over 20% in the range of 110-127GHz.

4.2 200 GHz PA designs

Several G-band PAs have been published over the past few years. Bulk or SOI CMOS processes have limited f_T/f_{max} as well as low supply voltage. In [26][27], output power and PAE of CMOS PAs are below 10-dBm and 8%. PA designs in SiGe HBT processes have shown decent power gain with multi-stage design and high output power with power combining at lower G-band range [28][28] but the efficiency is limited to single digits above 200 GHz [29][30]. Compared to SiGe HBT, the 250-nm InP HBT process has superior collector-emitter voltage breakdown and higher f_{max} for G-band PAs and has demonstrated high output power amplifiers with high small-signal gain across 140-220 GHz [31][32][33][34][35][36]. Despite higher gain, prior work reported similar PAE to

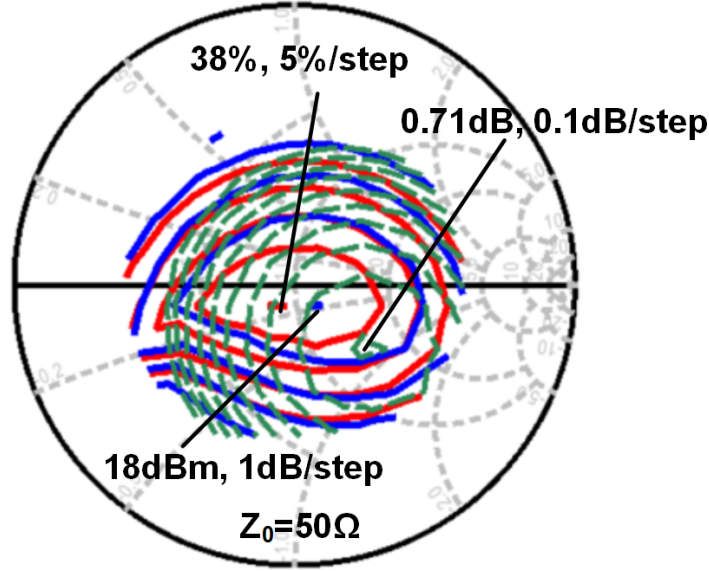


Figure 4.5: Simulated power contour (red), PAE contour (blue) and output matching loss contour (dashed green) of the proposed PA.

Table 4.1: Simulated parameters of CE and CB at 220 GHz

Simulated performance at 220 GHz	CE	CB
G_{max}	5 dB	11.7 dB
Stability factor	1.3	0.4
Peak PAE	38.3%	35.1%
$P_{out}@PAE_{peak}$	12.5 dBm	11.6 dBm
Peak PAE with 1-dB output matching loss	25.5%	26.9%
Peak PAE with 1-dB input and output matching loss	20.7%	25.5%

SiGe due to lossy matching networks and bulky power combiners. InP HEMT or GaN HEMT are processes that can achieve high f_T/f_{max} but PA performance at G-band is still not competitive compared to SiGe or InP HBT due to increased loadline matching conditions [37][38][39].

Transistor topology is a significant consideration above 100 GHz due to the role of parasitics in different device technologies. In general, higher gain is desired for compensating input matching losses of PA. Common-emitter (CE) is commonly selected for PA designs in millimeter-wave bands [33] but CB [31] is also a candidate for InP HBT

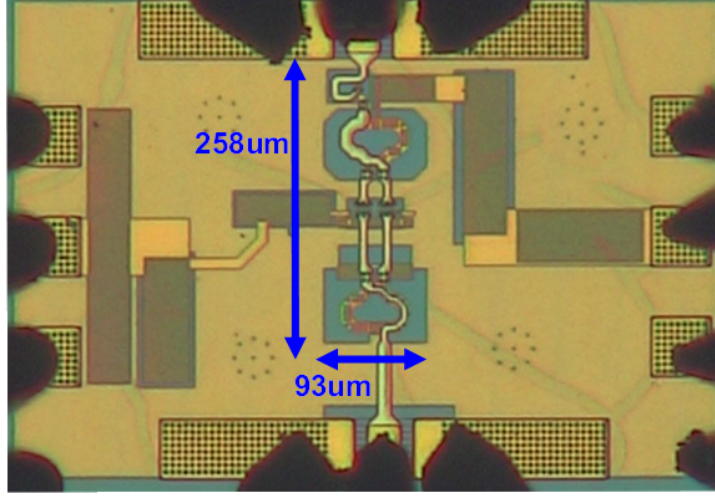


Figure 4.6: Micrograph of the proposed InP D-band PA.

process. From small signal simulation using 2-finger, $4\text{-}\mu\text{m}$ emitter length devices under current density of $2.75\text{ mA}/\mu\text{m}^2$, CE shows lower G_{max} across the whole G-band band compared to CB as plotted in Fig. 4.10. The performance summary of two topologies including small signal and large signal at 220-GHz is shown in Table 4.1. Although CE shows lower power gain than CB, the intrinsic PAE and output power of CE are both slightly better than those of CB. However, if passive matching loss is considered as shown in the last two rows in Table 4.1, CB designs maintain higher PAE compared to CE design. Comparing peak PAE including 1-dB input and output loss with the intrinsic PAE, PAE of CE is degraded with 17.6% while PAE of CB is only 9.6% lower. Therefore, CB is favorable for G-band PA design.

As plotted in Fig. 4.10, CB requires additional stabilization circuitry since the stability factor is less than one across the entire G-band. [31], the authors leverage the sizing of base capacitance to linearize and stabilize CB stages. A collector series resistor is applied in [40] for stabilizing CB stages. In [41], a partially neutralized capacitor is implemented to prevent degradation on G_{max} of CB. These three topologies and the rationale for design selection will be discussed in this section.

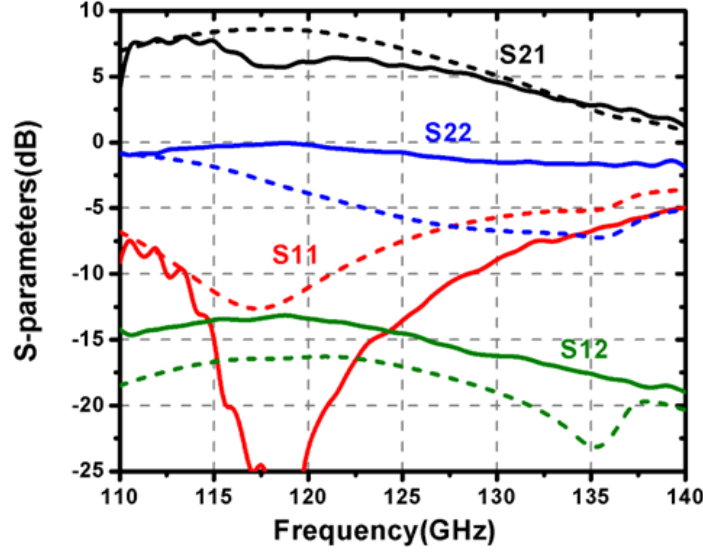


Figure 4.7: Measured (solid) and simulated (dashed) S-parameters.

Finite base capacitance is designed in [31] without revealing the design consideration or parameters. To understand the reasonable design parameters, simulation of stability factor and maximum gain at 220-GHz with the sweep of base capacitance and quality factor (Q) of capacitance are shown in Fig. 4.11 and 4.12. As observed from Fig. 4.11, Q of base capacitance should be kept below 10 for stability factor to be higher than 1. From Fig. 4.12, Q of base capacitance should be selected in the range of 2-4 for possibly obtaining higher G_{max} .

With the insight for setting Q of capacitor, the sweep of capacitance for 140, 180, and 220 GHz is shown in Fig.4.13. The simulated results show the base capacitance lower than 70 fF with Q of 2 is required to keep the entire band unconditionally stable. Notably, the MAG variation is less than 2 dB over the 80 GHz range suggesting that this technique is relatively wideband.

Using conventional stabilization technique, a series collector resistor is a straightforward methodology for stabilizing a CB stage [40]. The stability circles of the intrinsic device are reduced and move towards the unit circle by adding collector resistance. The

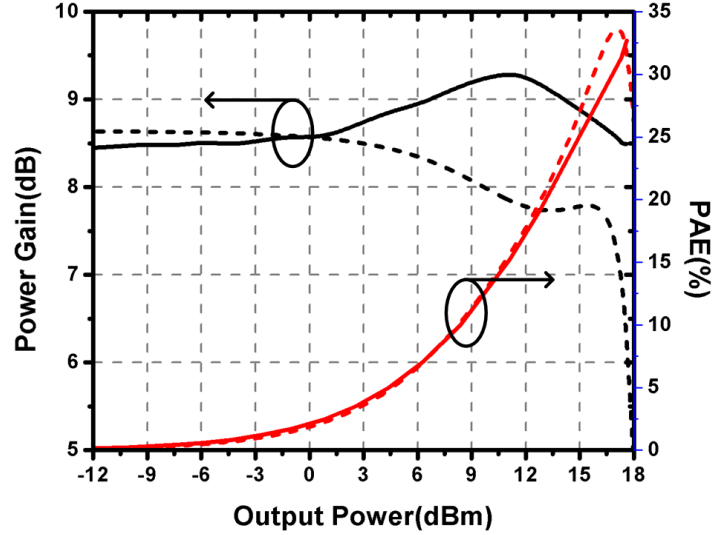


Figure 4.8: Measured (solid) and simulated (dashed) power gain and PAE versus output power at 114 GHz.

topology is simulated at G-band as shown in Fig.4.14. Simulation results show 11.5Ω or higher resistance would stabilize the whole G-band and higher gain at 140 GHz could be achieved compared to base capacitance approach, but gain rolls off quickly at 220 GHz suggesting that this technique will produce relatively narrowband results.

Pseudo-differential neutralization is widely adopted in mm-wave common-source and CE amplifier design in CMOS and BiCMOS process [42]. A pair of neutralization capacitors are added between input and output of amplifier in cross-coupled fashion to enhance the reverse isolation and therefore better stability could be obtained. However, this technique has not been widely adopted with CB mm-wave PAs. In [41], the CB neutralization technique is applied to 600 GHz in 130-nm InP HBT process for high gain but the performance for power amplifiers has not been described.

To understand the topology, simplified small signal model is shown in Fig. 4.15 and Y-parameter can be written as

$$Y_{11} = g_m + \frac{1}{r_{be}} + j\omega(c_{be} + c_{ce} + C_{neu}) \quad (4.1)$$

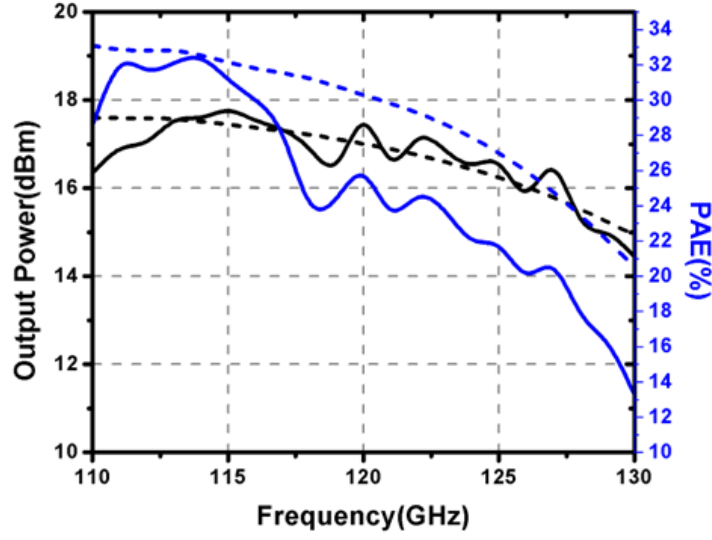


Figure 4.9: Measured (solid) and simulated (dashed) output power and PAE over 110-130 GHz.

$$Y_{22} = j\omega(C_{bc} + C_{ce} + C_{neu}) \quad (4.2)$$

$$Y_{21} = -g_m - j\omega(C_{ce} - C_{neu}) \quad (4.3)$$

$$Y_{12} = -j\omega(C_{ce} - C_{neu}) \quad (4.4)$$

where C_{neu} is neutralization capacitance. From 4.4, we could observe the reverse isolation will be maximized by choosing C_{neu} equals to C_{ce} . Adding C_{neu} tends to push the stability circles out of the Smith chart unit circle as shown in Fig. 4.16. The disadvantage of this topology from 4.1 and 4.1 is the increased total input and output capacitance, which will make input and output matching network more narrowband as well as more lossy. G_{max} and stability factor with the sweep of neutralization capacitance at 140, 180, and 220 GHz is shown in Fig. 4.17. From the plot, C_{neu} should be larger than 1.8 fF for stabilizing the entire band.

If the unconditional stability criteria are the same for all three approaches, G_{max} at 220 GHz of the base-capacitor stabilized approach drops to 6 dB, the collector series-

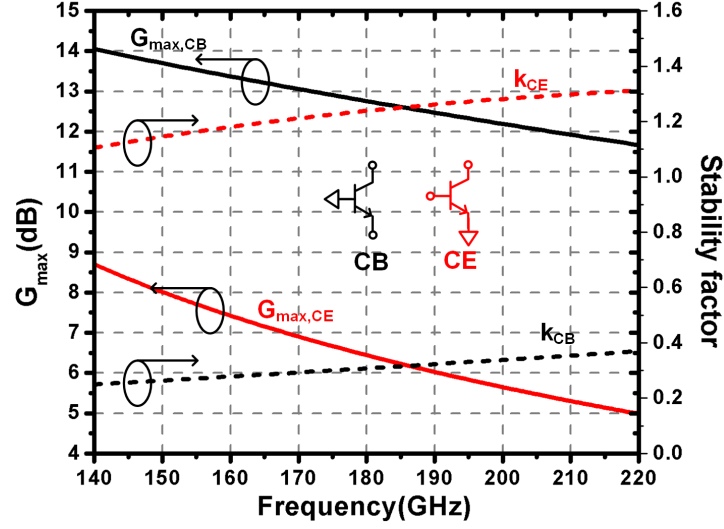


Figure 4.10: G_{max} (solid) and stability factor (dashed) of CE and CB at G-band.

resistor stabilization method drops to 6.8 dB, and the neutralized CB stabilization degrades to 10.2 dB. Therefore, the neutralized CB offers higher G_{max} than the other two cases. It is also worth mentioning that adding collector series-resistor will increase the effective knee voltage and this is not favorable for PA design.

Single-stage (Fig. 4.18) and 3-stage 4-way-combined (Fig. 4.19) PA designs are designed in InP HBT process. Teledyne 250-nm InP HBT process offers four gold metal layers in Benzocyclobutene (BCB) with 75 μm thick InP substrate and through-wafer vias. Thin film resistors and metal-insulator-metal (MIM) capacitors are available in this process.

The single-stage design is constructed with input and output baluns, the neutralized CB power cell, and additional matching network between power cell and balun. 3-stage 4-way-combined design includes both neutralized and non-neutralized CB stages for higher output power. A 4-way power splitter is added between first and second stage along with a 4-way power combiner at the output stage. The device size ratio of three stages is 1:4:8 while the highly coupled transformers are designed between second stage and the last

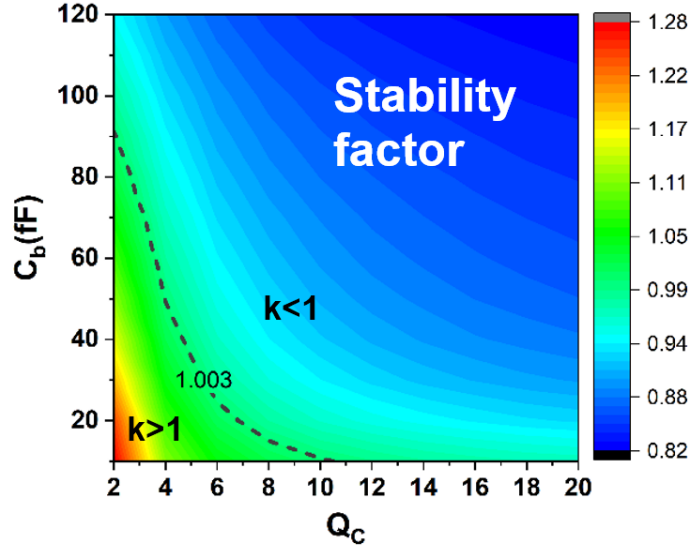


Figure 4.11: Contour of CB stage stability factor with the sweep of base capacitor size and Q of base capacitor at 220-GHz.

stage. Adaptive bias (ADB) is also added to ensure the last stage could be biased lower in small signal region for stability consideration while maintaining sufficient power gain at high power region.

The footprint of the proposed neutralized differential CB power cell is shown in Fig. 4.20 with total device size of $4\mu\text{m}^2$ composed of a pair of 2-finger $4\text{-}\mu\text{m}$ emitter length HBTs. To further increase the output power, the last stage of the 3-stage 4-way-combined PA uses $8\mu\text{m}^2$ total device size periphery formed from a pair of 4-finger $4\text{-}\mu\text{m}$ emitter length HBTs as shown in Fig. 4.22. In this large power cell, the neutralization capacitor is not applied due to large additional input and output capacitance that will increase the loss of matching network and lower PAE. Both designs occupy small area, 2-finger cell is $37\mu\text{m} \times 44\mu\text{m}$ and 4-finger cell is $30\mu\text{m} \times 47\mu\text{m}$.

In both designs, the collectors are shared between different fingers for the minimum footprint as well as reducing the series inductance and phase delay between fingers. The base voltage can be fed from either left or right side making it easier for multi-way power combining design. The distance between all base connections is minimized such that the

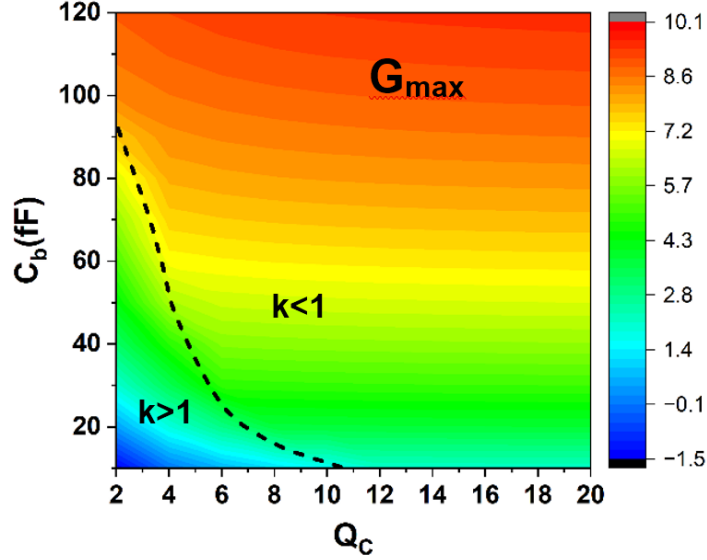


Figure 4.12: Contour of CB stage G_{max} with the sweep of base capacitor size and Q of base capacitor at 220-GHz.

ac currents have a low-impedance path between the devices as well as suppressing base inductances that might introduce instability. A secondary consideration to the distance between these cells is the self-heating between transistors.

Load-pull simulations of the G-band neutralized power cell in Fig. 4.22 are shown in Fig. 4.21 with characteristic impedance of $13.6 + j51\Omega$ at 220 GHz. The differential equivalent load impedance shows $40\text{pH} // 200\Omega$ is required to achieve 13.5 dBm peak power and 32.7% peak PAE at 220 GHz with 6-dBm input power.

Similar to CLB design in D-band PA, the balun design is moved to G-band for both single-stage and power-combined versions. Fig. 4.23 shows the output balun design in the single-stage PA. The differential port (IN+ and IN-) is on metal 3 (M3) while the single-ended port (OUT) is on metal 4 (M4). IN+ is directly connected to OUT while the signal from IN- is coupled from M3 to M4. The simulated equivalent inductance of two coils is 45.6 pH differential and 41.1 pH on single-ended side with coupling factor of 0.58 at 220 GHz. The simulated phase error and gain error between differential ports are

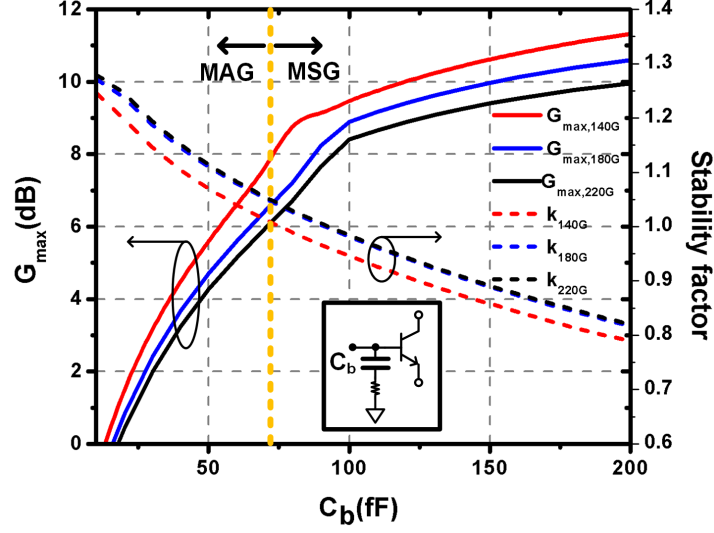


Figure 4.13: Simulated G_{max} and stability factor of sized C_b CB stage at 140, 180, and 220 GHz.

3.4° and 0.12 dB while G_{max} of this CLB is -0.78 dB at 220 GHz.

Low-loss power combiner is a key for keeping high efficiency while targeting high output power. A similar approach is applied to the 3-stage, 4-way-combined PA design. The design parameters at different nodes of parallel power combiner are shown in Fig. 4.24. In this implementation, the RF pad impedance is designed to minimize the length of transmission line for compact size and lower loss. The impedance trajectories are shown in Fig. ?? on Smith chart and the simulated loss of combiner is 0.25 dB.

Since the last stage of the 3-stage, 4-way-combined PA is not a neutralized CB stage, a lower bias condition, e.g. deeper class-AB, is applied for reducing the small signal gain. However, PAE drops with the lower bias condition due to low power gain at high power region. The ADB shown in Fig. 4.19 is formed with a BE diode-connected HBT, a RC filter and an emitter-follower. With capacitive coupling from the output of the first stage, the base voltage of Q1 drops and emitter voltage increases at high power region due to higher current flowing through the base and emitter resistors. The emitter voltage is later fed to an emitter-follower for providing isolation as well as controlling the adaptive

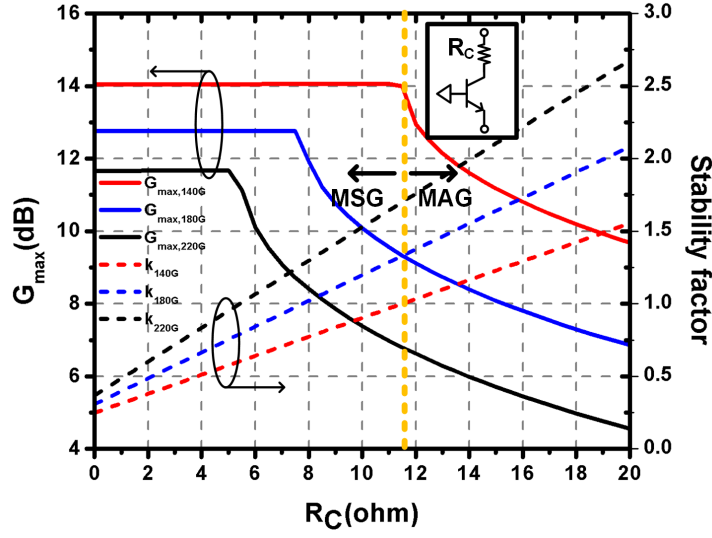


Figure 4.14: Simulated G_{max} and stability factor of collector series-resistor CB stage at 140, 180, and 220 GHz.

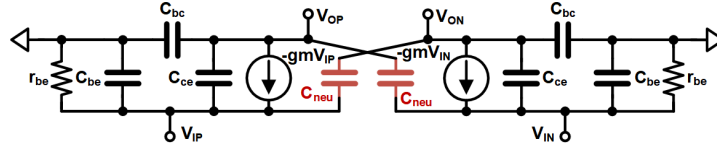


Figure 4.15: Small signal model of pseudo-differential neutralized CB stage.

voltage range. Simulated results of voltage at different nodes are shown in Fig. 4.26. The plot also shows stability factor of PA at 205 GHz is stable at low power region and is still stable at high power region with ADB.

The proposed PAs are implemented in 250-nm InP HBT technology and illustrated in the microphotograph in Fig. 4.27 (a) and (b). The core area of two designs are 0.011 mm² and 0.113 mm² while the chip area including pads are 0.119 mm² and 0.286 mm². The single-stage base is biased with 0.82 V and the collector supply is 2.5 V. The first and second stage bases of 3-stage 4-way-combined PA is biased at 0.83 V and 2.1 V collector. The third stage base is biased with ADB and supply voltage is 2.5 V.

The S-parameters are measured with G-band OML frequency extender with WR5 to WR4.3 wave guide taper as shown in Fig. 4.28. WR4.3 75-μm pitch waveguide probes are

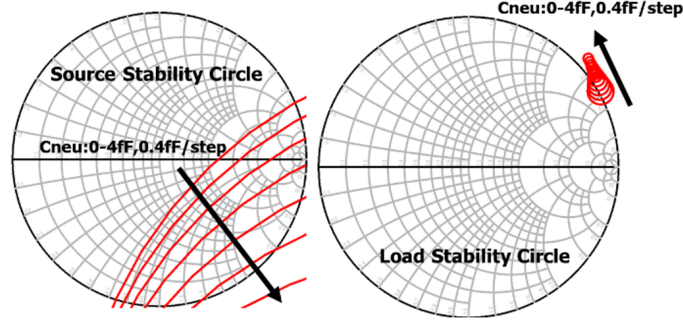


Figure 4.16: Simulated source and load stability circle with sweep of C_{neu} .

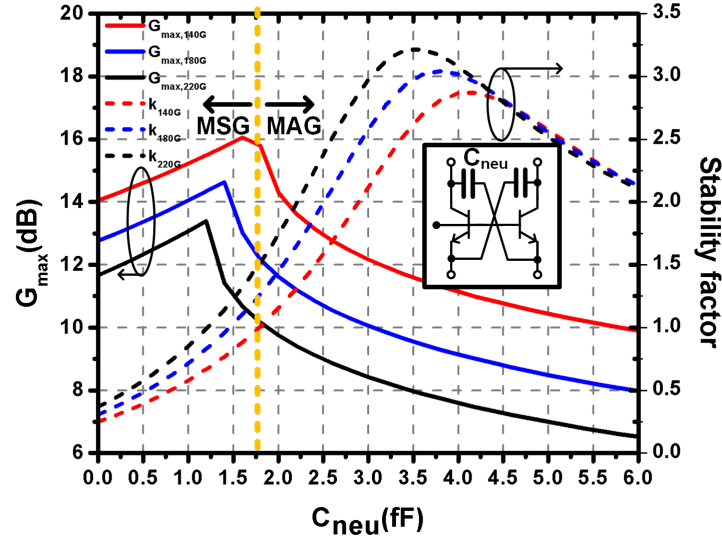


Figure 4.17: Simulated G_{max} and stability factor of collector neutralized CB stage at 140, 180, and 220 GHz.

used, and calibration is done with CS-15 calibration substrate to the probe tip. The power measurement setup is shown in Fig. 4.29 and is executed with VDI WR4.3SGX-M signal generation module as power source. The directional coupler with sub-harmonic mixer on coupled port is used to down convert the input signal for obtaining the calibration factor and tracking the input power. The output is connected to power meter with WR4 to WR10 waveguide taper. The probe loss is captured using the shortest thru line on CS-15 and therefore the calibration is also done to the probe tip for power measurement.

The measured and simulated S-parameters of the single-stage PA are plotted in Fig.

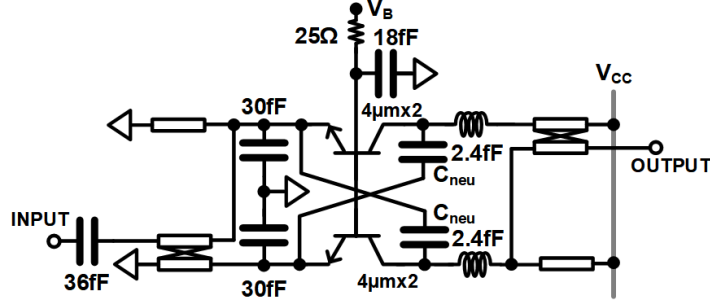


Figure 4.18: Schematic of the proposed single-stage G-band PA.

4.30. The measured peak gain is 7.8-dB at 197 GHz with 182-218 GHz 3dB bandwidth. Power measurements at 200 GHz are plotted in Fig. 4.31. The measured peak PAE is 17.3% at 10.5 dBm output power while still offering 5.7-dB power gain. The OP1dB at 200 GHz is 10.8 dBm. The output power and PAE across frequencies are also measured in Fig. 4.32. The measured output power is over 8.3 dBm and PAE is over 7.7% across a frequency range covering 180 to 220 GHz. The measured small signal gain is downshifted 10% of simulated center frequency which is due to the segmented EM cells that is not capturing the input and output coupling between passive matching networks as well as RF pads. The large signal discrepancy is most likely due to self-heating that is not incorporated into HBT devices model. Similar discrepancy is also observed in [9].

The measured and simulated S-parameters of the 3-stage, 4-way-combined PA are plotted in Fig. 4.33. The measured peak gain is 17.6-dB at 201 GHz with 194 to 207 GHz 3-dB bandwidth. Power measurements at 200 GHz are plotted in Fig. 4.34. The measured peak PAE is 9.1% at 17.8 dBm output power while still offering 16.5-dB power gain. Output power and PAE across frequencies are also measured in Fig. 4.35. The measured output power is between 16.2 to 19.7 dBm and PAE is 3.6-13% in the range of 185-215 GHz.

The PAE survey of G-band PAs is plotted in Fig. 22 and the proposed designs show superior efficiency compared to the prior arts.

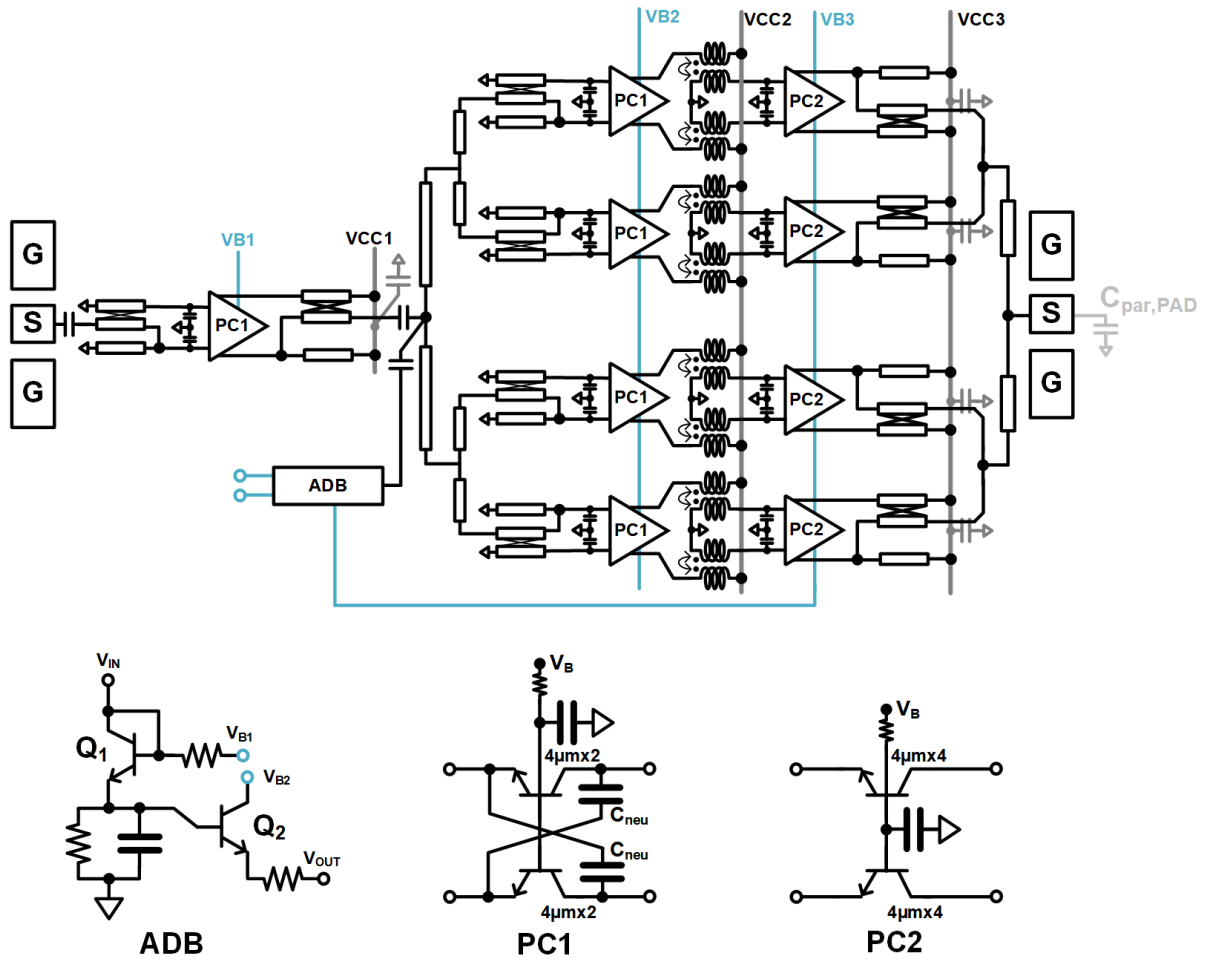
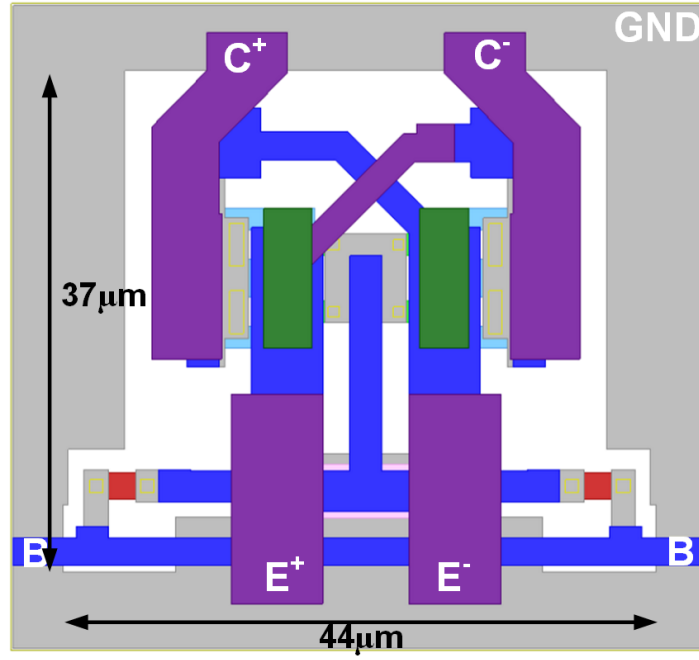
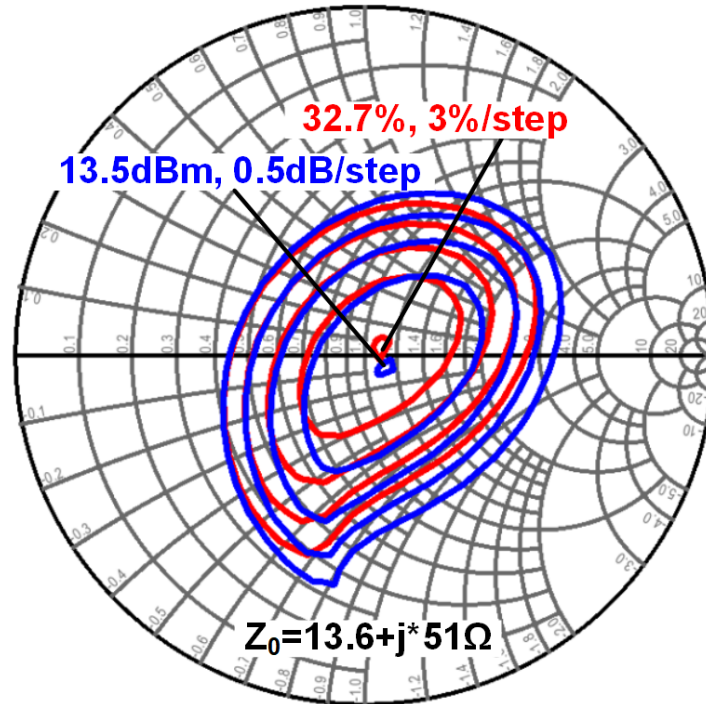
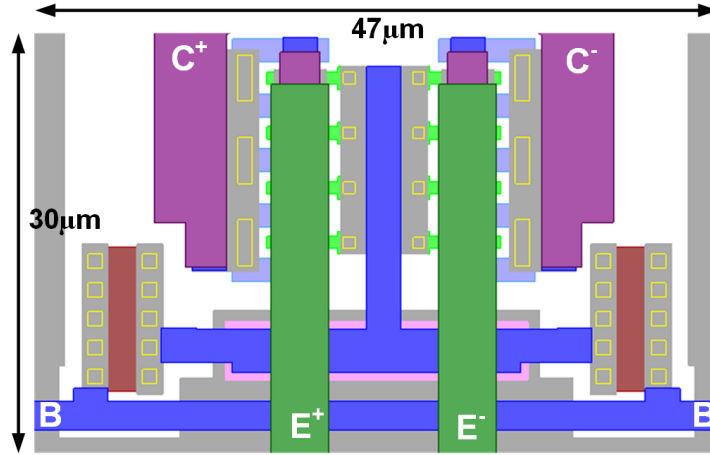
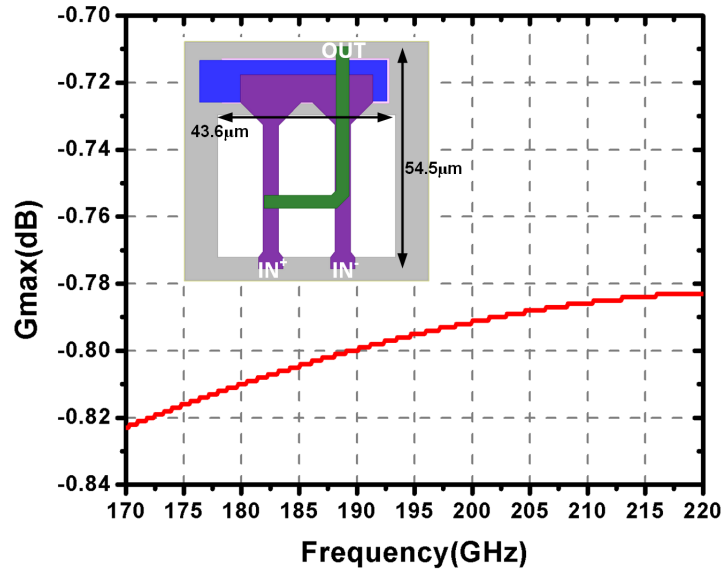


Figure 4.19: Schematic of the proposed 3-stage, 4-way-combined G-band PA.

Figure 4.20: Footprint of differential $2 \times 4 \mu\text{m}$ power cell.Figure 4.21: Simulated PAE contours (red) and power contours (blue) of differential $2 \times 4 \mu\text{m}$ power cell at 220 GHz.

Figure 4.22: Footprint of differential $4 \times 4 \mu\text{m}$ power cell.Figure 4.23: The layout of the proposed coupled line balun and the simulated G_{max} .

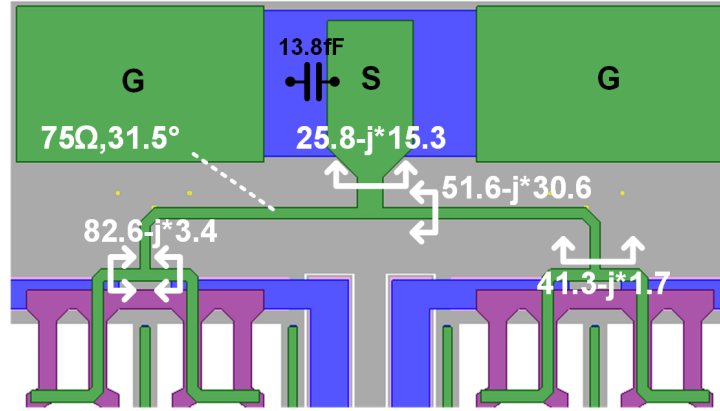


Figure 4.24: Layout and impedances of four-way output combiner.

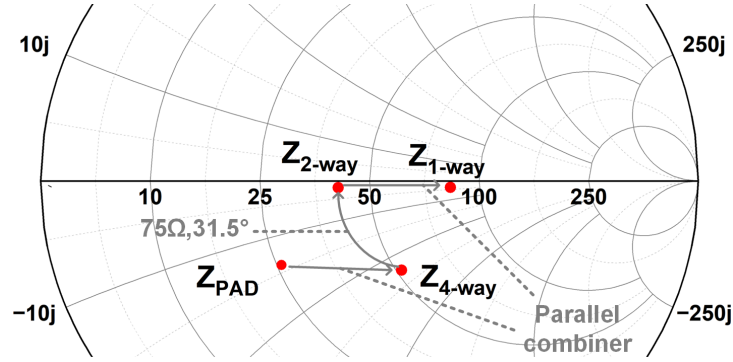


Figure 4.25: Trajectories of power combiner impedance transformation.

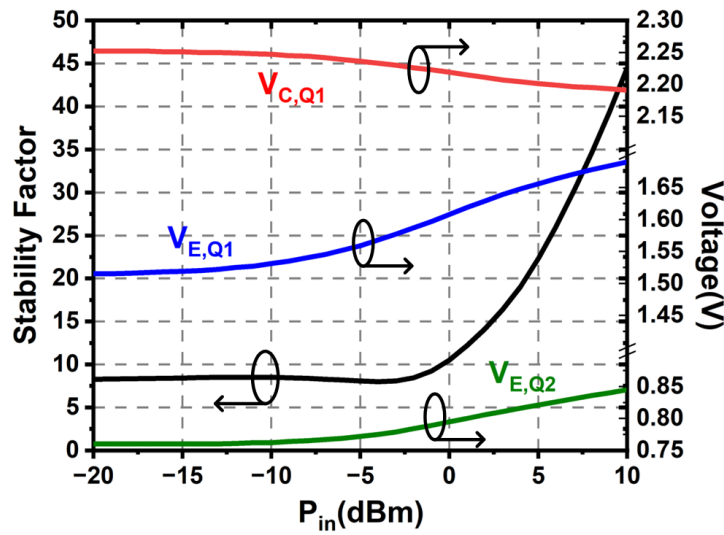


Figure 4.26: Stability factor of 3-stage 4-way-combined PA and voltages of adaptive bias circuit with sweep of input power.

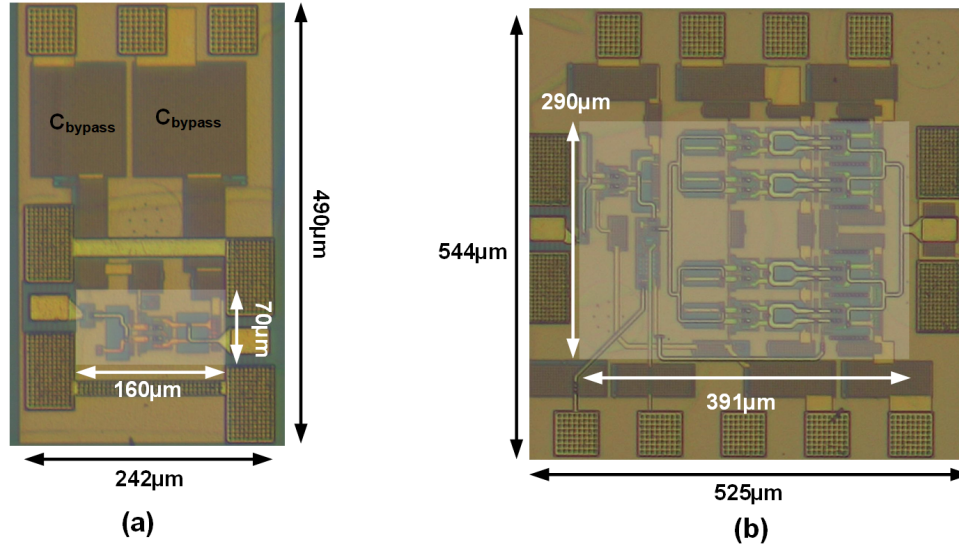


Figure 4.27: Micrograph of (a) Single-stage PA (b) 3-stage, 4-way-combined PA.

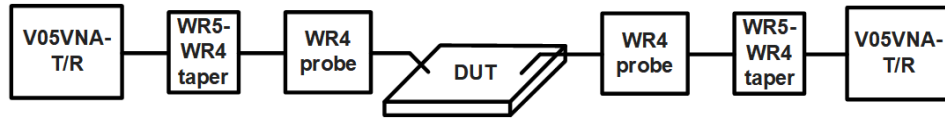


Figure 4.28: G-band S-parameter measurement.

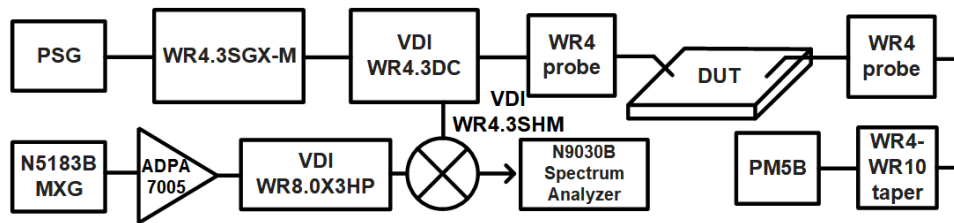


Figure 4.29: WR4.3 power measurement setup.

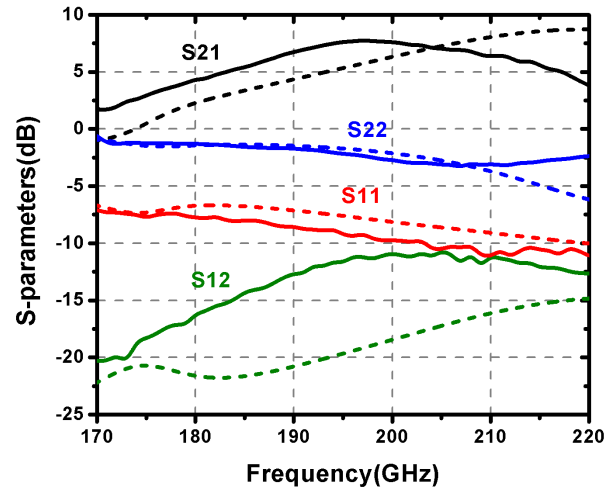


Figure 4.30: Measured (solid) and simulated (dashed) S-parameters of single-stage PA.

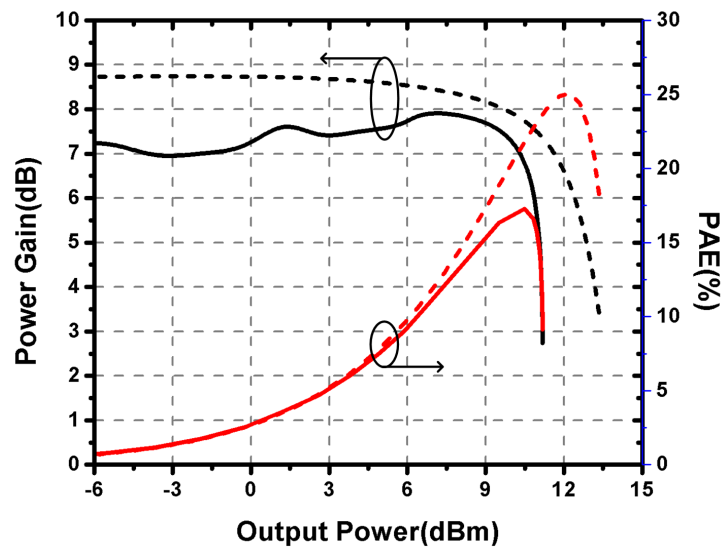


Figure 4.31: Power gain and PAE versus output power measured (solid) at 200 GHz and simulated (dashed) at 220 GHz of single-stage PA.

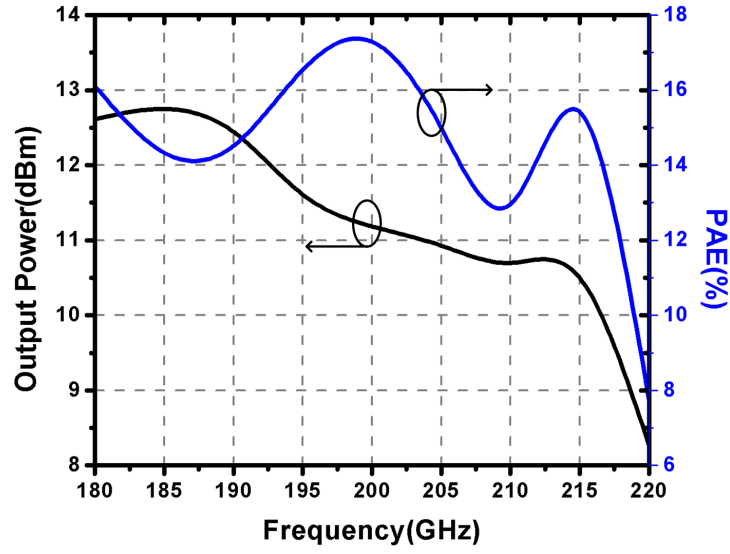


Figure 4.32: Measured P_{sat} and PAE over 180-220 GHz of single-stage PA.

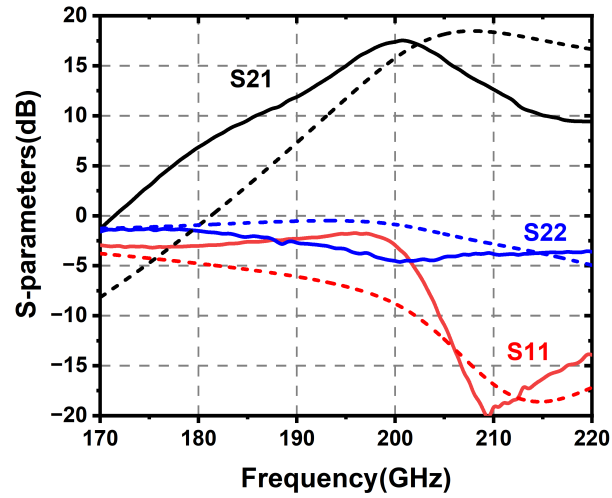


Figure 4.33: Measured (solid) and simulated (dashed) S-parameters of 3-stage, 4-way-combined PA.

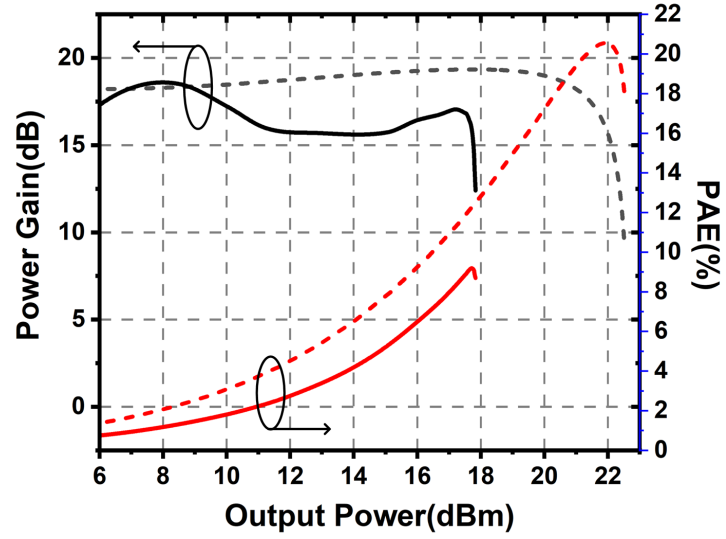


Figure 4.34: Power gain and PAE versus output power measured (solid) at 200 GHz and simulated (dashed) at 220 GHz of 3-stage, 4-way-combined PA.

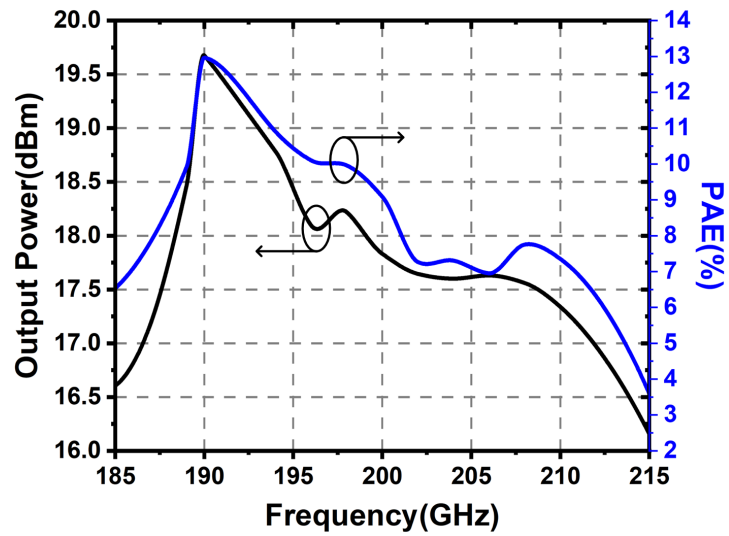


Figure 4.35: Measured P_{sat} and PAE over 180-220 GHz of 3-stage, 4-way-combined PA.

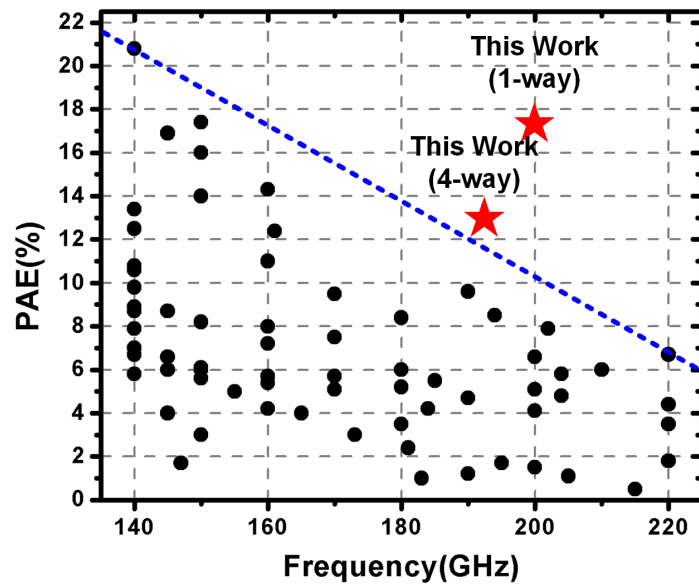


Figure 4.36: PAE comparison of published G-band PAs.

Chapter 5

D-band and G-band Switches Design in InP HBT

In Chapter 2, the trade-off of the conventional switches is discuss. To address the issue, reflective load topology is proposed in this dissertation. In the reflective-load termination, the transmission-line is replaced by a hybrid coupler in the SPDT shown in Fig. 5.1. The on-state IL is determined by loss of hybrid coupler and quality factor of reflective load while the off-state ISO is determined by balancing the magnitude and phase of the reflection across two independently tuned loads.

5.1 Operation of independent reflective load termination on hybrid coupler

The operation of the proposed switches is based on a hybrid coupler with two independent loads as shown in Fig. 5.2 and illustrates the signal flow across the two load impedances. The input of the hybrid coupler is the input of the switch while the isolation port of the coupler is the output port.

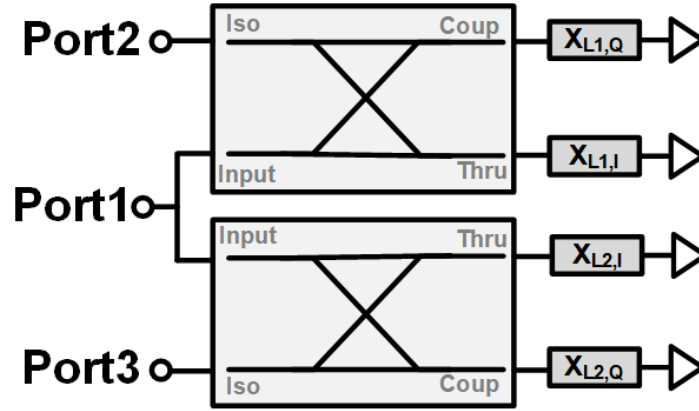


Figure 5.1: the proposed independent tuning reflective load SPDT.

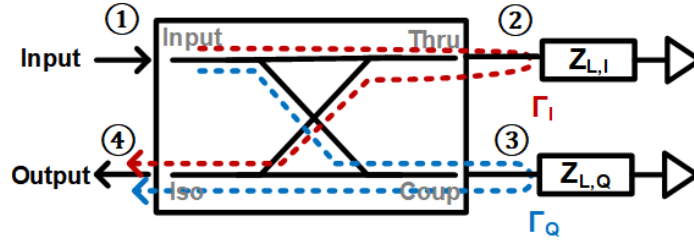


Figure 5.2: 90° hybrid coupler with two independent reflective loads.

The ideal scattering matrix of a 90° hybrid coupler is expressed as

$$S_{hybrid90^\circ} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & \alpha & -j\beta & 0 \\ \alpha & 0 & 0 & -j\beta \\ -j\beta & 0 & 0 & \alpha \\ 0 & -j\beta & \alpha & 0 \end{bmatrix} \quad (5.1)$$

where α and β are defined as transmission and coupling coefficients. The through port and coupled port are connected to $Z_{L,I}$ and $Z_{L,Q}$, respectively. The reflection coefficients from these two loads are defined as

$$\Gamma_I = \frac{Z_{L,I} - Z_0}{Z_{L,I} + Z_0}, \Gamma_Q = \frac{Z_{L,Q} - Z_0}{Z_{L,Q} + Z_0} \quad (5.2)$$

The two ports scattering matrix with two reflective loads could be determined with multiport network analysis [43]. Therefore, the action of the reflective load (RFL) is captured by cascading the 90° coupler, the reflective load, again, the 90° coupler. The transfer function from input and isolation ports is

$$S_{RFL} = \frac{1}{2} \begin{bmatrix} \alpha & -j\beta \\ -j\beta & \alpha \end{bmatrix} \begin{bmatrix} 1/\Gamma_I & 0 \\ 0 & 1/\Gamma_Q \end{bmatrix}^{-1} \begin{bmatrix} \alpha & -j\beta \\ -j\beta & \alpha \end{bmatrix} \quad (5.3)$$

Therefore, four S-parameters are given as

$$S_{11} = \frac{\Gamma_I \alpha^2 - \Gamma_Q \beta^2}{2}, S_{22} = \frac{\Gamma_Q \alpha^2 - \Gamma_I \beta^2}{2}, S_{12} = S_{21} = \frac{-j\alpha\beta(\Gamma_I + \Gamma_Q)}{2} \quad (5.4)$$

These expressions can be used to analyze the IL and ISO conditions.

If two reflective loads are equal, e.g., $Z_{L,I}=Z_{L,Q}$ and assuming 3-dB coupling, e.g., $\alpha=\beta$, the same reflection coefficient $\Gamma_I = \Gamma_Q$ is observed at the through and coupled ports, defining the on-state. Under these conditions, the input and output reflection conditions are zero and the IL of this operation derived from equation 5.4 could be expressed as

$$IL(dB) = -40\log(\alpha) - 20\log(|\Gamma_I|). \quad (5.5)$$

The minimum IL of the on-state switch is realized from both low hybrid coupler loss and low reflective loss for the load. Notably, the IL of coupler introduces twice the signal loss due to the round trip.

If $Z_{L,I}$ and $Z_{L,Q}$ are tuned differently, the out-of-phase impedance can be set between two reflective loads such that $|\Gamma_I| = |\Gamma_Q|$, but the phase between the loads differs by 180°, e.g. $\angle\Gamma_I = \angle\Gamma_Q \pm \pi$. From equation 5.4, $S_{21}=S_{12}=0$, defining the off-state condition.

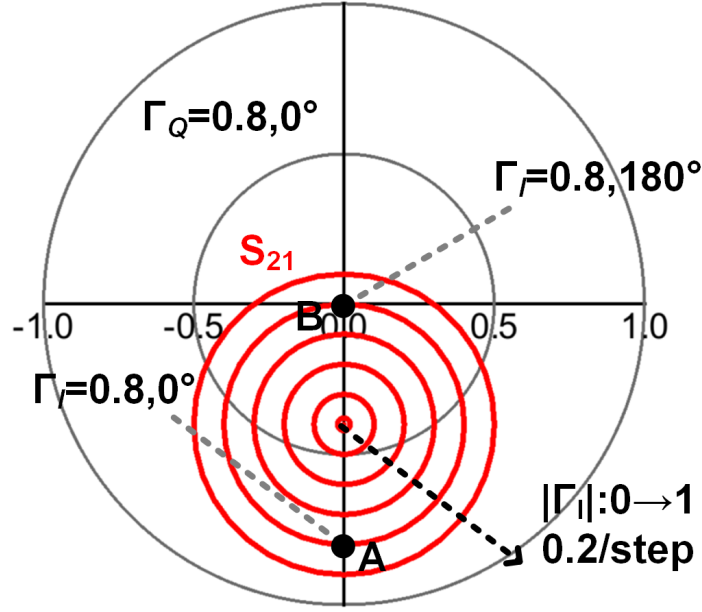


Figure 5.3: S_{21} contours with varying Γ_I and $\Gamma_Q=0.8\angle 0^\circ$.

Again enforcing $\alpha=\beta$, the input and output reflection coefficients become

$$S_{11} = \alpha^2 \Gamma_I, S_{22} = -\alpha^2 \Gamma_I. \quad (5.6)$$

The input and output impedance would be out-of-phase and relevant to two reflective loads. This is an important characteristic for building SPDT where high impedance is needed to present at the input of off-state path.

Simulation of a lossless ideal 3-dB hybrid coupler ($\alpha=\beta=1$) with tuners on through and coupled ports is shown in Fig. 5.3-5.6. In Fig. 5.3 and Fig. 5.4, $\Gamma_Q=0.8\angle 0^\circ$ and Γ_I is varying both magnitude and phase. The S_{21} contour on a polar chart is shown in Fig. 5.3. Point A shows the on-state where $\Gamma_I=\Gamma_Q$ and point B shows the off-state from two out-of-phase reflective load with same magnitude.

Ideal isolation will be limited by the matching between the coupler parameters as well as the magnitude and phase mismatch between Γ_I and Γ_Q . S_{11} and S_{22} contours on

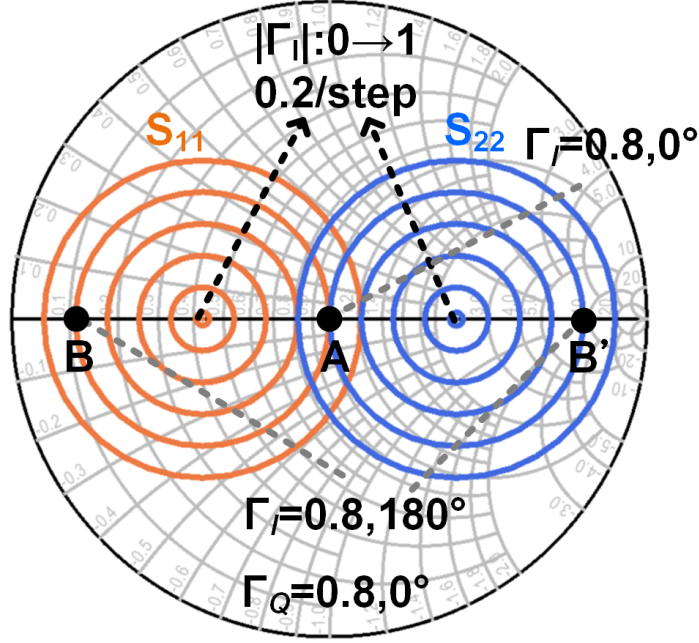
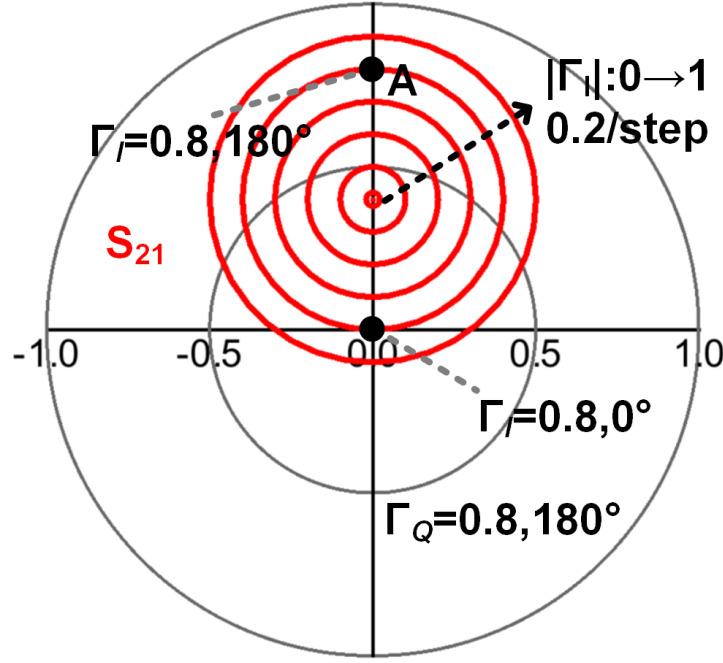


Figure 5.4: S_{11} and S_{22} contours with varying Γ_I and $\Gamma_Q=0.8\angle 0^\circ$.

Smith Chart are shown in Fig. 5.4. Point A is matched to 50Ω for both S_{11} and S_{22} and all the signal power in the on-state is delivered to the load. Point B and B' illustrates low impedance and high impedance for S_{11} and S_{22} , respectively. The results match with the analysis in equation 6.1. Fig. 5.5 and Fig. 5.6 show the contours under $\Gamma_Q = 0.8\angle 180^\circ$ and Γ_I is varying both magnitude and phase. The on-state IL is the same but with 180° phase shift while S_{11} and S_{22} impedances are swapped.

Including loss of the hybrid, e.g. $\alpha=\beta < 1$, the contours of $|\Gamma_I|=|\Gamma_Q|$ with varying phase of Γ_I and loss of hybrid coupler are shown in Fig. 5.7 and 5.8. The IL of the on-state switch increases with the loss of hybrid coupler which is observed in Fig. 5.7 and consistent with 5.5 while the off-state ISO is irrelevant to the loss of hybrid coupler. The loss of hybrid coupler also impacts the reachable impedance of S_{11} and S_{22} in the off-state as shown in Fig. 5.8, which will contribute to higher loading effect in SPDT design.

Figure 5.5: S_{21} contours with varying Γ_I and $\Gamma_Q=0.8\angle 180^\circ$.

5.2 Circuit implementation

As described in equation 5.4 and 5.5, the minimum IL of the hybrid coupler defined by α and β . In [44], a coupled-line based hybrid coupler shows extremely low loss at mm-wave band while occupying a limited area. The design targets are set by coupling factor $C = 10^{\frac{-3}{20}} = 0.708$, odd-mode impedance $Z_{0o} = 50 \cdot \sqrt{\frac{1-0.708}{1+0.708}} = 20.7\Omega$ and even-mode impedance $Z_{0e} = 50 \cdot \sqrt{\frac{1+0.708}{1-0.708}} = 121\Omega$. The simulated performance of D-band and G-band coupled-line based hybrid coupler in InP is plotted in Fig. 5.9 and Fig. 5.10. For the D-band design, the IL from input port to through and coupled ports are 0.15-dB while the phase error between them is 0.4 degree and 28-dB isolation at 110 GHz. For the G-band design, the IL from input port to through and coupled ports are 0.13-dB while the phase error between them is 1 degree and 27.3-dB isolation at 220 GHz. Notably, the area required for the coupler in Fig. 5.9 and Fig. 5.10 is only 0.011 mm^2 and 0.005 mm^2 . Consequently, the implementation of the coupler is attractive compared

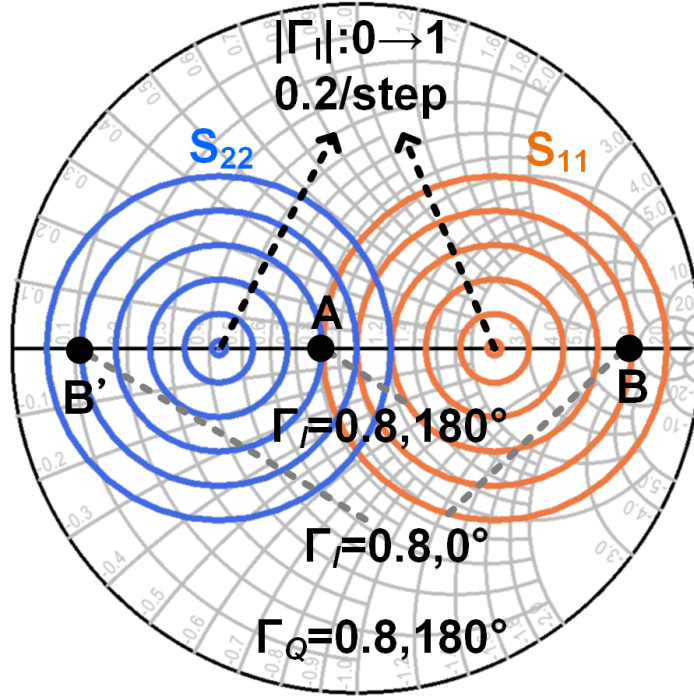
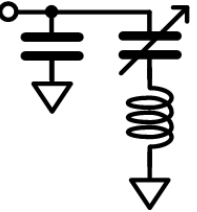


Figure 5.6: S_{11} and S_{22} contours with varying Γ_I and $\Gamma_Q=0.8\angle 180^\circ$.

to a quarter-wave transmission line used in the conventional SPDT in terms of both the loss and the area.

Table 5.1: Phase Range of Reflective Loads

Type of reflective load	Capacitive Load	L-C Resonant Load	C-L-C Resonant Load
Schematic			
Phase Range	$< 90^\circ$	$< 150^\circ$	$< 270^\circ$

The IL of on-state switch described in equation 5.5 not only depends on low-loss hybrid coupler but also high-Q reflective load. Commonly used reflective load designs are capacitive load, series L-C resonant load, parallel L-C resonant load and C-L-C resonant load [45][46]. The first three designs could not reach the phase range needed, that is,

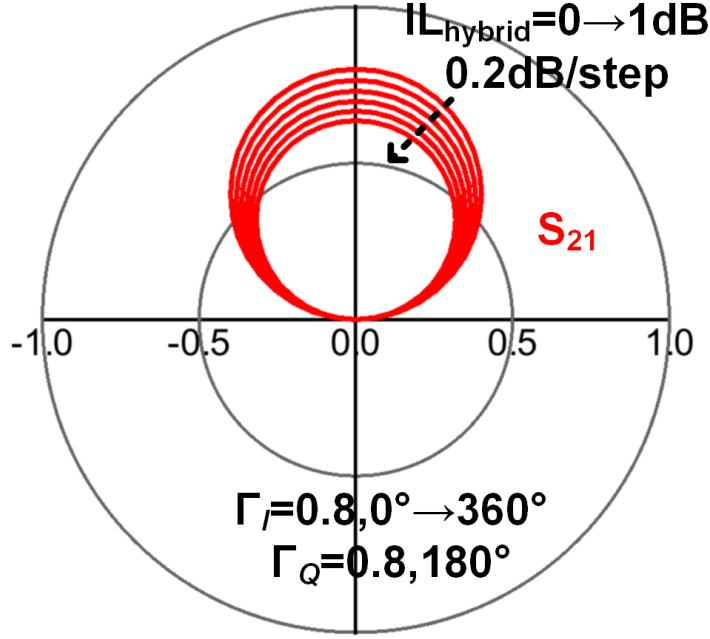


Figure 5.7: S_{21} contours with varying phase of Γ_I and loss of hybrid coupler.

180° for out-of-phase on the through and coupled ports and therefore we chose C-L-C resonant load as summarized in Table 5.1. Some other reflective load designs can reach 360° phase range which will provide more phase combination for better ISO. However, this will have to trade with IL. Here, the phase range is only slightly over-designed so that IL could be minimized.

The schematic of the proposed SPST is shown in Fig. 5.11. The first fixed capacitance comes from the parasitic capacitance of the routing and the second tunable capacitance is the diode connected HBT Q_I and Q_Q . We compare the base-emitter (BE) and base-collector (BC) diode behavior in terms of a tunable reactive element in Fig. 5.12. Notably, the BC diode is selected based on the higher $C_{\max}/C_{\min}$ ratio as illustrated in Fig. 5.12. The simulation indicates that the $C_{\max}/C_{\min}$ ratio for a 4- μm emitter length diode-connected HBT is 8 and maximum quality factor (Q) of 57 to minimum Q of 6 at 110 GHz as the collector voltage varies from 0.5 V to -0.5 V. Both the capacitance ratio and Q

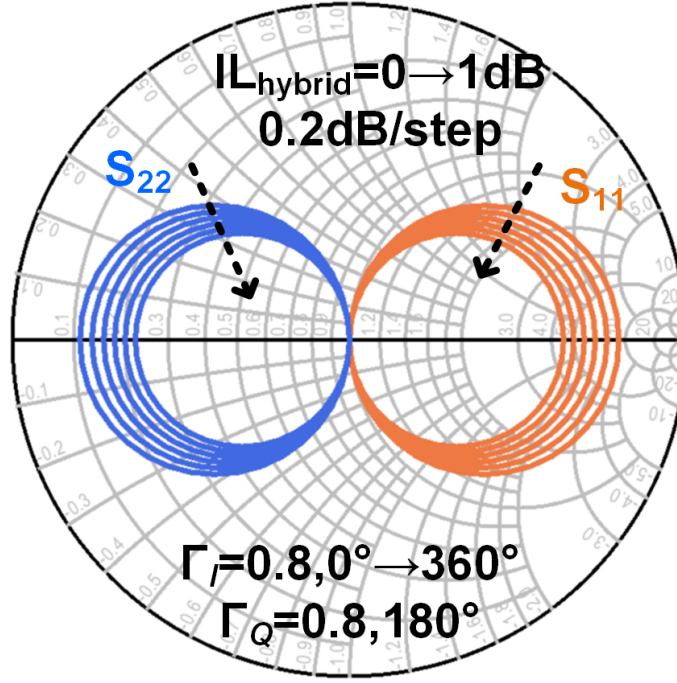


Figure 5.8: S_{11} and S_{22} contours with varying phase of Γ_I and loss of hybrid coupler.

for the BE diode is significantly smaller, making it impractical for the reflective load. A 2- μm emitter length BC diode-connected HBT is used in G-band design with C_{max}/C_{min} ratio of 5.8, maximum Q of 25 and minimum Q of 4.5 at 220 GHz. The C_{max}/C_{min} ratio and maximum Q of InP HBT at D- and G-band are both superior to those of SiGe HBT or SOI CMOS process, which do not offer as much capacitance variation at these bands.

In Fig. 5.13(a), the on-state S-parameters trajectories are plotted for the tunable reactance. We chose the impedance where the star is located to obtain the highest $\Gamma_{I(Q)}$ and, therefore, the lowest IL is realized. As described in Section 5.1, an important characteristic of the proposed SPST switch is the input and output impedance vary with different tuning voltage in the off-state as shown in Fig. 5.13(b)(c). In Fig. 5.13(b), when $V_{tune,I} = 0.5V$ and $V_{tune,Q} = -0.5V$, S_{11} shows low impedance while S_{22} shows high impedance. This indicates Port 2 in Fig. 5.11 is suitable for the common node in SPDT in this case. In Fig. 5.13(c), the similar trend could be observed, and the high

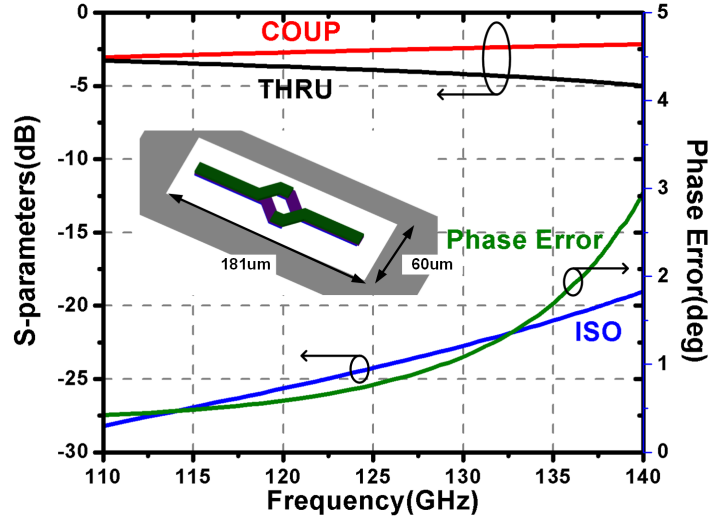


Figure 5.9: Simulated amplitude of 3 ports respect to input port in D-band hybrid coupler and the phase error between through and coupled ports.

Table 5.2: Design Parameters of SPSTs
D-band SPST

Q_I	Q_Q	L_I	L_Q	C_{bypass}	R_b
$4\mu\text{m}$	$4\mu\text{m}$	61.7pH	61.7pH	960fF	$1\text{k}\Omega$

G-band SPST

Q_I	Q_Q	L_I	L_Q	C_{bypass}	R_b
$2\mu\text{m}$	$2\mu\text{m}$	53.8pH	53.8pH	600fF	$1\text{k}\Omega$

impedance node is switched to Port 1 in Fig. 5.11. The design parameters of D- and G-band SPSTs are summarized in Table 5.2.

The SPDT is formed by merging two SPST described in Fig. 5.11 as shown in Fig. 5.14. For testing and characterization, one port of two inputs is directly connected to an on-chip 50-ohm termination at D-band and G-band. The varactors bias conditions are summarized in Table 5.3 and the design parameters are the same with SPST designs shown in Table 5.2.

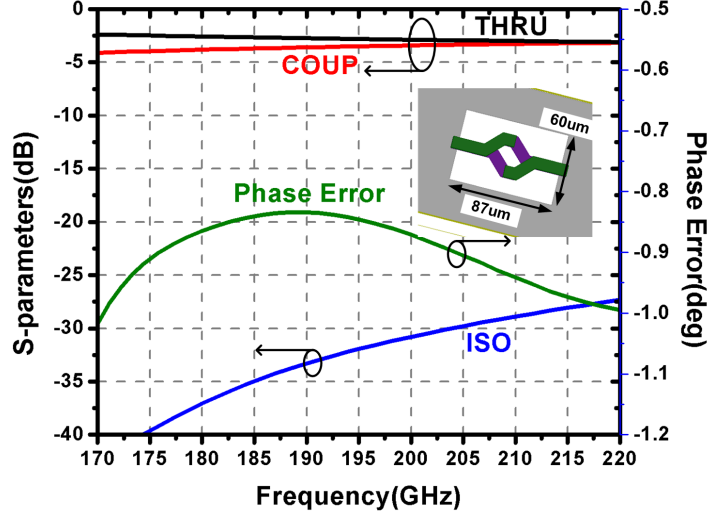


Figure 5.10: Simulated amplitude of 3 ports respect to input port in G-band hybrid coupler and the phase error between through and coupled ports.

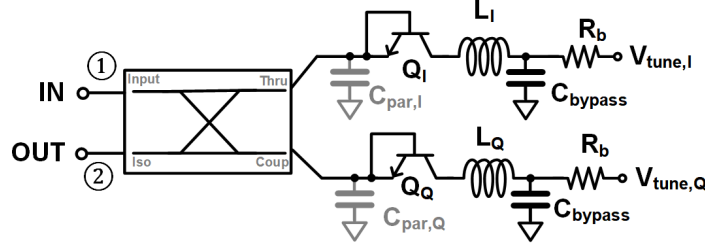


Figure 5.11: Schematic of the proposed SPST switch.

5.3 Simulation and measurement results

The proposed SPST and SPDT prototypes are fabricated in the Teledyne 250-nm InP HBT process and measured with VDI D-band and OML G-band frequency extender. WR-6 probes and WR-4 probes with WR4-to-WR5 waveguide tapers are used for probing the chips. Calibration is done using CS-15 calibration substrate for calibrating to probe

Table 5.3: Operation of SPDT Switch

	Bias condition in SW1	Bias condition in SW1
IN1 to OUT	$V_{tune,I1} = V_{tune,Q1}$	$V_{tune,I2} > V_{tune,Q2}$
IN2 to OUT	$V_{tune,I1} > V_{tune,Q1}$	$V_{tune,I2} = V_{tune,Q2}$

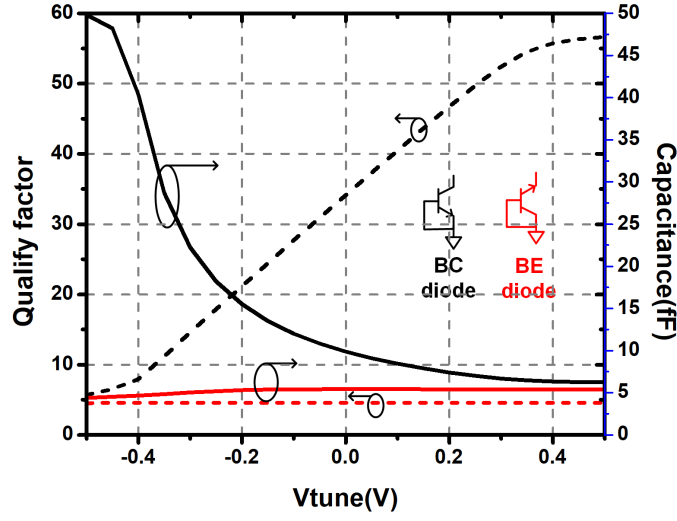


Figure 5.12: Simulated capacitance and quality factor of different diode versus bias voltage at 110 GHz.

tips. Fig. 5.15 shows the photographs of implemented D-band SPST and SPDT switches with core size of 0.048 mm^2 and 0.094 mm^2 , respectively. The fabricated G-band SPST and SPDT switches with core size of 0.046 mm^2 and 0.049 mm^2 , respectively.

The simulated and measured tuning range for the on-state SPST and SPDT switches at 110 GHz is shown in Fig. 5.16 and Fig. 5.17. The phase range measured at 110 GHz for SPST and SPDT are 216° and 232° , respectively. The on-state bias is chosen with minimum IL under $V_{tune}=0.6\text{V}$ in both cases where it shows IL of 0.77 dB for SPST and IL of 1.42 dB for SPDT at 110 GHz. S_{11} and S_{22} are all better than -8 dB under the selected bias condition for both designs. Discrepancy between simulation and measurement in negative bias region is due to the inaccurate modeling on the quality factor of BC diode biased close to turn-on voltage. From the plot, the off-state bias condition was also observed to find the best tuning positions. $V_{tune,I}=-0.42\text{V}$ and $V_{tune,Q}=-1\text{V}$ are selected for the off-state to have comparable loss from two reflective load while having 180° phase difference to achieve highest isolation.

In Fig. 5.18, IL of SPST switch measured results is between 0.77dB and 2.7dB across

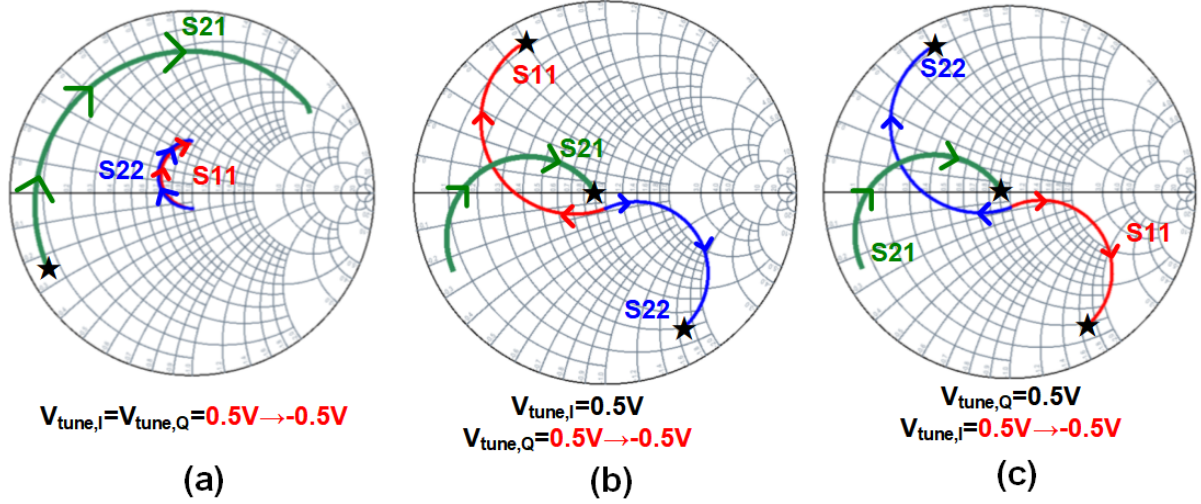


Figure 5.13: Simulated S_{11} , S_{22} and S_{21} trajectories with different tuning voltage sweeping for the tunable reactance at 110 GHz.

the 110-140 GHz measurement and IL of SPDT switch is between 1.42 dB and 3.8 dB up to 132 GHz. The minimum loss was found across a sweep of the on-state bias. The ISO of the SPST switch was better than 23 dB across the entire 110-140 GHz range while the ISO of the SPDT switch was below 35 dB and nominally around 40 dB. Large signal measurements of SPST and SPDT are also performed as shown in Fig. 5.19. The SPST demonstrates 1-dB power compression (P1dB) at 7.5 dBm. Insufficient power from the VDI frequency extender was available to drive the SPDT into compression but the measurement indicates a similar P1dB.

Due to the calibration limitation, the measured results only show 190 GHz to 220 GHz of G-band prototypes in this dissertation. The simulated and measured IL with $V_{tune,I}$ and $V_{tune,Q}$ from -1 V to 0.8 V with 0.1 V/step are conducted for G-band SPST. The minimum loss bias conditions with $V_{tune,I} = V_{tune,Q} = 0.5V$ is selected as shown in Fig. 5.20. Therefore, the on-state IL from 190 GHz to 220 GHz ranging from 1.7dB to 3.1dB. Fig. 5.21 shows the simulated (blue dashed line) and measured (black solid line) phase shift with $V_{tune,I}$ and $V_{tune,Q}$ under 0.8V, -0.3V and -1V for G-band SPST. Simulated

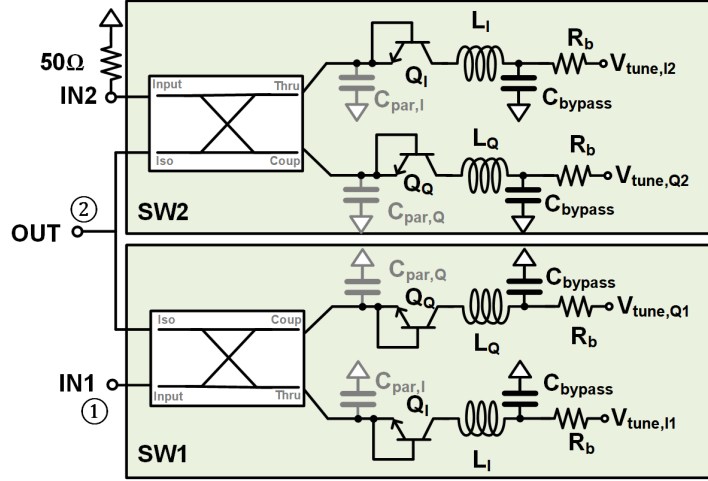


Figure 5.14: Schematic of the proposed SPDT switch.

and measured phase ranges based on the sweep are also plotted in dotted and solid red lines, respectively. The measured phase range varies from 225° to 232° from 190 GHz to 220 GHz. The off-state ISO is measured based on the results from Fig. 5.20 and Fig. 5.21.

With multiple bias conditions optimized for different frequencies, the maximum achievable ISO across 190 GHz to 220 GHz are 27.4dB to 42dB plotted in solid red line in Fig. 5.22.

A similar measurement approach is applied to G-band SPDT. The on-state IL and phase range is measured as shown in Fig. 5.23 and Fig. 5.24 with the other path biased in off-state. The measured on-state IL is between 2.3dB and 5.8dB while the phase range is from 213° to 224° across 190 GHz to 220 GHz. The off-state composite ISO with multiple bias conditions is measured with 25.3dB to 31dB in 190-220 GHz as shown in Fig. 5.25.

The IL and ISO survey of D-band and G-band SPDT switches are also plotted in Fig. 5.26 and Fig. 5.27. It is worth mentioning the D-band SPDT switch shows the highest FOM among all D-band SPDT without post processing.

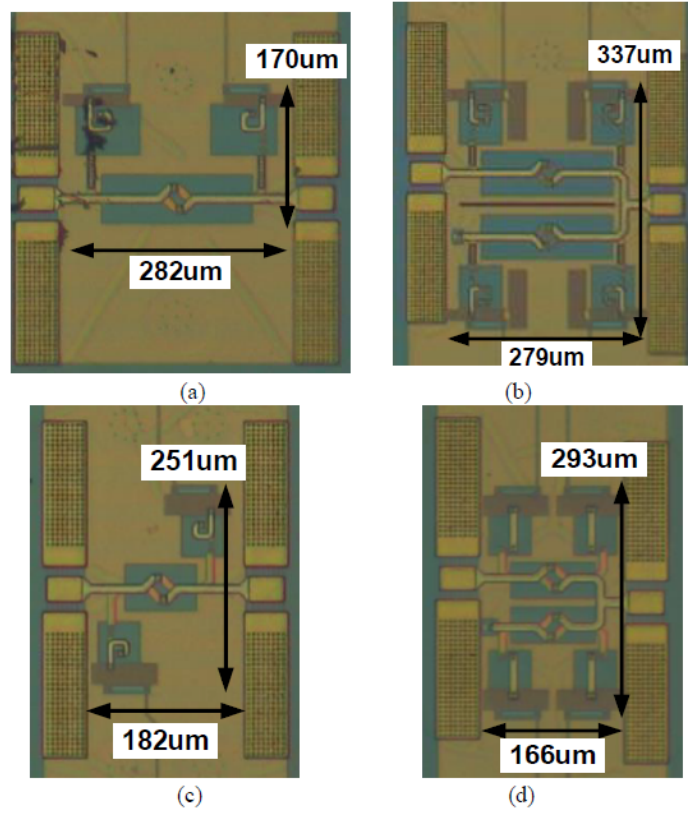


Figure 5.15: Micrograph of (a) D-band SPST switch (b) D-band SPDT switch (c) G-band SPST switch (d) G-band SPDT switch.

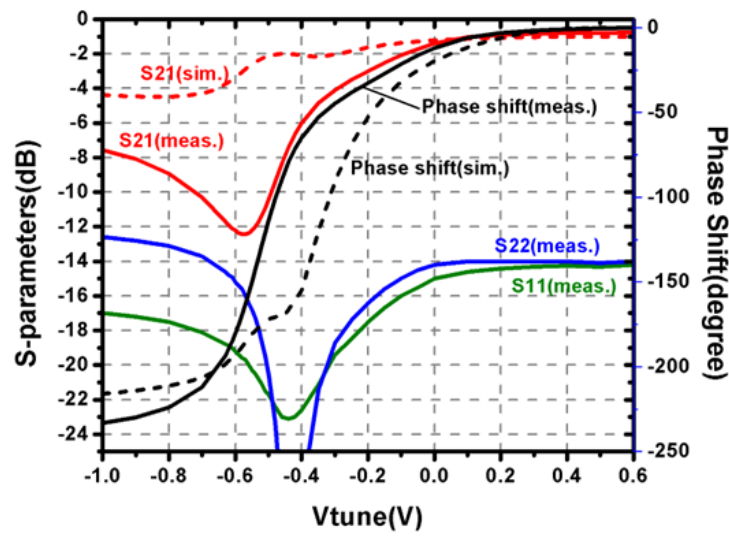


Figure 5.16: Simulated (dash) and measured (solid) S-parameters and phase shift of SPST in on-state at 110GHz.

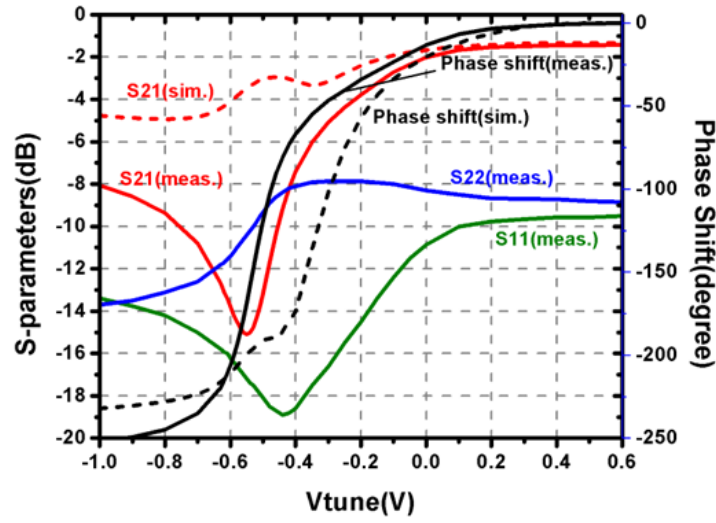


Figure 5.17: Simulated (dash) and measured (solid) S-parameters and phase shift of SPDT in on-state at 110GHz.

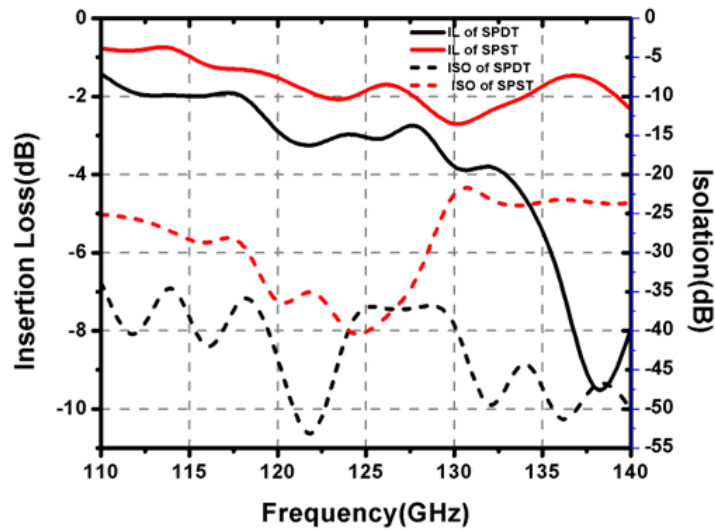


Figure 5.18: IL (solid) and Isolation (dash) of SPST and SPDT switches in 110-140 GHz.

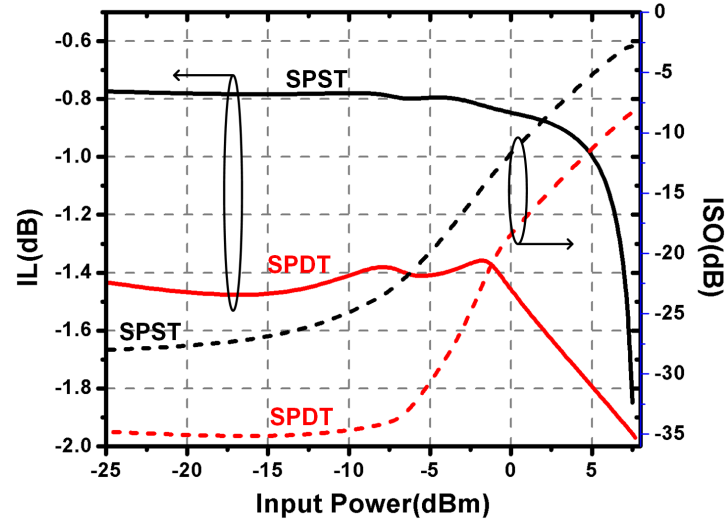


Figure 5.19: IL (solid) and ISO (dashed) of SPST and SPDT with input power sweep at 110 GHz.

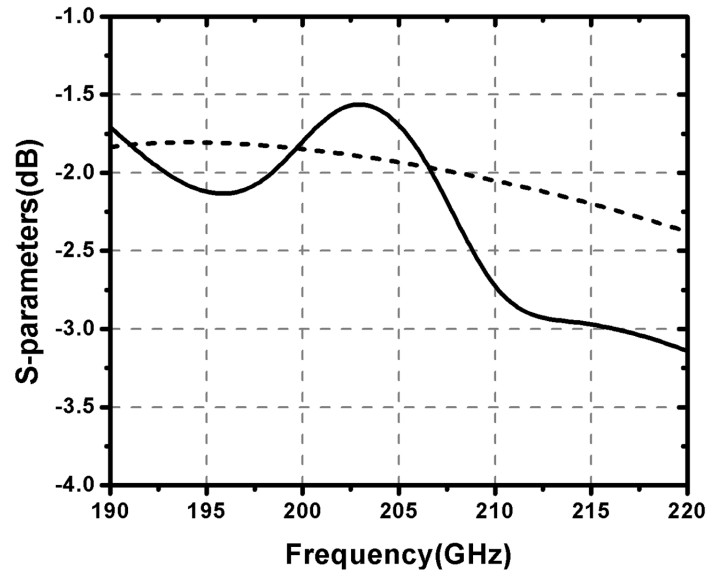


Figure 5.20: Simulated (dashed) and measured (solid) of IL of on-state G-band SPST under 0.5V varactor bias across 190-220 GHz.

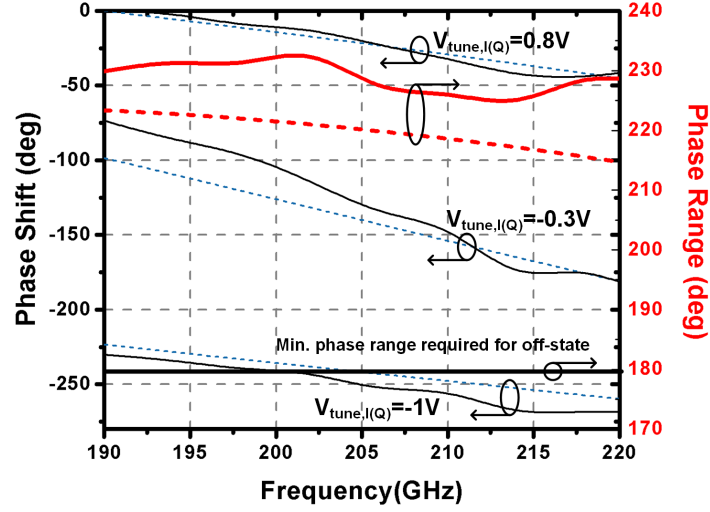


Figure 5.21: Simulated (dashed) and measured (solid) of phase shift and phase range of on-state G-band SPST under different varactor bias voltage across 190-220 GHz.

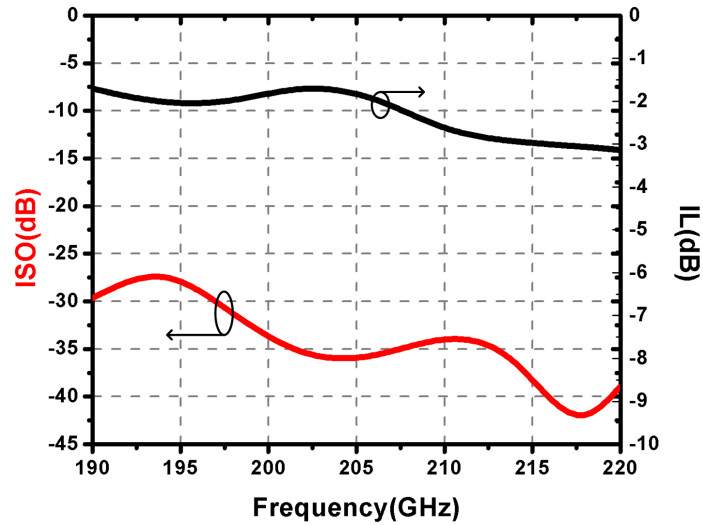


Figure 5.22: Composite ISO of off-state G-band SPST across 190-220 GHz under different bias conditions and IL of on-state G-band SPST.

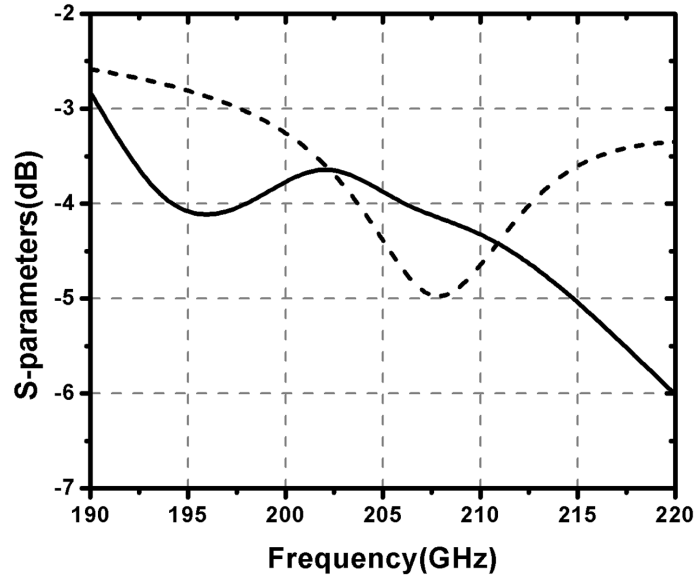


Figure 5.23: Simulated (dashed) and measured (solid) of IL of on-state G-band SPDT under 0.8V varactor bias across 190-220 GHz.

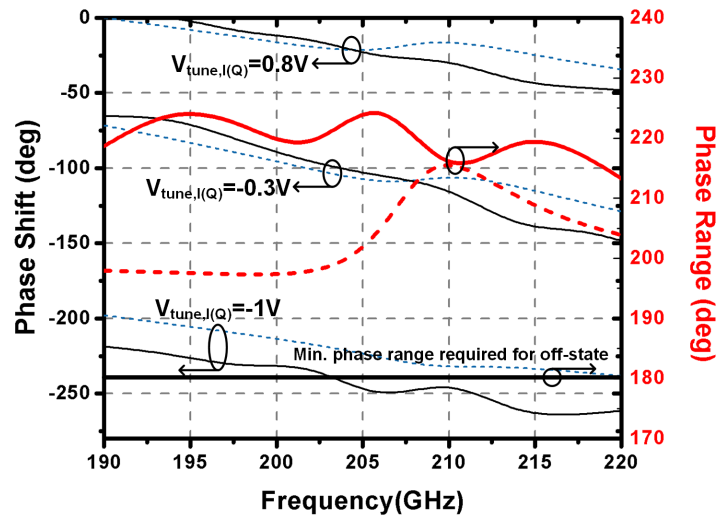


Figure 5.24: Simulated (dashed) and measured (solid) of phase shift and phase range of on-state G-band SPDT under different varactor bias voltage across 190-220 GHz.

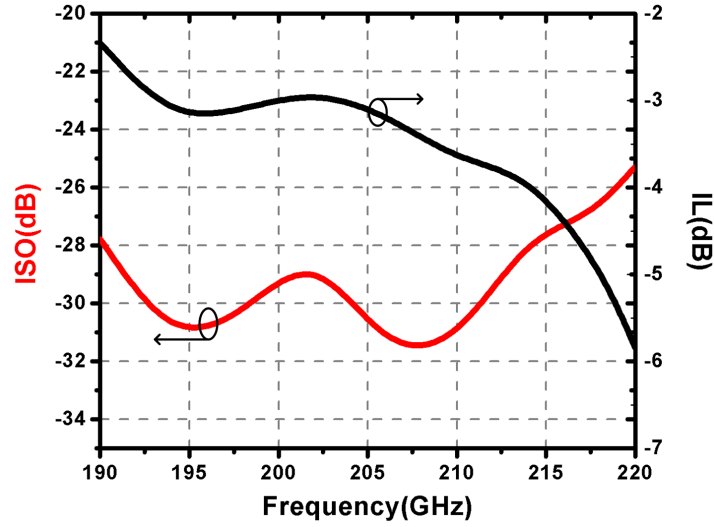


Figure 5.25: Composite ISO of off-state G-band SPDT across 190-220 GHz under different bias conditions and IL of on-state G-band SPDT.

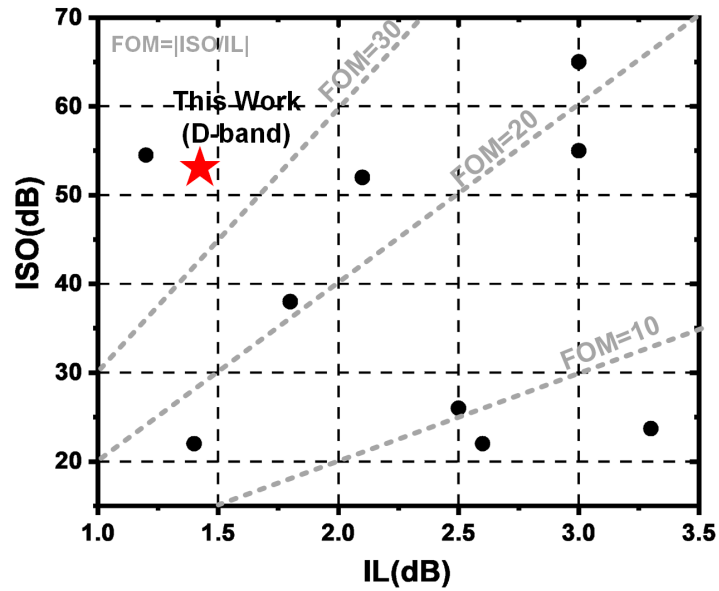


Figure 5.26: Performance survey of state-of-the-art D-band SPDT switches.

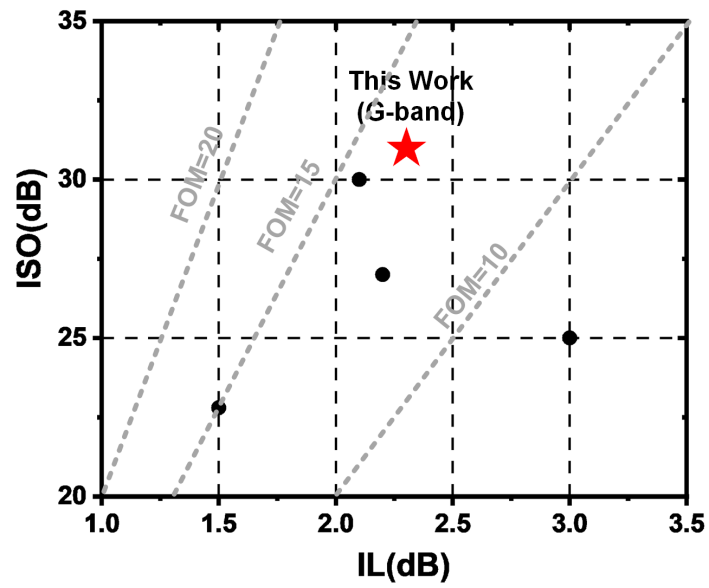


Figure 5.27: Performance survey of state-of-the-art G-band SPDT switches.

Chapter 6

D-band Outphasing Transmitter in 22-nm FDSOI CMOS

6.1 Efficiency of Sub-THz transmitters

As mentioned in Chapter 1, there are two significant problems to designing arrays of transmitters above 100 GHz. Firstly, the half-wavelength spacing between elements is only 1.25 mm at 120 GHz and, therefore, the entire transmitter (TX) must fit into an area of 1.56 mm-sq. Additionally, the dense packing of TXs demands high efficiency to avoid high temperature rise in the TX array. Earlier work has proposed TX architectures based on conventional IQ direct conversion, shown in Fig. 2.1, which limits the highest achievable transmitter efficiency as well as requires significant area. Although the overall efficiency could be enhanced by designing a high efficiency and high gain power amplifier (PA), the tradeoff between efficiency and bandwidth becomes severe due to lower G_{max} in D-band. In [6] and [7], direct conversion transmitter with multiplier chains are realized with 1% efficiency. The LO multiplier occupies 69% of overall power consumption in [6] while multiplier in [7] occupies 28.4% of overall power consumption due to a lower

Technology	RFIC'14 65nm CMOS	TMTT'16 250nm InP	RFIC'18 40nm CMOS	RFIC'19 22 FDSOI	JSSC'19 180nm SiGe	ISSCC'22 22nm Finfet	ISSCC'22 130nm SiGe
Topology	Two step up-conversion using 80GHz LO	Direct conversion with x3 multiplier	Direct conversion with x3 multiplier chain	Direct conversion with x9 multiplier chain	Direct conversion with x6 multiplier chain	RF-DAC with PLL and x3 multiplier	Phase shifter with VGA and PA
Carrier Frequency (GHz)	100-118	144	118	135	115	140	130-164
Data Rate(Gbps)	20.6	48	-	-	20	160	30
Modulation	BPSK/QPSK	16QAM/32QAM/ 64QAM	-	-	16QAM	QPSK/16QAM	64QAM/256QAM
Output Power(dBm)	-3	9	4.5	2.8	1	0.8	12
Chip Area(mm ²)	0.21	1.17	1.51	1.44	3.17	0.75	0.9
DC Power (mW)	280	165 (Multiplier+ Modulator+PA= 53+40.6+71.4)	271	196	520	173.5	265
LO power consumption/ Total power Consumption(%)	-	32	28.4	69	40	46	-
Peak DC-to-RF Efficiency(%)	0.18	4.81	1	0.97	0.24	0.7	6

Table 6.1: Performance comparison of published D-band transmitter

multiplication ratio and higher LO input power requirement. The I/Q mixer demands significant multiplier output power and places a bottleneck on the overall efficiency. More publications on D-band transmitter designs are summarized in Table. 6.1.

6.2 Multiplying outphasing modulator

To break the limitation of conventional direct conversion topology, a millimeter-wave outphasing modulator that eliminates the mixers, and 90° hybrid as a pathway to a more linear modulator is proposed. In [47], a multiplying outphasing transmitter (MOT) was demonstrated with high efficiency and linearity. In this dissertation, a MOT based on a reflection-type phase shifter (RTPS) is proposed.

Fig. 6.1 shows the demonstration of multiplying outphasing modulation with two input signals S1 and S2 at 20 GHz that are decomposed to a common phase θ and outphasing angle ϕ . The first case with red arrow showing $\theta=37.5^\circ$ and $\phi=0^\circ$. Two identical input signals are combined in phase at 120GHz and produce a 225° phase shift after 6-fold multiplication. The second case shows the blue arrow with $\theta=7.5^\circ$ and $\phi=7.5^\circ$. The two signals after being multiplied six-fold will be 90 degree out of phase and therefore the combined signal at 120 GHz will be 45 degree on the constellation and with smaller

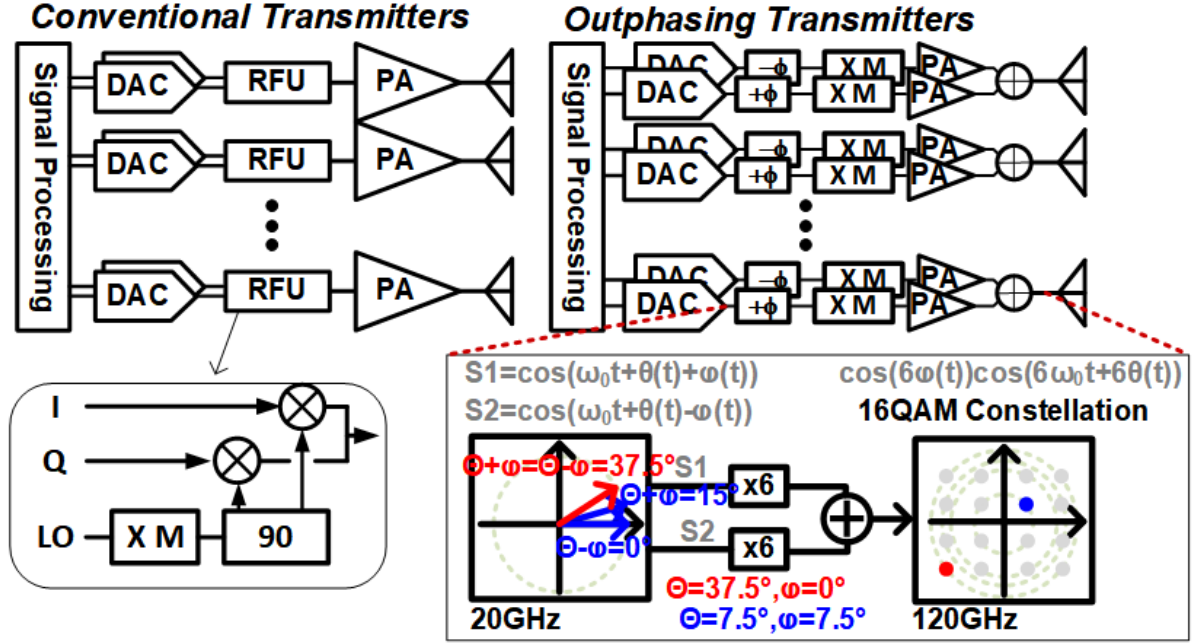


Figure 6.1: Comparison of millimeter-wave modulator approaches for arrays above 100 GHz.

output power compared to the first case. Therefore, the output signal generated by the MOT could be expressed as

$$V_{out}(t) = \cos(6\phi(t))\cos(6\omega_0 t + 6\theta(t)). \quad (6.1)$$

where $0 \leq \phi \leq \pi/12$, $0 \leq \theta \leq \pi/3$. The first implementation (MOT-1) of the MOT uses a single phase modulated 20 GHz input that is split through a Wilkinson power splitter and a single to differential (S2D) amplifier to provide isolation between two paths. The differential RTPS introduces the outphasing modulation on the two paths. Next, a frequency tripler converts the signal to 60 GHz, where it is amplified, and driven to frequency doubler to produce a 120 GHz modulated waveform. A three stage 120 GHz PA amplifies the signals on both paths and the signals are combined in a lumped-element Wilkinson power combiner for isolation. An isolated combiner is not typically used in outphasing modulators but we identify here the power and area savings of eliminating the

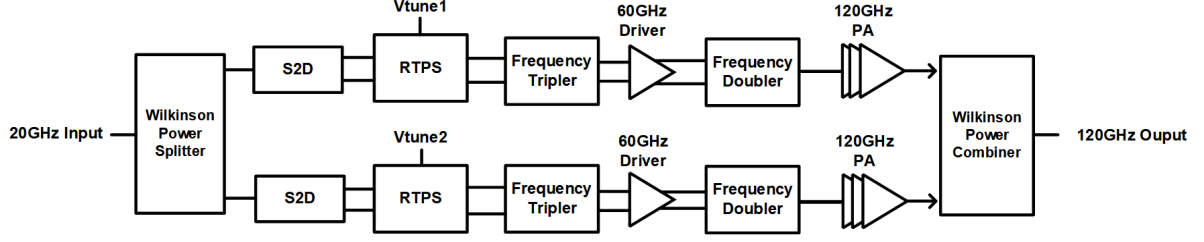


Figure 6.2: Block diagram of MOT-1.

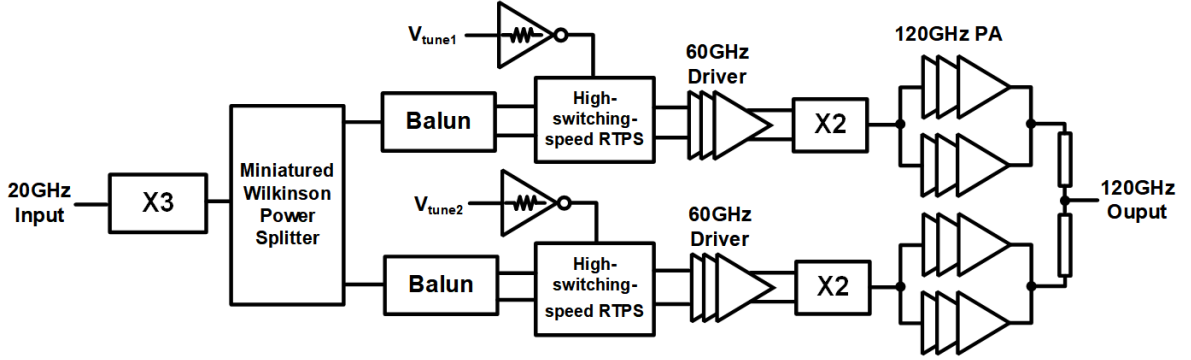


Figure 6.3: Block diagram of MOT-2.

I/Q mixers rather than the benefits of load modulation on the PAs. The block diagram of MOT-1 is shown in Fig. 6.2

However, the efficiency is limited due to the low gain and low efficiency frequency doubler as well as similar power level between 60-GHz driver and 120-GHz PA in MOT-1. Also, the minimum area is constrained by multiple 20-GHz building blocks. This limitation throttles the available link bandwidth. Additionally, the small pitch for D-band phased arrays (1-mm spacing) demands compact circuits.

In the second prototype MOT-2, three significant improvements are made that achieve a record DC-to-RF efficiency and power density for a D-band transmitter. First, the 20 GHz circuits are eliminated for smaller area. Second, the 60-to-120 GHz frequency doubler performance is improved with a harmonic reflector. Third, a higher output power 120 GHz PA is designed with improved PAE. The block diagram of MOT-2 is shown in Fig. 6.3.

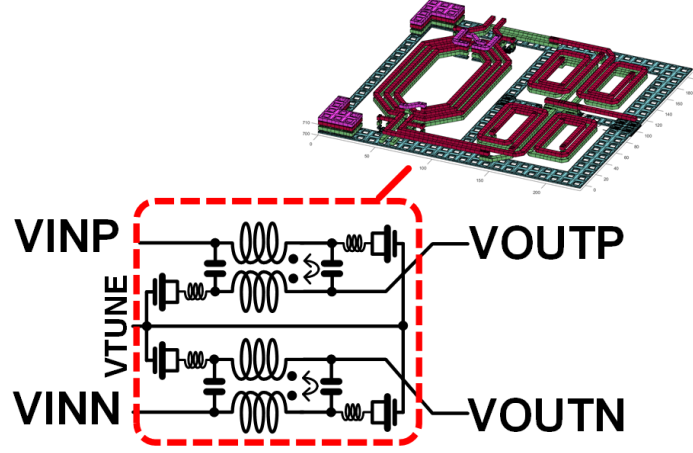


Figure 6.4: Schematic and layout of 20-GHz high-switching-speed differential RTPS.

A 20 GHz input LO is multiplied with tuned frequency tripler to 60 GHz. An eight-shape inductor based miniaturized Wilkinson power divider is designed to provide isolation between two paths. While earlier work used a phase modulator at 20 GHz, this was found to impose a significant bandwidth limitation on the modulation rate due to the bandwidth expansion from 20 to 120-GHz. A differential RTPS at 60-GHz is designed to enable the high-speed phase modulation at 120-GHz. To ensure sufficient input power to the frequency doubler, a three-stage, 60-GHz driver amplifier is inserted. Following the frequency doubler, a 14-dBm, 120-GHz PA is combined through a non-isolated combiner.

6.3 High-speed phase shifter design

In MOT-1, the phase range required at 20 GHz for outphasing modulation is around 30° . Also, high speed phase control is required modulation and earlier work in [48] controlled the Miller capacitance and inductance in a coupled transmission line to achieve 1GHz bandwidth. With small range and higher resolution needed, differential RTPS with C-L loading is proposed as shown in the red box in Fig. 6.4. The hybrid coupler based on a stacked transformer is designed to prevent the large size branch line coupler at

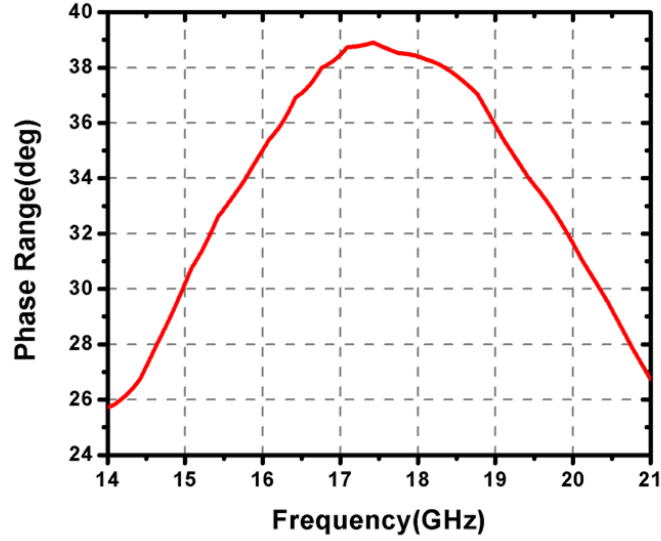


Figure 6.5: Measured phase range of 20-GHz high-switching-speed differential RTPS.

20 GHz where V_{tune} controls an NMOS-based varactor. The RTPS occupies 0.05 mm^2 . Measurements of the standalone indicate a phase range larger than 30° over frequency range of 15-20.3 GHz as shown in Fig. 6.5. The gain variation is around 2 dB while S_{11} and S_{22} are under -10 dB.

In MOT-2, a 60-GHz differential RTPS using an L-C resonant load is proposed in Fig. 6.6. The simulated phase range is plotted in Fig. 6.7, where it shows greater than 90° phase range across 40 GHz bandwidth. Also, the gain varies from -4.3 to -11 dB across different phase settings at 60-GHz. An inverter buffer with resistive feedback provides wideband impedance matching to ensure sufficient bandwidth to drive the varactors. With a $50\text{-}\Omega$ input, the buffer offers a 16.6 GHz 3-dB bandwidth in Fig. 6.8.

6.4 Other building blocks

There are several building blocks are overlapped between MOT-1 and MOT-2 including frequency tripler, frequency doubler, wilkinson power splitter, 60-GHz driver

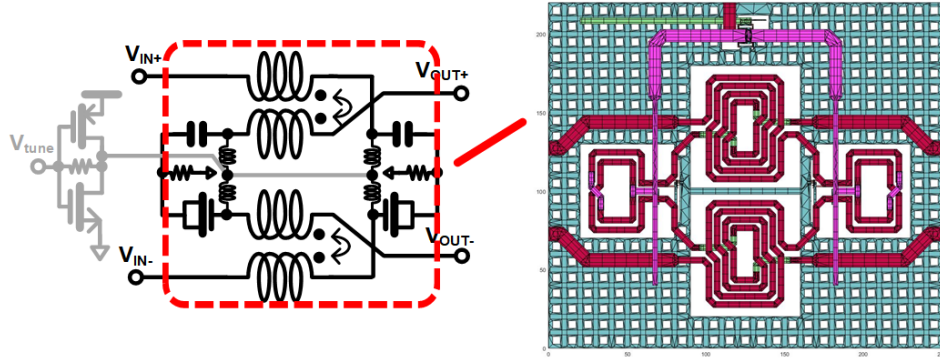


Figure 6.6: Schematic and layout of 60-GHz high-switching-speed differential RTPS.

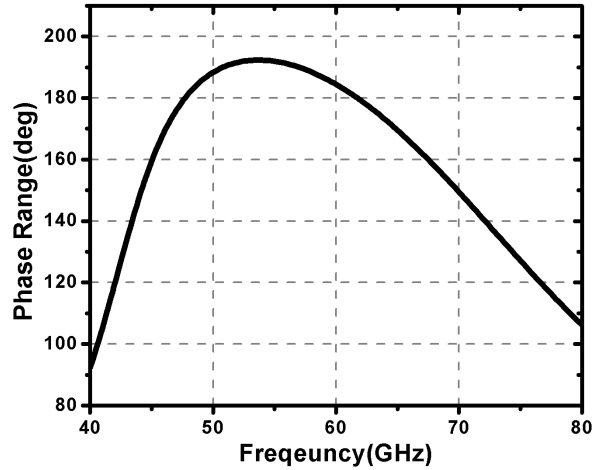


Figure 6.7: Simulated phase range of 60-GHz high-switching-speed differential RTPS.

amplifier, and 120-GHz power amplifier. In this section, the building blocks of MOT-2 will be discussed.

For outphasing transmitters, maintaining isolation between the two paths is critical to achieve high dynamic range. Instead of using conventional quarter wavelength Wilkinson design, the lumped element with eight shape inductor is used to reduce the area footprint as shown in Fig. 6.9. Simulated results including Wilkinson power divider and transformer based balun is shown in Fig. 6.10. The results show 2.9 dB loss at 60-GHz

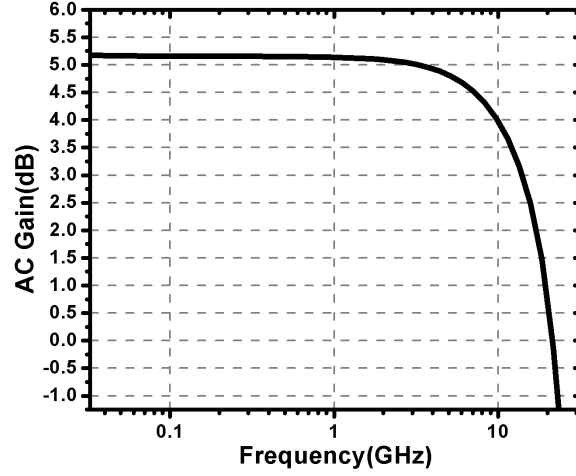


Figure 6.8: Simulated gain of phase modulated port.

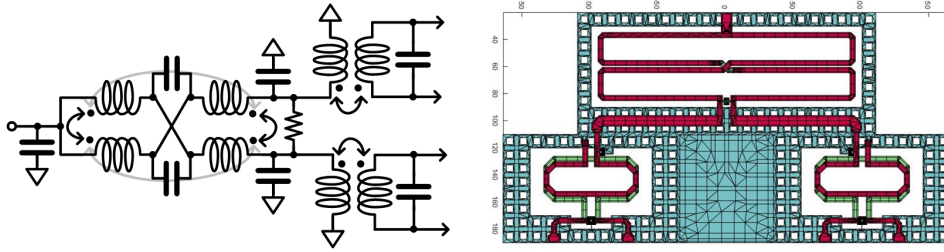


Figure 6.9: Schematic and layout of Wilkinson power splitter and balun.

with 24 GHz 1-dB bandwidth and >23 dB isolation between ports. The tuned frequency tripler schematic is shown in Fig. 6.11. While biasing at the maximum g_{m3} , the input is matched to $50\text{-}\Omega$ at 20-GHz while the output is matched to $50\text{-}\Omega$ at 60 GHz as shown in Fig. 6.12. The large signal simulation results are also shown in Fig. 6.12 to show the performance of tripler, when driver towards 0 dBm compression is with 7% efficiency.

The frequency doubler is one of the most important building blocks in the link since it requires not only high drain efficiency (DE) but also power gain from f_0 to $2f_0$ so that the driver is not required to generate high output power which will degrade the overall efficiency. By adding a $\lambda/2$ $2f_0$ reflector at the input of a push-push frequency doubler,

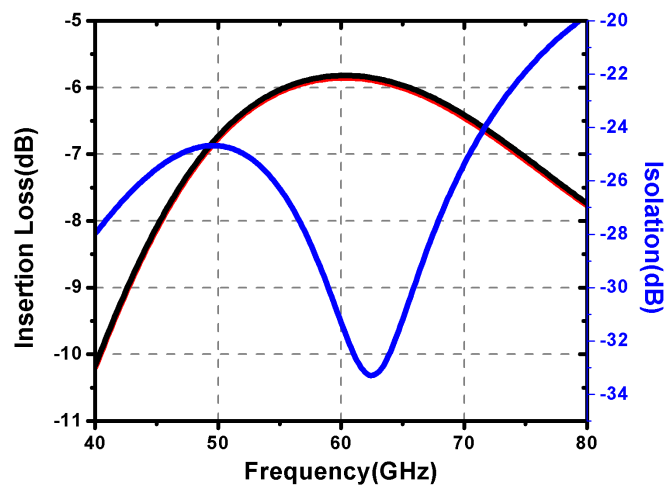


Figure 6.10: Simulated performance of Wilkinson power divider and baluns.

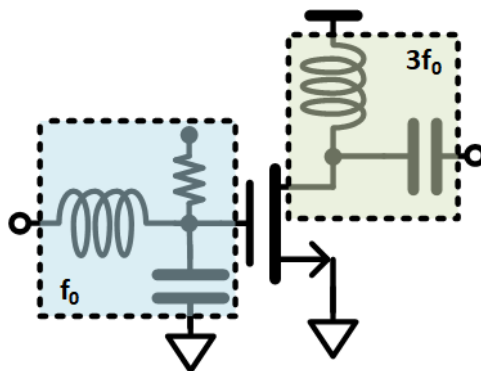


Figure 6.11: Schematic of frequency tripler.

the output power is improved in [49]. To reduce the area, an L-C notch filter resonates at $2f_0$ in Fig. 6.13. A 2^{nd} harmonic load-pull simulation with the reflector shows 9% improvement in DE as shown in Fig. 6.14 and Fig. 6.15. Simulation including output matching network of frequency doubler in Fig. 6.16 shows 14% peak DE with 0 dB conversion gain and -0.18 dBm output power.

The schematic of one-way in a three-stage two-way combined 120-GHz PA is shown in Fig. 6.17 to deliver high output power while still maintain high PAE. The design details are discussed in Chapter 3. Simulated PA results on each path is shown in Fig.

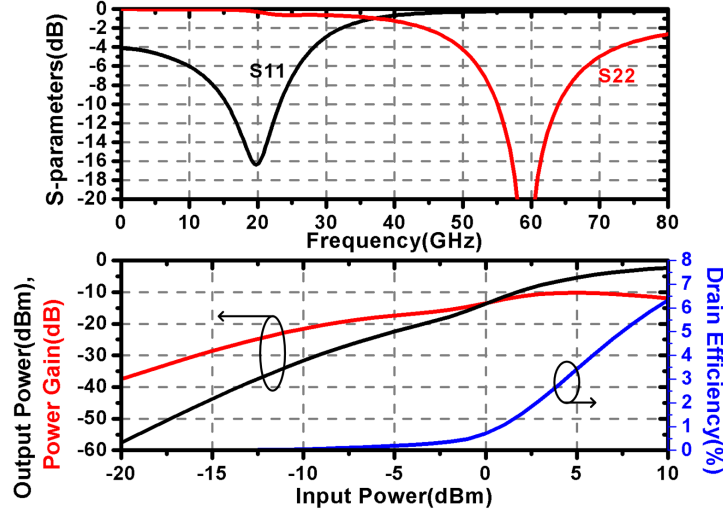


Figure 6.12: Simulated frequency tripler performance.

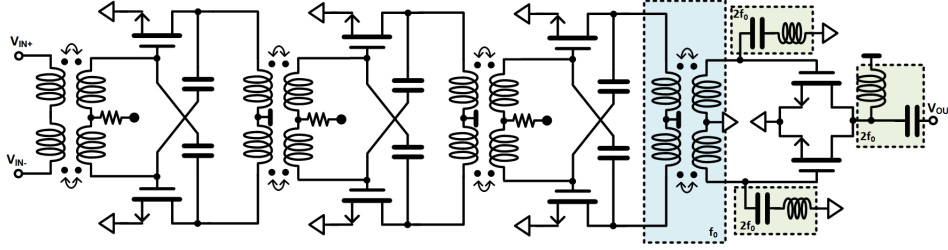


Figure 6.13: Schematic of 60 GHz driver and frequency doubler.

6.18 where it shows 14.8-dBm output power and 21.4% peak PAE.

6.5 Simulation and measurement results

MOT-1 is realized in GlobalFoundries 22-nm FDSOI CMOS process. The chip photograph is shown in Fig. 6.19 and the chip size including DC and RF pads occupies 1.58 mm² while the core circuit occupies 1.17 mm². The quiescent DC power consumption is 190 mW.

An output power sweep measurement is performed at 120 GHz as shown in Fig. 6.20(a) by sweeping the input power. The multiplier chain saturates with 0 dBm in-

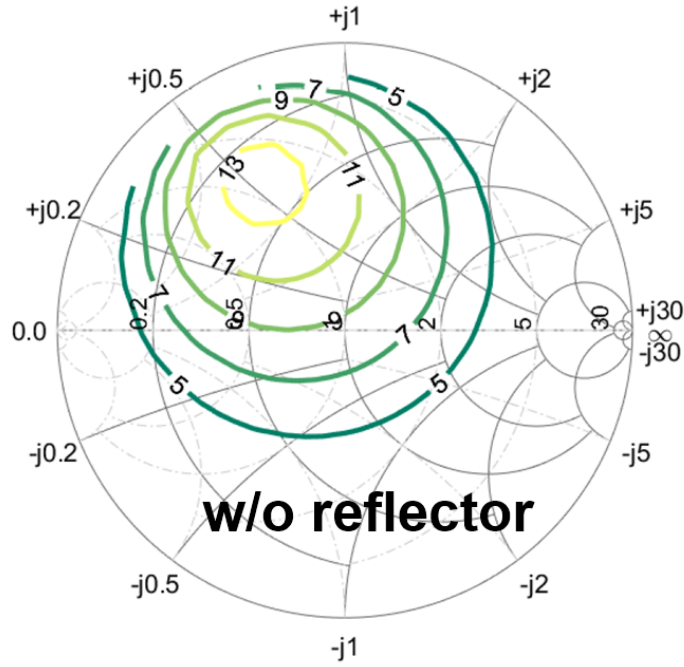


Figure 6.14: Drain efficiency load-pull simulation of frequency doubler without reflector.

put power at 20 GHz. The output power and transmitter efficiency across frequency is also plotted in Fig. 6.20(b) and shows the 5.9 dBm peak output power and 1.4% peak efficiency at 116.4 GHz. The 3dB output power bandwidth is 14.2 GHz while the bandwidth over 1% efficiency is 8.4 GHz. The static outphasing performance is shown in Fig. 6.21, where V_{tune} in RTPS of two paths are swept from -0.5V to 1V. The measured dynamic range is 25.2 dB, which is sufficient for QAM modulation. Initial modulation measurements are also shown in Fig. 6.22.

The proposed MOT-2 is fabricated in GlobalFoundries 22-nm CMOS FD-SOI technology with 1.42 mm² full chip size and 0.54 mm² core area as shown in Fig. 6.23. Power measurement is performed with Cascade 67 GHz probe at input, GGB WR-6 waveguide probe at output and Erickson power meter. The measured results show peak output power of 15.1 to 16.2dBm and peak efficiency of 9.2 to 12.2% from 110 to 120 GHz as shown in Fig. 6.24 and Fig. 6.25. The static outphasing performance of 17.6 dB by tun-

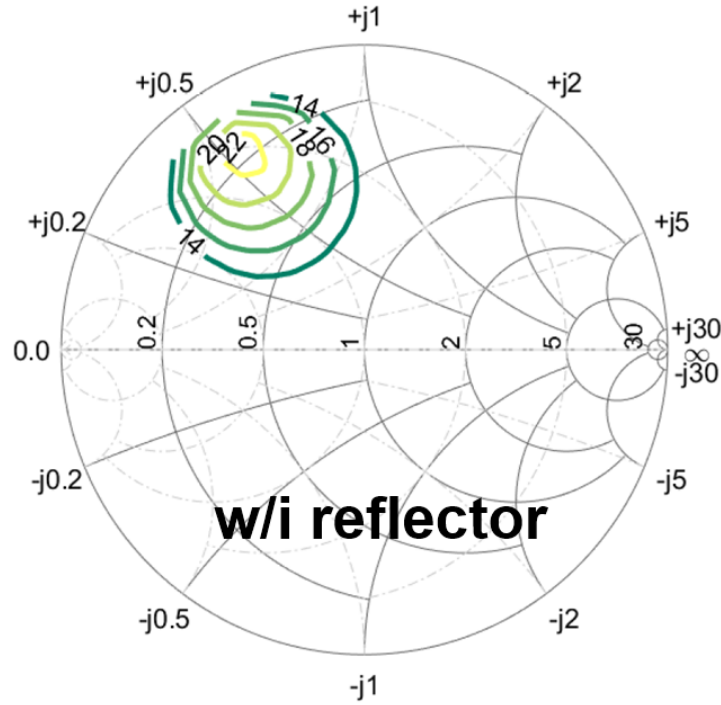


Figure 6.15: Drain efficiency load-pull simulation of frequency doubler with reflector.

ing RTPS in two paths dynamic range at 120 GHz is shown in Fig. 6.26. The dynamic range is over 13 dB in the range of 110-120 GHz and shown in the red curve in Fig. 5.6.25. It is worth mentioning the dynamic range could be further improved by varying input power at 20-GHz. Initial modulation measurements using AWG and off-shell components for down-conversion are also shown in Fig. 6.27. The highest data rate measured at 114 GHz is 13.5 Gbps with 18.9% EVM in 8PSK modulation scheme.

Output power and DC-to-RF efficiency of MOT-1 and MOT-2 compared to the prior arts is plotted in Fig. 6.28, where it shows the proposed transmitters have superior performance compared to prior arts.

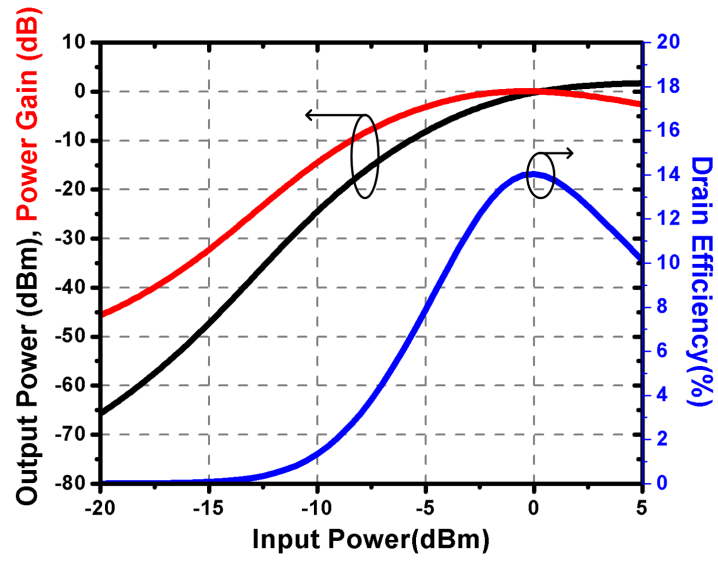


Figure 6.16: Simulated frequency doubler performance.

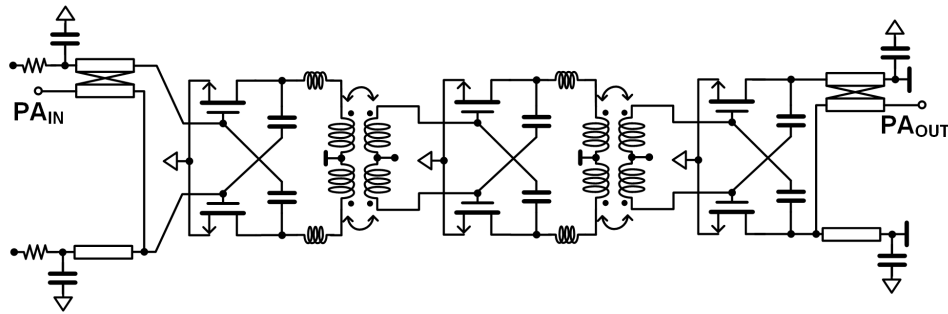


Figure 6.17: Schematic one-way three-stage 120 GHz PA.

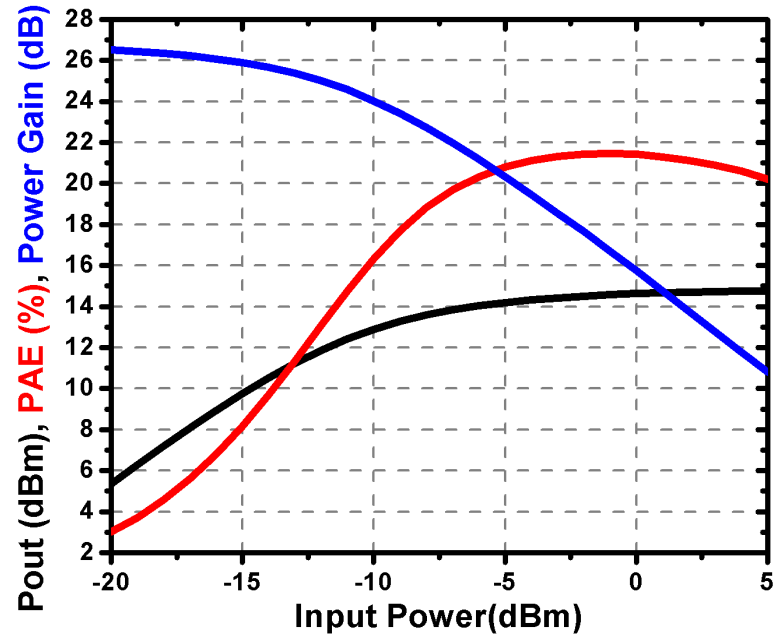


Figure 6.18: Simulated results of two-way three-stage PA.

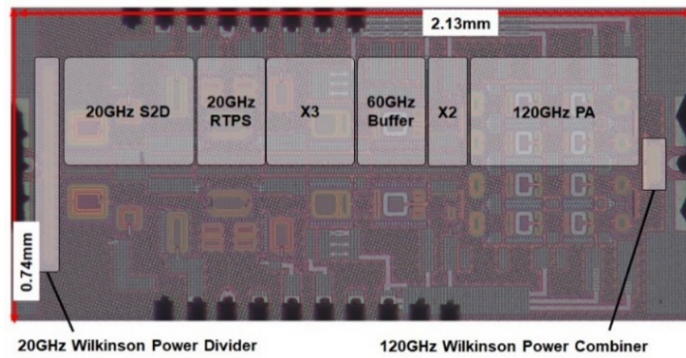


Figure 6.19: Die micrograph of MOT-1.

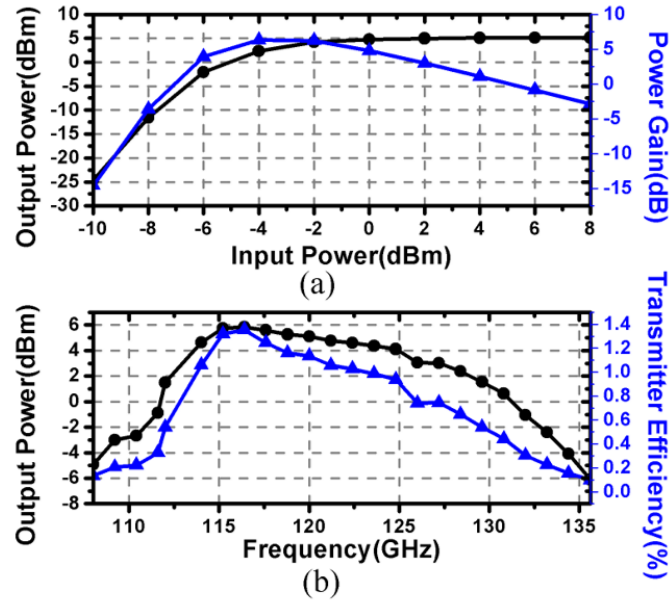
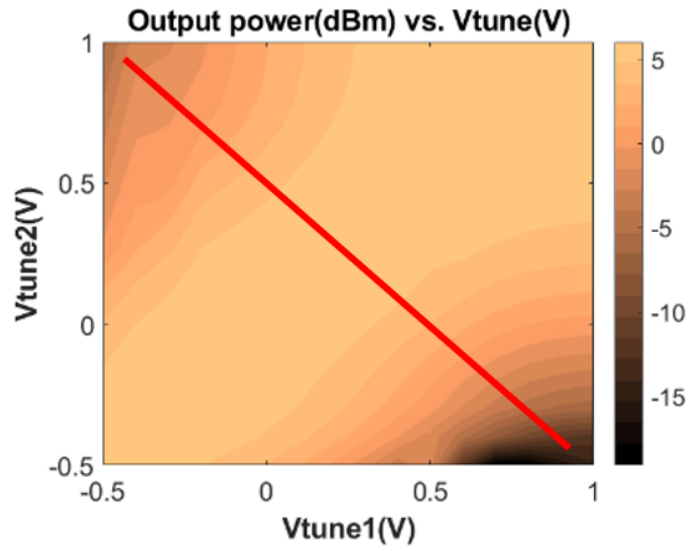


Figure 6.20: Measured power sweep of MOT-1.

Figure 6.21: Measured output power vs. V_{tune} of MOT-1.

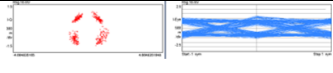
Modulation Scheme	Constellation and eye diagram	Data rate/EVM
QPSK		4Gbps/27.6%
8PSK		4.5Gbps/18.2%

Figure 6.22: Measured constellation diagram of MOT-1.

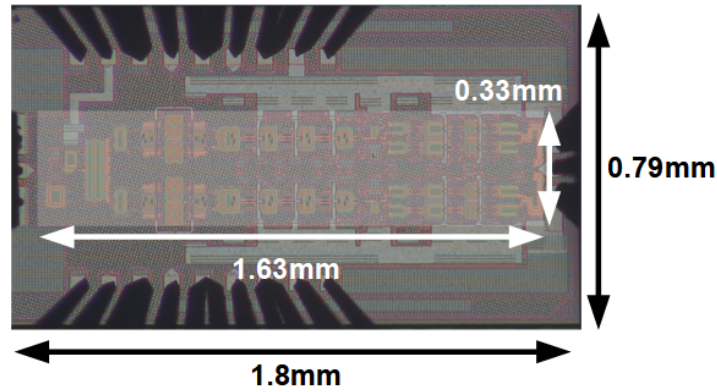


Figure 6.23: Die micrograph of MOT-2.

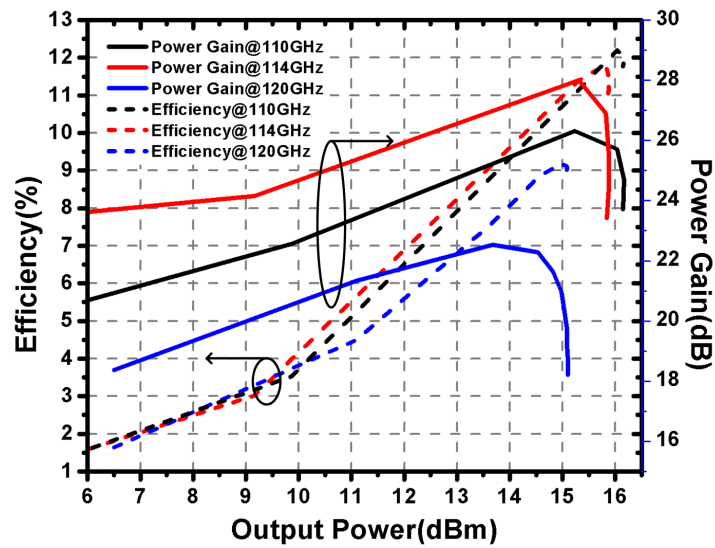


Figure 6.24: Measured power sweep of MOT-2.

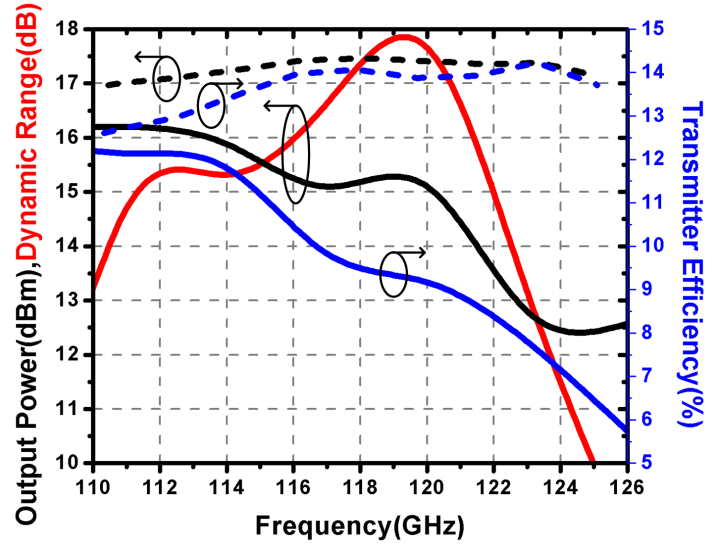


Figure 6.25: Simulated (dashed) and measured (solid) frequency response of MOT-2.

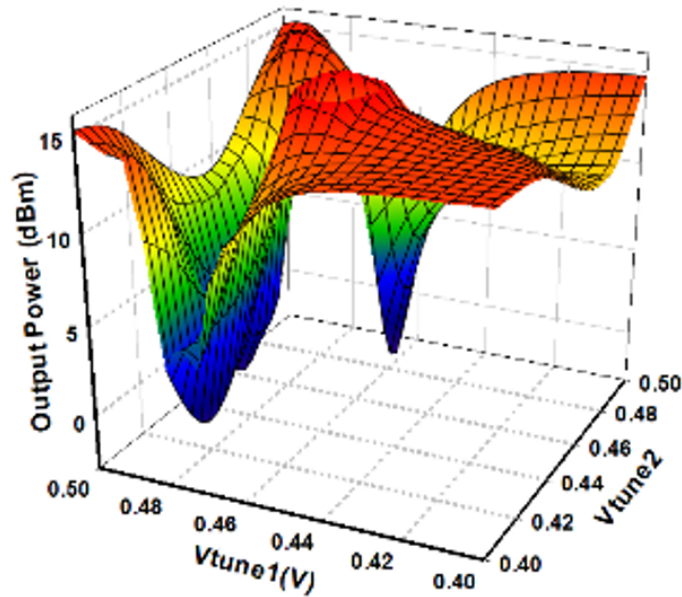


Figure 6.26: Measured output power vs. V_{tune} of MOT-2.

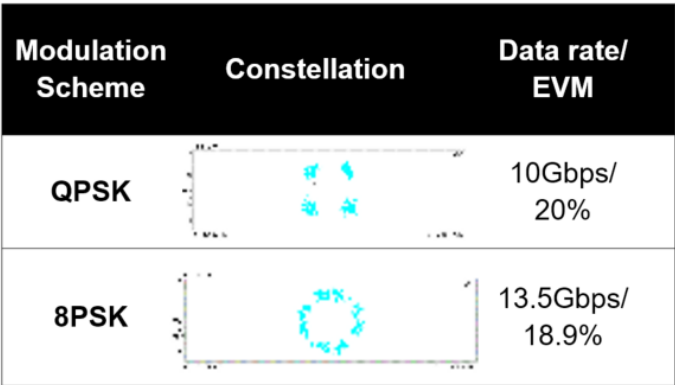


Figure 6.27: Measured constellation diagram of MOT-2.

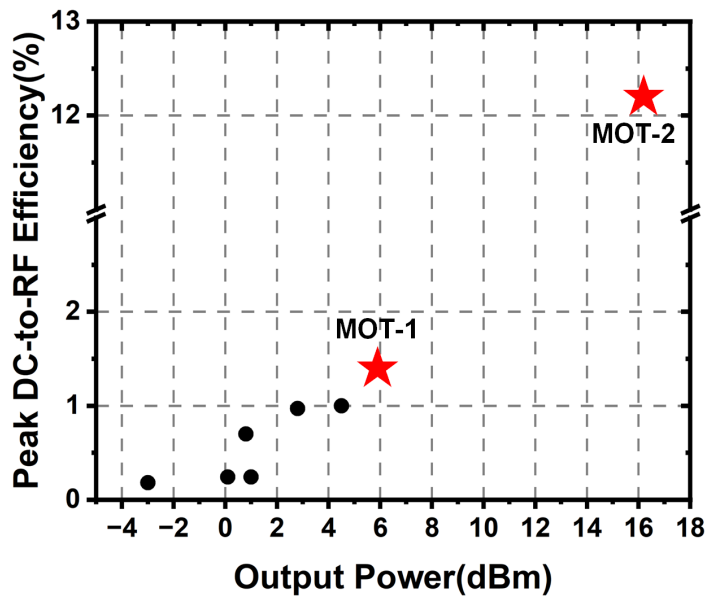


Figure 6.28: Performance survey of state-of-the-art D-band CMOS transmitters.

Chapter 7

Conclusion and Future Work

As demonstrated in Chapter3, CMOS PA with optimized transistor layout and low-loss CLB is capable of delivering higher than 15% PAE and high power with multi-way parallel power combiner at D-band. Chapter4 demonstrates InP PAs with PAE higher than 32% at D-band and PAE higher than 17% at G-band. Although these PAs show record numbers in D- and G-band, better performance could be possible from both calculation and simulation results. However, the better measured performance relies on more accurate models in both small and large signal as well as more precise EM simulation.

Chapter5 shows the new approach of switches implementation at sub-THz. With the benefit of low-loss hybrid coupler at D- and G-band as well as high Q and high capacitance range of InP HBT, the topology provides low loss and high isolation compared to prior arts. Besides, the proposed SPDT switches could be used as phase shifter as well for compact transmit-receive module as shown in Fig. 7.1.

Chapter6 reveals high efficiency transmitter topology using outphasing multiplier chains. Two prototypes all show higher efficiency than prior arts and especially MOT-2 shows 10-fold improvement in both efficiency , output power and power density. In the

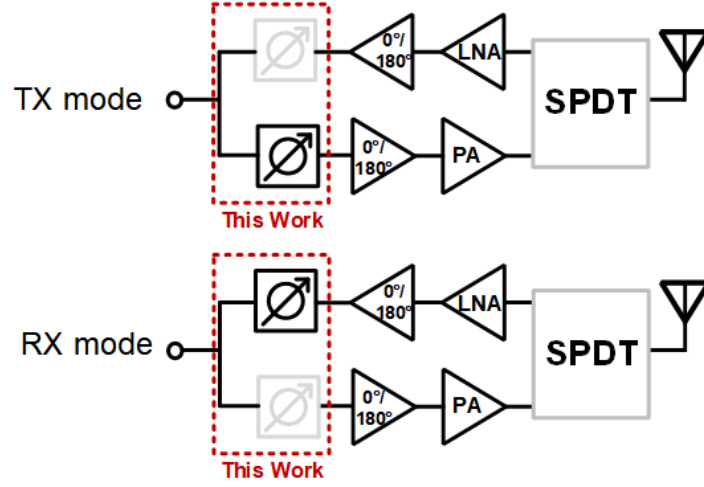


Figure 7.1: Potential use of the proposed SPDT with built in RTPS.

future work, load modulation with Chereix combiner could be explored for better back-off efficiency as well as integrating IF-DAC and PLL LO generation for full transmitter power consumption.

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