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DESIGN AND FABRICATION OF A MONOLITHICALLY INTEGRATED THERMAL SELF-PROTECTION CIRCUIT WITH A HIGH VOLTAGE GaN-on-Si POWER HEMT

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List of Publications

D. Risbud, M. Power, J. W. Pomeroy, M. Kuball, K. D. Pedrotti, "Thermal characterization of high voltage GaN-on-Si Schottky Barrier Diodes (SBD) for designing an on-chip thermal shutdown circuit for a power HEMT", WiPDA 2015, Blacksburg, VA, Nov. 2015

D. Risbud, K.D. Pedrotti, "Design of analog and digital building blocks using depletion mode High Electron Mobility Transistors (HEMTs) and Schottky Barrier Diodes (SBDs) fabricated in high voltage GaN-on-Si Schottky power semiconductor technology", WiPDA 2016, Fayetteville, AR, Nov. 2016. Abstract ready for submission.

M. Power, D. Risbud, I. Chatterjee, J.W. Pomeroy, B. Wynne, M. Gajda, J. Šonsky, "Reverse-biased induced mechanical stress in AlGaN/GaN power diodes", ISPSD 2016, Prague, Czech Republic, Jun. 2016

M. Power. D. Risbud, J. W. Pomeroy, M. Kuball, K. D. Pedrotti, "Electrothermal current redistribution in GaN power electronics and its effect on the peak channel temperature rise", Transactions on Electron Devices – Submitted Apr. 2016. In revision

B. Liu, D. Risbud, S. Bahl, D. Anderson, "Extraction of Dynamic On-resistance in GaN Transistors under Soft- and Hard-switching Conditions", CSICS 2011, Monterey, CA, Oct. 2011

D. Risbud, "HEMT Temperature sensor", USPTO 81626918US, Mar. 2014

Publications in progress:

D. Risbud, K.D. Pedrotti, "Electro-thermal modelling of high voltage lateral GaN HEMTs for power applications using Kirchhoff transformations"

Abstract

Dilip M. Risbud

DESIGN AND FABRICATION OF A MONOLITHICALLY INTEGRATED THERMAL SELF-PROTECTION CIRCUIT WITH A HIGH VOLTAGE GaN-on-Si POWER HEMT

In recent years, significant progress has been made in developing heterojunction GaN power high electron mobility transistors (HEMTs) on silicon substrates. While GaN-on-Si HEMTs have several performance advantages over silicon MOSFETs due to the material properties, the self-heating effect under high power dissipation conditions has a serious impact on device performance and reliability due to material degradation such as breakdown of the nitride or other dielectric layers. Instantaneous *di/dt* and *dv/dt* transients may cause rapid heating of the power HEMT during switching in applications such as automotive, power conversion and motor drive. Compared to the RF and microwave devices, high voltage power HEMTs (600 – 1200V) use a large number of gate fingers (or anode and cathode fingers in case of diodes) to achieve high voltage and current operation. However, such large designs using a compact layout to save die area run the risk of thermal crosstalk between the fingers. The resulting enhanced self-heating effect can lead to damage or destruction of the device. The assumption of uniform temperature distribution throughout the channel holds well for smaller power devices, but for the substantially larger high voltage power diodes the temperature distribution is

not uniform from the center of the die to the outer edge. This non-uniformity along with self-heating effects poses serious challenges for device reliability and highlights the need to design self-protection features to prevent the device from destruction during operation.

The purpose of this thesis is two-fold. First, the non-uniform temperature distribution across the die is modeled and measured to confirm that the fingers at the center are the hottest and there is a gradual decrease in temperature away from the center towards the edge. This work reports the thermal characterization results of various large area multi-finger AlGaN/GaN Schottky Barrier Diodes (SBDs) fabricated in high voltage GaN-on-Si power semiconductor technology. An accurate thermal model was developed and thermal simulations were performed for the device structure to estimate the device temperature near the 2-dimensional electron gas (2-DEG) in SBDs and HEMT switches for various power densities. Micro-Raman thermography and infrared imaging techniques were used for experimental measurements to validate simulation results. The rise in channel temperature under various power densities and mapping of the thermal gradient across the device during operation is reported.

The second purpose is to utilize the detailed knowledge obtained from thermal characterization and design a novel thermal shutdown scheme that can be monolithically integrated into a high voltage power HEMT, thus providing a self-protection feature. A cell library of individual analog and digital building block sub-circuits was developed starting with modeling of the diode and the HEMT. A test chip of all individual cell designs was fabricated and each cell

was tested at wafer level for functionality. This thesis describes the design, fabrication and test results of each building block sub-circuit. It was demonstrated that monolithic integration of smart control features is feasible in the emerging GaN-on-Si power semiconductor technology.

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My pursuit of a PhD has taken a few right and left turns, the most important one being my move to the United Kingdom to work for NXP Semiconductors who offered me a technical leadership position to develop their GaN-on-Si power semiconductor products. I am grateful to Andrew Rimmington, Dr. Julian Humphreys and Dr. Werner Riethmüeller on the management team for offering me a great technical role on the GaN team and granting me a permission to design and fabricate my chip on the NXP wafer process. My colleagues at NXP have been very helpful during my years there. In particular, Barry Wynne often helped me with simulation tools, PCB design and instrumentation needs. Dr. Mark Gajda's help in taping out my design and the actual fabrication of the wafer lot has been extremely critical in my success with first silicon. Mark and Dr. Saurabh Pandey also helped me with some of the on-wafer measurements even though it meant extra time for them in the lab over and above their own work. My manager Paul Spikers was extremely helpful in

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Chapter 1

Introduction

Gallium Nitride (GaN) on silicon substrate is an exciting new technology for high voltage discrete power semiconductors offering several key advantages over the highly mature silicon metal-oxide semiconductor field effect transistor (MOSFET) technology. The material advantages of GaN, particularly a wide band gap, high electron mobility, high critical electric field, high electron saturation velocity, and higher thermal conductivity make it possible to go beyond the technology limitations of silicon MOSFETs in high power applications such as switch mode power supplies, solar inverters, motor drives and automotive electronic systems [1]. Higher power density, faster switching, lower losses and more efficient power conversion system design with smaller magnetic components is now possible. Major technological advances have resulted in device performance that far exceeds the traditional silicon MOSFETs, particularly in breakdown voltage and on-state drain-source resistance Rds(on). The material properties of GaN and their impact on system design considerations as summarized in the following table clearly show the advantages over Silicon.

Table 1: GaN Material Properties

Property	Si	GaN	System Design Impact
Bandgap E_g (eV)	1.12	3.49	High BV, Large power capacity, High temperature operation, Rad hard
Electric Field E_c (MV/cm)	0.3	3.5	High current density, Reliability, Efficiency
Electron Mobility (cm^2/Vs)	1400	2000	Fast switching, Smaller size
Thermal conductivity k (W/mK)	117	158	High operation temperature, Less cooling requirement, Efficient heat removal
Saturation Electron Velocity V_{sat}($x10^7$cm/s)	1	1.3	Low R(on), Fast switching
Peak electron velocity V_p($x\ 10^7$cm/s)	1	2.7	High switching frequency, Low R(on) and high current handling capacity, Low power losses; Small magnetics

The semiconductor industry has focused on creating technologies that will enable fabrication of these novel devices in a cost effective manner. The obvious choice is to develop wafer process technology that is compatible with standard silicon fabs so that the economies of scale can be reached. Dynamic new start-up semiconductor companies such as Efficient Power Corporation (EPC) and Transphorm have been successful in introducing high voltage power discrete switches (HEMTs) manufactured using silicon compatible wafer processes. The first enhancement mode devices were introduced in June 2009 [1]. Since then, impressive gains have been made in releasing several new products with higher breakdown voltages, including power modules. Major semiconductor integrated device manufacturers (IDMs) such as Infineon and ON Semi. have been working on bringing GaN-on-Si technologies from R&D to high volume manufacturing.

Leading power and RF system product companies are adopting these novel devices to not just replace the silicon MOSFETs, but design new topologies that will truly exploit the material advantages of GaN. Table 2 shows the figure of merit (FOM) performance comparison between silicon MOSFETs and GaN HEMTs [2] [3]. The choice of using GaN HEMTs for high voltage high power applications is compelling based on these figures. It is a matter of time before the cost factor is resolved to effectively bring an "end of the road" for silicon in power conversion as we know them today [1].

Table 2: Figure of Merit

Figure of Merit	**Si**	**GaN**
E_g (eV)	1.1	3.49
n_i(cm^{-3})	1.5x10^{10}	1.9x10^{-10}
ε_r	11.8	9.0
μ_n (cm^2/Vs)	1350	2000
v_{sat} (10^7 cm/s)	1.0	2.5
E_{br} (MV/cm)	0.3	3.3
Θ (W/cm K)	1.5	1.3
Johnson	**1**	**27.5**
Baliga	**1**	**537**

Johnson's figure of merit is defined as $JM = \frac{V_{br} v_{sat}}{2\pi}$

Baliga figure of merit is defined as $BFOM = \varepsilon_r \mu E_c^3$

This is an emerging technology and thus poses some challenges of its own that need to be resolved. Self-heating is a known problem in power semiconductors and is of particular importance in AlGaN/GaN power HEMTs due to the higher power dissipation levels in high frequency switching power conversion, motor drive and automotive applications. Channel temperatures can reach several hundred degrees above the ambient temperature. In automotive applications, under extraordinary thermal stress, peak junction temperature of a power switch can exceed 200^{o}C for millisecond time intervals affecting device reliability over its life time [4] [5]. Even under static conditions, the effect of self-heating manifests itself as current collapse in the DC I-V measurements where a pronounced negative slope in the saturation region is observed as power dissipation is increased. Current collapse (or dynamic Rds(on)) gets worse at higher temperatures due to reduced mobility and higher gate leakage. Heat has detrimental effects on the temperature dependent material properties of GaN such as band-gap and mobility. Consequently, device performance as well as gate electrode reliability are adversely impacted [6] [7].

1.1 Motivation for This Work and the Approach

In applications such as power factor correction (PFC), boost circuits or motor drive control, the devices reach high temperatures very rapidly during switching and can lead to device degradation or even destruction as it exceeds the maximum junction temperature (T_j). Thus, accurate estimation of junction

temperature, understanding spatial and temporal heat distribution mechanism within the device and a way to self-protect the device are of paramount importance. The ultimate goal of this work is to design an integrated self-protection circuit that will put the power HEMT in an OFF state in an event of excessive heat.

The current research in the field is largely carried out on small radio frequency (RF) GaN devices on silicon carbide (SiC) substrates and is based on a number of assumptions that simplify numerical, analytical and experimental analysis [8]. However, this approach and assumptions do not hold true for multi-finger high power GaN HEMTs due to the fundamental differences in technology and the principles of device operation. These devices are designed on silicon substrates and are different in that the current flow (Drain to Source) is in a lateral direction as opposed to vertical in the case of silicon MOSFETs or SiC FETs. The total gate width can exceed one hundred millimeters, while the width of a single finger may have sub-mm dimensions. The number of fingers can vary depending on the layout methodology. The results from small device analysis and experiments cannot be easily extrapolated to predict thermal and electrical behavior of large devices.

One of the biggest challenges is how to take the heat out of these discrete devices efficiently and quickly during use. Innovation in power packaging technology, materials and heat sinks have resulted in practical solutions, though

at increased cost of materials and area. Temperature compensation schemes are applied at the board level, and external cooling is often implemented for thermal management [9]. Off-chip protection circuits entail design overhead, extra components, exotic materials, more board space and additional cost to the user. Thus, just as important these off-chip heat removal techniques are, there is a need to devise techniques to reduce heat generation from within the device itself. While fundamental material properties and electron transport at high voltage stress do put limitations on this approach, self-protection against excessive heat can be built into the device. This thesis demonstrates the feasibility of such an approach for the first time through monolithic integration of analog and digital build blocks of a novel thermal shutdown circuit to be integrated with a 600V power HEMT on the same process platform.

1.2 Design Approach

A Smart Discrete GaN-on-Si Schottky gate power HEMT with monolithic integration of a thermal shutdown circuit is designed using only the depletion mode HEMTs, Schottky Barrier Diodes and passive components. This is because enhancement mode devices were not available in the process technology at the time of this study. Schottky Barrier Diodes are used as temperature sensors to sense the increase in device temperature and raise a flag that activates a thermal shutdown of the gate to turn the device off beyond a predetermined threshold temperature, thus providing a self-protection feature. The design is based on analysis and characterization of various device design variants. A novel,

unconventional layout design approach is also proposed for more uniform heat distribution within the device. First, small geometry SBDs and HEMTs were designed and modeled to develop a cell library of analog and digital sub-circuit building blocks. Each individual cell was fabricated and tested at wafer level for functionality. This dissertation describes the electro-thermal modeling, temperature measurements of various SBDs, test results of the sub-circuits, and the design of the integrated thermal shutdown scheme. Fabrication and testing of the entire thermal shutdown scheme integrated into a large area multi-finger 600V depletion mode Schottky gate HEMT is the subject of further research.

1.3 Thesis Organization

Chapter 1 gives an introduction to the emerging field of GaN-on-Si high discrete power transistors and the advantages of using GaN based devices over Si MOSFETs in applications. Thermal issues associated with the high electron mobility transistors (HEMTs) are discussed. Motivation for this thesis is the need for designing a self-protection feature in case of an overheat event, which is a real concern due to their high power operation. Chapter 2 details the GaN-on-Si wafer process steps, a comparison between a Si MOSFET structure and a GaN HEMT structure, GaN material properties and device physics of GaN HEMTs and Schottky Barrier Diodes (SBDs). Chapter 3 presents the thermal characterization studies of 600V SBDs using micro-Raman and infrared imaging techniques. Chapter 4 explains the electro-thermal modeling parameters of a HEMT and SBD along with experimental data. These models are needed for simulating GaN based integrated building blocks and comparing the results to

simulation. Chapter 5 describes the development of a cell library comprising of several analog and digital sub-circuits leading to the monolithic integration of a thermal shutdown circuit and a large geometry high voltage power HEMT. Three different topologies are discussed, functional description and measurements of all the sub-circuits are presented. A final tape-out ready design of the complete monolithic integration is shown in the last section of Chapter 5. Chapter 6 presents the conclusion of this work and topics for further research.

Chapter 2

2.1 GaN-on-Si Schottky gate High Voltage Power Semiconductor Process Technology

The devices characterized in this work and used for circuit design were fabricated using an AlGaN/-GaN-on-Si Schottky gate process technology. The process uses Ti/Al-based ohmic contacts and Ni-based Schottky contacts which are patterned in a silicon nitride passivation-first integration scheme by dry etching. Argon implantation provides device isolation. Two Al-metal layers are used as interconnect and for high current routing. Plasma Enhanced Chemical Vapor Deposited (PECVD) silicon nitride layers are used as pre-metal and inter-metal dielectrics and final passivation. During the process flow, ohmic contact resistivity ρ_c, Schottky forward voltage at 0.1A/cm^2, reverse leakage current I_R at 50V and the diode ideality factor η are used as process monitor parameters. Circular TLM structures with varying metal to metal spacing were used to extract ρ_c . Circular diode structures with varying anode to cathode spacing were used for Schottky forward voltage, ideality and reverse leakage. The process supports up to 900V, 8A rated Schottky barrier diodes and 100 mΩ power switches with breakdown voltage above 1000V. [10]

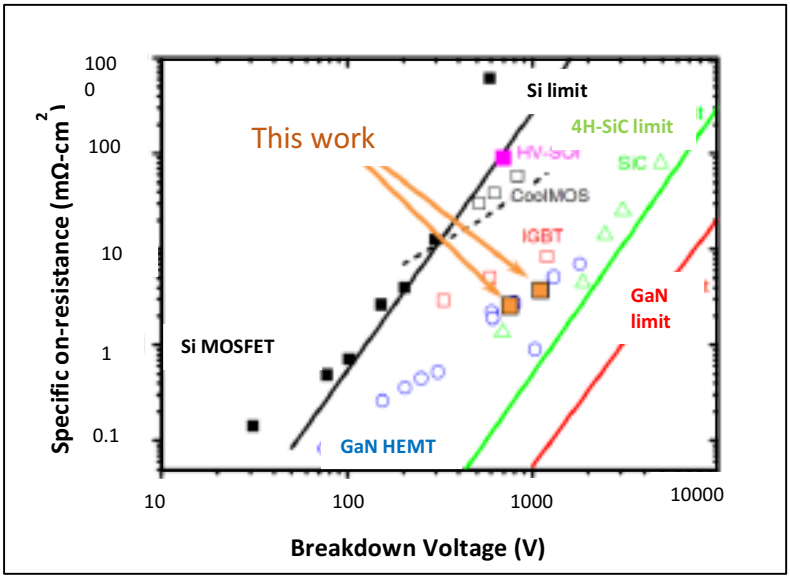

Figure 1: Benchmarking with state of the art GaN-on-Si technologies

Source: [11] [10]

The epitaxial structure is grown on a <111> silicon substrate and consists of a transition layer and a series of AlGaN/GaN buffer layers forming a superlattice (SL), followed by AlCu layer for the top metal. A superlattice is an artificial lattice fabricated by a periodic epitaxial growth. A periodic superlattice is realized by growing alternate layers of two semiconductors on top of each other, each semiconductor being grown to the same thickness and mole fraction each time [12]. In this case, AlGaN and GaN layers are grown alternatively. The electronic characteristics result from quantum interfaces as well as the % composition of Al and GaN. The SL consists of more than 150 layers, each between 1 to 3nm thick grown by Metal Organic Chemical Vapor Deposition (MOCVD). The advantage of using a SL instead of other GaN buffer layer schemes is that it reduces the sheet resistance by growing AlGaN/GaN super lattice layers over the channel region and reduces the potential barrier height at

the hetero-interface [13]. A few extra nanometers of GaN are grown on top of AlGaN to form a GaN cap layer. This layer helps decrease the reverse leakage through the Schottky contact and also reduces the peak electric field. The GaN cap layer protects the AlGaN layer during processing and prevents nitrogen degassing. In addition, this layer also has a positive impact on device performance such as increased gain, increased power added efficiency and improved DC stability [14]. Ohmic contacts are Ti/Al while Ni is used for Schottky contacts due to its high work function. Two Al metal layers are used for interconnect and for high current routing.

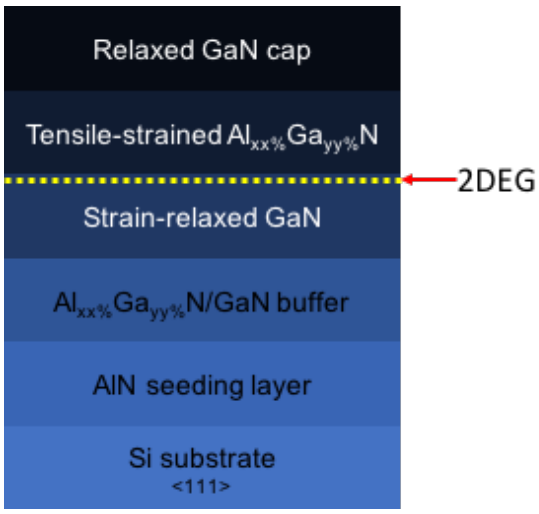

Figure 2: GaN-on-Si power epitaxial structure (superlattice)

Starting with the superlattice epi structure, the wafer process uses ten to thirteen mask layers to build high voltage discrete power semiconductor devices. Though similar to a MOSFET in operation, the wafer process is completely different as the materials involved are III-V compound semiconductors. However, the process is fully compatible with a standard silicon power fab

facility, with little or no specialized equipment. After initial cleaning of the incoming wafer (silicon substrate with epitaxial structure grown on it), a nitride layer is grown using LPCVD or PECVD techniques with pre-treatment steps to prepare the wafer for processing. Ohmic metal (Ti/Al) is then sputter deposited. This is followed by an isolation implant to define areas for device isolation. Isolation is achieved by implanting Argon from a standard implant equipment. Another nitride deposition is carried out using PECVD or LPCVD as a pre-step to formation of a gate electrode. In this Schottky gate technology, after characterizing various metals, Nickel was selected due to its high work function (5.01 eV). The nickel gate is patterned using ion beam etch in Ar ambient. Nickel thus forms the Schottky metal gate head. Openings for contact to electrodes are formed via another dry etch process. Two layers of interconnect metal are available in this process. Metal 1 and Metal 2 are both Al/Cu. A via etch process allows connection of M1 to M2. The two metal capability is very useful in discrete power technology for efficient device design by routing power bars on the top layer (M2) while using M1 for all other interconnects. Bond pad metallization followed by nitride passivation completes the process. To summarize, the mask steps are:

1) Ohmic Contact (OC): Ohmic Contact stage is designed to make apertures in LPCVD nitride preparation for ohmic metallization in Ohmic Metal (OM, next mask) stage. This applies to both diodes and HEMTs.

2) Ohmic Metal (OM): Ohmic Metal stage is designed to provide a metal contact to the GaN semiconductor. The measure at the end of this stage is a target contact resistivity (ohm.cm^2)
3) Isolation Implant (IM): Isolation implant stage is needed to provide device isolation via Ar+ implant. This means it is a way to destroy the 2DEG in regions where conduction is not required or is undesirable. Only the active regions are protected during the implant, everything else gets the damage implant.
4) Schottky Contact (SC): Schottky contact stage opens the apertures in the LPCVD nitride deposited in the OC stage. The SC etch is critical because the shape of the SC contact must be carefully controlled and maintained to make Schottky metal (SM, next mask) field plate as effective as possible. Contact leakage current and capacitance needs to be kept at the minimum. A capacitor is formed between the Schottky metal and the 2DEG, with the GaN cap and AlGaN working as a dielectric in between.
5) Schottky Metal (SM): Schottky metal stage defines the Schottky contact. The alignment between SC and SM layers is critical for optimal functioning of the Schottky field plate. There is a certain overlap for SM and SC, typically about 1.5μm. Any significant deviation from this overlap leads to increased leakage and lowering of the breakdown voltage. Pure Ni is very difficult to control with respect to delamination

before the contact (CO, next mask). A workaround this issue is to cap the Ni metal with TiWN to avoid delamination.

6) Contact (CO): Contact stage is the interface between contact metals and power metals, i.e. Metal 1 (next mask) and ohmic and Schottky metal layers. The contact is made by etching through PECVD nitride.
7) Metal 1 (IN): Metal 1 makes the second field plate in the structure. The field plate has significant influence on the dynamic behavior of the device. In addition to controlling the dynamic behavior, IN also provides support to the metal 2 (M2) layer to conduct large amounts of current.
8) Via stage (VI): Via stage connects the power layer M2 to the rest of the device. VI windows must be cleanly etched to maximize conforming to M2 and prevent voids that could lead to metal finger breaks by electro-migration.
9) Metal 2 (TC): TC stage defines the power metal, which supports high-current conduction in the device. Using AlCu helps increase electro-migration resistance. In order to be able to conduct high currents (more than $1mA/\mu m^2$) at 150^oC, M2 needs to be made as thick and wide as possible. While TC layer makes direct contact to IN layer via a wide window, the bulk of current conduction takes place in the TC layer. This is the only layer which makes physical bonding at the package level.
10) Top side passivation (CB): Top surface passivation keeps leakage current and current collapse low and under control. Typically, PECVD silicon nitride Si_3N_4 is used for passivation because silicon dioxide SiO_2

is known to lead to deep and slow traps, which is detrimental to the dynamic behavior of the device. Si_3N_4 has a trade-off between low leakage and acceptable level of current collapse.

11) Back-grind (GR): This is a commonly known technique to thin the wafer down to make the overall die thickness suitable for packaging, typically between 200 to 350 μm.

2.2 Device performance

GaN-on-Si HEMTs fabricated on this process showed good performance with 600V breakdown voltage and 13A current with 150mΩ on-resistance.

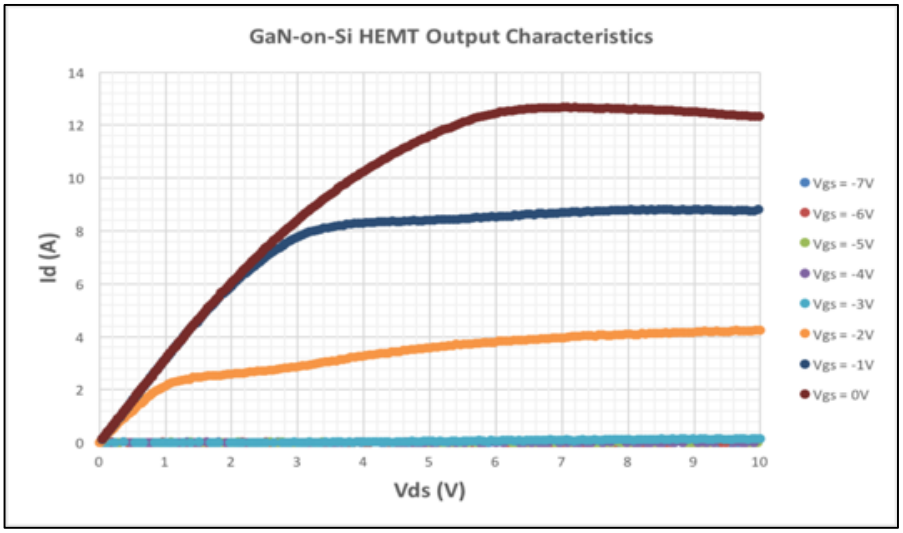

Figure 3: HEMT Output Characteristics ID-VDS

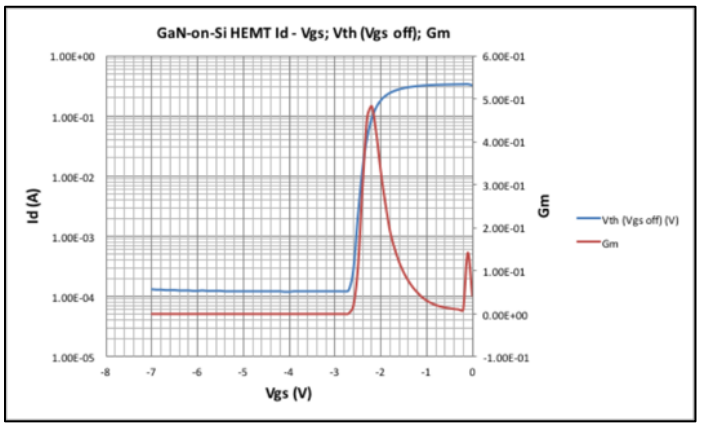

Figure 4: HEMT Output Characteristics ID-VGS

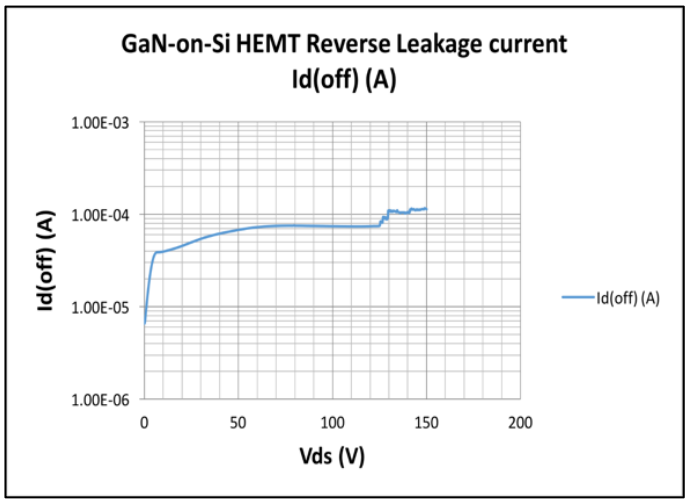

Figure 5: HEMT Reverse Breakdown

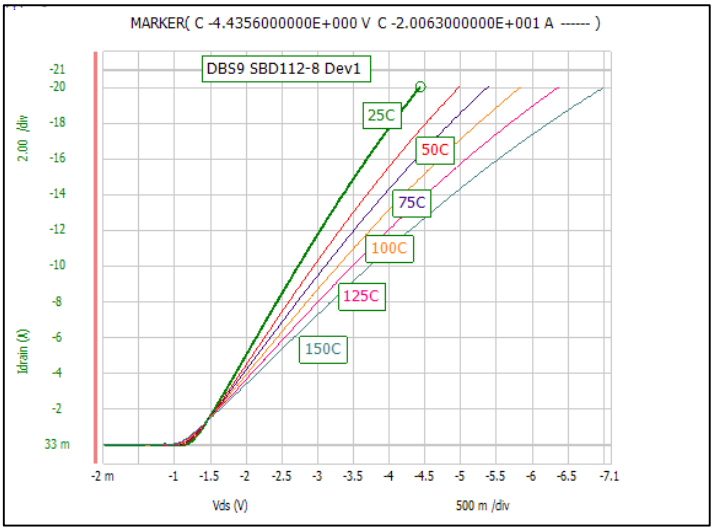

Figure 6: SBD If-VF @Temp.

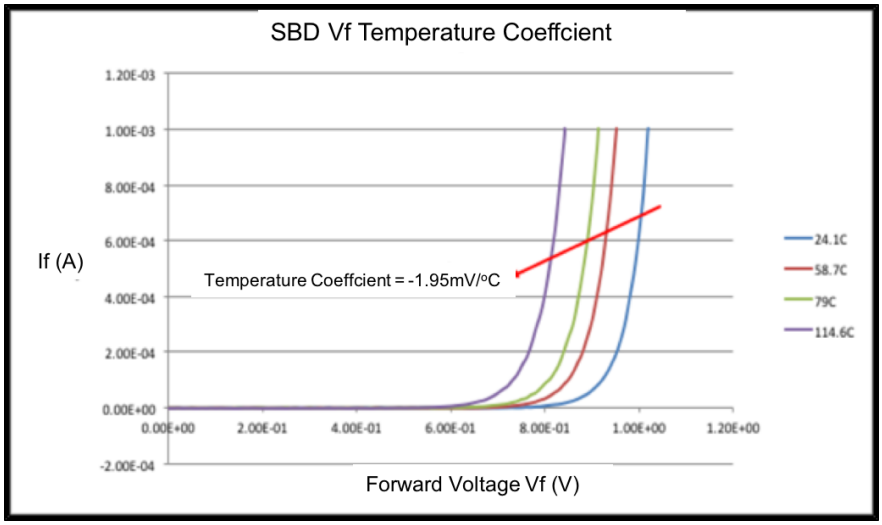

Figure 7: SBD Turn-on @ Temp.

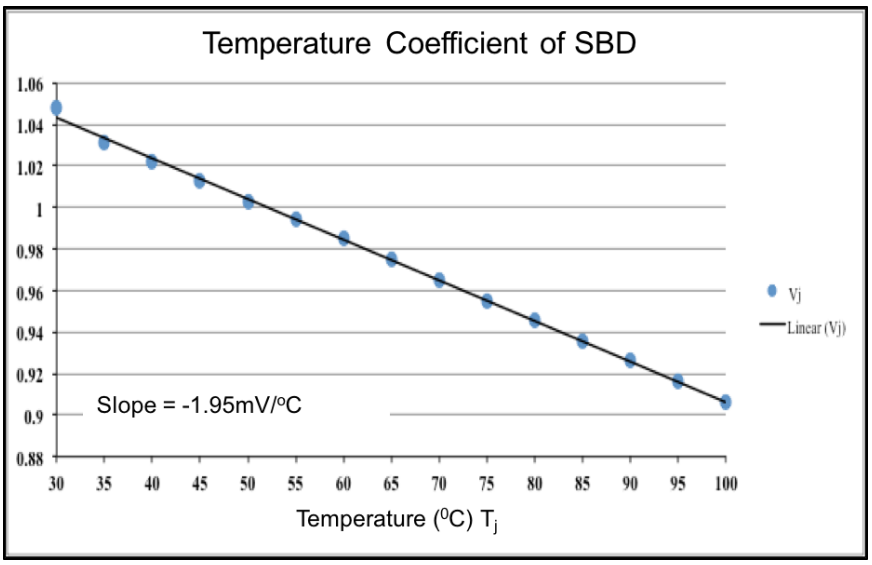

Figure 8: SBD Temperature Coefficient

2.3 Comparison of GaN devices with Si MOSFETs

Compared to the standard silicon based process technologies, GaN-On-Si process is relatively easier since it does not need as many layers as a silicon based process. This is because in a silicon MOSFET technology, several diffusion and implantation steps are required to make a transistor. In GaN-On-Si technology, most of the device engineering efforts are concentrated on designing a high quality GaN epi. This is illustrated in Fig. 9.

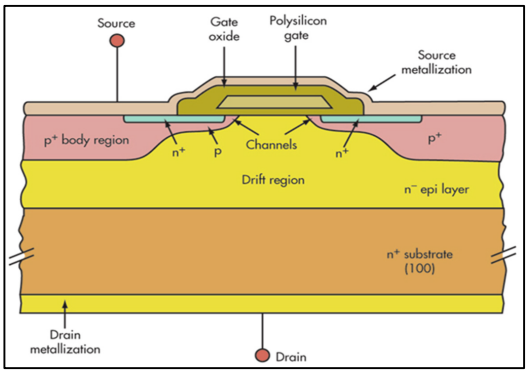

Figure 9: n-channel vertical MOSFET [source: www.mpdi.com]

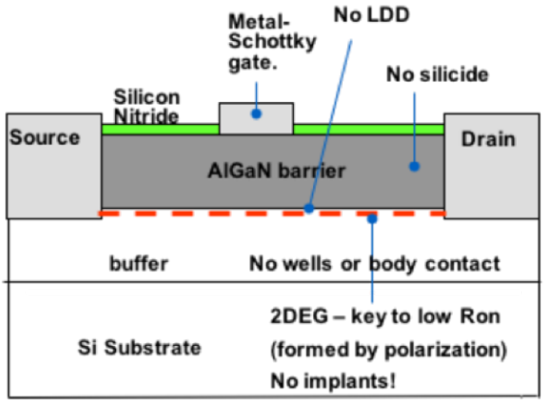

Figure 10: Lateral GaN HEMT

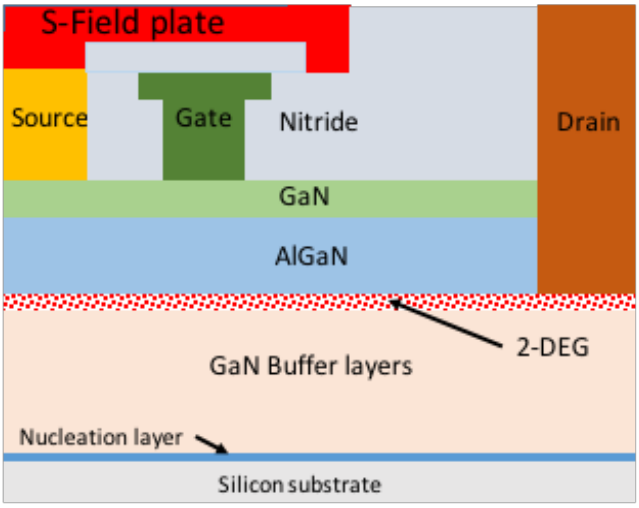

Figure 11: HEMT (S-Field plate)

Source [10]

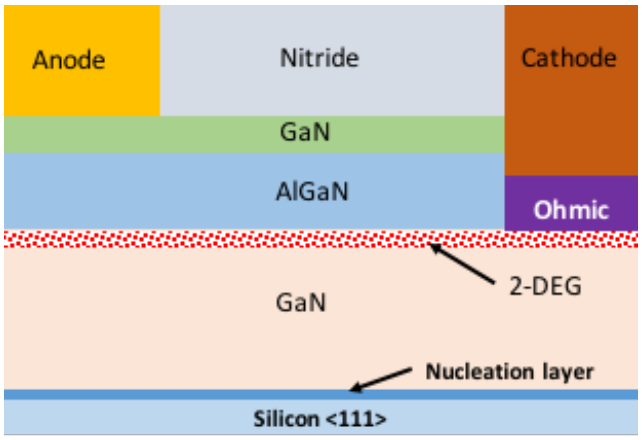

Figure 12: Schottky Barrier Diode

In silicon MOSFETs, charge is induced by intentionally doping the material with donors or acceptors. On the other hand, GaN devices are normally-ON (depletion mode) because of the inherent polarization at the hetero-interface

in the device structure. There are two types of polarization effects. Spontaneous polarization P_{SP} is inherent, the direction of which depends on the growth face of the crystal, Ga face or N face. The strain developed during the epitaxial growth induces polarization charges. This is called piezoelectric polarization. GaN is a noncentrosymmetric compound crystal exhibiting two different sequences of atomic layering in opposing direction parallel to certain crystallographic axes. The basal surface should be either Ga- or N-faced. The (0001) and (0001-) surfaces of GaN differ in their chemical and physical properties [15].

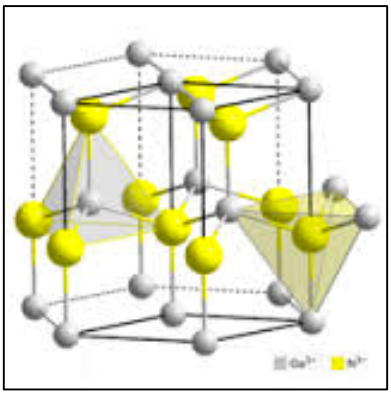

Figure 13: Wurtzite GaN crystal

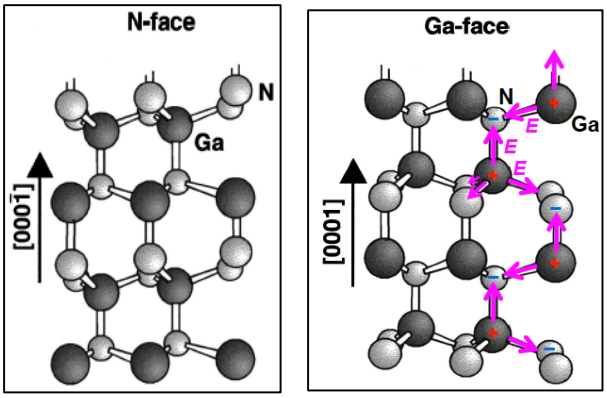

Figure 14: N-face; Ga-face Net Electric Field

Detailed discussion of the polarization phenomenon is beyond the scope of this thesis, but a diagram of 2-DEG formation at the hetero interface of AlGaN and GaN is in order. The electronic band-gap of AlN is larger than that of GaN. Therefore, band-gap of Al_xGa_{1-x} N is somewhere in between. Electrons are confined to a thin layer at the interface between Al_xGa_{1-x} N/GaN layers forming two-dimensional electron gas (2-DEG). Since there is no doping and no impurity scattering, the mobility is very high [11].

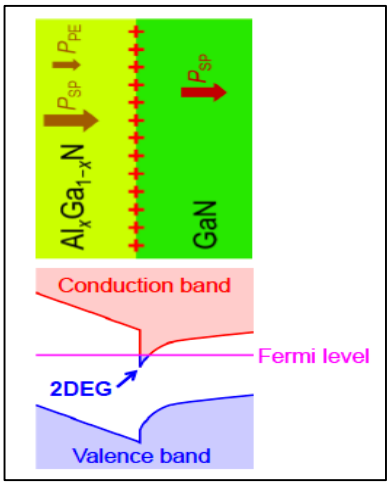

Figure 15: Formation of a 2-DEG

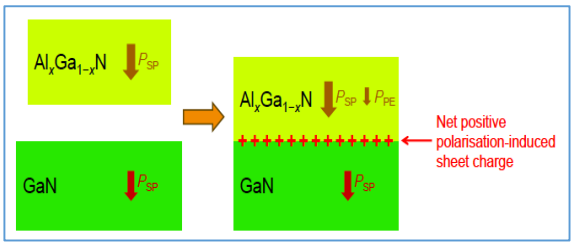

Figure 16: Net positive polarization charge

From a system designer's point of view, it is important to know that all the advantages of material properties lead to a fundamentally better power device. Vth of a GaN HEMT is generally lower than that of a Si MOSFET. There is no body diode, which means there are no minority carriers involved in conduction

and thus no reverse recovery losses. Since Gate-to-Drain capacitance C_{GD} is extremely low, high frequency switching in the MHz realm is possible. GaN switches do need a careful gate driver design due to its high speed and high gain operation [16]. For power designers, GaN technology is enabling product design possibilities that are beyond the technological limitations of silicon technologies.

Chapter 3

3.1 Thermal Characterization

Thermal cross-talk (inhomogeneous temperature distribution from finger to finger) studies have been reported over the years for RF and microwave devices, primarily on SiC substrates [17] [18]. GaN on silicon substrates for high voltage power devices is an emerging technology and such detailed studies are still underway [19]. Several theoretical models for channel temperature estimation have been proposed in the RF GaN area [20] [21] [22], but their accuracy can be limited by material properties and simplifying assumptions based on empirical results often obtained from single-finger or smaller devices. Until now, thermal analysis and measurements often assumed that the temperature stays uniform throughout the device for a given power dissipation for typical device layouts. Kuball *et al.* have reported differentiation between the contribution of the fingers at the center of the die and contribution from the fingers away from the center, observing that thermal gradients are larger in larger devices [23] [20]. It has also been reported [8] that the outer fingers of a microwave device are the coolest for device dimensions of L_g = 0.25μm, W_g = 250μm, gate pitch (s) = 25μm. In that analysis it was assumed that the dissipated power generates a constant heat flux directly under the gate. Furthermore, in Darwish *et al.*, the silicon substrate was assumed to have constant thermal conductivity k whereas in reality, k is temperature dependent [23] [24].

$$k_{GaN} = 160 * (\frac{T}{300})^{-1.4} W/(m.k)$$

$$k_{Si} = 130 * (\frac{T}{300})^{-1.3} W/(m.k)$$

3.2 Device structure and Simulation

The diodes characterized in this work are fabricated using an AlGaN/-GaN-on-Si Schottky gate process technology. The epitaxial structure is grown on a <111> silicon substrate and consists of a transition layer and a series of AlGaN/GaN buffer layers forming a superlattice, followed by AlCu layer for the top metal. Ohmic contacts are Ti/Al while Ni is used for Schottky contacts due to its high work function. Two Al metal layers are used for interconnect and for high current routing. The most common device layout is based on a comb like structure with interleaved gate fingers, all identical in length and width. The design methodology is the same for a HEMT (Source, Gate, Drain) and a diode (anode and cathode electrodes) since both are designed in Schottky technology. For the diode, each finger has L = 2μm, W = 700μm (total width = 3.5mm for a diode), finger pitch = 70μm.

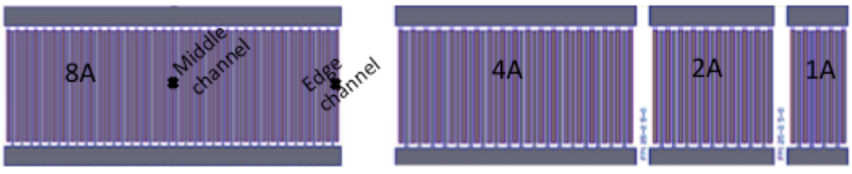

Figure 17: 8A, 4A, 2A and 1A Diodes

Finite element thermal simulations of the 1A, 2A, 4A and 8A diodes using ANSYS® were carried out to compare simulated and experimental middle and

edge channel temperatures and temperature distributions of the devices. Input parameters for the models are shown in Table 3. Isotropic thermal conductivity was assumed for each layer.

Table 3: Input parameters for FEM analysis

AlCu	221 W/m.K
GaN	$160 \times (T/300)^{-1.4}$ W/(m.K)
AlGaN/GaN superlattice + AlN	$30 \times (T/300)^{-1.4}$ W/(m.K)
Si substrate	$130 \times (T/300))^{-1.3}$ W/(m.K)
Thermal chuck (Aluminum)	237 W/m.K

In the model, a 5um layer was placed between Si substrate and chuck to represent thermal resistance between the chuck and sample – thermal conductivity was varied to match simulated temperature with measured temperature at a distance of > thickness of substrate away from the device. Ambient temperature was 22^{o}C. Temperature of the top of the chuck was measured with a thermocouple and this temperature was set as a boundary condition (25^{o}C). Heat flow was applied uniformly to 2D heaters in the channels. This heat flow is the power applied during the measurement.

As shown in Fig.18, the model required only a quarter of the device (A) due to symmetry. It is placed on a 1.5mm x 4mm epi layer structure consisting of a 1.5μm-thick GaN/3.45μm-thick AlGaN/GaN superlattice and AlN (B). The 240μm-thick Si substrate (C) spanned the 49cm^2 area of the 1 cm-thick thermal chuck (E) to simulate the fabrication of the devices on a 6-inch Si wafer. A thin

layer (D) was included between the Si substrate layer and thermal chuck to simulate the thermal resistance between the GaN device and the thermal chuck that occurs in measurement. The thermal conductivity of this layer was chosen by matching the simulated Si temperature at the point 300µm (greater than substrate thickness) away from the device to the experimental data. The thermal conductivity of the metal chuck and fingers modeled as gold, Si substrate and GaN layer were fixed at $400Wm^{-1}K^{-1}$, $119Wm^{-1}K^{-1}$ [25] and $160Wm^{-1}K^{-1}$ respectively at $25^{0}C$ [23] [24]. The thermal conductivity of the GaN layer and Si substrate were given a temperature dependence of $T^{-1.4}$ and $T^{-1.3}$ [21] respectively A thermal conductivity of $30Wm^{-1}K^{-1}$ with a temperature dependence of $T^{-1.4}$ was used for the AlGaN/GaN superlattice employed as a strain relief layer [26]. The largest contribution to the temperature rise comes from the thermal resistance between the Si wafer and the thermal chuck. For the 8A diode, ΔT was found to be significant across only

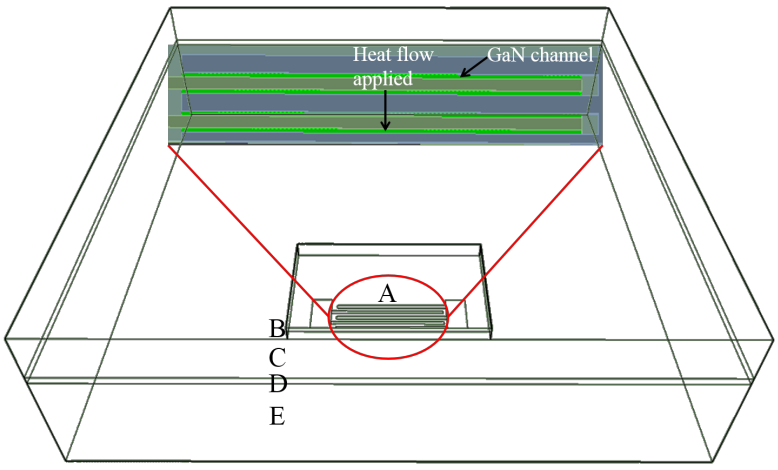

Figure 18: Thermal model layout of 1A device

In Fig. 18, (A) on epi layer structure; 1.5μm-thick GaN/3.45μm-thick AlGaN/GaN superlattice and AlN (B) which rests on a 240μm-thick Si substrate (C). There is a 1 μm-thick layer (D) between the Si substrate and thermal chuck (E), which represents the thermal resistance between these parts. Inset: Device layout showing heat flow equal to power dissipated applied to 2D heaters in GaN channels between the anode and cathode fingers.

the silicon layer while ΔT is insignificant across all layers of the superlattice for the 1A, 2A and 4A diodes. The thermal chuck was set to a temperature of 24°C. To simulate diode power dissipation at the three power densities used experimentally, a heat flow equal to the power dissipated in the device was applied to 2D heaters within the GaN channels between the anode and cathode fingers shown in Fig. 18 (inset).

3.3 Measurements and Observations

Raman thermography was used to obtain submicron resolution temperature information in the 2-DEG at various power levels, and IR imaging was used for thermal mapping across the die [27]. The device was held at a controlled 24^{o}C on a chuck and biased under DC conditions. The Raman thermography technique was preferred for determining device temperature over electrical methods because the temperatures measured by electrical methods average over the entire active region of the device and thus tend to underestimate the peak temperatures in the channel. Raman Thermography exploits the temperature dependence of phonon frequencies to determine the channel and substrate temperature of the device. It is a non-invasive, non-destructive temperature measurement technique based on the Raman peak shift due to the temperature change. The measurements are highly repeatable

and the technique is widely used in modern experimental research. The technique has a temperature accuracy of ±5-10°C and spatial resolution of better than 1μm [21]. Single spot and scanned measurements were performed. IR thermal imaging is suitable for investigating the temperature distribution within an AlGaN/GaN-on-Si device but has its challenges for accurately measuring the absolute temperatures because the Si substrate is transparent to the IR radiation [18].

The temperature coefficient of an SBD was measured (Fig. 20) to be -1.95mV/^{0}C, similar to that of a planar silicon diode. Therefore, SBDs can be used as the temperature sense elements. In the layout floor plan of a HEMT with on-chip thermal protection circuit, it is best to place the temperature sense diodes at a location where the heat rise is the quickest. This is to capture the onset of heat rise as quickly as possible and activate the protection circuit. To identify the ideal location for placement of sense diodes to observe a significant temperature rise, large gate width GaN diodes with 1A, 2A, 4A and 8A current ratings operating under DC bias conditions well beyond the turn-on voltage were used. Thermal crosstalk between the fingers was investigated by measuring the temperature in the non-active area between the anode and cathode fingers. Fig. 19 shows discoloration in the center of the 4A and 2A diodes after operation of the device above the recommended maximum current level. This is heat-induced damage. For the same time scale of 100μs and relatively the same power density, the smaller 1A diode did not show any damage while the metal damage on the large device was observed to progress with time. Temperature difference between the middle and edge channel ΔT vs Device Size and Peak Temperature versus

Power Density of the diodes obtained by Raman thermography are shown in Figures 21 and 22 respectively. Figs. 23-27 show the simulated and experimental results of temperature difference (between the center and the edge) versus power dissipation and IR images of 1A, and 8A diodes. There is good agreement between measured and simulated values for the 1A, 2A and 4A diodes. A 13^0C discrepancy was observed at high power density (0.3W/mm) between the simulation and measured values for the 8A diode. This could be due to current redistribution across the large diode, either due to current spreading in the metal, or the temperature dependent electrical resistance in the 2DEG channel. However, this agreement is still good within the margin of error. In other words, the larger the device, the larger possible electro-thermal effects may be. Nevertheless, reasonable agreement with the simplified thermal model was obtained.

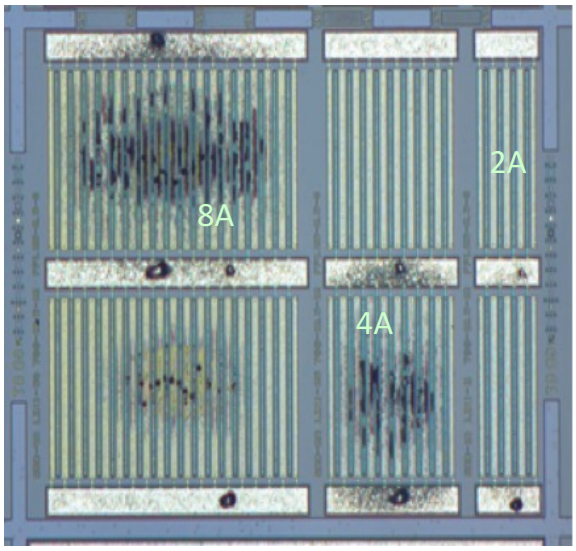

Figure 19: Thermally induced damage

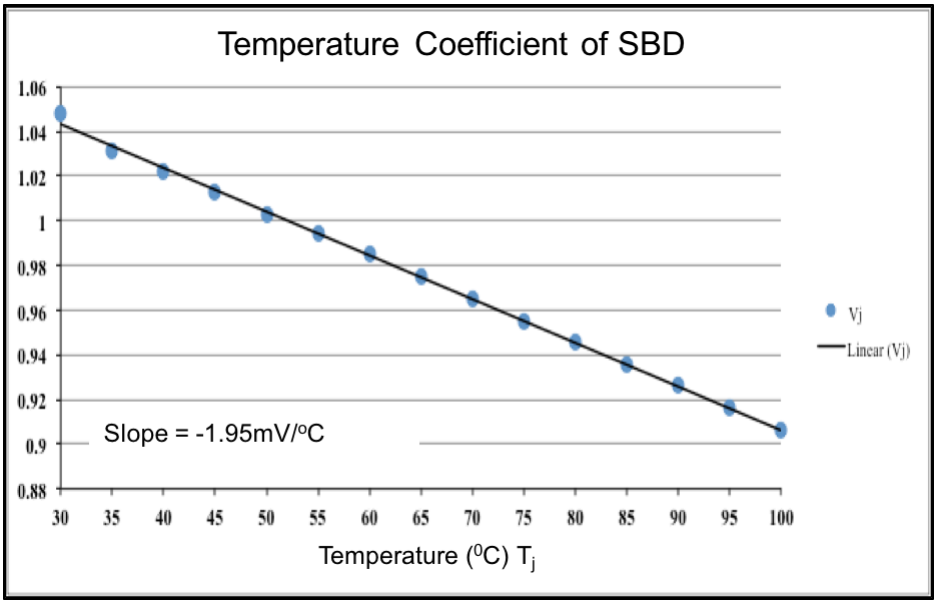

Figure 20: Temp. Coeff. GaN SBD

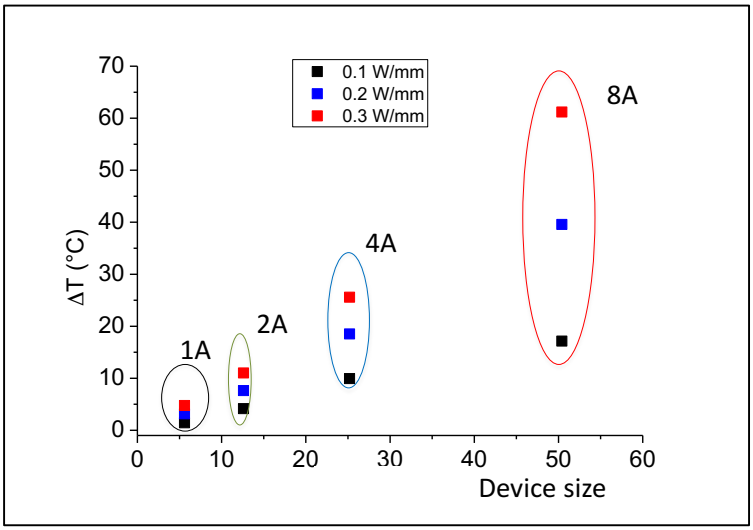

Figure 21: ΔT vs Device Size

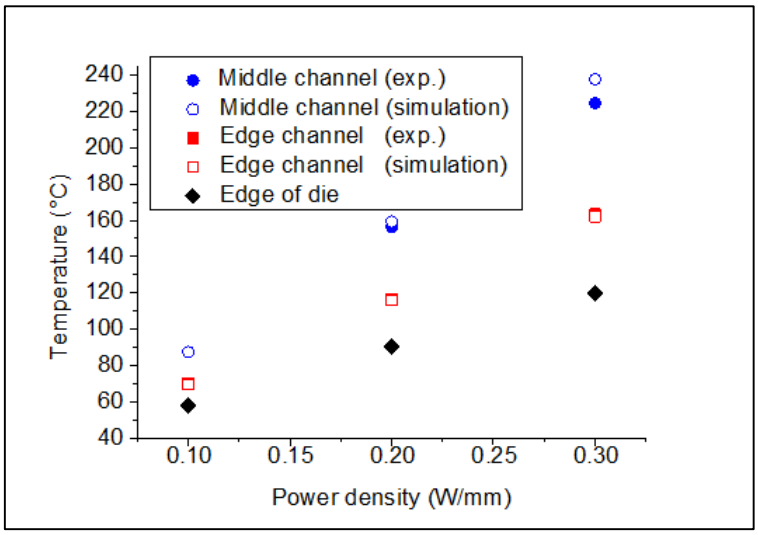

Figure 22: Peak Temp. vs Power Density

The experiments on several devices quantitatively confirmed that the central fingers do indeed heat up the most. Measurements indicate that the temperature difference between the center of the die and edge of the die can be as high as 60^0C at the high power densities considered here. The absolute temperature in the channel was measured at a peak of 225^0C, which is substantially higher than the typical commercial rating of 150^0C for Si MOSFETs. The high temperature measured is mostly due to the high thermal resistance R_{th} between the wafer and the chuck. With a solder die attach, the temperature would be substantially lower. Even though GaN-on-Si devices are expected to be able to operate at temperatures higher than Si MOSFETs, the peak temperature may be limited by the choice of package. The relationship between the total power dissipation and R_{th} is given by

$$P_{tot} = \frac{T_{jmax}-25}{R_{th(max)}} = I_{Dmax}{}^2 R_{ds(on)Tjmax}$$

$$P_{tot} = \frac{T_{jmax} - 25}{R_{th(max)}} = (I_{Dmax})^2 * R_{ds(on)T_{jmax}}$$

$$\Delta T = P * R_{th}$$

$$\Delta T = L * J_P$$

where L = number of fingers and J_p = power density in each finger.

3.4 Simulation and Experimental results of 1A and 8A Devices

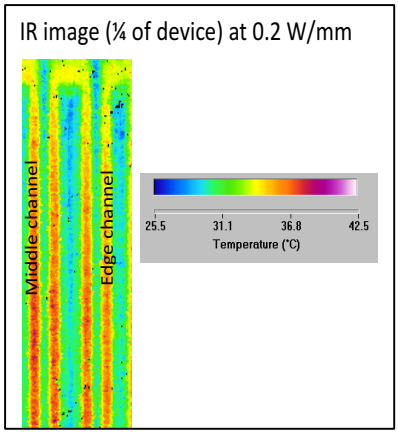

Figure 23: 1A diode IR Image at 0.2W/mm

Temperature uniform from middle to edge channel

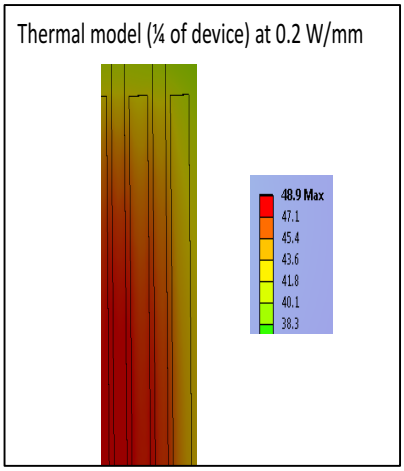

Figure 24: 1A Diode thermal model.

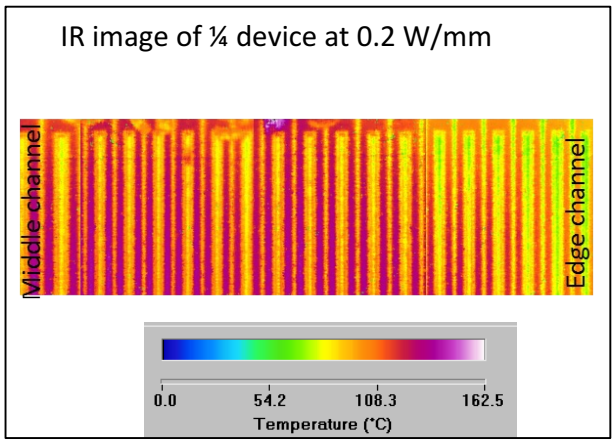

Figure 25: 8A Diode IR Image

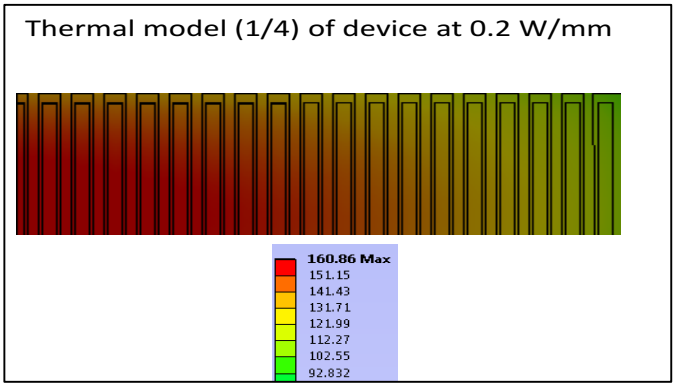

Figure 26: 8A Diode thermal model

Temperature non-uniformity significant

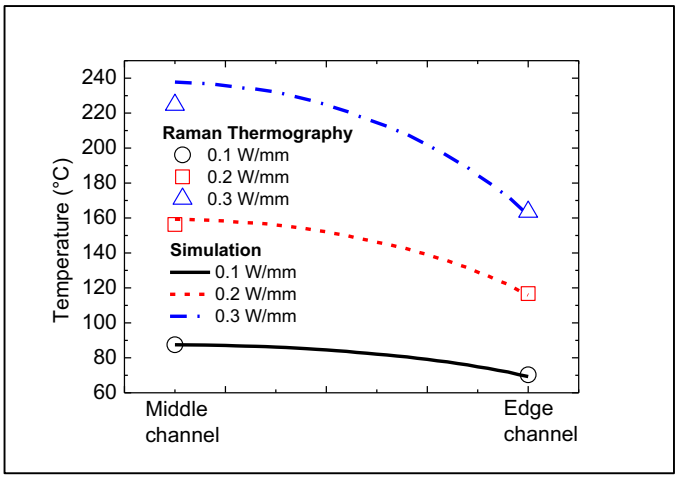

Figure 27: Temperature drop from middle to edge channel

The temperature drop is significant at 0.3W/mm

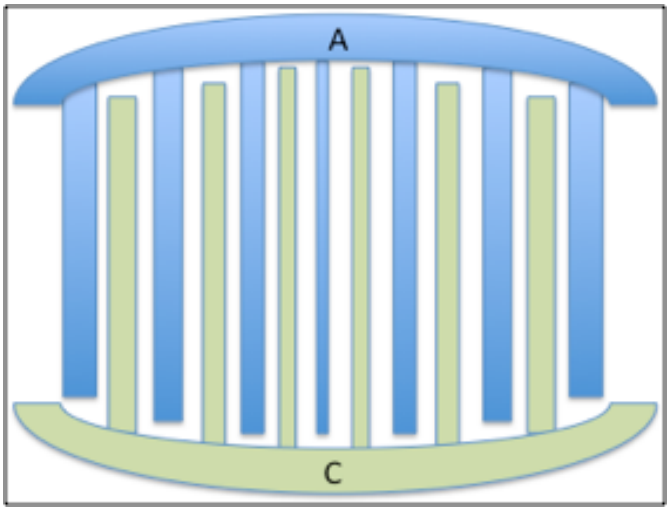

Figure 28: Alternative layout concept

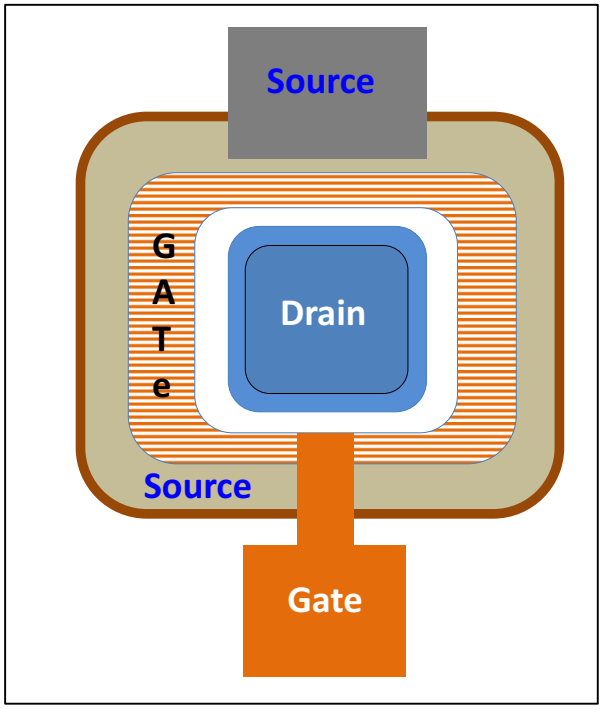

Figure 29: Square-gate layout[14]

Experimental results indicate that the device design and layout may need to achieve a more controlled current flow to enable constant temperature over the whole device area. This may be of benefit because the output power of a high voltage HEMT scales with the number of fingers in the layout. By designing the

fingers of different widths such that the power dissipated in the central and lateral fingers is less uniform, the localized thermal heating in the center part of the device can be reduced. This concept is illustrated in Fig. 28. An alternative is the square gate layout shown in Fig. 29 [28]. Applied voltage, the number of fingers and the finger pitch determine the maximum temperature rise in a device. It is worth noting that there is a trade-off between area, capacitance and thermal uniformity when optimizing for minimum self-heating. The heat distribution profile obtained from the measurements confirmed that the ideal location for placement of sense diodes is at the center of the die.

Chapter 4

Electro-Thermal Modeling of GaN-on-Si Schottky Barrier Diode and HEMT

Device models are needed to enable application development via circuit simulation and optimization. There are three types of compact models that can be used depending on the target design goals. Table based models use measured device data stored in large look-up tables. This is a very fast method, but extrapolation outside of the measured range is difficult and accurate scaling to other device dimensions cannot be done. Empirical models use whatever mathematical functions that can give a good fit to data, but parameters are not physically meaningful, scaling is not physical, and extrapolation is questionable. Physics based models use equations derived from modelling physical phenomena. They are complicated and difficult to solve, but parameters are physically meaningful, scaling is physical and extrapolation is reliable. This is the best method to extract models that can be used with confidence in device and circuit design. Surface potential based physical models use a single expression for all regions of operation of the device. It is the most preferred approach in MOS modelling [29]. A modified form of the Angelov model for GaN-on-Si power switches was used in this study during the early phase of design when the physics based models were not available, but eventually, physics based scalable models were used [30] [31].

In this chapter, development of physics-based electro-thermal models of GaN Schottky diode and HEMT are discussed. GaN Schottky diodes and HEMTs are both made in the same process technology and thus use the same stack of epitaxial layers of GaN and AlGaN. A super-lattice epitaxial structure on top of a silicon <111> substrate consists of more than hundred and twenty-five layers of nanometer scale packed in less than 4μm of thickness. Main layers in the stack are GaN layer, the semi-insulating AlGaN layer, a thin GaN cap layer and nitride on top. At the interface between the main GaN layer and AlGaN layer, a two-dimensional gas (2-DEG) is formed. As shown in Fig. 30, the region underneath the anode makes a Schottky contact to the 2-DEG, while the region under the cathode makes an Ohmic contact to the 2-DEG, thus forming a Schottky Barrier Diode. In case of a HEMT, the region under the gate makes a Schottky contact to the 2-DEG, while the regions underneath the source and drain make an Ohmic contact to the 2-DEG.

For both these devices, the models are electro-thermal since they take into account self-heating. The self-heating is implemented with a temperature dependent parameter set in the electrical model in combination with a thermal network, in which the power dissipation is calculated. The model equations include physical geometry scaling rules for the gate length, the finger width, the gate to drain distance, the anode length, the anode to cathode distance, the gate to source distance and number of devices in parallel. In short, the models support description of currents and capacitances, geometry scaling and self-

heating making them useful for circuit design for the analog and digital circuits developed in this work.

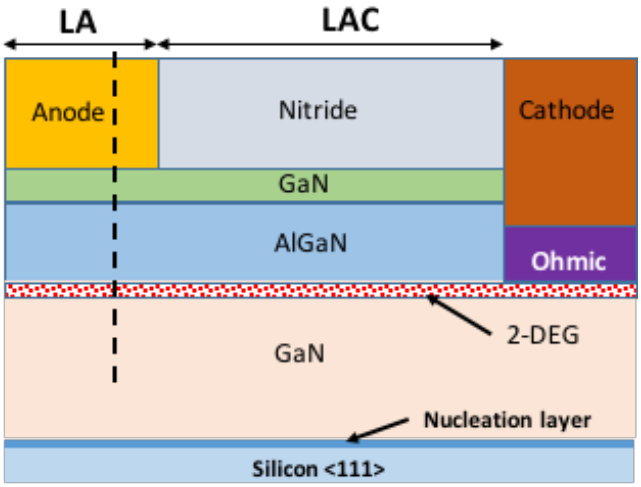

Figure 30: 2D Cross Section of a Diode

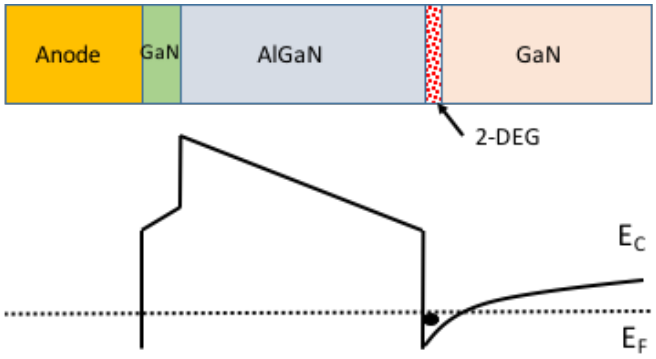

Figure 31: 1-D cross-section underneath the anode

4.1 Diode Electrical Model

The electrical model of the GaN Schottky diode is a sub-circuit with five elements and three internal nodes as shown in Fig. 32.

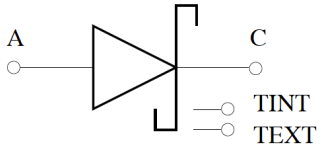

Figure 32: Diode Symbol

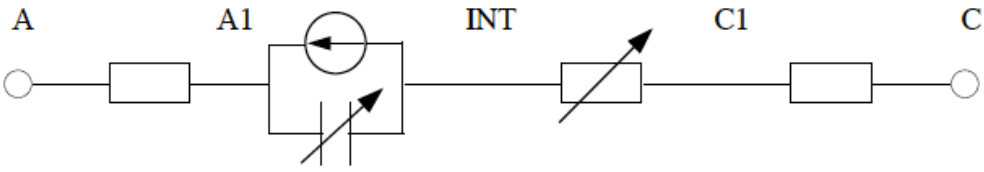

Figure 33: Equivalent circuit of the electro-thermal GaN Schottky diode model

The Schottky diode is modeled as a current source and a nonlinear capacitance between nodes A1 and INT. The 2-DEG resistance between the anode and cathode is modeled by the nonlinear resistance between nodes INT and C1 [32]. Metal resistances of the anode and cathode are modeled by the resistances between nodes A-A1 and C-C1 respectively. The instance parameters LA, LAC, WF, NCELL and PCELL specify the geometry of the simulated diode.

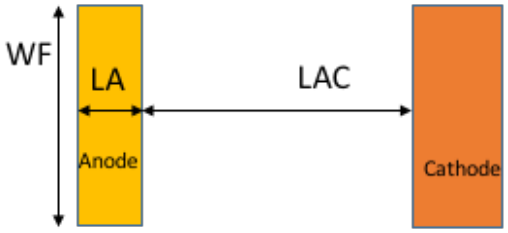

Figure 34: Top View of the device

Geometry scaling is achieved by using the appropriate scaling factors with respect to the reference device. For example,

$$K_{NCELL} = \frac{NCELL}{NCELLR}$$

$$K_{WF} = \frac{WF}{WFR}$$

$$K_{LA} = \frac{LA}{LAR}$$

$$K_{LAC} = \frac{LAC}{LACR}$$

Similarly, temperature scaling is achieved by a scaling factor using (T_0 *or* $\boldsymbol{DTA}$) the offset between the Celsius and Kelvin temperature scale, and T_A the ambient temperature of the circuit simulator.

$$T_{KR} = T_0 + TR$$

$$T_{KD} = T_0 + T_A + \boldsymbol{DTA} + \Delta T_{KSH}$$

where ΔT_{KSH} is the delta when the thermal model switch is turned on.

Temperature scaling of thermal voltages is given by

$$\emptyset_{T_{KD}} = \frac{k_B.T_{KD}}{q}$$

$$\emptyset_{T_{KR}} = \frac{k_B.T_{KR}}{q}$$

The scaled parameters are in turn used for scaling forward and reverse current, breakdown voltage and parasitics of the diode.

Table 4: Diode Electrical Instance Parameters

Parameter	Unit	Default	Min.	Max.	Description
LA	m	1.10^{-6}	1.10^{-8}		Length anode
LAC	m	12.10^{-6}	1.10^{-8}		Distance anode - cathode
WF	m	100.10^{-6}	1.10^{-8}		Finger width
NCELL	-	1	1		Number of cells
PCELL	m	50.10^{-6}	1.10^{-8}		Pitch of cells

Thermal model

A thermal network is used in the thermal model of the GaN Schottky diode to include the effect of self-heating on its electrical behavior during forward operation where the currents are large. The power dissipated in the diode (P_{diss}) is assigned to the current source in the thermal network. The temperature increase due to the dissipated power is calculated. The model parameters are recalculated at the diode temperature, which is equal to the sum of the ambient temperature and the temperature increase due to self-heating (ΔT). The recalculated diode parameters result in a different value of dissipated power. The final dissipated power and temperature of the diode are known after the diode model and thermal network have converged.

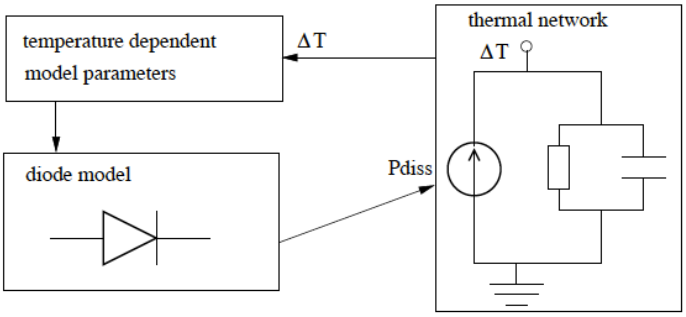

Figure 35: Thermal network in the GaN Schottky diode model.

The thermal model can be turned off by externally grounding both nodes TINT and TEXT.

Table 5: Diode Thermal model instance parameters

Parameter	Unit	Default	Min	Max	Description
SWET	-	1	0	1	Thermal network switch. 0 = OFF
RTHSW	-	0	0	1	Flag for external thermal network. 0 = no
RTHCALC	-	0	0	2	Mode of operation. 0 = on-wafer, 1= finite thick substrate, 2 = user defined
DTA	K	0	-	-	Temperature offset from ambient
RTH	K/W	1.10^{-3}	1.10^{-8}	-	Thermal resistance if **RTHCALC** = 2
CTH	J/K	1.10^{-12}	0	-	Thermal capacitance if **RTHCALC** = 2

In this model, only the current transport due to thermionic emission (TE) is considered while ignoring thermionic field emission (TFE) and field emission (FE), since TFE and FE are significant only for low temperatures and/or narrow barriers. Current density in the TE regime is given by [33]

$$J_{TE}(V) = A * T^2 . exp\left(-\frac{\emptyset_B}{k_B.T}\right).\left[exp\left(\frac{V}{n_{if}.{}^{T}/_{q}}\right)\right]$$

where $A^* = \frac{4\pi q m_{eff} k_B^2}{h^3}$ is the Richardson constant, $\emptyset_B$ is the Schottky barrier height, and n_{if} is the ideality factor. Using the geometry scaling factors leads to the diode current equation given by

$$I\ (V) = \frac{NCELL}{NCELLR}.\frac{WF}{WFR}.\frac{LA}{LAR}.ISR.\left(\frac{T}{T_{KR}}\right)^2.exp\left(-\frac{\boldsymbol{PHIB}}{k_B.T}\right).\left[exp\left(\frac{V}{\boldsymbol{IDF}.k_B.T/q.}\right)-1\right]$$

where the Schottky barrier height ***PHIB*** and the ideality factor ***IDF*** are temperature dependent [34].

The nonlinearity of the 2-DEG resistance due to velocity saturation of electrons is modeled by limiting the current to a maximum value which scales with the finger width, and the number of devices in parallel. The linear resistance increases with the anode to cathode distance **LAC**, and decrease with the finger width **WF**, and number of devices in parallel **NCELL**. Fig. x illustrates the smoothing parameter **MEXP** used in the I-V characteristics to account for this nonlinearity.

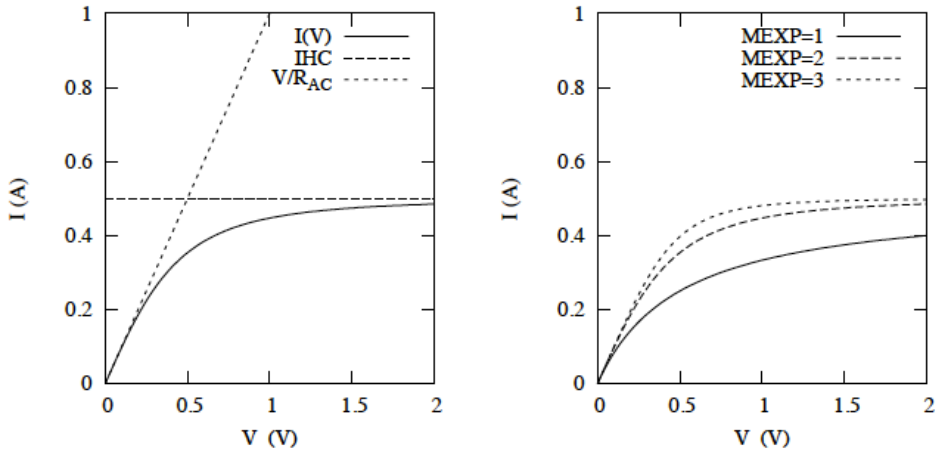

Figure 36: IV characteristics of a 0.5A diode

1Ω linear 2-DEG resistance with different values of the smoothing parameter.

In this model, charge formed underneath the anode and the diode capacitance are modeled empirically. The anode charge scales with the number of cells **NCELL**, and the area of the anode (**LA** and **WF**).

For a single diode, the heat is generated in a rectangular area at the surface defined by the finger width **WF** and the dimension of the lateral current flow $L_{TH,}$ approximately the same as **LAC**. This line source describes the heat source of a single diode cell. Thermal resistance scales inversely proportional to the finger width. Thermal resistance of a line source is given by [35]

$$R_{TH}^{no^{MH}} = \frac{1}{\boldsymbol{NCELL.WF}} \cdot \frac{1}{\pi\lambda} . ln\left(\frac{16.\boldsymbol{TSUBTH}}{2.\pi.L_{TH}}\right)$$

where λ is thermal conductivity and $\boldsymbol{TSUBTH}$ is the substrate thickness.

The electrical and thermal model parameter extraction was done by IV measurements (pulsed and non-pulsed, transient I at five temperatures between 25°C and 125°C. CV measurement was done at room temperature and f = 100kHz.

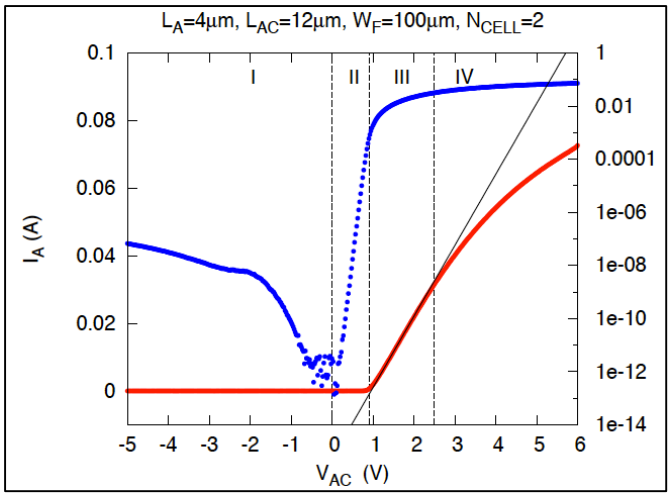

Figure 37: IV characteristics of a GaN Schottky diode

In Fig. 37, Region I: Reverse; Region II: Forward; Region III Linear series resistance; Region IV: Nonlinear series resistance

Model parameters prefactor **ISR**, the barrier height **PHIB**, ideality factor **IDF** and their temperature dependences are extracted from the diode current. Parameters for the nonlinear resistance are extracted in region IV. These are the saturation current **IHC** and its temperature dependence, and the smoothing parameter **MEXP**. The non-pulsed IV measurements and transient I measurements are used for extraction of self-heating parameters. The AC parameters are determined from the CV measurements. The following figures illustrate the comparison of measurements to model at different temperatures. On-wafer measurements were done on diode variants with LAC = 4, 8, 10, 12 and 16μm. The anode length was the same for in all the structures LA = 4μm. A good agreement between measurements and simulations was obtained. In the pulsed IV-measurements, a pulse width of 600 ns and a pulse period of 100μs was used. The measured increase in on-resistance with temperature and anode to cathode distance LAC was accurately captured by the model.

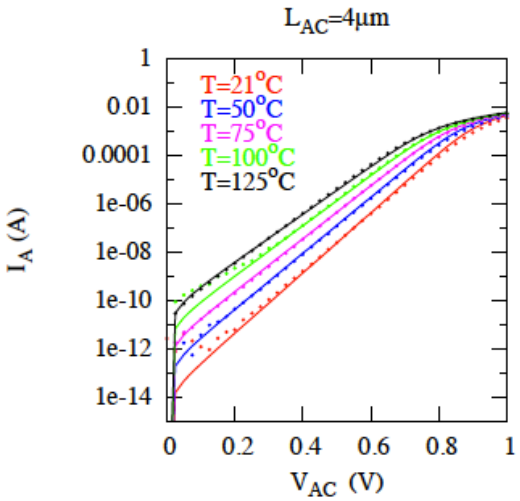

Figure 38: non-pulsed IV measurements (symbols) to model (solid lines)

LAC = 4µm, WF = 100µm, NCELL = 2, LA = 4µm,

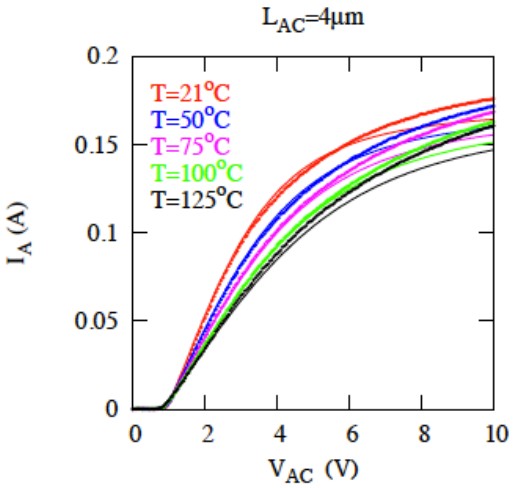

Figure 39: Pulsed IV measurements (symbols) to model (solid lines)

LAC = 4µm, WF = 100µm, NCELL = 2, LA = 4µm,

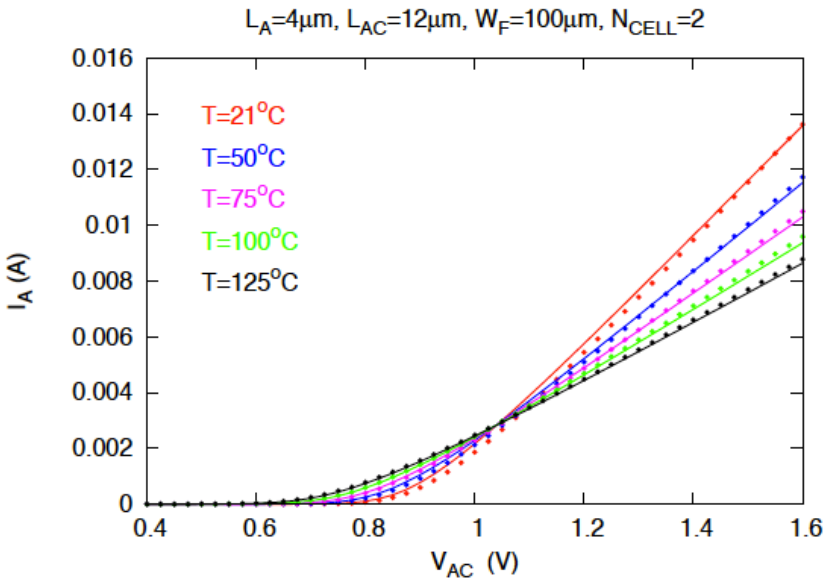

Figure 40: IV characteristics at the temperature inversion point

Current increases at lower bias conditions (follows thermionic emission theory) and decreases at higher bias conditions (due to increase in on-resistance with temperature).

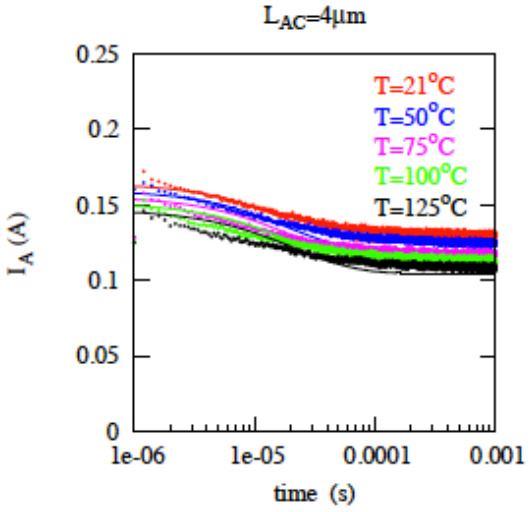

Figure 41: Measurements of decrease in current due to self-heating

LAC = 4µm, WF = 100µm, NCELL = 2, LA = 4µm,

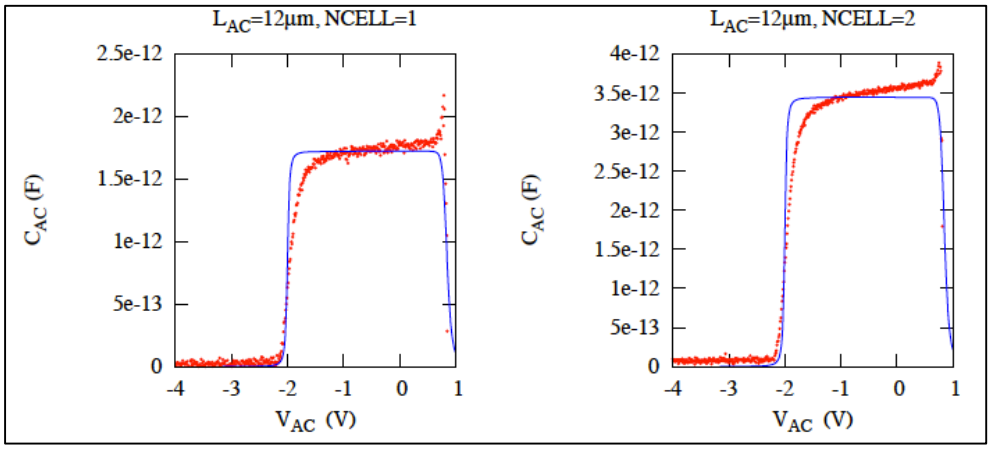

Figure 42: Comparison of CV measurements (symbols) to model (solid lines)

at room temperature and f = 100 kHz. WF = 100µm, LA = 4µm

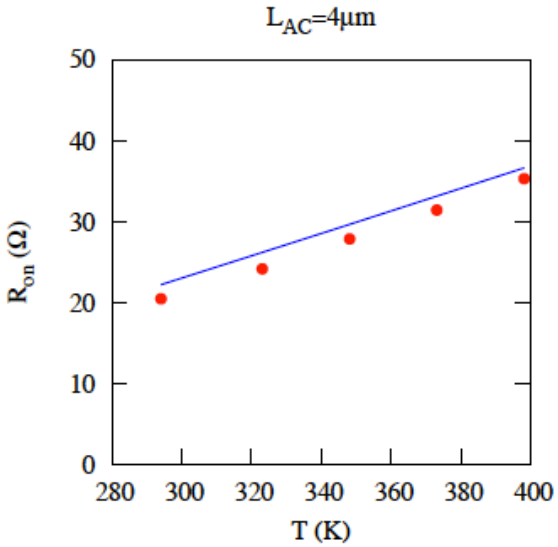

Figure 43: On-resistance as a function of temperature

Extracted from measurements (symbols) and model (sold line).

LA = 4µm, WF = 100µm, NCELL = 2

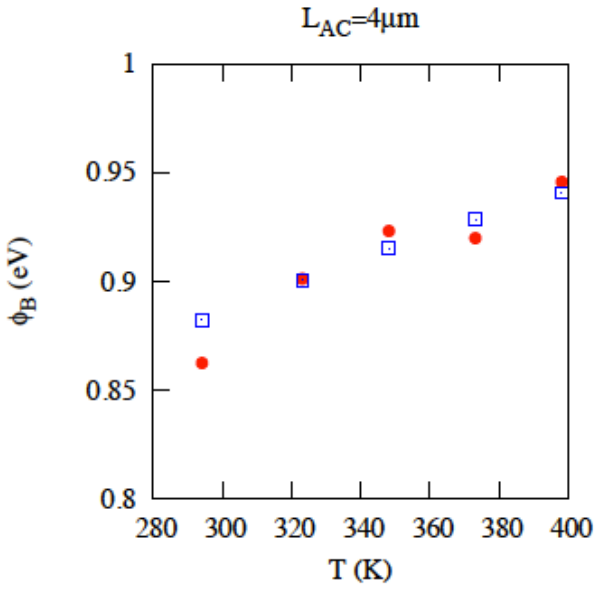

Figure 44: Schottky Barrier Height as a function of temperature

Extracted from measurements (red symbols) and model (blue symbols). LA = 4µm, WF = 100µm, NCELL = 2

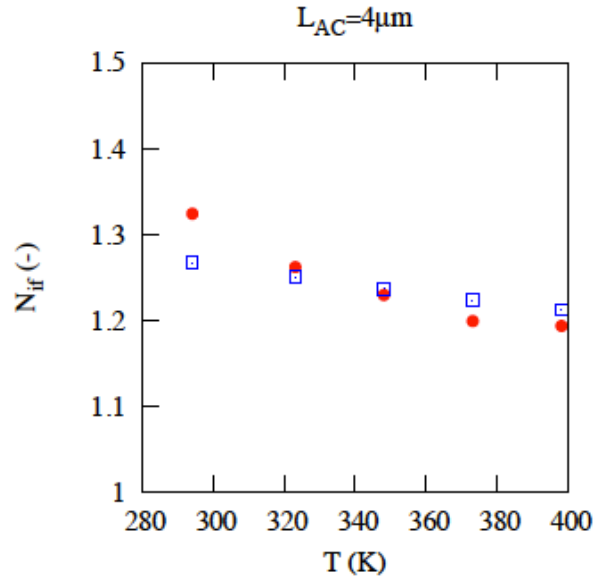

Figure 45: Ideality factor as a function of temperature

Extracted from measurements (red symbols) and model (blue symbols). LA = 4µm, WF = 100µm, NCELL = 2,

Dynamic behavior of the Schottky diode

The dynamic behavior of the diode was characterized using a 32mm diode array, consisting of 64 fingers with a finger width WF = 0.5mm, LA = 11.25µm, LAC = 12µm, f = 200kHz and f = 1MHz The test set up was as follows:

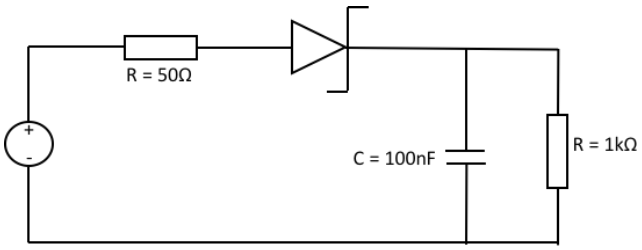

Figure 46: Test circuit for dynamic behavior of a GaN Schottky diode

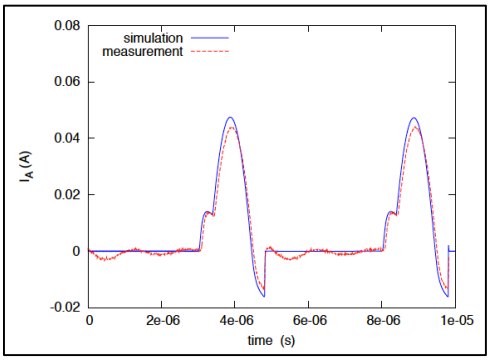

Figure 47: Anode current as a function of time f = 200 kHz

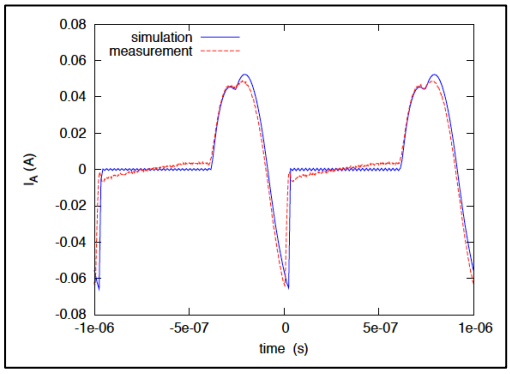

Figure 48: Anode current as a function of time f = 1 MHz

Summary of Model parameters

Table 6: Summary of Diode model parameters					
Diode parameters					
Name	Unit	Default	Min.	Max.	Description
ISR	A	1	0	-	Diode current in reverse (thermionic emission)
PHIB	eV	0.8	0	-	Schottky Barrier Height
STPHIB	-	1	0		Temperature scaling PHIB
IDF	-	1	1.0^{-3}	5	Ideality factor
STIDF	-	0	-	-	Temperature scaling IDF

Series resistance of 2-DEG					
Name	Unit	Default	Min.	Max.	Description
RAC	Ω	1.0	1.10^{-6}	-	Series resistance 2-DEG
STRAC	-	0	0	-	Temperature scaling RAC
IHC	A	1.0	1.10^{-6}		Saturation current of series resistance 2-DEG
STIHC	-	0	0	9	Temperature scaling IHC
MEXP	-	1	0	-	Smoothing factor

Capacitance					
Name	Unit	Default	Min.	Max.	Description
CAPA	F	$1.0.10\text{-}^{15}$	0	-	Anode capacitance

Diode voltage					
Name	Unit	Default	Min.	Max.	Description
VTH	V	0	-	-	Threshold voltage of 2-DEG formation underneath anode

Self-heating related parameters					
Name	Unit	Default	Min.	Max.	Description
TTH	s	1.10^{-6}	1.10^{-12}	-	Thermal time constant of reference device at TR
ATH	-	0	0	-	Temperature scaling coefficient of thermal resistance
EXRTH	-	0	0	1	Switch to include the effect of self-heating on thermal resistance
TSCALE	-	1	1	-	Convergence parameter for built-in thermal network
RTHCOR	-	0	0	-	Switch to include mutual heating between cells (1 = ON)
TSUBTH	m	250.10^{-6}	1.10^{-6}	-	Substrate thickness for thermal model (RTHCOR = 1)
KAPPA	W/(Km)	150	1	-	Thermal conductivity used for infinite thick substrate (RTHCALC = 1)
LTH	m	10.10^{-6}	1.10^{-8}	-	Width of heat source used for infinitely thick substrate (RTHCALC = 1)

4.2 GaN Hetero-Junction Field Effect Transistor (H-JFET) Model

For circuit design and SPICE simulations purposes, the GaN-on-Si HEMT in this work is modeled as an H-JFET.

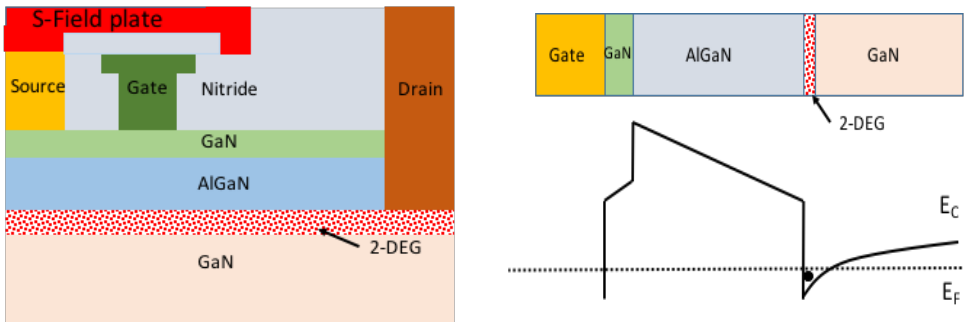

Figure 49: 2-D cross-section and 1-D cross-section underneath the gate

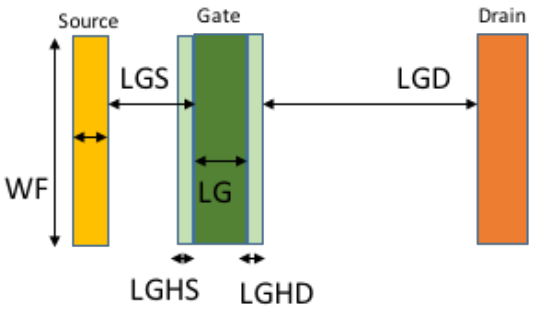

Figure 50: Top view of the HEMT

HJFET Electrical Model

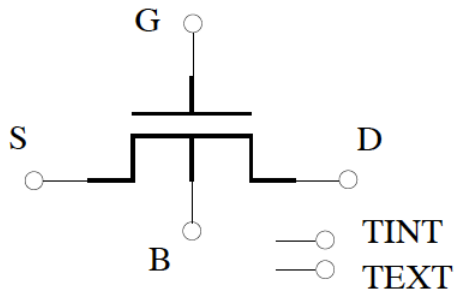

Figure 51: Symbol of the electro-thermal GaN HJFET model

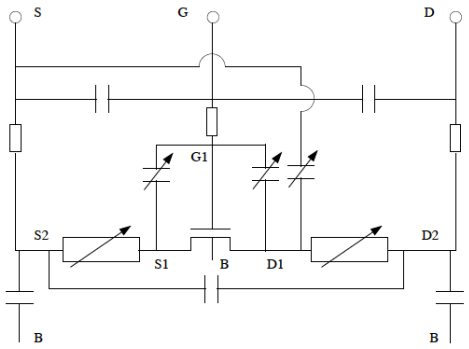

Figure 52: Equivalent circuit of the electro-thermal GaN HJFT model with external nodes D,G,S, and B and internal nodes D2,D1,G1,S1, and S2

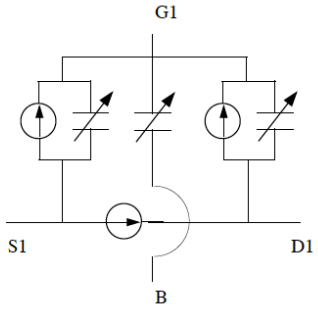

Figure 53: Equivalent circuit of the gate foot model.

The sub-circuit model of the GaN HJFET consists of a transistor model for the gate foot, non-linear and linear elements with five internal nodes a mentioned in

Fig. 53 above [36]. The transistor model between nodes D1, G1, and S1 describes the region underneath the gate foot which consists of three current sources, and a non-linear charge model. The current source between D1 and S1 describes current transport in the 2-DEG underneath the gate foot. The Schottky diode current is modeled with the current source between nodes G1-S1 and G1-D1. The non-linear charge model of the gate foot is represented by the three non-linear capacitances. The 2-DEG of the access region is modeled with non-linear resistances between nodes S2-S1 and D1-D2. The non-linear capacitances between nodes G1-S1 and G1-D1 form the capacitances of the gate head field plate. The metal-1 field plate is modeled by a non-linear capacitance between nodes S and D1. Metal and contact resistances of the drain, gate and source are also modeled with resistances between nodes D-D2, G-G1 and S-S2. Parasitic capacitances between gate and source metal as well as between gate and drain metal are also modeled. Finally, the capacitances between S2 and B, and D2 and B describe the capacitance between the substrate to source and substrate to drain respectively.

To derive the drain current, gate current and charges, first a surface potential for the gate foot is derived. The gate stack is comprised of a metal contact forming a Schottky contact with a GaN cap layer, with a barrier height ϕ_B, a semi-insulating AlGaN layer, and the main GaN layer. A 2-DEG forms between the main GaN layer and AlGaN layer. Polarization charges are induced by the spontaneous polarization effect in the GaN layer. Polarization charges in

the AlGaN layer are induced by spontaneous and piezoelectric polarization, which occurs due to strain. The polarization charges are given by [15]

$$\sigma_{GaN}^{pol} = |P_{GaN}^{SP}|$$

$$\sigma_{AlGaN}^{pol} = |P_{ALGaN}^{SP} + P_{AlGaN}^{PE}|$$

where $|P_{GaN}^{SP}|$ is the spontaneous polarization of GaN, $|P_{AlGaN}^{SP}|$ the spontaneous polarization of AlGaN, and $|P_{AlGaN}^{PE}|$ the piezo-electric polarization of AlGaN resulting from strain.

An equation for surface potential is derived by calculating the electric fields in the GaN cap layer and the AlGaN layer using Gauss' law. The electric field in the GaN cap layer and AlGaN layer are given by

$$E_{GaN} = -\left(\frac{\sigma_s}{\epsilon_{GaN}}\right)$$

$$E_{AlGaN} = -\left(\frac{\sigma_{AlGaN}^{pol} - \sigma_{GaN}^{pol} + \sigma_s}{\epsilon_{AlGaN}}\right)$$

where σ_s is the charge density due to electrons in the 2-DEG and ionized acceptors in the main GaN layer. The surface potential equation works out to be

$$V_{GB} - V_{FB}^{SB} - \psi_s = -\frac{\sigma_s}{C_{HJ}'}$$

where $C_{HJ}' = \frac{C_{GaN}' . C_{AlGaN}'}{C_{GaN}' + C_{AlGaN}'}$ is the capacitance of the heterojunction. The distribution of charges in the AlGaN-GaN stack of the Schottky barrier is shown in the fig. below.

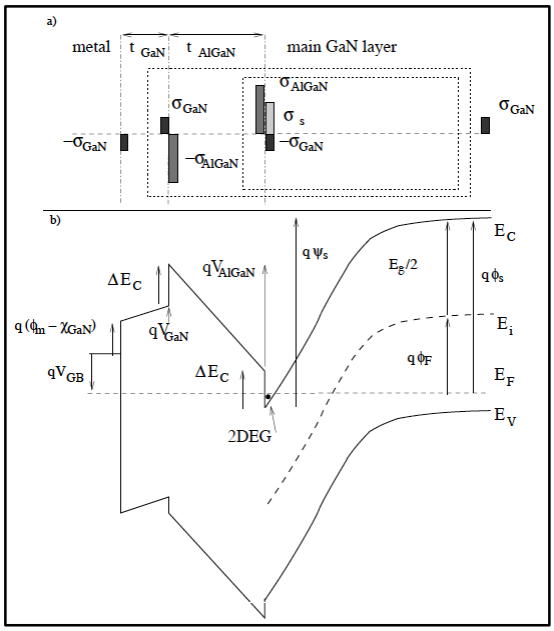

Figure 54: Distribution of charges in the gate stack

Source [15]

The unified model for 2-DEG charge density is given by [37]

$$n_s = \frac{C_g V_{go}}{q} \frac{V_{go} + V_{th}\left[1 - ln(\beta V_{gon})\right] - \frac{\gamma_0}{3}\left(\frac{C_g V_{go}}{q}\right)^{2/3}}{V_{go}\left(1 + \frac{V_{th}}{V_{god}}\right) + \frac{2\gamma_0}{3}\left(\frac{C_g V_{go}}{q}\right)^{2/3}}$$

where $V_{go} = V_g - V_{off}$ and γ is an experimentally determined parameter. This expression is also extended to sub-threshold regime and used as a basis for drain-current model.

Geometry scaling is achieved by using the appropriate scaling factors with respect to the reference device. For example,

$$K_{LGHD} = \frac{LGHD}{LGHDR}$$

$$K_{LGS} = \frac{LGS}{LGSR}$$

For gate foot geometry scaling,

$$BET_g = BET.\frac{K_{WF}}{K_{LG}}$$

$$ISR_g = ISR.K_{WF}.K_{LG}$$

$$CHJ_g = CHJ.K_{WF}.K_{LG}$$

Geometry scaling for gate heads, access regions, M1 field plate, parasitic resistances and capacitances is done by using appropriate scaling factors and relations as summarized in table x.

Similarly, temperature scaling is achieved by a scaling factor using (T_0 *or* $\boldsymbol{DTA}$) the offset between the Celsius and Kelvin temperature scale, and T_A the ambient temperature of the circuit simulator.

$$T_{KR} = T_0 + TR$$

$$T_{KD} = T_0 + T_A + \boldsymbol{DTA} + \Delta T_{KSH}$$

where ΔT_{KSH} is the delta when the thermal model switch is turned on.

Temperature scaling of thermal voltages is given by

$$\emptyset_{T_{KD}} = \frac{k_B.T_{KD}}{q}$$

$$\emptyset_{T_{KR}} = \frac{k_B.T_{KR}}{q}$$

Gate foot temperature scaling parameters are calculated by equations such as

$$PHIB0_T = PHIB0.\left(\frac{T_{KD}}{T_{KR}}\right)^{STPHIB0}$$

$$ISR_{gT} = ISR_g\left(\frac{T_{KD}}{T_{KR}}\right)^2$$

$$IDF_T = IDF.\left(\frac{T_{KD}}{T_{KR}}\right)^{STIDF}$$

etc.

Access regions temperature scaling parameters are RGS_{gT}, RGD_{gT} and IHC_{gT} are also calculated using $STR2DEG$ scaling factors.

The scaled parameters are in turn used for calculating currents in all regions of operation, capacitances, and power dissipation. The equations for HEMT are much more complicated than those for the diode because of involved second order effects of drain induced barrier lowering (DIBL), drain saturated voltage, surface potential and inversion charge at drain and source, channel length modulation, mobility reduction, interchange currents in the access regions, parasitic resistances and capacitances.

The equations for thermal model give expressions for thermal resistance from line source (including mutual heating) for finite and infinite substrate thickness, thermal capacitance. Finally, temperature scaling of R_{th} and C_{th} is calculated from $T_{0,}\ T_A, DTA, EXRTH, T_{KR}, and\ \Delta T_{KSH}$.

Table 7: HEMT model Instance Parameters

Instance parameters geometry scaling					
Parameter	Unit	Default	Min.	Max.	Description
NCELL	-	1	1.10^{-8}	-	Number of cells
WF	m	100.10^{-6}	1.10^{-8}	-	Finger width
PCELL	m	50.10^{-6}	1.10^{-8}	-	Pitch of cells
LG	m	1.10^{-6}	1.10^{-8}	-	Gate length
LGHS	m	1.10^{-6}	1.10^{-8}	-	Length gate-source head
LGHD	m	1.10^{-6}	1.10^{-8}	-	Length gate-drain head
LGS	m	1.10^{-6}	1.10^{-8}	-	Distance gate to source
LM1	m	1.10^{-6}	1.10^{-8}	-	Length M1 field plate

Thermal Model

Self-heating is most significant in the saturation region where the currents are large. The thermal model takes into account the effect of self-heating in the transistor on its electrical behavior by using a thermal network.

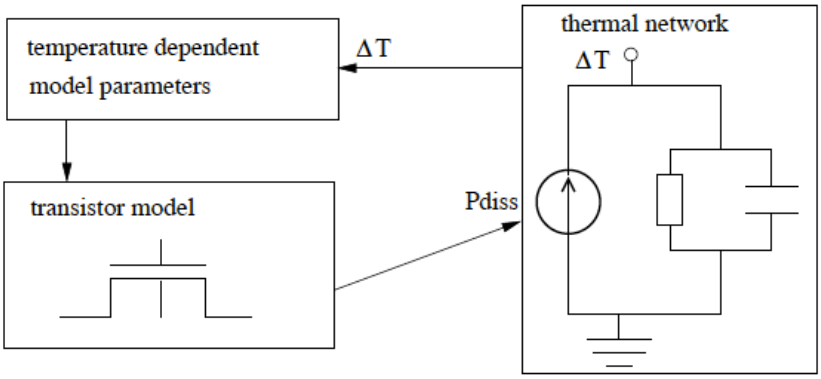

Figure 55: Thermal network

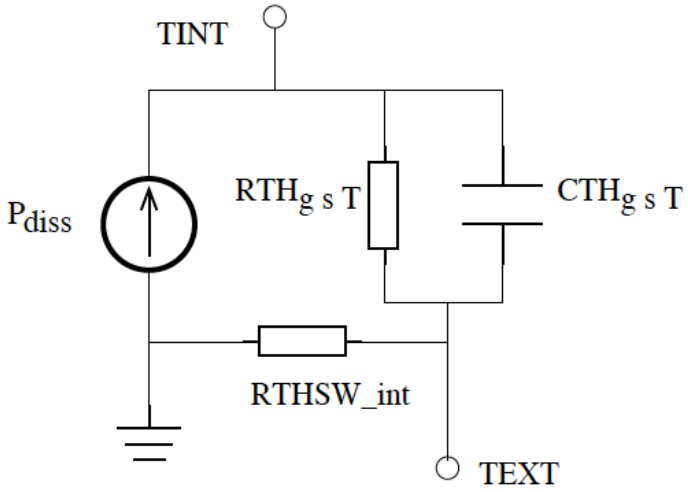

Figure 56: Equivalent circuit

Table 8: HEMT model thermal instance parameters

Instance parameters thermal model					
Parameter	Unit	Default	Min.	Max.	Description
SWET	-	1	0	1	Switch for thermal network 0 = OFF
RTHCALC	-	0	0	2	Flag to select mode of operation 0 = on-wafer, 1 = infinitely thick substrate, 2 = user defined
DTA	K	0	-	-	Temperature offset from ambient
RTH	K/W	1.10^{-3}	1.10^{-8}	-	Thermal resistance if RTHCALC = 2
CTH	J/K	1.10^{-12}	0	-	Thermal capacitance if RTHCALC = 2

The drain current has two components to it: Drift current and Diffusion current [38]

$$I_D = I_{drift} + I_{diffusion}$$

$$I_D = -\frac{WF}{LG}\mu\left[Q'_{inv}.(\psi_S^D - \psi_S^S\right] - \phi T_{KD}.(Q_{inv}^D - Q_{inv}^S)]$$

$$I_D = \frac{NCELL}{NCELLR}.BET.\frac{WF}{WFR}.\frac{LGR}{LG}\left[-V'_{inv}.(\psi_S^D - \psi_S^S + \phi T_{KD}.(V_{inv}^D - V_{inv}^S)\right]$$

where ϕT_{KD} the thermal voltage and BET is the gain factor,

$\psi_{inv}^{S,D}$ and $V_{inv}^{S,D}$ surface potential and inversion charge at the source and drain respectively.

As in the case of the diode, in this model, only the current transport due to thermionic emission (TE) is considered while ignoring thermionic field emission (TFE) and field emission (FE), since TFE and FE are significant only for low

temperatures and/or narrow barriers. Current density in the TE regime is given by

$$J_{TE}(V) = A^*.T^2.exp\left(-\frac{\emptyset_B}{k_B.T}\right).\left[exp\left(\frac{V}{n_{if}.{}^{T}/_{q}} - 1\right)\right]$$

where $A^* = \frac{4\pi q m_{eff} k_B^2}{h^3}$ is the Richardson constant, $\emptyset_B$ is the Schottky barrier height, and n_{if} is the ideality factor. The Schottky barrier height is not constant across the GaN cap layer and AlGaN layers, so effective barrier height is used in deriving the current equation.

$$J_{TE}(V) = A^*.T^2.exp\left(-\frac{\phi_B^{eff}}{k_B.T}\right).\left[exp\left(\frac{V}{n_{if}.{}^{T}/_{q}} - 1\right)\right]$$

$$J_{TE}(V) = A^*.T^2.exp\left(-\frac{(PHIB0 - PHIB1.V_{inv})}{k_B.T}\right).\left[exp\left(\frac{V}{n_{if}.{}^{T}/_{q}} - 1\right)\right]$$

where $PHIB0 = \phi_B + \frac{\Delta E_c}{q}$ and $PHIB1 \simeq t_{cap}/(t_{AlGaN} + t_{cap})$

The final current equation including geometry scaling works out to

$$I(V) = \frac{NCELL}{NCELLR}.\frac{WF}{WFR}.\frac{LG}{LGR}.ISR.\left(\frac{T}{T_{KR}}\right)^2.exp\left(-\frac{(PHIB0 - PHIB1.V_{inv})}{K_B T}\right).exp\left[\left(\frac{V}{IDF.K_B.T/q}\right) - 1\right]$$

In the model, barrier height $PHIB0$ and IDF are made temperature dependent. The measurements are in line with these temperature dependencies. The charges in the gate foot model are calculated using Ward-Dutton partitioning [39] using

$$Q_{G1} = WF.\int_0^{LG} dxQ_g$$

$$Q_{s1} = WF.\int_0^{LG} dxQ_{ch}.\left(1 - \frac{x}{LG}\right)$$

$$Q_{D1} = WF.\int_0^{LG} dxQ_{ch}$$

$$Q_B = WF.\int_0^{LG} dxQ_b = -Q_{G1} - Q_{S1} - Q_{D1}$$

The terminal charges can be calculated, but the contribution of holes in the accumulation region is ignored in the capacitances in GaN HJFETs.

The resistances in the 2DEG in the source and drain access region are described by non-linear series resistances. The series resistance of an access region is non-linear due to velocity saturation of electrons in the 2DEG. The linear resistance increases with the length of the access regions LGS and LGD. The resistances decrease with the finger width WF and the number of devices in parallel NCELL. The non-linearity in the resistance is implemented by limiting the current to a maximum value, which scales with finger width WF, and the number of devices in parallel NCELL. In this model, charge and capacitance of the field plates are modeled empirically.

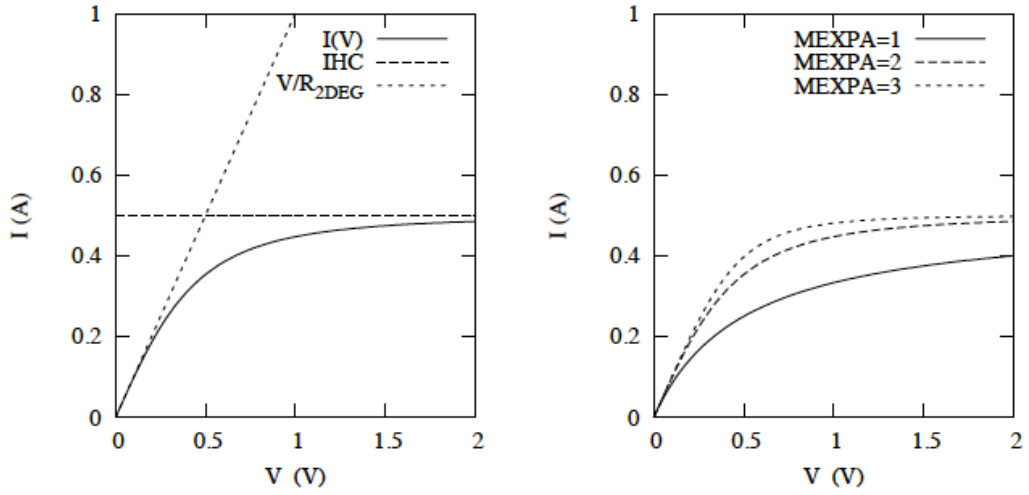

Figure 57: IV characteristics with R2DEG = 1.0 Ω and IHC = 0.5 A
and for different values of smoothing parameter MEXPA

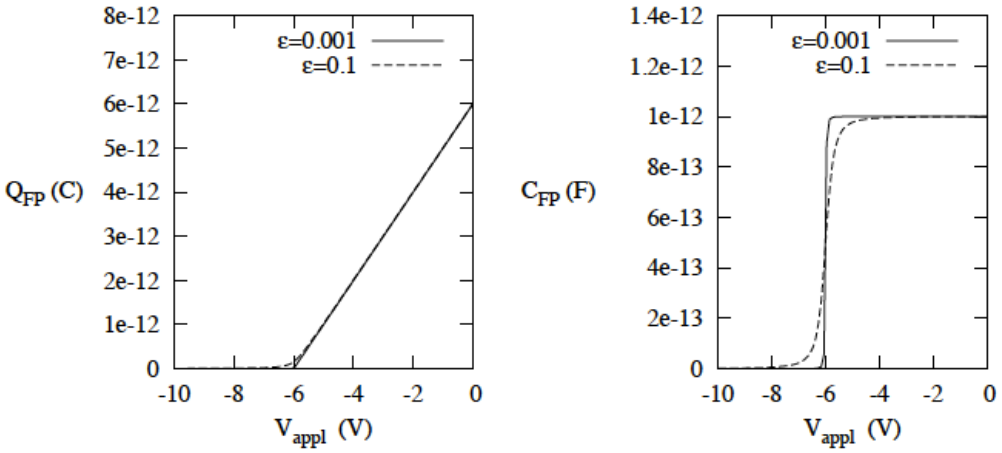

Figure 58: Field plate charge and capacitance as a function of bias

Metal interconnect and substrate capacitances have also been included in the model. Heat generated in the active regions at the surface where the currents are high. For a single transistor, heat is generated in a rectangular area formed by the finger width WF and dimension of the lateral current flow, Lth, roughly the same as G-D distance. Thermal resistance scales proportionately with the finger width. Using the equation for line source [40]

$$R_{TH}^{no^{MH}} = \frac{1}{\boldsymbol{NCELL.WF}} \cdot \frac{1}{\pi.KAPPA} . ln\left(\frac{16.\boldsymbol{TSUBTH}}{2.\pi.L_{TH}}\right)$$

where $KAPPA$ is the thermal conductivity, and $TSUBTH$ is the substrate thickness. The thermal conductance due to spreading into the substrate can be calculated using a conformal mapping technique [41]

The electrical and thermal model parameter extraction was done through non-pulsed and pulsed IV, and transient-I measurements of gate and drain currents, and CV measurements at five different temperatures between 25°C and 125°C. The pulsed IV measurements were done on a time-scale much smaller

than at which self-heating occurs. The transient current measurements were done at bias conditions where self-heating does occur. The pulse width was set such that it covers time scales below the thermal time-constant to steady-state, since these measurements were used to extract the thermal time constant. Parameter extraction was done in each region of operation of the device (Reverse, Forward, Linear series resistance, Non-linear series resistance) as illustrated in Fig. x below.

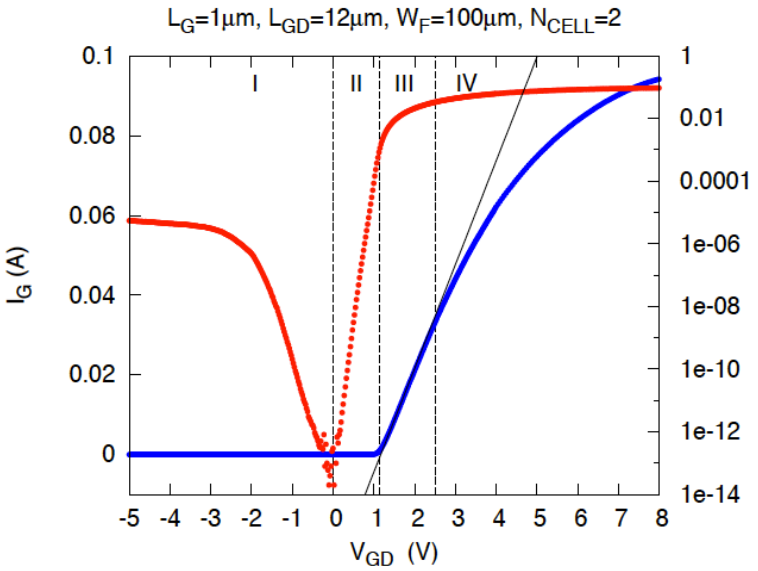

Figure 59: IG VGD measurement of a GaN HJFET

on a linear (blue) and log scale (red). LG = 1µm, LGD = 12µm, EF = 100µm, NCELL = 2

Parameter extraction in all regions of operation was done iteratively because the parameters dominant in determining IV characteristics may still have some impact in other regions of operation. The gate current in reverse and forward regions is due to thermionic emission. The parameters which determine the current are the pre-factor ISR, the barrier height PHIB0 and its temperature

dependence STPHIB0, the barrier height increase due to the GaN cap layer PHIB1, and the ideality factor IDF. The gate current was measured with the source floating and then again with the source connected to get better accuracy at small currents, and also because the measured drain current differs under these two bias conditions.

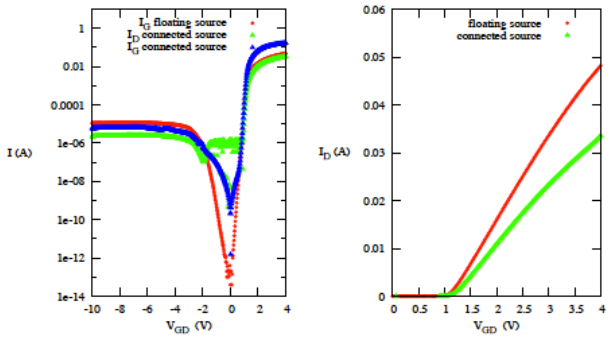

Figure 60: Gate current measurements

Floating source and connected source

The current equation is

$$I = A_{fit}.T^2.exp\left(-\frac{PHIB0+PHIB1}{k_B.T}\right).[\exp\left(\frac{V}{IDF.k_B.T/q}\right) - 1]$$

from which the starting values of STPHIB0 and STPHIB1 were extracted by repeating the fitting for all temperatures. Richardson plots were constructed from the gate current measurements over temperature and the barrier height and Richardson constant were obtained. A lot of variation was observed in barrier height and Richardson constants on the devices used for measurements. This made accurate curve fitting of the IV characteristics rather difficult.

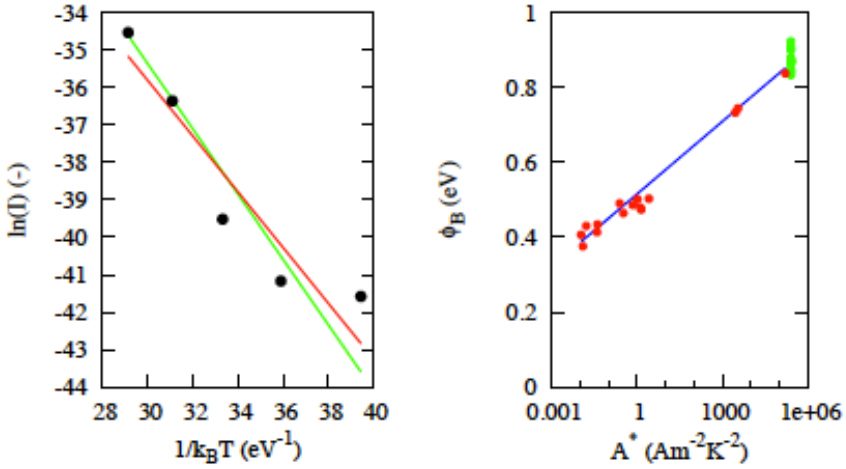

Figure 61a) 61b): Richardson plot of a single device.

a) The Richardson plot of a single device. Measurements (black markers), green line is a fit to measurements with the ideal Richardson constant. The red line is a fit to the measurements where both the Richardson constant and barrier height are fitted. b) Barrier height versus Richardson constant for several devices. Red markers are from fit to Richardson plots, where both the Richardson constant and the barrier height are fitted. The green markers are fits to Richardson plots where the barrier height is fitted and the ideal Richardson constant was used.

The parameters extracted from the drain current measurements are the parameters of the gate foot model, which are first extracted at the reference temperature and then scaled for other temperatures. These parameters are summarized in Table 9. The non-pulsed IV measurements and transient I measurements are used for extracting self-heating parameters. The AC-parameters are extracted from the CV measurements. The capacitance parameter of the hetero-junction CHJ is extracted on the gate capacitance in on-state. The charge model of the field plates is empirical.

Comparison of measurements to model

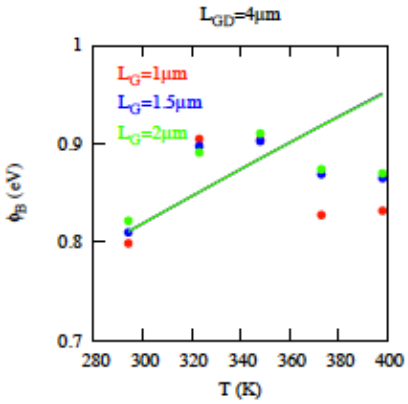

Figure 62: Barrier height as a function of temperature

Floating source LGD = 4µm

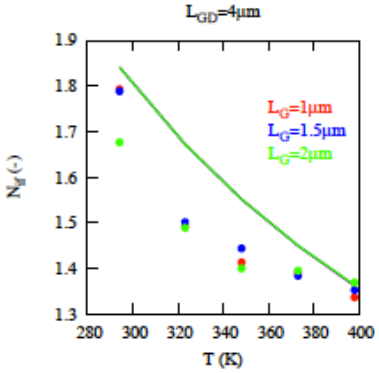

Figure 63: Non-ideality factor as a function of temperature.

Floating source LGD = 4µm

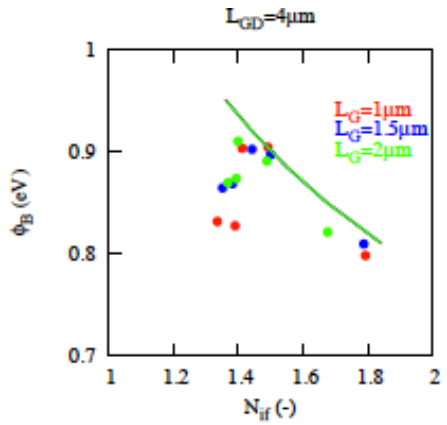

Figure 64: Barrier height versus non-ideality factor

Floating source LGD = 4µm

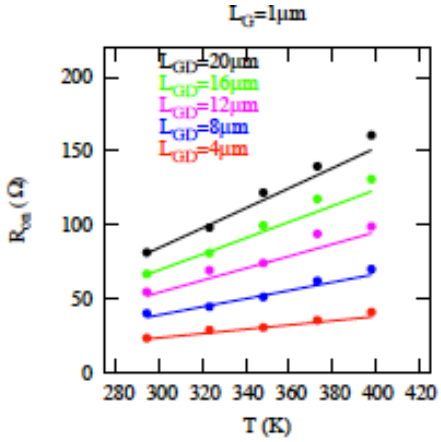

Figure 65: On-resistance as a function of temperature – floating source

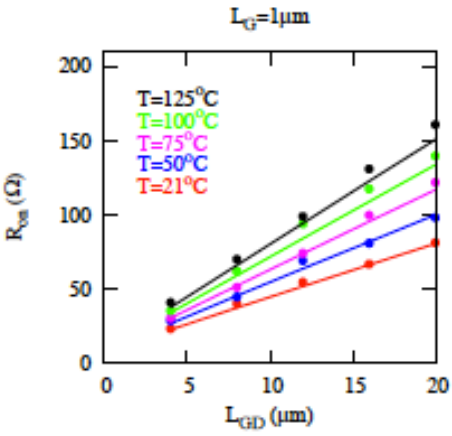

Figure 66: On-resistance as a function of G-D distance – floating source

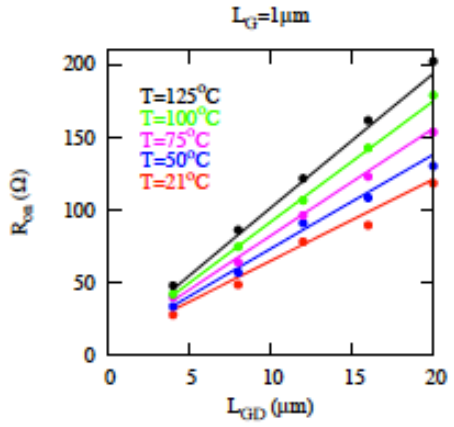

Figure 67: On-resistance as a function of G-D distance with VDS = 0V

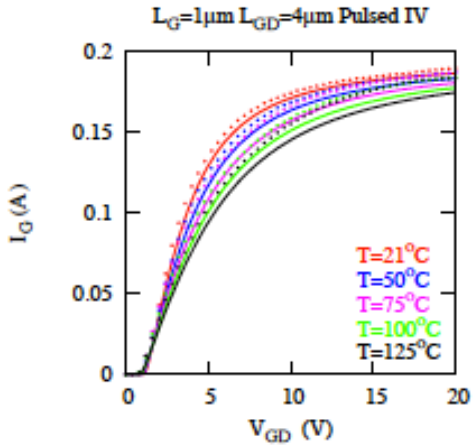

Figure 68: IG-VGD characteristics LGD = 4um – pulsed

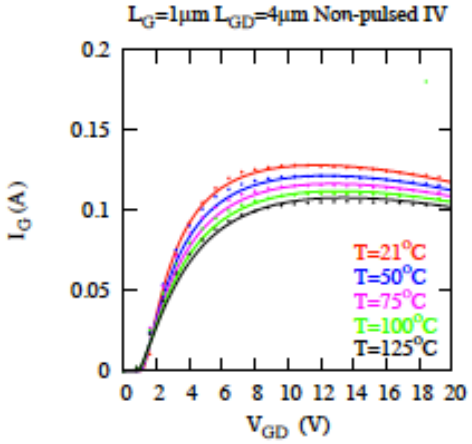

Figure 69: IG-VGD characteristics LGD = 4um – non-pulsed

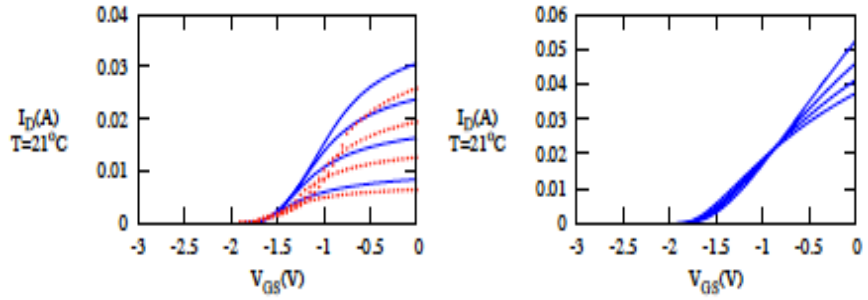

Figure 70: ID-VGS at 21°C(blue: model, red: measured)

a) with VDS = 0.25, 0.5, 0.75, 1V; b) with VDS = 10, 20, 30, 40V; LG = 1um, LGD = 4um

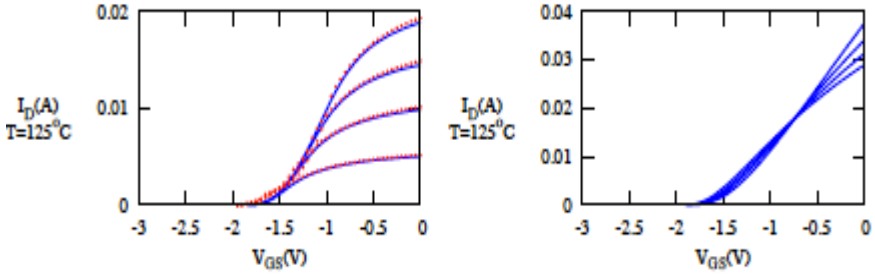

Figure 71: ID-VGS at 125°C (blue: model, red: measured)

a) with VDS = 0.25, 0.5, 0.75, 1V; b) with VDS = 10, 20, 30, 40V; LG = 1um, LGD = 4um

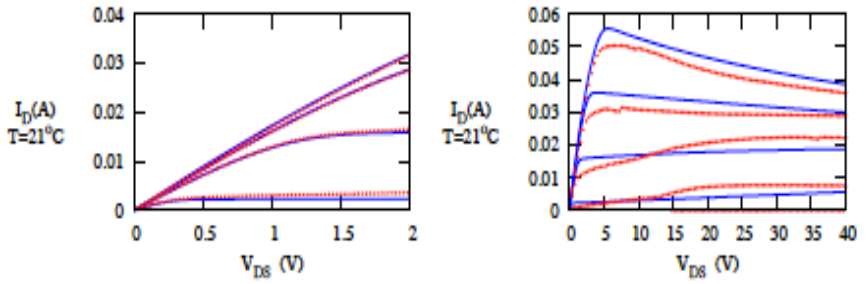

Figure 72: ID-VDS at 21°C (blue: model, red: measured)

a) with VGS = -1.5, -1.0 and 0V; LG = 1um, LGD = 12um

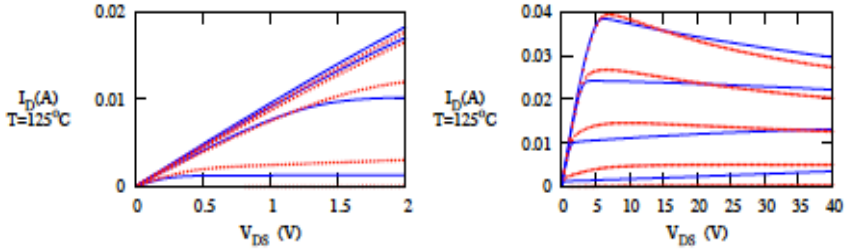

Figure 73: ID-VDS at 125°C (blue: model, red: measured)

a) with VGS = -1.5, -1.0 and 0V; LG = 1um, LGD = 12um

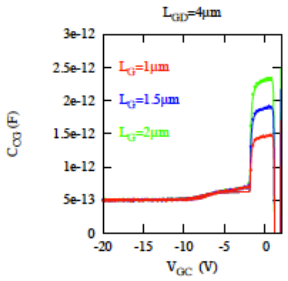

Figure 74: CV characteristics at f = 1MHz LGD = 4µm

Gate connected to high terminal, source and drain connected to low terminal of the CV meter.

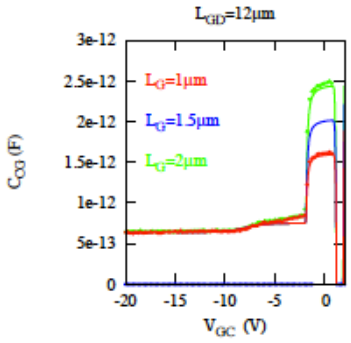

Figure 75: CV Characteristics at f = 1MHz LGD = 12µm

Gate connected to high terminal, source and drain connected to low terminal of the CV meter.

Table 9: Summary of HEMT model parameters

HEMT model parameters					
Gate foot DC parameters					
Parameter	Unit	Default	Min.	Max.	Description
BET	AV^{-2}	1.10^{-3}	0	1	Gain factor at ref. temperature
ETABET	-	1.3	-	-	Temperature scaling coefficient of BET
VFB	V	-2.0	-	-	Flatband voltage at ref. temperature
STVFB	-	0	-	-	Temperature scaling coefficient of VFB
KO	$V^{-1/2}$	0.1	$1.0.10^{-12}$	-	Body effect factor
PHIF	V	1.3	$1.0.10^{-12}$	-	Fermi voltage
STPHIF	-	0	-	-	Temperature scaling coefficient of PHIF
MO	-	0	0	1	Parameter for the sub-threshold slope
ALP	-	25.10^{-3}	$1.0.10^{-8}$	-	Factor for channel length modulation
MEXP	-	2	1	-	Smoothing factor for transition from linear to quasi-saturation region
SDIBL	$V^{-1/2}$	$3.6.10^{-5}$	1.10^{-12}	-	Drain induced barrier lowering

Gate foot Schottky diode parameters					
Parameter	Unit	Default	Min.	Max.	Description
ISR	A	1	0	-	Diode current in reverse from thermionic emission at ref. temperature
PHIB0	V	0.8	0	-	Barrier height
STPHIB0	-	1	0	-	Temperature scaling PHIB0
PHIB1	V	0.0	0	1	Barrier height increase due to GaN cap layer
IDF	-	1	1.10^{-3}	5	Ideality factor
STIDF	-	0	-	-	Temperature scaling IDF

2DEG Series resistance parameters					
Parameter	Unit	Default	Min.	Max.	Description
R2DEG	Ω	1.0	1.10^{-6}	-	Series resistance 2DEG
STR2DEG	-	0	0	-	Temperature scaling coefficient of R2DEG
IHC	A	1.0	1.10^{-6}	-	Saturation current of series resistance 2DEG
STIHC	-	0	0	-	Temperature scaling coefficient of IHC
MEXPA	-	1	0	-	Smoothing parameter

Gate capacitance parameters					
Parameter	Unit	Default	Min.	Max.	Description
CHJ	F	1.10^{-15}	1.10^{-18}	-	Hetero-junction capacitance
CAPGH	F	1.10^{-18}	1.10^{-18}	-	Gate head field plate capacitance
VTHGH	V	0	-	-	Threshold voltage of 2DEG formation underneath the gate head field plates
EPSGH	-	1.10^{-2}	1.10^{-6}	-	Smoothing parameter

Self-heating related parameters					
Parameter	Unit	Default	Min.	Max.	Description
TTH	s	1.10^{-6}	1.10^{-12}	-	Thermal time constant of ref device at TR
ATH	-	0	0	-	Temperature scaling coefficient of thermal resistance
EXRTH	-	0	0	1	Switch to include the effect of self-heating on the thermal resistance 1 = ON, 0 = OFF
TSCALE	-	1	1	-	Convergence parameter for built-in thermal network

RTHCOR	-	0	0	-	Switch to include mutual heating between cells 1 = ON
KAPPA	W/(Km)	150	1	-	Thermal conductivity used for infinitely thick substrate
TSUBTH	m	250.10^{-6}	1.10^{-6}		Substrate thickness for thermal model

Chapter 5

5.1 Design background

The thermal modeling and experimental characterization to quantify the effects of self-heating and thermal crosstalk in large area multi-finger AlGaN/GaN power diodes was described in Ch. 3. The simulation results and measurements confirmed that these effects cause a non-uniform channel temperature across the device periphery [42]. This temperature gradient leads to current redistribution from the hotter central fingers to the cooler outer fingers due to the temperature dependence of the channel electrical resistance [43]. In high power applications such as a switching power supply, inverter, motor drive or automotive systems, a discrete power HEMT is used as a switch in the half-bridge or full-bridge configuration, and a diode is used in power factor correction (PFC) or rectifying circuits. The HEMTs are subjected to high voltage and high current at the same time while switching inductive loads at high frequency. Therefore, the device can reach high temperatures very rapidly during switching which can lead to destruction of the device as it exceeds the maximum junction temperature (Tj) and the package limitations [44]. For example, during this study, it was found that in a boost converter application, with typical switching speeds are 100kHz to 200kHz, the 2-DEG temperature can rise to well over 200^{o}C within 5μs to 10μs. In traditional designs, there is no on-chip gate protection for the device under such over-temperature condition. Several techniques have been developed to remove the heat using novel power packaging solutions and materials. Some

efforts are being made to provide better thermal properties through engineering of the AlGaN/GaN buffer layers and engineered substrates [45]. However, there is a need to take the fundamental approach and design-in self-protection feature so that the device cannot be destroyed due to overheat during the operation. This thesis demonstrates the feasibility of such an approach through monolithic integration of analog and digital build blocks of a novel thermal shutdown circuit to be integrated with a 600V power HEMT on the same process platform. This chapter describes the design details of each cell and the characterization results.

The self-protection circuit proposed in this work and demonstrated through individual sub-circuits is a first of its kind and has not been seen implemented in its entirety in GaN-on-Si technology in the literature to the best of this author's knowledge [46].

5.2 Functional description of the thermal shutdown scheme:

The following figure depicts the three core components of the thermal shutdown circuit for the GaN power HEMT. As described earlier, accurate detection of temperature rise of a high voltage GaN power HEMT and temperature compensation is essential in order to design a protection circuit. This section describes an integrated circuit approach to embed GaN Schottky Barrier diodes as temperature sense elements into a GaN power HEMT and use the acquired temperature information to activate an on-chip gate shutoff circuit. The device is thus self-protected when the die gets too hot and a certain temperature is exceeded. Two different topologies were investigated, one based on a

proportional to absolute temperature (PTAT) circuit and the other based on translating the sensed change in temperature by an SBD into a detectable frequency, a thermometer design approach. Both techniques use a method to trigger the over-heat flag for the gate shutoff circuit to activate.

A PTAT based thermal shutdown circuit:

An on-chip PTAT circuit senses the temperature of the die and generates a voltage that accurately reflects the temperature. The output of the PTAT is connected to the input of a comparator. The comparator is designed such that it raises a flag (HI or LO) when a predetermined temperature condition is reached as it compares the input voltage to a fixed reference voltage. The precise reference voltage (V_{ref}) for the comparator is generated by a temperature compensated V_{ref} circuit using Schottky Barrier Diodes (SBDs) and a HEMT. The output of the comparator is then level shifted down (or up) to an appropriate V_{hs} voltage in order to shut off the power HEMT. In case of a depletion mode device (normally on), $V_{gs(th)}$ is negative and thus this voltage needs to be more negative than $V_{gs(th).}$ This requires polarity inversion of the signal, using an op-amp based design approach. This was verified via a breadboard hardware using an off-the shelf op-amp, but Due to limitations of the GaN-on-Si technology and devices available, an appropriate on-chip op-amp design was not found to be feasible. While only a positive voltage level change using SBDs has been physically demonstrated in this work, a design version with polarity inversion has been laid out and is ready for tape out.

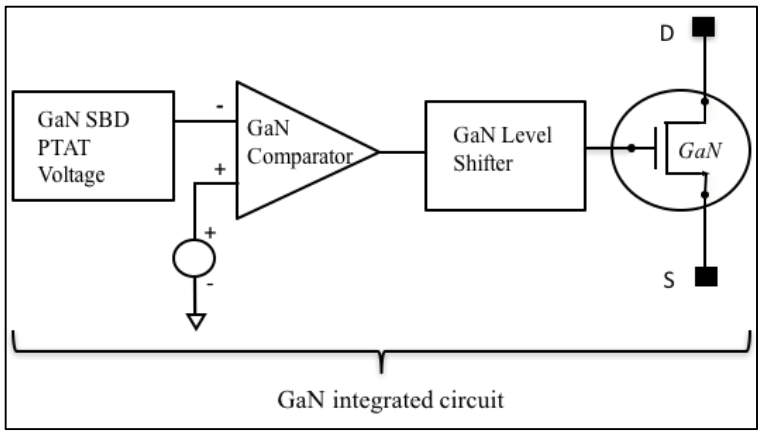

Figure 76: Block diagram - PTAT based thermal shutdown circuit

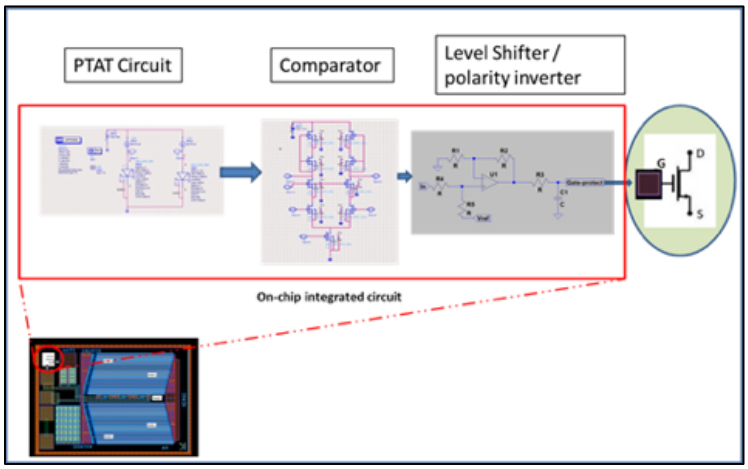

Figure 77: Schematic - PTAT based thermal shutdown circuit

A Thermometer design approach [47]**:**

An alternative approach to designing a thermal shutdown circuit involves a square wave generator circuit (a bi-stable multivibrator) using two SBDs at the input. With room temperature as a reference point, the output frequency increases as the temperature of the die rises. The square wave signal is fed into a frequency to voltage converter circuit. When the frequency reaches a certain value corresponding to an over-temperature condition, the comparator raises a flag and the output voltage is level shifted to an appropriate value in order to

shut off the power HEMT. The concept was implemented at a board level as depicted in Figures 80 and 81 where an LM331 F/V converter and an op-amp based level shifter was used. Two discrete GaN SBDs and GaN HEMTs were used to generate a square wave, the frequency of which corresponds to temperature.

Functional description of an SBD thermometer circuit:

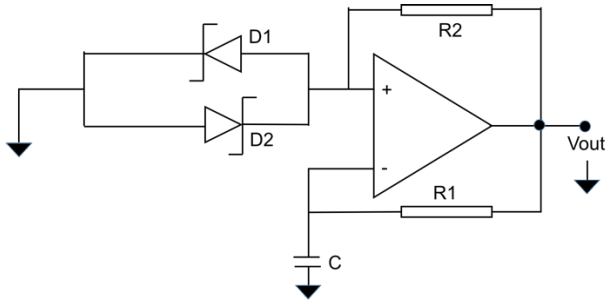

Figure 78: SBD Thermometer Circuit

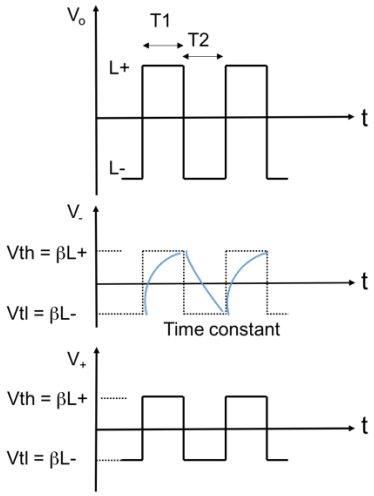

Figure 79: SBD Thermometer Waveform

Let the output be Vo = L+. The capacitor C will charge towards this level through R. Thus, the voltage across C, which is applied to a negative input terminal of the OpAmp will rise exponentially toward L+ with a time constant

τ = CR. Voltage at the positive terminal of the OpAmp id $V_+ = \beta L+$. This situation will continue until the capacitor voltage reaches the positive threshold Vth, at which point, the bi-stable multivibrator will reach the other stable state in which Vo = L- and $V_+ = \beta L-$. The capacitor will then discharge and its voltage V- will decrease towards L-. This state will continue until V- reaches the negative threshold Vth = βL-, at which time, the bi-stable multivibrator switches to positive output state, the capacitor begins to discharge, and the cycle repeats itself. Thus, the circuit oscillates and produces a square wave at the output of the OpAmp due to the positive feedback through R2. Period T of the square wave is calculated as follows:

During the charging interval T1, the voltage V- across the capacitor at any time t, with t = 0 at the beginning of T1 is given by STC analysis

$V_- = L_+ - (L_- - \beta L_-)e^{-t/\tau}$ where τ = CR. β is the fraction of the output voltage fed back to the positive terminal of the OpAmp. Substituting $V_- = \beta L_+$ at t = T1 gives

$$T1 = \tau ln \frac{1-\beta\left(L_-/L_+\right)}{1-\beta}$$

Similarly, during the discharge interval T2, the voltage V- at any time t, with t = 0 at the beginning of T2 is given by

$V_- = L_- - (L_- - \beta L_+)e^{-t/\tau}$ Substituting $V_- = \beta L_-$ at t = T2 gives

$$T2 = \tau ln \frac{1-\beta\left(L_+/L_-\right)}{1-\beta}$$

Combining T1 and T2 we get the period T = T1+T2. Normally, $L_+ = L_-$ for a symmetrical square wave.

$T = 2\tau ln\frac{1+\beta}{1-\beta}$

As an example, if R1 = R2 = 10kΩ, C = 0.1μF and V = 12V, we get

$T = 2\tau ln\left(\frac{12+V_D}{12-V_D}\right) = 2 * 0.1 * 10^{-6} * 10 * 10^3 x ln\left(\frac{12+V_D}{12-V_D}\right)$

$f = \frac{1}{T} = \frac{500}{ln\left(\frac{12+0.7}{12-0.7}\right)} = 4.28\ kHz$ at 25 °C

The temperature coefficient of the SBD in this work is -2mV/°C (just like a p-n diode). So, frequency at other temperatures can be calculated easily.

At 0 °C, $V_D = 0.7 + 0.05 = 0.75V$ and $f = \frac{1}{T} = \frac{500}{ln\left(\frac{12+0.75}{12-0.75}\right)} = 3.99\ kHz$

At 50 °C, $V_D = 0.7 - 0.05 = 0.65V$ and $f = \frac{1}{T} = \frac{500}{ln\left(\frac{12+0.65}{12-0.65}\right)} = 4.61\ kHz$

At 100 °C, $V_D = 0.7 - 0.15 = 0.55V$ and $f = \frac{1}{T} = \frac{500}{ln\left(\frac{12+0.55}{12-0.55}\right)} = 5.45\ kHz$

and so on. Thus, the circuit produces a square wave, the frequency of which corresponds to the temperature.

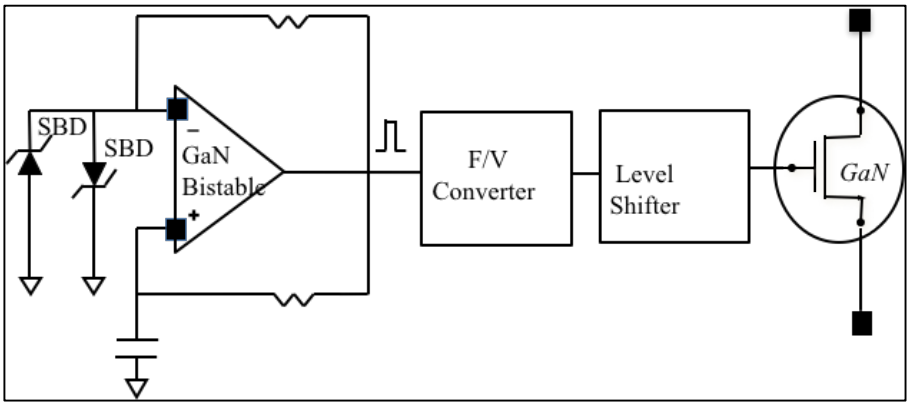

Figure 80: Block diagram - Thermometer based design

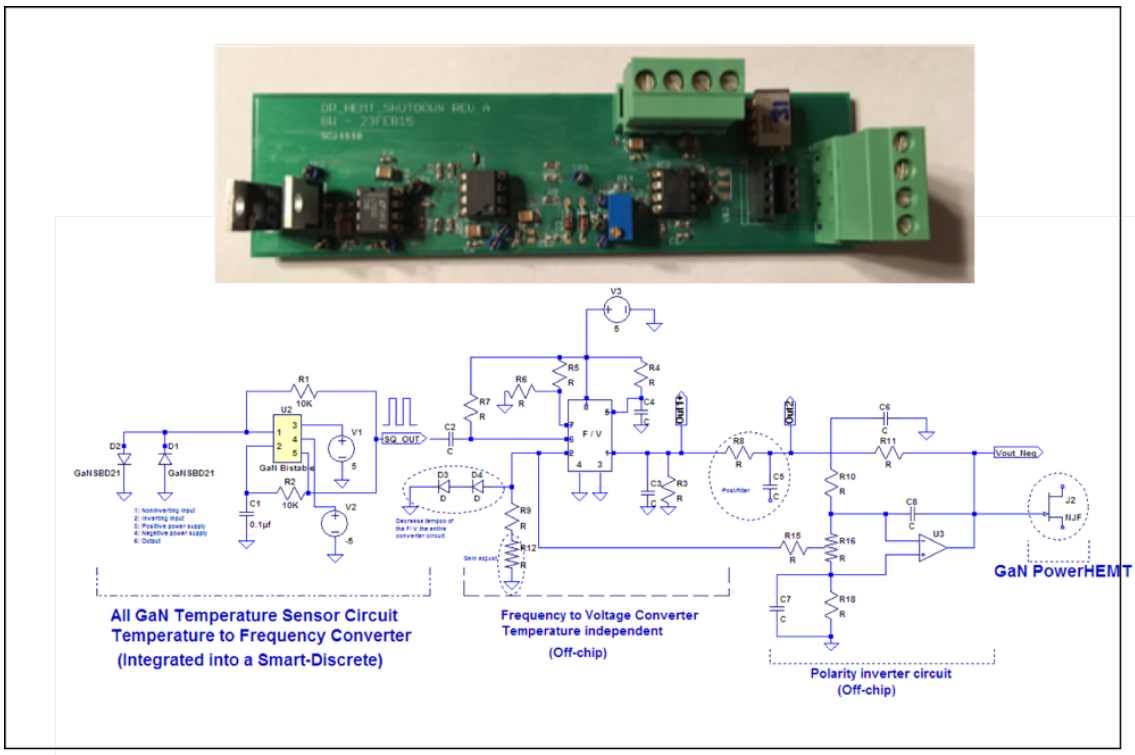

Figure 81: Thermometer based design - Schematic and Board

Figure 89 shows the square wave output and Figure 90 shows the level shifter output going negative enough (-6V) to put the GaN power HEMT in an OFF state.

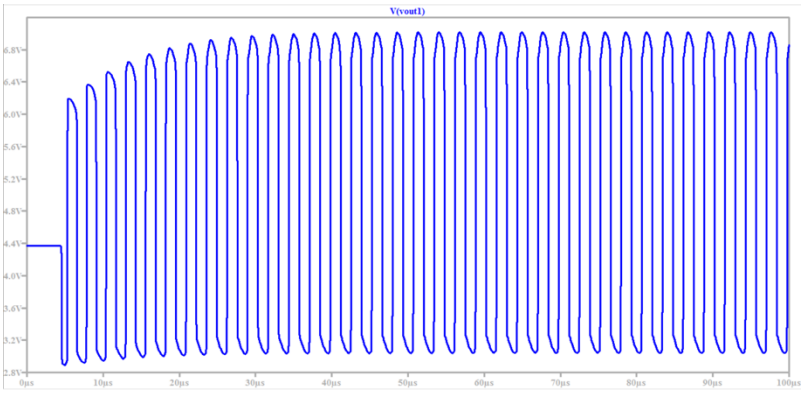

Figure 82: Temperature to Freq. conversion

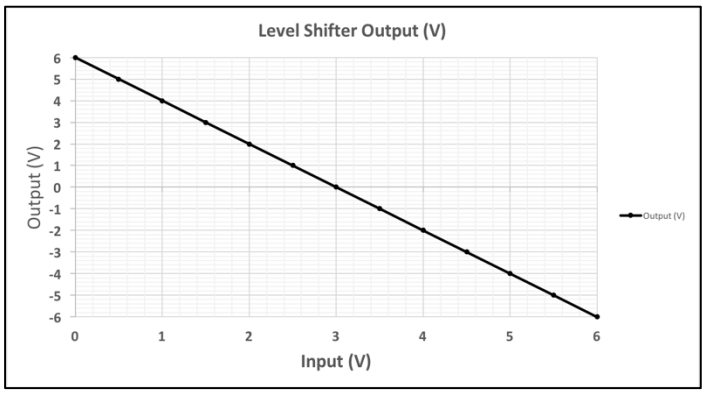

Figure 83: Gate Protect Voltage Shifter

Design using a Phase Locked Loop:

In yet another variation, a phase locked loop (PLL) approach can be applied to latch on to the frequency of interest using a XOR gate as a phase detector. Both these designs using a thermometer or PLL approach are much more complicated to implement in today's GaN-on-Si discrete semiconductor power technology. Therefore, these designs are left as topics of further research when the process technology is mature enough to offer CMOS-like complementary logic devices to realize such elaborate control circuits. In this thesis, a PTAT based approach is thus used as a proof of concept.

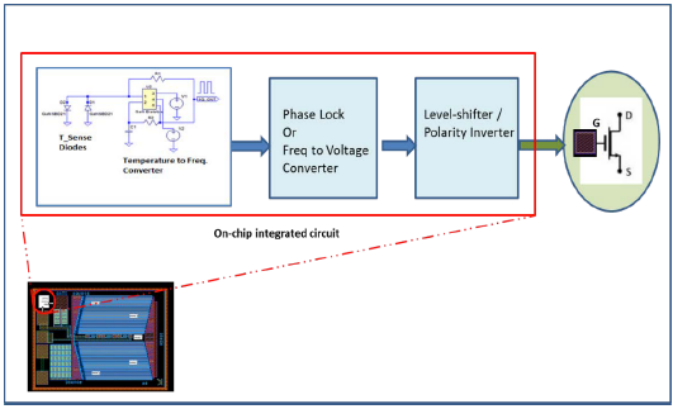

Figure 84: Schematic – PLL based Thermal Shutdown Circuit

This work started with designing stand-alone single instance HEMT and Schottky Barrier Diode of various widths (W) and lengths (L) which are required for developing the cell library of sub-circuits. The library consists of the following cells:

1) Single instance HEMT and Diode: **DR01, DR02**
2) Current Sources: **IS101**
3) Current Mirror: **IM102**
4) Bias Circuits: **DBIAS1**
5) Logic Circuit: **LOG101**
6) Inverter: **INV101**
7) Proportional to Absolute Temperature voltage generator (**PTAT**)
8) Voltage References: **VREF, VREF1**
9) Comparators: **CO101, CO102, CO103**

The final design of a large area multi-finger 600V HEMT utilizing these cells is presented at the end of this chapter.

The following section describes the function of each one of these circuits:

5.3 The Cell Library

5.3.1 Single instance HEMT and Diode

a. Minimum geometry for the HEMT was LG (Gate length) = 1um, LGD (gate to drain distance) = 4μm, WF = 100μm. Dimensions were varied to create other design variants with LGD = 4μm, 8μm, 12μm, 16μm and 20μm; LG = 1μm, 1.5μm and 2μm; LGS

devices = 1.5μm and 3.0μm; WF = 100μm and 200μm. The representative curves can be found in Chapter 4 (Modeling).

b. Minimum geometry (dictated by technology, processing tools, and design rules limitations) for the diode was LA (length of anode) = 1μm, WF (finger width) = 100μm, and LAC (distance between anode and cathode) = 4μm. Dimensions were varied to create other design variants with LA = 1μm, 1.5μm, 2μm and 4μm; LAC = 4μm, 6μm, 8μm, 10μm, 12μm and 16μm; WF = 50μm, 100μm and 200μm The representative curves can be found in Chapter 4 (Modeling).

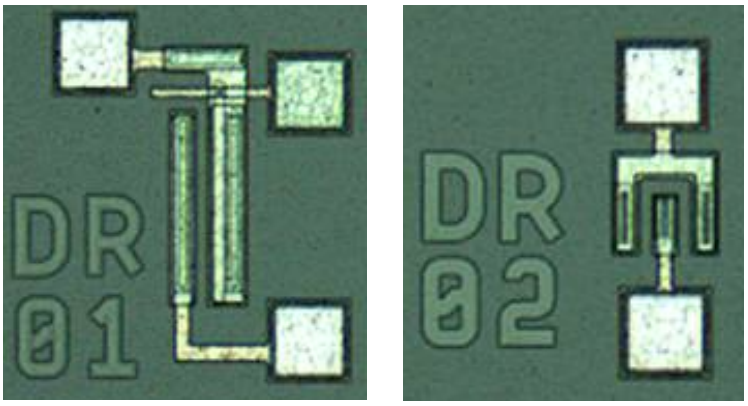

Figure 85: Die photo - HEMT and Diode

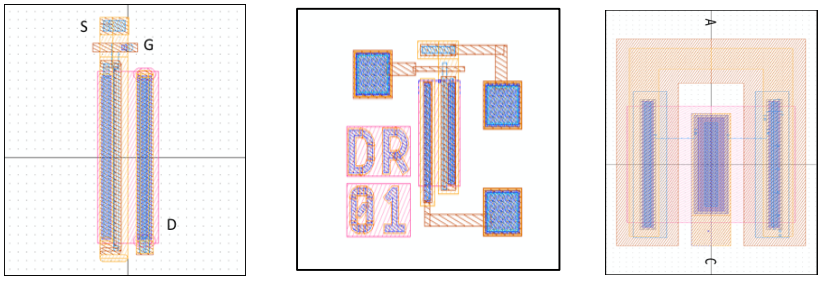

Figure 86: HET and SBD Layout

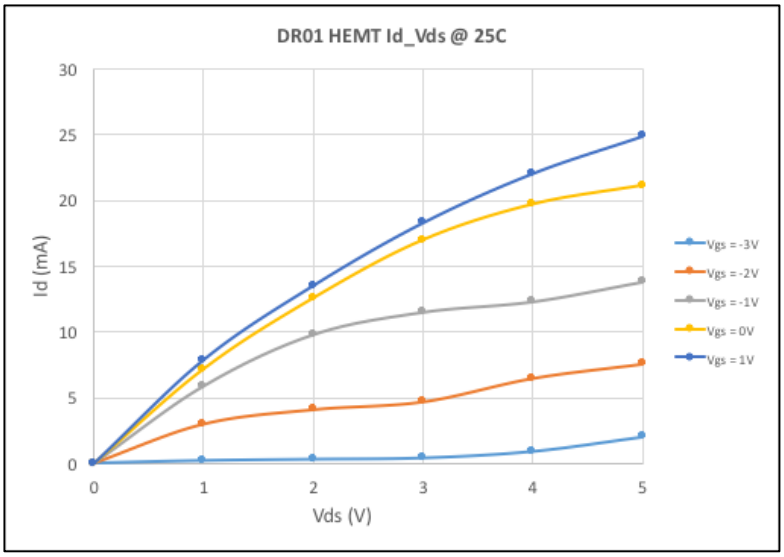

Figure 87: Minimum geometry HEMT

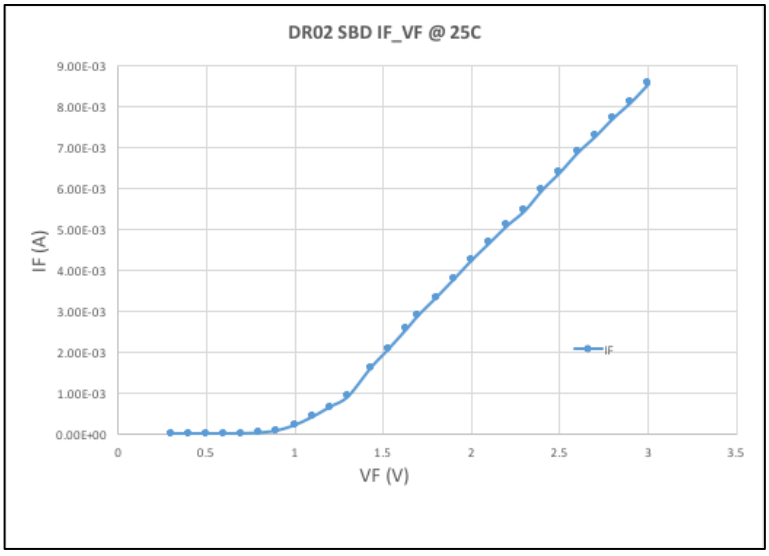

Figure 88: SBD turn-on Characteristics

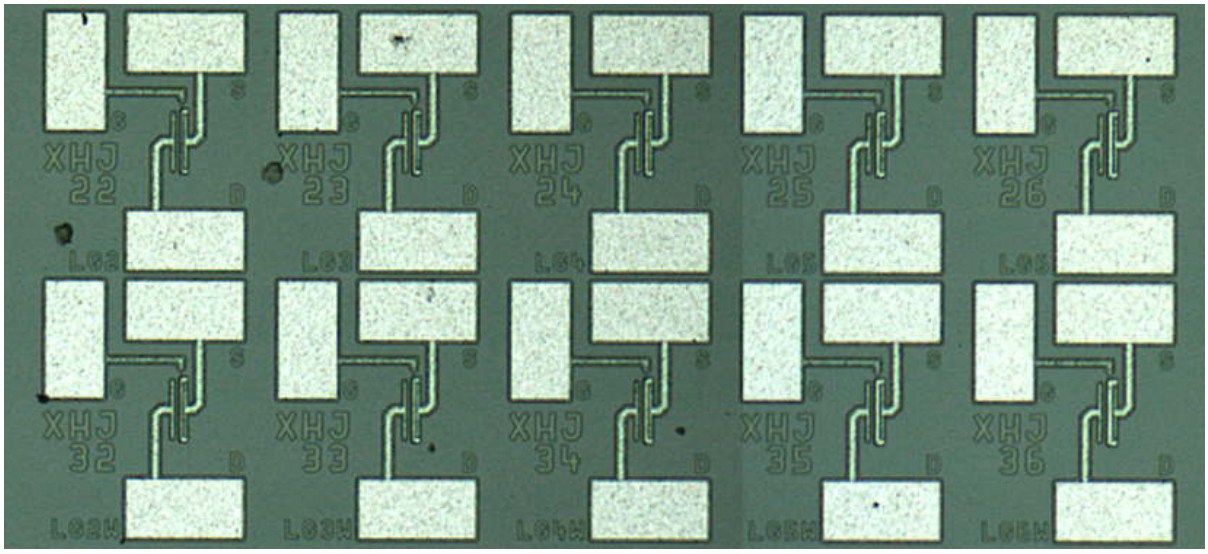

Figure 89: Die photo - HEMTs with various W/L dimensions

5.3.2 Current Source

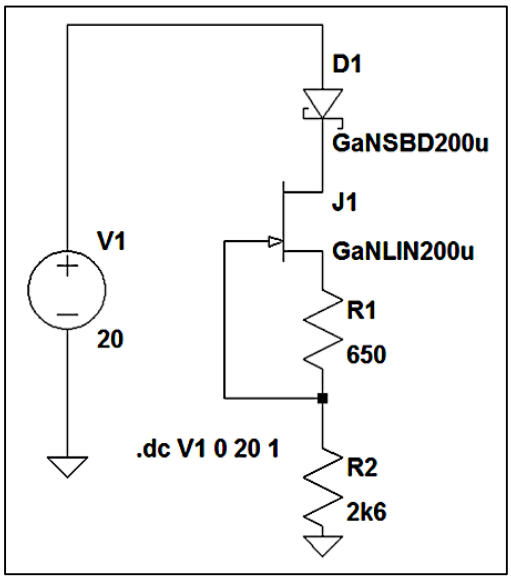

Figure 90: Current source

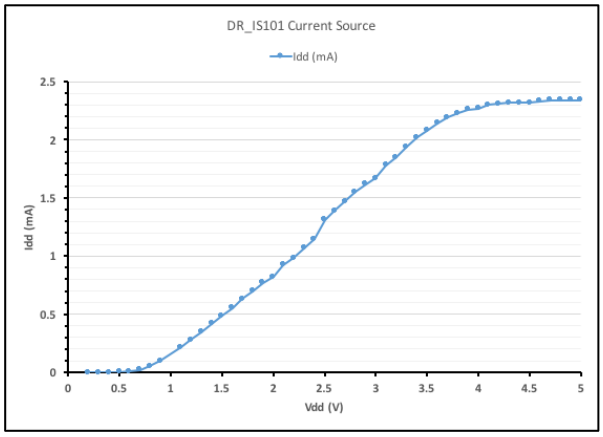

Figure 91: Saturated current

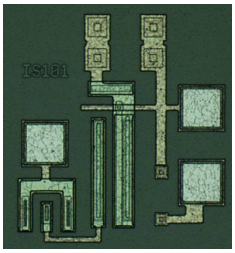

Figure 92: Current Source

The circuit follows a standard saturation current equation

$I_{D(sat)} = I_S \exp\left[q(V_{GS} - V_{on})/n_H kT\right.$

The diode current is given by $I_{D(sat)} = I_S \exp\left[q(V_D - I_D R)/n_D kT\right.$

The resistor ratio defines the slope of the current rise and can be adjusted by varying the ratio of R1 and R2 which sets the gate voltage of the HEMT. The current starts rising once the Schottky diode D1 turns on at 0.7V.

5.3.3 Current Mirror IM102 [48]

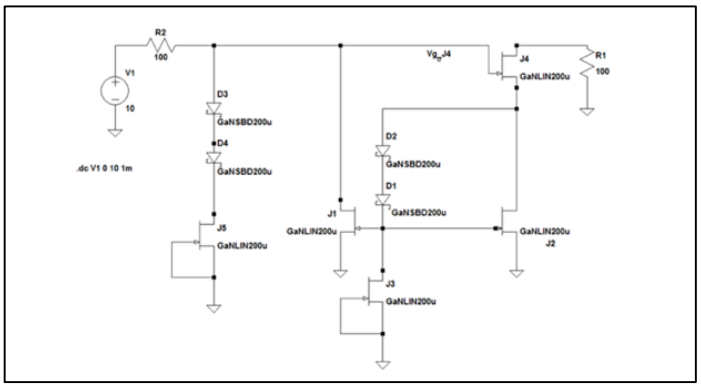

Figure 93: Current Mirror

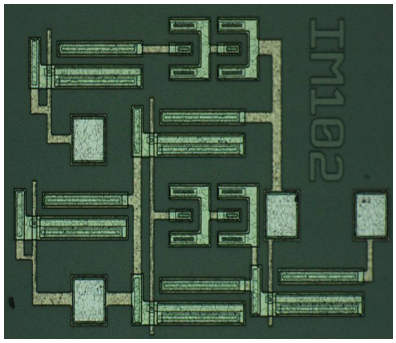

Figure 94: Current Mirror IM102

This circuit is a Wilson current mirror with level shifting and current compensation. The level shifting diodes D2 and D1 maintain HEMTs J2 and J1 in saturation mode. The drain voltage and the gate voltage of J2 are reflected so that the drain voltage of J1 is approximately equal to the drain voltage of J2, and the gate voltage of J1 equals the gate voltage of J2. The reflection is achieved by matching J1 and J2, so that $k_1 = k_2$, where k is a current gain factor proportional to the width of the HEMT. J1 is chosen such that at a specified nominal dc current level, its gate to source voltage V_{GS1}equals zero. Since J1 and J2 are matched, V_{GS2} of J2 also equals zero. J3 also matches J1, thus V_{GS3} of J3 also equals zero. Since J1 and J2 are matched, $V_{G3} = V_{D1}$and $V_{S3} = V_{D2} = V_{G3}$. Therefore, $V_{D1} = V_{D2}$. The gate voltage of J2 is level shifted down by two diode drops below its drain voltage $V_{D2}$by diodes D2 and D1. Therefore, gate voltage V_{Gs1} is also level shifted two diode drops down below its drain voltage V_{D1} so that J1 is maintained in saturation by the reflected drain and gate voltages of J1. The current drawn by the level shifting diodes D2, D1 reduces the output current, so diodes D3, D4 and J5 provide the current compensation that is proportional to the current drawn by D2, D1 by making $k_2/k_1 = k_3/k_5$. Therefore, $I_{out} = \left(\frac{k_2}{k_1}\right) I_{in}$. This equation is a transfer function of an ideal current mirror. If J1 and J2 are perfectly matched and identical, $I_{out} = I_{in}$. The addition of J3 raises the output impedance of this current mirror. J3 increases the linearity of of the current output of the current mirror by making it less susceptible to fluctuation caused by varying voltages present at the mirror output node.

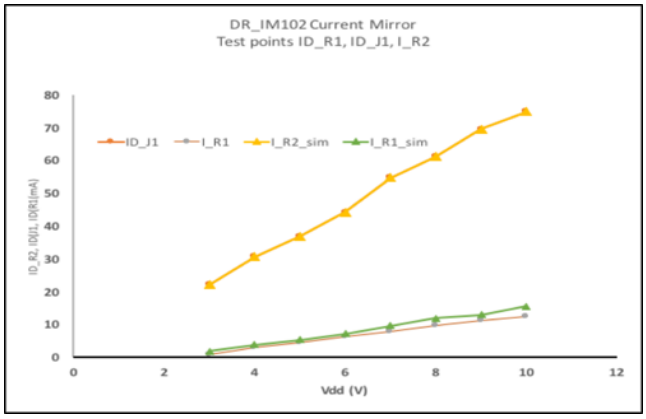

Figure 95: Current Mirror IM102 Output

5.3.4 DBIAS1

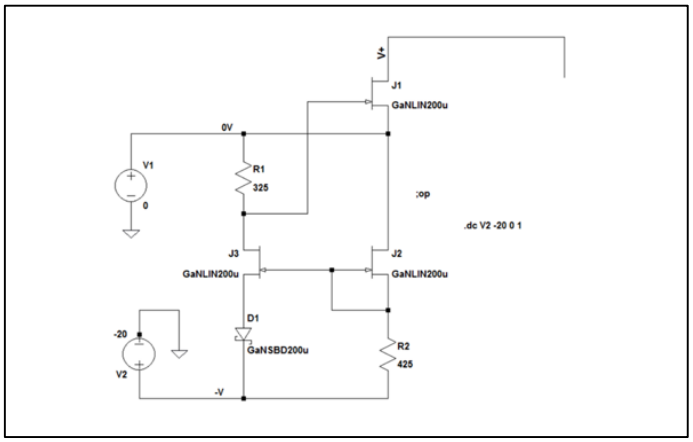

Figure 96: DBIAS1

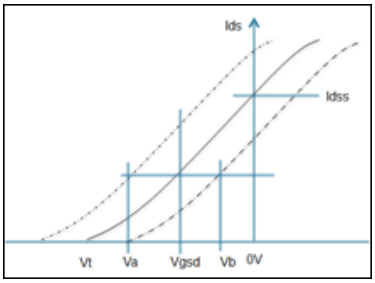

Figure 97: Bias point of a D-mode HEMT

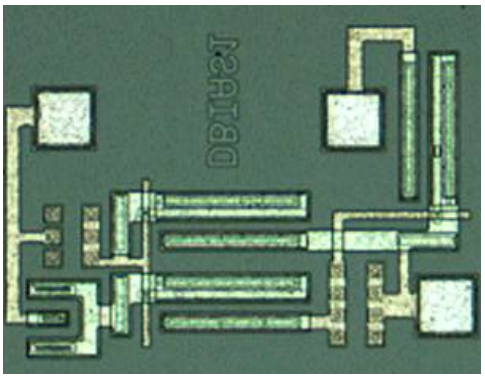

Figure 98: DBIAS1 Die Photo

DBIAS1 is a biasing circuit to determine the bias point of a depletion mode HEMT J2. The voltage drop across R1 due to drain current of J3 constitutes the gate-source voltage of J1. Forward voltage of diode D1provides a reference voltage Vref. The source follower configuration of J2 and R2 provide bias for J2. The circuit provides gate voltage control of J1 so that its drain current can be determined and maintained.

5.3.5 LOG101: Two inverters and an output stage [49]

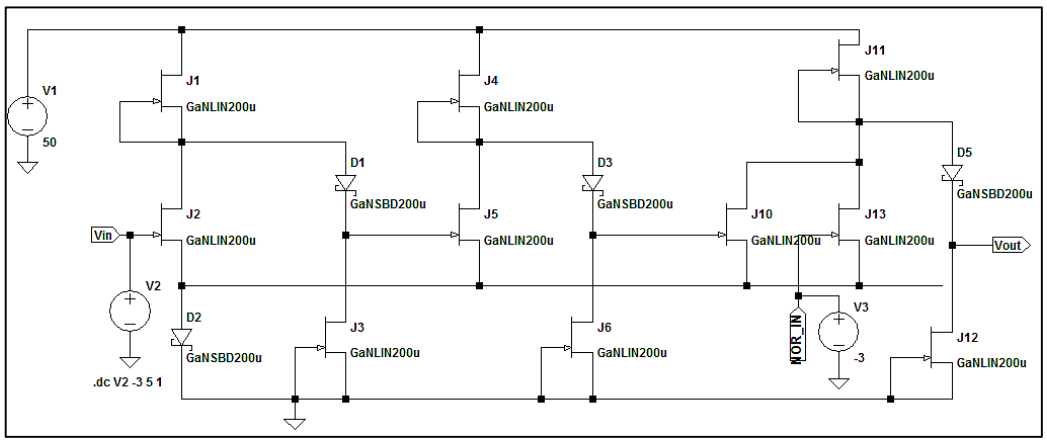

Figure 99: LOG101 – Two inverters and NOR gate

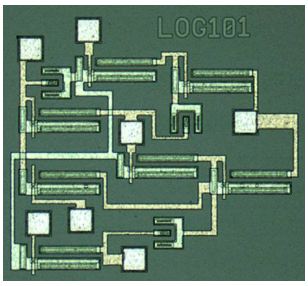

Figure 100: LOG101 Die Photo

The logic circuit LOG101 comprises of two inverters and a NOR circuit in series. HEMTs J1 and J4 serve as constant current sources with very high source resistance and thus as active loads. Schottky diode D2 maintains the source potential of switching HEMTs J2 and J5 at a potential higher by a predetermined positive voltage Vss than the ground potential, basically a diode drop above ground. Diode D1 functions as a level shifting constant-voltage (V_L) source. HEMT J3 constantly maintains the level shifting voltage V_L and serves as a constant current source having a current value smaller than the current value of the active load HEMT J1. The second inverter works in a similar manner. The following truth table was verified.

Table 10: Truth table for LOG101

X	Y	A	B	Output
1	0	1	0	0
1	0	1	1	0
0	1	0	0	1
0	1	0	1	0

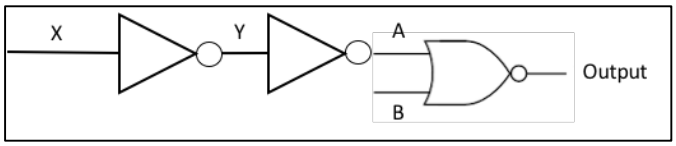

Figure 101: Logic Function

5.3.6 Inverter [49]

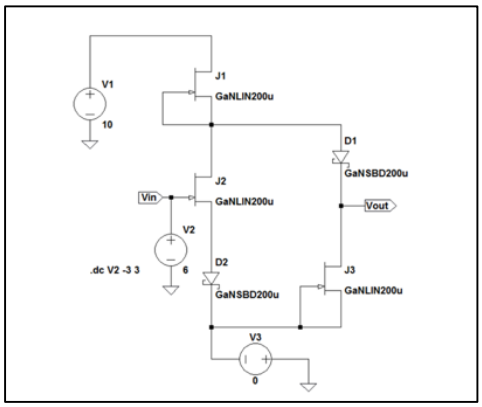

Figure 102: INV101

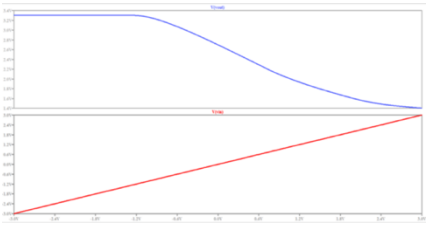

Figure 103: INV101 Output

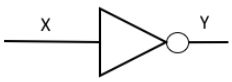

Table 11: Truth table - Inverter

X	Y
1	0
0	1

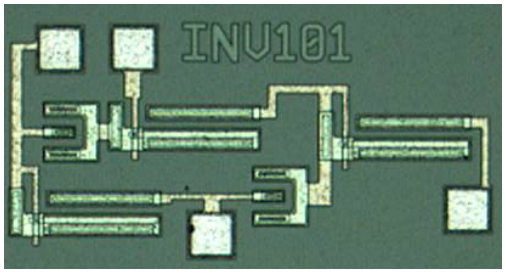

Figure 104: Inverter Die Photo

5.3.7 PTAT/CTAT Current Generator

PTAT Circuit: The circuit is based on the basic principle of generating a PTAT voltage that is linear with respect to temperature, but differs in design from the traditional PTAT current generator circuit. The traditional version of the circuit used ΔV_{SBD} for V_PTAT as described below, we use the total current through the circuit and calculate the voltage drop across a 100Ω resistor R1 (could use any reasonable value of R1).

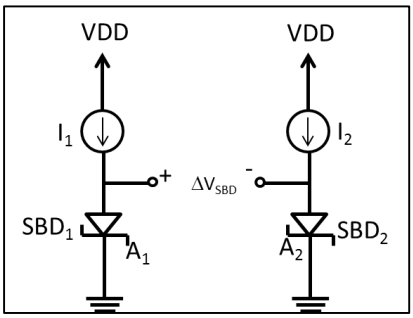

Figure 105: Principle of PTAT

The standard set of MOSFET equations still apply to GaN SBDs and HEMTs [49] [51]

$$V_{PTAT} = \Delta(V_{SBD1} - V_{SBD2}) = V_t ln\left(\frac{I_1}{I_{s1}}\right) - V_t ln\left(\frac{I_2}{I_{s2}}\right)$$

$$= V_t ln\left(\frac{I_1}{I_2}\frac{I_{s2}}{I_{s1}}\right) = V_t ln\left(\frac{I_{s2}}{I_{s1}}\right) = V_t ln\left(\frac{A_2}{A_1}\right) = \frac{kT}{q} ln\left(\frac{A_2}{A_1}\right) \qquad if\ I_1 = I_2$$

$If\ A_2 = 5A_1, \Delta V_{SBD}\ at\ room\ temperature\ becomes$

$$\Delta V_{SBD} = \left[\frac{k}{q} ln\left(\frac{A_2}{A_1}\right)\right] T$$

Therefore $V_{PTAT} = V_t ln\left(\frac{A_2}{A_1}\right)$

The constant current source (I_1 and I_2) is designed with GaN d-mode HEMT, SBD and appropriate resistor values to provide approximately 2mA of constant current. This current source replaces the PMOS current source in traditional PTAT circuits in CMOS technologies.

The circuit behaves well showing a linear relationship up to about 150^{o}C, but shows non-linearity between 150^{o}C and 225^{o}C. This may be due to the device mismatch errors, suspected nonlinear behavior of the resistors used in the current source (based on the epi sheet rho in-line measurements), and other second order effects. The process technology is still in development and such issues will need to be corrected. Nevertheless, the circuit shows good agreement with simulation.

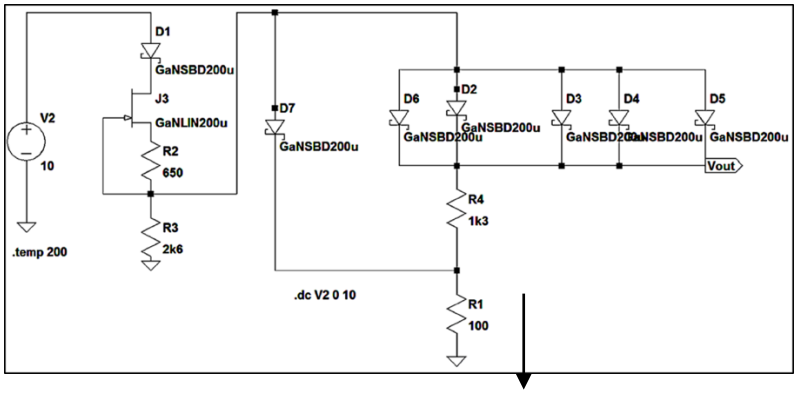

Figure 106: Schematic - PTAT voltage generator

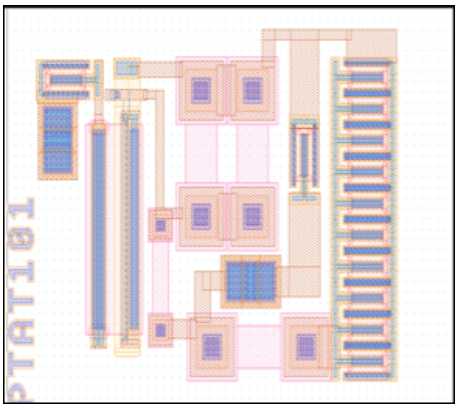

Figure 107: a) PTAT layout b) die photo

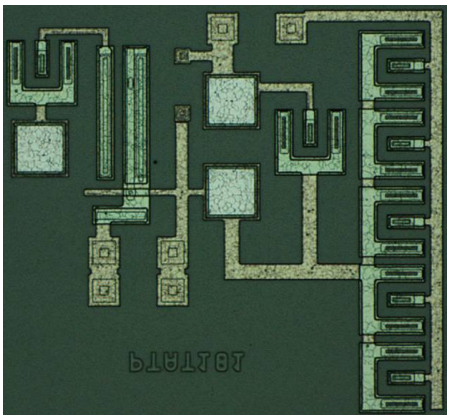

Figure 108: Die photo of PTAT circuit

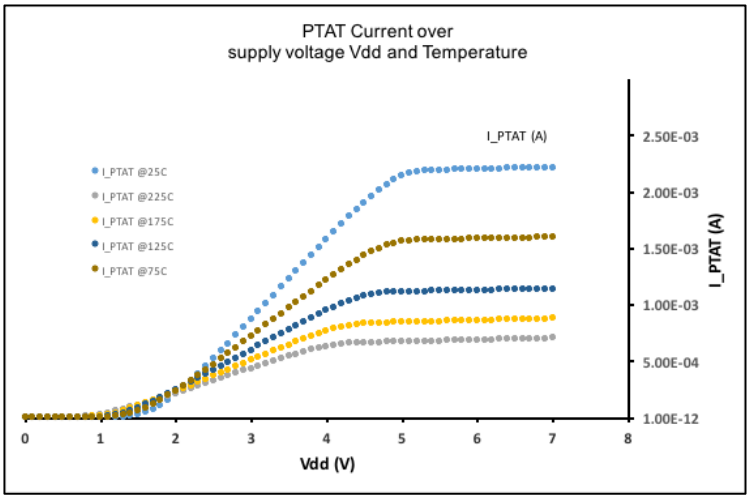

Figure 109: PTAT Current vs Supply Voltage (25°C to 200°C)

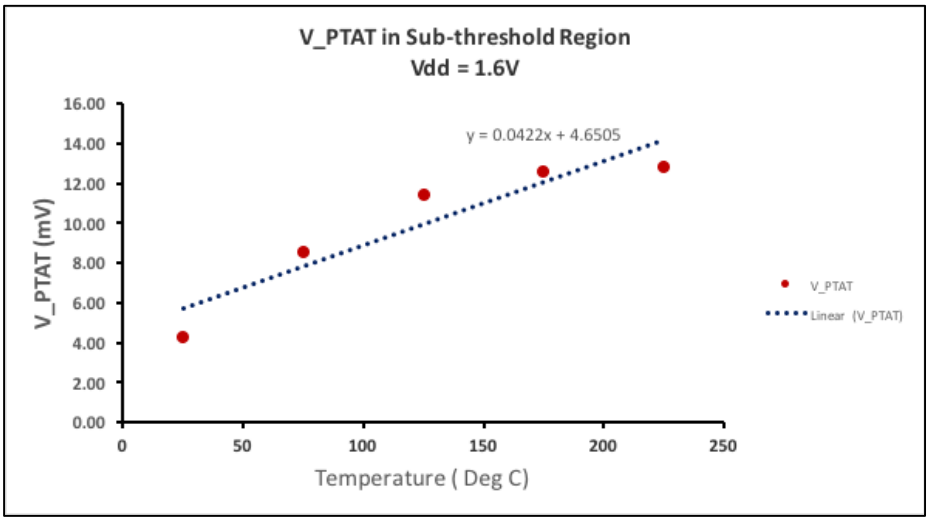

Figure 110: V_PTAT in Sub-threshold region

As mentioned in Ch.4, the current increases at sub-threshold bias conditions (follows thermionic emission theory) and decreases at higher bias conditions (strong inversion) due to increase in on-resistance with temperature. Thus, in the sub-threshold region, the temperature coefficient (TC) is positive, while in the strong inversion (saturation) region, the TC is negative as shown in Fig. 110.

The TC of the sub-threshold current with fixed gate-source voltage is given by [52]

$$T.C. = \frac{1}{I_{DS}}\frac{dI_{DS}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} + \frac{1}{\exp\left((V_{GS}-V_{TH})/\eta V_T\right.}\frac{d}{dT}\exp\left((V_{GS}-V_{TH})/\eta V_T\right.$$

$$T.C = \frac{2-m}{T} + \frac{k-(V_{GS}-V_{TH})/T}{\eta V_T}$$

where m is the mobility temperature exponent $\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m}$

and k is the temperature coefficient of V_{TH}

If such a PTAT generator were to be used to design a bandgap reference circuit, the bias conditions would have to be in sub-threshold region to compensate for the negative TC of the SBD. However, the purpose of using a PTAT generator in this thesis is to treat it as a temperature sensor. As such, a negative TC in Fig. 112 is useful as the V_PTAT drops from 221mV at 25°C to 70mV at 225°C. For example, the comparator can be designed to sense 87.6mV (V_PTAT at 175°C) and switch to generate an over-temperature flag.

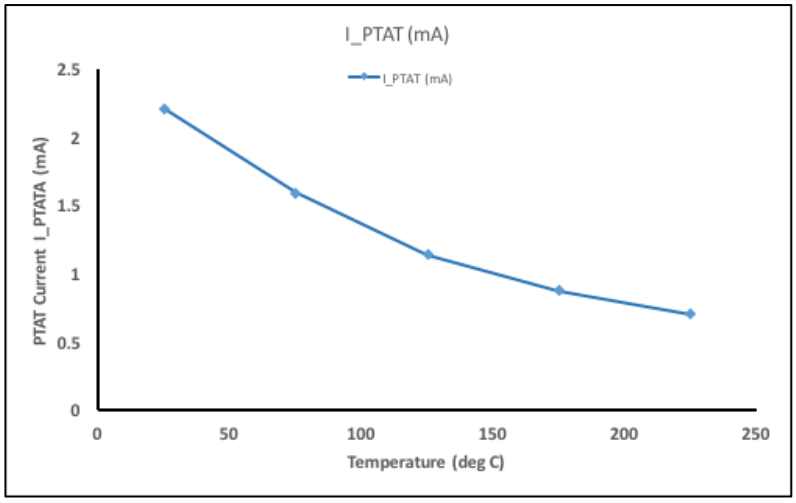

Figure 111: PTAT Current

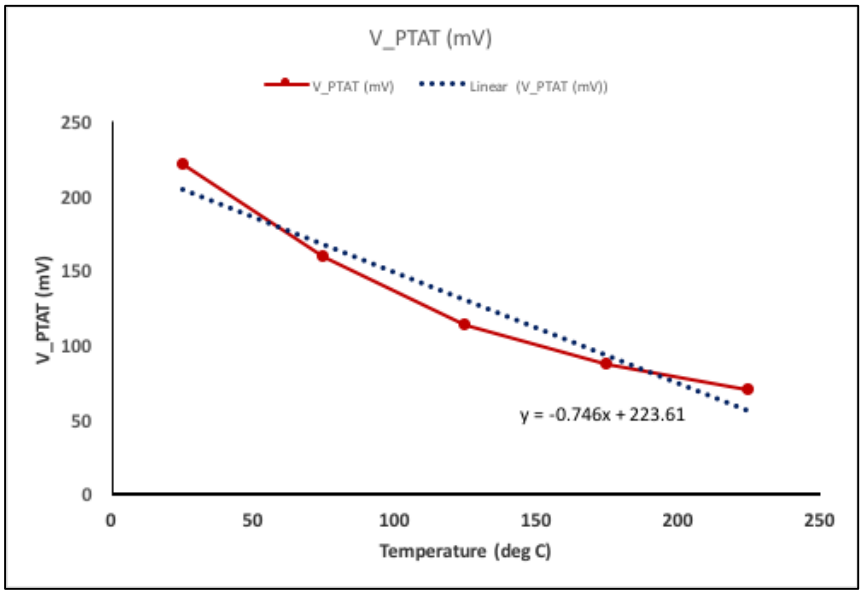

Figure 112: PTAT Voltage

A traditional PTAT circuit was also designed using GaN SBDs and GaN HEMTs for the current source and area ratio. The results show similar temperature coefficient and trend line as in the Pseudo-PTAT design.

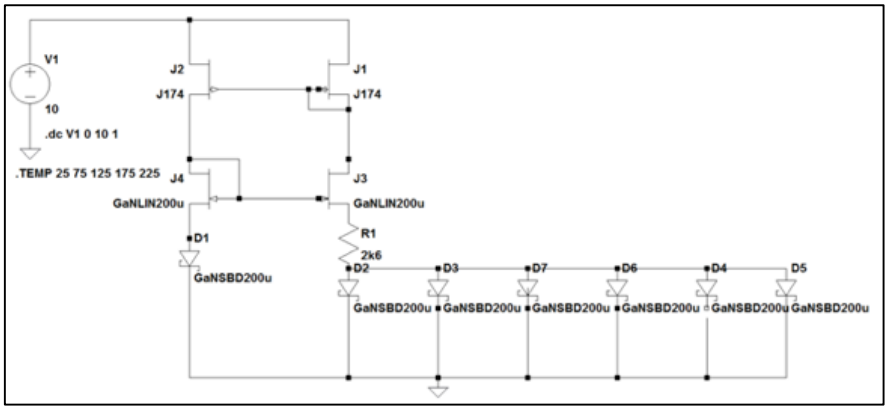

Figure 113: Traditional PTAT design using GaN devices

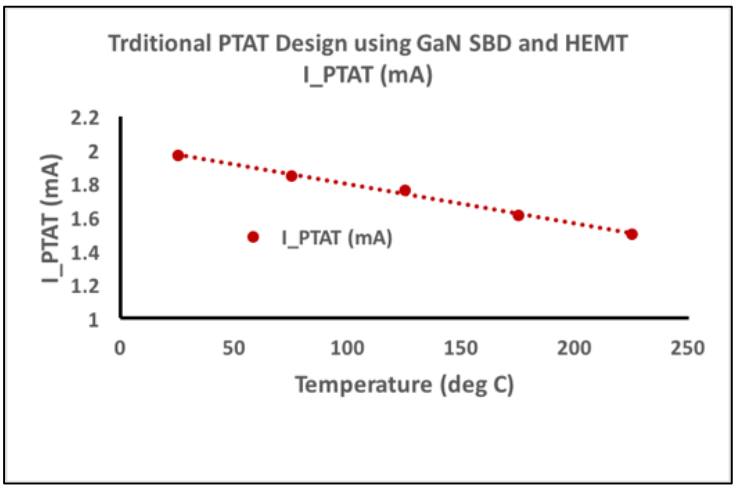

Figure 114: Traditional design I_PTAT

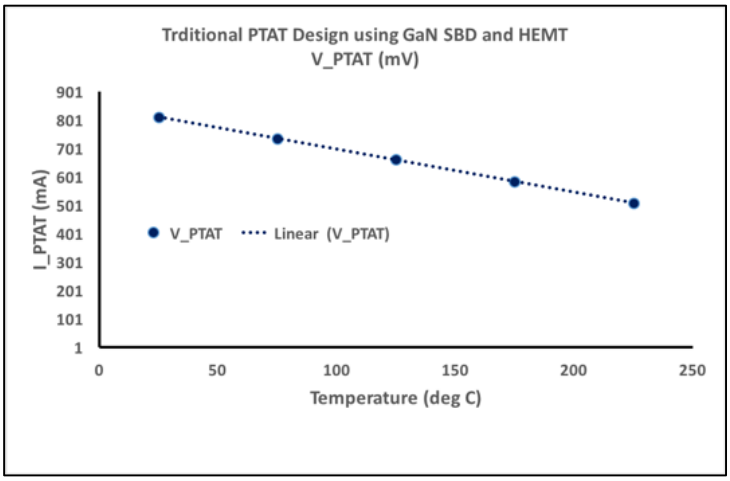

Figure 115: Traditional design V_PTAT

5.3.8 Voltage References [53] [54] [55]

Two voltage references were designed [56]. The first one was just a simple circuit using two SBDs and a HEMT. The second design included two additional SBDs to compensate for temperature that resulted in more precise reference voltage over the entire temperature range. In the temperature compensated circuit below, SBDs D3 and D4 are source degeneration diodes

and provide temperature compensation of D1 and D2. As the temperature goes up, the diode and HEMT current drops and V_{ref} tends to increase as the voltage drop across D1 and D2 gets smaller. With source degeneration, a larger effective V_{gs} tends to push the current up and inhibits rise in V_{ref}.

Measurements show that this V_{ref} has 166ppm accuracy.

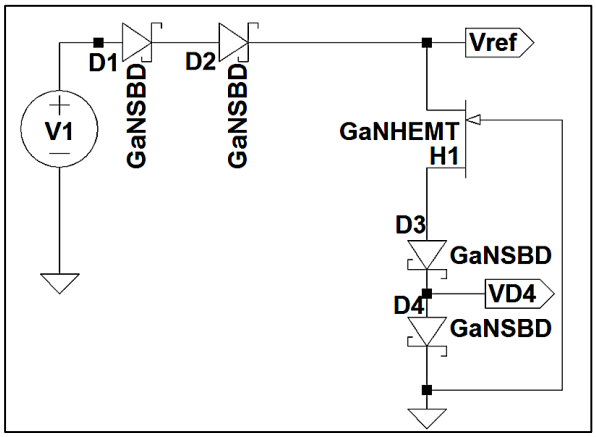

Figure 116: Temperature compensated (TC) voltage reference

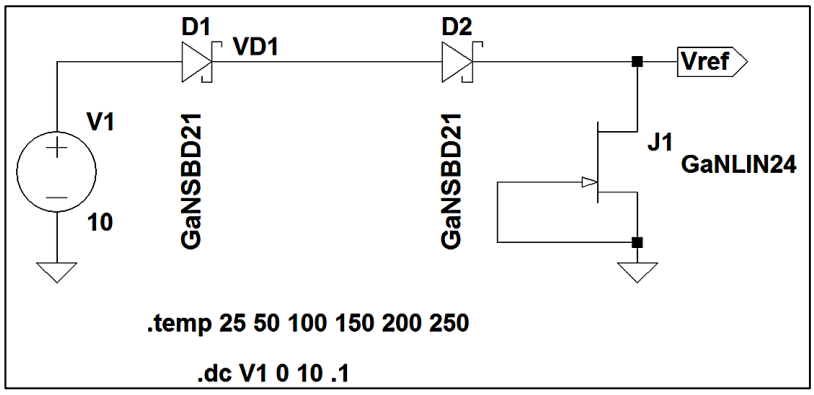

Figure 117: Voltage reference without source degeneration

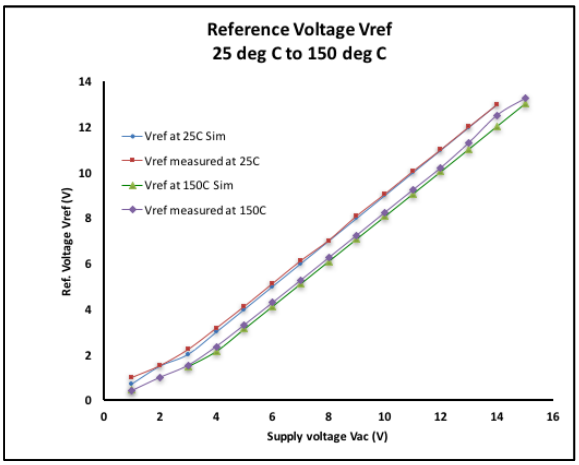

Figure 118: V_{ref} - Simulation vs Measurements

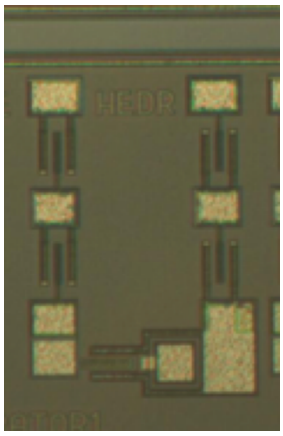

Figure 119: TC Voltage Reference

5.3.9 Comparators [53] [57]

Three different comparator configurations of increasing complexity were designed to determine the one that would best work for the final solution. All three variants were configured as a differential pair with pull up loads [58]. In conventional CMOS circuits, PMOS transistors are used as current source loads. In this design, no complementary devices are available. Instead, d-mode GaN

HEMTs are used in linear mode to emulate resistive loads. In the CO102 version, the drive stage HEMTs in the circuit had to be made several times larger than the active load in order to ensure a smooth fast transition occurs at the output when Vin crosses V_{ref}. Since all HEMTs used are depletion mode only, the circuit bias had to be adjusted for optimum switching performance. The comparator design was kept simple with no feedback for hysteresis control because the required capacitor values could not be achieved in the wafer process at the time. Nevertheless, this comparator showed good DC as well as transient switching performance when a square wave was fed at its input node. The rise time T_r and fall time T_f were very slow, but the comparator produced a clean square waveform with negligible delay. The comparator performance was very good between 20KHz and 500KHz. Beyond 500KHz, the output waveform started to deviate from a square to a triangular wave. The comparators were functional even at 1.5MHz, though the output waveform showed a very triangular wave at the output instead of a square wave. More sophisticated comparator design is a subject of future research.

Fig. 119 shows a simplified schematic of the comparator. J1 and J2 are identical (1μm x 400μm) forming a differential pair. J3 and J4 form the active loads (1μm x 100μm). J5 and J15 form the tail current source (1μm x 100μm). Due to the process technology limitations, device width of smaller than 20μm and length smaller than 0.5μm would have violated design rules and thus would have posed fabrication risk. A conservative design approach to use larger W and L dimensions was adopted to mitigate the risk. The trade-off is that the circuit

needs a supply voltage of at least 15V to function properly. When V4 exceeds V2 (Vref), transition occurs, and the decreasing output voltage reduces the current through J4 as well as the voltage drop at node VD_J5 putting J5 and J15 in linear region, thereby accelerating the transition at Vout. The choice of W/L ratio for the HEMTs defines the sharpness of transition. As seen from Fig. 122, this circuit shows reasonable sharpness in the Vout transition from 18V (High) to 5V (Lo). The theoretical limits of maximum and minimum levels at the output are V_{DD} and (V_{DD} - I_S*$R_{J3(J4)}$), where I_S is the tail current and $R_{J3(J4)}$ is the resistance of the active loads. The small signal gain (the slope of (Vout1 - Vout2) versus (Vin – Vref) is maximum for Vin = Vref gradually falling to zero as |Vin – Vref| increases. The circuit becomes nonlinear as the input voltage swing increases [58]. The circuit was tested with Vref values of 1V and 2V for a DC transition. It was observed that as the input voltage exceeds 3.5V, the V_{OL} level starts to rise as J1 is driven in deep saturation. The gate current rises and charges up node VD_J5 causing V_{OL} to go up [60]. Self-heating also contributes to this effect. Fig. 121 shows the DC transition curve at room temperature. Due to the probe station limitations, no accurate hot chuck measurements could be done. However, the circuit was tested empirically at higher temperature on-wafer up to approximately 125^{o}C to ensure functionality. It was observed that the gain of the differential pair drops significantly as the operating current reduces significantly. This is not surprising since the characterization of a single HEMT shows that the drain current drops as much as 50% from room temperature to 225^{o}C. The drain current also deviates from its flat characteristics

beyond V_{DS} = 5V indicating a rise in the HEMT's Rds(on) leading to current collapse. The comparator can be improved by making the tail current source temperature independent to keep the drain node VD_J5 constant. It was also observed that for Vin > 5V, V_{OL} rises up losing its "Lo" state. Thus the input range for this comparator is -2V (OFF state) to +3V (fully ON state). A temperature compensated Vref worked very well as illustrated earlier in section 5.3.8. The drain-source current equation used in this design is from the charge control model

$$I_{ds} = Z\mu e\beta(V_{gs} - V_{th} - V_{ds,sat})F_s$$

where F_s is the critical electric field for velocity saturation. V_{dsat} and I_{Dsat} are given by

$$V_{Dsat} = \left(V_{gs} - V_{th} - F_s L\right) - \sqrt{\left(V_{gs} - V_{th}\right)^2 + {F_s}^2 L^2} \text{ and}$$

$$I_{Dsat} = \beta e\mu F_s \left(\sqrt{(V_{gs} - V_{th})^2 + {F_s}^2 L^2} - F_s L^{\,2}\right)$$

where Z is the gate width, L is the gate length, and β is a complicated factor obtained by solving the quadratic equation for V_{Dsat} in strong saturation [61] The voltage gain works out to

$$A_v = \frac{v_{out}}{v_{in}} = g_m r_{out} = \frac{g_{m1} r_{oJ1}}{\frac{\left[1+\left(g_{mJ1}+g_{mJ5}g_{mJ15}\right)r_{oJ1}\right]\left(1+g_{J4}r_{oJ2}\right)}{\left[1+g_{mJ2}r_{oJ2}\right]}}$$

where g_m and r_{out} are the effective transconductance and output resistance of the comparator.

The design of this comparator was deliberately kept simple to reduce complexity. A better design can be realized using bootstrapped gain boosting techniques using controlled positive feedback [62] [60].

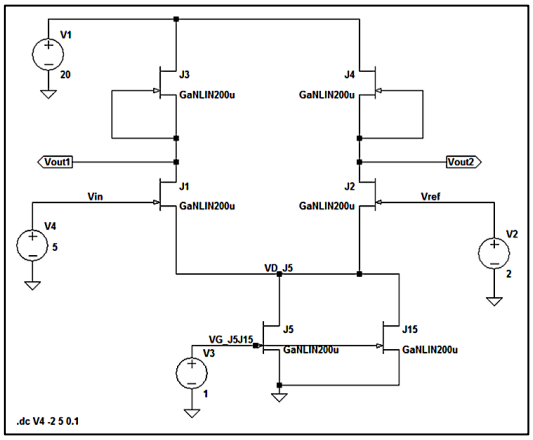

Figure 120: Schematic - Comparator CO102

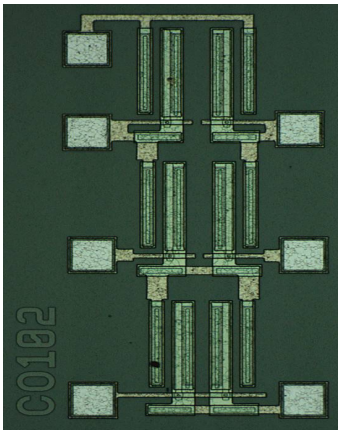

Figure 121: CO102 Die Photo

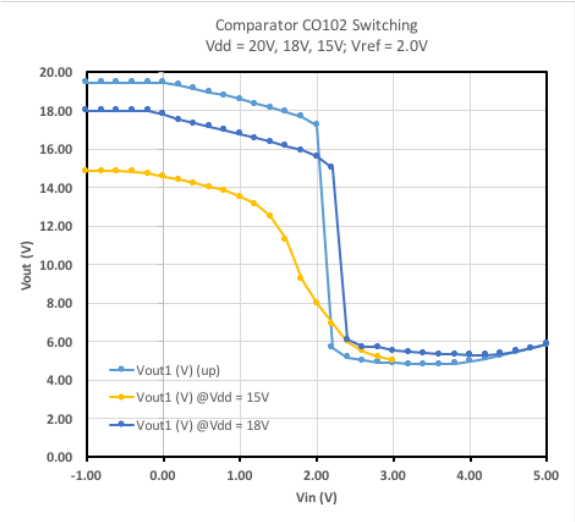

Figure 122: Comparator CO102 Output curve

CO102 DC Switching at three different supply voltages. V_{dd} = 15V is not enough for this comparator.

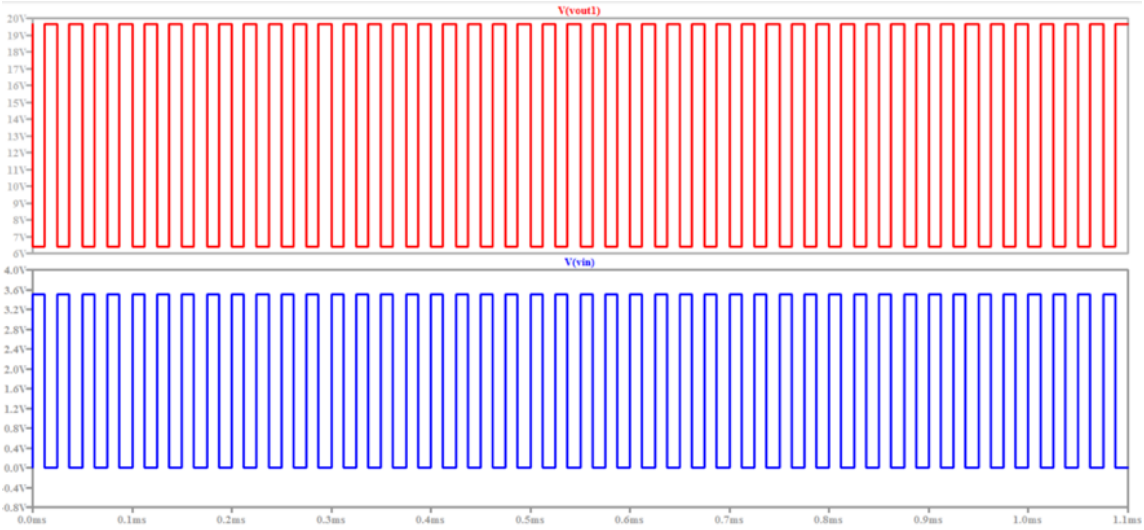

Figure 123: Comparator CO102 Simulation - Transient

Oscilloscope waveforms at 40kHz, 250kHz, 500kHz, 1.0MHz and 1.5MHz

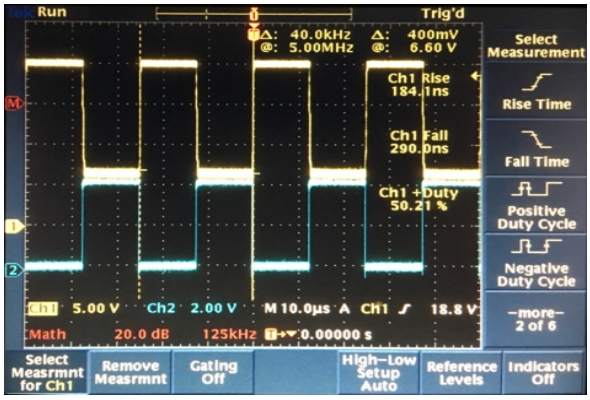

Figure 124: CO102 Switching @ 40KHz

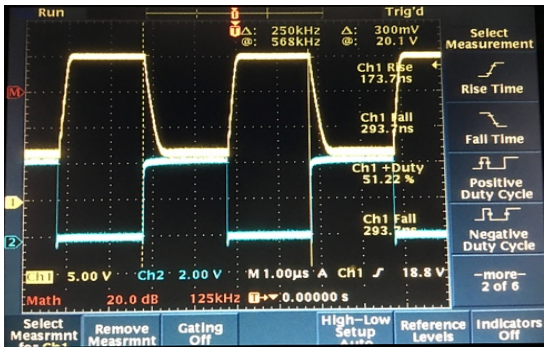

Figure 125: CO102 Switching @250KHz

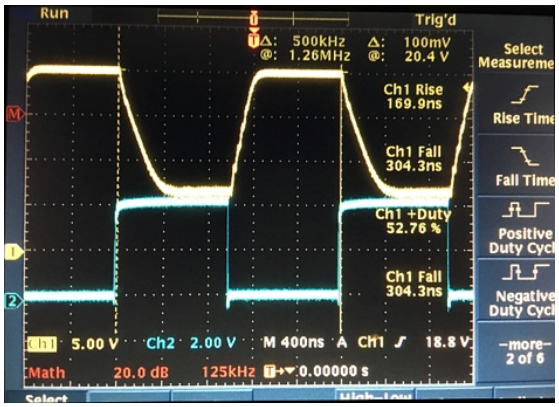

Figure 126: CO102 Switching @500KHz

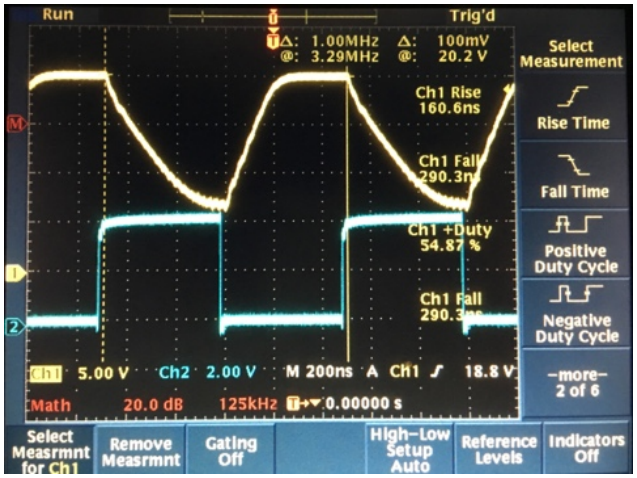

Figure 127: CO102 Switching @1MHz

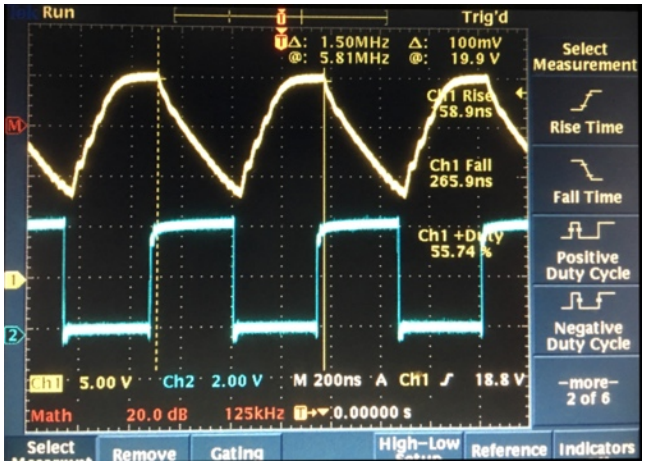

Figure 128: CO102 Switching @1.5MHz

In CO103 version of the comparator, two HEMTs in series are used for pull up loads. The HEMTs sizing is adjusted such that the output resistance of the combined configuration is higher than a single HEMT [58]. Increased output resistance and DC gain boost is achieved through cascoding the HEMTs in the driver stage. In this configuration, Vin1 is compared to a fixed Vin2 = 1V.

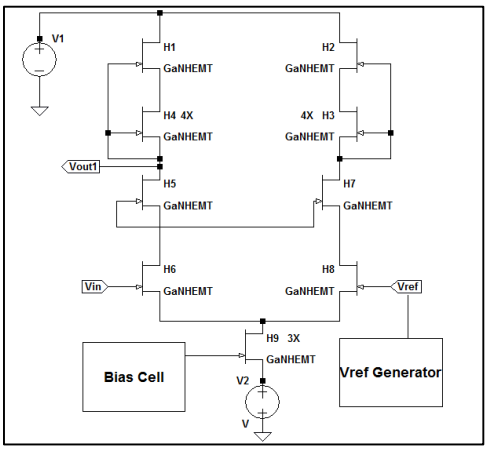

Figure 129: Comparator CO103

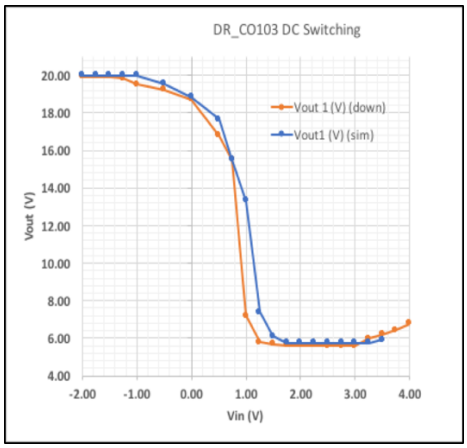

Figure 130: Comparator CO103 DC Switching

Simulation vs Measurement

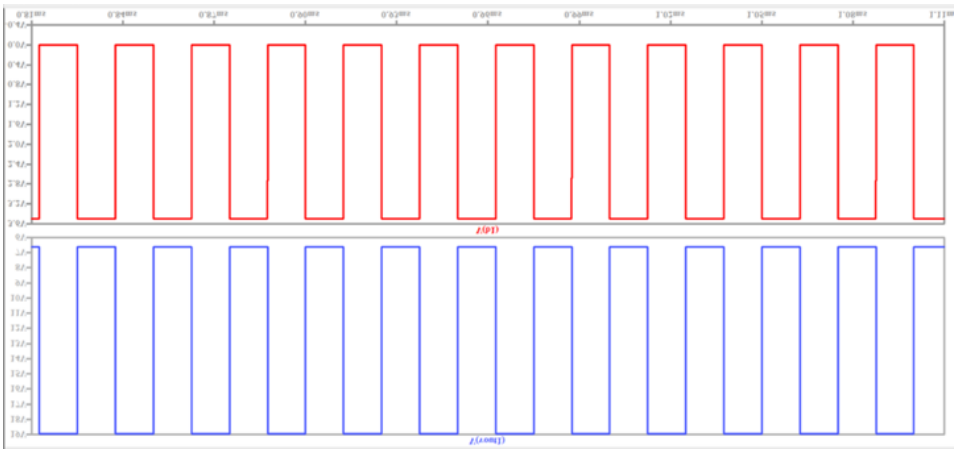

Figure 131: Comparator CO103 Simulation - Transient

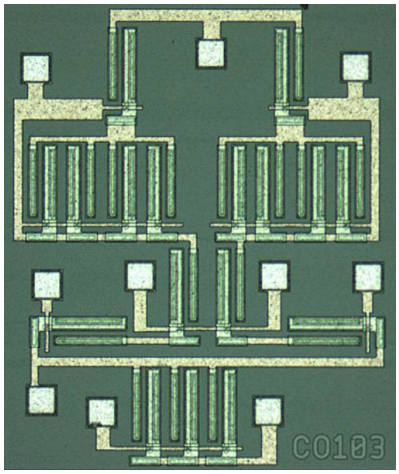

Figure 132: C0103 Die Photo

5.3.10 Application Hardware built to test the GaN SBD and HEMT:

A 25V to 400V boost converter was built to validate proper functioning of the GaN Schottky Barrier Diode and a GaN switch in a real world application, and also to study the piezoelectric stress distribution induced in the GaN layer of the AlGaN/GaN SBD under DC reverse bias voltage of -250V [43]. A current mode boost converter using an LT3757 DC/DC controller [63] that boosts from 25V to 400 V was designed for use in this study, shown schematically in Fig. 133.

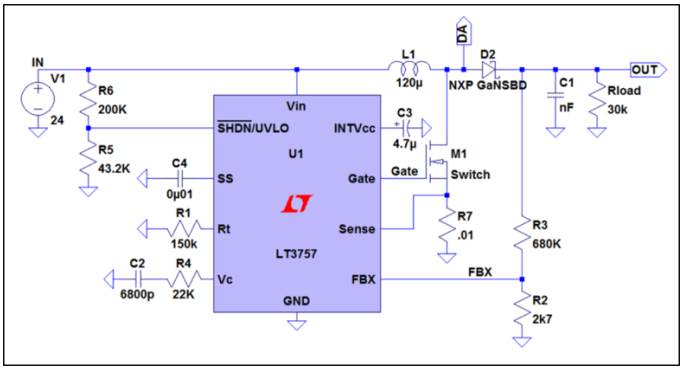

Figure 133: GaN SBD in 25V - 400V Boost Converter

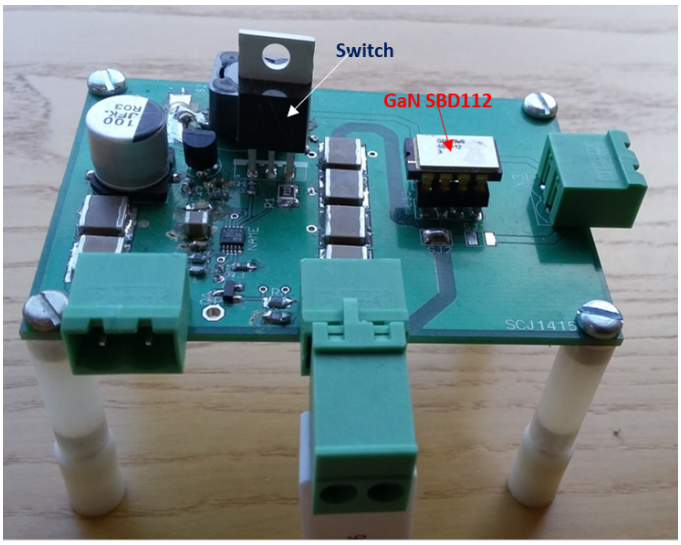

Figure 134: 25V - 400V Boost converter hardware

The start of each oscillator cycle sets the internal set-reset (S-R) latch (within the LT3757 controller) and turns on the external CoolMOS Si MOSFET switch through a gate drive of 7.2V, generated within the controller. However, there is an auxiliary 5V regulator used in this design that limits the gate drive to 5V. This switch-on is shown in the pulse train of the gate voltage of the MOSFET in Fig. 2. The switch current flows through the external current sense resistor (R7) and generates a voltage, which is added to the stabilizing slope compensation ramp. The resulting sum is fed into the positive terminal of the internal PWM comparator. When this voltage exceeds the voltage at the negative input of the comparator, the S-R latch is reset and the power switch is turned off. The voltage at the negative terminal of the comparator (Vc pin) is set by the error amplifier and is an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage. Thus, the output is regulated by the error amplifier setting the correct peak switch current level. The controller's soft-start function

(SS pin) helps limit the high peak switch currents during start-up by allowing the output capacitor to charge gradually towards its final voltage (V_{out}). The slew rate of the inductor current (I_L) is controlled by the SS function. The current mode control of the main loop (to regulate the output) simplifies loop compensation, which is achieved by a series RC network on the Vc pin. The output voltage, V_{out} is set by a resistor divider (R3, R2) by

$V_{out} = 1.6V * \left(1 + \frac{R3}{R2}\right) Vout = 1.6V * \left(1 + \frac{R3}{R2}\right)$ and in this case, V_{out}= 400 V. The conversion ratio as a function of duty cycle (D) is

$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)}$ in continuous conduction mode (CCM) operation. Maximum duty cycle D_{max} occurs when the converter has a minimum input voltage $V_{in,min}$where $D_{max} = \left(V_{out} - V_{in,min}\right)/V_{out}$ and D_{max} is 94%, in this case. An inductance L of 120 μH is chosen by calculating $L = \left(V_{in,min}/\Delta I_L f\right) * D_{max}$ where $\Delta I_L$is the inductor ripple current and f is the operating frequency. For the boost converter shown, the current in the inductor is approximately 1A at 400V. The power switch is chosen such that its breakdown voltage is higher than V_{out} by a safety margin. To maximize efficiency, the fast switching AlGaN/GaN SBD with low forward drop and low reverse leakage is used. When the switch turns off, the diode current increases from 0A to the peak inductor current and back to 0A within a short pulse as evident in Fig. 135. During the time intervals outside this current pulse, the diode is reverse-biased with a V_R equal to V_{out}. Therefore, the diode used has a peak reverse breakdown voltage of 600V, which is more than sufficient to withstand V_{out} plus any ringing from anode to cathode

during on time. The average forward current of the diode is approximately equal to the output current of 1A and the output capacitance is chosen for a maximum output ripple of 2%. The switching frequency of the converter is 100kHz set by an external resistor, Rt = 150kΩ. The choice of Rt between 150kΩ and 10kΩ determines the switching frequency between 100kHz and 1MHz, respectively. Low frequency operation (100kHz) is chosen in the design of this boost converter circuit as it improves the efficiency by reducing gate drive current and switching losses in the switch and diode.

Micro-Raman spectroscopy was used to directly measure the stress distribution. The highest piezoelectric stress measured was 380+/-40MPa near the anode field plate edge. Continuous operation of the SBD under this condition may lead to cracking of the GaN layer due to mechanical stress in addition to the heat generated. The on-time of the switch 5us. This study was carried out in collaboration with University of Bristol [43]

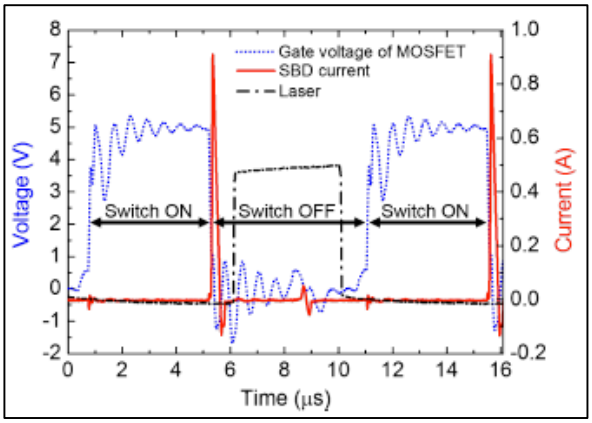

Figure 135: Switch voltage and Diode current during boost operation

Pulse train of the gate voltage of the switch and current of the SBD during boost converter circuit operation. The position of the laser pulse along the pulse train, used to probe the piezoelectric stress in the GaN buffer is overlaid.

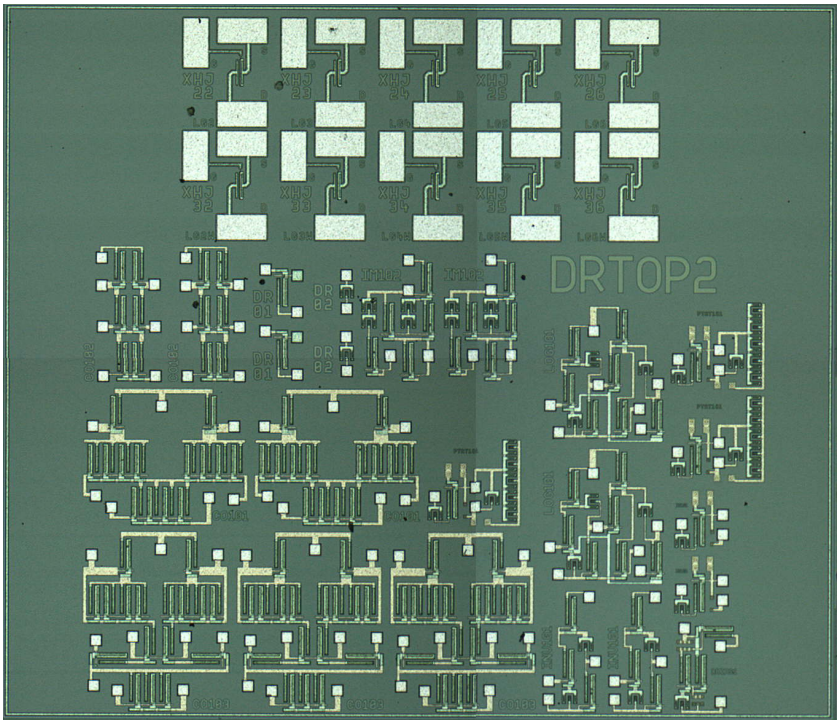

Figure 136: Die photo micrograph of DRTOP2 design tile

Die micro photograph of the design tile DRTOP2 of all the sub-circuit cells. Stand-alone HEMTS of various W and L are at the top quarter of the tile and the circuit building blocks occupy the rest of the area. Tile area of 3.5mm x 3.5mm was used for the layout. The pads were 50μm x 50μm in size and thus posed some challenge in probing the circuits as some of the circuits required seven probes to be used at the same time.

5.3.11 Final design: Monolithic integration of the thermal shutdown circuit with a large geometry multi-finger 600V HEMT

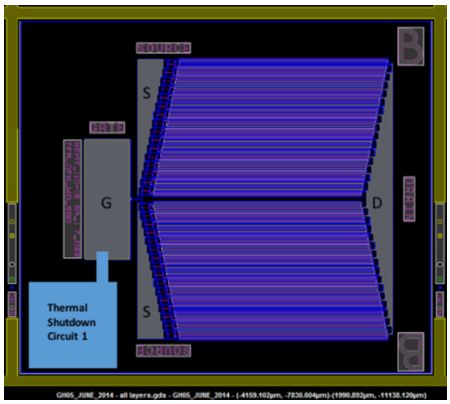

Figure 137: Power HEMT area available for monolithic integration

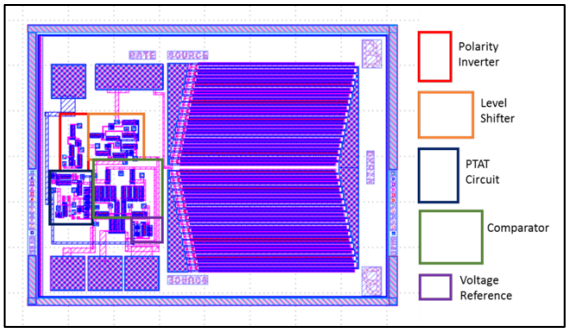

Figure 138: Power HEMT integrated with thermal shutdown circuit - with polarity inverter

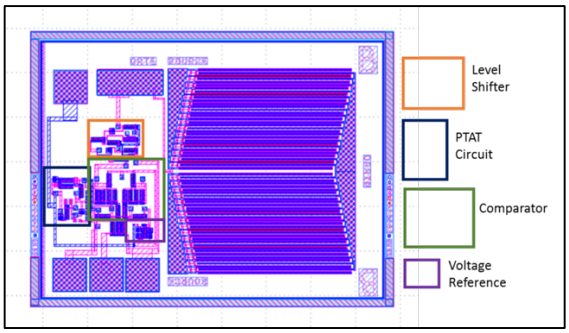

Figure 139: Power HEMT integrated with thermal shutdown circuit - without polarity inverter

Chapter 6

6.1 Conclusion

This work has presented an experimental chip design and fabrication of a novel thermal shutdown circuit monolithically integrated with a large geometry 600V GaN-on-Si power HEMT. This is the first time that the feasibility of using an integrated circuit approach for such a thermal protection circuit using only the normally-ON GaN devices has been demonstrated in a high voltage GaN-on-Si technology in a standard silicon fab.

The study started with thermal characterization of Schottky Barrier Diodes to gain an understanding of the self-heating phenomena as well as the time scale on which the switching device (HEMT) and diodes start exceeding the acceptable junction temperature. A 25V to 400V boost converter was used as an application for these devices operating at 100kHz and 200kHz. It was observed that the devices experience significant increase in heat within 5 to 10 microseconds. GaN devices enable design for high frequency applications in low MHz range, but at present, the applications are designed in low hundreds of kHz due to limitations in magnetic components. The integrated thermal shutdown scheme thus provides a very useful self-protection feature for a power discrete HEMT in high power applications such as solar inverters, switch mode power supplies (SMPS) and motor drive systems.

The design process started with investigation of three different methods, first building hardware designed with off-the-shelf components and discrete GaN devices. Out of these three, a PTAT based design was selected to be integrated on-chip. An array of stand-alone GaN HEMTs and SBDs were designed that were to be used in designing the analog and digital building blocks and electro-thermal models were extracted from small geometry device measurements. A cell library was developed for the sub-circuits that were used in designing the integrated circuit. After fabrication, each cell was tested under various conditions at a wafer level. All the cells were functional on the very first silicon. Measurement results for all the circuits were in good agreement with simulation results.

In summary, this work leads to a conclusion that integrated circuit approach can be adopted to design feature rich large geometry power HEMTs in GaN-on-Si process technology. The lack of complementary devices is a serious limitation in designing digital control circuits in today's technology, but this barrier is expected to be overcome in the coming years.

6.2 Future Research

The two final design versions of the monolithically integrated thermal shutdown circuit (Fig.s 138, 139) with the power HEMT have been completed and ready for tape out. After fabrication, these designs will be packaged in an 8x8 ThinPak surface mount power package for testing. A more sophisticated design to put the power HEMT in a sleep-mode under overheat condition will be investigated. When the power HEMT cools down, the circuit will turn the device

back on. The timing of sleep mode is estimated to be a few tenths of a μs and the wake up timing is estimated to be less than 10 μs.

At this time, only a small level of integration is possible in the wafer process used, but next level of integration will be possible as the technology matures. Future research includes developing a wide bandgap (WBG) process technology that will be more suitable for integrated circuits rather than discrete devices. There is a great demand for CMOS-like integration in the WBG semiconductor industry for power and RF applications with more on-chip control features. The interim step of multi-chip modules where CMOS digital (or analog) chips are co-packaged with a WBG device (for example, a half bridge power module) can then be eliminated. Further development of p-channel HEMT, dual gate HEMT, enhancement mode HEMTs and high quality resistors and capacitors is also being investigated. In addition, the author is actively involved in developing an engineered substrate technology that will enable large diameter wafer scaling at 6-inch, 8-inch and 12-inch for WBG semiconductors.

Summary of future research plans:

- Technology development for WBG integrated circuits
- WBG and CMOS integration
- Engineered substrates

Along with research, the author plans to teach university level device physics, compound semiconductors and circuit design courses.

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