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A Distance-Immune Low-Power Near-Field Data-Link for Biomedical Implants

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A Distance-Immune Low-Power Near-Field Data-Link for Biomedical Implants

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical and Computer Engineering

by

Alireza Yousefi

2018

ABSTRACT OF THE DISSERTATION

A Distance-Immune Low-Power
Near-Field Data-Link
for Biomedical Implants

by

Alireza Yousefi
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2018
Professor Asad A. Abidi, Co-Chair
Professor Dejan Marković, Co-Chair

In the past decade, there has been a great interest in bionic and neural implantable electronics to investigate the human body's working, to understand different physiological conditions, and to cure disease. Among them, neuromodulation systems have been found by the neuroscience community as a promising tool to decode the functioning of the brain, and an alternative strategy for diagnosis and treatment of neuropsychiatric disorders. Today's clinical neuromodulation systems, however, may suffer from many serious constraints. For instance, many are wired refrigerator-size electronic setups, which immobilize the patient, increase the risk of infections, and have a limited duration of operation[1]. The next generation of neuromodulation systems should contain a robust, energy-efficient solution to deliver wireless data and power.

In this work, first, we present an implantable distance-immune ultra low-power data link which would be used in a biomedical implant that most of the time relays monitoring data to a unit outside the human body. The near-field data link is based on a free-running oscillator tuned by coupled resonators. We have studied the properties of the inductively-coupled link

[1]Since, with these bulky setups, the patient has to stay at the hospital, the duration of study (recording and stimulation) may not be longer than a few weeks.

and derive its key features and constraints. After understanding the design space, we have designed and built transceiver chips in 40 nm CMOS technology which enable a bidirectional wireless connectivity. Data can be transferred in half-duplex at up to 4 Mbps in a Load Shift Keyed (LSK) uplink, and up to 2 Mbps in an ASK downlink. With one automatic adjustment, the link can maintain a reasonable error rate of less than 10^{-6} (BER$< 10^{-6}$) over coil separations of up to 4.5 cm.

In monitoring body/brain activities, with an air data rate of 4 Mbps, this wireless link can multiplex 16b-words acquired at 0.5 kS/s from each of up to 500 neural probes. Typically, the implant will transmit data on the uplink most of the time; the circuit reported here is optimized for this function, consuming less than 0.1 pJ/bit at 4 Mbps. When receiving on the downlink at 2 Mbps, the implant consumes 5 pJ/bit.

Second, we have integrated the designed data link in a state-of-the-art, human-quality implantable neuromodulation system, and verified its communication performance in bench-top and *in-vitro* environments. The data link achieved a maximum range of 3 cm packaged in a titanium can and using a bio-compatible coil.

Third, we describe a Medium Access Control (MAC) system for the designed transceivers (PHY layer). The MAC layer is designed as a stand-alone accelerator on an FPGA platform, capable of handling incoming and outgoing data in parallel. In the next generation of the data link, we can migrate this to an Application Specific Integrated Circuit (ASIC) to reduce the power consumption and the system form factor.

The dissertation of Alireza Yousefi is approved.

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Dejan Marković, Committee Co-Chair

Asad A. Abidi, Committee Co-Chair

University of California, Los Angeles

2018

"In the name of the Most High"

To my parents,

and my wife,

for all their love, kindness, patience and support.

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ACKNOWLEDGMENTS

I would like to take this opportunity to thank my advisors, and PhD committee co-chairs, Prof. Abidi and Prof. Marković . Prof. Abidi has been supportive since the beginning of my PhD program. He has constantly encouraged me to pursue high-quality research all along my PhD study. Prof. Marković gave me the invaluable opportunity to join his research group and to be involved in the design of the next-generation neuromodulation systems. It has been a great privilege to have them as my teachers and advisors. I cannot thank them enough.

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ADC analog-to-digital converter.

AES advanced encryption standard.

AFE analog front-end.

AM aggregator module.

ASIC application-specific integrated circuit.

ASK amplitude shift keying.

AWG American wire gauge.

BBFD bang-bang frequency detector.

BBPD bang-bang phase detector.

BCI brain-computer interface.

BER bit error rate.

CCU central control unit.

CDR clock and data recovery.

CM control module.

CMOS complementary metal oxide semiconductor.

CRC cyclic redundancy check.

Ctrl control.

DAC digital-to-analog converter.

DALYs disability-adjusted life years.

DBS deep brain stimulation.

DC direct current.

DCO digitally controlled oscillator.

DSM delta-sigma modulator.

DT dissection theorem.

EM electromagnetic.

ERM external radio module.

FET field-effect transistor.

FIFO first in, first out [data buffer].

FPGA field-programmable gate array.

GPIO general purpose input output.

IC integrated circuit.

IoT internet of thing.

ISI inter-symbol interference.

LFP local field potential.

LLNL Lawrence Livermore National Laboratory.

LSK load shift keying.

MAC media access control [layer].

Mbps mega bit-per-second.

MCU micro-controller unit.

MISO master-in-slave-out.

MOSI master-out-slave-in.

NFC near-field communication.

NIH National Institutes of Health.

NM neuromodulator module.

PC personal computer.

PCB printed circuit board.

PD phase detector.

PER packet error rate.

PHY physical layer.

PRBS pseudo-random binary sequence.

PVT process-voltage-temperature.

QFN quad flat no-leads [package].

RD running disparity.

RF radio frequency.

SCLK serial clock.

SNR signal-to-noise ratio.

SPI serial peripheral interface.

SS slave select.

TDD time-division duplex.

TSMC Taiwan Semiconductor Manufacturing Company.

UCLA University of California, Los Angeles.

UCSF University of California, San Francisco.

USB universal serial bus.

WHO World Health Organization.

VITA

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CHAPTER 1

Introduction

1.1 Motivation

According to the World Health Organization (WHO), hundreds of million people, nearly one in seven of the world's population, suffer from different neuropsychiatric disorders [8] such as Alzheimer's disease, Parkinson's disease, epilepsy, depression, strokes, etc. This impairs motor and non-motor functions during the patients' daily activities [9]. For instance, 1/3rd of patients with Parkinson's disease lose their jobs within one year of diagnosis, and after five years, most of them can barely find full-time jobs. These disorders are debilitating. The available statistics on the prevalence of mental illnesses, published by the National Institutes of Health (NIH), shows that neuropsychiatric disorders are the leading cause of disability in the US (Fig. 1.1) [10].

Despite this pervasiveness, the neuroscience community has not been able to understand the mechanisms underlying many of these disorders. In recent years, there has been greater interest to study this type of diseases [11, 12, 13, 14, 15, 16]. At the same time, there is a search for an effective treatment for these conditions [17, 18, 19]. The neuromodulation system is one of the fundamental tools that can give deep insight into brain's functions and increase the observability into neural systems that may explain brain disease [20, 21, 22, 23]. In neuromodulation (also know as nerve-stimulation) systems, direct electrical currents are delivered to a region of the brain[1] to alter their activity (Fig. 1.2).

Modern neuromodulation systems must be capable of simultaneously monitoring the activity of the target neurons as a stimulus current is being applied. Such systems not only

[1]The target neurons which are responsible for the condition.

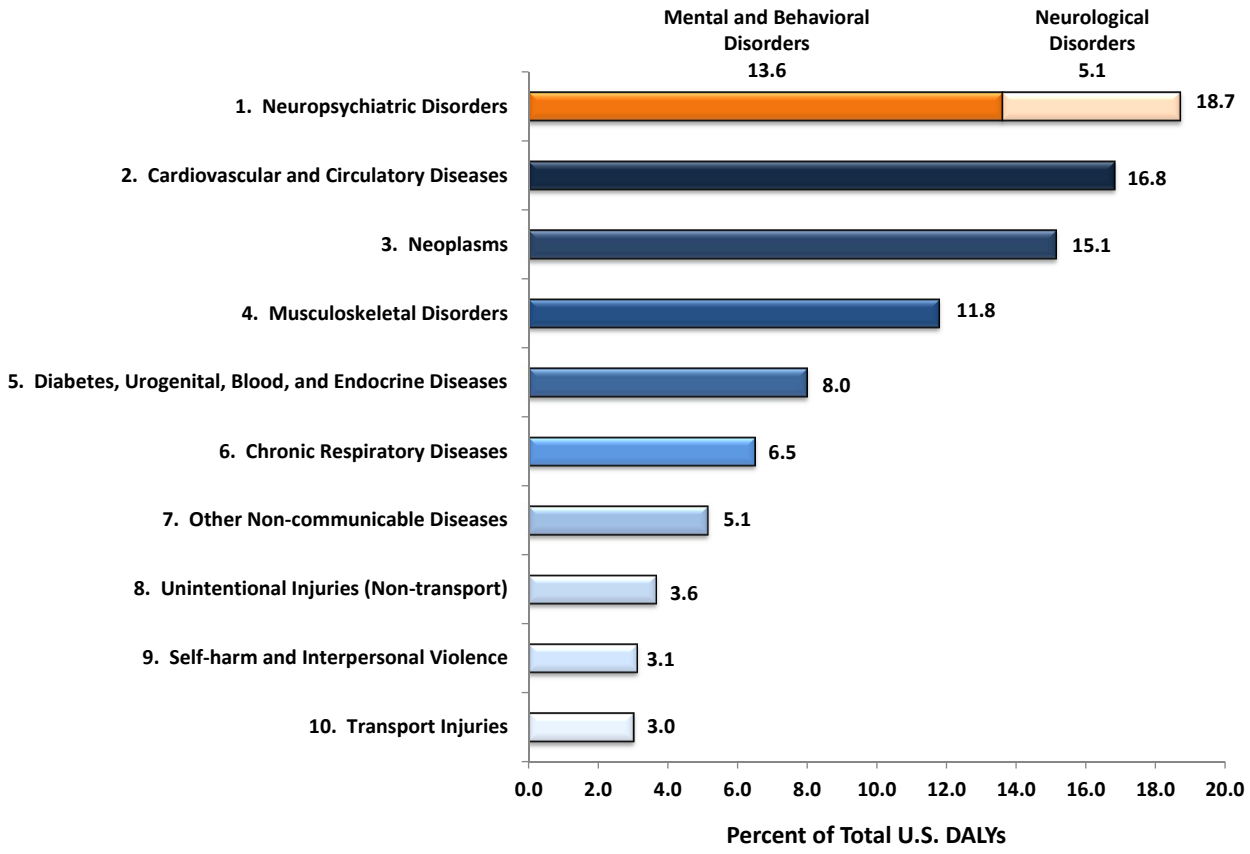


Figure 1.1: Top 10 leading disease/disorder categories contributing to global disability-adjusted life years (DALYs).[1]

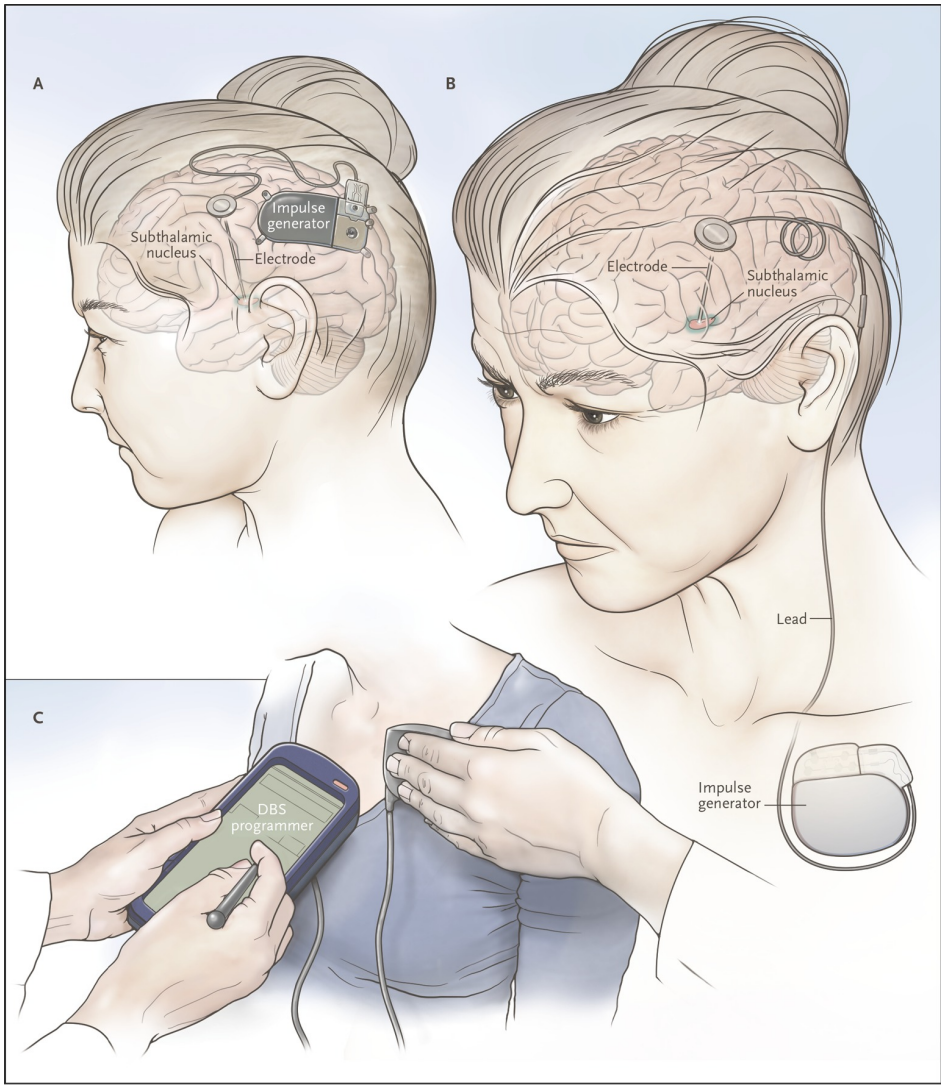


Figure 1.2: Implantable neuromodulation system (deep brain stimulation, DBS) [2].

may be used for diagnostics purposes, but also can be employed for treating the neurological conditions, especially in the cases where traditional treatments such as surgery, pharmaceutical and psychotherapeutics have failed [9, 24, 25]. Eventually, these systems with concurrent sensing and stimulation have the potential to become the platform for implementing closed-loop nerve-stimulation and a brain-computer interface (BCI) [26, 27].

Current neuromodulation technologies used by the neuroscience community suffer from multiple constraints. They are bulky, wired setups which immobilize the patients and put them at the risk for various infections (Fig. 1.3). They can modify the patient's behavior [28],

Figure 1.3: Today's neuromodulation technology: bulky, rack-mounted electronics,wired setups which immobilize the patient.

and also constrain the duration of recording and stimulation because the patient has to stay in the hospital while he/she is connected to the bed-side setup during the study period. This imposes a considerable cost to the patient and the hospital. However, if a neuromodulation system could be implanted in the patient's body, he/she would be sent back to his/her normal life after a short recovery time [29]. A wireless implantable low-power data-link is therefore an integral part of the next-generation neuromodulation system. Through the data link, the recorded neural data can be extracted for monitoring the brain, and stimulation parameters can be updated on the implant at will.

The wireless data link can also play a foremost role in future closed-loop applications (Fig. 1.4). In these systems, an algorithm governs stimulation parameters based on the recorded neural signals to improve effectiveness of the therapy, and to mitigate open-loop stimulation side effects, such as mania, depression, anxiety, hallucinations, suicidal thoughts, etc [30, 4, 31, 32]. Since, at this stage, neuromodulation devices for closed-loop applications are more of an investigational platform, the algorithms can involve significant computational load (e.g. machine learning algorithms [33, 34]). Due to power and area constraints in the implant, it might not be possible to implement the complete algorithm in the implant; therefore, it must be partially externalized with the data link, to allow greater computational freedom [4]. For instance, there may be an internal fast control loop for treatment in the implant, but a slower, more complicated external loop in the cloud which determines and

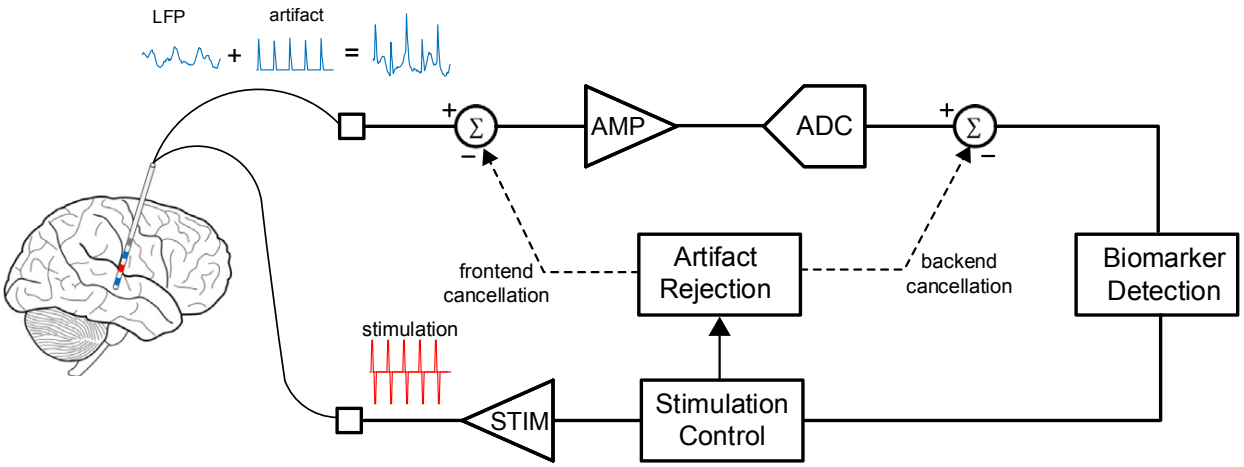


Figure 1.4: Block diagram of a closed-loop neurostimulation system [3].

updates the hyper-parameters in the algorithm through the wireless link (Fig. 1.5).

This dissertation will present a robust bidirectional low-power data link for next-generation neuromodulation implants. Although we are targeting this specific application, the data link can be employed in any neural and bionic implants and may inspire future work in NFC and IoT technologies.

1.2 Dissertation Outline

Chapter 2 presents the goals and challenges of the data link design. It goes over the prior state-of-the-art data-link for biomedical applications. The theoretical analysis on the data link is presented and the link features and constraints are identified. After understanding the design space, it discusses the different design choices and solutions. This chapter also explains the details of the data link hardware implementation and presents the measurement results. Lastly, the proposed data link is compared with the state-of-the-art biomedical near-field telemetry solutions.

Chapter 3 explains how the data link is integrated into an implantable human-quality neuromodulation device. The detailed measurement results of the neuromodulation system, CM and ERM, are included in this chapter, as well.

Chapter 4 discuss the MAC layer for the near-field transceiver chips (PHY layer), the

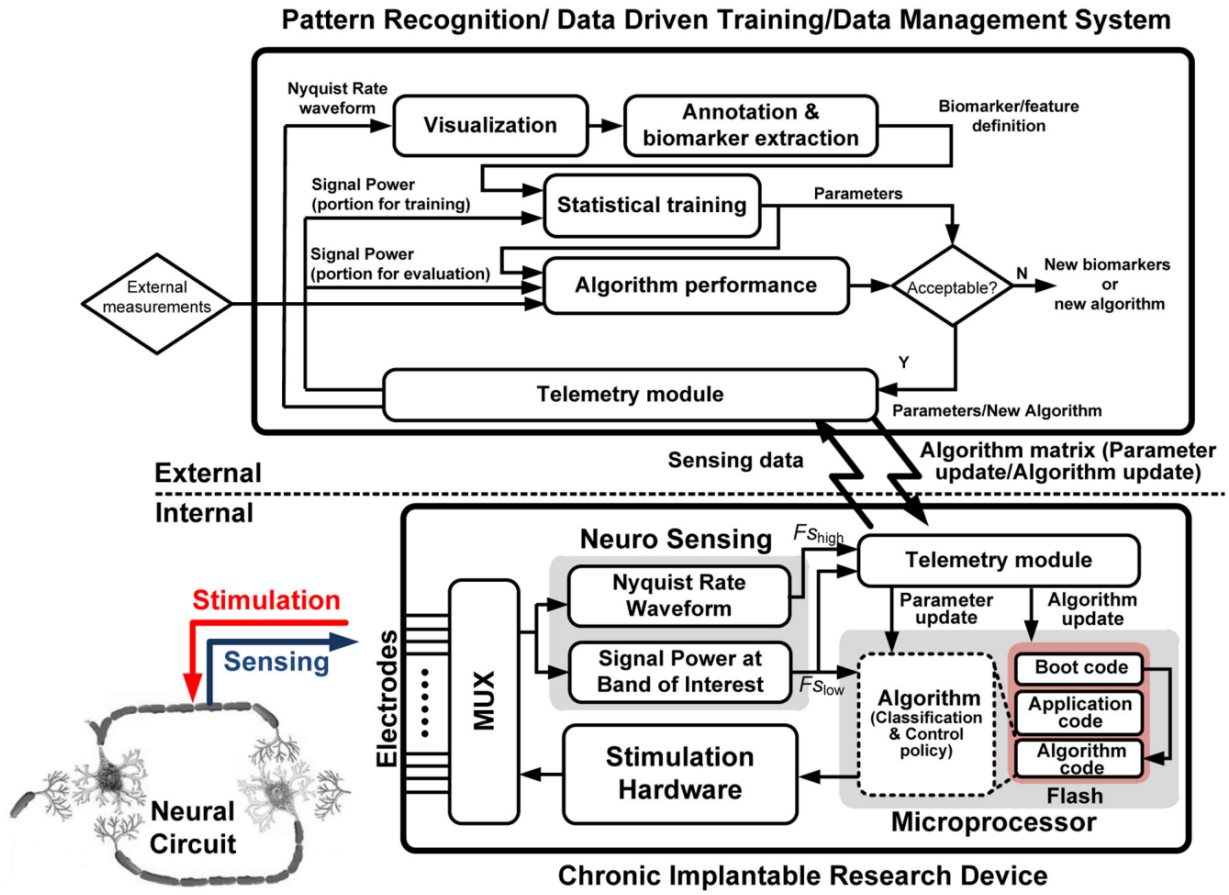


Figure 1.5: Diagram of a hybrid implantable neuromodulation system with internalized and externalized control loops.[4].

motivation to implement it as a stand-alone accelerator, the hardware realization on the FPGA, and its measurement results.

Chapter 5 concludes this dissertation. It discusses the main contributions of this work and possible future research.

CHAPTER 2

Distance-Immune Low-Power Data link Design

2.1 Design Goals and Challenges

Before describing the design of the data link, we must briefly discuss the design requirements and challenges. This will help us assess prior art and can guide us to an effective solution.

The bidirectional data link would be used in a biomedical implant, where communication is asymmetric (see Fig. 2.1). This means that most of the time the link relays monitoring data (i.e. neural recording and implant status) from the implant to an external unit outside the human body. Sometimes configuration data (i.e. modified stimulation or closed-loop system parameters) needs to be sent to the implant, but this is infrequent.

The link must support a data rate of $2 \sim 4\,\text{Mbps}$. For instance, with a net data rate of 2 Mbps in monitoring body or brain activities, the link can multiplex 16b-words [35], acquired at 500 samples per second[1], from about 250 neural probes.

The data link must consume very low power, especially in the implant, where the available energy to supply the unit is restricted and the temperature rise can not exceed 1°C [37]. Hence, the implant transceiver should be designed to consume ideally as low power as a single-channel neural recording front-end (i.e. $\sim 10\,\mu\text{W}$ [35, 38, 39]). Although the power limitation for the external transceiver is relaxed compared to the implant's, it still must be low (i.e. $\leq 1\,m\text{W}$) for long battery life (e.g. ear-piece in Fig. 2.1).

Prior works overlook the very important need for immunity to distance[2]. In practice, the

[1] Adequate sample rate to acquire waveforms of local-field-potential (LFP) [36].

[2] Only a few works have discussed and tried to address this issue [40, 41] in the data link.

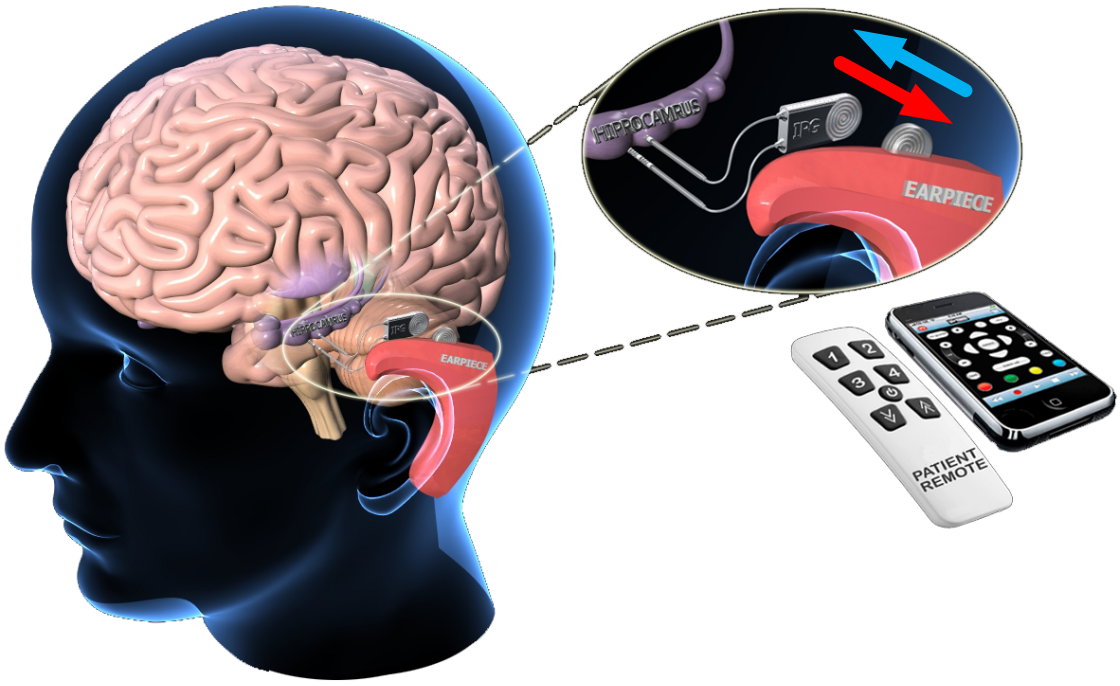


Figure 2.1: A neural/biomeical implant in the brain communicating through a bidirectional data link.

link distance (i.e. communication range) is prone to change due to patient movements, and different placements during surgery [42]. Considering the tissue thickness of different body regions [43], the data link must be able to cover a range of up to 3 cm while the bit error rate (BER) is lower than 10^{-6}.

The specifications of the data link are summarized in Table 2.1.

Table 2.1: Bidirectional data link specifications.

Data rate	$\geq 2 \sim 4$ Mbps
Power consumption (Implant/External)	$\leq 10\,\mu$W / $\leq 1\,m$W
Communication range	≥ 3 cm
Bit error rate (BER)	$\leq 10^{-6}$

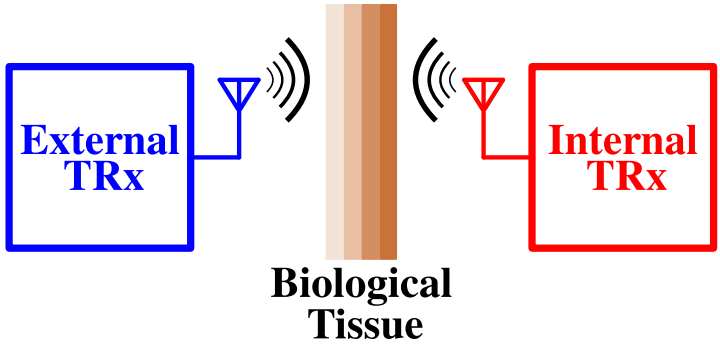


Figure 2.2: Far-field approach.

2.2 Review of Prior Art

Looking at prior work in bio-telemetry, the proposed solutions can be classified into two major categories: far-field approach and near-field approach.

2.2.1 Far-Field Approach

In far-field or also know as radiative approach, the fields detach from the transmitter antenna, travel the distance between the two sides as electromagnetic (EM) waves and later are picked up by the receiver antenna (Fig. 2.2).

To have an effective radiation for a given size of the antenna, usually the frequency of operation used in this approach is relatively high (e.g. higher than 1 GHz) compared to the near-field approach. Since power absorption in biological tissues increases with frequency ($\sim f^2$), the power dissipation in the body can be excessive (Fig. 2.3) [5, 44, 45, 46]. Consequently, the works which employ this approach usually have high power consumption (on the order nJ/bit [47, 48, 49, 50, 51, 52, 53]), although at high data rates, they may achieve a competitive power performance (on the order of few to tens of pJ/bit [54, 55, 56, 57]).

Unlike EM wave propagation in free space, the human body is a more complicated propagation medium. There are multiple layers of various biological tissues and fluids such as fat, bone, muscle and blood, each with different permittivity (dielectric constant) and, in general, different propagation characteristics. This inhomogeneous medium can cause variable channel conditions and propagation delays making it difficult to have a robust data link

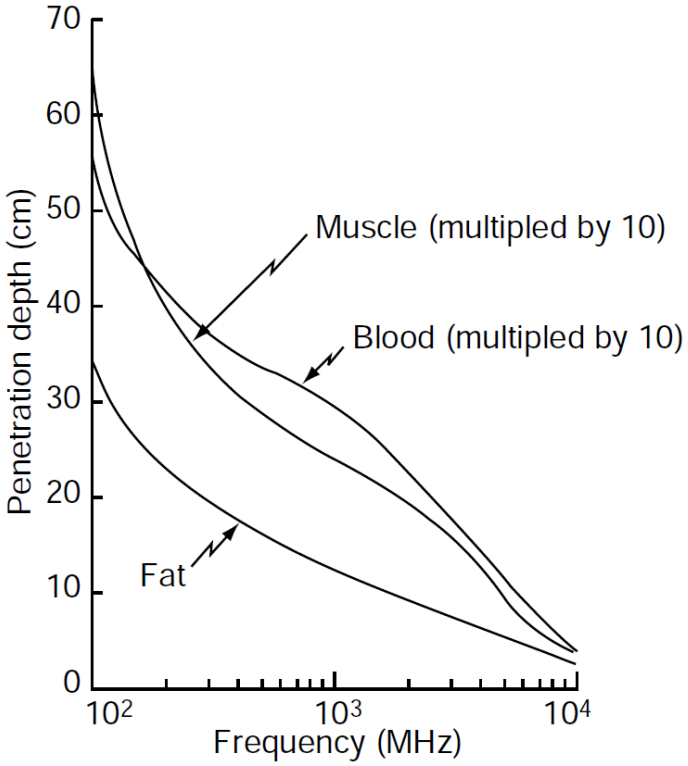


Figure 2.3: Penetration depth of different body tissues plotted versus frequency [5]. As frequency increases, the penetration depth decreases and therefore EM waves attenuate faster in tissue.

[42]. Since the propagation characteristics are strong function of frequency and may vary from person to person[3] [59, 60, 61], it would be hard to find a universal optimum solution for this multi-layered structure.

2.2.2 Near-Field Approach

In contrast, with the near-field approach (inductive coupling), the fields are confined to the vicinity of the link with very small radiated energy (Fig. 2.4). Since the coils generate mainly non-propagating-mode of EM waves and data communication happens through it, the link usually has a short range[4] [40, 45, 46, 62, 63, 64, 65, 66, 67, 68, 69, 70]. This might seem to be a negative, but for the application that we are targeting, it is useful. This can

[3]The propagation characteristics may even change time to time for a person under different conditions [58].

[4]A few centimeters assuming the coils diameters are also few centimeters.

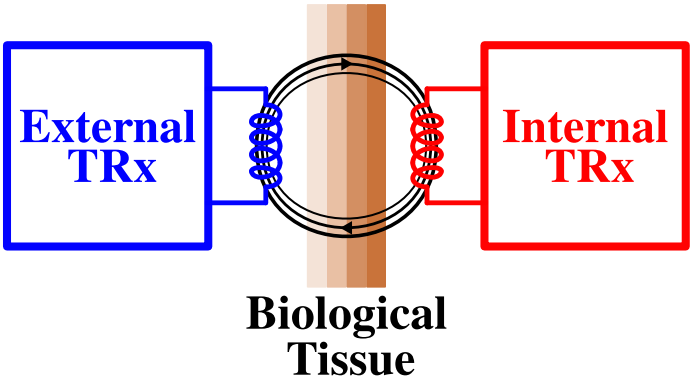


Figure 2.4: Near-field approach.

avoid eavesdropping and therefore achieves higher security, a critical feature in biomedical telemetry. Also, the carrier frequency can be reused for another link in a different region of the body provided the two links are far enough from each other.

Usually the frequency of operation is limited to tens of MHz, and therefore it has lower power absorption in water-rich environments such as biological tissues. Unlike the far-field approach, near-field inductively-coupled links have negligible variations in channel conditions even in an inhomogeneous lossy medium. That is because biological materials have permeability ($\mu = \mu_0\,\mu_r = \mu_0\,(1+\chi)$) close to the free space permeability (μ_0) [6]. Fig. 2.5 shows the susceptibilities for different materials ($\chi = \mu_r - 1$) and, as can be seen, the susceptibilities of human tissues are infinitesimal; most of them in the range from -7 to -11 ppm, and therefore close to that of free space ($\chi_0 = 0$).

Nonetheless, there is one limitation in this type of data link and that is to do with its sensitivity to the coil separation[5] . Addressing this issue is crucial for the technologies that need to support mobility.

2.3 Data Link Architecture

We have taken the near-field approach and therefore designed an inductively-coupled data link. Fig. 2.6 shows the data link as two modules: an external unit, worn outside the human

[5]By changing the distance, the coupling factor (k) will vary, and so will channel characteristics.

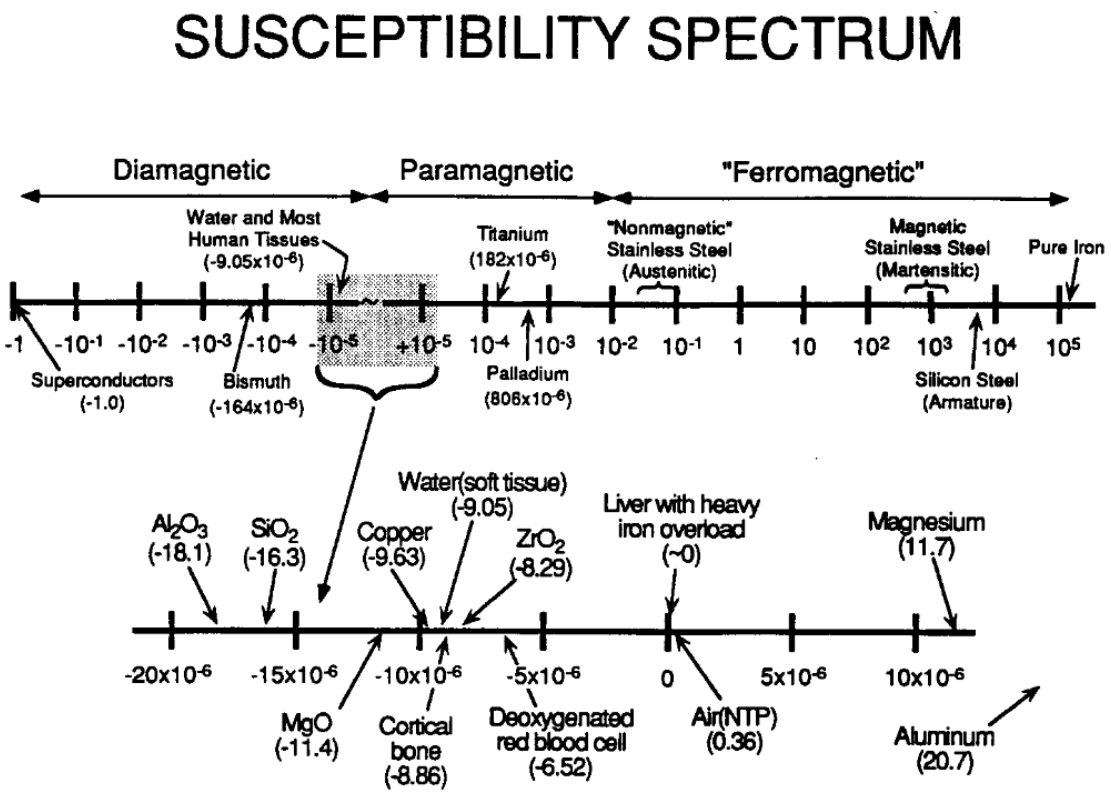


Figure 2.5: Susceptibility spectrum ($\chi = \mu_r - 1$). The upper diagram has a logarithmic scale, however, the one at the bottom uses a linear scale (ppm) [6].

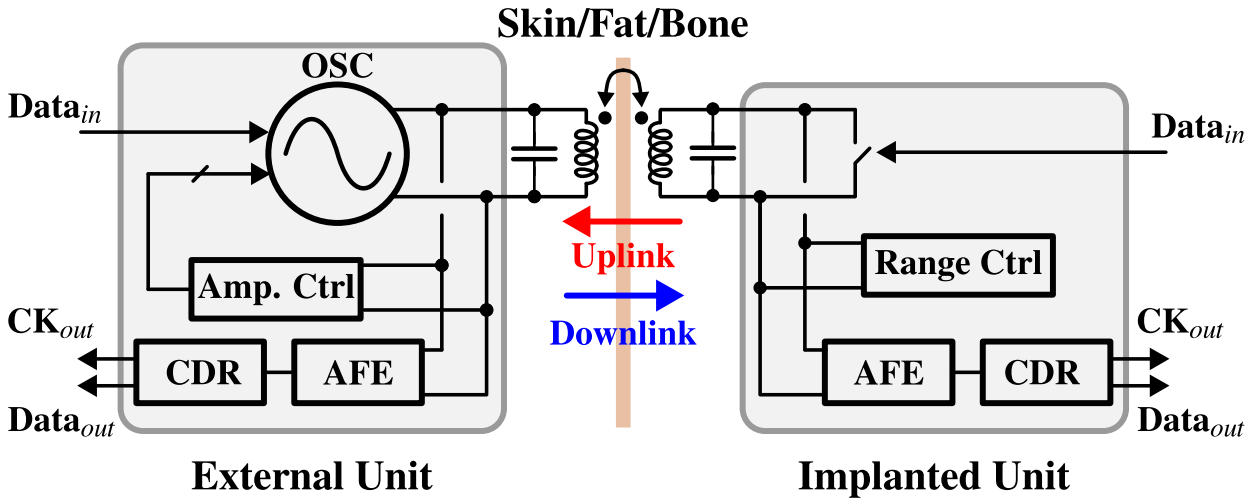


Figure 2.6: Data link architecture.

body close to the skin, and an implanted unit, surgically embedded in the body. The link has two coupled resonators at its core, each of which resonates at $f_0 = \omega_0/2\pi$[6]. Amplitude modulation is employed in both uplink and downlink. A simple envelope detector can therefore be used as a demodulator, leading to low power consumption [71].

On the primary side of the link (Fig. 2.6), a free running oscillator generates the carrier. The coupled resonators may be seen in Fig. 2.6 to tune the oscillator. This will be discussed in more details in later sections. The link also includes non-coherent receivers on both sides. Each receiver comprises an analog front-end (AFE) for demodulating the received waveform, and a clock and data recovery (CDR) loop for synchronous data decision.

In the downlink from the external unit to the implant, binary data modulates the carrier's amplitude between two levels (Fig. 2.7(b)). In the reverse direction, uplink, the carrier is modulated with a data-driven switch that shorts the load on the implant (Fig. 2.7(c)). The modulated load is, then, transformed across the oscillator terminals and sets the oscillation at one of two amplitudes. Since the load modulation involves only the activation of a switch in the implant, the transmitter power consumption will be very low, and this fits the design goal for the implant.

[6] if we are to transmit data at $2 \sim 4$ Mbps by carrier modulation, we need a carrier frequency of greater than 10 MHz. In our design $f_0 \approx 35$ MHz.

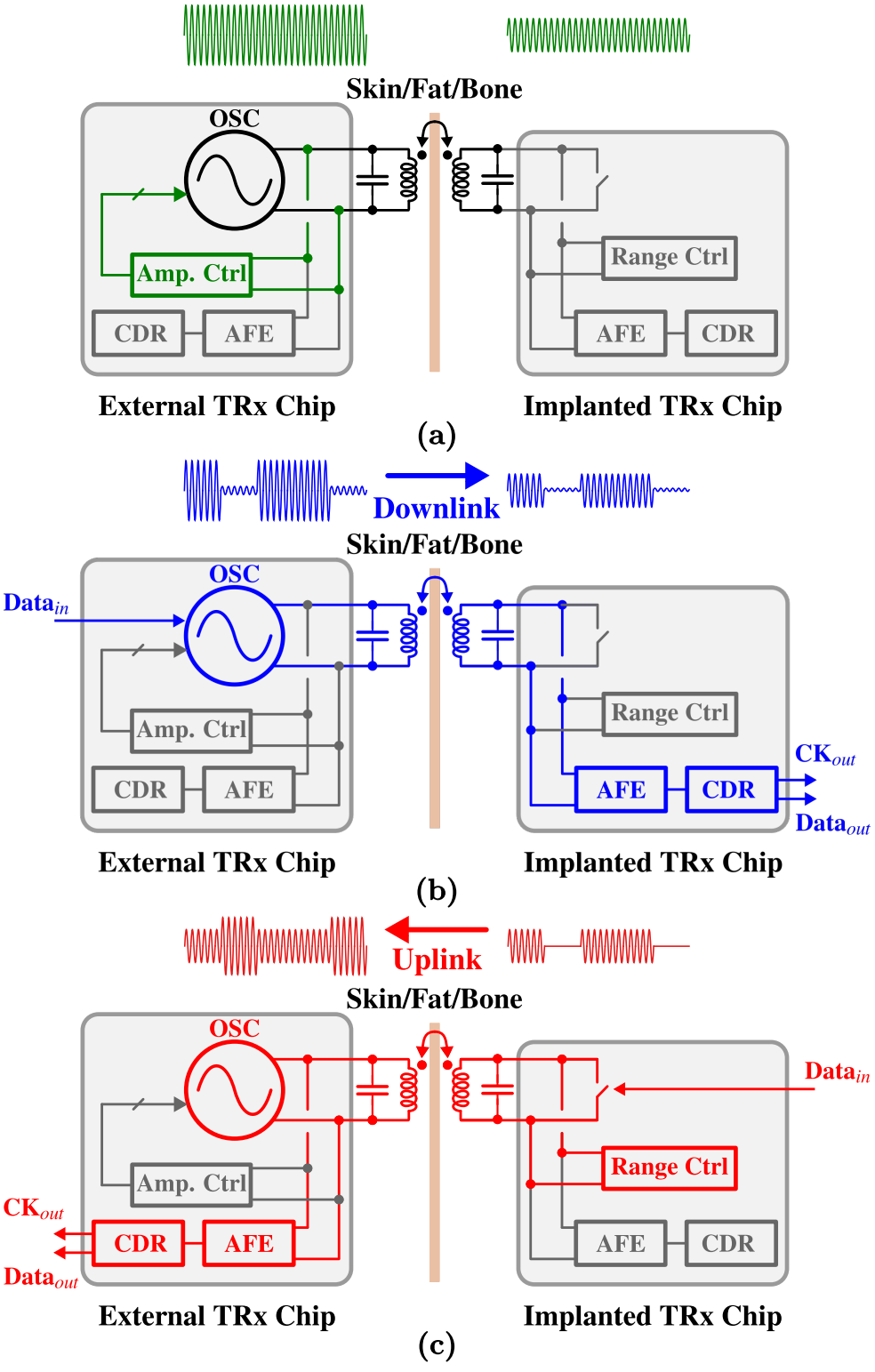


Figure 2.7: Different modes of operation in the data link: (a) power-up, (b) downlink, (c) uplink.

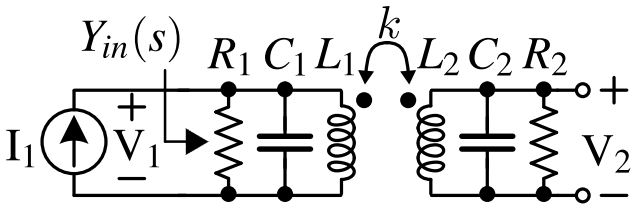


Figure 2.8: Inductively-coupled resonators.

The link also includes an amplitude control loop (Amp. Ctrl) and a range control unit (Range Ctrl) on primary and secondary sides, respectively. On the primary side, the amplitude control loop adjusts the carrier amplitude at the link power-up (Fig. 2.7(a)). This loop is deactivated during normal operation. The range control unit on the secondary side controls the quality factor of the secondary resonator (Q_2).

2.4 Data Link Theoretical Analysis

2.4.1 Inductive Link Analysis: Network Functions

To understand how the coupled resonators tune the oscillator, the circuit properties of two coupled resonators are first studied (Fig 2.8). Although several analyses on coupled resonators have been published in literature [40, 72, 73, 74, 75, 76], here, we present an insightful analysis that can help us specifically in design of the data link.

To analyze the inductive link and derive the transfer and driving-point functions (i.e. $H_{21}(s) = V_2/I_1$ and $Y_{in}(s) = I_1/V_1$), the dissection theorem (DT) [77, 78, 79] is used which helps us obtain low-entropy expressions for the network functions.

To employ the dissection theorem, as shown in Fig. 2.9, the coupling between the two resonators (i.e. mutual inductance) is modeled with a set of dependent voltage sources (i.e. sMI_{L_1} and sMI_{L_2}). Fig. 2.9 also shows how the test voltage source, V_Z, is introduced to the circuit to apply the theorem. From the dissection theorem, $H_{21}(s)$ is given by:

$$H_{21}(s) = \frac{V_2}{I_1} = H_{21}^{V_y} \times \frac{1 + \frac{1}{T_n}}{1 + \frac{1}{T}} \tag{2.1}$$

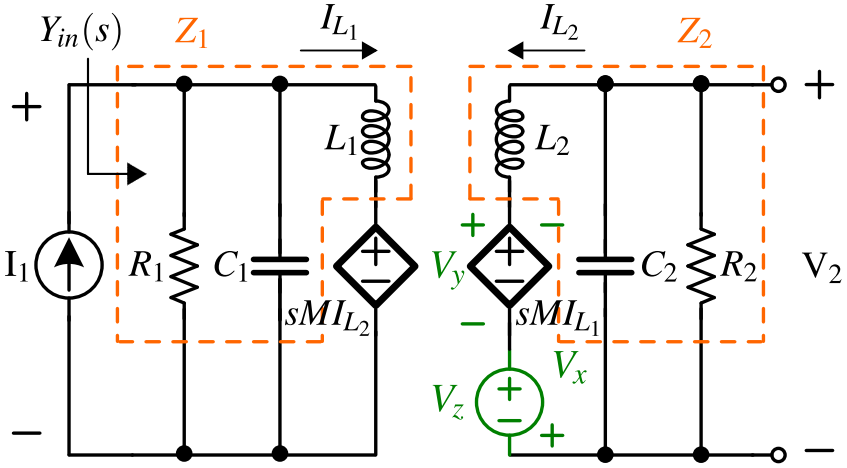


Figure 2.9: Modeling the mutual inductance with a set of dependent voltage sources in order to apply the DT.

with:

$$H_{21}^{V_y} = \frac{V_2}{I_1}\bigg|_{V_y=0} = -\frac{\left(R_1||\frac{1}{sC_1}\right)\left(R_2||\frac{1}{sC_2}\right)}{sM} = -\frac{Z_1' \,.\, Z_2'}{sM} \tag{2.2}$$

$$T_n = \frac{V_y}{V_x}\bigg|_{V_2=0} = \frac{sMI_1}{0} \to \infty \tag{2.3}$$

$$T = \frac{V_y}{V_x}\bigg|_{I_1=0} = -\frac{(sM)^2}{\left(R_1||\frac{1}{sC_1} + sL_1\right)\left(R_2||\frac{1}{sC_2} + sL_2\right)} = -\frac{(sM)^2}{Z_1.Z_2}\,. \tag{2.4}$$

Substituting (2.2), (2.3), (2.4) in (2.1), we have:

$$H_{21}(s) = \frac{Z_1'.Z_2'.(sM)}{Z_1.Z_2 - (sM)^2} \tag{2.5}$$

where $M \triangleq k\sqrt{L_1L_2}$ is the mutual inductance and Z_1', Z_2', Z_1 and Z_2 are defined as follows:

$$Z_1' = R_1||\frac{1}{sC_1} \tag{2.6}$$

$$Z_2' = R_2||\frac{1}{sC_2} \tag{2.7}$$

$$Z_1 = Z_1' + sL_1 \tag{2.8}$$

$$Z_2 = Z_2' + sL_2\,. \tag{2.9}$$

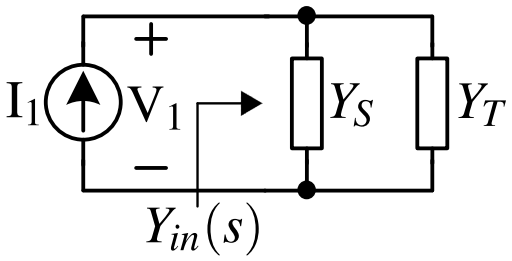


Figure 2.10: The input admittance, Y_{in}, can be considered as a parallel combination of two admittances of Y_S and Y_T.

Input admittance ($Y_{in}(s) = I_1/V_1$) of the inductive link is another network function of interest. Employing the input/output impedance/admittance theorem, which can be derived from the dissection theorem, the input admittance is given by:

$$Y_{in}(s) = \frac{I_1}{V_1} = Y_{in}\Big|_{T=0} \times \frac{1+T}{1+T'} \tag{2.10}$$

where:

$$Y_{in}\Big|_{T=0} = \frac{I_1}{V_1}\Big|_{T=0} = G_1 + sC_1 + \frac{1}{sL_1} \tag{2.11}$$

$$T' = \frac{V_y}{V_x}\Big|_{V_1=0} = -\frac{(sM)^2}{(sL_1).Z_2} \tag{2.12}$$

$$T = \frac{V_y}{V_x}\Big|_{I_1=0} = -\frac{(sM)^2}{Z_1.Z_2}\,. \tag{2.13}$$

If we substitute (2.11), (2.12) and (2.13) in (2.10), we obtain:

$$Y_{in}(s) = \frac{1}{Z_1'}.\frac{Z_1.Z_2 - (sM)^2}{(sL_1).Z_2 - (sM)^2}. \tag{2.14}$$

By using (2.6), (2.8) and (2.9), (2.14) can be simplified to a low entropy expression (Fig. 2.10):

$$Y_{in}(s) = Y_S(s) + Y_T(s) \tag{2.15}$$

where Y_S and Y_T are defiend as:

$$Y_S(s) = G_1 + sC_1 + \frac{1}{sL_1} \tag{2.16}$$

$$Y_T(s) = k^2\frac{L_2}{L_1} \times \frac{G_2 + sC_2}{1 + (1-k^2)sL_2(G_2 + sC_2)}. \tag{2.17}$$

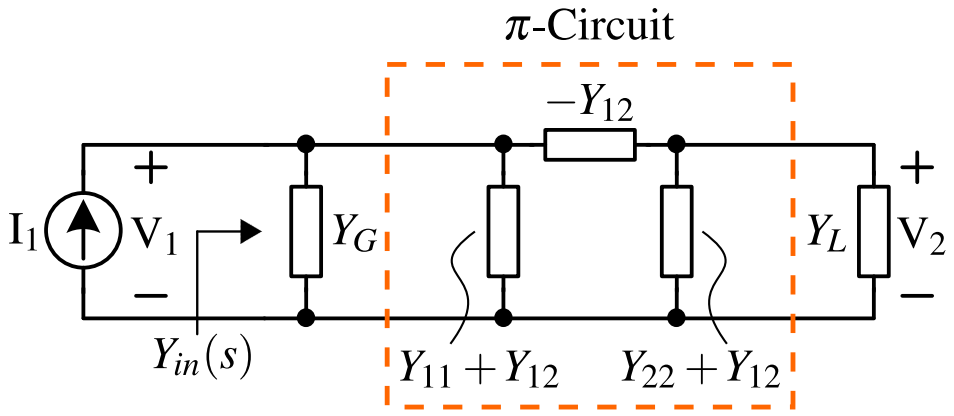


Figure 2.11: The coupled inductors in the link may be modeled as a two-port network represented by a short-circuit admittance matrix.

From (2.15), Y_{in} can be considered as a parallel combination of two equivalent admittances, Y_S and Y_T, where the source admittance, Y_S, is the parallel combination of R_1, C_1 and L_1, and Y_T is the transformed (reflected) admittance from the secondary side to the primary (Fig. 2.10). When the two resonators are uncoupled ($k = 0$), Y_T becomes zero and therefore $Y_{in} = Y_S$. This matches also with the intuition because by having no coupling from the secondary side of the link, the remaining circuit that may have effect on the input admittance will be the source admittance, Y_S.

2.4.2 A Second Approach for Inductive Link Analysis

The link can also be analyzed by modeling the coupled inductors as a two-port network which can be represented by a short-circuit admittance matrix, $\mathbf{Y}$ [68, 80, 81]:

$$\mathbf{Y} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{2.18}$$

Fig. 2.11 shows the π-circuit model of the reciprocal inductive link based on the short-circuit admittance parameters [81, Sec. 11-2]. Y_{11} and Y_{22}, the short-circuit driving-point admittances, are given by:

$$Y_{11}(s) = \frac{L_2}{s\Delta} \tag{2.19}$$

$$Y_{22}(s) = \frac{L_1}{s\Delta} \tag{2.20}$$

where $\Delta = det(\mathbf{L}) = L_1L_2 - M^2$ is the determinant of the 2×2 inductance matrix, $\mathbf{L}$:

$$\mathbf{L} = \begin{bmatrix} L_1 & M \\ M & L_2 \end{bmatrix} \tag{2.21}$$

The short-circuit transfer admittance, Y_{12} (= Y_{21}, due to the circuit's reciprocity), is given by:

$$Y_{12}(s) = Y_{21}(s) = -\frac{M}{s\Delta}. \tag{2.22}$$

In the circuit shown in Fig. 2.11, Y_G and Y_L are the generator and the load admittances and are defined as follows:

$$Y_G(s) = G_1 + sC_1 \tag{2.23}$$

$$Y_L(s) = G_2 + sC_2. \tag{2.24}$$

where $G_1 = 1/R_1$ and $G_2 = 1/R_2$ are the parallel conductances in the primary and secondary resonators, respectively (Fig. 2.8).

The total input admittance seen at the port V_1, Y_{in}, can be calculated as:

$$Y_{in}(s) = Y_G + Y_{11} - \frac{Y_{12}^2}{Y_L + Y_{22}}. \tag{2.25}$$

Substituting the admittance values in (2.25), we can write:

$$Y_{in}(s) = (G_1 + sC_1) + \frac{L_2}{s\Delta} - \frac{\dfrac{M^2}{(s\Delta)^2}}{(G_2 + sC_2) + \dfrac{L_1}{s\Delta}}. \tag{2.26}$$

Simplifying (2.26) to achieve a low-entropy expression for $Y_{in}(s)$, we obtain:

$$Y_{in}(s) = (G_1 + sC_1 + \frac{1}{sL_1}) + \big(k^2\frac{L_2}{L_1} \times \frac{G_2 + sC_2}{1 + (1-k^2)sL_2(G_2 + sC_2)}\big) \tag{2.27}$$

which is the same equation as (2.15), derived in previous section using the dissection theorem.

2.4.3 Resonance Frequencies and Critical Coupling Factor

In order to find the resonance frequencies of the circuit, the imaginary part of the total input admittance, $B_{in} = \mathrm{Im}[Y_{in}(s)]$, has to be derived and equated to zero. Substituting s with

$j\omega$, the input admittance $Y_{in}(j\omega)$ is given by:

$$\begin{aligned} Y_{in}(j\omega) =& Y_S(j\omega) + Y_T(j\omega) \\ =& G_1\Big(1 + jQ_1\big(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\big)\Big) \\ &+ k^2 G_1 Q_1\big(\frac{\omega_0}{j\omega}\big) \times \frac{\big(\frac{j\omega}{\omega_0 Q_2}\big)\Big(1 + Q_2\big(\frac{j\omega}{\omega_0}\big)\Big)}{1 + (1-k^2)\big(\frac{j\omega}{\omega_0 Q_2}\big)\Big(1 + Q_2\big(\frac{j\omega}{\omega_0}\big)\Big)} \end{aligned} \tag{2.28}$$

where $G_1 = 1/R_1$ is the parallel conductance in the primary resonator, $\omega_0 = 1/\sqrt{LC} = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$ is the resonance frequency of the uncoupled resonators, and $Q_1 = R_1/\omega_0 L_1$ and $Q_2 = R_2/\omega_0 L_2$ are the uncoupled quality factors of primary and secondary resonators, respectively.

The input admittance can be decomposed into its real and imaginary parts:

$$Y_{in}(j\omega) = \mathrm{Re}[Y_{in}(j\omega)] + j\mathrm{Im}[Y_{in}(j\omega)] = G_{in}(j\omega) + jB_{in}(j\omega) \tag{2.29}$$

with:

$$G_{in} = G_1 + \frac{L_2}{L_1}\frac{k^2 G_2}{\Big(1 - (1-k^2)\big(\frac{\omega}{\omega_0}\big)^2\Big)^2 + (1-k^2)\big(\frac{\omega}{\omega_0 Q_2}\big)^2} \tag{2.30}$$

$$\begin{aligned} B_{in} =& G_1 Q_1\big(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\big) \\ &+ k^2 G_1 Q_1\big(\frac{\omega}{\omega_0}\big) \times \frac{\big(1 - \frac{1-k^2}{Q_2^2}\big) + (1-k^2)\big(\frac{j\omega}{\omega_0}\big)^2}{1 + (1-k^2)\big(2 - \frac{1-k^2}{Q_2^2}\big)\big(\frac{j\omega}{\omega_0}\big)^2 + (1-k^2)^2\big(\frac{j\omega}{\omega_0}\big)^4} \end{aligned} \tag{2.31}$$

B_{in} can be simplified further as follows:

$$\begin{aligned} B_{in} =& -G_1 Q_1 \frac{1 + (1-k^2)\big(\frac{j\omega}{\omega_0}\big)^2}{\big(\frac{\omega}{\omega_0}\big)} \\ &\times \frac{1 + \big(2 - \frac{1-k^2}{Q_2^2}\big)\big(\frac{j\omega}{\omega_0}\big)^2 + (1-k^2)\big(\frac{j\omega}{\omega_0}\big)^4}{\Big(1 + (1-k^2)\big(\frac{j\omega}{\omega_0}\big)^2\Big)^2 - \frac{(1-k^2)^2}{Q_2^2}\big(\frac{j\omega}{\omega_0}\big)^2} \end{aligned} \tag{2.32}$$

As seen from (2.32), the equation $B_{in} = 0$ has up to three pairs of real solutions (numerator sixth-order polynomial in ω):

$$\omega_1 = \pm\frac{\omega_0}{\sqrt{1-k^2}} \tag{2.33}$$

$$\omega_2 \text{ or } \omega_3 = \pm\omega_0 \sqrt{\frac{1 \pm \sqrt{1 - \frac{1-k^2}{\left(1-\frac{1-k^2}{2Q_2^2}\right)^2}}}{\frac{1-k^2}{1-\frac{1-k^2}{2Q_2^2}}}} \tag{2.34}$$

From (2.33), it can be concluded that, as the coils come into closer proximity and k increases, ω_1 increases as well; however, for typical values of k (e.g. $k < 0.33$), we can assume $k^2 \ll 1$ and therefore:

$$\omega_1 \approx \pm\omega_0 = \pm\frac{1}{\sqrt{LC}} \tag{2.35}$$

To convert $\omega_{2,3}$ into a lower-entropy expression, (2.34) can be simplified by expanding the term $\sqrt{1-(1-k^2)/(1-(1-k^2)/2Q_2^2)^2}$ about $Q_2 = \infty$ (since $Q \gg 1$ for the coil we use):

$$\begin{aligned} \omega_2 \text{ or } \omega_3 &= \pm\frac{\omega_0}{\sqrt{1\pm k}} \times D_1 \\ &= \pm\frac{\omega_0}{\sqrt{1\pm k}} \times \sqrt{\left(1-\frac{1-k^2}{2Q_2^2}\right)} \\ &\quad \times \sqrt{1 \pm \frac{(1\pm k)(1-k^2)}{2kQ_2^2} \pm \frac{(1\pm k)(1-k^2)^2(1+2k^2)}{8k^3Q_2^4} \mp \cdots} \end{aligned} \tag{2.36}$$

In (2.36) the discrepancy factor, D_1, approaches 1 and can be neglected, if Q_2 is high enough (equivalently, $k \gg k_C$). In this case, $\omega_{2,3}$ is given by:

$$\omega_2 \text{ or } \omega_3 = \pm\frac{\omega_0}{\sqrt{1\pm k}} \tag{2.37}$$

For some values of k, $\omega_{2,3}$ may not be real values. In this case, the equation $jB_{in} = 0$ has only one pair of real solutions at ω_1 (i.e. no splitting resonance frequencies). To have real

$\omega_{2,3}$ (i.e. to have split in frequencies), the expression in the numerator (2.34) must remain greater than zero[7]; i.e.

$$\Big(1-\frac{1-k^2}{2Q_2^2}\Big)^2-(1-k^2)>0 \tag{2.38}$$

Equation (2.38) holds if k is greater than a critical coupling factor, k_C, (i.e $k>k_C$). To find k_C, equation (2.38) can be rewritten as a quadratic in $X=(1-k^2)$ as the variable:

$$X^2-4Q_2^2(1+Q_2^2)X+4Q_2^4>0 \tag{2.39}$$

Solving (2.39) for $X=(1-k^2)$, k_C could be calculated as (at $k=k_C$, the quadratic equation in (2.39) approaches zero):

$$k_C=\sqrt{1-2Q_2^2-2Q_2^4\Big(1-\sqrt{1+\frac{2}{Q_2^2}}\Big)} \tag{2.40}$$

Expanding about $Q_2=\infty$ using Taylor series gives:

$$\begin{aligned} k_C=&\frac{1}{Q_2}\times D_2 \\ =&\frac{1}{Q_2}\times\sqrt{1-\frac{5}{4Q_2^2}+\frac{7}{4Q_2^4}-\frac{21}{8Q_2^6}+\cdots} \end{aligned} \tag{2.41}$$

For large values of Q_2, k_C will be:

$$k_C\approx\frac{1}{Q_2} \tag{2.42}$$

However for smaller Q_2[8], the higher order terms in the discrepancy factor, D_2, will become significant and make k_C smaller than $1/Q_2$.

To better understand how the resonance frequencies behave as the coupling factor, k, changes, the input admittance across the input terminals, Y_{in}, should be plotted. Fig. 2.12 shows the admittance plot in the complex plane, (Re$[Y_{in}(j\omega)]$, Im$[Y_{in}(j\omega)]$), where frequency,

[7]This condition comes from the numerator of the second fractional term in (2.32) : $1+\big(2-\frac{1-k^2}{Q_2^2}\big)\big(\frac{j\omega}{\omega_0}\big)^2+(1-k^2)\big(\frac{j\omega}{\omega_0}\big)^4$.

[8]By inspection of (2.41), this would become important if $Q_2\lesssim 2$ – a very low quality factor.

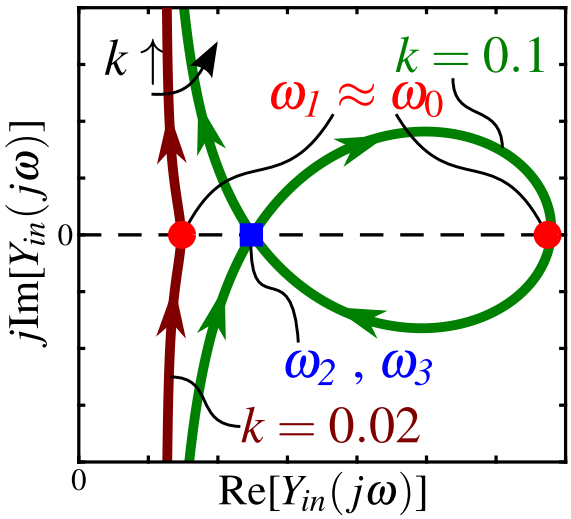


Figure 2.12: Total input admittance plot in a complex plain, where frequency ω is a parameter.

ω, is a parameter. Resonance frequencies are, by definition, where the admittance curves intersect the real axis:

$$\mathrm{Im}[Y_{in}(j\omega)] = 0 \tag{2.43}$$

As can be seen in Fig. 2.12, once coupled, the system of two resonators can have up to three resonance frequencies as a function of coupling factor, k. When the coils are far apart (e.g. $k = 0.02$), there is just one intersection with real axis, in other words, one resonance frequency (i.e. ω_1). When the coils are close together (e.g. $k = 0.1$), three resonances can appear (i.e. ω_1, ω_2 and ω_3).

This can be seen better in the input impedance magnitude, $|Z_{in}(j\omega)|$ $(= 1/|Y_{in}(j\omega)|)$, plotted versus frequency (Fig. 2.13). When the coils are far apart (e.g. $k = 0.02$), the impedance function resonates at one frequency, $\omega_1 = \omega_0/\sqrt{1-k^2}$. In this expression, k appears as the square and as mentioned before, since k is typically much lower than 1 the resonance frequency is very close ω_0.

However, as the coils come into closer proximity (e.g. $k \to 0.1$), the impedance peak bifurcates into two peaks separated by a trough; therefore, the impedance function can have three resonance frequencies: one close to ω_0 (the trough, at ω_1), and two split frequencies of $\omega_2, \omega_3 \approx \omega_0/\sqrt{1 \pm k}$. Since, in the denominator, k appears in first-order, the two resonance frequencies bifurcate as k increases. The bifurcation occurs at the critical coupling factor,

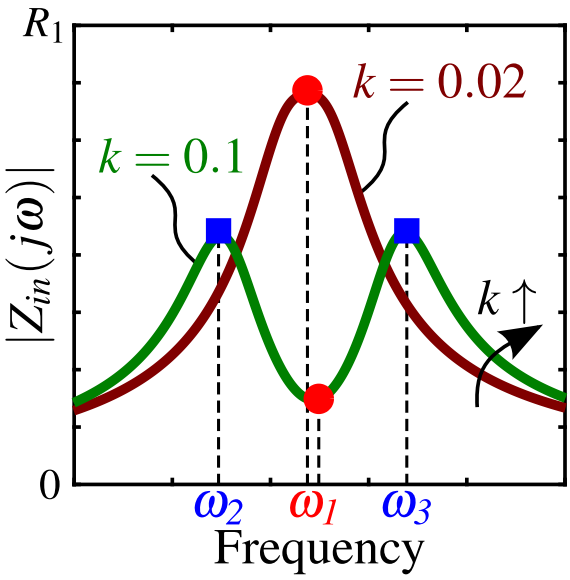


Figure 2.13: Total input impedance plotted versus frequency for two different values of coupling factor.

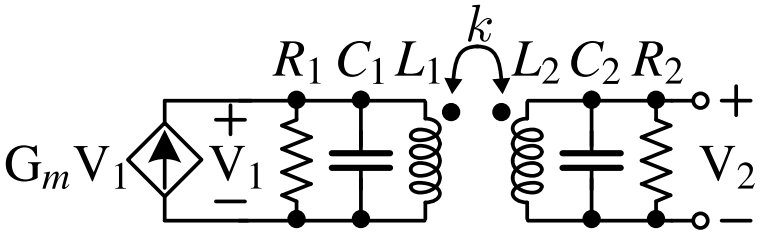


Figure 2.14: Building an oscillator with the coupled resonators.

k_C, which was shown in (2.42) to be roughly equal to $1/Q_2$, where Q_2 is the uncoupled quality factor of the secondary resonator.

2.5 Operation: Building An Oscillator

An oscillation can develop when a negative conductance, $-G_m$, is connected across the resonator's primary terminals (Fig. 2.14) [41, 82, 83, 84, 85]. The circuit can oscillate at one of the peak frequencies (Fig. 2.13): if $k < k_C$, it will oscillate at ω_1, and if $k > k_C$, the oscillation appears at either ω_2 or ω_3[9].

[9]The oscillation does not appear at ω_1 when $k > k_C$ because, as a property of the dynamical system, it is an unstable oscillation frequency [86].

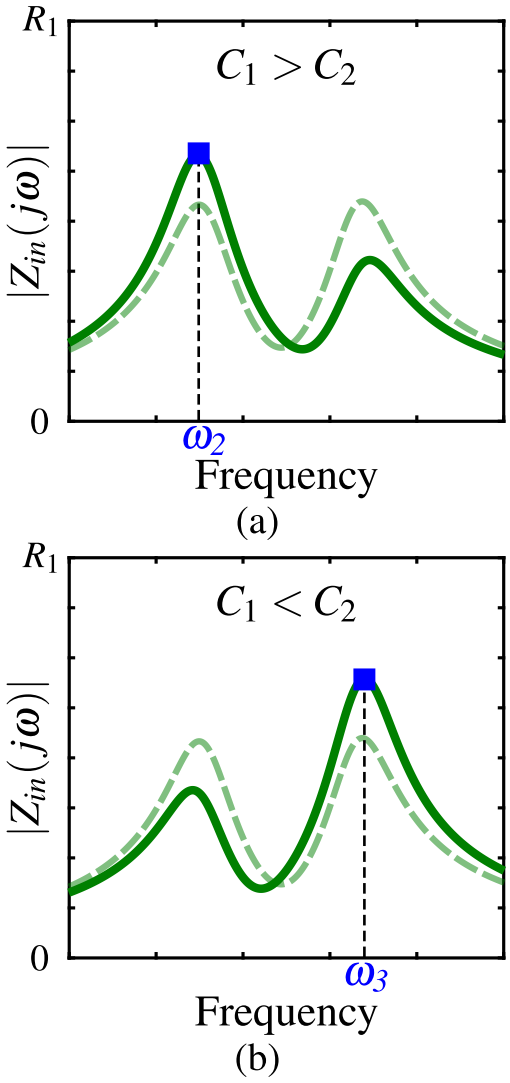


Figure 2.15: Stable oscillation frequencies when $k > k_C$: (a) at ω_2 when $C_1 > C_2$ (b) at ω_3 when $C_1 < C_2$.

In practice, the capacitors or the inductors on the two sides of the inductive link, C_1 and C_2 or L_1 and L_2, will be unequal [73]. This selects the oscillation frequency. For instance, as shown in Fig. 2.15, if $C_1 > C_2$, the two peaks in the impedance magnitude will be misaligned, and oscillation takes place at the frequency of the higher peak, ω_2.

This happens because, by presenting an impedance with two unequal peaks to the oscillator terminals, the loop gain in the oscillator is larger at the frequency of the higher peak. Thus, during the oscillation start-up, the envelope of oscillation at the frequency of the higher peak rises more rapidly than that of the lower peak. This faster growth then

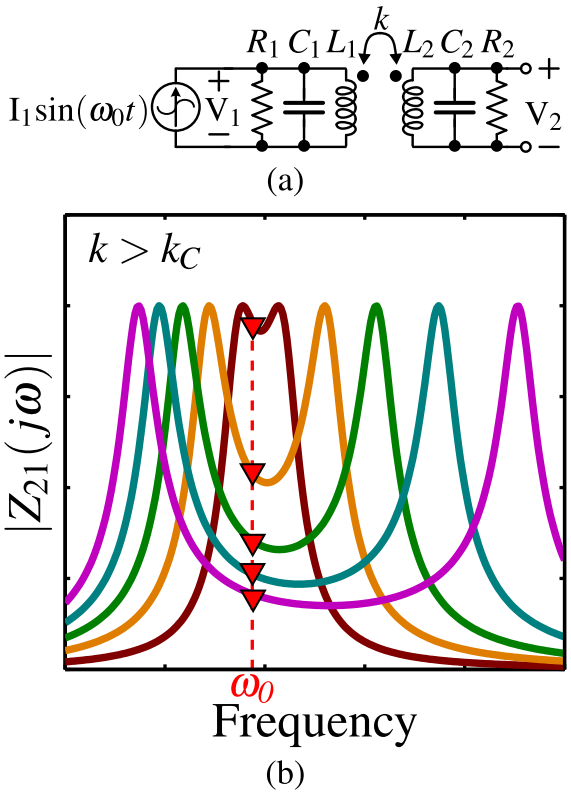


Figure 2.16: Downlink distance immunity, (a) Modulation at a fixed frequency (e.g. ω_0), (b) Transimpedance magnitude drops as the coils separation changes.

drives the non-linear devices into saturation, causing the loop gains at both frequencies drop significantly; and thereby, the oscillation at the frequency of the lower peak is squelched [87]. During the oscillator design, by deliberately choosing a slightly larger C_1, the oscillation frequency is defined to be ω_2 when $k > k_C$.

2.6 Fundamental Limits to Range

2.6.1 Downlink

To study the downlink's dependence on distance, the transimpedance, $H_{21}(s) = Z_{21}(s) = V_2/I_1$, is investigated (Fig. 2.16(a)) [40]. Links reported in the literature are mostly driven by an oscillator at a fixed frequency (e.g. ω_0). As the coils move into greater proximity and as the frequency remains constant, the transimpedance magnitude, and therefore V_2 drop

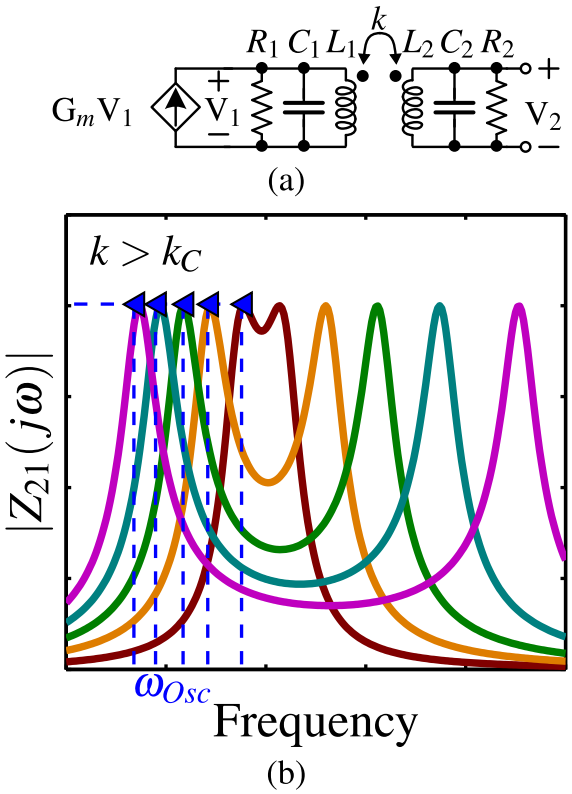


Figure 2.17: Downlink distance immunity, (a) Modulation with an oscillator (i.e. at ω_{Osc}) , (b) Transimpedance magnitude remains unchanged as the coils come close together.

significantly as shown in Fig. 2.16(b). It may run contrary to intuition that the response is weaker as the coils come together, but it is very much the case [40, 71, 88, 89].

This is in contrast to a free running oscillator which always tunes itself to the frequency of the peaks (Fig. 2.17(a)). As shown in Fig. 2.17(b), whereas the oscillation frequency changes with coil proximity, the load voltage remains constant. At the frequencies of the peaks, the circuit can be modeled as an ideal transformer whose turns ratio is independent of distance and only depends on the self-inductances of the two coils, $\sqrt{L_1} : \sqrt{L_2}$ (Fig. 2.18). This makes it obvious why the load voltage remains stable as distance changes:

$$\mathrm{V}_2 = \sqrt{\frac{L_2}{L_1}}\,\mathrm{V}_1 \tag{2.44}$$

Equation (2.44) will be proven by an intuitive analysis in Section 2.7.

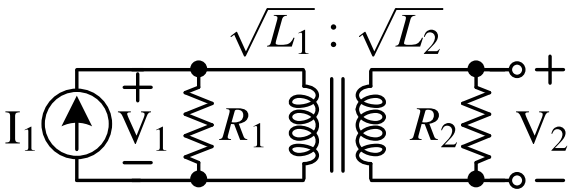


Figure 2.18: The link can be modeled as an ideal transformer.

2.6.2 Uplink

In the uplink direction, when the switch is open, the resistance at the secondary is by design a large $R_{2,off}$ (Fig. 2.19(a)). When the switch is closed, the resistance drops to $R_{2,on}$, which if the switch is ideal is zero Ohm. This switching action (changing between $R_{2,off}$ and $R_{2,on}$) transforms into a change in the impedance appearing across the oscillator (Z_{in}). Fig. 2.19(b) shows the modulation index, which is the difference between the two values of $|Z_{in}|$, when the switch is open and when it is closed, at a particular distance (in effect, k [90, 91]). Therefore, if the carrier frequency remains constant (e.g. $\omega = \omega_0$), modulation index shrinks with distance (rising k). As can be seen, the modulation index may even go to zero as the two resonators are at a certain short distance.

This violates intuition, yet with a simple mathematical analysis, it can be shown that it is correct. Using equation (2.27), the total input admittance at the uncoupled resonance frequency, ω_0, can be calculated as:

$$\begin{aligned} Y_{in}(j\omega_0) =& (G_1 + j\omega_0 C_1 + \frac{1}{j\omega_0 L_1}) \\ &+ \Big(k^2 \times \frac{j\omega_0 L_2(G_2 + j\omega_0 C_2)}{j\omega_0 L_1(1 + j\omega_0 L_2(G_2 + j\omega_0 C_2)(1-k^2))}\Big) \end{aligned} \tag{2.45}$$

Knowing that $Q_2 = 1/(\omega_0 L_2 G_2)$ and $\omega_0 = 1/\sqrt{LC} = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$, (2.45) simplifies to:

$$Y_{in}(j\omega_0) = G_1 + k^2 \times \frac{\frac{j}{Q_2} - 1}{j\omega_0 L_1(1 + (\frac{j}{Q_2} - 1)(1-k^2))} \tag{2.46}$$

When modulating the load resistance, R_2, the quality factor Q_2 also changes significantly between two values: when $R_2 = R_{2,off}$, Q_2 can have a large value ($Q_2 \gg 1$), and when

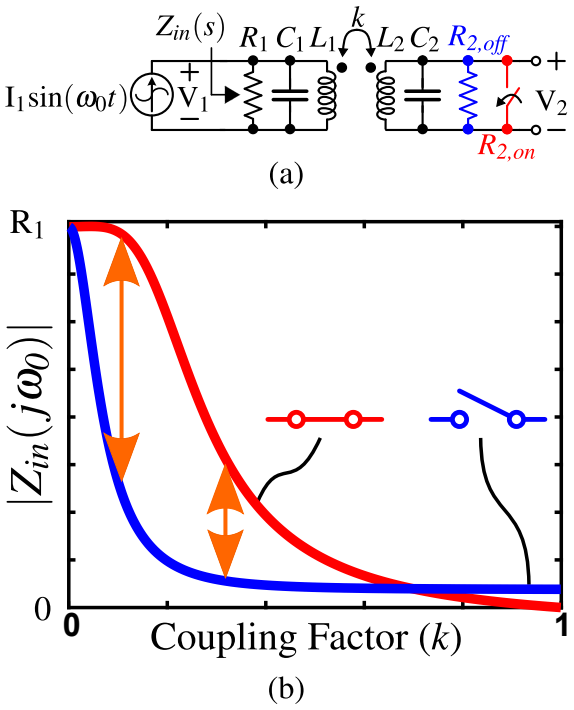


Figure 2.19: Uplink distance immunity, (a) Modulation at a fixed frequency (e.g. ω_0), (b) Modulation index shrinks as the coils separation changes.

$R_2 = R_{2,on}$, Q_2 is close to zero ($Q_2 \to 0$). Plugging these two extremes in (2.46), we have:

$$Y_{in}(j\omega_0)\Big|_{R_2=R_{2,off}} \approx G_1 - \frac{1}{j\omega_0 L_1} \tag{2.47}$$

$$Y_{in}(j\omega_0)\Big|_{R_2=R_{2,on}} \approx G_1 + \frac{k^2}{1-k^2} \times \frac{1}{j\omega_0 L_1} \tag{2.48}$$

As shown in Fig. 2.19(b), the modulation index can become zero when:

$$\Delta Z_{in} = \Big|Z_{in}(j\omega_0)\Big|_{R_2=R_{2,off}} - \Big|Z_{in}(j\omega_0)\Big|_{R_2=R_{2,on}} = 0 \tag{2.49}$$

or, in other words, since $Z_{in}(j\omega_0) = 1/Y_{in}(j\omega_0)$, we can say:

$$\Big|Y_{in}(j\omega_0)\Big|_{R_2=R_{2,off}} = \Big|Y_{in}(j\omega_0)\Big|_{R_2=R_{2,on}} \tag{2.50}$$

Applying this condition to (2.47) and (2.48) and solving for k, it is revealed that when operating at a fixed frequency (in this example ω_0) the modulation index will pinch off ($\Delta Z_{in} = 0$) always at about $k = \sqrt{2}/2 \approx 0.707$.

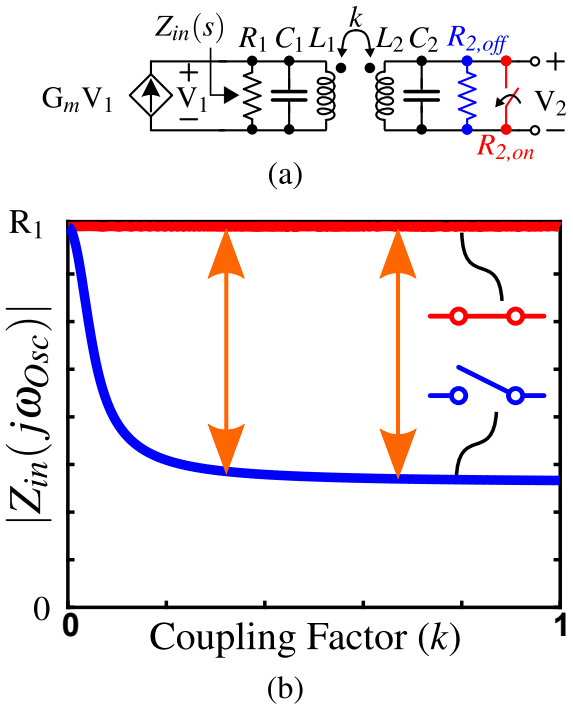


Figure 2.20: Uplink distance immunity, (a) Modulation with an oscillator (i.e. at ω_{Osc}) , (b) Large modulation index is preserved.

However, with a free running oscillator (Fig. 2.20(a)), a large modulation index is ideally preserved over a good range, as shown in Fig. 2.20(b). In data reception this modulation index defines eye opening; thus the larger the modulation index, the lower the error rate. All previous realizations using load keying (LSK) employ constant frequency, and hence suffer from this change in the modulation index [71, 76].

To develop a deeper understanding, it would be insightful to also analyze the inductive link and derive the governing equations for the input impedance curves. In Fig. 2.20(b), these curves are numerically plotted by using the appropriate oscillation frequency in (2.27) i.e. ω_1 for $k < k_C$ and $\omega_{2,3}$ for $k > k_C$ ($|Z_{in}| = 1/|Y_{in}|$). However, now, we want to use an asymptotic analysis so as to simplify the problem and achieve low-entropy expressions.

Assuming $R_2 = R_{2,off}$ ($Q_2 \gg 1$), then after frequency bifurcation ($k > k_C$), the oscillation occurs either at ω_2 or ω_3. But, when $k < k_c$, the circuit oscillates at ω_1. Therefore, the input admittance for the regions below and above k_C should be calculated at the respective frequencies of operation. Since at any resonance frequency of the circuit, the input

admittance must be real, we can write:

$$Y_{in}(j\omega_{Osc}) = G_{in}(j\omega_{Osc}) + jB_{in}(j\omega_{Osc}) \overset{B=0}{=} G_{in}(j\omega_{Osc}) \tag{2.51}$$

Assuming $k \gg k_C$ (asymptotic analysis), the input admittance can be calculated by putting (2.37) in (2.30), which can be written, after simplification ($Q_2 \gg 1$), as follows:

$$G_{in}(j\omega_{Osc}) = G_1 + \frac{L_2}{L_1}G_2 \tag{2.52}$$

Therefore, G_{in} in this region is independent of coupling factor, k. That is, for coil separation below that which corresponds to k_C, the second term in (2.52), $(L_2/L_1)G_2$, implies that the inductive link can be modeled as an ideal transformer whose turns ratio is $\sqrt{L_1} : \sqrt{L_2}$ (Fig. 2.18).

Equation (2.52) can also be written in terms of Q_1 and Q_2 as follows:

$$G_{in}(j\omega_{Osc}) = G_1\big(1 + \frac{Q_1}{Q_2}\big) \tag{2.53}$$

When $k < k_C$, (2.33) can be used to find the input admittance, $Y_{in}(j\omega_{Osc}) = G_{in}(j\omega_{Osc})$, which in this case is given by:

$$G_{in}(j\omega_{Osc}) = G_1 + \frac{L_2}{L_1}\big(\frac{k^2Q_2^2}{1-k^2}\big)G_2 \tag{2.54}$$

which implies that if we model the link as an ideal transformer, its turns ratio depends on k, that is, on coil separation:

$$\frac{N_2}{N_1} = \frac{kQ_2}{\sqrt{1-k^2}} \times \sqrt{\frac{L_2}{L_1}} \tag{2.55}$$

This is to be expected because as the coils are pulled further apart ($k \to 0$), the induced voltage at the load will gradually fade away to zero.

Equation (2.54), after further simplification, can also be written as follows:

$$G_{in}(j\omega_{Osc}) = G_1\big(1 + \frac{k^2}{1-k^2}Q_1Q_2\big) \tag{2.56}$$

which tends to G_1 as k approaches zero. Also, assuming that $k^2 \ll 1$, (2.56) can be considered as a quadratic function of k, since $Q_1Q_2 \gg 1$,

$$G_{in}(j\omega_{Osc}) \approx G_1(1 + k^2Q_1Q_2) \tag{2.57}$$

In conclusion, the input admittance magnitude, $|Y_{in}| = 1/|Z_{in}|$, when $R = R_{2,off}$, can be written as a piece-wise function:

$$\left|Y_{in}(j\omega_{Osc})\right|_{R=R_{2,off}} \approx \begin{cases} G_1(1+k^2Q_1Q_2), & \text{if } k < k_C \\ G_1\big(1+\dfrac{Q_1}{Q_2}\big), & \text{if } k > k_C \end{cases} \tag{2.58}$$

For the case where $R_2 = R_{2,on}$, by assuming $Q_2 \to 0$ in (2.28), the input admittance and the oscillation frequency can be derived:

$$Y_{in}(j\omega)\Big|_{R_2=R_{2,on}} = G_1\Big(1+jQ_1\big(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\big)\Big) + \frac{k^2G_1Q_1}{1-k^2}\big(\frac{\omega_0}{j\omega}\big) \tag{2.59}$$

The oscillation frequency can be calculated by equating the imaginary part of the input admittance, $B_{in} = \mathrm{Im}[Y_{in}]$, to zero:

$$B_{in}(j\omega)\Big|_{R_2=R_{2,on}} = G_1Q_1\big(\frac{\omega_0}{\omega}\big) \times \Big(\big(\frac{\omega^2}{\omega_0^2}-1\big) - \frac{k^2}{1-k^2}\Big) = 0 \tag{2.60}$$

Solving (2.60) for ω, the oscillation frequency, ω_{Osc}, is:

$$\omega_{Osc}\Big|_{R_2=R_{2,on}} = \omega_1 = \frac{\omega_0}{\sqrt{1-k^2}} \tag{2.61}$$

Under this condition, the input admittance is purely real as expected and equal to $G_1 = 1/R_1$ as shown in Fig. 2.20(b) (the curve for closed switch):

$$\left|Z_{in}(j\omega)\right|_{R_2=R_{2,on}} = R_1 = \frac{1}{G_1} \tag{2.62}$$

2.7 Intuitive Analysis of Data Link

A rigorous, mathematical analysis of the data link is presented in the previous sections but, as well, an intuitive insight of its operation will be very helpful during the link design. Since the link configuration in the downlink may be considered as a special case in uplink, when the switch is open, here, we only discuss the uplink (Fig. 2.21(a)).

In the case that the switch is closed (Fig. 2.21(b)), the load on secondary side falls to $R_{2,on}$. We will assume that $R_{2,on} \to 0$ so $R_{2,off}$ and C_2 can be neglected, as illustrated in

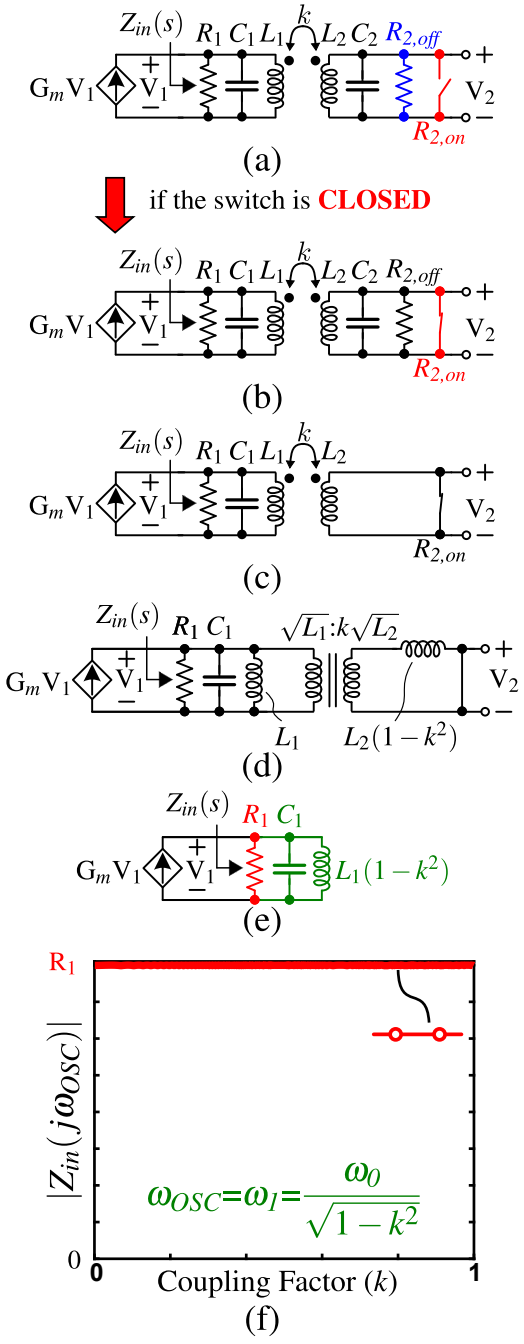


Figure 2.21: Intuitive analysis: When the switch is closed.

Fig. 2.21(c). To simplify the circuit, the coupled inductors are replaced with one equivalent circuit [92]. Many equivalent circuits exist for coupled inductors, and the one chosen in the circuit, shown in Fig. 2.21(d), is the one which is more convenient for analysis in this case. After transforming the inductor on the secondary to the primary, an RLC resonator remains (Fig. 2.21(e)), that in the presence of a negative resistance, oscillates at ω_1. With a clipping current source as the drive, the amplitude of oscillation, moreover, depends on the input impedance across the oscillator terminals. As Fig. 2.21(f) indicates, the input impedance at the oscillation frequency which is the LC resonant frequency, remains constant at R_1 over the range of k from 0 to 1. At the extreme $k = 0$, R_1 is the resistance of the primary side resonator alone.

When the switch is open, the resistance at the secondary is equal to $R_{2,off}$ (Fig. 2.22(b)). Similar to the previous case, to simplify the circuit further, the coupled inductors are replaced with an appropriate model. As illustrated in Fig 2.22(c), in this case, a different equivalent circuit [92] is deployed which is more convenient to work with here. Appendix A discusses the mathematical derivation of this equivalent circuit. At the oscillation frequency, the LC circuit consisting of C_2 and $L_2(1 \pm k)$ will resonate in parallel; the remaining components at the secondary are a resistance, $R_{2,off}$, and a reactance, $X_L = \pm j\omega_{Osc}L_2(1/k - k)$ (Fig 2.22(d)). $R_{2,off}$ will be greater than X_L, if $k > k_C$. Then the leakage reactance, X_L can be neglected[10] (Fig 2.22(e)) and $R_{2,off}$ can be transformed to the primary side. After simplifying the circuit, as shown in Fig 2.22(f), an RLC resonator is left which tells us about not only the frequency of oscillation, ω_2 or ω_3, but also that the input impedance remains constant and independent of k, as long as $k > k_C$ (Fig 2.22(g)). That is,

$$Z_{in}(j\omega_{Osc}) = R_1 || \frac{L_1}{L_2} R_2 \tag{2.63}$$

Fig. 2.22(e) also explains the distance immunity in the downlink. Indeed, the circuit shown in Fig. 2.22(e) is exactly the same as in Fig. 2.18. As can be seen, all the circuit parameters are independent of the coil distance and this justifies the constant load voltage, V_2, in the downlink, $V_2/V_1 = \sqrt{L_2/L_1}$.

[10]Here, we are actually analyzing the circuit asymptotically by assuming $k \gg k_C$.

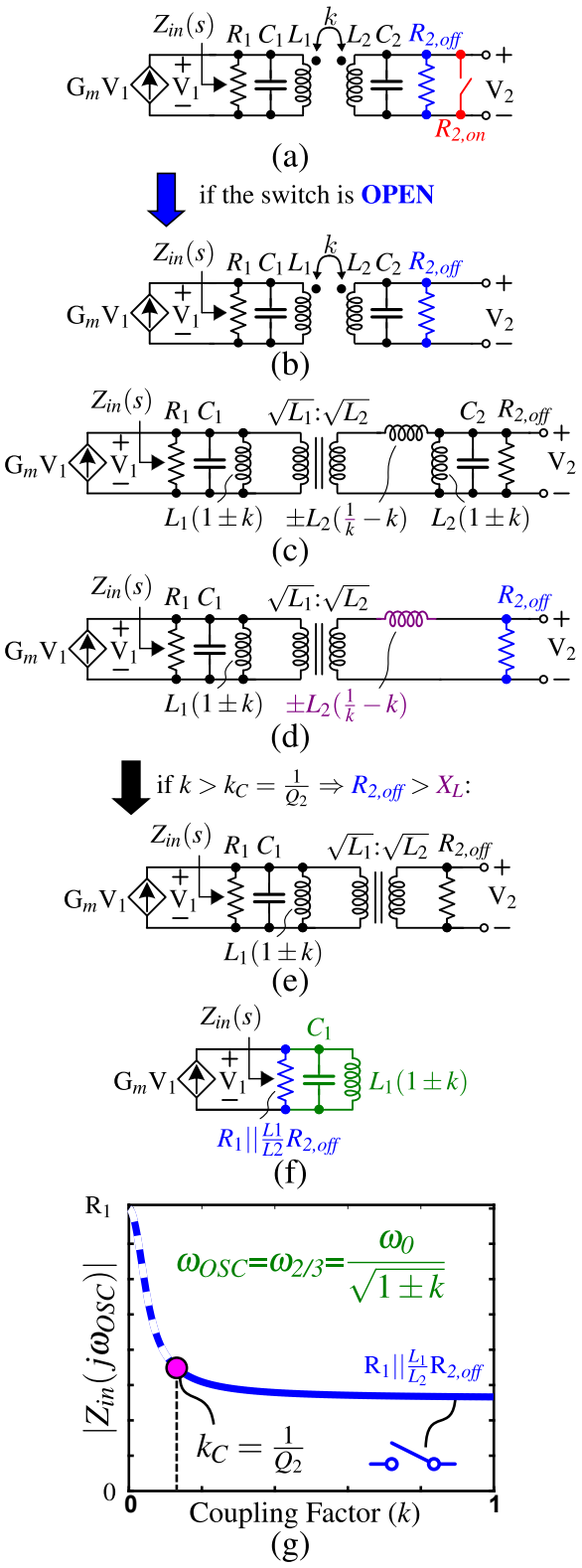


Figure 2.22: Intuitive analysis: When the switch is open and $k > k_C$.

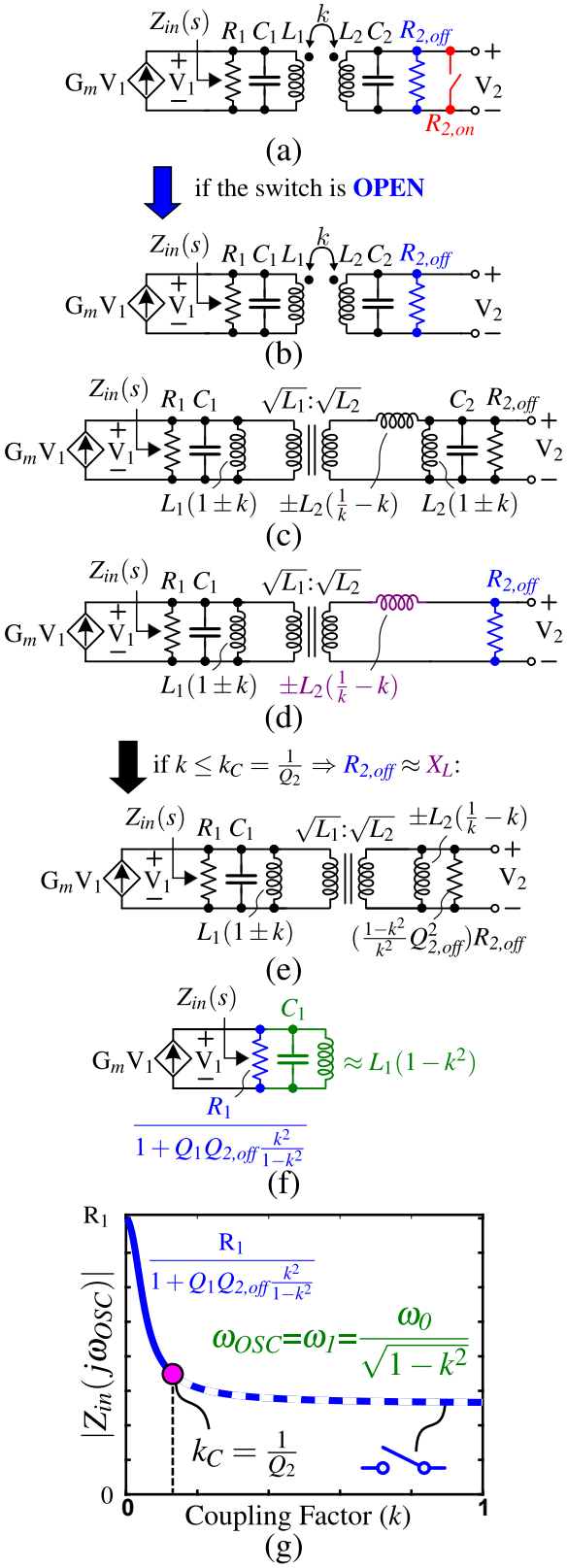


Figure 2.23: Intuitive analysis: When the switch is open and $k < k_C$.

When $k < k_C$, the assumption that $R_{2,off} > X_L$ must be revisited. Now, $R_{2,off}$ and X_L are comparable and therefore neither can be ignored. To simplify the circuit, the series RL circuit can be converted to its parallel equivalent, as illustrated in Fig. 2.23(e). Similar to the two previous cases, after simplifying the circuit, a parallel RLC resonator will remain, but it is different than the RLC circuit when $k > k_C$ (Fig. 2.23(f)). The oscillation now occurs at ω_1 and the input impedance, unlike the two previous cases, is a function of distance, k (Fig. 2.23(g)):

$$Z_{in}(j\omega_{Osc}) = \frac{R_1}{1 + \frac{k^2}{1-k^2} Q_1 Q_{2,off}} \tag{2.64}$$

It is obvious from (2.64) that as the coils move apart and k goes to zero, the input impedance becomes R_1. This is common sense because when k is equal to zero, the resonators are uncoupled and the input impedance will only be the resistance on the primary side, R_1.

It is worth noting that in the series-to-parallel RL conversion, illustrated in Fig. 2.23(e), when k is a very small value (i.e. $k \ll 1/Q_{2,off}$[11]), $j\omega L_2(1/k - k)$ ($\approx j\omega L_2/k$) is much larger in magnitude compared to $R_{2,off}$. This means the converted parallel RL in Fig. 2.23(e) can approximate the series RL circuit in Fig. 2.23(d) with a reasonable accuracy, because the RL circuit has a relatively high quality factor when $k \ll k_C$.

2.8 Practical Design Considerations : Non-zero On-Resistance

In practice, the on-resistance of an FET switch is non-zero (Fig. 2.24(a)), and this modifies the input impedance curve when the switch is closed. In our case, for a CMOS transmission gate with $(W/L) = 100\mu\text{m}/40n\text{m}$, the switch on-resistance is about $20\,\Omega$. As the load resistance, R_2, switches between $R_{2,on}$ and $R_{2,off}$, the jump in impedance appearing across the oscillator becomes a function of coupling factor as shown in Fig. 2.24(b) even when $k > k_C$ (compare with Fig. 2.20(b)). Now as the coils are brought close together, it is seen that the modulation index will pinch off to zero at a certain k (k_{Null}). When the coils are even closer, the modulation index reverses sign. Index reversal is always problematic in data

[11] Here, we are again effectively using an asymptotic analysis to simplify the problem.

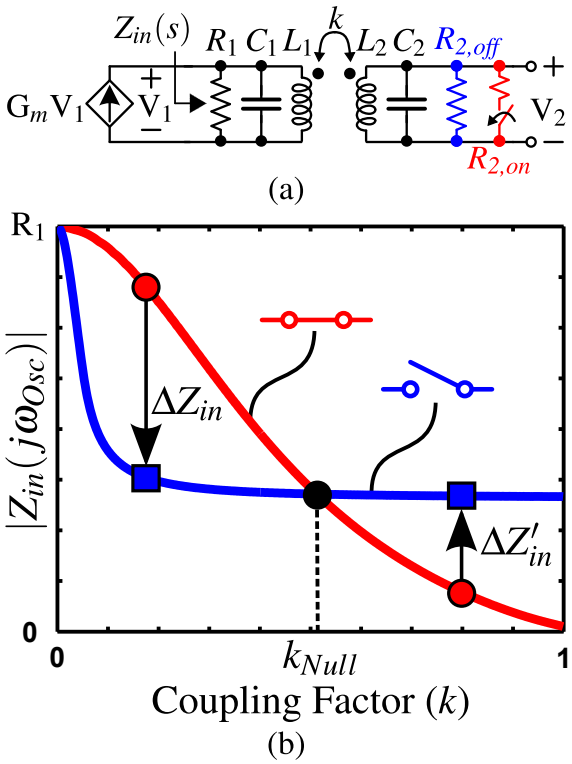


Figure 2.24: (a) Finite switch on-resistance, (b) Null point.

transmission. This means if the transmitter in the implant intends to send, for example, '1', the receiver in the external module will interpret the bit incorrectly as '0'.

This sign inversion can be understood better by looking at the input impedance magnitude, $|Z_{in}(j\omega)|$, as a function of frequency. Fig. 2.25(a) shows the frequency dependence of $|Z_{in}(j\omega)|$ when $k < k_{Null}$. Opening the switch lowers the magnitude of the peak, and shifts the frequency of oscillation a little. On the other hand, when $k > k_{Null}$, shown in Fig. 2.25(c), opening the switch raises the magnitude of peak while the frequency of oscillation changes by a lot. However, when $k = k_{Null}$, the change in the state of the switch shifts the frequency of oscillation only but the magnitude of the peak impedance stays the same (Fig. 2.25(b)). Oscillation takes place at the frequency of highest impedance. In this, since the envelope detector is oblivious to frequency, it is unable to detect the change in the switch state. In other words, at $k = k_{Null}$, binary data cannot modulate the oscillation amplitude, only its frequency. As the coils are brought closer together and k passes through the critical k_{Null}, the demodulated data is inverted.

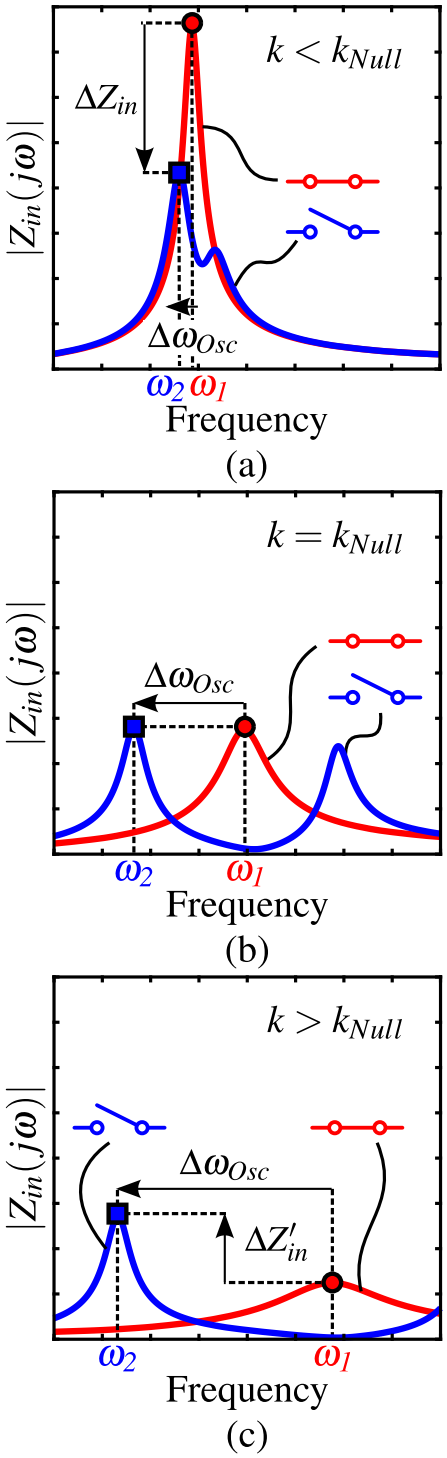


Figure 2.25: Input impedance magnitude plots vs. frequency: (a) When $k < k_{Null}$, (b) When $k = k_{Null}$, (c) When $k > k_{Null}$.

One way to avert data inversion is to employ frequency detection. That is because opening the switch shifts frequency always in one direction, decreasing, as seen in Fig. 2.25. However, there are two problems with this detection technique. First, the frequency shift when $k < k_{Null}$ can be very small. It may even reach zero for $k < 1/Q_{2,off}$, because, in this range, the oscillation frequencies for $R_2 = R_{2,on}$ and $R_2 = R_{2,off}$ are the same and equal to $\omega_1 = \omega_0/\sqrt{1-k^2}$. Secondly, the frequency detection is usually more complicated and therefore less energy-efficient compared to envelope detection. This is why we, and most small systems such as RF tags [76], use envelope detection. But we are the first to point out the hazard of the modulation null.

2.9 Modulation Null: Understanding The Design Space

The modulation null appears when the two input impedances when the switch is open and when it is closed become equal. In other words, as shown in Fig. 2.24(b), k_{Null} is where the two input impedance profiles intercept each other:

$$G_{in}(s = j\omega_{Osc}^{off}, R_2 = R_{2,off}) = G_{in}(s = j\omega_{Osc}^{on}, R_2 = R_{2,on}) \tag{2.65}$$

Using (2.53) and (2.56), this can be written as:

$$G_1\big(1 + \frac{Q_1}{Q_{2,off}}\big) = G_1\big(1 + \frac{k_{Null}^2}{1-k_{Null}^2} Q_1 Q_{2,on}\big) \tag{2.66}$$

Solving for k_{Null}:

$$k_{Null} = \sqrt{\frac{1}{1 + Q_{2,on}Q_{2,off}}} \tag{2.67}$$

where $Q_{2,off}$ and $Q_{2,on}$ are defined as follows:

$$Q_{2,off} = \frac{R_{2,off}}{\omega_{Osc}^{off} L_2} \tag{2.68}$$

$$Q_{2,on} = \frac{R_{2,on}}{\omega_{Osc}^{on} L_2} \tag{2.69}$$

Assuming $Q_{2,on},\ Q_{2,off} \gg 1$, (2.67) is approximately:

$$k_{Null} \simeq \sqrt{k_{C,on} \times k_{C,off}} \tag{2.70}$$

where $k_{C,off}$ and $k_{C,on}$ are defined as:

$$k_{C,off} = \frac{1}{Q_{2,off}} \tag{2.71}$$

$$k_{C,on} = \frac{1}{Q_{2,on}} \tag{2.72}$$

Equation (2.70) says that k_{Null} is roughly the geometric mean of the critical coupling factors corresponding to the switch states when being open and being closed.

2.10 Governing The Modulation Index Null by The Link Parameters

As shown in the previous section, the coupling factor at the modulation null, k_{Null} is a function of two parameters: the switch on-resistance ($R_{2,on}$) and the load resistance ($R_{2,off}$). A larger switch with its smaller on-resistance is expected to approach the ideal case where the on-resistance is zero. By enlarging the size of the switch, as Fig. 2.26(a) shows, the k_{Null} shifts to the right, which results in a broader range of operation. In practice, by pushing k_{Null} beyond the expected range of coupling factors (e.g. $k = 0.3 \sim 0.5$ for air-cored coils [40, 74]), the link will operate at a reasonable modulation index throughout.

The other way to avoid a null in AM index is to choose a proper load resistance $R_{2,off}$. A load resistance can be selected according to the expected operational range and the typical switch on-resistance. In practice, a more convenient method is to have tunability in the load resistance by using a resistor bank where the load resistance is changed according to the coil separation (Fig. 2.27). For instance, by lowering the load resistance using the resistor bank, the null point will also shift to the right, as shown in Fig. 2.26(b). But we need an automatic method to sense the coil separation which can be accomplished by estimating the oscillation frequency.

A larger size of the FET switch causes the power consumption for uplink data transmission to increase. That is because the gate capacitance is proportional to the switch size ($C \propto W \times L$). As the switch size increases, the modulation power consumed to drive the

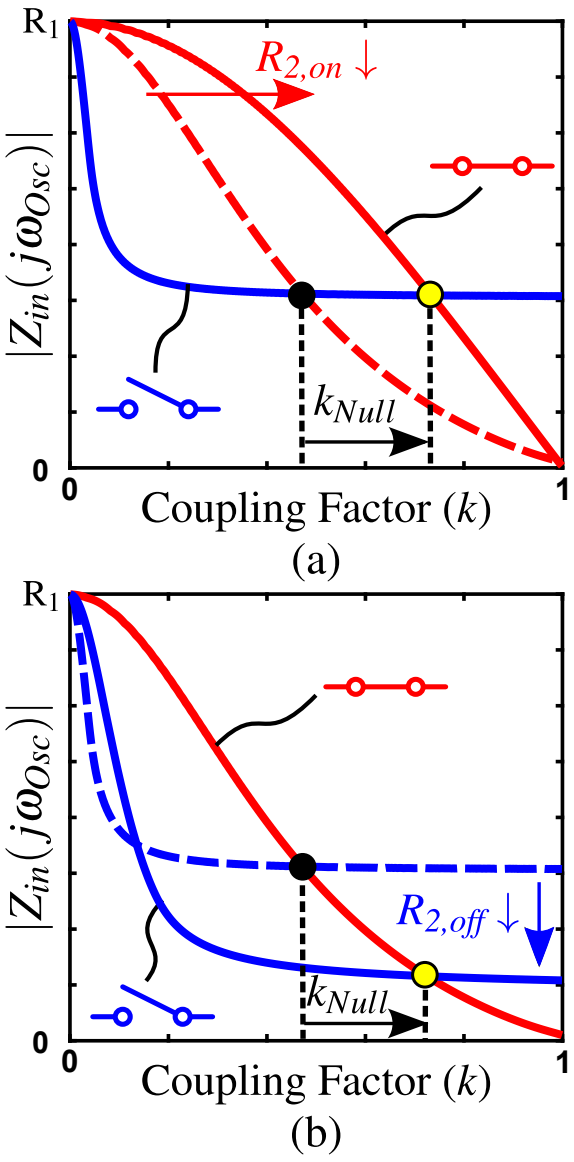


Figure 2.26: Expanding the region of operation: (a) increasing the size of the switch, (b) decreasing the load resistance.

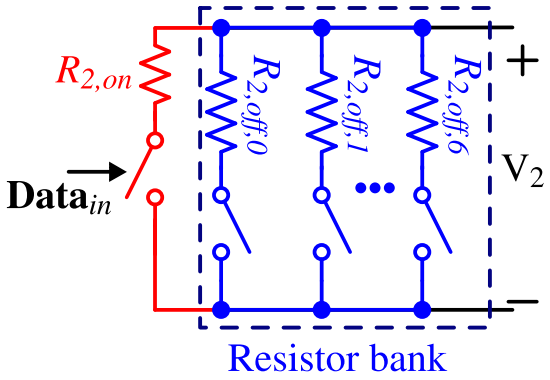


Figure 2.27: Resistor bank to choose a proper $R_{2,off}$.

switch ($\propto C \times V^2$) will increase. Therefore, there is a clear trade-off between the range of operation and the power consumption. We chose a switch size that gives about 20 Ohms on-resistance to achieve a reasonable compromise between the range and power, and then deployed the second approach to the degree possible.

2.11 Circuits

2.11.1 Oscillator and Inductive Link

The realized link, as shown in Fig. 2.28, consists of a resistor bank on the secondary side ($R_{2,off}$) for controlling the range of operation. As well, there is a resistor bank R_1 on the primary side that adjusts the channel bandwidth.

The oscillator uses a cross-coupled CMOS differential pair to obtain a negative conductance from a given bias current. The magnitude of the conductance is large enough to start up oscillation over a broad range of impedance at the the terminals. The oscillator circuit is biased with a binary weighted tail current controlled by the transmitted data and by an amplitude control loop. This loop is only active at start-up, when it adjusts the current source. During normal operation this loop is disabled, the data word controlling oscillation amplitude is held in a register, and only the downlink binary data modulates the amplitude of the oscillator. When the downlink data commands small amplitude, a minimum bias current is maintained to avoid the long start-up time of the oscillator. During uplink

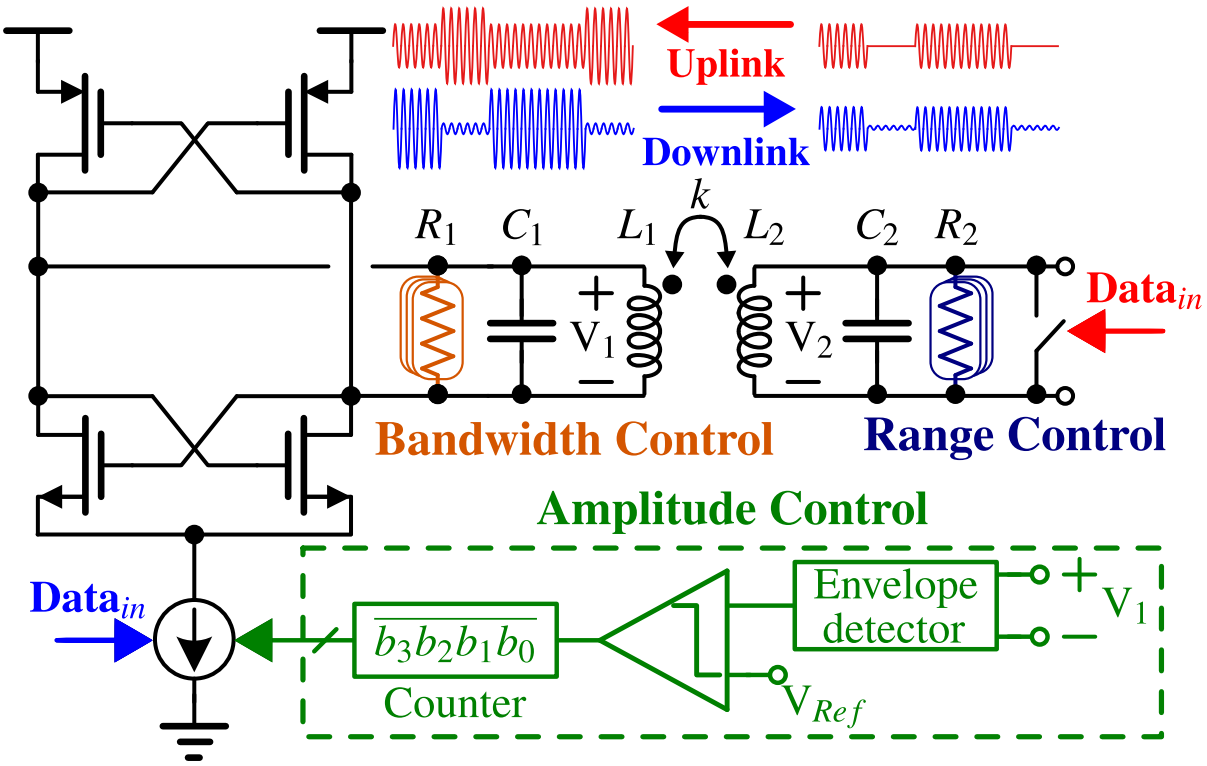


Figure 2.28: CMOS oscillator driving the inductive link.

communication, the bias current source is maintained at its maximum, while the switch in the implant modulates oscillation amplitude with switched resistance.

The amplitude control loop includes an envelope detector, a high gain amplifier to compare the detected amplitude with a DC reference voltage, V_{Ref}, and a digital counter which outputs a binary word controlling the binary-weighted tail current [93]. At start-up, the counter starts from zero and raises the tail current linearly with time. When the amplitude reaches the desired level, the input bit to the counter changes and stops the linear search. The counter is frozen while communication is established between the two sides. This search ensures that the oscillator starts up properly and consumes optimal current for a given impedance across its terminals — for a given oscillation voltage, the lower the load impedance, the higher the current needed. The DC reference voltage, V_{Ref}, biases the oscillator in current-limit operation mode [94, 95]. Otherwise, the oscillator could be desensitized to variations in the impedance across its terminals and oscillation amplitude might change very little when the switch in the implant toggles.

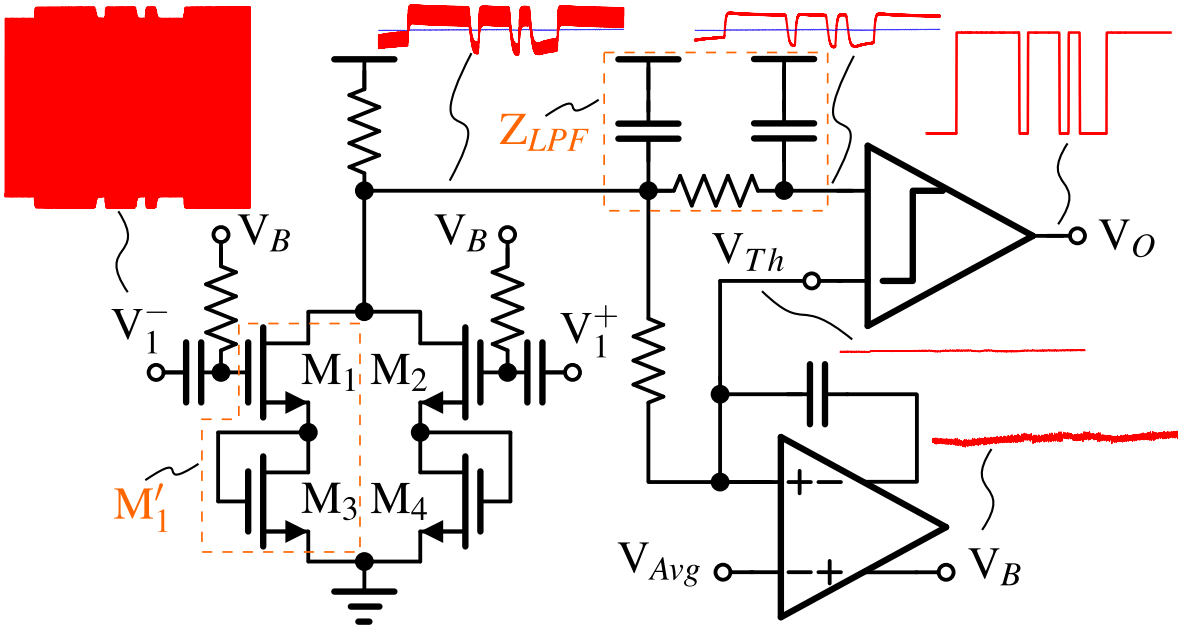


Figure 2.29: Analog front-end.

2.11.2 Analog Front-End

The received waveform is demodulated by an envelope-detector. As can be seen in Fig. 2.29, the detector consists of two identical degenerated common-source FETs with connected drains, with the input differential voltage applied to their gates. The diode-connected FETs extend the unclipped range of operation.

As an outcome of its bilateral symmetry, this detector circuit has an even-order non-linear voltage transfer characteristic from differential inputs to output, which rectifies the input waveform. The differential input sinusoidal voltage is translated to DC and the 2nd harmonic: the DC output is sufficient to indicate the envelope.

The rectification principle can be understood by writing the current equation for the common-source FETs and adding them together to find the total current, I_{total}. Assuming that we can model the stacked transistors pairs of M_1-M_3 and M_2-M_4 as two equivalent FETs of M_1' and M_2' with a threshold voltage of V_t' and an aspect ratio of $(W/L)'$[12], and M_1' and

[12]As It is shown in Appendix B, the stack of devices with the same sizes (i.e. $(W/L)_{M_1} = (W/L)_{M_3}$) and the same threshold voltages (i.e. $V_{t,M_1} = V_{t,M_3}$) shown in Fig. 2.29, can be modeled as an equivalent FET whose threshold voltage and size are, respectively, twice and 1/4th of each transistor threshold voltage and size (i.e $V_t' = V_{t,M_1'} = 2 \times V_{t,M_1}$ and $(W/L)_1' = (W/L)_{M_1'} = 0.25 \times (W/L)_{M_1}$).

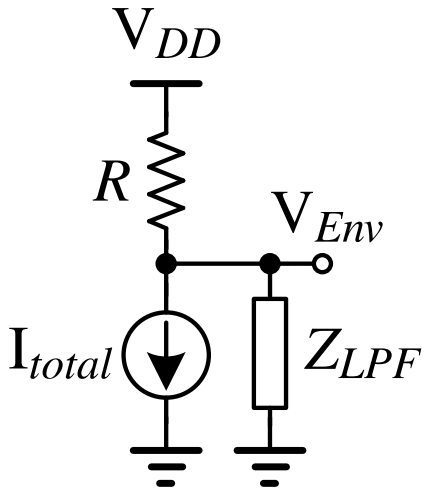


Figure 2.30: The envelope detector circuit model.

M_2' work in saturation mode for the expected input range, we have:

$$I_{total} = I_{M_1'} + I_{M_2'} \tag{2.73}$$

$$I_{M_1'} = \frac{\beta'}{2}(V_1^- + V_B - V_t')^2 \tag{2.74}$$

$$I_{M_2'} = \frac{\beta'}{2}(V_1^+ + V_B - V_t')^2 \tag{2.75}$$

where $\beta' = \mu_n C_{ox}(W/L)'$. For V_1^- and V_1^+, it can be assumed:

$$V_1^- = -A\sin(\omega t) \tag{2.76}$$

$$V_1^+ = +A\sin(\omega t) \tag{2.77}$$

where A is the amplitude of the input signal to the envelope detector. Substituting (2.76) and (2.77) in (2.73), we obtain:

$$I_{total} = \beta'\big[\big((V_B - V_T')^2 + \frac{A^2}{2}\big) - \frac{A^2}{2}\cos(2\omega t)\big] \tag{2.78}$$

I_{total} contains the DC and 2nd harmonic components. As shown in Fig. 2.30, I_{total} later goes into the parallel combination of a resistor, R, tied to the voltage source, V_{DD}, and an impedance, Z_{LPF}, with a 2nd order low pass characteristic and produces an output voltage, V_{Env}, as follows:

$$V_{Env} = V_{DD} - \beta' R\big((V_B - V_T')^2 + \frac{A^2}{2}\big) + \beta\frac{A^2}{2}\cos(2\omega t + \theta) \times \Big|R||Z_{LPF}(j2\omega)\Big| \tag{2.79}$$

Assuming $\left|R||Z_{LPF}(j2\omega)\right|$ is a very small value, the third term in (2.79) which is the 2nd harmonic component is negligible and the remaining DC component measures the envelope.

Assuming A_0 and A_1 are, respectively, the input signal amplitudes (i.e. A) for the bits '0' and '1', the envelope levels for '0' and '1' are given by:

$$V_{Env}\Big|_{bit=0} = V_{DD} - \beta' R\big((V_B - V'_T)^2 + \frac{A_0^2}{2}\big) \tag{2.80}$$

$$V_{Env}\Big|_{bit=1} = V_{DD} - \beta' R\big((V_B - V'_T)^2 + \frac{A_1^2}{2}\big) \tag{2.81}$$

Assuming $A_1 \geq A_0$, the envelope peak-to-peak can be calculated as:

$$V_{Env,pp} = V_{Env}\Big|_{bit=0} - V_{Env}\Big|_{bit=1} = \frac{\beta' R}{2}(A_1^2 - A_0^2) \tag{2.82}$$

Based on (2.82), for given values of β', A_0 and A_1, the larger the resistance R, the better the SNR, the lower the error rate (BER). However, for very large values of R, the transistors may go into triode mode, their transconductances g_m will collapse and V_{Env} will be roughly zero for the both input amplitudes, A_0 and A_1. Therefore, the peak-to-peak value is actually a concave function with respect to R (i.e. has a maximum). Assuming the transistors' overdrive voltages, $V'_{ov} = V'_{GS} - V'_T$, are relatively small, the optimum value for R is approximately as follows:

$$R_{Opt} = \frac{V_{DD}}{\beta'\big((V_B - V'_T)^2 + \frac{A_1^2}{2}\big)} \tag{2.83}$$

The typical values of A_0 and A_1 for uplink can be calculated using the impedance curves in Fig. 2.24. However, when the coils are far apart (e.g. $2\,\text{cm} \sim 4\,\text{cm}$ in our case: small k in Fig. 2.20(b)), the modulation index is small as expected, and thus detection becomes difficult. To mitigate this, a loop adaptively biases the detector in response to shrinking index (Fig. 2.29). In the loop, an integrator adjusts the bias V_B at the gates such that the DC level of the rectified waveform (i.e. average of the envelope, $\overline{V_{Env}}$), reaches a reference voltage, V_{Avg}. Since this adaptive loop also makes the detector bias robust to PVT variation, a similar bias loop has been used in reception of downlink data in the external module.

The rectified waveform, as shown above, passes a 2nd order RC low-pass impedance (Z_{LPF}), whose cutoff is chosen to suppress the 2nd harmonic of the carrier frequency but pass

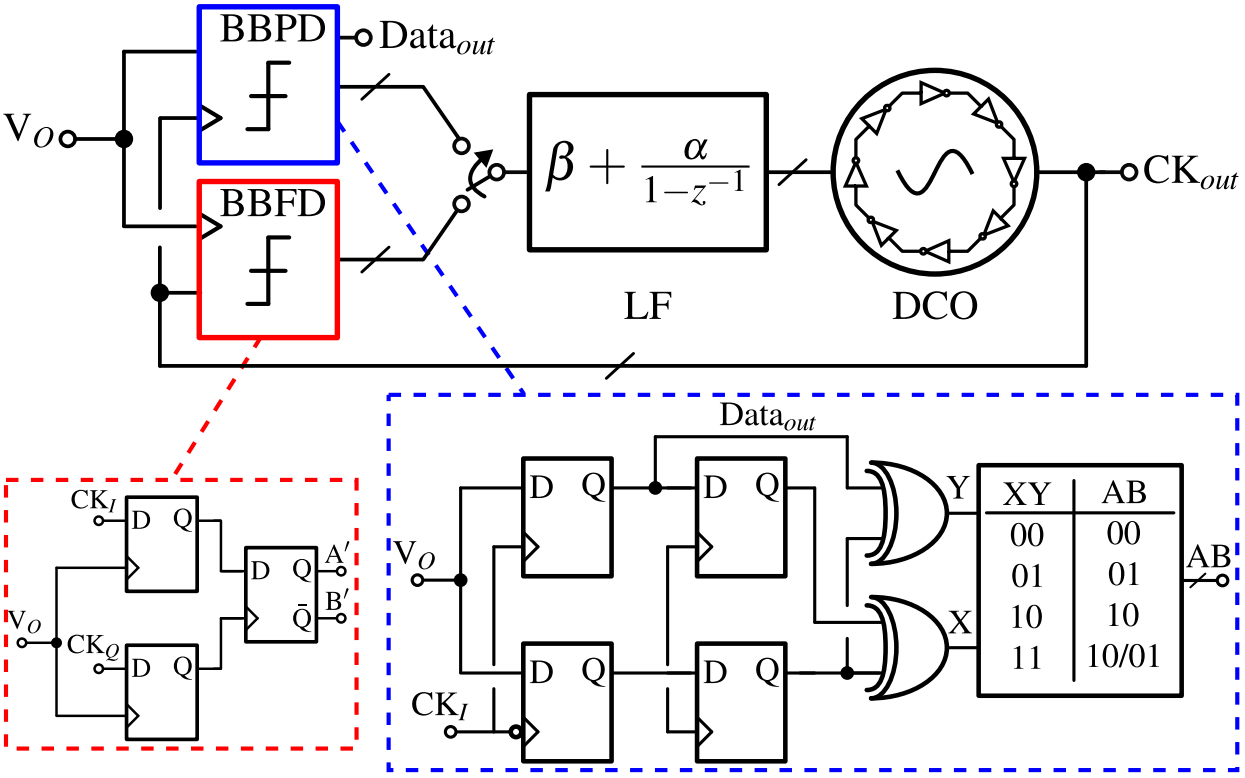


Figure 2.31: Clock and data recovery loop.

the spectrum of the modulated envelope. A limiting amplifier slices the envelope against an extracted threshold voltage, V_{Th} for adaptive thresholding. This threshold voltage is forced to the correct slice level, V_{Avg}, by the bias loop.

2.11.3 Clock and Data Recovery Loop

The output of the limiting amplifier, V_O, a two-level waveform with random transitions, must be re-timed and sampled at the right instants to reconstruct the data at a low error rate. This requires a clock and data recovery (CDR) loop. As shown in Fig. 2.31, the loop consists of a bang-bang phase detector (BBPD), a frequency detector (BBFD) to widen the acquisition range, an integral and proportional loop filter, and a digital controlled oscillator (DCO).

This BBPD is a modified form of the well-known Alexander phase detector [96], which produces synchronous data decisions. We have chosen this phase detector because it can

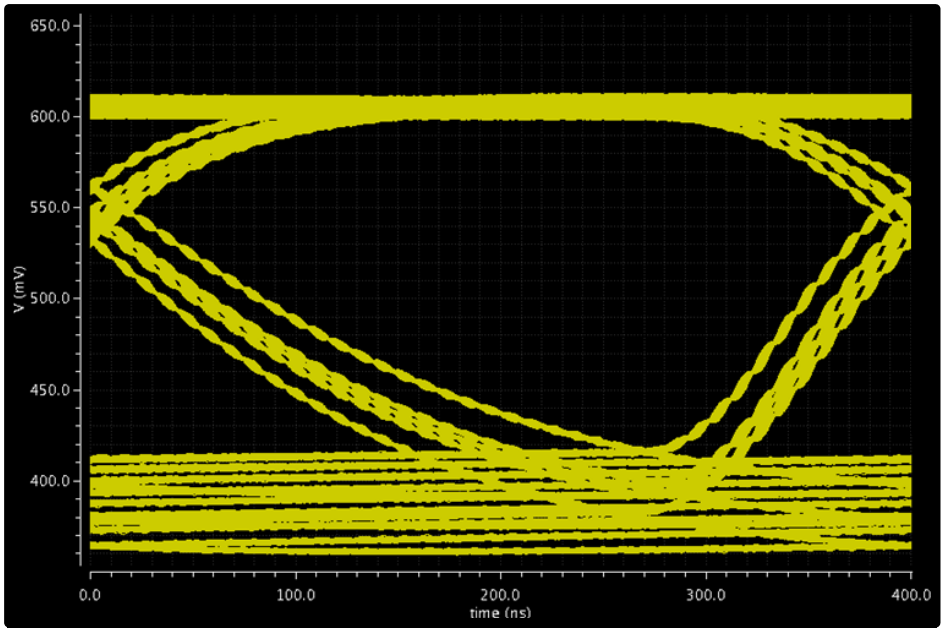


Figure 2.32: Distorted eye diagram at the receiver (At a data rate of 2.5 Mbps).

lock to data waveforms with a non-50% duty cycle. These unbalances are characteristic of this system because the two unequal values of modulation resistance in uplink mode cause unequal attack and decay times. Fig. 2.32 shows the simulated distorted eye diagram at the receiver.

The BBPD needs to be modified from its original design. To understand why, it is helpful to look the waveforms in an Alexander PD. Fig. 2.33(a) and Fig. 2.33(b) illustrate the "early-late" principle of an Alexander PD [97]. By sampling the data waveform (in our case, V_O) at three consecutive points around the data transition, we can infer if the clock (in our case, CK_I) lags or leads the data. In Alexander PD, if $X = A \oplus B =$ '1' and $Y = B \oplus C =$ '0', the clock leads and the clock frequency must decrease; if $X = A \oplus B =$ '1' and $Y = B \oplus C =$ '0', the clock lags and the clock frequency must increase; and when $X = A \oplus B = B \oplus C = Y =$ '0', there is no transition in the data, and the clock frequency is held constant. The output $X = A \oplus B = B \oplus C = Y =$ '1' is left undefined (erroneous output) as it can never happen normally, and indeed, thinking of a charge pump characteristic (push-pull), the PD output $XY =$ '11' will act similar to '00' for the loop filter. When the data has a 50% duty cycle, this logic makes the falling edge of the clock to lock to the edges of

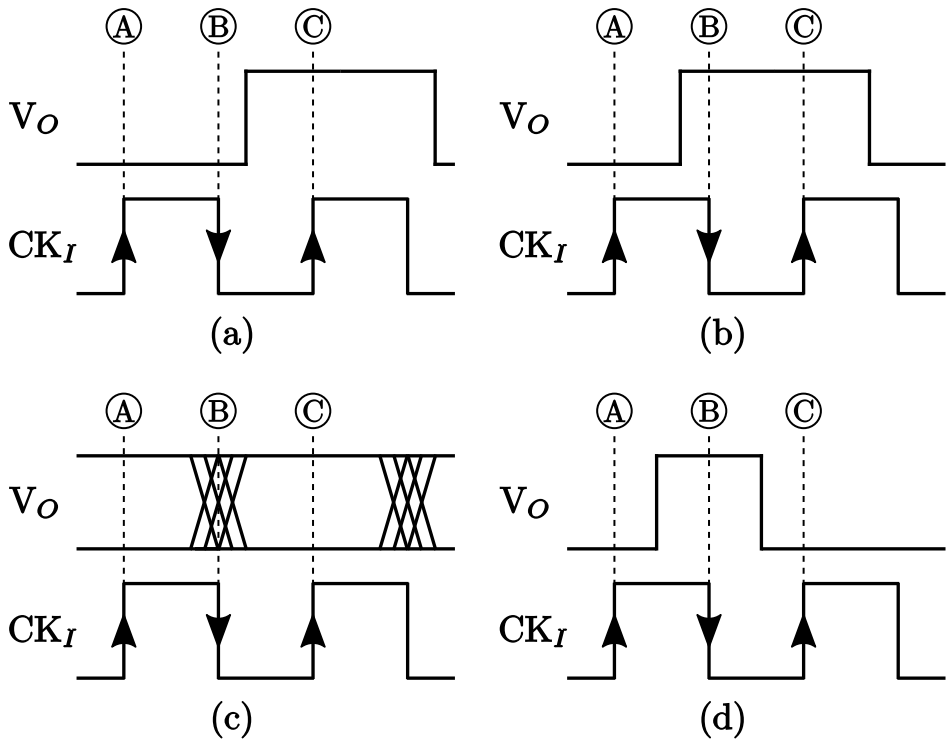


Figure 2.33: The principle of an Alexander phase detector: (a) the clock is early, (b) the clock is late, (c) the falling edge of the clock locks to the data edges, (d) erroneous output with non-50% duty-cycled data.

the data while the rising edge of the clock sampling the data at the eye center (Fig. 2.33(c)).

However, when the duty cycle of data is highly distorted from 50%, it is possible that $X = A \oplus B = B \oplus C = Y =$'1' as shown in Fig. 2.33(d). This causes the loop to have a second stable operating point, when the clock is trapped in the wrong phase (not locked to the data edges) and because of a time window that creates a dead zone, the jitter can increase. To help the BBPD recover from the wrong phase and lock to the edges of data, the XY output can be reinterpreted by an extra piece of logic circuit where the output $XY =$'11' is mapped to either '01' or '10' (truth table in Fig. 2.31).

The loop filter is realized as a digital circuit which implements the transfer function $\beta + \alpha/(1 - z^{-1})$. The proportional term, β, was calculated in such a way that it balances the jitter contributions of the DCO phase noise and the input waveform jitter (due to ISI) at

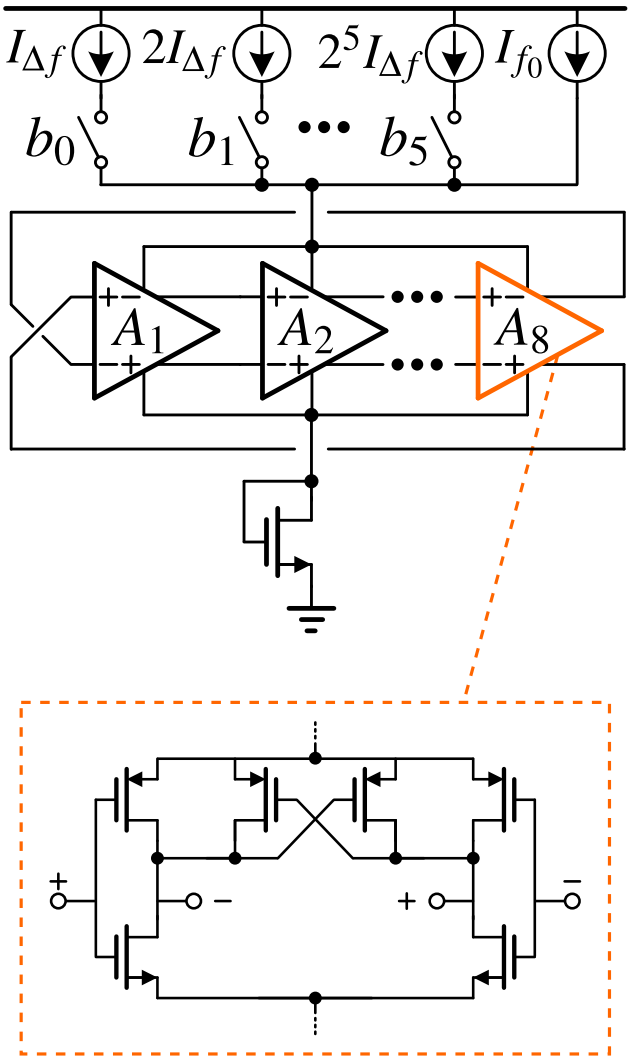


Figure 2.34: Digital-controlled oscillator: (a) Ring DCO architecture, (b) Delay cell circuit

the output of the loop [98]. The coefficient of the integral term, α, was chosen for stability. With a nominal input jitter, the loop has been designed for a phase margin of $50° \sim 60°$.

In the DCO, the frequency of an eight-stage differential ring oscillator is controlled by a 6-bit current DAC (Fig. 2.34). The number of the bits is selected so that the quantization noise from dithering of the frequency control word and the oscillator phase noise [99, 100] contribute equal amounts of jitter at the output of the CDR.

$\Delta\Sigma$ modulator (DSM) was not used to lower the quantization noise further because noise at the loop output is already dominated by the DCO phase noise due to its very low power consumption, even at 6-bit quantization.

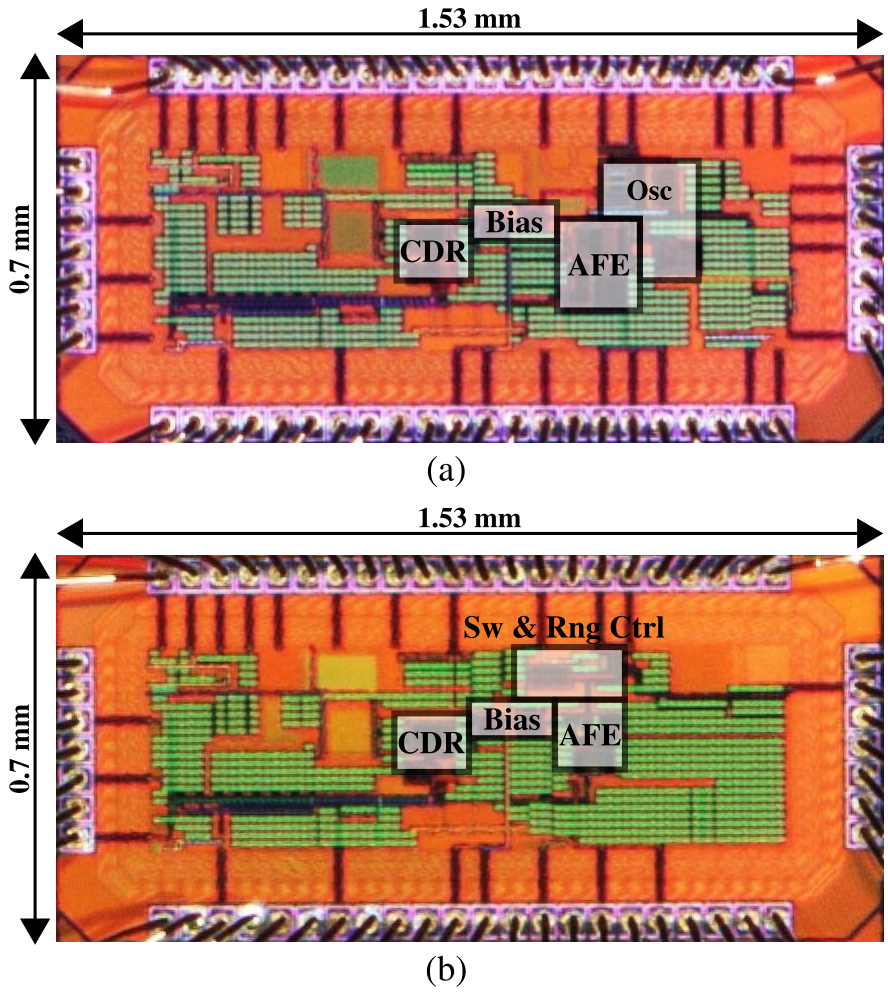


Figure 2.35: Transceiver chip micrographs: (a) External TRx, (b) Implanted TRx.

Each of the delay cells is realized with two current starved inverters, coupled and boosted with a PMOS cross coupled pair (Fig. 2.34) [46, 101, 102, 103].

2.12 Measurements

The transceiver chips were fabricated in TSMC 40 nm CMOS (Fig. 2.35). The active areas of the implanted and external transceivers are roughly 0.1 mm^2 and 0.12 mm^2. For testing, the transceiver chips were housed in 48-pin QFN packages and mounted on 4-layer polyimide PCBs. Hand wound 20 AWG wire coils with two turns, 3 cm diameter, and an inductance of

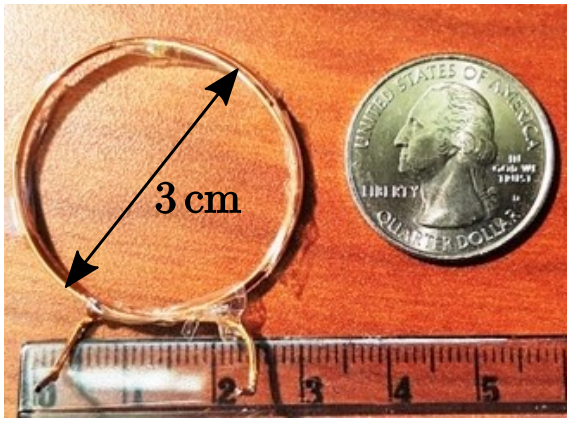


Figure 2.36: Hand wound wire coil with two turns, 3 cm diameter, and an inductance of $L \approx 330\,nH$.

$L \approx 330\,nH$[13] (Fig. 2.36) were mounted at the edges of the boards as the coupled inductors. The value of the coil inductance was chosen for a practical compromise. A larger inductance means lower power consumption in the free-running oscillator for a given oscillation amplitude, which we want. However, since the parasitic capacitance from PCB may be as high as $C_{parasitic} \sim 5\,pF$, the inductance cannot be very large; otherwise it will be difficult to define the oscillation frequency of 35 MHz accurately, since the tuning capacitor $\sim C_{parasitic}$. To operate at 35 MHz, an on-board discrete capacitor of 60 pF ($\gg C_{parasitic} \sim 5\,pF$) was used. The diameter of the coil is chosen based on the required range of operation (R_{Max}) and estimated minimum coupling factor (k_{min}) that the link can operate flawlessly[14].

The implanted chip consumes only 0.3 μW switching power for transmitting uplink binary

[13]The quality factor, Q, of this coil at 35 MHz is more than 200.

[14]A modified from of the Roz formula for coupling factor k [90] to capture reciprocity is:

$$k \approx \left(\frac{D_1 D_2}{4R^2 + D_1^2 + D_2^2}\right)^{3/2} \cos\theta \tag{2.84}$$

where R is the coil distance, θ is the angel between the planes of the coils, and D_1 and D_2 are the diameters of the external and implant's coils. Assuming $D_1 = D_2 = D$, at $k = k_{min}$, (2.84) can be simplified to:

$$k_{min} \approx \left(\frac{1}{4\left(\frac{R_{Max}}{D}\right)^2 + 2}\right)^{3/2} \cos\theta \tag{2.85}$$

Knowing the required range of operation, R_{Max}, and estimated minimum coupling factor (k_{min}), the coil diameter D can be calculated with (2.85).

data at 4 Mbps. Receiving downlink data at 2 Mbps, the power dissipation of the implant is nearly 10 μW. The power in the external module is mainly set by the free-running oscillator, approximately 600 μW in uplink and 400 μW in downlink.

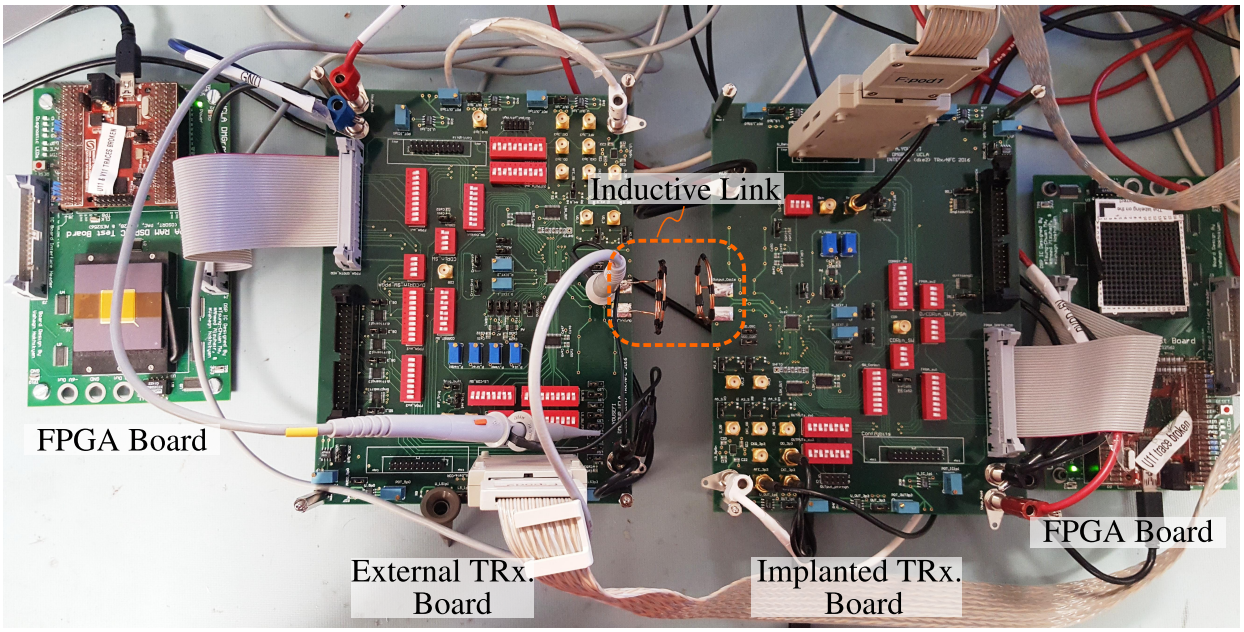
Fig. 2.37 shows the measurement setup. Fig. 2.37(a) shows implanted and external transceiver development boards on which the packaged transceiver ICs are assembled. There are two FPGA boards through which a PC terminal configures the development boards to operate under different modes of operation.

To test the data link, as shown in Fig. 2.37(b), a $2^7 - 1$ pseudo random data stream is generated by a logic analyzer (pattern generator function) and sent to the board. The recovered clock and data are then observed and compared with the transmitted data on an oscilloscope.

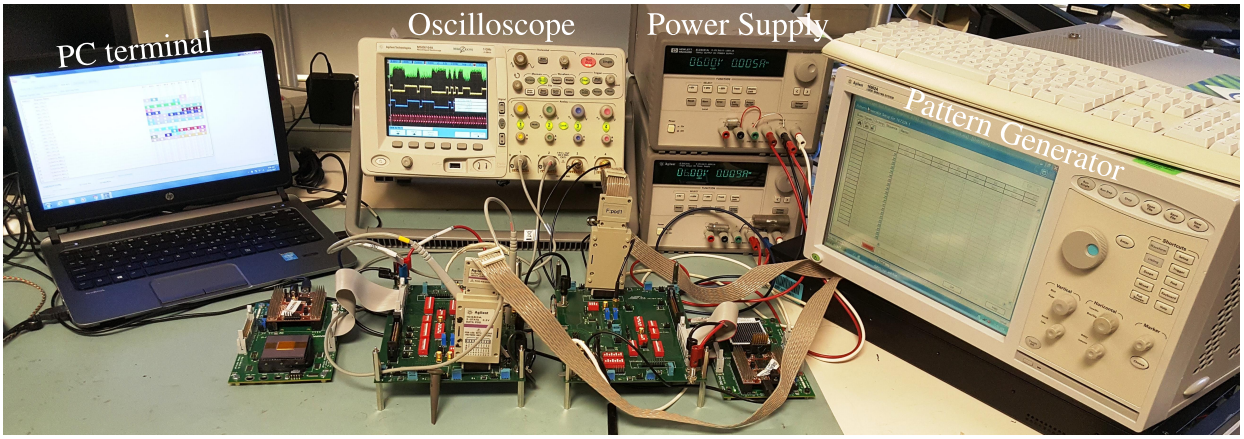
The waveforms shown in Fig. 2.38(a) are the measurement results for uplink at 4 Mpbs. From top to bottom, the first (V_1) and second ($Data_{in}$) waveforms are the free-running oscillator voltage response (on the primary; single-ended) to switching load on the implant, and the binary data which switches the implant load, respectively. The recovered data, $Data_{out}$, in the external unit is the third waveform. The fourth waveform is the reconstructed clock in the CDR. The one clock cycle delay of $Data_{out}$ with respect to $Data_{in}$ is mainly due to the flip-flops in the CDR phase detector, and the propagation delay is relatively insignificant.

Fig 2.38(b) shows the measured waveforms for downlink at 2 Mbps. Here, the binary data waveform ($Data_{in}$) is sent from the external transceiver to the implanted transceiver. In Fig 2.38(b), the first waveform from top, V_1, shows the single-ended amplitude of the oscillator modulated by the binary data. The last two waveforms are the recovered data ($Data_{out}$) and the recovered clock (CK_{out}) in the implant's transceiver.

The bit error rate (BER) of the data link is measured at different coil separations. A 2^7-1 pseudo-random generator (PRBS-7) is implemented on an FPGA to generate binary data at the transmitter. The received data on the receiver side is tested in a loop on the FPGA where the transmitted and received bits are compared. Fig. 2.39 exhibits the measured uplink BER versus coil separation. At a 4-Mbps data rate, when $R_1 = 1.6\,k\Omega$ and $R_2 = 0.8\,k\Omega$, the coils

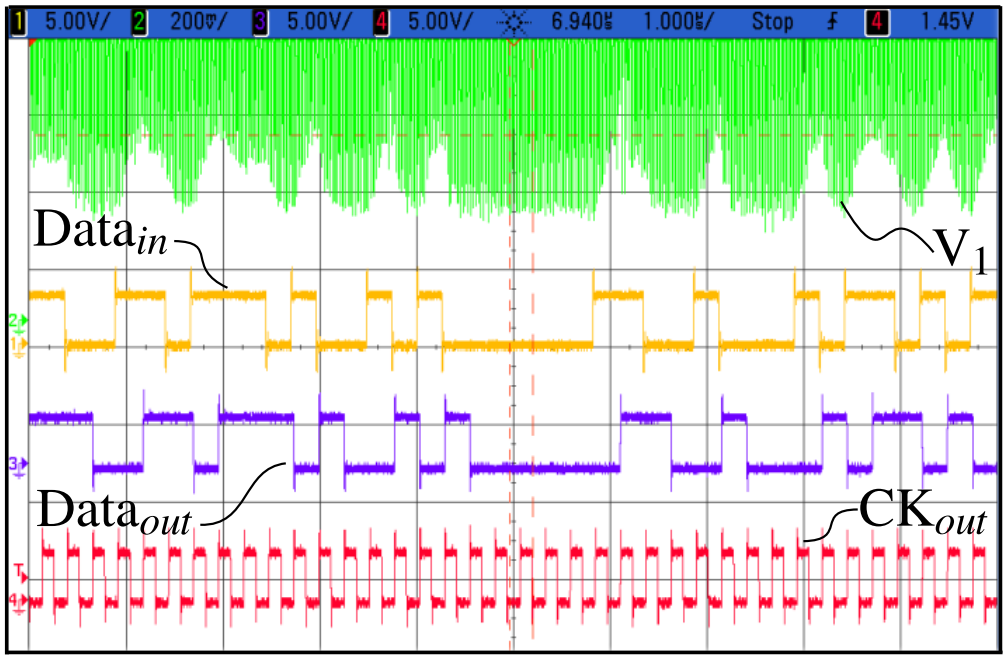


(a)

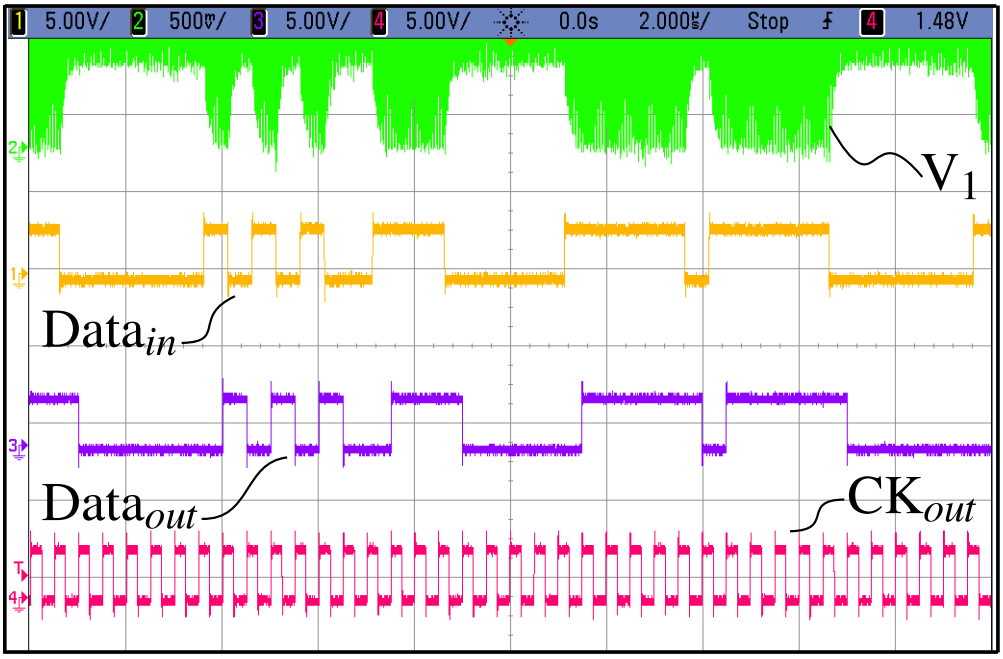


(b)

Figure 2.37: Measurement setup: (a) External and implanted development boards, communicating through the inductive link, (b) A pseudo-random binary sequence is being transmitted from the external transceiver to the implanted transceiver in downlink mode.



(a)



(b)

Figure 2.38: Transmitted vs. received measured waveforms : (a) for uplink mode, (b) for downlink mode.

Table 2.2: Comparison with the state-of-the-art.

References	TBCAS 2008	TCAS 2013	TBCAS 2015	TBCAS 2016	JSSC 2016	ISSCC 2018	**This Work**
Size of coils [cm]	3.5/3.5	1/3	3/1	3/2	6.5/4.2	1/1	**3/3**
Max. range [cm]	2	1	1	0.5	3.5	1.1	**4.5**
Norm. max. range	0.5	0.51	0.51	0.2	0.7	1.07	**1.5**
Car. freq. [MHz]	25	66.6	50	10	13.56	-	**35**
Data rate [Mb/s]	2.8/3	-/20	-/13.56	2/-	6.78/-	200/-	**4/2**
Implant Tx/Rx	36	-	-	-	9.5	1.5	**0.075**
power [pJ/bit]	467	12	162	-	-	-	**5**
External Tx/Rx	5000	180	960	-	-	-	**200**
power [pJ/bit]	892	-	-	-	-	186	**150**

can be separated by $3 \sim 3.5\,\text{cm}$ for a BER of 10^{-6}. By selecting a larger R_2 from the resistor bank (i.e. $R_2 = 6.4\,k\Omega$), this operational range can extend to $4 \sim 4.5\,\text{cm}$. This adjustment can be automatically done by a crude frequency detector where the oscillation frequency is compared with a threshold frequency $\sim \omega 1$.

When R_2 is large, for instance $6.4\,k\Omega$, the BER worsens as the coils are brought closer. This is because the modulation index is pinching off, and in this instance, goes through a null at 2 cm. For a lower data rate of 2 Mbps, the data link is functional up to 5 cm.

In downlink, due to higher modulation index (i.e. $\sim 80\%$) and larger load resistance ($R_2 = 1.6\,k\Omega$), the data link is error-free (BER $< 10^{-10}$) for a distance of 5 cm.

As shown in Table. 2.2, the link can cover the range of 4 cm at 4 Mbps with 3 cm diameter coils. By normalizing this distance (R_{Max}) to the coils diameter (D_1 and D_2) as follows[15] [83]:

$$R_{Norm} = \frac{R_{Max}}{\sqrt{D_1 \times D_2}} \tag{2.86}$$

[15]This can be justified by the modified from of the Roz formula for coupling factor k [90] in (2.84) as defining a unique k, when $R_{Max} > D_1,\, D_2$.

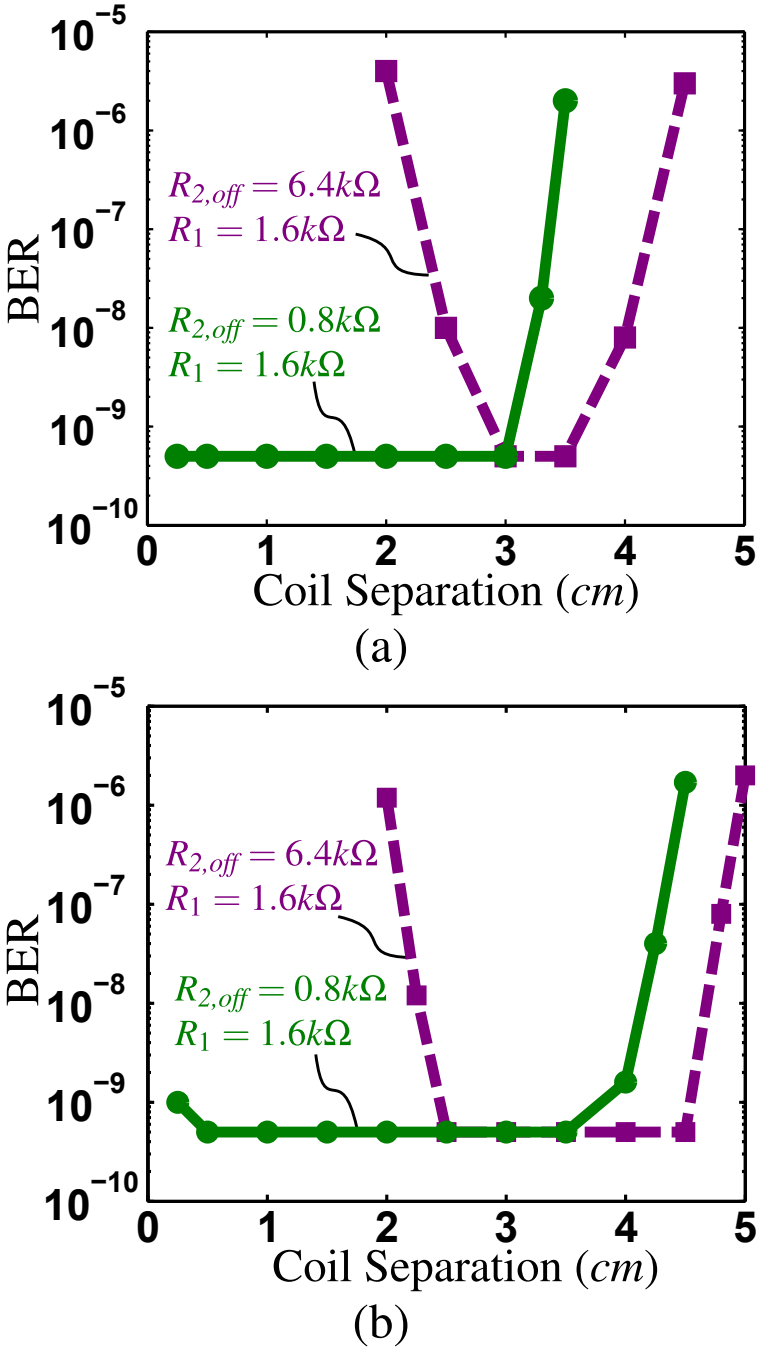


Figure 2.39: Measured bit error rate (BER) for uplink (a) at a 4 Mbps data rate, (b) at a 2 Mbps data rate

a fair comparison can be made between this work and prior art. At the time of presenting this work in 2017 VLSI Circuits Symposium [85], the link demonstrated $2 \sim 3$ times better normalized range (R_{Norm}) compared to prior art. With comparable data rates, bit error rate and external unit energy consumption per bit, the implanted transceiver consumes much lower energy compared to the state of the art: nearly $2 \sim 3$ times lower in receive mode and roughly 125 times lower in transmit mode. Compard to the work presented at ISSCC 2018 [70], the designed data link demonstrated about 40% longer normalized range and 20 times lower power consumption.

This link can work simultaneously beside a wireless power transfer link that operates at a much lower frequency (i.e. $\sim 100\,\text{kHz}$).

CHAPTER 3

System Integration

This chapter presents how the data link is embedded in a human-quality neuromodulation device. Fig. 3.1 shows the implantable neuromodulation system that has been developed by the UCLA team in collaboration with teams from University of California, San Francisco (UCSF) and Lawrence Livermore National Laboratory (LLNL).

The implant contains high density cortical and sub-cortical leads located at the front of the system to interface with brain regions. The leads are connected to the neuromodulator modules (NM) where the neural activity of the brain cells can be captured and digitized with analog front-ends (32 recording channels, each of which contains a low-noise high-dynamic-range amplifier and a high-resolution ADC) [35] and the brain regions can be modulated by stimulation current engines [104]. All the NM circuitry is housed in a bio-compatible titanium capsule.

The NMs are connected to a signal routing hub, aggregator module (AM), where all the recorded neural data is collected and then sent to CM, control module. CM contains a microcontroller (MCU), a wired power transmitter (to AM), wireless power receiver circuit , and the implanted wireless data transceiver chip.

To extract the recorded data or program the implant, there is an external module, ERM, on which an external transceiver chip is assembled. The external module collects the recorded neural data by the wireless link and sends it through a USB port to a PC terminal (or tablet). With a custom PC application, the neural activity can be monitored and modified stimulation parameters or a new closed-loop algorithm can be downloaded to the implant.

In this work, I mainly involved in the development of the CM and the ERM which are elaborated in the rest of this chapter.

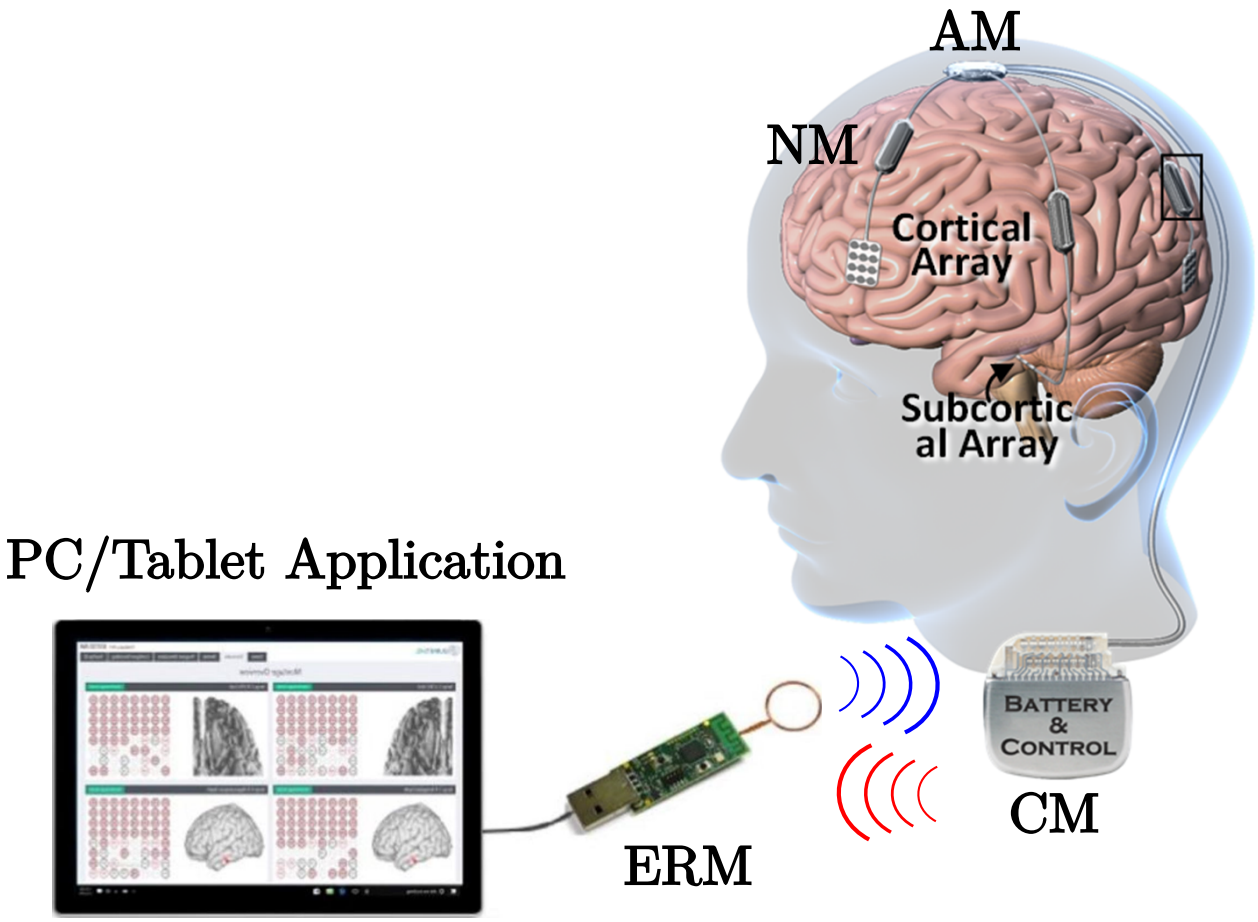


Figure 3.1: Implantable neuromodulation system.

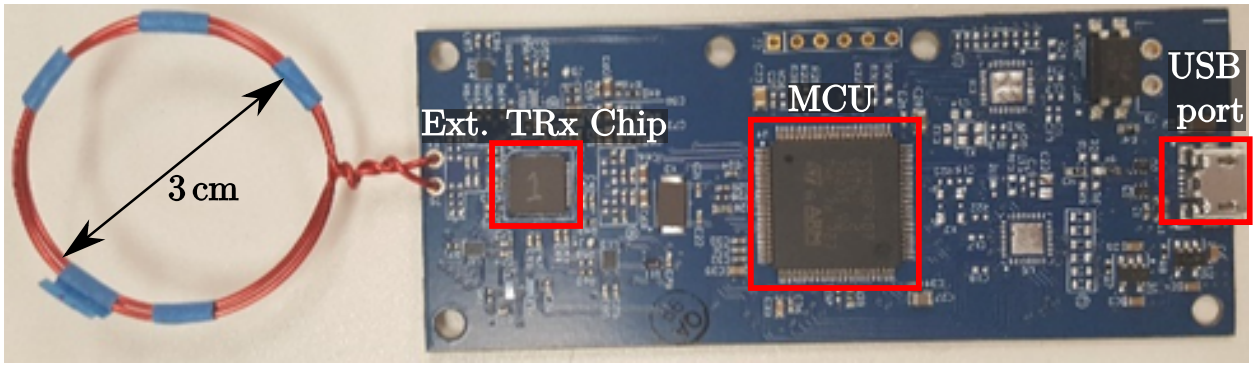


Figure 3.2: ERM with a copper wire coil.

3.1 External Radio Module (ERM)

Fig. 3.2 shows the ERM board consisting of the QFN-packaged transceiver chip, a microcontroller, a USB port and voltage regulators. All the components are mounted on a 4-layer polyimide PCB. The MCU contains a MAC layer processor similar to that discussed in Chapter 4. This handles the data coming from (recovered data) or going to (to-be-transmitted data) the transceiver chip (PHY Layer). For the coil, a hand-wound 20 AWG wire coil with 2 turns and 3 cm diameter similar to the ones in the development boards is used (see Section 2.12).

Fig. 3.3 shows the test setup for characterizing the ERM performance in downlink direction. In this test, binary random data generated in the MCU is sent through the inductive link from the ERM to the implanted transceiver board. The transmitted and received data streams are compared on the oscilloscope. In Fig. 3.3, the top and bottom waveforms on the oscilloscope screen are the transmitted and received data,respectively, and the waveform in the middle is the reconstructed data in the implant transceiver. The link is characterized at different distances for both downlink and uplink, and it is functional up to 5 cm at 2 Mbps. For size comparison as shown in Fig. 3.3, the development board for external transceiver chip is placed beside the ERM which has gone through a miniaturization factor of more than 10X.

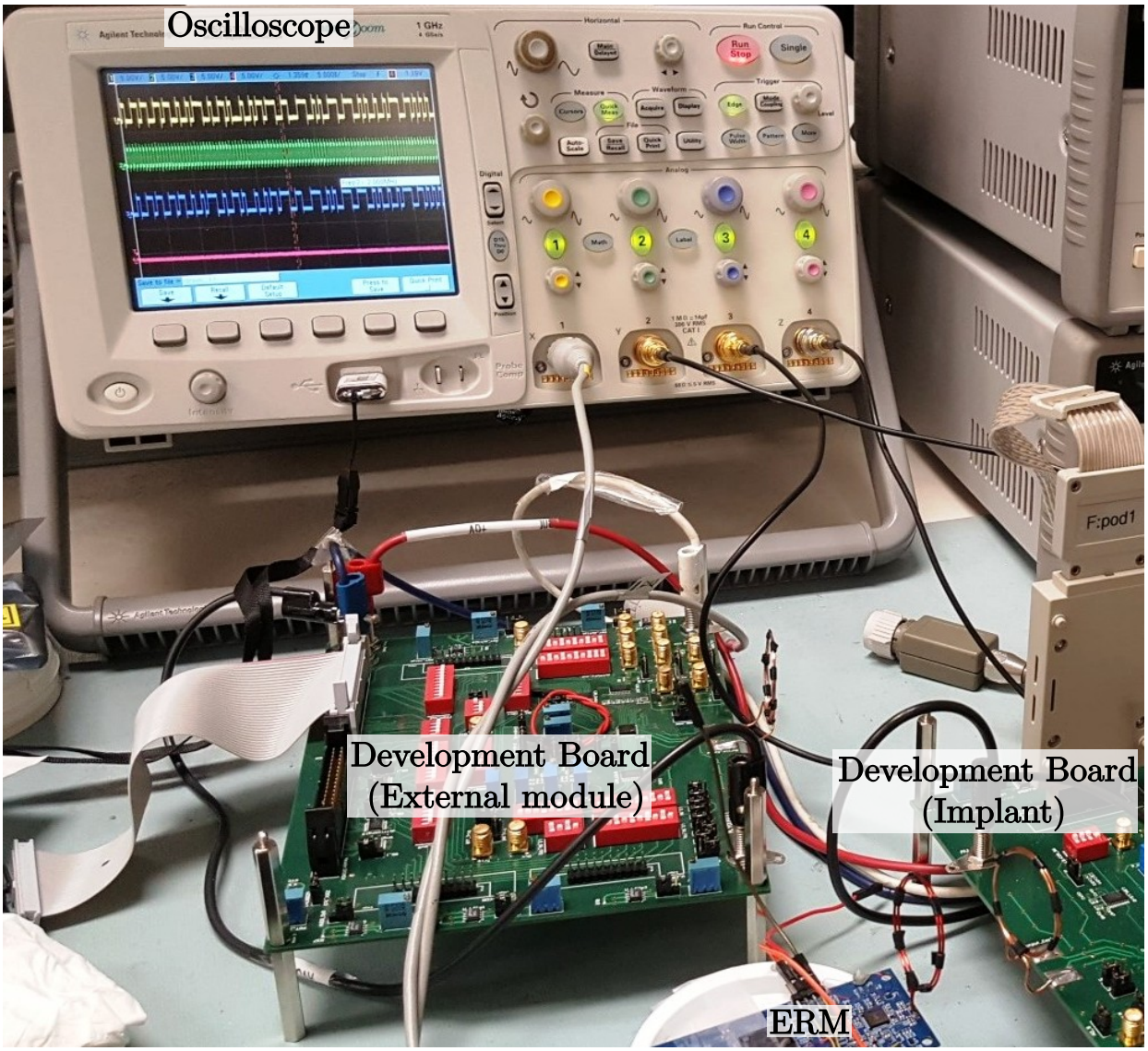


Figure 3.3: Test setup: testing ERM with a development board that contains an implant transceiver chip.

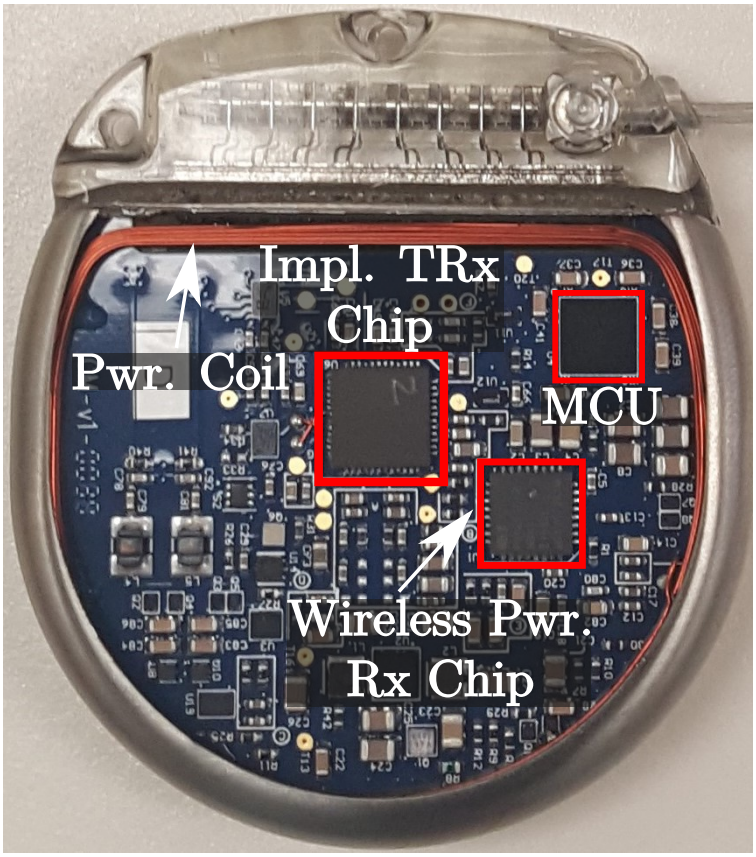


Figure 3.4: CM housed in a titanium can. The can is partially removed for testing.

3.2 Control Module (CM)

Fig. 3.4 shows the CM which will be surgically embedded in the patient's chest. For biocompatibility the board has to reside in a medical-grade titanium can. At the top, medical-grade silicone is hermetically sealed to the titanium can covering the CM header (the BalSeal connector) [105]. For testing and debugging purposes, as shown in Fig. 3.4, the can is partially removed so that the signals on the CM board may be easily probed. The CM consists of an MCU for the closed-loop algorithm and the MAC processor, wireless power receiver chip and coil, and the near-field transceiver chip (implanted), among others. The wireless power link operates at a relatively low frequency ($\sim 100\,\text{kHz}$) and therefore the coil can be kept inside the titanium can. The power link charges a small battery located at the back of the board from which the the power to the CM can be supplied when the wireless power is not present.

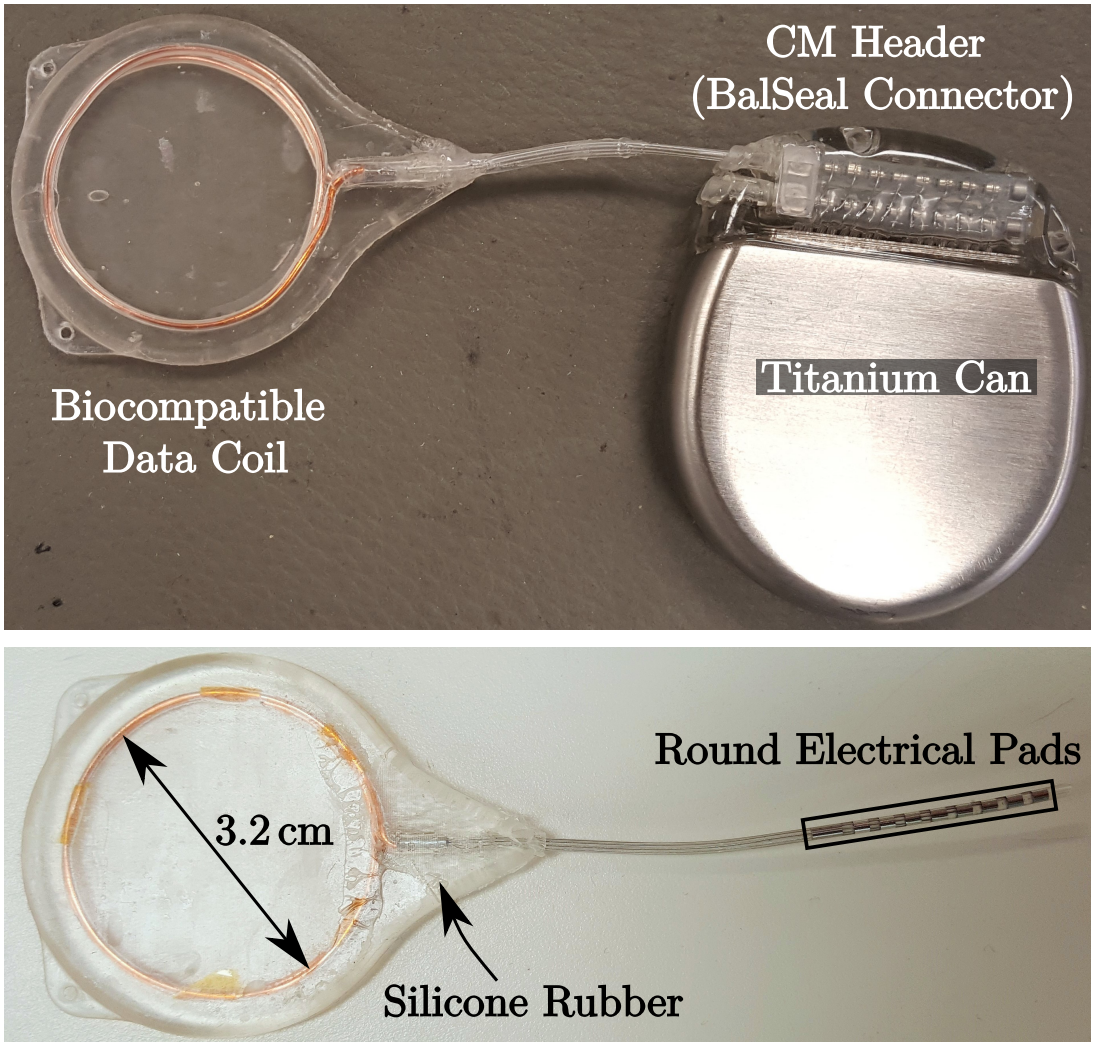


Figure 3.5: Data coil for control module (CM).

The data coil in CM has a similar structure to the ERM coil with a slightly larger diameter of 3.2 cm (Fig. 3.5). The coil is connected to the CM board through a BalSeal connector and coated with implantable-grade silicone rubber. Aside from properties of bio-compatibility and hermiticity, the coating is an intermediate layer to the high dielectric constant of the body, as we now explain.

Although the coils are coupled by magnetic fields so that essentially magnetic permeability matters, the electrical permittivity in the close vicinity of the coil defines the parasitic parallel capacitor to the coil and therefore its self-resonance frequency. The permittivity in biological tissues is very large compared to the free space permittivity (as high as 230 at

$\sim 30\,\mathrm{MHz}$) [60, 59]. Nonetheless, silicone rubber has a dielectric permittivity of $3 \sim 4$ [106], and as a thick coating it partly mitigates excessive lowering of the self-resonance frequency.

The quality factor and the inductance of the bio-compatible coil are measured with a Q-meter. At the operating frequency of the data link, 35 MHz, the coil has a quality factor of 39 and an inductance of about 340 nH[1]. The main reason for poorer Q is the high resistivity of the cable used to connect the coil to the CM. Since this cable was designed to handle low frequency signals only ($\sim$ 10s kHz), the high-frequency skin and proximity effects raise its resistance significantly.

The CM has been tested successfully for both downlink and uplink. Fig. 3.6 shows the test setup for link characterization for downlink. In the test, a pseudo-random data stream is transmitted from the development board to the CM through the inductive link. As seen on the oscilloscope screen, the waveform at the top is the transmitted data that modulates the oscillator in the external transceiver, and the waveform at the bottom is the received (reconstructed) data in the implant. The coil's Q degradation from more than 200 to less than 40 causes the operational range of the link to drop from about 5 cm to 3 cm.

[1]The quality factor, Q, of the coil alone at 35 MHz is more than 200.

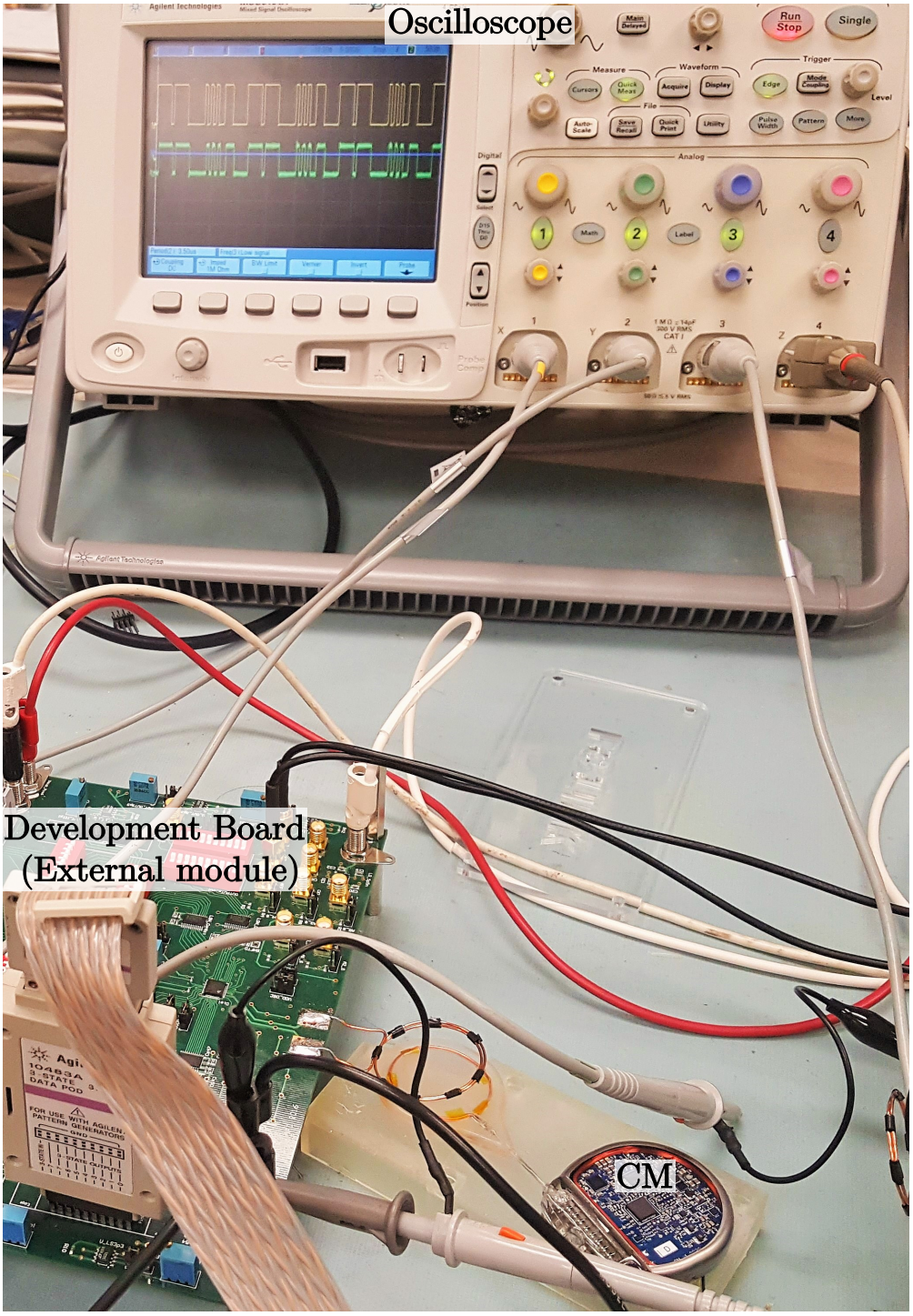


Figure 3.6: Test setup: testing CM with a development board that contains an external transceiver chip.

CHAPTER 4

MAC Layer Design and Implementation

4.1 Motivation

During the integration phase, we first used microcontrollers to implement the MAC layer for the near-field transceivers. However, we faced difficulties in implementing some of the MAC layer's inner blocks. After implementing it completely, we achieved a lower net data rate than expected. We conclude that an MCU is not an appropriate platform for realizing the MAC layer, and that it is necessary to dedicate specialized hardware to this task.

The MCU is responsible for handling several simultaneous tasks including, but not limited to, controlling all the blocks in the implant (CM, AM and NMs) and running the closed-loop algorithm, which altogether requires a significant amount of computation. Considering particularly the medical criticality of these tasks and the MCU's sequential scheduling, it may not be able to check the PHY layer frequently enough to handle incoming and outgoing data.

Furthermore, MCUs are general-purpose computation cores that are not optimized to perform the tasks in the MAC layer. Functions that may be trivial to implement in FPGA or ASIC, can be difficult in microcontrollers because of limitations of their specific instruction sets.

In conclusion, it is required to design hardware that can process data in parallel while consuming relatively low power. In this work, we implement the MAC layer as a stand-alone hardware accelerator on an FPGA platform (Xilinx Spartan-6). In the next generation of the data-link, the design might migrate to an ASIC to lower the power consumption and the system's form-factor.

Figure 4.1: Data packet structure.

Figure 4.2: Data burst structure.

4.2 Protocol Design

In order to transfer data between the implant and the external module (ERM), data packets are defined to contain 256 bytes of data payload (320 bytes of coded data, see Section 4.3.3). This chosen length of payload provides an optimal compromise between the relative packet overhead and packet error rate (PER[1]). Fig. 4.1 shows the structure of a data packet. Each packet consists of a specific header which is a unique codon and indicates the type of the packet, a payload, and a CRC check value (see Section 4.3.4).

The data link separates uplink and downlink signals based on a time-based scheme, known as time-division duplex (TDD) where different time slots at the same frequency band are adaptively allocated to each transmission direction [107]. Since the data link is asymmetric, this duplexing scheme can reduce the power consumption by dynamically mixing the reverse and forward traffics[2] and turning on only the transmitter and the receiver which are in use.

Fig. 4.2 shows the structure of a data burst which is a frame of multiple consecutive data packets that are sent in one direction. As the first block of the data burst, a synchronization preamble is sent whereby the CDR loop at the receiver can adjust the frequency and phase of the data sampling. At the end of the burst a terminating trailer appears which similar to packet headers, is a unique codon (does not appear in the 8b/10b coded data). A terminating trailer may imply a request for either changing the communication direction ("Mode Change"), or terminating the communication and going into an idle mode ("End Comm.").

[1]For a given bit error rate, the longer the packet, the higher the packet error rate: $PER \approx BER \times L_{packet}$.

[2]By allocating more time slots (higher capacity) to the direction (i.e. uplink or downlink) which has more data to transfer.

Fig. 4.3 shows the time scheme of the data communication in the link. The external module (ERM) acts as the master device in this point-to-point communication. To initiate the communication, the external module sends a wake-up signal to the internal module (implant) [108, 109, 110] and later transmits the first data burst (containing a synchronization preamble, N_1 data packets and a terminating trailer (in this case, "Mode Change")). Once the internal module receives the request for changing mode, it becomes the transmitter and sends back a data burst to the external module. The link will continue transferring data between the two sides and switching the communication direction (i.e. reverse and forward) until the external module, the master device, send an "End Comm." message in the terminating trailer. Afterwards both sides enter an idle mode to save power and remain in this mode until the external module initiates the communication again by sending a wake-up signal.

4.3 Architecture

Fig. 4.4 shows the architecture and building blocks of the MAC layer that is designed and implemented in this work. As can be seen, the MAC layer sits between the physical layer (i.e. the near-field transceiver, see Chapter 2) and the application layer or the master device (e.g. an MCU or a PC terminal). In this setup, the MAC layer is the slave device in the SPI communication [111]. In the following subsections, we discuss the internal structure of each building block.

4.3.1 SPI Slave

SPI (Serial Peripheral Interface) is a widely used synchronous serial interface in embedded systems developed by Motorola in the mid 1980s [111]. This interface offers a full-duplex communication in a master-slave setup on four signal lines:

- serial clock (SCLK)
- slave select ($\overline{SS}$)

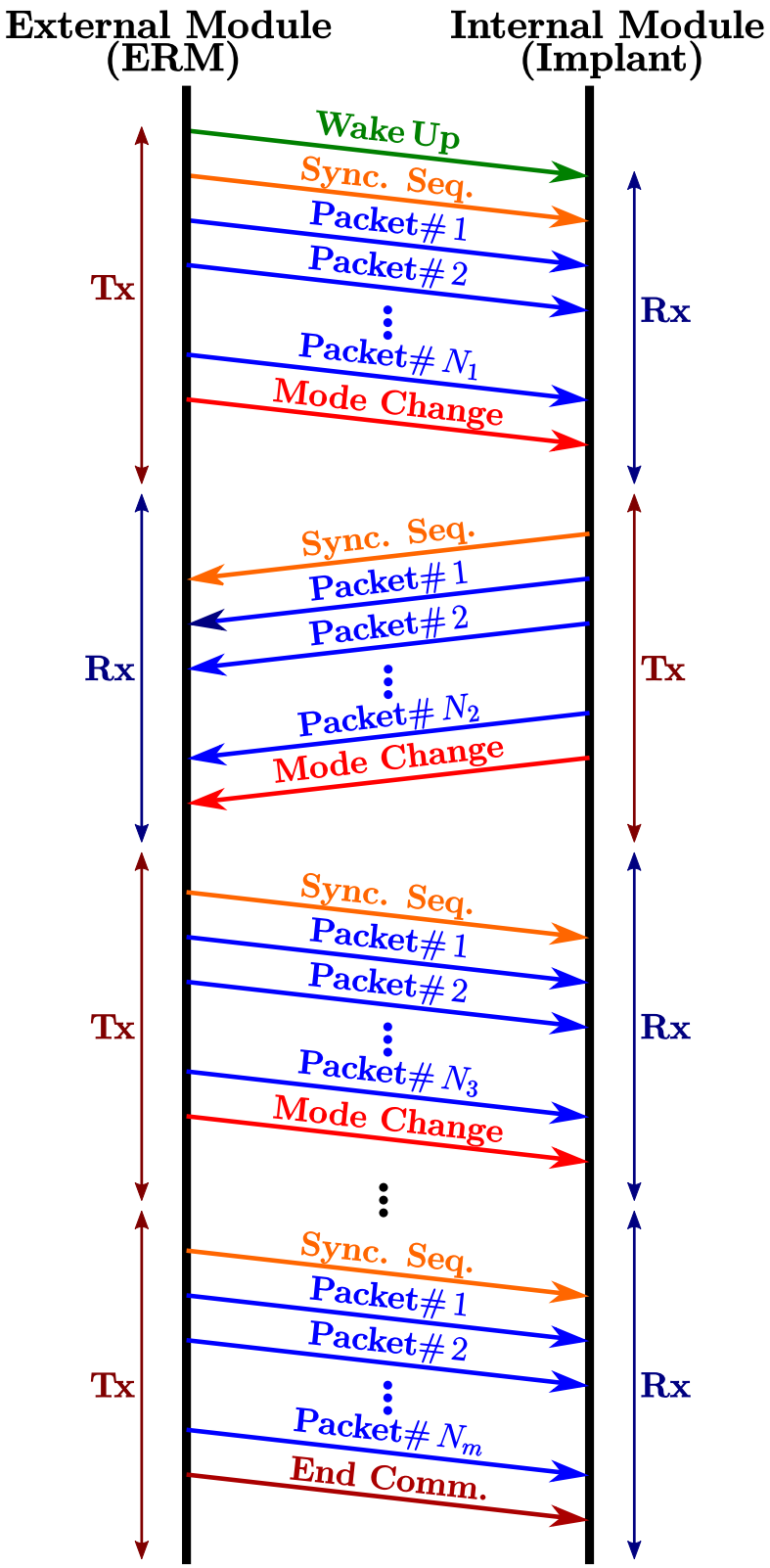


Figure 4.3: The time scheme of data transmission (Tx) and reception (Rx).

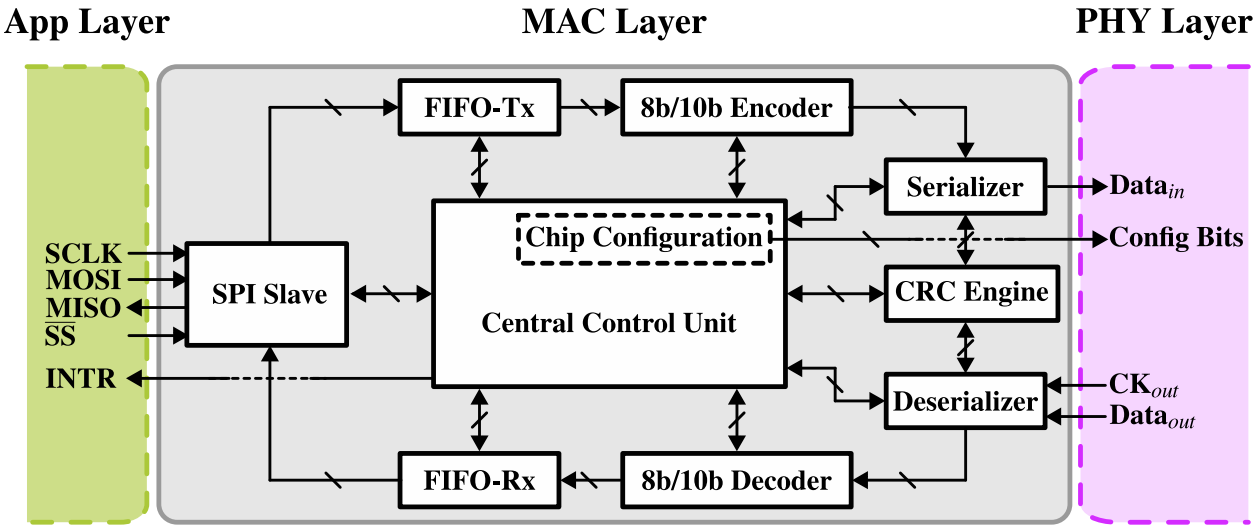


Figure 4.4: MAC layer architecture.

- master-out-slave-in (MOSI)
- master-in-slave-out (MISO)

Through the interface, the application layer (in this case an MCU) may send commands and data to the MAC layer (slave device), or receive the system status and the data. When the application layer starts communication with the MAC layer, it activates the SS signal line and sends out the clock signal (SCLK). While the application layer is transmitting 8-bit commands on MOSI line (Table 4.1), the MAC layer sends back, on MISO line, an 8-bit message about its status including the mode of operation (idle, transmit, receive and automatic modes), direction of communication (transmitting or receiving) and status of the FIFOs (full or empty).

When the SPI slave receives a command, it sends that to the CCU (central control unit) in order to be interpreted[3]. If the command contains data (i.e. "WRITE" command), the SPI block passes it to the FIFO-Tx and if the command is "READ", the 256-byte data payload of the first successfully received packet will be sent on the MISO line to the application layer (or master device).

[3] As can be understood from Table 4.1, the first four bits of an 8-bit command are sufficient for command interpretation in the CCU.

Table 4.1: Commands list for SPI slave.

Command Name	Command Bits	Implication
NOP	11110000	No operation (Obtains an update on the system status)
SLEEP	00001111	Makes the system go into the idle mode
TRANSMIT	11001010	Makes the system go into the transmit mode (For testing and debugging purposes)
RECEIVE	00110101	Makes the system go into the receive mode (For testing and debugging purposes)
WRITE	10101000	Writes a data payload into FIFO-Tx buffer
READ	10010001	Reads a received data payload from FIFO-Rx buffer
AUTO	10001011	Makes the system go into the automatic mode (The main communication command)

In addition to the four SPI lines between the application layer and the MAC layer, an interrupt line informs the application layer that the MAC layer needs attention. This avoids frequent checking upon the MAC layer by the application layer.

4.3.2 FIFO Data Buffers

There are two FIFOs in the MAC layer: one is located in the transmit path (FIFO-Tx) and the other in the receive path (FIFO-Rx). They store the payloads (256 bytes). FIFOs are responsible to receive the payloads byte-by-byte (8-bit input) from a preceding block in the path (SPI slave port in transmit path or 8b/10b decoder in receive path), store them and send them byte-by-byte (8bit output) to a following block (8b/10 encoder in transmit path or SPI slave port in receive path) at its request.

Each FIFO consists of three sub-blocks:

- a 256-byte shift register: to receive the payload from the preceding block,
- a stack of 3×256B memory cells: to store 3 data payloads,
- a 256B-to-1B multiplexer: select 1 byte to be sent to the following block.

All the sub-blocks in the FIFOs are controlled by the CCU.

4.3.3 8b/10b Encoder and Decoder

To recover clock and data in receivers successfully, the data stream should contain enough state transitions [97]. Otherwise lack of data transitions (long runs of '1's or '0's) may cause the oscillator (DCO, see Section 2.11.3) in the CDR loop to drift, generating jitter and therefore raising the error rate. To mitigate this, the data stream can be encoded. In our system, we use 8b/10b [112, 113] coding which not only assure sufficient data transitions (maximum run length of 5 bits), but also achieve DC-balance, a crucial feature for adaptive thresholding in the receiver analog front-end (adaptive bias loop in the AFE, see Section 2.11.2).

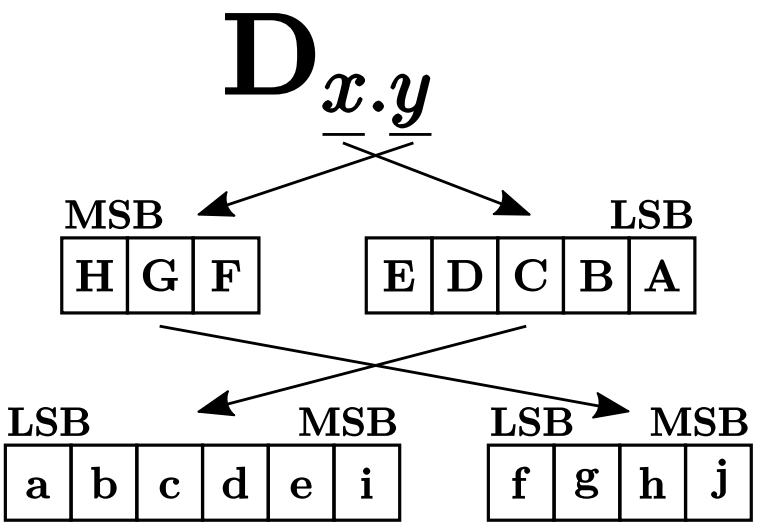


Figure 4.5: 8b/10b coding scheme.

8b/10b coding converts an 8-bit sequence to a 10-bit symbol by first splitting each byte to two sets of 3 bits (HGF) and 5 bits (EDCBA) and then mapping them to 4-bit (fghj) and 6-bit (abcdei) words, respectively, based on predefined look-up tables (Fig.4.5).

To achieve DC-balance, this coding employs the concept of running disparity (RD) which is the difference between the counts of '1's and '0's. Fig. 4.6 shows the running disparity state machine [114]. As can be seen, the transmitter starts encoding while assuming the running disparity to be RD-. The RD sign does not change if the symbol is disparity-neutral (equal numbers of '1's and '0's), otherwise the RD sign will reverse. Thereby, the difference between the counts of '1's and '0's will remain small[4] and the data stream will be DC-free in the long run.

Although this coding offers the DC-balance feature and allows clock recovery in the receivers, it comes at a cost of 25% overhead: if the air data rate is 2 Mbps, the best achievable net data rate will be 1.6 Mbps. However, this overhead is still smaller than other DC-balance methods such as Manchester coding.

In the MAC layer implementation, the 8b/10b encoder and decoder contain the conversion look-up tables and the disparity state machine.

[4]Less than two in a sequence of 20 bits.

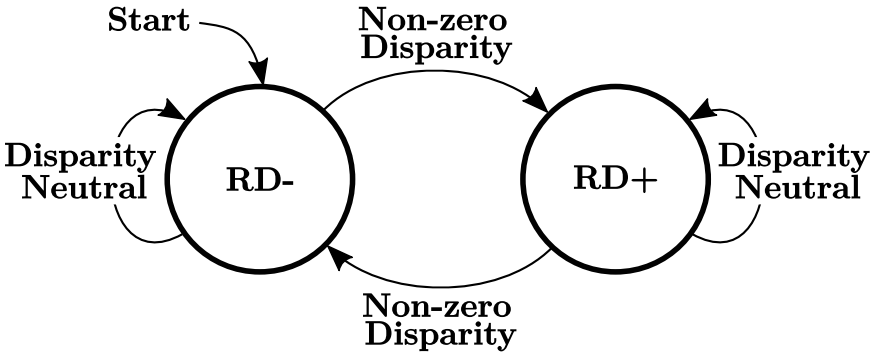


Figure 4.6: Running disparity selection mechanism.

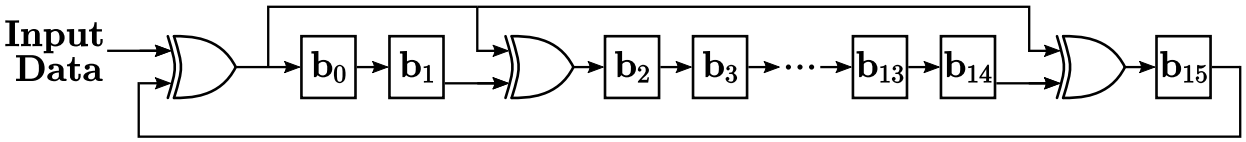


Figure 4.7: CRC checksum calculation; polynomial division scheme.

4.3.4 CRC Engine

CRC (Cyclic Redundancy Check) is a widely used error detecting code in communication networks[5] which has a simple implementation in digital hardware platforms, and therefore is suitable for our system [107, 116].

By entering the CRC engine, the data payloads obtain check values (checksums) that are the coefficients of the remainder polynomial calculated based on a long polynomial division. The divisor in this polynomial division is known as generator polynomial whose highest degree term generally determines the error detection strength. In our design, we use CRC-16-IBM which has a generator polynomial of $X^{16} + X^{15} + X^2 + 1$. Fig. 4.7 shows the CRC polynomial division implementation with exclusive-OR gates (XOR) and shift registers.

After passing the payload through the polynomial division and finding the remainder coefficients, the transmitter attaches the CRC check value, a binary representation of the remainder polynomial coefficients, to the end of the data payload. On the other side of the data link, the receiver uses the same 16th order generator polynomial to find the remainder of

[5]CRC code is usually employed in low-noise channels than can be modeled as binary symmetric channels (BSC's) with an error rate of less than 10^{-4} [115].

the received payload, and detects an error if the remainder does not match with the received check value.

In this prototype of the MAC layer, the packets with errors are discarded and the master device is informed. If required, retransmissions can be scheduled by the master device.

4.3.5 Serializer and Deserializer

The serializer and the deserializer in the MAC layer interface with the PHY layer directly and perform parallel-to-serial and serial-to-parallel conversions, respectively. In addition, the serializer adds proper header, trailer and CRC check values to the data payloads. However, the main task for the deserializer is data parsing for packet detection (based on the packet headers or the burst trailer) and sending the payload to the 8b/10b decoder (10 bits by 10 bits in parallel).

4.3.6 Central Control Unit

In the designed MAC layer, all the above-mentioned blocks are connected to and controlled by a core block called the Central Control Unit (CCU). This block organizes and assigns the tasks to the other peripheral blocks, interprets the received commands from the application layer (through the SPI port, see Fig. 4.4), and configure the transceiver chip (PHY layer) into different modes of operation.

For each peripheral block, the CCU has at least one state machine for task scheduling. However, to illustrate the MAC layer's top-level control mechanism, we take a look at the two main CCU's state machines shown in Fig. 4.8 and Fig. 4.9 which govern the external and internal (implanted) transceivers, respectively.

The two state machines will be activated if the application layers plan to run the MAC layers in "automatic mode", and therefore send "AUTO" command (see Table 4.1) to the MAC layers. On receipt, the MAC layers come out of their idle mode (IDLE), and wait for a wake-up signal which can be issued from the external module. As mentioned before, the external module is the master in the wireless communication. In this prototype, we are

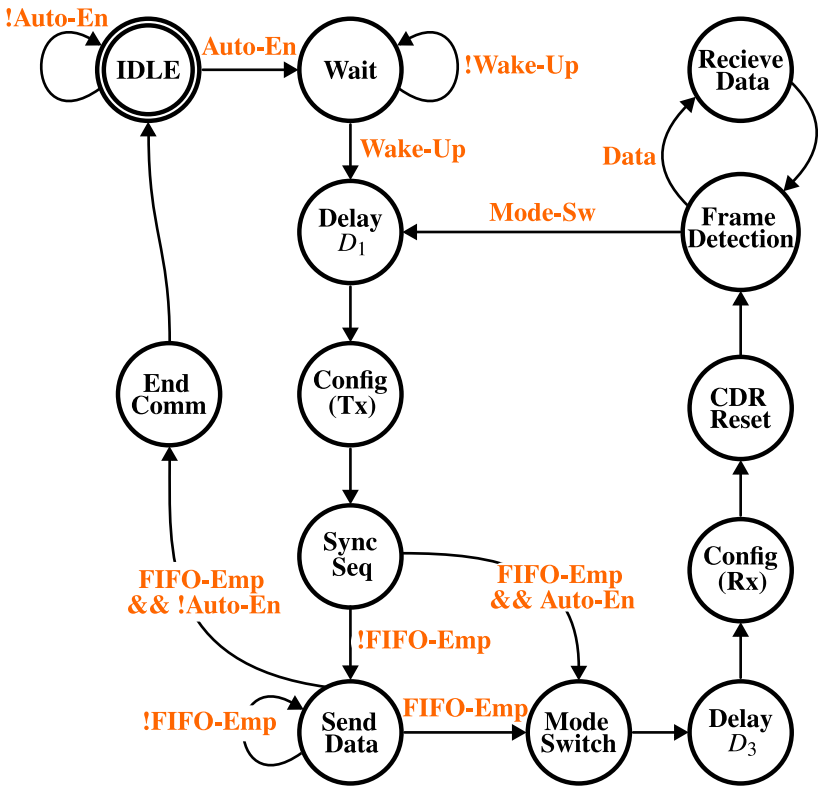


Figure 4.8: The finite state machine in the external transceiver's MAC layer.

assuming the wake-up signal can be sent through a secondary link, for instance, a wireless power transfer link[6].

As shown in Fig. 4.8 and Fig. 4.9, when the wake-up signal is detected, the two state machines enter loops of states which realize an automatic control of a bidirectional communication. The delays D_1, D_2, D_3 and D_4 are embedded in the loops to synchronize the two loops[7].

Since in the data link the external transceiver is the master, it starts the communication as the transmitter (Config(Tx)) by sending a synchronization preamble (Sync Seq). On the other side, the internal transceiver configured as the receiver (Config(Rx)) initializes its

[6]This is the same wake-up mechanism that is being used in the current design of the CM (see Chapter 3).

[7]If the propagation delay of the wake-up signal through the power link is significant, D_1 and D_2 may need to be split to two parts: one of which is located out of the loop compensating the wake-up propagation delay difference between the two sides (the external transceiver receives it directly from the master device on the ERM, however the internal transceiver receives it through the secondary link), and the other is embedded in the loop adjusting the systematic execution time difference in the two loops.

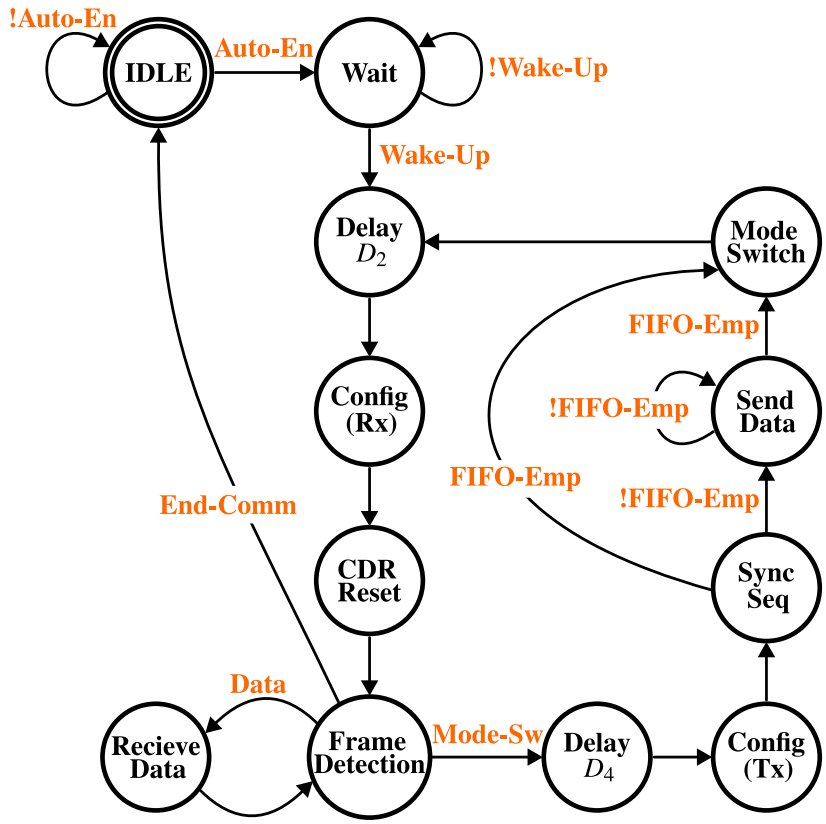


Figure 4.9: The finite state machine in the internal transceiver's MAC layer.

CDR loop (CDR Reset) and then begins to search for the packets (Frame Detection) in the received data. If the FIFO-Tx contains any payloads (FIFO-Emp is low), the external transceiver will start sending binary data (Send Data) and after detecting the data header in the incoming stream, the internal transceiver receives the data (Receive Data). This may continue until the external module, with the data burst trailer, asks for communication direction to be reversed (Mode Switch) or terminated (End Comm). If the external module requests for change in the communication direction, the two sides will enter the second half of the state machine loops where the external module acts as a receiver and the internal module becomes the transmitter. When terminating communication, both sides will go to idle mode (IDLE) and wait for the "AUTO" command (Auto-En) to be issued again by the application layer.

In case a secondary link does not exist or cannot deliver the wake-up signal, two other approaches may be taken to wake up the internal module. One way is to use the internal

transceiver's analog front-end (AFE, see Section 2.11.2) as a power detector for checking the presence of the in-band wake-up signal. For this approach, the adaptive bias loop in the AFE circuit is deactivated and instead, a constant voltage level corresponding to the wake-up signal strength biases the rectifier.

Another method is to employ frequency detection while the AFE is working (idle listening [117, 118]). This requires the external transceiver to send the same synchronization preamble for waking up the internal transceiver. A simple digital frequency estimation loop that over-samples the output of the AFE can measure the frequency of the binary sequence pattern ('1010' pattern of the synchronization preamble) and thereby activate other blocks in the internal module so as to receive the first incoming burst of data.

4.4 Implementation

A prototype of the designed MAC layer has been implemented on an FPGA platform (Fig. 4.10). We selected XC6SLX45 model from the Xilinx Spartan-6 series which contains about 6,800 slices implying that it has about 44,000 logic cells and 55,000 registers. The MAC layer implementation takes up 80% of the slices (i.e. the logic cells), and 50% of the registers. Although the FPGA is driven at a master clock frequency of 12 MHz, most of the MAC layer's blocks clock at 2 MHz.

The MAC layers of the external and internal modules were implemented on two separate FPGA boards each of which was programmed through the USB port. The FPGA boards were connected to the external and internal boards through their GPIO pins. The application layers (or master devices) can control the MAC layers on the FPGAs and exchange data payload through the defined SPI ports (on the FPGA GPIO pins).

4.5 Measurement

To test the MAC layer in presence of the PHY layer (with over-the-air hardware), as shown in Fig. 4.11, each of the external and internal transceiver development PCBs is connected

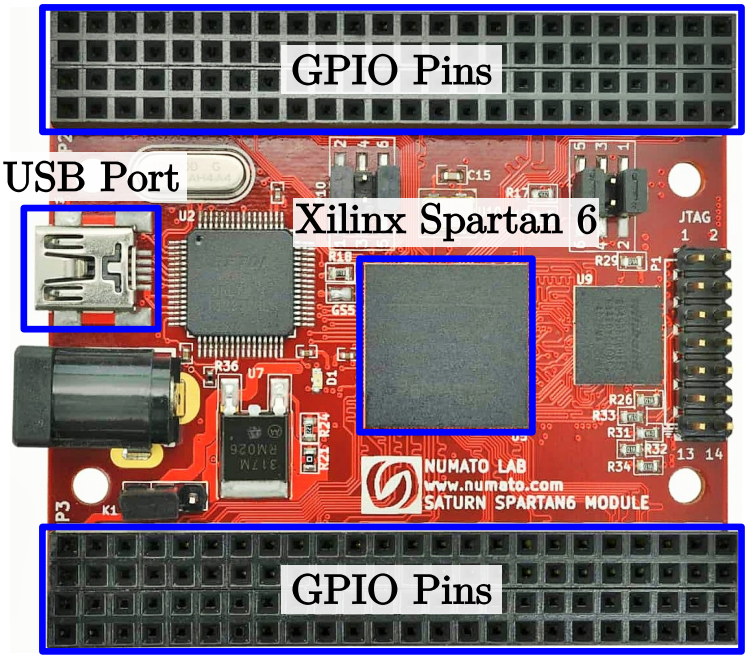


Figure 4.10: The MAC layer is implemented on a Xilinx Spartan 6 FPGA development board (Saturn by Numato Systems [7]).

to an FPGA board where the MAC layer is implemented. A tertiary FPGA board controls the MAC layer through their SPI ports by the commands shown in Table 4.1. This FPGA board emulates the the master devices (application layers) on the two sides of our wireless link. For that, a very simple FPGA from Xilinx Spartan-3 series (XC3S50A) has been used.

Fig. 4.12 shows the actual test setup. The digital inputs and outputs of the MAC layers were captured using a USB logic analyzer. The captured waveforms are shown in Fig. 4.13. The first eight waveforms at the top belong to the MAC layer in the internal module, and the remaining eight waveforms at the bottom are for the MAC layer in the external module.

The MOSI lines (i.e. MOSI_{Int} and MOSI_{Ext}) carry the commands and data which are sent to the MAC layers on the two FPGA boards. As can be seen, at the beginning two packets are sent to each of the MAC layers through their SPI ports, and then the communication command ("AUTO") is issued (see time-slot ① in Fig. 4.13). After receiving the wake-up signal, the MAC layers configure the external and internal modules (PHY layer) through the CNFG lines (configuration shift register) as the transmitter (Tx) and the receiver (Rx), respectively (as labeled in time-slot ② in Fig. 4.13). As the master device in the data link, the

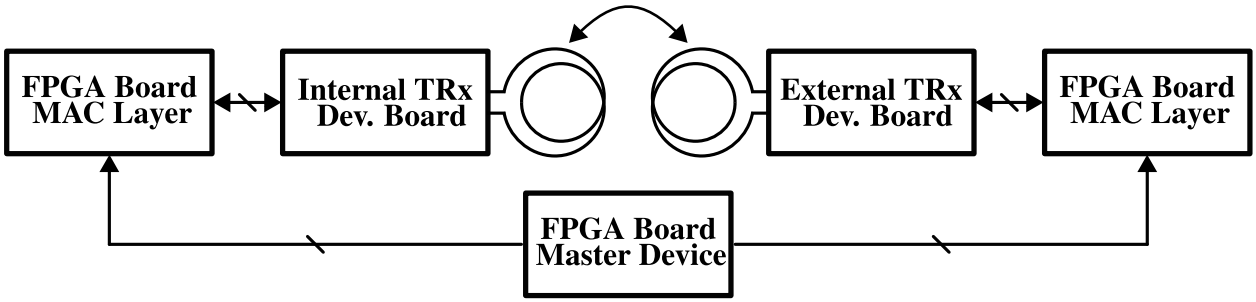


Figure 4.11: While the two development boards are communicating through the inductive link, the MAC layers on the two FPGA boards govern all the the communication tasks. The MAC layers are controlled by a tertiary FPGA board which emulates the two master devices on the two sides.

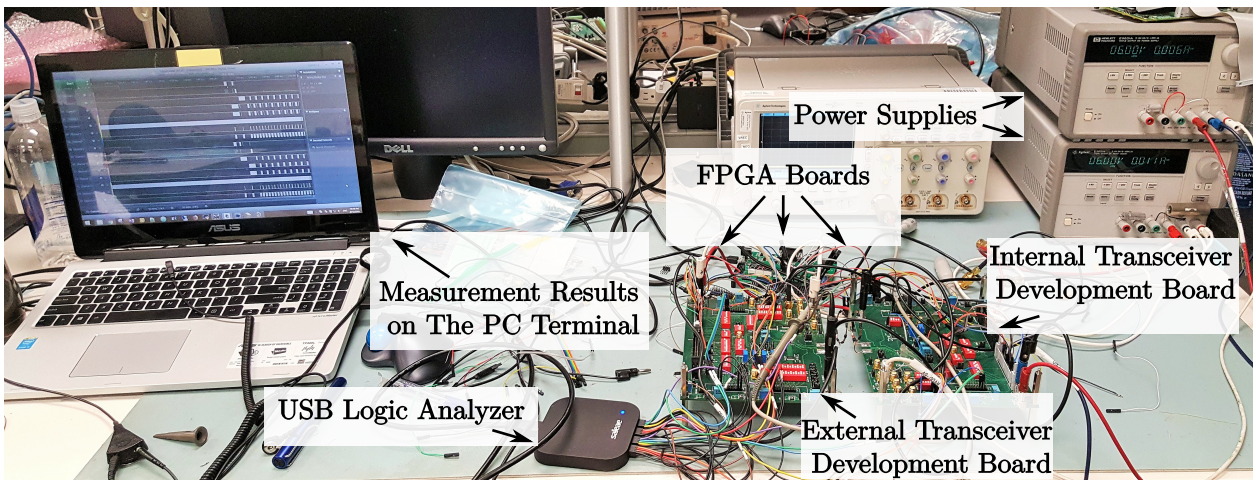


Figure 4.12: The test setup for characterization of the MAC layers.

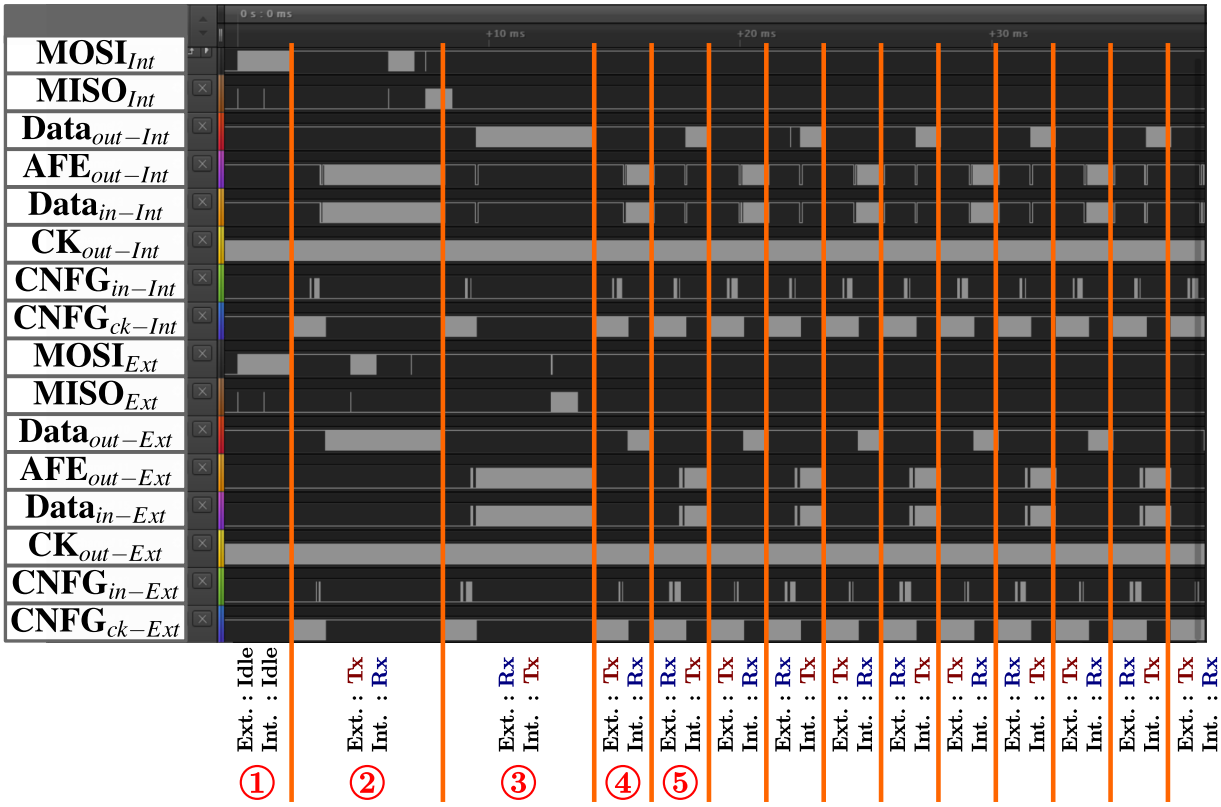


Figure 4.13: The captured waveforms of the digital inputs and outputs of the MAC layers. The waveforms are also annotated with explanatory notes on the modes of operation (Ext. : External module, Int.: Internal module, Rx: Receiving, Tx: Transmitting) and the time-slot numbers (e.g. ①, ②, etc.).

external module starts transmitting data (see $\text{Data}_{out-Ext}$ line in time-slot ② in Fig. 4.13). $\text{AFE}_{out-Int}$ and Data_{in-Int} are the analog front-end (AFE) output and the reconstructed data by the CDR loop in the internal module. After sending all the packets stored in the FIFO-Tx, the external module sends a "Mode Change" message and the communication direction reverses. After that, in the next time slot, the internal module acts as the transmitter and the external module receives the data on the other end (as labeled in time-slot ③ in Fig. 4.13). Once this transmission is completed, as shown in Fig. 4.13 (see time-slots ④ and ⑤), the link keeps swapping the communication direction without transferring any data payload until either side has data to send or the external module terminates the communication by sending an "End Comm." message.

To show that the MAC layer is capable of parallel processing, two other data payloads were sent (one for each side) on the SPI ports (see Fig. 4.13; on MOSI_{Int} and MOSI_{Ext} lines in time-slot ②), and as can be seen, while the communication was happening, no pause appeared for processing this task. The master FPGA board later requested the MAC layers of the internal and external modules to send out one of the data payloads that they have received successfully, and it is clear that the MAC layers handled this task with no pause while in parallel the data communication was occurring (see Fig. 4.13; on MISO_{Int} line in time-slot ②, and on MISO_{Ext} line in time-slot ③).

CHAPTER 5

Conclusion

5.1 Research Contributions

The dissertation describes a distance-immune, energy-efficient, inductively-coupled data link that can be used in next-generation human-quality biomedical implants. The main contributions of this research are as follows:

- A design-oriented analysis on the inductively-coupled link has been presented in Chapter 2. It leads to the fundamental constraints and features of the inductive link driven with a free-running oscillator (i.e. modulation index, logic inversion, frequency shift, etc.) enables comparison with a typical link driven at a fixed frequency. The main three findings that merit are as follows:
  - The link driven with a free-running oscillator is superior both in terms of *downlink robustness* and *uplink modulation index*.
  - With the *immunity to distance variation* and using *load modulation*, a very low power, yet robust data link can be achieved.
  - With proper selection of resistor value on secondary (R_2), using a resistor bank, the *range of the data link can be expanded*.
- This work has demonstrated near-field transceiver chips fabricated in 40 nm CMOS capable of transferring data at up to 4 Mbps and 2 Mbps in half-duplex with an LSK uplink and ASK downlink, respectively. With these transceivers, the data link can operate successfully over a separations of up to 4.5 cm with BER$< 10^{-6}$. Each transceiver occupies an active area of about 0.1 mm^2. The implanted transceiver consumes merely

0.3 μW when transmitting binary data at 4 Mbps (0.075 pJ/bit), and 10 μW when receiving data at 2 Mbps (5 pJ/bit). This is the lowest reported energy consumption per bit so far for wireless near-field data transmission ($\sim$ 125 X improvement). Also, this data link improves the normalized range by roughly 40% over the state-of-the-art.

- We have described the integration of the data link within an implantable human-quality neuromodulation system. The system's wireless communication performance has been verified with bench-top and *in-vitro* tests in which the data link establishes a robust communication over a separation of 3 cm when the CM is packaged in a titanium can and is using a low-quality-factor bio-compatible coil.

- A MAC layer suitable for the designed transceivers (PHY layer) has been defined and implemented as a hardware accelerator on an FPGA platform. This MAC hardware is able to process incoming and outgoing data in parallel fashion. This design can easily migrate to an ASIC platform which may shrink the system's power consumption and form-factor—two key features in biomedical implants.

5.2 Future Work

Areas for future work include:

- The coupled resonators analyzed in Section 2.4 and used in the data link, are parallel RLC circuits. However, in general, inductive data links may have series resonators on one or both sides of the link. It would be useful to develop a similar design-oriented analysis for these different combinations and explore their key potentials and constraints for this application.

- We have assumed that most of the time the implant sends data to the external module (uplink), but the external module may transmit back configuration data towards the implant (downlink) only infrequently. Therefore, the data link has not been well designed for very frequent changes in the communication direction. In case the data link

needs to have a fast direction turn-over, the CDR loop may need to be further refined and optimized:

  - To reduce the lock time (and consequently the power consumption), it would be wise to store the DCO's input frequency word after the reception of the first burst. The saved frequency word can be reused as the initial word value of the DCO's input register and, in this way, the frequency detection period, constituting most of the long synchronization preamble (256 bytes), can be eliminated from the next data bursts.
  - To minimize the lock time, a loop filter with a variable bandwidth can be used. This is know as "gear shifting". At the beginning, the loop bandwidth can relatively wide to accelerate the phase locking process, and later the bandwidth may be reduced back to its optimum value to minimize the jitter at the output of the loop.

- To avoid idle-listening and reduce the power consumption, an extremely low-power low-data-rate wake-up receiver can be added to the implant's transceiver chip [119, 120]. The wake-up receiver will turn on the implant's near-field transceiver when the external module is present.

- Much will be learned by placing the wireless link in an *in-vivo* setup. This will require surgical insertion of the CM inside an alive animal and measurement of the BER over different coil separations.

- To reduce the system power consumption, its form-factor and the surgery complications, it would be better to, instead of having three separate implantable modules (NM, AM, and CM), integrate all of them into one implantable piece which can be surgically placed on top of the patient's head under the scalp.

- To reduce the implant size further, it would be helpful to replace the titanium can with a non-metallic medically-grade silicone-based enclosure. Two concentric circular coils can be used (one for the power transfer link and the other for the data telemetry link)

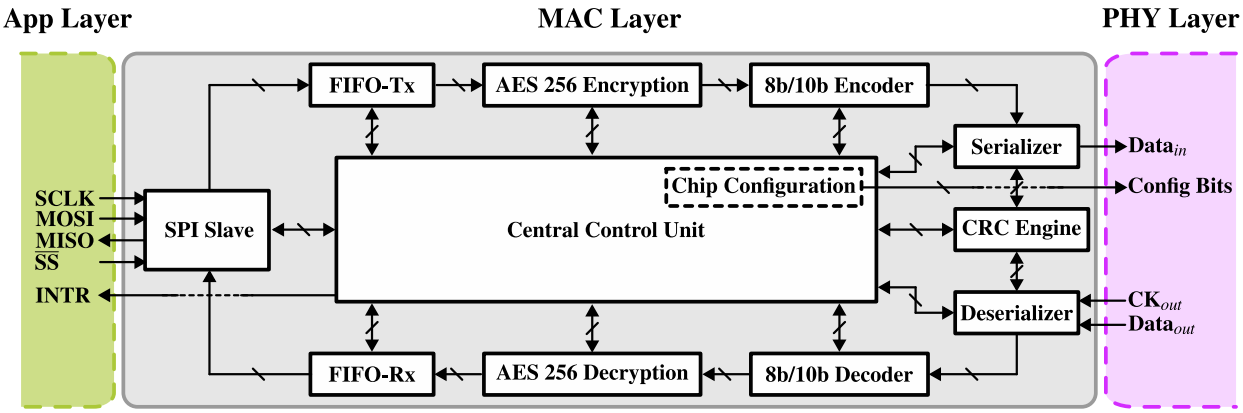


Figure 5.1: Addition of AES-256 coding blocks to the proposed MAC layer

which are place on the top of the implant's electronics. It would be useful to investigate sharing a coil between the data and power transfer links. In this idea, the two links can share the same coil while using it over different time intervals (time-duplexing). [121] presents another bright approach for simultaneously transferring power and data over one pair of coils.

- To minimize the power and size of the next-generation implant, the proposed MAC layer should be designed as an ASIC and integrated beside the near-field transceiver circuits on one single chip.

- To enhance the security in the biomedical data telemetry, data encryption/decryption engines like AES-256 should be added to the MAC layer architecture, as shown in Fig. 5.1.

APPENDIX A

An Equivalent Circuit for Coupled Inductors

In this appendix, we would like to find an equivalent circuit for coupled inductors (Fig. A.1(a)) which is convenient to be used in the intuitive analysis presented in Section 2.7. Considering the parallel structure of the inductive link shown in Fig. 2.22(b), the circuit shown in Fig. A.1(b) can be a good candidate to be used in the analysis as the equivalent circuit[1]. The parameters value in the equivalent circuit, L_a, L_b, L_c, and N_1/N_2, can be calculated by running four different tests on the coupled inductors and the desired equivalent circuit.

Test 1: Assuming $I_2 = 0$ (i.e. 2nd port is open-circuit), we calculate the driving point impedances seen at V_1:

$$Z_{11}\Big|_{I_2=0} = sL_1 \tag{A.1}$$

$$Z_{11}^{eq}\Big|_{I_2=0} = sL_a \Big|\Big| s\Big((L_b + L_c) \times \big(\frac{N_1}{N_2}\big)^2\Big) \tag{A.2}$$

Test 2: Assuming $I_1 = 0$ (i.e. 1st port is open-circuit), for the driving point impedances seen at V_2, we have:

$$Z_{22}\Big|_{I_1=0} = sL_2 \tag{A.3}$$

$$Z_{22}^{eq}\Big|_{I_1=0} = sL_c \Big|\Big| s\Big(L_b + \big(\frac{N_2}{N_1}\big)^2 L_a\Big) \tag{A.4}$$

Test 3: Assuming $V_2 = 0$ (i.e. 2nd port is short-circuit), the driving point impedances seen at V_1 can be calculated as:

$$Z_{11}\Big|_{V_2=0} = s\big(L_1 - \frac{M^2}{L_2}\big) \tag{A.5}$$

[1]We engineered the topology of the equivalent circuit shown in Fig. 2.22(b) to have two parallel magnetizing inductors which can resonate with the parallel capacitors on the two sides of the link. This makes the remaining circuit very simple and therefore convenient to analyze.

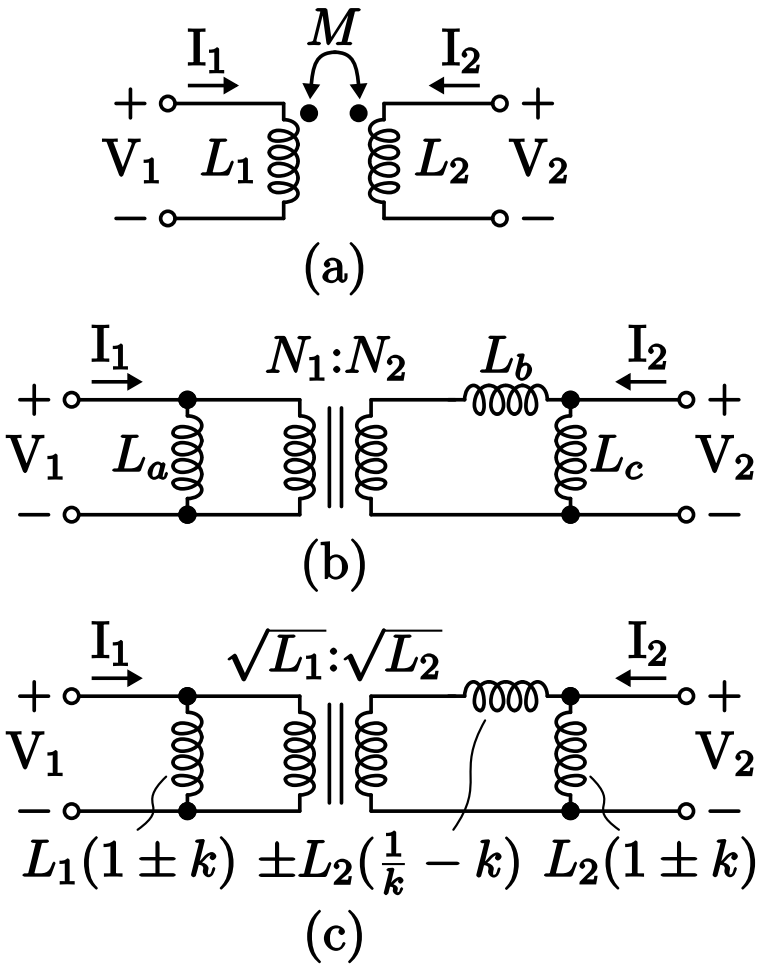


Figure A.1: Equivalent circuit for coupled inductors: (a) coupled inductors, (b) an appropriate topology for the desired equivalent circuit, (c) the equivalent circuit with its component values.

$$Z_{11}^{eq}\Big|_{V_2=0} = sL_a \| s\Big(L_b \times \big(\frac{N_1}{N_2}\big)^2\Big) \tag{A.6}$$

Test 4: Assuming $V_1 = 0$ (i.e. 1st port is short-circuit), for the driving point impedances seen at V_2, we have:

$$Z_{22}\Big|_{V_1=0} = s\big(L_2 - \frac{M^2}{L_1}\big) \tag{A.7}$$

$$Z_{22}^{eq}\Big|_{V_1=0} = sL_c \| sL_b \tag{A.8}$$

Now by equating the four pairs of the driving point impedances calculated for the two circuits (Fig. A.1(a) and Fig. A.1(b)), we obtain:

$$\begin{cases} L_1 = L_a || \Big((L_b + L_c) \times \big(\frac{N_1}{N_2}\big)^2 \Big) \\ L_2 = L_c || \Big(L_b + \big(\frac{N_2}{N_1}\big)^2 L_a \Big) \\ L_1 - \frac{M^2}{L_2} = L_a || \Big(L_b \times \big(\frac{N_1}{N_2}\big)^2 \Big) \\ L_2 - \frac{M^2}{L_1} = L_c || L_b \end{cases} \tag{A.9}$$

Since, in (A.9), we have four unknowns and three known values, the system of equations is dependent[2], and therefore one of the four parameters (L_a, L_b, L_c, and N_1/N_2) can be chosen arbitrarily as a design freedom. We chose the turns ratio N_1/N_2, as the free variable, to be[3]:

$$\frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \tag{A.10}$$

With this, (A.9) can be solved for L_a, L_b and L_c:

$$\begin{cases} L_a = L_1 \pm \sqrt{\frac{L_1}{L_2}} M \\ L_b = \pm \sqrt{\frac{L_1}{L_2}} \times \frac{L_1 L_2 - M^2}{M} \\ L_c = L_2 \pm \sqrt{\frac{L_1}{L_2}} M \end{cases} \tag{A.11}$$

If $M \triangleq k\sqrt{L_1 L_2}$, (A.11) can be written as follows:

$$\begin{cases} L_a = L_1(1 \pm k) \\ L_b = \pm L_2(\frac{1}{k} - k) \\ L_c = L_2(1 \pm k) \end{cases} \tag{A.12}$$

Fig. A.1(c) shows the equivalent circuit with its components values.

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[2]In other words, the system's coefficient matrix is not full rank.

[3]We have inspired by the mathematical analysis presented in Chapter 2 suggesting that the link can be modeled as a transformer with turns ratio of $\sqrt{L_1} : \sqrt{L_2}$ when $k > k_C$.

APPENDIX B

An Equivalent for Stacked Transistors

In this appendix, we would like to find an equivalent for the stack of two FETs used in the active rectifier of the receiver analog front-end (AFE, see Section 2.11.2, Fig. 2.29). Here, we suppose that the two FET devices have the same size (i.e. $(W/L) = (W/L)_{M_1} = (W/L)_{M_3}$) and the same threshold voltage (i.e. $V_t = V_{t,M_1} = V_{t,M_3}$). Also, we neglect the transistors' body effect.

For the stack of devices shown in Fig. B.1(a), assuming both the transistors are operating in saturation region, we can write:

$$V_X = V_{GS,3} = V_t + \sqrt{\frac{2I'_1}{\beta}} \tag{B.1}$$

$$V_{GS,1} = V_{in} - V_X \simeq V_t + \sqrt{\frac{2I'_1}{\beta}} \tag{B.2}$$

where $\beta = \mu_n C_{ox}(W/L)$. Adding (B.1) and (B.2) together, V_{in} can be calculated as:

$$V_{in} = V_{GS,1} + V_{GS,3} = 2V_t + 2\sqrt{\frac{2I'_1}{\beta}} \tag{B.3}$$

With this, I'_1 can be calculated in terms of V_{in}:

$$I'_1 = \frac{1}{2}\left(\frac{\beta}{4}\right)(V_{in} - 2V_t)^2 \tag{B.4}$$

Since V_{in} is the gate-source voltage of the equivalent transistor, $V'_{GS,1}$ (Fig. B.1(b)), (B.4) can be interpreted as the current equation for the equivalent device:

$$I'_1 = \frac{\beta'}{2}(V'_{GS,1} - V'_t)^2 = \frac{1}{2}\left(\frac{\beta}{4}\right)(V_{in} - 2V_t)^2 \tag{B.5}$$

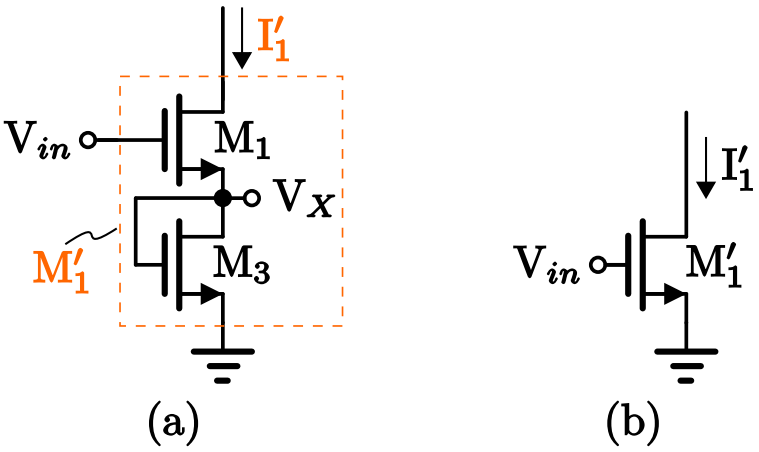

Figure B.1: Finding an equivalent transistor for a stack of two FETs

With this, we conclude that the stack of two FETs can be modeled as an equivalent FET whose threshold voltage and size are, respectively, twice and 1/4th of each transistor threshold voltage and size:

$$V_{t,M_1'} = V_t' = 2V_t = 2 \times V_{t,M_1} \tag{B.6}$$

$$\beta' = \frac{\beta}{4} \tag{B.7}$$

or equivalently:

$$(W/L)_{M_1'} = (W/L)_1' = \frac{1}{4}(W/L) = \frac{1}{4} \times (W/L)_{M_1} \tag{B.8}$$

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