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A 500-A/48-to-1-V Switching Bus Converter: A Hybrid Switched-Capacitor Voltage Regulator with 94.7% Peak Efficiency and 464-W/in^3 Power Density

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***Abstract*—This paper proposes an efficient and compact hybrid switched-capacitor (SC) converter for direct 48-to-1-V power conversion in data centers. The proposed topology can be viewed as a 2-to-1 SC converter merged with two 8-to-1 series-capacitor-buck (SCB) modules through two switching buses. Different from the conventional DC bus architecture, the switching bus architecture removes the bulky DC bus capacitors and reduces the number of switches. Compared with existing 48-to-1-V hybrid SC demonstrations, the proposed converter achieves the highest SC stage conversion ratio with the lowest normalized switch volt-ampere (VA) rating, which promises lightened conversion burden on the following buck stage and reduced switch stress. A hardware prototype is designed, constructed and tested up to 500-A output current, achieving 94.7% peak power stage efficiency, 86.4% full-load efficiency and 464-W/in^3 power density.**

I. Introduction

Data center electricity consumption is forecast to grow rapidly in the next decade and account for up to 13% of global electricity demand by 2030 [1]. As such, it is imperative to develop more energy-efficient and power-dense solutions for data center power delivery. As modern data centers shift towards the 48-V bus architecture, point-of-load (PoL) converters with a high step-down ratio (e.g., 48-to-1) and voltage regulation capability are needed to provide the low voltage ($\leqslant$ 1.0 V) and high current ($\geqslant$ 100 A) required by power-hungry microprocessors (e.g., CPUs, GPUs, ASICs, etc.).

The main challenges of 48-V-to-PoL power conversion include: i) high conversion ratio, ii) high output current, iii) high efficiency, iv) high power density, and v) fast dynamic response. Various solutions have been proposed to address these challenges, and they can be classified into two categories: 1) transformer-based solutions [2]–[6], and 2) hybrid switched-capacitor (SC) solutions [7]–[14]. In transformer-based solutions, highly optimized LLC converters are used for efficient fixed-ratio conversions, combined with an upstream buck-boost module [2], a multi-phase buck converter [3], a series-stacked buck converter with partial power processing [4], [5], or a multiphase current doubler rectifier [6] for output voltage regulation. Isolation is typically not necessary for 48-V-to-PoL applications [15].

As an emerging family of topology, hybrid SC converters have received increased attention in data center applications, since they can leverage the superior energy density of capacitors compared to inductors and transformers [16] and can achieve efficient utilization of switches [17]. In hybrid SC solutions, efficient and compact fixed-ratio SC converters are used to step down the input voltage first, followed by a buck stage for the rest of the voltage conversion task and output voltage regulation. Moreover, the buck inductor can enable complete soft-charging of the flying capacitors in the SC stage if the circuit is properly designed and operated [18]. Since the total 48-to-1 conversion ratio is split between the SC stage and the buck stage, if the SC stage can achieve higher conversion ratio, the conversion burden on the buck stage will be reduced. When the output voltage is constant, buck converters with lower conversion ratios typically require smaller inductors and achieve higher efficiency. Given that the converter volume is usually dominated by the buck inductors, it is favorable to design the SC stage to take on most of the voltage conversion task so that the buck inductor size can be reduced.

This paper proposes a high-performance hybrid SC converter based on a switching bus architecture for direct 48-to-1-V power conversion in data centers. The proposed topology consists of a 2-to-1 SC front-end and two 8-to-1 series-capacitor-buck (SCB) modules merged through two intermediate buses. Since the bus voltages are not DC but switch between two voltage levels, the two intermediate buses are called switching buses. Compared with the conventional DC bus architecture, the proposed switching bus architecture does not require bulky bus decoupling capacitors and can reduce the number of switches. As a sign of excellent theoretical potential, the proposed topology achieves the highest SC stage conversion ratio with the lowest normalized switch volt-ampere (VA) rating compared with existing 48-to-1-V hybrid SC demonstrations. A 500-A hardware prototype is built to demonstrate the performance of the proposed topology, achieving 94.7% peak power stage efficiency, 86.4% full-load efficiency and 464-W/in^3 power density.

II. Proposed Topology and Operating Principles

Fig. 1 shows the schematic of the proposed switching bus converter, with the key waveforms and control signals illustrated in Fig. 2. In the proposed topology, a 2-to-1 SC converter (i.e., Stage 1) is merged with two 8-to-1 series-capacitor-buck modules (i.e., Modules A and B in Stage 2)

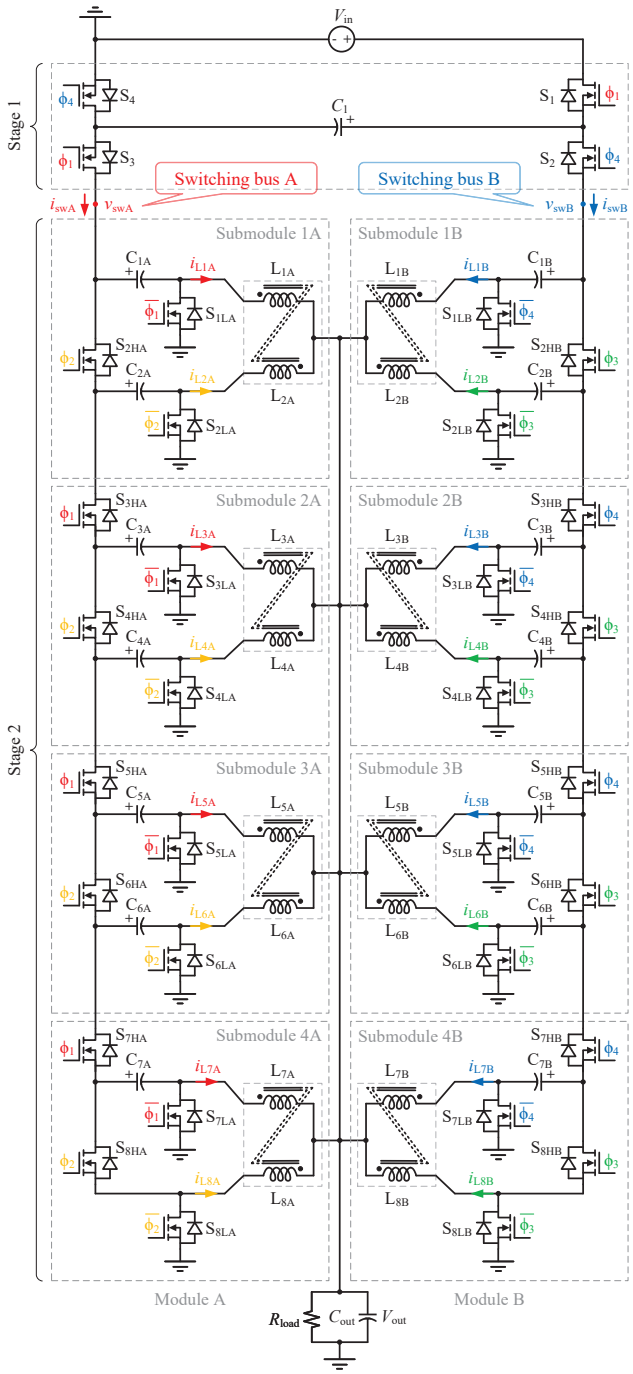


Fig. 1: Schematic of the proposed switching bus converter.

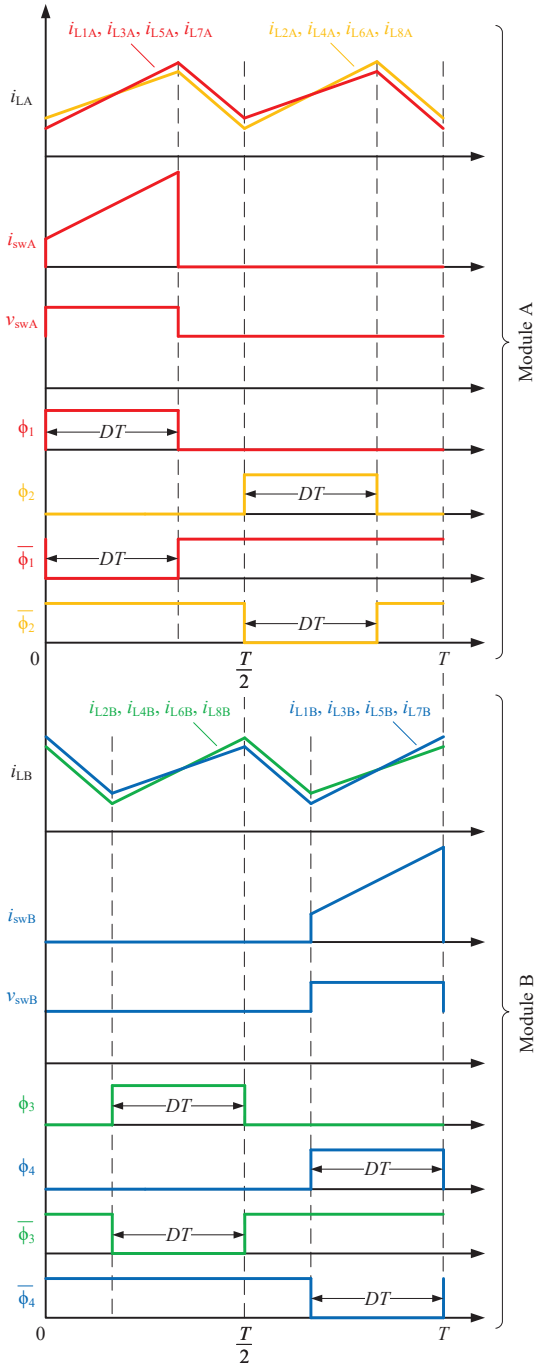


Fig. 2: Key waveforms and control signals.

through two switching buses (i.e., Switching buses A and B). As can be seen in Figs. 1 and 2, both SCB modules operate in a two-phase fashion, with a 180° phase shift between ϕ_1, ϕ_3 and ϕ_2, ϕ_4. The control signals in the two modules are staggered to achieve inter-module four-phase interleaved inductor currents. Each SCB module is divided into four submodules, within which each pair of inductors are negatively coupled. The details of the coupled inductor design is provided in Section III.

As Fig. 2 shows, the intermediate bus voltages v_{swA} and v_{swB} switch between two voltage levels, rather than being DC. Therefore, this type of intermediate bus is given the name *switching bus*. Compared to the conventional DC bus architecture, the proposed switching bus architecture has two advantages that promise higher efficiency and higher power density: 1) no bulky bus capacitor is required to maintain a stiff DC bus voltage, and 2) one redundant switch can be removed on each switching bus while the two stages are merged

TABLE I: Topological comparison between this work and existing 48-to-1-V hybrid SC works

Year	Topology	SC Stage Conversion Ratio	Buck Stage Conversion Ratio	Buck Stage Duty Ratio	Normalized Switch VA Rating
2020	Crossed-coupled QSD buck [7]	4:1	12:1	0.083	24.2
2021	CaSP-PoL [8]	6:1	8:1	0.125	23.5
2022	LEGO-PoL [9]	6:1	8:1	0.125	17.6
2022	SDIH [10]	6:1	8:1	0.125	14.7
2022	MLB-PoL [11]	8:1	6:1	0.167	23.7
2022	VIB-PoL [12]	8:1	6:1	0.167	14.3
2022	Multistack SC [13]	8:1	6:1	0.167	15.1
2022	Dickson^2-PoL [14]	9:1	5.33:1	0.188	14.8
2022	This work	16:1	3:1	0.333	10.2

together. In the schematic shown in Fig. 1, when Stages 1 and 2 are merged, the original highest high-side switch in Module A $\mathrm{S_{1HA}}$ is connected in series with $\mathrm{S_3}$ in Stage 1, and similarly, $\mathrm{S_{1HB}}$ is connected in series with $\mathrm{S_2}$. Since no bidirectional switch is required on the intermediate buses, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, the original highest high-side switches $\mathrm{S_{1HA}}$ and $\mathrm{S_{1HB}}$ are omitted in the circuit schematic illustrated in Fig. 1. Other examples of hybrid SC topologies constructed with intermediate switching buses include [8], [11] and [14], with all benefiting from a similar reduction in switch count due to the strategic merging of adjacent stages.

In the proposed topology, all flying capacitor voltages and inductor currents are naturally balanced thanks to the negative feedback mechanism similar to that explained in [8]. All flying capacitors are softly charged, and the low-side switches $\mathrm{S_{1LA/B-8LA/B}}$ can operate with zero-voltage switching (ZVS) turn-ON. The output voltage can be regulated by duty cycle control:

$$V_{\mathrm{out}} = \frac{D}{16} V_{\mathrm{in}}, \tag{1}$$

where V_{in} and V_{out} are the input and output voltages, and D is the duty ratio as illustrated in Fig. 2.

In this paper, two metrics are used to compare the theoretical potential of different hybrid SC topologies for 48-to-1-V conversion: 1) the SC stage conversion ratio and 2) the normalized switch VA rating. First, since the total 48-to-1 conversion ratio is split between the SC stage and the buck stage, a higher SC conversion ratio means a lower buck stage conversion ratio. When the output voltage is constant, buck converters with lower conversion ratios can achieve higher efficiency with smaller inductors. Therefore, a higher SC stage conversion ratio is desirable. However, higher SC conversion ratios usually require higher component count, which can lead to larger volume and higher loss. To take this trade-off into consideration, the normalized switch VA rating [17] is used as a second metric in the topological comparison. The normalized switch VA rating is defined as the total switch stress normalized to the output power:

$$\text{Normalized switch VA rating} = \frac{\sum V_{\mathrm{ds}} I_{\mathrm{d(rms)}}}{V_{\mathrm{out}} I_{\mathrm{out}}}, \tag{2}$$

where V_{ds} and $I_{\mathrm{d(rms)}}$ are the peak blocking voltage across and the RMS current through the switches when assuming no capacitor voltage ripple and no inductor current ripple, and V_{out} and I_{out} are the output voltage and output current, respectively. A lower VA rating indicates potentially lower switching loss, lower conduction loss, and smaller switch size and thus is more desirable.

In summary, the topologies with higher SC stage conversion ratio and lower normalized switch VA rating have greater potential for achieving higher efficiency and higher power density. Table I summarizes these metrics for several existing 48-to-1-V hybrid SC topologies and the proposed switching bus converter. Compared with the previous works listed in Table I, the proposed converter achieves the highest SC stage conversion ratio (16:1) with the lowest normalized switch VA rating, showing great theoretical potential for higher performance.

III. Hardware Implementation and Experimental Results

A 48-to-1-V hardware prototype is designed and built to verify the functionality and performance of the proposed converter. Fig. 3 shows the annotated photograph of the prototype, with the power stage components listed in Table II. The switching frequency of this prototype is 150 kHz. The PCB has 8 layers, with 2 oz copper on each layer.

As shown in Fig. 4, a two-phase coupled inductor is designed and customized for this prototype. The two phases are negatively coupled through the magnetic core combined from an E core and an I core. Each winding has two turns, and each turn is made from a piece of 0.5 mm thick and

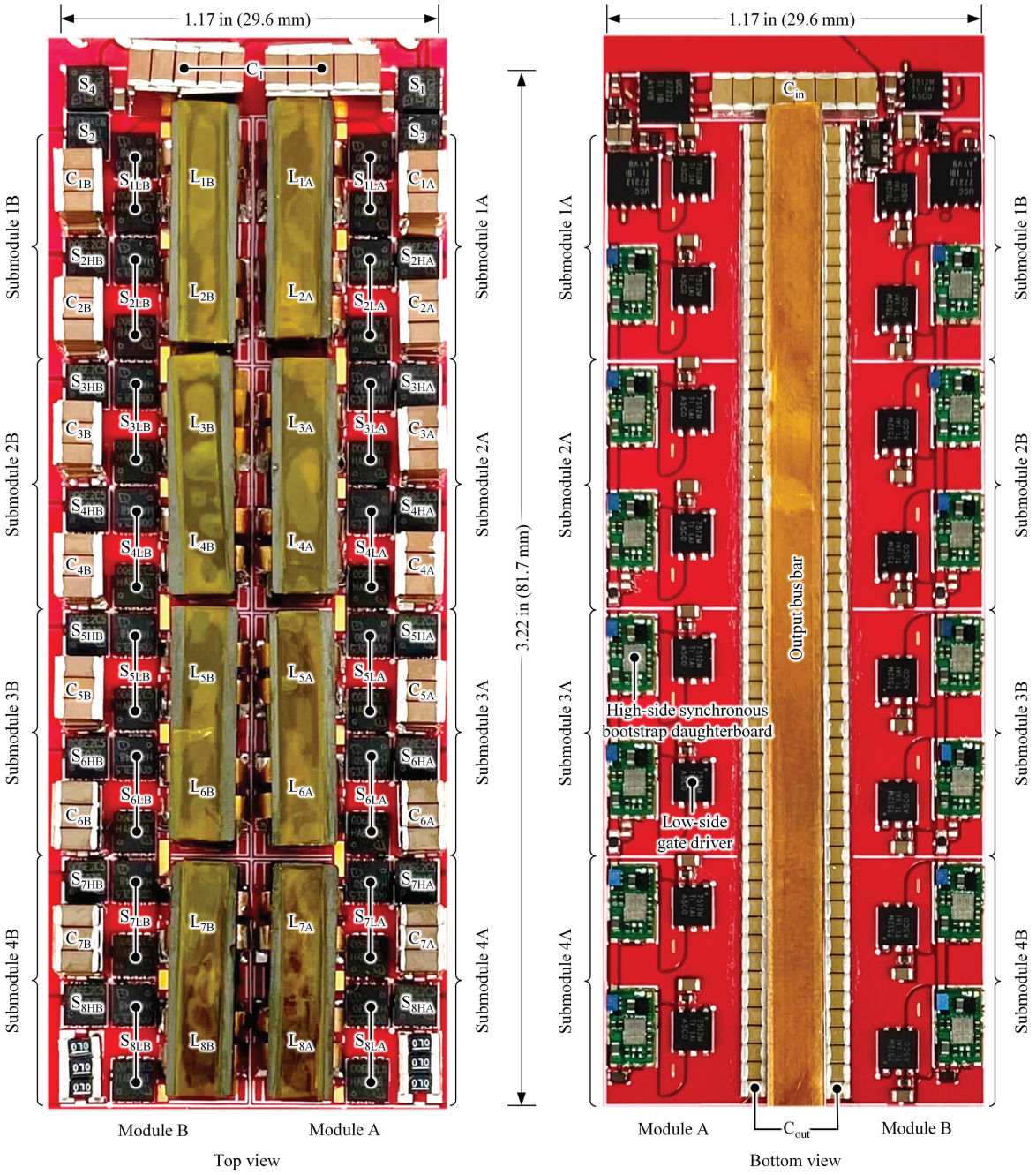


Fig. 3: Photograph of the hardware prototype. Dimensions: $3.22 \times 1.17 \times 0.29$ in^3 ($81.7 \times 29.6 \times 7.3$ mm^3).

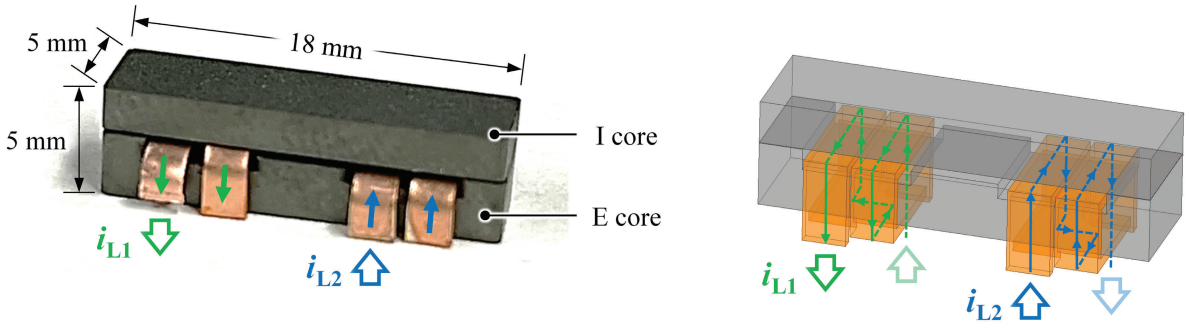
2 mm wide copper sheet. To reduce the total height of the coupled inductor, the two turns are connected with a PCB trace beneath the E core. As demonstrated in [11], compared with discrete inductors, coupled inductors can achieve the same equivalent steady-state inductance and inductor current ripple with significantly smaller volume. Operating at 0.333 duty ratio, the equivalent steady-state inductance of this two-phase coupled inductor is 606.5 nH, leading to a 7.33-A peak-to-peak inductor current ripple at 150 kHz switching frequency. All flying capacitors are stacked up to 3 layers to match the height of the coupled inductors so that the box volume of the prototype can be fully utilized. The stacked flying capacitors serve as natural heat sinks since they share nets with the the power MOSFETs. In addition, the distributed switch network provides an inherent heat spreading.

One practical challenge of the hardware implementation is the gate drive circuitry for the high-side switches in the second stage (i.e., $S_{2HA/B-8HA/B}$). Due to the large number of high-side switches, conventional cascaded bootstrapping [19] suffers from accumulative voltage drops across bootstrap diodes,

TABLE II: Component list of the power stage in the hardware prototype

Component	Part number	Parameters
MOSFET S_{1-4}	Infineon IQE013N04LM6CG	40 V, 1.35 mΩ
MOSFET $S_{2HA/B-8HA/B}$	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
MOSFET $S_{1LA/B-8LA/B}$	Infineon IQE006NE2LM5CG, IQE006NE2LM5	25 V, 0.65 mΩ (in parallel)
Flying capacitor C_1	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μF*×30 (in parallel)
Flying capacitor $C_{1A/B-5A/B}$	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μF*×9 (in parallel)
Flying capacitor $C_{6A/B,\ 7A/B}$	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×9 (in parallel)
Coupled inductor $L_{1A/B-8A/B}$	Custom two-phase coupled inductor: 1040 nH (self), 840 nH (mutual), 0.48 mΩ, 40 A	
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μF*×8 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μF*×108 (in parallel)

* The capacitance listed in this table is the nominal value before DC derating.



(a) (b)

Fig. 4: Custom two-phase coupled inductor. The two phases are negatively coupled. Each winding has two turns that are connected with a PCB trace beneath the E core. (a) Photograph with dimensions annotated. (b) 3D view with current paths annotated.

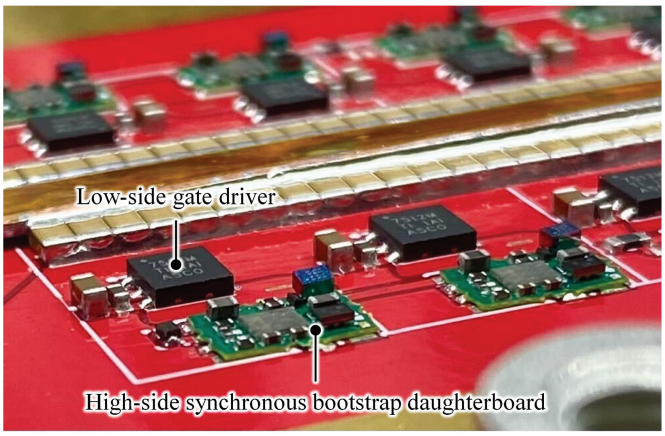


Fig. 5: Photograph of the gate drive circuitry using customized synchronous bootstrap daughterboards (green) to power the high-side switches.

leading to higher gate drive loss. To tackle this challenge, this work adopts the synchronous bootstrap technique [20], with a synchronous bootstrap daughterboard customized for this demonstration, as shown in Fig. 5. By replacing bootstrap diodes with active FETs, the voltage drops in the bootstrap circuit can be greatly reduced, eliminating the need for local LDOs and improving the gate drive efficiency. Experimental results show that the total voltage drop in the bootstrap circuit across 7 daughterboards is only 0.7 V, which is typically the voltage drop across one bootstrap diode in the conventional cascaded bootstrap circuit.

Fig. 6 shows the simulated and experimental waveforms of the switching bus voltages v_{swA} and v_{swB}. As can be seen in Figs. 6(a) and (b), at no load, the bus voltages switch between two voltage levels (21 V and 24 V), as has been explained in Section II and illustrated in Fig. 2. At full load, the flying capacitor ripples are superimposed on the two-level waveforms. As shown in Figs. 6(c) and (d), the experimental waveforms are in good agreement with the simulated waveforms.

The proposed converter is tested up to 500-A output current at 1-V output voltage and achieves a power density of 464 W/in^3 where converter volume is defined as a best-fit cuboid (box volume) encompassing the entire solution. Fig. 7 shows the thermal image of the prototype running continuously at full load with fan cooling only. Fig. 8 presents the measured efficiency of the prototype. It achieves 94.7% peak power stage

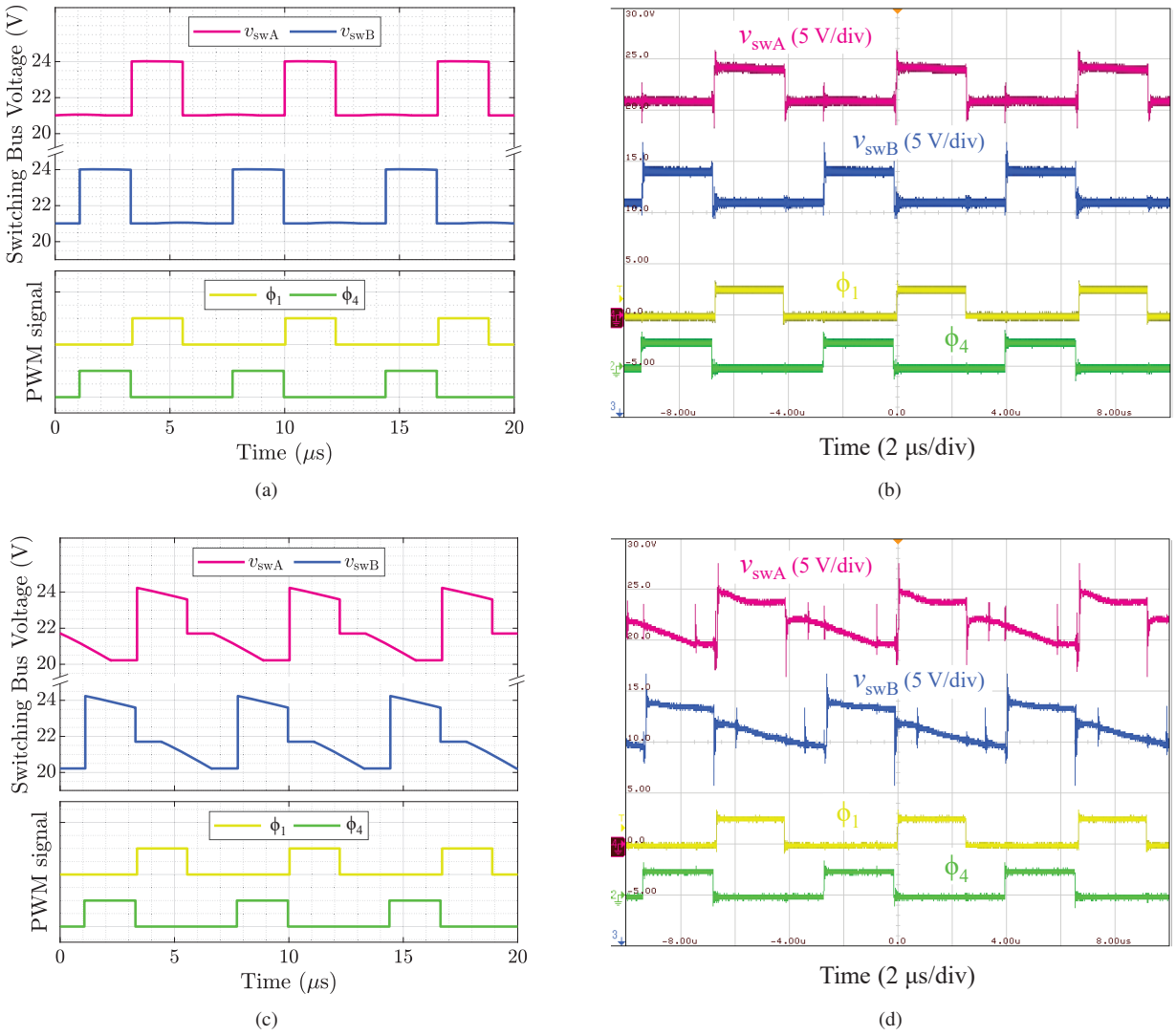


Fig. 6: Switching bus voltage waveforms v_{swA} and v_{swB}. (a) Simulated waveforms at no load. (b) Experimental waveforms at no load. (c) Simulated waveforms at full load. (d) Experimental waveforms at full load.

efficiency at 104-A output current and 86.4% full-load power stage efficiency at 500-A output current. With the gate drive loss included, it achieves 93.4% peak system efficiency at 132-A output current and 86.1% full-load system efficiency at 500-A output current.

Table III compares the performance of this work with that of the state-of-the-art 48-to-1-V works in previous literature. It can be seen that the proposed switching bus converter achieves a very high power density with the highest output current under air-cooled operation. In addition, it achieves an excellent peak power stage efficiency of 94.7% while maintaining a high efficiency at full load. The full-load efficiency can be further improved with better PCB layout using heavier copper.

IV. Conclusion

This paper presents a switching bus converter for direct 48-to-1-V power conversion in data centers. Through two switching buses, a 2-to-1 SC converter is merged with two 8-to-1 SCB modules, achieving an extremely high SC conversion ratio of 16-to-1 while maintaining a very low normalized switch VA rating. Compared with the conventional DC bus architecture, the switching bus architecture does not require bulky bus capacitors and can reduce the number of switches. A 48-to-1-V hardware prototype is designed, built and tested up to 500-A output current, achieving 94.7% peak power stage efficiency, 86.4% full-load efficiency and 464-W/in^3 power density (by box volume).

V. Acknowledgements

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References

[1] A. Andrae and T. Edler, "On Global Electricity Usage of Communication Technology: Trends to 2030," *Challenges*, vol. 6, pp. 117–157, 04 2015.

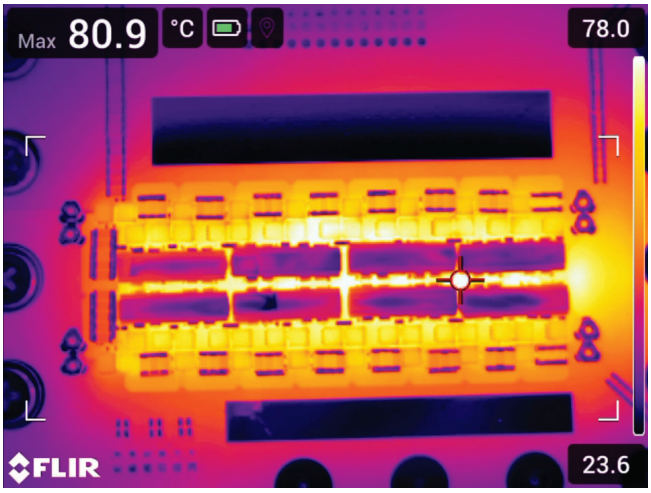

Fig. 7: Full-load thermal image at thermal equilibrium with fan cooling only ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 500$ A).

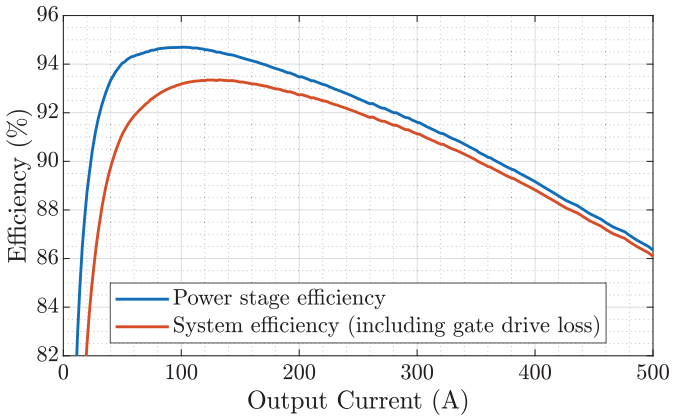

Fig. 8: Measured 48-to-1-V efficiency. Peak efficiency: 94.7% at $I_{\text{out}} = 104$ A (93.4% at $I_{\text{out}} = 132$ A including gate drive loss). Full-load efficiency: 86.4% (86.1% including gate drive loss) at $I_{\text{out}} = 500$ A.

TABLE III: Performance comparison between this work and the state-of-the-art 48-to-1-V works

Year	Reference	Output Current	Power Density	Power Stage Efficiency
2022	This work	500 A (31.3 A/phase)	464 W/in^3 (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%
2022	Dickson^2-PoL [14]	270 A (30 A/phase)	360 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%
2022	VIB-PoL [12]	450 A (28.1 A/phase)	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%
2022	MLB-PoL [11]	60 A (30 A/phase)	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%
2022	SDIH [10]	105 A (52.5 A/phase)	598 W/in^3 (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%
2022	LEGO-PoL [9]	450 A (37.5 A/phase)	294 W/in^3 (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%
2020	Crossed-coupled QSD buck [7]	40 A (20 A/phase)	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%* Full-load efficiency: 92.7%*
2020	Sigma [4]	80 A	420 W/in^3 (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%

* According to direct correspondence with the author.

[2] Vicor Inc., *Factorized Power Architecture and VI Chips: Flexible, High Performance Power System Solutions*, 2013. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/fpa101.pdf.

[3] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-Stage 48 V-12 V/6 V-1.8 V Voltage Regulator Module With Dynamic Bus Voltage Control for Light-Load Efficiency Improvement," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5628–5636, 2017.

[4] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2020.

[5] X. Lou, Q. Li, and M. H. Ahmed, "Adaptive Voltage Positioning Design of Single Stage 48/1V Sigma Converter for Fast Transient Response," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3530–3536.

[6] X. Lou and Q. Li, "300A Single-stage 48V Voltage Regulator with Multiphase Current Doubler Rectifier and Integrated Transformer," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1004–1010.

[7] M. Halamicek, T. McRae, and A. Prodić, "Cross-Coupled Series-Capacitor Quadruple Step-Down Buck Converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1–6.

[8] Y. Zhu, Z. Ye, T. Ge, R. Abramson, and R. C. N. Pilawa-Podgurski, "A Multi-Phase Cascaded Series-Parallel (CaSP) Hybrid Converter for Direct 48 V to Point-of-Load Applications," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1973–1980.

[9] J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, "Vertical Stacked LEGO-PoL CPU Voltage Regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6305–6322, 2022.

[10] N. M. Ellis and R. C. Pilawa-Podgurski, "A Symmetric Dual-Inductor

Hybrid Dickson Converter for Direct 48V-to-PoL Conversion," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1267–1271.

[11] T. Ge, R. Abramson, Z. Ye, and R. C. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1500–1505.

[12] Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano, and M. Chen, "Virtual Intermediate Bus CPU Voltage Regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6883–6898, 2022.

[13] P. Wang, D. Zhou, D. Giuliano, M. Chen, and Y. Chen, "Multistack Switched-Capacitor Architecture with Coupled Magnetics for 48V-to-1V VRM," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[14] Y. Zhu, T. Ge, Z. Ye, and R. C. Pilawa-Podgurski, "A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1272–1278.

[15] MPS Inc., *Increasing the Power Density and Efficacy of Datacenters Using a Two-Stage Solution for 48V Power Distribution*, 2017. [Online]. Available: https://www.monolithicpower.com/increasing-the-power-density-and-efficacy-of-datacenters.

[16] J. Zou, N. C. Brooks, S. Coday, N. M. Ellis, and R. C. Pilawa-Podgurski, "On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[17] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 903–10 919, 2022.

[18] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4008–4015.

[19] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020.

[20] N. M. Ellis, R. Iyer, and R. C. Pilawa-Podgurski, "A Synchronous Bootstrapping Technique with Increased On-time and Improved Efficiency for High-side Gate-drive Power Delivery," in *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2021, pp. 462–466.