Small-Scale Readout System Prototype for the STAR PIXEL Detector

Michal Szelezniak [1], Eric Anderssen [2], Leo C. Greiner [1], Howard S. Matis [1], Hans Georg Ritter [1], Thorsten Stezelberger [2], Xiangming Sun [1], James H. Thomas [1], Chinh Q. Vu [2], Howard H. Wieman [1]

[1] Nuclear Science Division, LBNL, Berkeley, CA 94720, USA
[2] Engineering Division, LBNL, Berkeley, CA 94720, USA

Abstract:
Development and prototyping efforts directed towards construction of a new vertex detector for the STAR experiment at the RHIC accelerator at BNL are presented. This new detector will extend the physics range of STAR by allowing for precision measurements of yields and spectra of particles containing heavy quarks. The innermost central part of the new detector is a high resolution pixel-type detector (PIXEL). PIXEL requirements are discussed as well as a conceptual mechanical design, a sensor development path, and a detector readout architecture. Selected progress with sensor prototypes dedicated to the PIXEL detector is summarized and the approach chosen for the readout system architecture validated in tests of hardware prototypes is discussed.

Keywords:
Vertex detector, APS, MAPS, Pixel

I. INTRODUCTION

The STAR Heavy Flavor Tracker (HFT) upgrade group is working to extend the capabilities of the STAR detector in the heavy flavor domain by providing a tracking system that will allow for very high resolution vertex measurements. This upgrade is designed to enable the direct topological reconstruction of D and B mesons through the identification of decay vertices displaced from the primary interaction vertex by more than 60 micrometers. The HFT upgrade, scheduled to be deployed in 2011, consists of three concentrically arranged detector systems. The outer most detector is an existing double-sided Silicon Strip Detector [1]. The second detector will be a new Inner Silicon Tracker based on single-sided silicon strip sensors [2]. The inner-most and highest precision system of the HFT tracker will consist of a pixel detector with a sub 30 micrometer DCA (distance of closest approach) pointing resolution [3]. The PIXEL detector will be composed of two layers of Monolithic Active Pixel Sensors (MAPS) that integrate the detector and front-end electronics layers in one silicon die and are fabricated using standard CMOS processes. Each sensor is a 1024×1088 array of pixels with 18.4 μm pitch giving the Pixel Detector system a total pixel count of more than 400 million pixels. Building a detector system with the required pointing resolution is challenging in all aspects of detector design. A number of these challenges will be addressed in the following sections.

II. CONCEPTUAL MECHANICAL DESIGN

Achieving the required pointing resolution requires limiting multiple-Coulomb scattering and constrains the detector to a design goal of < 0.3% radiation length per layer in the sensitive region. Sensors thinned to 50 microns, air cooling, a 500 micron thick Be beam pipe, and aluminum rather than copper conductor readout cables become necessary. The expected final system design is an array of 40 sensor ladders with ten 2 cm × 2 cm sensors per ladder and 10 parallel independent readout systems. The Pixel detector coverage is ± 1 in η with the first active sensor layer at a radius of 2.5 cm from the beam axis and the second layer at 8 cm radius. This geometry and the chosen pixel pitch of 18.4 μm offer pointing resolution of about 13 ⊕ 19 GeV/p·c μm. The resolution of the detector is limited by multiple-Coulomb scattering. To understand how different parts of the structure contribute to the overall layer thickness one can look at one of the preliminary designs, where estimates of the radiation length contribution from different layer components are summarized in Table 1.

Component	% radiation length	Si equivalent (μm)
silicon	0.053	50
adhesive	0.014	13.39
cable assembly	0.089	83.92
adhesive	0.014	13.39
Carbon composite	0.11	103
TOTAL	**0.28**	**264**

Table 1. Estimates of the material budget in a single PIXEL detector layer according to one of the preliminary designs. The cable assembly is intended as a 150 μm Kapton cable with 4 layers of aluminum rather than copper traces to minimize the material budget. Silicon sensors are attached to the readout cable assembly with a thin layer of adhesive and the cable assembly is attached to the carbon composite beam structure in the same fashion.

In recognition of difficulties encountered in previous experiments, one of the design requirements is a rapid (within 8 hour access time) removal and replacement of the PIXEL detector. The development plan includes building four copies of the detector. It is required that the insertion reproducibility is within a window of 20 μm to preserve detector alignment so that a detailed recalibration does not have to be done each time the detector is removed. To meet this requirement, the barrels will be divided in halves and supported with their own 3 point precision kinematic mounts located at one end close to the detector barrel. Quick detector replacement will also help to deal with radiation damage induced in sensors by allowing replacement of ladders containing sensors whose performance has deteriorated. A 3-D design view of the detector with mechanical support and cabling and cooling services is presented in Figure 1.

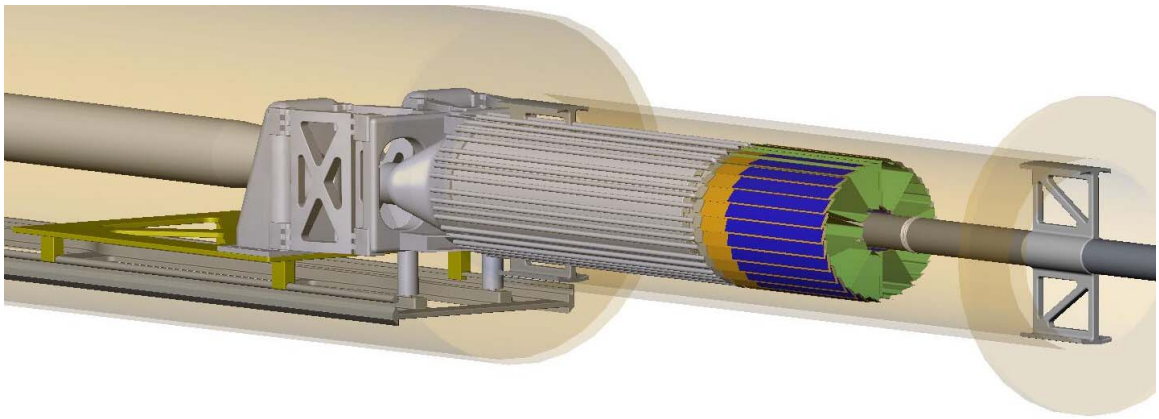

Figure 1. Drawing of the pixel detector design. 40 ladders equipped with 10 sensors each will be arranged cylindrically into two layers at 2.5 and 8 cm from the center of the beam pipe. Detector cabling and cooling infrastructure is designed to be located at one end of the detector so that the extraction and insertion of the detector is possible from one end. Mechanical support with kinematic mounts will allow precise positioning of the detector. A kinematic mount constrains but does not over-constrain all six degrees of freedom increasing stability and allowing precise repositioning of the mount.

The expected power dissipation of the detector, according to the design values, is at the level of 100 mW/cm^2 for the sensors and an additional 80 W for readout electronics out of the low mass region for a detector total of 240 W. To achieve low mass, the detector system is being designed to use air cooling for its detector structure in the active tracking volume. Cooling is obtained by air flowing from one end of the detector between the two barrel surfaces and returning in the opposite direction over both the outer barrel surface and along the inner barrel surface next to the beam pipe. Simulations for choosing the optimal air flow speed and air temperature are on-going. Initial results indicate that the air flow speed of 8 m/s should be sufficient to keep sensors temperature at less than 10 °C above the air temperature. It is expected that the sensors will operate at temperature of 20-30 ºC to provide satisfactory noise performance.

III. SENSOR DEVELOPMENT

The sensor technology chosen for the PIXEL detector is Monolithic Active Pixel Sensors (MAPS). MAPS are built using standard commercially available CMOS technology and integrate sensor and readout electronics in one silicon device [4, 5]. Sensor development for the PIXEL detector is done in collaboration with the CMOS and ILC group at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg. The sensor development path follows the development path of the technology as set by the IPHC group.

In this path, the first generation of sensors for the PIXEL detector features multiplexed serial analog outputs in a rolling shutter configuration. The MimoSTAR series of sensors are 50 MHz multiplexed analog readout sensors with 30 µm × 30 µm pixels in variously sized arrays. MimoSTAR2 is a small scale prototype with a 128 × 128 pixel array. This sensor demonstrated a good signal to noise ratio in the central pixel with the most probable value of approximately 16 and a collected charge of 220 electrons. This performance gives almost 100% detection efficiency for minimum

ionizing particles. The MimoSTAR2 design was scaled up to half reticle[1] size and designated MimoSTAR3. This larger device is under test to verify the scalability of the design.

Analog readout sensors with integration/readout-times of a few milliseconds are too slow to avoid significant pile-up of consecutive events at the rate expected for RHIC II luminosities (peak at 8×10^{27} $cm^{-2}s^{-1}$) and high particle densities. Digital signal transmission that allows faster readout speeds is necessary to meet the requirements of the short readout time.

The next generation of sensors will implement a digital binary readout system and will be used for construction of an engineering prototype detector with limited coverage that is planned to be deployed at STAR for the year 2010 run. The prototype called Phase-1, will be based on Mimosa8/Mimosa16 architecture, [6], and contain on-chip correlated double sampling (CDS), fine grained threshold discrimination and a fast serial Low-Voltage Differential Signaling (LVDS) readout. The prototype is designed to be a full size, 640 × 640 array, resulting in a full 2 cm × 2 cm sensor size. In order to achieve a 640 μs integration time, the sensor will be equipped with four LVDS outputs running at 160 MHz. The sensor has been recently designed and is ready for fabrication. Delivery of wafers of this sensor is expected in late 2008.

The final production sensor for the PIXEL detector to be installed in 2011 will contain all of the attributes of the previous prototype with the pixel sub-arrays clocked faster to give a <200 μs integration time. It will also feature an integrated zero suppression circuit with run length encoding to reduce data rates. Reduced data rates will allow reducing the number of outputs per sensor to two. The first prototype of this production design is expected to be available in the 2010 time frame.

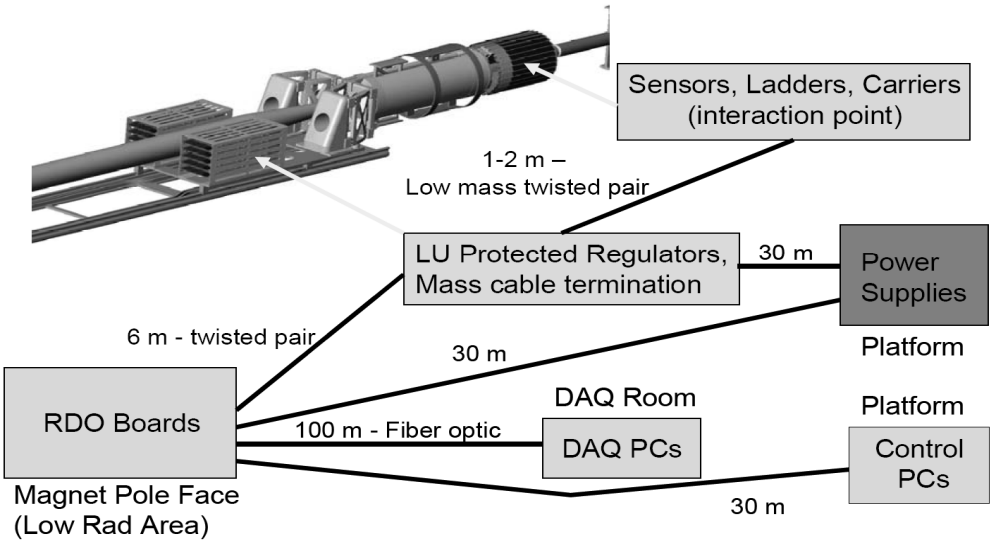

Figure 2. Physical layout of the readout system blocks. The detector ladders and accompanying readout system have a highly parallel architecture. There are ten parallel readout chain units in the full system serving modules of 4 ladders.

[1] A photomask used for lithography in wafer fabrication.

IV. READOUT SYSTEM DEVELOPMENT

Development of the readout system is strongly coupled to sensor development. As the sensor development advances and more electronics functionality (correlated double sampling and binary discrimination) are integrated on-chip, the readout system becomes less complex.

Since the PIXEL detector is an upgrade for the STAR experiment, one of the main requirements for the readout system is to easily integrate into the STAR environment. Therefore, the system has to be compatible with the existing trigger and data acquisition system infrastructure. It also needs to deliver full detector events for event building at a rate equal to or greater than the STAR central detector TPC with a manageable level of data rate on the order of a few hundreds of MB/s. With a 400 million pixel final detector, data reduction implemented on-chip or in the readout system is necessary.

For the Phase-1 prototype with binary readout of all pixels, the readout system (RDO) needs to provide zero suppression with address encoding and event forming in response to triggers received from STAR. This will allow reducing data flow from approximately 32 GB/s to 240 MB/s. For the final sensor, zero suppression and address encoding will be implemented on-chip reducing the complexity of the RDO system.

The architecture chosen for the readout system for the PIXEL detector is highly parallel. Each independent readout chain services a module of four ladders on a mechanical carrier unit. Each ladder is equipped with 10 sensors and has independently regulated power with latch up detection circuitry provided by power/mass termination board located approximately 1-2 meters from the ladders. Output, control and synchronization signals and latch-up protected power for each ladder are carried via low mass twisted pair cables (42 AWG) between the end of the ladder and a power/mass termination board. These wires have very low stiffness to avoid introducing stresses and distortions into the mechanical structure. From the mass termination board, the digital signals are carried via robust shielded twisted pair cables (24 AWG) to the RDO boards, which are mounted on the magnet iron of the STAR magnet structure approximately 6 meters away out of the high radiation environment. The RDO boards are based on a fast Xilinx Virtex-5 Field Programmable Gate Array (FPGA) development board that is a commercially available product. The RDO board is mated to a custom motherboard that provides LVDS buffering into the FPGA, the STAR trigger input, PCI mezzanine card (PMC) connectors for mounting the CERN developed fiber optic Detector Data Link (DDL) [7], SRAM, and various ADCs and I/O to be used in testing. The DDL provides a link between the readout system and data acquisition PCs. The chosen system architecture (presented in Figure 2) and the components used for its construction allow it to be a robust and a cost efficient solution.

V. RECENT PROTOTYPING RESULTS AND FUTURE DEVELOPMENT

Prototyping of the mechanical parts for the detector is planned to begin in a few months. By the end of the year the full-reticule size Phase-1 prototype with binary readout should be available for testing. This sensor will be used for constructing an engineering prototype corresponding to 3/10 of the full detector. The goal is to install the engineering prototype in STAR by summer 2010. This prototype detector will have the capability to perform limited physics measurements.

The first stage of development of the readout system was optimized for sensors with analog readout. A prototype system with a FPGA based cluster finding, pixel address encoding, and event forming, was developed and successfully tested in the STAR environment [8]. This early prototype system was operated as a subsystem of the STAR experiment and interfaces to the STAR trigger system were successfully tested.

The readout concept adopted for sensors with digital binary readout has been recently validated with a prototype readout system designed to study the reliability of the LVDS data path. Ladder mockup was built on FR4 PCB (0.031 in) sized to resemble the final ladder design. Appropriately configured sensors with binary readout were not available at the time of tests, so LVDS 1-to-4 fanout buffers were used in place of sensors. Three independent pseudo-random test patterns were sent from the FPGA on the RDO board to the ladder and back to check for data corruption and possible cross-talk. The transmission was carried on 1 and 2 m fine twisted pair cables (42 AWG), and after buffering stage, on a more robust (24 AWG) twisted pair cable. The measured bit error rate (BER) was below 10^{-14} for the maximum data rate of 160 MHz that can be expected in the readout system. This test fully validates the chosen approach to the system architecture. The next development step already taking place is building full readout system production prototypes.

ACKNOWLEDGMENT

This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231, Office of Nuclear Physics.

REFERENCES

[1] L. Arnold, J. Baudot, D. Bonnet, A. Boucham, S. Bouvier, J. Castillo, et al., "The STAR silicon strip detector (SSD)," *Nucl. Instr. Meth. A,* 499, 2003, pp. 652-658.

[2] F. Simon, "The STAR integrated tracking upgrade project", *Nucl. Instr. Meth. B,* 261, 2007, pp. 1063-1066.

[3] C. Chasman et al., "A Heavy Flavor Tracker for STAR", 2008, LBNL/PUB-5509-2008.

[4] G. Deptuch, J-D. Berst, G. Claus, C. Colledani, W. Dulinski, Y. Gornushkin, et al. "Design and testing of monolithic active pixel sensors for charged particle tracking", *IEEE Trans. Nucl. Sci*, 49, 2002 pp. 601 – 610.

[5] W. Dulinski et al., "CMOS Monolithic Active Pixel Sensors for Minimum Ionizing Particle Tracking Using Non-Epitaxial Silicon Substrate", *IEEE Trans. Nucl. Sci*, 51, 2004, pp 1613 – 1617.

[6] Y. Degerli, G.Deptuch, N. Fourches, A. Himmi, Y. Li, P. Lutz, F. Orsini, and M.Szelezniak, "A fast monolithic active pixel sensor with pixel-level reset noise suppression and binary outputs for charged particle detection", *IEEE Trans. Nucl. Sci*, 52, 2005, pp. 3186-3193.

[7] http://alice-proj-ddl.web.cern.ch/alice-proj-ddl/

[8] L. Greiner, H.S. Matis, H.G. Ritter, A. Rose, T. Stezelberger, X. Sun, M. Szelezniak, J. Thomas, C. Vu, H. Wieman, "Results from a prototype MAPS sensor telescope and readout system with zero suppression for the heavy flavor tracker at STAR", *Nucl. Instr. Meth. A*, 589, 2008, pp. 167-172.