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Authors

Fernandez, Kelly

Pilawa-Podgurski, Robert

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K. Fernandez
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Kelly Fernandez, Robert C.N. Pilawa-Podgurski
email: kefernandez@berkeley.edu

***Abstract*—Resonant hybrid switched-capacitor converters (ReSCs) have the ability to achieve high efficiencies, power densities, and high power-handling capabilities. However, ReSCs have yet to be widely explored in high-voltage (HV) step-up application areas. In this work, we attempt to bridge the gap between ReSCs and the HV step-up application space by proposing a 1-to-10 step-up cascaded series-parallel (CaSP) converter. The principles of operation and functionality of the circuit are discussed and are validated with a hardware prototype. Experimental results up to 300 W and 350 V including efficiency and load regulation measurements and demonstration of zero-current switching (ZCS) are provided.**

I. Introduction

In many electrical systems, a low-voltage (LV) dc-source must be stepped-up to a higher dc-voltage. Such areas include both commercial and residential photovoltaic inverters [1], [2], medical systems such as X-ray power generators and pulse electric fields (PEFs) [3]–[5], fuel cell and lithium-ion battery applications such as dc microgrids [6], [7], and space exploration systems that utilize Hall-effect-propulsion (HEP) [8].

Typically, a conventional two-level boost converter can be used for step-up applications. However, two-level boost converters generally exhibit poor power densities as they rely primarily on an inductor for energy transfer, which demonstrates energy densities up to 1000x smaller than those of capacitors [9]. Moreover, for high voltage dc-dc step-up applications, the two-level boost converter requires a sufficiently large duty cycle to produce a high input-to-output voltage gain. This is undesirable since it produces significant reverse recovery problems with the output diode and results in poor converter performance, low efficiency, and worsened electro-magnetic interference (EMI) performance [10]. The implementation of gallium nitride (GaN) devices eliminates the reverse recovery issue, but still produces lower efficiency due to dead-time losses of the GaN devices [11]. Transformer-based power converter topologies address the shortcomings of the two-level boost through the utilization of a transformer to achieve a high dc-dc gain [12]–[14], but the increase in converter performance and efficiency is undermined by the added physical volume of the transformer, resulting in poor power density metrics.

In the low-voltage (LV) step-down domain, resonant hybrid switched-capacitor converters (ReSCs) have been able to address and greatly overcome these shortcomings. Specifically, ReSCs have consistently demonstrated extremely low physical volumes through the utilization of a combination of capacitors and inductors for both energy storage and transfer. Additionally, ReSCs have demonstrated the ability to achieve high power-handling capabilities and thus ultra-high power densities, high efficiencies, and the soft-charging and soft-switching abilities [15]–[20]. When implemented with GaN devices, soft-switching ReSCs do not exhibit the previously mentioned dead-time losses since the inductor current is discharge to 0 A before any switches transition from an on to off state. Although ReSCs consistently push the limit in achieving state of the art performance in the LV step-down domain and offer an abundance of solutions to their magnetic-based topology counterparts in the high-voltage (HV) step-up domain, they have not yet been widely explored for the HV step-up application area.

In this work we attempt to bridge the gap between ReSCs and the HV dc-to-dc step-up space by investigating the use of a 1-to-10 step-up multi-resonant cascaded series-parallel (CaSP) converter, previously demonstrated in a LV, high step-down application [21]. The 1-to-10 CaSP converter comprises a 1-to-5 series-parallel swiched-capacitor (SC) stage followed by a 1-to-2 SC stage. Due to its multi-phase operation, the CaSP can achieve a 1-to-10 conversion ratio with a lower number of components compared to a standard two-phase SC converter, with a single inductor to provide soft-charging [18] operation, as well as soft-switching capabilities. The remainder of this paper is organized as follows: Section II details a passive component volume and switching stress analysis following the technique presented in [22] that motivate the selection of the CaSP converter in comparison to other ReSC topologies for high gain applications, Section III gives an overview of the principles of operation of the 1-to-10 CaSP converter, Section IV showcases the hardware and experimental validation of the 1-to-10 CaSP, and lastly, Section V concludes this paper.

II. Cascaded Series-Parallel (CaSP) Passive Component Volume and Switch Stress Analysis

There are several ReSC converters that can be considered for HV high-gain dc-dc applications. Therefore, even with a specific application and step-up ratio, it is not immediately clear what is the plausible converter choice to be examined in this work. Specifically, a converter topology that has the ability to achieve a very high power density while maintaining low power loss is desired.

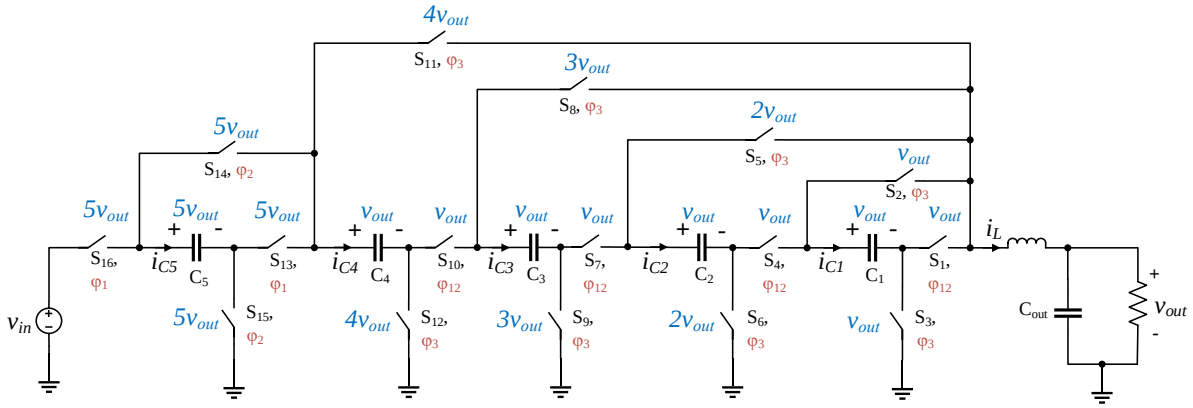

Fig. 1: Schematic drawing of a 10-to-1 CaSP converter with switch and capacitor voltage ratings and gate signals provided.

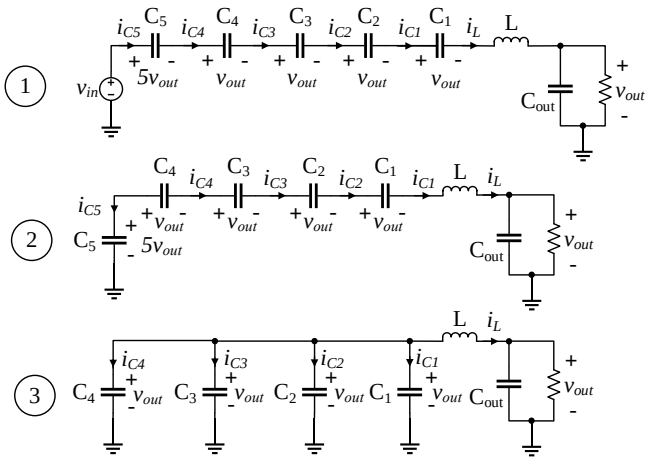

Fig. 2: The circuits states for each of the three sub-periods of the 10-to-1 CaSP converter.

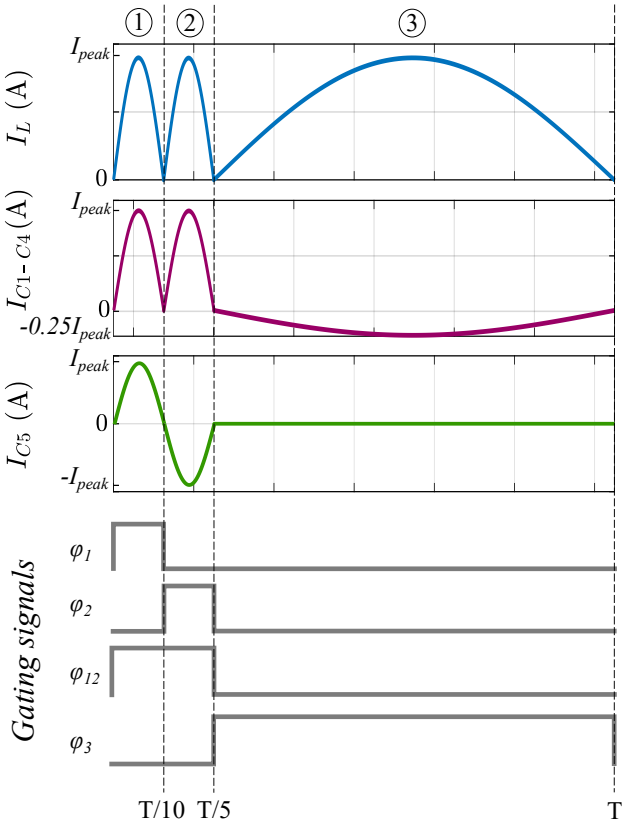

Fig. 3: The inductor and flying capacitor current waveforms along with gate signals for the 10-to-1 CaSP converter during the entire switching period. Note that the average inductor current is equal to I_{out} for each of the three sub-periods and thus for the entire switching period, hence $I_{peak} = \frac{\pi}{2} I_{out}$.

The work in [22] proposes an analytical technique that normalizes the passive component volume of ReSC converters to that of a buck converter, as well as a method for normalizing the total switching stress of several ReSC converters. These normalization analyses give insight to the total volume and power loss of the converter topology. In [22], the Buck, Dickson, Doubler, FCML, Ladder, and Series-parallel step-down topologies are examined. In this work, we take the analysis presented in [22] and apply it to the CaSP converter with a chosen generic step-down ratio of 10-to-1. The analysis results for a 10-to-1 step-down CaSP converter are the exact same as the 1-to-10 step-up scenario, and hence can be used to direct our topology choice for our high gain dc-dc converter. Figure 1 displays the 10-to-1 CaSP circuit topology while Figs. 2 and 3 show the CaSP sub-period circuit states and current waveforms along with gating signals, respectively.

A. CaSP Passive Component Normalization

The total passive volume of a converter can be determined by the total required energy stored by all of the passive elements divided by the the component's energy density:

$$Vol_{tot} = \frac{E_{C,tot}}{\rho_C} + \frac{E_{L,tot}}{\rho_L}, \tag{1}$$

where ρ_C and ρ_L are the energy densities for the capacitors and inductors in the topology and are assumed to be constant for each capacitor and inductor in the topology (i.e. all capacitors and inductors have energy density ρ_C and ρ_L respectively). As explained in [22], in order to obtain an expression for $E_{C,tot}$, there are three important topology-dependent vector quantities, k, α, and β pertaining to the the flying capacitors that must be identified:

$$P_{C,j} = k_j P_{out}, \tag{2}$$

$$V_{C,j} = \alpha_j V_{out}, \tag{3}$$

and

$$\Delta V_{C,j} = \beta_j \Delta V_{C0}, \tag{4}$$

where k_j is the ratio between processed reactive power for flying capacitor C_j and the converter's output power P_{out}, α_j is the ratio between the average dc voltage of C_j and the converter's output voltage V_{out}, and β_j is the ratio of the ac ripple voltage of C_j and capacitor ac ripple voltage V_{C0} in a standard 2-to-1 ReSC converter. For a detailed description of the methodology of how to obtain vector quantities k, α, and β, the reader is directed to [22]. By following such analysis for a 10-to-1 CaSP, the capacitive vectors are calculated as:

$$k = [\frac{1}{5} \quad \frac{1}{5} \quad \frac{1}{5} \quad \frac{1}{5} \quad \frac{1}{2}], \tag{5}$$

$$\alpha = [1 \quad 1 \quad 1 \quad 1 \quad 5], \tag{6}$$

and

$$\beta = [\frac{1}{2} \quad \frac{1}{2} \quad \frac{1}{2} \quad \frac{1}{2} \quad 3]. \tag{7}$$

In order to obtain an expression for $E_{L,tot}$ in (1), the vector quantity γ, which relates the power processed by the inductor(s) in the chosen topology to that of the 2-to-1 case must be identified:

$$P_{L,i} = \gamma_j P_{L0}. \tag{8}$$

Following the analysis in [22], it can be calculated that $\gamma = \frac{4}{5}$. The capacitive and inductive vectors can then be used to calculate the optimized total volume of (1).

B. CaSP Switching Stress Normalization

The total switching stress for a converter topology is commonly defined as the summation of the product of each switch's peak dc blocking voltage and the average current that flows through each switch:

$$\text{Converter switch stress} = \sum_{j=1}^{n} V_{ds,j} I_{ds,j}, \tag{9}$$

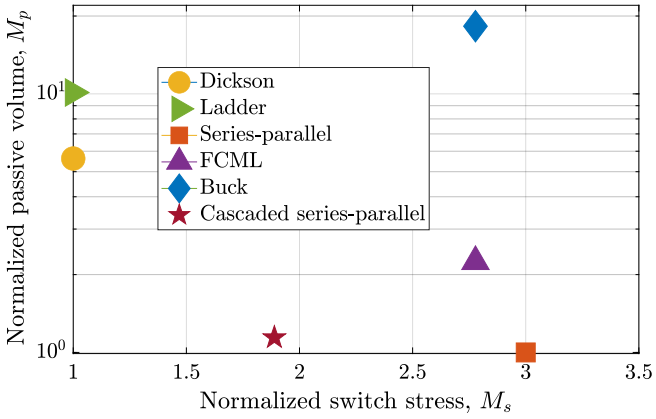

Fig. 4: Normalized passive volume M_P vs. normalized switch stress M_S from the analysis explained in [22] for several 10-to-1 ReSC topologies including the cascaded series-parallel converter.

where n is the number of switches in the converter. Both $V_{ds,j}$ and $I_{ds,j}$ can both be expressed in terms of the converter's output voltage V_{out} and output current I_{out}. We can then define the normalized switch stress for the converter as:

$$M_s = \frac{\text{Converter switch stress}}{V_{out} I_{out}} = \sum_{j=1}^{n} \beta_{v,j} \beta_{i,j}, \tag{10}$$

where $\beta_{v,j}$ is the ratio between the peak dc blocking voltage of switch j and V_{out}, and $\beta_{i,j}$ is the ratio between the average current through switch j and I_{out} [22]. As noted in [23], for converters with a duty cycle that deviates from 0.5, the rms current value, as opposed to the averaged amount, should be looked at instead for better accuracy of converter switching stress. However, because the majority of the ReSCs being analyzed in this work have a 50% duty ratio, the average current through each switch can be used for this analysis as a good approximation.

Figure 1 displays the dc-blocking voltages in terms of V_{out} for each of the switches in the 10-to-1 CaSP. The $\beta_{v,j}$ for each switch is the integer multiple of V_{out} that each switch blocks in the figure. For example, $\beta_{v,15} = 5$ whereas $\beta_{v,3} = 1$. Figure 3 displays the current flowing through each of the flying capacitors and the inductor and the gating signals for each switch. The inductor's average current in one switching period and each of the three sub-periods is equal to I_{out}. Due to this, $\beta_{i,j}$ is the duty ratio of each switch's gating signal For example, $\beta_{i,15} = 0.1$ whereas $\beta_{i,3} = 0.8$.

C. Analysis Results

Figure 4 displays the normalized passive volume vs. the normalized passive switch stress for several ReSC topologies performing a 10-to-1 step-down. To note, all topologies except for the CaSP have had this analysis previously performed by the author in [22], but for different conversion ratios. The 10-to-1 series-parallel converter achieves the lowest normalized

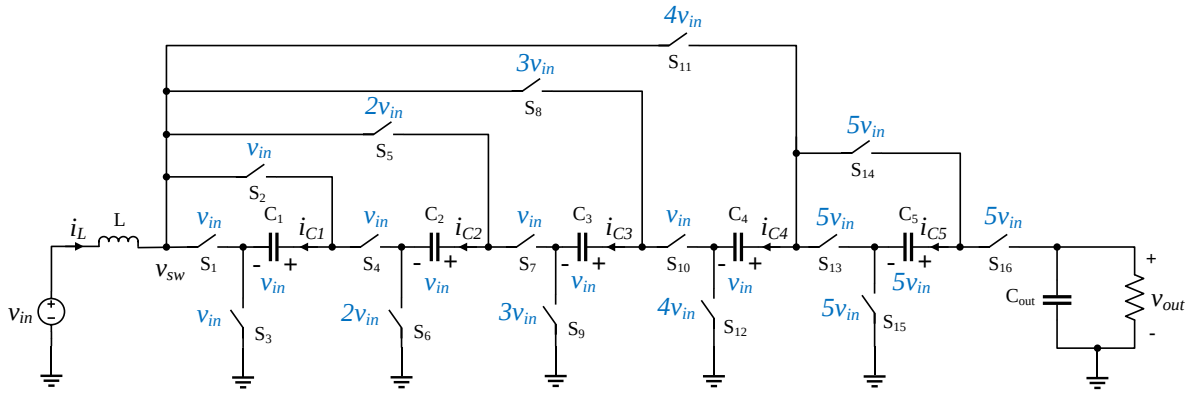

Fig. 5: Schematic drawing of a 1-to-10 CaSP converter with switch and capacitor voltage ratings provided.

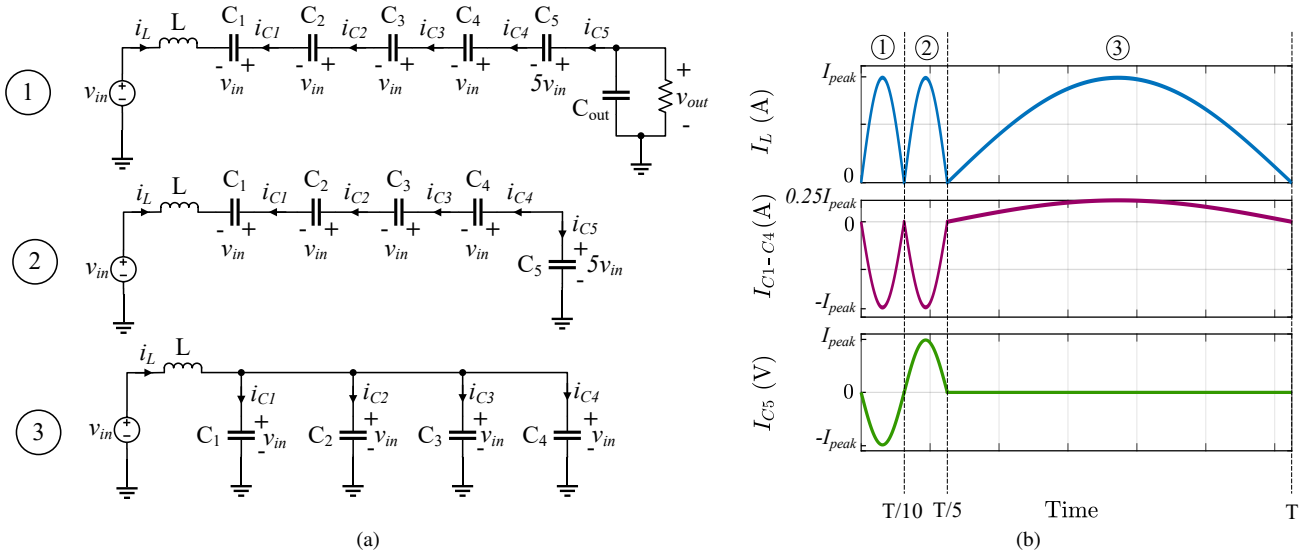

Fig. 6: The sub-period operation of the 1-to-10 CaSP. (a) The circuits states for each of the three sub-periods of the 1-to-10 CaSP converter. (b) The inductor and flying capacitor current waveforms for the 1-to-10 CaSP converter during the entire switching period.

passive volume. However, the 10-to-1 CaSP achieves a fairly similar normalized passive volume amount while achieving more than a 30% reduction in normalized switch stress. While the Dickson and Ladder topologies achieve the lowest normalized switch stress, they have a much larger normalized passive volume. From the analysis, it can be concluded that the 10-to-1 CaSP converter achieves a relatively low amount of power loss while maintaining a low passive volume in comparison to the other 10-to-1 ReSC topologies analyzed in [22].

III. 1-to-10 CaSP Principles of Operation

Figure 5 displays the schematic drawing of the 1-to-10 CaSP with $v_{out} = 10 \cdot v_{in}$. The dc-voltage rating and polarity of the switches and the flying capacitors are shown. Figure 6a shows the three different sub-period circuit states of the 1-to-10 CaSP converter while Fig. 6b shows exemplar current waveforms for the flying capacitors and inductor.

As detailed in [21], the switching period of the CaSP converter consists of three sub-periods with unique LC resonant tanks that allow for resonance and thus soft-switching operation. As shown in Fig. 6b, in each sub-period the average current flowing through the inductor remains the same. Due to this, the duration of time for each sub-period is equal to the fraction of total charge that is injected by the input source for each switching period T, that flows through the LC-tank in each sub-period. By following the charge flow analysis presented in [24], from the total charge injected from the input source in one switching period, a tenth of that charge flows through the LC-tank in sub-period 1, a tenth flows through the LC-tank in sub-period 2, and eight-tenths flow through the LC-tank in sub-period 3. Hence, sub-period one is a tenth of the

full switching period T, i.e. $T_1 = \frac{T}{10}$, followed by sub-period two $T_2 = \frac{T}{10}$, and sub-period three $T_3 = \frac{8T}{10}$.

1) Sub-Period One: From time $t = 0$ to $T/10$, the output load is connected in a direct path to the input voltage source. Capacitors C_1 through C_5 are connected in series with the inductor, and are discharged. Capacitors C_1 through C_4 have a dc-voltage equal to v_{in} displaced across each capacitor, while capacitor C_5 has a dc-voltage equal to $5v_{in}$ across it. The equivalent capacitance of the corresponding LC-tank can be calculated as

$$C_{eq1} = \frac{1}{\sum_{j=1}^{5} \frac{1}{C_j}}. \tag{11}$$

The capacitance of flying capacitors C_1 through C_4 can be set equal to a nominal capacitance C_o. From this, the resonant frequency of sub-period 1 is equal to:

$$\omega_1 = \frac{1}{\sqrt{L \frac{C_o C_5}{C_o + 4C_5}}}. \tag{12}$$

The duration of sub-period 1 is equal to half of the resonant period, i.e. $T_1 = \frac{\pi}{\omega_1}$. By obtaining expressions for each sub-period's duration of time in terms of L, C_o, and C_5, the capacitance C_5 can be calculated in terms of C_o. Specifically, we can relate sub-period duration T_1 and T_3 as $8 \cdot T_1 = T_3$, and an expression for C_5 can be obtained as $C_5 = \frac{C_o}{12}$.

2) Sub-Period Two: From time $T/10$ to $2T/10$, the load is disconnected from the CaSP converter and the polarity of capacitor C_5 is reversed. As a result, capacitor C_5 is now charged while capacitors C_1 through C_4 remain discharging. Although the orientation of C_5 is reversed, flying capacitors C_1 through C_5 remain connected in series. Hence, the equivalent capacitance and resonant frequency of sub-period 2 can be set equal to the expressions in (11) and (12) respectively.

3) Sub-Period Three: From time $2T/10$ to T, capacitor C_5 is disconnected and capacitors C_1 through C_4 are connected in parallel at the switch node. The polarity of capacitors C_1 through C_4 is reversed, such that the capacitors are now being charged by the input source. As previously mentioned, the inductor current i_L has the same average value in each sub-period. Due to this, it can be determined that the average voltage across the inductor in each sub-period is 0 V. Consequently, it can be examined through KVL analysis that in circuit state 3, capacitors C_1 through C_4 are charged to a dc-voltage equal to the input source v_{in}.

Due to the change in configuration of the flying capacitors in sub-period 3, new expressions for the sub-period equivalent capacitance C_{eq3}, resonant frequency ω_3, and time duration T_3 must be obtained. Since flying capacitors C_1 through C_4 are now connected in parallel and are equal to the same nominal capacitance C_o, the equivalent capacitance for sub-period 3 is $C_{eq3} = 4C_o$. From this, the resonant frequency and time duration of sub-period 3 can be respectively calculated as $\omega_3 = \frac{1}{\sqrt{4LC_o}}$ and $T_3 = \frac{\pi}{\omega_3}$.

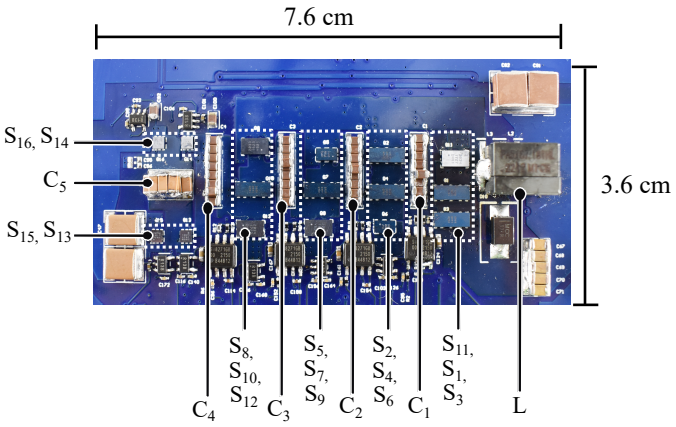

Fig. 7: Power stage of the hardware prototype that has passive storage elements and active devices labeled. Table I explains the detailed parameters for the annotated components.

TABLE I: Components for 1-to-10 CaSP

Component	Device	Parameters
S_1-S_4, S_7, S_{10}	EPC2020	60 V, 1.5 mΩ
S_5, S_6	EPC2053	100 V, 3.1 mΩ
S_8, S_9	EPC2033	150 V, 5 mΩ
S_{11}, S_{12}	EPC2034	200 V, 7 mΩ
S_{13}-S_{16}	EPC2050	350 V, 55 mΩ
C_1 - C_4	GRM21BR61H106KE43L	9 x 10 μF, 50 V, X5R, 0805
C_5	CGA5L3X7T2E224K160AA	8 x 0.22 μF, 250 V, X7T, 1206
L	PA5187.181HLT	180 nH, 55 A

IV. Hardware Validation and Experimental Results

Shown in Fig. 7 is an annotated photograph of the hardware 1-to-10 CaSP converter prototype. All active switching components are implemented with EPC Gallium nitride (GaN) devices. As shown in Fig. 5, the dc voltage rating of each switch varies from v_{in} to $5 \cdot v_{in}$. Therefore, a variety of switches with different voltage ratings may be used in order to optimize the power losses and efficiency of the system that are due to the active device circuitry. A wide variety of GaN switching devices were examined for individual blocking voltage categories. The $R_{ds,on}Q_g$ and $\frac{1}{\sqrt{R_{ds,on}C_{oss}}}$ products were calculated as figures of merit (FOMs) for each of the examined switches [25], [26]. The switches with the lowest FOMs for each blocking voltage category were chosen and are shown in Table I.

The 1-to-10 CaSP hardware has been validated up to 300 W with an output voltage of 350 V. Figure 8 demonstrates the efficiency vs. output power for the 1-to-10 CaSP. The CaSP is able to achieve a peak efficiency of 96.1% and a full load efficiency of 95.9%. Figure 9 displays the load regulation of the 1-to-10 CaSP between an output power of 50 to 300 W. At full load, the CaSP converter is within 97.6% of its desired output voltage of 350 V. Lastly, Fig. 10 displays the inductor current i_L and switch node voltage v_{sw} for 300 W of output power. The inductor current waveforms validates the possibility of achieving ZCS for the 1-to-10 CaSP converter.

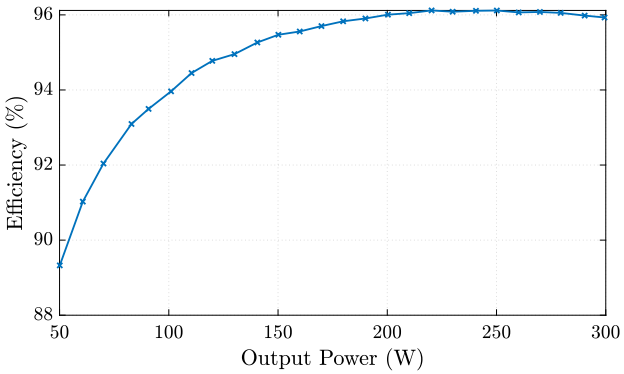

Fig. 8: Efficiency vs. output power for the CaSP converter performing a 35-to-350 V step-up.

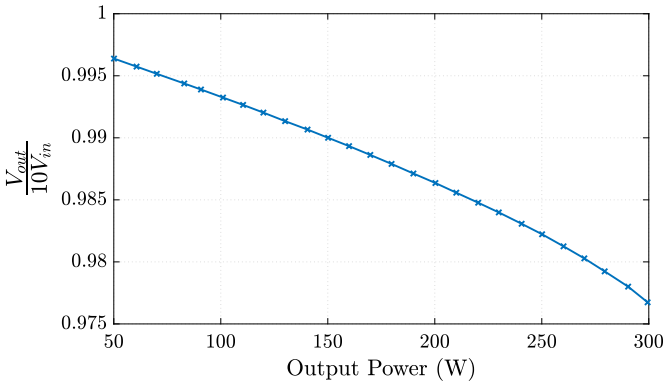

Fig. 9: Load regulation of the CaSP converter performing a 35-to-350 V step-up.

It can be seen that ZCS is achieved during the turn-on and turn-off of stage 3 and the turn-on of stage 2. The 1-to-10 CaSP converter has the ability to achieve complete ZCS for every turn-on and turn-off transition between each sub-period. However, in this hardware design there was a trade off between achieving ZCS for the transitions between sub-period two and one due to thermal stress with the EPC2050 devices. By reducing the dead time between the transitions of sub-periods two and one, the converter is able to experience ZCS. However, due to the small amount of dead time, it is expected that shoot-through between the complimentary devices occurs and thermally stresses the switches. To avoid this, the dead time was increased and undermined the ZCS performance.

V. Conclusion

In this manuscript, the operation of a high-voltage 1-to-10 cascaded series-parallel converter is presented. By following the analysis presented in [22], the CaSP converter is able to achieve a relatively low passive component volume and switching stress for high gain step-up and step-down dc-dc applications. The principle of operation of each of the sub-switching periods is explained with expressions provided for the sub-period duration and resonant frequencies. The theory of operation is validated with a high step-up and HV hardware prototype.

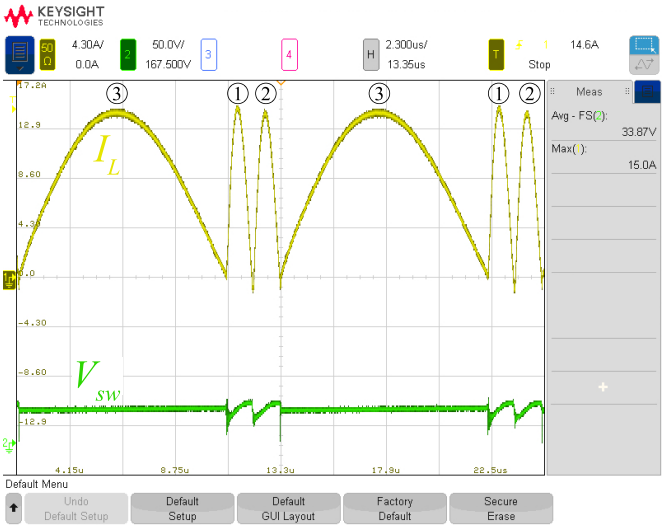

Fig. 10: Inductor current and switch node waveforms validating the ZCS operation of the 1-to-10 CaSP for a 35-to-350 V step-up at 300 W of output power.

References

[1] E. Serban, M. Ordonez, and C. Pondiche, "Dc-bus voltage range extension in 1500 v photovoltaic inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 901–917, 2015.

[2] *IQ8 and IQ8+ Microinverters*, Enphase, [Online] Datasheet available at www.enphase.com.

[3] J. Sun, H. Konishi, Y. Ogino, and M. Nakaoka, "Series resonant high-voltage zcs-pfm dc-dc converter for medical power electronics," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 3, 2000, pp. 1247–1252 vol.3.

[4] M. N. Adon, M. Noh Dalimin, M. M. Abdul Jamil, N. M. Kassim, and S. Hamdan, "Study of effect of microsecond pulsed electric fields on threshold area of hela cells," in *2012 IEEE-EMBS Conference on Biomedical Engineering and Sciences*, 2012, pp. 484–486.

[5] K. Saito, Y. Minamitani, and Y. Komatsu, "Investigation of selective sterilization of unnecessary microorganisms on pulsed electric field sterilization," in *2013 19th IEEE Pulsed Power Conference (PPC)*, 2013, pp. 1–5.

[6] N. Eghtedarpour and E. Farjah, "Distributed charge/discharge control of energy storages in a renewable-energy-based dc micro-grid," *IET Renewable Power Generation*, vol. 8, no. 1, pp. 45–57, 2014.

[7] F. Nejabatkhah and Y. W. Li, "Overview of power management strategies of hybrid ac/dc microgrid," *IEEE Transactions on power electronics*, vol. 30, no. 12, pp. 7072–7089, 2014.

[8] D. Miranda, "2020 NASA Technology Taxonomy," Tech. Rep., 2020.

[9] J. Zou, N. C. Brooks, S. Coday, N. M. Ellis, and R. C. Pilawa-Podgurski, "On the size and weight of passive components: Scaling trends for high-density power converter designs," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[10] R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, "High-efficiency dc-dc converter with high voltage gain and reduced switch stress," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 354–364, 2007.

[11] B. Sun, "Does gan have a body diode?-understanding the third quadrant operation of gan," *Application Report SNOAA36; Texas Instruments: Dallas, TX, USA*, 2019.

[12] S. Son, O. A. Montes, A. Junyent-Ferré, and M. Kim, "High step-up resonant dc/dc converter with balanced capacitor voltage for distributed generation systems," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4375–4387, 2019.

[13] P. Jia and Y. Mei, "Derivation and analysis of a secondary-side llc resonant converter for the high step-up applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5865–5882, 2021.

[14] F. Shang, G. Niu, and M. Krishnamurthy, "Design and analysis of a high-voltage-gain step-up resonant dc–dc converter for transportation applications," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, pp. 157–167, 2017.

[15] Z. Ye, R. A. Abramson, T. Ge, and R. C. N. Pilawa-Podgurski, "Multi-resonant switched-capacitor converter: Achieving high conversion ratio with reduced component number," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 492–507, 2022.

[16] P. H. McLaughlin, P. Aung Kyaw, M. H. Kiani, C. R. Sullivan, and J. T. Stauth, "Two-phase interleaved resonant switched-capacitor dc-dc converter with coupled inductors and custom lc resonator," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 37–44.

[17] R. Rizzolatti, C. Rainer, S. Saggini, and M. Ursino, "High density hybrid switched capacitor converter for data-center application," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1288–1293.

[18] R. Pilawa-Podgurski, D. Giuliano, and D. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *39th IEEE Power Electronics Specialists Conference*, 2008.

[19] T. Ge, R. Abramson, Z. Ye, and R. C. Pilawa-Podgurski, "Core size scaling law of two-phase coupled inductors – demonstration in a 48-to-1.8 v hybrid switched-capacitor mlb-pol converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1500–1505.

[20] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2020.

[21] R. A. Abramson, Z. Ye, T. Ge, and R. C. Pilawa-Podgurski, "A high performance 48-to-6 v multi-resonant cascaded series-parallel (casp) switched-capacitor converter," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1328–1334.

[22] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 903–10 919, 2022.

[23] W. C. Liu, Z. Ye, and R. C. Pilawa-Podgurski, "Comparative analysis on minimum output impedance of fixed-ratio hybrid switched capacitor converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2019, pp. 1–7.

[24] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," vol. 23, no. 2, pp. 841–851, 2008.

[25] J. T. Stauth, "Pathways to mm-scale dc-dc converters: Trends, opportunities, and limitations," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–8.

[26] J. A. Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.