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Ultra-wideband Gallium Nitride Electronics for Integrated Phase Array Systems

Author

Li, Yue

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Ultra-wideband Gallium Nitride Electronics for Integrated Phase Array Systems

A dissertation submitted in partial satisfaction

of the requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

Jerry Li

2024

ABSTRACT OF THE DISSERTATION

Ultra-wideband Gallium Nitride Electronics
for Integrated Phase Array Systems

by

Jerry Li

Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2024
Professor Yuanxun Ethan Wang, Chair

5G and Simultaneous Transmit and Receive (STAR) at radio frequency have led to an ever-increasing demand for physically smaller, wider bandwidth communication devices. In addition to civilian demand, electronic warfare also calls for robust RF systems that provide high fidelity communication and sensing in the presence of numerous interferences. Ultra-wideband Integrated Phased Array Systems are a major part of the solution to all this growing demand. Two components of particular interest to building an Ultra-wideband Integrated Phased Array System have been constructed with Gallium Nitride (GaN) transistors. The constructed circulator and power amplifier (PA) components both have excellent broadband, small-form factor, and scalability properties.

Using a switching network of transistors and transmission lines, it is possible to replicate the behavior of a traditional circulator. This constructed device, the Sequentially Switched Delay Line (SSDL), can overcome a circulator's conventional limitations in insertion loss, form factor and bandwidth. Using passive bootstrapping, it is possible to increase the power handling and

lower the insertion loss. Arranging SSDL devices in an array, it is possible to further raise the power handing and reduce distortions from the transistors' higher order intermodulation terms. The SSDL in a 3,4,..,N-port setting, can provide a non-reciprocal device for simultaneous transmit and receive at the same radio frequency. The SSDL can also be used as a gyrator in a 2-port setting; it can provide a wideband conversion of a capacitor into an inductor.

A new differential broadband GaN PA design for direct integration with a Tightly Coupled Dipole Array (TCDA) will also be discussed. Using differential amplifiers, the overall PA design can be made balun-less. Using direct integration to a TCDA load, the overall PA design can leverage the TCDA's common mode rejection of the second harmonic. Combining these design principles, the new integrated PA is also able to overcome conventional limitations in form factor and bandwidth.

The dissertation of Jerry Li is approved.

Gregory J. Pottie

Benjamin S. Williams

Chee Wei Wong

Yuanxun Wang, Committee Chair

University of California, Los Angeles

2024

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SYMBOLS AND ACRONYMS

ANT	Antenna
COTS	Commercial Off the Shelf
DMC	Distributed Modulated Capacitors
DPDT	Double Pole Double Throw
FOM	Figure of Merit
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
LO	Local Oscillator
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
Q factor	Quality Factor
RF	Radio Frequency
RFC	Radio Frequency Choke
RX	Receiver
SPDT	Single Pole Double Throw
SSDL	Sequentially Switched Delay Line
SW	Switching
TCDA	Tightly Coupled Dipole Array
TVTL	Time Varying Transmission Line
TX	Transmitter

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VITA

Education

2018-2024 Ph.D. candidate in Electrical Engineering

University of California, Los Angeles, CA USA

2017-2018 M.S. in Electrical and Computer Engineering

Worcester Polytechnic Institute, Worcester, MA, USA

2013-2017 B.S. (High Distinction) in Electrical and Computer Engineering

Worcester Polytechnic Institute, Worcester, MA, USA

Conferences

[1] Y. Li, J.P. Santos and Y.E. Wang, “Ultra-Wide Band Circulators for STAR Communications through Sequentially Switched Delayed Lines towards low losses” in 2021 IEEE-APS Topical Conference on Antennas and Propagation in Wireless Communications (APWC), doi: 10.1109/APWC52648.2021.9539646

Publications

[1] M. Biedka, Y. Li and Y. E. Wang, "Ultra-Wide Band On-Chip Circulator With Sequentially Switched Delay Lines (SSDL)," in IEEE Access, vol. 11, pp. 69033-69045, 2023, doi: 10.1109/ACCESS.2023.3268060.

[2] Y. Li and Y.E. Wang, “Balanced Sequentially Switched Delay Lines (SSDL) for further enhanced On-Chip Circulators” in IEEE Microwave and Wireless Technology Letters, in progress

[3] Y. Li, J.P. Santos and Y.E. Wang, “Sequentially Switched Delay Lines (SSDL) Gyrator for passive microwave component applications” in IEEE Microwave and Wireless Technology Letters, in progress

Chapter 1: Introduction

1.1 Overview

Electronic warfare and civilian services both demand smaller devices able to maintain high quality communication. Examples of proposed systems like Figure 1 have size bottlenecks at the transmit to receiver transition, phased array to power amplifier transition, and filters. These indicated locations in red generally correspond to where circulators, baluns, and RF/microwave band inductors are placed respectively. The form factor limitations can be overcome by further integration of components with the rest of the overall phased array system. Consequently, the bandwidth restrictions of the circulator, the balun and the high frequency band inductor by their form factor can also be overcome. In an overall complex transmit and receive system, using fundamental transistor and electromagnetic concepts, it is possible to design components to replace each component so that they are able to overcome traditional size and bandwidth restrictions

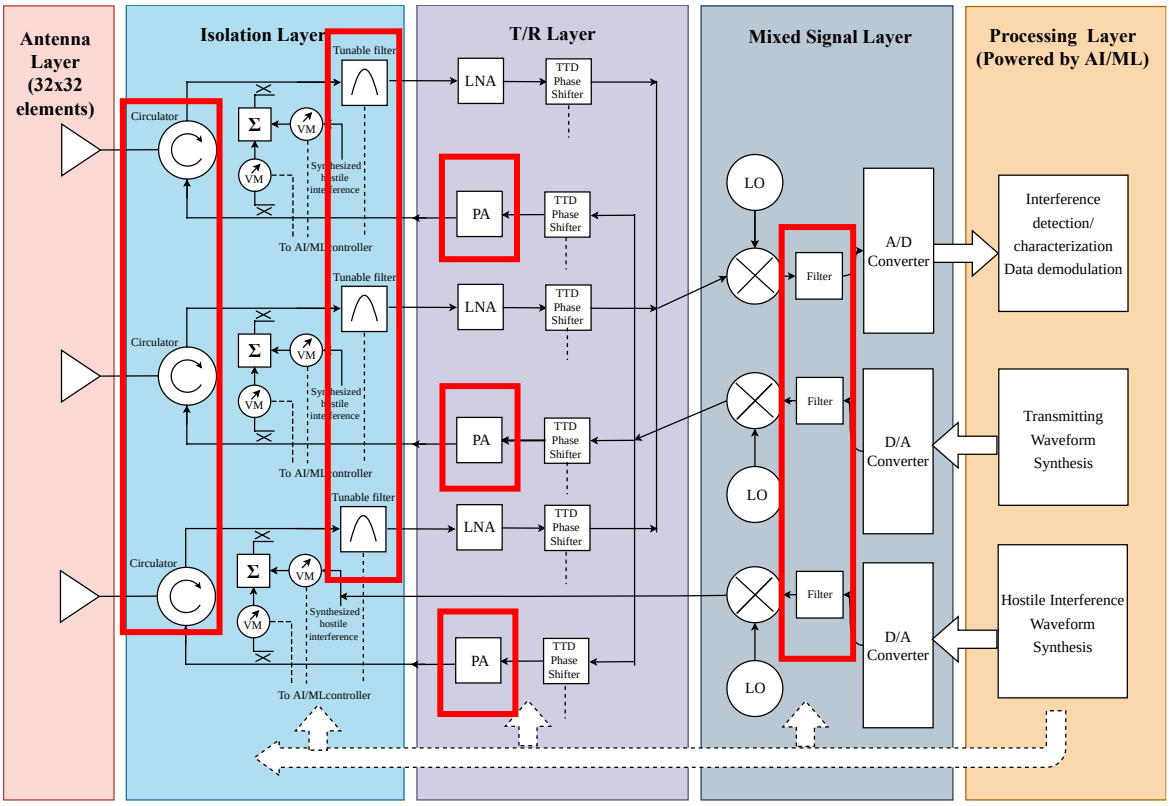


Figure 1 A proposed future phased array system for electronic warfare

1.2 Circulator

A circulator is a non-reciprocal 3 port device. A traditional ferromagnetic one achieves its non-reciprocity thanks to a property called Faraday rotation [1]. However, since its operational frequency range is dependent on the size resonant cavity, it is inherently limited to operation in a narrow bandwidth. Additionally, to have a circulator operating within the range of 500MHz to 2 GHz can require a resonant cavity size on the order of 15-60cm. For realizing a RF or microwave system this can be burdensome at best to impractical at worst. One can easily see in Figure 2 how a circulator is one of the largest components in an RF system.

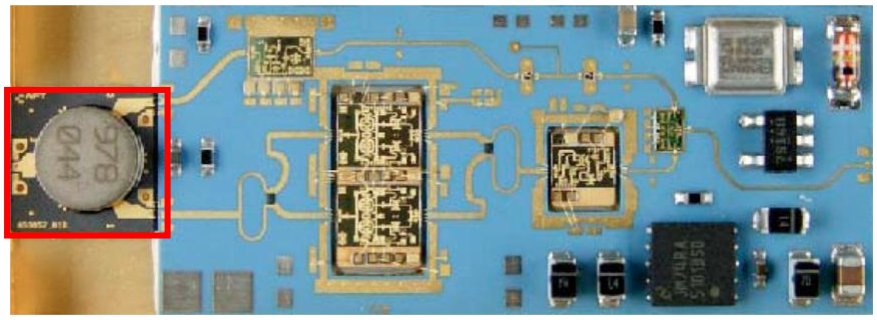


Figure 2 An RF system with an easily recognizable and large circulator

To further compound issues, a circulator is also traditionally one of the most lossy components in a RF system. Insertion loss in conventional circulators can be as high as 5dB! Its main purpose is often as a TX/RX module; it is near the beginning of both the transmit and receive signal chain. As a consequence of the high insertion loss in the circulator, both the TX and RX signal chain can potentially see severe degradation in noise figure.

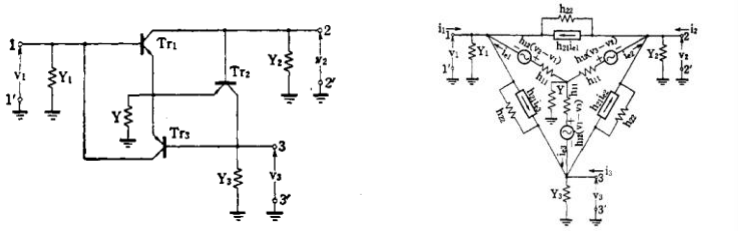


Figure 3 Active transistor gyrator (a) schematic (b) equivalent circuit

Magnetless circulators have been conceived of as early as 1965 as shown in Figure 3 [2]. However, they traditionally use transistors as amplifiers. This implies that they rely on the active device nature of the transistors to block signal backflow for nonreciprocity. At high frequencies, this option is no longer feasible due to leakage through capacitances. Hence the active transistor circulators have been limited to 100Hz-3MHz, significantly below RF applications and also suffer poor noise performance and linearity [2-4].

Luckily, a magnetless circulator can also be built using a network of transistors as switches and transmission lines called a Sequentially Switched Delay Line. Using careful switching, it will be shown later that it is possible to replicate the non-reciprocal behavior of a ferromagnetic circulator. Consequently, this magnetless circulator is no longer restricted in insertion loss, bandwidth, and size the way a ferromagnetic circulator is. The passive nature of the SSDL device also means it does not face the poor noise and linearity issues of an active transistor circulator.

1.3 Classical Antenna Design Principles

Traditional antenna design generally follows the textbook procedure:

1. Make the antenna resonate (tune the reactive component of the impedance to 0)
2. Match the antenna to a real impedance of 50 Ohms
3. In an antenna array, space the antenna elements $\lambda/2$ apart to avoid grating lobes from showing up due spatial aliasing

Unfortunately, this design process tends to be inherently narrowband. It is often difficult to beat a 2:1 bandwidth for the operating frequency due to impedance and size limitations [5].

1.4 Classical Power Amplifier Design Principles

Similarly, traditional power amplifier design generally follows the textbook procedure:

1. Load Pull the optimal output for efficiency
2. Source Pull the optimal input for noise figure

3. Use lumped conjugate matching components to connect input and output to 50 Ohms

This process also is inherently narrowband design due to lumped components being used [1].

1.5 Phased Array Components

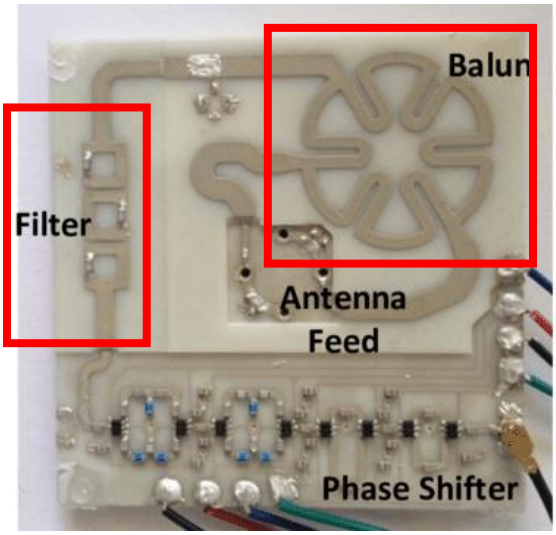
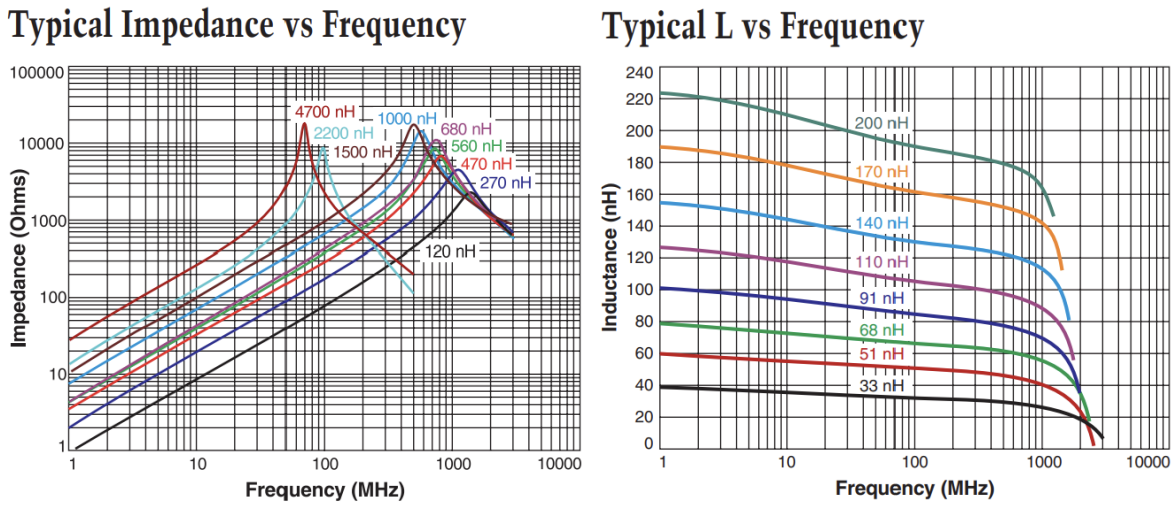


Figure 4 A typical phase array system noticeably size restricted by its balun and filter size

An overall phase array system introduces further narrowband constraints in its balun and filter(s). Phased arrays sizes also tend to be large due to requiring a balun as shown in Figure 4, [6]. A balun is generally necessary since it is used to connect an often differentially connected antenna element with an often single-ended antenna feed. Baluns are generally composed of either ferrite material or a λ/4 Pawsey stub. Once again, both popular options have inherent size and bandwidth restrictions when operating at RF frequency.

The phased array and balun are usually then connected to the preceding matching network designed for a power amplifier for optimal efficiency and noise figure. In addition to the matching network, the radio frequency choke (RFC) inductors used in the biasing network for the PA may yet introduce more narrowband and size restrictions. These same inductor size

restrictions can also affect the floor plan of filters used in a phased array system as shown in Figure 4. Figure 5 shows that there is a particularly prevalent lack of lumped inductors with stable inductance values in the 100MHz to 1 GHz range. The 10-30nH range is especially difficult to find in this frequency range.



(a) (b)

Figure 5 Common Coilcraft Lumped Inductor Values (a) 120nH-4700nH, (b) 33nH- 200nH

However, it is possible to shrink the size and improve the bandwidth of the overall phased array system by:

1. Using differential amplifiers to remove the use of the balun
2. Having inductors made of transmission line or converted over from a lumped capacitor with a gyrator in filters, biasing, and matching networks.
3. Using a Tightly Coupled Dipole Array (TCDA) load's inherent low profile and high common mode impedance behaving like an open circuit to load the power amplifier.

Thus, by constructing an integrated phased array, the form factor of the array can be reduced dramatically. This integrated phased array also has the additional benefit of 2nd harmonic rejection in the differential power amplifier just by loading it with a TCDA which greatly boosts the overall broadband amplifier efficiency.

1.6 Gallium Nitride

Gallium Nitride (GaN) transistors were selected for the usage in both devices. Since 5G and electronic warfare may demand high power consumption, components with high power handling are required. The III-V direct semiconductor GaN has a wide bandgap energy of 3.4 eV at room temperature. This wideband gap gives rise to many desirable properties such as high breakdown voltage and charge carrier saturation velocity.

As summarized by Table 1, GaN transistor has one of the highest Johnson's Figure of Merits [6,7] normalize to silicon for high power and high frequency application.

Material	Saturation Velocity [m/s]	Breakdown Voltage [MV/cm]	Johnson's Figure of Merit
Silicon	1.0×10^5	0.3	1
Silicon Carbide	2.0×10^5	3.5	20
Indium Phosphide	0.67×10^5	0.5	0.33
Gallium Arsenide	1.5×10^5	0.4	2.7
Gallium Nitride	2.5×10^5	3.3	27.5

Table 1 The Johnson's Figure of Merit of various semiconductors normalized to silicon

Chapter 2: Sequentially Switched Delay Lines

2.1 Basic SSDL theory

SSDLs fall under a category called time varying electromagnetic device. By physically changing the impedance of components of the device over time as shown in Figure 6, that device can behave like a circulator.

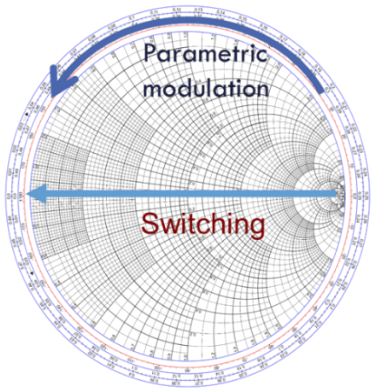


Figure 6 Changing impedance of time varying electromagnetic devices

The most common time varying electromagnetic devices fall under two categories: parametric modulation and switching. Time-Varying Transmission Line (TVTL) is an example of parametric modulation. By varying the capacitance of its distributed modulated capacitors (DMC) along the transmission line [8], it is possible to create a non-reciprocal device.

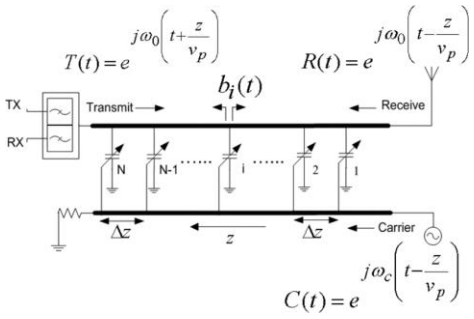


Figure 7 Time-varying transmission line

The SSDL is a case of the switching category of time varying electromagnetic devices. Using switching to break symmetry also allows achieving non-reciprocity [9]. Analysis of the 3-port, 4-port and later 2-port cases will be examined, though the SSDL can be extended to an N-port [10], with sufficient switches and transmission lines.

2.1.1 3-port Case

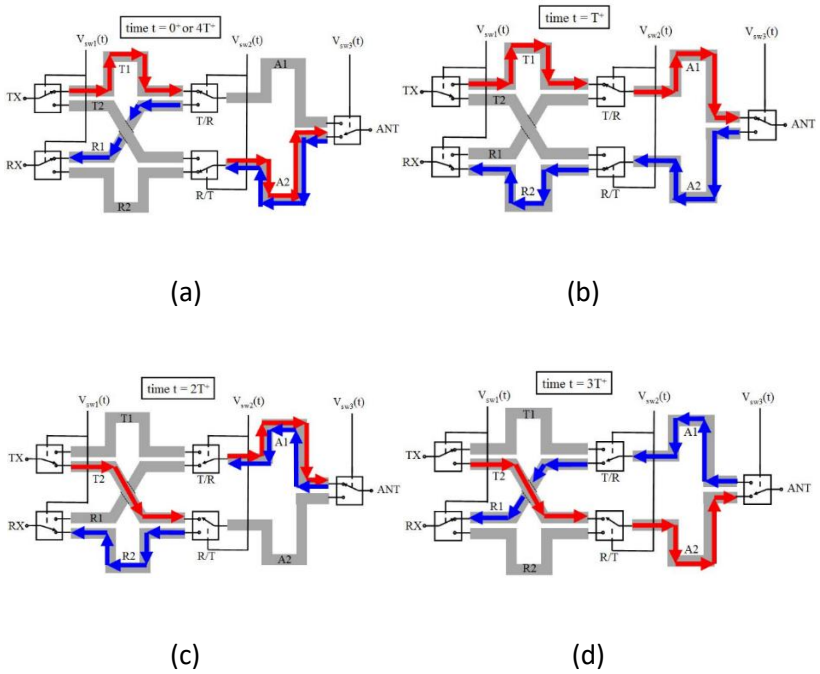


Figure 8 Timing Diagram of the signal immediately after switching at (a) 0+, (b) T+, (c) 2T+, (d) 3T+ of a 3-port, 6-line SSDL

By inspection, one can observe in Figure 8 (a)-(d) that:

1. The signal segment from the TX port will finish arriving at the ANT port after 2T since its transmission start
2. The signal segment from the ANT port will finish arriving at the RX port after 2T since its transmission start

3. The signal segment from the TX port will finish arriving at the RX port after 6T since its transmission start

These observations can be summarized by equations (1)-(3), which is the equivalent behavior of an asymmetric circulator as shown in Figure 9

$$ANT1^{-}(t) = TX^{+}(t - 2T) \quad (1)$$

$$RX^{-}(t) = ANT1^{+}(t - 2T) \quad (2)$$

$$TX^{-}(t) = ANT^{+}(t - 6T) \quad (3)$$

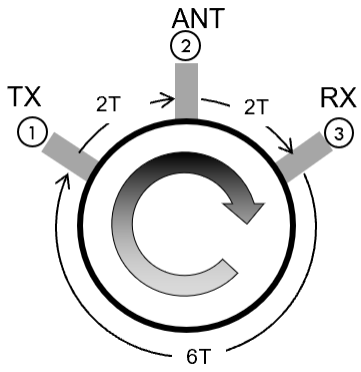


Figure 9 Conventional 3-Port Circulator diagram

It can also be observed that the only condition of operation is that the switching timing must be synchronized with the time delay, thus the theoretical bandwidth is infinite if aliasing is permitted. It is also possible to simplify the 6-line SSDL into a 2-line SSDL if the single pole double throw (SPDT) switches connecting the TX and RX ports to the transmission line are replace with double pole double throw switches (DPDT) as observed in Figure 10 (a)-(d)

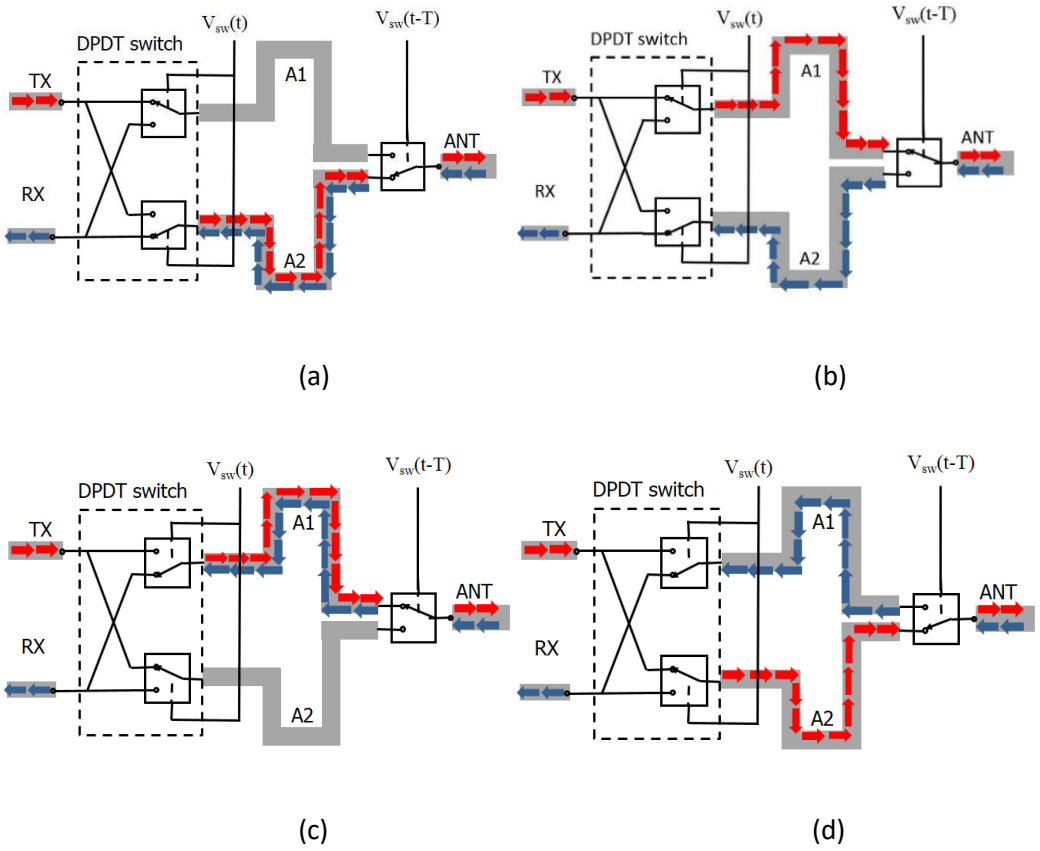


Figure 10 Timing Diagram of the signal immediately after switching at (a) 0+, (b) T+, (c) 2T+, (d) 3T+ of a 3-port, 2-line SSDL

The timing diagram in Figure 9 illustrates the process of wave propagation at the four switching moments of each cycle. Note that the transmitted and received waves are represented respectively by the colors red and blue. The TX, ANT, and RX ports are connected to the correct transmission line for a time of 2T. Each timing instance will be explained with respect to the switching action of the double-pole double-throw (DPDT) switch. Figure 10 (a) represents the locations of the transmitted and received waves at time 0+. The (+) sign indicates that the devices have just completed their switching action. The DPDT switch has just connected the TX and RX ports to transmission lines A1 and A2, respectively. The ANT port switch has been on for a time T+. This allows for the first received pulse to begin populating A2 simultaneously

with the tail end of the second transmitted pulse, which arrives at the ANT port. The transmitted and received waves that occupy A2 at the same time do not interfere with each other because they travel toward different directions. Next, we progress in time to Figure 10 (b), which is a time snapshot at T+. In this case, the DPDT switch stays in its same position while the ANT port switch connects to A1. Here, the first transmitted pulse can be seen starting along A1 which will be sent out through the ANT switch. At the same time, the first received pulse is seen completing its journey to the RX port. It is important to note that right before the ANT port switch flipped, the tail end of the second transmitted pulse was captured at the ANT port. As time moves forward to Figure 10 (c), the switch positions are now seen at time 2T+. The DPDT switch flips its orientation after being in its previous state for a time 2T. Now, the TX and RX ports are respectively connected to transmission lines A2 and A1. The first transmitted pulse now completes its journey along A1 and out through the ANT port. Also, the second received pulse begins to traverse A1. As time advances further, the positions of the transmitted and received waves in the circulator are seen at time 3T+ in Figure 10 (d). Here, the ANT port switch connects to transmission line A2 after being in its previous state for a time of 2T. Here, the second transmitted pulse starts to propagate along A2 while the second received pulse completes its journey along transmission line A1. As time progresses further, the switches and positions of the TX and RX signal pulses match those of Figure 10 (a).

2.1.2 4-port Case

By replacing the SPDT switch near the ANT port with a DPDT switch and adding an additional port, ANT2, A 4-port circulator is produced. Figure 11 (a)-(g) demonstrates the timing process of the signal flow.

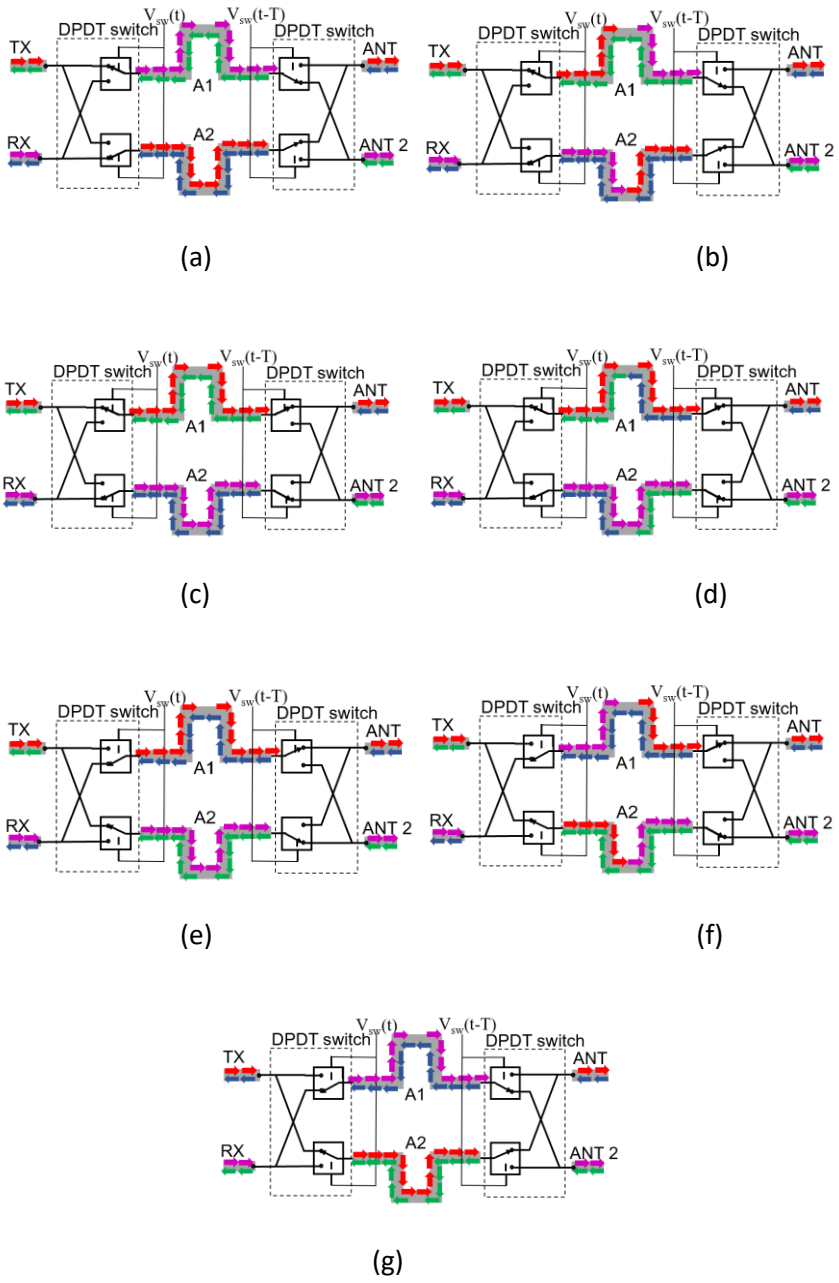


Figure 11 Timing Diagram of the signal at (a) 0+, (b) 0.5T, (c) T+, (d)1.5T, (e) 2T+, (f) 2.5T, (g) 3T+ of a 4-port, 2-line SSDL

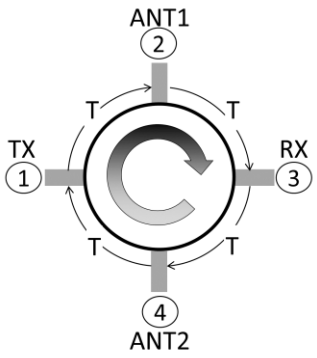


Figure 12 Equivalent 4-port circulator

Equations (4)-(7) and Figure 12 summarize the overall 4-port behavior. A S-parameters matrix, equation (8) can further simplify the overall signal flow. It can then be noted that by terminating one of the 4 ports with a matched load, the 4-port circulator simplifies once again into the 3-port circulator shown in Figure 9 (a)-(d).

$$ANT1^{-}(t) = TX^{+}(t-T) \quad (4)$$

$$RX^{-}(t) = ANT1^{+}(t-T) \quad (5)$$

$$ANT2^{-}(t) = RX^{+}(t-T) \quad (6)$$

$$TX^{-}(t) = ANT2^{+}(t-T) \quad (7)$$

$$[S] = \begin{bmatrix} 0 & 0 & 0 & e^{-jT} \\ e^{-jT} & 0 & 0 & 0 \\ 0 & e^{-jT} & 0 & 0 \\ 0 & 0 & e^{-jT} & 0 \end{bmatrix} \quad (8)$$

It can then be shown that a SSDL any number of ports is constructable given enough transmission lines, throws and poles per switches [10]. All the cases examined are summarized in Figure 13(a)-(c).

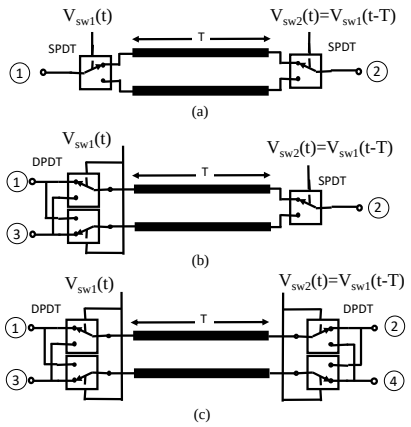


Figure 13 (a) 2-Port: Gyrator, (b) 3-Port: Circulator, (c) 4-Port: Circulator

2.2 Existing Prototypes

As shown in Figure 14, previous work [11][12] produced a working prototype SSDL was achievable for use as 3-port circulators. Initial testing was performed at 0.2 to 200MHz with a switching rate of 6MHz (this corresponds to a delay of 44ns for each transmission line). The best results at the time yielded 5-10dB insertion loss and 40dB of isolation.

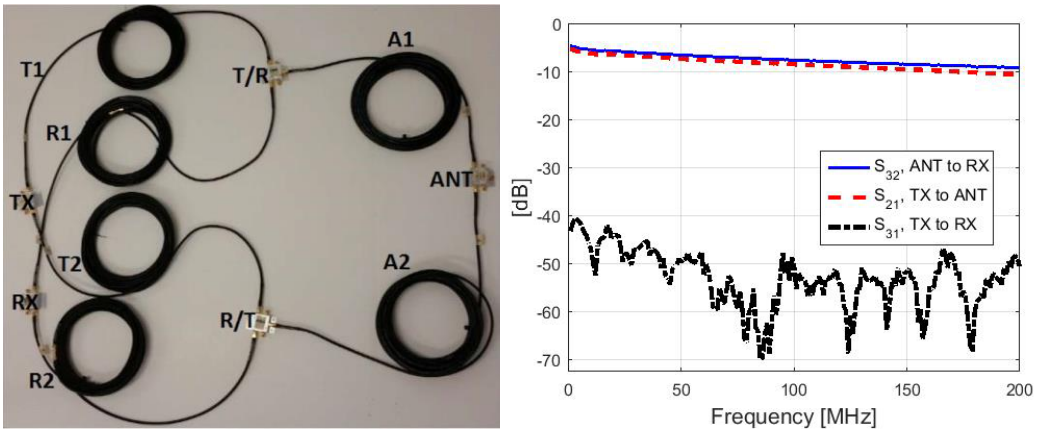


Figure 14 (a) Commercial off the shelf (COTS) parts proof of concept of the SSDL, (b) Corresponding measurements

Further progress showed as shown in Figure 15 to producing a SSDL on MMIC. With better figure of merit switches, the switching rate was increased to 1.25GHz and 2.5 GHz and

insertion loss improved to 2.7dB to 5.4dB from DC to 1GHz. Isolation was 18dB to 38dB from DC to 1GHz while the maximum P1dB is 11dBm. It was surmised that at a higher frequency the gate resistance of each transistor was no longer high enough to block unwanted turning ON/OFF at the gate voltage from RF signal leaking through, the self-turning on effect. This occurs when the gate voltage is set to pinch off yet the RF voltage swing across the drain and source during the turning-off states reach to a threshold so that the Vgs or Vgd may become greater than the pinch-off voltage. The self-turning on effects limit the power handling of switches to a level much lower than what the break down voltage or the maximum power dissipation the device allows.

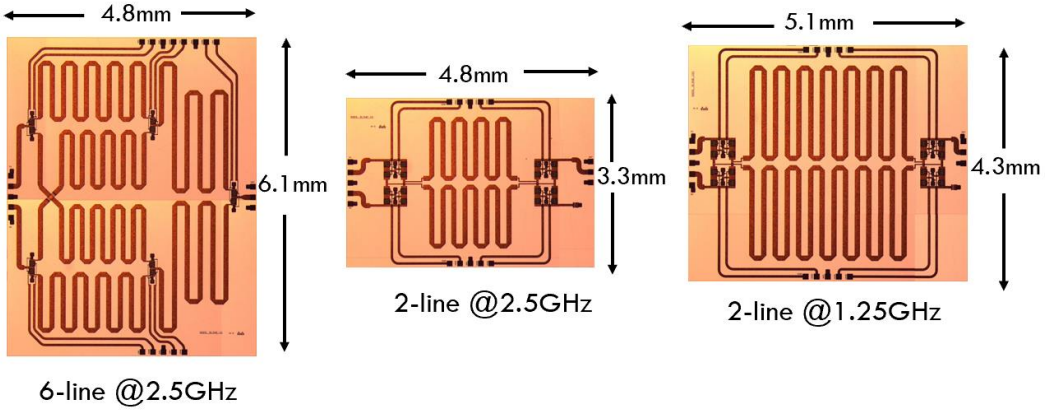


Figure 15 Various MMIC implementations SSDL

2.3 Theoretical limit

Compared to RF circulators made of magnetic materials, the insertion loss of the existing non-magnetic circulator prototypes are generally higher. Hence, it is important to understand the theoretical limit of SSDL circulator insertion loss for a given switch technology. The analysis carried out here assumes there is no leakage of the signal to the control path and that the insertion

loss is only contributed by the on-resistance and the off-capacitance of the switch. The transistor that is used to construct a switch has a technology dependent figure of merit defined as,

$$f_{FOM} = \frac{1}{2\pi R_{on} C_{off}} \tag{9}$$

where R_{on} is the on-resistance and the off-capacitance C_{off} of the transistor and the input power into the SSDL circulator can be defined as,

$$P_{input} = \frac{1}{2} I^2 Z_0 \tag{10}$$

where I is the current flowing on the transmission line and Z_0 is the characteristic impedance of the transmission line. For the single series switch, every time the switch is turned on from off, the energy stored in the off-capacitance of the transistor is lost. During one switching cycle of 4T, the transitions from off to on states in each DPDT switch happens once for all four transistors, which leads the capacitive power loss given by

$$P_{loss}^{C} = \frac{1}{2} f_s C_{off} V^2 \cdot 4 = \frac{1}{2} I^2 \cdot 4 f_s C_{off} Z_0^2 \tag{10}$$

where f is the switching frequency and the Ohmic loss at the switch is,

$$P_{loss}^{R} = \frac{1}{2} I^2 R_{on} \tag{11}$$

as the wave encounters the on-resistance of one transistor at any given time. The power lost in each DPDT switch is thus given by summing the capacitive power loss in (10) with the Ohmic power loss in (12),

$$P_{loss} = \frac{1}{2} I^2 \left(4 f_s C_{off} Z_0^2 + R_{on}\right) \tag{12}$$

The fractional power loss is then derived as:

$$\frac{P_{loss}}{P_{input}} = 4f_s C_{off} Z_0 + \frac{R_{on}}{Z_0} \tag{13}$$

It is noted that the two loss terms in (13) have a fixed product, therefore the minimum insertion loss is achieved when these two terms are equal (14).

$$\frac{R_{on}}{Z_0} = 4f_s C_{off} Z_0 \tag{14}$$

With some basic algebra dividing both sides by Z_0 (15).

$$\frac{R_{on}}{Z_0^2} = 4f_s C_{off} \tag{15}$$

Then multiplying both sides Ron, it can be found that:

$$\left(\frac{R_{on}}{Z_0}\right)^2 = 4f_s C_{off} R_{on} = \frac{2f_s}{\pi f_{FOM}} \tag{16}$$

Therefore, the optimum condition for switch design is to choose the periphery of the transistor to make

$$R_{on} = Z_0 \sqrt{\frac{2f_s}{\pi f_{FOM}}} \tag{17}$$

With this optimum matching condition and taking account of the fact two DPDT switches are needed in the SSDL, the fundamental limit of SSDL circulator insertion loss is defined as:

$$IL = 1 - 2\frac{P_{loss}}{P_{input}} = 1 - 4\frac{R_{on}}{Z_0} = 1 - 4\sqrt{\frac{2f_s}{\pi f_{FOM}}} \tag{18}$$

For example, the NGAS 0.2μm GaN MMIC process that was used, a typical transistor has an on-resistance of 4 Ohm-mm and an off-capacitance of 0.31pF/mm, which gives a switch figure of

merit of 128GHz. At the switching frequency of 1.25GHz and a 50Ohm reference impedance system, the optimum on-resistance of the switch should be,

$$R_{on} = Z_0 \sqrt{\frac{2f_s}{\pi f_{FOM}}} = 4\ \Omega \cdot mm \tag{19}$$

Under this optimum match, the insertion loss given by (18) is 1.65dB. Measurement results shown later get close to these derived predictions. It is also evident from (18) that the insertion loss can be further reduced when technology with a higher switch figure of merit is used.

Table 2 list of some potential transistors with even higher figure of merits including a higher quality NGAS 0.2 µm GaN MMIC process (The transistors used in the SSDL unfortunately were accidently fabricated with a thicker resistive layer than intended leading to a higher on-resistance). From these equations and table 2, one can expect SSDL results can still be pushed further with a better NGAS 0.2 µm GaN MMIC process or other higher switch figure of merit transistor options.

It should be noted that while the MACOM GaAs transistor has a competitive figure of merit leading to potentially high bandwidth and low insertion loss, its designers have explicitly stated it has lower power handling even compared to silicon in passive device application (such as switching in a SSDL) [13]. This restriction makes it less appealing for future work compared to InP, GaN and other even higher bandgap energy semiconductors.

Technology	R_{on}	C_{off}	Figure of Merit $(\frac{1}{2\pi R_{on} C_{off}})$	Q-factor at 1.25GHz
MACOM GaAs	4.2 Ohm	0.08 pF	474 GHz	378.94
NGAS 0.2 µm GaN	1.8 Ohm	0.378 pF	234 GHz	187.13
HRL T3 40nm GaN	1.89 Ohm	0.241 pF	350 GHz	279.53
Teledyne 300nm GaN	0.34 Ohm	0.4 pF	1.17 THz	936.21
NGAS 25nm InP	0.32 Ohm	0.332 pF	1.5 THz	1198.46

Table 2 Transistor Figure of Merits

2.4 Bootstrap SSDL

To overcome the power compression limitations of the existing SSDL, a high-Q impedance is at the gate of each switch to reintroduce the high Rg present at lower switching frequencies as shown in Figure 16 (b). The impedance response versus frequency for a series LC resonator creates a low impedance at resonance, and a high impedance out of band. This means that the switching signal can be passed to the gate, yet the RF signal will see a high impedance looking into the gate and continue across the drain-source as intended. A schematic of the SSDL with passive bootstrapping is presented below in Figure 17 (a), which shows a cascade of four inductors with one capacitor to realize the needed Q for the LC tank, where L1 has a value of 11nH at 1.25GHz and L2 has a value of 10nH at 1.25GHz. C is 235fF. Thus, the self-turning on effect can be mitigated.

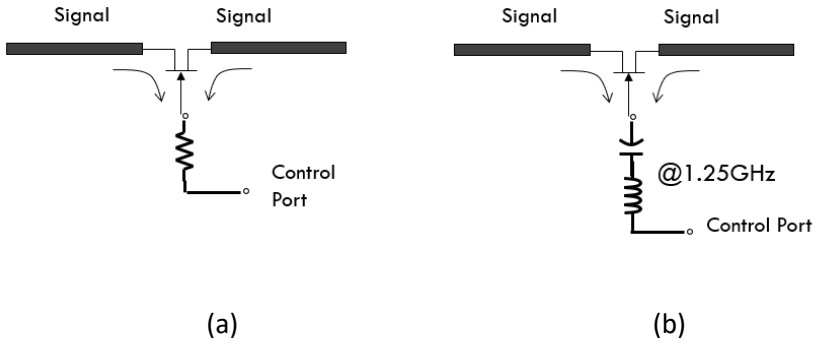


Figure 16 The passive bootstrap, (a) conventional low frequency implementation, (b) RF frequency implementation

As shown in Figure 17 (b), the series LC passive bootstrap is achieved by implementing spiral inductors and pad capacitors available from the existing NGAS 0.2um GaN MMIC process. It's worth noting that the additional passive bootstrapping minimally increases the overall form factor of the MMIC circulator compared with implementations from Figure 15.

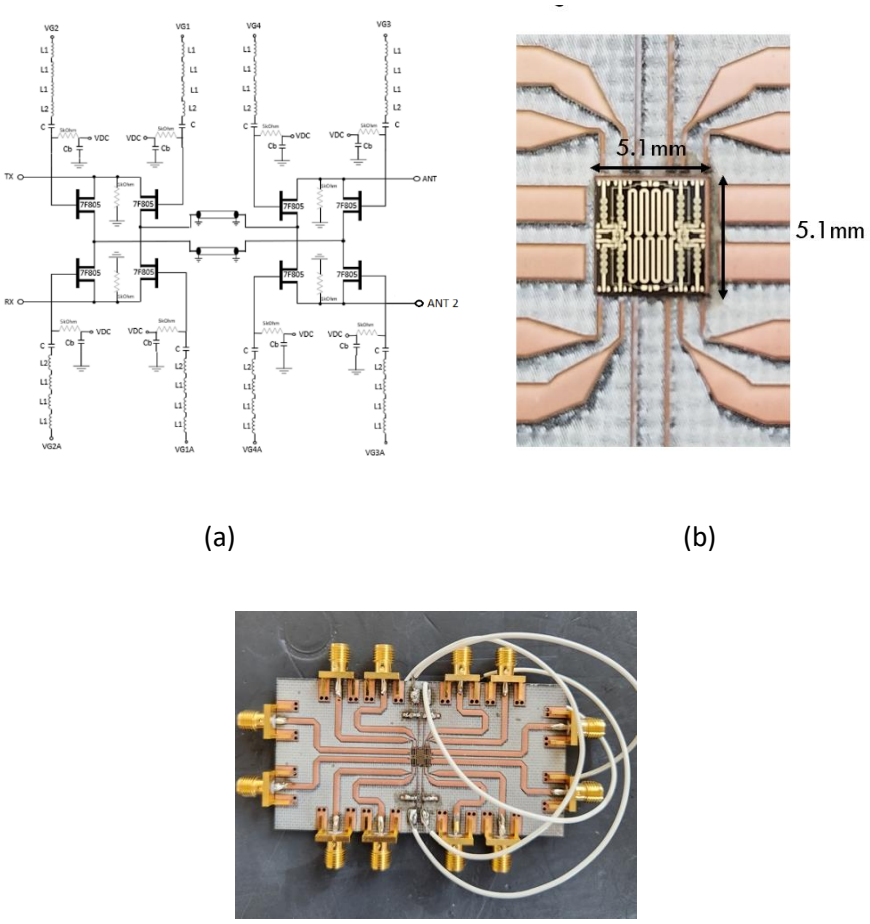
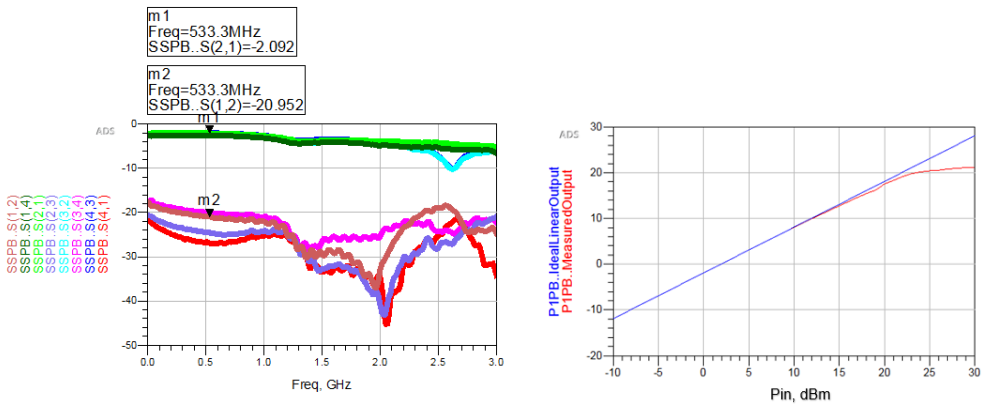


Figure 17 Passive LC bootstrap (a) schematic, (b) MMIC, (c) PCB measurement test board

When measured, the resulting SSDL performance was significantly better than prior SSDL implementations. Shown in Figure 18 (a), The insertion loss remained below 2.1dB from DC to 533.3 MHz while remaining below 3dB up to 1GHz. Difference from the theoretical insertion loss of 1.65dB can mostly be accounted for by the RO4003C PCB transmission lines connecting the SSDL off the chip to the SMA connectors on the measurement board. Meanwhile, the isolation retained being at least 18dB or greater like prior SSDL prototypes.



(a) (b)

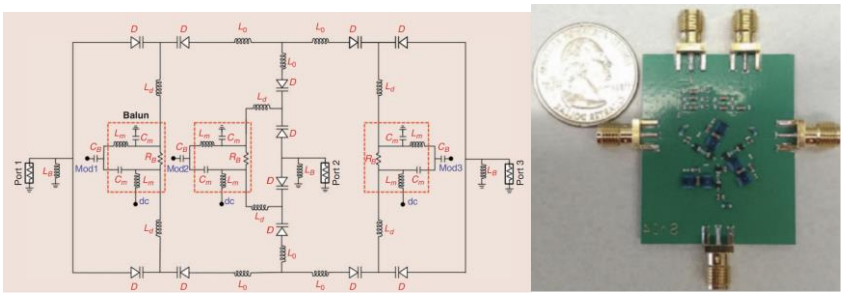
Figure 18 (a) Insertion loss and Isolation, (b) P1dB of the 4-port passive bootstrap SSDL

Most impressive were the power compression results shown in Figure 18 (b). Thanks to the passive bootstrap, the P1dB point was moved from 11dBm to just over 20dBm! Table 3 summarizes a comparison of this passive bootstrap implementation against other magnetless circulator implementations.

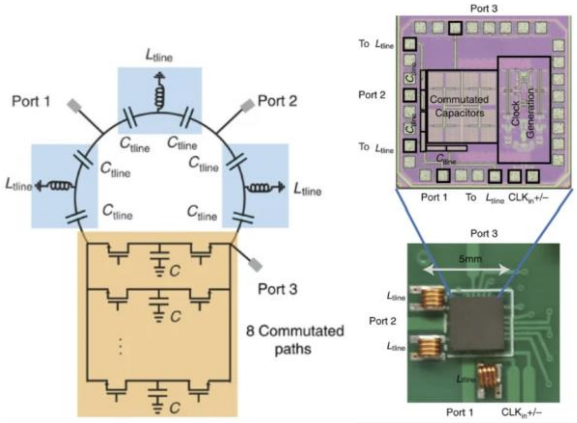
Circulator	[14]	[15]	[16]	[17]	[18]	This work (Passive Bootstrap)
Technology	180nm Silicon	65nm Silicon	65nm Silicon	180nm Silicon	45nm Silicon	200nm GaN
Frequency Range	421MHz-446MHz	600MHz-900MHz	61MHz-975MHz	0.86GHz-1.08GHz	22.7GHz-27.3GHz	10MHz-1GHz
Isolation (dB)	20-50	9.6-50	10.1-33	25	9-20.2	19-30
Insertion Loss (dB)	2-4.6	1.7-3.3	1.8-3	2.1(TX)/2.9(RX)	3.2-8.7	2.1 -3
P1dB (dBm)	28	N/A	N/A	30(TX)/21(RX)	21.5	20.5
IIP3 (dBm)	N/A	27.5	30	5(TX)/37(RX)	N/A	27
Device Area	11mm x 13mm	0.32 mm x 0.32mm	0.32mm x 0.65mm	16.5mm^2	1.2mm x 1.8mm	4.9mm x 5.1mm

Table 3 Comparison of magnetless circulators

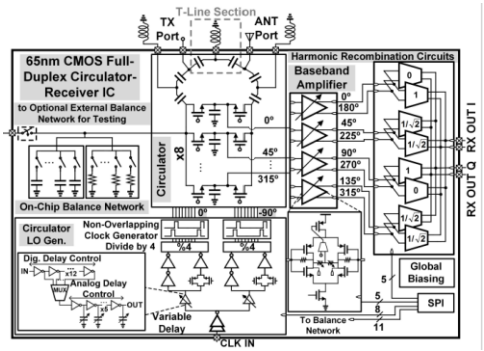
In Figure 19 the contrasting architectures of the various magnetless circulators mentioned in Table 3. It can easily be seen that all have a far more complex design compared with Figure 17 while not necessarily being able to outperform the SSDL in bandwidth, insertion loss, isolation and P1dB.

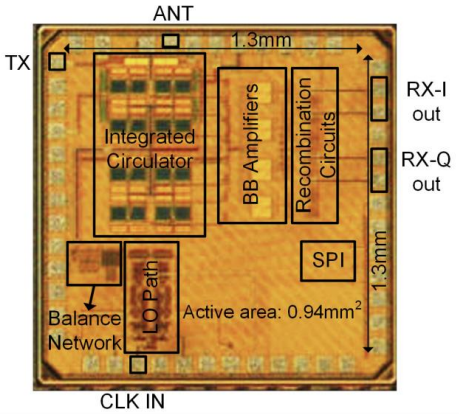


(a) (b)

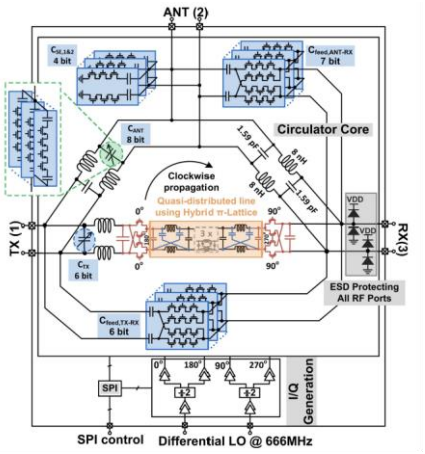


(c) (d)

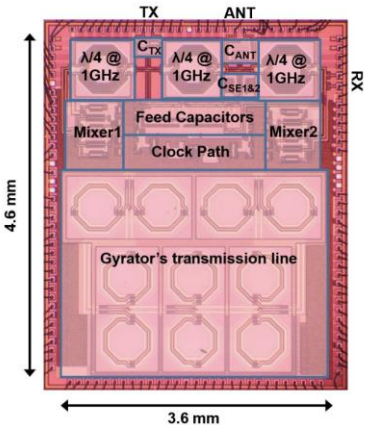




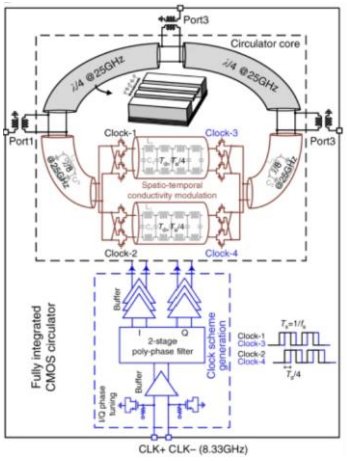
(e) (f)



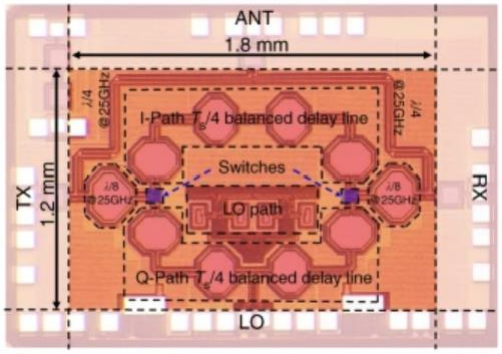
(g)



(h)



(i)



(j)

Figure 19 Various other magnetless circulators:

[14] A. Kord, et. al schematic (a) and layout (b),

[15] N. Reiskarimian and H. Krishnaswamy schematic (c) and layout (d),

[16] N. Reiskarimian, et al schematic (e) and layout (f),

[17] A. Nagulu and H. Krishnaswamy schematic (g) and layout (h),

[18] Dinc, T., et al schematic (i) and layout (j),

2.5 Intermodulation terms/Switching Noise in the SSDL

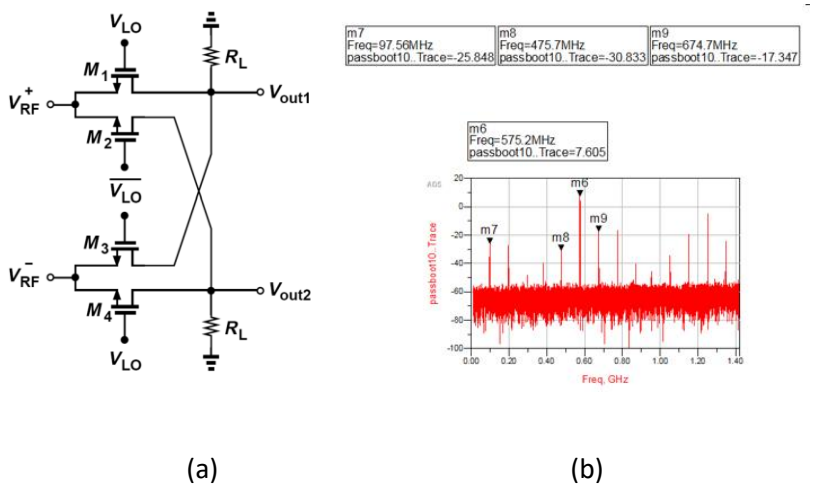
Unfortunately, an unaddressed issue remains with the SSDL circulator thus far. Since the infinite theoretical bandwidth was tied to the assumption that spectral aliasing is permitted, intermodulation problems have not been addressed thus far. In a broad overview, the SSDL allows an RF signal to go from one port to another port while enforcing nonreciprocity. Since the transistors are being switched on and off at a higher switching frequency than the RF signal, one half of the SSDL in Figure 17 (a) is roughly the same architecture as a passive up-conversion mixer like the one shown in Figure 20, [19].

f_{RF} =575.8MHz	f_{LO}=1.25GHz		
Order	Intermod. Products	Frequency (MHz)	Magnitude (dB)
2nd Order	f_{LO}-f_{RF}	674.2	-17.3
3rd Order	$2f_{RF}$-f_{LO}	(-)98.4	-25.8
4th Order	$3f_{RF}$-f_{LO}	477.8	-30.8

Table 4 Intermodulation product analysis of the passive bootstrap SSDL with a 10dBm Input RF signal

One can observe that the switching signal has been unintentionally used an LO frequency to generate unwanted intermodulation terms. Analysis of intermodulation terms in Table 4 and Figure 20 (b), show that the SSDL is already significantly at moderate power levels still under its P1dB point (measured at 10dBm input in the picture). Since these intermodulation terms are higher order than the intended signal, they will eventually overtake the signal and pose an issue of severely desensitizing the SSDL before it's P1dB. In prior SSDL art in Figure 14 and 15, the

P1dB point was not as high and the insertion loss was significantly greater such that this intermodulation problem was not yet relevant [11,12]. Since the bandwidth of those early devices were also much narrower, a low pass or bandpass filter sufficed for blocking the spurs. While a bandpass filter could still be implemented after the passive bootstrap SSDL, the overall insertion loss and bandwidth would suffer dramatically which would defeat the purpose of the passive bootstrap architecture. Luckily, an ingenious, scalable way of addressing this issue does exist.



(a) (b)

Figure 20 (a) A conventional passive up-conversion mixer, (b) intermodulation terms from unintentional mixing of SSDL RF signal with switching signal

2.6 Array/ Balanced arrangement of passive bootstrap SSDL

2.6.1 Theory

To remove the unwanted intermodulation terms of the switching and simultaneously further boost the power compression point, a 2-element array configuration of passive bootstrap SSDL is introduced. Both SSDL MMIC are biased under the same conditions, however the switching control network for the second SSDL is set 180° out phase with respect to the switching network

of the first SSDL. COTS splitters/combines at each of the 3 ports split at the entering port and then recombine the signal at the respective existing port as shown in Figure 21 (b).

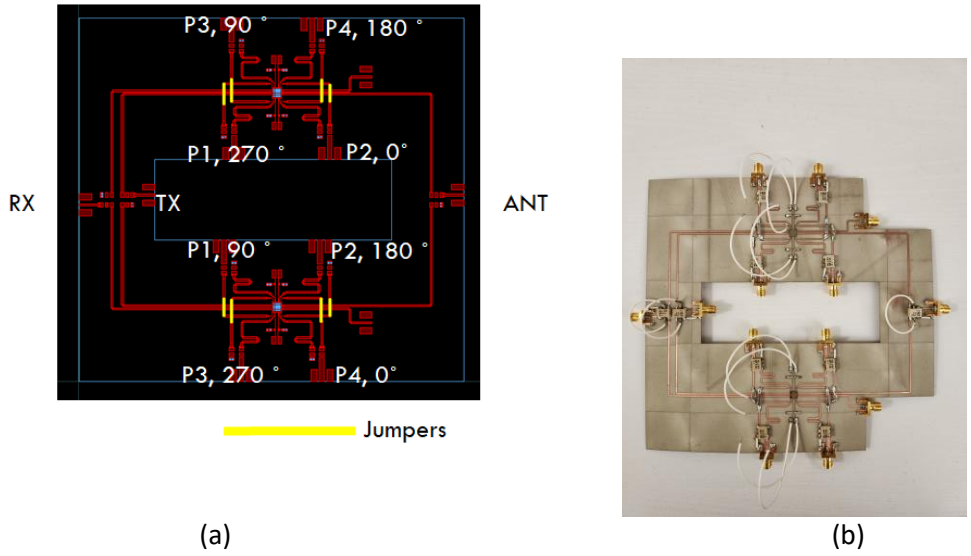


Figure 21 Passive bootstrap SSDL array (a) schematic, (b) test board

Derivation the intermodulation cancellation goes as follows. The intermodulation terms are a result the passive mixing by each transistor

$$Y_{intermod_{out}}(\omega t) = X_{RF_{signal}}(\omega t) * X_{Switching}(\omega t) \tag{20}$$

where $X_{RF_{signal}}(\omega t) = V_a \cos(\omega t)$

Approximate square wave switching signal as first 3 terms,

$$X_{Switching}(\omega t) = \frac{4V_b}{\pi}\cos(\omega t) - \frac{4V_b}{3\pi}\cos(3\omega t) + \frac{4V_b}{5\pi}\cos(5\omega t) \ldots \tag{21}$$

The intermodulation can be approximated with:

$$Y_{intermod_{out}}(\omega t) = X_{RF_{signal}}(\omega t) * X_{Switching}(\omega t) \tag{22}$$

$$Y_{intermod_{out}}(\omega t) = V_a \cos(\omega t) * \frac{4V_b}{\pi}\cos(\omega t) - V_a \cos(\omega t) \ * \frac{4V_b}{3\pi}\cos(3\omega t) - V_a \cos(\omega t) * \frac{4V_b}{5\pi} \cos(5\omega t) \ldots \quad (23)$$

Now modelling the second switching signal as shifted 180°:

$$X_{Switching2}(\omega t) = \frac{4V_b}{\pi}\cos(\omega t + 180°) - \frac{4V_b}{3\pi}\cos(3\omega t + 180°) + \frac{4V_b}{5\pi} \cos(5\omega t + 180°) \ldots \quad (24)$$

$$X_{Switching2}(\omega t) = -\frac{4V_b}{\pi}\cos(\omega t) + \frac{4V_b}{3\pi}\cos(3\omega t) - \frac{4V_b}{5\pi} \cos(5\omega t) \ldots \quad (25)$$

Therefore, second SSDL output intermodulation can be approximated with:

$$Y_{intermod2_{out}}(\omega t) = V_a \cos(\omega t) * -\frac{4V_b}{\pi}\cos(\omega t) \ -V_a \cos(\omega t) \ * -\frac{4V_b}{3\pi}\cos(3\omega t) - V_a \cos(\omega t) * -\frac{4V_b}{5\pi} \cos(5\omega t) \ldots \quad (26)$$

Which directly cancels with first SSDL output intermodulation (23)!

2.6.2 Implementation

Testing was done with the prototype displayed in Figure 21. The test board was constructed primarily with 2 MMICs from the same wafer run as past passive bootstrap SSDL tests with Northrop Grumman's 0.2um GaN HEMT process. Consequently, each passive bootstrap SSDL still has dimensions of 4.9mm by 5.1mm. Similar to how the past passive bootstrap SSDL 3-port testing was done, the fourth port of the of each of SSDL element was simply connected to a 50 Ohms termination to create 2 3-port passive bootstrap elements.

Additional COTS components were used to construct the test board. ADP-2-4+ splitter/combiners were used at each of the TX, RX, ANT port for splitting signal across the 2 SSDL elements with passive bootstrapping. ADP-2-20+ splitter/combiners and Harwin Inc.

S1621-46R and S1731-46R jumpers were used to arrange the switching network of the SSDLs to the correct ports.

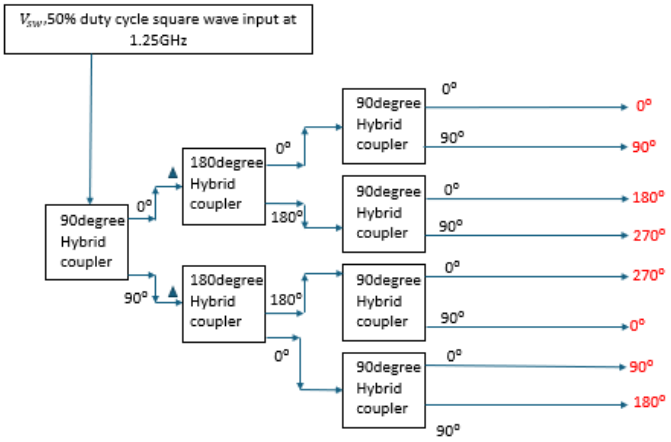
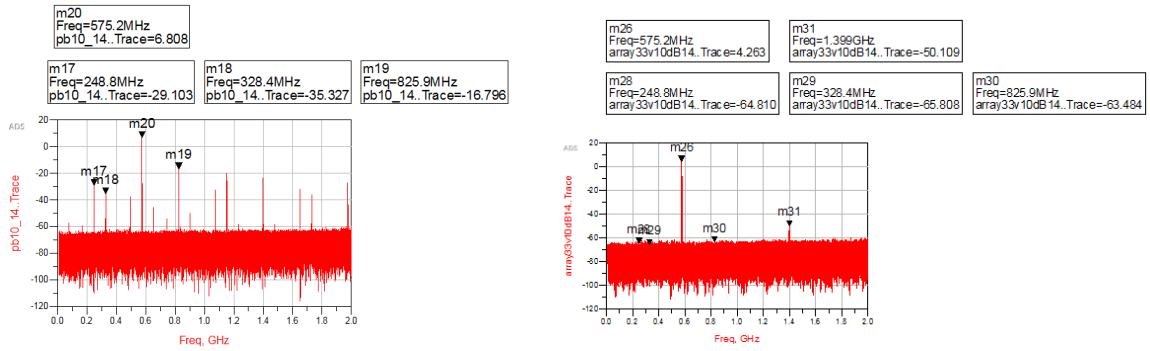


Figure 22 Switching control network setup for SSDL switching ports

Measurements were taken with a 575.8MHz RF signal going from the TX to ANT port while the RX port on the test board was terminated with a 50 Ohm impedance. 1.4 GHz switching was supplied to each of the 8 switching ports on the test board before being further split by ADP-2-20+ splitters and directed by jumpers to each of the total 16 ports on the 2 SSDL elements. This setup allows reuse of a prior 8-port switching control network setup used just for the single passive bootstrap SSDL as shown in Figure 22. Additionally, the same bias setup was carried over from the passive bootstrap.

2.6.3 Measurement Results

Testing the SSDL 2-element array in Figure 23 (b) then confirms that the intermodulation terms from the unintentional up conversion are reduced by 30-35dB! The reduction of intermodulation terms are also summarized in Table 4.



(a) (b)

Figure 23 Spectral Analysis comparing the (a) single passive bootstrap, (b) 2-element passive bootstrap SSDL array

f_{RF} =575.8MHz	f_{LO}=1.4GHz		
Order	Intermod. Products	Frequency (MHz)	Magnitude (dB)
2nd Order	f_{LO}-f_{RF}	824.2	-63.5
3rd Order	$2f_{RF}$-f_{LO}	(-)248.4	-64.8
4th Order	$3f_{RF}$-f_{LO}	327.8	-65.8

Table 5 Intermodulation product analysis of the passive bootstrap SSDL array with a 10dBm Input RF signal

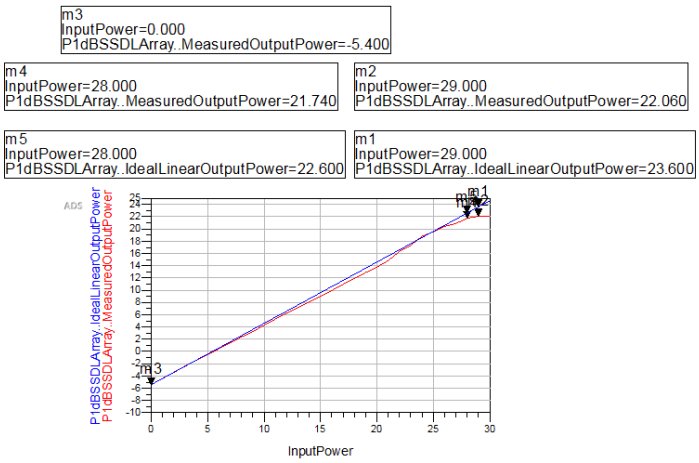


Figure 24 P1dB of the 2-element passive bootstrap SSDL

Shown in Figure 24, an additional benefit of the 2-element array is an increase in power compression. Since the signal power is split between the 2 passive bootstrap SSDLs each with a P1dB of around 20dBm, the overall array can theoretically handle 23dBm. It is observable now that the new P1dB is 28.3-5.4 = 22.9dBm. Note that the increased insertion loss in the signal bandwidth (5.4dB) is due to each of the COTS power splitters/combiners introducing over 1.5 dB of loss. An MMIC implementation of the power splitters/combiners will see far less increase in insertion loss. Therefore, the array arrangement of the SSDL provides a convenient and scalable way.

2.7 2-port Case: Gyrator

2.7.1 Theory

As previously mentioned, the SSDL can work with 2 delays and N-ports given enough switches. While the 3 port and 4 port SSDL has been shown to work as a circulator, the SSDL is versatile enough to also work in a two-port situation. Using the 4 ports differentially, the SSDL becomes a functional two port devices known as a gyrator.

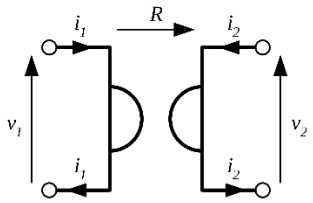


Figure 25 Conventional gyrator

Gyrators are traditionally a passive, linear element that is assumed to be near lossless. It's port satisfy the peculiar properties of equations (27) and (28),

$$V_2 = RI_1 \tag{27}$$

$$V_1 = -RI_2 \tag{28}$$

where R is known as the gyration resistance [20].

Their Z-parameter matrix is therefore:

$$Z = \begin{bmatrix} 0 & -R \\ R & 0 \end{bmatrix} \tag{29}$$

The corresponding S-parameter matrix for lossless case can be simplified to:

$$S = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{30}$$

Using the general gyrator S-parameter matrix is:

$$S = \begin{bmatrix} 0 & -e^{-\gamma l} \\ e^{-\gamma l} & 0 \end{bmatrix} \quad (31)$$

where $\gamma = \alpha + j\beta$

It can be derived from (31) with a capacitor, C_L, at port 2:

$$X_{in} = Z_0^2 \omega C_L + 2Z_0 \beta l(1 - 4\alpha^2 l^2) \approx Z_0^2 \omega C_L(inductive) \quad (32)$$

This equation (32) is similar to the λ/4 transformer equation (33) [21]:

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (33)$$

Thus, a gyrator too can be used as an impedance inverter. It's advantage over traditional impedance inverters like the λ/4 transformer is its much wider bandwidth. As shown in Figure 26 (a)-(g), the SSDL can be implemented as gyrator too. One can observe the reversion of polarity of the differential voltage supplied at port 2 once it arrives at port 1 while the differential voltage supplied at port 1 remains intact.

The SSDL gyrator is not limited to as strict a bandwidth as the λ/4 transformer since it's frequency range is not dependent on the wavelength. Again, it also has the advantage of a smaller form factor; a wavelength in the 100MHz to 1GHz frequency range is on the order of 30-300 cm. This would mean a conventional λ/4 transformer component would have a size dimension on the scale of 7.5-75 cm.

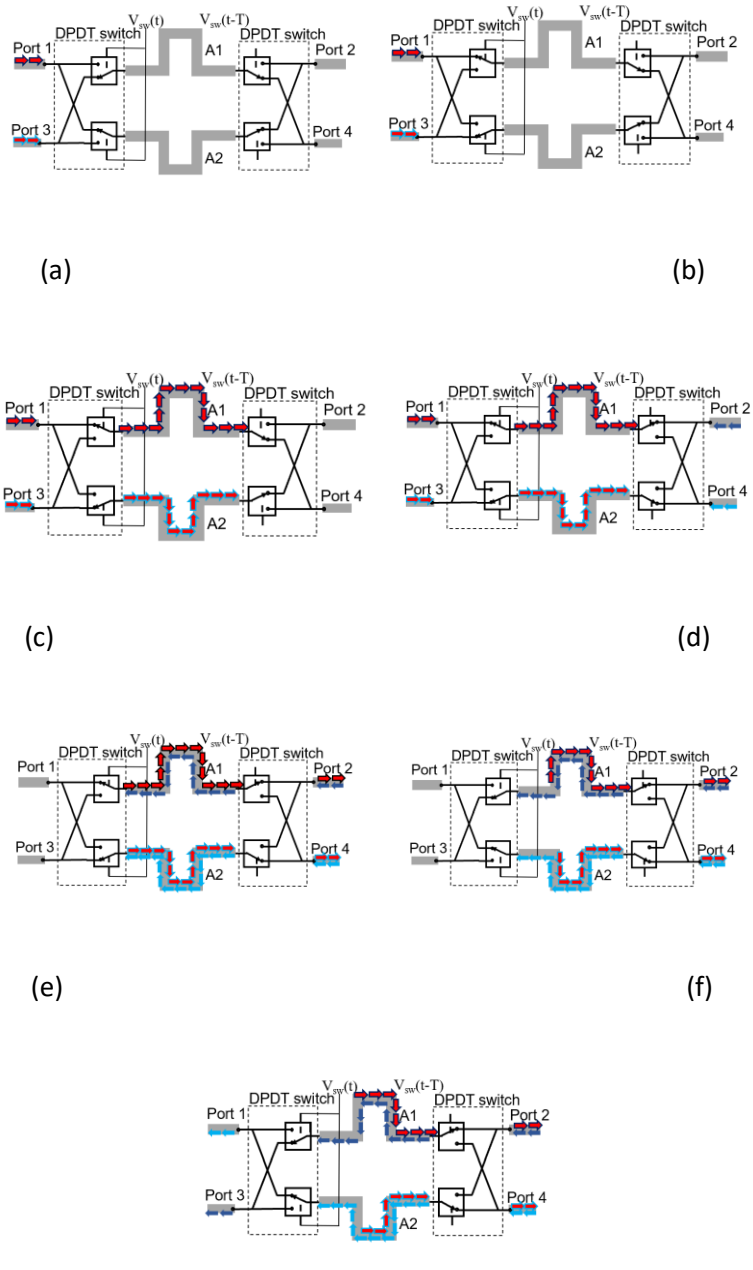


Figure 26 Timing Diagram of the signal at (a) 0-, (b) 0+, (c) T-, (d) T+, (e) 2T-, (f) 2T+, (g)3T-, 2-port, 2-line SSDL

Another conventional impedance invertor is the Gyrator-C shown in Figure 27 [15]. It used two transistors as amplifiers, the second transistor in inverting configuration to produce the same Z-parameter matrix (29). Its impedance inversion equation can be expressed as:

$$Z_{in} = \frac{1}{g_{m1}g_{m2}Z_L} \tag{34}$$

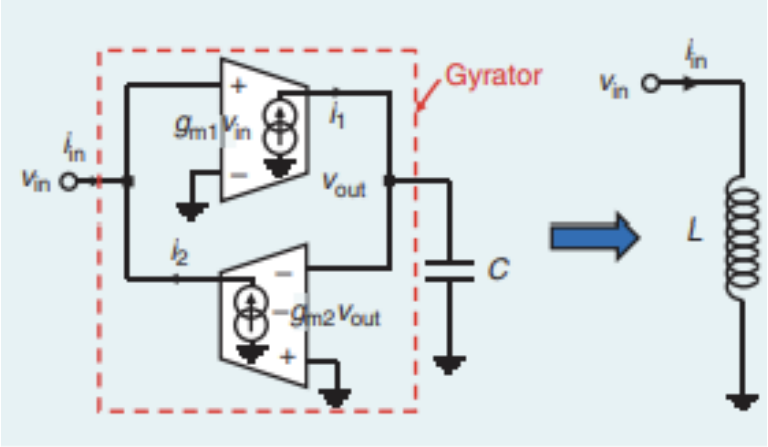


Figure 27 Typical Gyrator-C schematic

While the Gyrator-C can operate over a wideband due to its dependence on the transconductance of the transistors g_{m1} and g_{m2}, this same dependence damages its linearity. Generally, to then compensate for this poor linearity, a feedback resistance is connected between the transistors. However, this compensation can then reduce the Gyrator-C's bandwidth and raise its noise figure. Additionally, since both transistors are used as amplifiers, the power handling of the Gyrator-C tends to be low, resulting in a low P1dB point from early saturation. SSDL gyrator overcomes the variety of shortcomings of the Gyrator-C by instead using its transistors as switches.

From Figure 28, it is possible to derive the differential 2-port behavior from a 4-port of the SSDL. Assuming symmetry in port1 with port 3 and port 2 with port 4, the following assumptions can be summarized by equations (35)-(42).

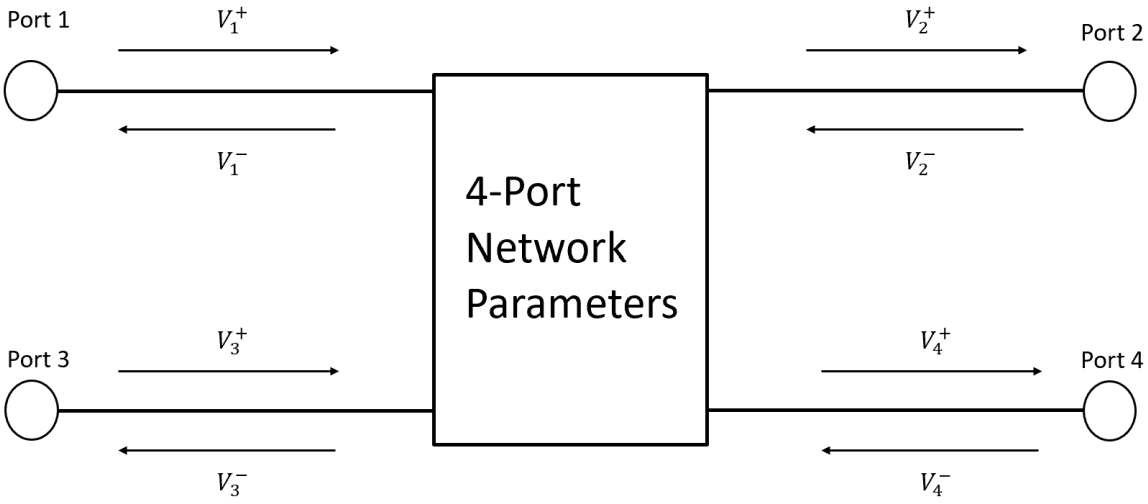


Figure 28 General 4-port Network

$$S_{11} = S_{33} \quad (35)$$

$$S_{22} = S_{44} \quad (36)$$

$$S_{24} = S_{42} \quad (37)$$

$$S_{13} = S_{31} \quad (38)$$

$$S_{32} = S_{14} \quad (39)$$

$$S_{23} = S_{41} \quad (40)$$

$$S_{12} = S_{34} \quad (41)$$

$$S_{21} = S_{43} \quad (42)$$

Assuming proper termination, the equations (43)-(46) can also be applied for their respective derivations.

$$V_2^+ - V_4^+ = 0 \qquad (43)$$

since it is assumed port 2 and port 4 are properly terminated when deriving S_{11}^d

$$V_2^+ - V_4^+ = 0 \qquad (44)$$

since it is assumed port 2 and port 4 are properly terminated when deriving S_{12}^d

$$V_1^+ - V_3^+ = 0 \qquad (45)$$

since it is assumed port 1 and port 3 are properly terminated when deriving S_{12}^d

$$V_1^+ - V_3^+ = 0 \qquad (46)$$

since it is assumed port 1 and port 3 are properly terminated when deriving S_{22}^d

Finally, equations (47)-(54) are commonly defined for 4-port networks

$$S_{11}^d = \frac{V_1^- - V_3^-}{V_1^+ - V_3^+} \qquad (47)$$

$$S_{21}^d = \frac{V_2^- - V_4^-}{V_1^+ - V_3^+} \qquad (48)$$

$$S_{12}^d = \frac{V_1^- - V_3^-}{V_2^+ - V_4^+} \qquad (49)$$

$$S_{22}^d = \frac{V_2^- - V_4^-}{V_2^+ - V_4^+} \qquad (50)$$

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ + S_{13}V_3^+ + S_{14}V_4^+ \qquad (51)$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ + S_{23}V_3^+ + S_{24}V_4^+ \qquad (52)$$

$$V_3^- = S_{31}V_1^+ + S_{32}V_2^+ + S_{33}V_3^+ + S_{34}V_4^+ \qquad (53)$$

$$V_4^- = S_{41}V_1^+ + S_{42}V_2^+ + S_{43}V_3^+ + S_{44}V_4^+ \qquad (54)$$

To derive S_{11}^d, equation (35), (38), (39), (41) are substituted into (53) to produce (55)

$$V_3^- = S_{13}V_1^+ + S_{14}V_2^+ + S_{11}V_3^+ + S_{12}V_4^+ \qquad (55)$$

Then subtracting (55) from (51),

$$V_1^- - V_3^- = S_{11}(V_1^+ - V_3^+) + S_{12}(V_2^+ - V_4^+) + S_{13}(V_3^+ - V_1^+) + S_{14}(V_4^+ - V_2^+) \qquad (56)$$

The terms multiplied by S_{13} and S_{14} in (56) can be rearranged:

$$V_1^- - V_3^- = S_{11}(V_1^+ - V_3^+) + S_{12}(V_2^+ - V_4^+) - S_{13}(V_1^+ - V_3^+) - S_{14}(V_2^+ - V_4^+) \qquad (57)$$

Using assumption (43), equation (57) can be reduced to:

$$V_1^- - V_3^- = S_{11}(V_1^+ - V_3^+) - S_{13}(V_1^+ - V_3^+) \qquad (58)$$

Which can be rearranged to:

$$V_1^- - V_3^- = (V_1^+ - V_3^+)(S_{11} - S_{13}) \qquad (59)$$

Dividing both sides by $(V_1^+ - V_3^+)$,

$$\frac{V_1^- - V_3^-}{V_1^+ - V_3^+} = (S_{11} - S_{13}) \qquad (60)$$

Thus, we finally arrive at:

$$S_{11}^d = (S_{11} - S_{13}) \qquad (61)$$

To further derive the input impedance from the differential S-parameters, the relation between input impedance and s-parameters it is defined by:

$$S_{11d} = \frac{Z_{in}-Z_o}{Z_{in}+Z_o} \qquad (62)$$

Multiplying both sides of (62) by $Z_{in} + Z_o$, we obtain

$$S_{11d}\, Z_{in} + S_{11d}\, Z_0 = Z_{in} - Z_0 \qquad (63)$$

Then solving (63) for Z_{in},

$$Z_{in} = (-Z_0)\,\frac{S_{11d}+1}{S_{11d}-1} \qquad (64)$$

2.7.2 Implementation

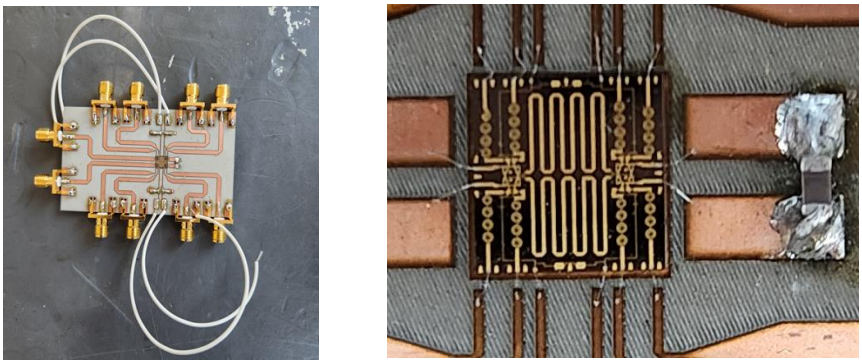
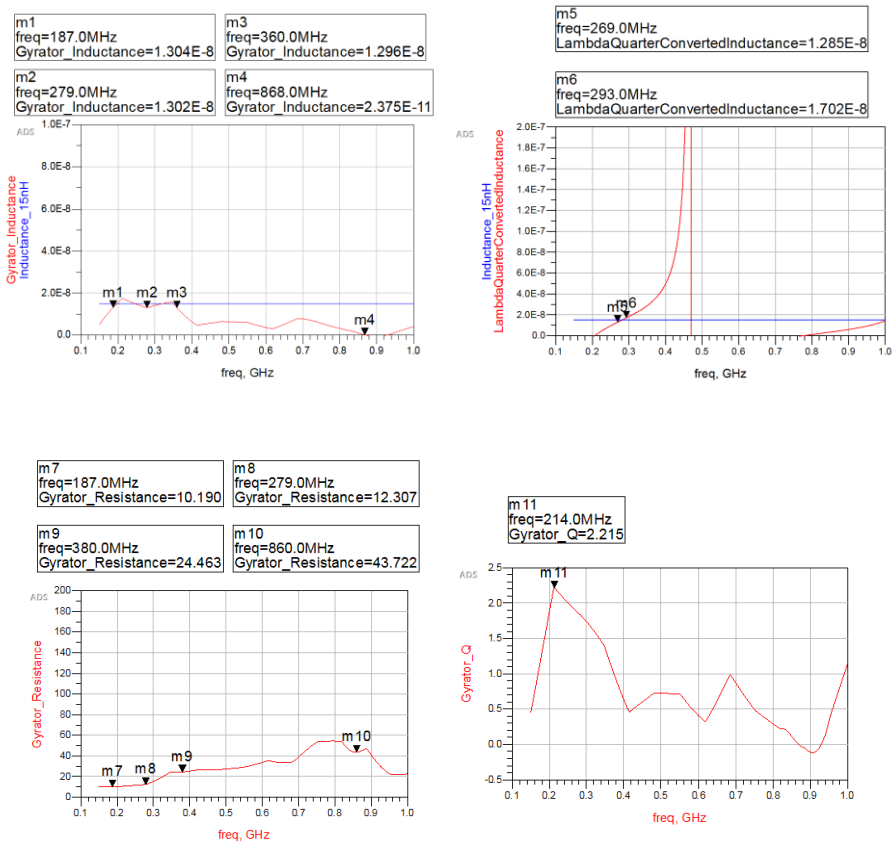


Figure 29 (a) SSDL Gyrator PCB test Board (b) Zoom in on actual gyrator portion

Measurements were taken using the same PCB testbed setup as with the prior passive bootstrap SSDL. The test board was constructed once again primarily with a MMIC from the same wafer run as past passive bootstrap SSDL tests with Northrop Grumman's 0.2um GaN HEMT process.

Thus, the exact same 1.25 GHz switching network in Figure 22 from prior the passive bootstrap SSDL was able to be applied. This also means that the previous 4.9mm by 5.1mm MMIC was used. The overall size of the actual gyrator circuit within the test board fits within a 9.8mm by 5.1 mm space as seen in Figure 29 (a).

A 6pF Murata GRM1555C1H6R0WA01 capacitor was used to conversion into an inductor. Given the 1.25 GHz switching frequency, using (32), an inductance of 15nH was expected to be observed by the network analyzer. The previous 4-port passive bootstrap SSDL was measured with its ports connected differentially to a network analyzer; this allowed the SSDL device to now operate as a 2-port device.



(c) (d)

Figure 30 (a) Impedance inversion results from converting a capacitor to an inductor, (b) Impedance inversion by a λ/4 transformer, (c) Real component of SSDL Gyrator impedance, (d) Q-factor of SSDL Gyrator

2.7.3 Measurement results

The 6pF capacitor was successfully inverted into a 13-17nH inductor from 187MHz-360MHz. This impedance inversion bandwidth of 173MHz (1.925:1) is much greater than that expected of an equivalent λ/4 transformer 24MHz (1.089:1) as shown in Figure 29 (c).

Table 6 compares conventional Gyrator-C to the SSDL gyrator. It can be observed that while the Gyrator-C generally had wider inductive bandwidth, it had significantly lower power handling and linearity represented by their lower P1dB point. Generally, the noise for the SSDL was also

significantly lower. Overall, in roughly the original target range of 100MHz to 1GHz, the SSDL gyrator outperforms the Gyrator-C at converting a capacitor into an inductor.

	Technology	Inductive Bandwidth (MHz)	Noise ($nV/\sqrt{Hz}$)	Power Consumption (mW)	Max Q	P1dB (dBm)
[23]	0.18 µm CMOS	-	-	16	70	8
[24]	0.18 µm CMOS	-	-	13	200	-9
[25]	0.13 µm CMOS	300-7320	3.1	1	3900	-
[26]	0.09 µm CMOS	250-12500	4.6	4	13159	-
[27]	0.18 µm CMOS	1.5-7940	7-21	0.6	497	-
[27]	45 nm CMOS	400-3100	6-40	0.109	-	-
[28]	90 nm CMOS	5500	15.6	0.515	895	4.28
[29]	0.18 µm CMOS	1900-3450	14.5	6.87	34-1819	-
This Work	0.2µm GaN	140-860	5.6	141	2.2	20.5

Table 6 Comparison of Gyrator-C to the SSDL gyrator

The quality factor of the SSDL gyrator is significantly lower than the Gyrator-C due to three reasons:

1. The on-resistance of the 0.2 µm NGAS transistors used in the SSDL gyrator were twice their expected value due to a fabrication error in the resistive layer (4 Ω instead of 1.8 Ω)

2. The Gyrator-C's use of transistors as amplifiers (active devices, saturation region) as opposed to the SSDL gyrator's use of transistors as switches (passive devices, triode region) means the

transconductances of the Gyrator-C significantly boosts the converted inductance more than the SSDL gyrator since they are operation in different regions

3. The Gyrator-C uses 2 transistors while the SSDL gyrator uses 4 transistors so there are twice as many transistors contributing on-resistance

Consequently, these same reasons in addition pushing the drive power to test the limits of power handling explain why the power consumption of the SSDL gyrator is much greater than the Gyrator-C.

Chapter 3: Broadband Amplifier for Integrated Phased Array

3.1 Theory

To construct a small form factor integrated phased array, 3 innovative ideas are leveraged and combine them to build a working theoretical model and proof of concept broadband power amplifier prototype.

3.1.1 Tightly Coupled Dipole Array

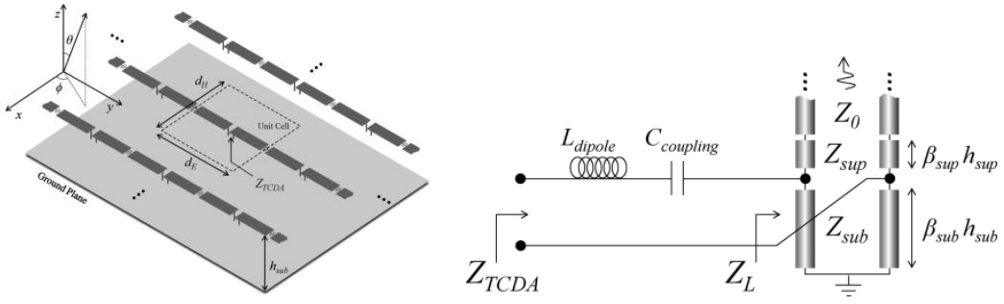


Figure 31 (a) Example of a Tightly Coupled Dipole Array by I. Tzanidis, et al, (b) corresponding TCDA equivalent circuit model

(a) (b)

The TCDA is a great low profile broadband antenna array. It is composed of several capacitively coupled horizontal dipoles above a conducting ground plane; this coupling allows antenna element spacing to be less than λ /2 since the whole behaves more like a single antenna [30-32]. The neighboring dipoles capacitively couple such that the array can support current at a wavelength much greater than a single element. This inter-element capacitance along with the dipole inductance, as shown in Figure 30 (b), allows the antenna array to resonate over a wide bandwidth allowing for a wide operating bandwidth commonly over 4:1.

Figure 30 (b) shows it is possible to model a TCDA with an equivalent circuit composed of transmission line, inductors, and capacitors [31,32]. The overall impedance of the TCDA can be expressed as:

$$Z_{TCDA} = L_{dipole} + C_{coupling} + \left(Z_0 \parallel Z_{sub} \parallel Z_{sup}\right) \quad (65)$$

Where L_{dipole} is the dipole inductance, $C_{coupling}$ is the inter-element capacitance, Z_0 is the free space layer, Z_{sub} is the substrate layer and Z_{sup} is the superstrate layer [32]. Each of the 3 layers (transmission line components) can be expressed as:

$$Z_r^E = \eta \sqrt{\frac{\mu_r}{\varepsilon_r}} \frac{d_E}{d_H} \cos\theta_r \quad (66)$$

when scanning in the E-plane (ϕ=90°), and

$$Z_r^H = \eta \sqrt{\frac{\mu_r}{\varepsilon_r}} \frac{d_E}{d_H} \frac{1}{\cos\theta_r} \quad (67)$$

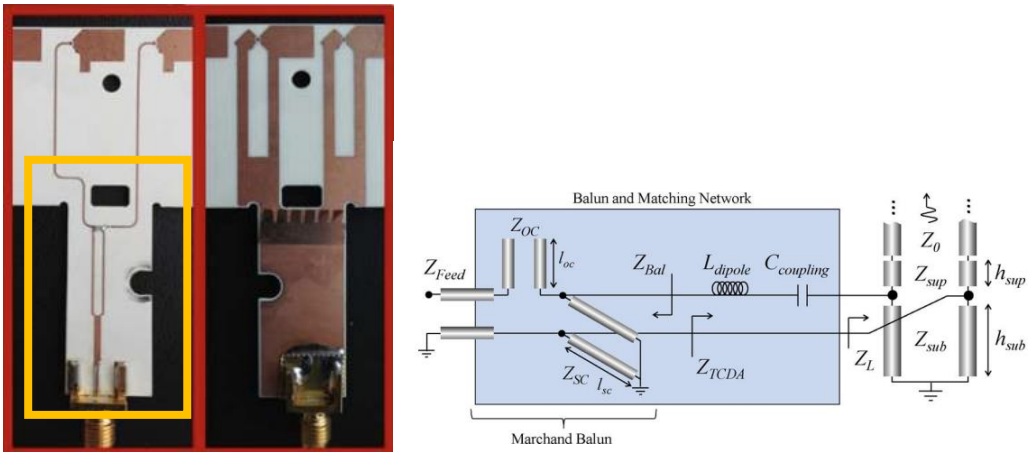
when scanning in the H-plane (ϕ=0°).

$\eta \approx 377\Omega$, is the characteristic impedance of free space. θ_r is corresponding angle of refraction within each layer given by

$$\theta_r = \sin^{-1}\left(\frac{\sin\theta}{\sqrt{\mu_r \varepsilon_r}}\right) \qquad (68)$$

where θ is the scan angle, ε_r and μ_r are the relative permittivity and permeability of each respective layer. d_E is the vertical spacing and $d_H$is the horizontal spacing. $L_{dipole}$and $C_{coupling}$ are also dependent on spacings d_E and d_H and the number of dipole elements. This means Z_{TCDA}, the overall impedance of the TCDA, can be controlled through the spacing and number of dipole elements. Generally, the TCDA has high common mode impedance behaving like an open circuit [32].

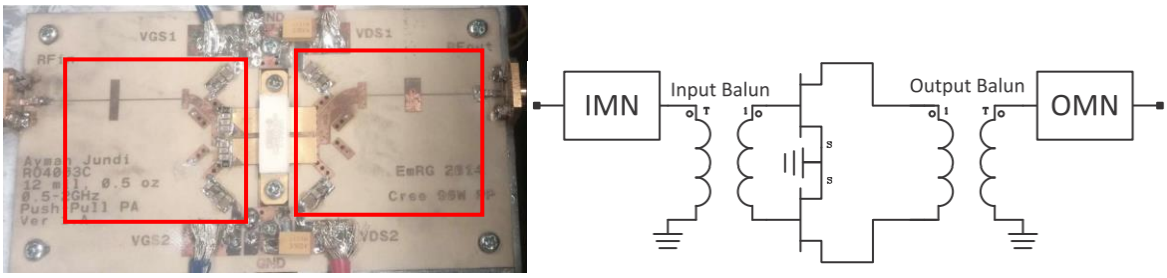
Previous work by I. Tzanidis, et al [32], has been done to produce an integrated phased array by directly integrating a Marchand Balun to a TCDA by using the balun as a wideband distributed component matching circuit as shown in Figure 31 (b). However, the overall integrated phased array can potentially be scaled even smaller if the balun can be outright removed; the Marchand Balun still takes up a significant amount of space as indicated in yellow in Figure 31 (a).



(a) (b)

Figure 32 (a) Example of a Tightly Coupled Dipole Array with Marchand Balun by I. Tzanidis, et al (b) corresponding TCDA equivalent circuit model

3.1.2 Broad Band PA



(a) (b)

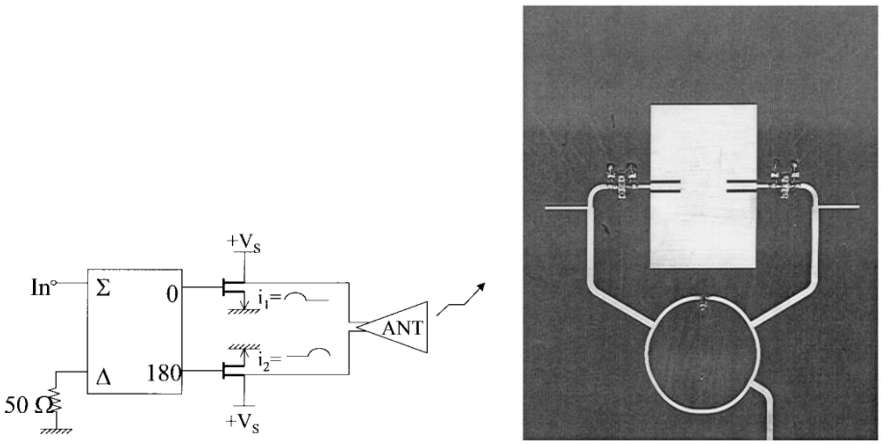
Figure 33 (a) Wideband Power Amplifier by A. Jundi et al (b) corresponding schematic

Broadband Power amplifiers are mature technology that has been commonly achieved by harmonic termination in pull-push amplifier. By terminating the second harmonic with broadband matching networks (usually transmission line segments), a power amplifier can achieve high broadband power efficiency while maintaining bandwidths as wide as 4.33:1 [33,34]. However, as shown in red by Figure 32 (a), the connection of a broadband power

amplifier to a phased array is still done by a balun, restricting how small an overall Phased Array System can be.

3.1.3 Integrated Frontend

Pioneer work for an integrated RF frontend was done under Prof. Itoh [36,37]. It was shown both that antenna performance could be improved by harmonic termination and the power amplifier could get an optimal loaded antenna for high power efficiency. Also, by using a differential architecture such as a push pull amplifier, a balun is no longer needed between the amplifier and antenna. However, both these integrated front ends were narrowband, optimized for 2.5 GHz.



(a) (b)

Figure 34 (a) Architecture of push–pull integrated antenna front-end, (b) PCB Integrated antenna push–pull PA with dual-feed patch antenna

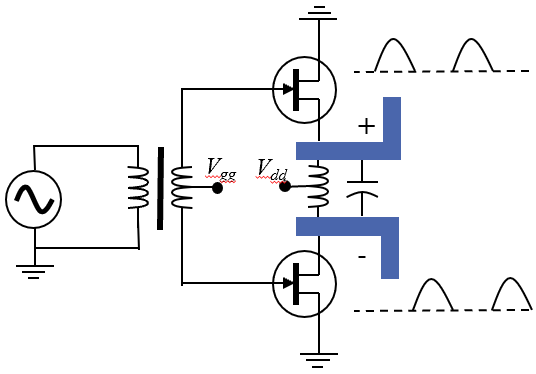
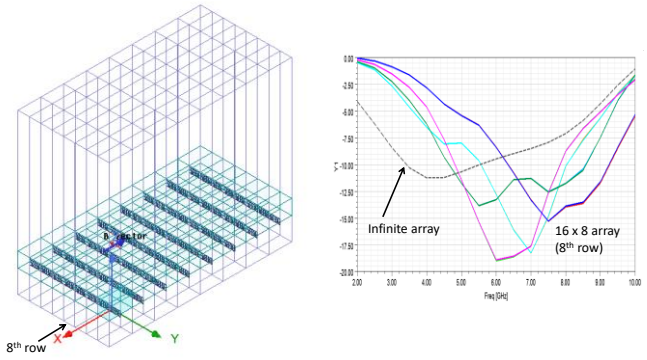


Figure 35 Theoretical TCDA loaded push-pull amplifier for Integrated frontend

Combining the prior art together, an integrated phased array system can be built. This overall architecture of an integrated phased array has several benefits:

1. The amplifier and TCDA are both differential, not balun is required to connect them
2. Using transmission lines segments, it is possible to have broadband matching to the TCDA load from the power amplifier
3. The 2nd harmonic termination from the TCDA high common mode impedance allows the power amplifier to achieve high gain and excellent efficiency over a broad bandwidth
4. Overall integration allows for dramatically smaller form factor

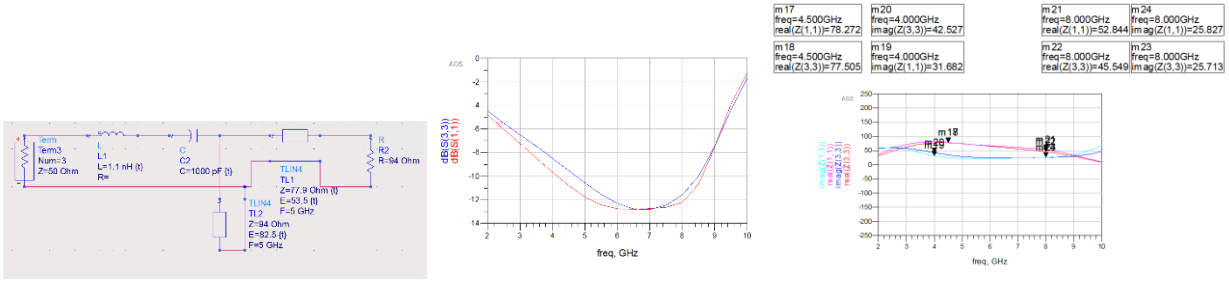
3.2 Simulation



(a) (b)

Figure 36 (a) HFSS simulation of a 16 x 8 TCDA (b) corresponding S-parameters

On HFSS, a prototype TCDA was constructed. Its overall equivalent circuit model was then extracted via S-parameters as shown in Figure 35. An equivalent circuit model was then reconstructed in ADS as shown in Figure 36 to find practical finite values that could replicate the TCDA load when it would eventually be connected to the push-pull amplifier.



(a) (b) (c)

Figure 37 ADS simulation of equivalent HFSS TCDA load (a) schematic, (b) S-parameters, (c) Real and Imaginary Impedance of TCDA

3.3 Small form factor biasing network

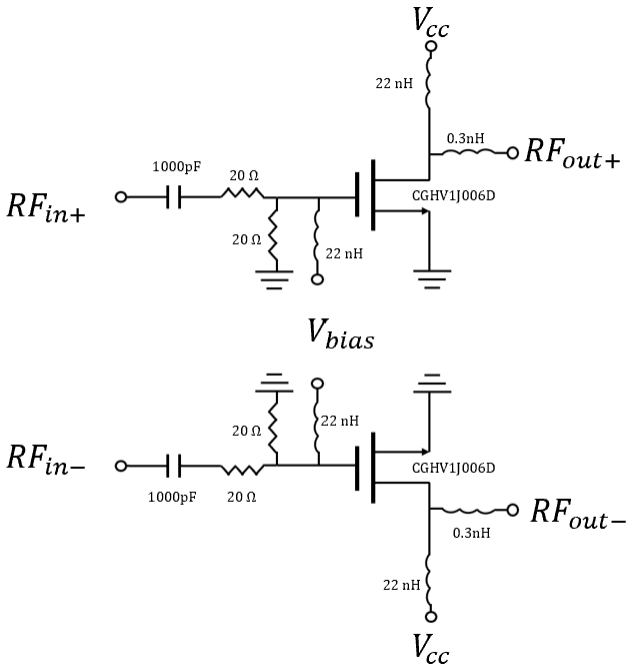


Figure 38 Broadband Differential Amplifier schematic with biasing network

A power amplifier traditionally uses lumped components for both a biasing network and maintaining stability on the input side. Figure 38 shows a schematic of the final biasing network used on the Wolfspeed CGHHV1J006D transistor. The resistors added at the gate were for stability to prevent the power amplified from oscillating. Fortunately, the 20 Ω CRCW060320R0FKEA thick film resistors are able to maintain the necessary stability over the target 4-10 GHz bandwidth while having a small form factor (0.85mm x 1.55mm). Thin film capacitors were used for blocking the DC bias since both conventional surface mount capacitors and microstrip line capacitors were unable to cover the entire wide target bandwidth. The 1000pF V30BZ102M6SX thin film capacitors were used since they could cover the necessary bandwidth while also having a small form factor (0.76mm x 0.76mm).

3.4 Inductor Design Challenge

Inductors also showed up in the bias network used as RFC (Radio Frequency Chokes) to block the AC signal while letting the DC bias pass. Since wideband inductors able to maintain a value of at least 22nH over the 4-10 GHz range were needed for the biasing network, microstrip transmission line inductors etched out of a 10mil RO5880C were used.

However, it was found that even traditional spiral shaped and meandering transmission line inductors were not wideband enough to cover the full 4-10GHz target bandwidth. This issue was mainly due to the capacitive coupling present in the gaps between meandering transmission line segments causing the inductors to resonate within the power amplifier operating bandwidth. Extensive modeling of this type of parasitic capacitance exists [38], as shown in Figure 39.

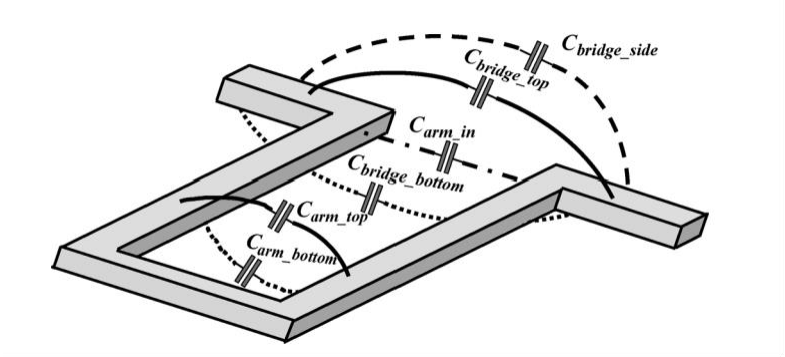
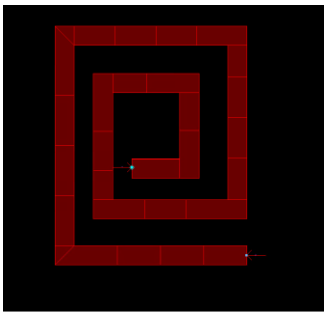


Figure 39 A model showing parasitic capacitance between meandering transmison line by B. Mohajer-Iravani and O. M. Ramahi

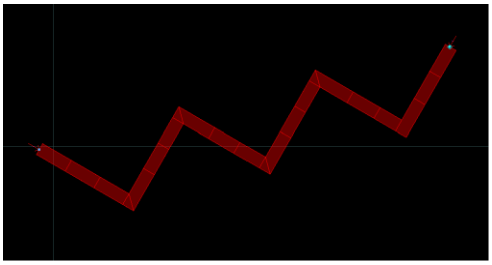
Resolving this parasitic capacitance could not simply be solved by increasing the gap distance between meandering transmission line segments. The inductance value of the transmission line inductor drops as the gaps are widened [19]. The laser machine for etching the microstrip inductors added the constraint of 100μm being the thinnest dimension (generally, the width) that

it could be etched. This size constraint also meant the gaps in the transmission line strips could not be made larger by thinning the inductors. Consequently, an unconventional recursive L-shaped was used instead since it was the only type of structure able to provide at least 22nH necessary for the entirety of the 4-10 GHz band. Each segment of the recursive L-shaped inductor is only 100 µm by 800 µm.

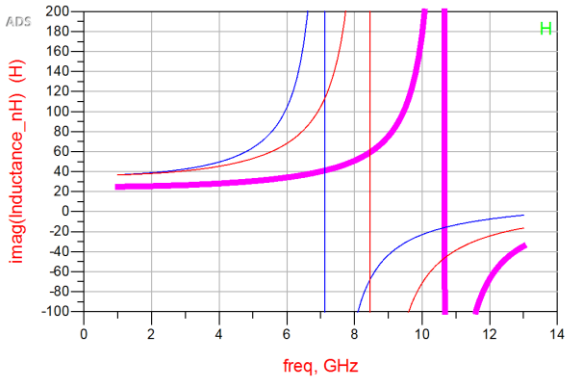
(a)



(b)



(c)



(d)

Figure 40 (a) Meandering line Inductor, (b) Spiral Inductor , (c) Recursive L-shape Inductor , (d) Performance of each type of inductor

A comparison of the 3 different transmission line inductors can be seen in Figure 40 (d) where spiral inductors are shown in red, meandering line inductors are shown in blue and recursive L-shaped inductors are shown in magenta.

3.5 Wideband Balun

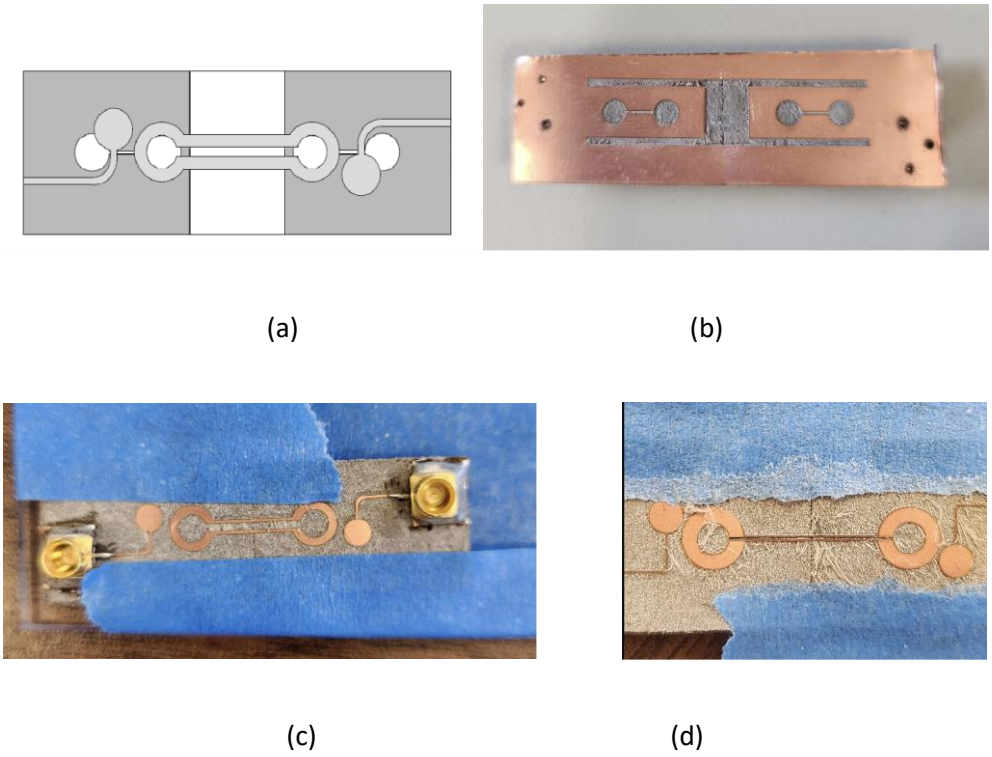


Figure 41 (a) Planar Double Balun Design by P. T. Nguyen et al, (b) backside of fabricated planar balun, (c) frontside of 4-6.5GHz planar balun , (d) frontside of 6-10GHz planar balun

While an eventual integrated phased array will be balun less, in order to measure the wideband performance of the power amplifier without a complete TCDA attached, a wideband balun was used. It interfaces the power amplifier with the network amplifier to show that the power amplifier can attain the necessary specifications in bandwidth, gain and efficiency. A common

planar balun [38] is used since it generally has the most wideband performance for radio frequency range baluns.

However, since the PA's operating frequency range is wider than any single balun can generally cover, multiple baluns were used to de-embed the power amplifier's performance over entire frequency range. One balun was optimized to cover the 4-6.5 GHz frequency range for de-embedding while another was optimized to cover the 6-10 GHz frequency range. It can be observed that the main difference between balun designs was the trace width and distance between traces in the center gap were 0.45mm in the 4-6.5 GHz frequency range balun and 0.15mm in the 6-10 GHz frequency range balun.

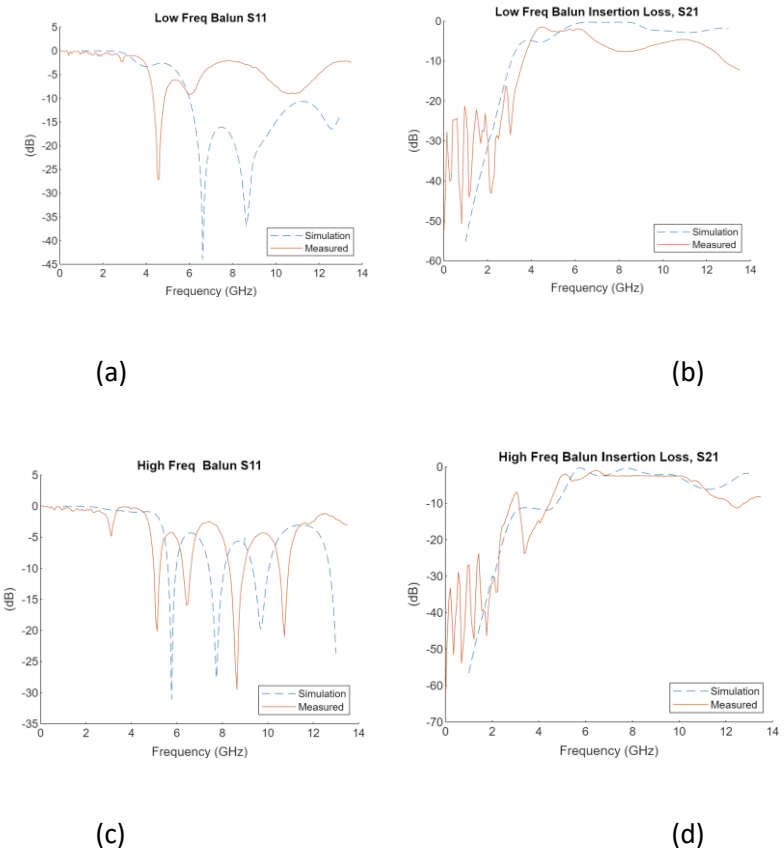


Figure 42 S- Parameters of Balun, (a) S11 of 4-6.5 GHz Balun, (b) S21 of 4-6.5 GHz Balun, (c) S11 of 6-10 GHz Balun, (d) S21 of 6-10 GHz Balun

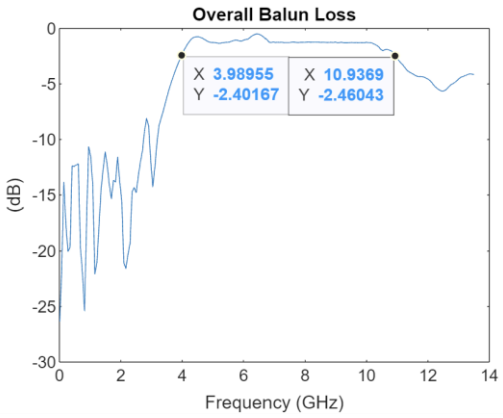
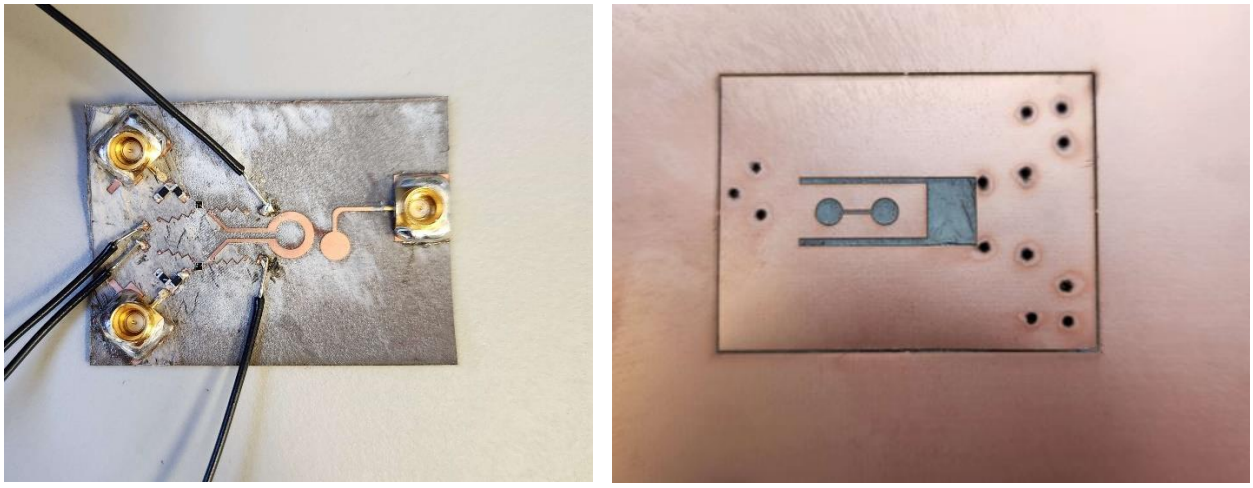


Figure 43 Overall loss contributed by Baluns

The overall balun loss over the entire 4-10 GHz spectrum, which is displayed in Figure 42, is for a double balun. The actual balun that will be attached to the differential amplifier will only be using half of the optimize balun structure. This also means the overall insertion loss contributed by the balun will be 1.23dB or less when de-embedding it during power amplifier measurements.

3.7 Combined Implementation



(a) (b)

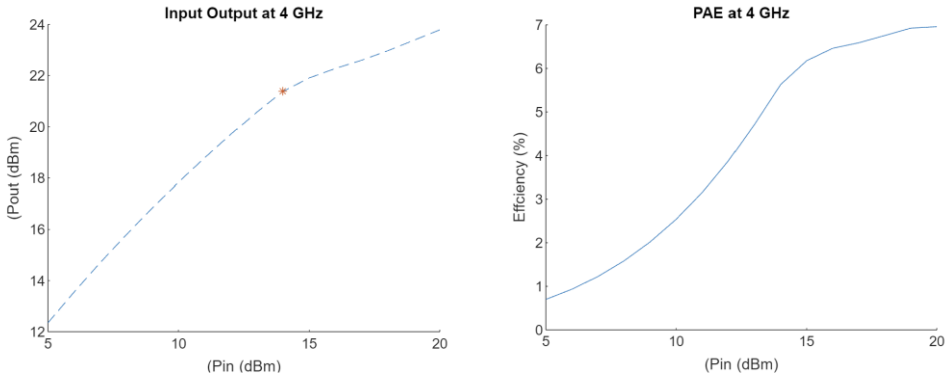
Figure 44 (a) Frontside of Power Amplifier integrated with balun , (b) Backside of Amplifier integrated with balun

The broadband amplifier and half balun are directly connected when measured by the network analyzer and spectrum analyzer in 1dB and 0.5 GHz increments. The total size of the test board is 1.6cm by 3.8cm; for comparison, flash drives are usually 4.572cm by 4.064cm. It can be observed that the actual broadband amplifier with its biasing network takes up less than half of total space. A significant amount of edge area with ground plane on the backside was kept to be used in mechanical stability. The 10mil thin RO5880C board etched on forming the PCB was not particularly sturdy and could deform without the ground plane provided by the edge area. The Power Added Efficiency (PAE), calculated with (69), was used alongside the gain as a general measure of the broadband amplifier's performance.

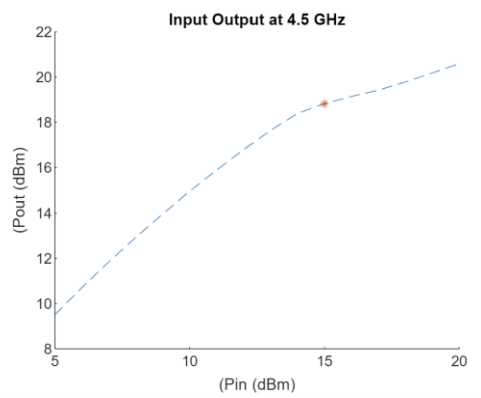
$$PAE(\%) = \left(\frac{P_{out} - P_{in}}{P_{dc}}\right) \times 100 \qquad (69)$$

3.8 Measurement Results

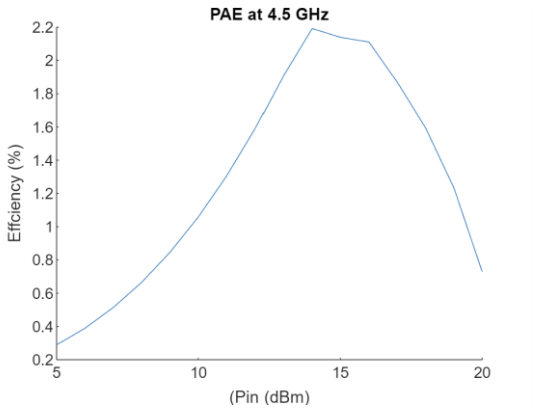
Generally, the P1dB saturation point (marked with the orange * symbol) of the broadband amplifier was around 14-15dBm over the frequency range of 4-10 GHz. The gain correspondingly was able to stay above 10dB from 5 to 9.9GHz. The PAE stayed above 50% from 5.5 to 9 GHz.



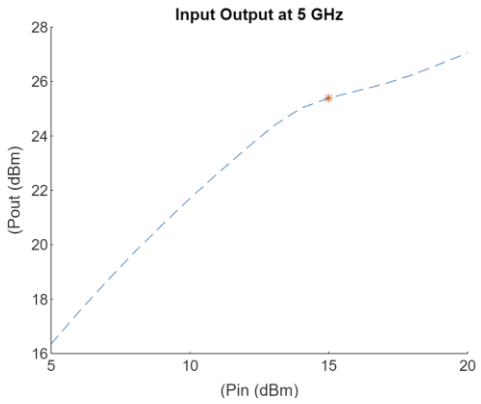
(a) (b)


Input Output at 4.5 GHz
(Pout (dBm)
(Pin (dBm)

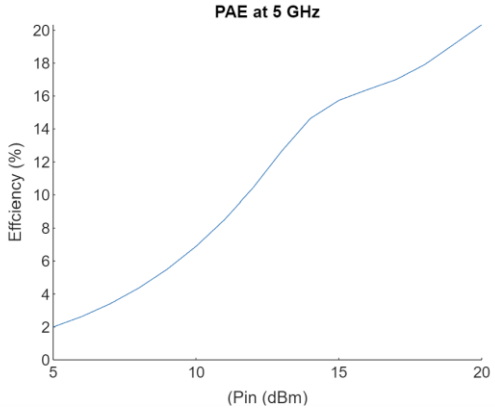
(c)


PAE at 4.5 GHz
Effciency (%)
(Pin (dBm)

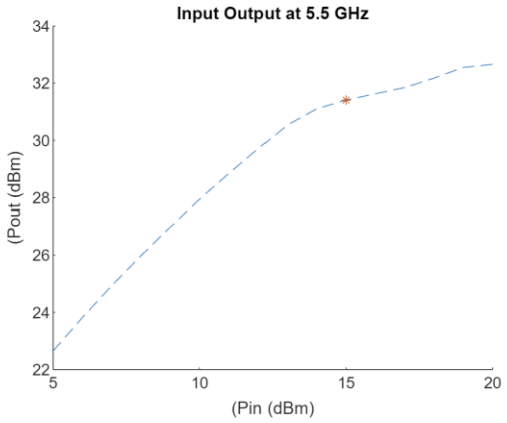
(d)


Input Output at 5 GHz
(Pout (dBm)
(Pin (dBm)

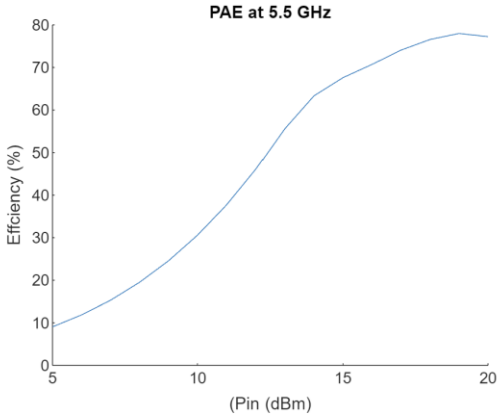
(e)


PAE at 5 GHz
Effciency (%)
(Pin (dBm)

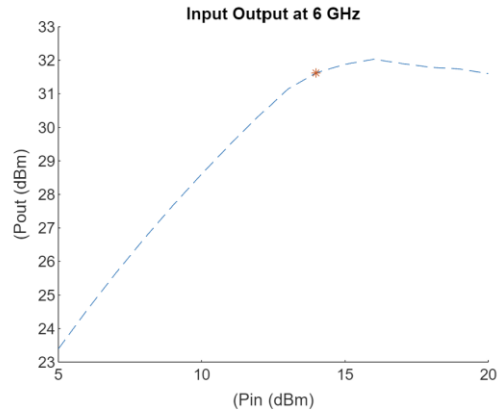
(f)


Input Output at 5.5 GHz
(Pout (dBm)
(Pin (dBm)

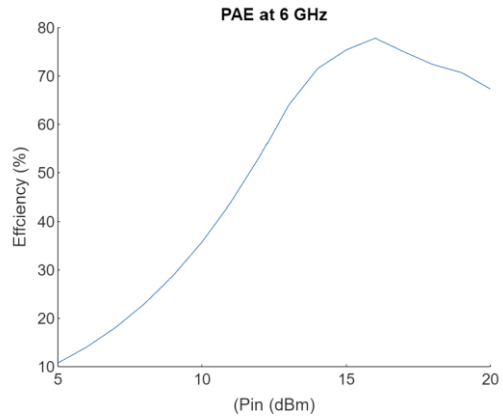
(g)


PAE at 5.5 GHz
Effciency (%)
(Pin (dBm)

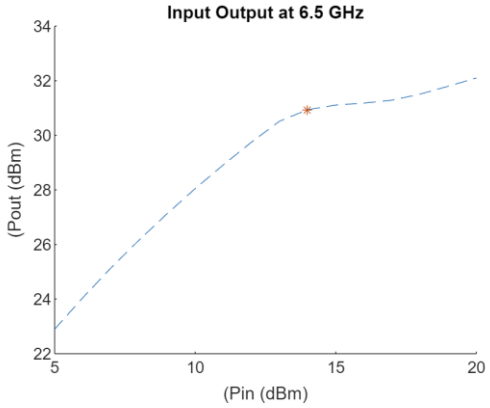
(h)


Input Output at 6 GHz
(Pout (dBm)
(Pin (dBm)

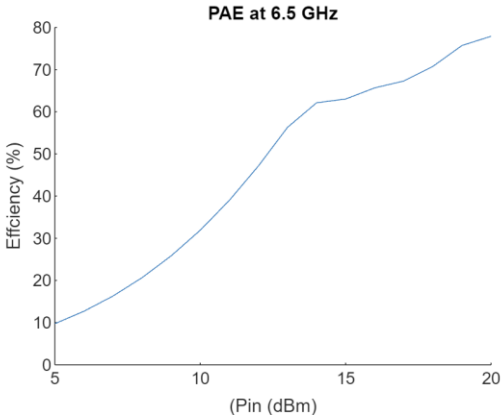
(i)


PAE at 6 GHz
Effciency (%)
(Pin (dBm)

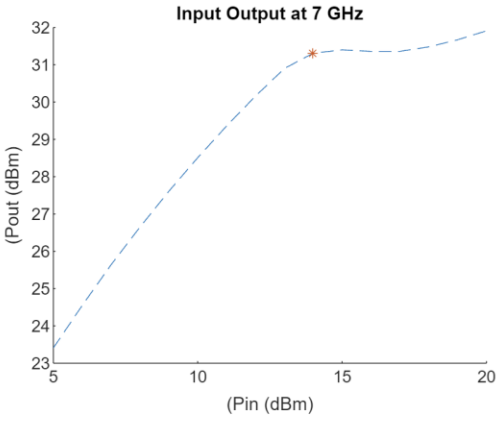
(j)


Input Output at 6.5 GHz
(Pout (dBm)
(Pin (dBm)

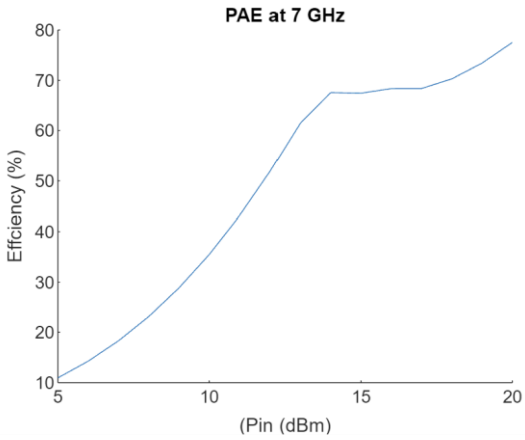
(k)


PAE at 6.5 GHz
Effciency (%)
(Pin (dBm)

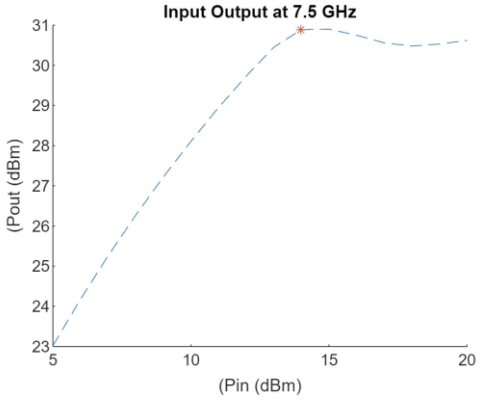
(l)


Input Output at 7 GHz
(Pout (dBm)
(Pin (dBm)

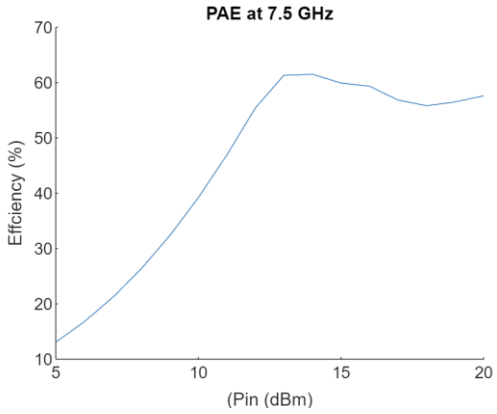
(m)


PAE at 7 GHz
Effciency (%)
(Pin (dBm)

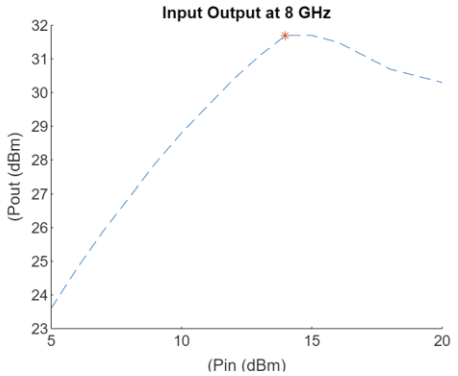
(n)


Input Output at 7.5 GHz
(Pout (dBm)
(Pin (dBm)

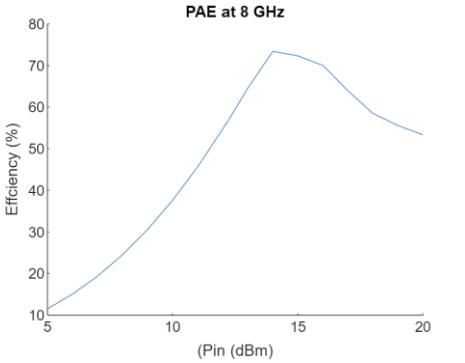
(o)


PAE at 7.5 GHz
Effciency (%)
(Pin (dBm)

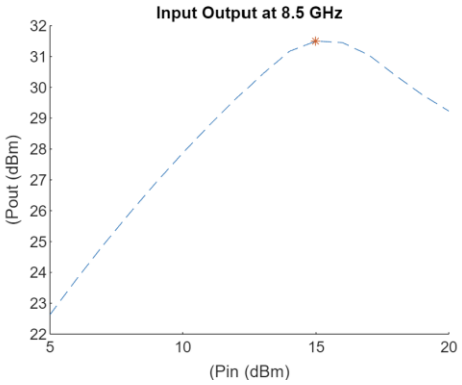
(p)


Input Output at 8 GHz
(Pout (dBm)
(Pin (dBm)

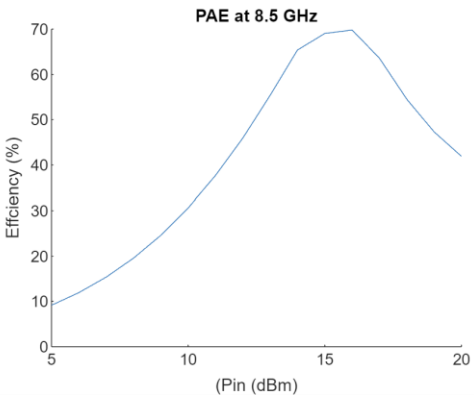
(q)


PAE at 8 GHz
Effciency (%)
(Pin (dBm)

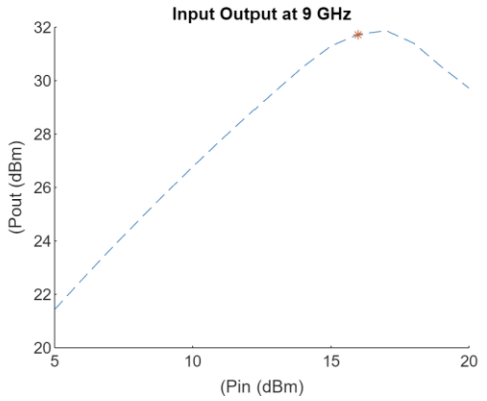
(r)


Input Output at 8.5 GHz
(Pout (dBm)
(Pin (dBm)

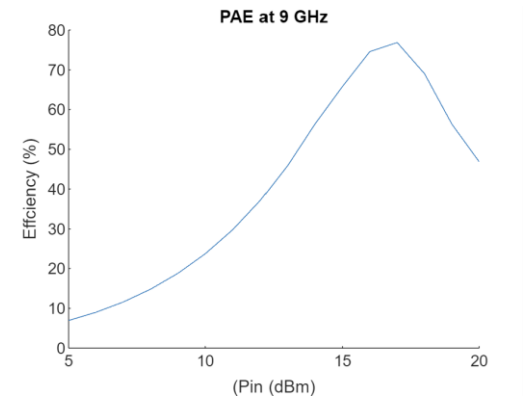
(s)


PAE at 8.5 GHz
Effciency (%)
(Pin (dBm)

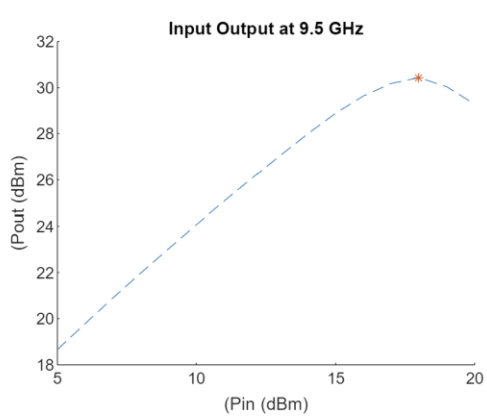
(t)



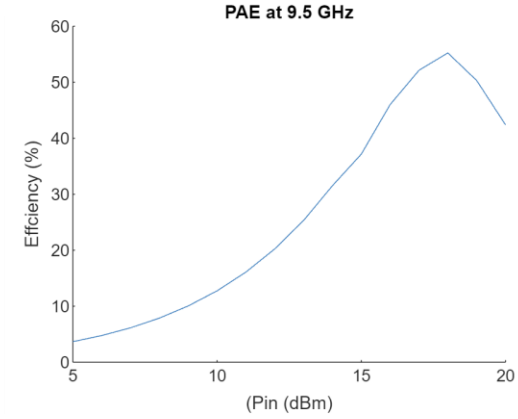
(u)



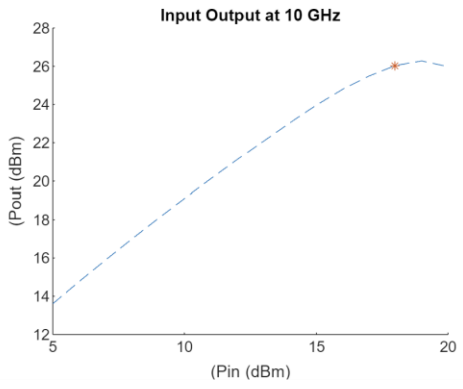
(v)



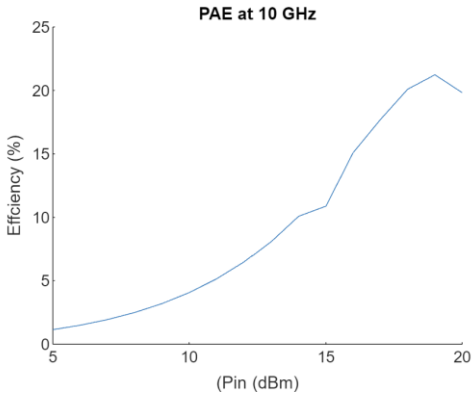
(w)



(x)

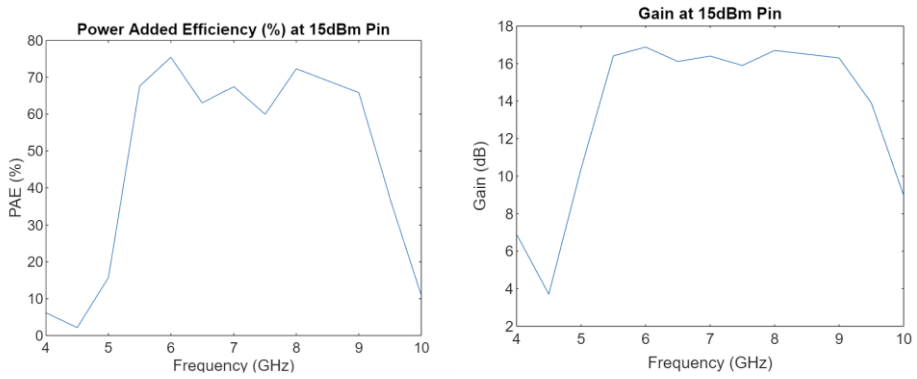


(y)

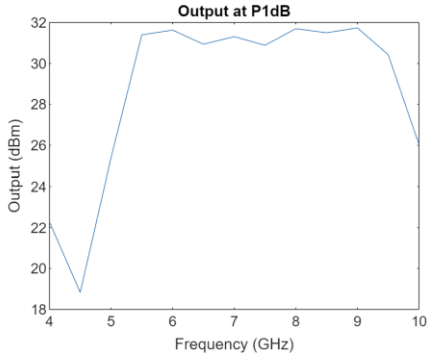


(z)

Figure 45 Output power and Power Added Efficiency graphs at various frequencies



(a) (b)



(c)

Figure 46 (a) PAE at 15dBm input power, (b) Gain at 15 dBm input power, (c) Output power at P1dB input power

As shown in Table 7, the performance of the broadband amplifier compared favorably with existing broadband, high efficiency, and high gain amplifiers. While it's bandwidth ratio wise was under 2:1, its overall bandwidth range of ~3.5GHz is significantly greater than the next greatest bandwidth range of 2.4 GHz.

	PAE above 50%	Gain above 10dB	Peak PAE	Peak Gain
[33]	0.45-1.95 GHz	0.45-1.95 GHz	84.2% at 0.63 GHz	20 dB at 0.63GHz
[34]	1.9-4.3 GHz	1.9-4.3 GHz	62% at 2 GHz	11.5 dB at 2.5 GHz
[35]	2-2.7 GHz	2.1-2.7 GHz	74% at 2.14 GHz	18.5 dB at 2.14GHz
This Work	5.5- 9 GHz	5-9.9 GHz	75.4% at 6.5 GHz	16.88 dB at 6GHz

Table 7 Comparison of wideband, high efficiency Power Amplifiers

Chapter 4 Conclusion

Summary

In this dissertation, components for a small form factor, broadband, Integrated Transmitter Array with high gain and power efficiency were designed. An overall Phased Array system can be improved in both bandwidth and form factor by replacing magnetic circulators, replacing conventional inductors, and removing baluns.

Non-reciprocity communication can be achieved without using ferromagnetic material using an SSDL device. The 3 and 4 Port SDDL can provide a broadband, small form factor magnetless circulator. The existing SSDL can be improved by implementing a high Q, series LC bootstrap to reduce insertion loss and improve P1dB. Then having 2 SSDLs with a 180° different phase shifts in their switching controls, intermodulation can be reduced and the P1dB can be further improved.

The SSDL can also operate as a differential 2 port Gyrator. The SSDL gyrator can convert a wide bandwidth capacitor to a wide bandwidth small form factor inductor. This impedance invertor provides significant bandwidth and form factor advantages over the $\lambda/4$ transformer and significant noise, linearity and power handling advantage the Gyrator-C.

A broadband amplifier to be loaded with a TCDA has several advantages over conventional broadband amplifiers. It can maintain comparable efficiency and gain over a wider frequency range in part thanks to its unconventionally shaped microstrip line inductors. It also allows the overall phase array system to have smaller form factor from removing the balun and matching network while reducing the matching network size.

Future Work

The SSDL has still more potential that can be explored. With just 128 GHz figure of merit transistors, it has already been demonstrated that:

- A magnetless circulator can achieve an insertion loss as low as 2.1dB from DC to 533.3 MHz, remaining below 3dB up to 1GHz, at least 18dB of isolation while providing a high-power handling P1dB point of over 20 dBm with a passive bootstrap all on a MMIC
- The magnetless circulator is scalable into a 2-element array allowing for unwanted modulation terms to be reduced by 30-35dB while raising the high-power handling P1dB further to nearly 23 dBm
- A switching-based gyrator can provide an approximately 15nH inductor from 187 MHz to 360 MHz from converting a capacitor. It is achieved while providing significantly better power handling and a competitively low noise of 5.6 nV/$\sqrt{Hz}$.

With better quality switches in terms of f_{FOM} and Q-factor, the operating bandwidth can be increased further while the insertion loss can be decreased further. Similarly, higher quality switches may also allow for still higher power handling if the insertion loss is successfully decreased. This means both the SSDL magnetless circulator and SSDL gyrator can see their performances enhanced using potential switches like those listed in Table 2. This can imply that SSDL structures may eventually even be able to operate on MMIC in the sub-THz range, ideal for scaling into 6G technology in future.

The integrated wideband PA also has a great deal of potential. With just COTS components and standard 10mil RO5880C board, it has already been demonstrated that:

- An unconventional recursive L-shaped microstrip inductor can remain inductive for nearly 2.5 GHz more bandwidth in the 1GHz to 10GHz range compared to conventional meandering line and spiral shaped inductors
- A differential broadband amplifier can maintain at least 50% PAE and 10dB gain over a ~3.5GHz frequency range, over 1 GHz more range than other conventional broadband amplifiers while occupying only 1.6cm by 3.8cm of area

Material with intrinsic wider bandwidth at RF and microwave frequencies, used in place of the 10mil RO5880C board for etching microstrip inductors, will allow for even wider inductive bandwidth recursive L-shape microstrip inductors. Combined with using MMIC designed, the corresponding differential broadband amplifier can be made even wider band and smaller form factor. As the size of the integrated phased array is limited by sturdiness of the board itself, it is also possible to further decrease the form factor of the overall design with an optimized support structure on the back plane of the system leading to more edge area then being able to be removed. Ultimately, the implications are that a potentially world record breaking phase array system in terms of both bandwidth and form factor lies startling close in the future. Such a future integrated phase array system would be scalable to 6G sub-THz and potentially certain niche optical applications temperature robustness permitting.

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