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Author

Liliental-Weber, Z.

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Z. Liliental-Weber, R. Gronsby, J. Washburn,
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Zuzanna Liliental-Weber, R. Gronsky, and J. Washburn

Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

N. Newman and W.E. Spicer
Stanford Electronics Laboratories
Stanford University
Stanford, CA 94305

E.R. Weber
Department of Materials Science
University of California
Berkeley, CA 94720

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Berkeley, CA 94720

N. Newman and W.E. Spicer
Stanford Electronics Laboratories
Stanford University
Stanford, CA 94305

E.R. Weber
Department of Materials Science
University of California
Berkeley, CA 94720

Abstract

We report here a systematic study which uses electrical device measurements and transmission electron microscopy (TEM) methods to investigate the electrical, morphological and structural properties of Au/GaAs Schottky diodes. The electrical characteristics of Au diodes formed on atomically clean and air-exposed GaAs (110) surfaces are found to change from rectifying to ohmic behavior after annealing above the Au-Ga eutectic temperature (360°C). This change is shown to be due to an ohmic-like contact at the periphery of the device. TEM studies of these structures indicate that the ohmic peripheral current pathway can be correlated with the formation of near surface Ga-rich Au crystallites at the diode circumference upon annealing. Further evidence of the correlation of the ohmic electrical characteristics with the morphology

of the periphery comes from data which indicate that the removal of these Au crystallites by mesa-etching is also accompanied with the elimination of the ohmic current. The morphology of the overlayer was found to depend strongly on annealing and surface treatment. TEM indicates that the interface is flat and abrupt for all unannealed diodes, as well as for annealed diodes formed on atomically clean surfaces. For annealed diodes formed on the air-exposed surfaces, the metal-semiconductor interface but contains large metallic protrusions extending up to several hundred Angstroms into the semiconductor. For comparison to practical structures, the morphology of annealed diodes formed using typical commercial processing technology (i.e. formed on chemically prepared (100) surfaces annealed in forming gas) was also investigated using TEM. The interface for these structures is more complex than interfaces formed on the atomically clean and air-exposed cleaved (110) surfaces. Evidence that Au diffuses through the interfacial native oxide layer and forms islands in intimate contact with the semiconductor was found.

I. Introduction

The efficiency and reliability of commercial III-V semiconductor devices very often depends on the properties of the metal/semiconductor contacts. Despite the amount of work done in this field [1-4] the physical mechanisms involved in contact formation is still a topic of controversy. The barrier height of Schottky contacts on GaAs has been proven to be independent on the metal work function. Observations show that the pinning position of the Fermi level for many metals as well as for oxygen on GaAs falls within two narrow ranges of ~ 0.7 and ~ 0.95 eV below the conduction-band minimum (CBM) [5]. Many models have been developed to explain metal-independent near-midgap pinning levels.

One model, called the "effective work function," involves metallurgical effects, due either to clustering of adsorbed metal atoms or to disruption of the semiconductor lattice induced by metal deposition [6]. This model suggest that the Fermi level at the surface is not fixed by interface states but rather is related to the work functions of micro-clusters of the interface phases resulting from oxygen contamination or metal-semiconductor reactions that occur during metallization. For most compounds metallization or oxidation results in the formation of cation alloys along with the anion compounds, and in some cases free excess anions. The difference between the work function of the anions and the semiconductor electron affinity is found to be in good agreement with the major barrier height of Au on many III-V and some II-VI compounds [6].

The results of photoemission spectroscopy (PES) studies on unannealed thin metal film/semiconductor systems (sub- to several monolayer

coverages), led to the development of a microscopic model--the unified-defect model [5,7]. This model suggests that, for metal/III-V semiconductors, the localized states responsible for pinning the interface Fermi level are associated with native point defects, at or near the semiconductor surface, induced by the deposition of foreign atoms. Spicer et al. [5,7] suggested that two defects are responsible for these two levels: an acceptor and a donor level. These authors suggested that the pinning position of the Fermi level of Au on n-type GaAs is at the donor level of the unified-defect model, due to the formation of an atomic dipole at the interface. The driving force for this dipole was attributed to strong tendency to attract electrons at the interface due to its large electronegativity. This depletes electrons from the 0.95 eV donors, thus pinning the Fermi level at that point even for n-type GaAs. This type of pinning behavior was found most recently as well for Pd, Ag and Cu [8]. Grant et al. [9] attributed these two levels to only one defect. Weber et al. [10] found experimentally that bulk As_{Ga} double donors have two energy levels essentially identical with interface Fermi-level pinning positions.

In contrast to these models, several authors suggest Fermi level pinning at Schottky contacts to be due to the properties of perfect metal-semiconductor interface [11-13]. Thus an experiment is needed to test if anion antisite or other defects are involved in the Fermi-level pinning at metal/GaAs interfaces.

Room-temperature deposition of several monolayers of Au onto clean cleaved GaAs (110) surfaces results in the transition of a system in which the Fermi-level is unpinned to a system in which the Schottky-

barrier height is fully established. Barrier heights on unannealed thick-metal film diodes (~100 nm) determined by electrical measurements are found to be essentially identical to those reported at the initial stages of Schottky-barrier formation (several monolayers). However, annealing of thick metal film Au/n-GaAs devices above the Au-Ga eutectic temperature (360°C) leads to "ohmic" behavior, while annealing of sub-monolayer to several-monolayer coverages of Au on n-GaAs results in a significant barrier.

Currents through the ohmic-like contacts at the periphery of the device were found to dominate the I-V characteristics for annealed devices. However, under the central portion of the device away from the perimeter, a rectifying large barrier device is found, even for anneals to 500°C [14-17]. Because Au has a high work function and is not known to form a shallow donor level in GaAs, the physical mechanism responsible for this "ohmic" behavior in the device is still unclear.

These structures are of particular interest, as they allow one to study barrier-type behavior as well as ohmic behavior in the same Au-GaAs system. Therefore, in this study electron microscopy and microscopic analytical methods were applied to as-deposited, annealed and mesa-etched Au contacts deposited on both UHV-cleaved, air-exposed and chemically prepared GaAs surfaces.

Experimental Procedure

The structure and electrical properties of Au contacts on GaAs have been studied by analytical and high resolution transmission electron microscopy (TEM), combined with electrical characterization.

To remove any unnecessary variables e.g. impurities on the GaAs surface, the diodes which were used in this study were produced on clean GaAs surfaces formed by cleaving in ultra-high vacuum (UHV) with the metal deposited in situ. Bulk n-GaAs bars (Si concentration $\sim 2 \times 10^{17}/\text{cm}^3$) were placed in an UHV chamber that was baked out to obtain a vacuum of $\sim 2 \times 10^{-10}$ torr. The bars were cleaved along their (110) planes. Au was then deposited in situ using a resistance type evaporator without breaking vacuum or additional heating (during deposition the vacuum was kept $< 4 \times 10^{-10}$ torr). To observe the contamination influence on the electrical and structural contact properties a second batch of Au diodes were deposited on the samples cleaved in air in the same vacuum chamber. In order that the air-exposed surfaces were not subjected to any unnecessary heat before metallization a chamber bakeout was not performed. For the diodes produced on the air-exposed surfaces, the pressure during the metal deposition was approximately 10^{-7} torr. The Au thickness for these two kind of diodes was ~ 100 nm. These two kinds of samples were annealed for 10 min at 405°C in a N_2 atmosphere. For comparison to diodes formed used in typical commercial GaAs processing technology, the third batch of samples was prepared by deposition of Au layers on chemically cleaned samples [17,18]. Electron-beam evaporation was used in the contact fabrication process. The annealing in 95% of Ar and 5% of H_2 was done for the same period of time and temperature as for the first two kind of samples.

Results

Cross-section of all three batches of unannealed Au layers (1) deposited in situ on UHV clean cleaved, (2) on air-exposed and (3) on chemically treated surfaces are very similar. The interfaces in all three cases are abrupt. The gold layer is polycrystalline with grain size 50-100 nm.

Significant differences between these samples occur after annealing at 405°C for 10 min (Fig. 1). For the UHV cleaved samples the interface remains flat and abrupt despite the annealing process (Fig. 1a). The same annealing treatment for the Au samples deposited on GaAs cleaved in air results in the formation of metallic protrusion at the interface (Fig. 1b). Such protrusions were observed in the past for annealed Au-Ni-Ge contacts [19,20] and Au contacts [21] and it was concluded that an elevated temperature gives a sufficient condition for their formation. Two different protrusion shapes are observed on the interface (Fig. 1b) using an electron beam parallel to the (110) GaAs: triangular whose sides are delineated by GaAs (111) planes and multifaceted delineated by GaAs (111), (110) and (100) planes. A high density of twins along Au (111) was found in the protrusions as well as in the Au layer between them (Fig. 1b). No other crystallographic phases besides Au were detected by electron diffraction methods.

Even more complicated interfaces were observed in annealed Au/GaAs samples formed on chemically prepared GaAs surfaces. The gold layer was separated from the GaAs substrate by a thin oxide band. In many areas, the interface was found to be very flat and abrupt (Fig. 1c). However, islands of gold with a wide range of shapes were found below the oxide

layer as well. These islands were epitaxially regrown with a much smaller density of defects than in the layer above the oxide. The observation of separated islands below the oxide layer would suggest that a thick gold layer breaks the oxide and gold diffuses into the GaAs substrate as suggested by Lu [22]. However an alternate and attractive possibility is that the gold diffuses through already existing pinholes in the oxide [18]. This suggestion would also explain why the observed gold grains are spread along the interface. In the case that solid state diffusion would take place through the oxide layer the existence of separated Au islands below the oxide would be difficult to explain.

X-ray spectra taken from the interfaces from the three batches of samples described above show distinguishable differences in the intensity of the oxygen line. The amount of oxygen detected at the interface was greatest in the samples where GaAs was treated chemically prior to the gold deposition (Fig. 2) and it was not present at all on the UHV cleaved samples. These observations show that GaAs is very sensitive to oxidation and that the interface morphology is strongly influenced by the surface preparation prior the Au deposition. This demonstrates that the protrusion formation is not the result of annealing at elevated temperature alone but it is clearly affected by the surface preparation technique.

As determined from I-V and C-V characteristics there was not a large difference in barrier height for the Au diodes deposited in situ on UHV-cleaved GaAs samples and deposited on the samples cleaved in air (Table I). A more serious problem is that the electrical characteristics of samples which were air exposed before Au deposition were found

to age with time and/or exposure to electrical measurements using large-bias voltage. The samples cleaved in the UHV condition do not show such aging. This is a very important issue for the reliability of devices built on oxidized surfaces.

Detailed analytical studies were done across the interfaces for the unannealed and annealed samples where Au was deposited in situ in UHV conditions [15,16]. The EDX spectra (Fig. 3a-c) show that both species, Ga and As, diffuse into the gold layer (Fig. 3a). (A higher Ga K_{α} intensity than As K_{α} intensity was usually observed in the Au layer.) The accumulation of As within GaAs ~10 nm from the metal/semiconductor interface was observed in both the annealed and unannealed cases, with higher As concentration in the annealed samples (Fig. 3b). (The EDX spectra taken on the GaAs substrate far from the interface with Au always show a slightly higher intensity of the Ga K_{α} line compared with the As K_{α} line (Fig. 3c)). TEM micrographs taken from annealed cross-section samples show clusters of a new phase (Fig. 4) in the GaAs in exactly the same areas where the As K_{α} intensity was increasing; therefore those clusters are considered as As rich. Large precipitates were occasionally observed close to the interface, and the selected area diffraction pattern of those structures shows spots characteristic of hexagonal As [15]. These observations show that GaAs deteriorates during gold deposition (even at room temperature), and presumably the formation of anion-rich point defects may be expected. Such defects may be responsible for pinning the Fermi level.

This situation is different at the periphery of the Schottky diodes (dots with diameter ~500 μm) [15,16], where As can escape easily. In

the case of annealed samples, extended Au crystallites were found at the edges of the Au dots by TEM observation of plan-view samples (Fig. 5). These gold crystallites are Ga rich and have been associated [14] with the leakage current observed in those samples (Fig. 5). Mesa-etching of those diodes removes the ohmic like current pathway at the periphery. The annealed Au/GaAs interfaces under the central portion of the device (away from the periphery) have a Schottky barrier height approximately 0.1 eV to 0.15 eV below the value of the barrier height for unannealed samples. This change in barrier height might be attributed to a decrease in the electronegativity of gold due to the observed increase of the Ga concentration in the gold overlayer. After mesa etching the elongated crystallites were no longer observed, but other areas of the contacts remain the same before and after mesa-etching.

Conclusions

Our investigations show that the As distribution is different underneath the Au dots and underneath the free GaAs surfaces between the Au dots. Obviously, the extent of As outdiffusion from under the Au contact is significantly reduced in comparison with As outdiffusion at the periphery due to the thick Au overlayer acting as a diffusion barrier. This indicates that the local stoichiometry of the crystal may be the key to understanding the difference between the Schottky/ohmic contact properties of the Au/GaAs system. The elongated Ga-rich Au crystallites on the periphery of Au contacts are strongly correlated with the change to ohmic behavior of those contacts. Arsenic accumulated near the interface in the Au/GaAs system is correlated with the Schottky

barrier formation, because this strong rectifying behavior was observed for both unannealed and annealed samples once the peripheral leakage current was removed.

In summary, a systematic study was performed which was able to correlate changes in electrical characteristics upon annealing with the morphological and structural properties of the Au/n-GaAs interface. An ohmic current pathway of the device was associated with near surface Ga-rich gold crystallites at the periphery which are formed upon annealing. The removal of this pathway by mesa-etching allowed us to accurately determine the characteristics of the central portion of the contact (i.e., not at the periphery). For this portion of the device, a decrease in the barrier height of over 0.1 eV was found and was attributed to a decrease in the electronegativity of the metal due to an increase in the Ga concentration in the predominantly-Au overlayer. Although the interface morphology was found to depend strongly on the surface preparation technique, large differences in the electrical characteristics were not found for these diodes.

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Table I. Barrier heights and ideality factors of as-deposited and annealed Au diodes on UHV cleaved and cleaved in air (110) n-GaAs.

Annealing temp.	UHV-cleaved			UHV-cleaved			Cleaved in air		
	doping $5 \times 10^{16} \text{ [cm}^{-3}\text{]}$			doping $2 \times 10^{17} \text{ [cm}^{-3}\text{]}$			doping $2 \times 10^{17} \text{ [cm}^{-3}\text{]}$		
	$\phi_b(I-V)$ ($\pm 0.02\text{eV}$) [eV]	n (± 0.02)	$\phi_b(C-V)$ ($\pm 0.05\text{eV}$) [eV]	$\phi_b(I-V)$ ($\pm 0.02\text{eV}$) [eV]	n (± 0.02)	$\phi_b(C-V)$ ($\pm 0.05\text{eV}$) [eV]	$\phi_b(I-V)$ ($\pm 0.02\text{eV}$) [eV]	n (± 0.02)	$\phi_b(C-V)$ ($\pm 0.05\text{eV}$) [eV]
Room temp.	0.92	1.05	1.00	0.87	1.10	0.95	0.83	1.09	0.9
150°C	0.91	1.06	0.99	—	—	—	—	—	—
220°C	0.85	1.07	0.92	—	—	—	—	—	—
290°C	0.80	1.06	0.89	—	—	—	—	—	—
405°C ^{a)}	—	—	—	0.72	1.12	0.83	0.72	1.10	0.81
430°C ^{a)}	0.80	1.06	0.88	—	—	—	—	—	—
495°C ^{a)}	0.80	1.05	—	—	—	—	—	—	—

a) After mesa-etching

Figure Captions

- Fig. 1. Cross-sections of the annealed Au/GaAs interfaces: a) Au deposited in situ on UHV cleaved GaAs, b) Au deposited on the GaAs cleaved in air, c) Au deposited on chemically clean GaAs.
- Fig. 2. X-ray spectrum from the annealed GaAs interface. Gold was deposited on chemically clean GaAs. Notice high intensity of oxygen line; SiK_α line is from the dopant in n-GaAs.
- Fig. 3. EDX-spectra of annealed Au/GaAs diode (Au deposited in situ on UHV cleaved surface) from different areas of a cross-section sample marked by circles on Fig. 4: a) from the Au layer, b) from the GaAs ~10 nm from the interface with Au, c) from the GaAs substrate far from the interface (the Cu peak is an artifact from the sample holder and microscope column.)
- Fig. 4. The interface of Au/GaAs sample (deposition in situ in UHV condition, annealing for 10 min at 405°C). Clusters of arsenic rich phase are seen in the GaAs ~10 nm below the interface. The circles represent the positions and the size of the electron beam during analysis.
- Fig. 5. Periphery of Au diode after annealing for 10 min at 405°C (Au deposited in situ in UHV condition). The extended Au crystallites are growing from the Au dots into surrounding GaAs. The EDX spectra taken from those crystallites show higher intensity of GaK_α line than from the substrate between them.
- Fig. 6. I-V characteristics of Au diodes on n-GaAs. The lower curve represents the forward and reverse I-V characteristic of the

unannealed diode ($\phi_b = 0.87$ eV). After annealing at 405°C for 10 min, the I-V characteristics are found to be almost completely dominated by non-rectifying peripheral leakage current, see upper trace (the results for forward bias greater than -0.25 V indicate a small rectifying barrier). The middle curve shows the strong rectifying diode characteristics ($\phi_b = 0.72$ eV) after elimination of the peripheral leakage current by mesa-etching.

XBB 862-1034

Fig. 1

XBL 861-165 A

Fig. 2

a **b** **c**

XBL 8510-4315A

Fig. 3

XBB 857-5115A

Fig. 4

XBB 862-1035

Fig. 5

XBL 862-545

Fig. 6

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