### UC San Diego UC San Diego Electronic Theses and Dissertations

### Title

An image rejection circuit with sign detection only

### Permalink

https://escholarship.org/uc/item/5xb5c9vd

#### **Author** Lerstaveesin, Supisa

# Publication Date 2006

Peer reviewed|Thesis/dissertation

### UNIVERSITY OF CALIFORNIA, SAN DIEGO

#### An Image Rejection Circuit with Sign Detection Only

A dissertation submitted in partial satisfaction of the requirements

for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Supisa Lerstaveesin

Committee in charge:

Professor Bang-Sup Song, Chair

Professor Peter M. Asbeck

Professor Chung-Kuan Cheng

Professor Vlado A. Lubarda

Professor Truong Nguyen

2006

Copyright Supisa Lerstaveesin, 2006 All rights reserved. The Dissertation of Supisa Lerstavees in is approved, and it is acceptable in quality and form for publication on microfilm:



University of California, San Diego

2006

To my dad, mom, and sister

# **Table of Contents**

Signature Pageiii
Dedicationiv
Table of Contentsv
List of Tables
List of Figuresix
Acknowledgments
Vitaxv
Abstractxvi
Chapter 1 Introduction
1.1 Motivation and Background
1.2 Thesis Organization
Chapter 2 Image Rejection Architectures
2.1 Hartley Image Reject Architecture
2.2 Weaver Image Reject Architecture
2.3 Polyphase Architecture
2.4 Complex Filter Architecture
2.5 Complex $\Delta\Sigma$ Modulator Architecture
2.6 Analog Calibration Techniques

2.7 Digital Calibration Techniques	32
2.8 Digital Signal Decorrelation Technique	34
2.8.1 Background on LMS Adaptive Decorrelation	34
2.8.2 Symmetric Adaptive Decorrelation	
Chapter 3 System Design	40
3.1 Zero-IF and Low-IF Systems	40
3.2 Gain and Phase Error Correction	41
3.3 Gain and Phase Error Detection	45
3.4 Comparison of Magnitude Detection and Sign Detection	48
3.5 Stability of Detection Algorithm	50
3.6 Acknowledgement	53
Chapter 4 Circuit Implementation	54
4.1 Three Possible Implemented Combinations	54
4.2 Step Size and Accumulation Period	59
4.3 Complex Baseband S/H	60
4.3.1 Bottom Plate S/H	61
4.3.2 Operational Amplifier	63
4.3.3 Trim Capacitor	68
4.4 Analog Comparator	68
4.5 Synchronous Up/Down Counter	72
4.6 Phase Clock Generator	74
4.7 Acknowledgement	75

Chapter 5 Experimental Results	76
5.1 Prototype IC Layout	76
5.2 Test Setup	77
5.3 Complex Baseband Spectrums	79
5.4 Constellations and Eye Diagrams	85
5.5 Effect of I/Q Imbalance on Probability of Error	
5.6 Acknowledgement	91
Chapter 6 Conclusion	92
Bibliography	94

# **List of Tables**

Number	Page
Table 4.1: Device Characteristics of Gain-Boosted Telescopic Amplifier	
Table 4.2: Device Characteristics of N-side Auxiliary Amplifier	
Table 4.3: Device Characteristics of P-side Auxiliary Amplifier.	67
Table 4.4: Device Characteristics of Preamplifier .	70
Table 4.5: Device Sizes of Latch	71
Table 5.1: Summary of Measured Performance	

# **List of Figures**

Number	Page
Figure 1.1: Real down-conversion receiver	2
Figure 1.2: Image problem.	2
Figure 1.3: Complex down-conversion receiver.	4
Figure 1.4: Complex image suppression.	5
Figure 1.5: Image rejection receiver with gain and phase errors	6
Figure 1.6: Impact of gain and phase error on IRR	8
Figure 2.1: Hartley image rejection architecture	12
Figure 2.2: Function of -90° phase shift	14
Figure 2.3: Image signal suppression in Hartley architecture.	15
Figure 2.4: Hartley image rejection architecture with RC-CR network	16
Figure 2.5: Weaver image reject architecture	17
Figure 2.6: Image signal suppression in Weaver architecture	19
Figure 2.7: Secondary image spectrums	20
Figure 2.8: Polyphase filter.	21
Figure 2.9: Down-conversion receiver with polyphase filter	22
Figure 2.10: Double down-conversion receiver with polyphase filters	23
Figure 2.11: Down-conversion receiver with complex filter.	24

Figure 2.12: Active-RC implementation of single pole complex filter	24
Figure 2.13: Frequency response and pole plot of complex filter	25
Figure 2.14: Down-conversion receiver with complex $\Delta\Sigma$ ADC	26
Figure 2.15: Fourth order complex modulator diagram.	27
Figure 2.16: An example of frequency responses of STF and NTF	27
Figure 2.17: External controlled digital error correction [14]	
Figure 2.18: Down-conversion receiver with offline analog calibration	29
Figure 2.19: Down-conversion receiver with online analog calibration	31
Figure 2.20: Digital error correction in [17]	32
Figure 2.21: (a) Sub-sampling mixers. (b) Phase error detection	34
Figure 2.22: Basic LMS adaptation for noise cancellation.	
Figure 2.23: Complex signal and complex image leakage	
Figure 2.24: Signal separation adaptation for <i>I/Q</i> imbalance	
Figure 3.1: Zero-IF down-conversion and complex zero-IF image	41
Figure 3.2: Low-IF down-conversion and complex low-IF image	41
Figure 3.3: Non-ideal complex channel and its simplified linear model	42
Figure 3.4: Proposed image rejection concept.	43
Figure 3.5: <i>I/Q</i> vectors before and after image rejection	45
Figure 3.6: $I/Q$ path gain and phase error detection.	47
Figure 3.7: Direction of gain and phase error update	51
Figure 3.8: Recursive function of the detection error	52
Figure 3.9: IRR versus gain and phase errors	53

Figure 4.1: Image rejection for low- or zero-IF receiver	55
Figure 4.2: Digital image rejection system	56
Figure 4.3: Hybrid image rejection system.	57
Figure 4.4: Analog image rejection system.	
Figure 4.5: Simulation of the accumulated correlation.	60
Figure 4.6: Complex baseband S/H	61
Figure 4.7: Real bottom plate S/H	
Figure 4.8: Gain-boosted telescopic cascode operational amplifier	64
Figure 4.9: Switch-capacitor common-mode feedback circuit	65
Figure 4.10: Auxiliary folded cascode amplifier for N-side	66
Figure 4.11: Auxiliary folded cascode amplifier for P-side	67
Figure 4.12: 9-bit trim capacitor	68
Figure 4.13: Analog comparator	69
Figure 4.14: Preamplifier	69
Figure 4.15: Latch.	70
Figure 4.16: Effect of comparator offset on IRR.	72
Figure 4.17: N+1 bit synchronous counter with ripple chain	73
Figure 4.18: Phase clock generator.	74
Figure 4.19: Phase clock timing diagram.	75
Figure 5.1: Die photo	77
Figure 5.2: Test setup diagram.	78
Figure 5.3: Complex 256-QAM spectra before image rejection	79

Figure 5.4: Complex 256-QAM spectra after 12-b digital image rejection.	80
Figure 5.5: Complex 256-QAM spectra after hybrid image rejection.	80
Figure 5.6: Complex 256-QAM spectra after analog image rejection	81
Figure 5.7: Complex 256-QAM spectra after 15-b digital image rejection	82
Figure 5.8: Complex 256-QAM spectra after 10-b digital image rejection	82
Figure 5.9: Complex 256-QAM spectra after 8-b digital image rejection.	83
Figure 5.10: Signal and blocker spectra before image rejection.	84
Figure 5.11: Signal and blocker spectra after 15-b digital image rejection	84
Figure 5.12: Measured 64-QAM constellation before and after image rejection	86
Figure 5.13: Measured 256-QAM constellation before and after image rejection	86
Figure 5.14: Measured 64-QAM eye before and after image rejection.	87
Figure 5.15: Measured 256-QAM eye before and after image rejection.	87
Figure 5.16: Probability of error versus SNR of 64-QAM system	89
Figure 5.17: Probability of error versus SNR of 256-QAM system	90
Figure 5.18: Probability of error versus IRR of 64-QAM system	90
Figure 5.19: Probability of error versus IRR of 256-QAM system	91

## Acknowledgments

I am very indebted and thankful to my advisor, Professor Bang-Sup Song. He guides me to an interesting topic of image rejection and also provided an invaluable help on the dissertation and my professional development. He always provides insightful comments that greatly improve my thesis. I am grateful for the opportunity to have worked under his guidance. I also would like to extend great appreciation to my other thesis committee members: Professor Peter M. Asbeck, Professor Truong Nguyen, Professor Chung-Kuan Cheng and Professor Vlado A. Lubarda for their valuable comments.

Many discussions with my colleagues help improve the quality of this research. I am thankful to work with Sourja Ray, Yunshaing Shu, Manoj Gupta, and David Kang. I would like to thank Professor Bruce A. Wooley to support me to come to UCSD. In addition, I would like to extend my thanks to Thai friends to make my life in San Diego an unforgettable experience. Special thanks to Panu Chaichanavong for his support and helpful comments to improve this thesis.

My great gratitude goes to the Anandamahidol Foundation, Thailand, and Department of Electrical and Computer Engineering, UCSD for financial support.

Most of all, I would like to thank my parents and my sister, who have provided continual support and encouragement in all of my endeavors.

Chapter 3, Chapter 4, and Chapter 5, in part, have been submitted for publication as it appears in IEEE Journal of Solid-State Circuits, S. Lerstaveesin and B. Song, Dec 2006. The dissertation author was the principle researcher and author of this paper.

## Vita

1979	Born, Bangkok, Thailand
2000	B.Eng. Electrical Engineering Chulalongkorn University Bangkok, Thailand
2000	Test Engineer Philips Semiconductor, Inc Bangkok, Thailand
2003	M.S. Electrical Engineering Stanford University Stanford, CA
2003-2005	Research Assistant University of California, San Diego San Diego, CA
2004	Design Engineer (Internship) Marvell, Inc San Jose, CA
2005-2006	Design Engineer Chrontel, Inc San Diego, CA
2006	Ph.D. Electrical Engineering University of California, San Diego La Jolla, CA

## **Publications**

S. Lerstaveesin and B. Song, "A Complex Image Rejection Circuit with Sign Detection Only," *IEEE Journal of Solid-State Circuits*, Dec. 2006.

S. Lerstaveesin and B. Song, "A Complex Image Rejection Circuit with Sign Detection Only", *ISSCC Dig. Tech. Papers*, pp. 454-455, Feb., 2006.

S. Lerstaveesin, N. Wongkomet, and N. Wongkomet., "A Low Power Baseband Channel Filter for Cordless Telephone Receivers", *IEEJ International Analog VLSI Workshop*, 2001.

#### **ABSTRACT OF THE DISSERTATION**

An Image Rejection Circuit with Sign Detection Only

by

Supisa Lerstaveesin

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems) University of California, San Diego, 2006

Professor Bang-Sup Song, Chair

In direct-conversion receivers, radio frequency (RF) signals are downconverted to zero or low intermediate frequency (IF) using complex in-phase and quadrature (I/Q) mixers with no prior image filtering. Due to I/Q path gain and phase errors, image leaks into the signal band during the down-conversion process. A generic image rejection algorithm is proposed to reject image in the baseband using a zero-forcing sign-sign adaptive feedback concept. The orthonormal property of complex I/Q channels is exploited to update their gain and phase errors by detecting only four signs, and image is corrected with four multiplications and two additions. The correction and detection algorithms can be implemented in a digital or analog form. The analog correction circuit consists of a complex baseband sample and hold (S/H) with trim capacitors. At 40 MS/s sampling rate, the analog, 12-b digital, and hybrid (analog correction and digital detection) image rejection circuits achieve an image rejection of 62, 65, and 65 dB, respectively. The prototype chip fabricated in 0.18-µm CMOS occupies 800 x 450 µm<sup>2</sup>, and consumes 23 mW at 1.8 V.

# Chapter 1 Introduction

In recent efforts to integrate RF receivers without RF or IF image filters, complex down-conversion architectures similar to Hartley and Weaver receivers have been revised with digital signal processing. In direct-conversion zero-IF or low-IF receivers, the down-converted baseband signal is complex and represented by two I/Q real signals. Gain and phase errors between them result from analog parameter variations in local oscillators, mixers, automatic gain controls (AGCs), filters, and even analog-to-digital converters (ADCs). They limit image rejection ratio (IRR) to about 30 ~ 40 dB. To improve IRR, many analog solutions such as double quadrature mixer, complex  $\Delta\Sigma$  modulator, complex polyphase filter, and I/Q oscillator have been suggested [1]-[5]. These analog methods still rely on I/Q path gain matching, and their effectiveness is limited to specific local elements, and image at the system level still remains. The goal of this thesis is to design a low-complexity low-power image

rejection circuit that achieves high IRR. In addition, the circuit should require no test tone and be able to correct system-level image regardless of the source.

### **1.1 Motivation and Background**

In conventional RF receiver, the heterodyne architecture consists of a low noise amplifier (LNA), an image reject filter, a mixer, and a channel select filter as shown in Figure 1.1.



Figure 1.1: Real down-conversion receiver.



Figure 1.2: Image problem.

Referring to Figure 1.2, if the image reject filter were not present, the real mixer multiplies the local oscillator (LO) signal,  $A_{LO}cos(\omega_{LO}t)$ , with the input signals, and so the input signals at  $\omega_{RF} = \omega_{LO} + \omega_{IF}$  and  $\omega_{RF} = \omega_{LO} - \omega_{IF}$  are down-converted to the same IF; one is the desired signal and the other is the image signal. The low-side LO down-conversion is assumed through out this thesis. Thus, the desired signal is at  $\omega_{SIG} = \omega_{LO} + \omega_{IF}$  and the image signal is at  $\omega_{IM} = \omega_{LO} - \omega_{IF}$ . Therefore, the RF image reject filter is required to suppress the image signal so that the output after downconversion contains only the desired signal. Then the channel select filter passes the desired channel and attenuates the adjacent channels. For high sensitivity, high IF is preferred to improve the rejection of the image signal. However, for high selectivity, low IF is preferred to improve the attenuation of the nearby channels. The trade-off between sensitivity and selectivity in heterodyne receivers restricts the frequency planning and requires external high-Q filters such as LC or surface acoustic wave (SAW) filters. In most existing RF receivers, IF is usually set at about  $1/10 \sim 1/20$  of the RF: 10.7 MHz for FM radio and 36 or 44 MHz for TV.

In modern RF receiver, the heterodyne architecture is replaced by the complex direct conversion zero-IF or low-IF architecture to eliminate the need for external image reject filter, and therefore it can be fully integrated on a single chip. In complex direct conversion receiver [6], the input RF signal is multiplied by two real local carriers with 90° phase difference as shown in Figure 1.3. Two I/Q signals at zero or low IF represent the real and imaginary parts of the complex baseband signal.



Figure 1.3: Complex down-conversion receiver.

The complex mixing process is mathematically equivalent to multiplying the real RF signal by a complex negative frequency carrier,  $e^{-j\omega_{LO}t} = \cos(\omega_{LO}t) - j\sin(\omega_{LO}t)$ . The complex signal I+jQ is the positive RF frequency signal moved down to IF while the complex image I-jQ is the negative RF frequency image moved up to IF. If the I/Q signals are perfectly matched in gain and 90° out-of-phase, only the desired complex signal I+jQ appears at baseband. In practice, I/Q path gain and phase errors cause the complex image to leak into the same baseband as shown in Figure 1.4. The baseband signal now contains both signal and image as if the complex local carrier also has a small positive frequency component. That is, the non-ideal complex carrier is now  $e^{-j\omega_{LO}t} + \gamma \cdot e^{j\omega_{LO}t}$ , where  $\gamma$  is a complex constant called the leakage coefficient. The IRR depends on the magnitude of this leakage coefficient.



Figure 1.4: Complex image suppression.

Consider a complex channel with a gain mismatch of  $\alpha$  and a phase mismatch of  $\theta$ . Both  $\alpha$  and  $\theta$  are assumed to be independent of frequency. This assumption is usually valid since I/Q mixers, AGCs, anti-aliasing filters, and ADCs found in most digital RF receivers have wide bandwidths, and digital I/Q channel filters are exact. However, in systems with analog channel filters,  $\alpha$  and  $\theta$  can be frequency-dependent. In such a case, the proposed algorithm loses some accuracy. In a single-tone example, the non-ideal I/Q signals are denoted by I' and Q' as in (1.1) and (1.2). Then, assuming  $\alpha$  and  $\theta$  are small, the non-ideal complex signal I'+jQ' and the non-ideal complex image I'-jQ' can be simplified as (1.3) and (1.4) using Taylor series approximation.

$$I' = (1 + \frac{\alpha}{2})\cos(\omega t + \frac{\theta}{2}) = (1 + \frac{\alpha}{2}) \left\{ \frac{e^{j(\omega t + \frac{\theta}{2})} + e^{-j(\omega t + \frac{\theta}{2})}}{2} \right\},$$
 (1.1)

$$Q' = (1 - \frac{\alpha}{2})\sin(\omega t - \frac{\theta}{2}) = (1 - \frac{\alpha}{2}) \left\{ \frac{e^{j(\omega t - \frac{\theta}{2})} - e^{-j(\omega t - \frac{\theta}{2})}}{2j} \right\},$$
 (1.2)

$$I' + jQ' \approx e^{j\omega t} + \left(\frac{\alpha - j\theta}{2}\right)e^{-j\omega t}, \qquad (1.3)$$

$$I' - jQ' \approx \left(\frac{\alpha + j\theta}{2}\right)e^{j\omega t} + e^{-j\omega t}.$$
 (1.4)

There are symmetric leakages between complex signal and complex image. Also the definitions of signal and image are inter-changeable. The signal I'+jQ' is approximately the ideal I+jQ plus I-jQ attenuated by  $(\alpha-j\theta)/2$ . Similarly, I'-jQ' is approximately the ideal I-jQ plus I+jQ attenuated by  $(\alpha+j\theta)/2$ . From (1.3) and (1.4), the image leakage coefficient  $\gamma$  is  $(\alpha-j\theta)/2$ , and the signal leakage coefficient  $\gamma^*$  is  $(\alpha+j\theta)/2$ , the complex conjugate of  $\gamma$ .



Figure 1.5: Image rejection receiver with gain and phase errors.

Now the IRR will be derived in terms of gain error and phase error. Let  $\omega_{SIG} = \omega_{LO} + \omega_{IF}$  denote the desired signal frequency and let  $\omega_{IM} = \omega_{LO} - \omega_{IF}$  denote the image signal frequency. Continuing with the single-tone example, the in-phase signal *I* in Figure 1.5 can be written as the sum of signal and image:

$$I = I_{SIG} + I_{IM}$$
  
=  $(1 + \frac{\alpha}{2})A\cos\left\{(\omega_{LO} - \omega_{SIG})t + \frac{\theta}{2}\right\} + (1 + \frac{\alpha}{2})A\cos\left\{(\omega_{LO} - \omega_{IM})t + \frac{\theta}{2}\right\}.$  (1.5)

Similarly, the quadrature signal after 90-degree phase shifter can be written as

$$Q_{90^{\circ}} = Q_{90^{\circ},SIG} + Q_{90^{\circ},IM} = (1 - \frac{\alpha}{2})A\sin\left\{(\omega_{LO} - \omega_{SIG})t - 90^{\circ} - \frac{\theta}{2}\right\} + (1 - \frac{\alpha}{2})A\sin\left\{(\omega_{LO} - \omega_{IM})t - 90^{\circ} - \frac{\theta}{2}\right\}.$$
(1.6)

Then the image in IF output signal is as follows.

$$IM = (1 + \frac{\alpha}{2})A\cos\left\{(\omega_{LO} - \omega_{IM})t + \frac{\theta}{2}\right\} + (1 - \frac{\alpha}{2})A\sin\left\{(\omega_{LO} - \omega_{IM})t - \frac{\theta}{2} - 90^{\circ}\right\}$$
$$= (1 + \frac{\alpha}{2})A\cos\omega_{IF}t\cos\frac{\theta}{2} - (1 + \frac{\alpha}{2})A\sin\omega_{IF}t\sin\frac{\theta}{2}$$
$$-(1 - \frac{\alpha}{2})A\sin\omega_{IF}t\sin\frac{\theta}{2} - (1 - \frac{\alpha}{2})A\cos\omega_{IF}t\cos\frac{\theta}{2}$$
$$\approx \alpha A\cos\omega_{IF}t\cos\frac{\theta}{2} - 2A\sin\omega_{IF}t\sin\frac{\theta}{2}.$$
(1.7)

On the other hand, the desired signal is approximately  $SIG=2A\cos\omega_{IF}t$ .

Therefore, IRR can be derived and approximated as the following.

$$\frac{1}{IRR} = \frac{IM^2}{SIG^2} \approx \frac{\alpha^2 A^2 \cos^2 \frac{\theta}{2} + 4A^2 \sin^2 \frac{\theta}{2}}{4A^2} \approx \frac{\alpha^2 + \theta^2}{4}.$$
(1.8)

The IRR is plotted as a function of gain error  $\alpha$  and phase error  $\theta$  in Figure 1.6. It is clear that the plot for constant IRR is circular. To achieve IRR higher than 60 dB, the gain error must be less than 0.1% and the phase error must be less than 0.1°.



Figure 1.6: Impact of gain and phase error on IRR.

### **1.2 Thesis Organization**

This thesis presents a generic image rejection algorithm to reject image later in the baseband using a zero-forcing sign-sign adaptive feedback concept [7]. Complex image rejection algorithm is reformulated with real signal processing. The orthonormal property of complex I/Q channels is exploited to update their gain and phase errors by detecting only four signs, and image is corrected with four multiplications and two additions. The proposed image rejection algorithm can be implemented in a digital, analog, or hybrid form.

Two key functional blocks to be added to the receiver for image rejection are an image rejecter and an error detector. If image rejecter is made digitally, IRR is ultimately limited by the quantization noise of I/Q ADCs, as is true for all digital methods. In fact, most RF systems have high-resolution ADCs for wide dynamic range to quantize signal with large blockers, and thus digital image rejection using such ADCs would suffice. In analog implementation, IRR is restricted by DC offsets of analog comparators used for sign detection. For an analog complex baseband S/H with a digital error detector, which is the hybrid form, the IRR is not limited by the resolution of ADCs. When applied to any direct-conversion zero-IF or low-IF receivers, the proposed baseband image rejection algorithm can suppress the total accumulated image at the system level irrespective of its sources using a simple post baseband processing. Therefore, any elaborate complex I/Q analog circuits, which have been used to improve IRR, are no longer necessary. With the proposed image rejection, RF receiver architecture can be greatly simplified.

This thesis is organized as follows. In Chapter 2, prior image rejection techniques are discussed. First, the conventional Hartley and Weaver architectures are

described, followed by an overview on some additional components for improving the Hartley architecture, such as polyphase filter, complex filter, and complex  $\Delta\Sigma$ modulator. Next, analog and digital calibration techniques for correcting I/O imbalance are explained. Finally, the digital signal decorrelation technique, which is the basis of the proposed image rejection, is described. Chapter 3 begins with a formulation of *I/Q* imbalance problem into complex channel model. Based on this model, the proposed gain and phase error correction algorithm is derived. Then the signal decorrelation and LMS techniques are used to develop the proposed error detection algorithm. The stability of the detection algorithm is analyzed. In Chapter 4, the implementation of a prototype image rejection circuit is presented. Three possible types of implementation—analog, digital, and hybrid—are described. All components within the circuit and their parameters are elaborated. Chapter 5 explains the experimental setup and results, including the signal and image spectra, eye diagrams and constellations. The thesis is concluded in Chapter 6, in which some possible future work is also discussed.

# Chapter 2 Image Rejection Architectures

This chapter reviews the existing image rejection techniques. First, the Hartley and Weaver architectures are explained, in particular how the image and the desired signals are distinguished, and how the image signal is suppressed. Then several techniques to make system components more robust to process and condition variations are presented. The techniques include making use of polyphase filter, complex filter, double quadrature mixer, and complex  $\Delta\Sigma$  modulator, and performing analog and digital calibrations. Finally, the digital signal decorrelation technique is described in detail.

### 2.1 Hartley Image Reject Architecture

Hartley image reject down-conversion architecture [8] shown in Figure 2.1 takes advantage of its complex down-conversion architecture to differentiate the desired signal and the image signal by using two down-conversion mixers, quadrature

LOs and low pass filters (LPFs). Let the RF input signal be  $A_{SIG} \cos(\omega_{SIG}t) + A_{IM} \cos(\omega_{IM}t)$ , which consists of the desired signal at  $\omega_{SIG}$  and the image signal at  $\omega_{IM}$ . The RF signal is multiplied by quadrature LOs,  $\cos(\omega_{LO}t)$  and  $\sin(\omega_{LO}t)$ , and low-pass filtered to obtain the IF signals at points A and B as in (2.1) and (2.2).

$$IF_{A} = \frac{A_{SIG}}{2}\cos(\omega_{SIG} - \omega_{LO})t + \frac{A_{IM}}{2}\cos(\omega_{LO} - \omega_{IM})t$$
(2.1)

$$IF_{B} = -\frac{A_{SIG}}{2}\sin(\omega_{SIG} - \omega_{LO})t + \frac{A_{IM}}{2}\sin(\omega_{LO} - \omega_{IM})t$$
(2.2)



Figure 2.1: Hartley image rejection architecture.

Since the low-side LO down-conversion is assumed,  $(\omega_{SIG} - \omega_{LO})$  and  $(\omega_{LO} - \omega_{IM})$  are positive and equal to  $\omega_{IF}$ . Although the IF signal of both desired

signal and image signal are on the same band at  $\omega_{IF}$ , the desired signal and the image signal rotate on the opposite directions as proved in complex scheme in (2.3).

$$IF_{A} + jIF_{B} = \frac{A_{SIG}}{2} \left( \cos \omega_{IF} t - j \sin \omega_{IF} t \right) + \frac{A_{IM}}{2} \left( \cos \omega_{IF} t + j \sin \omega_{IF} t \right)$$

$$= \frac{A_{SIG}}{2} e^{-j\omega_{IF} t} + \frac{A_{IM}}{2} e^{j\omega_{IF} t}$$
(2.3)

Since the complex mixer architecture down-converts the desired signal and the image signal to the same IF band but on the opposite phase rotations, the image signal can be eliminated by 90° phase shifting the quadrature signal  $IF_B$  and combining with the in-phase signal  $IF_A$ .

The function of -90° phase shifter is known as the Hilbert transform [9]. The impulse response h(t) of the Hilbert transform is given in (2.4), and the frequency response H(f) which is the Fourier transform of h(t) is shown in (2.5).

$$h(t) = \frac{1}{\pi t} \,. \tag{2.4}$$

$$H(f) = -j \operatorname{sgn}(f) = \begin{cases} +j & ; f < 0\\ 0 & ; f = 0\\ -j & ; f > 0. \end{cases}$$
(2.5)

Feeding the quadrature signal through the -90° phase shifter is equivalent to multiplying H(f) to input signal spectrum. That is, the positive frequency components of quadrature signal are multiplied by *-j*, whereas the negative frequency components of quadrature signal are multiplied by *j*. Figure 2.2 shows the -90° phase shift function

in frequency domain. The IF signal at point C (in Figure 2.1) after -90° phase shifted can be derived as in (2.6). It follows that the IF output signal, which is the sum  $IF_A+IF_C$ , is image free as shown in (2.7). The image signal suppression process is also explained in Figure 2.3. In addition, if the IF signal at point C is subtracted from IF signal at point A, the image signal can be obtained. Hence, we can select either the channel at  $\omega_{SIG}$  or the channel at  $\omega_{IM}$ .



Figure 2.2: Function of -90° phase shift.

$$IF_{C} = \frac{A_{SIG}}{2}\cos(\omega_{SIG} - \omega_{LO})t - \frac{A_{IM}}{2}\cos(\omega_{LO} - \omega_{IM})t. \qquad (2.6)$$

$$IF_{OUT} = \frac{A_{SIG}}{2} \cos(\omega_{SIG} - \omega_{LO})t. \qquad (2.7)$$



Figure 2.3: Image signal suppression in Hartley architecture.

In the Hartley architecture, the -90° phase shifter is realized with an RC-CR network as shown in Figure 2.4. Even though the output phases of RC-CR filter are frequency dependent, the phase difference between two outputs differs from the phase difference between two inputs by 90°. However, the magnitudes of outputs are equal only at  $\omega = 1/RC$ . Therefore, this architecture can be used only for narrow band system.



Figure 2.4: Hartley image rejection architecture with RC-CR network.

In practice, due to process variation, these two resistors and capacitors cannot have exactly the same values. As a result, the phase difference between two outputs is no longer 90° and the magnitudes of two outputs are not equal. Therefore, the image signal cannot be fully suppressed. These magnitude and phase errors degrade the IRR of the system.

### 2.2 Weaver Image Reject Architecture

To overcome the band limitation of the RC-CR filter and the image leakage problem due to the process variation of passive components, the Weaver image reject architecture [10] replaces the RC-CR networks with two active mixers. It is a dual conversion receiver with two LO frequencies,  $\omega_{LO1}$  and  $\omega_{LO2}$ , with the second frequency much smaller than the first one. Figure 2.5 shows a block diagram of the Weaver architecture.



Figure 2.5: Weaver image reject architecture.

It is clear that the first down-conversion part up to points A and B of Figure 2.5 is the same as in Figure 2.1. When applying RF signal of  $A_{SIG} \cos(\omega_{SIG} t) + A_{IM} \cos(\omega_{IM} t)$  to input of the Weaver architecture, the IF signals at A and B in (2.8) and (2.9) are the same as (2.1) and (2.2).

$$IF_{A} = \frac{A_{SIG}}{2}\cos(\omega_{SIG} - \omega_{LO1})t + \frac{A_{IM}}{2}\cos(\omega_{LO1} - \omega_{IM})t, \qquad (2.8)$$

$$IF_{B} = -\frac{A_{SIG}}{2}\sin(\omega_{SIG} - \omega_{LO1})t + \frac{A_{IM}}{2}\sin(\omega_{LO1} - \omega_{IM})t.$$
 (2.9)

After second down-conversion, the second IF signals at points C and D are derived in (2.10) and (2.11).

$$IF_{C} = \frac{A_{SIG}}{4} \cos(\omega_{SIG} - \omega_{LO1} + \omega_{LO2})t + \frac{A_{SIG}}{4} \cos(\omega_{SIG} - \omega_{LO1} - \omega_{LO2})t + \frac{A_{IM}}{4} \cos(\omega_{LO1} - \omega_{IM} - \omega_{LO2})t + \frac{A_{IM}}{4} \cos(\omega_{LO1} - \omega_{IM} - \omega_{LO2})t,$$
(2.10)

$$IF_{D} = \frac{A_{SIG}}{4} \cos(\omega_{SIG} - \omega_{LO1} + \omega_{LO2})t - \frac{A_{SIG}}{4} \cos(\omega_{SIG} - \omega_{LO1} - \omega_{LO2})t - \frac{A_{IM}}{4} \cos(\omega_{LO1} - \omega_{IM} + \omega_{LO2})t + \frac{A_{IM}}{4} \cos(\omega_{LO1} - \omega_{IM} - \omega_{LO2})t.$$
(2.11)

After subtracting the signal at point D from the signal at point C, the output signal is as shown in (2.12).

$$IF_{OUT} = \frac{A_{SIG}}{2}\cos(\omega_{SIG} - \omega_{LO1} - \omega_{LO2})t + \frac{A_{IM}}{2}\cos(\omega_{LO1} - \omega_{IM} + \omega_{LO2})t . (2.12)$$

When filtering out the high frequency component at  $(\omega_{LO} - \omega_{IM} + \omega_{LO2})$ , we can obtain the desired signal. Similar to Hartley architecture, Weaver architecture can also select either the channel at  $\omega_{SIG}$  or the channel at  $\omega_{IM}$ . The image channel can be obtained by combining the signals at point C and point D and filtering out the high frequency component at  $(\omega_{SIG} - \omega_{LO1} + \omega_{LO2})$ . Figure 2.6 shows how image signal is suppressed in Weaver architecture.



Figure 2.6: Image signal suppression in Weaver architecture.
Even though the Weaver image reject architecture can solve the band limit problem and reduce gain and phase errors due to mismatches of passive elements, the image rejection still relies on the path matching. Moreover, like other dual heterodyne receivers, the Weaver architecture has the secondary image problem [11] due to the second mixer.

For lower side LO1 and LO2, the secondary image sources are at frequency  $\omega_{IM2,1}$  and  $\omega_{IM2,2}$  as derived in (2.13) and (2.14). The spectrums of these secondary image signals are illustrated in Figure 2.7.

$$\omega_{IM2,1} = \omega_{LO2} - (\omega_{IF1} - \omega_{LO2}) + \omega_{LO1} = 2\omega_{LO1} + 2\omega_{LO2} - \omega_{SIG}, \qquad (2.13)$$

$$\omega_{IM2,2} = -\omega_{LO2} + (\omega_{IF1} - \omega_{LO2}) + \omega_{LO1} = \omega_{SIG} - 2\omega_{LO2}.$$
(2.14)



Figure 2.7: Secondary image spectrums.

### 2.3 Polyphase Architecture

Another way to improve the image leakage problem from the mismatches in passive components of the Hartley down-conversion architecture is to replace a 90° phase shift RC-CR filter with an asymmetric RC structure called polyphase filter [1]. A RC network polyphase filter is shown in Figure 2.8. Input signals *A* and *B* have 90° phase difference and input signals  $\overline{A}$  and  $\overline{B}$  are the 180° compliments of signals *A* and *B* which are readily available in differential implementation.



Figure 2.8: Polyphase filter.

A polyphase filter is more tolerant to R and C passive component mismatches than RC-CR network used in the Hartley architecture. The analysis on one output of the polyphase filter is as follows.

$$O_1 = A \left( \frac{1}{1 + j\omega RC} \right) + \overline{B} \left( \frac{j\omega RC}{1 + j\omega RC} \right).$$
(2.15)

From above equation, output  $O_I$  is the sum of -45° phase shift of the input A and 45° phase shift of the input  $\overline{B}$  at frequency  $1/2\pi RC$ . Thus, if the input A is 90° phase lag of the input  $\overline{B}$ , the two signals in the sum will cancel each other. In contrast, if the input A is 90° phase lead of the input  $\overline{B}$ , the two signals will strengthen each other. Therefore, since the inputs A and B, which are given in (2.1) and (2.2), are from quadrature down-conversion as shown in Figure 2.9, the output of polyphase filter will reinforce either the desired signal or image signal and cancel the other.



Figure 2.9: Down-conversion receiver with polyphase filter.

However, the polyphase filter also has the band-limitation problem as the RC-CR network. The problem of mismatch in passive elements is relieved but still remains. The mismatch problem can be much further relieved by using the double down-conversion architecture, which consists of two polyphase filters and four mixers as shown in Figure 2.10. The double quadrature down-conversion architecture [2] uses the first polyphase filter to generate the 90° phase different signals from RF input. The quadrature signals are down-converted using the four mixers and then image rejected by the second polyphase filter.



Figure 2.10: Double down-conversion receiver with polyphase filters.

### 2.4 Complex Filter Architecture

Similar to the Hartley image rejection architecture, complex filter exploit the phase relationship of the desired signal and image signal to accumulate the desired signal and cancel the image signal. Instead of using the RC-CR network, the complex filter [12] is applied as shown in Figure 2.11. An active RC implementation of the complex filter is shown in Figure 2.12.



Figure 2.11: Down-conversion receiver with complex filter.



Figure 2.12: Active-RC implementation of single pole complex filter.

The transfer function of the single pole complex filter shown in Figure 2.12 can be derived as in (2.16).

$$H(j\omega) = \frac{OUT_I}{IN_I} = \frac{A}{1 + \frac{j(\omega - \omega_C)}{\omega_O}},$$

$$A = -\frac{R_2}{R_1}, \quad \omega_O = \frac{1}{R_2C}, \quad \omega_C = \frac{1}{R_CC}.$$
(2.16)

From the above equation, the asymmetric frequency response and pole plot are shown in Figure 2.13. If there is no path mismatch, the out-of-band image is filtered out by the complex filter. However, similar to previous architectures, with gain and phase mismatches, the image leakage part will be on the same phase and same band as the desired signal which cannot be rejected by the complex filter. The advantage of the complex filter over the RC-CR filter and polyphase filter is that its bandwidth can be designed to pass the whole desired band and reject other bands.



Figure 2.13: Frequency response and pole plot of complex filter.

### **2.5** Complex $\Delta\Sigma$ Modulator Architecture



Figure 2.14: Down-conversion receiver with complex  $\Delta\Sigma$  ADC.

A  $\Delta\Sigma$  modulator has become an indispensable component for ADC in the CMOS digital receiver. The complex  $\Delta\Sigma$  modulator architecture is modified from  $\Delta\Sigma$  modulator to have asymmetric frequency responses of signal transfer function (STF) and noise transfer function (NTF) [3], which help the image suppression. The STF of complex  $\Delta\Sigma$  ADC can be an all-pass filter or a complex band-pass filter, which can reject the image signal but pass the desired band, whereas the NTF shapes the noise floor so that the noise in the desired signal band is greatly reduced. Figure 2.14 shows the diagram of quadrature down-conversion receiver with the use of a complex  $\Delta\Sigma$  modulator.



Figure 2.15: Fourth order complex modulator diagram.

An example of fourth-order complex chain of integrators with distributed feed forward and feedback paths [3] is shown in Figure 2.15. Each block is drawn in replicate for real and imaginary parts. By choosing complex constants  $A_1$ - $A_4$ ,  $B_1$ - $B_4$ and  $p_1$ - $p_4$ , the complex poles and zeros can be placed to get desired frequency responses of the STF and the NTF. Figure 2.16 shows an example of frequency responses of STF and NTF.



Figure 2.16: An example of frequency responses of STF and NTF.

Calibrating, trimming and tuning gain and phase to reduce mismatches may obtain higher IRR than simple analog I/Q matching methods. The hand tuning methods are proposed to adjust the variable gain amplifier for gain mismatch and vary the phase of the second local oscillator [13]. Image can also be rejected digitally using an externally-controlled AGC for gain correction and a bit error rate optimizer for phase correction [14] as shown in Figure 2.17. The gains *AI* and *AQ* and the phase correction  $\phi$  are typically selected manually.



Figure 2.17: External controlled digital error correction [14].

Although these methods can reduce mismatches, they require hand tuning or manual parameter selection. Hence, they cannot be used for mass products, for which an automatic calibration method is necessary. Automatic on-chip analog and digital calibration methods will be described in sections 2.6 and 2.7, respectively.

### 

### 2.6 Analog Calibration Techniques

Figure 2.18: Down-conversion receiver with offline analog calibration.

In most analog calibrations, a variable gain amplifier and a phase shifter are used to correct I/Q path gain and phase errors. Offline calibration is presented in [15] to correct the gain and phase mismatches in I/Q path by injecting the image tone. The diagram of down-conversion receiver with offline analog calibration is shown in Figure 2.18. Gain and phase errors are independently cancelled in second downconversion. The LMS algorithm is applied to gradually adjust the coefficients,  $w_1$  and  $w_2$ , to reduce the image tone to zero. Let the variable phase and variable gain blocks have transfer function of  $\theta = k_1 w_1$  and  $\alpha = k_2 w_2$ . With only image input, the output error is as follows.

$$\varepsilon = -y = A\sin(\omega_{LO2}t + \theta) - B \cdot \alpha \cos(\omega_{LO2}t). \tag{2.17}$$

From the general LMS coefficient update equation in (2.18), the coefficients to calibrate phase and gain errors,  $w_1$  and  $w_2$ , are as derived in (2.19). It should be noted that the phase error is assumed to be small in the derivation.

$$w(n+1) = w(n) - 2\mu\varepsilon \frac{\partial\varepsilon}{\partial w}.$$
(2.18)

$$w_{1}(n+1) = w_{1}(n) - 2\mu\varepsilon \frac{\partial\varepsilon}{\partial w_{1}},$$
  

$$= w_{1}(n) - 2\mu\varepsilon \{k_{1}A\cos(\omega_{LO2}t)\}.$$
  

$$w_{2}(n+1) = w_{2}(n) - 2\mu\varepsilon \frac{\partial\varepsilon}{\partial w_{2}},$$
  

$$= w_{2}(n) + 2\mu\varepsilon \{k_{2}B\cos(\omega_{LO2}t)\}.$$
  
(2.19)

After the image tone is driven to zero, the final LMS coefficients are used for operating mode. Obviously, this offline calibration cannot constantly track drifting parameters.

To track drifting parameters, an online calibration or compensation method is needed to continuously adapt correction coefficients. Figure 2.19 shows a downconversion receiver with online analog calibration, which is proposed in [16]. It also uses two control signals to correct gain and phase mismatches using variable gain and phase circuits. Since the outputs  $b_1$  to  $b_4$  can be approximated as in (2.20), the gain and phase errors can be extracted from the outputs using (2.21).



Figure 2.19: Down-conversion receiver with online analog calibration.

$$b_{1} \approx (1 + \frac{\alpha}{2}) A \cos\{(\omega_{LO1} - \omega_{LO2})t + \frac{\theta}{2}\},\$$

$$b_{2} \approx -(1 - \frac{\alpha}{2}) A \sin\{(\omega_{LO1} - \omega_{LO2})t - \frac{\theta}{2}\},\$$

$$b_{3} \approx (1 + \frac{\alpha}{2}) A \sin\{(\omega_{LO1} - \omega_{LO2})t + \frac{\theta}{2}\},\$$

$$b_{4} \approx (1 - \frac{\alpha}{2}) A \cos\{(\omega_{LO1} - \omega_{LO2})t - \frac{\theta}{2}\}.\$$
(2.20)

Then,

$$V_{\theta} = LPF\{(b4 - b1)(b2 - b3)\} \approx -\frac{1}{2}A^{2}\theta,$$

$$V_{\alpha} = LPF\{(b4 - b1)(b4 + b1)\} \approx -\frac{1}{2}\alpha A.$$
(2.21)

These correction coefficients are fed back to variable gain and phase circuit to adjust gain and phase errors, and thereby force the inside loop gain and phase errors to zero.

For these offline and online analog calibrations, the additional analog circuits such as variable gain, variable phase and extra multipliers are required. Moreover, the gain and phase mismatches correction relies on the accuracy of these extra circuits. Therefore, the digital calibrations are usually preferable.

### **2.7 Digital Calibration Techniques**

Image rejection in digital domain is preferable due to no mismatch in correction process. Several methods were proposed with the use of complicated computation [17]-[30]; some of which are described below. In 1981, Churchill [17] proposed to correct the I/Q imbalance by multiplying correction coefficients *E* and *P* to I/Q signal as shown in Figure 2.20.



Figure 2.20: Digital error correction in [17].

The correction coefficients are obtained from DFT of the I/Q signal samples. Define F to be the DFT of I+jQ. For N samples, F(1/NT) is the DFT value at test signal frequency, while F((N-1)/NT) is the DFT value at image signal frequency. The coefficients E and P can be calculated from the following equations.

$$E = 1 - \operatorname{Re} \left( 2 \frac{F(\frac{N-1}{NT})}{\left[ F^*(\frac{1}{NT}) + F(\frac{N-1}{NT}) \right]} \right), \qquad (2.22)$$
$$P = -\operatorname{Im} \left( 2 \frac{F(\frac{N-1}{NT})}{\left[ F^*(\frac{1}{NT}) + F(\frac{N-1}{NT}) \right]} \right). \qquad (2.23)$$

It was shown in [17] that

$$E = \frac{\cos\theta}{1+\alpha}, \ P = \frac{-\sin\theta}{1+\alpha}.$$
 (2.24)

It follows that the outputs  $OUT_I$  and  $OUT_Q$ , given in the figure, are image free.

Another digital image reject architecture was proposed by Pun [18]. It consists of sub-sampling mixers and phase error detection and correction. During calibration, the inputs  $X_I$  and  $X_Q$  to the sub-sampling mixers in Figure 2.21 (a) are set to test tone Iand ground, respectively. Two outputs of the sub-sampling mixers,  $I_I$  and  $Q_I$ , are sent to phase error detector in Figure 2.21 (b) to estimate the phase error  $\theta$  by integrating the I/Q product. During operation,  $X_I$  and  $X_Q$  are set to I and Q. The phase mismatch is corrected as follows.

$$I' = I_I + \frac{\theta}{2}Q_Q, \qquad (2.25)$$

$$Q' = Q_I + \frac{\theta}{2} I_Q. \qquad (2.26)$$



Figure 2.21: (a) Sub-sampling mixers. (b) Phase error detection.

### 2.8 Digital Signal Decorrelation Technique

Among all image rejection methods reported to date, the most general one is a post digital processing method for I/Q imbalance correction [26]-[30], which separates signal from image by least-mean-square (LMS) noise cancellation algorithm [31] and symmetric adaptive decorrelation [32].

#### 2.8.1 Background on LMS Adaptive Decorrelation

The advantage of the LMS adaptive filter is its ability to automatically adjust its own parameters with less requirement of knowledge on desired signal and undesired signal characteristics. It can operate under changing condition by adjusting itself to minimize error.

The adaptive noise canceller [31] is shown in Figure 2.22. The primary input is the desired signal *s*, degraded by uncorrelated noise  $n_0$ . If we have a reference signal *x* which is uncorrelated to the desired signal but correlated in some way with the noise  $n_0$ , it can be used to generate the output *y* which is a close replica to  $n_0$  by passing it through the adaptive filter weight *w*. By subtracting this signal *y* from the primary input, the system output *e* will be much closer to desired signal *s*.

The problem of finding the filter weight *w* can be formulated as an estimation problem: Given *x*, find an estimate of  $n_0$  that minimizes mean squared error. Assuming that the estimate *z* takes the form *z*=*wx*, it is well known that the weight *w* must satisfy the orthogonality condition [33] below.

$$\sum_{n} (n_0(n) - wx(n))x^*(n) = 0.$$
(2.27)

In other words, the estimation error must be uncorrelated with reference signal x. Since the desired signal s is assumed to be uncorrelated with x, the orthogonality condition can be rewritten as

$$\sum_{n} (s(n) + n_0(n) - wx(n))x^*(n) = \sum_{n} e(n)x^*(n) = 0.$$
(2.28)

Finding the weight w in close form is difficult. Moreover, statistics of signals may be time-varying. Thus, the weight w is usually computed adaptively using the LMS algorithm.



Figure 2.22: Basic LMS adaptation for noise cancellation.

The LMS algorithm is a technique for achieving the minimum expected squared error by iteratively estimating the gradient. Although there are several minimization algorithms that have better performance and faster convergence, the LMS algorithm requires only simple calculations. The LMS coefficient update equation is the following.

$$w(n+1) = w(n) + \mu \cdot e(n) \cdot x^{*}(n).$$
(2.29)

The LMS update equation is very intuitive. The weight *w* is adapted until e(n) and x(n) are uncorrelated, which makes *w* satisfy the orthogonality condition in (2.28).

Assuming that all signals are real rather than complex, the Sign-Sign (SS) LMS algorithm is even simpler. Compared to the LMS algorithm, it is more robust to offsets and less complex. The SS-LMS update equation is described as follows.

$$w(n+1) = w(n) + \mu \cdot \operatorname{sgn}(e(n)) \cdot \operatorname{sgn}(x(n)) .$$
(2.30)

In the I/Q imbalance problem, since image leaks into signal band and similarly signal also leaks into image band, the LMS adaptive noise cancellation is modified to be two loops coupling to each other. To separate those two, symmetric adaptive decorrelation is applied.

#### 2.8.2 Symmetric Adaptive Decorrelation

The symmetric signal decorrelation method for I/Q imbalance is based on the simple fact that signal and image are uncorrelated. In practice, image leaks into signal band, and similarly, signal leaks into image band. This symmetric leakage can be modeled using two small complex coefficients H and G as shown in Figure 2.23. Comparing this figure to Figure 1.4, the coefficient H is equivalent to  $\gamma$ . In the scope of I/Q imbalance problem, H and G are complex conjugate of each other. However, it should be noted that this may not be true for general symmetric signal decorrelation.



Figure 2.23: Complex signal and complex image leakage.

The complex signal I+jQ can be viewed as the positive frequency component at IF, and H is the image leakage coefficient into the signal. Similarly, the complex image I-jQ can be viewed as the negative frequency component at IF, and G is the signal leakage coefficient into the image. These bi-directional leakages can be removed as shown in Figure 2.24.



Figure 2.24: Signal separation adaptation for I/Q imbalance.

By comparing the LMS adaptive noise cancellation in Figure 2.22 with the signal separation algorithm in Figure 2.24, I'+jQ' can be considered as the desired signal with noise  $s+n_0$ , I''+jQ'' as the output e, and H as the correlation weight w. Although I'-jQ' is supposed to be the correlated noise x, it also has some correlation with the desired signal. Therefore, if I'-jQ' is used to eliminate the image signal leakage in I'+jQ', the desired signal will also be attenuated. Hence, I''-jQ'' which is the image signal after signal rejection, should be used as the correlated noise x. Thus, the weights H and G can be obtained from the following equations.

$$H(n+1) = H(n) + \mu \cdot \{I''(n) + jQ''(n)\} \cdot \{I''(n) - jQ''(n)\}^*, \qquad (2.31)$$

$$G(n+1) = G(n) + \mu \cdot \{I''(n) - jQ''(n)\} \cdot \{I''(n) + jQ''(n)\}^*.$$
(2.32)

Frequency-dependent multi-tap signal separation adaptation for these two coefficients is conceptually very general, but it suffers from phantom solutions [32]. In particular, it fails to converge if the signal is made of strong discrete tones such as TV, video, and sound carriers. Therefore, the signal needs to occupy the full bandwidth to update the frequency-dependent multiple taps [26]-[28]. On the other hand, single-tap adaptation taking advantage of the fact that two leakage coefficients are complex conjugate to each other performs as two identical LMS adaptation loops, and is known to converge well for all signal conditions [29]. Another variation of asymmetric one-loop adaptation saves power and area with shared computation resource [30].

It is shown in (2.31) and (2.32) that to detect errors and adjust H and G using the symmetric adaptive decorrelation technique, at least 8 multipliers and 8 adders are required for single tap adaptation. Taking advantage of the assumption that  $H = G^*$ , the LMS adaptive decorrelation technique can be applied, and only 4 multipliers and 4 adders are needed. This dissertation proposes a simplified version of single-tap adaptation algorithm to correct I/Q imbalance problem. It is implemented in real domain and uses only the signs of signals to detect the gain and phase error. The algorithm is discussed in Chapter 3.

## Chapter 3 System Design

### **3.1 Zero-IF and Low-IF Systems**

The zero-IF and low-IF down-conversions are shown in Figure 3.1 and 3.2. Since there are I/Q path mismatches in the down-conversion system, the complex images for zero-IF and low-IF system are as shown. For zero-IF system, the local oscillator frequency is the same as the desired signal frequency. Therefore the complex image is the desired signal itself but rotating in the opposite direction. For low-IF system, the local oscillator frequency is the anearby channels. The complex image of low-IF system is more critical than the complex image of zero-IF since the adjacent channel can be much stronger than the desired channel. However, both complex images of zero-IF and low-IF systems need to be eliminated, and since they are mathematically the same, they can be rejected with the same algorithm.



Figure 3.1: Zero-IF down-conversion and complex zero-IF image.



Figure 3.2: Low-IF down-conversion and complex low-IF image.

### **3.2 Gain and Phase Error Correction**

I/Q channels with gain and phase errors are modeled as a small-signal nonideal complex channel shown in the left side of Figure 3.3. They provide outputs I'and Q' as in (1.1) and (1.2). Since the errors are small, the non-ideal complex channel transfer function can be simplified as in (3.1). With the simplification, I' and Q' are linear combinations of I and Q as shown on the right side of Figure 3.3.



Figure 3.3: Non-ideal complex channel and its simplified linear model.

$$\begin{bmatrix} I'\\ Q' \end{bmatrix} = \begin{bmatrix} 1 + \frac{\alpha}{2} & -\frac{\theta}{2} \\ -\frac{\theta}{2} & 1 - \frac{\alpha}{2} \end{bmatrix} \begin{bmatrix} I\\ Q \end{bmatrix}.$$
 (3.1)

The process of rejecting the image is to recover the ideal orthonormal I/Q signals from I' and Q'. That is, by undoing what the non-ideal complex channel did to I/Q signals, the original complex signal can be restored. This is possible by inverting the matrix of the channel transfer function as in (3.2). This concept is graphically explained in Figure 3.4. Note that the image-free outputs from the image rejecter are I'' and Q''.

$$\begin{bmatrix} I''\\ Q''\end{bmatrix} = \begin{bmatrix} 1 - \frac{\alpha}{2} & \frac{\theta}{2}\\ \frac{\theta}{2} & 1 + \frac{\alpha}{2} \end{bmatrix} \begin{bmatrix} I'\\ Q'\end{bmatrix}.$$
 (3.2)



Figure 3.4: Proposed image rejection concept.

Mathematically, the image rejected I'' and Q'' signals contain higher-order terms of  $\alpha$  and  $\theta$ . From the simplified channel model in (3.1) and the image rejecter in (3.2), I'' and Q'' are orthonormal as derived in (3.3), and very close to the ideal I and Q.

$$\begin{bmatrix} I''\\Q''\end{bmatrix} = \begin{bmatrix} 1 - \frac{\alpha^2}{4} - \frac{\theta^2}{4} & 0\\ 0 & 1 - \frac{\alpha^2}{4} - \frac{\theta^2}{4} \end{bmatrix} \begin{bmatrix} I\\Q \end{bmatrix} \approx \begin{bmatrix} I\\Q \end{bmatrix}$$
(3.3)

However, without the simplified channel model, outputs I'' and Q'' can be derived from (1.1), (1.2), and (3.2) as follows. Assuming that the third- and higher-order terms of  $\alpha$  and  $\theta$  are negligible, then  $\cos(\theta)$  and  $\sin(\theta)$  can be approximated by  $1-\theta^2/2$  and  $\theta$ .

$$I'' = (1 - \frac{\alpha}{2})I' + \frac{\theta}{2}Q',$$
  

$$= (1 - \frac{\alpha}{2})\left[(1 + \frac{\alpha}{2})\cos(\omega t + \frac{\theta}{2})\right] + \frac{\theta}{2}\left[(1 - \frac{\alpha}{2})\sin(\omega t - \frac{\theta}{2})\right],$$
  

$$= (1 - \frac{\alpha^{2}}{4})\left[(1 - \frac{\theta^{2}}{8})\cos(\omega t) - \frac{\theta}{2}\sin(\omega t)\right] + (\frac{\theta}{2} - \frac{\alpha\theta}{4})\left[(1 - \frac{\theta^{2}}{8})\sin(\omega t) - \frac{\theta}{2}\cos(\omega t)\right],$$
  

$$= (1 - \frac{\alpha^{2}}{4} - \frac{3\theta^{2}}{8})\cos(\omega t) - \frac{\alpha\theta}{4}\sin(\omega t).$$

$$Q'' = (1 + \frac{\alpha}{2})Q' + \frac{\theta}{2}I',$$

$$= (1 + \frac{\alpha}{2})\left[(1 - \frac{\alpha}{2})\sin(\omega t - \frac{\theta}{2})\right] + \frac{\theta}{2}\left[(1 + \frac{\alpha}{2})\cos(\omega t + \frac{\theta}{2})\right],$$

$$= (1 - \frac{\alpha^{2}}{4})\left[(1 - \frac{\theta^{2}}{8})\sin(\omega t) - \frac{\theta}{2}\cos(\omega t)\right] + (\frac{\theta}{2} + \frac{\alpha\theta}{4})\left[(1 - \frac{\theta^{2}}{8})\cos(\omega t) - \frac{\theta}{2}\sin(\omega t)\right],$$

$$= (1 - \frac{\alpha^{2}}{4} - \frac{3\theta^{2}}{8})\sin(\omega t) + \frac{\alpha\theta}{4}\cos(\omega t).$$
(3.4)

Equation (3.4) is rearranged into matrix format in (3.5). It is clear that I'' and Q'' are still orthonormal, and very close to the ideal I and Q. The two vectors before and after image rejection are also conceptually sketched in Figure 3.5.

$$\begin{bmatrix} I''\\ Q''\end{bmatrix} = \begin{bmatrix} 1 - \frac{\alpha^2}{4} - \frac{3\theta^2}{8} & \frac{-\alpha\theta}{4} \\ \frac{\alpha\theta}{4} & 1 - \frac{\alpha^2}{4} - \frac{3\theta^2}{8} \end{bmatrix} \begin{bmatrix} I\\ Q \end{bmatrix} \approx \begin{bmatrix} 1 & 0\\ 0 & 1 \end{bmatrix} \begin{bmatrix} I\\ Q \end{bmatrix} = \begin{bmatrix} I\\ Q \end{bmatrix} . \quad (3.5)$$



Figure 3.5: *I/Q* vectors before and after image rejection.

Since the third- and higher-order terms are assumed to be negligible,  $|\alpha^3|$  and  $|\theta^3|$  have to be less than 2<sup>-12</sup> to achieve IRR of higher than 72 dB. Therefore,  $\alpha$  must be in the range of ±6.25% and  $\theta$  must be in the range of ±3.58°. In addition, the values of  $\alpha$  and  $\theta$  should be known accurately for the correct operation of this image rejection scheme. Hence, an accurate gain and phase error detection scheme is required.

### **3.3 Gain and Phase Error Detection**

Small errors of  $\alpha$  and  $\theta$  still exist in the image-rejected *I* and *Q* (*I*" and *Q*") signals unless exact values of  $\alpha$  and  $\theta$  are used in (3.2). These residual errors are reduced adaptively with a zero-forcing feedback loop. The gain error  $\alpha$  can be estimated by low-pass filtering  $I^2-Q^2$  as in (3.6). The low-pass filtered  $I^2-Q^2$  will converge to zero if *I* and *Q* have the same magnitude. Similarly, the phase error can be obtained using the orthogonal property of I/Q signals. Low-pass filtering the product

of *I* and *Q* yields the phase error of  $-\theta/2$  as in (3.7). The low-pass filtered *I/Q* product will approach zero if *I* and *Q* are exactly 90° out-of-phase.

$$LPF(I^{2} - Q^{2}) = LPF\left[\left\{\left(1 + \frac{\alpha}{2}\right)\cos\left(\omega t + \frac{\theta}{2}\right)\right\}^{2} - \left\{\left(1 - \frac{\alpha}{2}\right)\sin\left(\omega t - \frac{\theta}{2}\right)\right\}^{2}\right]$$
$$= LPF\left[\left(1 + \frac{\alpha}{2}\right)^{2}\frac{\left\{1 + \cos(2\omega t + \theta)\right\}}{2} - \left(1 - \frac{\alpha}{2}\right)^{2}\frac{\left\{1 - \cos(2\omega t - \theta)\right\}}{2}\right]$$
$$= \frac{\left(1 + \frac{\alpha}{2}\right)^{2}}{2} - \frac{\left(1 - \frac{\alpha}{2}\right)^{2}}{2}$$
$$= \alpha.$$
(3.6)

$$LPF(IQ) = LPF\left[\left\{\left(1 + \frac{\alpha}{2}\right)\cos\left(\omega t + \frac{\theta}{2}\right)\right\}\left\{\left(1 - \frac{\alpha}{2}\right)\sin\left((\omega t - \frac{\theta}{2})\right)\right\}\right]$$
$$= LPF\left\{\left(1 - \frac{\alpha^{2}}{4}\right)\frac{\sin(2\omega t) - \sin(\theta)}{2}\right\}$$
$$= -\theta \frac{\left(1 - \frac{\alpha^{2}}{4}\right)}{2}$$
$$\approx -\frac{\theta}{2}.$$
(3.7)

The above detection of  $\alpha$  and  $\theta$  is rather intuitive. The same conclusion can be drawn even by applying the signal decorrelation principle directly to (1.3) and (1.4). To decorrelate the signal from image, the image component in I+jQ is correlated with I-jQ. That is,  $(I+jQ)(I-jQ)^* = I^2-Q^2 + 2jIQ$ . This residual complex error averaged to

be  $\alpha$ -*j* $\theta$  gives the same results as derived in (3.6) and (3.7). This conclusion, drawn for the single-tone case, remains true for any amplitude-, frequency-, or phasemodulated signals. In this work, rather than estimating these gain and phase errors exactly as described above, only the signs of the errors are detected for the sign-sign LMS adaptation as discussed in section 3.4.

Recall from section 2.8 that the complex symmetric signal decorrelation technique, eight multiplications and eight additions are needed to estimate gain and phase errors, whereas the complex LMS adaptation can be simplified to use four multiplications and four additions. In the proposed sign-detection approach, however, only four sign detectors and two XNOR gates are needed as shown in Figure 3.6. Note that the sign of  $I^2-Q^2$  can be obtained by XNORing the signs of I+Q and I-Q, and similarly, the sign of IQ can be obtained from the signs of I and Q.



Figure 3.6: I/Q path gain and phase error detection.

The  $\alpha$  and  $\theta$  errors can be updated using two standard LMS-based sign-sign algorithms as in (3.8) and (3.9), where the estimated  $\alpha$  and  $\theta$  errors are written as  $\alpha'$ and  $\theta'$ . Thus, if the low-pass filtered sgn( $I^2-Q^2$ ) is positive,  $\alpha'$  is increased by  $\mu_{\alpha}$ . Similarly, if the low-pass filtered sgn(IQ) is positive, the parameter  $\theta'$  is decreased by  $\mu_{\theta}$ . These step sizes,  $\mu_{\alpha}$  and  $\mu_{\theta}$ , should be small enough to achieve high IRR, but not too small to slow down the adaptation process.

$$\alpha'[k+1] = \alpha'[k] + \mu_{\alpha} \operatorname{sgn}[LPF\{\operatorname{sgn}(I+Q) \cdot \operatorname{sgn}(I-Q)\}], \quad (3.8)$$

$$\theta'[k+1] = \theta'[k] - \mu_{\theta} \operatorname{sgn}[LPF\{\operatorname{sgn}(I) \cdot \operatorname{sgn}(Q)\}].$$
(3.9)

# **3.4** Comparison of Magnitude Detection and Sign Detection

The proposed error detection algorithm uses only the signs of *I*, *Q*, *I*+*Q* and *I*-*Q*, instead of their magnitudes. This allows a simple hardware implementation. However, using only the sign detection may be inferior to the magnitude detection in terms of error estimation accuracy. In magnitude detection, LPF {sgn(*I*-*Q*)sgn(*I*+*Q*)} in (3.8) becomes LPF { $(I^2-Q^2)$ }. Assuming that  $I^2-Q^2$  is Gaussian distributed with a mean of  $\alpha$  and a variance of  $\sigma^2$ , averaging *N* samples leads to

$$\frac{1}{N}\sum_{i=1}^{N}(S+\alpha),$$
(3.10)

where  $S \approx N(0, \sigma^2)$ . This average is a random variable with mean  $\alpha$  and variance  $\sigma^2/N$ . The update direction is correct with probability

$$P_{C} = 1 - Q\left(\frac{|\alpha|\sqrt{N}}{\sigma}\right), \qquad (3.11)$$

where  $Q(X) = \frac{1}{\sqrt{2\pi}} \int_{X}^{\infty} e^{-\frac{x^2}{2}} dx$ .

With sign detection, the average becomes

$$\frac{1}{N}\sum_{i=1}^{N}\operatorname{sgn}(S+\alpha).$$
(3.12)

Each term in the sum has a mean value of  $1-2Q(\alpha/\sigma)$ . Then the variance of (3.12) is

$$Var\left\{\frac{1}{N}\sum_{i=1}^{N}\operatorname{sgn}(S+\alpha)\right\} = \frac{1}{N}\left(E\left\{\operatorname{sgn}(S+\alpha)\right\}^{2} - \left[E\left\{\operatorname{sgn}(S+\alpha)\right\}\right]^{2}\right)$$
$$= \frac{1}{N}\left[1 - \left\{1 - 2Q\left(\frac{\alpha}{\sigma}\right)\right\}^{2}\right]$$
$$= \frac{1}{N}\left\{4Q\left(\frac{\alpha}{\sigma}\right) - 4Q^{2}\left(\frac{\alpha}{\sigma}\right)\right\}.$$
(3.13)

If the gain error  $\alpha$  is assumed to be small,  $Q(\alpha/\sigma)$  can be approximated as

$$0.5 - \frac{\alpha}{\sqrt{2\pi\sigma}}$$
. The mean and the variance are approximately  $\sqrt{\frac{2}{\pi}} \frac{\alpha}{\sigma}$  and  $\frac{1}{N}$ 

respectively. Similarly, the update direction is correct with probability

$$P_{C} = 1 - Q\left(\sqrt{\frac{2}{\pi}} \frac{|\alpha|\sqrt{N}}{\sigma}\right) \approx 1 - Q\left(0.8 \frac{|\alpha|\sqrt{N}}{\sigma}\right), \qquad (3.14)$$

which is slightly lower than that of the magnitude detection in (3.11). In other words, more samples should be accumulated for the same probability of obtaining the correct update direction with the sign detection. Using update equations with error magnitudes instead of the sign, other than achieving a more reliable direction of updates, has other benefits such as faster convergence and a smaller steady-state error. However, the advantage is not significant enough to justify the increased complexity over the proposed simple update algorithm using signs only.

### **3.5** Stability of Detection Algorithm

The directions of the gain and phase error updates from (3.8) and (3.9) are plotted in Figure 3.7. To better show the trajectory, the directions of  $LPF\{sgn(I+Q) \cdot sgn(I-Q)\}$  and  $LPF\{sgn(I) \cdot sgn(Q)\}$  are plotted instead of their signs. The figure shows that the solutions of  $\alpha$  and  $\theta$  converge to the correct values regardless of the initial values in the two-dimensional plane.



Figure 3.7: Direction of gain and phase error update.

To analyze the stability and convergence of the algorithm, let  $e_{\alpha}[k]$  and  $e_{\theta}[k]$ be the errors detected for  $\alpha$  and  $\theta$ , which are defined as the difference between the ideal value and the current estimate. The update terms in (3.8) and (3.9) are written using  $e_{\alpha}[k]$  and  $e_{\theta}[k]$ :

$$\alpha'[k+1] = \alpha'[k] + \mu_{\alpha} \operatorname{sgn}(e_{\alpha}[k]), \qquad (3.15)$$

$$\theta[k+1] = \theta[k] - \mu_{\theta} \operatorname{sgn}(-e_{\theta}[k]).$$
(3.16)

The newly detected errors,  $e_{\alpha}[k+1]$  and  $e_{\theta}[k+1]$ , can be written in a self-recursive form as follows.

$$e_{\alpha}[k+1] = \alpha - \alpha'[k+1] = e_{\alpha}[k] - \mu_{\alpha} \operatorname{sgn}(e_{\alpha}[k]), \qquad (3.17)$$

$$e_{\theta}[k+1] = \theta - \theta'[k+1] = e_{\theta}[k] - \mu_{\theta} \operatorname{sgn}(e_{\theta}[k]) .$$
(3.18)

The recursive function is shown in Figure 3.8. The detected error follows the dashed trajectory. The error will get smaller in the next update if the magnitude of the detected error is greater than  $\mu$ . Once the detected error e[k] falls within the error bound of  $\pm \mu$ , then e[k+2] = e[k]. Thus, the estimated gain and phase errors,  $\alpha'$  and  $\theta'$  will converge to the correct  $\alpha$  and  $\theta$  within  $\pm \mu$  irrespective of the initial condition.



Figure 3.8: Recursive function of the detection error.

The IRR is plotted as a function of  $\alpha$  and  $\theta$  in Figure 3.9. This threedimensional plot shows that the IRR is maximized if  $\alpha$  and  $\theta$  converge to the correct values. There is only one minimum error point, and there are no other local minima.



Figure 3.9: IRR versus gain and phase errors.

### 3.6 Acknowledgement

Chapter 3, in part, has been submitted for publication as it appears in IEEE Journal of Solid-State Circuits, Lerstaveesin, Supisa; Song, Bang-Sup, Dec, 2006. The dissertation author was the principle researcher and author of this paper.

## Chapter 4 Circuit Implementation

### **4.1 Three Possible Implemented Combinations**

The proposed image rejection algorithm consists of two major parts; the error correction and error detection models described in Chapter 3 provide the foundation upon which image rejection can be implemented. Figure 4.1 shows how to apply this proposed image rejection circuit in the zero-IF or low-IF down-conversion system. The error detector uses the I/Q outputs from the image rejecter to estimate the gain and phase errors, and these are fed back to the image rejecter to correct I/Q imbalance. The performance of the proposed method depends on how the signs of I, Q, I+Q, and I-Q are detected. ADCs of I/Q can be located in different places for three possible variations of the implementation. The ADCs can be placed before the image rejecter for a complete digital implementation. The other extreme is a complete analog implementation in which both image rejecter and error detector are implemented in the analog domain. In the hybrid form, the image rejecter is implemented as an analog block, but the error detector is implemented digitally. The ADCs, in this case, are

placed after the image rejecter but before the error detector. Image rejection is more accurate when performed with only complex signal and image without other blockers. Therefore, it is advisable to detect signs after I/Q channels are completely filtered.

Figure 4.1 also explains the complex I/Q spectra at different points of the receiver system. The proposed LMS-based feedback algorithm accumulates error at DC. As a result, the accuracy of the error detector is strongly affected by any signal and offset components at DC. For this reason, the proposed method requires that the DC component be notched out as marked. DC notching is not an issue in low-IF receivers. However, in zero-IF systems receiving RF signal with a fast-changing power envelope, DC calibration is a better solution than DC notching because of the well-known DC wandering problem.



Figure 4.1: Image rejection for low- or zero-IF receiver.


Figure 4.2: Digital image rejection system.

A digital implementation of the image rejection system is shown in Figure 4.2. This symmetric image rejecter uses four multipliers and two adders, and the gains of the multipliers are constantly updated by using the error detector. Note that an asymmetric image rejecter correcting the *I* or *Q* path only while keeping the other path constant is also possible using two multipliers and one adder. Two digital comparators detect the signs of *I*+*Q* and *I*-*Q*, and the signs of *I* and *Q* are determined by examining only the MSB sign bits. The products of these detected signs are fed into two 20-b up/down (U/D) counters working as low-pass filters. The update directions of  $\alpha$  and  $\theta$  are decided after accumulating signs for 2<sup>19</sup> cycles (The number of cycles is chosen for the reason explained in Section 4.2). This decision is used to increase or decrease

the values of  $\alpha$  and  $\theta$  stored in the 9-b U/D counters. The advantage of the digital approach is that the sign detection is very accurate due to its high oversampling ratio, and the mismatch between the two I/Q ADCs is corrected. The IRR is limited by the resolution of ADCs, and hence the system image rejection requirement for ADC resolution may be higher than the application requirement.



Figure 4.3: Hybrid image rejection system.

The hybrid implementation shown in Figure 4.3 is an alternative solution that is a compromise between the analog and the digital implementations. A sampled-data example of an analog image rejecter is a complex S/H with trim capacitors. This also serves as S/Hs for the following I/Q ADCs. The complex S/H should be linear, and its gain steps should be fine enough to achieve the desired IRR. Since the error detector is the same as in the digital case, this hybrid form has the advantages of the digital

implementation. The mismatch between the I/Q ADCs is also corrected. The performance of the hybrid system is limited by the analog trimming step size. Therefore, only the application requirement sets the resolution of the ADCs independently of the system image rejection requirement.



Figure 4.4: Analog image rejection system.

In the analog implementation shown in Figure 4.4 using analog comparators, the image rejecter is a complex S/H with trim capacitors, which is the same as in the hybrid system. The inputs of the error detector are the analog outputs of the S/H. These analog signals are latched using four comparators to get the signs of I, Q, I+Q, and I-Q. The rest of the error detector is the same as in the other two cases. Highresolution ADCs are not required as in the digital implementation. However, the disadvantage is that the system IRR is limited by analog imperfections such as the offsets of analog comparators and the mismatches between I/Q ADCs.

### 4.2 Step Size and Accumulation Period

This section explains how the step size and accumulation period are chosen. The error detection algorithm using sign only as discussed in Chapter 3 is simulated in MATLAB to determine the appropriate step size and accumulation period that give sufficiently accurate estimates of gain and phase errors for the required IRR.

High IRR requires small coefficient update step size  $(\mu)$ . For IRR of 70 dB, the coefficient update step size of  $2^{\cdot 12}$  is chosen. To implement  $LPF\{\text{sgn}(I) \cdot \text{sgn}(Q)\}$  and  $LPF\{\text{sgn}(I+Q) \cdot \text{sgn}(I-Q)\}$  in (3.9) and (3.10), the up-down counters are used as sinc low pass filters as discussed in section 4.1. The signs of terms sgn(I+Q)sgn(I-Q) and sgn(I)sgn(Q) are accumulated using up/down counters for a fixed period of time. This period must be long enough to obtain the correct signs of  $LPF\{\text{sgn}(I) \cdot \text{sgn}(Q)\}$  and  $LPF\{\text{sgn}(I+Q) \cdot \text{sgn}(I-Q)\}$  even when the smallest size of mismatch is present. Figure 4.5 shows  $\sum [\mu\{\text{sgn}(I) \cdot \text{sgn}(Q)\}]$  and  $\sum [\mu\{\text{sgn}(I+Q) \cdot \text{sgn}(I-Q)\}]$  of the 256-QAM signal with minimum gain error of 0.024% and minimum phase error of 0.014°. It is clear that the period of  $5 \times 10^5 \approx 2^{19}$  clock cycles is sufficiently long, and so the up-down counters of 20-bit counters are chosen.



Figure 4.5: Simulation of the accumulated correlation.

### 4.3 Complex Baseband S/H

A simplified schematic of a complex switched-capacitor S/H circuit used in hybrid and analog implementations is shown in Figure 4.6. It consists of two operational amplifiers, eight unit capacitors, and eight 9-b trim capacitors. Note that this figure does not show the switches needed for the operation of the switched capacitor circuit. This block samples the I/Q inputs differentially on the bottom plates of four input capacitors that are digitally trimmed. Negative capacitance values can be obtained by reversing the input polarity in the differential implementation. The S/H input capacitors are sized to be around 1 pF so that the signal to noise ratio (SNR) limited by kT/C noise can be higher than 72 dB as derived in (4.1).

$$SNR = 20 \log \left( \frac{V_{rms}}{\sqrt{\frac{kT}{C} \times 2}} \right) = 20 \log \left( \frac{\frac{0.5}{\sqrt{2}}}{\sqrt{\frac{4 \times 10^{-22}}{1 \times 10^{-12}} \times 2}} \right) = 79 dB > 72 dB.$$
(4.1)



Figure 4.6: Complex baseband S/H.

### 4.3.1 Bottom Plate S/H

The real differential bottom plate S/H with switches is shown in Figure 4.7. It is designed to operate at 40 MS/s. Even though gain error between two S/Hs can also be compensated by the image rejection algorithm, the input-dependent errors in S/H should be minimized. In addition, the DC offsets in the S/Hs due to device mismatches

in sampling switches and in Op-Amp reduce the accuracy of gain and phase error detection. Therefore, the fully differential bottom plate S/H [34] is chosen and sized to reduce input-dependent errors and DC offsets.



Figure 4.7: Real bottom plate S/H.

From Figure 4.7, with  $\phi 1$  and  $\phi 1 ps$  high, the input voltages *VINP* and *VINN* are tracked. When  $\phi 1 ps$  is low, *VINP* and *VINN* are held on capacitors  $C_H$  and charge injection from these switches is independent of the input voltage. This eliminates the effect of charge injection at the differential output. Then, when  $\phi 1$  is low, there is no charge injection from these switches since the two capacitors  $C_H$  are floating. Finally,  $\phi 2$  is high causing the output voltage to be as following.

$$VOUTP - VOUTN = \frac{C_H}{C} (VINP - VINN).$$
(4.2)

The phase clock generator and its timing diagram will be discussed in section 4.6.

#### **4.3.2 Operational Amplifier**

In this prototype, a telescopic gain-boosted operational amplifier is used so that the gain is set high enough to obtain better than 12-b linearity as shown in Figure 4.8. It is planned to drive external ADC and test equipment which have around 20pF load. For sampling rate of 40MS/s, 20pF load, and 12-b accuracy, the op-amp should have gain of higher than 72dB for linearity purpose, and the loop unity gain bandwidth should be higher than 106MHz as shown in (4.3) and (4.4), respectively.

$$A > 20\log(2^{N}) = 20\log(2^{12}) = 72dB.$$
(4.3)

$$\omega_{L,u} = \frac{1}{\tau} > \frac{\ln(2^N)}{t} \frac{1}{2\pi} = \frac{\ln(2^{12})}{2\pi \times 12.5 \times 10^{-9}} = 106 MHz.$$
(4.4)

Due to the process variation, the gain and bandwidth requirements should have some margins. In this prototype, the op-amp is designed to have DC gain of 86dB. For feedback factor of higher than 0.5, the open-loop unity gain bandwidth of 250MHz is designed. For testing, transistors M10-M12 are applied to cancel the offset due to device mismatches by manual tuning. The device sizes of telescopic gain-boosted amplifier are listed in Table 4.1.

The switched-capacitor common-mode feedback [35] shown in Figure 4.9 is applied to control the output common-mode voltage to be 0.9V. The capacitor C1 generates the average of the output voltage while the capacitor C2 determines the DC voltage across the capacitor C1.



Figure 4.8: Gain-boosted telescopic cascode operational amplifier.



Figure 4.9: Switch-capacitor common-mode feedback circuit.

Table 4.1: Device Chara	cteristics of Gain-	-Boosted Telesco	opic Amplifier.

Device	W/L ( $\mu$ m/ $\mu$ m)	I <sub>DC</sub> (mA)
M1	720/0.36	6
M2-M3	264/0.18	3
M4-M5	280/0.18	3
M6-M7	420/0.18	3
M8-M9	420/0.18	3
M10	24/0.36	0.2
M11-M12	12/0.18	0.1

The auxiliary amplifiers for N-side shown in Figure 4.10 and P-side shown in Figure 4.11 are designed using a folded cascode amplifier to enhance the gain. The transistor M2 in both N-side and P-side auxiliary amplifiers is used to replace common-mode feedback by controlling the bias current of the input pair. The device sizes of N-side auxiliary amplifier are listed in Table 4.2 and the device sizes of P-side auxiliary amplifier are listed in Table 4.3.



Figure 4.10: Auxiliary folded cascode amplifier for N-side.

|--|

Device	W/L (μm/μm)	I <sub>DC</sub> (mA)
M1	60/0.18	0.3
M2	14/0.18	0.1
M3-M4	14/0.18	0.1
M5-M6	8/0.18	0.2
M7-M8	4/0.18	0.1
M9-M10	20/0.18	0.1
M11-M12	20/0.18	0.1



Figure 4.11: Auxiliary folded cascode amplifier for P-side.

Device	W/L (μm/μm)	I <sub>DC</sub> (mA)
M1	72/0.18	0.6
M2	20/0.18	0.2
M3-M4	20/0.18	0.2
M5-M6	8/0.18	0.2
M7-M8	8/0.18	0.2
M9-M10	40/0.18	0.2
M11-M12	80/0.18	0.4

Table 4.3: Device Characteristics of P-side Auxiliary Amplifier.

### 4.3.3 Trim Capacitor



Figure 4.12: 9-bit trim capacitor.

The 9-b trim capacitor is made of a capacitor T-network with an array of 100fF unit capacitors as shown in Figure 4.12. Each trim capacitor covers a  $\pm 6.25\%$  range of  $\alpha$  with a 0.024% step and a  $\pm 3.5^{\circ}$  range of  $\theta$  with a 0.014° step. Since  $\alpha$  and  $\theta$  are initialized to the middle values of the ranges, a total of  $2^{19} \times 2^8$  cycles are needed to complete the worst-case initial adaptation assuming the step size is minimum. However, the initial adaptation time can be shortened if the standard gear-shifting algorithm is used.

## 4.4 Analog Comparator

The analog comparator used in the analog image rejection implementation is shown in Figure 4.13. Each comparator consists of two preamplifiers and a latch. The preamplifiers are implemented using a differential pair with diode-connected loads, and gain-enhanced using positive feedback as shown in Figure 4.14. The device characteristics of the preamplifier are presented in Table 4.4. The latch is simply a dynamic positive-feedback regenerator as shown in Figure 4.15 and its device sizes are provided in Table 4.5.



Figure 4.13: Analog comparator.



Figure 4.14: Preamplifier.

Device	W/L (μm/μm)	I <sub>DC</sub> (mA)
M1	96/0.36	2
M2-M3	24/0.18	1
M4-M5	8/0.18	0.4
M6-M7	12/0.18	0.6

Table 4.4: Device Characteristics of Preamplifier.



Figure 4.15: Latch.

Device	W/L (µm/µm)
M1	16/0.18
M2-M3	16/0.18
M4-M5	16/0.18
M6-M7	40/0.18
M8-M9	5/0.18

Table 4.5: Device Sizes of Latch.

From Figure 4.13, the two preamplifiers and the capacitors are switched for offset cancellation using the correlated double sampling principle [36]. The offset and feed-through errors of the first preamplifier are amplified, and sampled on the input capacitor of the second preamplifier stage, thereby reducing the first stage offset and feed-through errors. Offset and feed-through compensation is necessary since the input-referred offset of the comparator significantly affects the image rejection performance. The plot in Figure 4.16 shows a simulation that quantifies the degradation of the IRR with input-referred offset of the comparator. An offset as large as 1.5 mV for  $1-V_{pp}$  signal is acceptable for an IRR higher than 70dB.



Figure 4.16: Effect of comparator offset on IRR.

### 4.5 Synchronous Up/Down Counter

The 20-b up/down counters are applied to average the detected errors as a sinc filter while the 9-b up/down counters are used for storing the error values. The 20-b and 9-b synchronous up/down counters are implemented by combining the incrementer ripple chain in Figure 4.17(a) and the decrementer ripple chain in Figure 4.17(b) to be the up/down counter as shown in Figure 4.17(c). For *N*-bit block, the delay through the ripple chain will be *N* times the unit logic delay. For simplicity, these up/down counters do not use the prescaler technique [37], thus the carry/borrow chain is the critical path. Therefore, the carry/borrow propagation delay has to be less than the period of digital clock. For 20-b up/down counter running at 40MHz, the logic gates are designed to have propagation delay less than 1.25ns.







(b)



Figure 4.17: N+1 bit synchronous counter with ripple chain.(a) Up counter. (b) Down counter. (c) Up/down counter.

## 4.6 Phase Clock Generator



Figure 4.18: Phase clock generator.

The phase clocks are generated using the circuit shown in Figure 4.18 to ensure that two phase clocks will not overlap each other. The inverter delay lines are applied to make phase clocks  $\phi lps$  and  $\phi 2ps$  come prior to  $\phi 1$  and  $\phi 2$ , respectively, and to be a buffer to drive switches. Therefore these inverters are sized to be large enough to drive the transistor switches. The  $\phi 2pps$  clock is designed to be high at the same time as  $\phi 2ps$  but to be low before  $\phi 2ps$ . The timing diagram of these phase clocks is shown in Figure 4.19.



Figure 4.19: Phase clock timing diagram.

## 4.7 Acknowledgement

Chapter 4, in part, has been submitted for publication as it appears in IEEE Journal of Solid-State Circuits, Lerstaveesin, Supisa; Song, Bang-Sup, Dec, 2006. The dissertation author was the principle researcher and author of this paper.

## Chapter 5 Experimental Results

## 5.1 Prototype IC Layout

The prototype image rejection chip is fabricated in 0.18- $\mu$ m CMOS technology. It occupies an area of 800 x 600  $\mu$ m<sup>2</sup> as shown in Figure 5.1. The complex S/H with trim capacitors occupies half of the die. The other half contains analog comparators, clock generator, and digital sign detectors. Note that the analog comparators are used only for the analog implementation. These four analog comparators with offset-cancelled preamplifiers used for the analog sign detector occupy an area of 800 x 150  $\mu$ m<sup>2</sup>. Therefore, the hybrid implementation occupies an area of 800 x 450  $\mu$ m<sup>2</sup>.



Figure 5.1: Die photo.

## 5.2 Test Setup

Since multi-constellation digital receivers are more sensitive to image, 64 and 256 constellation quadrature amplitude modulation (64-QAM and 256-QAM) are chosen for testing. I/Q signals of 1 V<sub>pp</sub> are generated from computer and fed to the I/Q modulation generator R&S AMIQ [38] which works as D/A converter. The I/Q signals has 1-MHz IF and 800-kHz symbol rate. Constant 5% gain and 3° phase errors are injected into the signal to emulate I/Q path mismatch. The test signal from R&S AMIQ is fed to image rejection circuit at 40 MS/s. For analog implementation, the

analog error detector also runs at 40 MS/s. However, for hybrid implementation, due to the limitation in sampling rate of two external 15-b  $\Delta\Sigma$  ADCs, TI ADS1605 [39], the image rejecter output is digitized at 5 MS/s, and hence the digital error detector must also run at 5 MS/s. The digitized image rejected signal is stored in logic analyzer, Agilent 1670G, and transferred to computer to plot the complex signal spectrum, and also demodulated to plot constellation and eye diagram using MATLAB. For digital implementation, the image rejecter and error detector are implemented in software, which takes the digitized signal from R&S AMIQ as input. Note that the complex image blocker used for testing is from the complex signal itself, so the complex image has the same power level as the complex signal. Therefore, all the IRRs quoted in this work are relative to the signal level. The test setup diagram is shown in Figure 5.2.



Figure 5.2: Test setup diagram.

### 5.3 Complex Baseband Spectrums

The measured complex 256-QAM spectra for all three cases are shown in Figures 5.3-5.6. With a gain mismatch of 5% and phase mismatch of 3°, the IRR before image rejection is about 26dB. The IRR is improved to about 65dB in the digital implementation using 12-b ADCs. For the hybrid case, the IRR is also about 65dB. The analog case, however, exhibits a lower IRR of 62dB mainly due to the offsets of analog comparators.



Figure 5.3: Complex 256-QAM spectra before image rejection.



Figure 5.4: Complex 256-QAM spectra after 12-b digital image rejection.



After hybrid Image rejection

Figure 5.5: Complex 256-QAM spectra after hybrid image rejection.



Figure 5.6: Complex 256-QAM spectra after analog image rejection.

Figures 5.4 and 5.7–5.9 show the effect of ADC resolution on IRR for 256-QAM signal in the digital image rejection. With 15-b ADCs in the digital implementation, the image is suppressed well below the noise level of the test set-up. As discussed above, IRR of 12-b ADCs digital image rejection is around 65dB. And as expected, IRRs of only 60dB and 50dB are observed with 10-b and 8-b ADCs.



Figure 5.7: Complex 256-QAM spectra after 15-b digital image rejection.



Figure 5.8: Complex 256-QAM spectra after 10-b digital image rejection.



Figure 5.9: Complex 256-QAM spectra after 8-b digital image rejection.

So far, since the R&S AMIQ output is limited to one channel, it is inherently assumed that the signal is down-converted to DC and thus the source of image is the leakage of desired signal. However, the spectra are plotted as if the signal is down-converted to low IF to make the image spectrum visible and not overlapped with the signal spectrum. (See the shaded spectrum in Figure 2.23.) In the scenario when the signal is down-converted to low IF, the source of image is the adjacent channel blocker. This is indeed the case in Figure 2.23 where the white spectrum image overlaps with the shaded signal. To test this case, the I/Q signals are generated from MATLAB. It is shown in Figures 5.10 and 5.11 that even when the blocker is 20dB stronger than the desired signal, the digital image rejecter suppresses the image all the way down to the quantization noise level. As long as the blocker stays within the ADC range, its image is rejected.



Figure 5.10: Signal and blocker spectra before image rejection.



Figure 5.11: Signal and blocker spectra after 15-b digital image rejection.

### **5.4** Constellations and Eye Diagrams

The *I/Q* of single channel 64-QAM and 256-QAM signals before and after image rejection are demodulated and then their constellations and eye diagrams are plotted. Figures 5.12 and 5.13 show the measured constellations, before and after image rejection, of 64-QAM and 256-QAM, respectively. The constellation is significantly dislocated due to self image with an IRR of 26dB before image rejection. It can be seen that the constellation goes back to the ideal location after image rejection with 65dB IRR. The measured eye diagrams of the 64-QAM and 256-QAM signals are shown in Figures 5.14 and 5.15. It is clear that the eyes are almost closed before image rejection but they open up completely after image rejection especially in 256-QAM case. Image also affects the error probability of the received data and it is more severe in the 256-QAM system than the 64-QAM system as discussed in the next section. Table 5.1 summarizes the measured performance of the propose image rejection circuit.



Figure 5.12: Measured 64-QAM constellation before and after image rejection.



### After, IRR=65dB



Figure 5.13: Measured 256-QAM constellation before and after image rejection.



Figure 5.14: Measured 64-QAM eye before and after image rejection.



Figure 5.15: Measured 256-QAM eye before and after image rejection.

Parameter	Measurement Results		
Implementation	12b Digital	Hybrid	Analog
Technology	0.18µm CMOS		
Correction Rate	5MS/s	40MS/s	40MS/s
Detection Rate	5MS/s	5MS/s	40MS/s
IRR	65dB	65dB	62dB
Input/Load Capacitances	-	1pF / 20pF	1pF / 20pF
$\Delta C/C$ Correction Range	$\pm 2^{-4} (\pm 6.25\% / \pm 3.5^{\circ})$		
ΔC/C Minimum Step	2 <sup>-12</sup> (0.0244% / 0.014°)		
Averaging Cycles for Update	2 <sup>19</sup> Cycles		
Worst Case Initial Adaptation	$2^{19} \times 2^8$ Cycles		
Chip Area	-	$800 \times 450 \ \mu m^2$	$800 \times 600 \ \mu m^2$
Power @ 1.8V	-	23mW	37mW

Table 5.1: Summary of Measured Performance.

# 5.5 Effect of I/Q Imbalance on Probability of Error

The probability of error of 64-QAM and 256-QAM systems are estimated from simulation for 4 sets of gain and phase mismatches which generate IRR of 30dB, 40dB, 50dB and 60dB. The plots of probability of error versus SNR of 64-QAM and 256-QAM are shown in Figures 5.16 and 5.17, respectively. In addition, the plots of probability of error versus IRR for 64-QAM and 256-QAM are also shown in Figures 5.18 and 5.19, respectively. It is observed that the I/Q imbalance degrades the bit error

rate (BER) performance of the system. It also shows that the 256-QAM case is more sensitive to image than the 64-QAM case. Furthermore, the performance degradation becomes more severe when SNR increases. It is less sensitive when SNR is low due to the fact that the received noise dominates the system performance. With an IRR > 60 dB, the error probability converges to the ideal value but the error probability increases very rapidly when IRR is less than 60 dB.



Figure 5.16: Probability of error versus SNR of 64-QAM system.



Figure 5.17: Probability of error versus SNR of 256-QAM system.



Figure 5.18: Probability of error versus IRR of 64-QAM system.



Figure 5.19: Probability of error versus IRR of 256-QAM system.

## 5.6 Acknowledgement

Chapter 5, in part, has been submitted for publication as it appears in IEEE Journal of Solid-State Circuits, Lerstaveesin, Supisa; Song, Bang-Sup, Dec, 2006. The dissertation author was the principle researcher and author of this paper.
## Chapter 6 Conclusion

The gain and phase errors of the I/Q signals give rise to the image problem, in which the down-converted desired signal is corrupted by an image from the signal leakage or the adjacent channel. This image problem is one of the major obstacles in the implementation of direct-conversion zero-IF or low-IF receivers. The proposed image rejection algorithm can detect and correct I/Q imbalance continuously. It is based on an adaptive zero-forcing feedback concept using sign bits only, and therefore does not require complicated digital processing. The total accumulated image component at the system level is rejected in the complex baseband domain regardless of the source. It is demonstrated that the image rejecter and error detector can be implemented either in the analog or the digital domain. The hybrid implementation with a complex S/H and digital sign detectors alleviates the need for a high resolution ADC in the digital image rejecter, while maintaining the same performance. The proposed image rejection algorithm allows simple zero-IF or low-IF receiver implementation since no accurate analog circuits are necessary for complex I/Qprocessing. The image rejection can be implemented on chip and requires no off-chip

components. Moreover, it contains on-line adaptation and requires no test tone. Any down-conversion receiver should benefit from its low cost, low power, and image rejection performance.

There are several possibilities for improvement in future research. One drawback of the proposed image rejection algorithm is the long initial convergence time since the accumulation period is fixed to be long enough to detect the minimum gain and phase errors of 0.0244% and 0.014°. An algorithm to reduce the initial time by automatically adjusting the accumulation period or the step size in error detector such as gear shifter is advantageous. In addition, the main obstacle to achieve high IRR is the system DC offset, since the detection algorithm accumulates errors at DC. Therefore the system DC offset calibration is helpful to improve the proposed image rejection algorithm.

## **Bibliography**

[1] A. A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399-1410, Dec. 1995.

[2] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873-887, Jun. 2001.

[3] S. Jantzi, K. Martin, and A. Sedra, "Quadrature Bandpass  $\Delta\Sigma$  Modulation for Digital Radio," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1935-1950, Dec.1997.

[4] J. Crols and M. Steyaert, "An Analog Integrated Polyphase Filter for a High Performance Low-IF Receiver," *VLSI Dig. Tech. Papers*, pp. 848-854, Jun. 1995.

[5] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900MHz CMOS LC-Oscillator with Quadrature Outputs," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 392-393, Feb. 1996.

[6] B. Razavi, <u>RF Microelectronics</u>, Prentice Hall, 1998.

[7] S. Lerstaveesin and B. Song, "A Complex Image Rejection Circuit with Sign Detection Only," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 454-455, Feb., 2006.

[8] R. Hartley, "Modulation System," U.S. Patent 1 666 206, Apr. 1928.

[9] S. Haykin, Communication Systems, John Wiley & Sons, 2001.

[10] D.K. Weaver, "A Third Method of Generation and Detection of Single Side Band Signals," *Proc. IRE*, pp. 1703-1705, Dec. 1956.

[11] P. Gudem and L. Larson, "Transceiver Architectures," lecture given in course ECE265A: Communication Circuit Design I, University of California, San Diego, 2003.

[12] P. Gudem, "Analog Filter Design," lecture given in course ECE283: Special Topics in Electronic Circuits and Systems, University of California, San Diego, 2004.

[13] I. Bouras et al, "A Digitally Calibrated 5.15-8.825 GHz Transceiver for 802.11a Wireless LANs in 0.18µm CMOS," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp 352-498, Feb. 2003.

[14] M. Dawkins, A. Burdett, and N. Cowley, "A Single-Chip Tuner for DVB-T," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1307-1317, Aug. 2003.

[15] L. Der and B. Razavi, "A 2GHz CMOS Image-Reject Receiver with LMS Calibration," *IEEE J. Solid-State Circuits*, vol. 38, pp. 167-175, Feb. 2003.

[16] M. Elmala and S. Embabi, "Calibration of Phase and Gain Mismatches in Weaver Image-Reject Receiver," *IEEE J. Solid-State Circuits*, vol. 39, pp. 283-289, Feb. 2004.

[17] F.E. Churchill, G.W. Ogar, and B.J. Thompson, "The Correction of I and Q Errors in a Coherent Processor," *IEEE Trans. Aerosp. Electron. Syst.*, Vol. 17, 131-136, Jan. 1981.

[18] K. Pun, J. Franca, and C. Azeredo-Leme, "A Digital Method for the Correction of *I/Q* Phase Errors in Complex Sub-Sampling Mixers," *Proc. 2000 Southwest Symp. on Mixed-Signal Design*, pp. 171-174, Feb. 2000.

[19] A. Lohtia, P. A. Goud, and C. G. Englefield, "An Adaptive Digital Technique for Compensating for Analog Quadrature Modulator/Demodulator Impairments," *Proc. IEEE Pac. Rim Conf.* vol. 2, pp. 447-450, May 1993.

[20] Z. Wang, "A Random Wave Method for Detecting Phase Imbalance in a Coherent Radar Receiver," *IEEE J. Atmos. Oceanic Tech.*, vol. 10, pp.887-891, Dec. 1993.

[21] M. D. Kulkarni, A. B. Kostinski, "A Simple Formula for Monitoring Quadrature Phase Error with Arbitrary Signals", *IEEE Trans. Geosciences and remote sensing*, Vol.33, no.3, pp. 799-802, May 1995.

[22] G. Yang, G. Vos, and H. Cho, "*I/Q* Modulator Image Rejection through Modulation Pre-distortion," *IEEE Veh. Tech. Conf.*, pp. 1317-1320, May 1996.

[23] J. Glas, "Digital *I/Q* Imbalance Compensation in a Low-IF Receiver," *Global Telecom. Conf.*, pp. 1461-1466, Nov. 1998.

[24] E. Coersmeier, E. Zielinski, and K. Wachsmann, "Software IQ Sample Estimation for Multi-Antenna Systems," *Proc. Radio and Wireless Conf.*, pp. 175-178, Aug. 2003.

[25] I. Vassiliou et al, "A Single-Chip Digitally Calibrated 5.15-5.825 GHz 0.18μm CMOS Transceiver for 802.11a Wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2221-2231, Dec. 2003.

[26] L. Yu and W.M. Snelgrove, "A Novel Adaptive Mismatch Cancellation System for Quadrature IF Radio Receivers," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 789-801, Jun. 1999.

[27] E. Cetin, I. Kate, and R. C. S. Morling, "Adaptive Compensation of Analog Front-End *I/Q* Mismatches in Digital Receivers," *Proc. ISCAS*, vol. 4, pp. 370-373, 2001.

[28] C. Chen and C. Huang, "On the Architecture and Performance of a Hybrid Image Rejection Receiver," *IEEE J. Selected Comm.*, vol. 19, pp. 1029-1040, Jun. 2001.

[29] C. Heng, M. Gupta, S. Lee, D. Kang, and B. Song, "A CMOS TV Tuner/Demodulator IC with Digital Image Rejection," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2525-2535, Dec. 2005.

[30] I. Elahi, K. Muhammad, and P. Balsara, "*I/Q* Mismatch Compensation using Adaptive Decorrelation in a Low-IF Receiver in 90-nm CMOS Process," *IEEE J. Solid-State Circuits*, vol. 41, pp. 395-404, Feb. 2006.

[31] B. Widrow *et al.*, "Adaptive Noise Cancelling: Principles and Applications," *Proc. IEEE*, vol. 63, pp. 1692-1716, Dec. 1975.

[32] S. van Gervan and D. van Compernolle, "Signal Separation by Symmetric Adaptive Decorrelation: Stability, Convergence, and Uniqueness," *IEEE Trans. Signal Process.*, vol. 43 no. 7, pp. 1602-1612, Jul. 1995.

[33] S. Haykin, <u>Adaptive Filter Theory</u>, Prentice Hall, 1996.

[34] Y. Lin, B. Kim, and P.R. Gray, "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 26, pp. 628-636, Apr. 1991.

[35] D. Johns and K. Martin, <u>Analog Integrate Circuit Design</u>, John Wiley & Sons, 1997.

[36] R. Poujois and J. Borel, "A Low Drift Fully Integrated MOSFET Operational Amplifier," *IEEE J. Solid-State Circuits*, vol. 13, pp. 499-503, Aug. 1978.

[37] M. R. Stan, "Synchronous Up/Down Counter with Clock Period Independent of Counter Size," *Proc. 1997 IEEE Symp. Computer Arithmetic*, pp. 274-281, Jul. 1997.

[38] AMIQ-B2 Manual, Rohde-Schwarz, Germany.

[39] ADS1605/1605 EMV User's Guide, Texas Instrument, Texas.