Design of CMOS Ternary Latches

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***Abstract*—This paper describes the design methodology of latches with three stable operating points. Open-loop analysis is used to obtain insight into how a conventional binary latch structure can be modified to yield a ternary latch. Four novel ternary latch structures, compatible with a standard CMOS process, are presented. Properties of each latch, including robustness of the ternary behavior, speed, and power dissipation, are described. Measurement results of four RS ternary flip-flops based on the proposed latch structures, fabricated in a standard 0.18-μm CMOS process, are presented. Maximum operating frequency and skew tolerance are reported for each of the four latches.**

***Index Terms*—CMOS digital integrated circuits, CMOS memory circuits, digital integrated circuits, integrated logic circuits, multivalued logic circuits.**

I. Introduction

CONVENTIONAL latch circuits, widely used in sequential logic and memory, are able to take either of two possible stable states. In fact, such circuits possess three operating points, two stable and one unstable (sometimes referred to as "metastable"). An early theoretical study claimed any circuit containing two bipolar transistors, independent sources and resistors can possess no more than three operating points [1]. However, recently it was reported for CMOS circuits [2] and later for bipolar junction transistor (BJT) circuits [3] that a certain assumption used in [1] is not necessarily true. In [2] and [3] two-transistor latch circuits possessing five operating points, three out of which are stable, were presented.

Ternary logic circuits, which allow three logic levels instead of two, have been studied for a number of years [4]. Although design of circuits implementing combinational ternary logic is straightforward, the design of a simple and robust ternary memory element (i.e., latch) suitable for integrated circuit (IC) implementation has been challenging. For example, a rather complex CMOS circuit proposed in [5] requires multiple supplies in order to reduce static power dissipation; in [6] a ternary latch is proposed that creates the ternary output by switching in reference voltages in a latch structure; in [7] a resonant tunneling diode (RTD) is employed to obtain multilevel logic; in [8] MOS circuits are used to emulated the behavior of RTDs in order to realize multiple-valued logic; in [9] ternary memory is realized by a dynamic circuit that requires a sophisticated timing scheme. In this paper, a new type of ternary latch, based on a simple topology compatible with a standard CMOS fabrication process and powered by a single supply voltage, is presented.

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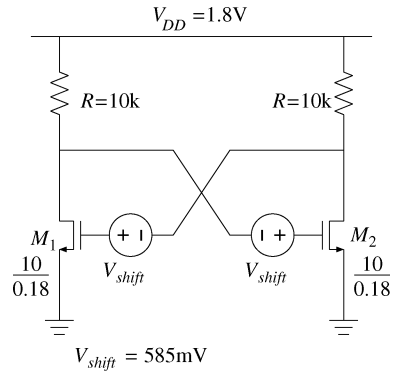

Fig. 1. Tristable latch with two n-channel MOSFETs.

This paper is organized as follows. Section II presents theoretical background, analysis and design methodology for a novel ternary latch. Section III describes four variations of a new ternary latch that possess three stable operating points. Section IV provides preliminary experiment results. Section V offers conclusions.

II. Theoretical Background

In this section, we briefly review some recent theoretical findings about latch circuits and then present new design methodology to construct two-transistor tri-stable circuits.

In [10], it was shown that the simple nMOS latch circuit shown in Fig. 1 can be made to possess five operating points, three of which are stable. The existence of five operating points is made possible by the presence of floating voltage sources $V_{\rm shift}$. These voltage sources function to bias the symmetric operating point (i.e., the operating point where both transistors are biased identically) of the circuit such that the transistors are biased not in the saturation region, which would be the case for a bistable latch, but instead in the triode region.

To understand how this simple circuit could possess five operating points, we perform an open-loop analysis using the circuit shown in Fig. 2. The voltage transfer characteristic $V_{\rm out}$ versus $V_{\rm in}$ is shown in Fig. 3(a). The simulation results presented here and throughout this paper use BSIM3 transistor models provided by the Jazz Semiconductor CA18 0.18-μm CMOS process.

From the close-up view of the graph of $V_{\rm out}-V_{\rm in}$ versus $V_{\rm in}$ shown in Fig. 3(b), it can be observed that the circuit possesses five operating points since $V_{\rm out}-V_{\rm in}$ crosses zero five times. To determine the stability of these operating points, we observe the small-signal open-loop gain $dV_{\rm out}/dV_{\rm in}$ versus $V_{\rm in}$ curve shown in Fig. 3(c). From criteria given in [11] and [12], it is straightforward to conclude operating points OP2 and OP4 are

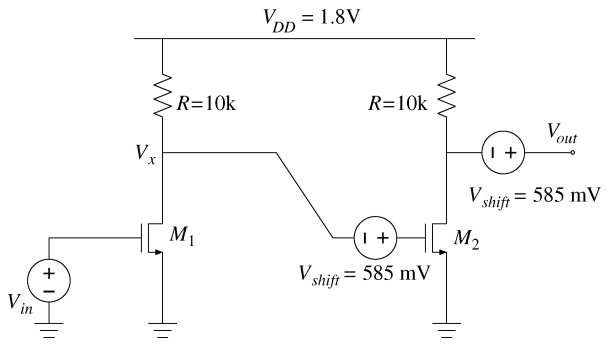

Fig. 2. Circuit used for open-loop analysis of the Fig. 1 latch.

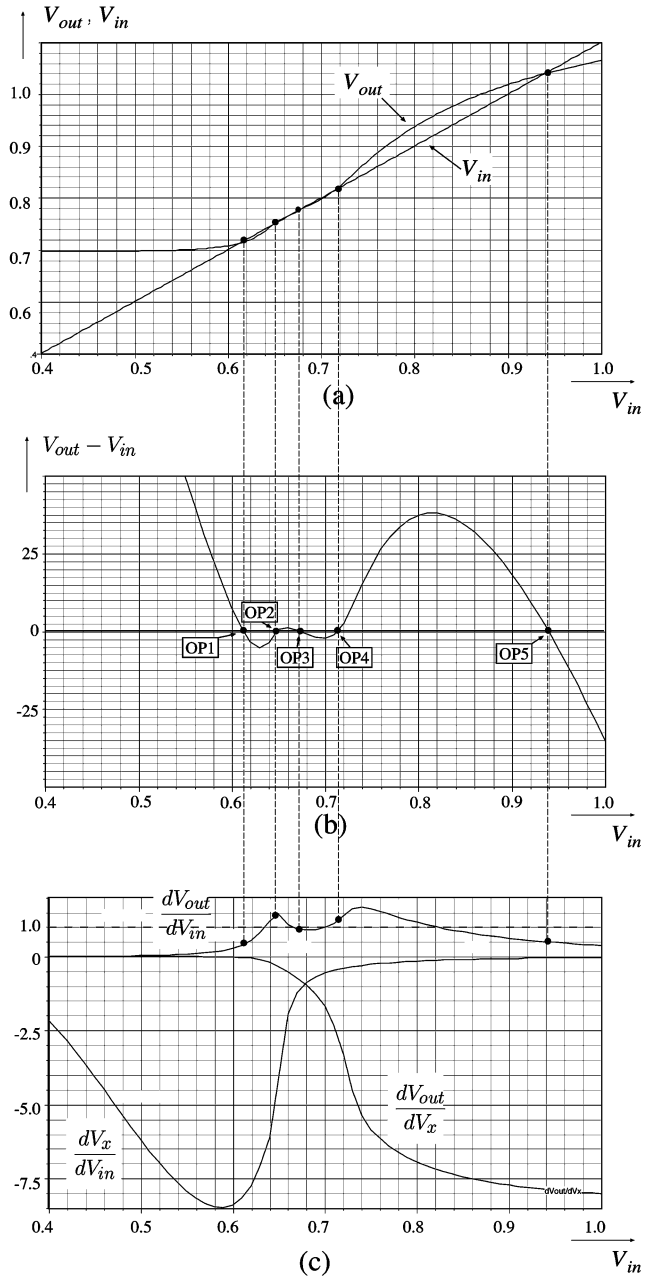

Fig. 3. Open-loop curves corresponding to the Fig. 2 circuit. (a) Voltage transfer characteristic $V_{\rm out}$ versus $V_{\rm in}$. (b) $V_{\rm out} - V_{\rm in}$ versus $V_{\rm in}$. (c) Gain curves.

unstable. Stable operating points OP1 and OP5 correspond to the usual binary state of latches when one of the cross-coupled transistors is off and the other one is in triode. OP3 corresponds to both transistors identically biased in triode. Since the small-signal loop gain is less than unity at this operating point, it is stable as well.

To obtain greater insight into how five operating points can exist, we can write the small-signal loop gain T corresponding to the Fig. 2 circuit as

$$T = \frac{dV_{\rm out}}{dV_{\rm in}} = \frac{dV_x}{dV_{\rm in}} \cdot \frac{dV_{\rm out}}{dV_x}. \tag{1}$$

From observing Fig. 3(c), we can see that there exist two distinct relative maxima with magnitudes greater than unity in the T versus $V_{\rm in}$ plot. It is the presence of these peaks that allows the two unstable operating points OP2 and OP4 to exist.

We now explore how the proper choice of circuit parameters of the Fig. 1 circuit can determine the number of operating points. We can make two general observations:

1) The resistor value R will primarily influence the gains $dV_x/dV_{\rm in}$, $dV_{\rm out}/dV_x$, and T. It is thus necessary to make R sufficiently large such that T can exhibit peak values above unity.
2) The voltage source $V_{\rm shift}$ will influence the separation of the rapidly increasing portion of $dV_x/dV_{\rm in}$ and the rapidly decreasing portion of $dV_{\rm out}/dV_x$. This separation will in turn affect the peaks of T. It is necessary to have T higher than unity at the peaks and a region with gain less than unity between them.

For example, let us consider the behavior of the Fig. 1 circuit with $R = 220$ and $V_{\rm shift} = 0$. As shown in Fig. 4(a), the loop gain T always remains below unity due to the small gain in each stage. Hence, this latch can possess only one operating point. When R is increased to 10 k and $V_{\rm shift}$ remains at 0, T has a single peak with magnitude greater than 70 as shown in Fig. 4(b) because the relative minima in $dV_x/dV_{\rm in}$ and $dV_{\rm out}/dV_x$ are located very close together. Hence, this latch can possess at most three operating points. By increasing $V_{\rm shift}$ to 585 mV, we are able to separate the increasing portion of $dV_x/dV_{\rm in}$ and the decreasing portion of $dV_{\rm out}/dV_x$ in order to create two peaks above unity in T (with a region below unity in between them) as is shown in Fig. 3(c). In this case, it is observed that $dV_{\rm out}/dV_x$ flattens as $V_{\rm in}$ approaches 1.8 V while $dV_x/dV_{\rm in}$ is close to zero. This is because when transistor M_1 enters the triode region and V_x is close to zero, appropriate selection of $V_{\rm shift}$ can still allow transistor M_2 to be biased in the saturation region. Thus, the loop gain can be made greater than unity even while M_1 is biased in triode. However, a further increase in $V_{\rm shift}$ would lead to the decrease in the peaks of T to below unity as shown in Fig. 4(c), resulting in only one operating point. (In the next section, we will present more robust realizations of the ternary latch.)

From the above analysis, clearly the value of $V_{\rm shift}$ is critical in determining whether or not the latch can exhibit three stable operating points. If $V_{\rm shift}$ is too small, then the transistors will not be able to enter the triode region near the symmetric operating point; if $V_{\rm shift}$ is too large, then the loop gain will not be sufficient to give rise to more than one operating point. Thus, there is a specific range of $V_{\rm shift}$ for which three stable operating points exist.

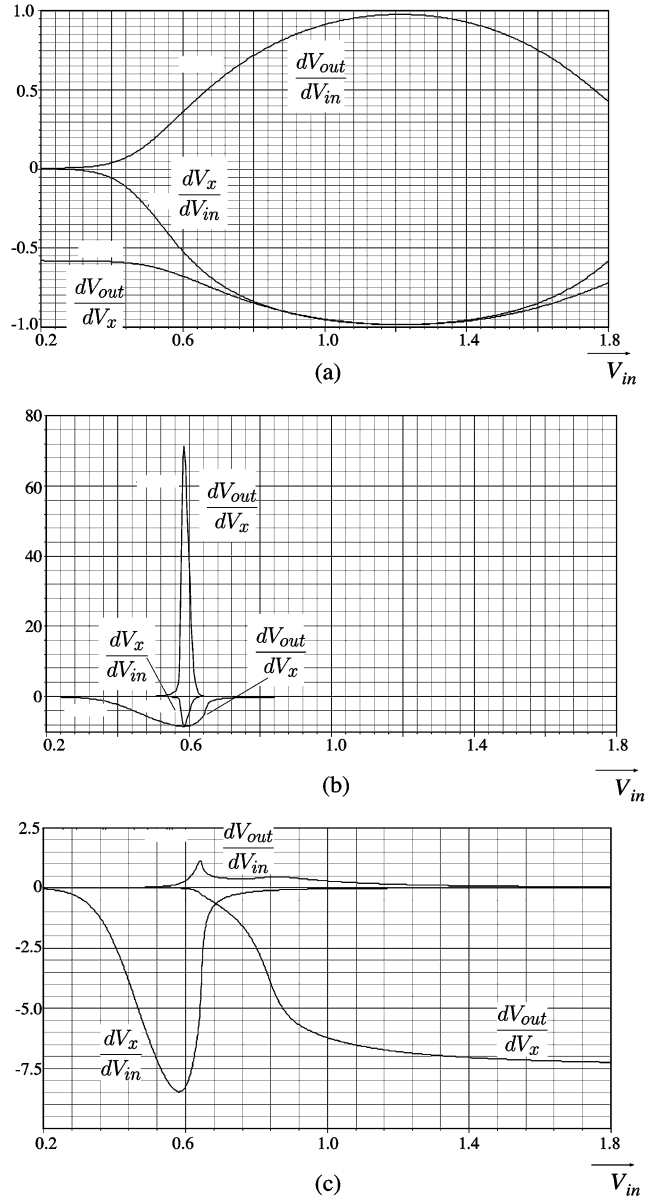

Fig. 4. Gain curves for: (a) $R = 220, V_{\rm shift} = 0$; (b) $R = 10$ k, $V_{\rm shift} = 0$; (c) $R = 10$ k, $V_{\rm shift} = 600$ mV.

To verify stability of the operating points possessed by the Fig. 1 circuit, the dynamic response corresponding to various initial conditions was simulated. In this way, we numerically confirm that the circuit does indeed possess three stable operating points. The transistor gate-to-source voltages $V_{\rm gs1}$ and $V_{\rm gs2}$ are taken as state variables assuming capacitors $C_{\rm gs1}$ and $C_{\rm gs2}$ dominate the circuit's dynamic behavior. The transient waveforms in Fig. 5(a) clearly show the three stable operating points; Fig. 5(b) displays the regions of attraction for each of them. For any initial condition within one of the regions, the system finally converges to the corresponding operating point. Thus, the Fig. 1 circuit is indeed "tristable."

III. Design of Single-Supply CMOS Tristable Latch Circuits

In this section, we will discuss practical realization of tristable latches that is compatible with a standard CMOS process. Despite its simple structure, the Fig. 1 circuit has two disadvantages for IC implementation. First, the floating voltage sources cannot be realized on chip. Second, the circuit's tristable operation is not robust since this property is exhibited only for a small range of circuit parameters.

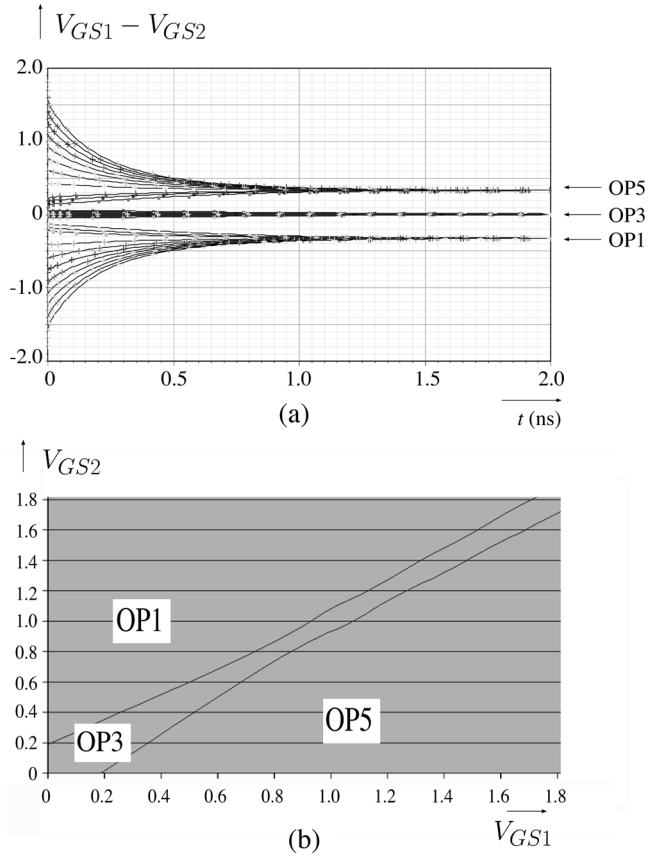

Fig. 5. Dynamics of tristable latch. (a) Transient response for various initial conditions. (b) Basins of attraction for the three stable operating points.

Four novel tristable latches compatible with a CMOS process, first presented in [13], are shown in Fig. 6. The Fig. 6(a) circuit is biased so that the voltage drop across each resistor is equal to $V_{\rm ref}$ at the symmetric operating point OP3. Hence, the voltage source $V_{\rm shift}$ in the Fig. 1 circuit is realized in the Fig. 6(a) circuit by the IR drop in each resistor. As mentioned in Section II, this voltage drop must be within a specified range in order for tristable behavior to exist. Thus, for a given set of transistor sizes, the resistor values must be within a certain range.

The biasing of the Fig. 6(b) circuit is designed in a similar way, but in this case the voltage drop is across diode-connected transistors M_{3A} and M_{3B}. The biasing circuit comprised of the op-amp, M_{2C} and R_{1C} (or M_{3C}) can be shared by many latches.

Fig. 7(a) and (b) shows the small-signal open-loop gains corresponding to the Fig. 6(a) and (b) circuits, respectively. (The three curves are defined in the same way as those in Fig. 4.) It is observed that the Fig. 6(a) circuit has sufficient gain such that transistor M_{1A} quickly enters the triode region for $V_{\rm in} > 0.8$ V. This is due to the relatively large small-signal resistance, consisting of the series connection of R_{1A} and r_{ds2A}, connected between the drain of M_{1A} and $V_{\rm DD}$. In order to generate two peaks in T, the resistor voltage drop must be precisely set by

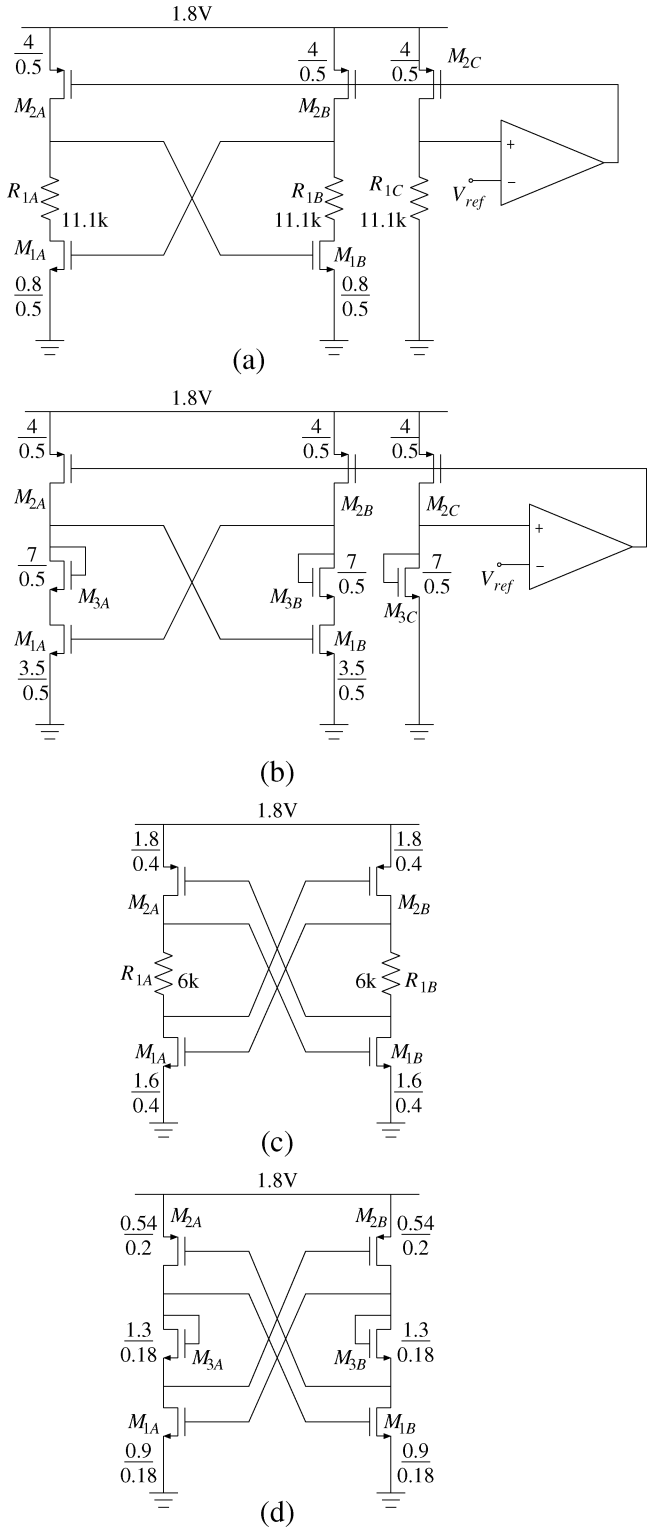

Fig. 6. Four variations of a CMOS tristable latch.

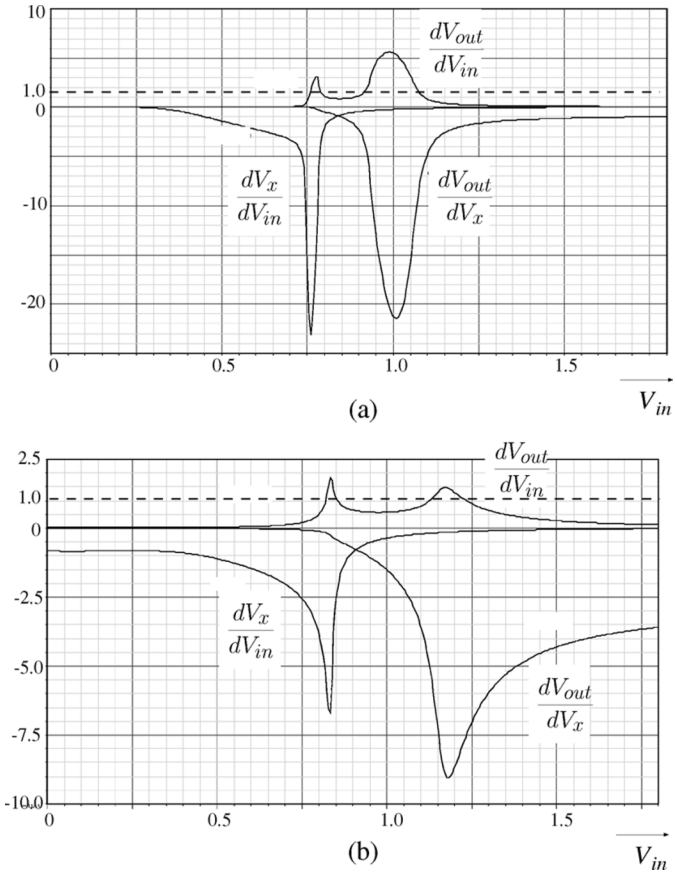

Fig. 7. Loop gain. (a) Fig. 6(a) circuit. (b) Fig. 6(b) circuit.

the bias circuit. Similarly, the second stage gain $dV_{\rm out}/dV_x$ also has high peak and narrow width. Simulations show that five operating points exists for Fig. 6(a) circuit only when $V_{\rm ref}$ is between 0.5 V and 0.65 V. However, the Fig. 6(b) circuit is more robust due to the nonlinear nature of the diode-connected transistors M_{3A} and M_{3B}. In particular, an appropriate dc voltage drop can be achieved between the drain and the source of M_{3A} while keeping its small-signal resistance r_{ds3A} smaller than the value of R_{1A} in Fig. 6(a). Thus, the small-signal resistance between the drain of M_{1A} and $V_{\rm DD}$, consisting of the series connection of r_{ds3A} and r_{ds2A}, is smaller. As a result, the Fig. 7(b) graphs exhibit a more gradual change than those of Fig. 7(a). The overall circuit exhibits tristable behavior for $V_{\rm shift}$ between 0.3 to 0.7 V, a significant improvement over the Fig. 6(a) range.

The Fig. 6(c) and (d) ternary latches are derived from the standard CMOS latch topology, rather than using current source biasing. Alternatively, these circuits can be viewed as a parallel combination of an nMOS and pMOS version of the Fig. 6(a) and (b) circuits, respectively. Both of these circuits exhibit rail-to-rail output voltage levels and near-zero static current at operating points OP1 and OP5. As mentioned earlier, the resistor values (diode dimensions) in Fig. 6(c) [Fig. 6(d)] must be within a certain range in order for tristable behavior to exist. It is this limitation that determines the minimum power dissipation in these circuits.

Simulations show that the Fig. 6(d) circuit is more robust than the Fig. 6(c) circuit for the same reason that Fig. 6(b) is more robust than Fig. 6(a). A summary of stable operating points of the Fig. 1 and the Fig. 6 circuits is provided in Table I.

The Fig. 6 latches were designed by first choosing nominal widths and lengths for the cross-coupled transistor structures. Then the other component values were chosen such that the most robust tristable behavior was realized. From this, the static power dissipation for each operating point was then determined. Note that each latch design could be scaled down by a factor k—that is, the transistor W/L ratios and current source values

TABLE I
SUMMARY OF STABLE DC OPERATING POINTS

Circuit version		OP_1	OP_3	OP_5
Fig. 1	V_{G1}/V_{G2} (V)	0.58/1.25	0.67/0.67	1.25/0.58
	V_{D1}/V_{D2} (V)	0.61/0.02	0.08/0.08	0.02/0.61
	I_{DD} (μA)	312	342	312
Fig. 6(a)	V_{G1A}/V_{G1B} (V)	0.75/1.03	0.84/0.84	1.03/075
	V_{D1A}/V_{D1B} (V)	0.80/0.08	0.21/0.21	0.08/0.80
	I_{DD} (μA)	488	492	488
Fig. 6(b)	V_{G1A}/V_{G1B} (V)	0.65/1.62	0.92/0.92	1.62/0.65
	V_{D1A}/V_{D1B} (V)	0.90/0.08	0.20/0.20	0.08/0.90
	I_{DD} (μA)	700	733	700
Fig. 6(c)	V_{G1A}/V_{G1B} (V)	0/1.8	0.9/0.9	1.8/0
	V_{D1A}/V_{D1B} (V)	1.8/0	0.15/0.15	0/1.8
	I_{DD} (μA)	0	251	0
Fig. 6(d)	V_{G1A}/V_{G1B} (V)	0/1.8	0.9/0.9	1.8/0
	V_{D1A}/V_{D1B} (V)	1.8/0	0.17/0.17	0/1.8
	I_{DD} (μA)	0	156	0

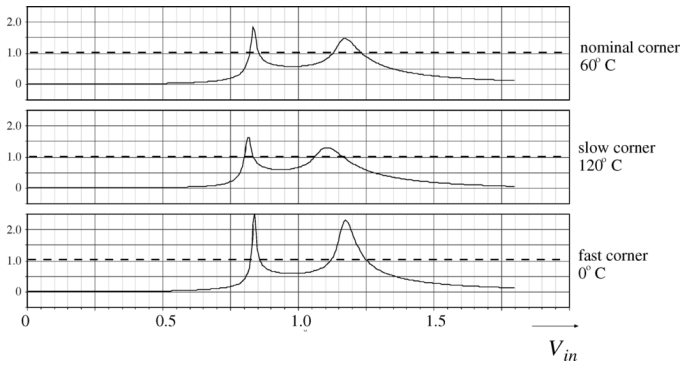

Fig. 8. Open-loop curves for the Fig. 6(d) latch at three process corners.

could be decreased by k and resistor values increased by k. Such scaling would maintain the same dc operating points—i.e., voltage levels at each operating point would be independent of such scaling—while the static power dissipation would be reduced by k. However, the latch's driving capability would also be reduced by a factor of k—that is, for a fixed capacitive load, the latch would operate k times slower with the scaling. Thus, as is normally the case for CMOS circuits, there is a direct tradeoff between power dissipation and operating speed. In addition, there is also a practical constraint: fabrication design rules always specify minimum transistor dimensions.

To verify robust operation of the Fig. 6(d) latch, open-loop simulation results for three process corners are shown in Fig. 8. All three gain curves exhibit double peaks higher than unity.

IV. CIRCUIT FABRICATION AND MEASUREMENTS

To verify operation of each of the four ternary latches presented in the previous section, ternary RS flip-flops were designed and fabricated using the Jazz Semiconductor CA18 0.18-μm CMOS process for each of the four ternary latch variations shown in Fig. 6. The schematic of the RS latch constructed from Fig. 6(d) is shown in Fig. 9. The other RS latch variations were constructed in a similar way.

The truth table for a ternary RS latch is given in Table II. Note that unlike a conventional RS latch, the simultaneous application of $R = 1$ and $S = 1$ is allowed, and results in the latching in of the middle state. Measurements verifying correct operation of the four latch variations are shown in Fig. 10.

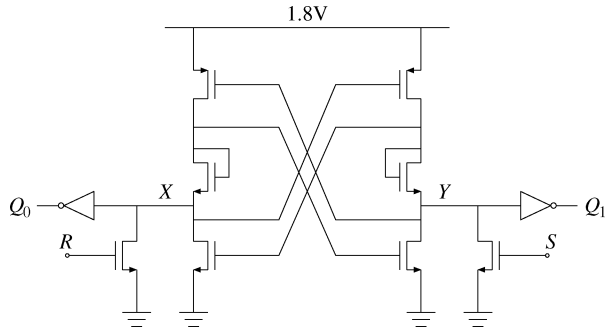

Fig. 9. RS ternary latch.

TABLE II
TRUTH TERNARY LATCH

R	S	Q_1	Q_0	op. pt.
1	0	0	1	OP1
0	1	1	0	OP5
1	1	1	1	OP3
0	0	Previous State		

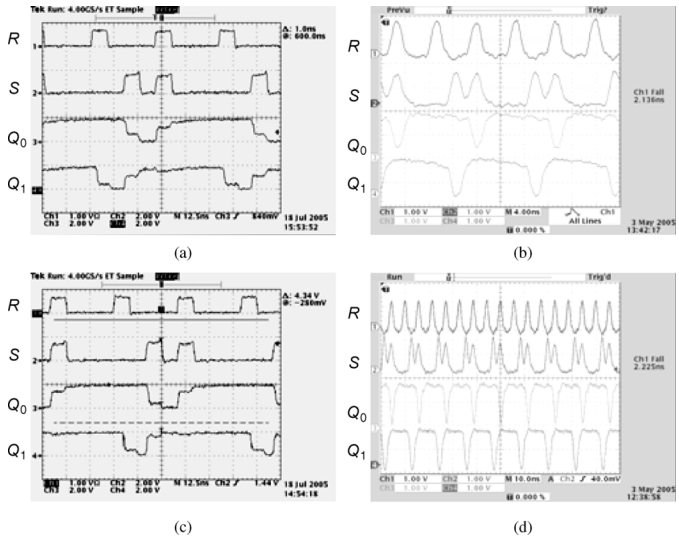

Fig. 10. Measured input and output waveforms of RS ternary latches based on: (a) Fig. 6(a) latch; (b) Fig. 6(b) latch; (c) Fig. 6(c) latch; (d) Fig. 6(d) latch.

The measured maximum frequency for each variation is summarized in Table III. Note that this maximum frequency is significantly larger for the Fig. 6(b) and (d) latches than for the Fig. 6(a) and (c) latches. The reason for this is the choice of device used to realize the voltage drop between the gates and drains of transistors in the cross-coupled structure. The diode-connected transistors used in Fig. 6(b) and (d) can realize the appropriate voltage drop with smaller incremental resistance than can the resistors used in Fig. 6(a) and (c).

Unlike the conventional RS flip-flop, the ternary version allows both R and S inputs to go high then low simultaneously in order to settle to the middle state. Thus, it is important to know the maximum skew time between these two inputs in order for this to occur. This skew region is bounded by the two metastable regions described in Section II. To measure this region, the circuit shown in Fig. 11(a) was used, where the skew between R and S was varied in 40-ps increments. The circuit operates as follows. Only one of the signals $S_0, \ldots, S_7$ is high, depending

TABLE III
PERFORMANCE SUMMARY OF FIG. 6 LATCH VARIATIONS

Latch variation	Max. frequency (MHz)	Max. skew (ps)	V_{ref} range (mV)
Fig. 6(a)	180	240	500 – 650
Fig. 6(b)	600	320	300 – 700
Fig. 6(c)	100	< 40	N/A
Fig. 6(d)	700	< 40	N/A

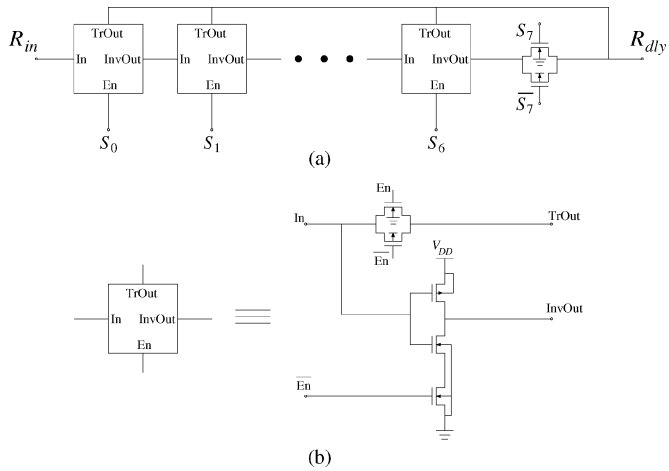

Fig. 11. Block diagram of skew generator.

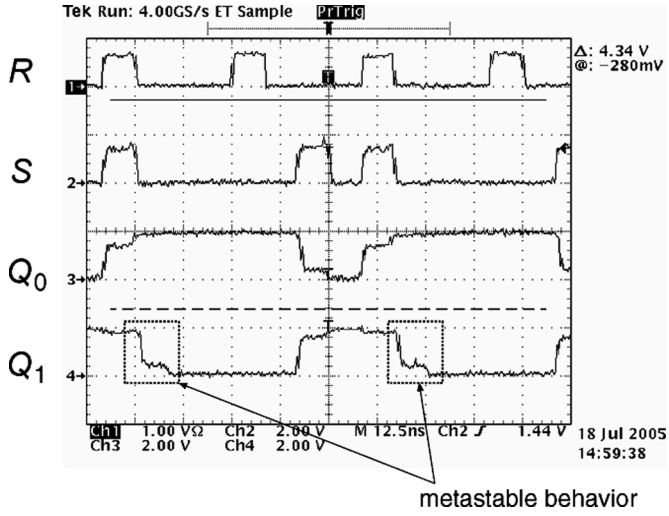

Fig. 12. Measured waveforms of RS latch based on Fig. 6(c) latch exhibiting metastable behavior.

on the desired delay. If signal $S_k, k \in [1, 2, \ldots, 7]$ is high, then the output R_{dly} will be delayed by $k \cdot T_d$ with respect to R_{in}, where T_d is the delay time of one inverter, designed to be 40 ps. In this way, variable skew can be applied between the R and S signals during measurement. The schematic of each individual delay cell is shown in Fig. 11(b). Measured results showing the metastable behavior are shown in Fig. 12. The skew ranges over which the latch will settle at OP3 for each latch are given in Table III. These ranges, given in picoseconds, are determined by the rise and fall times at nodes X and Y in the Fig. 9 circuit and by the voltage differences between the cross-coupled transistor gates corresponding to the metastable states—that is, the two states that define the boundary between the middle stable operating point and each of the two stable binary operating points.

V. CONCLUSION

This paper discussed the methodology of constructing two-transistor circuits with five operating points, three of which are stable. Open-loop analysis was employed to examine the stability properties of these operating points. As a result, some design guidelines for achieving ternary behavior were developed. Applying these guidelines, a family of CMOS ternary latches was proposed, all of which are able to possess five operating points.

Ternary CMOS RS flip-flops were simulated and implemented in the Jazz Semiconductor 0.18-μm CMOS process. Simulation and experiment demonstrated robust performance of these circuits.

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