UC Berkeley
UC Berkeley Electronic Theses and Dissertations

Title
Thermal Ground Plane for Chip-Level Electronics Cooling

Permalink
https://escholarship.org/uc/item/61v0s8q3

Author
So, Hongyun

Publication Date
2014

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

Thermal Ground Plane for Chip-Level Electronics Cooling

by

Hongyun So

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Mechanical Engineering

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Albert P. Pisano, Chair
Professor Liwei Lin
Professor Tsu-Jae King Liu

Fall 2014

Thermal Ground Plane for Chip-Level Electronics Cooling

Copyright © 2014
by
Hongyun So

Abstract

Thermal Ground Plane for Chip-Level Electronics Cooling

by

Hongyun So

Doctor of Philosophy in Mechanical Engineering

University of California, Berkeley

Professor Albert P. Pisano, Chair

The three-dimensional thermal ground plane was developed in response to the needs of high-power density electronics applications in which heat must be removed as close to the chip surface as possible. The novel design for this planar cooling device was proposed with three key innovations in the evaporator, wick, and reservoir layer, which provided enhanced and reliable cooling performance without wick dryout and back flows. For the evaporator and reservoir layer, a combination of a tapered channel and a triple-spike microstructure was designed to break up the pinned meniscus at the end of the vapor and liquid channels. The overall microstructure had three spikes where the main liquid meniscus was separated by a middle spike and then continued to flow between the tapered walls of the middle and side spikes. For the wick layer, a nanowire-integrated microporous silicon membrane was developed to overcome dryout by driving the coolant out of the channels and spreading the coolant on top of the wick surface with the assistance of extended capillary action. This innovative design used nanowires to extend and enhance capillary force, especially at the end of the pores where the coolant was pinned and unable to overflow out of the pores. The chronic dryout problem in micro cooling devices could be solved by these innovative designs.

To analyze the thermal-fluid system, fluid dynamic and phase-change models were used to calculate thermodynamic and fluidic properties, such as operating temperature, pressure, vapor-liquid interface radius of curvature, and rate of bubble formation. The microscale heat conduction theory derived from traditional Fourier's law with classical size effect and effective medium theory were used to calculate the thermal conductivities of nanowires and porous silicon wick in the cross-plane direction, respectively. The theoretical results of porous silicon showed good agreement with the experimental results measured by the 3ω technique, demonstrating the reduction of thermal conductivity from bulk silicon. Cooling performance of the developed device was demonstrated experimentally with a micro ceramic heater, thermocouple modules, and microfabrication techniques, including photoelectrochemical etching to create porous silicon, deep reactive-ion etching to form a thin wick membrane, and hydrothermal synthesis to grow nanowires on top of the wick membrane. This study shows the feasibility of reliable, continuous, and high-performance micro cooling devices using enhanced capillary forces to address the increasing requirements of thermal management for chip-level electronics.

To my family

TABLE OF CONTENTS

Dedication ... i
Table of Contents ... ii
List of Figures ... iv
List of Tables ... ix
Acknowledgements ... x

Chapter 1 Introduction ... 1
1.1 Motivation ... 1
1.1.1 Current Cooling Technologies ... 2
1.1.2 Thermal Management for High-Power Density Electronics ... 2
1.2 Dissertation Outline ... 3

Chapter 2 Design and Operating Principles ... 5
2.1 Three-Dimensional Stacked Design ... 5
2.1.1 Evaporator: Self-Transport of Condensed Liquid ... 7
2.1.2 Coherent Wick: Continuous Fluid Transport through Micropores ... 8
2.1.3 Reservoir: Rapid Refilling of Coolant ... 9
2.2 Operating Principles for Heat Removal ... 11
2.2.1 Continuous Feeding of Coolant ... 12
2.2.2 Thermal Barrier of Coherent Wick ... 13
2.2.3 Drop Propulsion in Microchannel ... 14

Chapter 3 Heat Transfer Analysis ... 15
3.1 Microscale Heat Conduction ... 15
3.1.1 Kinetic Theory of Thermal Transport ... 15
3.1.2 Temperature Dependence of Thermal Conductivity ... 17
3.2 Thermodynamics Analysis of Closed Loop System ... 23
3.2.1 Thermal Resistance Network of System ... 23
3.2.2 Thermodynamic Cycle during Operation ... 25

3.3 Liquid-Vapor Phase Change 27
3.3.1 Analysis for Fluidic and Thermal Properties 27
3.3.2 Two-Phase Nucleation Analysis 30

Chapter 4 Device Fabrication 32
4.1 Evaporator and Reservoir Fabrication by Top-Down Process 32
4.1.1 Principles of Deep Reactive-Ion Etching 32
4.1.2 Fabrication Flow for Evaporator and Reservoir 33
4.1.3 Fabrication Results 35
4.2 Coherent Porous Silicon Wick Fabrication 36
4.2.1 Principles of Photoelectrochemical Etching 36
4.2.2 Fabrication Flow for Coherent Porous Silicon Wick 37
4.2.3 Fabrication Results 39
4.3 Zinc Oxide Nanowire Synthesis by Bottom-Up Approach 40
4.3.1 Vapor-Liquid-Solid Mechanism 40
4.3.2 Hydrothermal Methodology 42

Chapter 5 Experimental Testing of Device 45
5.1 Liquid Feeding Performance Test 45
5.1.1 Self-Transport of Condensed Liquid 45
5.1.2 Continuous Wicking through Hierarchical Membrane 49
5.2 Thermal Conductivity Measurement 51
5.2.1 Principles of 3ω Method 51
5.2.2 Experimental Results 54
5.3 Cooling Performance Test 55
5.3.1 Final Feature of Device 55
5.3.2 Experimental Results 57

Chapter 6 Conclusions 60

Bibliography 62

List of Figures

Figure 2.1 General limit of handling heat flux with respect to the critical dimension of the devices. 5

Figure 2.2 Three-dimensional schematic illustration of the three-layer stacked thermal ground plane device for chip-level electronics cooling. 6

Figure 2.3 Schematic illustration of the design development process for evaporator channels: (a) straight vapor channels for simple design, (b) tapered vapor channels with specific tapered angle to enhance the capillary pressure, and (c) tapered vapor channels with crown-shaped triple-spike microstructures at the end of channels to distribute the liquid meniscus inducing overflowing of liquid. 7

Figure 2.4 Schematic illustration of the design for coherent wick layer: (a) pinned liquid meniscus at the end of vertically aligned microchannels and (b) overflowing liquid by the enhanced and extended capillary force using nanowires grown over the top surface of the wick. 9

Figure 2.5 Schematic illustration of the design for reservoir layer with a combination of tapered microchannels and triple-spike microstructures at the end of each channel to rapidly collect the condensed liquids into the reservoir. 10

Figure 2.6 Scheme of cross-sectional view of the thermal ground plane with hot chip integrated on the evaporator layer for cooling purposes and internal fluid status at (a) device off-mode and (b) device on-mode. 11

Figure 2.7 Pressure drop across the wick in response to the pore radius for (a) different porosity with constant heat flux of 40 W/cm^2 and wick membrane thickness of 200 μm and (b) different wick membrane thickness with constant heat flux of 40 W/cm^2 and porosity of 0.2. 13

Figure 2.8 Schematic illustration of the role of the coherent wick layer as a thermal barrier to initiate boiling on the evaporator site: (a) dryout limitation when the thermal resistance of the wick is low and (b) desirable operation of the device when the thermal resistance of the wick is high enough. 14

Figure 3.1 Schematic of (a) classical size effect when the characteristic length (L) is smaller than the mean free path (Λ) and larger than the wavelength (λ) and (b) control volume for a derivation of modified Fourier's law rested on kinetic theory. 16

Figure 3.2 Calculated thermal conductivities for silicon from kinetic theory and comparison with experimentally measured thermal conductivities for a different diameter of silicon nanowires. 18

Figure 3.3 Calculated thermal conductivities of (a) zinc oxide (ZnO) with experimental results for a bulk sample and nanowires of different diameters and (b) silicon of the same diameter as ZnO for comparison purpose. The result shows that the thermal conductivities of ZnO are lower than those of silicon for all temperature ranges. 18

Figure 3.4 Theoretical analysis of the (a) thermal conductivity, (b) thermal resistance, and (c) effective mean free path of the evaporator layer at 100℃ with respect to the thickness. Active cooling area is 5×5 mm^2. 20

Figure 3.5 Comparison of theoretical models to predict the effective thermal conductivity of porous silicon with respect to the porosity. 22

Figure 3.6 (a) Image of the MEMS chip mounted on a chip carrier for first-level cooling, (b) schematic illustration of the chip integrated on a thermal ground plane for second-level cooling, and (c) thermal resistance network of the combined devices for simultaneous cooling. Scale bar: (a) 5 mm. 24

Figure 3.7 T (temperature)-s (specific entropy) and P (pressure)-v (specific volume) thermodynamic diagram during the operation in the thermal ground plane with a schematic illustration for each state point in the device. 26

Figure 3.8 Schematic illustration of the overall thermal ground plane device with geometry and noticeable points for the thermal system analysis. 28

Figure 3.9 Computed rate of bubble formation with different liquid temperatures for homogeneous nucleation based on the kinetic limit of superheat. 31

Figure 4.1 Schematic illustrations of (a) asymmetrical reactive-ion etching system chamber and (b) working principles of deep reactive-ion etching using alternative etching and polymer deposition cycles. 33

Figure 4.2 Fabrication flow schematic of (a) evaporator layer and (b) reservoir layer using standard photolithography and deep reactive-ion etching. 34

Figure 4.3 SEM images of deep reactive-ion etched evaporator layer: (a) neck part where the evaporator site and vapor channels are connected and (b) intermediate chamber, which is the end of the tapered vapor channels where the condensed liquid meniscus overflows by triple-spike microstructure. Scale bars: 200 μm for both (a) and (b). 35

Figure 4.4 Zoomed-in view of triple-spike microstructures at the end of tapered vapor and liquid channels to drive the liquid meniscus out of the channels by extending the capillary action. Scale bar: 100 μm. 35

Figure 4.5	Schematic illustration of the coherent porous silicon fabrication process by photoelectrochemical etching process. The minority carriers in n-type silicon move to the hydrofluoric acid-silicon contact surface to attack the weaken silicon-silicon bond.	37
Figure 4.6	Fabrication flow of (a-c) coherent porous silicon wick by local photoelectrochemical etching, (d-f) deep reactive-ion etching of backside of wafer, and (g) laser etching through the layer for via hole connected to the condenser.	38
Figure 4.7	SEM images of photoelectrochemically etched coherent porous silicon: (a) top surface view, (b) zoomed-in view of micropores, (c) 45° tilted view, and (d) zoomed-in view of straight and vertically aligned microchannels generated by coherent porous silicon. Scale bars: (a) 10 μm, (b) 2 μm, (c) 30 μm, and (d) 10 μm.	39
Figure 4.8	SEM images of coherent porous silicon wick membrane after backside deep reactive-ion etching: (a) 30° tilted view and (b) cross-sectional view. Scale bars: (a) 30 μm and (b) 10 μm.	40
Figure 4.9	Schematic illustration of experimental setup for vapor-liquid-solid zinc oxide nanowires growth on the photoelectrochemically etched porous silicon wick layer.	41
Figure 4.10	SEM images of the porous silicon wick membrane decorated by zinc oxide nanowires synthesized by vapor-liquid-solid mechanism: (a) initiation of growth from the gold catalyst particles on the porous silicon substrate, (b) zoomed-in view of initial formation of whiskers, (c) top surface view of nanowire-integrated porous silicon wick, and (d) zoomed-in view of micropore ends covered by zinc oxide nanowires. Scale bars: (a) 2 μm, (b) 1 μm, (c) 10 μm, and (d) 1 μm.	41
Figure 4.11	Fabrication flow of nanowire-decorated porous silicon wick layer by (a-b) standard photolithography, (c-d) deposition of zinc oxide nanoparticles by lift-off, and (e-f) hydrothermal synthesis in precursor solution.	43
Figure 4.12	SEM images of the porous silicon wick membrane covered by zinc oxide (ZnO) nanowires synthesized by hydrothermal methodology: (a) seeded porous silicon wick by ZnO nanoparticles, (b) zoomed-in view, (c) top surface view of nanowire-integrated porous silicon wick, and (d) zoomed-in view of micropore ends covered by ZnO nanowires. Scale bars: (a) 1 μm, (b) 200 nm, (c) 2 μm, and (d) 1 μm.	44

Figure 4.13 SEM images of the hierarchical porous silicon wick layer decorated by zinc oxide nanowires to drive the coolant out of the pore by the assistance of extended capillary action: (a) 20° tilted view and (b) zoomed-in view. Scale bars: (a) 10 μm and (b) 2 μm. 44

Figure 5.1 Schematic illustrations of microchannel designs in the evaporator layer to transport the condensed liquid into the reservoir chamber: (a) tapered design, (b) micropost design in the tapered design, (c) single-spike design in the tapered design, and (d) triple-spike design in the tapered design. 45

Figure 5.2 SEM images of four different fabricated designs for vapor and liquid channel in the thermal ground plane: (a) tapered channel, (b) microposts design in the tapered design, (c) single-spike design in the tapered design, and (d) triple-spike design in the tapered design. Scale bars: 20 μm for (a), (b), (c), and (d). Lower images: measured contact angles on the different surfaces including silicon with native oxide, quartz, and silicon dioxide. 46

Figure 5.3 Comparison of results between computational and experimental results for each designed microchannel to transport the liquid liquid by extended capillary action. Scale bars: 100 μm for (a), (b), (c), and (d). 47

Figure 5.4 Sequential images of self-transporting condensed liquids in the evaporator channel (from top left to bottom right). The liquids were first transported along the tapered channels and then collected on the triple-spike microstructures by distributing menisci. Scale bar: 400 μm. 48

Figure 5.5 Comparison of wicking performance between (a) traditional wick structure and (b) nanowire-decorated coherent porous silicon wick structure. Sequential images were taken by a high-speed camera. Scale bars: 5 mm for (a) and (b). 49

Figure 5.6 Feeding of coolant from reservoir to evaporator surface by nanowire-decorated coherent porous silicon wick structure. The microscale gap between evaporator and wick layer was filled with coolant in a short period of time. The blue arrow indicates the moving meniscus. Scale bar: 100 μm. 50

Figure 5.7 Sample preparation process for thermal conductivity measurement of the porous silicon wick structure by 3ω method: (a) photoelectrochemical etching for forming the porous silicon wick, (b) deep reactive-ion etching of bulk silicon, (c) deposition of electrically insulating layer, followed by the microheater line, and (d) SEM image of fabricated heater line on the back side of porous silicon wick. Scale bar: (d) 100 μm. 52

Figure 5.8 Thermal conductivities of bulk silicon (20 μm) and porous silicon wick (170 μm) measured by the 3ω method as compared to computational results calculated by the kinetic theory and effective medium theory. 55

Figure 5.9 Final device feature of the thermal ground plane composed of three layers: (a) evaporator layer with triple-spike microstructure, (b) wick layer with nanowire-decorated coherent porous silicon, and (c) reservoir layer with triple-spike microstructure. Scale bars: (a) 200 µm, (b) 2 µm, (c) 200 µm, and (d) 5 mm. 56

Figure 5.10 Schematic illustration of the experimental setup to analyze both qualitative and quantitative cooling performance of final fabricated thermal ground plane. 57

Figure 5.11 Transient phase-change of coolant in the evaporator site and movement of condensed liquid along vapor channels toward the intermediate chamber. The condensed liquids were collected on the triple-spike microstructures and continued to flow into the liquid channels in the reservoir layer. Time interval: 5 s; scale bar: 5 mm. 58

Figure 5.12 Temperature change of the micro ceramic heater during cooling by the fabricated thermal ground plane device. The device was removed from the heater after 3 min and 40 sec to verify the cooling performance of the device. 59

List of Tables

Table 3.1 Parameter values determined by a combination of theory and fitting thermal conductivities with respect to temperature for bulk silicon and zinc oxide (ZnO) samples. 17

Table 3.2 Thermal conductivities, lengths, and heat transfer area of each component participating heat conduction across the thermal ground plane layers from top of the junction to bottom of the reservoir. 25

Table 3.3 Dimensions of the thermal ground plane device used for thermal and fluidic analysis. 29

Table 3.4 Calculated thermal and fluidic properties in the thermal ground plane based on the designed specifications. 29

Table 5.1 Input parameters to extract the thermal conductivity from out-of-phase 3ω voltage for anisotropic porous silicon wick structure. 54

Acknowledgements

First and foremost, I would like to express my sincere appreciation to my research advisor, Professor Albert P. Pisano, for his technical guidance and financial support during my Ph.D. program. This research could not have been completed without the exceptional degree of freedom and encouragement Professor Pisano gave, which will always be remembered.

I also greatly acknowledge Professor Liwei Lin for providing the research environments in his laboratory and supporting active collaboration in my other project–microfluidic microdevices. All his classes inspired me with enthusiasm and helped broaden my perspectives in the field of nanoscience and technology. I am also very grateful to Professor Tsu-Jae King Liu for serving as a committee member for my doctoral qualifying examination and dissertation. Professor Liu offered me valuable feedback on my dissertation. I also wish to thank Professor Chris Dames for serving as a committee member for my doctoral qualifying examination and providing research collaboration for thermal conductivity measurement.

My fellow colleagues in the Berkeley Micromechanical Analysis and Design (BMAD) lab have played a large part in making my graduate life at Berkeley enjoyable. I especially want to thank Dr. Jim Cheng and Ms. Lilla Smith for their valuable discussions and instrumentation assistance for my research. I also wish to thank to Geoff Wehmeyer and Fan Yang in Professor Dames' group for their friendship and help in measurement of thermal conductivity.

I wish to express my deep gratitude to Professors Yongmo Kim and Sukkee Um at Hanyang University for their continuous encouragement, which always motivated me to chase my dream since I was an undergraduate. They were not only excellent advisors in academic aspects but also great mentors in my life. I also cannot forget to acknowledge Professor Young Ho Seo at Kangwon National University for providing various research collaborations with insightful ideas and invaluable advice during his sabbatical at the BMAD lab.

Last but not least, I would like to extend my deepest gratitude to my family, especially my parents. Without their unconditional support, endless love, and encouragement over many years, I could never have earned my doctorate in the United States. I also would like to thank my elder and younger brothers for their enduring care and belief in me no matter what I do. Thank you all again for making me appreciate what I have earned here at the University of California, Berkeley.

Chapter 1

Introduction

1.1 Motivation

Thermal management for electronics is a chronic, essential issue for achieving a high performance level of electronic devices by preventing thermal damages including degradation, thermal shock, and vibration. In general, poor removal of heat flux causes device failure with severe problems, which can affect whole operating systems. Efficient cooling of hot electronic devices is one of the key pieces for achieving high performance of devices. During the past decade, developments in semiconductor industries have allowed electronics such as sensors and actuators to be miniaturized in microscale to increase the yield in a limited space. Consequently, thermal management of chip-level electronics is now becoming critical for next-generation electronics. To satisfy the increasing market demand for cheaper, smaller, faster, and more reliable cooling, new miniaturized active and passive cooling devices are being developed for efficient and rapid heat removal away from the heat sources.

The advent of microelectromechanical systems (MEMS) and nanotechnologies has allowed for the development of new microscale cooling devices that are compact and compatible with traditional semiconductor devices to efficiently remove high heat flux from heat sources. Among various heat removal methods including active, passive, or a combination of both, passive cooling is now prevailing in current chip-level applications because it does not require an additional power source that might need supporting electric circuit on the platform. The main passive cooling systems use the basic heat transfer mechanisms—conduction [1,2], convection [3,4], and radiation [5,6]—where the heat transfer rate generally relies on the thermal conductivity of substrates, properties of surrounding gases, or emissivity of surfaces. However, these systems are not suitable for many chip-level electronic applications because the systems' efficiency significantly depends on the material properties. Therefore, the combination of emerging MEMS technology and rapidly increasing demands for thermal management for advanced miniaturized electronics has led to the phase-change cooling techniques using superior heat absorption properties when the liquid coolants change to vapor [7-9].

Miniaturized planar-type cooling devices have recently been proposed to handle higher heat flux in a wide range of applications, from ground to space environments [10-13]. In these systems, the microchannels have been fabricated by various silicon etching technologies to utilize the capillary force of coolants during the device operation. However, unexpected dryout problems [14], backward bubble flow [15], and liquid-vapor interface oscillating [16] were caused by unstable capillary forces during the phase-change process. Consequently, the development of a MEMS-based phase-change micro cooling device, which would be able to overcome dryout problems with continuous, reliable, and controllable operation, has remained an engineering challenge.

1.1.1 Current Cooling Technologies

Based on the physical mechanism, current cooling technologies can be categorized as active, passive, or hybrid systems. The most well-established active cooling device is a fan utilizing the forced convection to enhance the air velocity and thus the convective heat transfer coefficient and heat transfer rate [17-19]. The fan does not rely on the thermal conductivity of substrate materials and has an advantage for large area cooling applications. However, these active cooling systems require additional supporting power supply equipment and generate noise during the operation. The traditional passive cooling systems are thermal spreaders and heat pins utilized widely because of their advantages of zero noise and zero power consumption. These systems are based on the thermal conductivity of the solid substrate by contacting the substrate surface and heat source surface. To enhance the efficiency of heat removal, a heat pipe using the principles of both thermal conductivity and phase transition of a working fluid has been developed for many electronic applications [20,21]. A liquid in contact with conductive solid surface changes to a vapor by absorbing heat from the hot substrate. While traveling to the heat sink where the latent heat is released, the vapor turns into a liquid again and completes a cycle by returning the condensed liquid to the hot substrate through the capillary action. Although heat pipes require no maintenance because of the absence of mechanical moving parts, non-condensed gases may diffuse through the pipe walls, which may increase the thermal resistance and operating temperature and thus result in the breakdown of circulation of coolant and destruction of the device by increased pressure from non-condensed gases [22,23]. In addition, heat pipes developed thus far are more suitable in large-scale applications, such as solar power plants or building systems, rather than chip-level electronics. To maximize the efficiency of heat removal, hybrid cooling systems integrating both active and passive systems have been recently developed and are now being used for many applications [24,25].

1.1.2 Thermal Management for High-Power Density Electronics

According to Moore's law, the number of transistors in an integrated circuit (IC) doubles approximately every two years, while the size of the individual chip decreases [26,27]. The decrease in the size of chips has led to increased heat dissipation per unit area of chip surface, while overall performance of ICs has improved, and the cost of individual transistors has been reduced [28]. Heat dissipation is considered to be a well-known reason for energy loss and a potential issue that may limit the performance of information processing [26,28]. Most MEMS actuators, which allow mechanical actuating parts to have a large surface-to-volume ratio, also generate tremendous heat flux during the operation using Joule heating through the electrodes. In such systems, current chip-level heat fluxes have already reached 10 W/cm^2 and are expected to exceed 200 W/cm^2 within a decade for many high-power density electronic applications. When these high heat fluxes exceed critical heat flux levels, which is the maximum heat flux that can be loaded on the chip and represents the operational limit of the device because of significantly reduced heat transfer coefficients, the device temperature will be dramatically increased, resulting in device failure [29,30]. Therefore, the increasing demand for thermal management of high-power density electronic devices, including laptops, mobile phones, light emitting diodes, solar cells, and batteries, has led to the development of various innovative cooling technologies [31-33].

1.2 Dissertation Outline

This dissertation reports the development of a new three-dimensional planar-type cooling device. The overall outline for the dissertation is composed of five main chapters: (a) design of the device and operating principles, (b) heat transfer and thermodynamic analysis of the device, (c) device fabrication, (d) experimental testing of the fabricated device, and (e) conclusion and outlook. This dissertation is expected to provide promising and significant groundwork for next-generation cooling technologies to address the thermal management demands for high-power density electronics. The detailed overview of each chapter is as follows.

In Chapter 2, the novel design for a MEMS-based three-dimensional planar cooling device is described with three key innovations in each layer (i.e., evaporator, wick, and reservoir layer). To remove heat coming from hot chips through the evaporator layer, continuous feeding of the coolant without dryout is most important and key innovation in the overall system. In this chapter, the scheme of continuous fluid transport by a hierarchical micro- or nano-structured wick layer is proposed to prevent severe dryout problems during operation. This first novel structure in the wick layer was designed to maintain the circulation of coolant in the device during the steady-state operation. However, when the chip was turned off, droplets suddenly condensed due to decreased vapor pressure and temperature became stuck in the middle of the microchannels on the evaporator layer, which may cause dryout again, as these droplets did not return to the reservoir. Therefore, a second novel structure in the evaporator was designed to transport the stuck liquids automatically from microchannels to the reservoir for the preparation of the next cycle before the chip is turned on again. The last innovation in the device is directly related to the first innovation mentioned above. To induce the boiling of coolant near the evaporator site, the wick layer must act as a thermal barrier to prevent the nucleation of coolant in the reservoir by providing reasonably high thermal resistance. For this innovation, zinc oxide (ZnO) nanowires that have low thermal conductivity were selected and characterized rather than the other type of nanowires. The design and fabrication of nanowire-integrated porous silicon wick have been disclosed elsewhere [H. So, J. C. Cheng, and A. P. Pisano, "Nanowire-integrated microporous silicon membrane for continuous fluid transport in micro cooing device," *Appl. Phys. Lett.*, vol. 103, 163102, 2013 and H. So, J. C. Cheng, and A. P. Pisano, "Multi-scale pore membrane for continuous, passive fluid transport in a micro cooling device," in *Tech. Dig. Int. Conf. Solid-State Sensors., Actuat. Microsyst.*, 2013, pp. 2197–2200].

Chapter 3 describes microscale heat conduction theory derived from traditional Fourier's law with classical size effect to estimate the thermal conductivity of nanowires and evaporator layer in the cross-plane direction. Because the thermal conductivity of the device depends on the operating temperature, the temperature dependence on thermal conductivity in each layer is discussed with the kinetic theory. The effective medium theory is also discussed to estimate the thermal conductivity of porous silicon wick structure in cross-plane direction practically. After calculating the thermal conductivities for all components with the kinetic theory and effective medium theory, the thermal resistance network analysis is performed to determine the values of design parameters. Finally, numerical analysis for two-phase flow during the phase-change is discussed with various two-phase models and corresponding thermodynamic cycles to calculate the fluidic and thermal properties, such as operating pressure, temperature, interface radius of curvature, and rate of bubble formation.

In Chapter 4, the detailed overall fabrication process and results are presented for each layer. The overall fabrication process for the device includes four main processes: (1) photoelectrochemical (PEC) etching to create coherent porous silicon, (2) deep reactive-ion etching (DRIE) to form a thin wick membrane, (3) the hydrothermal method to synthesize nanomaterials on top of the wick membrane, and (4) surface treatment for changing the device surface property from hydrophobic to hydrophilic, which enhances the capillary action in the microchannels. The fabrication process is described in detail, layer by layer, using either a top-down or a bottom-up approach. Scanning electron microscope (SEM) images are shown in this chapter to characterize the fabrication results.

In Chapter 5, experimental results are shown, including the thermal conductivities in the cross-plane direction for each layer that were measured by the 3ω technique, wicking performance through the fabricated wick structure, and self-transported liquid along the tailored microchannel, along with acquired data and captured images. These experimental data are compared with the data from the numerical analysis from Chapter 3 to demonstrate the reliability of the proposed device. The detailed experimental setups and a sample preparation process are also presented, along with necessary images. Finally, the efficiency and heat removal capability of the fabricated device are discussed at the end of the chapter, along with the temperature change of the chip during cooling performance.

In Chapter 6, the entire content of the dissertation is summarized, and future works are discussed, including hermetic device sealing, the feasibility of the direct integration with ICs, and applications in harsh environments. The chapter concludes with a future outlook of the proposed device in relation to the field of MEMS-based micro cooling devices.

Chapter 2

Design and Operating Principles

2.1 Three-Dimensional Stacked Design

The dimensions of micro cooling devices rely on the heat flux handling limit. Figure 2.1 shows the general limit of handling heat flux with respect to the dimension of MEMS-based cooling devices. In general, a one-dimensional design of a device is able to be fabricated easily by anisotropic silicon etching using potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). After etching, wick materials such as mesh screen, nickel foam, or stainless steel fibers can be filled out along the edges of the triangle-shaped passage. After hermetic sealing of the evaporator layer, heat dissipation can be removed by phase-change inside the device, as shown in Fig. 2.1. Once the liquid receives heat from chips, the liquid in contact with the edges turns into a vapor, and this vapor travels to the other side of the device (i.e., condenser) across the middle of the chamber. After the vapor is condensed to liquid, liquid droplets return to the evaporator section through the wick materials. However, because the traveling vapor is in direct contact with turning liquid in the wick material, there is parasitic heat transfer from vapor to liquid during the circulation, which may cause oscillating vapor-liquid interface [15].

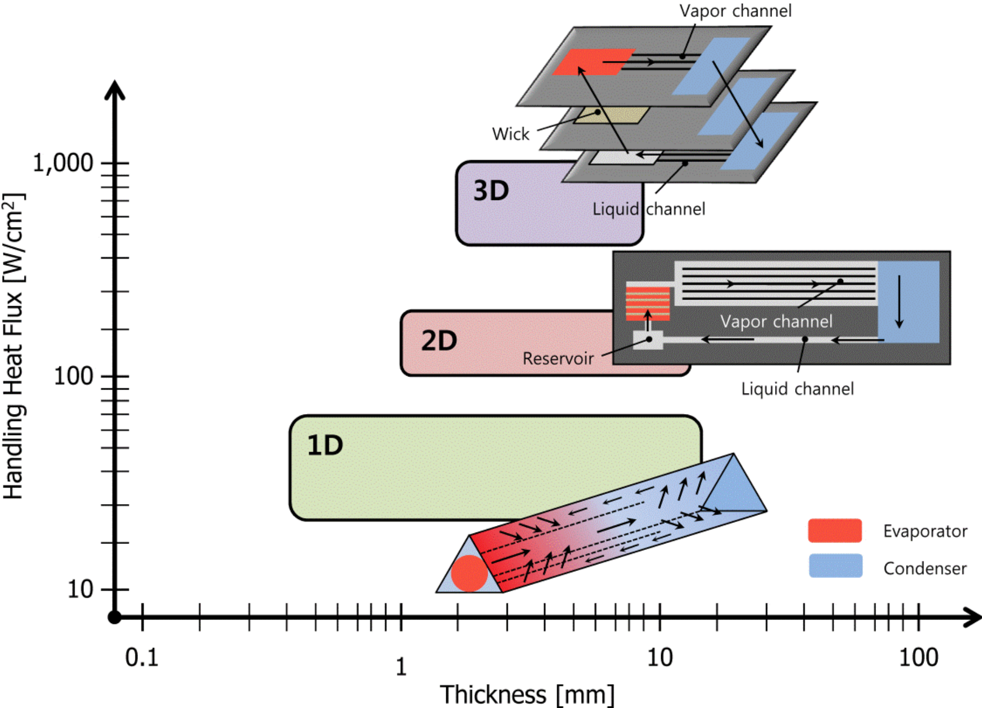

Figure 2.1 General limit of handling heat flux with respect to the critical dimension of the devices.

The two-dimensional design has been recently proposed and widely investigated, both theoretically and experimentally [11,34,35]. The critical innovation of these planar cooling devices is to use a thermal barrier between vapor and liquid channels to prevent parasitic heat transfer to the compensation chamber (see Fig. 2.1). Therefore, the condensed liquid can continue to remove heat from the sources within a thermodynamically stable state, which may maximize the efficiency of cooling performance. The wick structure—vertically aligned rectangular walls with a certain pitch distance—was also integrated using anisotropic silicon etching to maintain coolant contact with the evaporator surface. At initial state of the operation, the spaces between walls were filled with coolant, and thus there was contact with evaporator surface. However, as the liquid changed to vapor on the evaporator surface, a thin vapor film began to cover the heated evaporator surface and disturbed continuous feeding of the coolant from the wick structure, resulting in dryout problems. Furthermore, the fabrication of a vapor channel and a liquid channel on the same plane allowed vapor bubbles to form during boiling near the evaporator surface and to flow back to the coolant chamber. Therefore, a new and novel design microscale planar cooling device needed to be developed for improvement of cooling efficiency with a reliable operation that prevents severe dryout.

In this study, the three-dimensional Thermal Ground Plane (TGP), which is analogous to an electronic ground plane, was developed in response to high-power density electronic applications in which heat is removed as close to the chip surface as possible, which provides enhanced and reliable cooling performance without dryout and back flows. The TGP includes three main layers: evaporator, wick, and reservoir layer, as seen in Figure 2.2. It is noticeable that the wick layer also acts as a thermal barrier to separate the liquid channel from the vapor channel. The basic cooling mechanism is to use phase-change of coolant, similar to the process used in one- and two-dimensional devices. However, in the present study, novel and innovative structures were developed to feed the coolant continuously from the reservoir to the evaporator surface and to prevent the back flows of both bubbles and condensed liquids (i.e., achievable one-way flow).

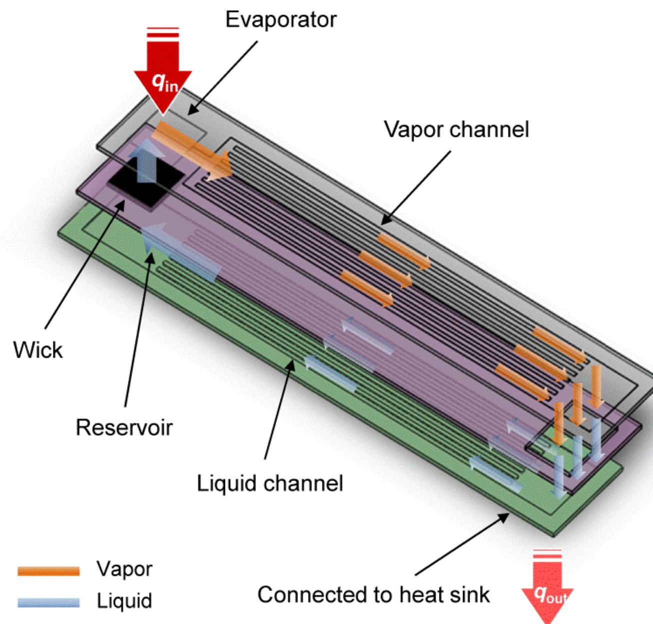

Figure 2.2 Three-dimensional schematic illustration of the three-layer stacked thermal ground plane device for chip-level electronics cooling.

2.1.1 Evaporator: Self-Transport of Condensed Liquid

The evaporator layer that is in direct contact with hot chips on top of the layer is basically composed of three sections: an evaporator site, vapor channels, and an intermediate chamber connected to the condenser on the reservoir layer, as seen in Figure 2.3(a). The dimension of the evaporator site can be scaled up or down in response to the size of the chip. The vapor channels play an important role in transporting vapors from the evaporator site to the intermediate chamber with minimum pressure loss. A number of channel, length, and cross-section areas of the channel depend on the desirable heat flux that can be handled by the TGP device. One of the most important roles of this vapor channel is that channels must be able to transport unexpected liquid droplets to the reservoir without external forces to prevent dryout. For example, when the operation of a chip mounted on the evaporator site is turned off, some portion of vapors that were flowing along the vapor channels turn into liquid in the middle of the channel due to the suddenly decreased temperature near the evaporator site. In such a case, the condensed liquids can be stuck in the middle of the vapor channel and thus affect the next cooling cycle by making a dryout in the reservoir. Consequently, a novel design for vapor channels was necessary to safely and rapidly transport condensed liquids in the channels to the liquid chamber. For this design, three different designs were first considered to use capillary pressure, as seen in Fig. 2.3. As the size of the channel becomes microscale, liquids can propel themselves using capillary

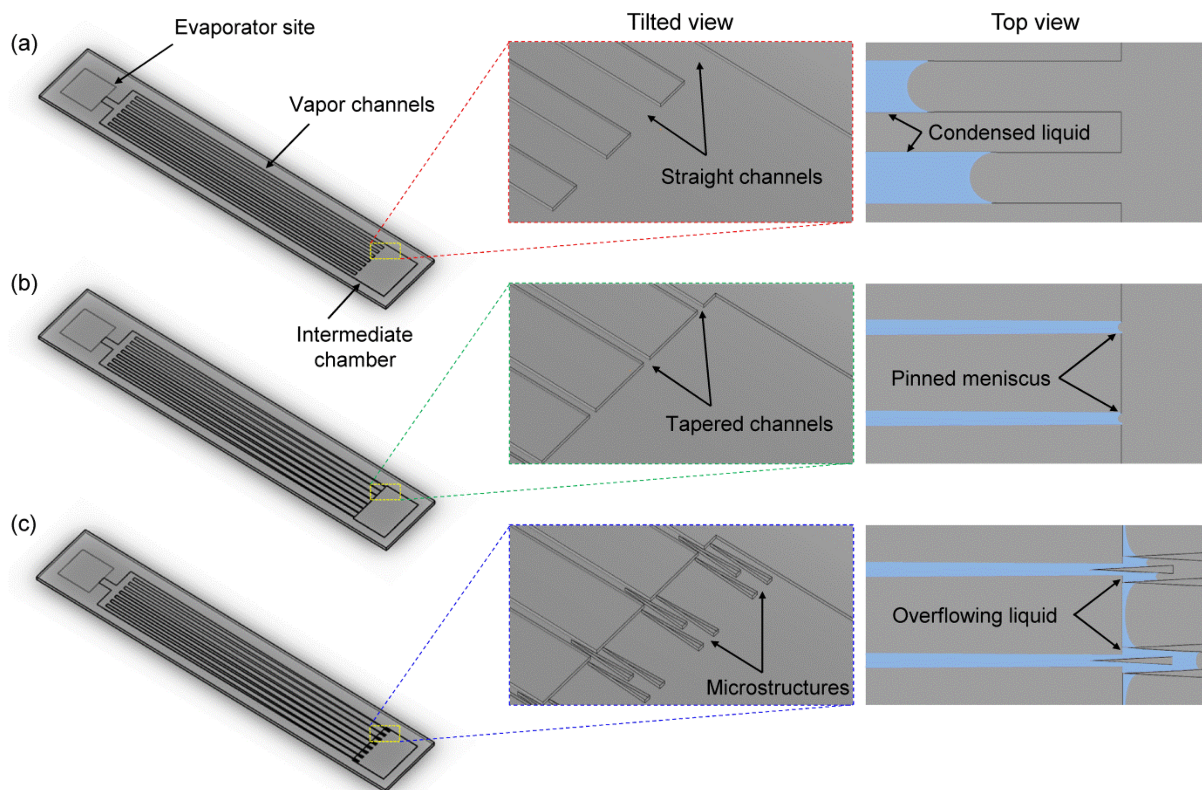

Figure 2.3 Schematic illustration of the design development process for evaporator channels: (a) straight vapor channels for simple design, (b) tapered vapor channels with specific tapered angle to enhance the capillary pressure, and (c) tapered vapor channels with crown-shaped triple-spike microstructures at the end of channels to distribute the liquid meniscus inducing overflowing of liquid.

force, forming a meniscus along the wall with a contact angle. However, because the capillary force cannot transport fluid without a sufficient force gradient, even in the microscale channels, very few liquids may reach the end of the channels, as seen in Fig. 2.3(a). To enhance capillary force in the channel, a tapered channel with a small angle can be used to propel the liquids farther [36]. Because the tapered shape makes a difference in curvature of the liquid surface (i.e., a narrower region has smaller curvature of the liquid), a liquid droplet flows in the direction of lower pressure (i.e., narrower region) due to the differences in the axial pressure resulting from different curvatures. Fig. 2.3(b) shows the tapered vapor channel with a tapered angle of 0.286°. Due to the gradually narrowed width of the channel, liquid is expected to flow faster and farther than in a straight channel and also expected to reach the end of the channel due to enhanced capillary pressure. Unfortunately, however, it is also obvious that the liquid meniscus in this design cannot be advanced beyond the end of the channel without an external driving pressure pushing the liquid into the intermediate chamber [37-40]. This means that the liquid meniscus is pinned at the end of the channel and thus unable to flow farther. Therefore, to break up the pinned meniscus at the end of the channel, a crown-shaped triple-spike microstructure was finally introduced, as seen in Fig. 2.3(c). The overall microstructure has three spikes where the main liquid meniscus is separated by a middle spike and then continues to flow between the tapered walls of the middle and side spikes. After liquids overflow into the intermediate chamber, these liquids fall down to the condenser part of the reservoir layer via a hole in the wick layer and then must be transported again through the liquid channels to the reservoir chamber (see Fig. 2.2). The design of liquid channels is almost equal to that of vapor channels, except for liquid flow direction. The detailed strategy will be explained in subsection 2.1.3.

2.1.2 Coherent Wick: Continuous Fluid Transport through Micropores

The capillary force also limits the feeding of coolant from the liquid reservoir to the top surface of the evaporator layer. Although the condensed liquids can return to the reservoir with the assistance of a combination of tapered channels and triple-spike microstructures, liquid coolant must be pumped to the evaporator surface again for reliable operation without dryout. Therefore, in a three-dimensional TGP device, continuous pumping of coolant from reservoir to evaporator site is also significantly important to maintain the device’s operation. One of the key components for achieving this continuous liquid pumping is the coherent wick, which consists of vertically aligned cylindrical microchannels on the second layer (i.e., coherent wick layer) between the evaporator and reservoir layer, as seen in Fig. 2.2. This crucial component needs to provide reliable and continuous pumping capability against gravity (even several times that of gravity for aviation applications). Figure 2.4 depicts the design of the coherent wick layer for sufficient coolant pumping. The area of the wick also depends on the area of evaporator site, as mentioned in the previous subsection. If a typical wick structure is used in the TGP, as seen in Fig. 2.4(a), the liquid would be sucked into the micropores and then surge up through the vertically aligned cylindrical microchannels against gravity because of primary capillary action. However, the surged liquid would not be able to advance out of the micropores forming a meniscus again at the edge of the pores, which would cause a severe dryout problem in the entire TGP device. Therefore, a novel design and innovation for the wick layer is necessary to allow the pinned liquid meniscus to overflow out of the microchannels so that coolant is able to remove the heat flux by touching the evaporator surface.

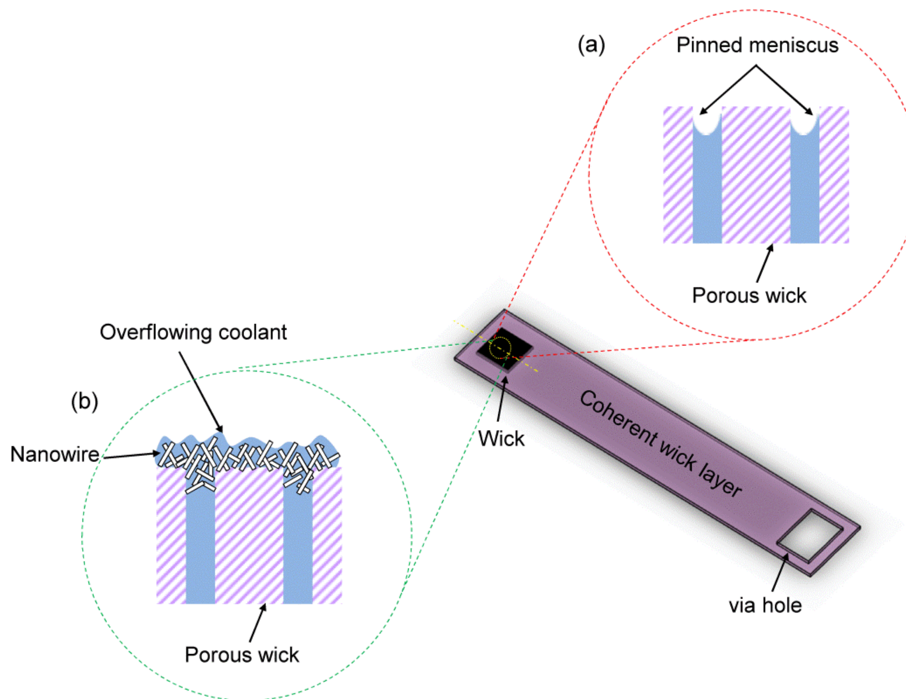

Figure 2.4 Schematic illustration of the design for coherent wick layer: (a) pinned liquid meniscus at the end of vertically aligned microchannels and (b) overflowing liquid by the enhanced and extended capillary force using nanowires grown over the top surface of the wick.

Figure 2.4(b) shows the proposed nanowire-integrated microporous silicon membrane to overcome the dryout problem by driving the liquid out of the channels and spreading it on top of the wick surface with the assistance of extended capillary action [41]. The innovation in this design is the use of nanomaterials (i.e., nanowires) to extend and enhance the capillary force, especially at the end of the pores where the liquid is pinned and not able to overflow out of the pores. The nanowires synthesized on top of the wick surface would help break up the pinned meniscus, forming tremendous nanochannels with a nano-gap and thus pulling it up between the nanowires, as seen in Fig. 2.4(b). In this study, ZnO nanowires were carefully selected and used due to their low thermal conductivity related to a role as a thermal barrier and a simple synthesis method as opposed to other types of nanowires. The role and impact of ZnO nanowires on the thermal properties of the whole TGP system will be discussed in section 2.2. Because the surface property of ZnO to water is hydrophobicity, surface treatments with ultraviolet irradiation [42-44] or silicon dioxide (SiO_2) deposition [45,46] were additionally needed to change the surface wettability from hydrophobicity to hydrophilicity. The detailed fabrication process for nanowire-integrated microporous silicon membranes is described in Chapter 4.

2.1.3 Reservoir: Rapid Refilling of Coolant

The reservoir layer in the TGP device includes three main parts: a liquid chamber, liquid microchannels, and an intermediate chamber connected to a heat sink. As the vapor channels in the evaporator layer, the liquid microchannel in the reservoir layer also plays a pivotal role in

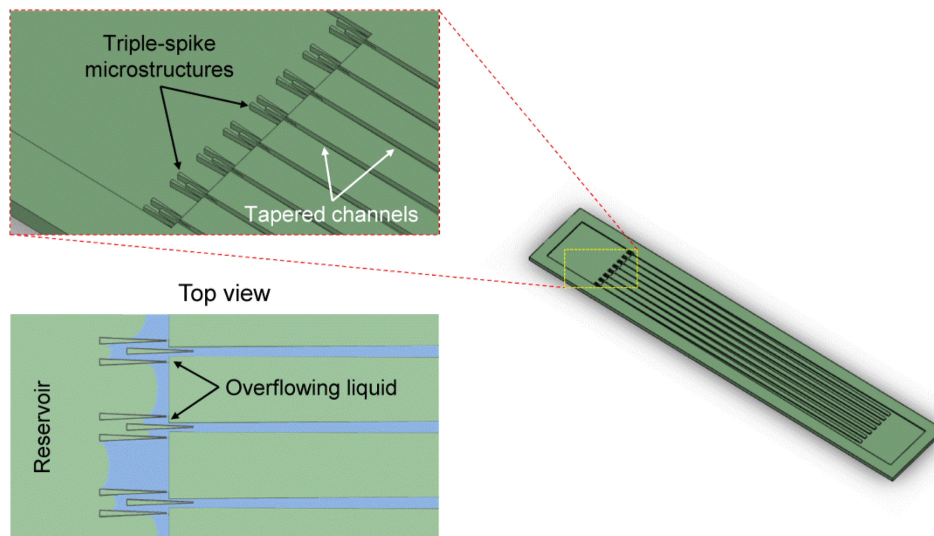

Figure 2.5 Schematic illustration of the design for reservoir layer with a combination of tapered microchannels and triple-spike microstructures at the end of each channel to rapidly collect the condensed liquids into the reservoir.

transporting the condensed coolant from the intermediate chamber to the liquid chamber. Therefore, the dryout limitation can be prevented by a rapid refilling of coolant into the reservoir. To collect the condensed liquids into the reservoir, the same innovative design used for the evaporator layer was adopted to the reservoir layer. Figure 2.5 illustrates the scheme of the reservoir layer, which includes tapered channels to transport the coolant from the intermediate chamber to the entrance of reservoir and triple-spike microstructures to drive the liquid out of the microchannels, spreading liquids across the reservoir by distributing meniscus with the assistance of triple-spike microstructures. To complete the operating cycle, the flow direction on the reservoir layer is reversed to that of the evaporator layer. The reservoir layer would be etched deeper than the other layers are to contain more coolant in the chamber. Because of the gradually narrowed width of the tapered channel and tailored microstructures at the end of the channels, coolant would move rapidly, refill the chamber, and finally touch the bottom of the coherent wick structure for the next cooling cycle. In the present study, a cooling test has been performed with three different kinds of polar fluids: deionized (DI) water, methanol, and isopropyl alcohol (IPA). As mentioned previously, the surface wettability is an important factor to transport the liquids through the microchannels. Even though methanol and IPA, which have relatively low surface energy, are completely wetted on the silicon surface of the channels, DI water is preferred as a coolant for TGP in this study because of water's larger latent heat of vaporization (2257 kJ/kg at 1 atm) [47]. In addition, the volatility of alcohol-type coolants may accelerate coolant loss to the atmosphere when the sealing between the main three layers has a leakage problem. Because using a partial wetting fluid (i.e., water) may reduce the propulsion of liquids due to the contact angle hysteresis, a few droplets of a wetting agent should be added to the coolant if the silicon surface was not handled with surface treatments to enhance the wettability.

2.2 Operating Principles for Heat Removal

The principal operating principle of the TGP to remove heat flux is to use the latent heat of vaporization of the coolant, similar to conventional heat pipes. One of main advantages of TGP is that the device can be directly integrated with ICs because the TGP is essentially fabricated from the silicon substrate. For example, the MEMS-based sensors and actuators can be fabricated directly onto the evaporator surface of the TGP, resulting in reduced fabrication cost and enhanced cooling efficiency due to the direct contacting interface. Figure 2.6 illustrates the design of the final device integrated with the chip directly contacting the evaporator surface. To integrate many other semiconductor chips with cooling devices, the material of the system must be thermally and electrically matched with semiconductor chips. Hence, the developed cooling device fabricated with all-silicon substrate is superior to the conventional cooling devices. Fig. 2.6(a) shows a device off-mode when the chip mounted on the evaporator stops operating or the chip temperature does not reach the critical temperature to operate the TGP. At this state, the coolant is collected in the reservoir and wets the evaporator surface by enhanced capillary actions from nanowires underneath the evaporator. Once the chip starts operation and increases the evaporator temperature, liquid in contact with the evaporator surface turns into a vapor by absorbing heat incoming from the hot chip, as seen in Fig. 2.6(b). After the vapor travels along the vapor microchannels, the vapor changes its phase from vapor to liquid again by transferring the heat to the heat sink connected to the end of the reservoir layer. Then, the condensed liquid moves back to the chamber through the liquid microchannels on the reservoir layer. This process continues during the operating cycles until the chip temperature has cooled down to the desired temperature. Thus, the chip can be operated safely without thermal damages such as thermal shock, vibration, or degradation.

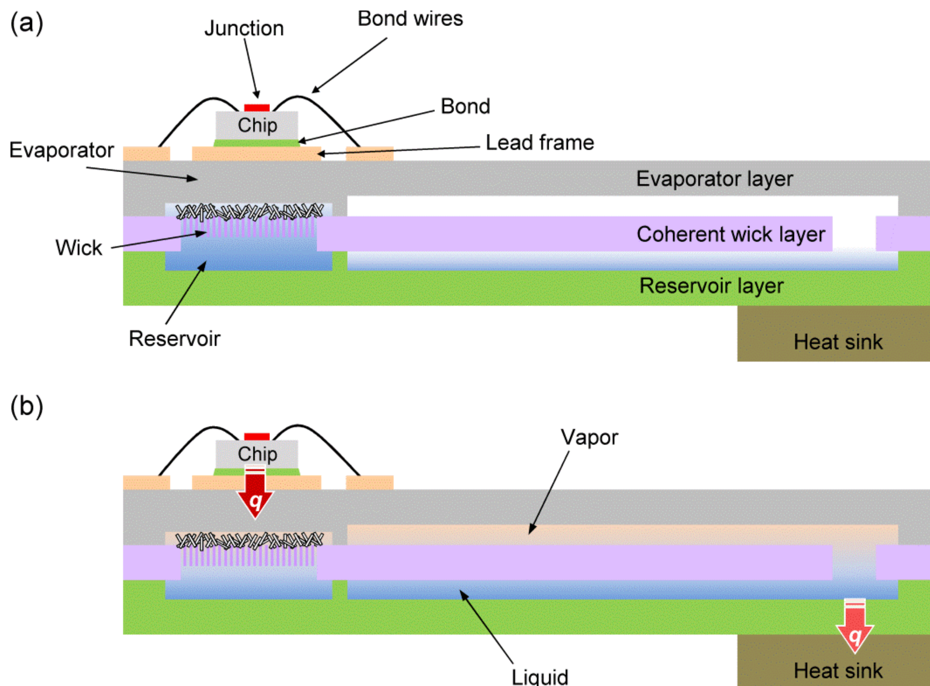

Figure 2.6 Scheme of cross-sectional view of the thermal ground plane with hot chip integrated on the evaporator layer for cooling purposes and internal fluid status at (a) device off-mode and (b) device on-mode.

2.2.1 Continuous Feeding of Coolant

The principal operating mechanism of the TGP is the phase-change of the coolant, which absorbs the tremendous heat flux from hot chips. To provide continuous cycles during the operation, vapors and liquids must be circulated smoothly along the microchannels. Therefore, the capillary forces on each layer play an important role in keeping operations reliable and without dryout limitations. As described in the previous section, each layer forming the entire TGP has an innovative design that overcomes the dryout limitation by using enhanced and extended capillary pressure. The tailored microstructures and nanomaterials were introduced to the evaporator-reservoir layers and the coherent wick layer, respectively. The design of the coherent wick layer was based on the device on-mode, whereas the design of the evaporator and reservoir layer was developed based on the device off-mode. The mass flow rate across the wick structure depends on a variety of parameters of the wick structure. To calculate a mass flow rate through the wick theoretically and to demonstrate the enhanced capillary action, a model based on hydrodynamic steady-state can be used in the present study. Assuming the flow surging up to pore ends by the primary capillary pressure is fully developed laminar steady-state with constant properties, the pressure drop across the interface (meniscus) can be given by the Young-Laplace equation as follows [48]:

$$\Delta P_{capillary} = P_{sat,v} - P_{sat,l} = \frac{2\sigma_l}{r}\cos\theta \tag{2.1}$$

where $P_{sat,v}$ and $P_{sat,l}$ are the saturated vapor and liquid pressure, respectively. σ_l is the surface tension of the liquid (i.e., free surface energy per unit area at the liquid-vapor interface), r is the radius of the pore, and θ is the contact angle at the liquid-vapor interface. Because the vertically aligned cylindrical microchannels in the wick are expected to be filled with liquid to maintain the stable interface, the pressure difference across the membrane is accounted for [15]:

$$P_2 - P_1 = \frac{2\sigma_l}{r}\cos\theta - \left(\frac{8\dot{q}}{\rho_l \varepsilon h_{fg}}\mu_l t_w\right)\left(\frac{1}{r^2}\right) \tag{2.2}$$

where P_1 and P_2 are the pressure of the bottom surface and upper surface of the wick, respectively; t_w is the thickness of wick membrane; $\dot{q}$ is the heat transfer rate per cross-sectional area of the wick; ρ_l is the density of fluid; ε is the porosity of the wick structure; h_{fg} is the latent heat of vaporization of the coolant; and μ_l is the dynamic viscosity of fluid. $\dot{q}$ is also related to latent heat and mass flow rate: $\dot{q} = \dot{m}h_{fg}/A$, where $\dot{m}$ is the mass flow rate of fluid through the wick. Physically, the first and second terms on the right side of Equation (2.2) represent the capillary pressure in the microscale channel and Hagen-Poiseuille pressure loss due to friction along the wall of the channel, respectively [48]. From Eq. (2.2), the volumetric flow rate across the coherent wick structure can be estimated theoretically. The contact angle can be experimentally determined by dropping the coolant onto the wick surface. Figure 2.7 shows the pressure drop across the wick layer versus the pore radius for different porosity (Fig. 2.7(a)) and thickness of wick membrane (Fig. 2.7(b)). From these preliminary results, pore radius of the

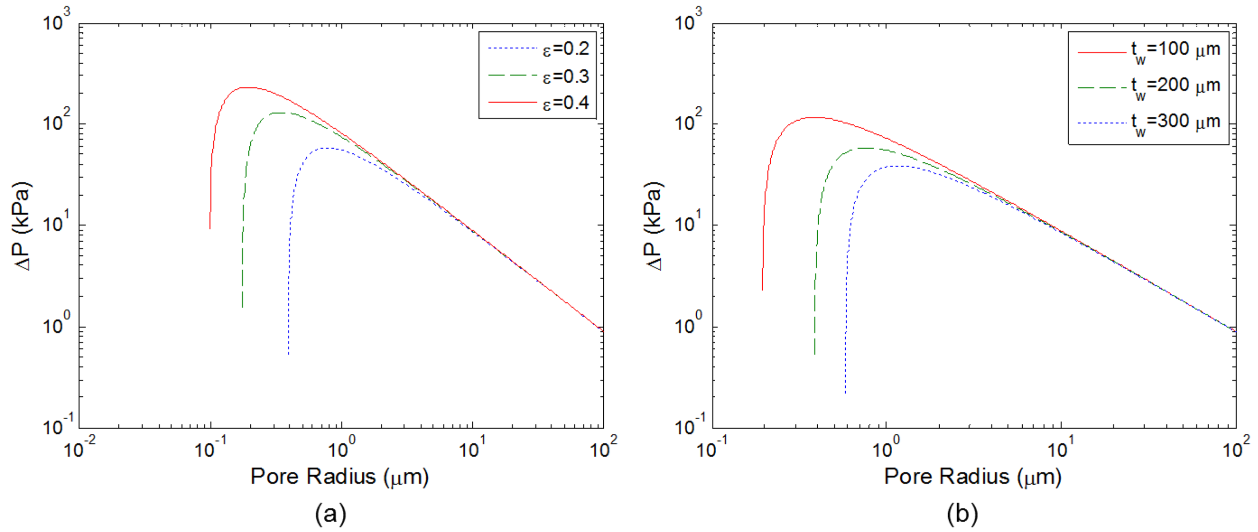

Figure 2.7 Pressure drop across the wick in response to the pore radius for (a) different porosity with constant heat flux of 40 W/cm^2 and wick membrane thickness of 200 μm and (b) different wick membrane thickness with constant heat flux of 40 W/cm^2 and porosity of 0.2.

coherent wick structure can be determined for fabrication once the desirable pressure drop across the wick is calculated from the two-phase analysis. It is noticeable that the effect of porosity and wick thickness becomes weaker at the region where the pore radius is larger than 6–7 μm. This means that the maximum pressure drop across the wick membrane significantly depends on pore radius rather than on the other parameters. The detailed fabrication strategy to adjust both porosity and pore size will be discussed in Chapter 4.

2.2.2 Thermal Barrier of Coherent Wick

When the chip mounted on the evaporator layer starts operating, waste heat will penetrate across the TGP device, initiating cooling of the chip. If the heat passes across the all layers of the TGP, the coolant in the reservoir will start boiling, resulting in a dryout limitation, as seen in Figure 2.8(a). Therefore, there must be a thermal barrier between the evaporator and reservoir layer to minimize the heat transfer rate coming to the reservoir when the device starts cooling. In other words, the coherent wick layer must have a low thermal conductivity (i.e., high thermal resistance) to initiate the first boiling near the evaporator surface, as seen in Fig. 2.8(b). Because the active height from the bottom of evaporator surface to the reservoir surface is less than 1 mm and coolant is stationary at the initial state, the heat conduction from the evaporator across the reservoir with thermal conductivities of the coolant, nanowires, and porous silicon wick becomes a main mechanism in this case. Therefore, the estimation of the nucleation location by the thermal network analysis with thermal properties is necessary to analyze the overall thermal-fluidic system. Assuming the one-dimensional heat conduction and steady-state, thermal resistances of each component have a combination of parallel and serial connection from the chip to the bottom of the reservoir. To estimate the thermal conductivity of ZnO nanowire and the porous silicon wick, microscale heat conduction theory will be discussed in Chapter 3.

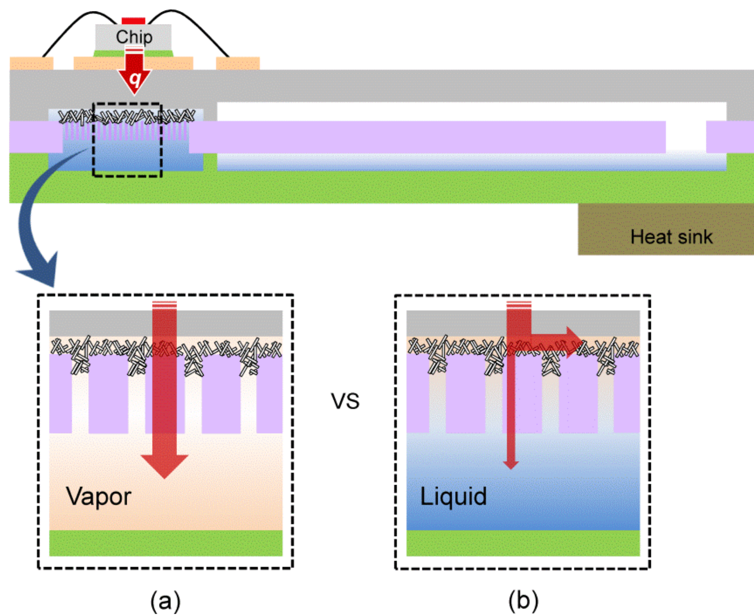

Figure 2.8 Schematic illustration of the role of the coherent wick layer as a thermal barrier to initiate boiling on the evaporator site: (a) dryout limitation when the thermal resistance of the wick is low and (b) desirable operation of the device when the thermal resistance of the wick is high enough.

2.2.3 Drop Propulsion in Microchannel

As described in section 2.1, the microchannels were designed with decreasing gap thickness to transport the coolant by itself to the liquid chamber. In general, the contact angle (θ) is the equilibrium angle between the liquid-vapor interface and the wetted solid surface when the fluid droplet is placed on a solid surface. For wetting fluids such as silicone oil or methanol, the contact angle goes to zero, whereas partial wetting fluids such as water have a finite angle with advancing and receding contact angles. An important hysteresis of so-called contact angle hysteresis is the difference between advancing and receding contact angles and acts to resist the sliding of partial wetting fluids on the surface [49-51]. Due to this hysteresis, although the vapor and liquid channels are tapered with decreasing gaps, the droplet of a partial wetting fluid may be pinned between two walls, causing the liquid to be stuck in the middle of the channel. Consequently, either surface treatments for solids or wetting agents for liquids play an important role in changing the wettability between the solid surface and liquid because a wetting fluid confined in a tapered channel can be self-transported toward the narrower end with the assistance of axial force arising from the different curvature pressures [52].

Chapter 3

Heat Transfer Analysis

3.1 Microscale Heat Conduction

3.1.1 Kinetic Theory of Thermal Transport

By definition, heat transfer is the energy flow involving the motion of heat carriers across a boundary under temperature difference. The well-known macroscopic Fourier's law for heat transfer is derived from averaging microscopic motions over a long period in a sufficiently large boundary. Fourier's law is useful for analyzing the average behavior of mass, energy, and momentum in macrosystems. However, such classical macroscopic averaging equations may no longer represent the motion of heat carriers in microscale or nanoscale domains because the conditions for average behavior are no longer valid [53]. Figure 3.1(a) depicts a wavepacket, which represents an energy carrier propagating through a system, traveling from left to right in the medium with the characteristic length L [54]. The wavepacket can be treated as a particle unless the characteristic length is comparable to the wavelength λ. However, the wavepacket collides with the boundary of the medium, impurities, or another wavepacket in the system with L, which is comparable or smaller than the mean free path Λ, as seen in Fig. 3.1(a) (e.g., thickness of a thin film or diameter of a nanowire). In this case, these numerous collisions impede the energy flow from left to right, resulting in "*classical size effect*" [53,54]. Therefore, heat conduction at the microscale is quite different from heat conduction at the macroscale, where the characteristic length is much larger than the mean free path.

The major difference between microscale and macroscale is that the effective thermal conductivity of microscale material is not equal to that of bulk material, even if they are the same material. In most cases, the values of thermal conductivities that can easily be found in textbooks or handbooks are valid for only bulk materials. Consequently, a microscopic approach is necessary to apply the effective thermal conductivity for microstructures, such as a thin film or nanowire. As a first step, the macroscopic Fourier's law must be modified based on kinetic theory to be useful at microscale domains. Considering a one-dimensional domain where the net heat flux flows from a hot surface to a cold surface as shown in Fig. 3.1(b), the net heat flux transported by heat carriers in x-direction is given by [53]:

$$\dot{q}_x = \frac{1}{2}\eta E v_x\bigg|_{x_0-\Lambda} - \frac{1}{2}\eta E v_x\bigg|_{x_0+\Lambda} \tag{3.1}$$

where η is the number of heat carriers per unit volume, E is the internal energy in J, and v_x

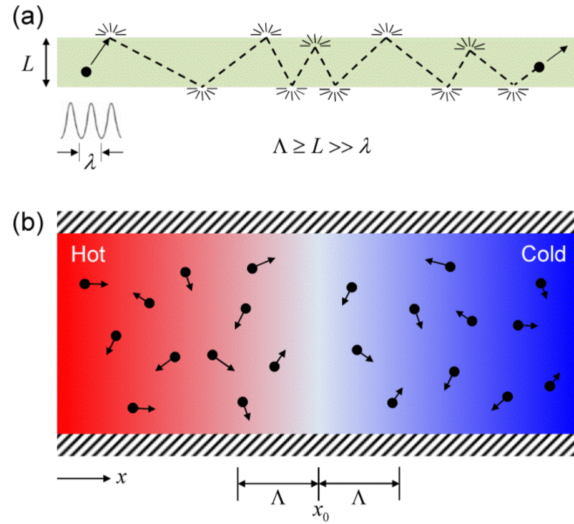

Figure 3.1 Schematic of (a) classical size effect when the characteristic length (L) is smaller than the mean free path (Λ) and larger than the wavelength (λ) and (b) control volume for a derivation of modified Fourier's law rested on kinetic theory.

is the x-component of the heat carriers' random velocity. By using a Taylor expansion and assuming that v_x is in an isotropic system and does not have preferred direction (i.e., ${v_x}^2 = (1/3)v^2$), Equation (3.1) can be expressed as follows:

$$\dot{q}_x = -\frac{v}{3}\Lambda\frac{dU}{dT}\frac{dT}{dx} \tag{3.2}$$

where v is the average velocity of the heat carriers, U is the internal energy density per unit volume in J/m^3, and dU/dT is the volumetric heat capacity C in J/m^3·K. Comparing Equation (3.2) with the classical Fourier's law ($\dot{q}_x = -k(dT/dx)$) leads to the thermal conductivity equation as follows:

$$k = \frac{1}{3}Cv\Lambda. \tag{3.3}$$

By treating C, v, and Λ in the above equation as lumped and frequency-independent quantities, most physical cases can be analyzed by calculating the thermal conductivity. However, because the particular nanostructures and energy carriers depend on frequency (ω) in real nature, kinetic theory can be expressed as an integral form to account for the frequency dependence [54]:

$$\begin{aligned} k &= \frac{1}{3}\int C(\omega,T)v(\omega)\Lambda_{eff}(\omega,T)d\omega \\ &= \frac{1}{3}\int \hbar\omega D(\omega)\frac{\partial f(\omega,T)}{\partial T}v(\omega)\Lambda_{eff}(\omega,T)d\omega \end{aligned} \tag{3.4}$$

where $\hbar$ is the reduced Planck constant, $D(\omega)$ is the density of state ($D(\omega) = D(\kappa) d\kappa / d\omega$), $f(\omega,T)$ is the Bose-Einstein distribution, and $\Lambda_{eff}(\omega,T)$ is the effective mean free path expressed by $\Lambda^{-1}{}_{eff}(\omega,T) = \Lambda^{-1}{}_{umkl}(\omega,T) + \Lambda^{-1}{}_{imp}(\omega) + \Lambda^{-1}{}_{bdy}$ based on the Matthiessen's rule. Each mean free path, due to phonon-phonon Umklapp scattering (denoted Λ_{umkl}), impurity scattering (denoted Λ_{imp}), and boundary scattering (denoted Λ_{bdy}), is also expressed with frequency (ω), temperature (T), and diameter of the sample (D) [55,56]:

$$\Lambda^{-1}{}_{umkl}(\omega,T) = \frac{B_1 \omega^2 T \exp(-B_2/T)}{v_g} \qquad \Lambda^{-1}{}_{imp}(\omega) = \frac{A_1 \omega^4}{v_g} \qquad \Lambda^{-1}{}_{bdy} = D^{-1} \tag{3.5}$$

where v_g is the group velocity and given by $v_g = d\omega / d\kappa$. To account for the frequency dependence, the Born-von Karman dispersion relation ($\omega = \omega_0 \sin(\pi\kappa / 2\kappa_D)$) can be used, where $\omega_0 = 2 v_s \kappa_D / \pi$ and $\kappa_D = (6\pi^2 \eta_{PUC})^{1/3}$ for the Debye cutoff wave vector, where v_s is the average sound velocity, and η_{PUC} is the number density of a primitive unit cell in m^{-3}. The coefficients A_1, B_1, and B_2 in Equation (3.5) depend on the material. By integrating Equation (3.4) with all parameters described above, more accurate thermal conductivity can be calculated for microscale and nanoscale samples.

3.1.2 Temperature Dependence of Thermal Conductivity

To validate the kinetic modeling, the silicon, which is well and widely investigated for both experimental value and theory, was tested with previously reported experimental data. Table 3.1 shows the values of physical parameters and fitting parameters determined by matching the modeling to experimental data for bulk silicon. Using these parameters, the thermal conductivities of silicon for different sample sizes were calculated in response to the temperature and compared with the experimentally measured data [57,58], as seen in Figure 3.2. As a result, the estimated thermal conductivity of silicon was able to reproduce the experimental results for bulk and nanowires in low temperature regions. In the same manner, fitting parameters for ZnO samples in Table 3.1 were carefully selected based on the effective sound velocity of ZnO [59] to match the calculated results to experimental data for a bulk sample. Figure 3.3(a) shows the calculated thermal conductivities of ZnO for bulk and nanowires from a temperature of 10 to 1000 K. As seen in the figure, the modeling shows good agreement with experimental data [60,61] for the bulk sample, and the significant reduction in thermal conductivity appears as the

Table 3.1 Parameter values determined by a combination of theory and fitting thermal conductivities with respect to temperature for bulk silicon and zinc oxide (ZnO) samples.

	η_{PUC} (m^{-3})	v_s (m/s)	A_1 (s^3)	B_1 (s/K)	B_2 (K)
Silicon	2.5e28	5880 [54]	2.4e-45	1.7e-19	210
ZnO	2.1e28	3186 [59]	8.0e-44	2.6e-19	100

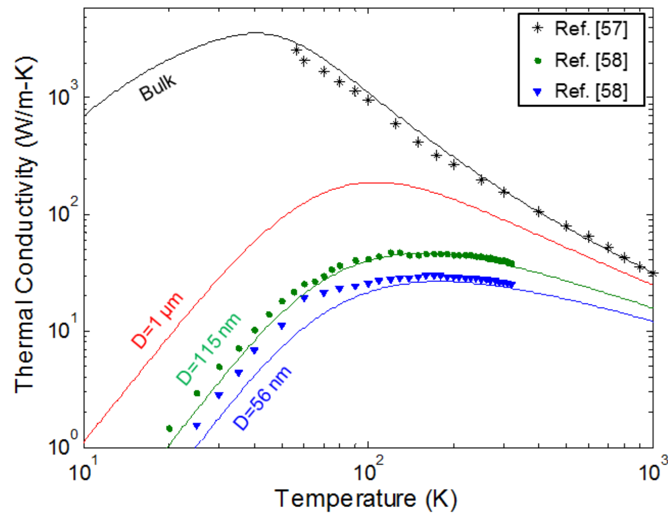

Figure 3.2 Calculated thermal conductivities for silicon from kinetic theory and comparison with experimentally measured thermal conductivities for a different diameter of silicon nanowires.

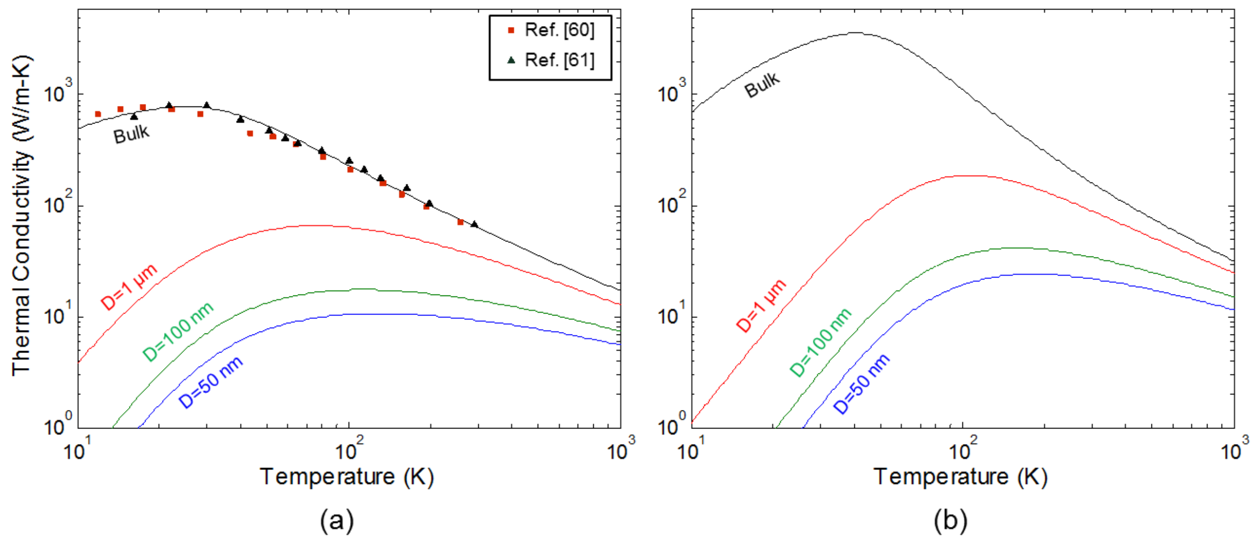

Figure 3.3 Calculated thermal conductivities of (a) zinc oxide (ZnO) with experimental results for a bulk sample and nanowires of different diameters and (b) silicon of the same diameter as ZnO for comparison purpose. The result shows that the thermal conductivities of ZnO are lower than those of silicon for all temperature ranges.

size of the sample is reduced due to the phonon scattering effects, as expected. To demonstrate the lower thermal conductivity of ZnO nanowire used in the present study, it was compared with the thermal conductivities of silicon nanowire of the same dimension as the samples have, as seen in Fig. 3.3(b). For example, the ZnO nanowire with a 100 nm diameter has a thermal conductivity of 12.8 W/m·K at 100℃, which is an estimated temperature at the evaporator surface at initial state, whereas the silicon nanowire has 30.4 W/m·K at the same temperature. Considering the operating temperature (90–200℃) of the TGP, ZnO nanowires have approximately a two times lower thermal conductivity than silicon nanowires that may help to

analyze the thermal system and provide a critical design parameter to determine the other design parameters, such as channel height, width, or volume of the reservoir for the device fabrication.

To analyze the thermal conductivity of the evaporator layer with respect to the layer thickness, Equation (3.3) can be used with the Debye approximation, which can be suitable for the thermal conductivity dominated by acoustic phonons [53,54]. Because the heat generation passes in a perpendicular direction to an evaporator surface, the thermal conductivity and corresponding thermal resistance are the function of evaporator thickness. For simplicity, the specific heat and group velocity in the evaporator layer are assumed to be equal to those in bulk. According to the Debye approximation, the volumetric heat capacity C is given by:

$$C = \frac{3\eta_{PUC} k_B}{1 + \frac{5}{4\pi^4}\left(\frac{\theta_D}{T}\right)^3} \tag{3.6}$$

where k_B is the Boltzmann constant in J/K, θ_D is the Debye temperature given by $\theta_D = \hbar\omega_D / k_B$, where $\omega_D = v_s \kappa_D$ (Debye frequency). Equation (3.3) needs the effective mean free path to calculate the thermal conductivity of the evaporator layer. For heat flow perpendicular to a thin film with thickness L, the mean free path due to the boundary scattering Λ_{bdy} is expressed by the Rosseland diffusion approximation [54]:

$$\Lambda_{bdy} = \frac{\frac{3}{4}L}{\alpha_1^{-1} + \alpha_2^{-1} - 1} \tag{3.7}$$

where α_1 and α_2 are the absorptivity of two parallel surfaces (i.e., top and bottom surface of the evaporator layer). These absorptivities can be approximated as unity at both sides of the evaporator layer. Therefore, the thermal conductivity of the evaporator layer with respect to the layer thickness can be obtained by applying the volumetric heat capacity and effective mean free path Λ_{eff} that can be calculated by the Matthiessen's rule. Corresponding conduction thermal resistance R is calculated as follows:

$$R = \frac{L}{kA} \tag{3.8}$$

where A is the contact area for heat transfer in the TGP. Figure 3.4 shows the calculated thermal conductivity, thermal resistance, and effective mean free path with respect to the thickness of the evaporator layer. It is noticeable that the thermal conductivity and effective mean free path for the thick film region (i.e., $L >> \Lambda_{bulk}$) become independent of the thickness of the evaporator layer because the diffusion of heat carriers dominates the thermal resistance. In this "diffusive" regime, the thermal resistance is proportional to the thickness of the evaporator layer. However, thermal conductivity is significantly dominated by the thickness of the evaporator layer for thin film region (i.e., $L << \Lambda_{bulk}$), which is also known as the "ballistic"

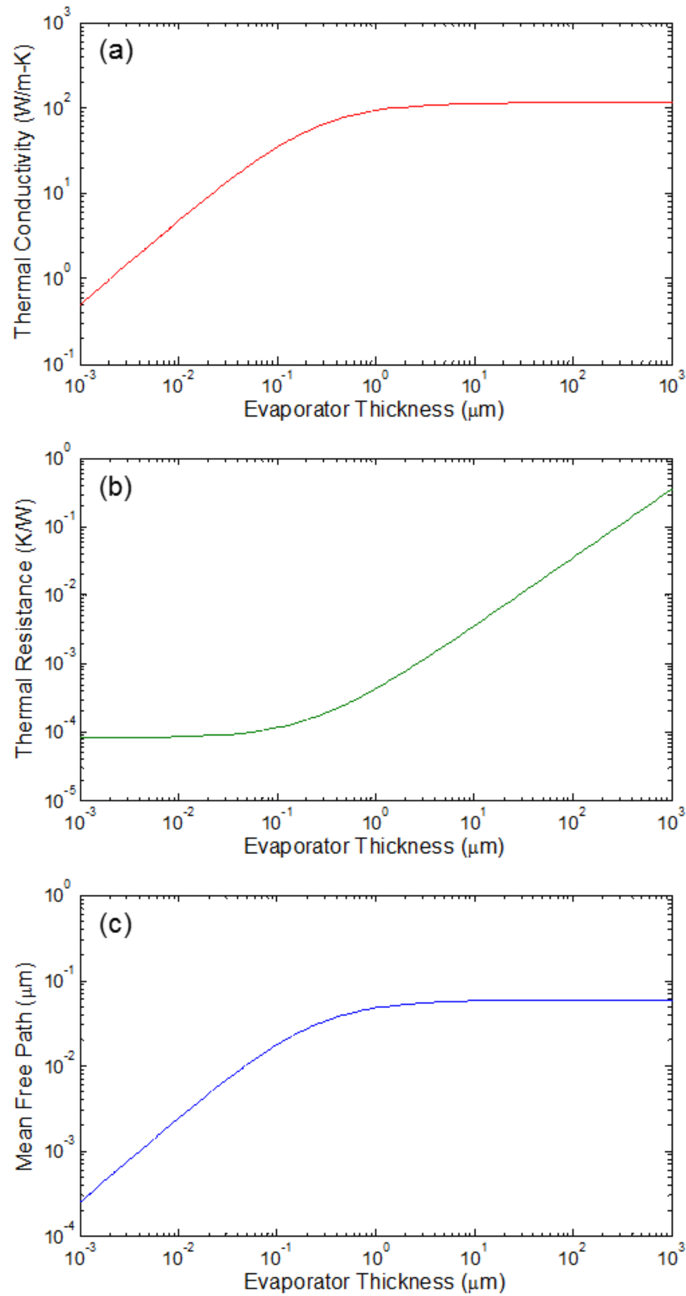

Figure 3.4 Theoretical analysis of the (a) thermal conductivity, (b) thermal resistance, and (c) effective mean free path of the evaporator layer at 100℃ with respect to the thickness. Active cooling area is 5×5 mm^2.

regime because the effective mean free path is dominated by the phonon scattering as the thickness is decreased [54]. Considering the estimated evaporator temperature of 100℃ at the initial state of operation and a layer thickness of around 500 μm, which is the general thickness of a 4-inch silicon wafer where the evaporator will be fabricated, thermal conductivity and thermal resistance for a 5×5 mm^2 heat transfer area are calculated as 115.3 W/m·K and 0.1739 K/W, respectively.

To predict the electrical, thermal, and optical properties of porous and inhomogeneous media, various theoretical models have been extensively developed [62-65]. For the prediction of the thermal conductivity of a coherent porous silicon wick structure, several models have been adopted and compared with respect to the porosity of the wick. The most well-known effective medium theory is the Maxwell Garnett approximation, which is given by [62]:

$$k_r = \frac{1-\frac{2}{3}[k]\phi}{1+\frac{1}{3}[k]\phi} \tag{3.9}$$

where

$$[k] = \frac{3(k_m - k_i)}{2k_m + k_i} \tag{3.10}$$

is defined as intrinsic thermal conductivity [64]. In Equation (3.9), ϕ is the porosity, which is the volume fraction of pores, and k_r is the relative thermal conductivity expressed by $k_r = k_{eff}/k_m$, where k_{eff} is the effective thermal conductivity of porous media k_{PSi}. In Equation (3.10), k_m and k_i are the thermal conductivity of the matrix phase (i.e., silicon) and of the inclusion phase (i.e., air or coolant), respectively. Thus, the effective thermal conductivity k_{eff} is in the range from k_m (when ϕ=0) to k_i (when ϕ=1). While the Maxwell Garnett approximation rests on an effective field concept, the self-consistent approximation given by Equation (3.11) [63] was based on an effective medium concept considering the inclusion as embedded in a homogeneous matrix [66]:

$$k_r = \frac{\beta + \sqrt{\beta^2 + 8k_m k_i}}{4k_m} \tag{3.11}$$

where $\beta = (2-3\phi)k_m + (3\phi - 1)k_i$. It is noticeable that the above approximation has a critical porosity of around 0.67 where the thermal conductivity becomes zero, whereas the Maxwell Garnett approximation has the finite thermal conductivities from porosity of 1 up to 0. To further account for porosity dependence, the second-order approximation also developed as follows [64]:

$$k_r = 1 - [k]\phi + \left([k]-1\right)\phi^2. \tag{3.12}$$

By treating the pores as non-conductive gases (i.e., k_i=0), a modified model with exponential form has also developed as follows [65]:

$$k_r = \exp\left(\frac{-B\phi}{1-\phi}\right) \tag{3.13}$$

where B is related intrinsic thermal conductivity $[k]$ and may set as 1.5 from Eq. (3.10).

Furthermore, if the connection between the matrix phase and the inclusion phase is simply approximated as a parallel relationship, simple effective medium theory equation can be explicitly expressed as follows:

$$k_r = (1-\phi) + \frac{k_i}{k_m}\phi \, . \tag{3.14}$$

Figure 3.5 shows the comparison of the above five models to estimate the effective thermal conductivity of a porous silicon wick structure in response to the porosity. Note that the effective thermal conductivity obviously depends on the thermal conductivity of bulk silicon, which also depends on the temperature, as already discussed. Without a doubt, direct measurement of thermal conductivity of porous silicon wick using the laser-flash [67] or 3-omega techniques [68] is the best method to obtain correct values. However, considering the necessary process time, cost for experimental setting, and practical purposes, the models based on the effective medium theory may provide estimated values with significantly reduced time and cost. For example, if the coherent porous silicon wick has a porosity of 0.2 and thickness of 200 μm, the effective thermal conductivity of the wick structure becomes 82.66 ± 4.98 W/m·K at 100°C, because the ratio of bulk thermal conductivity (113.7 W/m·K from kinetic theory) to the porous wick thermal conductivity is around 0.69–0.8, as seen in Fig. 3.5. Because the thermal conductivities of all components on three layers in TGP were estimated using the kinetic theory and effective medium theory, the thermal resistance network analysis can be performed to understand the thermal behavior in the TGP and to determine the specific values for design parameters before device fabrication. Once the dimensions of the TGP are specified based on the thermal resistance network analysis, a two-phase flow analysis can be also conducted to obtain the fluidic and thermal properties, such as operating pressure, temperature, vapor-liquid interface radius of curvature, and rate of bubble formation.

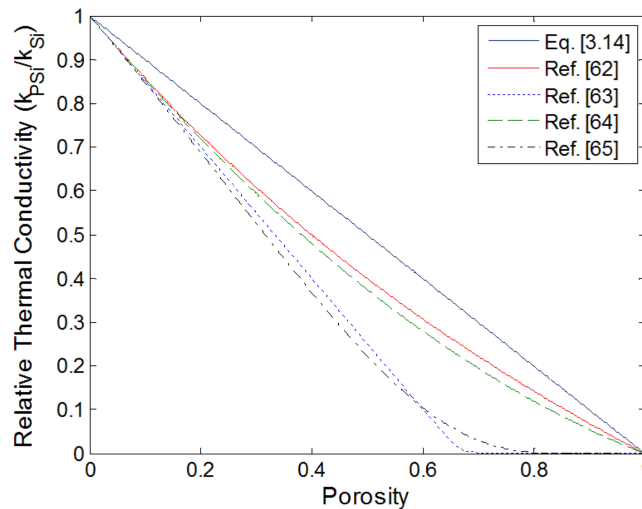

Figure 3.5 Comparison of theoretical models to predict the effective thermal conductivity of porous silicon with respect to the porosity.

3.2 Thermodynamic Analysis of Closed Loop System

3.2.1 Thermal Resistance Network of System

The heat analysis of the TGP begins with the junction of the chip mounted on the evaporator layer. Once the junction of the chip generates heat, the heat transfers through the chip carrier surrounding the chip and the TGP layers. In the system, the operating chip would be cooled down by two levels. One is the chip package level, which serves for first-level cooling, and the other is the board level as second-level cooling. In essence, the main operating chips are packaged by the chip carrier or dual in-line package for the purposes of electric connection through the leads and protection of the die from contamination such as dust, vibration, humidity, and radiation. Figure 3.6(a) shows the MEMS die mounted on a chip carrier where the lead frame is bonded to electrodes with highly conductive bonding wires (typically gold or aluminum). As a first transport, the heat generated from the junction spreads throughout the silicon chip and is transferred across the chip thickness using conduction, as shown in Fig. 3.6(b). It is clear that heat spreads from the junction to the chip body in all directions (i.e., three-dimensional directions). However, for simplicity, it can be approximated as a one-dimensional direction by introducing a constriction thermal resistance to the network analysis [69,70]. For a junction with a diameter of d on the die, the constriction thermal resistance is given by:

$$R_{constriction} = \frac{1}{\sqrt{\pi} dk} \tag{3.15}$$

where k is the thermal conductivity of the chip material. Given the low thermal conductivity of the inert air between the case and chip, heat transfer through the plastic case can be negligible. Therefore, the thermal resistance network for the chip package level cooling can be simplified, as shown in Fig. 3.6(c). When the chip package is integrated on the TGP, heat spreads further into the evaporator surface, as depicted in Fig. 3.6(b). Considering a relatively small heat transfer area along the in-plane direction due to the several-hundred-micron thickness of each TGP layer, the thermal resistance along the in-plane direction would be relatively large so that heat transfer can be approximated as one-dimension, although heat spreads in three-dimensional directions. Therefore, the thermal resistance network for the combined level cooling before the operation of the TGP reaches steady-state can be presented, as shown in Fig. 3.6(c). As seen in the figure, the temperature of the evaporator is determined by the first chip package level's cooling, whereas the temperature of the reservoir is affected by internal elements in the TGP, including coolant, nanowires, and porous silicon. Because the coolant/nanowires and coolant/porous silicon are considered to be parallel connections, the overall thermal resistance of the TGP is given by:

$$R_{TGP} = R_{evap} + \frac{1}{1/R_{cool-NWs} + 1/R_{NWs}} + \frac{1}{1/R_{cool-PSi} + 1/R_{PSi}} + R_{cool-res} \tag{3.16}$$

where $R_i = L_i / k_i A_i$. Subscripts NWs and PSi refer to the nanowires and porous silicon, respectively. Note that the liquid is also considered a conductive solid medium having a specific

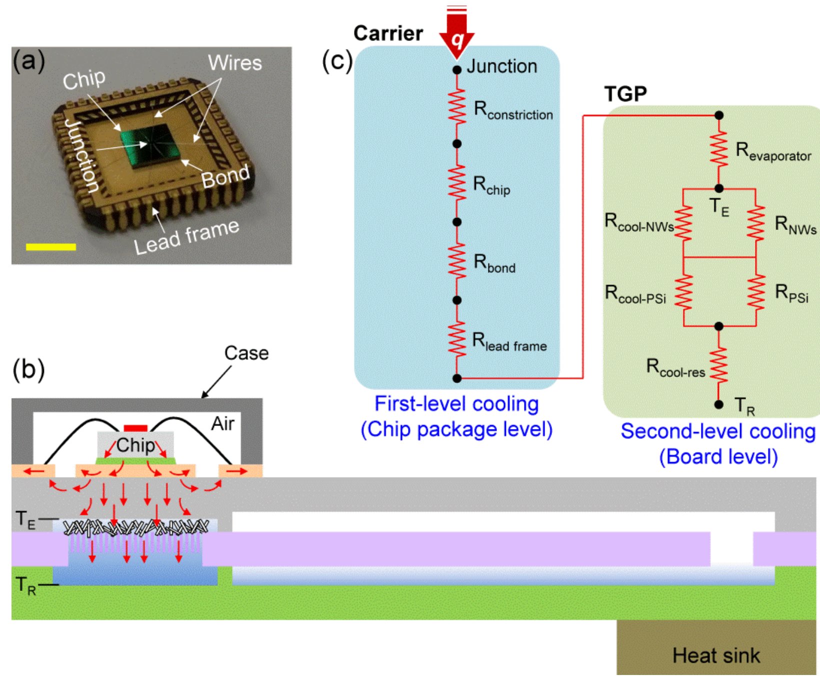

Figure 3.6 (a) Image of the MEMS chip mounted on a chip carrier for first-level cooling, (b) schematic illustration of the chip integrated on a thermal ground plane for second-level cooling, and (c) thermal resistance network of the combined devices for simultaneous cooling. Scale bar: (a) 5 mm.

thermal conductivity because free and forced convection arising from the liquid can be negligible due to a small enough micron gap between each layer. Considering the reservoir temperature T_R must be below the boiling point of the coolant to prevent the initial dryout limitation, the maximum temperature of junction to be handled by the TGP can be calculated using Equation (3.16) with thermal resistances of each component previously obtained by kinetic theory and effective medium theory. Assuming that a MEMS device mounted on the TGP is dissipating 10 W of power in a chip, which is the general characteristic of microprocessors [71], thermal resistance analysis can be performed with corresponding values of thermal conductivities, length, and heat transfer area (see Table 3.2 for example). Note that the heat transfer area for ZnO nanowires underneath the evaporator layer depends on the number of nanowires contacting the bottom surface of the evaporator layer. In Table 3.2, δ is the ratio of the contacting area of nanowires to the heat transfer area of the evaporator surface. The value of δ is approximated between 0.01–0.02 because the tip area of the nanowire is extremely small and nanowires would be grown in all directions rather than vertical only. The heat transfer area of the porous silicon wick is also complementary to porosity ϕ (i.e., 1-ϕ). As mentioned earlier, because the temperature of the reservoir bottom must be below boiling point of coolant to overcome the initial dryout problem when the chip initiates operation, heat must be removed by increasing the depth of the reservoir chamber. As the 4-inch wafer will be used for fabrication of the TGP, the maximum depth of the reservoir would be 500 μm. As a result, the maximum temperature of the top surface of the evaporator layer is 402.4℃ for a 10 W chip where the TGP can initiate the steady two-phase flow operation without an initial dryout problem.

Table 3.2 Thermal conductivities, lengths, and heat transfer area of each component participating heat conduction across the thermal ground plane layers from top of the junction to bottom of the reservoir.

	k (W/m·K)	L (μm)	A (heat transfer area)
Junction	-	-	d =500 μm
Silicon chip	115.3	500	5 mm×5 mm
Bonding paste	25	10	5 mm×5 mm
Copper lead	401	254	5 mm×5 mm
Evaporator	115.3	490	5 mm×5 mm
ZnO nanowires	12.8	10	(5 mm×5 mm)δ
Coolant (water)	0.679	-	5 mm×5 mm
Porous silicon	82.66	200	(5 mm×5 mm)(1-ϕ)

3.2.2 Thermodynamic Cycle during Operation

When the TGP starts the cooling performance using two-phase flow, the device reaches the steady-state as long as the chip mounted on the evaporator provides the uniform heat flux. The steady-state process of the TGP can be described on thermodynamic diagrams, as shown in Figure 3.7. The thermodynamic process for each point can be described as follows:

⑧→①: The liquid turns into a vapor as it absorbs the high heat flux from the chip mounted on the evaporator layer and becomes a superheated vapor leaving the evaporator site toward the condenser. The process may be an isothermal process because the coolant is assumed to remove constant heat flux, maintaining a uniform temperature during the phase-change.
①→②: The superheated vapor moves toward the middle of the vapor channel connected to the condenser part. During this movement, the temperature and pressure drop slightly due to the convective heat transfer to the atmosphere and the friction loss in the vapor channel, respectively. In case of an adiabatic layer, the temperature will not drop because of the isothermal process.
②→③: During this process, the superheated vapor starts to condense by lowering the pressure, which causes the pressure gradient in the vapor channel and provides the driving forces for transport to the condenser section. At the condenser, the superheated vapor turns into the saturation condition.
③→④: At the condenser, phase-change occurs from the saturated vapor, and the change will continue until it reaches the saturated liquid. The saturated liquid moves along the liquid channel on the reservoir layer in the TGP by a combination of inertial force due to the vapor and capillary forces that arise from the tapered width of the channel. The process may occur in isobaric and isothermal conditions because the overall distance for the process is relatively shorter than other processes, resulting in unnoticeable gradient in temperature and pressure across the condenser.

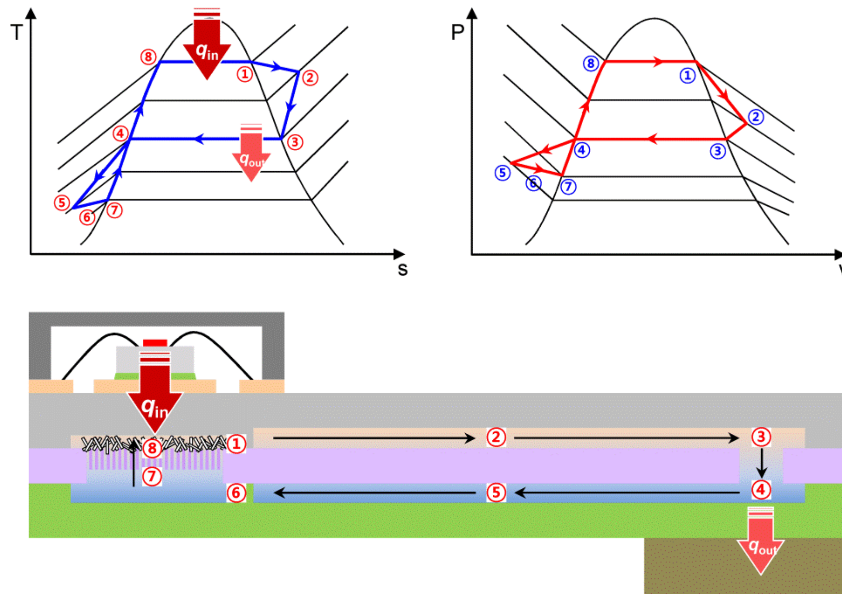

Figure 3.7 T (temperature)-s (specific entropy) and P (pressure)-v (specific volume) thermodynamic diagram during the operation in the thermal ground plane with a schematic illustration for each state point in the device.

④→⑤: The saturated liquid will further lose the latent heat and become a sub-cooled liquid near the middle of the liquid channel. The pressure also drops due to frictional loss in the liquid channel.

⑤→⑥: As the sub-cooled liquid approaches the reservoir chamber due to the lower pressure in the reservoir, the temperature of the liquid will increase because it is near the active heat removal site where the high heat flux enters the evaporator.

⑥→⑦: The sub-cooled liquid continues to move into the reservoir chamber due to minimum pressure value at point 7, resulting in high pressure of vapor-liquid interface across the wick structure. The liquid then has the saturation condition to prepare the phase-change underneath the evaporator surface.

⑦→⑧: The saturated liquid underneath the wick structure will surge up along the saturated liquid line and spread across the entire wick surface due to the enhanced capillary effect by the nanowires on the wick structure. Then, the saturated liquid will touch the evaporator surface and remove the heat flux by changing the phase from liquid to vapor and continue the cycle.

3.3 Liquid-Vapor Phase Change

3.3.1 Analysis for Fluidic and Thermal Properties

To estimate the fluidic and thermal properties in the designed TGP, heat transfer and fluid dynamic models can be used with the TGP geometry, as seen in Figure 3.8 regarding wick characteristics and working fluid properties. If the vapor flow is considered to be a fully developed laminar flow in channels, the pressure drop along the vapor channel is given by the Darcy-Weisbach equation [48,72]:

$$P_1 - P_3 = \frac{64}{\psi \operatorname{Re}_v}\left(\frac{L_{eff}}{D_v}\right)\frac{\rho_v V_v^{\,2}}{2} \tag{3.17}$$

where

$$\operatorname{Re}_v = \frac{\rho_v V_v D_v}{\mu_v}, \quad D_v = \frac{4A_v}{P_v}, \quad A_v = \xi H_v W_v$$

and ψ depends on the aspect ratio of width and height of a rectangular cross section, L_{eff} is the effective length, and ξ is the number of channels. The pressure drop across the condenser is

$$P_4 - P_3 = \rho_l g h \tag{3.18}$$

where g is the gravity and h is the height difference between the upper and lower surface of the condenser part. Because h is in micron scale, the pressure gradient between points 3 and 4 can be ignored, resulting in $P_4 \approx P_3$. The flow in the liquid channel is assumed to obey Darcy's law and is defined as follows:

$$P_4 - P_7 = \frac{\mu_l L_{eff} \dot{m}}{\zeta\, \rho_l A_l} = \frac{12 \mu_l L_{eff} \dot{m}}{\xi H_l^{\,3} W_l \rho_l} \tag{3.19}$$

where

$$A_l = \xi H_l W_l$$

and $\dot{m}$ is the mass flow rate of coolant across the wick and ζ is the a permeability given by $\zeta = H_v^{\,2}/12$ for the channel with a rectangular cross section [73]. In the evaporator and reservoir, the Young-Laplace equation from Eq. (2.2) can be used again:

$$P_1 - P_7 = \frac{2\sigma_l}{r}\cos\theta - \left(\frac{8\dot{q}}{\rho_l \varepsilon h_{fg}}\mu_l t_w\right)\left(\frac{1}{r^2}\right). \tag{3.20}$$

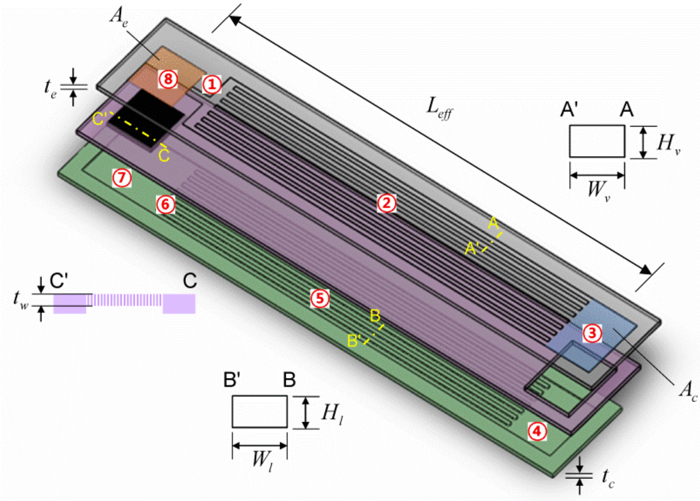

Figure 3.8 Schematic illustration of the overall thermal ground plane device with geometry and noticeable points for the thermal system analysis.

The heat flux across the evaporator surface and condenser surface can be expressed as follows:

$$\frac{\dot{Q}}{A_e} = k_e \left(\frac{T_{w,e} - T_{sat,e}}{t_e} \right), \quad \frac{\dot{Q}}{A_c} = k_c \left(\frac{T_{w,c} - T_{sat,c}}{t_c} \right) \tag{3.21}$$

where $T_{w,e}$ and $T_{w,c}$ are the wall temperature of the evaporator and condenser surface, respectively. $T_{sat,e} = T_{sat}(P_1)$, $T_{sat,c} = T_{sat}(P_3)$, A_e is the heat transfer area of the evaporator site, A_c is the heat transfer area of the condenser section, and $T_{sat,e}$ is calculated by iteratively solving the following equation [74]:

$$P_1 = P_{sat}(T_{sat,e}) \exp\left(\frac{-2\sigma_l}{r \rho_l R T_{sat,e}} \right). \tag{3.22}$$

Combining Equations (3.17)–(3.20) provides the final relation for the system:

$$\frac{2\sigma_l}{r}\cos\theta - \left(\frac{8\dot{q}}{\rho_l \varepsilon h_{fg}} \mu_l t_w \right)\left(\frac{1}{r^2} \right) - \frac{64}{\psi \mathrm{Re}_v}\left(\frac{L_{eff}}{D_v} \right)\frac{\rho_v V_v^2}{2} = \frac{12 \mu_l L_{eff} \dot{m}}{\xi H_l^3 W_l \rho_l}. \tag{3.23}$$

Once r and $P_3 = P_{sat}(T_{sat,c})$ are determined by Equation (3.23) and (3.21), respectively, $P_1 = P_{sat}(T_{sat,e})$ can be calculated by Eq. (3.17). Inserting these results to Equation (3.22) and iterating until the difference between P_1 obtained by Eq. (3.17) and (3.22) has a minimum value, give the final value of $T_{w,e}$ from Eq. (3.21). The specific dimensions used for the above calculations are listed in Table. 3.3. Note that the primary purpose of thermal and fluidic analysis with these dimensions is to demonstrate the reliable operation of the TGP when the real device is

Table 3.3 Dimensions of the thermal ground plane device used for thermal and fluidic analysis.

Parameters	Value	Unit
Effective length, L_{eff}	48	mm
Height of vapor channel, H_v	250	μm
Width of vapor channel, W_v	500	μm
Height of liquid channel, H_l	250	μm
Width of liquid channel, W_l	500	μm
Area of evaporator, A_e	5×5	mm^2
Area of condenser, A_c	5×6.8	mm^2
Thickness of evaporator, t_e	490	μm
Thickness of condenser, t_c	250	μm
Thickness of coherent wick, t_w	200	μm
Correction factor for noncircular duct, ψ	1.03	-
Number of channel, ξ	8	-
Wick porosity, ε	0.2	-

Table 3.4 Calculated thermal and fluidic properties in the thermal ground plane based on the designed specifications.

Results	Value	Unit
Wall temperature of evaporator, $T_{w,e}$	167.06	℃
Saturation temperature of evaporator, $T_{sat,e}$	165.36	℃
Saturation temperature of condenser, $T_{sat,c}$	24.36	℃
Exit pressure of evaporator, P_1	704.76	kPa
Pressure at condenser, P_3	704.63	kPa
Pressure at reservoir, P_7	672.08	kPa
Interface radius of curvature at wick, r	2.79	μm
Mass flow rate across wick, $\dot{m}$	4.84e-6	kg/s

fabricated with the same specification. Thus, it will provide the robust design tool if the specifications need to be modified based on the electronic platform for chip packaging. Table 3.4 shows the estimated thermal and fluidic properties during the cooling performance in the TGP when the power of 10 W is directly dissipating on the evaporator surface. As a result, because the wall temperature at the evaporator is slightly higher than is the saturation temperature (165.36°C) at the exit pressure (704.76 kPa), the vapor would become a superheated vapor before moving toward the vapor channel. This explanation is reasonably matched with the thermodynamic diagram in Fig. 3.7. It is also noticeable that at least 2.79 μm radius of pores or less is essential to maintain the pressure gradient across the coherent wick structure, which will be adopted as a maximum pore size for the fabrication of the coherent porous silicon wick later.

3.3.2 Two-Phase Nucleation Analysis

To further understand phase-change phenomena underneath the evaporator surface, an analysis of the kinetics of the nucleation process was performed using two-phase models. During the operation, nucleation is expected on the middle of the coolant or evaporator surface. In general, nucleation can be divided to homogeneous and heterogeneous nucleation, depending on the nucleation sites. Heterogeneous nucleation starts on the preferential solid surfaces in the system, whereas homogenous nucleation appears away from the surfaces, which makes it more difficult to create an interface in the interior of a single phase. To distinguish between the two cases, the relation between the rate of embryo formation J and the system properties given by the following equation can be usefully used [74-76]:

$$J = \left(\frac{\rho_l}{m}\right)\left(\frac{3\sigma}{\pi m}\right)^{1/2} \exp\left[\frac{-16\pi\sigma^3}{3k_B T_l \left[\varphi P_{sat}(T_l) - P_l\right]^2}\right] \tag{3.24}$$

where

$$\varphi = \exp\left\{\frac{\left[P_l - P_{sat}(T_l)\right]}{\rho_l R T_l}\right\}.$$

Because J is the rate at which bubbles of critical size are formed in steady-state, the increase in J means the probability of the formation of bubbles greater than the critical size will also increase [74]. Therefore, the kinetic limit of superheat, which is defined as a temperature range below which homogeneous nucleation does not start, and above which it definitely occurs, can be determined using the above equation [74]. Using the values in Table 3.4, which obtained thermal and fluidic analysis, the rate of bubble formation was calculated for different liquid temperatures underneath the evaporator surface, as shown in Figure 3.9. Although an exact threshold value of J for homogeneous nucleation is not known for the kinetic limit of superheat, $J = 10^{12}$ m^{-3}s^{-1} is in good agreement with experimental data [74,77]. According to Fig. 3.9, the corresponding liquid temperature is approximately 306.7°C, which is the minimum liquid temperature underneath the evaporator surface to cause the homogeneous nucleation at given pressure. Hence, only heterogeneous nucleation on the evaporator surface is expected to

occur during the operation of the TGP. This also means that all bubbles smaller than the critical size are likely to completely collapse, which suppresses homogeneous nucleation in the TGP.

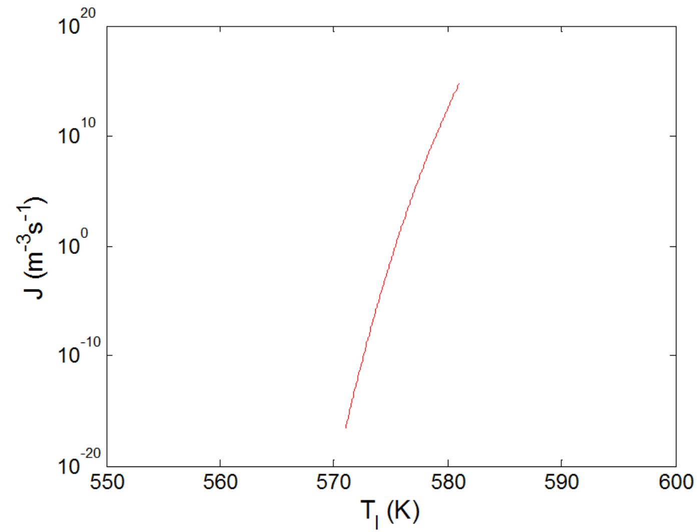

Figure 3.9 Computed rate of bubble formation with different liquid temperatures for homogeneous nucleation based on the kinetic limit of superheat.

Chapter 4

Device Fabrication

4.1 Evaporator and Reservoir Fabrication by Top-Down Process

4.1.1 Principles of Deep Reactive-Ion Etching

The basic etching techniques used in microfabrication can be categorized as wet chemical etching and dry etching, based on the type of etchant. Hydrofluoric (HF) acid, potassium hydroxide (KOH), or tetramethylammonium hydroxide (TMAH) are the common wet chemicals used to etch SiO_2 layer or bulk silicon. The etching can be performed by immersing the samples in the chemical solution. Because the etching rate by wet chemicals depends on the temperature, careful monitoring of the reaction temperature is most important to etch for the desirable thickness. In general, wet chemical etching tends to etch the targets in all directions, which is an isotropic process forming the “undercut” under the resist. This etch bias becomes a serious problem in the microfabrication process where a vertical sidewall is needed [78]. Although the KOH and TMAH provide anisotropic silicon etching, they are highly dominated by the silicon orientation and extremely sensitive to temperature. Consequently, dry etching techniques are now widely used in the microfabrication process to avoid the undercut problem. First, a common dry etching technique is performed with plasma etching using radio frequency (RF) excitation, which frequency is typically 13.56 MHz, to ionize etchant gases in a vacuum chamber. In the vacuum chamber, the wafer can be placed on a lower plate among parallel two electrode plates, and the RF excites free radicals in the source gases to create the plasma reacting with the wafer surface for anisotropic etching. The type of source gases can be selected based on the target materials to be etched. A second dry etching technique is sputter etching and ion milling, which are purely physical processes that use energetic gas ions, such as argon ions, to maximize the ion bombardment [79]. When these highly energetic ions physically hit the atoms on the wafer surface, directional and anisotropic etching occurs. However, these techniques are not typically used these days because there are several accompanying problems during the process, such as redeposition of materials, ion path distortion, or lattice damage [79]. To overcome these problems, reactive-ion etching (RIE), which combines plasma and sputter etching, has been developed for highly anisotropic etching. Because the two different etching processes are included in RIE, a combination of chemical reactions and physical bombardment achieves the etching. By using an asymmetrical connection between parallel plates in the vacuum chamber, the high voltage (in the range of 100–700 V) required to accelerate energetic ions from the plasma to the wafer can be generated, as seen in Figure 4.1(a) [78]. The upper electrode is grounded in the RIE system, whereas the lower electrode is grounded in the plasma etching. The etching is generally run in the range of 10–100 mTorr.

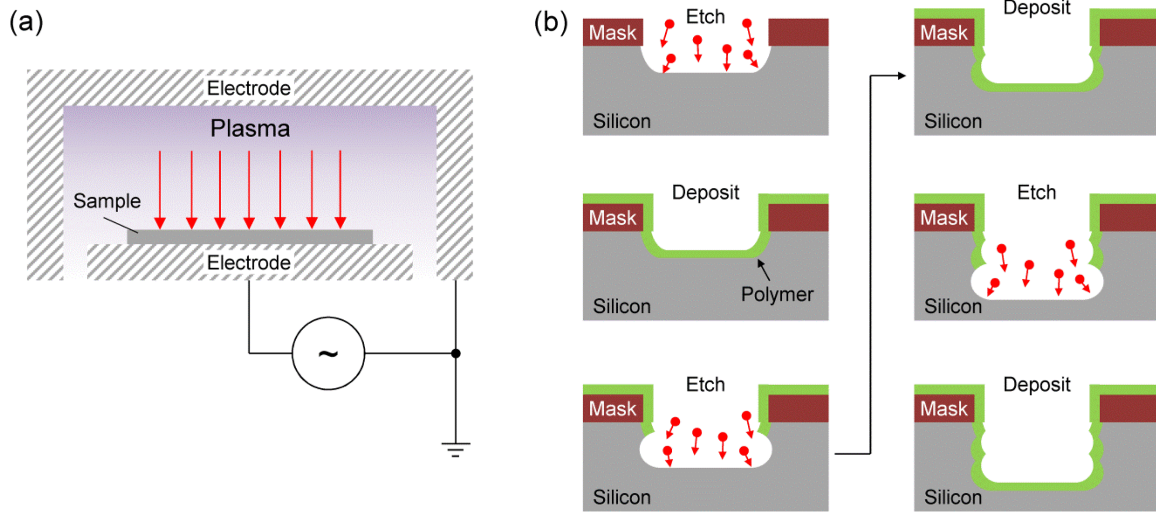

Figure 4.1 Schematic illustrations of (a) asymmetrical reactive-ion etching system chamber and (b) working principles of deep reactive-ion etching using alternative etching and polymer deposition cycles.

Deep reactive-ion etching (DRIE) is a modification of RIE for highly anisotropic and deep etching using alternating etching and polymer deposition cycles. Figure 4.1(b) depicts the high-aspect-ratio and vertical trench etching by the alternative etching and protective polymer deposition cycles in the DRIE process. The SF_6 and C_4F_8 gases are generally used as a source for silicon etching and etch-resistant polymer deposition, respectively. As a conformal deposition, the passivation polymer is deposited on the bottom of the etching target as well as the sidewall. However, anisotropic plasma etching etches the polymer on the bottom of the sample faster than the polymer on the sidewalls because the polymer dissolves slowly in this etching process and thus achieves highly anisotropic vertical etching of the silicon by protecting sidewalls from etching. The sidewalls are often slightly tapered rather than being a perfect 90° and optically not very smooth. The key difference between RIE and DIRE is the etching rate: the etching depth by RIE is generally limited to around 10–15 μm with an etching rate of 1 μm/min, whereas the DRIE can etch up to 600 μm with an etching rate of 1–20 μm/min. Hard-baked photoresist or SiO_2 can be used as an etching mask due to its high selectivity to silicon. From the thermal resistance network analysis discussed in Chapter 3, the deeper reservoir depth is preferred to prevent the boiling of the coolant in the reservoir before it flows up to the evaporator surface. Therefore, DRIE technique can be used to fabricate both the evaporator and reservoir layer.

4.1.2 Fabrication Flow for Evaporator and Reservoir

Figure 4.2 illustrates the fabrication flow of the evaporator and reservoir layer in the TGP. A single photomask for standard photolithography was used to fabricate the reservoir layer, whereas two lithography steps were needed for the evaporator layer because the etching depth for the evaporator depends on the length of the ZnO nanowires to make sure the coolant touching the evaporator surface overcomes the dryout limitation. Thus, the etching depth on the evaporator site was less than the vapor channels on the layer were, resulting in two lithography steps and alignment work, as seen in Fig. 4.2(a). In this work, clean p-type <100> 4-inch silicon

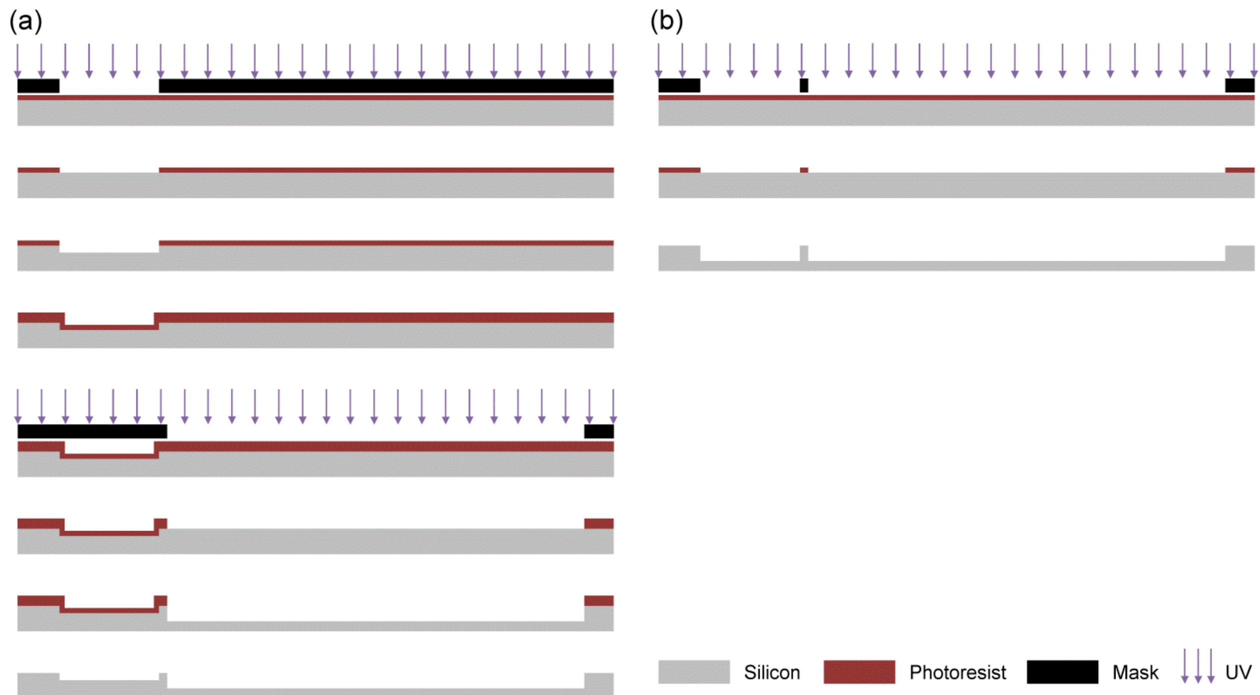

Figure 4.2 Fabrication flow schematic of (a) evaporator layer and (b) reservoir layer using standard photolithography and deep reactive-ion etching.

wafer with 10–20 Ω-cm resistivity was used. The I-line positive photoresist (PR, OiR 906-12, Fujifilm, Japan) was then spin-coated at 1,300 rpm for 30 s to deposit the thickness of approximately 2 μm. After PR coating, the wafer was softly baked at 90°C for 1 min to evaporate the solvent in the PR so that the PR was not sticky. The patterning of the evaporator site by contact photolithography (MA6, Karl Suss, Germany) with 17 mW/cm^2 for 6 s was followed by the post exposure bake at 120°C for 1 min to reduce the mechanical stress in the PR film. The wafer was then developed in the developer (OPD-4262, Arch Chemicals, Inc., CT) for 1 min. After rinsing in DI water, the hard baking of the developed wafer was performed on a hot plate at 120°C for 20 min to make the developed photoresist physically, thermally, and chemically hard and thus more adhesive to the silicon wafer for subsequent etching processes. For etching silicon substrate for the evaporator site, anisotropic etching was conducted by a DRIE etching machine (STS2 ICP-SR, SPTS, CA) for 3 min to etch the trench to a depth of 10 μm. To fabricate the vapor channels and intermediate chamber on the evaporator layer, the same standard photolithography procedures were performed on the etched wafer. The second photomask was aligned with the evaporator site, and the wafer was exposed by ultraviolet (UV) for 6 s. The previous recipes for baking and development could be applicable to the second photolithography. Finally, the photoresist on the wafer was stripped by oxygen plasma (Technics PE II-A, Technics West, Inc., CA) at 300 W for 7 min. The fabrication of the reservoir layer was much easier than the evaporator layer was because the reservoir layer contains only a single photolithography step to etch both the reservoir chamber and the liquid channel on the layer. The same recipes for standard photolithography and DRIE were used for this process.

4.1.3 Fabrication Results

Figure 4.3 shows the scanning electron microscope (SEM) images of the fabricated evaporator layer, which is the top layer among three layers in the TGP for transporting the vapor through the microchannels. Once the coolant removes the heat by touching the evaporator surface underneath the hot chip, the vapor escapes from the evaporator site through the neck connected to the vapor channels, as seen in Fig. 4.3(a). The width of the vapor channel at the entrance is 500 μm and gradually decreases until it reaches 100 μm at the end of the channel. Because the total length of the vapor and liquid channels was designed at 40 mm, the tapered angle of both channels is 0.286°. The result of the reservoir layer was pretty much the same as the evaporator layer was except in a reversed direction, as already shown in Fig. 2.3(c) and Fig. 2.5. Figure 4.4 shows the zoomed-in view of triple-spike microstructures at the end of the tapered vapor and liquid channels. As mentioned in Chapter 2, the triple-spike microstructures at the entrance of the reservoir chamber will drive the liquid out of the microchannels, spreading liquid across the reservoir by distributing the meniscus and extending the capillary action by the assistance of the microstructures, which achieve rapid refilling of coolant into the reservoir.

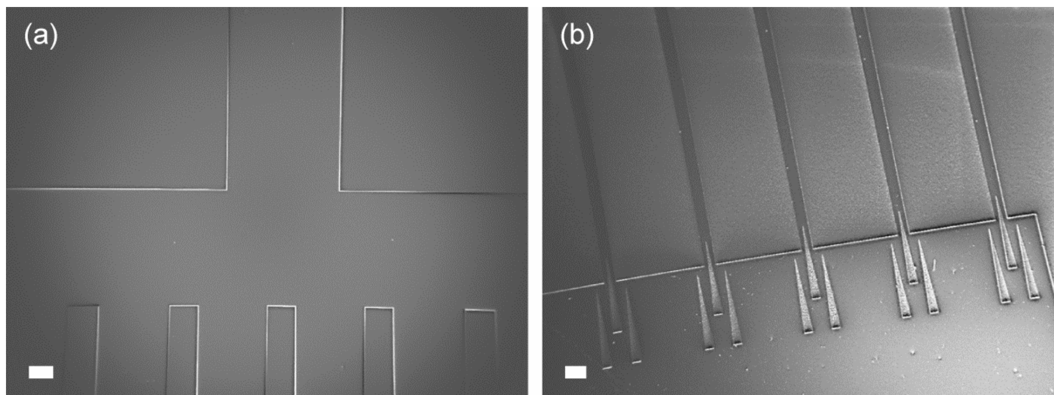

Figure 4.3 SEM images of deep reactive-ion etched evaporator layer: (a) neck part where the evaporator site and vapor channels are connected and (b) intermediate chamber, which is the end of the tapered vapor channels where the condensed liquid meniscus overflows by triple-spike microstructure. Scale bars: 200 μm for both (a) and (b).

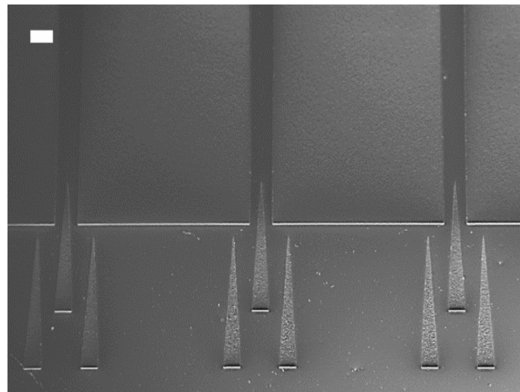

Figure 4.4 Zoomed-in view of triple-spike microstructures at the end of tapered vapor and liquid channels to drive the liquid meniscus out of the channels by extending the capillary action. Scale bar: 100 μm.

4.2 Coherent Porous Silicon Wick Fabrication

4.2.1 Principles of Photoelectrochemical Etching

The crucial feature of the coherent wick layer is that the vertically aligned microchannels transport the coolant from the reservoir chamber to the end of pores using capillary pressure before the coolant spreads across the entire wick surface by the nanowires. To fabricate the multiple straight microchannels through the silicon substrate, a combination of standard photolithography and DRIE technique can be used for deep trenches. However, considering the fabrication cost, time, and yield, it would seem that dry etching is no longer suitable to fabricate the coherent porous silicon wick structure in the TGP. Accordingly, wet chemical etching assisted with electric platform and photo-illumination of so-called photoelectrochemical (PEC) etching was used in this study to fabricate high-aspect-ratio trenches in the silicon wafer for wick structure. The PEC etching in HF acid is basically a highly anisotropic wet etching, which can achieve an aspect ratio over 10:1 and often 100:1 in silicon substrates [80-83]. As the HF acid is used in PEC etching, a charge exchange between the semiconductor and fluoride ions (F^-) in the electrolyte (i.e., HF acid) becomes the operating mechanism of the PEC etching [84]. This formation mechanism is also affected by the dopant type of the silicon substrate [81-84]. In an n-type silicon substrate, minority carriers (i.e., holes) can be formed by illumination that reduces the width of the carrier-depleted space charge region (SCR) [85]. Without photo-illumination, pore formation occurs only at doping levels above around 10^{18} cm^{-3}, at which the tunneling effect appears due to the narrow SCR [84]. The holes generated by photo-illumination move to the silicon-HF acid contact interface, where silicon-silicon bonds weaken, under anodic bias which allows the silicon surface to be attacked by F^- ions in the HF acid [84]. The overall chemical reaction during the PEC etching can be expressed as follows [81]:

$$2h^+ + 6HF + Si \rightarrow SiF_6^{2-} + H_2 + 4H^+. \quad (4.1)$$

Because, under the anodic bias, n-type silicon always forms SCR, the initiation of pores occurs spontaneously at random locations on the silicon surface, whose position is dominated by the local capturing efficiency of minority carriers [81,86,87]. Figure 4.5 illustrates the scheme of the experimental setup for fabrication of the coherent porous silicon structure using the PEC etching process [41,88]. The basic setup was based on the commercially available PEC etcher (MPSB 150, AMMT GmbH, Germany) [89]. The experimental setup is composed of a chemically resistant polyether ether ketone (PEEK) tank to contain the HF acid, a wafer holder, a sapphire window to illuminate the backside of the wafer, parallel platinum mesh electrodes for anodic bias, and a compressed air line to seal the HF acid flows between the cathode and anode chamber. Once the bias is applied from the external power supply, holes in the n-type silicon wafer generated by UV photo-illumination move toward the HF acid-silicon contact surface where the silicon-silicon bonds are attacked by F^- ions in electrolyte and thus is etched, forming deep trenches at random positions on the silicon surface, as seen in the rectangle showing the close-up view of the wafer surface during the etching. Because hydrogen bubbles occur during the etching (Equation (4.1)), a few droplets of a wetting agent or ethanol can be added to the HF acid to remove bubbles trapped in trenches, which may hinder the deep etching of the trenches [90,91].

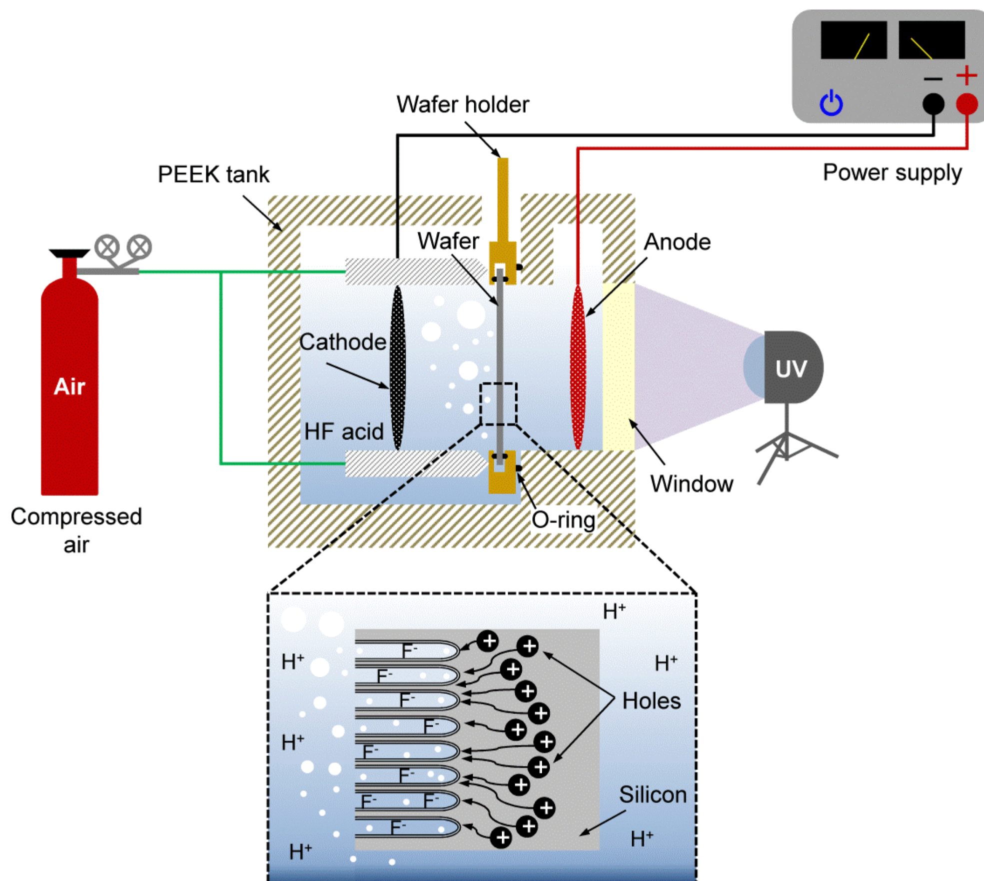

Figure 4.5 Schematic illustration of the coherent porous silicon fabrication process by photoelectrochemical etching process. The minority carriers in n-type silicon move to the hydrofluoric acid-silicon contact surface to attack the weaken silicon-silicon bond.

4.2.2 Fabrication Flow for Coherent Porous Silicon Wick

The fabrication flow of the coherent porous silicon wick layer is shown in Figure 4.6. The illustration depicts the fabrication flow of the porous silicon wick before the ZnO nanowires are synthesized on the wick surface, which will be discussed in the next section. Because the porous region must be placed where the evaporator and coolant chamber were aligned together, the PEC etching was performed on a local area using standard photolithography with a suitable mask layer. To protect the unexposed silicon surface from the attack of F^- ions, a suitable mask selection is important in PEC etching. The most common mask layers such as silicon oxide and nitride, cannot be used in a PEC etching process because they dissolve in HF acid [92]. Accordingly, noble metals (gold or platinum), polysilicon [93], photoresist [94], or silicon carbide [91,92] have been used for a mask layer in PEC etching. It is obvious that the standard photolithography and mask layer were necessary to define the local pattern where a porous silicon would be formed. Considering the large dimension of the evaporator site (5×5 mm^2), however, precise control to define the porous region would increase the fabrication cost as well as the process time. Therefore, in this study, a simple mask pattern method using commercially available polyimide film (Kapton, Dupont, DE) was used to make the mask layer. Because the

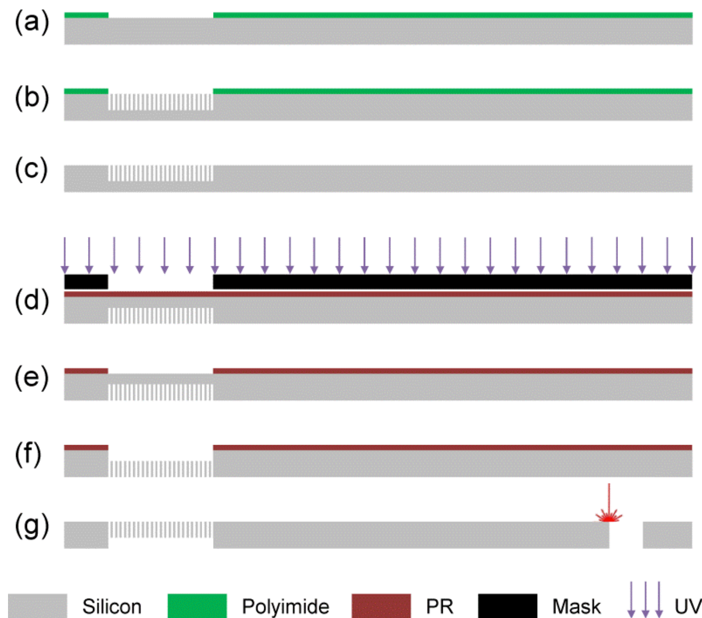

Figure 4.6 Fabrication flow of (a-c) coherent porous silicon wick by local photoelectrochemical etching, (d-f) deep reactive-ion etching of backside of wafer, and (g) laser etching through the layer for via hole connected to the condenser.

polyimide provides good thermal stability and is chemically resistant, it can be effectively utilized in PEC etching, except for patterning the microscale features. As a first step for fabrication of a coherent porous silicon wick, an n-type <100> silicon wafer with 10–20 Ω-cm resistivity and 5 wt % HF acid were prepared. A near-UV light bulb (365 nm wavelength, Spectronics Corporation, NY) was used for the photo-illumination source to generate holes in the n-type silicon wafer. During the etching, the applied current density and voltage were kept constant at 8.6 mA/cm^2 and 4.5 V, respectively [41,95]. To remove the hydrogen bubbles trapped in the trenches during the etching, 1% v/v of ethanol was additionally mixed with the HF acid before etching. Once the PEEK tank was filled with HF acid and the UV light source was set near the window, the wafer was carefully patterned with polyimide tape to expose only the desired area where the macro pores would be generated after etching (Fig. 4.6(a)). After 1 h and 30 min, the sample wafer was taken out of the tank and thoroughly rinsed with DI water. Note that it also requires care to remove the polyimide film because it may still be sticky on the silicon surface, even after etching. In this case, acetone can be used to remove the polymer residue on the wafer (Figs. 4.6(b) and (c)). Considering a reservoir containing a large volume is preferred based on the numerical analysis in Chapter 3, the pore depth was limited to approximately 200 μm, and the backside of the wafer was aligned, patterned with PR, and etched by DRIE (with the same recipe in subsection 4.1.2) to open the pores on both sides of the wick layer (Figs. 4.6(d)-(f)). Finally, the "via hole" (see Fig. 2.4) was punched by a laser etcher (10.6 μm 30 W CO_2, PLS6MW, Universal Laser Systems, AZ). Even though DRIE can also be used to etch through the wafer to form the "via hole", the laser etcher was more suitable for this fabrication in terms of sample preparation time, labor, and fabrication cost.

4.2.3 Fabrication Results

As a result of PEC etching, Figure 4.7(a) shows a top view of the coherent porous silicon surface with a porosity of 17.5% (approximately 11,000 pores/mm^2). An average diameter of pores and pitch (i.e., distance between pore to pore) is around 4.5 μm and 9.3 ± 1.5 μm, as seen in Fig. 4.7(b). Considering the design value for pore radius (< 2.79 μm) and porosity (20%) derived from the numerical analysis in Chapter 3, reasonable values were obtained by the PEC etching. It is also noticeable that the top surface was not evenly smooth, as it showed shallow trenches near the main deep trenches. Because the PEC etching in the present study does not require a mask to pattern initial grooves where the nucleation of pores is induced, sequent and discrete nucleation sites occur on the silicon surface, which initiates the formation of new trenches next to the previously etched trenches with a time lag [96]. The cross-sectional view with a 45° tilted angle shows straight and high-aspect-ratio vertical microchannels with an average length of 240 μm, as seen in Figs. 4.7(c) and (d). After fabricating the coherent porous silicon by PEC etching, the backside of the wafer was etched by DRIE to form a thin porous wick membrane structure that allows the coolant to pass across the wick membrane from the reservoir to the evaporator surface. Figure 4.8 shows the coherent porous silicon wick membrane after back etching of the porous silicon. Through this porous membrane, the coolant can surge up to the end of the pores by primary capillary pressure, but the coolant is unable to overflow out of the pores due to the pinned liquid meniscus at the end of the pores.

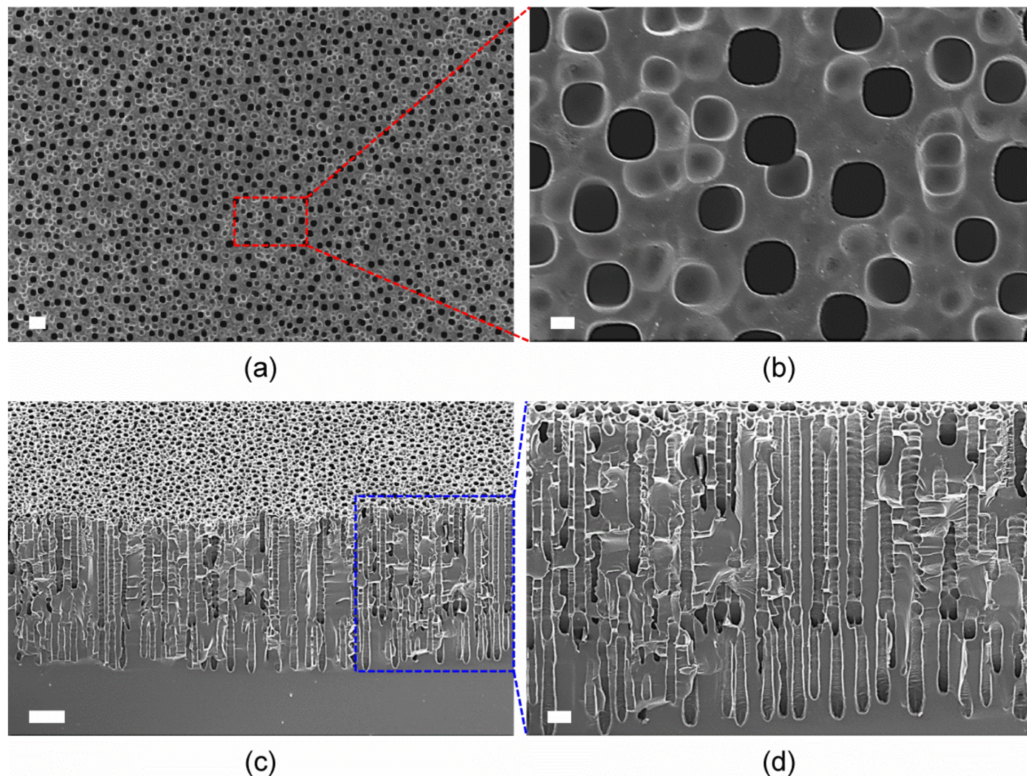

Figure 4.7 SEM images of photoelectrochemically etched coherent porous silicon: (a) top surface view, (b) zoomed-in view of micropores, (c) 45° tilted view, and (d) zoomed-in view of straight and vertically aligned microchannels generated by coherent porous silicon. Scale bars: (a) 10 μm, (b) 2 μm, (c) 30 μm, and (d) 10 μm.

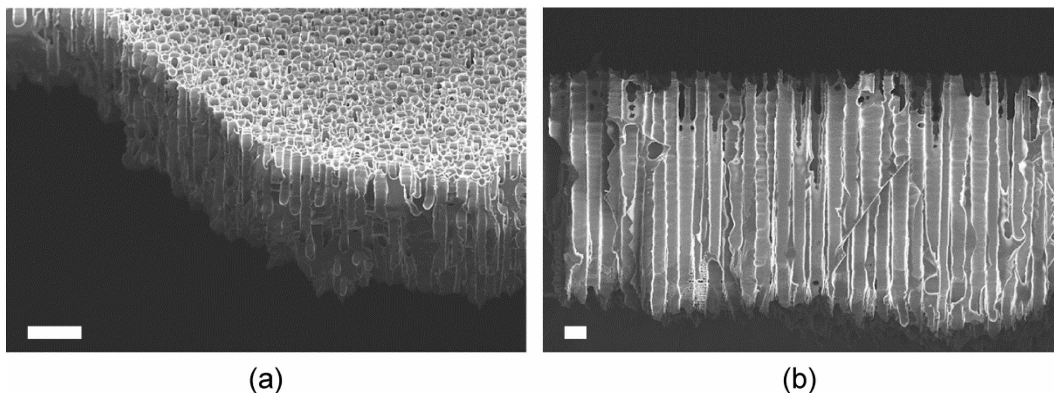

Figure 4.8 SEM images of coherent porous silicon wick membrane after backside deep reactive-ion etching: (a) 30° tilted view and (b) cross-sectional view. Scale bars: (a) 30 μm and (b) 10 μm.

4.3 Zinc Oxide Nanowire Synthesis by Bottom-Up Approach

4.3.1 Vapor-Liquid-Solid Mechanism

Most semiconductor nanowires can be synthesized by the vapor-liquid-solid (VLS) mechanism originally proposed by Wagner and Ellis 50 years ago [97]. In this process, the vapor phase of semiconductor material is absorbed by a liquid alloy droplet of impurity or appropriate catalysts. Commonly, the catalyst is a eutectic alloy with a low melting point that plays an important role in growing the whiskers by precipitation of the substrate material and providing seeds for whisker growth. The state of the catalyst relies on chamber's pressure and temperature [98]. The semiconductor vapor is then condensed at the interface between the liquid alloy droplet and the whiskers, which may extend the length of the nanowire [99]. In the VLS process, the diameter of the nanowire is defined by the size of the catalyst particle (i.e., related to the thickness of catalyst layer), and the location where the nanowire grows is determined by the site of the particle [100,101]. In the present work, the same VLS method was initially performed to synthesize the ZnO nanowires on the coherent porous silicon wick structure [95]. The schematic illustration of growth process is shown in Figure 4.9. In this process, a thin gold layer of 1.5 nm was deposited on the porous region of the wick layer using electron beam evaporation (Edwards Auto 306 e-beam evaporator, Edwards, England) and a lift-off process. The deposited gold played a role in initiating the growth of ZnO nanowires as a catalyst particle [102]. After deposition of the catalyst, the sample was placed inside a quartz tube 2 cm downstream from the source powder, which was composed of ZnO (99.999% metals basis, Puratronics, Alfa Aesar, MA) and graphite power (Crystalline, 325 mesh, 99%, Alfa Aesar, MA) with a 1:1 w/w ratio in an alumina boat [95, 103-105]. The quartz tube was then pumped to remove contaminants in the tube and purged back with argon (Ar) gas. The furnace (Lindberg/Blue M, Thermo Fisher Scientific, MA) was heated to 900℃ and kept there for 10 min for the synthesis of nanowires under an Ar gas of 22.5 and oxygen (O_2) gas of 0.5 sccm (standard cubic centimeters per minute) flow rate, as seen in Fig. 4.9.

Figure 4.10 shows the SEM images of the porous silicon wick decorated by ZnO nanowires grown using the VLS mechanism. At the gold/silicon eutectic temperature (363℃ [106]),

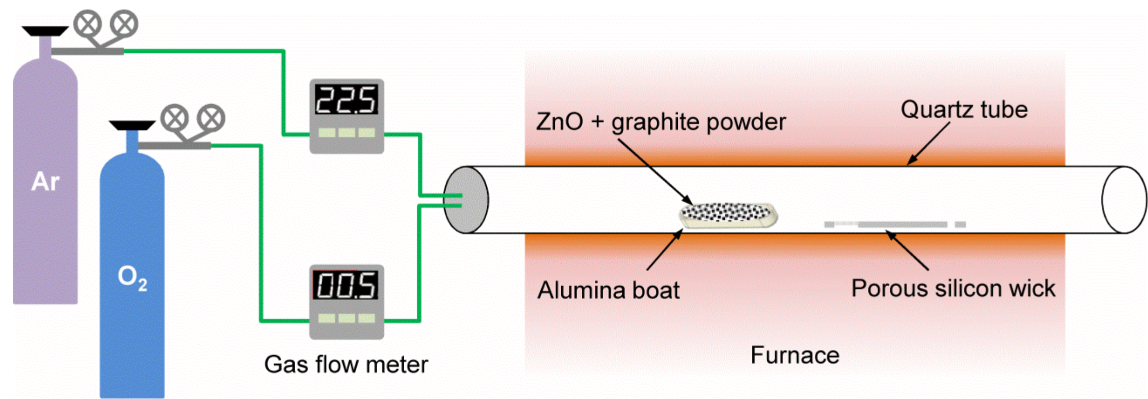

Figure 4.9 Schematic illustration of experimental setup for vapor-liquid-solid zinc oxide nanowires growth on the photoelectrochemically etched porous silicon wick layer.

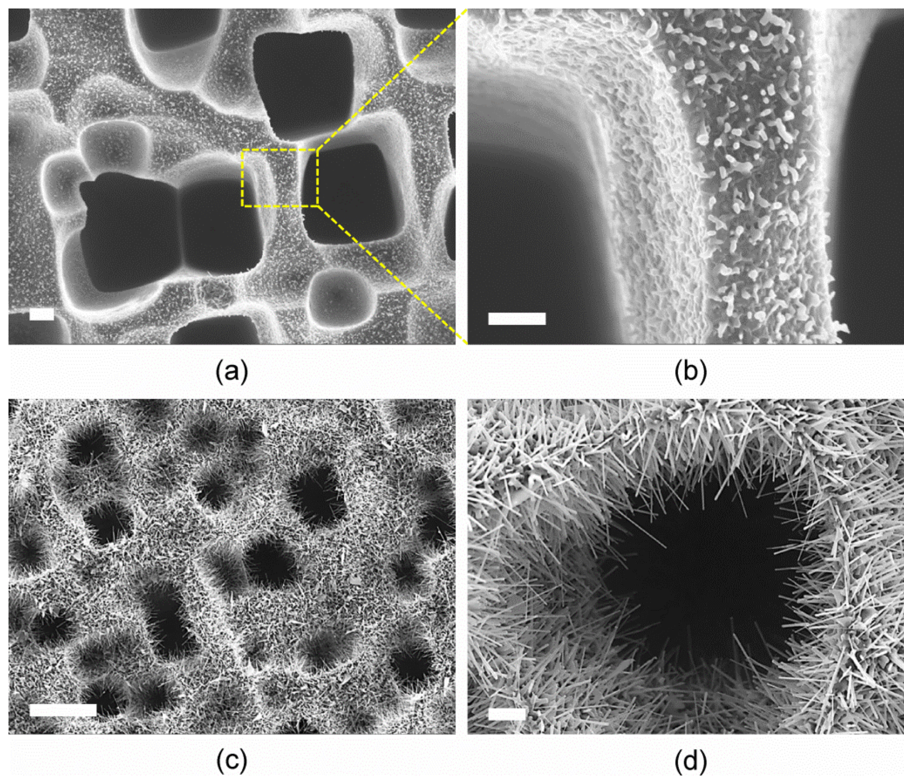

Figure 4.10 SEM images of the porous silicon wick membrane decorated by zinc oxide nanowires synthesized by vapor-liquid-solid mechanism: (a) initiation of growth from the gold catalyst particles on the porous silicon substrate, (b) zoomed-in view of initial formation of whiskers, (c) top surface view of nanowire-integrated porous silicon wick, and (d) zoomed-in view of micropore ends covered by zinc oxide nanowires. Scale bars: (a) 2 µm, (b) 1 µm, (c) 10 µm, and (d) 1 µm.

a seeded gold layer would make liquid alloy nanodroplets like an island on the silicon substrate, which absorbs ZnO vapor at the interface between the liquid droplet and solid silicon surface. The absorbed ZnO vapor is then condensed under the alloy droplets, where the whisker initiates growth, as seen in Figs. 4.10(a) and (b). Because the catalyst remains at the tip of the nanowires grown in the VLS process, it may be necessary to remove the catalyst to prevent metal contamination. The orientation of the nanowires depends on the lattice of the substrate, on which an epitaxial relationship between the nanowire and substrate can be made [100]. Because the ZnO *a*-axis is related to the *c*-axis of the sapphire, vertical growth can be built on the sapphire or silicon carbide substrate [103,104]. In the present study, however, random direction of nanowires on the porous silicon wick structure was preferred to spread the coolant across the entire wick and evaporator surface; vertical growth was not necessary. The top and zoomed-in view of the porous silicon wick membrane decorated by ZnO nanowires both on the surface and periphery of the pore are shown in Figs. 4.10(c) and (d), respectively. The results show that the nanowires, which had an average diameter of 100 nm, were successfully grown on top of the porous silicon wick to drive the liquid out of the pore by extended capillary action. In the following subsection, the results of the VLS process will be compared with those in the hydrothermal synthesis method, which is an easier and more practical method and thus was selected for use in this study.

4.3.2 Hydrothermal Methodology

Despite the VLS synthesis method that provides high-quality ZnO nanowire, the vapor phase approaches require a high temperature, a long process time for sample preparation, and expensive thermal deposition systems. Consequently, a new approach, the so-called hydrothermal method, has been developed for ZnO nanowire synthesis with a large-scale growth area and relatively cheaper equipment at low temperatures [107-110]. The advantages of this aqueous approach are that the ZnO growth is independent from the substrate (i.e., it can be grown on any substrates, such as metals, semiconductors, and polymers), and large-scale growth is achievable. In addition, the total synthesis time is relatively shorter than the VLS method because the hydrothermal method does not need to wait until the temperature has cooled down to room temperature—it can be done at a low temperature (around 90–95℃) [107,108]. In this study, the hydrothermal method was preferred for the ZnO nanowire synthesis on the porous silicon wick structure because it may minimize the metal contamination at the tip of the nanowire (such contamination may affect the thermal properties of the system), and it provides an easier, more practical, and faster process than the VLS method. The overall process to synthesize the ZnO nanowires on the porous silicon wick is shown in Figure 4.11. As a first step, the porous region where the nanowires are to be grown was defined by the standard photolithography step (Figs. 4.11(a) and (b)). The ZnO nanoparticles (NPs, < 130 nm, 40 wt % in ethanol, Sigma Aldrich, MO) were then spin-coated on the porous silicon wick (Fig. 4.11(c)) and followed by the lift-off process to retain NPs on the porous area (Fig. 4.11(d)). After seeding NPs, the sample was immersed in an aqueous solution containing zinc nitrate hydrate (25 mM, $Zn(NO_3)_2{\cdot}6H_2O$, Sigma Aldrich), hexamethylenetetramine (25 mM, $C_6H_{12}N_4$, Sigma Aldrich), and polyethylenimine (5mM, C_2H_5N, branched, low molecular weight, Sigma Aldrich) at 92℃ for 2 h (Figs. 4.11(e) and (f)) [41,88,108,111,112]. The sample was then taken out of the solution, rinsed thoroughly with DI water, and baked on a hot plate at 400℃ for 30 min for removal of residual organics on the sample [41,111].

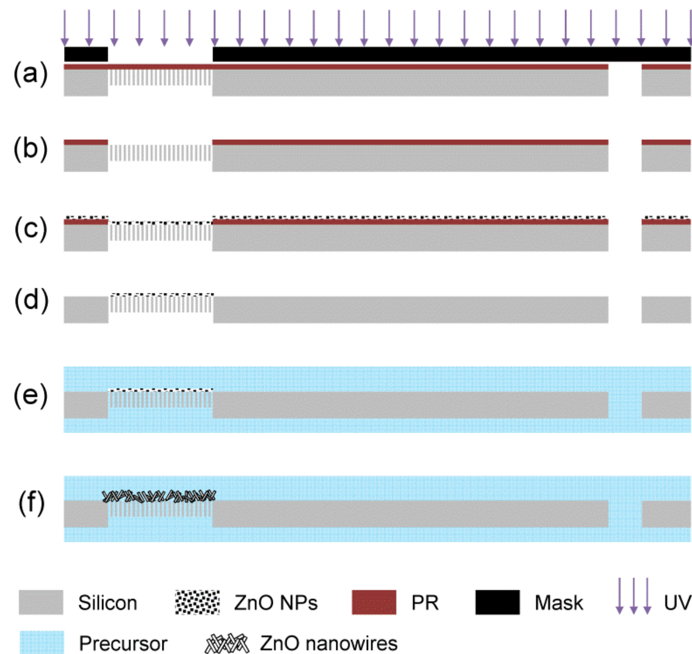

Figure 4.11 Fabrication flow of nanowire-decorated porous silicon wick layer by (a-b) standard photolithography, (c-d) deposition of zinc oxide nanoparticles by lift-off, and (e-f) hydrothermal synthesis in precursor solution.

Figure 4.12 shows the SEM images of the porous silicon wick layer covered by ZnO nanowires synthesized by hydrothermal methodology. The uniformly deposited ZnO NPs using the spin-coating are shown in Figs. 4.12(a) and (b) showing an average diameter of 75 nm. Because the growth sites of nanowires is defined by the locations of deposited NPs, uniform deposition is critically important to synthesize dense nanowire forests. After heating the seeded sample for 2 h in the precursor solution, the dense nanowire forests were synthesized on the surface of the wick structure, as seen in Figs. 4.12(c) and (d). Note that nanowires can be also synthesized in the inner wall of pores to accelerate a feeding speed of coolant from the reservoir to the evaporator surface by enhanced capillary action in the inner wall. To grow nanowires over the top surface and inner wall of the pores simultaneously, the ZnO NPs can simply be dropped onto the porous silicon wick region rather than the deposition by spin-coating so that the NPs dispersed in ethanol can penetrate pores, which can deposit NPs in the inner wall of pores [41]. Figure 4.13 shows the hierarchical porous silicon wick, where the top surface is decorated by ZnO nanowires to drive the coolant out of the pores and spread it between the entire wick and evaporator surface by enhanced capillary action. In the typical porous wick structure without nanowires, coolant surges up to the end of pore by the primary capillary force in the vertical microchannel, but it is unable to overflow out of the pore because the liquid meniscus is pinned at the end of the pore, which causes the wick dryout limitation in the TGP. With the assistance of decorated nanowires, the pinned meniscus at the pore is broken, and liquid is sucked into the nanochannel generated between individual nanowires. Therefore, the chronic dryout problem in the micro cooling devices can be solved by the fabricated hierarchical structure.

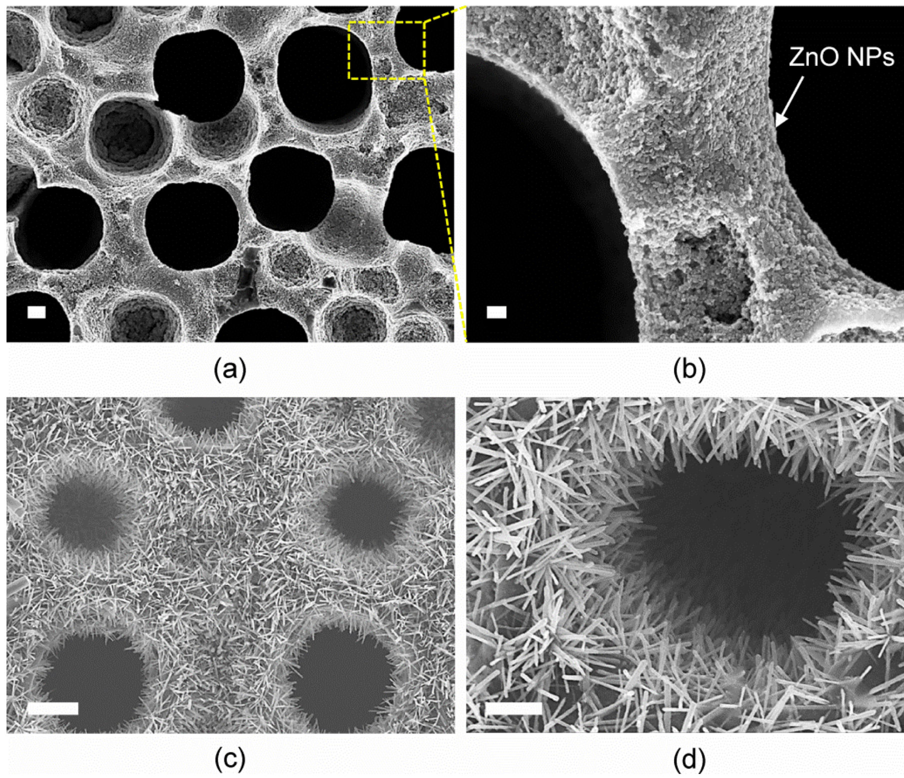

Figure 4.12 SEM images of the porous silicon wick membrane covered by zinc oxide (ZnO) nanowires synthesized by hydrothermal methodology: (a) seeded porous silicon wick by ZnO nanoparticles, (b) zoomed-in view, (c) top surface view of nanowire-integrated porous silicon wick, and (d) zoomed-in view of micropore ends covered by ZnO nanowires. Scale bars: (a) 1 μm, (b) 200 nm, (c) 2 μm, and (d) 1 μm.

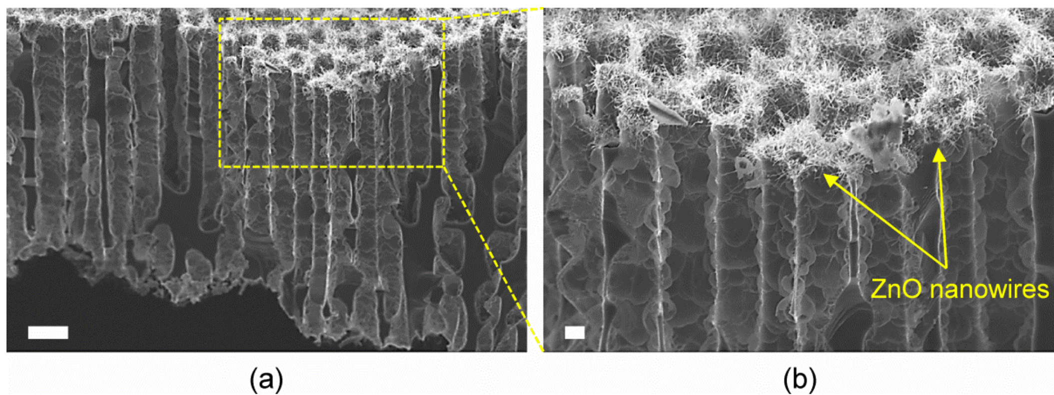

Figure 4.13 SEM images of the hierarchical porous silicon wick layer decorated by zinc oxide nanowires to drive the coolant out of the pore by the assistance of extended capillary action: (a) 20° tilted view and (b) zoomed-in view. Scale bars: (a) 10 μm and (b) 2 μm.

Chapter 5

Experimental Testing of Device

5.1 Liquid Feeding Performance Test

5.1.1 Self-Transport of Condensed Liquid

To demonstrate the ability of transport liquids condensed from superheated vapor, four different shapes of vapor and liquid channels were designed and fabricated. Figure 5.1 shows the four different designs to test the transporting performance of condensed liquids in each channel. The first designed channel is the tapered channel with a decreasing gap thickness toward the intermediate chamber to transport the liquids by themselves with the assistance of an axial force arising from the different curvature pressures [52]. Although this tapered channel can transport the liquids up to the channel ends, the liquid meniscus is expected to be pinned at the neck of the channel due to the surface tension. Thus, various microstructures were introduced at the end

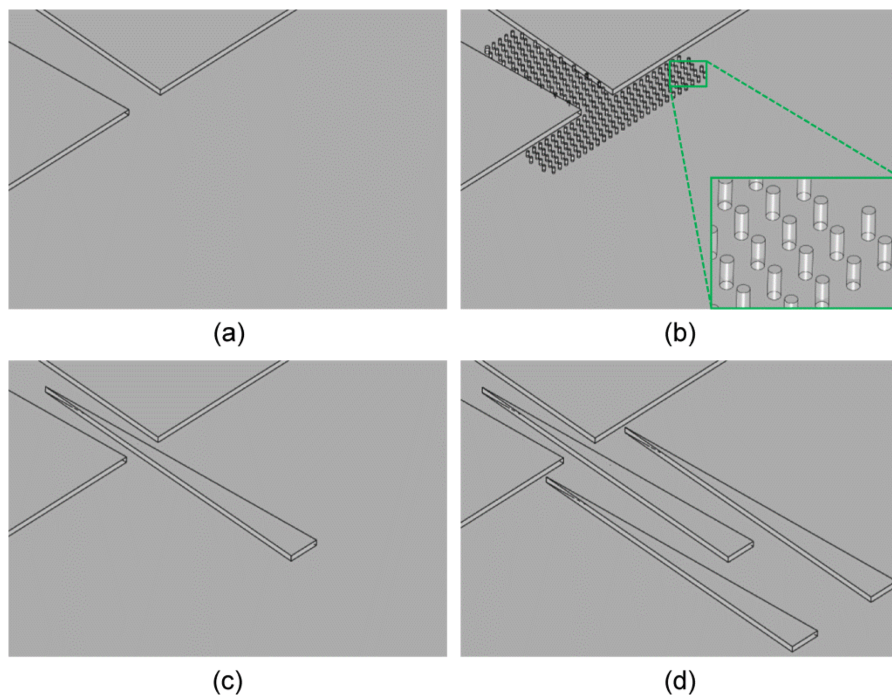

Figure 5.1 Schematic illustrations of microchannel designs in the evaporator layer to transport the condensed liquid into the reservoir chamber: (a) tapered design, (b) micropost design in the tapered design, (c) single-spike design in the tapered design, and (d) triple-spike design in the tapered design.

of the tapered channel to break the meniscus up and further extend the capillary action. The micropillar structure, which is extensively used in microfluidic applications to provide extended capillary force [113-115], was first designed and adopted, as seen in Fig. 5.1(b). For the novel design in the present study, the single-spike and triple-spike designs previously proposed in Chapter 2 were also suggested for the comparison, as seen in Figs. 5.1(c) and (d). The SEM images of four fabricated channels are shown in Figure 5.2. The fabrication flow and recipes are the same as described earlier in subsection 4.1.2, using standard photolithography and DRIE. The microposts with a diameter of 5 μm and a pitch (center-to-center distance between posts) of 20 μm were successfully fabricated, as seen in the rectangle showing the zoomed-in view of the microposts in Fig. 5.2(b). Because the interface between silicon and water has hydrophobicity with a contact angle of approximately 77°, the condensed liquid cannot be transported by the capillary action unless the wettability of the interface is changed [116,117]. To investigate the wettability of the fabricated channel, the contact angle on the surface was measured by the contact angle measurement system (DSA10, Krüss GmbH, Germany), as shown in the captured images below Fig. 5.2. The silicon surface with thin native oxide shows a contact angle of 52.1°,

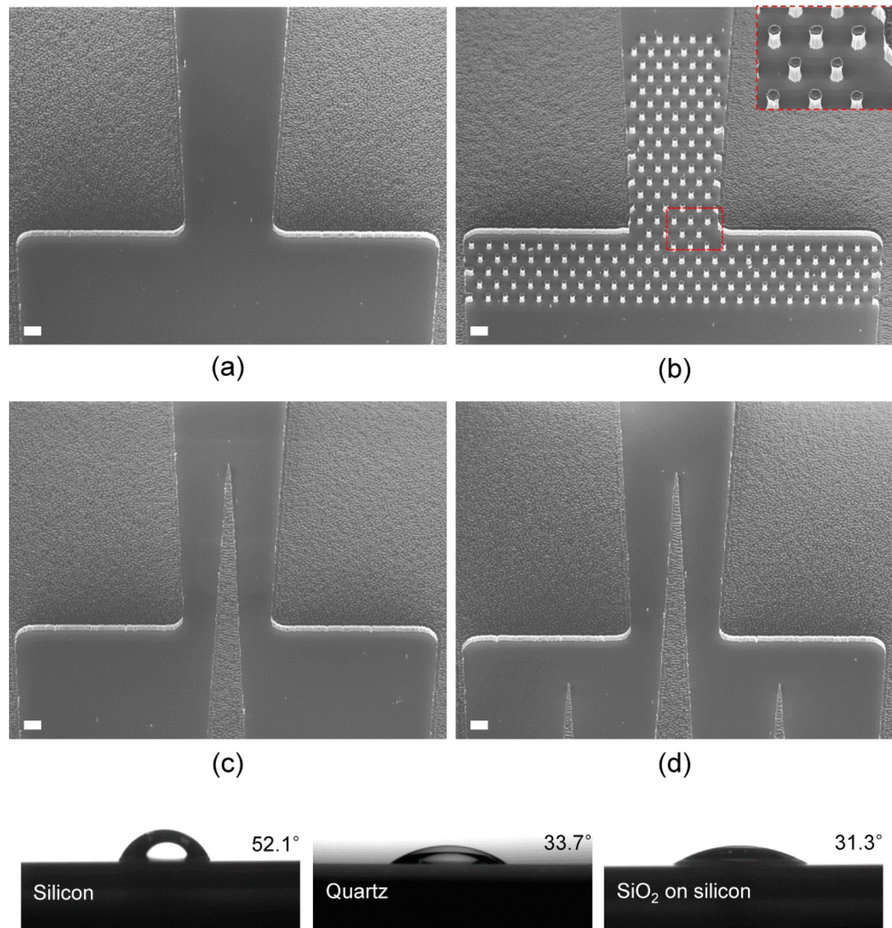

Figure 5.2 SEM images of four different fabricated designs for vapor and liquid channel in the thermal ground plane: (a) tapered channel, (b) microposts design in the tapered design, (c) single-spike design in the tapered design, and (d) triple-spike design in the tapered design. Scale bars: 20 μm for (a), (b), (c), and (d). Lower images: measured contact angles on the different surfaces including silicon with native oxide, quartz, and silicon dioxide.

whereas the quartz and SiO_2 surface on the silicon have a contact angle of less than 35°, which may help condensed liquids be transported by the capillary force arising from the interface between the liquid and channel wall surface. To demonstrate the movement behavior of liquids in the fabricated channels, a three-dimensional finite elements analysis was also carried out using ANSYS Multiphysics (CFX 13.0). Figure 5.3 shows the comparison of results between computation and experiment. The sequential images during the experiment were taken by a high-speed camera (Phantom Miro eX4, Vision Research, NJ) with a time interval of 50 ms. For both computation and experiment, a liquid volume of 1.6 µL was used. As a result, the overall experimental results showed good agreement with those of the finite element analysis for each channel. The tapered channel design shows the pinned meniscus at the end of channel as expected. To transport the liquid in the channel, this pinned meniscus must move farther against the surface tension. Even though the micropost design was fabricated and tested, the meniscus was unable to overflow out of the channel end in this study, which might be caused by sparse density of the microposts, indicating that the capillary force in the micropost design highly

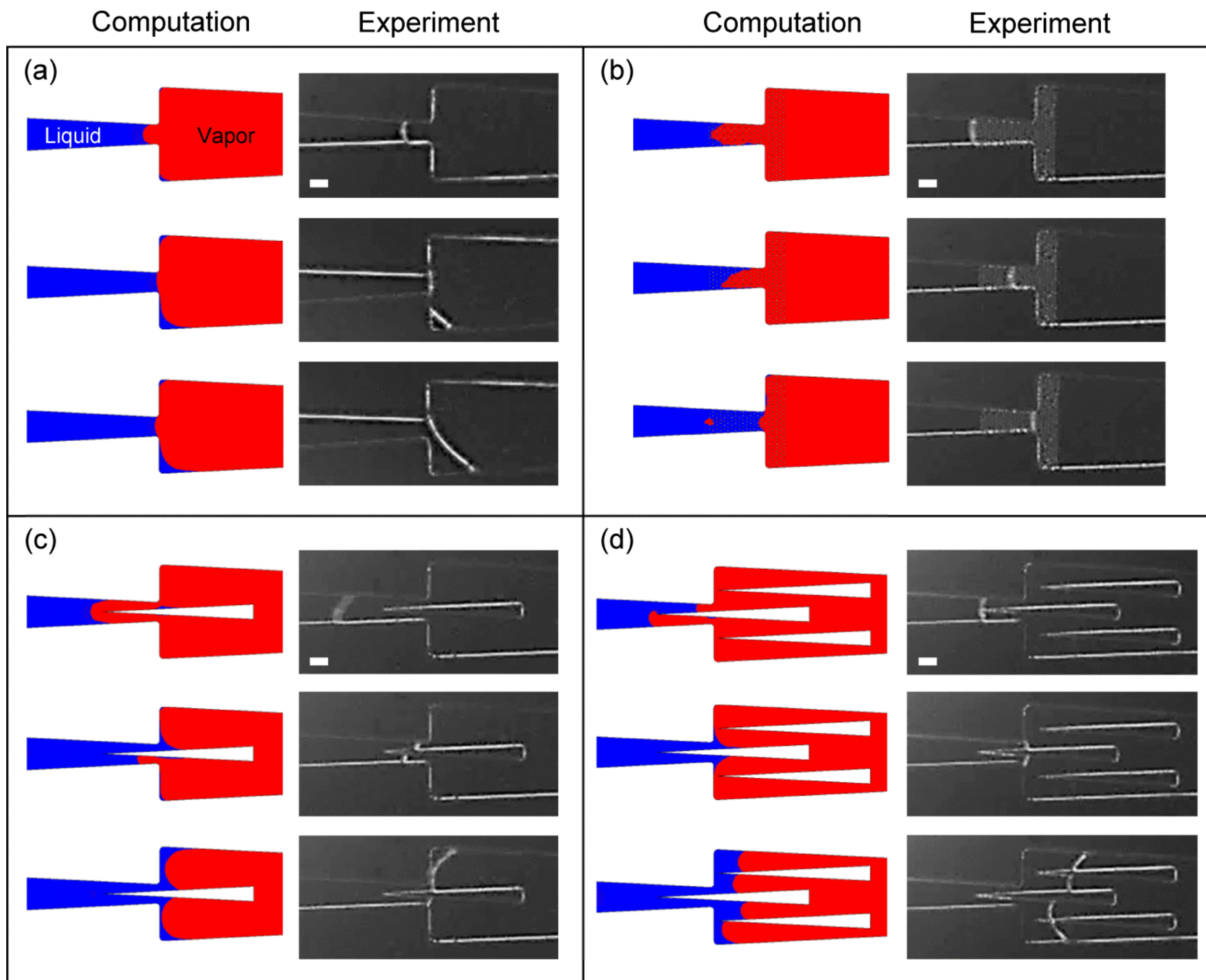

Figure 5.3 Comparison of results between computational and experimental results for each designed microchannel to transport the liquid liquid by extended capillary action. Scale bars: 100 µm for (a), (b), (c), and (d).

depends on the diameter and pitch distance. The computational result also showed that the meniscus in the channel with the micropost design was stopped at the end of channel, the same with the experimental data (Fig. 5.3(b)). In the single-spike design, the liquid meniscus was successfully separated, but the two distributed menisci were unable to move farther away from the channel end due to the secondary surface tension on the corner that was pulling the menisci again. These results showed that the smaller meniscus was preferred to overcome the surface tension in the channel. Consequently, the triple-spike design showed the best results for transporting the condensed liquids by distributing the meniscus and extending the capillary action between four separated channel gaps, as seen in Fig. 5.3(d). Therefore, the triple-spike structure, which is a promising design for transporting the liquids when the chip mounted on the evaporator is turned off, was selected for channel design in the TGP. The sequential images of self-transporting liquids in the evaporator channel are shown in Figure 5.4. The liquid condensed from the superheated vapor in the channel was first transported along the 40 mm tapered channel with a decreasing gap from the vapor entrance of 500 μm to the channel exit of 100 μm (i.e., tapered angle of 0.286°). The meniscus of the transported liquid was then separated by the middle spike of the triple-spike structure, forming two menisci. After overflowing out of the channel end, these menisci were separated again by the two side spikes and flowed along the sidewalls of the spike structure, which allowed the liquid to be collected on the spike structure (see Fig. 5.3(d)). As the vapor is condensed to the liquid droplet continuously, condensed liquids could be collected to the triple-spike structure in the intermediate chamber and finally dropped down to the liquid channels on the reservoir layer. Therefore, all liquids could be collected rapidly and safely into the reservoir chamber even if the chip mounted on the evaporator surface stopped operating, which might induce the vapor in the channel to be condensed due to an abruptly decreased temperature near the evaporator site.

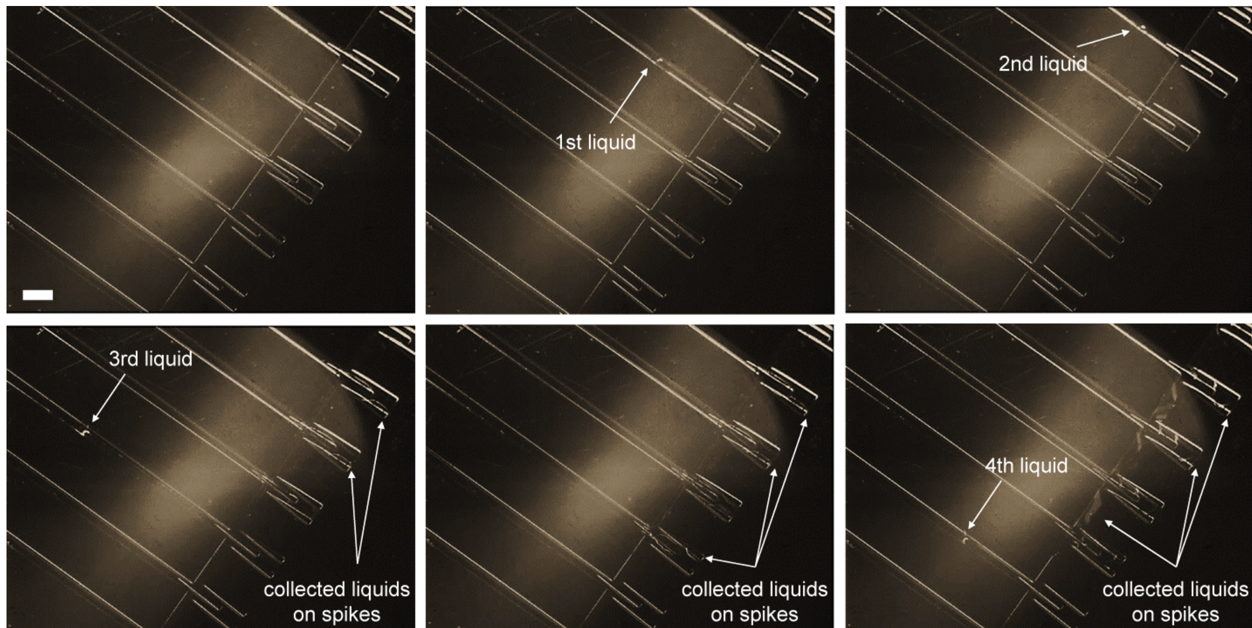

Figure 5.4 Sequential images of self-transporting condensed liquids in the evaporator channel (from top left to bottom right). The liquids were first transported along the tapered channels and then collected on the triple-spike microstructures by distributing menisci. Scale bar: 400 μm.

5.1.2 Continuous Wicking through Hierarchical Membrane

To verify the wicking ability of the fabricated nanowire-decorated coherent wick layer, sequential images taken by a high-speed camera were compared to images of the porous silicon wick structure without nanowires. Figure 5.5(a) shows the top surface view of the coherent wick layer in which the black-colored area indicates the porous silicon wick region without nanowire growth. For the experiment, the wick layer was placed on the microchannel, and the DI water mixed with a 1% v/v wetting agent (Photo-Flo 200, Kodak, NY) was injected underneath the layer at a small volumetric flow rate to minimize unwanted external pressure, which might push the water out of the pores. As a result, the liquid was unable to overflow at all through the porous wick structure without nanowires even after 5 s because all the liquid menisci were pinned at the end of the pores by the surface tension. However, the hierarchical nanowire-decorated porous silicon wick structure could push the coolant up out of the pores and spread it across the top surface of the wick due to the enhanced and extended capillary action, as seen in Fig. 5.5(b). The coolant was first sucked into the pores immediately after the coolant touched the bottom of the

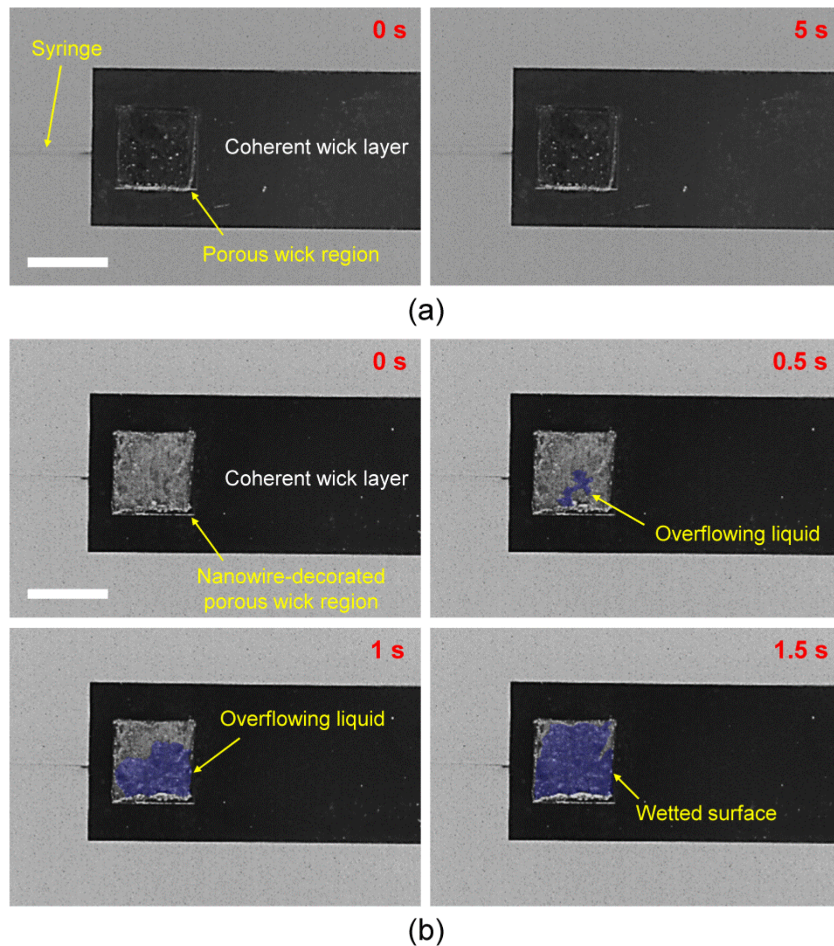

Figure 5.5 Comparison of wicking performance between (a) traditional wick structure and (b) nanowire-decorated coherent porous silicon wick structure. Sequential images were taken by a high-speed camera. Scale bars: 5 mm for (a) and (b).

wick layer and surged up to the pore ends due to the primary capillary pressure. At the pore ends, liquid menisci were able to flow further out of the pore due to the nanowires synthesized at the pore ends, resulting in overflowing liquid across the top surface of the wick structure. Consequently, this overflowing liquid kept the entire wick surface wetted and hydrated at all times, overcoming the dryout limitations during operation. To observe the overflowing liquid in the different view, the coherent wick layer was placed between the evaporator and reservoir layer, and a cross-sectional view was recorded by a high-speed camera, as seen in Figure 5.6. The sequentially captured images with a time interval of 100 ms show that the microscale gap between the evaporator and wick layer, which might have been caused by imperfect bonding, was filled with the coolant within 300 ms. This result means the rapid feeding of the coolant from reservoir to the evaporator surface was achieved by the nanowire-decorated hierarchical porous silicon wick structure, which did not occur when a typical porous wick structure without nanowires was used for the experiment. It is also noticeable that coolant could reach the upper surface by jumping the microscale gap, which is often formed due to the imperfect bonding process between silicon surfaces. Therefore, the fabricated nanowire-decorated hierarchical porous silicon wick structure could achieve the overflowing of the coolant from the reservoir chamber to the evaporator surface, allowing the TGP device to regenerate the cooling system by overcoming the dryout limitation.

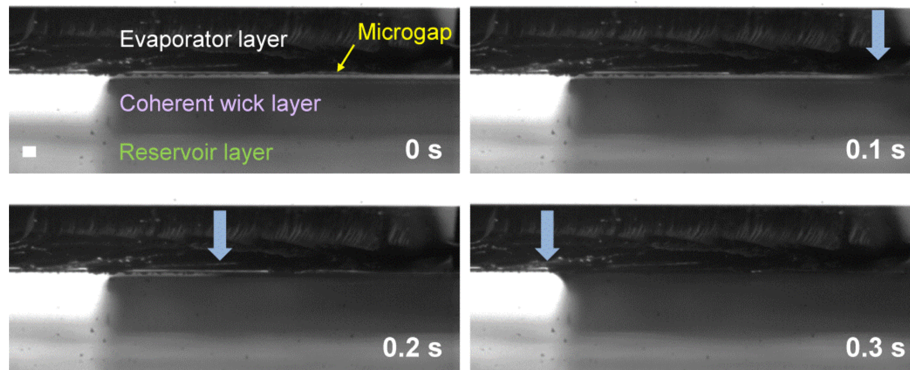

Figure 5.6 Feeding of coolant from reservoir to evaporator surface by nanowire-decorated coherent porous silicon wick structure. The microscale gap between evaporator and wick layer was filled with coolant in a short period of time. The blue arrow indicates the moving meniscus. Scale bar: 100 µm.

5.2 Thermal Conductivity Measurement

5.2.1 Principles of 3ω Method

In Chapter 3, the thermal resistance network analysis for the overall system was performed with computationally estimated thermal conductivities of ZnO nanowires and a coherent porous silicon wick structure. In this study, the thermal conductivity of porous silicon was experimentally measured by the 3ω method, which is widely used for thermal conductivity measurement using the frequency domain and microheater line [118]. In this method, a periodic current I at the frequency ω causes the Joule heating ($\dot{Q} = I^2 R$) with a 2ω, which leads to the variation of the temperature and electrical resistance R with a 2ω component [119]. Thus, the voltage signal across the heater line has a 3ω component. This technique has been extensively used to measure the thermal conductivity of thin films in a cross-plane direction [120] and superlattice samples [121,122] as well as bulk materials with high accuracy because Joule heating can be precisely controlled by the external electronics. As a transient method, the maximum measurable depth can be controlled by changing the heating frequency. Because a relatively small input current (generally tens of mA) would not heat the sample (usually less than 1K), temperature stabilization can be achieved rapidly compared to the steady-state methods in which a long waiting time is needed to stabilize the temperature. To measure the thermal conductivity by the 3ω method, the heater line must be fabricated by microfabrication techniques and electrically insulated from the sample substrate by depositing a thin layer of electrical insulating material, such as SiO_2 or silicon nitride, between the heater line and the sample.

In this study, a sinusoidal voltage source and lock-in amplifier (SR850, Stanford Research Systems, CA) were used to provide the voltage and measure the sinusoidal voltage signals, respectively. Because the 3ω voltage is generally four to five orders of magnitude smaller than 1ω voltage, the dynamic reserve needed to be tuned carefully to ensure the amplifier had a sufficient reserve for the measurement of 3ω voltage. To improve the resolution, a precision resistor (1433 series decade resistor, resolution of 0.01 Ω, GenRad, MA) connected with the heater line in series was added and tuned carefully to match the resistance of the heater line [119]. Therefore, the 1ω voltage would be cancelled by subtracting the precision voltage from the sample voltage, allowing the leftover 3ω signal to become the 3ω voltage of the sample. Figure 5.7 shows the sample preparation process for the thermal conductivity measurement of the porous silicon wick structure. The pore trenches in the bulk 4-inch silicon wafer were first generated by the PEC etching (part (a)), followed by DRIE back side etching (part (b)) to make the thermal penetration depth ($\delta_p = \sqrt{\alpha/\omega}$, where α is the thermal diffusivity) propagate in the porous medium even at the high frequency. The electrically insulating layer, SiO_2, was then deposited with 50 nm thickness using a sputter (Edwards Auto 306 DC/RF sputter, Edwards) and gold was deposited by e-beam evaporator (Edwards) for the heater line on the SiO_2 film (part (c)). The fabricated heat line with a length of 1.5 mm and a width of 80 μm is shown in Fig. 5.7(d). The voltage differences across the heater line were converted to a single output by an amplifier chip (AD524, Analog Devices) and measured by the lock-in amplifier.

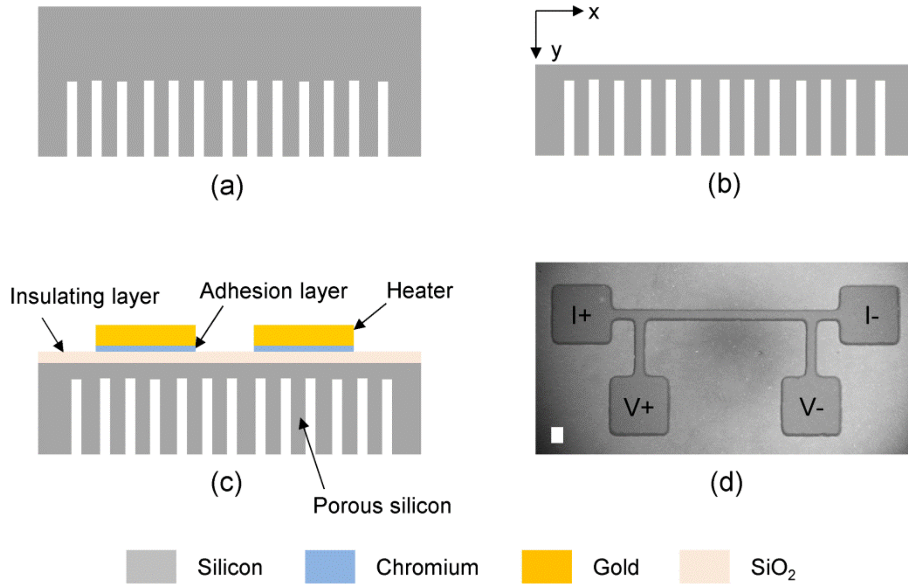

Figure 5.7 Sample preparation process for thermal conductivity measurement of the porous silicon wick structure by 3ω method: (a) photoelectrochemical etching for forming the porous silicon wick, (b) deep reactive-ion etching of bulk silicon, (c) deposition of electrically insulating layer, followed by the microheater line, and (d) SEM image of fabricated heater line on the back side of porous silicon wick. Scale bar: (d) 100 μm.

To measure the thermal conductivity with respect to the temperature, the sample was placed on a hot plate, and thermal grease was applied between the sample and the hot plate to minimize thermal contact resistance by eliminating air gaps from the interface. Because the sample on the hot plate was capped with a small box, heat conduction and convection through the air were negligible. As with the sample with a SiO_2 surface on top, errors from the black-body radiation were reported at less than 2% at 1000 K [118]. Therefore, considering the operation temperature range of the TGP device peaks at around 165℃, the radiation effect can be also negligible. The heating frequency from 500 to 10,000 Hz was selected to find the appropriate heating frequency range and the thermal penetration depth was simultaneously calculated to make sure that the penetration length was shorter than the sample thickness. A periodic current of 45 mA passing across the heater line was used for the measurement. The correction factor, which is generally used to minimize error resulting from the use of a given voltage source, was not adopted during the measurement because the resistance of the heater line was much smaller than that of the electric circuit [119]. From this measurement, the thermal conductivity of the bulk silicon placed between heater line and porous silicon and of the porous silicon itself could be obtained from raw 3ω voltage acquired as a function of heating frequency. For the thermal conductivity of the bulk silicon layer, the slope of the heating frequency in logarithmic scale versus the in-phase 3ω voltage in linear scale was used according to the following equation [118]:

$$k = \frac{RI^3}{4\pi L_h}\left(\frac{\partial \ln \omega}{\partial V_{3\omega,in-phase}}\right)\frac{dR}{dT} \tag{5.1}$$

where L_h is the length of the heater line. The term in the round brackets is the inverse slope of the in-phase 3ω voltage in linear scale versus the logarithmic heating frequency. This method is applicable for most single isotropic samples to extract the thermal conductivity from 3ω voltage data. However, it is not suitable for the coherent porous silicon wick structure, which is an anisotropic medium and requires fitting parameters with out-of-phase 3ω voltage data. Therefore, the analytical solution for the average complex temperature rise with heating frequency at 2ω was used to extract the thermal conductivity of the anisotropic porous silicon wick structure as follows [123]:

$$T = \frac{P}{\pi L_h k_y \sqrt{k_{xy}}} \left[\frac{1}{2} \ln\left(\frac{\alpha_y k_{xy}}{b^2} \right) - \frac{1}{2} \ln(\omega) + \tau \right] - i \left(\frac{P}{4 L_h k_y \sqrt{k_{xy}}} \right) \tag{5.2}$$

where P is heating power, b is the half width of the heater line, and the constant τ depends on the thermal contact resistance at the interface between the heater line and the underlying substrate [118,124]. Subscripts x and y refer to the directions parallel (in-plane) and perpendicular (cross-plane) to the heater/substrate interface, respectively (see Fig. 5.7(b)). Equation (5.2) is valid for multilayer films on the substrate. The bottom surface of the porous silicon wick structure was considered as having adiabatic and isothermal boundary conditions, and the effects of heat conduction in the heater line can be negligible. To calculate the temperature rise from the measured 3ω voltage, the resistance along the heater line, the calibrated temperature coefficient of resistance, the current, and the length of the heater line had to be determined. Table 5.1 shows the input parameters to extract the thermal conductivity from experimentally measured out-of-phase 3ω voltage for three layers including SiO_2, bulk silicon, and porous silicon part (Fig. 5.7(c)). Subscripts 1, 2, and 3 in the table refer to the SiO_2, bulk silicon, and porous silicon layer, respectively. The anisotropic ratio of the porous silicon was based on the effective medium theory discussed in subsection 3.1.2. Considering the porous silicon wick structure consists of the array of hollow and cylindrical microchannels in the bulk silicon, the thermal conductivity of the porous silicon wick can be simply approximated as a sum of thermal resistors in parallel connection, as seen in Eq. (3.14), and can be further simplified to $k_{eff,y} = (1-\phi)k_m$ because the k_i (thermal conductivity of air) is nearly equal to 0 in this case. The thermal conductivity along the in-plane direction, which is also insensitive to the alignment of pores [125], can be also modeled as $k_{eff,x} = (1-\phi)/(1+\phi)k_m$ [126,127], resulting in the expression of anisotropic ratio $k_{xy,3} = 1/(1+\phi)$.

Table 5.1 Input parameters to extract the thermal conductivity from out-of-phase 3ω voltage for anisotropic porous silicon wick structure.

Parameter	Value	Unit
Thickness of SiO_2 film, t_1	50	nm
Thermal conductivity (cross-plane), $k_{y,1}$	T dependent	W/m·K
Anisotropy ratio, $k_{xy,1}$	1 (isotropic)	-
Thickness of bulk silicon, t_2	20	μm
Thermal conductivity (cross-plane), $k_{y,2}$	T dependent	W/m·K
Anisotropy ratio, $k_{xy,2}$	1 (isotropic)	-
Thickness of porous silicon, t_3	170	μm
Thermal conductivity (cross-plane), $k_{y,3}$	Target value	W/m·K
Anisotropy ratio, $k_{xy,3}$	0.83 (ϕ=0.2)	-
Resistance of heater line, R	6.83	Ω
dR/dT	0.0237	Ω/K
Length of heater line, L	1.5	mm
Half width of heater line, b	40	μm

5.2.2 Experimental Results

The thermal conductivity of the bulk silicon layer and the porous silicon wick layer was measured simultaneously using the 3ω method; the results are shown in Figure 5.8. The data were extracted from the in-phase (for bulk silicon) and out-of-phase (for porous silicon) 3ω voltage in the temperature range of 25–200 °C, which is the desirable operating temperature of the TGP. As a result, experimentally measured thermal conductivity of the bulk silicon layer with a thickness of 20 μm was decreased as the temperature increased, which can be explained by Umklapp scattering between phonons at high temperatures in the kinetic theory. The measured thermal conductivity was also reasonably matched with the theoretical results calculated using Eq. (3.4) in Chapter 3. The thermal conductivities of the porous silicon wick structure showed smaller values than those of the bulk silicon, which was already expected because of the low thermal conductivity of the inclusion phase in the matrix phase. Using the theoretically estimated thermal conductivity of bulk silicon with a thickness of 170 μm and the Maxwell Garnett approximation (Eq. (3.9)), the thermal conductivity of the porous silicon wick structure was theoretically estimated as shown by the dotted line in Fig. 5.8 showing good agreement with the experimental data measured by the 3ω method. The maximum error between the theoretical and experimental values for thermal conductivities of the porous silicon wick is 15.5% at room temperature. Therefore, the numerical analysis of the overall fluidic/thermal system in Chapter 3 was verified and demonstrated through both theories and experiments.

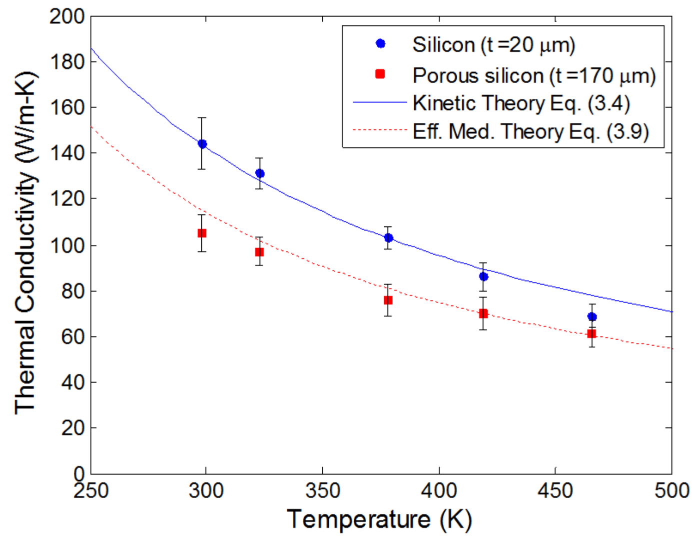

Figure 5.8 Thermal conductivities of bulk silicon (20 μm) and porous silicon wick (170 μm) measured by the 3ω method as compared to computational results calculated by the kinetic theory and effective medium theory.

5.3 Cooling Performance Test

5.3.1 Final Feature of Device

The final TGP device was fabricated by bonding each of the three layers (i.e., evaporator, wick, and reservoir layer) as shown in Figure 5.9. As already investigated from previous chapters, each layer contains novel tailored design structures to perform desirable functions including self-transport of condensed liquids in the evaporator layer, continuous feeding of the coolant in the wick layer, and the rapid refilling of the coolant in the reservoir layer. To achieve these functions in each layer, the triple-spike microstructures in the intermediate/reservoir chamber (Figs. 5.9(a) and (c)) and nanowire-decorated porous silicon wick membrane underneath the evaporator surface (Fig. 5.9(b)) were developed and successfully demonstrated in the evaporator/reservoir layer and wick layer, respectively. For a preliminary experiment, the three layers were tightly bonded by epoxy adhesive (#99393, Loctite, CT) at room temperature. In general, conventional direct bonding [128-130] and intermediate layer bonding techniques, including eutectic [131], polymer [132,133], and solder bonds [134], can be used to bond the silicon-silicon interface. However, direct bonding requires a high annealing temperature (800–1000℃) to increase the bonding strength by means of higher surface energy, and eutectic bonding also needs a temperature higher than the eutectic temperature (400℃ when gold is used as an intermediate layer [135]). Considering that coolant must be kept in the reservoir chamber during the bonding process, these direct bonding techniques are not suitable for the TGP device because the DI water will be completely evaporated at a temperature higher than the boiling point. Although direct bonding using surface treatments including oxygen plasma [136] and argon beam etching [137] at room temperature has been investigated, additional thermal cycles at high temperature (450℃) or vacuum pressure are needed to enhance the bonding strength, which remains an engineering challenge for hermetic sealing of the TGP device, given the presence of coolant.

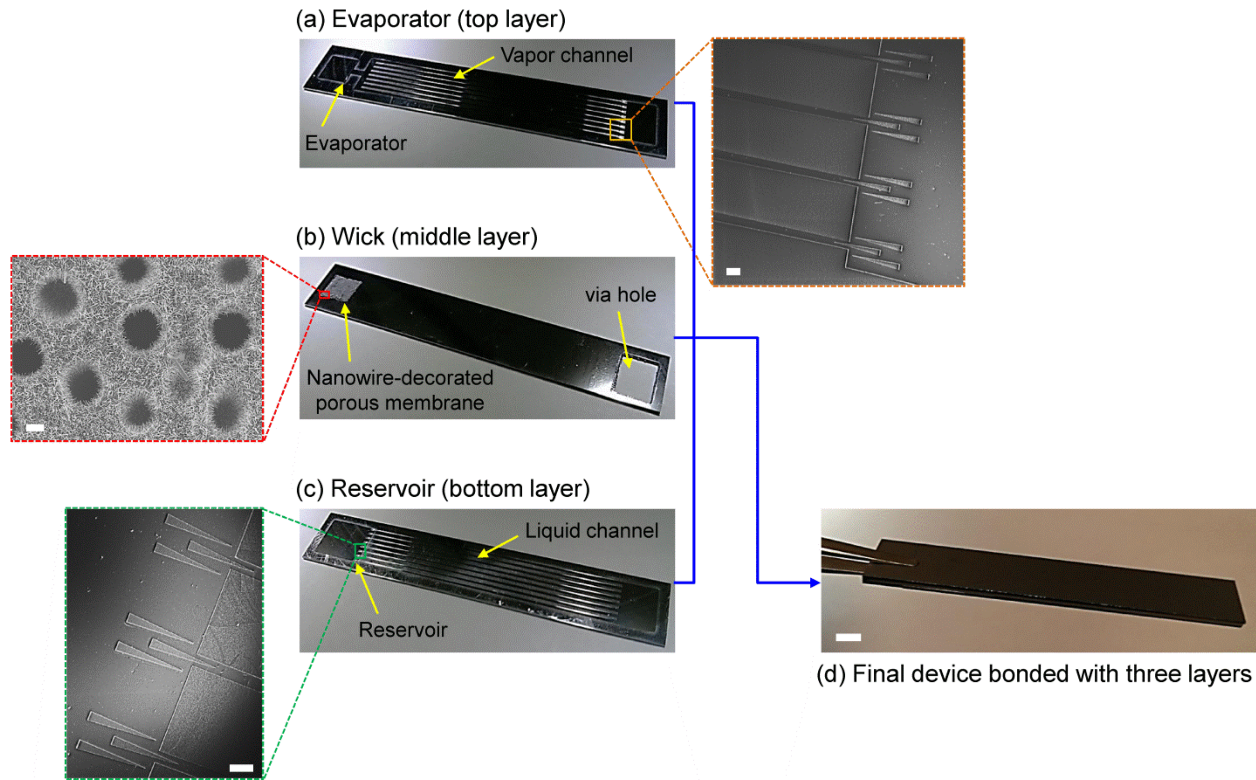

Figure 5.9 Final device feature of the thermal ground plane composed of three layers: (a) evaporator layer with triple-spike microstructure, (b) wick layer with nanowire-decorated coherent porous silicon, and (c) reservoir layer with triple-spike microstructure. Scale bars: (a) 200 μm, (b) 2 μm, (c) 200 μm, and (d) 5 mm.

The final thickness of the bonded TGP device is less than 2 mm because the three 4-inch silicon wafers were stacked. Therefore, it would be helpful to utilize this tiny planar feature of the device as the cooling devices in current electronic packages, which are now getting smaller and smaller as MEMS and nanotechnologies are being developed. Because the total length of the device can also be adjusted and optimized based on the size of the mounted chip, package, and dissipating heat flux, the TGP can provide efficient cooling performance for chip-level electronics. To test the cooling performance of the fabricated device, qualitative and quantitative experiments were simultaneously performed using a high-speed camera and thermocouple modules, as seen in Figure 5.10. A micro ceramic heater (5×5×1.75 mm, MS-M 1000, Sakaguchi E.H Voc Corp, Japan) was mounted on the evaporator site (5×5 mm). The temperature was monitored by a thermocouple wire (L-0044K, Omega Engineering, CT) fixed on the ceramic heater by thermal grease (Thermalcote, Aavid Thermalloy, NH). The current and voltage applied to the heater were kept constant at 0.5 A and 1.6 V, respectively, to provide approximately 130℃, which was slightly lower than the theoretically calculated operating temperature. The high-speed camera was used to observe the movement of two-phase flow in the channel. For the qualitative experiment, the evaporator layer was additionally fabricated on a quartz wafer instead of a silicon wafer to verify the two-phase flow and movement of condensed liquids in the vapor channel visually. Using the same recipe of standard photolithography used for the fabrication of the evaporator layer on the 4-inch silicon wafer, a hard-baked PR mask was patterned on a 4-inch quartz wafer, followed by an anisotropic DRIE (STS-OXIDE MPX APS, SPTS, CA).

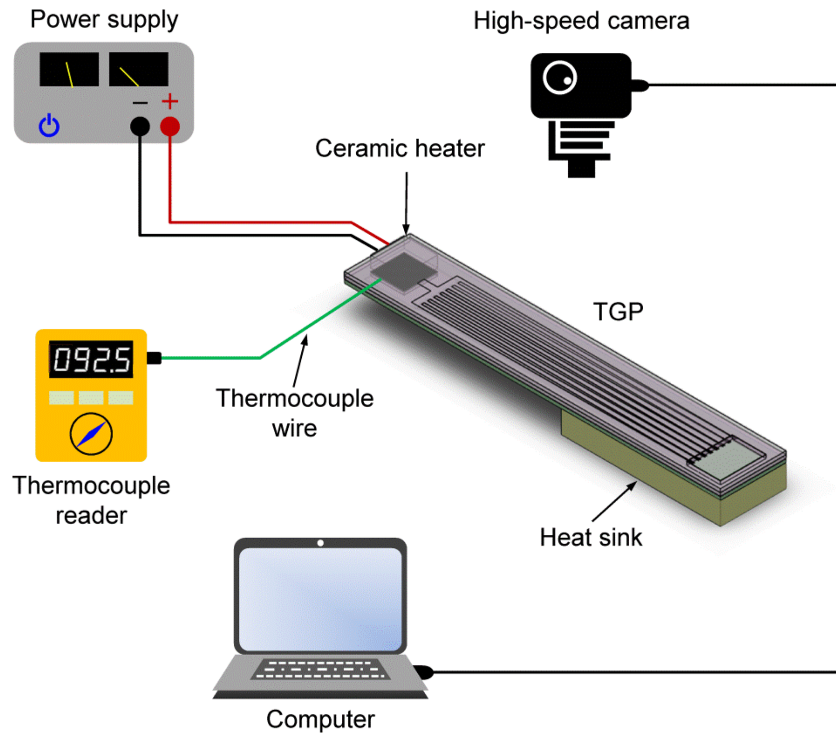

Figure 5.10 Schematic illustration of the experimental setup to analyze both qualitative and quantitative cooling performance of final fabricated thermal ground plane.

5.3.2 Experimental Results

For qualitative analysis, the top surface of the evaporator layer fabricated on a quartz wafer was monitored by the high-speed camera. Figure 5.11 shows the transient movement of both liquid and vapor along the vapor channel during the phase-change of coolant (DI water) with a time interval of 5 s. Once the coolant was evaporated between the evaporator and wick surface, the vapor moved toward the condenser part connected to the copper heat sink. The vapors then returned to the liquid phase where the heat sink was connected. After condensed liquids moved to the intermediate chamber along the tapered vapor channel by capillary force, menisci were separated by triple-spike microstructures and flowed along the sidewalls of the spike structure, which allowed the liquid to be collected on the spike structure, as seen in first three sequential images in Fig. 5.11. The condensed liquids then dropped down to the liquid channels on the reservoir layer and were transported rapidly into the reservoir chamber, which completed the cooling cycle. Considering the nanowire-decorated coherent wick structure, the coolant was fed again to the evaporator surface by enhanced capillary force due to the nanowires. It was also noticeable that the starting position of condensation depended on the position of the heat sink, which was located underneath the TGP and maintained at room temperature. Therefore, the length scales of vapor/liquid channels or the heat sink will affect the cooling performance.

For quantitative analysis of cooling performance, the temperature of the heater was continuously monitored using a thermocouple module during the operation of the TGP. In the experiment, the final feature of all silicon-based TGP (see Fig. 5.9) and water were used as a source of testing device and coolant, respectively. The temperature of the heater was kept

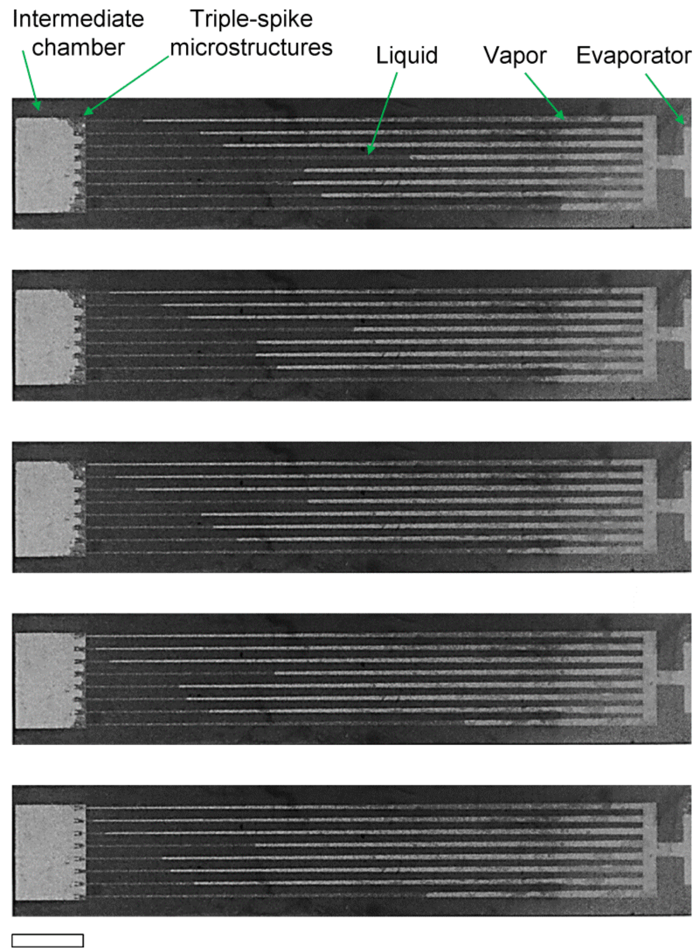

Figure 5.11 Transient phase-change of coolant in the evaporator site and movement of condensed liquid along vapor channels toward the intermediate chamber. The condensed liquids were collected on the triple-spike microstructures and continued to flow into the liquid channels in the reservoir layer. Time interval: 5 s; scale bar: 5 mm.

constant at approximately 130℃. Figure 5.12 shows the temperature change of the micro ceramic heater during cooling by the TGP. The initial temperature rapidly dropped to 97℃ within 75 sec after the heater was mounted on the evaporator site of the TGP because the heat initially spread through the silicon evaporator surface using conduction and was then transferred to liquid coolant underneath the evaporator surface. After this transient change of the temperature, the temperature was maintained at approximately 94–97.5℃, resulting in the steady-state operation of the cooling performance by phase-change. Therefore, the TGP was able to successfully remove, by means of coolant phase-change, the high heat flux generated by the heater. To demonstrate the significant role of the TGP, the device was disassembled from the heater again after 3 min and 40 sec, as seen in Fig. 5.12. As a result, the heater temperature abruptly increased to the initial temperature, showing that the cooling performance was quantitatively verified by the experiment. As discussed earlier, the minimum temperature at steady-state may be much lower when device dimensions and hermetic sealing of the three layers are optimized to minimize coolant leakage during the operation.

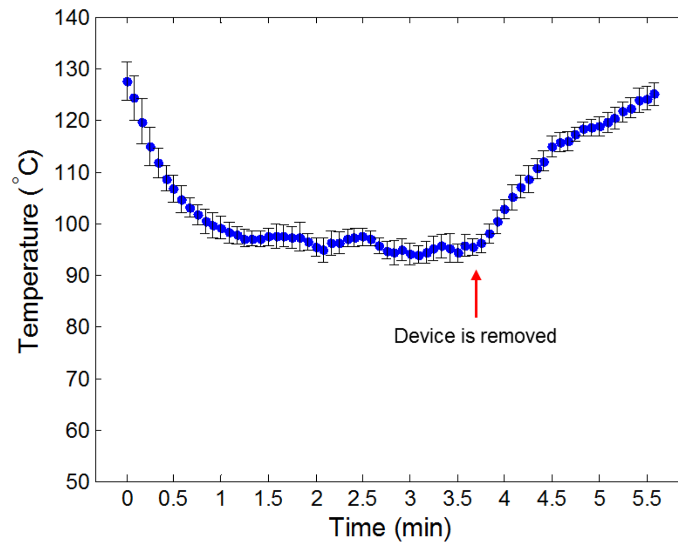

Figure 5.12 Temperature change of the micro ceramic heater during cooling by the fabricated thermal ground plane device. The device was removed from the heater after 3 min and 40 sec to verify the cooling performance of the device.

Chapter 6

Conclusions

In this dissertation, a three-dimensional thermal ground plane was developed in response to the needs of high-power density electronics applications in which heat must be removed as close to the chip surface as possible. The novel design for this planar cooling device was proposed with three key innovations in the evaporator, wick, and reservoir layer to provide enhanced and reliable cooling performance without wick dryout and back flows. For the evaporator and reservoir layer, a combination of a tapered channel and a triple-spike microstructure was designed to break up the pinned meniscus at the end of the vapor and liquid channels. The overall microstructure had three spikes where the main liquid meniscus was separated by the middle spike and then continued to flow between the tapered walls of the middle and side spikes. After condensed liquids overflow into the intermediate chamber, these liquids fell down to the condenser section of the reservoir layer and then be transported again through the liquid channels to the reservoir chamber, which provided self-transporting liquids in channels when the hot chip was turned off, thus preparing the next cycle by collecting coolant in the reservoir chamber before the chip was turned on again. For the wick layer, a nanowire-integrated microporous silicon membrane was developed to overcome the wick dryout problem by driving the coolant out of the channels and spreading the coolant on top of the wick surface with the assistance of extended capillary action. This innovative design used nanowires to extend and enhance the capillary force, especially at the end of the pores where the coolant was pinned and not able to overflow out of the pores. The chronic dryout problem in micro cooling devices could be solved by these innovative designs.

To analyze the proposed thermal-fluid system for desired handling of heat flux, fluid dynamic and phase-change models were used to calculate crucial properties, such as operating pressure, temperature, vapor-liquid interface radius of curvature at wick pore, and rate of bubble formation at the evaporator region. The microscale heat conduction theory derived from traditional Fourier's law with classical size effect and various models from effective medium theory were used to calculate the thermal conductivities of nanowires and porous silicon wick in the cross-plane direction, respectively. The calculated thermal conductivities of zinc oxide showed good agreement with experimental data for bulk sample and the significant reduction as the size of the sample was reduced due to the phonon scattering effects. In the operating temperature of the device, zinc oxide nanowires showed approximately a two times lower thermal conductivity than silicon nanowires of the same dimensions, which provided critical parameters for thermal system analysis. With calculated thermal properties, the thermal resistance network analysis with thermodynamic cycles was performed to understand the thermal behavior in the developed device. The device was then demonstrated with microfabrication techniques, including photoelectrochemical etching to create coherent porous silicon, deep reactive-ion etching to form a thin wick membrane, and hydrothermal synthesis to grow

nanowires on top of the wick membrane. The fabrication processes were described in detail, layer by layer, using either a top-down or a bottom-up approach, which was also accompanied by scanning electron microscope images for characterization of the results.

To demonstrate the cooling performance of the proposed device, the thermal conductivities of the silicon evaporator layer and porous silicon wick in the cross-plane direction, which were calculated theoretically from the kinetic theory and effective medium theory, were measured experimentally by the 3ω technique and compared with the theoretical results. The measured thermal conductivity of the porous silicon wick showed lower values than those of the bulk silicon showing good agreement with the theoretically estimated values and demonstrating the numerical heat transfer analysis of the overall thermal system. For the nanomaterial to extend and enhance the capillary force at the end of the pores, zinc oxide nanowires were synthesized using the vapor-liquid-solid mechanism (vapor phase approach) and hydrothermal mechanism (aqueous approach). The results of the nanowire-integrated porous silicon wick membrane from the two different synthesis methods were compared with respect to the total process time, operating temperature, and quality of nanowires. Wicking performance through the fabricated wick membrane and self-transporting condensed liquids along the microchannel with triple-spike microstructures were also verified with acquired data and captured images. These experimental data were compared with data from the numerical analysis and showed good agreement. Finally, the cooling efficiency and heat removal capability of the fabricated device were demonstrated with a micro ceramic heater, which provided a constant temperature of 130℃. The transient two-phase flow in the evaporator channel and rapid decrease in the heater's temperature were observed during the operation, which demonstrates the developed thermal ground plane was able to successfully remove the high heat flux generated from the hot source using phase-change of the coolant.

Although the three silicon layers were tightly bonded by epoxy adhesive at room temperature to fabricate the final device, it was observed that the strength of the adhesive became weaker as the operating temperature increased, which also accelerated coolant loss to the atmosphere. For future research directions, the cooling performance of the thermal ground plane could be improved by optimum hermetic sealing of the three silicon layers to minimize coolant leakage during the operation. Furthermore, based on theoretical models, smaller wick pore radius (nanopores) and higher porosity may lead to enhanced capillary pressure across the wick membrane and thus extend the application of the thermal ground plane to harsh environments, such as high gravity conditions for avionics. However, because a depth of nanopores will be relatively shallower than that of micropores, and this thin thickness and higher porosity may reduce the mechanical strength of the porous silicon membrane, parametric investigations for pore size, porosity, and depth of the membrane will be needed for harsh environment applications. The length of the nanowires was not optimized in this study, the cooling efficiency and a feeding speed of coolant with respect to different length of the nanowires could be also investigated further. To demonstrate the merit of direct cooling underneath the chip's substrate, high-performance microchips must be fabricated on the evaporator site directly using microfabrication techniques and tested operation by monitoring the chip temperature during cooling performance. This study shows the feasibility of reliable, continuous, and high-performance micro cooling devices using enhanced capillary forces to address the increasing requirements of thermal management for chip-level electronics.

Bibliography

[1] P. K. Schelling, L. Shi, and K. E. Goodson, “Managing heat for electronics,” *Mater. Today*, vol. 8, pp. 30–35, 2005.

[2] S.-S. Hsieh, R.-Y. Lee, J.-C. Shyu, and S.-W. Chen, “Thermal performance of flat vapor chamber heat spreader,” *Energy Convers. Manage.*, vol. 49, pp. 1774–1784, 2008.

[3] S. Narasimhan and J. Majdalani, “Characterization of compact heat sink models in natural convection,” *IEEE Trans. Compon. Packag. Technol.*, vol. 25, pp. 78–86, 2002.

[4] G. Ledezma and A. Bejan, “Heat sinks with sloped plate fins in natural and forced convection,” *Int. J. Heat Mass Transfer*, vol. 39, pp. 1773–1783, 1996.

[5] B. Orel, M. K. G, and A. Krainer, “Radiative cooling efficiency of white pigmented paints,” *Sol. Energy*, vol. 50, pp. 477–482, 1993.

[6] N. M. Nahar, P. Sharma, and M. M. Purohit, “Performance of different passive techniques for cooling building in arid regions,” *Build. Environ.*, vol. 38, pp. 109–116, 2003.

[7] K.-S. Kim, M.-H. Won, J.-W. Kim, and B.-J. Back, “Heat pipe cooling technology for desk PC CPU,” *Appl. Therm. Eng.*, vol. 23, pp. 1137–1144, 2003.

[8] A. Faghri, *Heat Pipe Science and Technology*, Washington, D.C., Taylor & Francis, 1995.

[9] T. J. Lu, “Thermal management of high power electronics with phase change cooling,” *Int. J. Heat Mass Transfer*, vol. 43, pp. 2245–2256, 2000.

[10] M. Ghajar, J. Darabi, and N. Crews Jr, “A hybrid CFD-mathematical model for simulation of a MEMS loop heat pipe for electronics cooling applications,” *J. Micromech. Microeng.*, vol. 15, 313, 2005.

[11] N. S. Dhillon and A. P. Pisano, “Enabling two-phase microfluidic thermal transport systems using a novel thermal-flux degassing and fluid charging approach,” *J. Micromech. Microeng.*, vol. 24, 035021, 2014.

[12] S. Lin, J. Broadbent, and R. McGlen, “Numerical study of heat pipe application in heat recovery systems,” *Appl. Therm. Eng.*, vol. 25, pp. 127–133, 2005.

[13] R. R. Riehi and T. Dutra, “Development of an experimental loop heat pipe for application in future space mission,” *Appl. Therm. Eng.*, vol. 25, pp. 101–112, 2005.

[14] S. Launay, V. Sartre, and J. Bonjour, “Parametric analysis of loop heat pipe operation: a literature review,” *Int. J. Therm. Sci.*, vol. 46, pp. 621–636, 2007.

[15] M. Hamdan, D. Cytrynowicz, P. Medis, A. Shuja, F. M. Gerner, H. T. Henderson, E. Golliher, K. Mellott, and C. Moore, “Loop heat pipe (LHP) development by utilizing coherent porous silicon wicks,” in *Proc. 8th Inter Society Conference on Thermal Phenomena*, 2002, pp. 457–465.

[16] Y. Chen, M. Groll, R. Mertz, Y. F. Maydanik, and S. V. Vershinin, “Steady-state and transient performance of a miniature loop heat pipe,” *Int. J. Therm. Sci.*, vol. 45, pp. 1084–1090, 2006.

[17] S. C. Morris, J. J. Good, and J. F. Foss, “Velocity measurements in the wake of an automotive cooling fan,” *Exp. Therm. Fluid Sci.*, vol. 17, pp. 100–106, 1998.

[18] J.-H. Zhou and C.-X. Yang, “Design and simulation of the CPU fan and heat sinks,” *IEEE Trans. Compon. Packag. Technol.*, vol. 31, pp. 890–903, 2008.

[19] R. Grimes, M. Davies, J. Punch, T. Dalton, and R. Cole, “Modeling electronic cooling axial fan flows,” *J. Electron. Packag.*, vol. 123, pp. 112–119, 2001.

[20] V. G. Pastukhov, Y. F. Maydanik, C. V. Vershinin, and M. A. Korukov, “Miniature loop heat pipes for electronics cooling,” *Appl. Therm. Eng.*, vol. 23, pp. 1125–1135, 2002.

[21] Y. F. Maydanik, “Loop heat pipes,” *Appl. Therm. Eng.*, vol. 25, pp. 635–657, 2005.

[22] A. Basiulis, R. C. Prager, and T. R. Lamp, “Compatibility and reliability of heat pipe materials,” AIAA Paper No. 75-660, 1975.

[23] K. Hijikata, S. J. Chen, and C. L. Tien, “Non-condensable gas effect on condensation in a two-phase closed thermosyphon,” *Int. J. Heat Mass Transfer*, vol. 27, pp. 1319–1325, 1984.

[24] S. Krishnan, S. V. Garimella, and S. S. Kang, “A novel hybrid heat sink using phase change materials for transient thermal management of electronics,” *IEEE Trans. Compon. Packag. Technol.*, vol. 28, pp. 281–289, 2005.

[25] M. K. Sung and I. Mudawar, “Single-phase hybrid micro-channel/micro-jet impingement cooling,” *Int. J. Heat Mass Transfer*, vol. 51, pp. 4342–4352, 2008.

[26] G. E. Moore, “Cramming more components onto integrated circuits,” *Proc. IEEE*, vol. 86, pp. 82–85, 1998.

[27] G. E. Moore, “No exponential is forever: But “forever” can be delayed!,” in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2003, pp. 20–23.

[28] R. Grimes, M. Davies, J. Punch, T. Dalton, and R. Cole, "Towards a thermal Moore's law," *IEEE Trans. Adv. Packag.*, vol. 30, pp. 462–474, 2007.

[29] C. H. Amon, J. Murthy, S. C. Yao, S. Narumanchi, C.-F. Wu, and C.-C. Hsieh, "MEMS-enabled thermal management of high-heat-flux devices EDIFICE: embedded droplet impingement for integrated cooling of electronics," *Exp. Therm. Fluid Sci.*, vol. 25, pp. 231–242, 2001.

[30] K.-H. Chu, Y. S. Joung, R. Enright, C. R. Buie, and E. N. Wang, "Hierarchically structured surfaces for boiling critical heat flux enhancement," *Appl. Phys. Lett.*, vol. 102, 151602, 2013.

[31] C. J. M. Lasance and R. E. Simons, "Advances in high-performance cooling for electronics," *Electron. Cooling*, vol. 11, 2005.

[32] J. Torresola, C.-P. Chiu, G. Chrysler, D. Granners, R. Mahajan, R. Prasher, and A. Watwe, "Density factor approach to representing impact of die power maps on thermal management," *IEEE Trans. Adv. Packag.*, vol. 28, pp. 659–664, 2005.

[33] S. V. Garimella, "Advances in mesoscale thermal management technologies for microelectronics," *Microelectron. J.*, vol. 37, pp. 1165–1185, 2006.

[34] N. S. Dhillon, J. C. Cheng, and A. P. Pisano, "Device packaging technologies for implementing a novel thermal flux method for fluid degassing and charging of a planar microscale loop heat pipe," in *Proc. ASME Int. Mech. Eng. Cong. Exp.*, 2011, pp. 963–971.

[35] N. S. Dhillon, J. C. Cheng, and A. P. Pisano, "Minimizing the wick thickness in a planar microscale loop heat pipe using efficient thermodynamic design," in *Proc. ASME Int. Mech. Eng. Cong. Exp.*, 2011, pp. 1121–1129.

[36] P. Renvoisé, J. W. M. Bush, M. Prakash, and D. Quéré, "Drop propulsion in tapered tubes," *Europhys. Lett.*, vol. 86, 64003, 2009.

[37] M. Mitzbleck and E. Delamarche, "Advanced capillary soft valves for flow control in self-driven microfluidics," *Micromachnies*, vol. 4, pp. 1–8, 2013.

[38] M. I. Mohammed, E. Abraham, and M. P. Y. Desmulliez, "Rapid laser prototyping of valves for microfluidic autonomous systems," *J. Micromech. Microeng.*, vol. 23, 035034, 2013.

[39] H. Cho, H.-Y. Kim, J. Y. Jang, and T. S. Kim, "How the capillary burst microvalve works," *J. Colloid Interface Sci.*, vol. 306, pp. 379–385, 2007.

[40] M. Yao, G. Shah, and J. Fang, "Highly sensitive and miniaturized fluorescence detection system with an autonomous capillary fluid manipulation chip," *Micromachnies*, vol. 3, pp. 462–479, 2012.

[41] H. So, J. C. Cheng, and A. P. Pisano, "Nanowire-integrated microporous silicon membrane for continuous fluid transport in micro cooing device," *Appl. Phys. Lett.*, vol. 103, 163102, 2013.

[42] R. Wang, K. Hashimoto, A. Fujishima, M. Chikuni, E. Kojima, A. Kitamura, M. Shimohigoshi, and T. Watanabe, "Light-induced amphiphilic surface," *Nature*, vol. 388, pp. 431–432, 1997.

[43] R.-D. Sun, A. Nakajima, A. Fujishima, T. Watanabe, and K. Hashimoto, "Photoinduced surface wettability conversion of ZnO and TiO_2 thin films," *J. Phys. Chem. B,* vol. 105, pp. 1984–1990, 2001.

[44] X. Feng, L. Feng, M. Jin, J. Zhai, L. Jiang, and D. Zhu, "Reversible super-hydrophobicity to super-hydrophilicity transition of aligned ZnO nanorod films," *J. Am. Chem. Soc.,* vol. 126, pp. 62–63, 2004.

[45] R. Williams and A. M. Goodman, "Wetting of thin layers of SiO_2 by water," *Appl. Phys. Lett.*, vol. 25, 531, 1974.

[46] H. Kim, H.-B. -R. Lee, and W.-J. Maeng, "Applications of atomic layer deposition to nanofabrication and emerging nanodevices," *Thin Solid Films*, vol. 517, pp. 2563–2580, 2009.

[47] Y. A. Çengel and M. A. Boles, *Thermodynamics: An Engineering Approach*, Boston, MA, McGraw Hill, 2008.

[48] B. R. Munson, T. H. Okiishi, W. W. Huebsch, and A. P. Rothmayer, *Fundamentals of Fluid Mechanics*, Hoboken, NJ, John Wiley & Sons, 2012.

[49] P. G. de Gennes, "Wetting: statics and dynamics," *Rev. Mod. Phys.*, vol. 57, pp. 827–863, 1985.

[50] C. W. Extrand, "Model for contact angles and hysteresis on rough and ultraphobic surfaces," *Langmuir*, vol. 18, pp. 7991–7999, 2002.

[51] C. W. Extrand, “Contact angles and hysteresis on surface with chemically heterogeneous islands,” *Langmuir*, vol. 19, pp. 3793–3796, 2003.

[52] M. Prakash, D. Quéré, and J. W. M. Bush, “Surface tension transport of prey by feeding shorebirds: the capillary ratchet,” *Science*, vol. 320, pp. 931–934, 2008.

[53] G. Chen, *Nanoscale Energy Transport and Conversion: A Parallel Treatment of Electrons, Molecules, Phonons, and Photons*, New York, NY, Oxford University Press, 2005.

[54] C. Dames, *Microscale Conduction*, in the *Heat Conduction* by L. M. Jiji, Springer, 2009.

[55] J. Callaway, “Model for lattice thermal conductivity at low temperature,” *Phys. Rev.*, vol. 113, pp. 1046–1051, 1959.

[56] D. T. Morelli, J. P. Heremans and G. A. Slack, “Estimation of the isotope effect on the lattice thermal conductivity of group IV and group III-V semiconductors,” *Phys. Rev. B*, vol. 66, 195304, 2002.

[57] C. J. Glassbrenner and G. A. Slack, “Thermal conductivity of silicon and germanium from 3°K to the melting point,” *Phys. Rev.*, vol. 134, pp. A1058–A1069, 1964.

[58] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar, “Thermal conductivity of individual silicon nanowires,” *Appl. Phys. Lett.*, vol. 83, pp. 2934–2936, 2003.

[59] R. A. Robie and J. L. Edwards, “Some Debye temperature from single-crystal elastic constant data,” *J. Appl. Phys.*, vol. 37, pp. 2659–2663, 1966.

[60] M. W. Wolf and J. J. Martin, “Low temperature thermal conductivity of zinc oxide,” *Phys. Status Solidi A*, vol. 17, pp. 215–220, 1973.

[61] O. Madelung, *Semiconductors: Data Handbook*, 3rd ed., Springer, 2004.

[62] J. C. M. Garnett, “Colours in metal glasses, in metallic films,” *Philos. Trans. R. Soc. Lond. A*, vol. 203, pp. 385–420, 1904.

[63] D. A. G. Bruggeman, “Berechnung verschiedener physikalischer Konstanten von heterogenen Substanzen. I. Dielektrizitätskonstanten und Leitfähigkeiten der Mischkörper aus isotropen Substanzen,” *Ann. Phys.*, vol. 24, pp. 636–664, 1935.

[64] W. Pabst, “Simple second-order expression: for the porosity dependence of thermal conductivity,” *J. Mater. Sci.*, vol. 40, pp. 2667–2669, 2005.

[65] G. Tichá, W. Pabst, and D. S. Smith, “Predictive model for the thermal conductivity of porous materials with matrix-inclusion type microstructure,” *J. Mater. Sci.*, vol. 40, pp. 5045–5047, 2005.

[66] S. Torquato, *Random Heterogeneous Materials: Microstructure and Macroscopic Properties*, New York, NY, Springer, 2002.

[67] W. J. Parker, R. J. Jenkins, C. P. Bulter, and G. L. Abbott, "Flash method of determining thermal diffusivity, heat capacity, and thermal conductivity," *J. Appl. Phys.*, vol. 32, pp. 1679–1684, 1961.

[68] D. G. Cahill, "Thermal conductivity measurement from 30 to 750K: the 3ω method," *Rev. Sci. Instrum.*, vol. 61, pp. 802–808, 1990.

[69] Y. A. Çengel, *Heat Transfer: A Practical Approach*, Boston, MA, McGraw Hill, 2003.

[70] S. Lee, S. Song, V. Au, and K. P. Moran, "Constriction/spreading resistance model for electronics packaging," in *Proc. ASME/JSME Therm. Eng. Conf.*, 1995, pp. 199–206.

[71] R. C. Chu and R. E. Simons, *Cooling Technology for High Performance Computers: Design Applications*, in the *Cooling of Electronic Systems* by S. Kakaç, H. Yüncü, and K. Hijikata, Springer, 1994.

[72] R. M. Olson, *Essentials of Engineering Fluid Mechanics*, 2nd ed., Scranton, PA, International Textbook Company, 1966.

[73] H. A. Stone, *Introduction to Fluid Dynamics for Microfluidic Flows*, in the *CMOS Biotechnology* by H. Lee, D. Ham, and R. M. Westervelt, Springer, 2007.

[74] V. P. Carey, *Liquid-Vapor Phase-Change Phenomena*, 2nd ed., New York, NY, Taylor & Francis, 2008.

[75] Y. Kagen, "The kinetics of boiling of a pure liquid," *Russian J. Phys. Chem.*, vol. 34, pp. 42–46, 1960.

[76] J. L. Katz and M. Blander, "Condensation and boiling: corrections to homogeneous nucleation theory for nonideal gases," *J. Colloid Interface Sci.*, vol. 42, pp. 496–502, 1973.

[77] M. Blander and J. L. Katz, "Bubble nucleation in liquids," *AIChE J.*, vol. 21, pp. 833–848, 1975.

[78] R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd ed., Upper Saddle River, NJ, Prentice Hall, 2002.

[79] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*, Upper Saddle River, NJ, Prentice Hall, 2000.

[80] V. Lehmann, "The physics of macropore formation in low doped n-type silicon," *J. Electrochem. Soc.*, vol. 140, pp. 2836–2843, 1993.

[81] V. Lehmann and H. Föll, "Formation mechanism and properties of electrochemically etched trenches in n-type silicon," *J. Electrochem. Soc.*, vol. 137, pp. 653–659, 1990.

[82] H. Föll, M. Christophersen, J. Carstense, and G. Hasse, "Formation and application of porous silicon," *Mat. Sci. Eng. R.*, vol. 39, pp. 93–141, 2002.

[83] G. Sun, X. Zhao, and C.-J. Kim, "Fabrication of very-high-aspect ratio microstructures in complex patterns by photoelectrochemical etching," *J. Microelectromech. Syst.*, vol. 21, pp. 1504–1512, 2012.

[84] T. E. Bell, P. T. J. Gennissen, D. DeMunter, and M. Kuhl, "Porous silicon as a sacrificial material," *J. Micromech. Microeng.*, vol. 6, pp. 361–369, 1996.

[85] M. Bail, M. Schulz, and R. Brendel, "Space-charge region-dominated steady-state photoconductance in low-lifetime Si wafers," *Appl. Phys. Lett.*, vol. 82, pp. 757–759, 2003.

[86] M. J. J. Theunissen, J. A. Appels, and W. H. C. G. Verkuylen, "Application of preferential electrochemical etching of silicon to semiconductor device technology," *J. Electrochem. Soc.*, vol. 117, pp. 959–965, 1970.

[87] M. J. J. Theunissen, "Etch channel formation during anodic dissolution of n-type silicon in aqueous hydrofluoric acid," *J. Electrochem. Soc.*, vol. 119, pp. 351–360, 1972.

[88] H. So, K. Lee, N. Murthy, and A. P. Pisano, "All-in-one nanowire-decorated multifunctional membrane for rapid cell lysis and direct DNA isolation," *ACS Appl. Mater. Interfaces*, vol. 6, pp. 20693–20699, 2014.

[89] http://www.ammt.com/support/files/AMMT_PI_MPSB.pdf

[90] G. Sun, J. I. Hur, X. Zhao, and C.-J. Kim, "Fabrication of very-high-aspect ratio micro metal posts and gratings by photoelectrochemical etching and electroplating," *J. Microelectromech. Syst.*, vol. 20, pp. 876–884, 2011.

[91] P. Steiner, A. Richter, and W. Lang, "Using porous silicon as a sacrificial layer," *J. Micromech. Microeng.*, vol. 3, pp. 32–36, 1993.

[92] P. Steiner and W. Lang, "Micromachining applications of porous silicon," *Thin Solid Films*, vol. 255, pp. 52–58, 1995.

[93] W. Lang, P. Steiner, A. Richter, K. Marusczyk, G. Weimann, and H. Sandmaier, "Application of porous silicon as a sacrificial layer," *Sens. Actuators*, *A*, vol. 43, pp. 239–242, 1994.

[94] W. Lang, P. Steiner, U. Schaber, and A. Richter, "A thin film bolometer using porous silicon technology," *Sens. Actuators*, *A*, vol. 43, pp. 185–187, 1994.

[95] H. So, J. C. Cheng, and A. P. Pisano, "Multi-scale pore membrane for continuous, passive fluid transport in a micro cooling device," in *Tech. Dig. Int. Conf. Solid-State Sensors., Actuat. Microsyst.*, 2013, pp. 2197–2200.

[96] H. So, K. Lee, Y. H. Seo, N. Murthy, and A. P. Pisano, "Hierarchical silicon nanospikes membrane for rapid and high-throughput mechanical cell lysis," *ACS Appl. Mater. Interfaces*, vol. 6, pp. 6993–6997, 2014.

[97] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," *Appl. Phys. Lett.*, vol. 4, pp. 89–90, 1964.

[98] S. Kodambaka, J. Tersoff, M. C. Reuter, and F. M. Ross, "Germanium nanowire growth below the eutectic temperature," *Science*, vol. 316, pp. 729–732, 2007.

[99] V. Schmidt and U. Gösele, "How nanowires grow," *Science*, vol. 316, pp. 698–699, 2007.

[100] C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bull.*, vol. 32, pp. 99–104, 2007.

[101] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, vol. 279, pp. 208–211, 1998.

[102] M. H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber, and P. Yang, "Catalytic growth of zinc oxide nanowires by vapor transport," *Adv. Mater.*, vol. 13, pp. 113–116, 2001.

[103] P. Yang, H. Yan, S. Mao, R. Russo, J. Johnson, R. Saykally, N. Morris, J. Pham, R. He, and H.-J. Choi, "Controlled growth of ZnO nanowires and their optical properties," *Adv. Funct. Mater.*, vol. 12, pp. 323–331, 2002.

[104] L. Luo, Y. Zhang, S. S. Mao, and L. Lin, "Fabrication and characterization of ZnO nanowires based UV photodiodes," *Sens. Actuators*, *A*, vol. 127, pp. 201–206, 2006.

[105] C.-Y. P. Yang and L. Lin, "Vertical integration of ZnO nanowires into asymmetric Pt/ZnO/Ti schottky UV photodiodes," in *Proc. Int. Conf. Micro Electro Mech. Syst.*, 2011, pp. 1382–1385.

[106] R. F. Wolffenbuttel and K. D. Wise, "Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature," *Sens. Actuators*, *A*, vol. 43, pp. 223–229, 1994.

[107] L. Vayssieres, K. Keis, A. Hagfeldt, and S.-E. Lindquist, "Three-dimensional array of highly oriented crystalline ZnO microtubes," *Chem. Mater.*, vol. 13, pp. 4395–4398, 2001.

[108] L. Vayssieres, “Growth of arrayed nanorods and nanowires of ZnO from aqueous solutions,” *Adv. Mater.*, vol. 15, pp. 464–466, 2003.

[109] L. E. Greene, M. Law, J. Goldberger, F. Kim, J. C. Johnson, Y. Zhang, R. J. Saykally, and P. Yang, “Low-temperature wafer-scale production of ZnO nanowire arrays,” *Angew. Chem. Int. Ed.*, vol. 42, pp. 3031–3034, 2003.

[110] B. Liu and H. C. Zeng, “Hydrothermal synthesis of ZnO nanorods in the diameter regime of 50 nm,” *J. Am. Chem. Soc.*, vol. 125, pp. 4430–4431, 2003.

[111] M. Law, L. E. Greene, J. C. Johnson, R. Saykally, and P. Yang, “Nanowire dye-sensitized solar cells,” *Nature Mater.*, vol. 4, pp. 455–459, 2005.

[112] J. Kim, J. W. Hong, D. P. Kim, J. H. Shin, and I. Park, “Nanowire-integrated microfluidic devices for facile and reagent-free mechanical cell lysis,” *Lab Chip*, vol. 12, pp. 2914–2921, 2012.

[113] L. Sainiemi, T. Nissilä, R. Kostiainen, R. A. Ketola, and S. Franssila, “A microfabricated silicon platform with 60 microfluidic chips for rapid mass spectrometric analysis,” *Lab Chip*, vol. 11, pp. 3011–3014, 2011.

[114] L. Sainiemi, T. Nissilä, V. Jokinen, T. Sikanen, T. Kotiaho, R. Kostiainen, R. A. Ketola, and S. Franssila, “Fabrication and fluidic characterization of silicon micropillar array electrospray ionization chip,” *Sens. Actuators*, *B*, vol. 132, pp. 380–387, 2008.

[115] T. Nissilä, L. Sainiemi, T. Sikanen, T. Kotiaho, S. Franssila, R. Kostiainen, and R. A. Ketola, “Silicon micropillar array electrospray chip for drug and biomolecule analysis,” *Rapid Commun. Mass Spectrom.*, vol. 21, pp. 3677–3682, 2007.

[116] Z. Chu and S. Seeger, “Superamphiphobic surfaces,” *Chem. Soc. Rev.*, vol. 43, pp. 2784–2798, 2014.

[117] A. Egatz-Gomez, R. Majithia, C. Levert, and K. E. Meissner, “Super-wetting, wafer-sized silicon nanowire surfaces with hierarchical roughness and low defects,” *RSC Adv.*, vol. 2, pp. 11472–11480, 2012.

[118] D. G. Cahill, “Thermal conductivity measurement from 30 to 750 K: the 3ω method,” *Rev. Sci. Instrum.*, vol. 61, pp. 802–808, 1990.

[119] C. Dames and G. Chen, “1ω, 2ω, and 3ω methods for measurements of thermal properties,” *Rev. Sci. Instrum.*, vol. 76, 124902, 2005.

[120] D. G. Cahill, M. Katiyar, and J. R. Abelson, "Thermal conductivity of a-Si:H thin films," *Phys. Rev. B*, vol. 50, pp. 6077–6081, 1994.

[121] S.-M. Lee, D. G. Cahill, and R. Venkatasubramanian, "Thermal conductivity of Si-Ge superlattices," *Appl. Phys. Lett.*, vol. 70, pp. 2957–2959, 1997.

[122] B. Yang, J. L. Liu, K. L. Wang, and G. Chen, "Simultaneous measurements of seebeck coefficient and thermal conductivity across superlattice," *Appl. Phys. Lett.*, vol. 80, pp. 1758–1760, 2002.

[123] T. Borca-Tasciuc, A. R. Kumar, and G. Chen, "Data reduction in 3ω method for thin-film thermal conductivity determination," *Rev. Sci. Instrum.*, vol. 72, pp. 2139–2147, 2001.

[124] F. P. Incropera, D. P. Dewitt, T. L. Bergman, and A. S. Lavine, *Introduction to Heat Transfer*, 5th ed., Hoboken, NJ, John Wiley & Sons, 2007.

[125] D. Song and G. Chen, "Thermal conductivity of periodic microporous silicon films," *Appl. Phys. Lett.*, vol. 84, pp. 687–689, 2004.

[126] A. Jain, Y.-J. Yu, and A. J. H. McGaughey, "Phonon transport in periodic silicon nanoporous films with feature sizes greater than 100 nm," *Phys. Rev. B*, vol. 87, 195301, 2013.

[127] Z. Hashin and S. Shtrikman, "A variational approach to the theory of the effective magnetic permeability of multiphase materials," *J. Appl. Phys.*, vol. 33, pp. 3125–3131, 1962.

[128] U. Gösele and Q.-Y. Tong, "Semiconductor wafer bonding," *Annu. Rev. Mater. Sci.*, vol. 28, pp. 215–241, 1998.

[129] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation," *Proc. IEEE*, vol. 86, pp. 1575–1585, 1998.

[130] M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, "Silicon-to-silicon direct bonding method," *J. Appl. Phys.*, vol. 60, pp. 2987–2989, 1986.

[131] R. F. Wolffenbuttel and K. D. Wise, "Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature," *Sens. Actuators*, *A*, vol. 43, pp. 223–229, 1994.

[132] G. Kräuter, A. Schumacher, U. Gösele, T. Jaworek, and G. Wegner, "Room temperature silicon wafer bonding with ultra-thin polymer films," *Adv. Mater.*, vol. 9, pp. 417–420, 1997.

[133] V. L. Spiering, J. W. Berenschot, M. Elwenspoek, and J. H. J. Fluitman, "Sacrificial wafer bonding for planarization after very deep etching," *J. Microelectromech. Syst.*, vol. 4, pp. 151–157, 1995.

[134] A. Singh, D. A. Horsley, M. B. Cohn, A. P. Pisano, and R. T. Howe, "Batch transfer of microstructures using flip-chip solder bonding," *J. Microelectromech. Syst.*, vol. 8, pp. 27–33, 1999.

[135] S. M. L. Nai, J. Wei, P. C. Lim, and C. K. Wong, "Silicon-to-silicon wafer bonding with gold as intermediate layer," in *Proc. Electronics Packag. Tech. Conf.*, 2003, pp. 119–124.

[136] O. Zucker, W. Langheinrich, and M. Kulozik, "Application of oxygen plasma processing to silicon direct bonding," *Sens. Actuators*, *A*, vol. 36, pp. 227–231, 1993.

[137] H. Takagi, K. Kikuchi, R. Maeda, T. R. Chung, and T. Suga, "Surface activated bonding of silicon wafers at room temperature," *Appl. Phys. Lett.*, vol. 68, pp. 2222–2224, 1996.