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RIVERSIDE

Electrostatic Discharge Protection and Circuits for Ultrasonic Imager-on-Chip

A Dissertation submitted in partial satisfaction  
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Jian Liu

June 2012

Dissertation Committee:

Dr. Albert Wang, Chairperson

Dr. Roger Lake

Dr. Qi Zhu

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The Dissertation of Jian Liu is approved:

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Committee Chairperson

University of California, Riverside

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*To my family.*

## ABSTRACT OF THE DISSERTATION

Electrostatic Discharge Protection and Circuits for Ultrasonic Imager-on-Chip

by

Jian Liu

Doctor of Philosophy, Graduate Program in Electrical Engineering

University of California, Riverside, June 2012

Dr. Albert Wang, Chairperson

Electrostatic discharge (ESD) is one of the main reasons that cause integrated circuit (IC) reliability problem. Transient high voltage and current released by ESD in a very short time could produce latent damage or permanent breakdown in ICs, which may affect circuit performance, shorten product life time and increase manufacturing and assembling cost. Various ESD protection structures have been developed to protect ICs against ESD stress. However, with the advancement of IC technology and the increasing applications of mobile electronics, ESD protection design is facing severe challenges.

This dissertation presented two novel ESD protection structures. One is a very-low-triggering-voltage dual-direction silicon-controlled rectifier (VLTdSCR) with adjustable ESD critical parameters and dual-polarity high ESD protection ability, as well as insignificant ESD-induced parasitics. The other one is a new nano crossbar ESD protection device consisting of the  $\text{Si}_x\text{O}_y\text{N}_z$  composite, as dielectric, and two

metal layers, as top and bottom electrodes. This device has insulator between electrodes and hence extremely-low leakage current, ideal for mobile applications where power consumption is a great concern.

Among all the medical imaging technologies, pulse-echo ultrasonic imaging system features low risk, low cost and real time scan, etc. It interprets the reflected ultrasonic waves to build clear inner image of human body or tissues to aid doctor's diagnosis. In recent years, the portability of ultrasonic imaging system is attracting the attention of public, for its promising applications in harsh environments, such as rural villages or battlefields where stable power supply is usually not available.

In this dissertation, the concept of ultrasonic imager-on-chip (UIC), integrating all the function modules in traditional ultrasonic imaging system onto one die, is proposed. It has the advantages of low cost, high power efficiency and great degree of mobility. UIC system architecture, design challenges and reliability issues, especially ESD protection, are discussed, too. A high-voltage pulse generator, as the driver of ultrasonic transducer and usually fabricated in HV process, is designed in a low-voltage (LV) silicon-on-insulator complementary-metal-oxide-semiconductor (SOI CMOS) technology based on an RC-biasing stacked LV device topology, demonstrating the idea of UIC system integration.



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## **Chapter 1 Introduction to ESD Protection**

### **1.1 ESD Phenomenon and ESD Protection for IC**

Electrostatic discharge (ESD) phenomenon was found by the ancient people long time ago: rubbing the leather with amber will enable the amber to attract small and light objects, even generate electric sparks if the rubbing time is long enough. The reason for this is that the electron transferring between objects due to friction will generate net electrostatic charge and electrostatic potential in the objects. When two objects with different electrostatic potentials get close enough or contact, electrostatic discharge will occur, meanwhile producing transient high voltage or current in a very short time.

In the last 40 years, with the development of integrated circuit (IC) which integrates thousands of electronic cells and function circuits into a small die on a silicon substrate, ESD has gained more and more attentions both in academic and industry, because the small ICs are extremely sensitive and vulnerable to the high voltage and current generated by ESD [1]. Transient ESD high voltage usually causes IC dielectric breakdown, while ESD high current often generates massive heat in silicon and finally burn down the ICs, as shown in Figure 1.1. Up to billions of dollars loss is caused by ESD damage in IC industry every year.

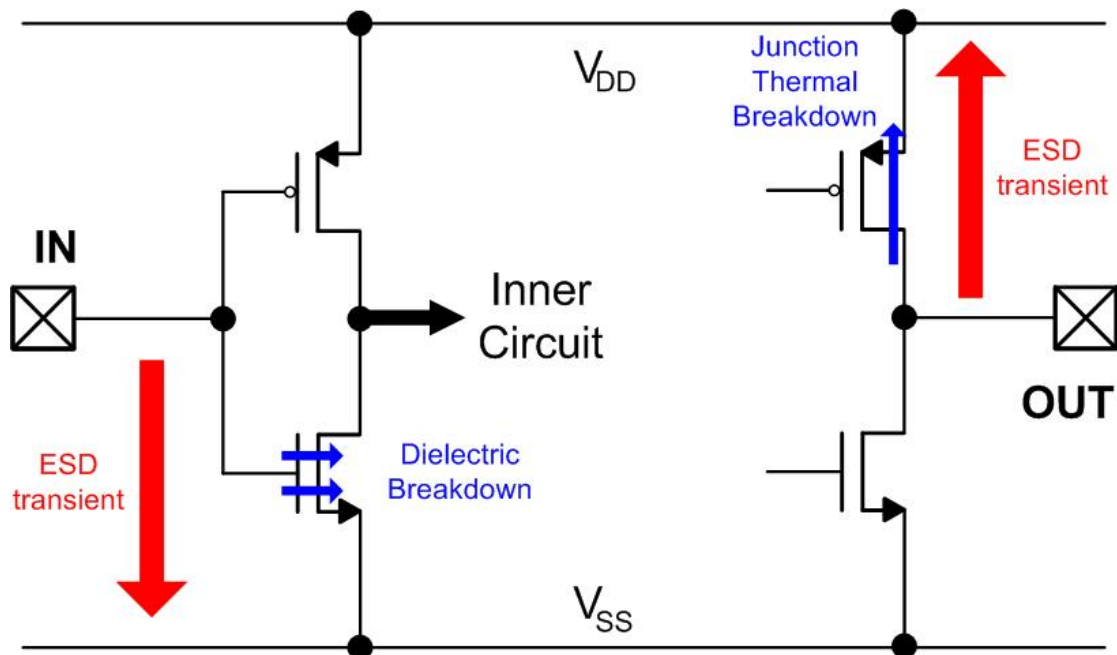


Figure 1. 1 ESD could produce severe damages to ICs.

Different measures and standards were developed and applied in the whole process of IC manufacturing, assembling, verification and transportation, to prevent the increasing cost because of ESD damage. In addition, various off-chip and on-chip ESD protection structures and solutions were designed and employed in ICs to handle the ESD transient high voltage and current. However, in recent years when the IC characteristic size has been reduced to deep-sub-micron level, ESD protection design in ICs is facing all sorts of challenges: thinner gate oxide leads to lower dielectric breakdown voltage and cause gate oxide more vulnerable to ESD high voltage; shallower P+ or N+ junction fails to conduct ESD high current into the deep substrate and hence worsen the heat dissipation; shallow trench isolation (STI) technology replaces previous field oxide (FO), as well as the adoption of light-doped

drain (LDD) technology, making some traditional ESD protection structures less effective or invalid, as presented in Figure 1.2.

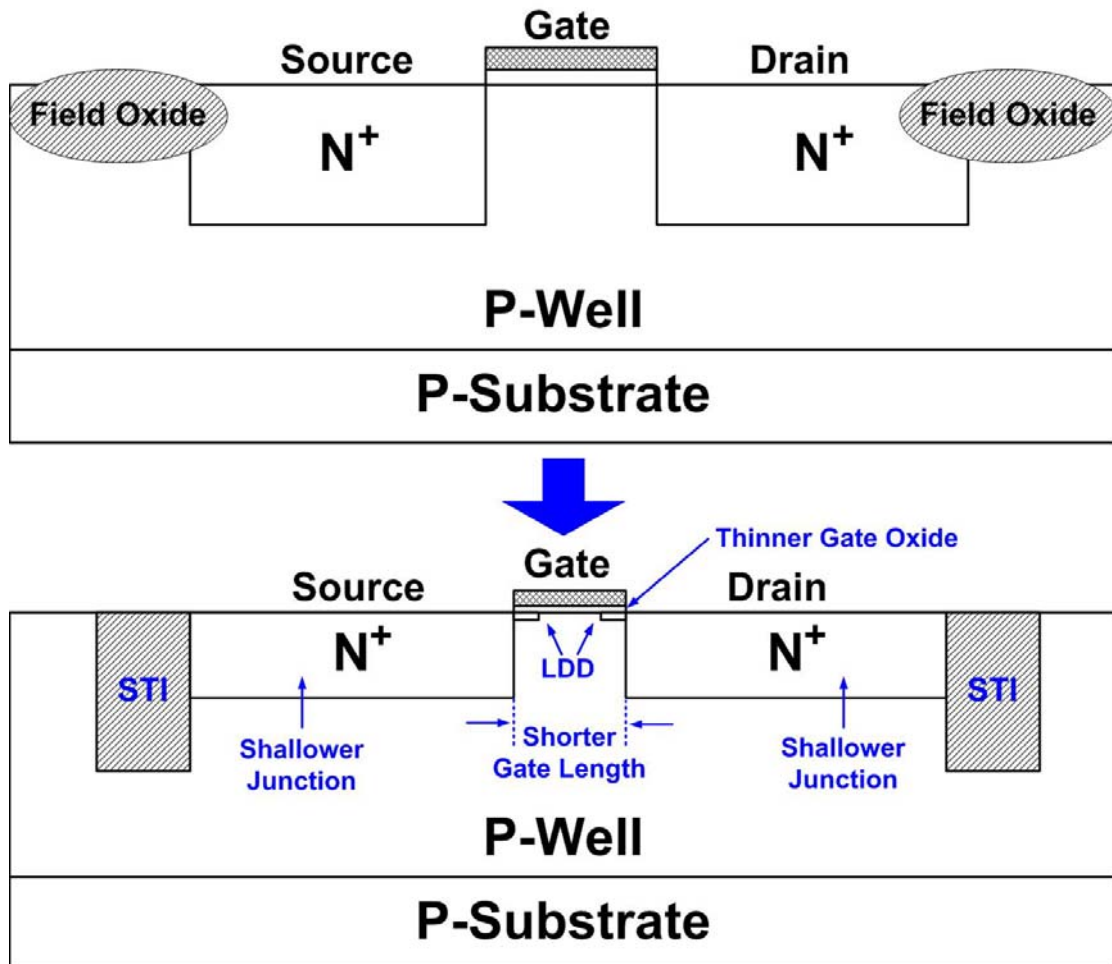


Figure 1. 2 IC technology progresses bring new challenges to ESD protection design in ICs.

Moreover, with the development of radio frequency (RF) and high-speed mixed-signal ICs, the ESD-induced parasitic effects, such as parasitic ESD capacitor ( $C_{ESD}$ ), parasitic ESD resistor ( $R_{ESD}$ ) and extra noises, have severely influenced the performance of the ICs being protected [2]. To provide sufficient ESD protection level while reduce ESD-caused circuit performance degradation has become a very important topic for the ESD protection design in ICs.

## 1.2 ESD Protection Principles

### 1.2.1 ESD Protection Aims and Full-Direction ESD Protection Strategy

All ESD protection structures or circuits in integrated circuit system aim to realize two functions during ESD stressing: provide low-resistance ESD current shunting path, to prevent thermal damage in circuits generated by high ESD current, and clamp ESD voltage surging at pads to safe level, to avoid dielectric breakdown, especially for MOS gate oxide. Besides providing dependable ESD protection to the circuits, ESD protection structures should also avoid inducing too much parasitic effects, such as parasitic capacitance and extra noises, into the circuits and affect the function of circuits, especially for high-speed or high-frequency applications.

A complete full-direction ESD protection strategy is necessary to protect the whole chip against transient ESD pulses from different directions [3]. As shown in Figure 1.3, for a simple circuit with four ports, IN, OUT, power supply  $V_{DD}$  and ground  $V_{SS}$ , the ESD protection in the circuit should provide ESD protections in the directions as follows: positive ESD from I/O to  $V_{SS}$  (PS), negative ESD from I/O to  $V_{SS}$  (NS), positive ESD from I/O to  $V_{DD}$  (PD), negative ESD from I/O to  $V_{DD}$  (ND), positive ESD from  $V_{DD}$  to  $V_{SS}$  (DS) and positive ESD from  $V_{SS}$  to  $V_{DD}$  (SD). The ESD protection structures must be placed in the circuits according to that full-direction ESD protection strategy, in order to provide ESD current shunting path between any two ports.

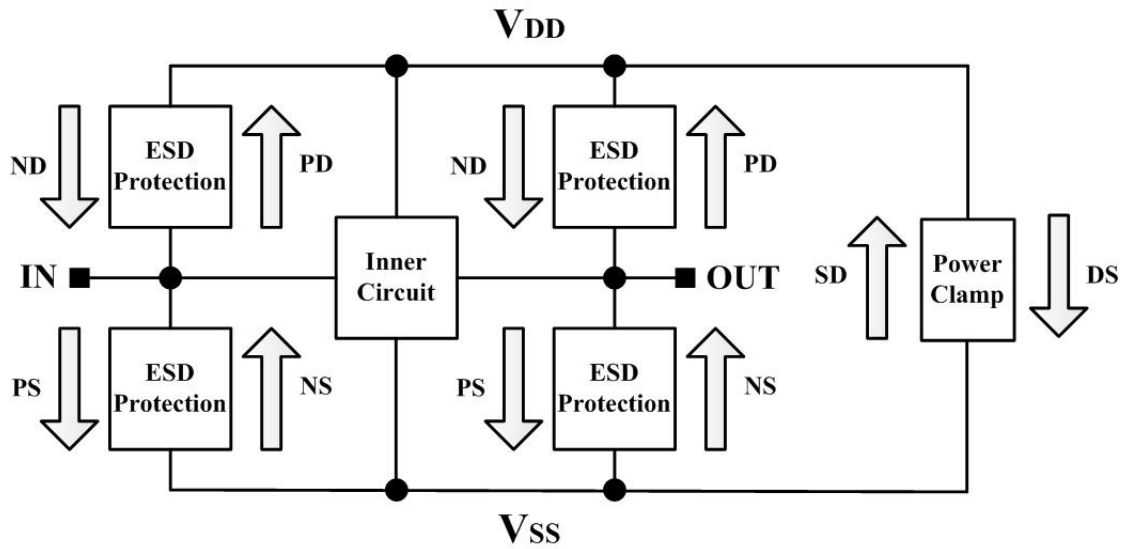


Figure 1. 3 Whole-chip full-direction ESD protection strategy.

### 1.2.2 ESD Critical Parameters and ESD Design Window

The discharging I-V curves of typical ESD protection structures can be classified into two categories: diode-type and bipolar-type. The diode-type ESD protection structure, as shown in the Figure 1.4 (a), will be triggered to discharge ESD current at the "trigger point" after the voltage on device reaches its turn-on voltage, called "triggering voltage" ( $V_{t1}$ ). The discharging resistance of the I-V curve is called "on-resistance" ( $R_{on}$ ). The lower the  $R_{on}$ , the lower the clamping voltage that the ESD protection structure could provide. When the ESD current exceeds its ESD current handle ability, the ESD protection structure will breakdown and cannot recover.

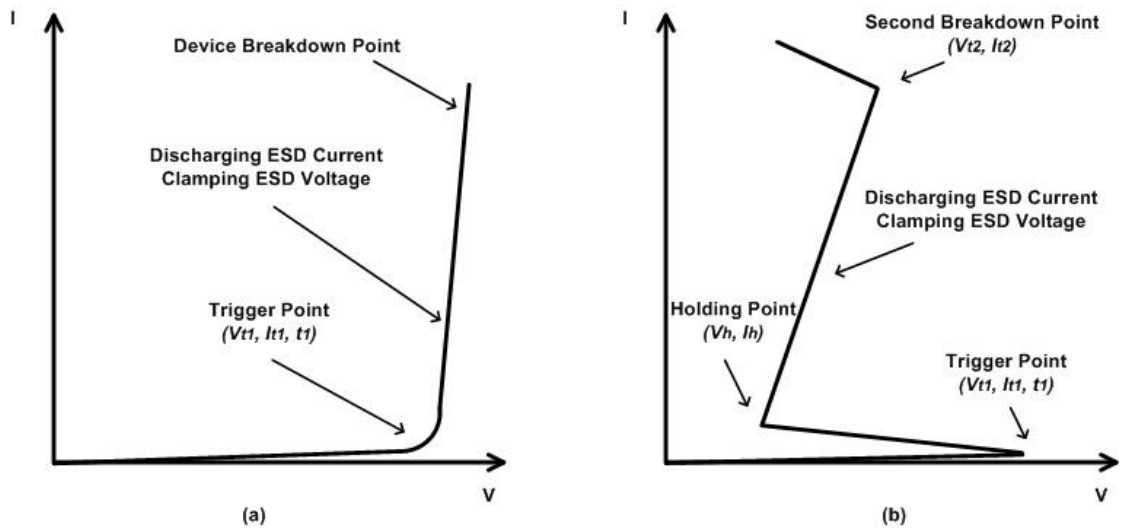


Figure 1. 4 (a) diode-type and (b) bipolar-type discharging IV curves.

On the other hand, as shown in Figure 1.4 (b), when the ESD voltage stress on the bipolar-type ESD protection structure reaches its trigger point, instead of discharging ESD current immediately, it will firstly go into a state of negative resistance until the device voltage reduces to the holding voltage " $V_h$ ", or holding point. This behavior, also known as "snapback", will clamp the ESD voltage on device to a low level and hence protect the inner circuits from dielectric breakdown. After holding point, the ESD protection structure begins to discharge ESD current in a low- $R_{on}$  state until it reaches the device thermal breakdown, or second breakdown. The voltage at the second breakdown is called " $V_{t2}$ ", while the current at the second breakdown is called " $I_{t2}$ ".

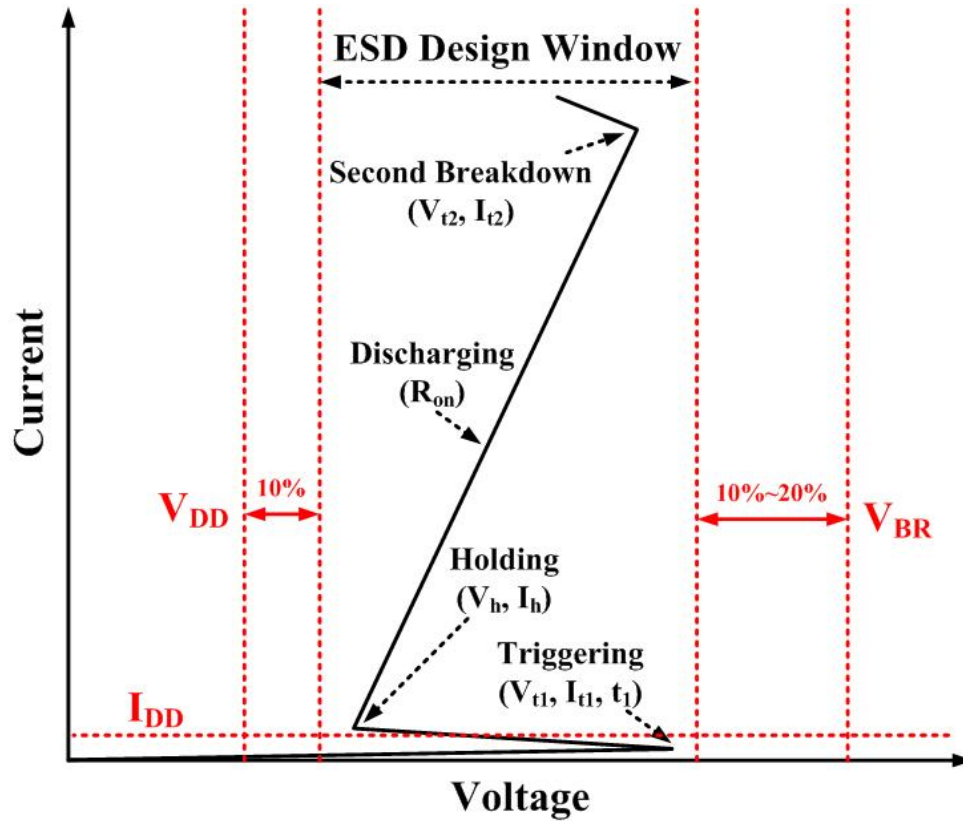


Figure 1. 5 ESD Design Window.

The triggering voltage, current and time ( $V_{t1}$ ,  $I_{t1}$  and  $t_1$ ), holding voltage and current ( $V_h$  and  $I_h$ ), discharging on-resistance ( $R_{on}$ ), and second breakdown voltage, and current ( $V_{t2}$ ,  $I_{t2}$ ), are all critical feature parameters of ESD protection structures. As illustrated in Figure 1.5, the region between inner circuit breakdown voltage ( $V_{BR}$ ) and power supply voltage ( $V_{DD}$ ) with proper safety margins (at least 10%), with current bounded by the total on-chip supply current ( $I_{DD}$ ), is called “ESD Design Window”, which must be followed in practical ESD protection designs.

$V_{t1}$  has to be less than  $V_{BR}$  because the ESD protection structure should be able to turn on before the inner circuit is broken by the ESD stress, while  $V_{t1}$  also needs to



be higher than  $V_{DD}$  since the ESD protection structure should be kept off during inner circuit normal operation. In addition, the restrictions to ESD protection structure  $V_h$  and  $I_h$  are the requirements of latch-up immunity. To prevent ESD protection structure causing any latch-up issues, this rule about I-V curve holding point must be followed. Similar to  $V_{t1}$ ,  $V_{t2}$  has also to be less than  $V_{BR}$  to avoid any breakdown in inner circuits. Moreover,  $I_{t2}$ , the second breakdown current of the ESD protection structure, is the highest current that semiconductor P-N junction can maintain, which can be used to represent the structure ESD protection level. The higher the  $I_{t2}$ , the higher the ESD protection level device could provide. The other critical ESD protection design specs is to ensure that the triggering time for ESD protection structure ( $t_1$ ) is less than the typical rising time ( $t_r$ ) of incoming ESD pulse waveforms per given testing standards, i.e.,  $t_1 < t_r$ . That means the ESD protection device should be fast enough to turn on during ESD transient.

### **1.3 ESD Stress Models and Test Methods**

To better study the ESD phenomenon in different environments with all kinds of discharging speeds and peak current levels, various ESD stress models were developed and standardized. ESD stress models summarized the features of ESD stresses in real world and could reproduce similar ESD damages on the IC dies and parts.

### 1.3.1 Human Body Model

Human body model (HBM) is one of the most-widely adopted ESD stress models in both academic and industry. HBM represents the process that the electrostatic charges storing in human body, possibly generated by triboelectrification between clothes and skins or other factors, discharge to ground through IC parts when human body make a contact with the pins of the IC parts. This human body discharging process usually lasts several hundred nanoseconds (nS) and the peak current could reach to several amperes (A). The heat produced by the human body discharging current will cause thermal breakdown damage in the IC parts if proper on-chip ESD protection structures are not available.

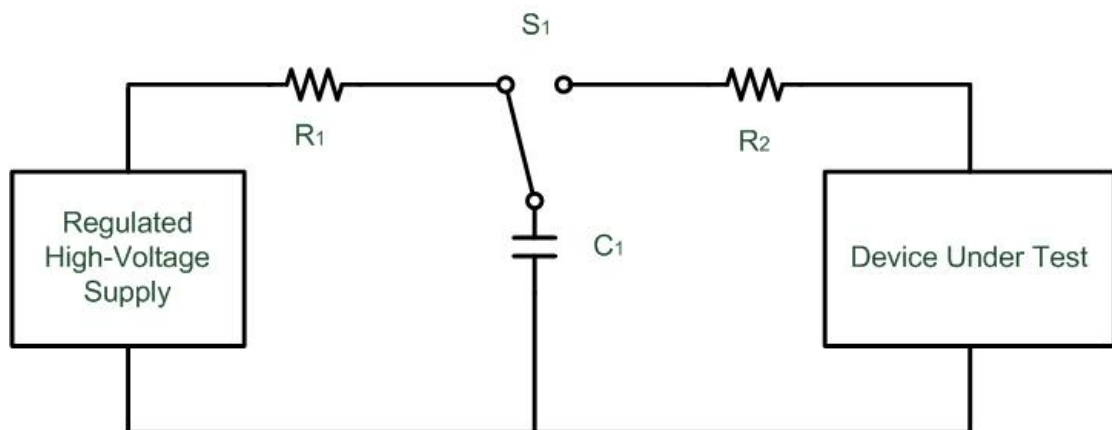


Figure 1. 6 HBM equivalent circuit.

Many organizations have developed standards of HBM. Figure 1.6 shows the HBM test equivalent circuit from the HBM standard of MIL-STD-883E Method 3015.7 [4]. The HBM equivalent discharging circuit is composed of a 100pF capacitor  $C_1$  and

a  $1500\Omega$  resistor  $R_2$  in series, representing the human body parasitic capacitance and resistance, respectively. When the switch  $S_1$  is on the left, the voltage value stressed on the capacitor  $C_1$  is the HBM stress level. The capacitor  $C_1$  is charged with electrostatic charges through a resistor  $R_1$  of  $1\sim 10\text{ M}\Omega$  at this moment. Then it will discharge through the resistor  $R_2$  after the switch  $S_1$  moves to the right.

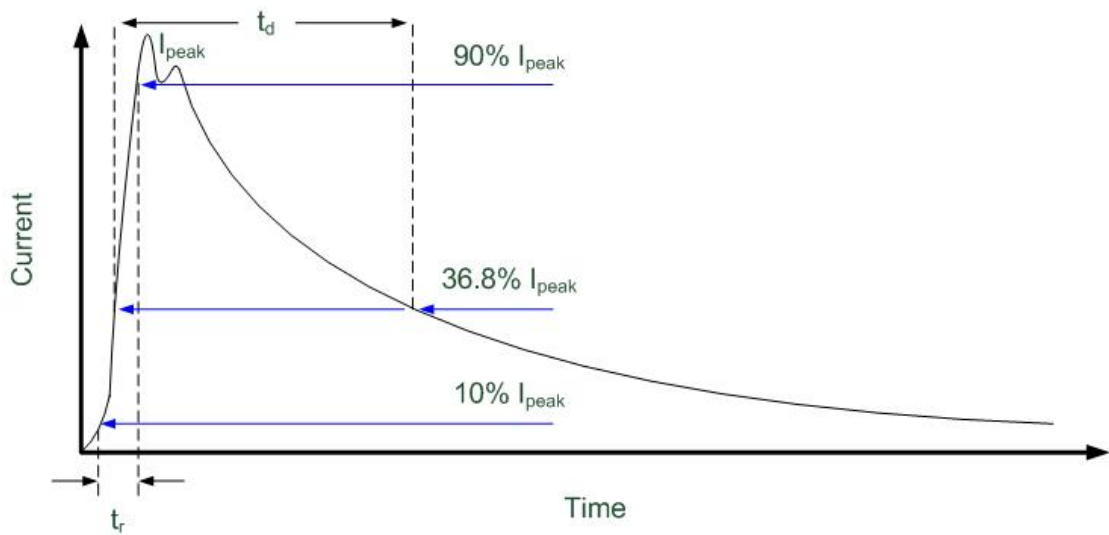


Figure 1. 7 Typical HBM current waveform.

Typical HBM discharging current waveform, defined in ESD Association HBM standard [5], has the main features as follows: pulse rise time ( $t_r$ ) is between  $2 \sim 10\text{ nS}$ ; pulse duration time ( $t_d$ ) is around  $150\text{ nS}$ , as shown in Figure 1.7. Commercial HBM ESD testers must follow these rules of waveform, and waveform verification has to be done before every HBM test begins.

### 1.3.2 Machine Model

Machine model (MM) is used to simulate the ESD event that when IC parts contact the metal surface of machines in IC manufacturing and assembling factories, the electrostatic charges in machines will discharge through low-R metal surface to IC parts. The equivalent circuit of MM tester from ESDA MM standard is shown in the Figure 1.8 [6], which contains a 200pF capacitor  $C_1$  in the MM pulse generator and zero discharging resistance, leading to a high-peak discharging current within scores of nanoseconds even though a relative low voltage level is applied. As also stated in the ESDA MM standard, the performance of MM testers are largely impacted by the parasitic capacitance and inductance, often producing an oscillating current waveform in time domain.

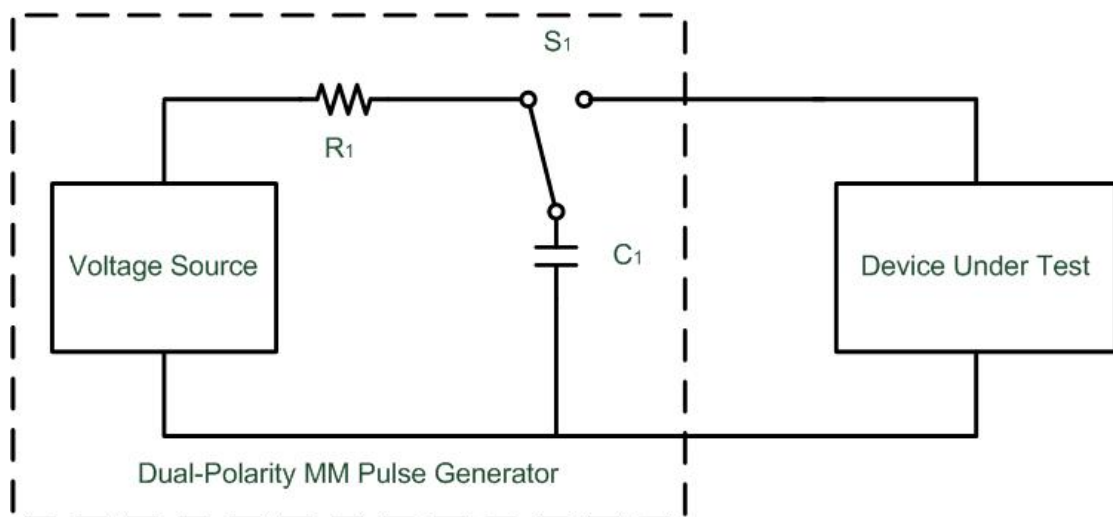


Figure 1. 8 MM test equivalent circuit.

### 1.3.3 Charged Device Model

Charged device model (CDM) is totally different from both the HBM and MM mentioned above. The CDM discharging process is not an outside electrostatic source discharging to ground through some IC part pins any more, but the electrostatic charges, accumulated inside the part itself, discharging through its own pin when this pin is connected to ground or any conductive object. CDM discharging current is very fast and high-peak, and the whole CDM discharging event usually only lasts for several nS. The CDM discharging current waveforms are influenced by many factors, such as the IC part package size and material, which decides the total equivalent CDM capacitor and the electrostatic charges storing inside the IC part [7].

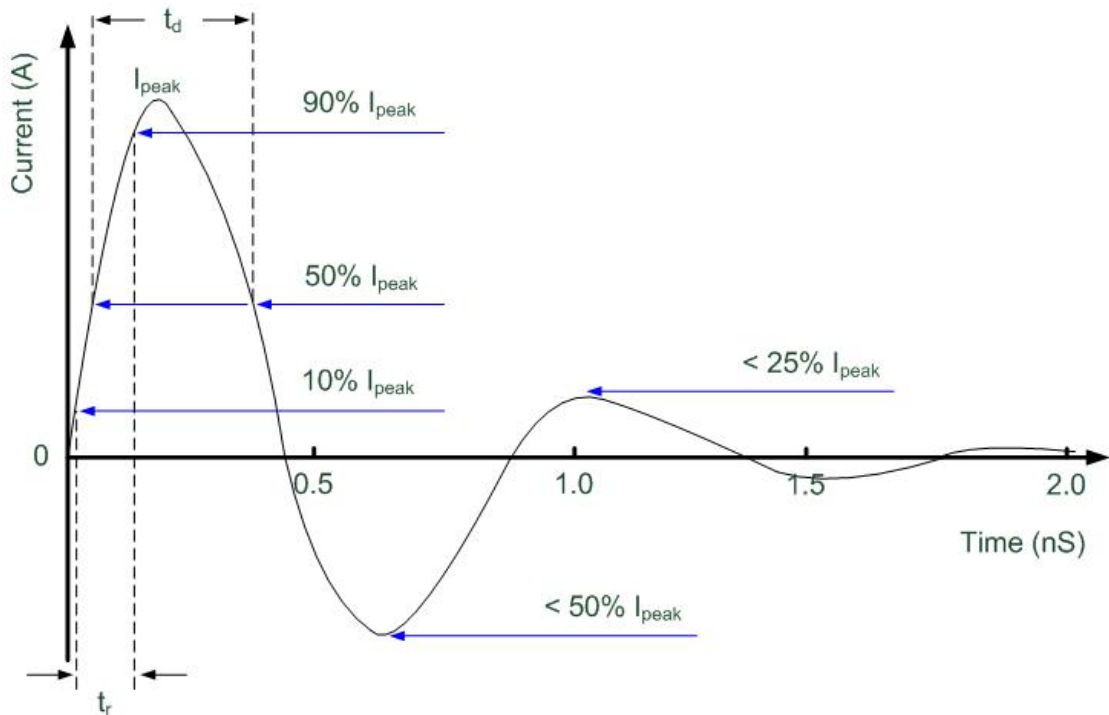


Figure 1. 9 CDM discharging waveform under a 3.5GHz bandwidth measurement system.

A typical CDM discharging waveform under a 3.5GHz bandwidth measurement system is presented in Figure 1.9 based on the ESDA CDM standard [7]. The standard also points out that with a 4pF verification module, the pulse rise time  $t_r$  has to be less than 200pS, while the pulse duration time  $t_d$  has to be less than 400pS. In addition, when the charged voltage is 500V, the CDM waveform peak current  $I_{peak}$  should be 7.5A. This fast and large CDM ESD current will generate high voltage at IC part pins and cause dielectric breakdown damage to the IC parts if the ESD protection in the IC part cannot response rapidly.

#### **1.3.4 Transmission Line Pulse Test**

For the common ESD stress models, such as HBM, MM and CDM, the only information after those tests is the IC part passed or failed at certain ESD level. No more details can be extracted. Different from those ESD stress models, Transmission line pulse (TLP) test, first being introduced into ESD testing in 1985 [8], has become a very important tool to characterize the ESD protection structures behavior during transient ESD pulses.

A typical TLP test system [9][10], as shown in Figure 1.10, employs a short transmission line cable discharging to generate a series of ESD-like current and voltage square waveforms in different levels, and then force those waveforms successively into the device under test (DUT) through 50 $\Omega$  transmission line cable. By

monitoring and sampling the voltage and current waveforms on the DUT after each pulse, a series of voltage and current data points are obtained. In the meanwhile, after each TLP pulse zapping, a DC leakage current test will be done to check if the DUT has been broken by the TLP ESD-like waveform. All the data obtained above will be used to draw the characteristic I-V curve of DUT under ESD stresses.

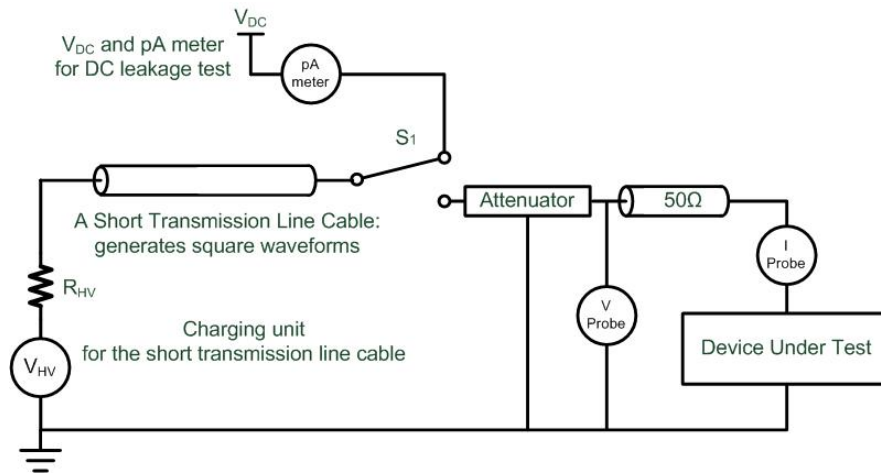


Figure 1.10 A typical TLP testing system scheme.

Usual commercial TLP testers will produce HBM-like pulses which have  $t_r$  of 10nS and  $t_d$  of 100nS, which could be used to characterize HBM features of ESD protection devices. To evaluate or predict the DUT performance under extremely-fast pulses such as CDM ESD, very-fast transmission line pulse (VF-TLP) tester is designed based on the same mechanism as that of TLP tester [9], but with much faster and shorter pulses. The pulse rise time  $t_r$  and pulse duration time  $t_d$  of current VF-TLP testers could be as low as 100pS and 1nS, respectively, consistent with the CDM waveforms defined by the standards [11].

## 1.4 Basic ESD Protection Structures

Various ESD protection structures have been developed and applied in different circuits and designs of CMOS technology. However, almost all of them are based on several basic ESD protection structures, which will be introduced in the following sections.

### 1.4.1 Diode and Diode String

Diode contains a P-N junction, as shown in Figure 1.11 (a) and (b), which could be formed by N+/P-Well or P+/N-Well in CMOS IC process. The P+ is used as anode (A), while the N+ is connected as cathode (K). The forward P-N junction (from P to N) has very high current handle ability and low triggering voltage  $V_{t1}$ ,  $\sim 0.65V$ , while reverse P-N junction shows low ESD current handle ability and high turn-on voltage (reversed P-N junction avalanche breakdown voltage,  $V_{AVBR}$ ).

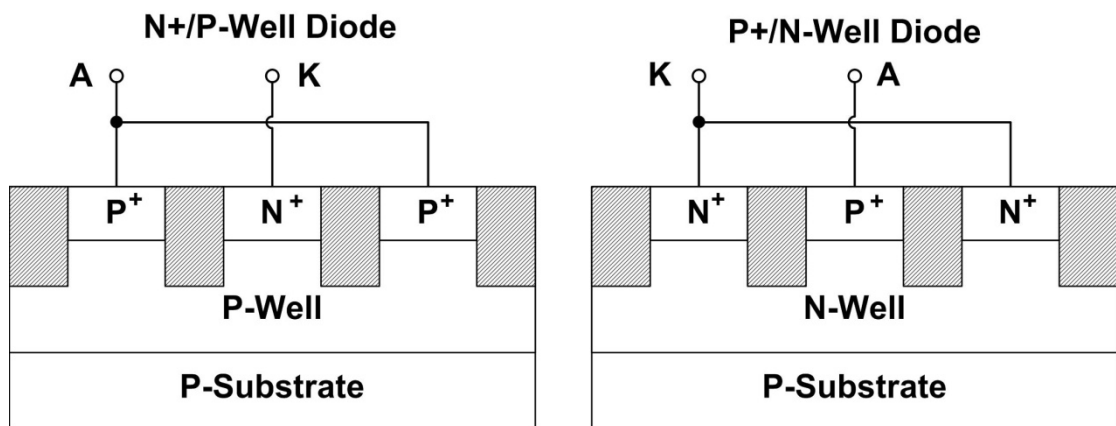


Figure 1. 11 (a) N+/P-Well diode (b) P+/N-Well diode in CMOS IC process.



Thus, diode, as an ESD protection device, is often placed at input and out (I/O) ports because of its low ESD parasitics and high-level ESD protection in the forward direction, as shown in Figure 1.12. At this time, a power clamp will be necessary between the circuit power supply net  $V_{DD}$  and ground net  $V_{SS}$ , which will provide full-direction ESD protection together with those diodes at I/O ports. For example, during ESD zapping from I/O port to  $V_{SS}$  (or from  $V_{DD}$  to I/O ports), the forward diode  $D_{up}$  (or  $D_{down}$ ) plus the power clamp will form the ESD current shunting path  $P_1$  (or  $P_2$ ), because the  $D_{down}$  (or  $D_{up}$ ) avalanche breakdown  $V_{AVBR}$  is much higher than the  $P_1$  (or  $P_2$ ) triggering voltage  $V_{t1,P1}$  (or  $V_{t1,P2}$ ). Based on the "ESD Design Window" concept, the  $V_{t1,P1}$  (or  $V_{t1,P2}$ ), equal to the sum of power clamp  $V_{t1}$  and diode forward  $V_{t1}$ , should be less than inner circuit breakdown voltage  $V_{BR}$ .

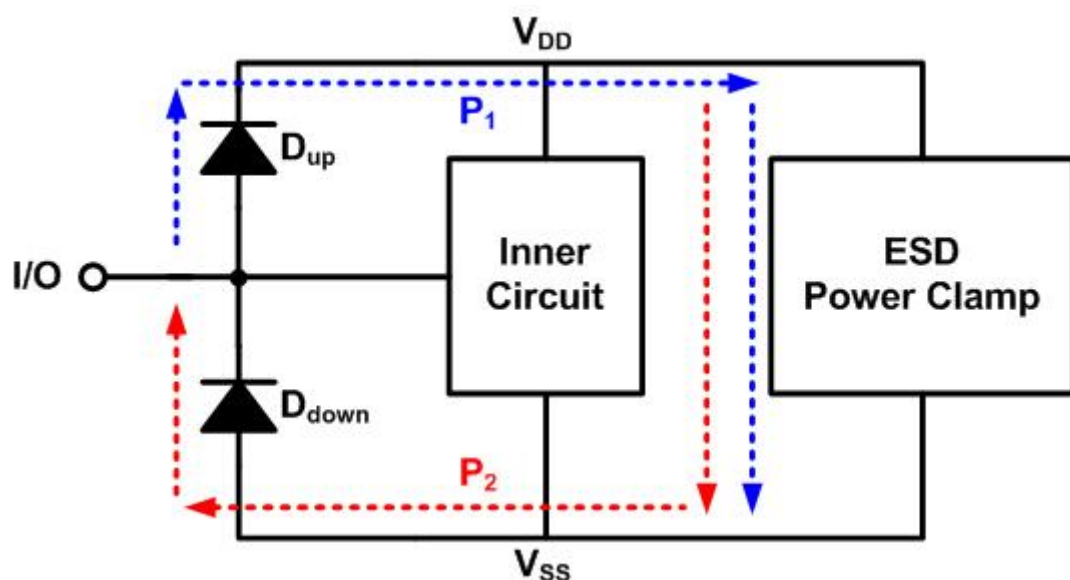


Figure 1. 12 Diodes at I/O ports plus ESD power clamp protection scheme.

Although reverse diode has relatively low ESD protection ability, under some circumstances large-size Zener diode is still used reversely between circuit power supply and ground, serving as a power clamp to discharge the ESD transient current.

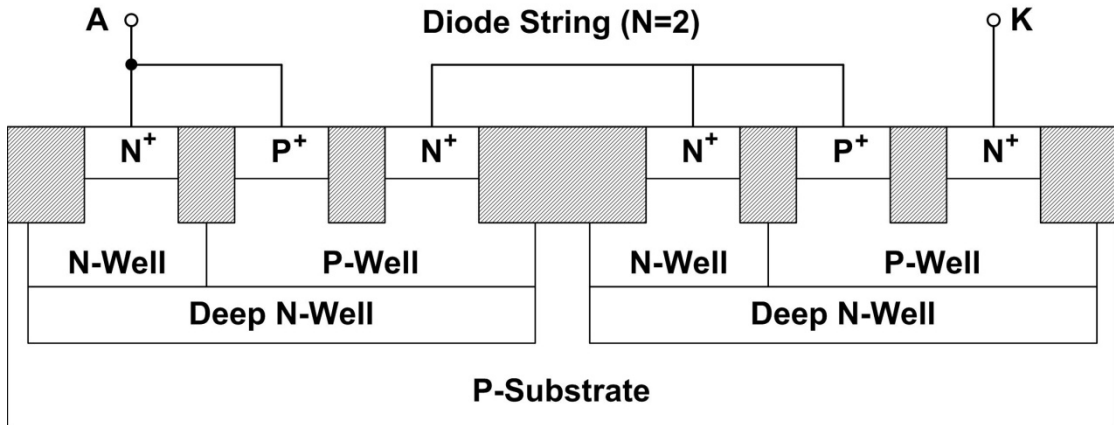


Figure 1.13 X-section of diode string in CMOS technology (N=2).

Figure 1.13 presents a "diode string" ESD protection structure, which is  $N$  ( $N \geq 2$ ) isolated diodes connected in series. Obviously, if those  $N$  diodes in the diode string are all the same, theoretically the diode string total parasitic capacitance will be  $1/N$  of the single diode. However, the total ESD discharging  $R_{on}$  of the diode string will rise to  $N$  times of the original single diode, too. In [12] the relation between the diode string number increase and device total parasitic capacitance reduction was studied, indicating an optimum value for  $N$  is 2 or 3 if also consider the overall layout area. As regular diodes, diode string could be placed at I/O ports to provide low parasitic ESD protection. In addition, it could also be used as a power clamp, whose number of diodes should be decided by the power supply voltage and DC leakage current requirements.

### 1.4.2 Bipolar

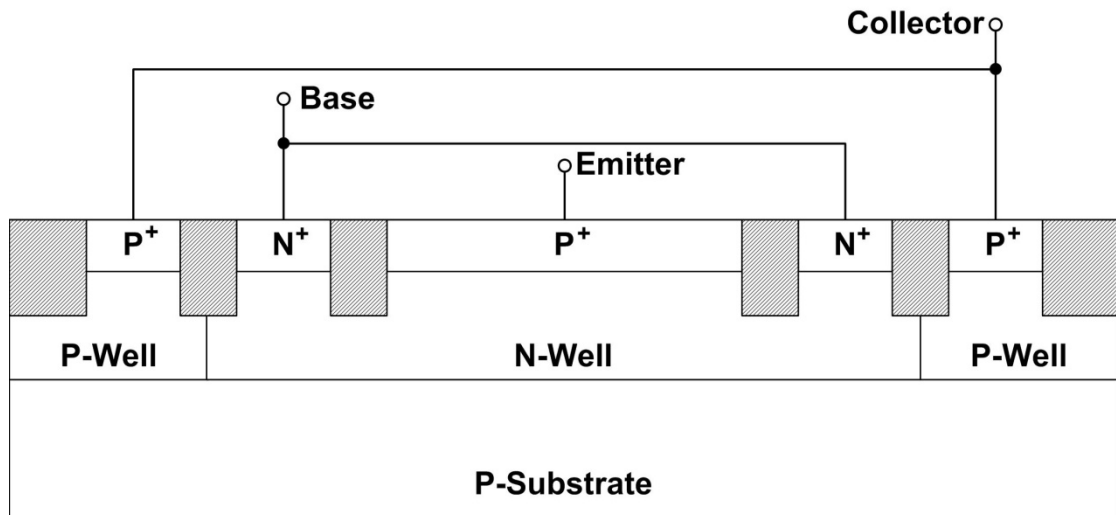


Figure 1. 14 X-section of a vertical PNP bipolar in CMOS process.

In CMOS technology, a vertical PNP bipolar can always be realized, which is composed of emitter (P<sup>+</sup> in middle N-Well), base (middle N-Well with N<sup>+</sup> pick-up ring) and collector (P-Substrate with P-Well and P<sup>+</sup> pick-up ring), as shown in Figure 1.14.

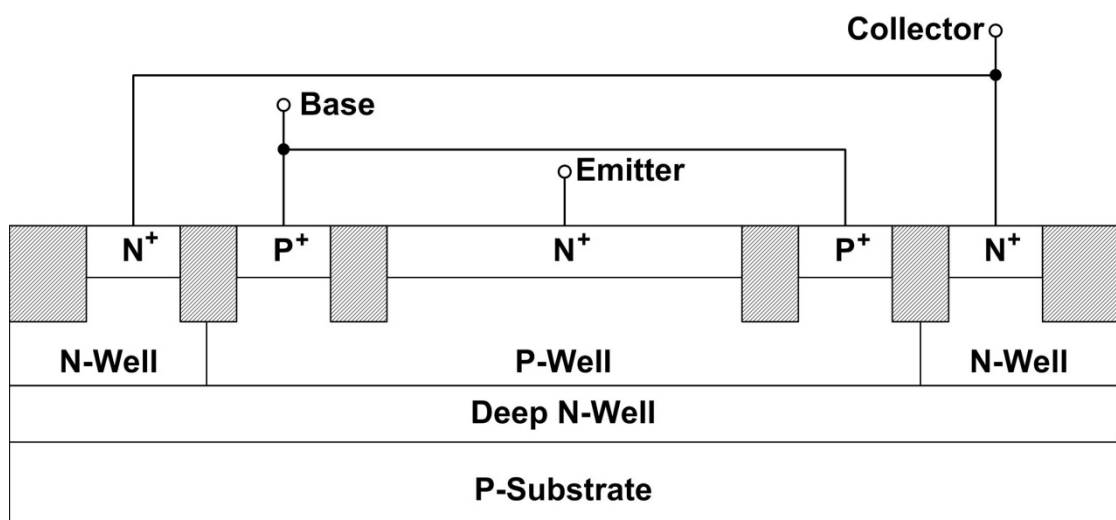


Figure 1. 15 X-section of a vertical NPN bipolar in CMOS process.

For some CMOS technology with Deep N-Well implant, a vertical NPN bipolar is available, too. That NPN bipolar contains emitter (N+ in middle P-Well), base (middle P-Well with P+ pick-up ring) and collector (Deep N-Well with N-Well and N+ pick-up ring), as shown in Figure 1.15.

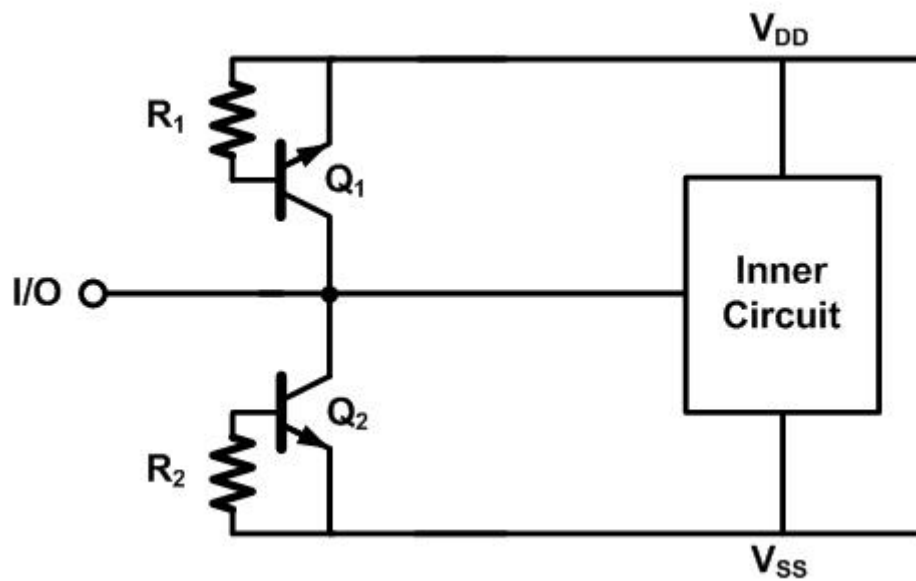


Figure 1. 16 Bipolar connection scheme for ESD protection application.

When the bipolar is used as an ESD protection device, it could be connected as shown in the Figure 1.16 [13]. Take the NPN bipolar  $Q_1$  as an example, its collector is connected to I/O port, while its emitter is connected to  $V_{DD}$ . In addition, its base is connected to  $V_{DD}$  through an external resistor  $R_1$ .

At the beginning, the  $Q_1$  is off. When ESD transient is stressed between I/O port and  $V_{DD}$ , the increasing voltage at I/O port will force the bipolar  $Q_1$  collector-base P-N junction into avalanche breakdown. Then the avalanche current going through the resistor  $R_1$  will generate a voltage drop between bipolar  $Q_1$  base-emitter P-N junction.

When the voltage drop is large enough, it will forward turn on the base-emitter P-N junction and open the bipolar  $Q_1$ . Immediately, the voltage at I/O port (or bipolar collector) starts to reduce rapidly while the ESD current still rises up, creating a negative-resistance region, or "snapback" region, in the bipolar I-V curve. When the voltage at I/O port drops to the holding voltage, the bipolar will go into the active region and start shunting ESD current in low-R state. Now the voltage at I/O port will go up with the increasing ESD current until its thermal breakdown. The whole process of the bipolar behavior during ESD transient is exactly the same with the bipolar-type I-V curve described in Figure 1.4 (b).

### 1.4.3 MOS

Gate-grounded NMOS transistor (ggNMOS) could be used as an ESD protection device. Figure 1.17 shows the X-section, connection and equivalent circuit of a ggNMOS: NMOS drain node is connected to A, while its gate, source and bulk nodes are connected to K. There is a parasitic NPN bipolar under the gate channel: P-Well (or P-substrate) will be the bipolar base, being connected to K through P-Well parasitic resistor  $R_{P-Well}$ ; drain N+ will be the bipolar collector, being connected to A; source N+ will be the emitter, being connected to K.

When there is an ESD transient pulse between A and K, the parasitic bipolar will discharge ESD transient just like the regular bipolar snapback behavior described in

last section: the collector-base avalanche current through the well resistor  $R_{P-Well}$  will forward bias the base-emitter P-N junction and then trigger the parasitic bipolar into snapback region and the following active region, to shunt ESD current and clamp voltage at node A.

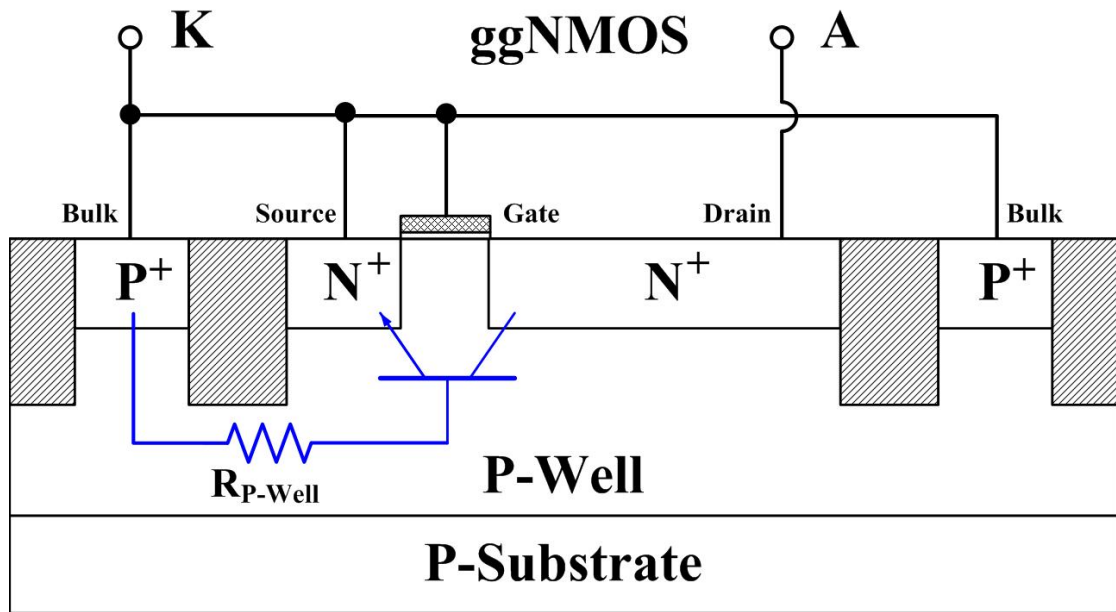


Figure 1. 17 The X-section, connection and equivalent circuit of ggNMOS.

PMOS could also be connected as ggNMOS for ESD protection. However, the parasitic PNP bipolar will be the discharging device in the gate-grounded PMOS (ggPMOS). Another difference is the ggPMOS cathode will be tied to the power supply when it is placed in the circuits.

The ggNMOS is usually drawn in the layout as a large-size multi-finger structure, which is equivalent to many small and equal size ggNMOS being connected parallel to provide ESD protection. However, for ggNMOS, its second breakdown voltage  $V_{12}$

is often lower than its triggering voltage  $V_{t1}$ . That means, for the multi-finger ggNMOS with many small parallel units, uniform turn on of all fingers is impossible. One way to solve this problem is finely adjusting the layout dimension parameters in ggNMOS, such as drain contact to gate space (DCGS), source contact to gate space (SCGS) and gate length ( $L$ ), as shown in Figure 1.18, to improve the uniformity of multi-finger ggNMOS turn on. Another possible way is using trigger-aid technology, such as gate-coupled NMOS[14].

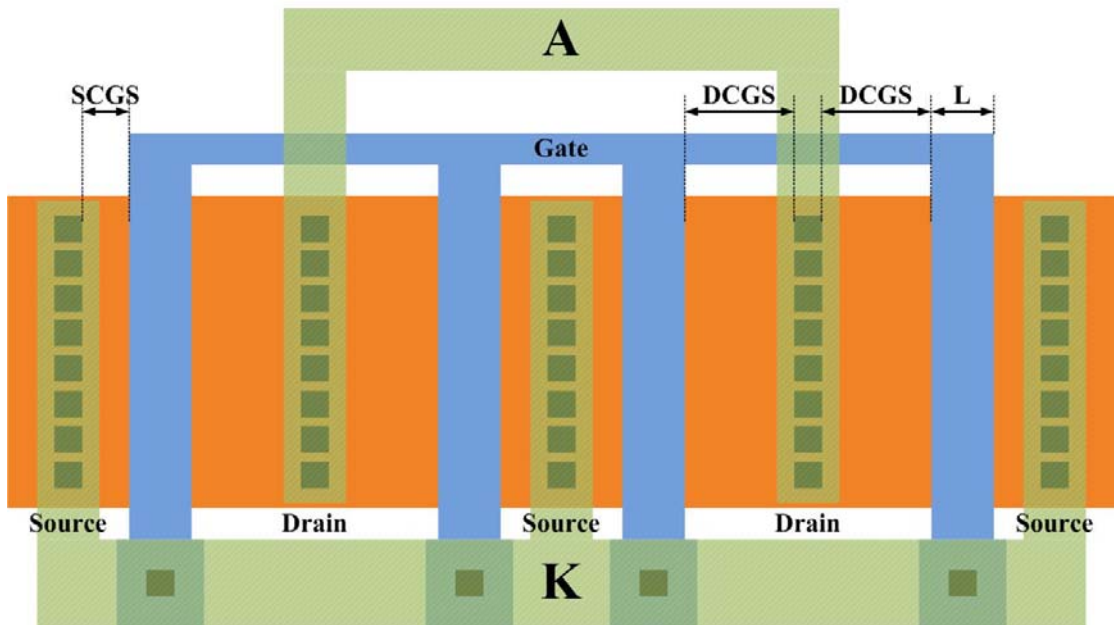


Figure 1. 18 The layout of a multi-finger ggNMOS (finger number = 4, neglect Bulk node).

Due to the low ESD protection rating of the parasitic bipolar, it generally needs large-size ggNMOS to provide enough ESD protection level. Considering the fact that MOS gate is also connected to the ggNMOS cathode, large parasitic capacitance will be induced into the ports being protected. That is sometimes intolerable to the inner

circuits, especially for high-speed or high-frequency designs. Moreover, according to the triggering mechanism indicated above, ggNMOS  $V_{t1}$  is related to the MOS drain-source breakdown voltage ( $BV_{DS}$ ), which is higher than MOS gate oxide breakdown voltage ( $BV_g$ ) for the advanced CMOS technologies under 100nm. That means the ggNMOS will not fit in the "ESD Design Window" of those technologies. Additional ESD implant in drain area helps to reduce ggNMOS  $V_{t1}$ , but it increases the manufacturing cost because of the extra process flows for the ESD implant.

#### 1.4.4 Silicon-Controlled Rectifier

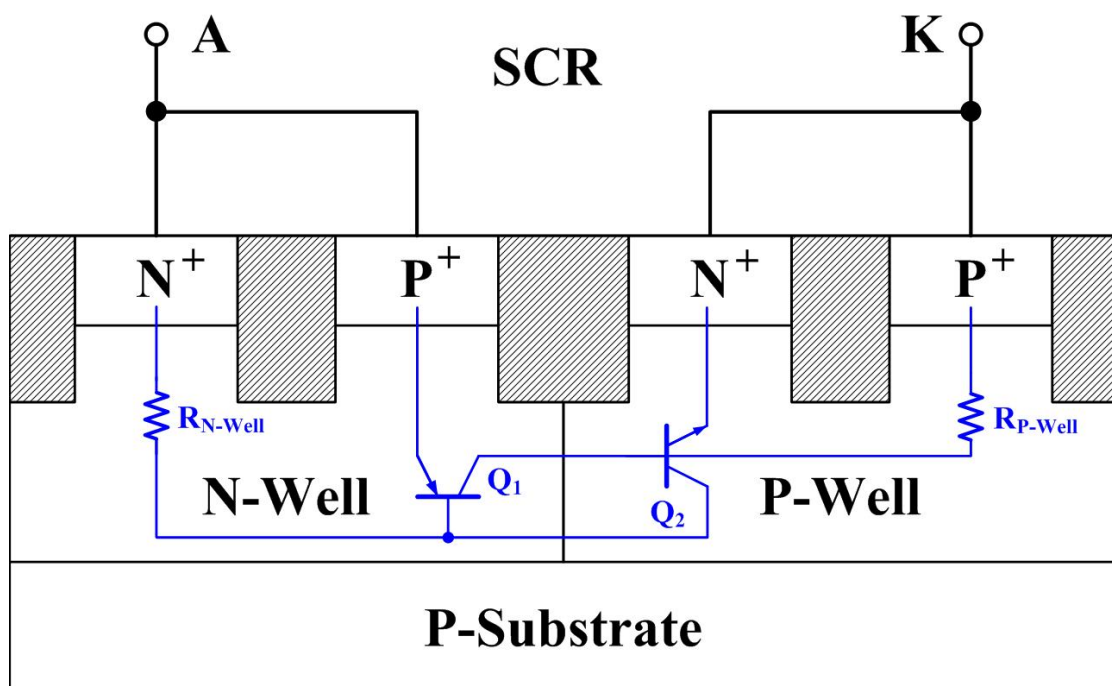


Figure 1. 19 The X-section and equivalent circuit of SCR in CMOS technology.

The X-section of a lateral silicon-controlled rectifier (SCR) in CMOS technology is shown in Figure 1.19. It contains a series P-N-P-N structure inside, composed by the



P+ in N-Well, N-Well, P-Well and N+ in P-Well. The N+ and P+ in N-Well are connected to anode (A), while the N+ and P+ in P-Well are connected to cathode (K). Figure 1.19 also presents the equivalent circuit of SCR, which contains two back-to-back parasitic bipolars,  $Q_1$  and  $Q_2$ , and two parasitic well resistors,  $R_{N-Well}$  and  $R_{P-Well}$ . The bipolar  $Q_1$  is a PNP bipolar, which formed by the P+ in N-Well (emitter), N-Well (base) and the P-Well (collector), while  $Q_2$  is an NPN bipolar, which is composed of the N-Well (collector), the P-Well (base) and the N+ in P-Well (emitter).

When a positive ESD transient pulse surges from A to K, the current from the N-Well/P-Well junction avalanche breakdown will generate a voltage drop on  $R_{N-Well}$ . With the increasing of the avalanche current, the voltage drop will be high enough to forward bias the base-emitter P-N junction of the PNP bipolar  $Q_1$  and turn the bipolar  $Q_1$ . The current from the collector of  $Q_1$  will go into the base of the NPN bipolar  $Q_2$ , finally forward biasing the base-emitter P-N junction of  $Q_2$  and turning on the  $Q_2$ . Then, both of the bipolars will feed current from their own collector for the other one's base, thus the voltage on the node A will drop rapidly to the holding voltage ( $V_h$ ). The two bipolars, both in active region, will start to discharge ESD current in a low-R status and clamp the voltage at node A until the second breakdown.

Because of the existence of two parasitic bipolars, SCR has high ESD protection efficiency. However, one of the drawbacks of SCR is that it has a relatively higher  $V_{t1}$  than those of other devices introduced above, according to the high avalanche

breakdown voltage between N-Well and P-Well. In addition, SCR  $V_h$  is usually too low to be below the circuit supply voltage, causing potential latch-up issues. In sum, original SCR cannot meet the requirement of "ESD Design Window". Therefore, improvements on SCR are necessary.

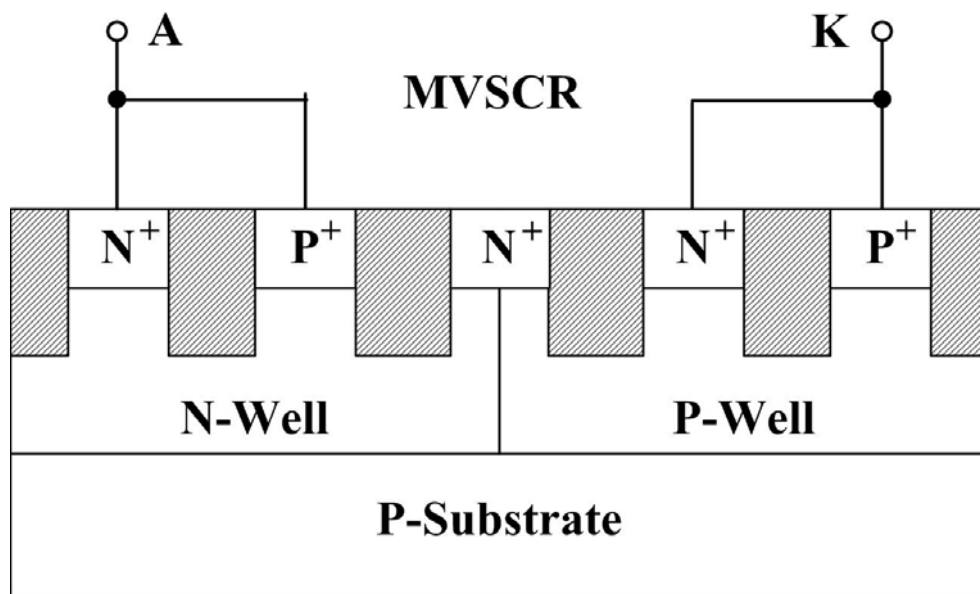


Figure 1. 20 The X-section of MVSCR in CMOS technology.

As shown in Figure 1.20, medium-triggering-voltage SCR (MVSCR) adds an N+ (or P+) between N-Well and P-Well of SCR. By this method, the reverse P-N junction high breakdown voltage between N-Well and P-Well will be reduced to the breakdown voltage between N+ (or P+) and P-Well (or N-Well). MVSCR used to be a useful ESD protection device when the isolation technology was still field oxide (FOX) [15]. However, after the Shallow Trench Isolation (STI) technology replaced the FOX technology in CMOS process for isolation, the  $V_{th}$  reduction from MVSCR to SCR was not significant any more [16].

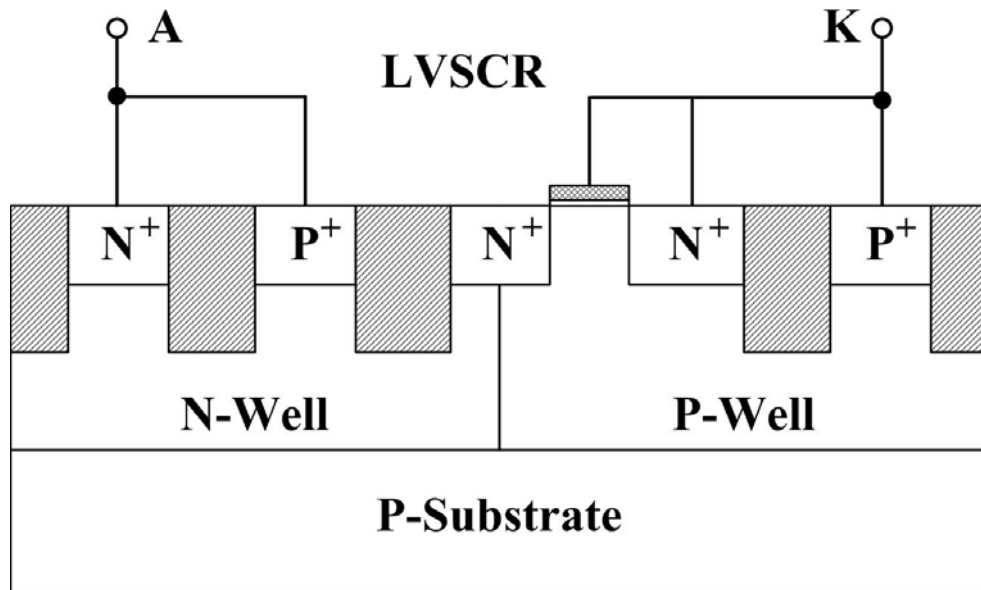


Figure 1. 21 The X-section of LVSCR in CMOS technology.

Instead of inserting N+ (or P+) between N-Well and P-Well of SCR, lower-triggering-voltage (LVSCR) employs a ggNMOS into the two wells, as shown in Figure 1.21 [17]. During the ESD events, ggNMOS in LVSCR will be triggered at a low  $V_{t1}$  first and then help the SCR in LVSCR turn on. In this way, LVSCR  $V_{t1}$  could be reduced, almost equal to ggNMOS  $V_{t1}$  of the same technology.

## **Chapter 2 Novel ESD Protection Structures**

### **2.1 Very-Low-Triggering-Voltage Dual-Direction SCR (VLTdSCR)**

#### **2.1.1 Background**

Tunable low triggering voltage, low-parasitic, compact and fast response ESD protection solutions are extremely essential to low-voltage (LV) and parasitic-sensitive radio-frequency (RF), high-speed analog and mixed-signal (AMS) ICs. SCR, featuring deep snapback behavior and high ESD current handling ability, is considered as an ideal low-parasitic ESD protection structure, but SCR high triggering voltage  $V_{t1}$  and very low ESD holding voltage  $V_h$  make it usually fail to fulfill the requirements of ESD design window. To reduce SCR  $V_{t1}$ , MVSCR and LVSCR are developed by adding triggering-aid implant or low- $V_{t1}$  device into the original SCR structure. Moreover, in [18-21] different modified SCR ESD protection designs are reported, not only reducing the  $V_{t1}$  but also tuning  $V_h$  through outside triggering-aid methods or complicated dimension adjustments. However, those modifications to original SCR usually induce extra ESD parasitic and cause slow response.

Furthermore, complete whole-chip ESD protection requires full ESD protection scheme against all possible ESD events and stressing modes. This ideal full-direction ESD protection scheme means that many ESD protection units may be needed on

chip if traditional single-polarity ESD protection structures are used. Therefore, chip area has to be increased due to large size of all ESD protection structures, adding severe ESD-induced parasitics into the chip and finally affect its normal operation.

Figure 2.1 presents the X-section and critical dimension parameters of VLTdSCR core ESD protection structure in standard bulk CMOS, while Figure 2.2 shows its equivalent circuit. VLTdSCR core structure has a five-layer ( $N_1P_2N_3P_4N_5$ ) two-node (A and K) symmetrical SCR-type device, containing one lateral PNP transistor ( $Q_1$ ), two vertical NPN transistor ( $Q_2$  &  $Q_3$ ), four resistors ( $R_1$ ,  $R_2$ ,  $R_3$  &  $R_4$ ) and two embedded open-gate NMOS units ( $M_1$  &  $M_2$ ). Terminal A and K could be connected between two IC pads, to provide ESD protection.

Figure 2. 1 X-section of VLTdSCR core structure.

Consider the SCR part in the VLTdSCR X-section without the two embedded NMOS  $M_1$  and  $M_2$ : when a positive ESD transient comes to A against K, it biases the collector (i.e., Deep N-Well/P-Well, marked as  $N_3/P_4$ ) of  $Q_1$  ( $P_2N_3P_4$ ) transistor negatively until its junction breakdown occurs. Avalanche current will then flows to K through the  $R_2$  (i.e.,  $P_4$ ) that forward-biases the emitter of  $Q_3$  ( $N_3P_4N_5$ ) transistor. It hence turns on  $Q_3$  and  $Q_1$ , which triggers the SCR of  $Q_1+Q_3$  at given  $V_{t1}$  and forms a low-R conduction path to shunt the large ESD pulse. SCR's deep snapback I-V helps to clamp ESD voltage at node A to a very low holding  $V_h$  to protect CMOS gate oxide. For negative ESD stressing mode, the collector (i.e., Deep N-Well/P-Well, labeled as  $N_3/P_2$ ) of  $Q_1$  ( $P_4N_3P_2$ ) transistor is biased negatively to its junction breakdown. Avalanche current then flows to A via the  $R_1$  (i.e.,  $P_2$ ) that forward-biases the emitter of  $Q_2$  ( $N_3P_2N_1$ ) transistor, which turns on  $Q_2$  and  $Q_1$ , hence triggers the SCR of  $Q_1+Q_2$  to discharge the ESD transient current. Therefore, a symmetrical dual-polarity SCR ESD protection device is built.

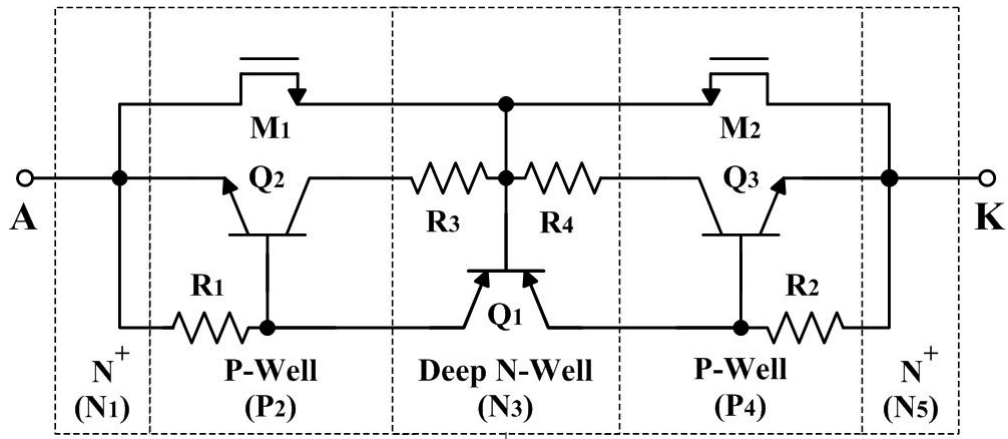


Figure 2. 2 Equivalent circuit of the new VLTdSCR core ESD protection structure.

Such dual-direction SCR structure in VLTdSCR has the same high ESD  $V_{t1}$  as that of the traditional SCR. To reduce the  $V_{t1}$ , the new VLTdSCR core structure employs two embedded  $M_1/M_2$  devices, which are designed for likely channel punch-through breakdown. The MOS punch-through breakdown normally occurs at a lower voltage than that of MOSFET Drain/Well junction breakdown, leading to very low triggering  $V_{t1}$  for the VLTdSCR ESD protection structure. Meanwhile, VLTdSCR core  $V_{t1}$  is adjustable by fine-tuning the  $M_1/M_2$  channel length ( $L$ ) and the width of  $P+/N+$  STI, able to fit different ESD design windows.

In addition, latch-up immunity is required for SCR ESD structures by designing its holding  $V_h$  to be higher than IC power supply voltage with at least 10% safe margin. However, a low  $V_h$  is also desired for ESD voltage clamping at pads. Theoretically, SCR  $V_h$  is determined by  $\beta$ -product of the embedded BJTs, which is mainly dictated by the base width of the lateral PNP ( $Q_1$ ) in the new VLTdSCR structure. Thus, careful design trade-off for  $V_h$  could be done by fine-tuning base width of  $Q_1$  (decided by the middle  $N+$  extension to  $N$ -Well labeled as “a” and the middle  $N$ -Well width marked as “b”) in the VLTdSCR, to eliminate latch-up issues. Furthermore, as stated before, the second breakdown current  $I_{t2}$  is the highest ESD current value that a ESD protection device could handle and hence is usually used as indicator for ESD device protection level. Drain contact to gate space (DCGS) in VLTdSCR core has great impact on device  $I_{t2}$  performance and hence could be used to change its ESD protection level.

A group of new VLTdSCR ESD protection core structures and its CULTdSCR ESD protection circuits were designed and fabricated in a commercial 0.18 $\mu$ m CMOS for design optimization and comparison, to be discussed in the following sections.

### **2.1.3 VLTdSCR Core ESD Protection Design and Measurement**

#### **2.1.3.1 Dual-Direction ESD Protection Ability**

Comprehensive ESD simulation, mainly by Technology Computer-Aid Design (TCAD), was conducted based on the predictive mixed-mode ESD simulation-design methodology [22]. Figure 2.3 depicts the ESD discharging current contours for one VLTdSCR core under positive ESD stressing from A (Left node) to K (Right node) by ESD simulation. The number of current contours for each contact are in proportion to their discharging current value in the same moment. Compare Figure 2.3 with Figure 2.1, it is obvious that most ESD current flows along the path of  $P_2 \rightarrow N_3 \rightarrow P_4 \rightarrow N_5$ , which confirms that new VLTdSCR core works as described previously: the embedded  $M_1/M_2$  units only serve to trigger the VLTdSCR core, but it is the parasitic bipolar circuitry inside the SCR that forms the main ESD current discharging channel to provide robust ESD protection. Likewise, if negative ESD stressing surges at terminal A with respect to terminal K, then, ESD current will discharge through the path of  $P_4 \rightarrow N_3 \rightarrow P_2 \rightarrow N_1$ .



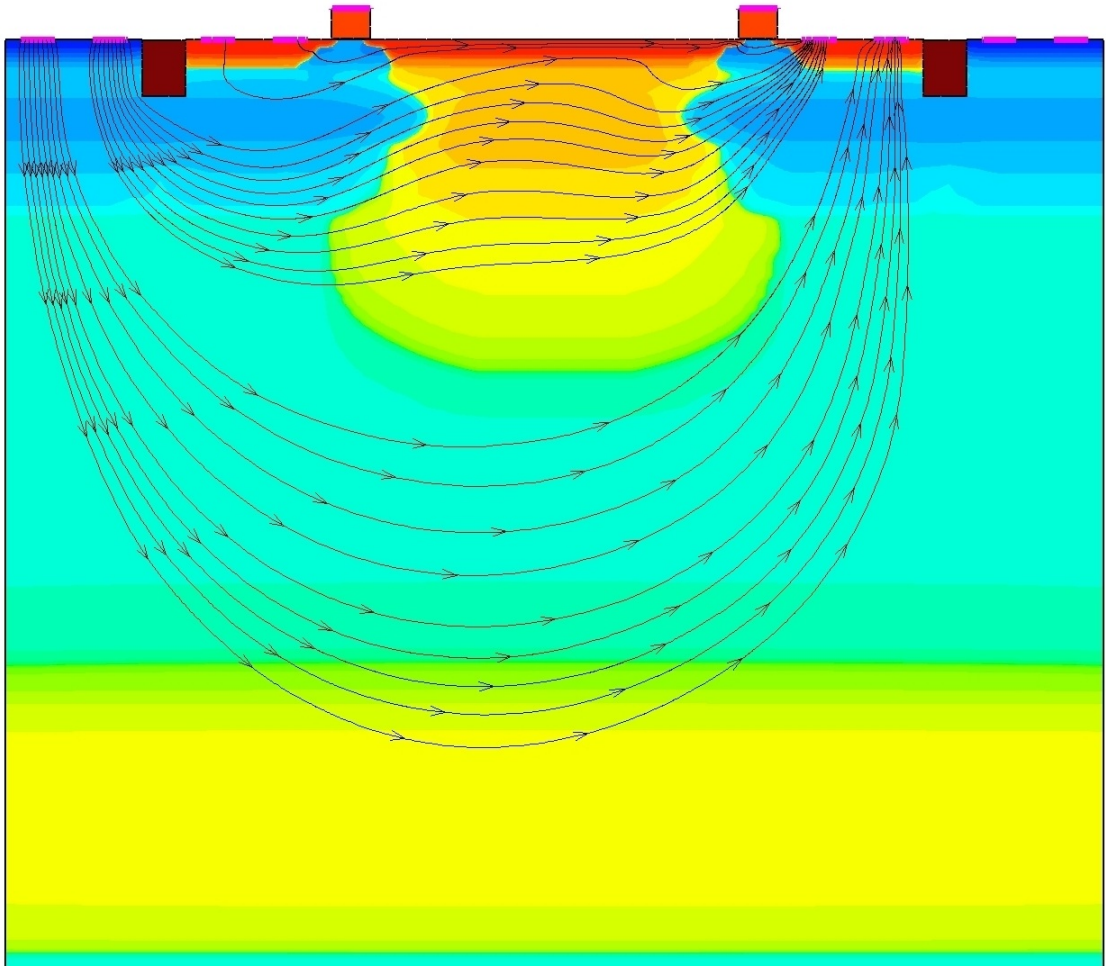


Figure 2. 3 TCAD-simulated X-section and ESD discharging current flow lines for the new VLTdSCR core ESD protection structure.

Figure 2.4 displays the maximum lattice temperature ( $T_{\max}$ ) distribution inside the VLTdSCR core structure during low-R discharging status. The “hotspot” of  $T \sim 700\text{K}$  is at the VLTdSCR middle N+ extension under  $M_2$ , part of the VLTdSCR discharging path of  $P_2 \rightarrow N_3 \rightarrow P_4 \rightarrow N_5$ . The hotspot will initiate ESD damage in the protection device and must be carefully considered in ESD protection designs by ESD simulation.

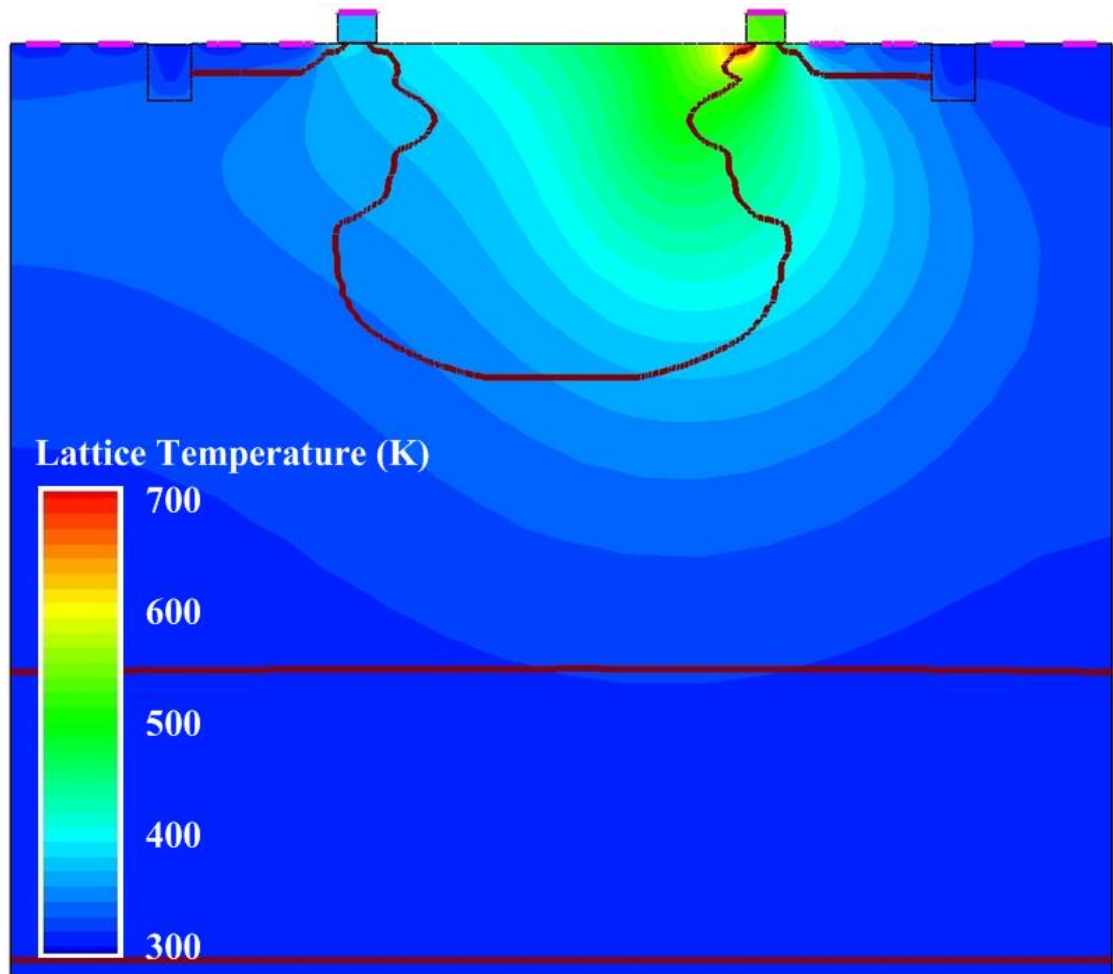


Figure 2. 4 TCAD-simulated maximum lattice temperature across the new VLTdSCR core.

Figure 2.5 presents the dual-polarity I-V curves for one VLTdSCR core sample from ESD simulation and TLP testing, which confirms the expected very low triggering  $V_{t1}$  of 5.03V and symmetrical snapback I-V curves by SCR ESD discharging. The measured holding voltage  $V_h$  is 2.93V. Very low discharging resistance of  $R_{on} \sim 0.19\Omega$  was obtained by TLP testing, which is highly desirable for robust ESD protection designs. The discrepancy between simulation and TLP test could be contributed to less initial silicon data during early stage of the design.

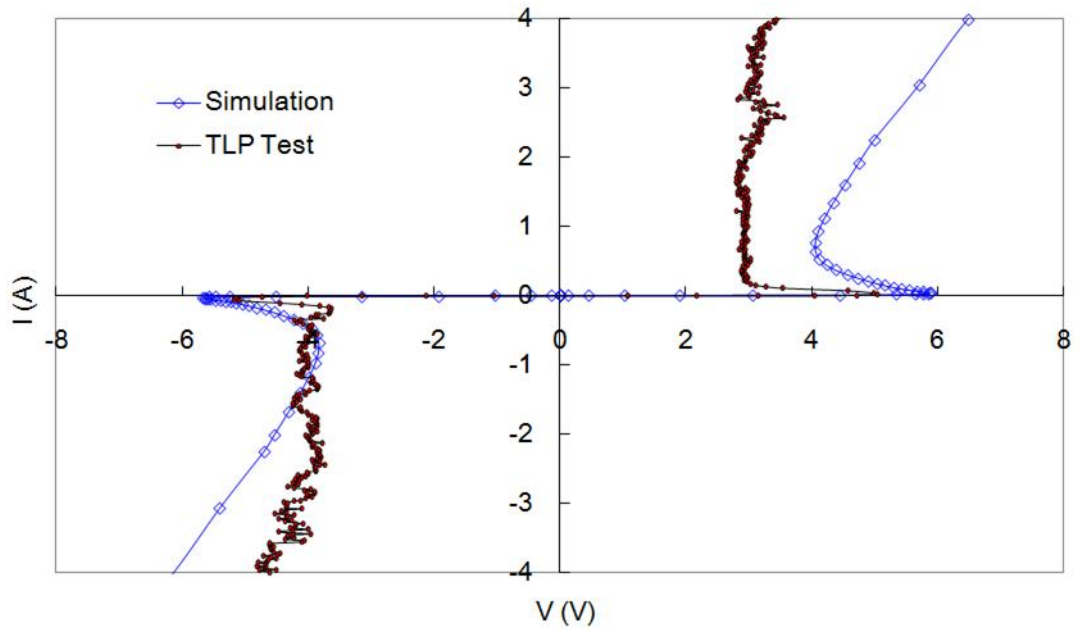


Figure 2. 5 Symmetrical I-V characteristics for one sample VLTdSCR core by ESD simulation and TLP measurement.

### 2.1.3.2 High-Level and Low-Parasitic ESD Protection

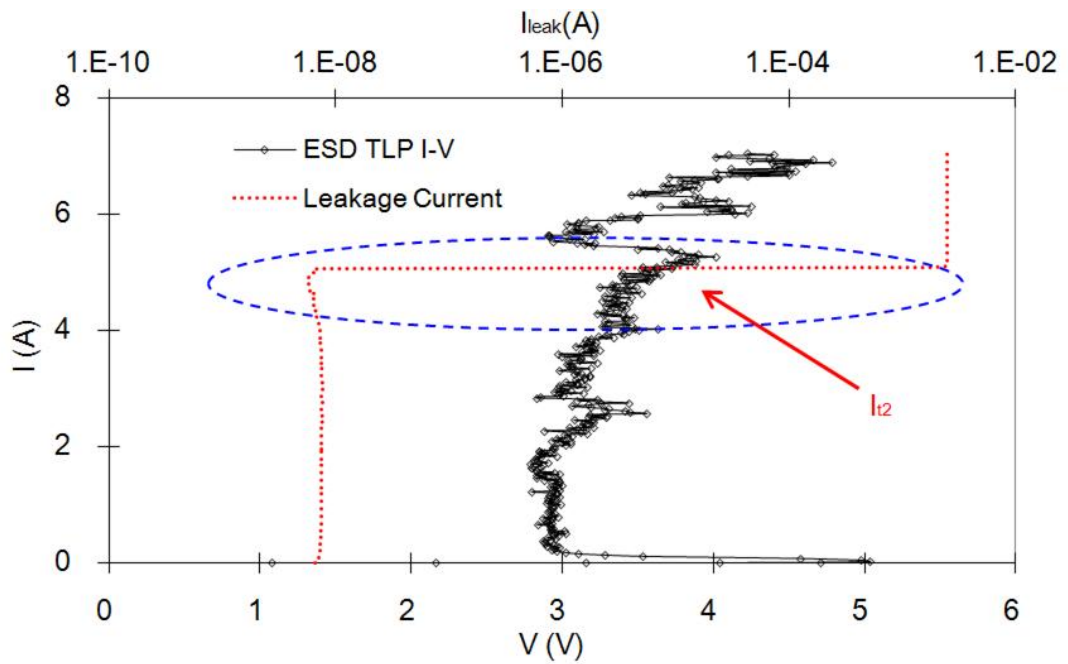


Figure 2. 6 Measured TLP I-V curve and leakage current for one sample VLTdSCR core.

The new VLTdSCR design managed to achieve low triggering voltage and meanwhile avoid inducing high ESD parasitics. Figure 2.6 shows the measured full I-V curve, along with the DC leakage curve indicating the thermal breakdown point, for one sample VLTdSCR core SCR structure by TLP testing. All the ESD-critical parameters have to be tuned carefully to meet the ESD design window of the circuit being protected. Table 2.1 summarizes critical ESD function parameters for VLTdSCR core structures from simulation to measurement.

Table 2. 1 Specs for sample VLTdSCR core.

| ESD Specs             | Characterization Methods |      |        |
|-----------------------|--------------------------|------|--------|
|                       | Simulation               | TLP  | VF-TLP |
| $V_{t1}$ (V)          | 5.89                     | 5.03 | 5.51   |
| $V_h$ (V)             | 4.06                     | 2.93 | 4.84   |
| $I_{t2}$ (A)          | 8.65                     | 5.07 | 4.10   |
| $R_{on}$ ( $\Omega$ ) | 0.73                     | 0.19 | 2.15   |

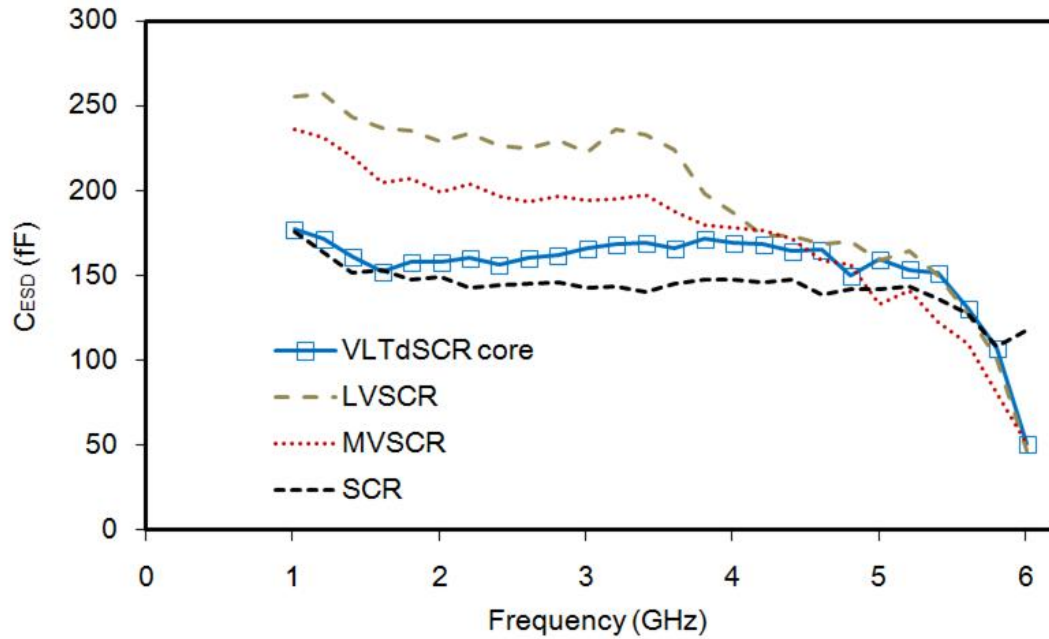


Figure 2. 7 Measured parasitic  $C_{ESD}$ ~frequency relationship for various SCR-type structures.

Complete s-parameter and noise measurements on VLTdSCR core structures were also performed up to 10GHz. Figure 2.7 shows the measured parasitic capacitance versus frequency relationship for one sample VLTdSCR split in comparison with other widely-used SCR-type ESD protection structures, extracted from s-parameter data. TLP and VF-TLP testing were also conducted to VLTdSCR core for HBM and CDM ESD protection performance evaluation. Table 2.2 lists tested critical ESD parasitic parameters and ESD protection levels of HBM and CDM. It confirms that for a compact 90 $\mu$ m wide VLTdSCR core ESD structure, it can provide ~7.6kV HBM and ~500V CDM ESD protection level, while it only introduces very low parasitic capacitance of  $C_{ESD}$ ~150fF and noise of NF~0.2dB at 3.5GHz. The low  $C_{ESD}$

achieved for new VLTdSCR core is mainly because the total capacitance is dominated by serious junction capacitances of all N+/P-Well and N-Well/P-Well junctions between two terminals A and K.

Table 2. 2 VLTdSCR core device ESD performance summary.

| Performance    |                                   | Testing |
|----------------|-----------------------------------|---------|
| ESD Protection | HBM (kV)                          | ~7.6    |
|                | CDM (V)                           | >500    |
|                | ESDV ( $\text{V}/\mu\text{m}^2$ ) | >7      |
| ESD Parasitics | NF (dB)/3.5GHz                    | ~0.2    |
|                | $C_{\text{ESD}}$ (fF)/3.5GHz      | ~150    |
|                | $I_{\text{leak}}$ (nA)            | ~7.03   |
| Response (pS)  |                                   | <100    |

### 2.1.3.3 Very Fast ESD Protection Response

HBM ESD protection was evaluated by TLP testing (Barth Model 4002 TLP Tester) for VLTdSCR core structures. In addition, the harsh CDM ESD stress, with a fast rising time of  $t_r \sim 400\text{pS}$ , was examined by VF-TLP testing through Barth Model 4012 VFTLP+ tester, which could generate extremely fast ESD pulse with  $t_r = 400\text{pS} \sim 100\text{pS}$ . Figure 2.8 shows the measured I-V curve for one sample VLTdSCR core structure by VF-TLP testing. Table 2.3 summarizes the  $V_{t1} \sim t_r$  relationship, which

readily confirms that the new VLTdSCR is able to respond to very fast ESD surges with ultra short rising time of  $t_r \sim 100\text{pS}$ , indicating its ESD protection ability for the fast CDM ESD mode. It is believed that the very fast response speed for VLTdSCR is due to the fast punch-through breakdown of the embedded  $M_1/M_2$  devices.

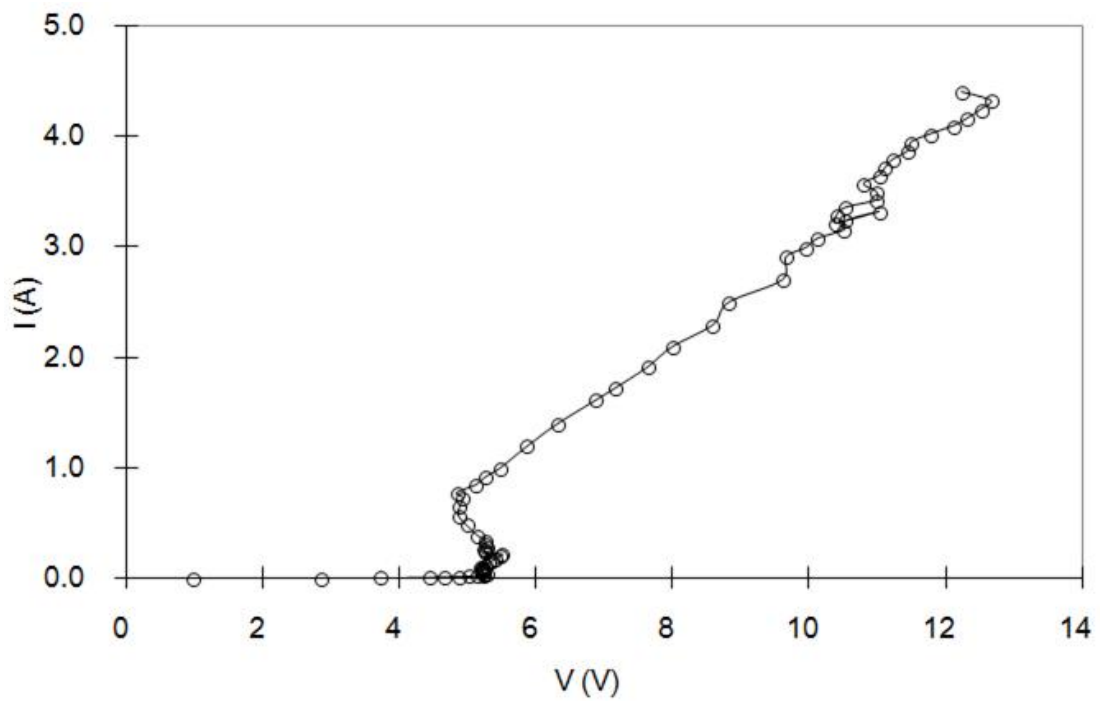


Figure 2. 8 Measured I-V curve by VF-TLP testing for one sample VLTdSCR core structure.

Table 2. 3 Measured  $V_{t1} \sim t_r$  for VLTdSCR core device.

| $t_r$ (pS)   | 10nS | 400  | 200  | 100  |
|--------------|------|------|------|------|
| $V_{t1}$ (V) | 5.03 | 5.76 | 5.78 | 5.51 |

#### 2.1.3.4 VLTdSCR ESD Operation in Wide Temperature Range

Temperature effects on new VLTdSCR core SCR structures were investigated by TLP testing across wide temperature range from  $-50^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ . VLTdSCR samples were placed inside a temperature-variable chamber where temperature could be changed from  $-50^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ . Figure 2.9 presents the measured  $V_{t1}\sim T$  and  $I_{\text{leak}}\sim T$  relationship for sample VLTdSCR structures, which shows that new VLTdSCR ESD protection structure can work in harsh high and low temperature conditions. The observed  $\Delta V_{t1}$  varies between 5.00V and 4.67V and  $\Delta I_{\text{leak}}$  changes from pA to  $\mu\text{A}$  scale within a  $150^{\circ}\text{C}$  temperature variation range.

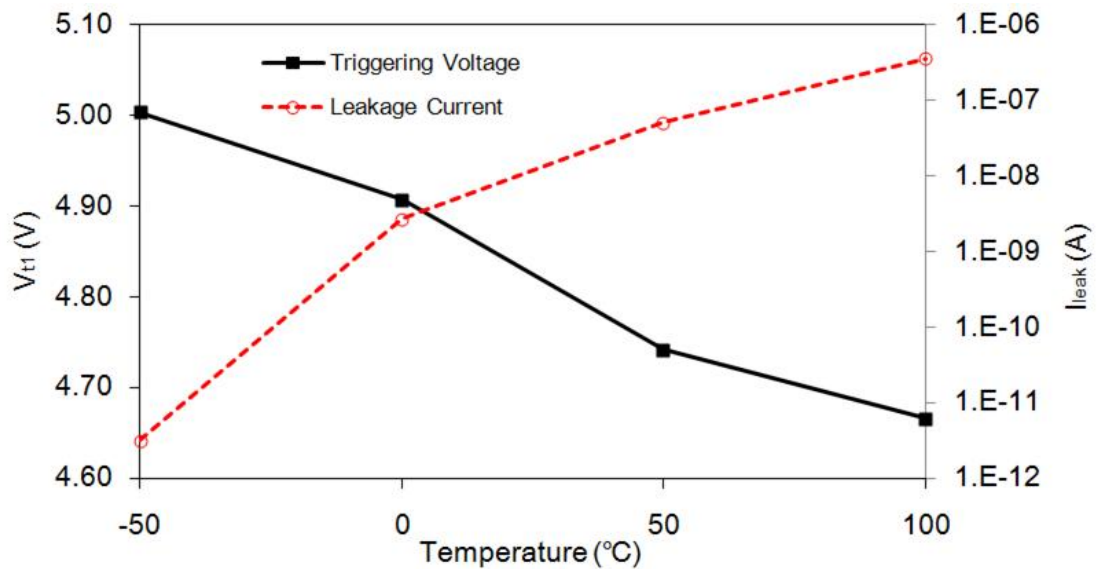


Figure 2. 9 Measured  $V_{t1}\sim T$  and  $I_{\text{leak}}\sim T$  curves for one sample VLTdSCR core structure.



## 2.1.4 Adjustable ESD-Critical Parameters for VLTdSCR Structures

### 2.1.4.1 Ultra Low and Tunable ESD Triggering

As discussed above, a flexible  $V_{t1}$  is available for this new VLTdSCR structure by varying its ESD-critical parameters. The channel length ( $L$ ) of the embedded  $M_1/M_2$  devices could be used to adjust the  $V_{t1}$  for new VLTdSCR ESD structures. Figure 2.10 presents the  $V_{t1} \sim L$  relationship for a sample VLTdSCR core structure from both TCAD simulation and TLP testing. It clearly shows that new VLTdSCR core structures have adjustable  $V_{t1}$  of from 5.55V to 4.58V by selecting  $L=0.45\text{-}0.18\mu\text{m}$  in one simple design split. A wider  $V_{t1}$  range can be expected with even shorter channel length.

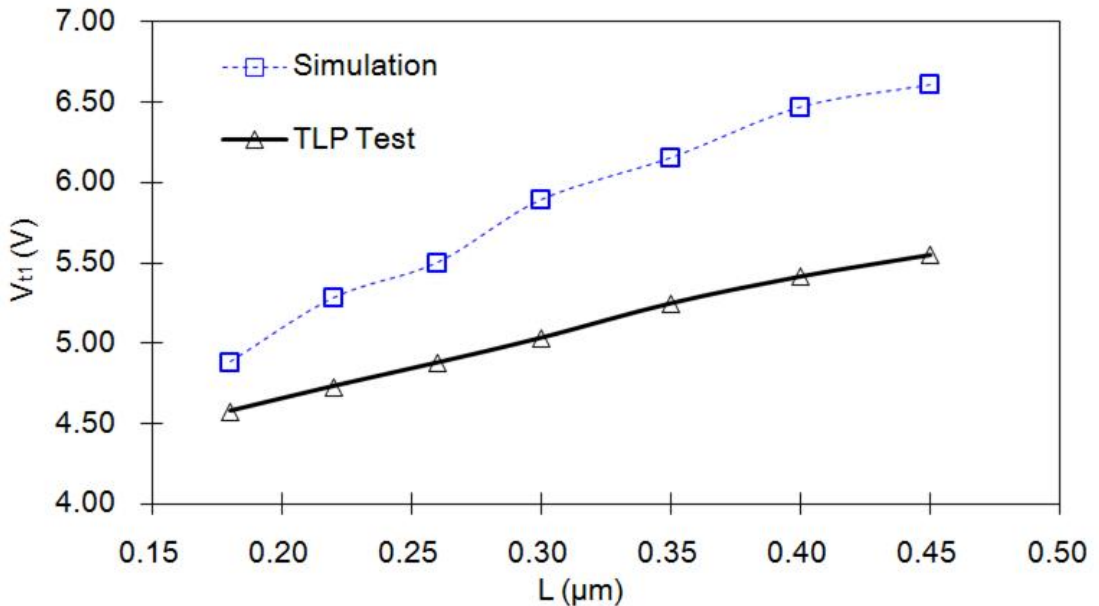


Figure 2. 10 Simulation and TLP testing results show that new VLTdSCR core  $V_{t1}$  may be

adjusted by designing the channel length,  $L$ , of the embedded  $M_1/M_2$ .

Another design dimension for  $V_{t1}$  adjustment in VLTdSCR structures is the P+/N+ STI width. A slightly wider STI means a higher P-Well resistor  $R_1$  or  $R_2$ . Thus, it makes  $Q_2$  or  $Q_3$  transistor base-emitter P-N junction turn on easier and hence reduce the  $V_{t1}$  for VLTdSCR core structures. Table 2.4 summarizes the measured  $V_{t1} \sim$  STI relationship for one sample VLTdSCR structure. Combining both L and STI design factors, the VLTdSCR structure could have wider  $V_{t1}$  range.

Table 2. 4 Measured  $V_{t1} \sim$  STI width for LTdSCR core device.

| STI width ( $\mu\text{m}$ ) | 0.28 | 1    | 2    |
|-----------------------------|------|------|------|
| $V_{t1}$ (V)                | 5.62 | 5.48 | 5.31 |

#### 2.1.4.2 Adjusting ESD $V_h$ for Better Latch-up Immunity

As discussed earlier, for VLTdSCR ESD protection structure, it is possible to tune the device holding voltage  $V_h$  through changing the dimension parameters, such as the middle N+ extension to N-Well "a" and the middle N-Well width "b", to realize nice latch-up immunity and appropriate low clamping simultaneously.

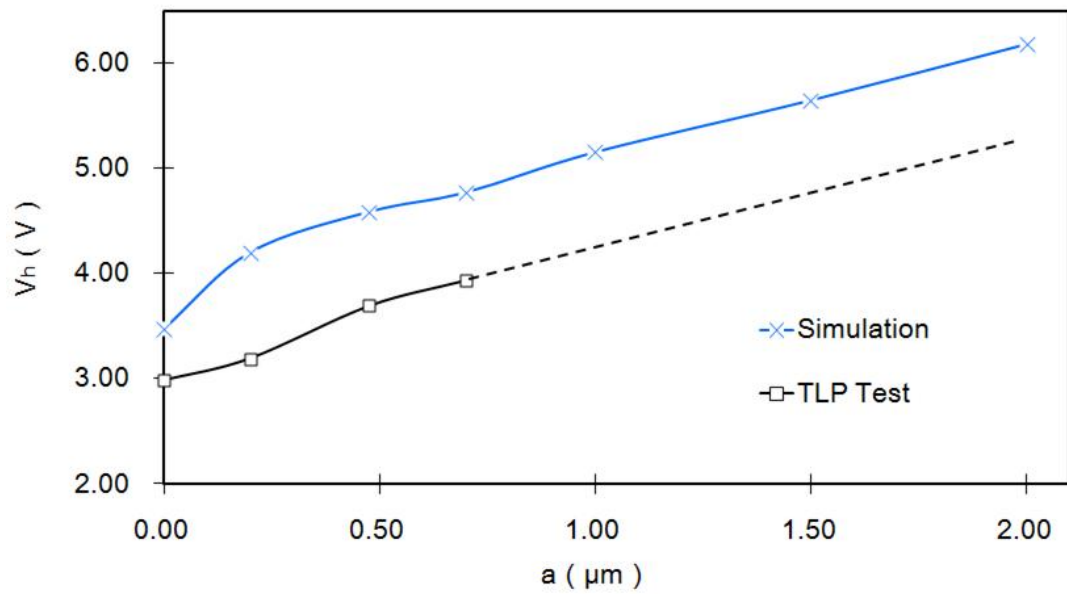


Figure 2. 11 The  $V_h \sim a$  relationship for one sample VLTdSCR core ESD protection structure from simulation and TLP testing.

Table 2. 5  $V_h \sim a$  controllability for VLTdSCR core device.

| N+ Extension to N-Well | $V_h$ (V)  |      |
|------------------------|------------|------|
|                        | Simulation | TLP  |
| a (μm)                 |            |      |
| 0                      | 3.47       | 2.98 |
| 0.2                    | 4.20       | 3.19 |
| 0.475                  | 4.59       | 3.69 |
| 0.7                    | 4.77       | 3.94 |
| 1                      | 5.15       | -    |
| 1.5                    | 5.65       | -    |
| 2                      | 6.18       | -    |

Figure 2.11 and Table 2.5 present the measured  $V_h \sim a$  relationship for one sample VLTdSCR structure. Both simulation and testing show that  $V_h$  can be fine-tuned by carefully designing  $Q_1$  base width to change the  $V_h$  from a 2.98V to >4.5V. In addition, Figure 2.12 and Table 2.6 present testing results for the  $V_h \sim b$  relationship for one sample VLTdSCR structure. In sum, higher  $V_h$  could be obtained by carefully increasing the  $a$  and/or  $b$  dimensions. However, with the increase of the base ( $N_3$ ) width of parasitic bipolar  $Q_1$  in the VLTdSCR, its ESD current capability will be reduced. Therefore, careful design trade-off between latch-up immunity and ESD protection level must be considered in practical designs for new VLTdSCR ESD structure splits.

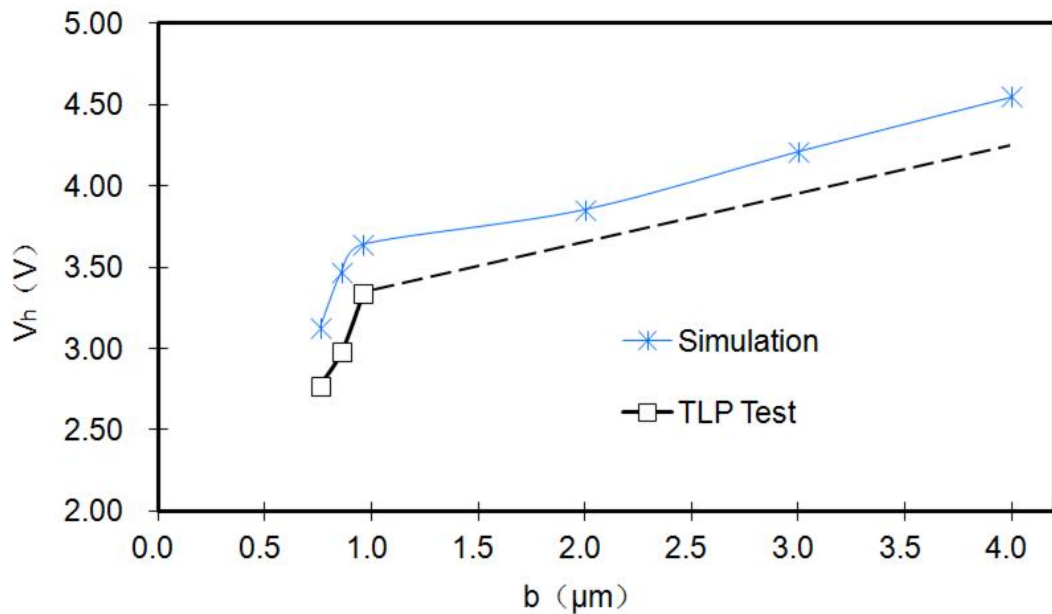


Figure 2. 12 The  $V_h \sim b$  relationship for one sample VLTdSCR core ESD protection structure

from simulation and TLP testing shows varying ESD holding voltage by design splits.

Table 2. 6  $V_h \sim b$  controllability for VLTdSCR core device.

| Middle N-Well Width   | $V_h$ (V)  |      |
|-----------------------|------------|------|
| $b$ ( $\mu\text{m}$ ) | Simulation | TLP  |
| 0.76                  | 3.13       | 2.77 |
| 0.86                  | 3.47       | 2.98 |
| 0.96                  | 3.64       | 3.34 |
| 2                     | 3.86       | -    |
| 3                     | 4.21       | -    |
| 4                     | 4.55       | -    |
| 5                     | 4.70       | -    |

#### 2.1.4.3 Tunable ESD Protection Level

As mentioned earlier, the drain contact to gate space (DCGS) of the embedded triggering unit  $M_1/M_2$  could impact the  $I_{t2}$  level of VLTdSCR device. Theoretically, a wider DCGS shall introduce extra ballasting resistance and distribute the ESD transient current more uniformly across the active VLTdSCR structure, hence leading to a higher  $I_{t2}$ . The simulated  $I_{t2} \sim \text{DCGS}$  relation curve in Figure 2.13 clearly proves that  $I_{t2}$  rises with a increasing DCGS, but the measured results suggest the  $I_{t2}$  increasing speed will become slow with a wider DCGS.

Table 2. 7 Measured and Simulated  $I_{t2}$  &  $R_{on}$  ~ DCGS for VLTdSCR core device.

| DCGS ( $\mu\text{m}$ )          | 0.16 | 1    | 2    | 3    | 4    |
|---------------------------------|------|------|------|------|------|
| Simulated $I_{t2}$ (A)          | 7.64 | 7.78 | 8.07 | 8.55 | 9.57 |
| Measured $I_{t2}$ (A)           | 5.25 | 5.93 | 6.13 | 6.18 | 6.4  |
| Simulated $R_{on}$ ( $\Omega$ ) | 1.02 | 1.56 | 1.88 | 2.34 | 2.7  |
| Measured $R_{on}$ ( $\Omega$ )  | 0.44 | 0.50 | 1.01 | 1.53 | 1.72 |

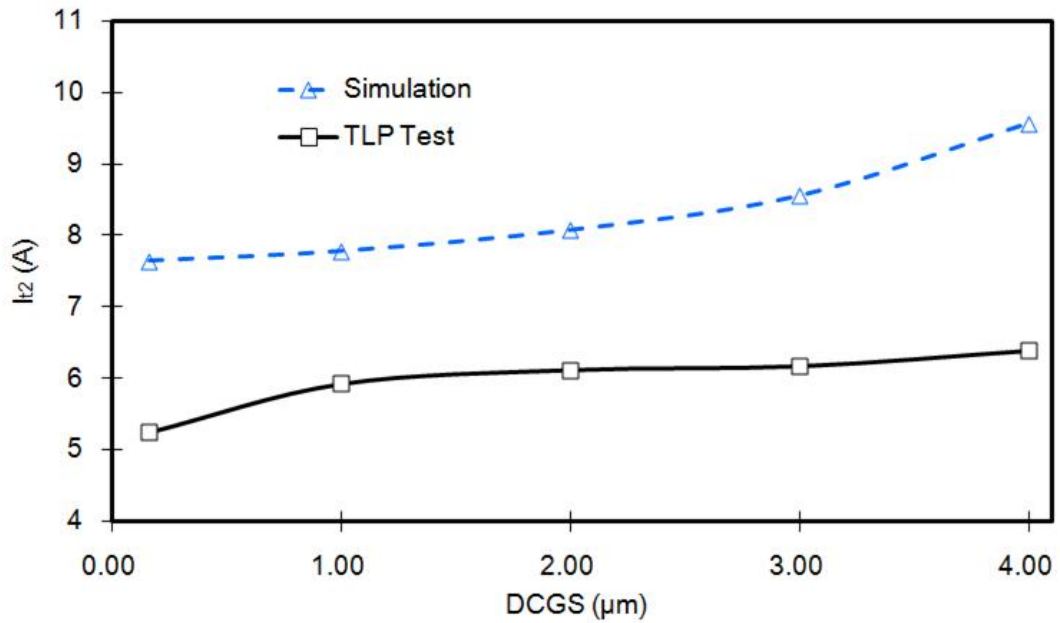


Figure 2. 13 The  $I_{t2}$ ~DCGS curves for sample VLTdSCR core SCR ESD protection structure from simulation and TLP testing reveals impact of DCGS spacing on ESD protection level.

This difference between simulation prediction and testing data may be attributed to two possible factors. Firstly, a wider DCGS introduces more series resistance in the ESD discharging channel, as confirmed by the testing data listed in Table 2.7, which

will cause stronger local heating effect inside the VLTdSCR core structure and hence a lower  $I_{t2}$ . Secondly, the ESD simulation was not very comprehensive, as stated before, due to lack of initial Si data for calibration because this project had only one design tapeout. Consequently, some discrepancies between ESD simulation and testing may be expected for new VLTdSCR designs.

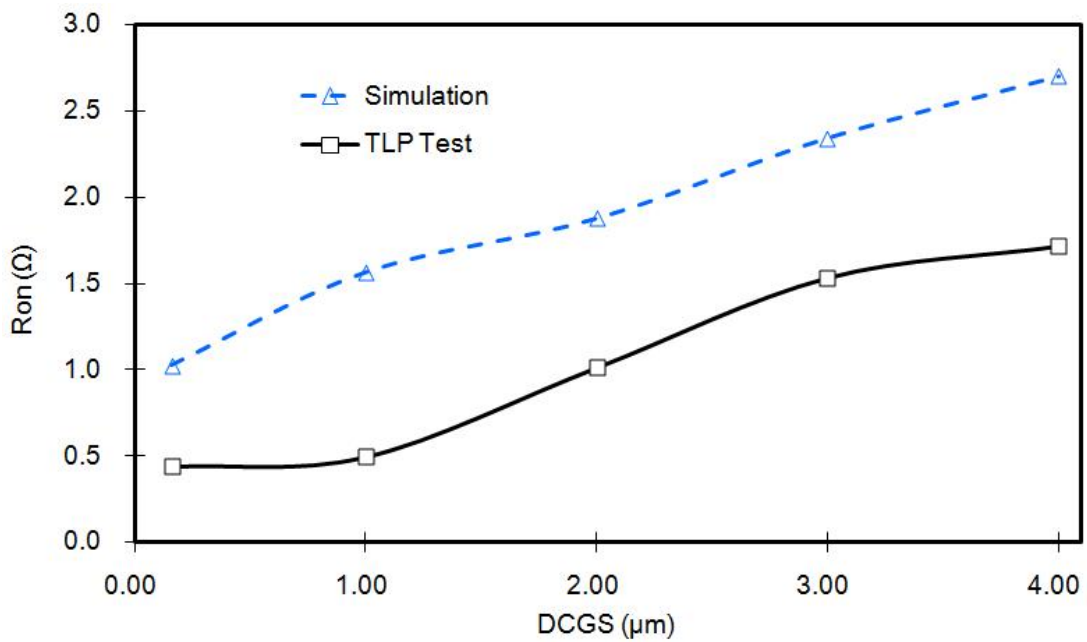


Figure 2.14 The  $R_{on}$ ~DCGS relationship for one sample VLTdSCR core ESD protection structure shows that the series resistance  $R_{on}$  increases as DCGS spacing increases.

Figure 2.14 shows that the series  $R_{on}$  does increase as DCGS increases. A larger  $R_{on}$  means a higher  $V_{t2}$ , which will force new VLTdSCR core structure parameters to break the critical ESD Design Window. Therefore, a good balance should be made between ESD protection level and DCGS spacing in practical design.

### 2.1.5 CULTdSCR ESD Protection Circuits

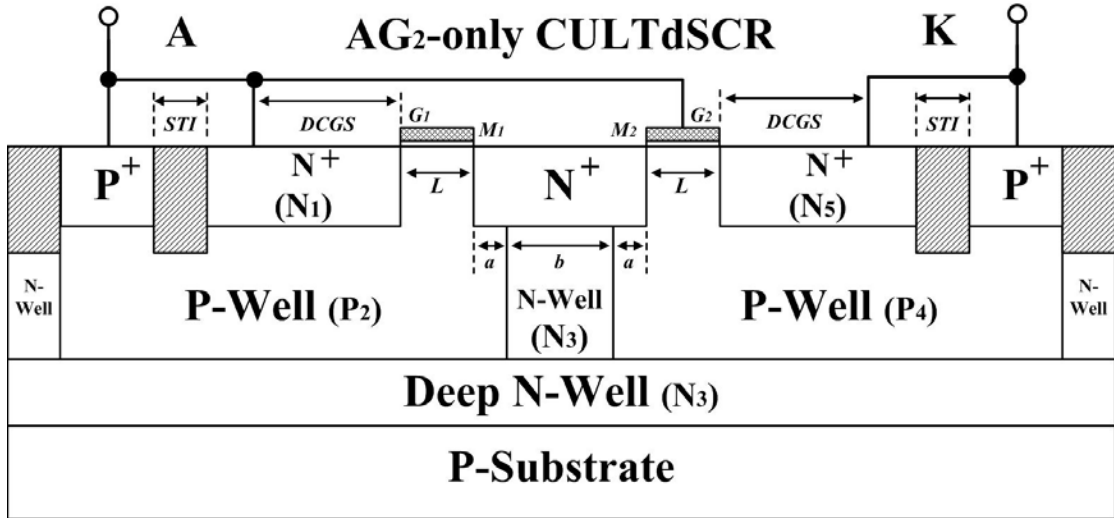


Figure 2. 15 X-section for new AG<sub>2</sub>-coupled CULTdSCR ESD protection circuit.

To further reduce the ESD triggering  $V_{t1}$  for new VLTdSCR ESD protection structures to meet more aggressive ESD design window requirement in advanced CMOS technologies, a novel cross-coupling trigger-assisting technique was developed for VLTdSCR ESD protection structure, too. This unique technique utilizes cross-coupling connection between the open-gate of the embedded  $M_1/M_2$  devices and the terminals of new VLTdSCR, creating a new cross-coupling ultra low triggering SCR-type ESD protection circuitry (CULTdSCR). Three different versions of CULTdSCR ESD protection circuits were designed and characterized in 0.18 $\mu$ m CMOS.



### 2.1.5.1 AG<sub>2</sub>-Coupled CULTdSCR ESD Protection Circuit

Figure 2.15 shows cross-section for the first type of CULTdSCR ESD circuit, which cross-couples the gate of NMOS device M<sub>2</sub> (i.e., G<sub>2</sub>) to the anode (A) of VLTdSCR, hence forming a new asymmetrical AG<sub>2</sub>-coupled CULTdSCR ESD circuit with its equivalent circuit depicted in Figure 2.16.

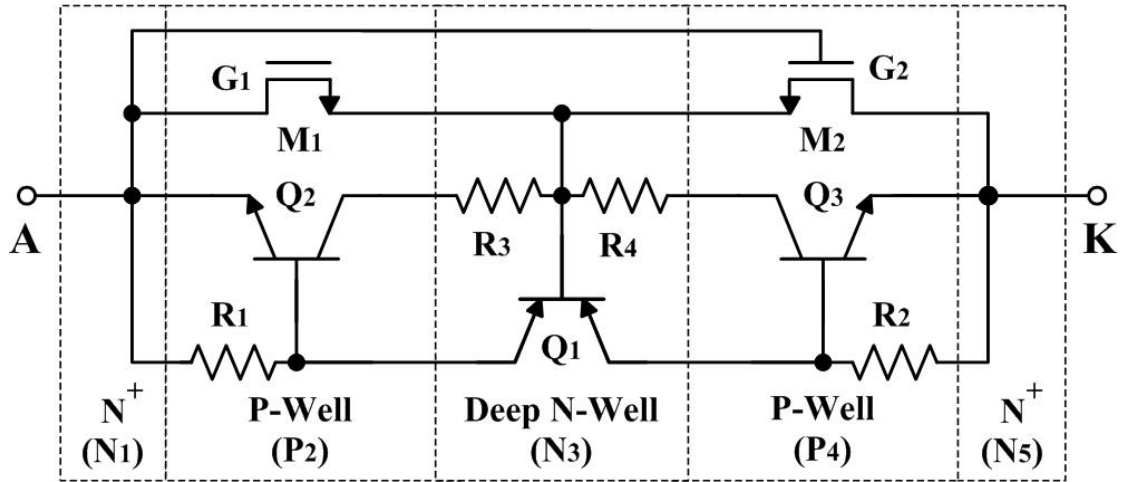


Figure 2. 16 Equivalent circuit of new AG<sub>2</sub>-coupled CULTdSCR ESD protection circuit.

Figure 2.17 presents the I-V characteristics for one sample AG<sub>2</sub>-coupled CULTdSCR ESD circuit from ESD simulation and TLP testing, which clearly shows the required lower ESD triggering of V<sub>t1</sub>~4.14V under positive A to K ESD stressing. The obtained V<sub>t1</sub> for new CULTdSCR ESD circuit is much lower than that V<sub>t1</sub>~5.29V for the same baseline VLTdSCR ESD structure.

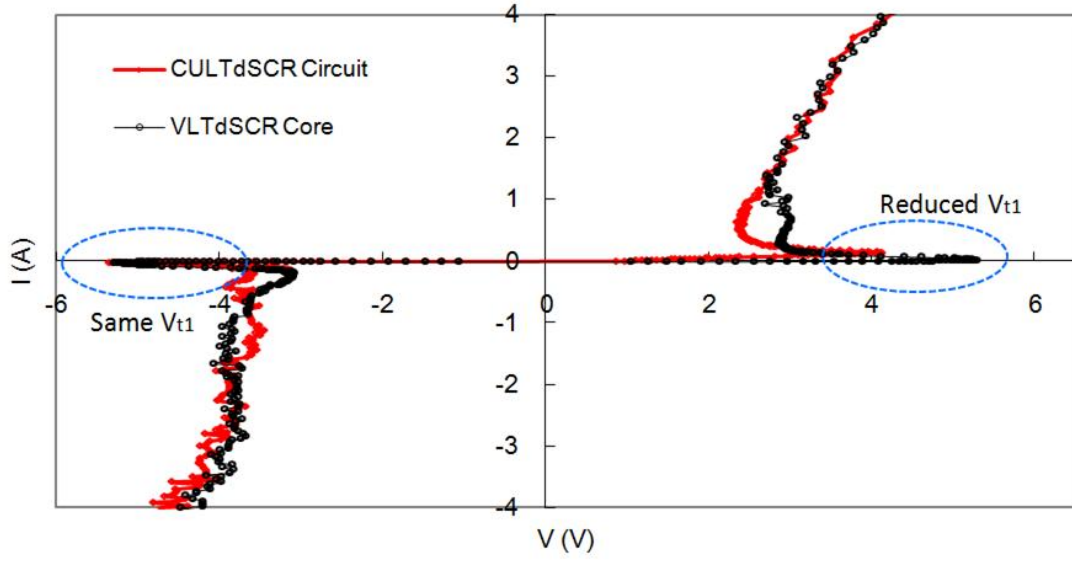


Figure 2. 17 Measured I-V curves by TLP testing for sample VLTdSCR core ESD structure and cross-coupled CULTdSCR ESD protection circuit.

Table 2.8 lists the critical ESD parameters for new CULTdSCR ESD circuit. The new CULTdSCR ESD circuit has a completely different ESD triggering mechanism, compared to that of the baseline VLTdSCR core SCR structure. For CULTdSCR ESD protection circuit, when a positive ESD transient surges at terminal A with respect to terminal K, the voltage coupling effect raises up potential of gate  $G_2$  of NMOS  $M_2$ , which will increase the total substrate current ( $I_{sub}$ ) flowing to terminal K, generating an earlier turn-on of transistor  $Q_3$  base-emitter junction. Then the  $AG_2$ -coupled CULTdSCR ESD circuit will be triggered on at a lower  $V_{t1}$ , proved by both simulation and testing. On the other hand, if a negative ESD transient comes to terminal A against terminal K, the  $AG_2$ -coupled CULTdSCR circuit will still rely on punch-through breakdown under the open-gate  $M_1$  device to trigger the core VLTdSCR structure.

Hence, ESD triggering for the AG<sub>2</sub>-coupled CULTdSCR circuit has a triggering voltage of  $V_{t1} \sim 5.35V$  similar to the  $V_{t1} \sim 5.29V$  for the VLTdSCR core device. In addition, since the new CULTdSCR triggering effect does not affect ESD holding and discharging procedures, no change in  $V_h$  and  $R_{on}$  was observed for new CULTdSCR ESD protection circuit as confirmed in Figure 2.17. Therefore, an asymmetrical I-C curve is observed for the new AG<sub>2</sub>-coupled CULTdSCR ESD circuit as depicted in Figure 2.17.

#### 2.1.5.2 KG<sub>1</sub>-Coupled CULTdSCR ESD Protection Circuit

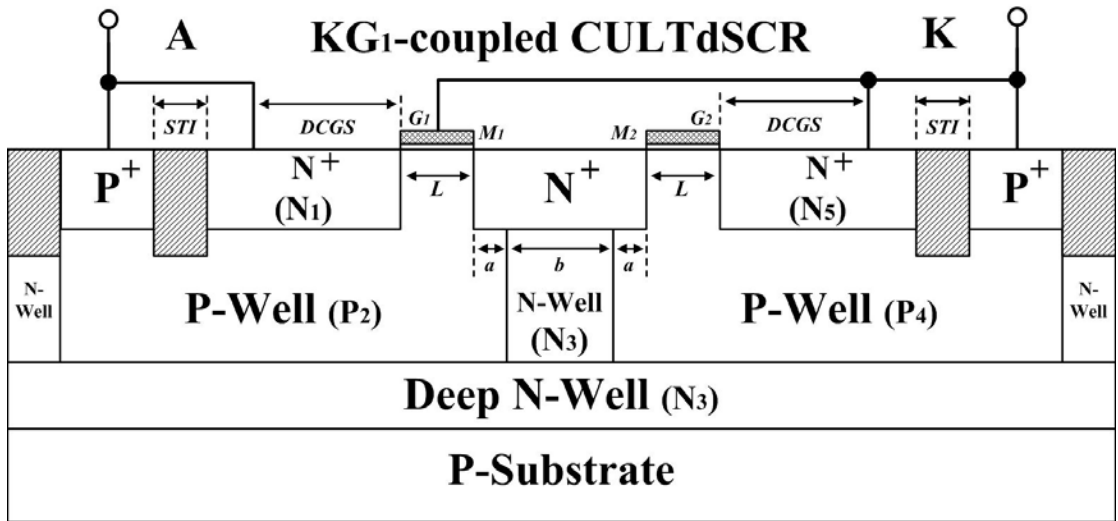


Figure 2. 18 X-section for sample KG<sub>1</sub>-coupled CULTdSCR ESD protection circuit.

Similarly, Figures 2.18 & 2.19 illustrate an alternative KG<sub>1</sub>-coupled CULTdSCR ESD protection circuit and its equivalent circuit where terminal K is connected to gate  $G_1$  of NMOS  $M_1$ , while gate  $G_2$  of NMOS  $M_2$  remains floating. The KG<sub>1</sub>-coupled CULTdSCR ESD circuit works similarly as the AG<sub>2</sub>-coupled CULTdSCR counterpart circuit.

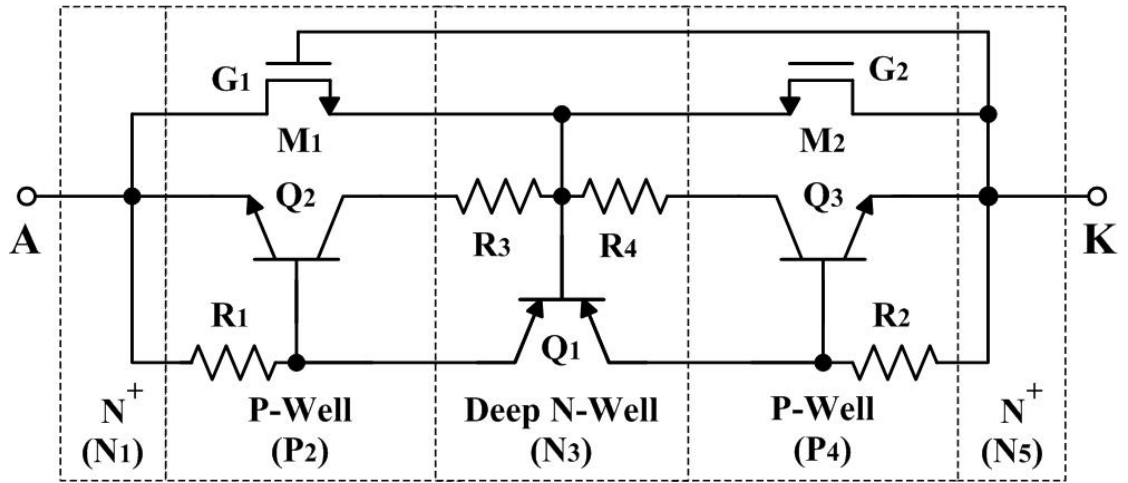


Figure 2. 19 Equivalent circuit of KG<sub>1</sub>-coupled CULTdSCR ESD protection circuit.

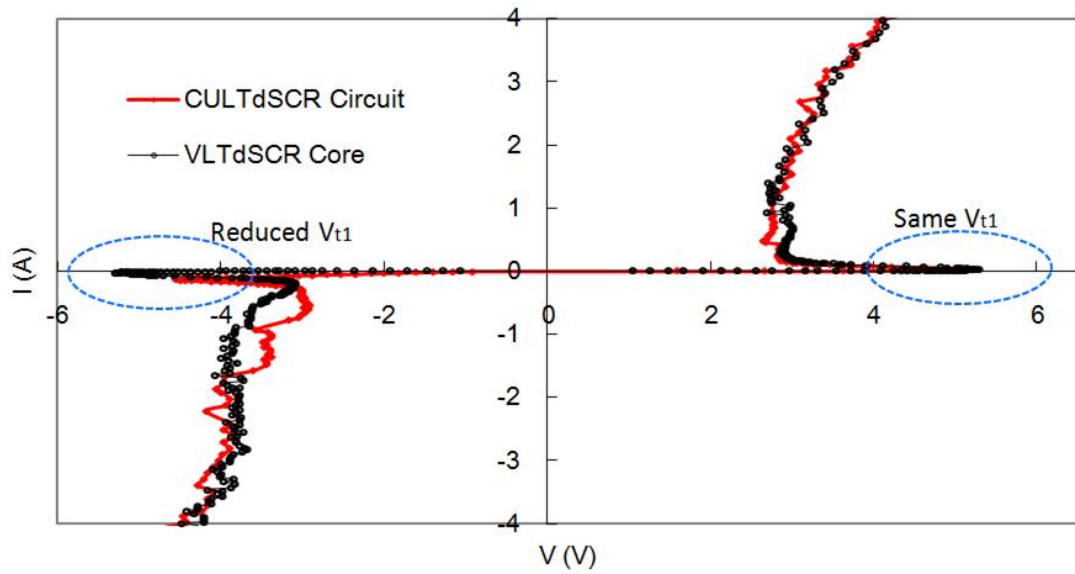


Figure 2. 20 Measured I-V curves by TLP testing sample VLTdSCR core SCR structure and cross-coupled CULTdSCR ESD protection circuit.

Figure 2.20 presents the expected asymmetrical I-V characteristics for new KG<sub>1</sub>-coupled CULTdSCR ESD circuit under negative ESD stressing from terminal A to terminal K by simulation and testing, which again shows required lower ESD

triggering of  $V_{t1} \sim 4.54V$ , however, an roughly unchanged triggering of  $V_{t1} \sim 5.23V$  under positive ESD surge terminal A to terminal K. The key testing data are also listed in Table 2.8. Clearly, the new cross-coupling trigger-assisting technique works well in reducing ESD triggering voltage for CULTdSCR ESD protection circuits. The CULTdSCR asymmetrical ESD protection features could be applied in specific RF/AMS ICs where various I/O ports may require different triggering voltages.

#### **2.1.5.3 AG<sub>2</sub>-KG<sub>1</sub> CULTdSCR ESD Protection Circuit**

A fully symmetrical double cross coupling CULTdSCR ESD circuit, i.e., AG<sub>2</sub>-KG<sub>1</sub> CULTdSCR ESD circuit was designed, based on the exactly same ESD triggering mechanism. As shown in Figure 2.21 for its cross-section and equivalent circuit, the new AG<sub>2</sub>-KG<sub>1</sub> CULTdSCR ESD circuit has the gate  $G_2$  of NMOS  $M_2$  connected to terminal A and the gate  $G_1$  of NMOS  $M_1$  connected to terminal K. In this way, for different polarity ESD transients between terminals A and K, the similar coupling effect will always aid the AG<sub>2</sub>-KG<sub>1</sub> CULTdSCR ESD circuit to achieve a reduced  $V_{t1}$ .



Figure 2.22 shows the measured symmetrical I-V curves for both the VLTdSCR core SCR structure and the CULTdSCR ESD circuit. It readily confirms that the CULTdSCR ESD circuit realizes lower ESD triggering voltages, 3.88V and 4.09V, in both directions. Table 2.8 summarizes all ESD-critical parameters for the new CULTdSCR ESD circuit and other traditional SCRs. Compared to other traditional SCR protection structures fabricated in the same technology, the CULTdSCR ESD circuits feature much lower triggering voltage.

#### **2.1.6 Conclusion**

The design, analysis and optimization of a new low-parasitic, ultra-low-triggering, dual-polarity VLTdSCR core ESD protection structure as well as a cross-coupling CULTdSCR ESD protection circuit implemented in a commercial 0.18 $\mu$ m CMOS. Embedded punch-through device and gate cross-coupling technique served as internal trigger-aiding methods to achieve ultra low ESD triggering for SCR-type ESD protection in CMOS.

Experiments fully verified the new ESD protection concepts. Measures show a record low  $V_{t1}$  of 3.83V, very fast ESD response within 100pS, NF of 0.2dB and parasitic  $C_{ESD}$  of 150fF for exemplary ESD structures. The sample VLTdSCR ESD structure of 90 $\mu$ m wide can handle  $I_{t2}$  of 5.07A for HBM and 4.10A for CDM ESD testing in both directions, translating into a very high ESD protection capability of

$\sim 7\text{V}/\mu\text{m}^2$ . Design techniques were provided to program ESD critical parameters, including  $V_{t1}$ ,  $V_h$  and  $I_{t2}$ , which are desired to meet different requirements on ESD design window in complex advanced CMOS technologies.

Table 2. 8  $V_{t1}$  comparison for different ESD protection structures

| ESD Structures                 |                                                              | TLP $V_{t1}(\text{V})$ |
|--------------------------------|--------------------------------------------------------------|------------------------|
| <b>Traditional ESD Designs</b> | SCR                                                          | 16.71                  |
|                                | MVSCR                                                        | 13.61                  |
|                                | LVSCR                                                        | 6.74                   |
|                                | ggNMOS                                                       | 6.58                   |
| <b>This Work</b>               | VLTdSCR core device baseline A-to-K Zapping (+)              | 5.29                   |
|                                | VLTdSCR core device baseline A-to-K Zapping (-)              | 5.29                   |
|                                | AG <sub>2</sub> -only CULTdSCR A-to-K Zapping (+)            | <b>4.14</b>            |
|                                | AG <sub>2</sub> -only CULTdSCR A-to-K Zapping (-)            | 5.35                   |
|                                | KG <sub>1</sub> -only CULTdSCR A-to-K Zapping (+)            | 5.23                   |
|                                | KG <sub>1</sub> -only CULTdSCR A-to-K Zapping (-)            | <b>4.54</b>            |
|                                | AG <sub>2</sub> -KG <sub>1</sub> CULTdSCR A-to-K Zapping (+) | <b>3.88</b>            |
|                                | AG <sub>2</sub> -KG <sub>1</sub> CULTdSCR A-to-K Zapping (-) | <b>4.09</b>            |



## **2.2 Nano Crossbar ESD Protection Structure**

### **2.2.1 Background**

ESD-induced leakage is becoming a serious concern in advanced IC designs, especially with the emergence of mobile electronics for which low power is a big issue. However, most traditional ESD protection structures contain PN junctions inside, unavoidably causing junction leakage current. On the other hand, the need for the ESD protection design against the very fast CDM is increasing [2][23]. Furthermore, ICs with multiple power domains ask for flexible ESD triggering voltage  $V_{t1}$  locally optimized for each power domain in order to meet the specific ESD design window. Therefore, there is an apparent demand for non-traditional novel and robust new ESD protection mechanism and structures, especially with extremely-low leakage and tunable triggering behavior in RF CMOS technologies.

### 2.2.2 Layout and X-section of Nano Crossbar ESD Protection Structure

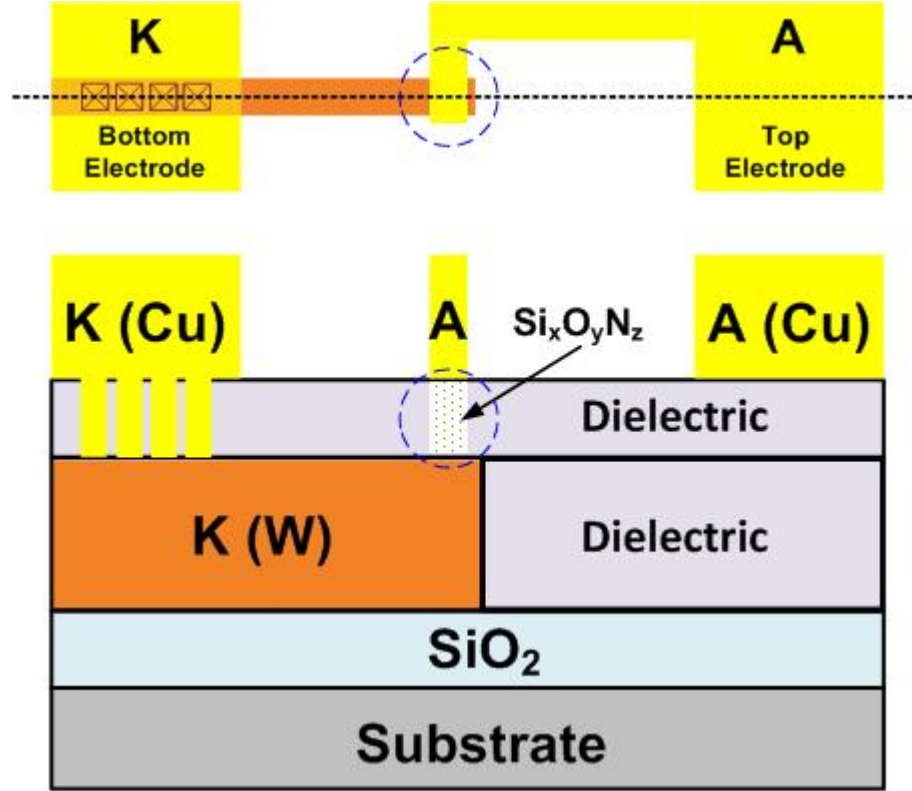


Figure 2. 23 Layout and X-section of nano crossbar ESD protection structure.

Figure 2.23 presents a new nano phase switching ESD protection concept realized as a nano crossbar structure. The core of the new structure is a new nano phase changing material, e.g.,  $\text{Si}_x\text{O}_y\text{N}_z$ , placed between two metal layers, i.e., Cu and W, being used as the electrodes anode (A) and cathode (K), respectively. Theoretically, the insulator nano dielectric ( $\text{Si}_x\text{O}_y\text{N}_z$ ) in the middle ensures no leakage. The new nano crossbar ESD protection structure has several advantages: First, it has extremely-low leakage in off state and uniform ESD discharging; Second, it could provide dual-direction ESD protection, reducing the amount of ESD protection

structures used on a chip [2]. Third, its unique structure allows the fabrication of nano crossbar array, which will contain many parallel-connected single nano crossbar ESD protection structure and can turn on together to form massive ESD shunting branches.

### 2.2.3 Fabrication of Nano Crossbar ESD Protection Structure

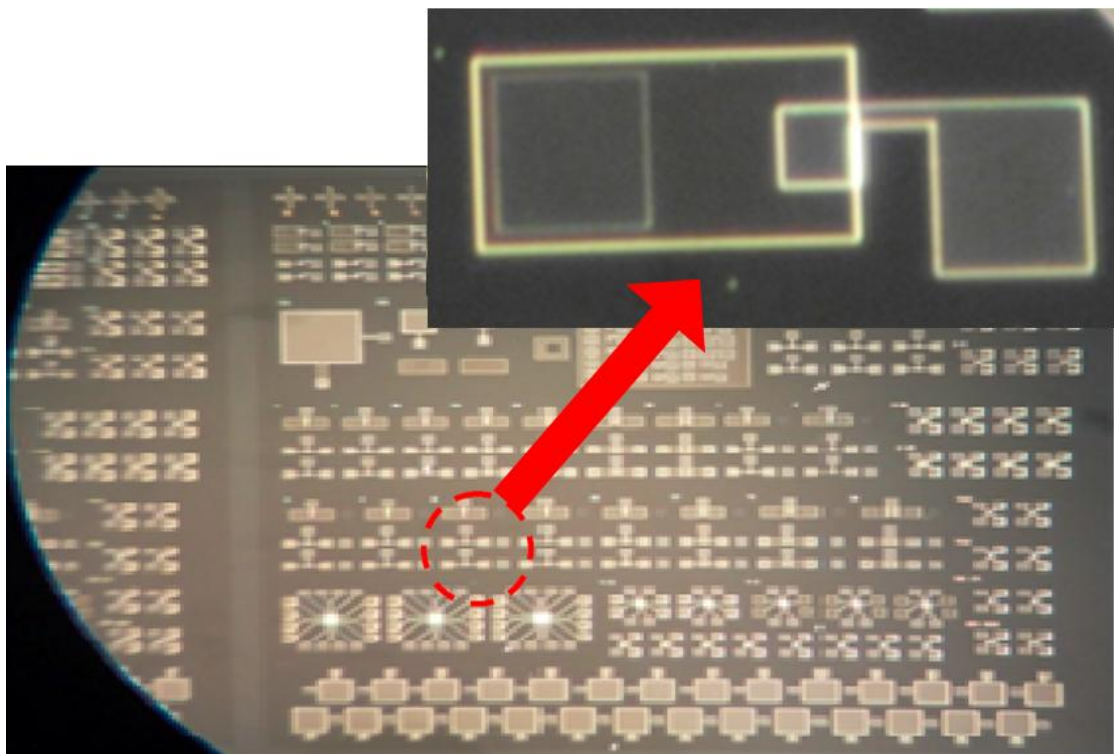


Figure 2. 24 Die photo of nano crossbar ESD protection structures.

The new nano crossbar ESD protection structures were fabricated using a simple process module compatible to common IC technologies: First, a 100nm-thick W layer was deposited onto the  $\text{SiO}_2$  layer above a substrate. Second, reactive ion etching (RIE) was used to define the electrode K. Third, a 50nm-thick nano  $\text{Si}_x\text{O}_y\text{N}_z$  medium

was formed by plasma-enhanced chemical vapor deposition (PECVD). Careful tuning was done to adjust the material composition by reactive gas ratio of  $N_2O/SiH_4$ . Fourth, vias were formed for bottom connection. Finally, Cu was deposited by physical vapor deposition (PVD) to form the A and K pads. A large set of nano crossbar structures were designed and fabricated for complete characterization. The design splits include size variation (from  $1\mu m \times 1\mu m$  to  $80\mu m \times 80\mu m$ ), composition ratio and thickness change of nano phase changing materials ( $Si_xO_yN_z$ ). Figure 2.24 shows the die photo of the new ESD devices.

#### **2.2.4 Nano Crossbar Structure ESD Protection Scheme and Mechanism**

Figure 2.25 depicts a typical on-chip ESD protection scheme with the new nano crossbar ESD protection structures. One nano crossbar ESD protection device can provides dual-direction ESD protection to against ESD transients in different directions, such as PD, ND, PS and NS, as shown in Figure 2.25.

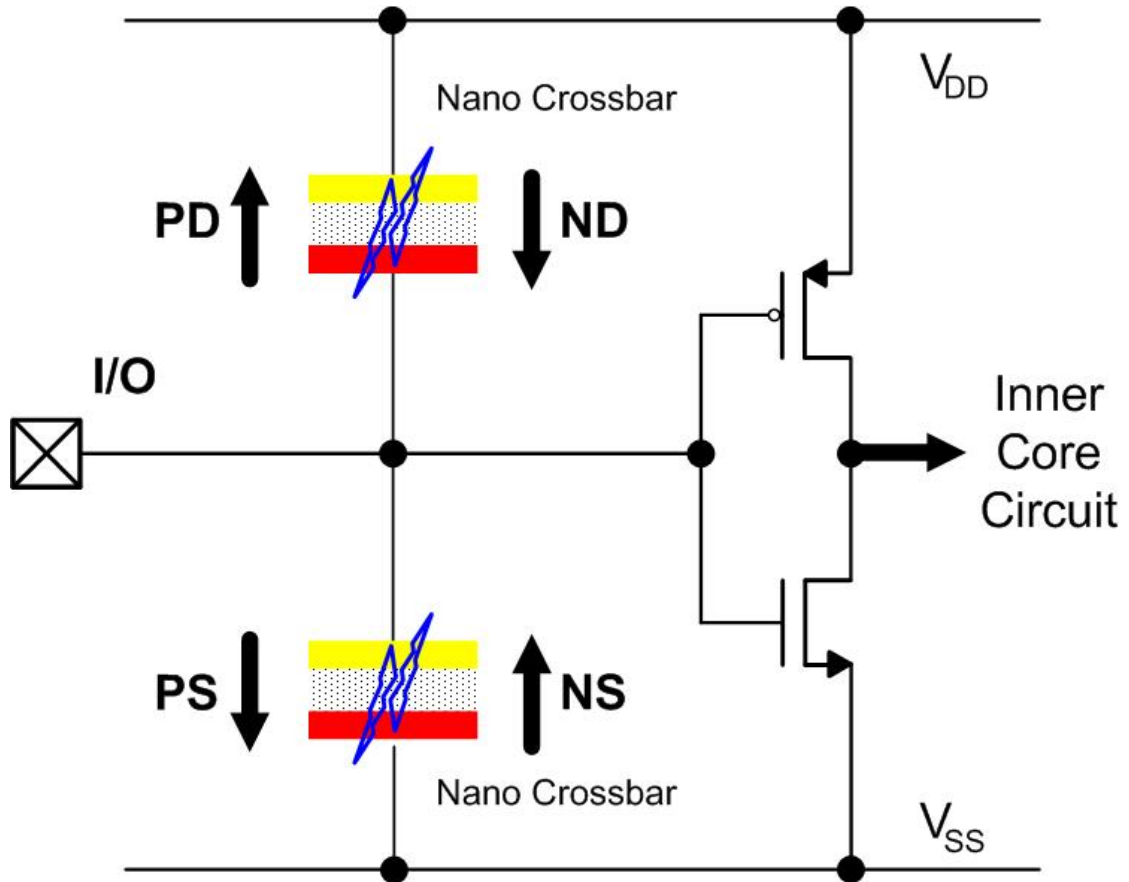


Figure 2. 25 ESD protection scheme of nano crossbar ESD protection structures.

The nano ESD crossbars act like ideal switches. They will stay off and eliminate leakage during normal IC operation. When an ESD transient surges at the I/O port, one of the nano crossbar will be turned on at a given ESD triggering  $V_{t1}$  to shunt the ESD surge. After the ESD event, the nano crossbar ESD protection device will return to off status. Different from the traditional ESD protection structures including diode, bipolar, ggNMOS, gcNMOS, SCR and their derivatives, there is no PN junction inside the nano crossbar structure. Thus, the nano crossbar ESD protection device ensures extremely-low leakage, which has been confirmed experimentally.

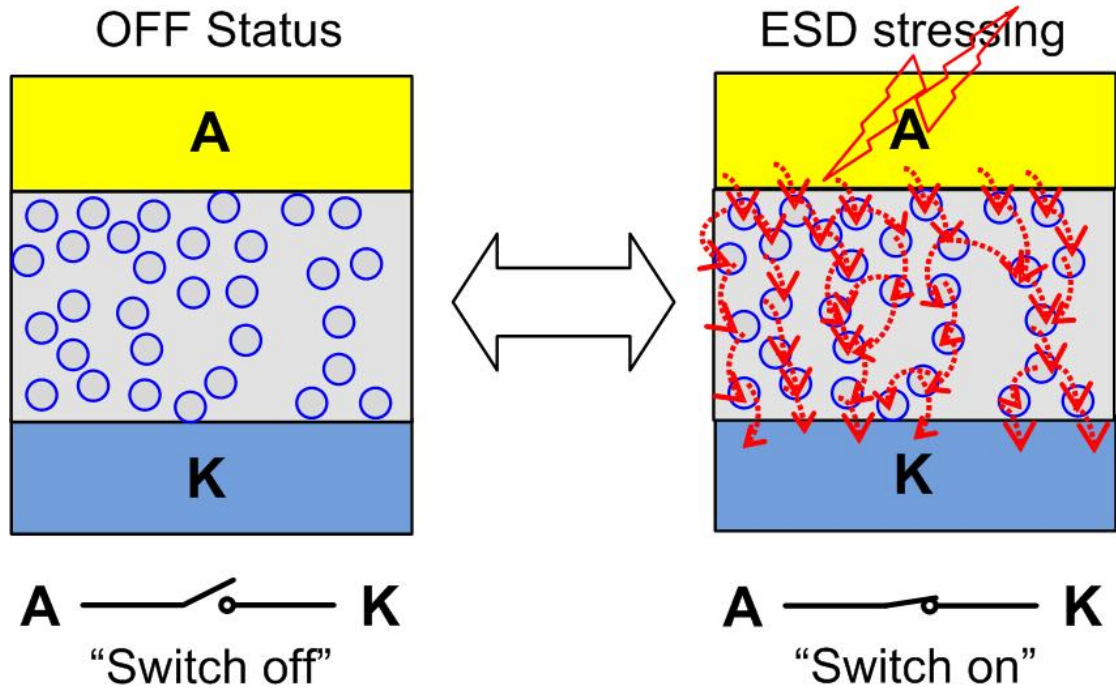


Figure 2. 26 The dispersed local ESD tunneling model of nano crossbar structure.

Figure 2.26 shows a new dispersed local ESD tunneling model proposed to depict the new nano crossbar ESD protection mechanism. The porous nano  $\text{Si}_x\text{O}_y\text{N}_z$  medium is formed for easy Cu diffusion. Low-temperature annealing pre-diffuses and disperses Cu ions into  $\text{Si}_x\text{O}_y\text{N}_z$  where Cu is trapped by O/N atoms throughout. The device remains in hi-R OFF state during IC normal operation. When ESD stress comes between nodes A and K, a strong electric field forms and leads to local electron tunneling between neighboring Cu ions, which have been dispersed throughout  $\text{Si}_x\text{O}_y\text{N}_z$ , to form low-R ( $R_{\text{on}}$ ) conduction tunnels for ESD discharging. After ESD transient, tunneling process ends and nano crossbar device returns to OFF status.

## 2.2.5 Experimental Results and Characterizations

TLP and VF-TLP tests were done to evaluate nano crossbar ESD structures ESD protection ability. In addition, DC leakage current tests under different conditions were done to investigate the nano crossbar leakage immunity, too.

### 2.2.5.1 Nano Crossbar Structure ESD Protection Behavior

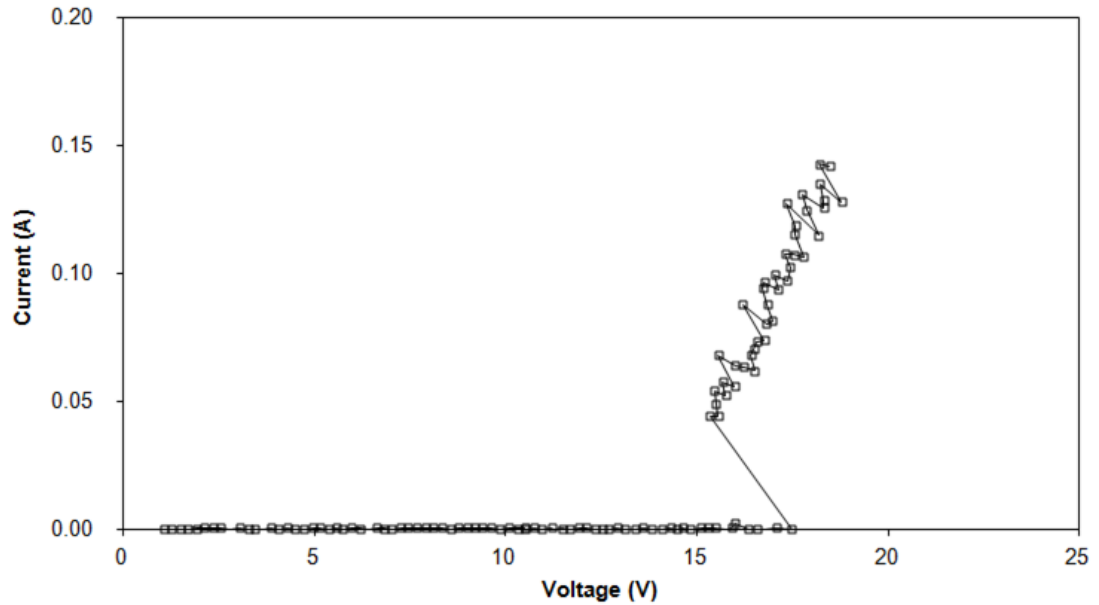


Figure 2. 27 Measured TLP I-V curve of a 1 $\mu$ mX1 $\mu$ m nano crossbar ESD protection structure.

HBM ESD performance is characterized by TLP testing. Figure 2.27 presents the measured I-V curve for a 1 $\mu$ mX1 $\mu$ m nano crossbar device by TLP testing from A to K. It can be seen that the nano crossbar ESD protection device is triggered at  $V_{t1} \sim 17.5V$  and then starts discharging in low-R status. The observed ESD discharging current for this 1 $\mu$ mX1 $\mu$ m nano crossbar device could reach 143mA, equivalent to a HBM ESD

protection level of at least  $215\text{V}/\mu\text{m}^2$ . TLP testing from K to A was also done, proving dual-direction ESD protection ability.

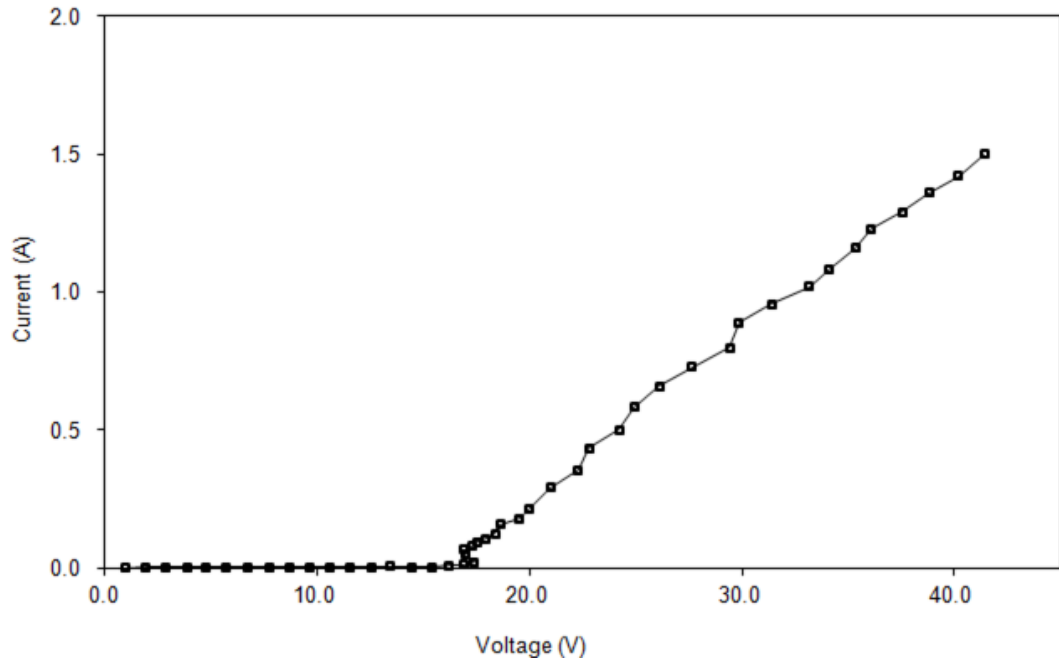


Figure 2. 28 Measured VF-TLP I-V curve of a  $60\mu\text{m} \times 60\mu\text{m}$  nano crossbar structure.

Very fast VF-TLP testing was also done to study the device ultra fast CDM ESD discharging performance. Figure 2.28 shows the measured fast ESD discharging I-V curve for a  $60\mu\text{m} \times 60\mu\text{m}$  nano crossbar sample device by VF-TLP pulses with  $t_r \sim 100\text{pS}$  and  $t_d \sim 5\text{nS}$ . It shows that for the VF-TLP stress, the nano crossbar ESD device is able to turn on at  $V_{t1} \sim 17.4\text{V}$ , confirming that it can be used for ultra fast CDM ESD protection.



### 2.2.5.2 Nano Crossbar ESD Protection Structure Triggering Features

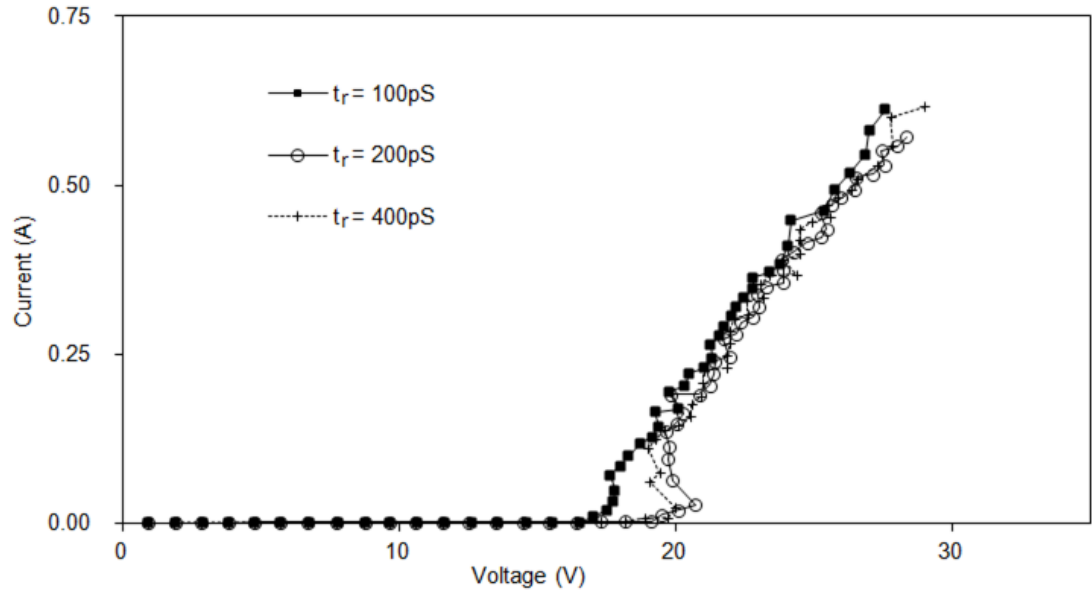


Figure 2. 29 Measured VF-TLP I-V curves of a 40μmX40μm nano crossbar structure under different pulse rise time  $t_r$  from 100pS to 400pS.

Figure 2.29 depicts I-V curves for several 40μmX40μm nano crossbar samples by VF-TLP testing with different fast rise time  $t_r$  from 100pS, 200pS to 400pS. The testing results further prove that that the new nano crossbar ESD protection devices can respond to extremely fast CDM ESD surges. The extracted  $V_{t1}$  values for different rise time are summarized in Table 2.9.

Table 2. 9  $V_{t1} \sim t_r$  comparison by VF-TLP testing.

| VF-TLP $t_r$ (pS) | 100    | 200    | 400    |
|-------------------|--------|--------|--------|
| $V_{t1}$ (V)      | 17.809 | 20.688 | 19.987 |

Table 2. 10  $V_{t1}$  comparison among various device sizes by VF-TLP testing.

| Size ( $\mu\text{m} \times \mu\text{m}$ ) | 20X20  | 30X30  | 40X40  | 50X50  | 60X60  |
|-------------------------------------------|--------|--------|--------|--------|--------|
| $V_{t1}$ (V)                              | 20.095 | 20.699 | 18.958 | 20.405 | 19.610 |
| $R_{on}$ ( $\Omega$ )                     | 26.941 | 22.975 | 21.513 | 18.930 | 17.246 |
| $I_{leak}$ (pA)                           | 2.878  | 1.013  | 2.725  | 1.894  | 1.908  |

Table 2.10 compares critical ESD parameters obtained by VF-TLP testing for sample nano crossbar ESD structures with different sizes ranging from  $20\mu\text{m} \times 20\mu\text{m}$  to  $60\mu\text{m} \times 60\mu\text{m}$  but with the same  $\text{Si}_x\text{N}_y\text{O}_z$  composition ratio and material thickness. It is readily observed that the ESD triggering  $V_{t1}$  for different devices may not be affected by the device sizes; however, the ESD discharging resistance  $R_{on}$  is roughly inversely proportional to the crossbar size in a monolithic mode. The phenomena strongly support the new dispersed local ESD tunneling model proposed above in two ways: First, ESD discharging is triggered by nano material phase switching by certain electrical field density determined by the ESD surges between nano crossbar device electrodes. Second, the dispersed local tunneling effect leads to ESD discharging directly proportional to the device size. Larger device size means more dispersed local shunting tunneling effects will emerge during ESD transient. It is very different from the reported phase changing memory mechanism, for which a rather fixed number of conducting strings within a device resulted in a constant conduction resistance [24][25].

Table 2. 11  $V_{t1} \sim \text{Si}_x\text{O}_y\text{N}_z$  composition by VF-TLP testing.

| Devices | Si:O:N      | $V_{t1}$ (V)                       |                                    |                                    |
|---------|-------------|------------------------------------|------------------------------------|------------------------------------|
|         |             | 30 $\mu\text{m}$ X30 $\mu\text{m}$ | 40 $\mu\text{m}$ X40 $\mu\text{m}$ | 60 $\mu\text{m}$ X60 $\mu\text{m}$ |
| I       | 1:0.95:0.54 | 39.193                             | 39.495                             | 37.065                             |
| II      | 1:0.66:0.45 | 16.135                             | 15.932                             | 17.426                             |
| III     | 1:0.42:0.39 | 8.987                              | 8.704                              | 9.059                              |
| IV      | 1:1.93:0.08 | 20.670                             | 20.213                             | 19.350                             |

Atomic emission spectroscopy (AES) analysis was conducted to understand the nano dielectric materials used including the composition ratios. Table 2.11 summaries ESD  $V_{t1}$  related to different nano  $\text{Si}_x\text{O}_y\text{N}_z$  compositions, which further confirms that ESD triggering threshold seems to be independent of the device sizes as suggested the new tunneling model. It also shows that the nano medium composition has strong impact on ESD triggering, mainly due to the different local tunneling effects decided by the different amount of Cu ions trapped by O/N atoms. In addition, it demonstrates clearly that a wide adjustable ESD triggering voltage, i.e.,  $V_{t1}$  of 8.7V ~ 39.50V, can be achieved by designing the nano phase switching materials, which is highly desirable for ICs with multiple power domains.

### 2.2.5.3 Nano Crossbar ESD Protection Structure DC Leakage Properties

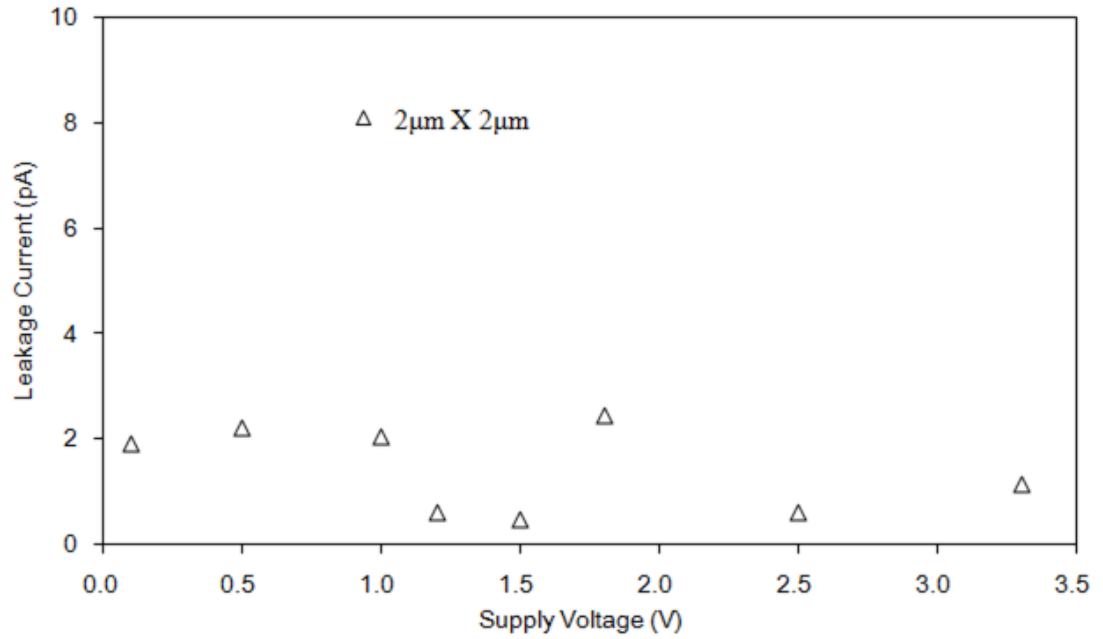


Figure 2. 30 Measured extremely-low pA-level leakage current for a 2 $\mu$ mX2 $\mu$ m sample.

Figure 2.30 shows the measured leakage current for one sample 2 $\mu$ mX2 $\mu$ m nano crossbar ESD device under typical DC biasing voltage from 0.1V to 3.3V, which is extremely low, i.e., <2.5pA. The reason for the new nano switching ESD structure extremely low leakage could be attributed to the insulating nano medium between two metal layers, which keeps OFF under normal IC biasing. Such extremely-low leakage level cannot be expected for all traditional PN-junction-based ESD structures, especially those fabricated in the advanced nanometer-scale ICs. Table 2.10 shows that the measured leakages for nano ESD devices with different sizes are all extremely low.

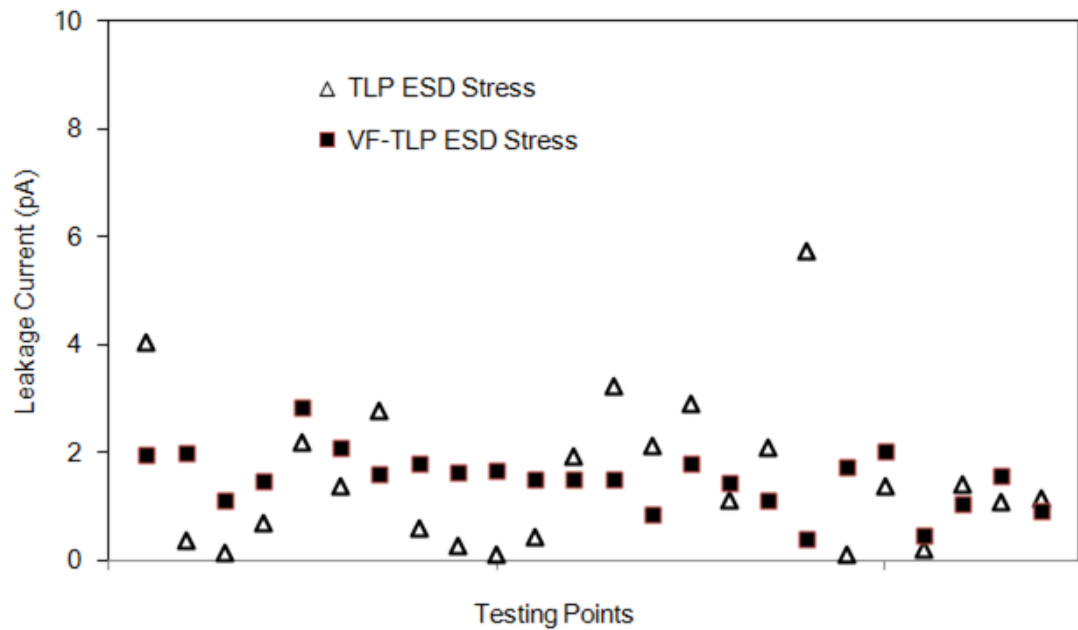


Figure 2. 31 Measured leakages for 60μmX60μm devices after repeating TLP and VF-TLP

ESD stresses remain very low.

Figure 2.31 shows the measured leakage currents for several 60μmX60μm devices after repeating TLP and VF-TLP surges. It seems that repeating ESD stressing has no negative influence on leakage of the tested nano crossbar ESD devices. That means the nano materials inside the nano crossbar devices could survive repeating TLP and VF-TLP ESD stresses without any latent damages and leakage current increase.

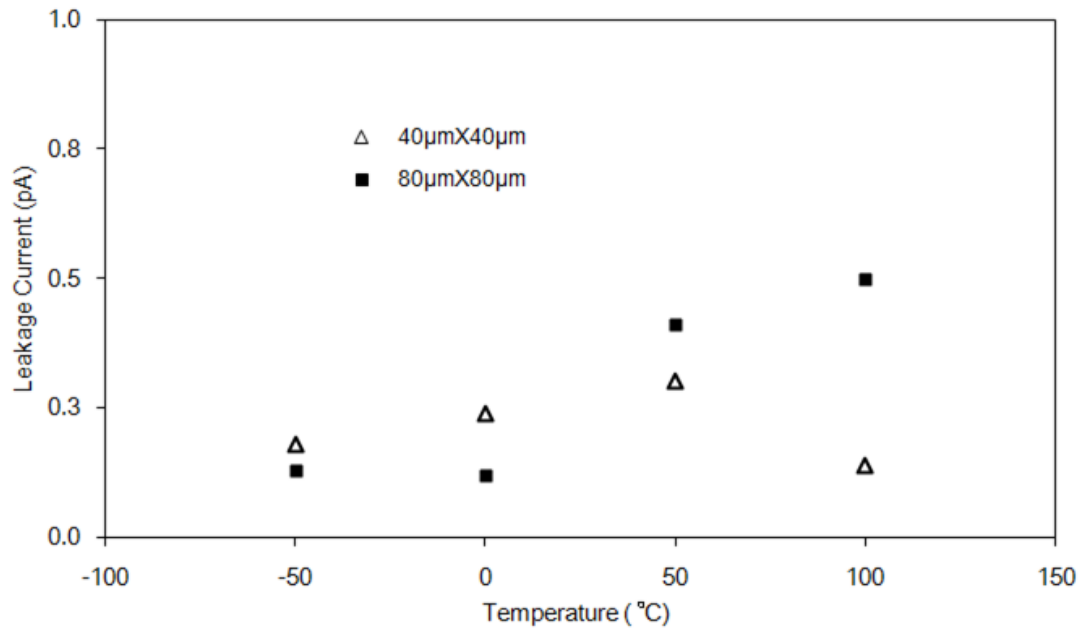


Figure 2. 32 Measured ESD leakage across a wide temperature range remains very low.

Figure 2.32 presents the measured leakage for sample nano crossbar ESD devices across a wide temperature range from -50° C to +100° C. For such a wide temperature range, the leakage currents of all sample nano crossbar ESD protection devices always stay very low. It can be seen that the new nano crossbar ESD protection structures ensure extremely low leakage around pA level, in spite of some fluctuations on the some absolute leakage current values. It is a huge advantage over all traditional PN-junction-based ESD protection structures.

### 2.2.6 Conclusion

A new nano crossbar ESD protection structure is proposed, which features dual-direction ESD protection ability, extremely-low leakage current, adjustable triggering voltage  $V_{t1}$  and fast turn-on speed. A new dispersed local ESD tunneling model was used to explain the new ESD protection concept and mechanism. The model shows the device local ESD tunneling could be affected by the nano material  $\text{Si}_x\text{O}_y\text{N}_z$  composite ratio, leading to tunable  $V_{t1}$  with wide range of more than 30V. In addition, the unique P-N-junction-free device structure ensures the nano crossbar ESD protection device extremely-low leakage under various conditions, superior to most traditional ESD protection structures. Experiments also confirm the nano crossbar device has ultra fast ESD response time, around 100pS, and fairly robust ESD protection capability of at least  $215\text{V}/\mu\text{m}^2$ . The nano crossbar ESD protection device is suitable for ESD protection designs in applications with high standard on leakage.

## **Chapter 3 Overview of Ultrasonic Medical Imaging**

### **3.1 Background**

Biomedical electronics is becoming indispensable to modern health care solutions. Among many medical imaging solutions, ultrasonic medical imaging is an enabling technology and popular method for medical diagnosis, which collects reflected ultrasonic waves from human body in the path of ultrasonic wave propagation, convert them into electronic signal, process those signals and generate real-time image of tissues or organs in human body. Compared with other medical imaging methods, such as computed tomography (CT) and magnetic resonance imaging (MRI), the ultrasonic medical imaging features dynamic and continuous real-time scan, which is critical for doctors to conduct accurate examinations for many health problems, e.g., organ tumors and heart disease [26]. In addition, its non-invasive and non-radioactive nature is particularly desired for pregnancy and infant examinations.

### **3.2 Ultrasonic Imaging System Architecture**

A pulse-echo ultrasonic (B-mode) medical imaging system is usually composed by a chain of processing stages, as shown in Figure 3.1. The transducer is excited by the pulse from the high-voltage pulse generator (HV pulser) to transmit ultrasonic waves. Then it will function as a receiver to convert ultrasonic echoes to electronic



signal. The transmit/receive switch (T/R switch) controls the system to switch between transmitting and receiving cycles. The preamplifier (usually a low-noise amplifier, LNA) and time-gain compensator (TGC) realize the signal amplifying and dynamic range compressing. Then the analog/digital convertor (ADC) will convert the analog signal to digital signal, which will be processed by the image processing stage and output to the display terminal. All the stages above are controlled by the timing logic.

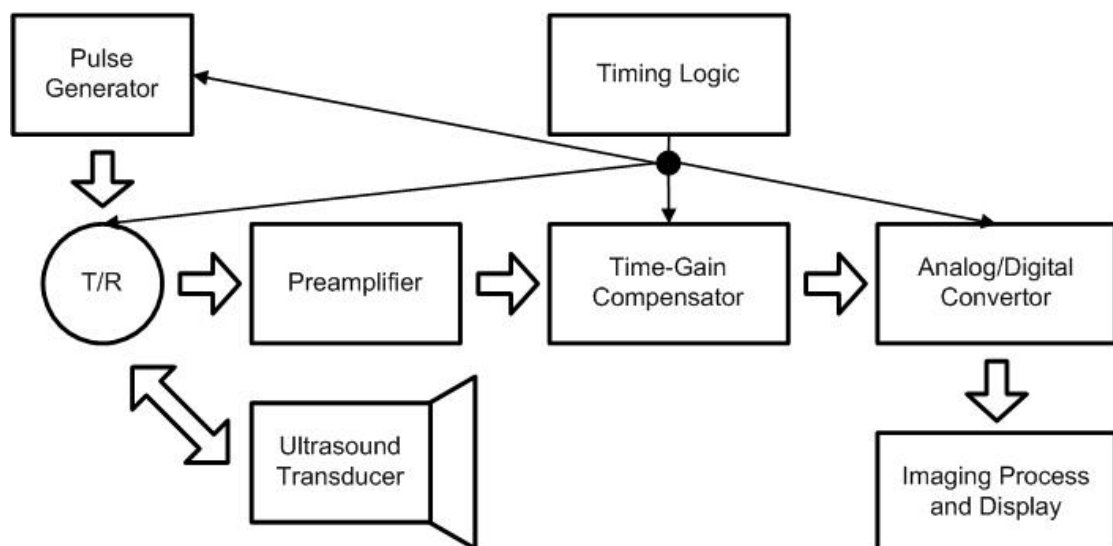


Figure 3. 1 The architecture of a pulse-echo ultrasonic (B-mode) medical imaging system.

### 3.2.1 Piezoelectric Materials, Transducer and cMUT

Ultrasonic transducer, converting electrical energy to ultrasonic mechanical energy and vice versa, is a necessary part for the ultrasonic medical imaging system. It could generate and transmit ultrasonic waves when excited by electric signals; it could be used to receive and convert ultrasonic waves to electric signals, too.

### 3.2.1.1 Piezoelectric Materials

The piezoelectric material is the most important element among all the transducer materials because it realizes the transducer core function: the interconversion between electric energy and mechanical energy. In 1880, several piezoelectric asymmetrical crystalline minerals, such as Quartz, Tourmaline and Rochelle salt, were discovered by Curie brothers. It was showed that the mechanical deformation of piezoelectric material would generate voltage drop on itself, known as direct piezoelectric effect. On the other hand, forcing voltage on the piezoelectric material will cause the material itself deformation, which is referred as inverse piezoelectric effect.

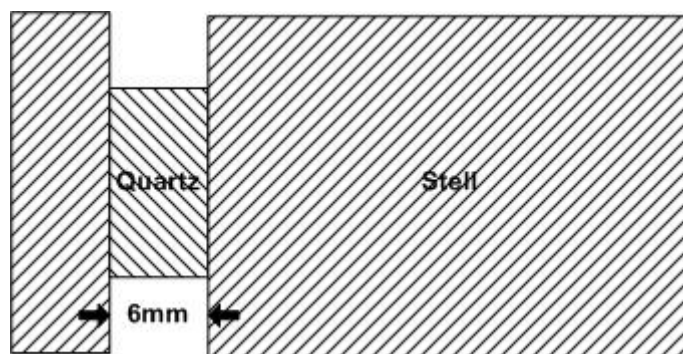


Figure 3. 2 "Langevin's sandwich" transducer.

The first application of the piezoelectric effect to a practice device was developed by Langevin during the First World War. His invention, known as "Langevin's sandwich", was designed to generate high frequency sound waves in the water to detect enemy's submarines, shown in Figure 3.2.

As for the development of the ultrasonic piezoelectric materials besides quartz, in 1940s, Barium Titanate ( $\text{BaTiO}_3$ ) was discovered and applied on medical ultrasonic. This lead-free ceramic has piezoelectric properties and can be used to efficiently generate acoustic bulk waves above 1MHz. In the middle of 1950s, the Lead Zirconate Titanate (PZT) ceramics was discovered and soon became the dominant piezoelectric materials in medical ultrasonic field to produce ultrasonic in MHz range. In 1969, piezoelectric polymers, especially Polyvinylidene Fluoride (PVDF, or  $\text{PVF}_2$ ), were discovered, it had higher sensitivity than PZT but lower electromechanical coupling, thus it cannot replace PZT ceramics in some high frequency applications. Different piezoelectric composites, combining PZT and PVDF together, have also been developed to provide better ultrasonic transducers. In recent years, some PZT-based crystals, like Lead magnesium niobate / lead titanate (PMN-PT) and Lead zirconate niobate / lead titanate (PZN-PT), were investigated, too. These piezoelectric crystals have high performance of piezoelectricity but relatively high cost of production.

Table 3. 1 Properties of Piezoelectric Materials.

| Piezoelectric Materials | Name                                                       | Chemical Formula                                                      | Density $\rho$<br>$10^3 \text{ kgm}^{-3}$ | $T_u / T_c$<br>$^{\circ}\text{C}$ | $d_{33}$<br>$10^{-12}\text{C/N}$ | $g_{33}$<br>$10^{-2}\text{V/mN}$ | Electromechanical Coupling Coefficient |          |          |          |       |                           | Loss                 |  |
|-------------------------|------------------------------------------------------------|-----------------------------------------------------------------------|-------------------------------------------|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------|----------|----------|----------|-------|---------------------------|----------------------|--|
|                         |                                                            |                                                                       |                                           |                                   |                                  |                                  | $k_p$                                  | $k_{31}$ | $k_{33}$ | $k_{15}$ | $k_t$ | $Q_M$                     | $Q_E = 1/\tan\delta$ |  |
| Single Crystals         | Quartz (x-cut)                                             | $\text{SiO}_2$                                                        | 2.65                                      | 573                               | $d_{11} \sim 2.30$               | $g_{11} \sim 5.80$               |                                        |          |          |          | 0.14  | 180,000<br>$\sim 290,000$ | $\sim 2,000,000$     |  |
|                         | Lithium niobate                                            | $\text{LiNbO}_3$                                                      | 4.64                                      | 1150                              | 6                                |                                  |                                        |          |          |          | 0.49  | 10,000                    | 1,000                |  |
|                         | Lead magnesium niobate / lead titanate (PMN-%35PT 001-cut) | $\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3\text{--PbTiO}_3$ | 8.06                                      | 160                               | 1240                             |                                  |                                        |          | 0.923    |          |       | 35.3                      | 32                   |  |
|                         | Lead zirconate niobate / lead titanate (PZN-%8PT 001-cut)  | $\text{Pb}(\text{Zn}_{1/3}\text{Nb}_{2/3})\text{O}_3\text{--PbTiO}_3$ | 8.2                                       | 165                               | 2070                             |                                  |                                        |          | 0.938    |          |       | 39.5                      | 59                   |  |
|                         | Barium titanate                                            | $\text{BaTiO}_3$                                                      | 5.7                                       | 115                               | 190                              |                                  | -0.36                                  | -0.21    | 0.50     | 0.48     | 0.38  | 300                       | 100                  |  |
| Piezoelectric Ceramics  | Potassium-sodium niobate                                   | $\text{K}_{0.5}\text{Na}_{0.5}\text{NbO}_3$                           | 4.46                                      | 420                               | 127                              |                                  | -0.46                                  | -0.27    | 0.605    | 0.645    | 0.46  | 240                       | 70                   |  |
|                         | Lead Metaniobate                                           | $\text{PbNb}_2\text{O}_6$                                             | 6.0                                       | 570                               | 85                               |                                  | -0.07                                  | -0.045   | 0.38     | -        | 0.37  | 11                        | 100                  |  |
|                         | Lead zirconate titanate (PZT)<br>(PZT-5H)                  | $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$                     | 7.5                                       | 193                               | 593                              | 1.91                             | -0.65                                  | -0.39    | 0.75     | 0.675    | 0.505 | 65                        | 50                   |  |
|                         | Barium lead metaniobate                                    | $\text{Pb}_{0.6}\text{Ba}_{0.4}\text{Nb}_2\text{O}_5$                 | 5.9                                       | 260                               | 220                              |                                  | -0.38                                  | -0.22    | 0.55     | -        | -     | 250                       | 100                  |  |
|                         | Polyvinylidene Fluoride (PVDF)                             | " $-\text{CH}_2\text{--CF}_2$ "                                       | 1.78                                      | 150                               | 15                               | 14                               |                                        |          |          |          | 0.144 | 10                        | 4                    |  |

As summarized in the Table 3.1, there are many different parameters to describe the features of the piezoelectric materials [27-41]. The electromechanical coupling coefficients, such as  $k_{33}$ ,  $k_t$ ,  $k_{31}$ ,  $k_p$ , and  $k_{15}$ , describe the conversion of energy from electrical to mechanical form or vice versa. The ratio of the stored converted energy of one kind (mechanical or electrical) to the input energy of the second kind (electrical or mechanical) is defined as the square of the coupling coefficient, which is generally used to evaluate material piezoelectric performance.

The piezoelectric constants relating the mechanical strain produced by an applied electric field are termed the strain constants, or the "d" coefficients. Large  $d_{ij}$  constants mean large mechanical displacements, usually desirable for the applications of motional transducers. Further, the piezoelectric constants relating the electric field produced by a mechanical stress are termed the voltage constants, or the "g" coefficients. High  $g_{ij}$  constants lead to large voltage output for even small deformation, necessary for building acoustic sensors.

Curie temperature is the temperature at which the crystal structure changes from a non-symmetrical (piezoelectric) to a symmetrical (non-piezoelectric) form. In addition,  $Q_m$  is the ratio of reactance to resistance in the equivalent series circuit representing the mechanical vibrating resonant systems.

### 3.2.1.2 Capacitive Micromachined Ultrasonic Transducer (cMUT)

Another technology used to produce ultrasonic transducer, especially for large-scale arrays integrated to the front-end electronic circuits [42][43], is the capacitive micromachined ultrasonic transducer (cMUT). The X-section of cMUT is shown in the Figure 3.3. An evacuated and sealed cavity is placed between two electrodes. The distance between two electrodes,  $D$ , is around several hundred of nanometers, increasing the electric field strength across the electrodes. In addition, the top and bottom electrodes are composed of very thin material. A membrane is attached under the top electrode and able to vibrate. The cMUT can be used to generate ultrasonic waves, to replace piezoelectric materials in transducers. The thickness of the cavity and membrane will decide the cMUT operating frequency and output power.

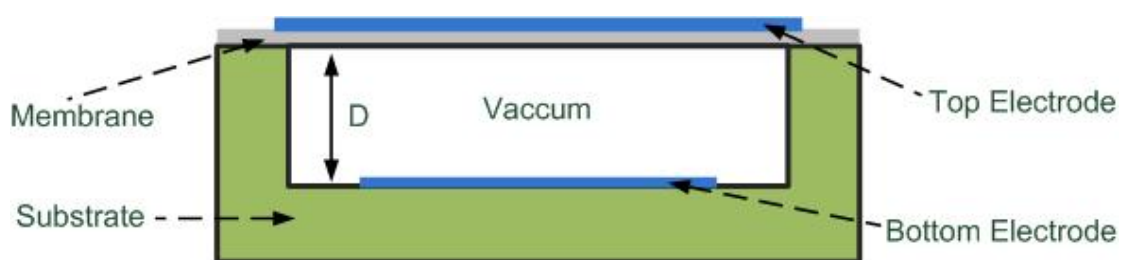


Figure 3. 3 cMUT X-section.

Two methods, surface micromachined devices and bulk micromachined devices [44], are usually employed to fabricate cMUTs. However, It is hard to maintain uniformity and consistence in the fabrication of cMUTs in large scale. In addition, the

cMUTs are needed to be steadily bonded to the electrodes for proper function. Another problem for cMUTs application in ultrasonic imaging is that its performance still cannot match the traditional piezoelectric materials, especially PZTs.

### 3.2.2 High-Voltage Pulse Generator

A widely-used architecture for the ultrasonic high-voltage pulse generator (HV pulser) is shown in the Figure 3.4. The circuit uses a level shifter to control the HV double diffused MOS (DMOS) devices to generate the exciting voltage pulse for ultrasound transducer. The peak-to-peak transmit voltage is typically on the order of 300V. For some portable systems, it could be reduced to as low as 50V.

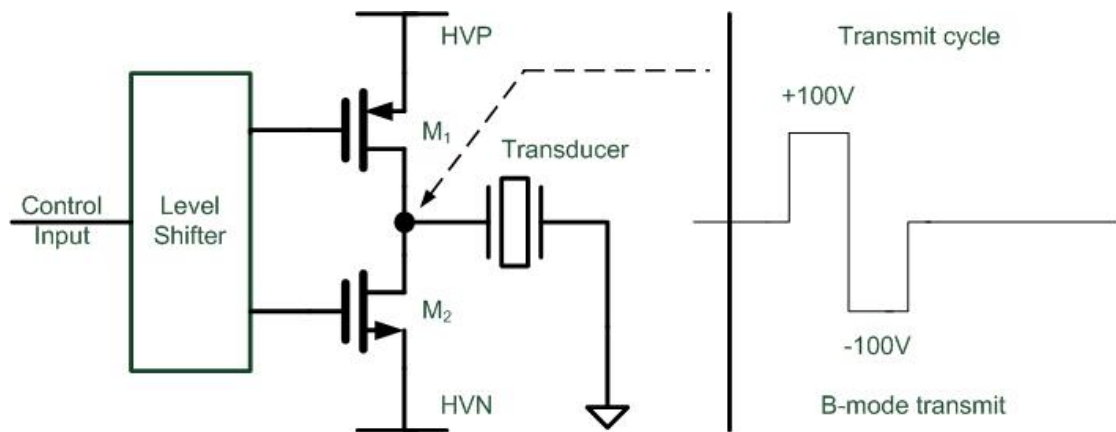


Figure 3. 4 HV pulser controlled by level shifter and its output HV pulse.

The timing logic control input signals, generated by the LV timing logic unit, will be shifted up by the level shifter to the high voltages, such as HVP and HVN. The level shifter should be able to drive the input capacitances of the large output devices  $M_1$  and  $M_2$ , to produce fast pulses for high-frequency transducer.

### 3.2.3 Transmit/Receive Switch

A transmit/receive switch (T/R switch) works as a voltage limiter to avoid high voltage impulse getting into the receiver. It could be implemented by resistor, diode or MOSFET.

A simple solution to T/R switch is a resistor limiter, shown in Figure 3.5 (a), consisting of a resistor and a parallel-connected diode voltage limiter. In the transmitting period, the limiter diodes will clamp the amplifier input to a forward diode voltage drop and most of the high-voltage pulse will drop on the resistor  $R_1$ . In the receiving period, the received small signals will not turn on the limiter diode and hence input into the pre-amplifier.

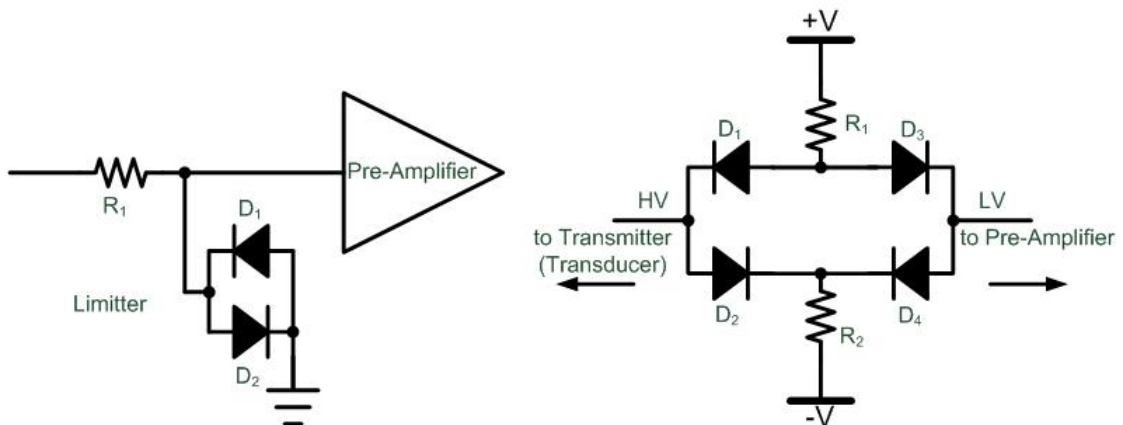


Figure 3. 5 (a) resistor limiter circuit or (b) diode bridge used as a T/R switch.

In addition, the diode bridge could be used as a T/R switch, too [45]. As shown in Figure 3.5 (b), the diodes are all forward biased by the positive and negative voltage biases. In the transmitting period, two diodes,  $D_1$  and  $D_4$ , will be reversed biased by



the high voltage at transmitter side. The diode bridge is now close and hence transmitter and pre-amplifier are isolated from each other. In the receiving period, the low received signal will keep the diode bridge in on status and be able to pass the bridge to the pre-amplifier input. However, with the increasing channel number, the always-on forward diodes in the diode bridge will cause the problem of high power consumption.

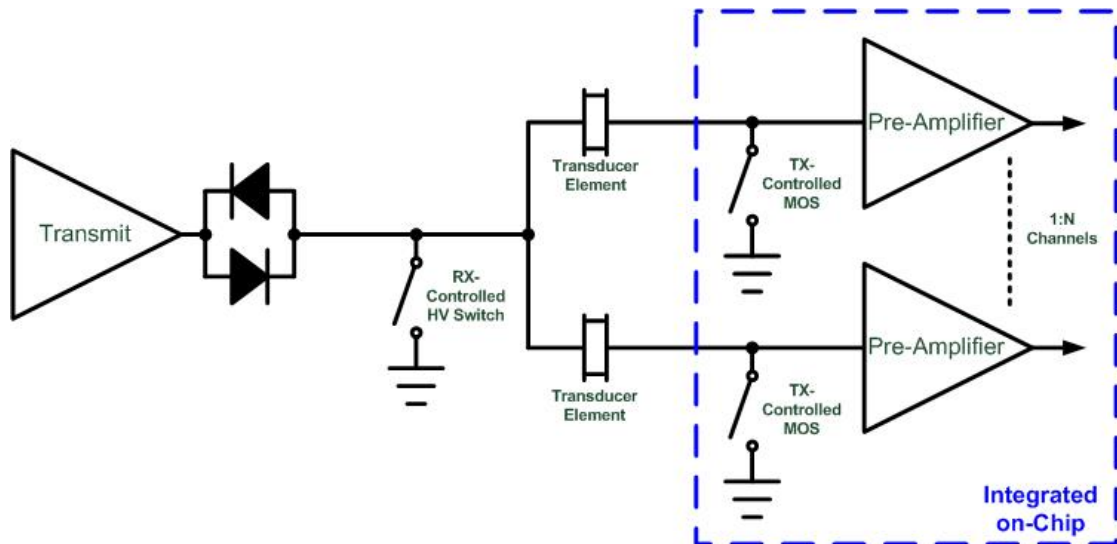


Figure 3. 6 on-chip TX-controlled MOSFET is used as the T/R switch.

Another solution to the T/R switch is the MOSFET switch. In [46], the MOSFET with control circuit is used as the switch between transmitter and pre-amplifier, shown in Figure 3.6. Compared to the diode bridge switch, the off-state MOSFET switch has lower leakage current and hence the lower power consumption, but the existence of control circuit increases the design complexity.

### **3.2.4 Pre-Amplifier**

The pre-amplifier in the receiving signal chain of an ultrasonic imaging system should meet some requirements: low-noise, to minimize the interferences for the received ultrasonic echoes, wide bandwidth from 10MHz to 40MHz, to meet the ultrasonic wave frequency range, and the input impedance close to transducer equivalent impedance, to bypass cable capacitance induced loss and work as an impedance converter between the transducer and beamforming stage [47] .

#### **3.2.4.1 Low-Noise Amplifier**

Low-noise amplifier (LNA) is a widely-used pre-amplifier in the front-end of ultrasonic imaging system. In [48], a high-frequency ultrasonic signal amplifier array composed by the two-stage low noise amplifier units is reported. The first stage provides most of the gain and the second stage aims to supply enough current and high output swing. Another case of the two-stage low noise amplifier for ultrasonic front end signal processing is presented in [49]. That LNA topology is a two stage open loop configuration. The first stage is a transconductance stage which is used to convert the input small signal voltage to current. Then the second stage, a current mirror, will drive a resistive load.

### 3.2.4.2 Charge Sampling Amplifier and Transimpedance Amplifier for cMUT

Charge sampling amplifier (CSA), based on the capacitive feedback charge amplifier, is often employed as the analog front-end for cMUTs in medical ultrasonic imaging systems. In [50], a time-control charge sampling amplifier is reported. As shown in the Figure 3.7 (a), the CSA circuit contains two switches,  $S_1$  and  $S_2$ , which are controlled by outside clock timing logic  $\phi_1$  and  $\phi_2$ .  $A(s)$  is the transfer function of the operational amplifier. The input current  $i_{in}$  is integrated on  $C_f$  to provide an output voltage that is proportional to the integral of the input current.

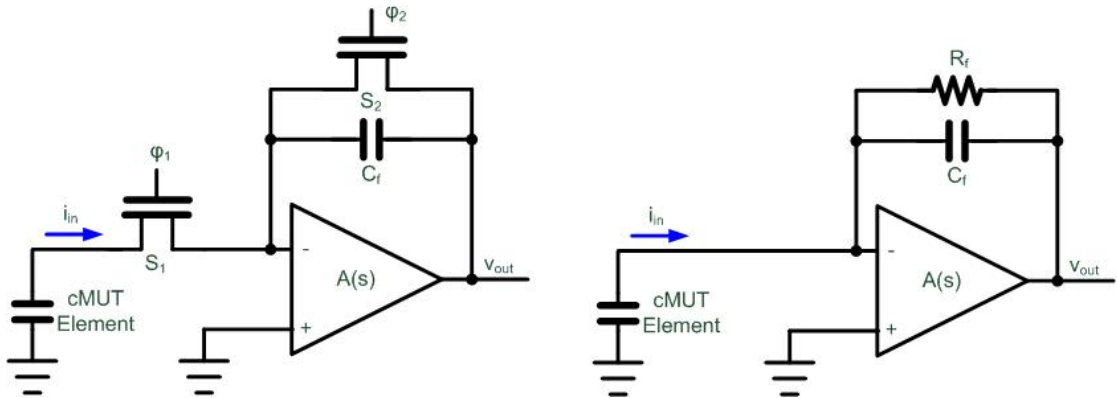


Figure 3. 7 (a) a CSA with two control switches (b) a simple TIA for cMUT.

In [51], a 1V transimpedance amplifier (TIA) is designed in a 90nm CMOS technology to be an analog front-end for cMUTs for medical ultrasonic imaging, as shown in Figure 3.7 (b).

### 3.2.5 Time-Gain Compensation

The energy of acoustic wave will diminish exponentially when the wave propagates through the human body or tissues. In [52], it reports that the output from a 20dB pre-amplifier and a band-pass filter in a medical diagnostic ultrasonic imaging system will vary from 10pV to 1V peak-to-peak, equal to 100dB dynamic range. Up to 60dB of this variation is caused by the attenuation of the ultrasonic signal propagating through human body. To better reveal the properties of the tissues, thus, the received echo signals by transducer should pass through the time-gain compensator (or time-gain controller, TGC) to compensate this exponential energy attenuation before they are input to the pre-amplifier. In addition, the TGC is also necessary to compress the received signal dynamic range, which is usually too large to be processed by the following analog/digital convertor and presented by the display equipments. Sometimes an additional logarithmic amplifier is even necessary to further compress the signal dynamic range.

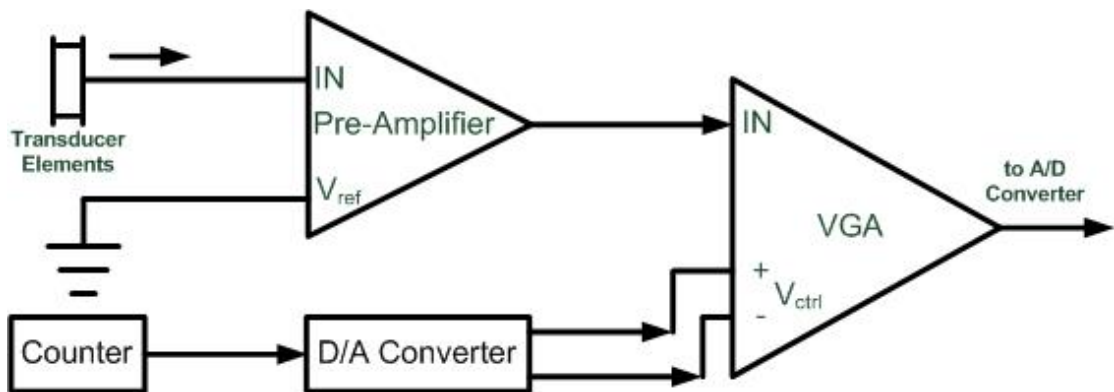


Figure 3. 8 VGA for TGC and its off-chip pseudo-exponential control signal.

The general time-gain compensator design is based on the variable gain amplifier (VGA) with a time-gain function control signal. This control signal could either be a time-gain function signal, which is automatically and adaptively modified by a digital signal processor (DSP) compensation loop [52], or a pseudo-exponential control signal, which is generated from external circuitry with a FPGA chip and a D/A convertor [53], as shown in Figure 3.8.

### **3.2.6 Analog/Digital Converter**

The analog/digital convertor (ADC) is used to convert the compensated analog signal to digital signal for the display processing back-end. Oversampling to the input signal is often necessary, to reduce the design complexity of following digital processing and filtering. The sampling frequency is usually set to 30 ~ 60MHz, corresponding to the typical biomedical ultrasonic frequency. Typical systems quantize to 12 bits accuracy. Different structures of ADC are employed based on different imaging system specifications and requirements. For example, a parallel-pipelined ADC is adopted [54], while a threshold inverter quantizer (TIQ) ADC unit is used [55]. Moreover, the single-bit or double-bit sigma-delta ADC is used as the basic unit, reported in [56-58]. There is a trade-off between ADC bit depth and TGC gain compensation range. Increasing the bit number of ADC will ask for smaller gain compensation ranges in TGC and hence a reduction in the TGC design complexity.

### **3.3 Ultrasonic Imager-on-Chip and Reliability Issues**

#### **3.3.1 Need for Ultrasonic Imaging System Integration**

On the one hand, system Integration will bring many advantages. First, the integration will reduce product size and power consumption when the whole system is integrated on a single chip, which will extend the battery lifetime for portable applications. Second, the integration can facilitate the communications between different modules in the system, and reduce interference and parasitic effects from outside discrete components and routing wires on PCB. Third, with many cells and function modules being integrated into a single chip, less welding work is needed, not only reducing the cost of assembling and manufacturing, but also improving the reliability of the whole system. Fourth, the system integration will save the software and hardware calibration and adjustment time and reduce cost, too. Finally, by integration, each function module in the system could be optimized with the other units, and thus the maximal performance of the whole system can be achieved.

On the other hand, many demanding applications need the integrated ultrasound imaging system, which could provide real-time scanning anywhere. For example, field emergency medical service (EMS) teams will have quicker access to a patient and will be able to send results to hospital before they arrive at the emergency room (ER). The doctors in hospital could analysis the results sent by the EMS team and then provide

in-time treatment to the patient. In addition, increased portability offers opportunities to use these devices to provide a better grade of medical service in remote areas and villages short of reliable electrical power.

So far, several solutions or prototypes for the portable ultrasonic imaging system have been developed [59-61]. The function modules in those systems, such as HV pulser, T/R switch and front-end signal process chain, are placed together on a PCB and connected to the separated transducer array, forming ultrasonic imaging systems. Obviously, they are still not the high-degree integrated system on a single chip and hence have the disadvantages of large size, high power consumption, high cost and low reliability. In [55], an ultrasonic imaging transceiver chip with receiving front-end and transmit beam-former is proposed. However, the main transmitting units, HV pulser and transducer array, are still off the transceiver chip and connected to the transceiver by a PCB.

### **3.3.2 Ultrasonic Imager-on-Chip System Design**

Ultrasonic imager-on-chip (UIC), a new concept of the ultrasonic imaging system with all function modules being integrated onto a single chip, is proposed. All the function units in ultrasonic imaging system, including transducer, T/R switch, HV pulser, pre-amplifier, time-gain compensator and A/D converter, should be integrated into a chip to build reliable, low-cost and high-performance ultrasonic imaging system.

Among all the different function modules in the UIC system, it could be easily concluded that the transducer and the HV pulser are the bottlenecks of UIC system integration, because all the other function circuit blocks in UIC system have been studied for many years and their mature solutions have been available in common low-voltage (LV) IC processes except two of them, seen from the review above.

For the ultrasonic transducer, suitable piezoelectric materials and compatible manufacturing process need to be developed, to make the transducer array available on silicon wafer and match the other function units in UIC system. On the other hand, HV pulser is usually fabricated in HV technology or HV-compatible LV technology, completely incompatible with the other function circuits in UIC system most of which are produced in LV CMOS technology. That will increase the cost of manufacturing and reduce the system reliability of the UIC. To solve the problem, HV pulser should be fabricated in LV CMOS technology, too.

### **3.3.3 UIC System Reliability**

Considering the application conditions and environments listed above, the UIC system should be high-reliable, with complete ESD protection strategy against possible ESD damages, small-size, with high integration degree for the whole system, and power-efficient, with low-power signal transmitting and receiving circuits inside.



Apparently, reliability may be the most important concern for the UIC design because of its life threatening nature, particularly for implantable and portable applications. Because of its nature, UIC system requires robust ESD protection. Several unique ESD design challenges must be concerned for UIC system. First, relatively higher ESD protection required for many remote and mobile UIC applications means higher ESD-induced parasitic effects. This requires careful ESD design optimization to minimize those ESD-induced parasitic in order to maintain IC performance, which means traditional ESD devices may not be utilized because of their severe parasitics. Second, UIC system often involves multiple supply domains, from low to high voltages. That means the ESD design window becomes very complicated for the whole UIC system. Therefore, ESD designs must be customized for each block, which requires different ESD structures with different ESD-critical parameters. Third, accurate UIC performance requires careful ESD-circuit co-design to ensure whole chip/system performance with robust ESD protection. Fourth, the fully integrated ultrasound system requires all on-chip ESD protection, not off-chip ESD protection. These factors must be addressed in UIC design to ensure both system performance and reliability.

## **Chapter 4 HV Pulser Design in LV Technology**

### **4.1 HV Pulser Realization in LV CMOS Technology**

#### **4.1.1 Requirements for HV Design in LV CMOS Technology**

As stated above, UIC system has high degree of integration requirement, and the realization of HV pulser in LV processes is a key to the solution. To design a HV pulser in LV CMOS technology, several requirements must be fulfilled.

First, a circuit topology of stacked devices has to be adopted. It is because that LV device cannot stand the high voltage that the HV pulser needs, unless the LV devices are stacked one by one to make the high voltage being distributed uniformly in each LV device. Second, this topology of stacked devices needs to be expandable to higher N-stage stacks, or “N-stage-scalable”. For different transducers or different application environments, HV pulser may need different HV output voltages, varying from scores of volts to several hundred of volts. If the topology of stacked devices is not N-stage-scalable, the cost on the design of each specific HV pulser for different HV outputs will increase intolerably. Third, for a HV pulser which will work in at least four stages: output "LOW", output "HIGH", output "LOW" to "HIGH" and output "HIGH" to "LOW", the LV devices used in it should be always kept in their LV safe operation regions for all those four stages.

Last but not least, the chosen LV CMOS technology itself has to be able to stand the high voltage of HV pulser. That means the bulk CMOS technology cannot be employed because the HV pulser highest output voltage, higher than scores of volts, could easily exceed the breakdown voltages of parasitic P-N junctions between drain/source and wells, or between wells and bulks of most bulk CMOS technologies, usually lower than 20V, causing stacked devices breakdown and malfunction. In other word, the silicon-on-insulator (SOI) CMOS technology, in which all active devices are isolated from one another by the buried oxide layer and STI oxide, leading to completely-isolated wells and substrate, seems to be an ideal option for HV pulser design in LV CMOS technology, as shown in Figure 4.1. It is necessary to point out that the limitation of HV pulser highest voltage now will become the breakdown voltage of the buried oxide layer or the capacitor dielectric of the SOI CMOS technology.

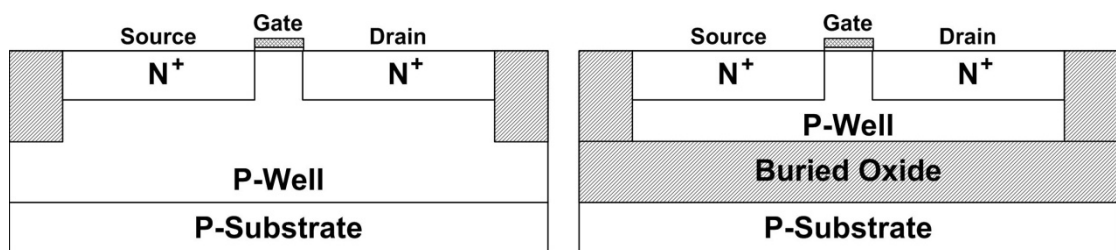


Figure 4. 1 X-sections of (a) Bulk CMOS and (b) SOI CMOS.

## 4.1.2 Possible Candidates of HV Pulser Designs

### 4.1.2.1 Charge Pump and Level Shifter

Charge pump (or “Dickson charge pump”), first proposed by Dickson in 1976, is a widely-used method to generate HV output by stacked LV devices in LV IC technologies [63-65]. It uses capacitor and diode (or MOS transistor) stacking network with two non-interleaving controlling clock signals to generate high voltage, as shown in Figure 4.2. Although it is N-stage-scalable, the Dickson charge pump can only provide DC high voltages and usually be used as a high voltage power supply generation circuit in LV technology. Thus it cannot be adopted to create HV waveforms consisting of fast transient low and high pulses that transducer needs.

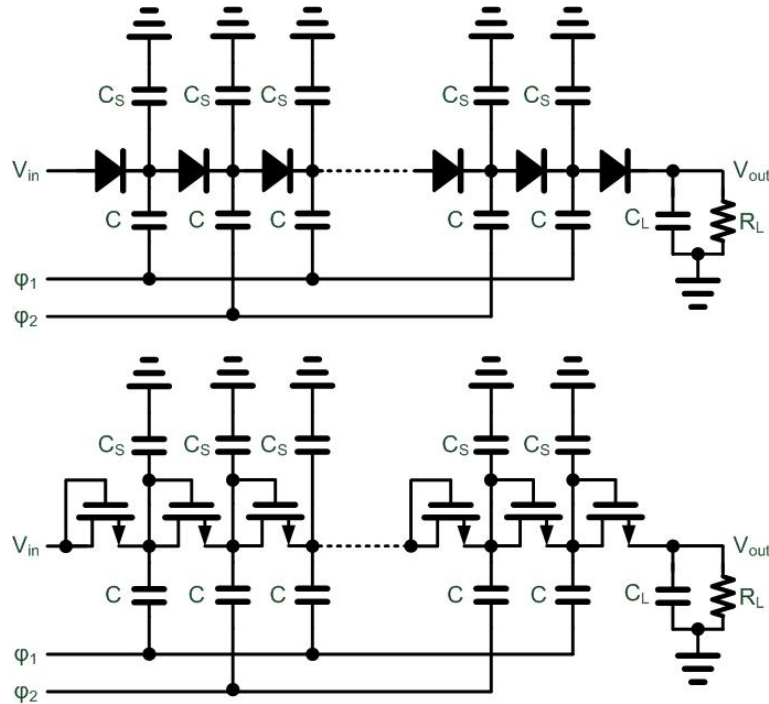


Figure 4. 2 Dickson charge pump: (a) diode and capacitor (b) MOS and capacitor.

Level shifter is another way to realize HV output voltage in LV process. A lot of level shifters with different output voltages have been reported in various applications [66-71]. However, level shifter is often used to produce HV control signals for HV transistors in HV-compatible LV technologies. In addition, most of level shifter structures are specially designed for certain type of application and they are not N-stage-scalable at all. Moreover, the output voltage of the level shifter is much lower than the values that ultrasonic transducer asks for. All those factors above rule out the possibility of level shifter's application in HV pulser design for UIC system.

#### **4.1.2.2 PMOS-Biasing N-Stage Stacked LV NMOS HV Pulser**

As stated above, a key to the design of HV pulser in LV technology is always keeping the stacked LV devices (mainly MOS transistors) within safe operation region. To realize this, appropriate biasing circuit unit is essential to each stacked LV MOS. When the HV pulser circuit output voltage is "LOW", the biasing circuit should turn on all the LV MOS devices quickly. When the circuit output voltage is "HIGH", the biasing circuit should turn off the stacked LV MOS transistors and the output high voltage should be almost equally distributed on each LV MOS transistors.

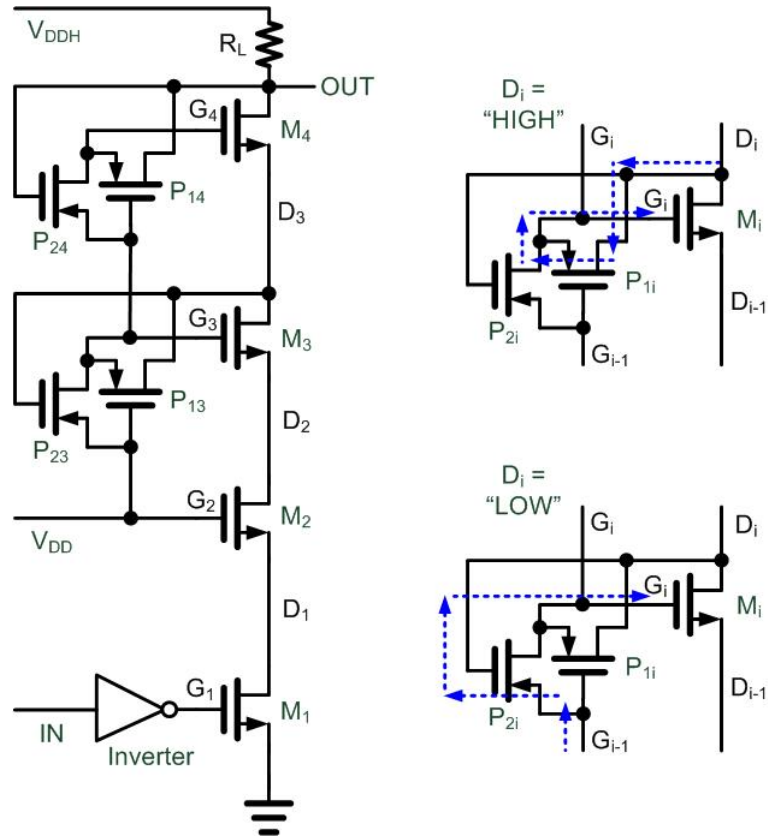


Figure 4. 3 The schematic of HV pulser circuit with PMOS-biasing LV NMOS: 4-stage.

Figure 4.3 presents a stacked HV pulser circuit with PMOS biasing circuit for higher stage stacked LV MOS transistors [72]. The mechanism of the PMOS biasing circuit is as following: when the input node “IN” is “LOW” ( $IN=0V$ ), all four MOS transistors are turned on and the biasing voltage  $V_{DD}$  at  $M_2$  gate  $G_2$  will pass through PMOS  $P_{23}$  and  $P_{24}$  to bias the  $M_3$  and  $M_4$  gates  $G_3$  and  $G_4$ , respectively. The  $V_{DD}$  is the normal operation supply voltage for LV MOS, so all the MOS transistors in the HV pulser are on and in safe operation region. At this moment, the output node “OUT” is “LOW”, too. When the input node “IN” is “HIGH” ( $IN=V_{DD}$ ), the bottom NMOS  $M_1$  and  $M_2$  will be turned off first, then the other MOS transistors will also be shut off. The

MOS  $M_3$  will be biased by PMOS  $P_{13}$  to “diode-connected” MOS with its drain and gate being tied together, while the MOS  $M_4$  will also be biased by PMOS  $P_{14}$  to “diode-connected” MOS. Now the output node “OUT” voltage is “HIGH”, almost equal to  $V_{DDH}$ . The high voltage at “OUT” node will be distributed among those stacked LV MOS transistors.

It is claimed by the author that as long as the circuit  $V_{DDH}$  is within the IC technology breakdown voltage limit, this circuit scheme can stack as many stages as possible for even higher voltage output. However, further investigation proved this PMOS-biasing HV pulser circuit scheme will have the problem of voltage overstress with increasing stage number and high voltage output.

Figure 4.4 shows the schematics of a PMOS-biasing HV pulser with 7-stage stacked LV MOS transistors in a 2.5V SOI CMOS technology. The HV DC power supply voltage  $V_{DDH}$  is set to 7.5V (Figure 4.4 (a)) and 10V (Figure 4.4 (b)), respectively. When the circuit input node “IN” is set to “HIGH”, all the LV MOS transistors will be off, with distributed high voltage on each of them. The voltage values at drain nodes of each MOS transistors from transient simulation are shown in Figure 4.4, too.

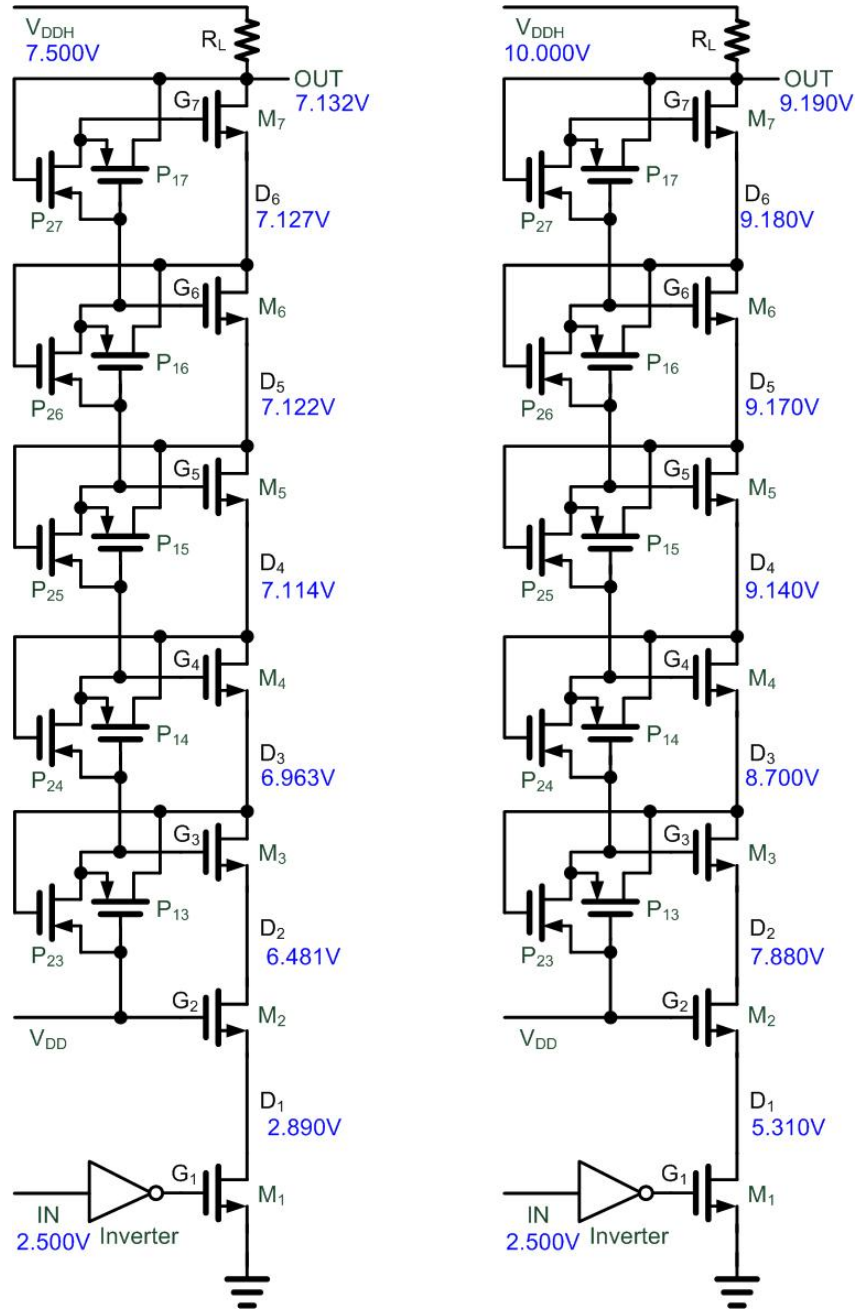


Figure 4. 4 A 7-stage PMOS-biasing HV pulser with different  $V_{DDH}$  power supplies.

The voltage values at nodes of the HV pulser circuits clear show that almost all the high voltage falls onto the MOS  $M_1$  and  $M_2$ , while MOS  $M_3$  to  $M_7$  only take small part of the high voltage stress. The reason is that the “diode-connected” MOS cannot shut off completely and hence cannot share much voltage drop on themselves. The



diode-connected MOS  $M_3$  to  $M_7$ , together with the lowest PMOS  $P_{11}$  and  $P_{21}$ , form a leakage current conducting path when all MOS transistors should have been completely off. Thus, when the HV DC supply voltage  $V_{DDH}$  increases, even though the stacked number of LV MOS transistors can be increased accordingly, the MOS  $M_1$  and  $M_2$  will still face the voltage overstress problem. In other word, this circuit cannot be used to pursue HV pulser with very high voltage output.

#### 4.1.2.3 RC-Biasing N-Stage Stacked LV NMOS HV Pulser

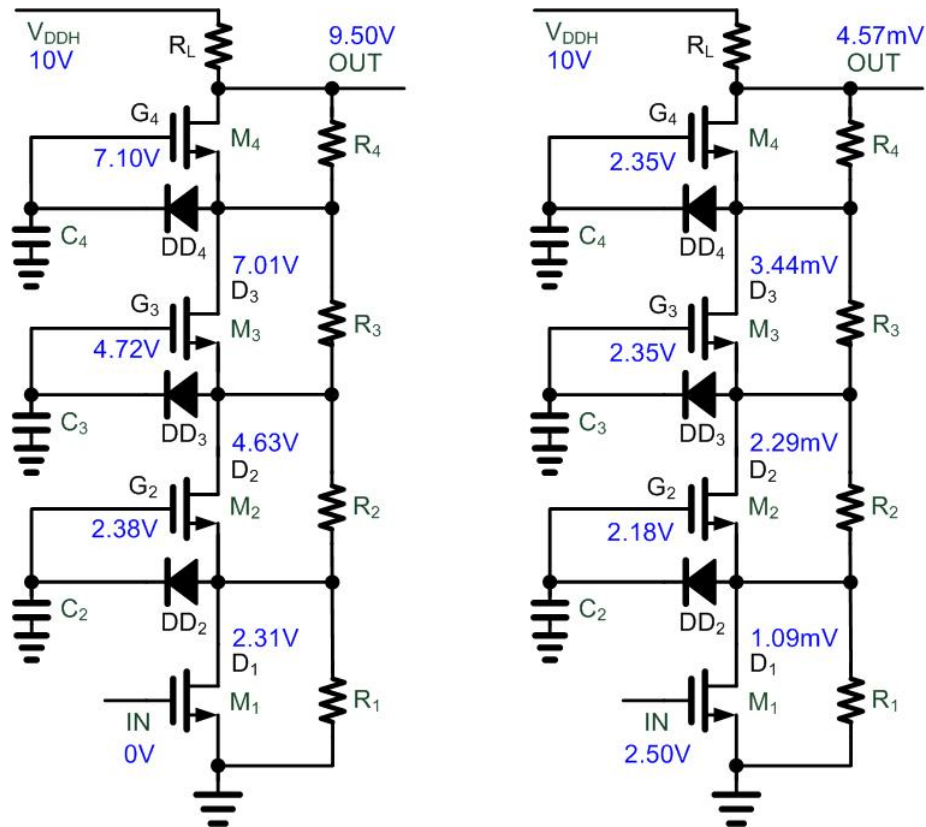


Figure 4. 5 RC-biasing 4-stage stacked LV NMOS HV pulser: (a) IN = "LOW" (b) IN = "HIGH".

Figure 4.5 depicts the schematic of another type of HV pulser with N-stage RC-biasing stacked LV NMOS transistors [73]. Here N is equal to 4. For each LV NMOS stage except the 1<sup>st</sup> one, it contains a biasing circuit composed of a capacitor ( $C_i$ ), a diode ( $DD_i$ ) and a resistor ( $R_i$ ).

The working mechanism of the RC-biasing circuit is as following: the high voltage supply  $V_{DDH}$  is set to N times of the normal operation power supply voltage for LV NMOS, or  $V_{DD}$ . The load resistor is  $R_L$ , whose resistance is usually set to be much smaller than that of the biasing resistor  $R_i$ . When the input node "IN" is set to "LOW", all the stacked LV NMOS are in off status and output node "OUT" will be "HIGH". The N (=4) large biasing resistors,  $R_1$  to  $R_4$ , with the same resistance, will equally divide the "OUT" node voltage  $V_{DDH}$  into  $V_{DDH} / N$ , also equal to  $V_{DD}$ , between each LV NMOS drain and source nodes. The corresponding biasing diode  $DD_i$  now forward turns on, by which the biasing voltage generated by biasing resistors will bias the LV NMOS gate node and charge the capacitor  $C_i$  in the same time.

When the "IN" is set to "HIGH", all the stacked LV NMOS are in on status. The voltages at their drain and source nodes will rapidly fall to almost zero. In addition, the charge stored in the biasing capacitor  $C_i$  during LV NMOS off status will be re-distributed among a new capacitor network, composed by the biasing capacitor  $C_i$  itself, plus the reverse biasing diode parasitic capacitor  $C_{diode,i}$  and the MOS gate oxide capacitor  $C_{gate,i}$ . By selecting suitable capacitance for all the  $C_i$ , every LV NMOS

gate node will be biased to an appropriate value, normally LV normal power supply  $V_{DD}$ , and kept in the safe operation region in the whole process.

Initial circuit simulation proves that this type of RC-biasing stacked LV NMOS HV pulser circuit is an ideal option to realize the HV pulser design in LV SOI CMOS technology. The LV SOI technology used here is a 2.5V SOI CMOS technology. The initial HV pulser contains 4 stages. Circuit node voltages at different statuses are extracted from the initial HV pulser transient simulation, as presented in Figure 4.5: (a) for HV pulser whose "IN" is set to "LOW", while (b) for HV pulser whose "IN" is set to "HIGH". The transient simulation shows that the high voltage are almost equally distributed on each LV NMOS when the "OUT" is "HIGH", while all LV NMOS gates are biased close to 2.5V  $V_{DD}$  when the "OUT" is "LOW". Therefore, the LV NMOS in this stacked HV pulser are always in the device safe operation region ( $\leq V_{DD}$ ) and there is no overstress issue at all.

To achieve a suitable biasing voltage for the LV NMOS gate, the biasing capacitor  $C_i$  should be calculated based on the formula 4.1:

$$C_i = C_{p,i} \left( \frac{V_g}{(i-1) \cdot \left( \frac{V_{DDH}}{N} \right) - V_g} \right) \quad (4.1)$$

In this formula, "i" is the stage number.  $C_{p,i}$  is the total parasitic capacitance at LV NMOS gate node of the  $i^{\text{th}}$  stage, which is equal to the sum of reverse biasing diode parasitic capacitor  $C_{\text{diode},i}$  and the MOS gate oxide capacitor  $C_{\text{gate},i}$ .  $V_g$  is the expected

biasing voltage absolute value at gate node of the  $i^{\text{th}}$  stage LV NMOS when the “OUT” is “LOW”.  $N$  is the total stage number of HV pulser. It is noticed that with an increasing stage number  $i$ ,  $C_i$  value will be reduced accordingly, which means the size of high-stage stacked HV pulser is convergent. Compared with the extremely large  $C_1$  in first stage, the other biasing capacitor will take much less area in the HV pulser layout.

The HV pulser design needs to be considered thoroughly and all the cells in the circuit should be adjusted carefully, to make a good balance among many merits of figures. From the formula 4.1, it could also be concluded that  $C_i$  is decided by the value of  $C_{p,i}$ , or  $C_{\text{diode},i}$  and  $C_{\text{gate},i}$ , which means small size of NMOS or diode will ask for a small  $C_i$  in each stage and hence reduce the circuit layout size. However, besides working as a biasing instance, the diode also provides ESD protection for the LV NMOS gate oxide, while the LV NMOS size decides the HV pulser output power. Thus they cannot be too small. Moreover, the resistance ratio between  $R_L$  and total  $R_i$  will decide the “OUT” node “HIGH” voltage level, while the resistance ratio between the total series resistance of the  $N$ -stage “on” LV NMOS and  $R_L$  will determine the “OUT” node “LOW” voltage level.

The HV pulser with  $N$ -stage RC-biasing stacked LV NMOS transistors introduced in this section has several advantages, such as simple circuit architecture, overstress immunity and relatively high frequency, up to 20MHz. Therefore, it has been chosen to be the HV pulser core circuit in the next section. It needs to be pointed out that, due to

the existence of many large-size biasing capacitors and resistors, this HV pulser will take a lot of area in layout.

## **4.2 HV Pulser Design and ESD-Circuit Co-Design Methodology**

To verify the possibility of fabricating HV pulser in LV SOI CMOS technology, several HV pulser circuits are designed and simulated in IBM C507RF 0.18 $\mu$ m 2.5V SOI CMOS technology. Full-direction ESD protection strategy is considered in the HV pulser design, too. To predict and reduce the ESD-induced parasitic effect impact on HV pulser function, ESD-circuit co-design methodology is also used [74].

### **4.2.1 HV Pulser Core Circuit Design**

As mentioned above, the stage number is mainly restricted by the size of biasing cells and total available die space. Thus, a 4-stage HV pulser core circuit with RC-biasing stacked LV NMOS is designed in that IBM 2.5V SOI CMOS technology. Its HV power supply voltage  $V_{DDH}$  is set to 10V, equal to 4 times of normal power supply  $V_{DD}$  of this LV CMOS technology. All the property values of the devices used in the circuit, such as LV NMOS, biasing capacitors, diodes and resistors, are decided by careful and multiple circuit simulation. LV NMOS total width is set to 600 $\mu$ m, which not only shows relatively low resistance when it is turned on, creating low-enough output "LOW" voltage level, but also induce insignificant parasitic capacitance to the output

node, guaranteeing an output HV waveform frequency above 10MHz. Biasing diode total width is 100 $\mu$ m, enough to provide initial ESD protection to LV NMOS gate. Biasing capacitor  $C_1$  to  $C_4$  values are calculated from total parasitic capacitance of diode and LV NMOS, the designed gate biasing voltage  $V_g$  and the stage number. Considering that the HV pulser could be applied in future mobile medical UIC system, biasing resistor  $R_1$  to  $R_4$  are specially tuned to 3M $\Omega$ , together to limit the DC leakage current under 1 $\mu$ A and meantime prevent unnecessary leakage power consumption when all the LV NMOS transistors are in off status.

The HV pulser function transient simulation results are presented in Figure 4.6. With an input of 2.5V peak-to-peak voltage ( $V_{pp}$ ) and 10MHz square waveform, the HV pulser output is a 10MHz, 10V- $V_{pp}$  HV waveform, whose major SPECs are summarized in Table 4.1. The circuit leakage current obtained from DC simulation is less than 1 $\mu$ A when all LV NMOS transistors are in off status, as expected.

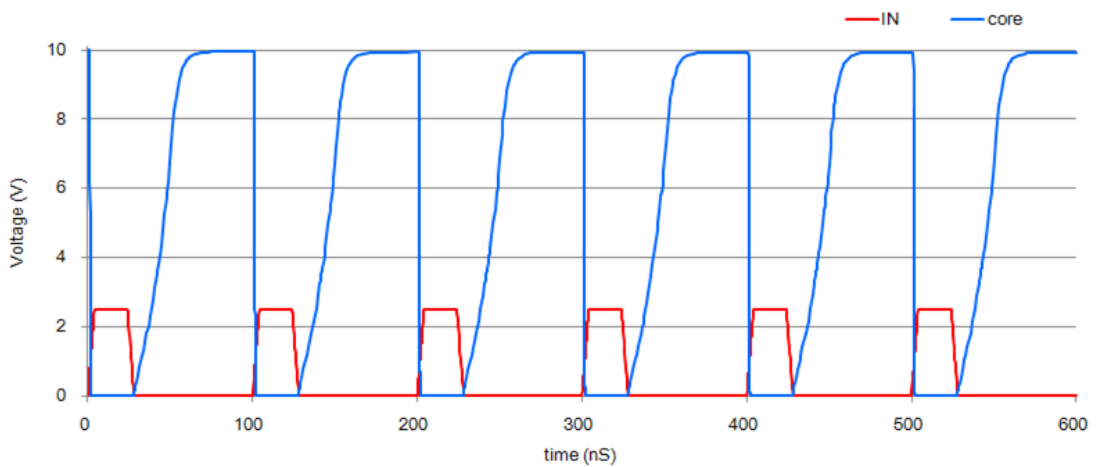


Figure 4. 6 The output waveform of a 4-stage HV pulser core circuit with RC-biasing LV NMOS.

Table 4. 1 HV pulser output waveform major properties: core circuit and circuit with ESD.

| HV pulser              | $I_{leak}$ (nA)<br>@ 10V | $V_{OUT}$ (V) |       |          | Pulse Speed (V/ $\mu$ S) |          | Range of<br>Freq.<br>(MHz) |
|------------------------|--------------------------|---------------|-------|----------|--------------------------|----------|----------------------------|
|                        |                          | Low           | High  | $V_{pp}$ | $t_r$                    | $t_f$    |                            |
| core                   | 859.33                   | 0.0046        | 9.946 | 9.941    | 348                      | 1.95E+04 | >35                        |
| core + ESD<br>Pad Ring | 888.68                   | 0.0053        | 9.885 | 9.880    | 219                      | 1.72E+04 | >23                        |

Figure 4.7 shows the layout of this HV pulser core circuit. As expected, the biasing capacitors,  $C_1$  to  $C_4$ , and biasing resistors,  $R_1$  to  $R_4$ , take the most area in the layout. The four PADs, IN, OUT,  $V_{SS}$  and  $V_{DDH}$ , occupy a large layout area, too. There is no ESD protection in this HV pulser core circuit.

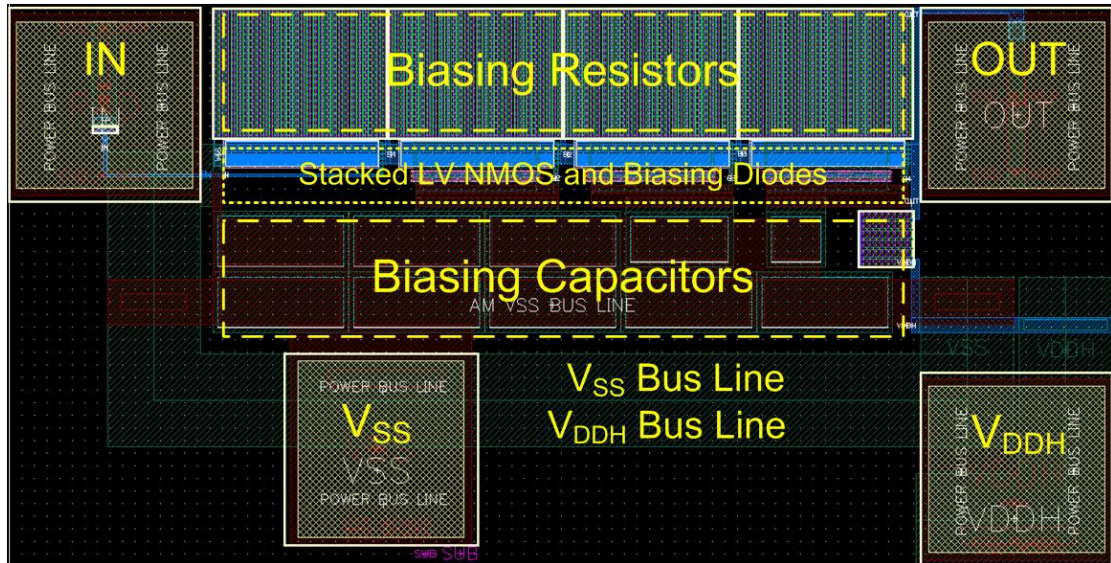


Figure 4. 7 Layout of a 4-stage HV pulser core circuit with RC-biasing LV NMOS.

## 4.2.2 Full-Direction ESD Protection and ESD-Circuit Co-Design

### 4.2.2.1 Full-Direction ESD Protection Scheme for HV Pulser

The full-direction ESD protection strategy is applied to the HV pulser core circuit, to provide robust ESD protection between any two ports of the HV pulser. The aimed ESD protection level for the whole circuit is HBM 2kV, enough for common portable electronic applications. As shown in Figure 4.8, there are four ports in this circuit: IN, OUT,  $V_{DDH}$  and  $V_{SS}$ . Two power domains exist in this HV pulser circuit: LV 2.5V domain and HV 10V domain. They share a common ground net  $V_{SS}$ . In both power domains, the “diodes at I/O ports plus ESD power clamp protection scheme” are applied. "ESD Design Window" rule still needs to be fit, even for multiple power domains.

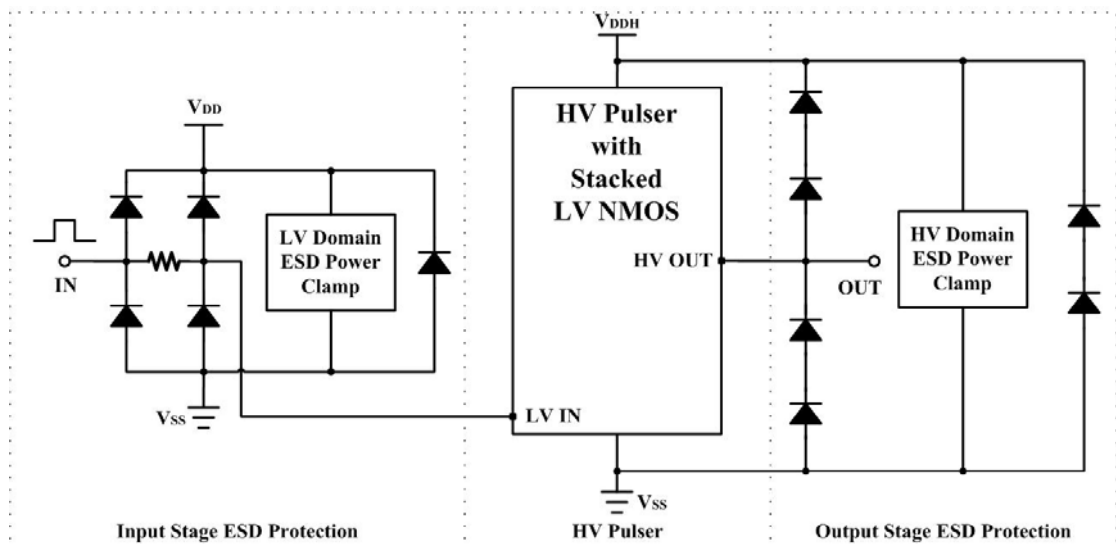


Figure 4. 8 A 4-stage HV pulser with full-direction ESD protection scheme.



At the input port “IN” of LV 2.5V domain, an input ESD protection network with two primary diodes, an input resistor and two secondary diodes is added. The power clamps used in LV domain is RC-triggering inverter-driven NMOS transistors, which will be triggered by the RC-inverter network during ESD transient, to shunt ESD current and clamp ESD voltage through large NMOS normal turn on [75]. Since there is no snapback behavior during the whole ESD event, this RC-inverter -driven power clamp can be simulated in SPICE. In addition, the IBM 2.5V SOI CMOS technology provides ESD protection diode behavior models under fast and high ESD current. Therefore, HBM simulation can be run in SPICE, to accurately predict the ESD protection performance in LV domain.

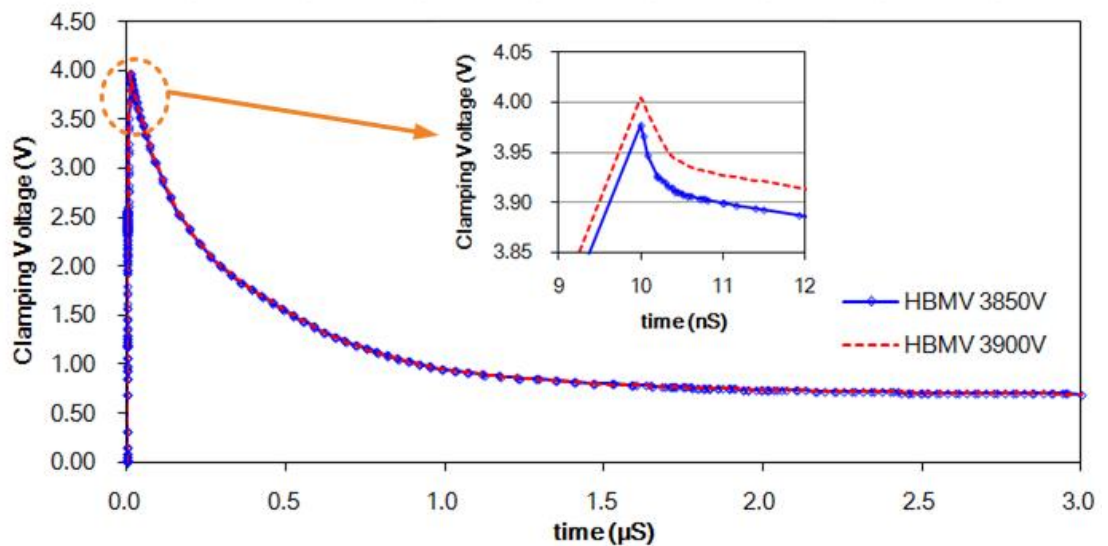


Figure 4. 9 Simulated time-voltage curve of positive HBM ESD from “IN” to “VSS” in HV pulser.

Figure 4.9 presents the time-voltage curve from positive HBM transient simulation from port “IN” to port “V<sub>SS</sub>”. As discussed in Chapter 1, this path is the most vulnerable ESD path for the “I/O diodes plus power clamp ESD protection scheme”. The NMOS gate safe operation voltage limit is 4V for this 2.5V SOI CMOS technology. It can be observed from Figure 4.9 that the ESD protection circuit manages to clamp the gate voltage below 4V even for a 3850V HBM ESD transient pulse.

At the output port “OUT” and “V<sub>DDH</sub>” of HV 10V domain, ESD protection stacked diodes are employed. The reverse breakdown voltage of two stacked diodes is 16V, high enough to keep stacked diodes off for 10V HV power supply. Three two-stacked ESD protection diodes are placed between V<sub>SS</sub> and OUT ports, OUT and V<sub>DDH</sub> ports, and V<sub>SS</sub> and V<sub>DDH</sub> ports, respectively.

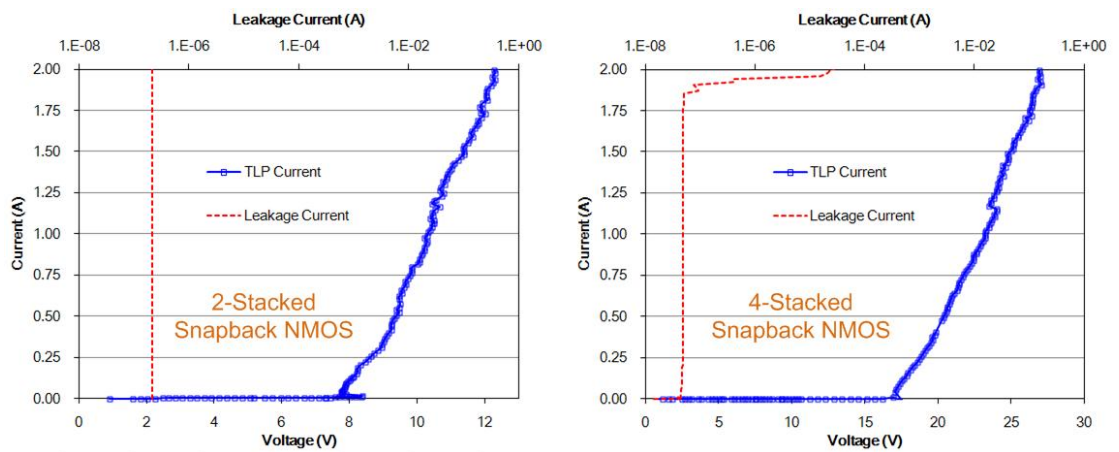


Figure 4. 10 Snapback I-V curves of (a) a 2-stacked snapback NMOS structure and (b) a 4-stacked snapback NMOS structure from TLP testing.

Table 4. 2 HV pulser ESD protection structure SPECS.

| Structure Type                     | Domain and Location | Dimensions                                                                                       | HBM ESDV (V) |
|------------------------------------|---------------------|--------------------------------------------------------------------------------------------------|--------------|
| Clamp Diode                        | LV $V_{DD}/V_{SS}$  | Perimeter=525 $\mu$ m;                                                                           | >4.00kV      |
| RC-Inverter-Driven NMOS Clamp      | LV $V_{DD}/V_{SS}$  | Total Width=2.312mm for 1 NMOS;                                                                  | >3.85kV      |
| Input Primary and Secondary Diodes | LV IN               | Primary: Perimeter=513 $\mu$ m;<br>Secondary: Perimeter = 60 $\mu$ m;<br>$R_{in}$ =50 $\Omega$ ; | >4.00kV      |
| Clamp 2-Stacked Diode              | HV $V_{DDH}/V_{SS}$ | Perimeter=875 $\mu$ m for 1 diode;                                                               | >4.00kV      |
| 4-Stacked Snapback NMOS            | HV $V_{DDH}/V_{SS}$ | Total Width=480 $\mu$ m for 1 NMOS;                                                              | >2.50kV      |
| 2-Stacked Diodes                   | HV OUT              | Perimeter=1mm for 1 diode;                                                                       | >4.00kV      |

Because there is no mature HV ESD protection structures available in this LV process, a 4-stacked snapback-NMOS structure (ggNMOS) are used as the power clamp in the HV power domain. As stated above, the snapback behavior cannot be simulated in SPICE. Figure 4.10 shows two snapback I-V curves of a 2-stacked snapback-NMOS structure (Figure 4.10 (a)) and a 4-stacked snapback NMOS structure (Figure 4.10 (b)) from TLP testing. Those TLP testing results not only prove

that the stacked snapback NMOS can successfully turn on during ESD transients and fit the ESD design window of HV domain, but also certify that they could provide at least 2500V HBM ESD protection, high enough for the aimed ESD protection level HBM 2kV. The main specifications of all the ESD protection structures used in the HV pulser are summarized in Table 4.2.

#### **4.2.2.2 ESD-Circuit Co-Design and HV Pulser Performance Recovery**

As stated above, full-direction ESD protection requires many ESD protection structures, which will definitely induce heavy ESD parasitics, such as  $C_{ESD}$ ,  $R_{ESD}$ , leakage and noise, into the core circuit and hence interfere the circuit original performance, probably causing problems like RC delay and impedance mismatching, etc. However, ESD-induced negative influences on the IC performance cannot be accurately estimated, evaluated and fixed unless the designed IC is produced and its complete performance characterization is done. This traditional "test and error" ESD protection design methodology will waste time and increase cost. Therefore, the ESD-circuit co-design methodology is developed to efficiently solve this ESD-related circuit performance degradation, which has been applied in this HV pulser design.

The proposed co-design method is as following: after the HV pulser core circuit design and full-direction ESD protection scheme implementation are completed, additional simulation will be done to evaluate the ESD protection structure impact on

the HV pulser core circuit performance. In other word, all the parasitics from ESD protection structures used in HV pulser circuit will be extracted and added into the HV pulser circuit simulation, to predict the circuit performance. Any performance degradation caused by ESD protection structures has to be recovered through careful ESD-circuit co-design, to completely eliminate possible ESD-induced negative effect to the HV pulser core circuit.

The ESD protection device parasitics used in the co-design could come from either ESD protection structure characterization, usually extracted through S-parameter and noise figure testing results of ESD test patterns, or directly from device parasitic models provided by the IC foundry. In IBM CSOI7RF 2.5V SOI CMOS technology, ESD protection device models already contain the necessary parasitics, which have been used in ESD-circuit co-design for the HV pulser circuit in this work.

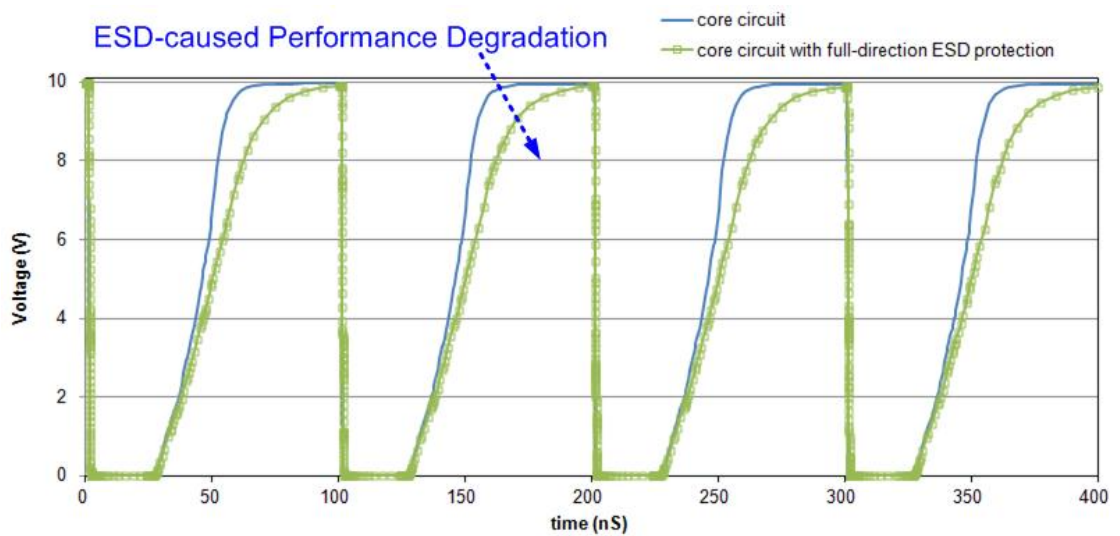


Figure 4. 11 Output waveforms of HV pulser core circuit and circuit with ESD protection.

HV pulser circuit performance degradation, caused by the additional full-direction ESD protection, has been observed in the simulation, as shown in Figure 4.11. Compared with that of HV pulser core circuit, the output waveform of HV pulser with ESD protection has a 37% degradation on rise time  $t_r$  and a 12% degradation on fall time  $t_f$ , causing the HV pulser maximum frequency drops from 35.7MHz to 23.8MHz, as shown in Table 4.1. The output HV  $V_{pp}$  is reduced a little bit, too. The main reason for this degradation is the stacked diodes at the “OUT” port increase the total capacitance at the port. Compared with the output waveform fall time  $t_f$ , the rise time  $t_r$  is less than 1/50 of  $t_f$ , making  $t_r$  the major factor that restricts the HV pulser output waveform frequency. Thus, the following HV pulser waveform recovery will mainly focus on the rise time  $t_r$  recovery.

The rise time  $t_r$  is mainly decided by the RC time constant at port "OUT". On the one hand, the load resistor  $R_L$  and biasing resistors  $R_1$  to  $R_4$  are connected in parallel to form the total resistance at "OUT" port. Because the  $R_L$  resistance is much less than that of the four biasing resistors in series, the final resistance will be close to the resistance value of  $R_L$ . On the other hand, the stacked LV NMOS transistors and ESD stacked diodes together provide the total capacitance at the "OUT" port. Obviously, among those cells that affect the RC time constant at the "OUT" port, tuning the  $R_L$  will be the easiest way to rebuild the HV output waveform rise time  $t_r$ .

Figure 4.12 shows the output waveforms of three different HV pulsers: core circuit, circuit with full-direction ESD protection and circuit by ESD-circuit co-design. It can be seen that the output waveform of the HV pulser by ESD-circuit co-design rises fastest than the other two. In the last one, the loading resistor  $R_L$  is reduced from 13.3k $\Omega$  to 7.5 k $\Omega$ , leading to a lower RC time constant and a shorter rise time  $t_r$  of its output waveform. In this way of ESD-circuit co-design, the ESD-caused circuit performance degradation is not only predicted precisely, but also fixed successfully.

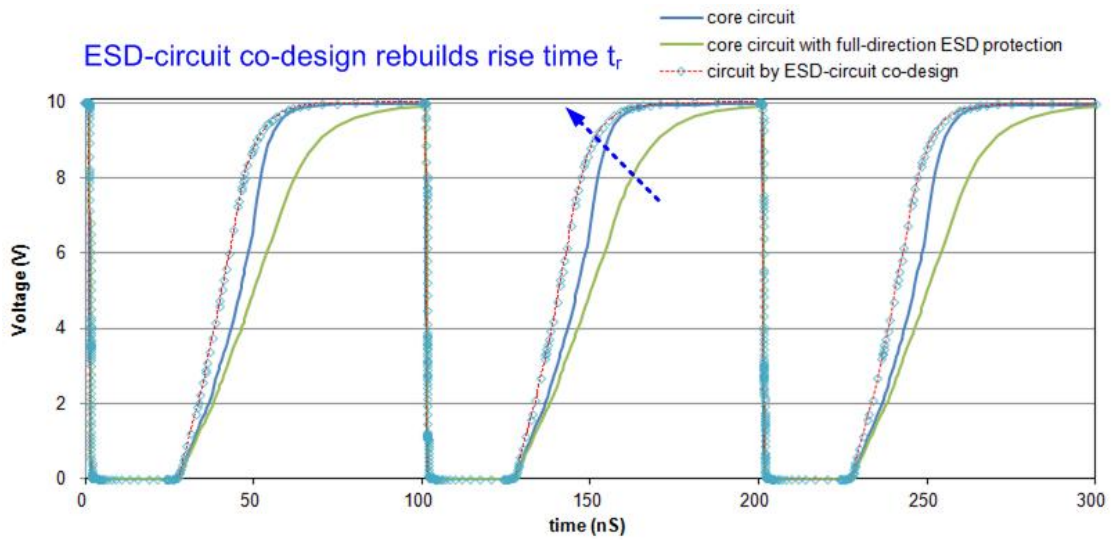


Figure 4. 12 Output waveforms of HV pulsers: core circuit, circuit with full-direction ESD protection and circuit by ESD-circuit co-design.

#### 4.2.2.3 Post-Layout Simulation and Final Designs

All those three types of HV pulsers mentioned above, original core circuit, core circuit with full-direction ESD protection and optimized circuit by ESD-circuit co-design,

are designed and drawn in the layout. The layouts of the two ESD-protected HV pulser splits are shown in Figure 4.13. As presented in Figure 4.13, all the ESD protection structures are placed under the PADs or power bus lines due to the technology called "circuit under pad" (CUP), which allows circuits being placed under the PADs and hence save circuit layout area. The CUP technology has been proved by numerous reliability tests and verifications. Compared with the layout of the original HV pulser core circuit, these two ESD-protected HV pulser splits occupy the same layout size,  $439.10 \times 221.76 \mu\text{m}^2$ .

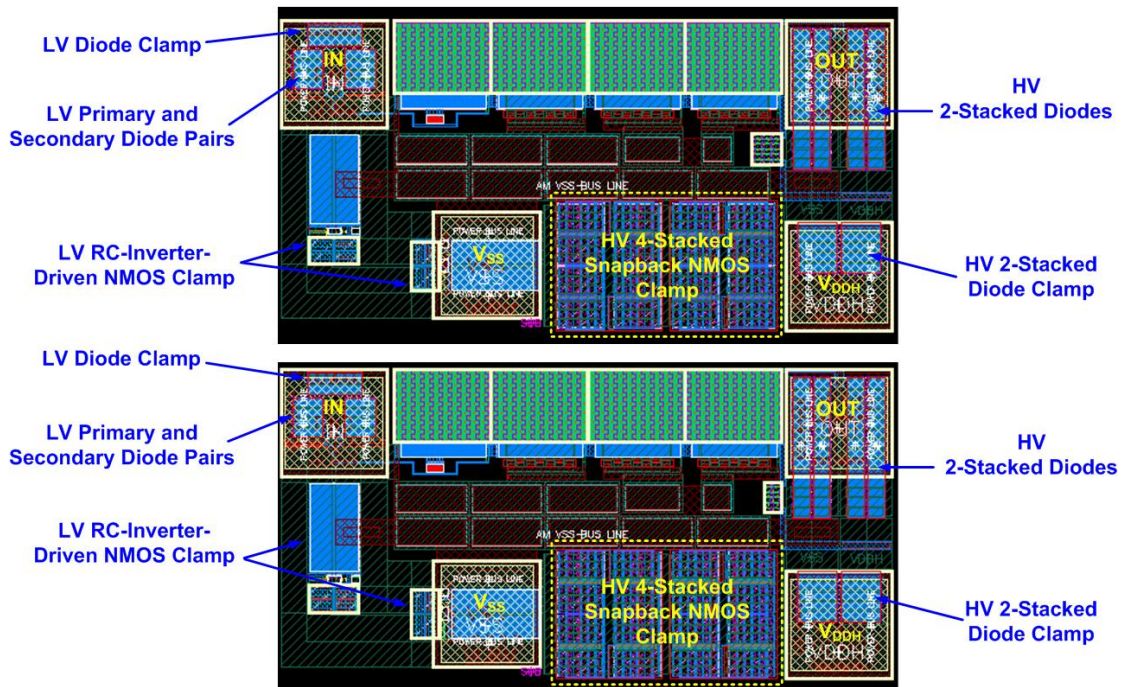


Figure 4. 13 The layouts of two ESD-protected HV pulser splits: (a) core circuit with full-direction ESD protection and (b) optimized circuit by ESD-circuit co-design.



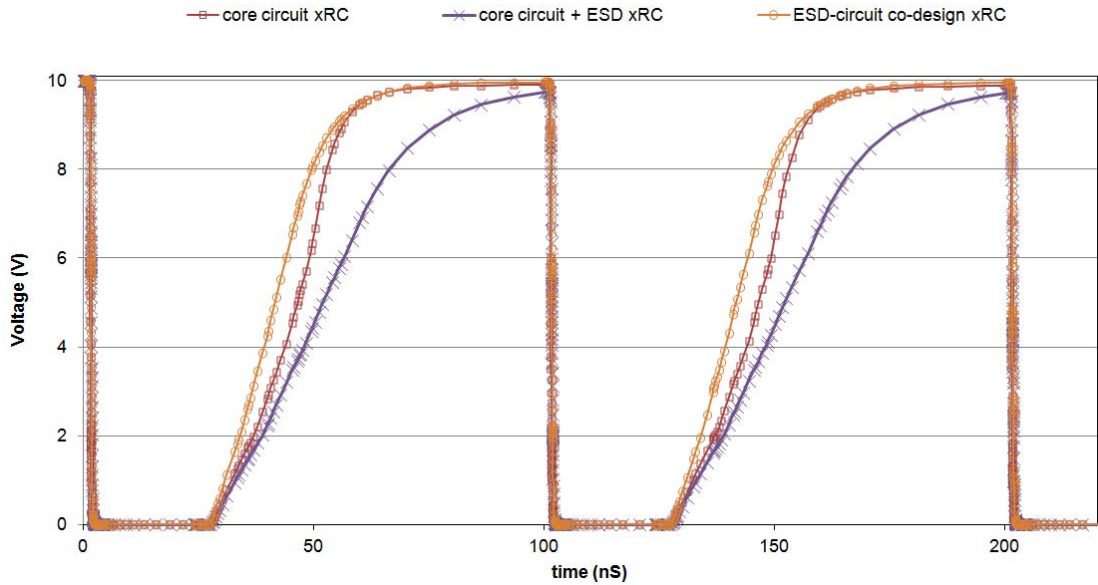


Figure 4. 14 Output waveforms of HV pulser splits: post-layout simulation.

All the layouts have passed design rule check (DRC) and layout V.S. schematic check (LVS). The post layout simulation of all three HV pulser splits were run with the layout parasitics extracted by Calibre xRC tool.

Figure 4.14 contains the waveforms of those three HV pulser splits from post-layout simulation. The critical data of HV pulser waveforms have been summarized in the Table 4.3, too. From the data above, it can be concluded that the HV pulser core circuit severe performance degradation on the critical parameter rise time  $t_r$ , caused by the additional full-direction ESD protection structures, has been fixed through ESD-circuit co-design method. In addition, compared to the ESD-protected circuit without co-design, the circuit with co-design has better fall time  $t_f$  but almost the same off-status leakage current at 10V. Figure 4.15 presents the final layout for three splits of HV pulser.

Table 4. 3 HV pulser split performance summary from schematic and post-layout simulation.

| HV pulser split                    | $I_{leak}$ (nA)<br>@ 10V | $V_{OUT}$ (V) |        | Pulse Speed        |                    | Range of Freq.<br>(MHz) |
|------------------------------------|--------------------------|---------------|--------|--------------------|--------------------|-------------------------|
|                                    |                          | Low           | High   | $T_r$ (V/ $\mu$ S) | $T_f$ (V/ $\mu$ S) |                         |
| core: schematic                    | 859.33                   | 4.64E-03      | 9.9455 | 348                | 1.95E+04           | >35                     |
| core: xRC                          | 854.99                   | 4.82E-03      | 9.8849 | 329                | 2.05E+04           |                         |
| core + ESD: schematic              | 888.68                   | 5.30E-03      | 9.885  | 219                | 1.72E+04           | >23                     |
| core + ESD: xRC                    | 872.24                   | 5.48E-03      | 9.7016 | 190                | 1.65E+04           |                         |
| core + ESD Co-Design:<br>schematic | 889.14                   | 9.49E-03      | 9.9814 | 388                | 1.77E+04           | >40                     |
| core + ESD Co-Design:<br>xRC       | 872.69                   | 9.78E-03      | 9.9469 | 333                | 1.67E+04           |                         |

### 4.3 Conclusion

A HV pulser for transducer in UIC system, consisting of RC-biasing stacked LV devices, is designed and fabricated in a 2.5V LV SOI CMOS technology. It has four stacked stages, full-direction ESD protection ability higher than HBM 2kV and 10V HV pulse output at the frequency of 20MHz or even higher. ESD-circuit co-design method is applied to predict the ESD-induced negative impacts on the HV pulser and recover its circuit performance. This design verifies the idea of integrating the transducer HV pulser together with the other UIC function units into a chip of LV technology.

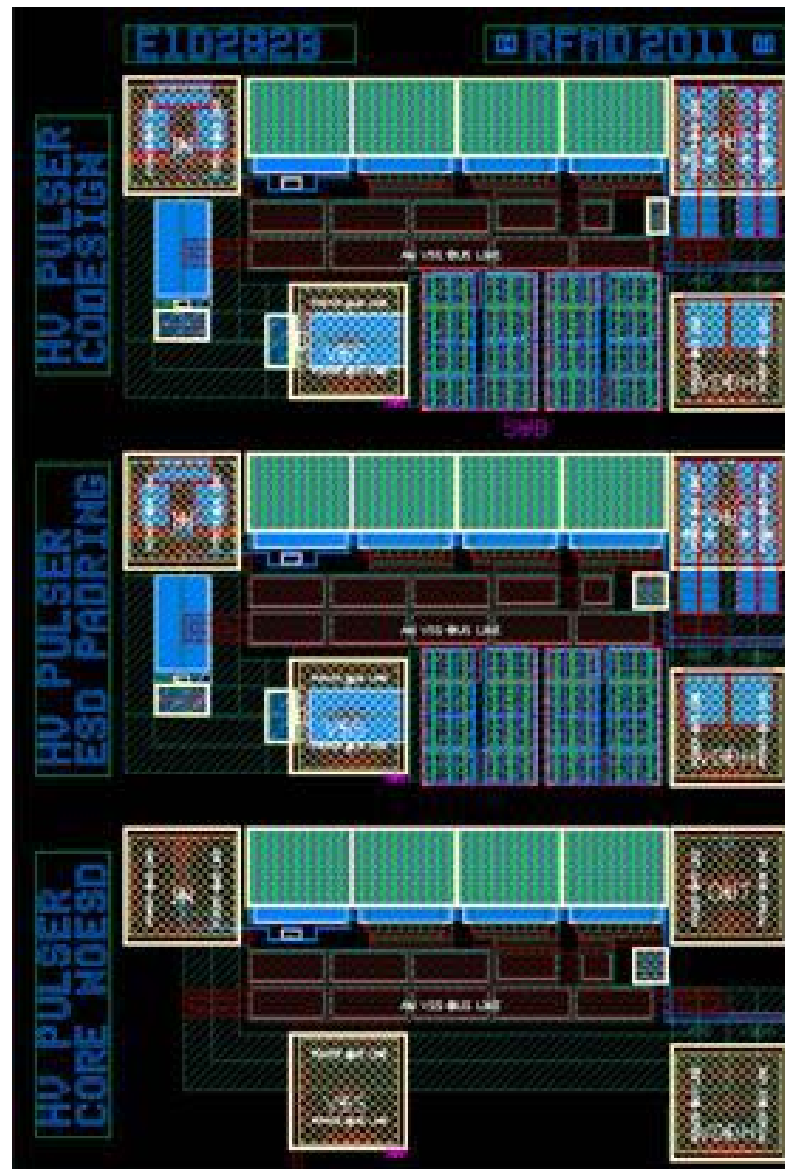


Figure 4. 15 Final layout for 3 splits of HV pulser: core circuit, core circuit with full-direction ESD protection and circuit with full-direction ESD protection by ESD-circuit co-design .

## Chapter 5 Conclusion

### 5.1 Summary

This dissertation introduces the principles of ESD protection design, ESD test models and basic ESD protection structures. As stated before, characteristic size shrinkage and IC technology advancement bring new challenges to the ESD protection design, especially on technology "ESD Design Window". To solve this problem, two novel ESD protection structures are proposed.

The first novel ESD protection structure is the VLTdSCR, which is fabricated in a common 0.18 $\mu\text{m}$  bulk CMOS technology. TCAD-ESD design methodology is applied here and verified by the testing results. The VLTdSCR core structure is a five-layer ( $\text{N}_1\text{P}_2\text{N}_3\text{P}_4\text{N}_5$ ) two-node (A=Anode & K=Cathode) symmetrical SCR-type device consisting of one lateral PNP transistor and two vertical NPN transistor, four resistors and two embedded open-gate NMOS units, forming a symmetrical dual-polarity low- $V_{\text{t1}}$  SCR ESD protection device. Its  $V_{\text{t1}}$  can be tuned by adjusting embedded NMOS gate length or STI width, while its  $V_{\text{h}}$  could be controlled by the other dimension parameters such as middle N+ extension and middle N-Well width, able to fit the changing IC "ESD Design Window". In addition, the CULTdSCR circuits with further lower  $V_{\text{t1}}$  are also proposed.

Another novel ESD protection structure is the nano crossbar, which consists of two metal layers on the top and bottom, as anode and cathode, and one dielectric layer of  $\text{Si}_x\text{O}_y\text{N}_z$  composite in the middle. The insulator in the middle enables the device have extremely-low leakage. Electric field instantly triggers phase switching and turn on the nano crossbar device to shunt ESD current during ESD transient. After ESD pulse, it returns OFF state automatically. Testing results show nano crossbar  $V_{t1}$  could be controlled by the ratio of  $\text{Si}_x\text{O}_y\text{N}_z$  composite. Moreover, it can be used against very fast CDM ESD. The extremely-low leakages under various circumstances are observed in testing, too.

The dissertation also reviews the ultrasonic imaging principles, system architecture and the realization of each function units, such as transducer, T/R switch, HV pulser, pre-amplifier, TGC and ADC. Further, the design of ultrasonic imager-on-chip (UIC) is proposed, and its reliability issues are discussed, too.

As one of the most important units in the UIC system, the HV pulser design in LV technology is studied carefully. Among several possible candidates, the topology with RC-biasing stacked LV NMOS is chosen because of its several unique advantages, like simple biasing circuit, N-scalable topology and overstress immunity. Then a series of verification HV pulser splits, core circuit, core circuit with full-direction ESD protection and circuit by ESD-circuit co-design, are designed and simulated in a 2.5V SOI CMOS technology. Post-layout simulation has proved that ESD-circuit co-design

methodology is able to predict ESD-induced negative influences on the HV pulser and reduce its performance degradation while providing sufficient ESD protection.

## **5.2 Future Work**

Next important step for UIC system design is to integrate the transducer array into the ICs with HV pulser, T/R switch, front-end signal processing chain and the control logic circuit. That means the transducer fabrication process has to be compatible with the IC manufacturing process. Another vital issue is the design of signal processing chain with ESD protection. Even though they will be integrated into one die, the difference among them still complicates the ESD protection design. Different power supplies will generate different "ESD Design Window" and ask for specific ESD protection for every unit. Moreover, the cross-domain or cross-unit cells will face the threats from overstress. All above have to be considered in the future.

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