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A 0.4-4 THz PIN Diode Frequency Multiplier in 90nm SiGe BiCMOS

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***Abstract*—This paper introduces a silicon-based source that can radiate power from the lower end of the THz spectrum into the far-infrared region. The radiator consists of a mm-wave oscillator that drives a PIN diode multiplier. PIN diodes exhibit reverse recovery when driven strongly, and the diode switches a large amount of current in a short interval. This process is highly non-linear and generates a harmonic-rich waveform, which is utilized here for higher harmonic generation. An on-chip folded dipole antenna is used to radiate the generated THz signal. The harmonic radiation properties of the folded dipole are analyzed and presented here. Wireless harmonic injection locking is also demonstrated in this work in order to synchronize the chip to an external source. Designed in GlobalFoundries 90 nm SiGe BiCMOS process, the chip has an effective isotropic radiated power (EIRP) of 13 dBm, and -14.2 dBm radiated power at 0.39 THz. The chip is characterized up to 0.8 THz using VDI mixers, and an EIRP of -3.8 dBm is measured at 0.78 THz. In order to measure the radiated tones at higher frequencies, Fourier-transform infrared (FTIR) spectroscopy is used with a room-temperature deuterated triglycine sulfate (DTGS) detector. Measurement results confirm the presence of tones extending from THz region into the far-infrared region, with an SNR of 18.4, 14, 9.3, and 6.7 dB at 1.17, 2.21, 3.25, and 4.03 THz, respectively. This work is the first demonstration of a silicon source capable of generating detectable tones at far-infrared frequencies.**

***Index Terms*—mm-Wave, THz, far-infrared, PIN diode, SiGe, frequency multiplier, FTIR, folded dipole, injection locking**

I. Introduction

THE THz band of the electromagnetic spectrum, from 0.3-3 THz, has been of increasing interest in recent years due to its unique position between RF and optical frequencies in the electromagnetic spectrum [1]. This band offers several attractive features from both ends of the spectrum. THz has a much smaller wavelength than RF and attenuates less than optical frequencies, making it an optimal candidate for high-resolution imaging and radar. Micro-doppler radars at THz frequencies can enable high precision sub-μm vibration sensing [2]. THz also finds applications in spectroscopy since several gases exhibit absorption windows within the THz band. Due to the vast amount of unallocated spectrum, THz can enable multi-Gbps communication [3]. The far-infrared frequency range beyond 3 THz also offers several applications in astronomy and medicine [4].

However, the THz band has largely remained commercially untapped due to the challenges in THz generation. The electronics and photonics community have attempted to bridge the THz gap [5]. However, these have only been successful to some extent, and there is significant interest in designing energy-efficient and economically viable THz sources.

Photonic approaches to THz generation are mainly limited by the lack of materials that have sufficiently small bandgaps which can generate THz. Typical THz generation approaches involve techniques such as difference frequency generation, photo-mixing, quantum cascade lasers, and photo-conductive antennas. These approaches have severe limitations which prevent commercial use. They are bulky, require cryogenic operating conditions, and are sometimes limited to slow pulsed operation [6], [7].

On the electronics front, silicon-based THz generation is of interest due to its digital circuit integration capabilities. Advanced CMOS nodes offer f_T/f_{max} as high as 350/370 GHz [8]. Heterojunction bipolar transistors (HBTs) in commercial SiGe BiCMOS processes have achieved f_T/f_{max} as high as 470/610 GHz [9]. HBTs also offer a higher breakdown voltage when compared to CMOS. Despite this, the highest frequency reported for a fundamental oscillator in silicon is 300 GHz [10]. This is due to the challenges in fundamental oscillator design at frequencies above $f_{max}/2$. Harmonic generation approaches need to be used to generate power at higher frequencies.

Among existing literature, only a few silicon-based sources operate beyond 1 THz. In [11], a 1 THz radiator array is implemented using 91 oscillators having a fundamental frequency of 250 GHz. Active frequency multipliers have been presented in [12], [13], and [14] to generate power at 0.92 THz, 1 THz, and 1.4 THz, respectively. A harmonic oscillator is demonstrated in [15], with tones observed up to 2.45 THz. These tones were measured using a highly sensitive cryogenic bolometer detector. Compound semiconductor-based approaches have also been demonstrated [16]–[18]. However, these technologies do not offer the same extent of digital integration capabilities as silicon.

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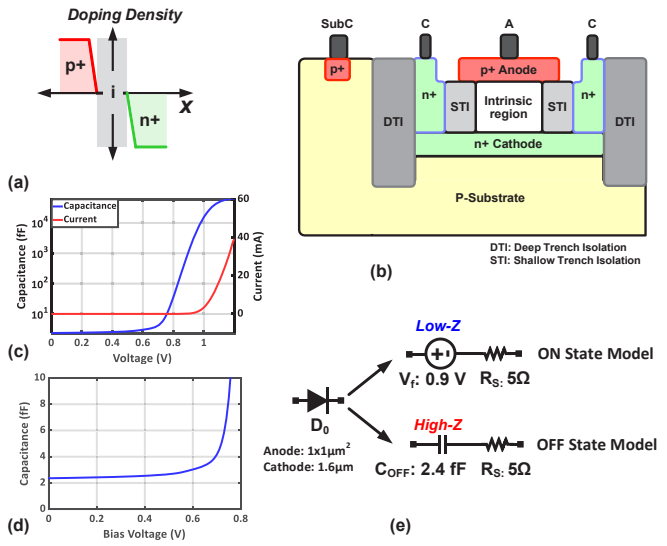

Fig. 1. (a) Doping profile of a PIN diode (b) Illustration of a PIN diode in the GlobalFoundries 90 nm process (c) Diode I-V and C-V curves (d) Diode C-V curve (re-plotted to show depletion capacitance) (e) Small signal model of the PIN diode during ON state and OFF state

There is a need for silicon-based integrated solutions for THz generation. Existing works use the non-linearity in varactors and transistors to generate THz. These devices show weak non-linearity, which ultimately limits the generated harmonic power. Highly efficient harmonic generation was demonstrated in the 1960s at lower microwave frequencies using discrete step-recovery diodes (a category of PIN diodes). These devices are highly non-linear due to strong reverse recovery, and this was utilized for comb generation and high-efficiency harmonic generation [19], [20].

In our previous work [21], we report pulse generation using reverse recovery in silicon PIN diodes. A digital trigger at 15 GHz is used to excite a PIN diode into reverse recovery. During reverse recovery, PIN diodes generate a highly non-linear waveform rich in harmonics. Measurement results showed strong tones were generated and could be measured up to 1.1 THz. This confirms the highly non-linear nature of the PIN diode since a 15 GHz signal could generate a tone at its 73rd harmonic at 1.1 THz. However, in [21], the digital trigger signal could not be increased beyond 15 GHz. Due to this low repetition rate, the generated power is low at high frequencies and cannot generate detectable tones beyond 1.1 THz.

This work builds on the PIN diode pulse generator from [21]. The goal here is to maximize the number of harmonics generated and study the possibility of signal generation beyond 1 THz. In this work, the PIN diode is driven using an on-chip mm-wave oscillator at 130 GHz. The oscillator follows a standard Colpitt's topology [22], [23]. Because of the mm-wave trigger, the PIN diode can generate detectable tones at THz frequencies and even into the far-infrared region. A folded dipole antenna is used because of its impedance profile and harmonic radiation properties, which are explained in subsequent sections. This work also proposes wireless harmonic injection locking to lock the chip to an external source. Wireless locking consumes no DC power and does not limit the tuning range of the mm-wave LO. Using an FTIR spectrometer, broadband measurements are performed to measure the radiation up to 6 THz. This is the first demonstration of silicon-based generation above 2.5 THz. This work was presented in [24], and a detailed analysis is provided in this paper.

The rest of this paper is organized as follows. Section II explains the fundamentals of a PIN diode, reverse recovery mechanism and gives a general approach to frequency multiplier design. The circuit design details are explained in Section III. Section IV explains the antenna design and analysis and wireless harmonic injection locking. Measurement results are presented in Section V, and the paper is concluded in Section VI.

II. PIN Diode

A PIN diode is a semiconductor diode with an undoped intrinsic region positioned between two heavily doped p+ and n+ semiconductor regions. Fig. 1 (a) shows the doping profile of a PIN diode. The presence of the intrinsic region differentiates a PIN diode from a regular diode. Conventionally, these diodes are used in RF/microwave switches, attenuators, limiters, photodetectors, and as step recovery diodes [25], [26]. PIN diodes can easily be fabricated in standard silicon processes without any additional masks and are provided as standard cells in some process design kits (PDKs). Fig. 1 (b) shows the structure of a PIN diode in GlobalFoundries 9HP PDK. It consists of a p+ anode, an intrinsic region, and an n+ cathode. The intrinsic region is realized using an n- layer in 9HP. A deep-trench surrounds the diode for isolation. These diodes have low parasitic capacitance and a high breakdown voltage [27].

A. Reverse Recovery in PIN Diodes

For the analysis presented in this paper, we use the default PIN diode model from the GlobalFoundires 90nm SiGe BiCMOS process (9HP - V1.2) PDK. Otherwise specified, the diode chosen has an anode area of 1x1 μm^2 and a cathode width of 1.6 μm. The reasons for choosing this size are explained later in this section.

The I-V and the C-V behavior of the diode are plotted in Fig. 1 (c), (d). The C-V curve is obtained through small signal Y-parameter simulations. The dominant capacitance is the diffusion capacitance when the diode is ON and the depletion capacitance when the diode is OFF. Due to the large diffusion capacitance, the diode behaves like a voltage source when ON and can sink a large current. When OFF, the diode behaves as a high-impedance capacitor (2.4 fF at 0 V bias). Based on this, a small signal equivalent circuit for a PIN diode is given in Fig. 1 (e) for both ON and OFF states. The diode contact resistance is also included in this model.

During a large-signal drive cycle, the PIN diode switches abruptly from the low-impedance ON stage to the high-impedance OFF stage. The abrupt switching is due to the reverse recovery and is the basis for multiplier design. A detailed

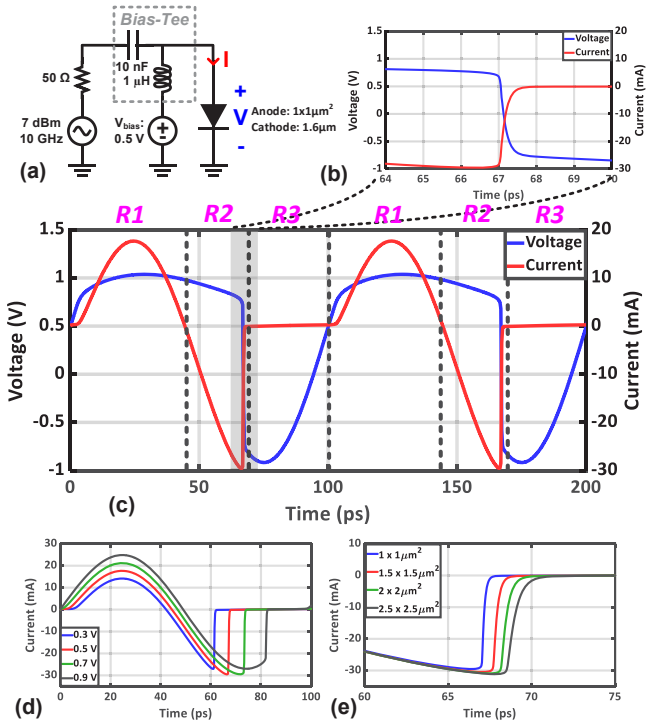

Fig. 2. (a) PIN diode driven by a 7 dBm RF source at 10 GHz (b,c) Corresponding voltage and current waveforms simulated using SpectreRF (d) Current waveform for different V_{bias} (e) Current waveform for different diode sizes (waveform is magnified to show the variation in slope)

analysis of a charge storage model for reverse recovery can be found in [28].

The reverse recovery phenomenon can be understood by analyzing the circuit in Fig. 2 (a). Here, the PIN diode is driven by an RF source at 10 GHz. A power level of 7 dBm is chosen such that there is sufficient power to drive the diode into reverse recovery under unmatched impedance conditions. The selection of the DC bias and diode size is explained later in this section. The corresponding voltage and diode current waveforms for the circuit in Fig. 2 (a) under the above bias and drive conditions (simulated using SpectreRF) are plotted in Fig. 1 (b), (c). Three distinct regions of operation can be observed and are explained below.

During R1, the diode is in forward conduction mode. The p+ and n+ regions inject electrons and holes into the I-region. Due to the long minority carrier lifetime, τ ($>$ 1 ns, as per simulations), these carriers get stored in the I-region. The amount of stored charge Q_i for a diode current I is given by

$$I = \frac{dQ_i}{dt} + \frac{Q_i}{\tau} \tag{1}$$

Because of this carrier storage, a large diffusion capacitance is formed (Fig. 1 (c)). The voltage across the diode is clamped to the diode turn-on voltage V_f, which is about 0.9 V in this process.

During R2, the diode enters reverse conduction mode, and the diode continues to conduct by depleting the stored carriers. The voltage across the diode still remains approximately equal to V_f.

Once all the carriers are depleted, the diode can no longer sustain current and undergoes reverse recovery. This is denoted in region R3. The current across the diode abruptly switches to zero (in $<$ 1 ps as per simulations), and the diode turns OFF. The time constant for the reverse current switching to zero, τ_t, depends on the diode capacitance, and junction resistance, and is independent of the frequency of the source that drives the PIN diode. This enables realizing sharp switching using PIN diodes. Once all the carriers are depleted, the diode behaves like a small depletion capacitance (Fig. 1 (d)). To summarize, the PIN diode switches a large amount of current in a short interval due to reverse recovery.

B. Bias and Diode Size Selection

The fast switching behavior makes PIN diodes a prime candidate for building frequency multipliers. The generated harmonic content is proportional to the rate of switching (di/dt). For multiplier design, we wish to maximize the amount of current that is being switched while minimizing the time taken for switching. The former can be maximized by choosing the DC bias of the diode such that it undergoes reverse recovery while carrying peak current. This is illustrated in Fig. 2 (d), where the V_{bias} is varied while the diode size is fixed. In this example, a V_{bias} of 0.5 V switches more current compared to other biases. Note that this bias can vary with the amount of input RF power.

The time taken for switching can be minimized by proper diode size selection. While larger diodes have less contact resistance, smaller diodes have less capacitance. It is shown in [21] that smaller diodes present sharper reverse recovery and time to switch. This is illustrated in Fig. 2 (e), where the V_{bias} is fixed at 0.5 V, while the diode size is varied. It can be seen that the anode area of 1 x 1 μm^2 presents the fastest switching, and this size is chosen for multiplier design in this work. While choosing the cathode area, we chose a large cathode width of 1.6 μm. This is because a larger cathode allows low-impedance contacts to the diode. Since the cathode is connected to an RF ground, its size does not contribute to parasitic capacitance.

C. PIN Diode Multiplier Design

Based on the discussion above, we present an approach to multiplier design. A PIN diode driven by an AC current source is given in Fig. 3 (a). The diode is replaced by its small-signal equivalent in Fig. 3 (b). Here, R_P models the losses in the circuit.

The voltage and current waveforms for the ideal circuit in Fig. 3 (b) are plotted in Fig. 3 (c). In region R1, the current source provides a large-signal RF current to the PIN diode, which turns it ON. The intrinsic region of the PIN diode gets filled with carriers during R1, and the voltage across the diode gets clamped to V_f ($\approx$ 0.9 V). Since a DC voltage appears across the inductor, it conducts a ramp current during this interval, all of which sinks into the diode. In region R2, the current source has a negative current. The PIN diode can source this current due to the presence of stored carriers. The voltage across the diode remains clamped to V_f. However, reverse conduction depletes these carriers. The

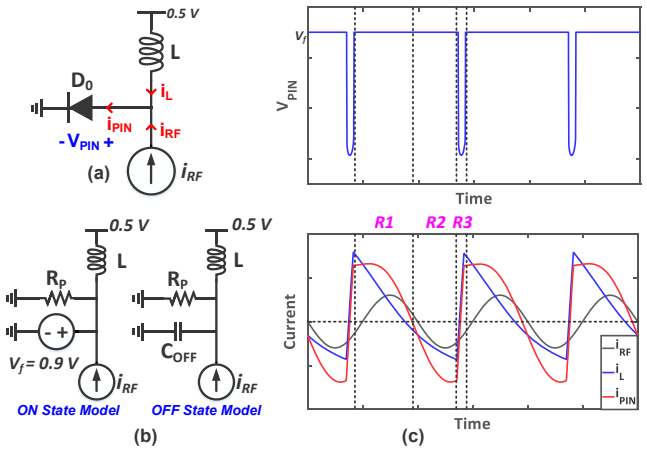

Fig. 3. (a) PIN diode multiplier at f_0 (b) Equivalent circuit model of the PIN diode multiplier during ON and OFF states (c) Voltages and currents in the idealized PIN diode multiplier

carriers eventually run out, and the diode turns OFF (region R3). Once OFF, the diode behaves like a capacitor, C_{OFF}. However, KCL has to be satisfied, which forces the inductor to source the required current. The sudden change in inductor current creates a sharp negative voltage pulse at the diode. The height and width of this pulse depend on the quality factor of the L-C tank. This voltage pulse causes a damped oscillation in the RLC circuit and charges C_{OFF}. Once the diode is sufficiently charged, it starts conducting and enters forward conduction (region R1). This cycle is repeated.

The generated voltage pulse is rich in harmonics, and this circuit can behave like a comb generator when connected to a resistive load. When connected to a resonant load at a harmonic, this circuit can efficiently generate just that harmonic. It should be noted that the diode bias voltage sets the inductor current, which can be adjusted to change the onset of reverse recovery. Choosing a diode bias where the diode turns OFF while carrying peak reverse current will create the sharpest pulse. Based on this, the following design procedure is adopted:

1) Appropriate selection of diode size and biasing as discussed above.
2) Perform a conjugate match between the PIN diode and the RF source using the large-signal impedances at the fundamental frequency.
3) If a large number of output harmonics are desired (such as a frequency comb), connect the load to the PIN diode while avoiding additional matching networks.
4) If high power is required at a specific harmonic, connect a resonant load at that frequency to the PIN diode. The unwanted harmonics can be reactively terminated.

III. Circuit Design

This section explains the circuit design techniques. We design the circuit with the goal of maximizing the number of harmonics generated in order to study the possibility of signal generation beyond 1 THz.

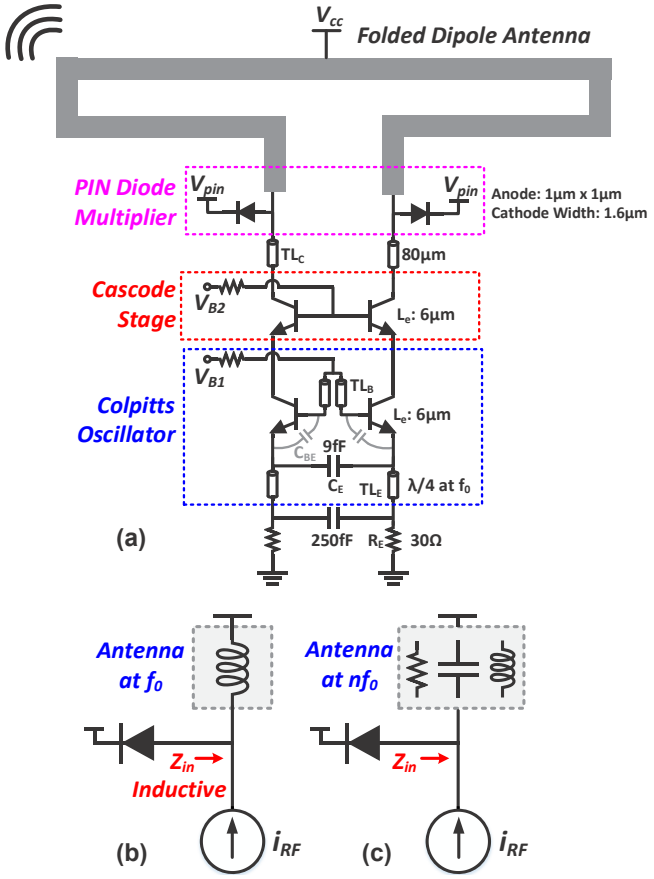

Fig. 4. (a) Schematic of a mm-wave Colpitts oscillator driving a PIN diode multiplier and folded dipole antenna (b) Equivalent circuit model of the oscillator-multiplier-antenna system at f_0 (c) Equivalent circuit model of the oscillator-multiplier-antenna system at higher harmonics

A. mm-Wave Colpitts Oscillator

A differential Colpitts oscillator is used in this design to drive the PIN diode. Fig. 4 (a) shows the schematic of the Colpitts oscillator. The Colpitts tank formed by the capacitor C_E, the parasitic C_{BE}, and base transmission-line (TL) TL_B sets the resonance frequency to 130 GHz. TL_B is shorted to a resistor, ensuring that the oscillator only starts up in the required odd mode. In odd mode conditions, the resistor appears on the virtual ground and does not load the tank. The emitter is connected to a TL, which is $\lambda/4$ at the fundamental frequency f_0. This line creates a high impedance and does not load the oscillator core. Resistors R_E are used to set the bias. Alternatively, a single resistor of $0.5R_E$ can also be used with a shunt capacitor to set the bias. An active current source bias is avoided since this would result in an upconversion of the flicker noise and can impact the phase noise performance of the oscillator.

Frequency tuning is achieved by changing the base voltage, V_{B1}, which varies the capacitance C_{BE} and shifts the tank resonance. This frequency tuning method is advantageous at mm-wave frequencies compared to other techniques, such as varactor tuning, which is lossy and can degrade the quality factor of the resonance tank. However, changing the base voltage also changes the bias current. At a frequency away

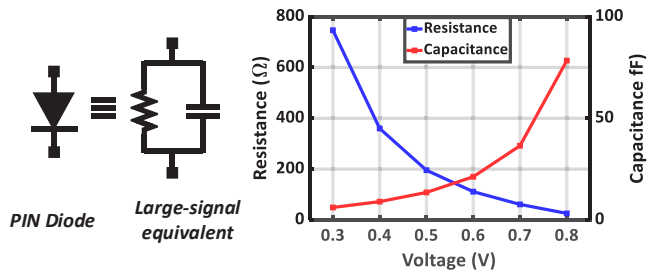

Fig. 5. Large-signal equivalent circuit and simulated large signal input impedance for different voltage biases across the diode

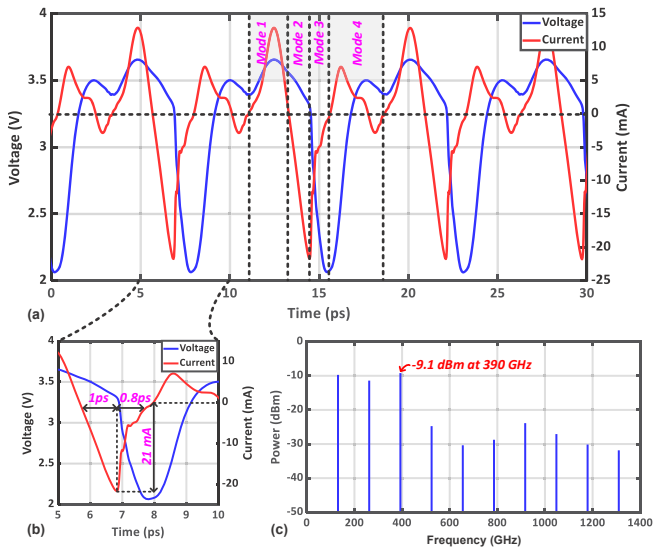

Fig. 6. (a) Simulated voltage at the antenna node, and current flowing into the PIN diode for the circuit in Fig. 2(a) (b) Magnified view (c) Simulated spectrum of the power flowing into the antenna

from the center frequency, the oscillator generates less power, and consequently, the generated harmonic power degrades. A cascode transistor driver stage connects the oscillator core to the PIN diode. This stage buffers the oscillation and drives the PIN diode multiplier through TL_C, which performs impedance matching at the fundamental frequency. Under optimal bias conditions, when the transistors are biased at peak f_{max}, the oscillator generates 5 dBm power and consumes 23 mA.

B. PIN Diode Frequency Multiplier

The PIN diode is directly connected to a folded dipole antenna, as shown in Fig. 4 (a). The diode size is chosen to have an anode area of 1 μm x 1 μm and a cathode width of 1.6 μm based on the discussions in Section II. The antenna simultaneously behaves like an inductor at the fundamental frequency, f_0, and radiates at the other harmonics. Analysis of this antenna is provided in Section IV. Fig. 4 (b), (c) shows a simplified picture of the oscillator-multiplier-antenna system. An AC current source drives a PIN diode connected to the antenna. At f_0, the diode sees an inductive impedance, and at other harmonics, the diode sees the antenna load.

Due to the non-linear nature of multipliers, the large signal impedance needs to be considered. The large signal impedance of the diode at 130 GHz is simulated using SpectreRF and is plotted in Fig. 5. Here, the x-axis denotes the DC voltage across the diode. It can be observed that as the bias voltage increases, the diode turns ON, and the impedance of the diode drops. The diode-antenna inductor circuit is large-signal impedance matched to the oscillator at the fundamental frequency using transmission line TL_C. Since the goal is to maximize the harmonic content at multiple frequencies, additional matching networks to match the antenna and isolate the oscillator core are not used. This is because matching networks are narrow-band and can add loss, which becomes increasingly significant at upper THz frequencies. This may be pursued if a specific harmonic is of interest.

The PIN diode multiplier behavior from Fig. 4 (a) is simulated using SpectreRF. A broadband SNP file (common file format for storing S-parameter data) models the antenna. The voltage at the antenna node and the current flowing into the PIN diode is plotted in Fig. 6 (a), and the waveforms are analyzed. In Mode 1, the diode is in forward conduction, and the intrinsic region is filled with excess carriers. The diode enters reverse conduction in Mode 2. By the end of Mode 2, the carriers get depleted, and the diode stops conducting. The inductive antenna is forced to source the current, creating a sharp negative impulse voltage (Mode 3). This current also charges the diode, and it enters forward conduction again. In mode 4, due to the finite Q of the system, the circuit undergoes damped oscillations and eventually settles and re-enters forward conduction (Mode 1).

During this drive cycle, the peak negative current is 21 mA, with a 10% fall-time and rise-time of 1 ps and 0.8 ps, respectively. This is magnified in Fig. 6 (b). A spectrum of the simulated amount of power that enters the antenna is plotted in Fig. 6 (c). Antenna efficiency is not considered here. A peak power of -9.1 dBm is observed at the third harmonic.

IV. Folded Dipole Antenna - Design and Analysis

The PIN diode requires an inductive load at the fundamental frequency for efficient harmonic generation, and the generated harmonics need to be efficiently radiated. This work achieves both these requirements simultaneously by using a folded dipole antenna. The folded dipole also has harmonic radiation properties, which enables its use over the broad frequency range.

The folded dipole antenna used in this work is shown in Fig. 7 (a). It is designed to have good radiation at the third harmonic (390 GHz), with the length, $L = \lambda/2$ at 390 GHz. A biasing stub line is connected to the antenna in order to bias the oscillator. A ground ring is placed around the antenna for isolation.

The folded dipole antenna is basically an unbalanced transmission line and can be analyzed by dividing its current into two modes: an antenna mode and a transmission line mode. This is illustrated in Fig. 7 (b). To simplify the analysis, the spacing d between two individual dipoles is assumed to be

negligible. The input impedance of the folded dipole is given by [29]:

$$Z_{in} = \frac{4Z_t Z_a}{2Z_a + Z_t} \tag{2}$$

were Z_t and Z_a stand for the input impedance of the transmission line mode and the antenna mode, respectively. Using this method, the impedance and radiation characteristics of the folded dipole antenna at several harmonics are analyzed.

A. Fundamental Harmonic (130 GHz)

The oscillator excites the antenna differentially at the fundamental harmonic. Because of this, the bias line lies on a PEC (Perfect Electric Conductor) plane with a virtual ground and can be ignored. Fig. 8 (a) shows the model of the folded dipole at the fundamental frequency. Since the dipole has $L = \lambda/2$ at the third harmonic, the effective length of each half side is $\lambda/12$ at the fundamental. Thus, the length of each half is less compared to the fundamental wavelength, and we can assume that the current distributions on two parallel wires are nearly identical in amplitude but opposite in direction. These two currents can be seen as the forward current and the reverse current of a two-wire transmission line. Since the two wires are connected at the end, the TL is shorted with a length of $L = \lambda/12$. The input impedance is identical to the single-side TL, and is given by:

$$Z_t = \frac{V}{I_t} = jZ_0 tan(\beta L/2) \tag{3}$$

where Z_0 and β represents the characteristic impedance and phase-constant of the two-wire TL. Therefore, when $L/2 = \lambda/12$, the folded dipole antenna can provide an inductive impedance to the PIN diode without requiring an additional matching network. In contrast, when a regular dipole is driven at low frequencies (where $L < \lambda/2$), it will present a capacitive load. This is because the regular dipole behaves like a TL, which transforms a high-impedance open through an $L < \lambda/2$ line to a capacitive impedance which lies on the bottom half of the Smith Chart.

B. Third Harmonic (390 GHz)

The folded dipole antenna is designed to have optimum radiation at 390 GHz, and the length, L, is chosen to be $\lambda/2$ at 390 GHz. According to the transmission line mode analysis, Z_t can be written as:

$$Z_t = \frac{V}{I_t} = [jZ_0 tan(\beta L/2)]_{(L=\lambda/2)} = \infty \tag{4}$$

Therefore, the total input impedance is derived as follows:

$$Z_{in} = 4Z_d \tag{5}$$

where Z_d is the impedance of an isolated dipole antenna. Eq. (5) shows that the input impedance of the folded dipole is four times that of a regular dipole antenna. The current and electric field distribution of the folded dipole antenna at 390 GHz is given in Fig. 8 (b). Note that the TL mode is extensively suppressed at this frequency since the currents in the two parallel wires are the same in amplitude and direction.

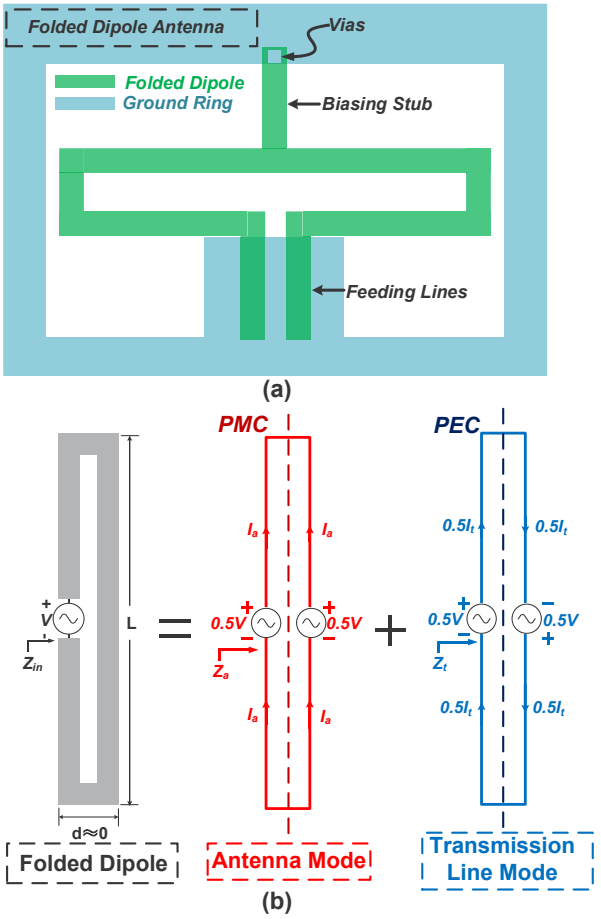

Fig. 7. (a) Folded dipole antenna (b) Equivalent antenna mode and transmission line mode of the folded dipole antenna

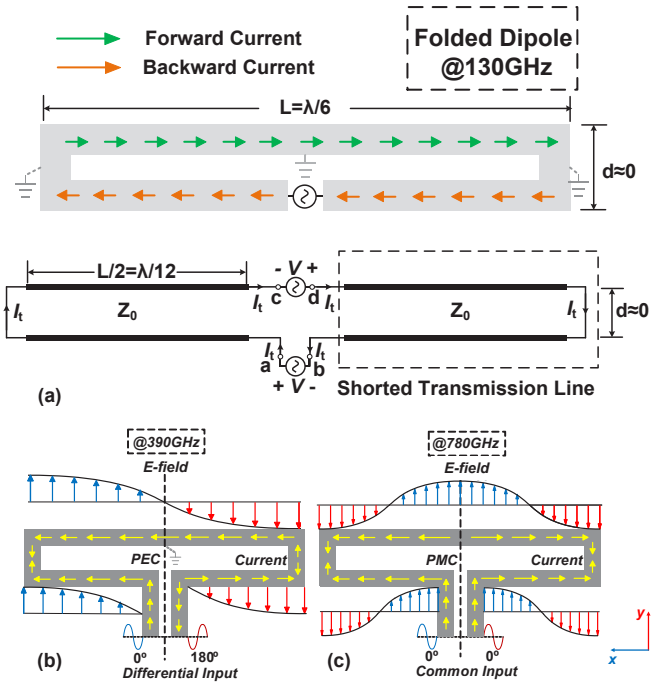

Fig. 8. (a) Folded dipole antenna behaving like a transmission line at the fundamental frequency, 130 GHz (b) Antenna behavior at 390 GHz (c) Antenna behavior at 780 GHz

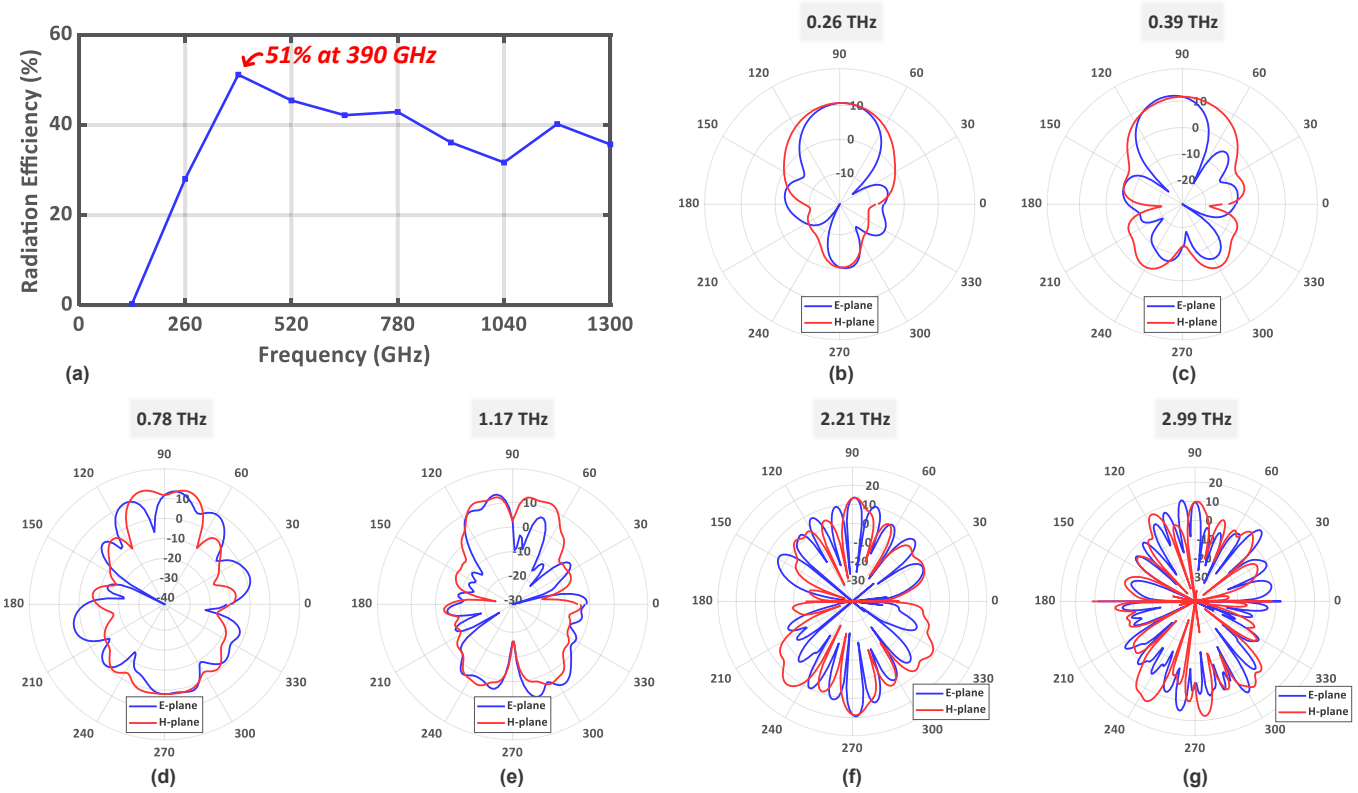

Fig. 9. (a) Simulated antenna efficiency (b)-(g) Simulated radiation pattern of the antenna at 0.26, 0.39, 0.78, 1.17, 2.21 and 2.99 THz. The radial axis shows directivity.

Therefore, it can be regarded as two regular dipoles placed near each other, resulting in good radiation combining.

This analysis can be generalized to any odd multiples of 390 GHz, such as 1170 GHz, 1950 GHz, etc. Although the antenna is electrically longer than $L = \lambda/2$ at these frequencies, the currents in the extra electrical length cancel each other and do not affect radiation.

C. Even Harmonics

The analysis of the folded dipole is challenging at even harmonics. The even harmonics generated from the PIN diode multiplier are in-phase, and the antenna is driven in common-mode. This means that the bias line and the ground-isolation ring will impact radiation behavior.

At frequencies that are even multiples of 390 GHz, the electrical length of the folded dipole is a multiple of λ. For example, at the sixth harmonic, the length $L = \lambda$ and the current and E-filed distributions are shown in Fig. 8 (c). The currents on the two main lines are identical in amplitude and direction. However, the currents flow in opposite directions at the left/right side of the antenna. Ideally, the radiations will cancel each other. However, because of the silicon lens, the two halves behave as two individual folded monopoles placed away from the axis of the lens and will produce a beam that does not fully get canceled. Moreover, the bias line and the ground ring will have currents that cause radiation. Because of this, the antenna radiates in both horizontal (HP) and vertical polarization (VP).

At other even harmonics, which are not multiples 390 GHz, the antenna behavior becomes very challenging to predict and is not analyzed here. However, as observed in simulations and measurements, the antenna radiates in both HP and VP.

D. Radiation Pattern and Efficiency

To better demonstrate the performance of the folded dipole antenna, the radiation pattern and efficiency at different harmonics are simulated using CST studio. A high-resistive hyper hemispherical silicon lens is used, which reduces substrate modes and enhances the directivity. The antenna with the lens takes unreasonable simulation times at THz frequencies. To reduce simulation time, the simulations are performed using a lens with a 0.6 mm radius up to 1.3 THz. Beyond this, a lens radius of 0.3 mm is used. The simulated efficiency and radiation patterns are plotted in Fig. 9. It can be seen that the radiation efficiency at 130 GHz is close to zero, thus validating that the folded dipole behaves more like a TL instead of an antenna at this frequency. The antenna has the highest efficiency of 51% at 390 GHz. The radiation efficiency remains largely unaffected beyond 390 GHz due to minimal changes in both ohmic loss in copper and the dielectric loss in the substrate. The antenna radiation pattern is clean at 260 GHz and 390 GHz. Multiple side lobes start to appear above 1 THz. Due to the small wavelength at these frequencies, the antenna becomes electrically very large ($L > \lambda$) and behaves as multiple small antennas, all of which provide beams that are focused in different directions by the lens.

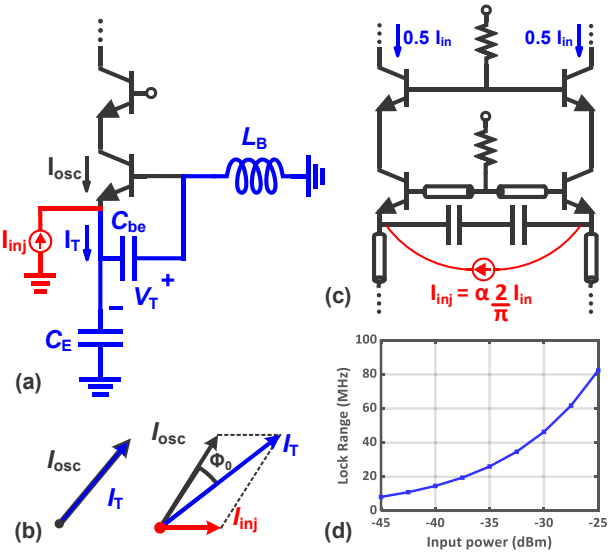

Fig. 10. (a) Half-circuit of oscillator core under external injection I_{inj} (b) Current phasors (c) Oscillator under an injection current at second harmonic (d) Calculated lock range vs injection power

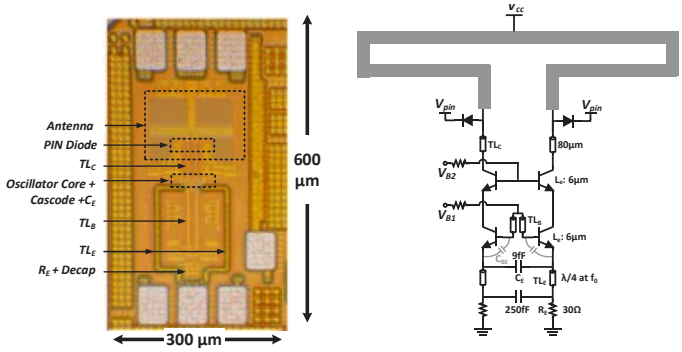

Fig. 11. Die micrograph indicating the circuit components

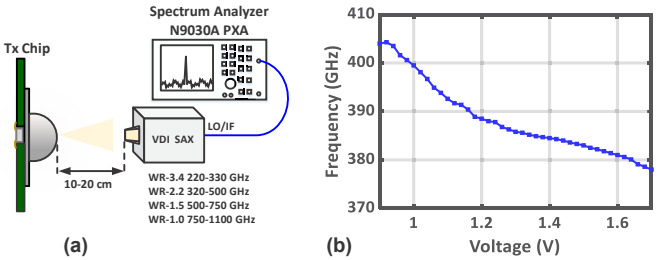

Fig. 12. (a) Measurement setup used for characterizing the chip using VDI mixers (b) Measured tuning range at 390 GHz

To conclude the antenna analysis, although the folded dipole antenna behaves best at 390 GHz, it can still radiate at other harmonics with good efficiency and reasonable radiation pattern. The antenna also behaves like an inductor at 130 GHz, which is essential for multiplier operation.

E. Wireless locking

Some THz applications, such as spectroscopy and coherent detection, require precise frequency and phase alignment with good phase noise [30]. This may be achieved using a PLL or a frequency multiplier chain. These, however, are challenging to build at THz frequencies, consume high DC power, and offer limited frequency tuning. This work demonstrates harmonic wireless injection locking. A harmonic of the fundamental oscillation frequency is injected wirelessly into the chip and is used for locking. Wireless locking does not take any additional DC power. By tuning the frequency of the external source, the entire frequency range of the on-chip oscillator can be covered. Wireless locking also enables frequency synchronization among an array of independent chips.

This work uses an external source at twice the fundamental frequency, $2f_0$, to lock the chip. The external source is radiated to the top side of the chip so that it does not block the backside radiation coming from the chip. The folded dipole antenna receives this external signal in its common-mode. The 260 GHz locking signal in this work is generated using commercial test equipment. A separate silicon chip may be employed to generate this signal.

The injection locking analysis from [31] and [32] is extended to this work. Fig. 10 (a) shows a half-circuit of the oscillator core when injected with an external current source I_{inj}. The tank has a quality factor of 9, as per simulations. The resultant tank current I_T, consists of the transconductor current I_{osc} and the injected current I_{inj}. I_{inj} creates a phase difference between I_T and I_{osc}, shifting the oscillation frequency to f_{inj} by making the tank compensate for the introduced excess phase. These currents are visualized in Fig. 10 (b), and all the phasors are normalized to the I_{inj}.

The wireless injection signal received at $2f_0$ generates a common-mode injection current, I_{in}, flowing towards the core, as shown in Fig. 10 (c). This current mixes with the fundamental oscillator current in the core [31], and results in a differential injection current I_{inj}, around the fundamental frequency.

$$I_{inj} = \alpha \frac{2}{\pi} I_{in} \tag{6}$$

where α is a loss factor that accounts for the fraction of I_{in} that reaches the core and gets mixed. Simulations show α to be 0.125. Using the analysis in [31], under the weak injection assumption, we estimate the one-sided lock range to be:

$$f_L \approx \frac{f_0}{2Q} \frac{I_{inj}}{I_{osc}} = \frac{f_0}{\pi Q} \frac{\alpha I_{inj}}{I_{osc}} \tag{7}$$

The calculated double-sided lock range at the third harmonic, 390 GHz is plotted in Fig. 10 (d). These calculations match simulations at high injected powers ($>$ -10 dBm). At lower injected powers, the simulation takes unreasonably long to converge.

V. Measurements

The design was fabricated in GlobalFoundires 90 nm SiGe BiCMOS process (9HP - regular variant V1.2). This process has NPN transistors with f_T= 300 GHz, f_{max} = 360 GHz and BV_{CEO} = 1.7 V [33]. A die micro-graph is shown in

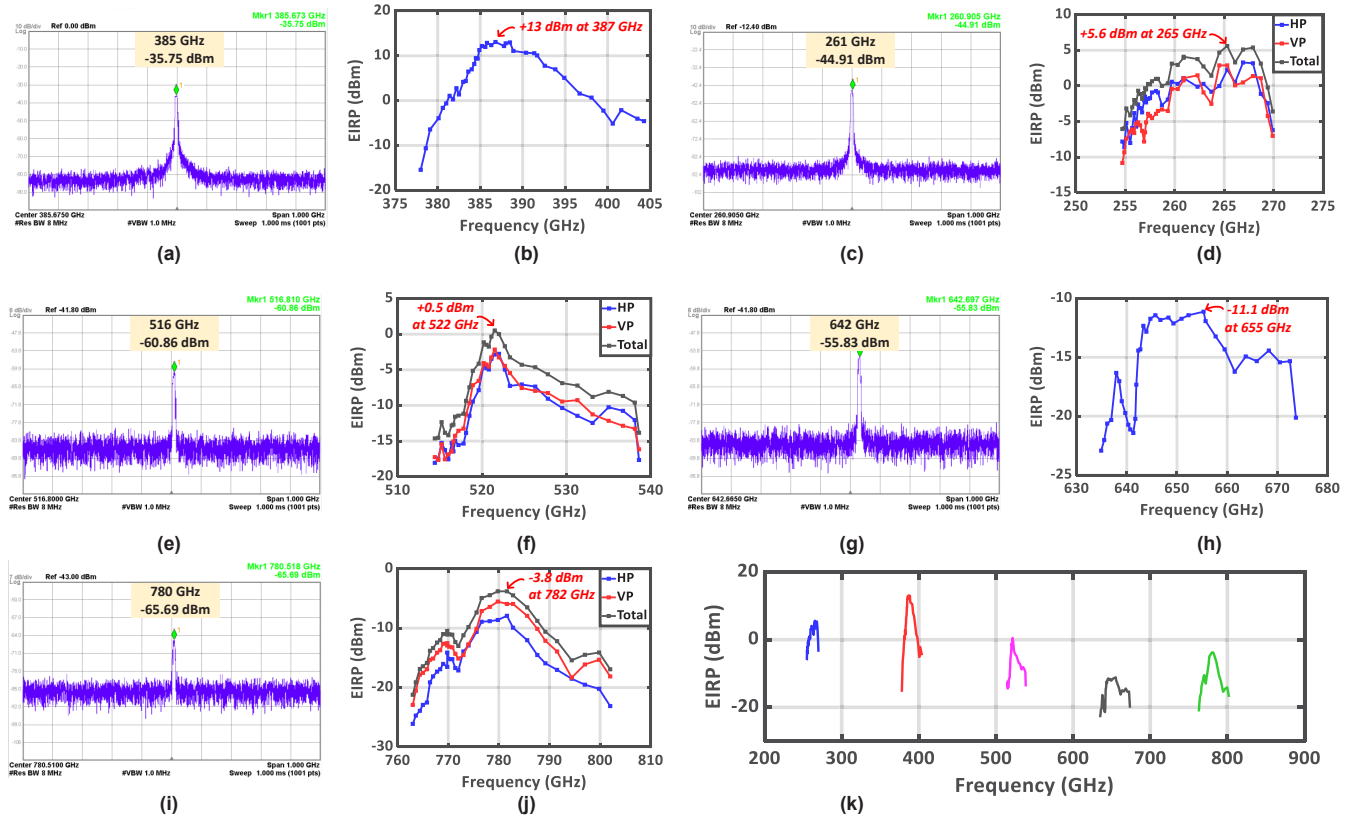

Fig. 13. (a) - (j) Measured tones and the corresponding EIRP spectrum at harmonics of 130 GHz (k) EIRP variation across multiple harmonics

Fig. 11. The design occupies an area of 0.18 mm^2 (including pads) and consumes 70 mW DC power in nominal operation. The chip is mounted on a custom-designed PCB, and a hyper-hemispherical silicon lens of a 6 mm radius is attached to the backside of the chip. An undoped high-resistive dual-side-polished (DSP) silicon wafer of 0.5 mm thickness is placed between the chip and the lens.

A. Radiation Measurements

The antenna is designed to radiate efficiently at 390 GHz; hence, the chip is characterized mainly at that frequency. Fig. 12 (a) shows the measurement setup used to characterize the EIRP. The chip is kept at a far-field distance of 20 cm from a Virginia Diodes (VDI) WR 2.2 spectrum analyzer extender (SAX). The VDI SAX is used in spectrum-analyzer extension mode with an Agilent N9030A spectrum analyzer. The measured spectrum at 385 GHz is plotted in Fig. 13 (a). The oscillation frequency is varied by changing the base voltage, and the voltage tuning curve is plotted in Fig. 12 (b). A 6% tuning range covering a span of 24 GHz is obtained at 390 GHz.

The EIRP is measured at different harmonics of the fundamental frequency, from 260 GHz (second harmonic) to 780 GHz (sixth harmonic). Multiple VDI spectrum analyzer extenders are used to cover the whole band (WR3.4, WR2.2, WR1.5, WR1). For the WR3.4 and WR2.2 measurements, the chip is kept at a 20 cm distance, while for WR1.5 and WR1, the chip is kept at a 10 cm distance from the VDI

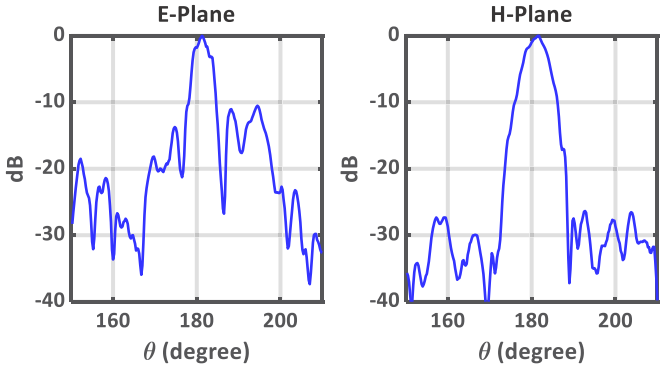

Fig. 14. Measured radiation pattern along E-plane and H-plane at 390 GHz

SAX. The measured tones across the bands are plotted in Fig. 13 (a,c,e,g,i). The base voltage is varied, and the radiated powers are measured across the tuning range. It should be noted that the chip radiates along the horizontal polarization for odd-harmonics. For even harmonics, the chip radiates along both horizontal and vertical polarizations. This matches the conclusions from the antenna analysis section.

The EIRP is calculated by de-embedding the free-space path loss, VDI downconversion loss, VDI antenna gain, and cable loss. The measured EIRP around different harmonics are plotted in Fig. 13 (b,d,f,h,j). The highest EIRP of +13 dBm is observed for the third harmonic at 387 GHz. This matches the expectations and simulation results since the

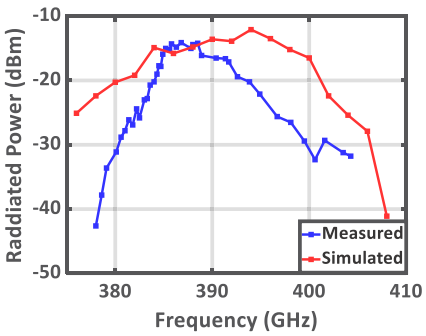

Fig. 15. Measured and simulated radiated powers at the third harmonic

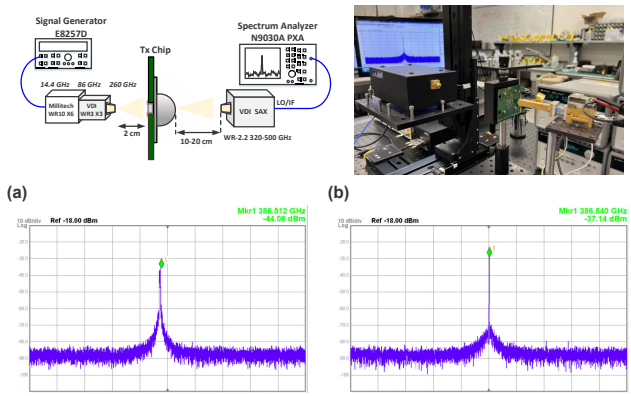

Fig. 16. (a) Measurement setup used to demonstrate wireless locking (b) Photograph of the measurement setup (c) Measured unlocked tone at 386 GHz (d) Measured locked tone at 386 GHz

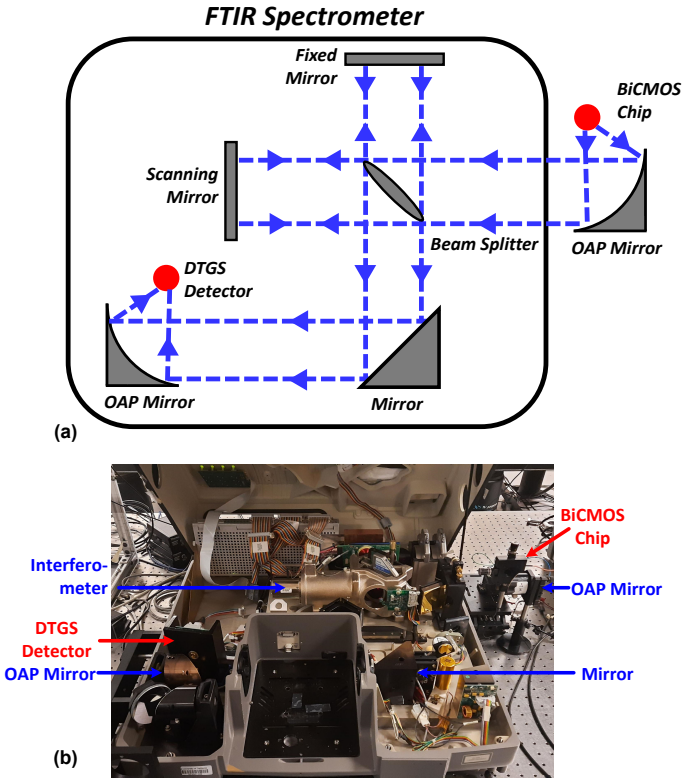

Fig. 17. (a) FITR spectrometer measurement setup (b) Photograph of the FTIR setup

antenna radiates optimally at that frequency. The chip radiates along two orthogonal polarizations for the even harmonics, and the total EIRP is obtained by summing them. At the second harmonic, a peak EIRP of +5.6 dBm is measured at 265 GHz. At the fourth harmonic, a peak EIRP of +0.5 dBm is measured at 522 GHz. A peak EIRP of -11.1 dBm is measured at 655 GHz for fifth harmonic. Finally, a peak EIRP of -3.8 dBm is measured at 782 GHz for the sixth harmonic. The seventh harmonic could not be measured as the VDI extender has a high conversion loss at this frequency (0.91 THz). Fig. 13 (k) shows the EIRP spectra across all these measured frequencies.

The radiation pattern of the chip is measured at 390 GHz. The chip is mounted on a rotatable stage kept at 20 cm from the VDI SAX and the powers are measured at different angles. The measured radiation patterns across the E-plane and H-plane are given in Fig. 14. The directivity is calculated to be 27.2 dB, using the directivity formula from [34]. After de-embedding the directivity from EIRP, the peak radiated power at 387 is calculated to be -14.2 dBm. The measured and simulated radiated powers are plotted in Fig. 15 and they align reasonably well. The peak power has been reduced by 3 dB, and we attribute it to potential device and circuit modeling errors.

B. Wireless Locking Measurements

Wireless harmonic injection locking is demonstrated in this work, where the mm-wave oscillator is locked wirelessly using an external source at a harmonic of the fundamental frequency. Fig. 16 (a) shows the setup used for wireless injection locking. A 260 GHz external signal is used to injection lock the on-chip oscillator. A multiplier chain consisting of a Millitech WR10 multiply-by-6 module and VDI WR3 tripler generates about -6 dBm at 260 GHz. The wireless injection source is kept at a 2 cm distance from the front side of the chip. Fig. 16 (b) shows a photograph of the setup. The measured third harmonic tone around 386 GHz, without and with wireless locking enabled, is shown in Fig. 16 (c) and (d), respectively. It should be noted that the spectrum analyzer resolution bandwidth is reduced to 510 kHz in order to highlight the effect of wireless locking. In the unlocked tone, the power is spread across multiple frequency bins. The locked tone is sharp, and all the power is present in a single-frequency bin. The frequency of the injection source is varied, and a double-sided wireless lock range of 42 MHz is measured at the third harmonic.

C. FTIR Measurements

An FTIR spectrometer is used in this work in order to measure the radiation at frequencies beyond 1 THz. A Nicolet 8700 FTIR spectrometer is used in linear scan mode with a room-temperature pyroelectric DTGS detector. This detector has a responsivity of 300 V/W at far-infrared frequencies.

Fig. 17 (a) shows the measurement setup. The chip is placed at the focus of an off-axis parabolic (OAP) mirror. The OAP mirror collimates the beam and sends it to an interferometer inside the FTIR spectrometer. Here, the beam

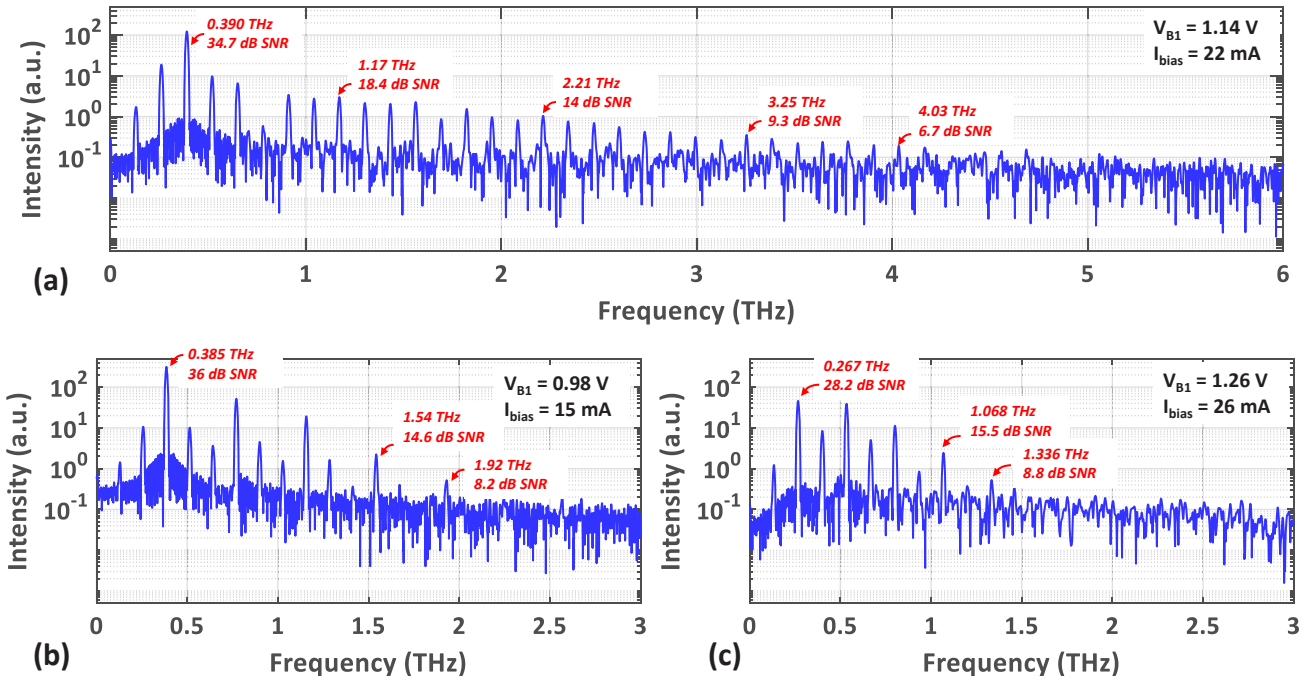

Fig. 18. Intensity spectrum generated from the FTIR spectrometer. These spectra are plotted at bias of (a) V_{B1} = 1.14 V (b) V_{B1} = 0.98 V (c) V_{B1} = 1.26 V

TABLE I
TUNING RANGE FROM FTIR SPECTRUM

Harmonic Index	Frequency (GHz)	Tuning Range (GHz)
3	381 – 403	22
6	761 – 806	45
9	1142 – 1220	78
12	1513 – 1591	78

passes through a beam splitter. One beam is reflected from a stationary mirror, while the other reflects off a scanning mirror, which is controlled through a PC. The reflected beams are then focused on a polarization-insensitive DTGS detector. During this process, interference takes place between the beams. Based on the relative positions of the stationary and the scanning mirror, the beams add up in different phases. For a mono-tone signal, the measured time domain waveform at the detector output would have peaks and nulls separated by a time 't' corresponding to the scanning mirror moving a distance equalling half the wavelength of the signal. This scanning process is repeated over multiple cycles, and the measured time-domain signal is converted to the frequency domain through a Fourier transform. A photograph of the setup used is given in Fig. 17 (b). The measurement is performed at room temperature, and the external beam path is unpurged.

The intensity spectrum is measured at multiple bias points; at each point, 50 interferograms are averaged to produce a spectrum. The interferograms are apodized using a symmetric Happ-Genzel window function, which provides a good tradeoff between spectral resolution and sidelobe suppression. The FTIR spectral resolution is 7.5 GHz. Fig. 18 (a) shows the results for a bias of V_{B1} = 1.14 V. Strong harmonics are present above 1 THz, with all the harmonics of 0.13 THz observable up to 4 THz having an SNR of 34.7, 18.4, 14, 9.3, and 6.7 dB at 0.39, 1.17, 2.21, 3.25, and 4.03 THz, respectively. The SNR is calculated by comparing the spectral peak to the noise floor. Beyond 4.03 THz, although we do see occasional peaks, some of the intermediate harmonics are not detected. The third harmonic at 390 GHz is the strongest, which matches the simulations and the measurements performed with the VDI. Also, note that at at V_{B1}=1.14 V, the circuit draws 22 mA current, which approximately matches the simulated current required for biasing the transistors at peak f_{max}. In Fig. 18 (b), measured at a bias of V_{B1} = 0.98 V, the third, sixth, ninth, twelfth, and fifteenth harmonics at 0.385, 0.77, 1.155, 1.54, 1.925 THz, respectively, are observable. The 1.925 THz has a good SNR of 8.2 dB. In Fig. 18 (c), measured at a bias of V_{B1} = 1.26 V, the even harmonics at multiples of 0.267 THz are strong. It should be noted that only V_{B1} is varied between Fig. 18 (a), (b), (c), and the other biases are unchanged. Changing V_{B1} changes not just the oscillation frequency but also the amount of power that the Colpitts oscillator generates. Because of this, the PIN diode is driven with different powers and thus undergoes reverse recovery at different time instances in its RF drive cycle. This affects the generated waveforms, which can explain the variation in relative strengths of harmonics among Fig. 18 (a), (b), (c). It should also be noted that there is some uncertainty in the relative strengths of the peaks in the FTIR spectrum. The

TABLE II

Reference	**This Work**	[15]	[11]	[12]	[14]	[21]	[16]	[17]	[18]
Highest measured Frequency (THz)	**4.03**	2.45	1.01	0.92	1.85	1.1	2.76	1.64	1.92
Method	**PIN Diode multiplier**	Harmonic Oscillator	Harmonic Oscillator	BJT Frequency Multiplier	Varactor Multiplier	Digital to Impulse	SBD Multiplier	SBD Multiplier	RTD Oscillator
Receiver Used	**Thermal Pyroelectric DTGS Detector**	Liquid Helium Cooled Bolometer	VDI WR1.0 Zero Bias Detector	VDI PM4 Power Meter	VDI WR0.65 Zero Bias Detector	VDI WR1.0 SAX	VDI PM4 Power Meter	VDI PM5 Power Meter	N/A
Locking	**Wireless Locking**	Unlocked	Unlocked	Wired Locking	Wired Locking	Wired Locking	Wired Locking	Wired Locking	Unlocked
RF Input Power (mW)	**0**	0	0	6.3	63	31	500	40	0
DC Power (mW)	**70**	N/A	1100	5.7	0	40	0	0	N/A
Technology	**90nm SiGe BiCMOS**	65nm CMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	65nm CMOS	90nm SiGe BiCMOS	GaAs	GaAs	Si-InP

collection efficiency in FTIR optics is not uniform from 0.4 - 4 THz because of factors such as beam collimation efficiency, atmospheric absorption, attenuation from the mirrors and the beam-splitter, and the variation in DTGS detector responsivity.

Changing the base voltage V_{B1} also varies frequency. The tuning range for the tones at 0.39, 0.78, 1.17, and 1.56 THz are reported in Table I. The tuning ranges are not integer multiples of each other. This is because the frequency resolution of the FTIR interferometer is limited to 7.5 GHz. Also, some higher-order tones are weak and cannot be detected at the edge of the tuning range.

It should be noted that this experiment used a room-temperature DTGS detector. A liquid-helium-cooled bolometer is a more sensitive detector and could be used. The FTIR spectral resolution may also be reduced. This can potentially detect higher-order tones, provided the signal below 1 THz is filtered to prevent the detector saturation.

A comparison with other silicon and compound semiconductor-based radiators above 1 THz is given in Table II. To the best of the author's knowledge, this is the only silicon-based radiator with measures tones beyond 2.5 THz. The other silicon radiators such as [15] use a sensitive liquid helium-cooled bolometer detector and could not still detect tones above 2.5 THz. The THz sources presented in [16] and [17] are waveguide modules designed using GaAs diodes pumped by external GaN amplifiers.

This chip can be used for a variety of sensing applications, such as imaging [21], gas spectroscopy [30], [35], and doppler radar [2]. It can be wirelessly locked to an external reference, and a small resolution bandwidth can be used at the receiver side to maximize the received SNR. The broadband nature of this chip can enable applications such as hyperspectral imaging.

Although the radiated power above 1 THz is less, the PIN diode harmonic generation approach presented here can be adapted to other technologies to generate high power. It should also be noted that the PIN diodes in the GlobalFoundries 9HP process reuse the vertical profile from the NPN transistors. Thus, it is reasonable to assume that as SiGe HBT processes become faster and provide higher f_{max}, the performance of PIN diode multipliers will also improve. PIN diode multipliers can also replace the conventional Schottky diode multipliers in a faster technology such as GaAs or InP to increase the output power.

VI. Conclusion

This paper presents a SiGe BiCMOS PIN diode multiplier capable of generating power from the THz range to the far-infrared range. The reverse recovery of a PIN diode is used in this work, to generate strong higher-order harmonics. A peak EIRP of 13 dBm is measured at 387 GHz, and an EIRP of -3.8 dBm is measured at 782 GHz. An FTIR spectrometer with a room-temperature DTGS detector is used to characterize the higher-order harmonics chip. Measurements show tones up to 4 THz, with the highest tone at 4.03 THz having an SNR of 6.7 dB. Wireless injection locking is also demonstrated in this work, with a lock range of 42 MHz at the third harmonic, around 390 GHz.

Acknowledgments

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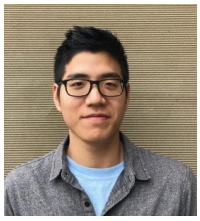

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