UNIVERSITY OF CALIFORNIA, SAN DIEGO

Low noise Millimeter-wave and THz Receivers, Imaging Arrays, Switches in Advanced CMOS and SiGe Processes

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Mehmet Uzunkol

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor James F. Buckwalter
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Lawrence E. Larson

2013

Copyright
Mehmet Uzunkol, 2013
All rights reserved.

The dissertation of Mehmet Uzunkol is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

____

____

____

____

____

Chair

University of California, San Diego

2013

DEDICATION

To my parents, Bekir and Hafize

TABLE OF CONTENTS

Signature Page iii

Dedication iv

Table of Contents v

List of Figures vii

List of Tables xii

Acknowledgements xiii

Vita and Publications xvi

Abstract of the Dissertation xviii

Chapter 1 Introduction 1
1.1 60 GHz Applications 1
1.2 Imaging Systems 2
1.3 Thesis Overview 4

Chapter 2 Design and Analysis of a Low-Power 3–6-Gb/s 55-GHz OOK Receiver With High-Temperature Performance 7
2.1 Introduction 7
2.2 V-band LNA 8
2.3 V-band Detector 10
2.3.1 Design 10
2.3.2 Measurements 14
2.4 V-band OOK Receiver Characterization 15
2.4.1 LNA/Detector 15
2.4.2 BER Measurements 15
2.4.3 Effect of LO Leakage and Power Compression on OOK Detection 21
2.4.4 Effect of Temperature on OOK Receiver Dynamic Range . 24
2.5 Conclusion 25
2.6 Acknowledgement 25

Chapter 3 A Low-NEP 0.32 THz SiGe 4×4 Imaging Array Using High-Efficiency On-chip Antennas 26
3.1 Introduction 26
3.2 Design 29
3.2.1 Antenna Design 29
3.2.2 Detector Design 33
3.2.3 Simulated System Response 36
3.3 Measurements 40

3.4 Discussion 47
3.5 Conclusion 49
3.6 Acknowledgement 49

Chapter 4 60 GHz CMOS Amplifiers, Phase Shifters and Switches 51
4.1 Introduction 51
4.2 A 65-GHz LNA/Phase Shifter with 4.3-dB NF in 45 nm CMOS SOI 52
4.2.1 Design 52
4.2.2 Measurements 56
4.3 A Low-Loss 50–70 GHz SPDT Switch in 90 nm CMOS 58
4.3.1 Design 58
4.3.2 Measurements 61
4.4 Conclusion 63
4.5 Acknowledgement 66

Chapter 5 150–300 GHz Switches, Detectors and Imaging Arrays in 45 nm CMOS SOI 67
5.1 Introduction 67
5.2 140–220 GHz SPST and SPDT Switches in 45 nm CMOS SOI . . . 68
5.2.1 Design 68
5.2.2 Measurements 71
5.3 A Low-Noise 150–210 GHz Detector in 45 nm CMOS SOI 75
5.3.1 Design 75
5.3.2 Measurements 77
5.4 A 0.3 THz 4×4 Cold-FET Imaging Array using Differential High-Efficiency On-chip Antennas in 45 nm CMOS SOI 82
5.4.1 Antenna Design 83
5.4.2 Detector Design 83
5.4.3 Measurements 86
5.5 Conclusion 91
5.6 Acknowledgement 92

Chapter 6 Conclusion 93
6.1 Future Work 96

Appendix A Derivation of the Detector Responsivity 98

Appendix B Derivation of the BER for a Non-ideal OOK Modulation 100

Appendix C Isolation Comparison of Series and Shunt Switches 102
C.1 Without an Inductor 102
C.2 With an Inductor 104

Appendix D Single-Shunt and Double-Shunt Switches 107

Bibliography 112

LIST OF FIGURES

Figure 1.1: Primary applications in 60 GHz ISM band. 2
Figure 1.2: Imaging system architectures: (a) incoherent detection and (b) coherent detection. 3
Figure 1.3: Relation between the system responsivity and inherent detector responsivity. 4

Figure 2.1: OOK receiver system consisting of a SiGe LNA and a detector. 8
Figure 2.2: (a) LNA schematic and (b) G-CPW transmission line ($Z_0 = 60\ \Omega$, all dimensions are in μm). 9
Figure 2.3: Measured LNA (a) gain versus temperature (25–105 °C with 10° steps) and (b) NF versus frequency. 9
Figure 2.4: (a) Detector schematic and large-signal model for nonlinearity analysis. (b) Simulated (using SpectreRF with IBM models) and calculated (using (2.1)) detector open-circuit responsivity versus I_Q. 11
Figure 2.5: Simulated responsivity of the 60 GHz detector with and without the degeneration inductor (L_e = 128 pH). 11
Figure 2.6: Output noise contribution of each component versus frequency and integrated (1 MHz–10 GHz) noise voltage at (a) I_Q = 100 μA and (b) I_Q = 350 μA. 13
Figure 2.7: Integrated output noise voltage (1 MHz–10 GHz) due to R_1 and R_2 versus R_1 at (a) I_Q = 100 μA and (b) I_Q = 350 μA. R_2 values are also changed proportionally for each R_1. 13
Figure 2.8: Measured and simulated S-parameters of the OOK detector. 15
Figure 2.9: (a) Detector output noise voltage measurement setup and (b) measured and simulated detector output noise voltage versus output IF frequency at I_Q = 100 μA and I_Q = 350 μA. 16
Figure 2.10: Measured and simulated detector responsivity, output noise voltage and NEP versus I_Q (f_0 = 60 GHz). The output IF frequency is 500 MHz. . . . 16
Figure 2.11: Measured and simulated detector responsivity and NEP versus frequency at I_Q = 100 μA and I_Q = 350 μA. The output IF frequency is 500 MHz. . . . 17
Figure 2.12: Measured and simulated detector responsivity versus input power. Input P_{1dB} = –20 dBm. 17
Figure 2.13: Microphotograph of the OOK receiver (1.1 $\times$ 0.5 mm^2 including the pads). 18
Figure 2.14: Measured and simulated OOK receiver responsivity and NEP versus (a) I_Q and (b) frequency. The output IF frequency is 500 MHz. 18
Figure 2.15: (a) BER measurement setup and (b) Measured BER versus data rate at a carrier frequency of 55 GHz. 20
Figure 2.16: Measured BER versus (a) input power and (b) temperature at a carrier frequency of 55 GHz. 22
Figure 2.17: (a) OOK modulated waveform. (b) BER versus E_b/N_0 for non-ideal OOK modulation. (c) SNR degradation versus α at a fixed BER. 23
Figure 2.18: Simulated NEP of the (a) detector and (b) OOK receiver versus temperature. 24

Figure 3.1: Imaging front-ends: (a) amplifier-detector, (b) amplifier-mixer, (c) mixer, and (d) detector. 27

Figure 3.2: Antenna radiation methods: a) above-chip, b) below-chip, c) dielectric lens, and d) micro-machining techniques. 27
Figure 3.3: Metal stack-up of the 0.18 μm SiGe BiCMOS process (Jazz SBC18H3). Metal fillings underneath the on-chip antenna and 50 Ω G-CPW transmission line are also shown. All dimensions are in μm. 30
Figure 3.4: Block diagram of the 320 GHz SiGe 4×4 imaging array. 30
Figure 3.5: (a) Metal-fill cases (Oxide/Polymide/Nitride and Quartz layers are not shown) and (b) on-chip single-ended slot antenna with the metal-fill underneath the antenna. 31
Figure 3.6: Simulated on-chip elliptical slot-ring antenna S_{11} for different metal-fill cases. 31
Figure 3.7: Simulated on-chip elliptical slot-ring antenna (a) efficiency and (b) gain for different metal-fill cases. 32
Figure 3.8: (a) Conventional and (b) proposed detector design, and (c) equivalent circuit model. Biasing circuit is not shown. 34
Figure 3.9: Simulated responsivity at 360 GHz versus (a) detector bias current (I_Q) for the conventional/proposed designs and (b) transmission line electrical length (θ) for the proposed design at I_Q = 100 μA. 34
Figure 3.10: Simulated detector S_{11} versus frequency for different L_E at I_Q = 100 μA. . 35
Figure 3.11: Simulated detector responsivity, noise and NEP at 360 GHz versus I_Q for different L_E. 35
Figure 3.12: Schematic of the (a) complete detector, and (b) buffer and opamp. 36
Figure 3.13: Microphotograph of the chip (2.6×2.6 mm^2) and a blow-up view of a single pixel (0.41×0.3 mm^2). 37
Figure 3.14: Simulated S_{11} of the detector and opamp. 38
Figure 3.15: Simulated responsivity of the detector and opamp versus frequency at $I_Q =$ 100 μA. System responsivity ($\Re_s$) including the antenna efficiency is also shown. 39
Figure 3.16: Simulated NEP of the detector alone and detector + amp. + mux. versus IF frequency at 360 GHz and I_Q = 100 μA. 39
Figure 3.17: Simulated responsivity and NEP of the detector and opamp versus I_Q at 320 and 360 GHz. System responsivity/NEP including the antenna efficiency is shown with a subscript (i.e. $\Re_s$ and NEP$_s$). 40
Figure 3.18: Measurement setup (a) block diagram and (b) photograph with inset of mounted imaging array chip on printed circuit board. 42
Figure 3.19: (a) Measured output power of VDI AMC-334 multiplier chain module, and (b) measured and calculated WR-3.4 horn antenna gain. 43
Figure 3.20: Measured responsivity versus frequency of a single pixel at $I_Q = 100$ μA. 44
Figure 3.21: Measured and simulated output noise voltage versus freqeuency at $I_Q =$ 100 μA and versus I_Q at IF = 100 kHz. 44
Figure 3.22: Measured and simulated H-plane antenna patterns at 315 GHz with (a) quartz (4 channels) and (b) without quartz (2 channels). (c) Measured X-pol of the slot-ring antenna with quartz versus frequency at $\theta = 0$. 45
Figure 3.23: Measured (a) responsivity and (b) NEP versus I_Q with and without a quartz superstrate at 316 GHz (IF = 100 kHz). 46

Figure 3.24: Measured responsivity versus channel and incidence angle at $I_Q = 100\ \mu$A at 316 GHz for four detectors in a single row. 47

Figure 4.1: Schematic of the V-band (a) LNA and (b) 3-bit phase shifter. 53
Figure 4.2: Equivalent circuit model of the 45°/90° phase shifters in the (a) bypass and (b) phase-delay states. 53
Figure 4.3: Microphotograph of the LNA/phase shifter. 54
Figure 4.4: Measured and simulated (a) phase difference and (b) gain of 180° and 45° phase shifter test-cells. 55
Figure 4.5: Measured S_{11}, S_{22}, S_{21}, relative phase, rms phase error and rms gain error of the 3-bit phase shifter. 55
Figure 4.6: Measured and simulated input P_{1dB} of the 3-bit phase shifter versus (a) frequency and (b) phase state. 56
Figure 4.7: Measured (a) gain and (b) noise figure of the LNA/phase shifter for different phase states. The red curve is the average of all phase states. 56
Figure 4.8: (a) Schematic of SPDT switch; (b) cross-sectional view and layout of the transistor. Dimensions are in micrometers. 59
Figure 4.9: (a) Simulated insertion loss, isolation at 60 GHz and bandwidth versus transistor size; (b) inductance and stub length versus transistor size; (c) insertion loss and isolation at 60 GHz versus Z_0 of the $\lambda/4$ line. 60
Figure 4.10: Impedance transformation of the $\lambda/4$-based SPDT switch. 62
Figure 4.11: Microphotograph of SPDT switch. The size is 0.5 $\times$ 0.55 mm^2, not including the pads. 62
Figure 4.12: Measured and simulated (a) return loss, (b) insertion loss, (c) isolation of the SPDT switch. 64
Figure 4.13: Measured IIP3 of the SPDT switch at 60 GHz. 65
Figure 4.14: Simulated switching time performance of the SPDT switch versus R_gate at 60 GHz. 65

Figure 5.1: (a) Metal stack-up and 50 Ω grounded co-planar waveguide (GCPW) transmission line dimensions (not to scale), (b) Cross-section of the transistor in a 45-nm CMOS SOI process. 69
Figure 5.2: Transistor connections. 70
Figure 5.3: Simulated insertion loss and isolation of series and shunt switches vs. transistor width at 180 GHz. 70
Figure 5.4: Schematic of (a) SS-SPST (b) DS-SPST and (c) SPDT switches. 72
Figure 5.5: Chip photo of (a) SS-SPST (0.45$\times$0.35 mm^2), (b) DS-SPST (0.45$\times$0.45 mm^2), (c) SS-SPDT (0.55$\times$0.45 mm^2), (d) DS-SPDT (0.53$\times$0.55 mm^2) switches, all including the pads. 72
Figure 5.6: Measured and simulated return loss, insertion loss and isolation of (a) SS-SPST and (b) DS-SPST switches. 73
Figure 5.7: Measured and simulated return loss, insertion loss and isolation of (a) SS-SPDT and (b) DS-SPDT switches. 74
Figure 5.8: Schematic of the 150–210 GHz detector. 76
Figure 5.9: Cross-section of the 45 nm CMOS SOI process and 50 Ω G-CPW transmission line (dimensions are not to scale). 76

Figure 5.10: Microphotograph of the detector. The chip size is 0.45 $\times$ 0.45 mm^2 including the pads. 78
Figure 5.11: Measured and simulated detector S_{11} and S_{21} at I_{DC} = 200 μA. 78
Figure 5.12: Measured and simulated detector responsivity versus (a) V_{GS} and (b) I_{DC} at 170 GHz. 79
Figure 5.13: Measured and simulated detector responsivity versus frequency at I_{DC} = 200 μA. 79
Figure 5.14: Noise measurement setup for (a) lower IF frequencies (< 1 MHz) and (b) higher IF frequencies (> 0.1 MHz). (c) Measured and simulated output noise voltage versus IF frequency at I_{DC} = 200 μA. 80
Figure 5.15: Measured and simulated detector output noise voltage versus I_{DC} at an IF frequency of 10 kHz, 100 kHz and 10 MHz. 80
Figure 5.16: Measured and simulated detector NEP versus (a) I_{DC} at an IF frequency of 10 kHz, 100 kHz and 1 MHz, (b) RF frequency at I_{DC} = 200 μA and an IF frequency of 10 MHz. 81
Figure 5.17: (a) Metal-fill cases and (b) on-chip differential slot antenna with the metal-fill underneath the antenna. 84
Figure 5.18: Simulated on-chip antenna S_{11} for different metal-fill cases. 84
Figure 5.19: Simulated on-chip antenna (a) efficiency and (b) gain for different metal-fill cases. 85
Figure 5.20: Schematic of the single element of 4×4 CMOS imaging array. 86
Figure 5.21: Microphotgraph of the 4×4 CMOS imaging array chip and zoomed view of the board showing the bondwires. 87
Figure 5.22: Block diagram of the responsivity and antenna pattern measurement setup. 87
Figure 5.23: Measured responsivity versus frequency of a single pixel at $V_{GS} = 250$ mV. 88
Figure 5.24: Measured responsivity versus V_{GS} of a single pixel at 300 GHz. 88
Figure 5.25: Measured and simulated output noise voltage of a single pixel versus frequency at $V_{GS} = 250$ mV and versus V_{GS} at IF = 100 kHz. 89
Figure 5.26: Measured NEP of a single pixel versus frequency at $V_{GS} = 250$ mV and versus V_{GS} at 300 GHz, both for IF = 100 kHz. 90
Figure 5.27: Measured and simulated H-plane antenna patterns of a single element at 295, 300 and 305 GHz with quartz superstrate. 91

Figure 6.1: Schematic of the single element of the 1 THz 4×4 CMOS imaging array. 95
Figure 6.2: Simulated on-chip antenna gain for 3 different quartz superstrate thicknesses. 95
Figure 6.3: Microphotograph of the 1 THz 4×4 CMOS imaging array and zoomed view of the board showing the bondwires. 97

Figure B.1: BER versus E_b/N_0 for coherent and noncoherent OOK modulation. 101

Figure C.1: (a) Equivalent simple model for a transistor switch in the on and off states; (b) Series switch; (c) Shunt switch. 103
Figure C.2: (a) Series switch with an inductor for isolation and (b) shunt switch with an impedance matching inductor. R_1 and R_2 are the parasitic resistances due to inductor Q. 105

Figure C.3: Simulated (a) insertion loss and (b) isolation of the series and shunt switches with inductors. 106

Figure D.1: (a) Single-shunt switch and its on/off-state equivalent models; (b) double-shunt switch and its on/off-state equivalent models. 108
Figure D.2: Schematic of (a) SS, (b) DS, (c) 4S and (d) 8S switches. 110
Figure D.3: Simulated (a) S_{11}, (b) insertion loss and (c) isolation of the SS, DS, 4S and 8S switches. 111

LIST OF TABLES

Table 3.1: Performance Summary 48
Table 3.2: Sources of Error in Measurements 49

Table 4.1: LNA/Phase Shifter Comparison 57
Table 4.2: SPDT Switch Comparison 66

Table 5.1: Detector Comparison 82
Table 5.2: Performance Summary 92

ACKNOWLEDGEMENTS

This dissertation would not have been possible without the help and support of many people. First, I would like to thank my advisor, Prof. Gabriel Rebeiz. He has invested enormous amount of time in my technical training and his guidance has always been valuable. His motivation and enthusiasm has inspired me to pursue further analysis and understand complex problems. I especially appreciate having the opportunity to do measurements in a cutting edge research lab, where we have several equipments all the way up to THz frequency range. Aside from his great technical knowledge and expertise, I also admire his leadership and managerial skills as well as his sense of humor. He has taught so many lessons that I believe will guide me for the rest of my life: how to behave in a professional environment, how to give a nice presentation, how to write a good technical paper. It has been a great pleasure and honor working with him.

Next, I would like to thank my dissertation committee members, Prof. Larry Larson, Prof. James F. Buckwalter, Prof. Gert Cauwenberghs and Prof. William Hodgkiss for their time, interest, and valuable comments about my research.

I would also like to thank Prof. Yasar Gurbuz at Sabanci University, Istanbul, Turkey, who encouraged me to do a Ph.D. in the U.S.

I want to thank my co-authors: Ozan Dogan Gurbuz, Woorim Shin, Fatih Golcuk and Jennifer M. Edwards. Especially, Ozan and Jen did a great job in designing the on-chip antennas in the imaging arrays. Woorim designed the 60 GHz SiGe LNA in the OOK receiver. Fatih provided his opamp and I re-used it in the SiGe imaging array. I also want to thank Dr. Andy Fung from NASA Jet Propulsion Laboratory for his help in 180 GHz switch and detector measurements.

Special thanks to the Sabanci Mafia: Berke Cetinoneri, Yusuf A. Atesal and Ozgur Inac. I shared the same house with them for several years. Their friendship and support has been invaluable. The kitchen table and the patio were the places where I have most of the memories: long weekend breakfasts and exciting soccer games, various TV series and movies, long discussions about pretty much everything.

I also want to thank my close friends who also have made my life in San Diego more enjoyable: Mehmet Parlak, Fatih Golcuk and Tufan Gokirmak for all the fun events and coffee breaks at the Scripts Inst. of Oceanography with a magnificent ocean view.

There are many people in the TICS group that I would like to acknowledge here for their support and friendship: Woorim Shin, Donghyup Shin, Chirag Patel, Romain Stefanini,

Kwang-Jin Koh, Michael Chang, Mohammed El-Tanani, Tiku Yu, Jason May, Isak Reines, Alex Grichener, Dong-Woo Kang, Sang-Young Kim, Bon-Hyun Ku, Ramadan Alhalabi, Jennifer M. Edwards, Kevin Ho, Ozan Dogan Gurbuz, Seyhmus Cacina, Tumay Kanar, Bilgehan Avser, Samet Zihir, Yu-Chin Ou, Choul-Young Kim, Yi-Chyun Chiou, Chih-Chieh Cheng, Rashed Mahameed, Hojr Sedaghat Pisheh, Hosein Zareie, Chenhui Niu, Chih-Hsiang Ko, Yang Yang, Hsin-Chang Lin, Hong-Ming Lee, Tao Yang.

The support and encouragement of my parents, Bekir and Hafize Uzunkol, was a great contributor in completing my Ph.D. degree. I can never forget their support, dedication and unending love throughout my life.

The material in this dissertation is based on the following papers which are either published, or has been submitted for publication.

Chapter 2 is based on and mostly a reprint of the following paper:

- M. Uzunkol, W. Shin, and G. M. Rebeiz, ”Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance,” IEEE Trans. Microwave Theory and Tech., vol. 60, no. 10, pp. 3263-3271, Oct. 2012.

Chapter 3 is based on and mostly a reprint of the following paper:

- M. Uzunkol, O. D. Gurbuz, F. Golcuk, and G. M. Rebeiz, ”A low-NEP 0.32 THz SiGe 4×4 imaging array using high-efficiency on-chip antennas,” submitted for publication in IEEE Journal of Solid-State Circuits, Nov. 2012.

Chapter 4 is based on and mostly a reprint of the following papers:

- M. Uzunkol, and G. M. Rebeiz, ”A 65 GHz LNA/phase shifter with 4.3 dB using 45 nm CMOS SOI,” IEEE Microwave and Wireless Comp. Lett., vol. 22, no. 10, pp. 530-532, Oct. 2012,
- M. Uzunkol, and G. M. Rebeiz, ”A low-loss 50-70 GHz SPDT switch in 90 nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 45, no. 10, pp. 2003-2007, Oct. 2010.

Chapter 5 is based on and mostly a reprint of the following papers:

- M. Uzunkol, and G. M. Rebeiz, ”140-220 GHz SPST and SPDT switches in 45 nm CMOS SOI,” IEEE Microwave and Wireless Comp. Lett., vol. 22, no. 8, pp. 412-414, Aug. 2012.
- M. Uzunkol, and G. M. Rebeiz, ”A low-noise 150-210 GHz detector in 45 nm CMOS SOI,” submitted for publication in IEEE Microwave and Wireless Comp.

Lett., Jan. 2013.

- M. Uzunkol, Jennifer M. Edwards, and G. M. Rebeiz, "A 0.3 THz 4×4 imaging array using differential high-efficiency on-chip antennas in 45 nm CMOS SOI," submitted for publication in IEEE Microwave and Wireless Comp. Lett., Mar. 2013.

The dissertation author was the primary author of the work in these chapters, and coauthors (Prof. Gabriel M. Rebeiz, Dr. Jennifer M. Edwards, Mr. Woorim Shin, Mr. Fatih Golcuk, and Mr. Ozan D. Gurbuz) have approved the use of the material for this dissertation.

Mehmet Uzunkol
La Jolla, California
March, 2013.

VITA AND PUBLICATIONS

2003 - 2007	B. S. in Microelectronics Engineering, Sabanci University, Istanbul, Turkey
2007 - 2009	M. S. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego, La Jolla, California
2009 - 2013	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego, La Jolla, California

M. Uzunkol, O. D. Gurbuz, F. Golcuk, and G. M. Rebeiz, ”A low-NEP 0.32 THz SiGe 4×4 imaging array using high-efficiency on-chip antennas,” *IEEE Journal of Solid-State Circuits*, submitted for publication, November 2012.

M. Uzunkol, J. M. Edwards, and G. M. Rebeiz, ”A 0.3 THz 4×4 cold-FET imaging array using differential high-efficiency on-chip antennas in 45 nm CMOS SOI,” *IEEE Microwave and Wireless Comp. Lett.*, submitted for publication, March 2013.

M. Uzunkol, and G. M. Rebeiz, ”A low-noise 150-210 GHz detector in 45 nm CMOS SOI,” *IEEE Microwave and Wireless Comp. Lett.*, submitted for publication, January 2013.

M. Uzunkol, W. Shin, and G. M. Rebeiz, ”Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance,” *IEEE Trans. Microwave Theory and Tech.*, vol. 60, no. 10, pp. 3263-3271, October 2012.

M. Uzunkol, and G. M. Rebeiz, ”A 65 GHz LNA/phase shifter with 4.3 dB using 45 nm CMOS SOI,” *IEEE Microwave and Wireless Comp. Lett.*, vol. 22, no. 10, pp. 530-532, October 2012.

M. Uzunkol, and G. M. Rebeiz, ”140-220 GHz SPST and SPDT switches in 45 nm CMOS SOI,” *IEEE Microwave and Wireless Comp. Lett.*, vol. 22, no. 8, pp. 412-414, August 2012.

M. Uzunkol, F. Golcuk, B. Cetinoneri, Y. A. Atesal, O. D. Gurbuz, J. M. Edwards, and G. M. Rebeiz, ”Millimeter-wave and terahertz sources and imaging systems based on 45nm CMOS technology,” *IEEE Int. Microwave Symp. Dig.*, pp. 1-3, June 2012.

M. Uzunkol, J. W. May, and G. M. Rebeiz, ”Design and characterization of a SiGe RFICs for millimeter-wave radiometers,” *IEEE Int. Microwave Symp. Dig.*, pp. 1-3, June 2012.

O. Inac, B. Cetinoneri, M. Uzunkol, Y. A. Atesal, and G. M. Rebeiz, ”Millimeter-wave and THz circuits in 45-nm SOI CMOS,” *IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 1-4, Oct. 2011.

M. Uzunkol, and G. M. Rebeiz, ”A low-loss 50-70 GHz SPDT switch in 90 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 10, pp. 2003-2007, October 2010.

W. Shin, M. Uzunkol, and Gabriel M. Rebeiz, ”60 GHz low power 1.5 Gb/s ASK transmitter in 90 nm CMOS with on-board Yagi-Uda antenna,” *IIEEE European Microwave Conference*, pp. 272-275, Oct. 2010.

G. M. Rebeiz, J. W. May, M. Uzunkol, W. Shin, O. Inac and M. Chang, ”Towards high performance 100 GHz SiGe and CMOS circuits,” *IEEE Int. Microwave Symp. Dig.*, pp. 1-4, June 2010.

M. Uzunkol, and G. M. Rebeiz, ”Ultra Low-Loss 50-70 GHz SPDT Switch in 90 nm CMOS,” *IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 1-4, Oct. 2009.

W. Shin, M. Uzunkol, and G. M. Rebeiz, ”Ultra Low Power 60 GHz ASK SiGe Receiver with 3-6 GBPS Capabilities,” *IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 1-4, Oct. 2009.

ABSTRACT OF THE DISSERTATION

Low noise Millimeter-wave and THz Receivers, Imaging Arrays, Switches in Advanced CMOS and SiGe Processes

by

Mehmet Uzunkol

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Gabriel M. Rebeiz, Chair

The thesis presents advanced millimeter-wave and THz receivers, imaging arrays, detectors and switches in CMOS and SiGe BiCMOS technologies. First, an in-depth analysis of a SiGe BiCMOS on-off keying (OOK) receiver composed of a low noise SiGe amplifier and an OOK detector is presented. The analysis indicates that the bias circuit and bias current have a substantial impact on the receiver and should be optimized for best performance. Also, the LO leakage from the transmitter can have a detrimental impact on the receiver sensitivity and should be minimized for best performance. The receiver consumes 11 mW, has a noise equivalent power (NEP) of 5–10 fW/Hz$^{1/2}$ at 55 GHz, and an instantaneous dynamic range of 27–30 dB. The OOK receiver achieves 6 Gb/s communication with a bit-error rate (BER) $< 10^{-12}$ at room temperature. Operation is also demonstrated up to 105 °C at 3 Gb/s with a BER $< 10^{-12}$.

Next, a 0.32 THz 4×4 imaging array based on an advanced SiGe technology (Jazz

SBC18H3) is presented. Each pixel is composed of a high efficiency on-chip antenna meeting all metal-density rules, which is coupled to a SiGe detector and a low noise CMOS operational amplifier. The array results in an average NEP of 34 pW/Hz$^{1/2}$ for a detector bias current of 50–150 μA, a responsivity of 18 kV/W and a 3-dB bandwidth of 25 GHz. The power consumption is 2.4 mW/pixel. Extensive measurements are presented which show the challenges encountered in obtaining accurate measurements at THz frequencies, and the decisions taken to quote the average NEP values.

A high performance 0.3 THz 4×4 imaging array in a 45 nm silicon-on-insulator (SOI) CMOS technology is also presented. The single element of the array is composed of a high-efficiency on-chip antenna meeting all metal-density rules, which is coupled to a differential detector and a low noise CMOS IF amplifier. The array results in an NEP of 100 pW/Hz$^{1/2}$, a responsivity of 1.8–2.0 kV/W with a 3-dB bandwidth of 20 GHz. The power consumption is 3.6 mW/pixel. These values are competitive with the best CMOS THz imaging arrays to-date.

For 60 GHz applications, a 45 nm CMOS SOI LNA/phase shifter and an ultra low-loss single-pole double-throw (SPDT) switch in a 90 nm CMOS process are presented. The 3-bit phase shifter is designed using a switched-LC approach and results in only 6 dB loss at 65 GHz. The LNA/phase shifter front-end results in a gain of 6.5 dB, a noise figure of 4.3 dB, and an input P_{1dB} of –13.5 dBm (limited by the amplifier) with a power consumption of 15 mW. This work shows that advanced CMOS processes are essential for low power, medium linearity 60 GHz phased arrays. The SPDT switch is based on $\lambda/4$ transmission lines with shunt inductors at the output matching network. The switch results in a measured insertion loss of 1.5–1.6 dB at 53–60 GHz and $<$ 2.0 dB at 50–70 GHz. The measured isolation is $>$ 25 dB, and the output port-to-port isolation is $>$ 27 dB at 50–70 GHz. The measured P_{1dB} is 13.5 dBm with a corresponding IIP3 of 22.5 dBm at 60 GHz. The return loss is better than –8 dB at 50–70 GHz. The active chip area is 0.5×0.55 mm^2 and can be reduced in future designs by folding the on $\lambda/4$ transmission lines. When this work was published, it presented the lowest insertion loss 60 GHz SPDT in any CMOS technology to-date.

140–220 GHz single-pole single-throw (SPST) and single-pole double-throw (SPDT) switches built using 45 nm semiconductor-on-insulator (SOI) CMOS technology are presented. A tuned-shunt topology is used to minimize the insertion loss, and the transistor layout results in very low ground inductance and high isolation. The double-shunt SPST switch results in an insertion loss of 1.0 dB and an isolation of 20 dB, while the SPDT switches result in an insertion loss of 3.0 dB and an isolation of 20–25 dB, all at 180 GHz. The switches are well

matched with a return loss at all ports greater than 10 dB at 140–220 GHz. The work shows that advanced CMOS nodes can be used for transmit-receive switches in emerging 140–220 GHz CMOS systems.

A G-band (140–220 GHz) detector in a 45 nm silicon-on-insulator (SOI) CMOS technology is presented. The measured detector responsivity is 3 kV/W at 170–180 GHz with a 3-dB bandwidth of 150–210 GHz. The detector results in an NEP of 8–10 pW/Hz$^{1/2}$ at a bias current of 50–200 μA for an IF of 10 MHz and is well matched with an input return loss $>$ 10 dB at 167–194 GHz. The responsivity and NEP values are close to the best SiGe detectors, and show that advanced CMOS nodes are suitable for $\sim$200 GHz imaging arrays.

Chapter 1

Introduction

1.1 60 GHz Applications

Recent advances in silicon technologies have made it possible to build high performance transceivers operating at millimeter-wave frequencies, including the 57–64 GHz Industrical, Scientific and Medical (ISM) band [1–4]. This 7 GHz wide bandwidth is very attractive in order to achieve high data-rate wireless communications. However, due to higher path loss (68 dB/m) and atmospheric loss, the 60 GHz band is mostly suitable for short-range applications ($\sim$10 m) and point-to-point communication link is necessary unless a phased-array transceiver topology is considered. Fig. 1.1 presents the primary applications such as transferring uncompressed high-definition (HD) video from a set-top box to a display screen and downloading media contents from a kiosk to a portable hand-held device. Note that these applications require a relatively controlled environment (i.e. within a room in a house or an office space), and therefore there are no stringent interference specifications like in cell-phone bands. Modulation scheme choice is an important criteria in terms of achieving high spectral efficiency, low-cost and low-power systems. Modulation schemes such as binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), and 16 quadrature amplitude (QAM) are attractive for higher data-rates. However, they require local oscillators (LOs), dividers and phase-locked loops (PLLs), which can be power hungry especially at high temperatures. The on-off keying (OOK) modulation scheme, while spectrally inefficient, allows for a low power architecture since receivers do not employ LOs, and transmitters generally use a free-running LO without a divider/PLL circuit. Therefore, the OOK modulation scheme is especially advantageous for mobile applications which seek low-power and low-cost solutions. The OOK system results in lowest power consumption, but has

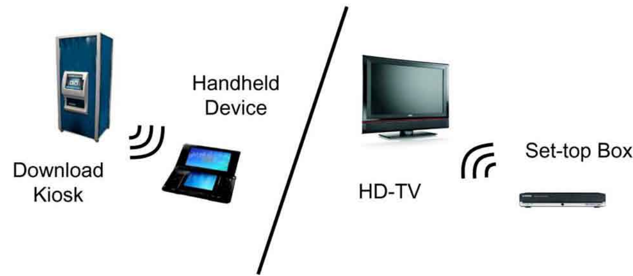


Figure 1.1: Primary applications in 60 GHz ISM band.

limited dynamic range and virtually no immunity to interferences. The interference issue could easily be alleviated due to the low possibility of having more than one pair of 60 GHz communication link within a short range. The dynamic range of OOK transceiver depends on the receiver noise floor, target bit-error rate and system bandwidth. Also the dynamic range could be improved by using variable gain amplifiers. On top of that, if the OOK system is operated with directional antennas (G $>$ 10 dB), it becomes highly advantageous for increasing the range and avoiding interferences.

1.2 Imaging Systems

The imaging systems are typically implemented using either a coherent or an incoherent detection [5]. The coherent detection is based on a square-law detector, and an optional pre-amplification before the detector; whereas the incoherent detection is based on a down-conversion mixer and an optional pre-amplification before the mixer (Fig. 3.1). These systems are either wave-guide based or antenna-coupled using high-efficiency planar antennas, and results in a noise-equivalent power (NEP) of fW-pW/Hz$^{1/2}$ over a wide bandwidth (10–30 GHz). The incoming radiation from the target could be a thermal emission or a transmitted power from the sensor itself, and is rectified from THz to baseband using the afore-mentioned receiver architectures. The imaging systems which are based on the thermal emission (black-body radiation) are passive imaging systems, and they typically require a pre-amplification. This results in a lower noise floor which is essential to achieve less than 1 K temperature resolution. On the other hand, the LNA requirement limits the operating frequency of passive imaging systems due to finite f_t/f_{max}. Therefore, $>$ 200–300 GHz imaging systems typically require the use of an active illuminator (active imaging system) so as to obtain acceptable signal-to-noise ratios. Recently,

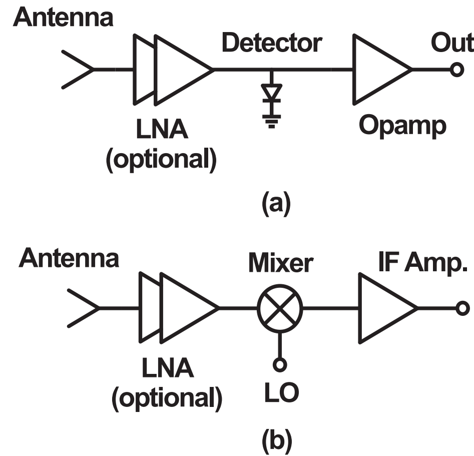


Figure 1.2: Imaging system architectures: (a) incoherent detection and (b) coherent detection.

there has been a lot of interest in using SiGe and CMOS technologies for THz imaging arrays. SiGe-based radiometers were demonstrated at 100–165 GHz with an NEP of 2–10 fW/Hz$^{1/2}$, which is competitive with the best III-V tecnologies [6–9]. Due to the lack of low-noise high-gain amplifiers in silicon technologies operating at $>$ 200 GHz, the active imaging systems with antenna coupled detectors are used and an NEP of 30–100 pW/Hz$^{1/2}$ were reported at 300–1000 GHz [10–13].

The NEP is one of the most important figure of merit for the imaging systems, and is dependent on the antenna efficiency and inherent detector NEP. Assuming a plane wave with a power density S is incident on the antennas, the system responsivity and NEP are defined as:

$$S = \frac{P_t G_t}{4\pi R^2} \tag{1.1}$$

$$P_{available} = S \times A_{physical} \tag{1.2}$$

$$\Re_s = \frac{V_{OUT}}{P_{available}} \tag{1.3}$$

$$NEP_s = \frac{V_n}{\Re_s} \tag{1.4}$$

where P_t is the transmit power, G_t is the transmit antenna gain, R is the distance between the transmitter and the imaging array, and $A_{physical}$ is the antenna aperture. Also, as illustrated in Fig. 1.3, the system responsivity ($\Re_s$) and NEP (NEP_s) can be related to the inherent detector responsivity($\Re$) and NEP by multiplying with the antenna efficiency (ϵ).

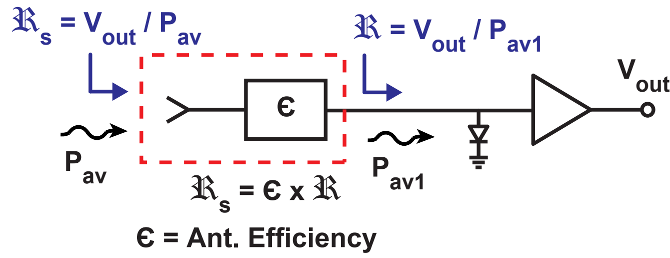


Figure 1.3: Relation between the system responsivity and inherent detector responsivity.

$$\Re_s = \epsilon \times \Re \tag{1.5}$$

$$NEP_s = \epsilon \times NEP \tag{1.6}$$

1.3 Thesis Overview

The thesis presents advanced millimeter-wave and THz receivers, imaging arrays, detectors, switches, and LNA/phase shifters in CMOS and SiGe BiCMOS technologies at 60–300 GHz.

Chapter 2 presents an in-depth analysis of a SiGe BiCMOS on-off keying (OOK) receiver composed of a low noise SiGe amplifier and an OOK detector is presented. The analysis indicates that the bias circuit and bias current have a substantial impact on the receiver and should be optimized for best performance. Also, the LO leakage from the transmitter can have a detrimental impact on the receiver sensitivity and should be minimized for best performance. The receiver consumes 11 mW, has a noise equivalent power (NEP) of 5–10 fW/Hz$^{1/2}$ at 55 GHz, and an instantaneous dynamic range of 27–30 dB. The OOK receiver achieves 6 Gb/s communication with a bit-error rate (BER) $< 10^{-12}$ at room temperature. Operation is also demonstrated up to 105 °C at 3 Gb/s with a BER $< 10^{-12}$.

Chapter 3 presents a 0.32 THz 4×4 imaging array based on an advanced SiGe technology (Jazz SBC18H3) is presented. Each pixel is composed of a high efficiency on-chip antenna meeting all metal-density rules, which is coupled to a SiGe detector and a low noise CMOS operational amplifier. The array results in an average NEP of 34 pW/Hz$^{1/2}$ for a detector bias current of 50–150 μA, a responsivity of 18 kV/W and a 3-dB bandwidth of 25 GHz. The power consumption is 2.4 mW/pixel. Extensive measurements are presented which show the challenges

encountered in obtaining accurate measurements at THz frequencies, and the decisions taken to quote the average NEP values.

Chapter 4 presents a 45 nm CMOS SOI LNA/phase shifter and an ultra low-loss single-pole double-throw (SPDT) switch in a 90 nm CMOS process for 60 GHz applications. The 3-bit phase shifter is designed using a switched-LC approach and results in only 6 dB loss at 65 GHz. The LNA/phase shifter front-end results in a gain of 6.5 dB, a noise figure of 4.3 dB, and an input P_{1dB} of –13.5 dBm (limited by the amplifier) with a power consumption of 15 mW. This work shows that advanced CMOS processes are essential for low power, medium linearity 60 GHz phased arrays. The SPDT switch is based on $\lambda/4$ transmission lines with shunt inductors at the output matching network. The switch results in a measured insertion loss of 1.5–1.6 dB at 53–60 GHz and $<$ 2.0 dB at 50–70 GHz. The measured isolation is $>$ 25 dB, and the output port-to-port isolation is $>$ 27 dB at 50–70 GHz. The measured P_{1dB} is 13.5 dBm with a corresponding IIP3 of 22.5 dBm at 60 GHz. The return loss is better than –8 dB at 50–70 GHz. The active chip area is 0.5×0.55 mm^2 and can be reduced in future designs by folding the on $\lambda/4$ transmission lines. When this work was published, it presented the lowest insertion loss 60 GHz SPDT in any CMOS technology to-date.

Chapter 5 presents 140–220 GHz single pole single throw (SPST) and single pole double throw (SPDT) switches, A G-band (140–220 GHz) detector and a high performance 0.3 THz 4×4 imaging array, all in a 45 nm silicon-on-insulator (SOI) CMOS technology. A tuned-shunt topology is used to minimize the insertion loss, and the transistor layout results in very low ground inductance and high isolation. The double-shunt SPST switch results in an insertion loss of 1.0 dB and an isolation of 20 dB, while the SPDT switches result in an insertion loss of 3.0 dB and an isolation of 20–25 dB, all at 180 GHz. The switches are well matched with a return loss at all ports greater than 10 dB at 140–220 GHz. The work shows that advanced CMOS nodes can be used for transmit-receive switches in emerging 140–220 GHz CMOS systems. The measured G-band detector responsivity is 3 kV/W at 170–180 GHz with a 3-dB bandwidth of 150–210 GHz. The detector results in an NEP of 8–10 pW/Hz$^{1/2}$ at a bias current of 50–200 μA for an IF of 10 MHz and is well matched with an input return loss $>$ 10 dB at 167–194 GHz. The responsivity and NEP values are close to the best SiGe detectors, and show that advanced CMOS nodes are suitable for $\sim$200 GHz imaging arrays. The single element of the 0.3 THz 4×4 array is composed of a high-efficiency on-chip antenna meeting all metal-density rules, which is coupled to a differential detector and a low noise CMOS IF amplifier. The array results in an NEP of 100 pW/Hz$^{1/2}$, a responsivity of 1.8–2.0 kV/W with a 3-dB bandwidth of 20 GHz.

The power consumption is 3.6 mW/pixel. These values are competitive with the best CMOS THz imaging arrays to-date.

The thesis concludes with a summary of the work and suggestions for future work.

Chapter 2

Design and Analysis of a Low-Power 3–6-Gb/s 55-GHz OOK Receiver With High-Temperature Performance

2.1 Introduction

Millimeter-wave communication systems at 60 GHz offer the possibility of a wide spectral bandwidth that allows for Gbps communication links [1]. Several designs have been demonstrated recently using BPSK, QPSK and 16 QAM modulation [2–4], but these require local oscillators, dividers, and PLLs, which can be power hungry especially when operated at high temperatures. The OOK modulation scheme, while spectrally inefficient, allows for a very low power architecture since receivers do not employ a local oscillators, and transmitters generally use a free-running LO without a divider/PLL circuit. Several OOK receivers, transmitters and transceivers have been demonstrated recently using SiGe and advanced CMOS nodes and with good performance [14–20]. However, none of these papers have presented an in-depth analysis of these systems showing their ultimate sensitivity and limitations. Also, to the authors' knowledge, none of the published systems have shown Gb/s operation up to 105 °C.

This chapter presents an expanded and in-depth analysis of an OOK receiver [15], together with analysis showing the noise due to the bias circuit, NEP versus bias current, instantaneous dynamic range, ultimate sensitivity, and the effect of transmitter local oscillator leakage on the receiver sensitivity. The receiver consists of an LNA followed by an OOK detector (Fig. 2.1). It is shown that an NEP of 5–10 fW/Hz$^{1/2}$ can be achieved at 55 GHz using an advanced

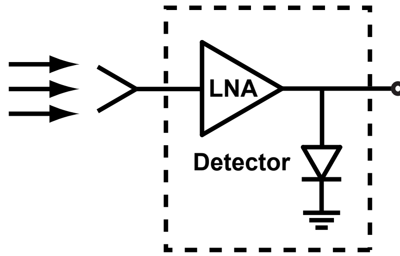


Figure 2.1: OOK receiver system consisting of a SiGe LNA and a detector.

SiGe BiCMOS technology, which results in an OOK receiver dynamic range of 27–30 dB. The OOK receiver is tested versus different input power levels and can achieve 6 Gb/s communication with a BER $< 10^{-12}$ at room temperature. Also, operation is demonstrated up to 105 °C at 3 Gb/s with a BER $< 10^{-12}$.

2.2 V-band LNA

The LNA and OOK detector are fabricated in a 0.12-μm SiGe BiCMOS technology (IBM8HP) with 7 metal layers [21]. This process has 0.12-μm SiGe HBTs with an f_t of 180–200 GHz and 0.12-μm CMOS transistors with an f_t of 90–100 GHz, but the CMOS transistors are not used. Grounded coplanar-waveguide (G-CPW) transmission lines with dimensions of 11/12/11 μm (Z_0 = 50 Ω) are implemented in the top 3 metal layers, with a simulated loss of 0.55 dB/mm at 60 GHz. The 50 Ω G-CPW transmission lines are used at the input/output interconnections; whereas 60 Ω (11/4/11 μm) and 55 Ω (11/6/11 μm) G-CPW transmission lines are used as shorted stubs with a Q of 11–12 at 60 GHz. Standard IBM transistor cells and metal-insulator-metal (MIM) capacitor models are used, and full electromagnetic modeling is done on the transmission lines and stubs using Sonnet [22].

Fig. 2.2 presents the 4-stage common-source SiGe LNA which is designed for low-noise and high-gain [15]. The first stage is designed for simultaneous power and noise matching with an emitter degeneration inductor and consumes 1 mA, while the following stages are designed for high gain with 2 mA per stage. The bias circuits are implemented using standard current mirrors. The simulated gain is $>$ 25 dB at 52–61 GHz, and the simulated NF is 5.7–5.8 dB at 55–60 GHz. The amplifier consumes 10.5 mW (7 mA from a 1.5 V supply) and is biased using a current mirror. A PTAT current source is not used, and the LNA current increases to 7.5 mA at 105 °C.

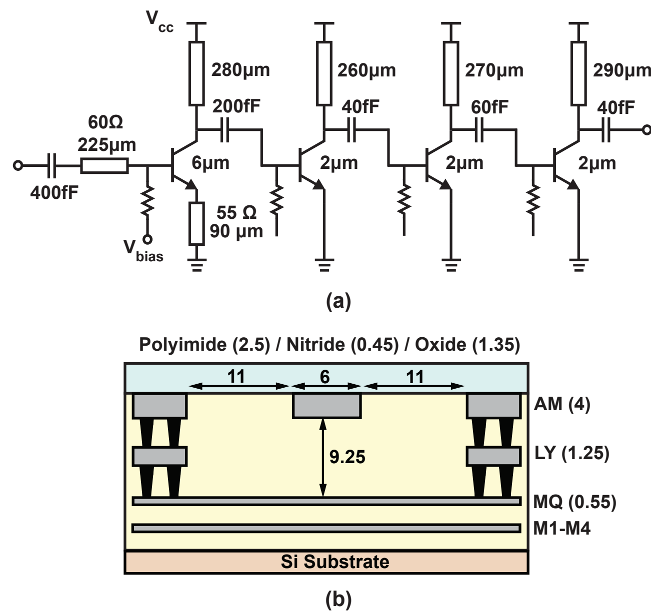


Figure 2.2: (a) LNA schematic and (b) G-CPW transmission line ($Z_0 = 60\ \Omega$, all dimensions are in μm).

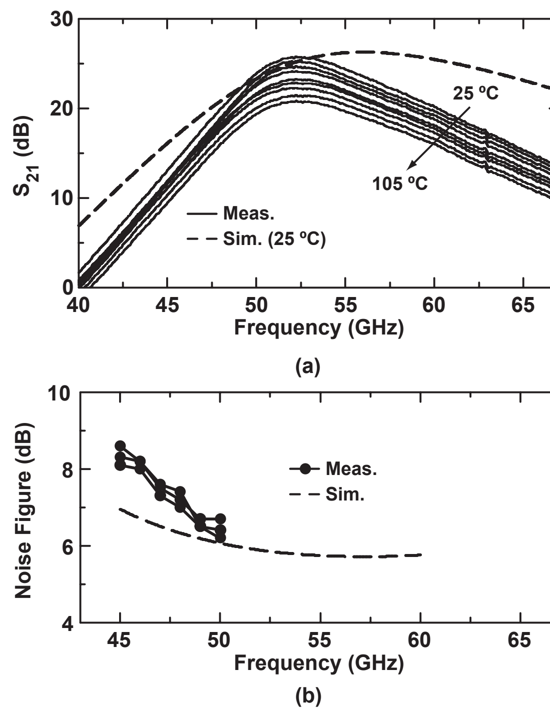


Figure 2.3: Measured LNA (a) gain versus temperature (25–105 °C with 10° steps) and (b) NF versus frequency.

Fig. 2.3(a) presents the measured amplifier gain versus temperature. A gain of 26 dB occurs at 52 GHz with a NF of 6–6.5 dB at 50–60 GHz (Fig. 2.3(b)). The gain decreases by 4.9 dB at 105 °C (simulations predict 3.5 dB). The measured output P_{1dB} at 55 GHz is –10 dBm (IP_{1dB} = –32 dBm), which does not limit the receiver P_{1dB} as shown in Section III.

2.3 V-band Detector

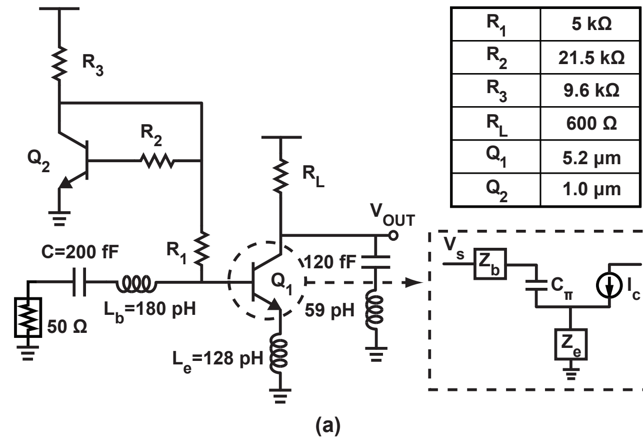
2.3.1 Design

The V-band OOK detector is shown in Fig. 2.4(a). The design employs emitter degeneration and a base inductor to match the detector input impedance to 50 Ω. A 60 GHz notch filter with L = 59 pH and C = 120 fF is used at the collector to filter out the fundamental signal, and the collector impedance is set to 600 Ω for DC biasing purposes. The nonlinear BJT response with emitter degeneration is analyzed using the large signal model shown in Fig. 2.4(a) and is presented in the appendix. The detector open-circuit responsivity, defined as V_{out}/P_{avs} under input impedance-match conditions, is calculated using the Volterra kernels, and can be expressed as

$$\Re = \frac{g_m}{1 + g_m R_e} \frac{R_L}{2w_0^2 C_\pi^2 R_s V_T} \tag{2.1}$$

where $R_e = r_e + \omega_0 L_e/Q$ is the addition of the intrinsic BJT emitter resistance and the extrinsic resistance due to the finite Q of the emitter inductance (L_e), R_s is the source resistance (50 Ω), R_L is the load resistance (600 Ω), C_π is the total capacitance of the base-emitter depletion capacitance (C_{je}) and diffusion capacitance (τg_m), and V_T is the thermal voltage (26 mV at 300 K). At low bias currents ($g_m R_e \ll 1$, and $C_\pi \approx C_{je}$), the responsivity increases linearly with DC bias current (I_Q). As the bias current is increased, the $g_m R_e$ and τg_m terms in C_π cause the responsivity to peak and then roll off.

Fig. 2.4(b) presents a comparison between the calculated open-circuit responsivity using (2.1) and the simulated responsivity in SpectreRF using the transistor models provided by IBM. A device size of 5.2 μm width and R_L = 600 Ω are used, and the detector input impedance is matched to R_s = 50 Ω at each bias current point by corresponding ideal L_e and L_b inductors. For the calculated responsivity, the C_π values are estimated from the f_t versus I_Q plots given in the IBM8HP design manual [21]. The calculated and the simulated responsivity values agree well with each other. It should be noted that these simulations/calculations are for the open-circuit responsivity. Therefore, the loading effect needs to be considered when the detector is followed



R1	5 kΩ
R2	21.5 kΩ
R3	9.6 kΩ
RL	600 Ω
Q1	5.2 μm
Q2	1.0 μm

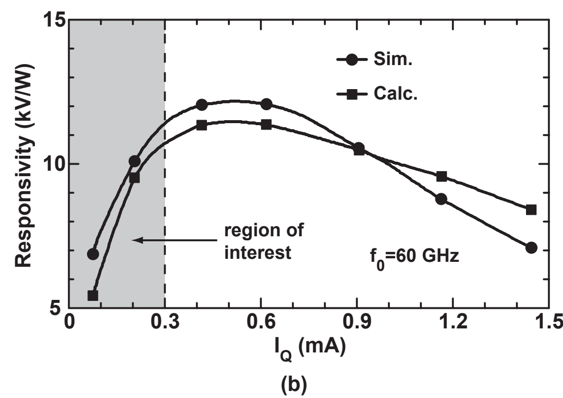


Figure 2.4: (a) Detector schematic and large-signal model for nonlinearity analysis. (b) Simulated (using SpectreRF with IBM models) and calculated (using (2.1)) detector open-circuit responsivity versus I_Q.

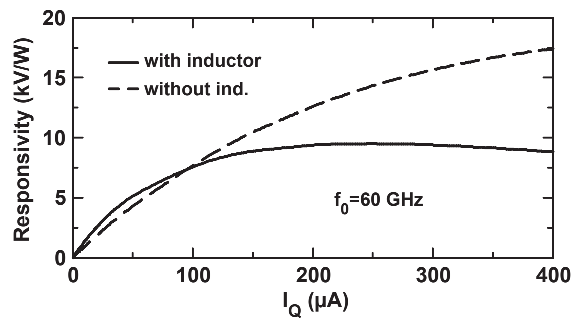


Figure 2.5: Simulated responsivity of the 60 GHz detector with and without the degeneration inductor (L_e = 128 pH).

by a wideband baseband amplifier.

The emitter degeneration inductor linearizes the device and reduces the responsivity (Fig. 2.5). In this case, L_e = 128 pH and L_b = 180 pH for all bias currents, and the simulations include the inductor Q (11–12). At low bias currents ($<$ 120 μA), the inductive feedback is negligible since $g_{m1}\omega_0 L_e \ll 1$. As the bias current is increased ($\approx$ 300 μA), the simulated responsivity drops by a factor of 2 when the emitter inductor is used. Since L_e results in a wide impedance match, it is preferable to use an emitter inductor to account for process and temperature variations.

One of the key parameters of a detector is the noise equivalent power (NEP), and it is defined as the input power that results in a signal-to-noise ratio (SNR) of 1 at the detector output. In other words, NEP is the output noise voltage divided by the responsivity. Therefore, it is of interest to analyze the noise contribution of each component in the OOK detector shown in Fig. 2.4(a). The output noise voltage at low frequencies is

$$\begin{aligned} V_{n,out}^2 \approx\ & 4kTBR_1(g_{m1}R_L)^2 + 4kTBR_2(g_{m1}R_L)^2 + 4kTBR_3\left(\frac{g_{m1}R_L}{g_{m2}R_3}\right)^2 \\ & +2kTBg_{m1}R_L^2 + 2kTBg_{m2}(5.2)^2R_L^2 + 4kTBR_L \end{aligned} \quad (2.2)$$

where the noise contribution of R_1, R_2, R_3, Q_1, Q_2 and R_L are expressed respectively, neglecting the r_π of Q_1. 1/f noise is neglected because this is a wideband receiver. At very low I_Q ($<$ 50 μA), $V_{n,out}$ is proportional to $\sqrt{g_{m1}}$, whereas the responsivity is proportional to g_{m1}, and the NEP decreases as I_Q increases. As I_Q is further increased, $V_{n,out}$ becomes proportional to g_{m1}, and the responsivity is no longer proportional to g_{m1}, and the NEP starts to degrade. Therefore, there is a certain bias current that minimizes the detector NEP.

Fig. 2.6 presents the simulated output noise contribution of each component versus frequency for a bias current of 100 μA and 350 μA. The bias resistors (R_1, R_2) have the highest noise contribution at low frequencies with a noise transfer function pole at f $\approx$ 160 MHz (R_1 = 5 kΩ, C = 200 fF). Therefore, the integrated total output noise due to the bias resistors at a fixed I_Q and R_L depends only on the input capacitance, and can be expressed as

$$V_{N,OUT,R_1,R_2}^2 \approx \frac{kT}{C}(g_{m1}R_L)^2 + \frac{kT}{C}\frac{R_2}{R_1}(g_{m1}R_L)^2 \quad (2.3)$$

Even though lower-value bias resistors could be used to improve the spot noise, the integrated output noise due to R_1 and R_2 is the same as long as the pole frequency is lower than the output signal bandwidth. This is an important observation for wide-band OOK receivers.

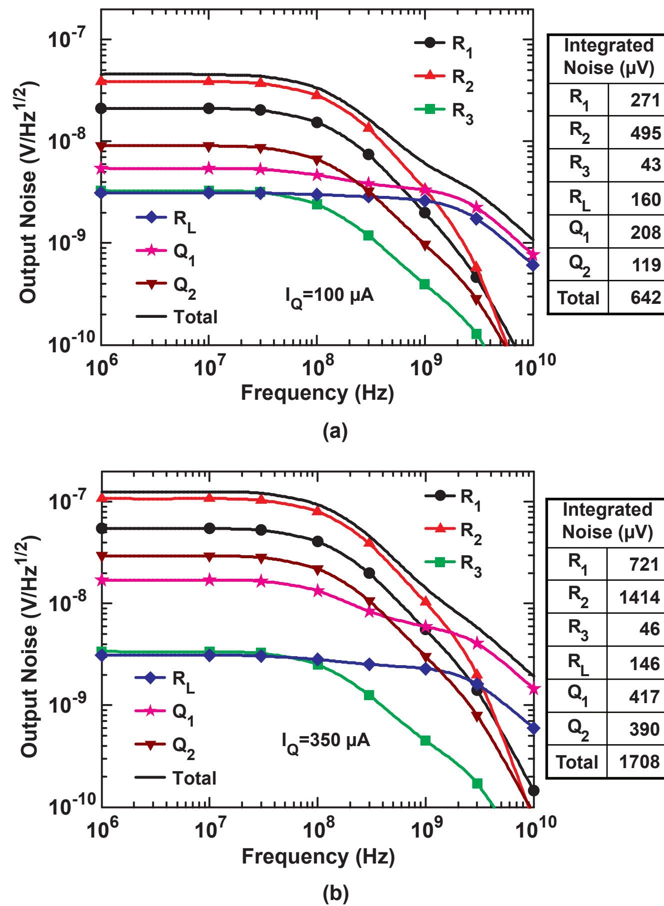


Figure 2.6: Output noise contribution of each component versus frequency and integrated (1 MHz–10 GHz) noise voltage at (a) I_Q = 100 μA and (b) I_Q = 350 μA.

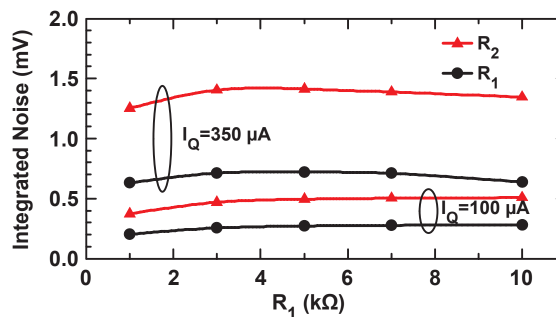


Figure 2.7: Integrated output noise voltage (1 MHz–10 GHz) due to R_1 and R_2 versus R_1 at (a) I_Q = 100 μA and (b) I_Q = 350 μA. R_2 values are also changed proportionally for each R_1.

However, for narrow-band imaging receivers with a bandwidth of 30–3000 Hz, it is essential to choose a much lower noise biasing network [6, 7]. Fig. 2.7 presents the integrated (1 MHz–10 GHz) output noise voltage due to R_1 and R_2 for different R_1 values (1–10 kΩ) at I_Q of 100 μA and 350 μA. In these simulations, the R_2 values are changed proportionally for each R_1 to keep the same current mirror ratio and I_Q. The integrated output noise due to the bias resistors is virtually constant as expected.

For future designs, the detector output noise can be reduced with the following design choices: 1) A lower current-mirror ratio will reduce the noise contribution of Q_2, R_3 and R_2 as given by (2.2) since a lower R_2 value is used. The current-mirror ratio could be set to 1 or even higher since the detector power consumption is negligible compared to the LNA. 2) A larger input capacitor will result in a lower integrated noise from the bias network (refer to (2.3)), but since it is in the RF path, attention should be placed on its resonating frequency. 3) Most importantly, an input matching network with a shunt inductor can be used. Hence, the R_1 and R_2 will be completely eliminated since the bias is applied to an AC ground.

2.3.2 Measurements

Fig. 2.8 presents the measured and simulated S-parameters of the OOK detector. The detector is well matched and the notch filter characteristic is clearly seen in the S_{21} response. Fig. 2.9(a) presents the detector output noise measurement setup. The detector output impedance is 600 Ω and an SMA-tee together with an SMA 50 Ω termination is placed right after the output GSG probe in order to eliminate the standing waves due to the long SMA cable to the spectrum analyzer (Agilent E4448A). The spectrum analyzer internal preamp (100 kHz–3 GHz) is turned on to reduce the noise-floor to –168 dBm/Hz. The noise contribution of the bias resistors can be clearly seen especially below 500 MHz (Fig. 2.9(b)).

Fig. 2.10 presents the measured and simulated responsivity, output noise voltage and NEP of the detector versus I_Q at 60 GHz. The noise voltage is sampled at an output IF frequency of 500 MHz so that the noise contribution of the bias resistors is reduced. The measured responsivity into a 50 Ω load is 600–700 V/W at I_Q = 100–350 μA, and the measured output noise at 500 MHz is 1.4–2.9 nV/Hz$^{1/2}$ $\left(\Re_{50\Omega} = \Re_{oc} \times \frac{50}{650}\right)$. This results in a measured NEP of 2.0–4.5 pW/Hz$^{1/2}$ at 60 GHz for I_Q = 100–350 μA. Fig. 2.11 shows the measured and simulated responsivity and NEP of the OOK detector versus frequency. Note that the NEP at 100 μA is 2–2.5 $\times$ lower than at 350 μA.

Fig. 2.12 presents the measured detector responsivity versus input power. The detector

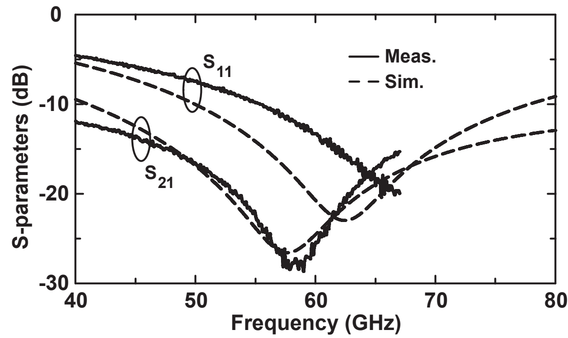


Figure 2.8: Measured and simulated S-parameters of the OOK detector.

input P_{1dB} is defined as the input power which results in a relative output voltage of 0.9 (V^2 = 0.8), and is –20 dBm for both cases. The transistor self-bias at –20 dBm with an additional 120 μA of current.

2.4 V-band OOK Receiver Characterization

2.4.1 LNA/Detector

The OOK receiver occupies 0.57 $\times$ 1.1 mm^2 including the pads and is based on the SiGe LNA followed by the OOK detector (Fig. 4.3). The OOK receiver responsivity is simply the LNA gain multiplied by the detector responsivity. The measured responsivity in a 50 Ω load at 55 GHz is 160–190 kV/W for I_Q = 100–350 μA. Since the LNA S_{21} response shifted from 56 GHz to 52 GHz, the measured LNA S_{21} will be used in the OOK receiver simulations (Fig. 2.3(a)). The measured OOK receiver NEP is 10–24 fW/Hz$^{1/2}$ at I_Q = 100–350 μA for an output IF frequency of 500 MHz (Fig. 2.14). The NEP is dominated by the OOK detector and is again 2–2.5 $\times$ higher than for 350 μA compared to 100 μA. The OOK receiver consumes 7.5 mA from a 1.5 V supply (11 mW).

2.4.2 BER Measurements

Fig. 2.15(a) presents an OOK transmitter system based on an Agilent N4903A BER tester sending $2^{31} - 1$ pseudo-random binary sequence (PRBS). A carrier frequency of 55 GHz is chosen. A coaxial mixer was used to achieve the OOK modulation by multiplying the PRBS data with the carrier. If the incoming data is 1, then the carrier signal passes through the mixer; else, there is no signal at the mixer output. However, due to the finite LO-RF isolation, there

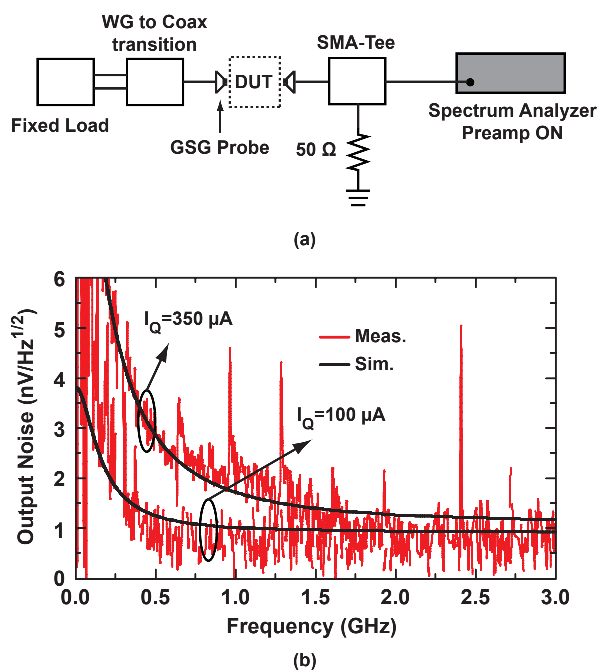


Figure 2.9: (a) Detector output noise voltage measurement setup and (b) measured and simulated detector output noise voltage versus output IF frequency at I_Q = 100 μA and I_Q = 350 μA.

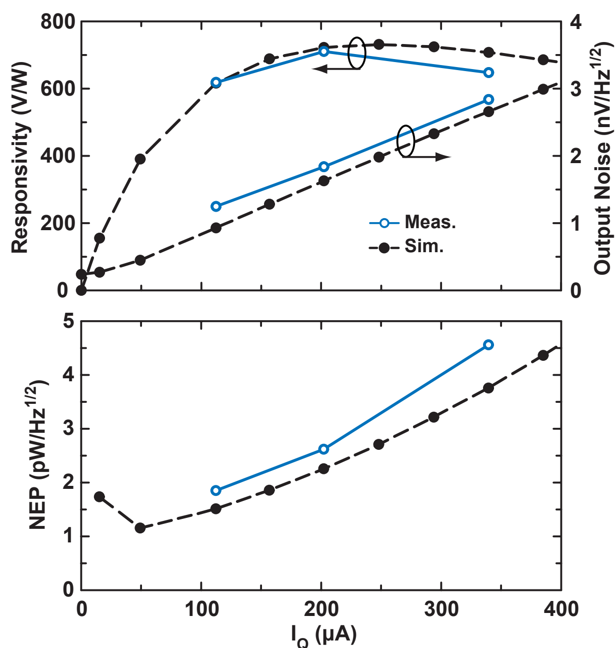


Figure 2.10: Measured and simulated detector responsivity, output noise voltage and NEP versus I_Q (f_0 = 60 GHz). The output IF frequency is 500 MHz.

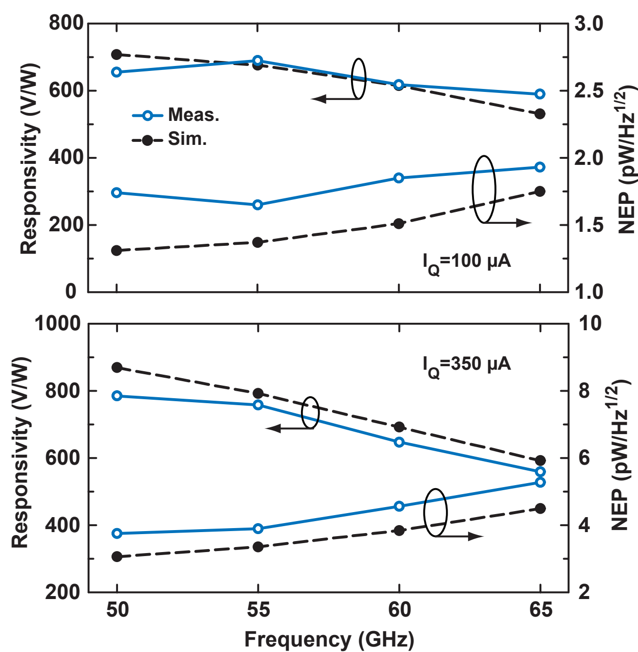


Figure 2.11: Measured and simulated detector responsivity and NEP versus frequency at I_Q = 100 μA and I_Q = 350 μA. The output IF frequency is 500 MHz.

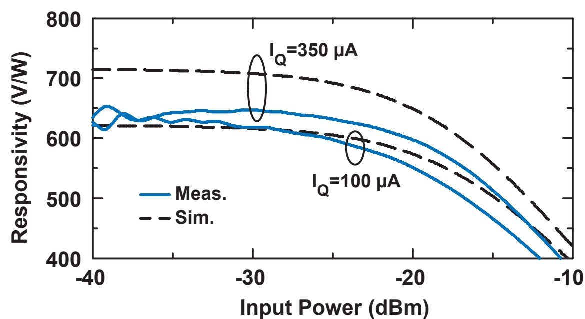


Figure 2.12: Measured and simulated detector responsivity versus input power. Input P_{1dB} = –20 dBm.

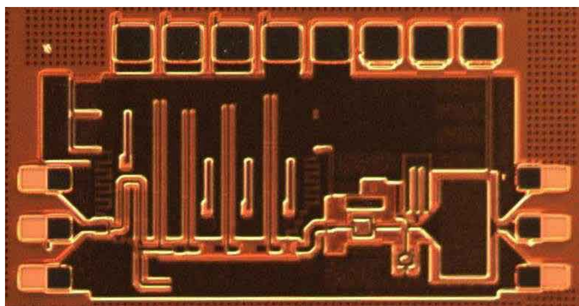


Figure 2.13: Microphotograph of the OOK receiver (1.1 $\times$ 0.5 mm^2 including the pads).

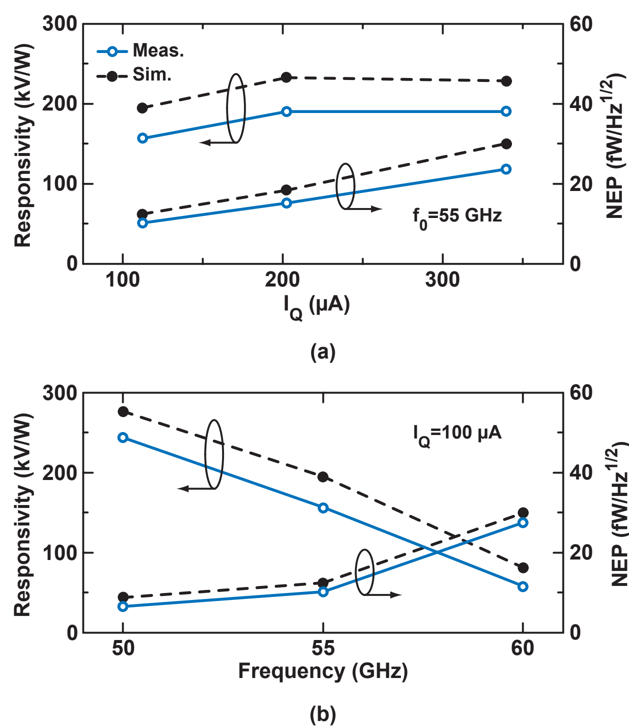


Figure 2.14: Measured and simulated OOK receiver responsivity and NEP versus (a) I_Q and (b) frequency. The output IF frequency is 500 MHz.

is a residual signal at the mixer output when the data is 0, which greatly reduces the system dynamic range. In order to cancel the residual signal, an LO leakage cancelation path with the same residual amplitude and 180° out of phase is used together with a waveguide Magic-Tee summer (Fig. 2.15(a)).

The OOK modulated signal is transmitted and received using WR-15 waveguide antennas over variable distances, but this is normalized out of the experiment and all power levels are referred to the available input power at the GSG probe tips. The detected baseband signal after the DUT (OOK receiver chip) is amplified by coaxial 50 Ω 1–6000 MHz wideband amplifiers and fed back to the BER tester. The baseband amplifier has a NF of < 5 dB, which is insignificant compared to the output noise from the OOK receiver. Their power consumption is not included in the calculations.

Fig. 2.15(b) presents the BER versus data rate for different input power levels, and a 6 Gb/s wireless communication link is achieved with a 10^{-12} bit error rate. The measured BER is actually $< 10^{-12}$, but it takes significant amount of time to measure a BER $< 10^{-12}$, so 10^{-12} is determined to be the lower limit. The optimum BER is achieved at a mid-point input power of –36 dBm. Fig. 2.16(a) presents the BER versus input power for a fixed data rate (3 Gb/s). The dynamic range of the OOK receiver is 23–27 dB taking the BER of 10^{-9} as a reference. Additionally, the OOK receiver is measured versus temperature at 3 Gb/s with an input power of –36 dBm, and the BER remains $< 10^{-12}$ at 25–105 °C (Fig. 2.16(b)). The eye-diagram at 25 °C is also presented in Fig. 2.16(b).

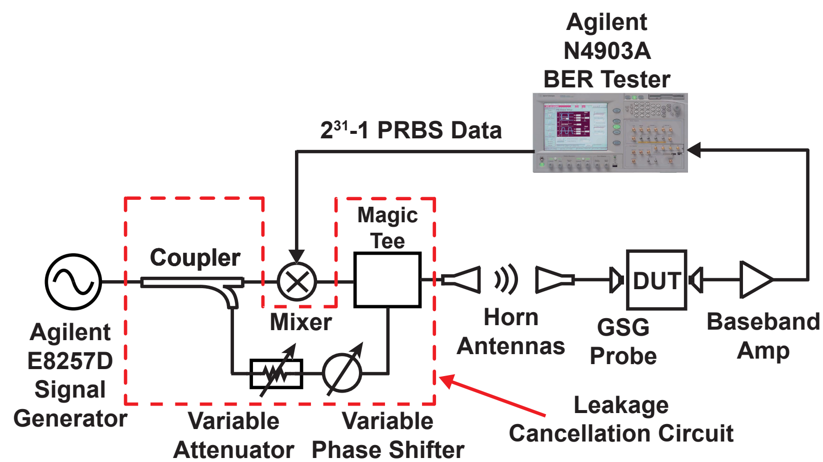
It is instructive to analyze the minimum input power for a certain BER. For a coherent OOK modulation with a double-side spectrum, the BER is

$$BER = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{2N_0}}\right) \tag{2.4}$$

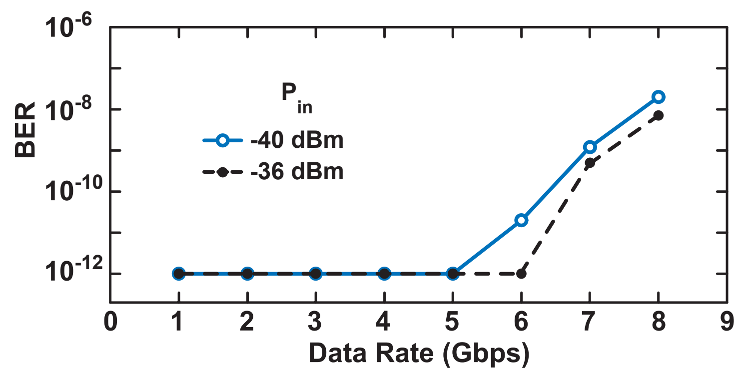
where erfc is the complementary error function, E_b/N_0 is the energy per bit to the noise power spectral density ratio [23]. Using (2.4), the OOK modulation scheme requires an E_b/N_0 = 17 dB for BER = 10^{-12}. The required SNR is calculated using [24]:

$$SNR[\text{dB}] = \frac{E_b}{N_0}[\text{dB}] + 10\log(\text{Data Rate/BW}) \tag{2.5}$$

Considering 3 Gb/s data rate and a 6 GHz baseband amplifier bandwidth (BW), the required SNR for a BER of 10^{-12} is 14 dB. The measured NEP of the OOK receiver is 10–24 fW/Hz$^{1/2}$ at 100–350 μA which is equivalent to –110 to –106 dBm/Hz$^{1/2}$. The minimum input power necessary for a BER of 10^{-12} can be calculated using



(a)



(b)

Figure 2.15: (a) BER measurement setup and (b) Measured BER versus data rate at a carrier frequency of 55 GHz.

$$P_{in} = NEP[\text{dBm/Hz}^{1/2}] + 10\log(\sqrt{BW}) + SNR[\text{dB}] \tag{2.6}$$

and is –47 dBm to –43 dBm for 100–350 μA. As shown in Fig. 2.16(a), the measured minimum input power for a BER of 10^{-12} is –41 dBm at 350 μA. The 2-dB difference is due to the LNA S_{21} response, where the measured peak gain is centered at 52 GHz. Therefore, the LNA/detector performs almost a one-sided spectral detection when a 55 GHz carrier is chosen.

A higher-gain LNA can be used to improve the OOK receiver sensitivity at the expense of a lower input P_{1dB}. However, since the output noise is mostly dominated by the detector, a higher-gain LNA will shift the lower sensitivity and upper compression power levels by the same amount, and the receiver dynamic range will not change. If a lower-gain LNA is used, the receiver input P_{1dB} can be improved at the expense of receiver sensitivity. Again, the dynamic range will not change. Therefore, in order to improve the dynamic range, a variable gain LNA should be used.

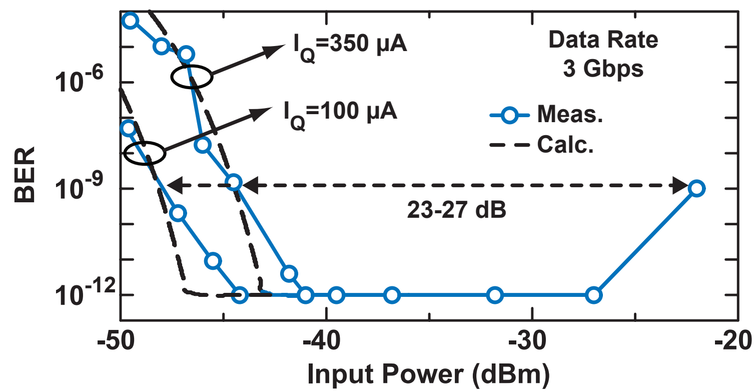
2.4.3 Effect of LO Leakage and Power Compression on OOK Detection

Fig. 2.17(a) shows the voltage waveform of the OOK modulated signal in time domain, and in an ideal OOK modulator, V_{OFF} = 0. However, due to the LO leakage in the OOK modulator, there is a residual signal which limits the receiver dynamic range. In a non-ideal OOK modulator, the LO leakage can be modeled as $V_{OFF} = \alpha V_{ON}$ where $0 < \alpha < 1$, and the BER is (see appendix)

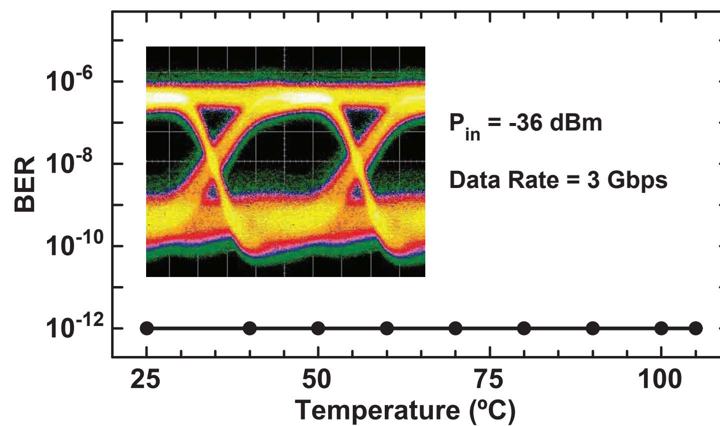
$$BER = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{2N_0}\frac{(1-\alpha)^2}{1+\alpha^2}}\right) \tag{2.7}$$

(2.7) simplifies to (2.4) when α = 0, for an ideal OOK modulation. Additionally, α = –1 corresponds to a BPSK modulation scheme, and it is observed in (2.7) that the OOK modulation requires 3 dB more energy per bit to achieve the same performance as BPSK modulation. Fig. 2.17(b) presents the BER versus E_b/N_0 for various α values. When α = 0.32–0.1 (10–20 dB isolation), the sensitivity degradation is 4 dB and 1 dB, respectively (Fig. 2.17(c)). There is virtually no sensitivity degradation above 30 dB isolation.

In the BER measurement setup shown in Fig. 2.15(a), the OOK modulator is a coaxial Marki-Microwave mixer [25], with 50 Ω matched ports with an IF bandwidth of DC–10 GHz, an input P_{1dB} of +2 dBm, a conversion loss of 9 dB, and an LO-RF isolation of 25 dB. The LO drive level is +10 dBm at 55 GHz. The IF data signal from the BER tester has an amplitude of 300



(a)



(b)

Figure 2.16: Measured BER versus (a) input power and (b) temperature at a carrier frequency of 55 GHz.

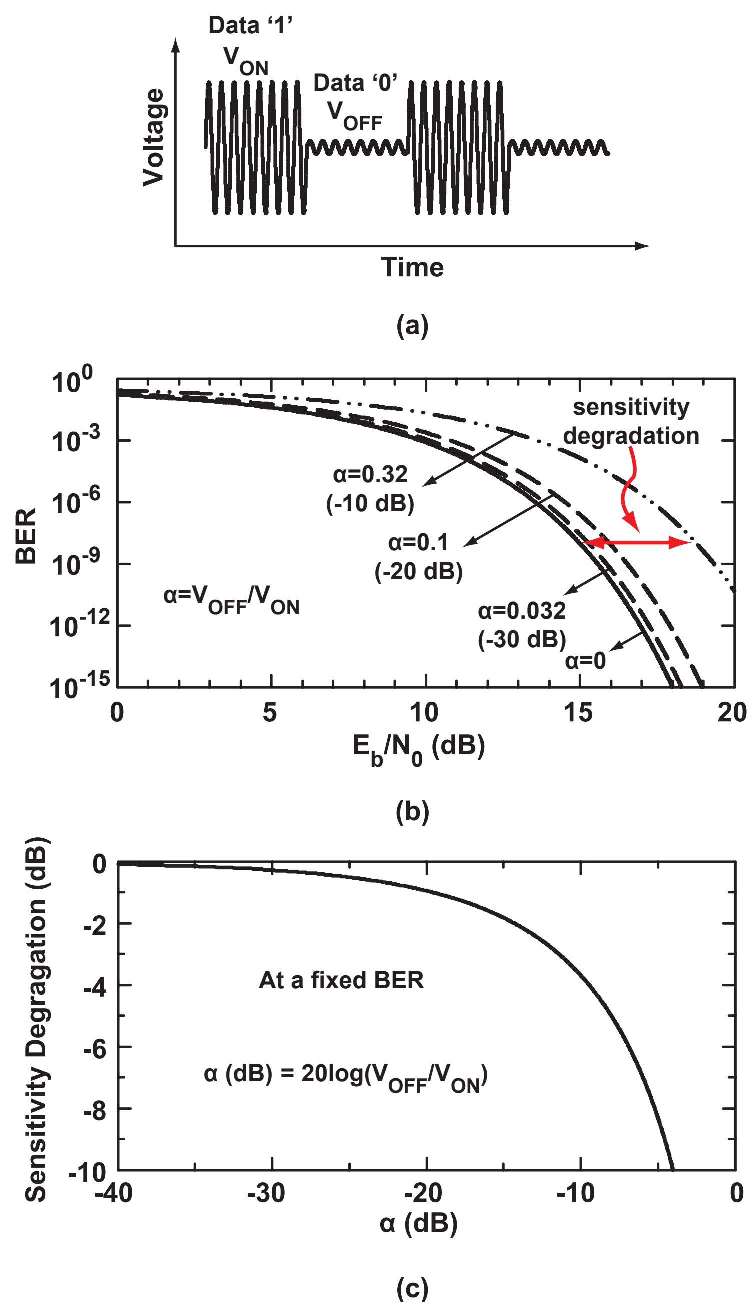


Figure 2.17: (a) OOK modulated waveform. (b) BER versus E_b/N_0 for non-ideal OOK modulation. (c) SNR degradation versus α at a fixed BER.

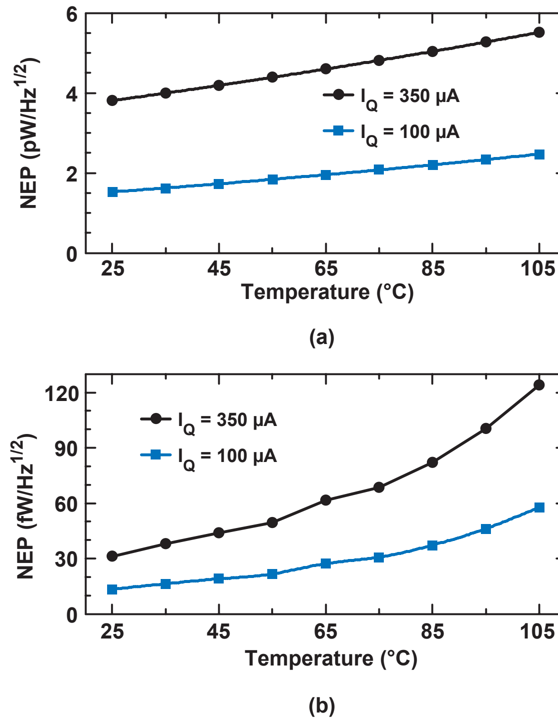


Figure 2.18: Simulated NEP of the (a) detector and (b) OOK receiver versus temperature.

mV for bit 1 and 0 mV for bit 0. Therefore, the V_{ON} has an amplitude of $\approx$ 105 mV considering the 9 dB conversion loss, and the V_{OFF} has an amplitude of $\approx$ 56 mV. This corresponds to $\alpha \approx$ 0.5 (6 dB isolation) and a sensitivity degradation of 7 dB (Fig. 2.17(c)). The LO leakage was reduced from -15 dBm to $<$ -50 dBm using the cancellation path which corresponds to $\alpha <$ -40 dB and no sensitivity degradation.

As shown in Fig. 2.16(a), the BER performance degrades at high input power levels when the LNA and OOK detector enter into compression. Intuitively, the gain is different for the V_{ON} (with compression) and V_{OFF} (without compression) intervals, and this results in a decrease of the effective V_{ON}/V_{OFF} isolation. Therefore, the system BER decreases by a similar reasoning as LO leakage effects.

2.4.4 Effect of Temperature on OOK Receiver Dynamic Range

Fig. 2.18 presents the simulated NEP of the detector and the OOK receiver versus temperature at I_Q = 100–350 μA. The NEP degradation of the OOK detector is only $\approx$ 1 dB at 105 °C, but that of the entire receiver is 6 dB, mostly due to the 5 dB drop in the LNA gain. Therefore, the minimum input power level for a certain BER will increase by 6 dB. On the other

hand, the LNA IP_{1dB} is 5 dB higher at 105 °C due to the LNA gain decrease. Hence, the OOK receiver dynamic range is estimated to be 1 dB lower at 105 °C.

Finally, as discussed in Section III.A, the NEP can be improved by eliminating the noise of R_1 and R_2 through the use of a shunt inductor at the base of Q_1 (see Fig. 2.4(a)). In this case, the NEP improves by 3 dB and is 5 fW/Hz$^{1/2}$ for the entire receiver, which increases the instantaneous dynamic range to 30 dB. The authors believe that this is an inherent limit for OOK receivers, given on one side by the NEP and on the other side by receiver compression.

2.5 Conclusion

A low-power OOK receiver at V-band is developed in a commercial 0.12-μm SiGe BiCMOS process, and 3–6 Gb/s wireless communication link has been demonstrated with a BER $< 10^{-12}$ up to 105 °C. In depth analysis indicate that the OOK receiver operates best at low bias currents, and care should be taken to reduce the bias circuit noise, and to reduce the LO leakage from the transmitter. The OOK receiver, when well designed, can have an instantaneous dynamic range of 30 dB.

2.6 Acknowledgement

This work was supported by the Intel Corporation and University of California (UC) Discovery program, Dr. Ian Young and Dr. Jad Rizk, program monitors. The authors would like to thank Prof. James Buckwalter at UCSD for his help in the BER measurements.

Chapter 2 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2012. Mehmet Uzunkol; Woorim Shin; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 3

A Low-NEP 0.32 THz SiGe 4×4 Imaging Array Using High-Efficiency On-chip Antennas

3.1 Introduction

Terahertz (THz) imaging systems, defined as antenna-coupled detectors or radiometer in the focal plane at f $>$ 300 GHz, have been developed using GaAs and InP since the 1980s with applications in radio-astronomy and contraband detection [26–35]. Traditionally, these imaging systems are implemented using a low-noise amplifier followed by a square-law detector and an operational amplifier, a low-noise amplifier followed by a mixer and a wideband IF amplifier, or at f $>$ 200-300 GHz, using a low-noise fundtamental/sub-harmonic mixer with a NF $<$ 10 dB, followed by a wideband IF amplifier (Fig. 3.1(a),(b),(c)) [5, 36]. These systems are either waveguide based, or antenna-coupled using high efficiency planar antennas, and results in a noise equivalent power (NEP) of fW/Hz$^{1/2}$ over a wide bandwidth (10-30 GHz) [37–39]. Therefore, they can operate without the need of an active illuminator, that is, the imaging array is sensitive enough for a detection of the source thermal radiation, P = kT W/Hz$^{1/2}$. However, they require GaAs or InP technologies, consume a lot of DC power, and are not suitable for low-cost imaging arrays.

Recently, there has been a lot of interest in using SiGe and CMOS for THz imaging arrays, SiGe-based radiometers based on high gain amplifiers and a detector were demostrated at 100-165 GHz with an NEP of 2-10 fW/Hz$^{1/2}$, which is competitive with the best III-V tech-

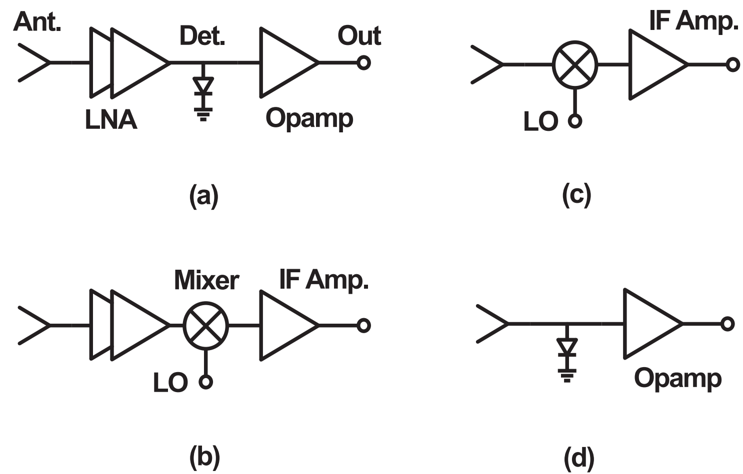


Figure 3.1: Imaging front-ends: (a) amplifier-detector, (b) amplifier-mixer, (c) mixer, and (d) detector.

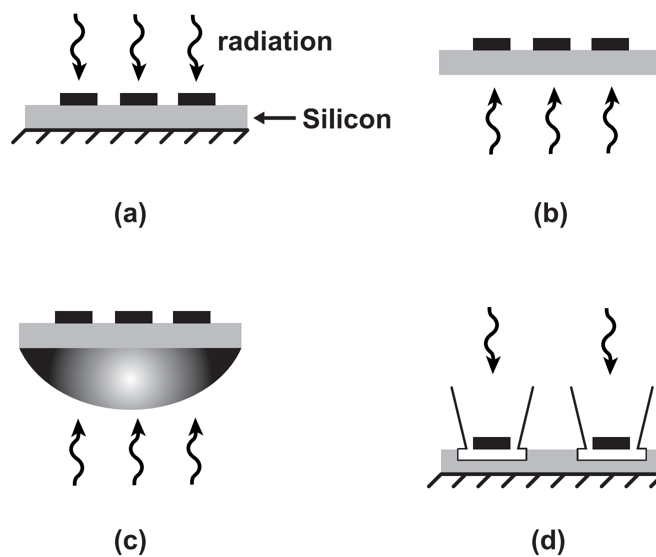


Figure 3.2: Antenna radiation methods: a) above-chip, b) below-chip, c) dielectric lens, and d) micro-machining techniques.

nologies [6–9]. However, this topology is not suitable for applications above 200 GHz due to the lack of low-noise high-gain amplifiers in silicon technologies. In this case, antenna-coupled detectors (with no amplification) have been demonstrated at 300-1000 GHz with an NEP of 30-100 pW/Hz$^{1/2}$ (Fig. 3.1(d)) [10–13]. This is 1000-5000 times higher compared to radiometers and therefore, require the use of an active imaging system so as to obtain acceptable signal-to-noise ratios (0.1-5 mW transmitted power level depending on the application). However, they consume a very small amount of power and are scalable to a large number of elements. Single-frequency imaging systems result in shadowing and specular reflections, and one way to combat these effects is to illuminate the subject with several frequencies and at different angles so as to create a diffuse effect. Therefore, the imaging system must be wideband (30-60 GHz at 300 GHz) and with high efficiency for optimal performance.

The NEP of an imaging array is dependent on 1) the antenna efficiency, and 2) the inherent detector NEP. Therefore, it is essential that high-efficiency on-chip antennas be used for a low system NEP. The on-chip antennas can be implemented in several ways (Fig. 3.2): a) above-chip radiation, b) below-chip radiation, c) below-chip with a dielectric lens, and d) above-chip with micromachining and focusing techniques. It is our opinion that the above-chip radiation results in the lowest-cost and most robust system since it operates with full-thickness silicon chips which can be placed on a low-cost carrier substrate. The dielectric-lens approach also operates with full thickness wafers, but the lens can be expensive for THz operation, and special mounting is required. The below-chip radiation require thinning of wafers to unacceptable levels (< 50 μm) at f > 300 GHz and therefore is not robust. Finally, the above-chip radiation with micromachining techniques does result in high-efficiency antennas, but requires post-processing and may be expensive to implement. This work focuses on above-chip radiation with the silicon chip mounted on standard FR-4 substrates.

This chapter presents a 4×4 SiGe imaging array with efficient above-chip radiators and integrated low-frequency operational amplifiers to achieve an NEP of 34 pW/Hz$^{1/2}$ at 320 GHz with a 3-dB bandwidth of 25 GHz. The entire chip consumes 25 mA from 1.5 V supply, and with a responsivity of 18 kV/W at 320 GHz. The imaging chip is accurately characterized using a far-field THz system, and this chapter details the systematic errors encountered in measuring imaging arrays at THz frequencies and shows the decisions made to report a measured NEP of 34 pW/Hz$^{1/2}$.

3.2 Design

The 320 GHz imaging array is fabricated in a 0.18 μm in a SiGe BiCMOS process (Jazz SBC18H3) with 6 metal layers [40]. This technology has high-speed 0.13 μm SiGe HBTs with an f_t/f_{max} of 240/280 GHz. Grounded coplanar waveguide (G-CPW) transmission lines with dimensions 8/8/8 μm ($Z_0 = 50\ \Omega$) are implemented in the top three metal layers, with a measured loss of 1.25 dB at 110 GHz [41] (Fig. 3.3).

Fig. 3.4 presents the block diagram of the 4×4 imaging array. The single-ended slot antenna is connected to the detector, and a reference detector is used together with the main detector to drive a 22 dB gain differential IF amplifier. A 16-to-1 on-chip differential multiplexer (mux) is used to read out the output voltage in a pixel by pixel fashion. Also, in order to read out an entire row (4 pixels simultaneously), a 16-to-4 differential mux is also placed on the chip.

3.2.1 Antenna Design

The 360 GHz elliptical slot-ring antenna is designed using a 100 μm quartz superstrate above the silicon chip [42–44]. The antenna is single-ended and placed on the top metal layer (M6), and the ground plane is defined as M1. This creates a parallel-plate condition which can channel a lot of power away from the antenna and reduce its efficiency. The quartz superstrate is not patterned, and is used to equalize the TEM mode in the dielectric underneath M6 and the TM_0 mode in the quartz superstrate [42]. This results in a high-efficiency antenna since the two radiating slots in the elliptical slot-ring antenna are placed at $\lambda_{TM_0}/2$ = $\lambda_{TEM}/2$ apart, and therefore cancel any spurious radiation in the X-Y plane. The antenna, without meeting any metal-density rules, results in a radiation efficiency of 57-62$\%$ and a gain of 4.1-4.6 dB at 320-390 GHz showing a wideband design using a quartz superstrate.

In this work, the antennas are designed to meet the metal-density rules even if this results in a detrimental effect on the antenna performance due to increased capacitance effects and added loss. This is done so that no metal exclusion is taken on the wafer, which is congruent with a full mask containing thousands of imaging array chips. In the SBC18H3, the metal density rules are 30$\%$ for M1-M6, and Fig. 3.5 presents the different cases under consideration. The simulated S_{11} is shown in Fig. 3.6 and as expected, the antenna without any metal density rules (Case 3) shows a bit wider bandwidth than Case 1 and Case 2. The radiation efficiency of a Case 2 antenna is 43$\%$ (metal fill not connected to each other or ground) at 360 GHz and is 1.7 dB better than Case 1 with a radiation efficiency of 30$\%$ (metal fill connected to each other and ground) (Fig. 3.7(a)). The simulated gain also indicates a similar trend (Fig. 3.7(b)). The antenna used

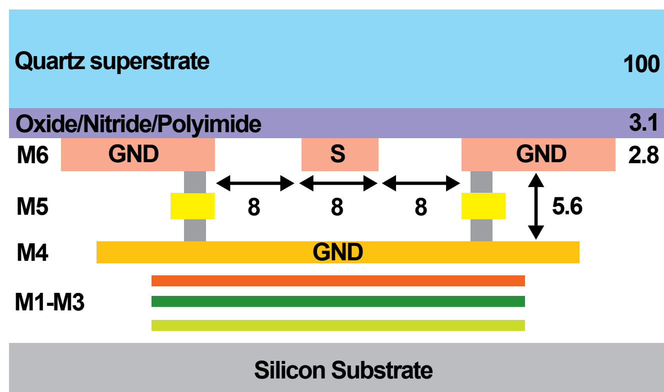


Figure 3.3: Metal stack-up of the 0.18 μm SiGe BiCMOS process (Jazz SBC18H3). Metal fillings underneath the on-chip antenna and 50 Ω G-CPW transmission line are also shown. All dimensions are in μm.

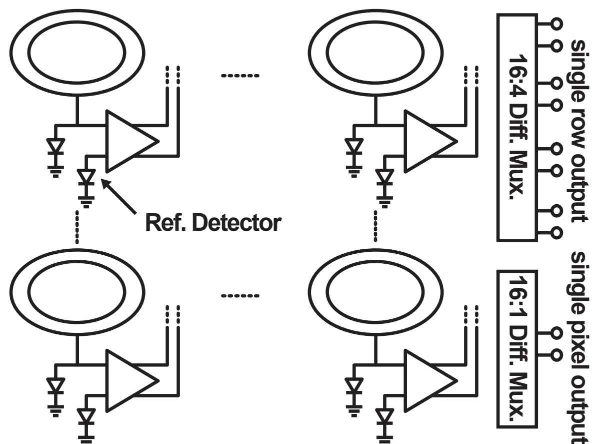


Figure 3.4: Block diagram of the 320 GHz SiGe 4 $\times$ 4 imaging array.

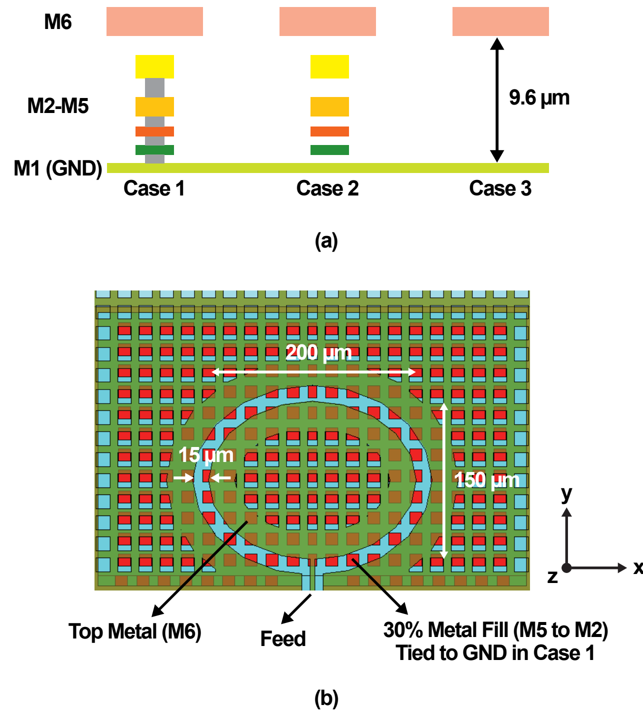


Figure 3.5: (a) Metal-fill cases (Oxide/Polymide/Nitride and Quartz layers are not shown) and (b) on-chip single-ended slot antenna with the metal-fill underneath the antenna.

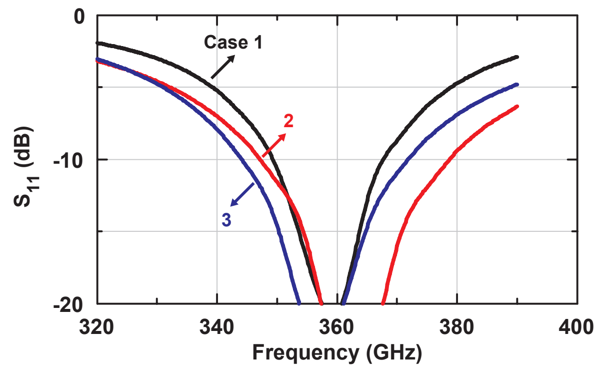
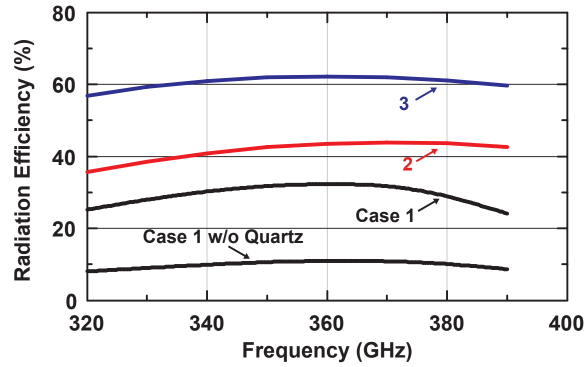
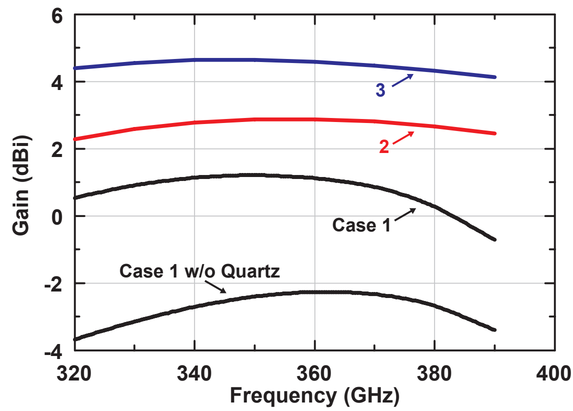


Figure 3.6: Simulated on-chip elliptical slot-ring antenna S_{11} for different metal-fill cases.



(a)



(b)

Figure 3.7: Simulated on-chip elliptical slot-ring antenna (a) efficiency and (b) gain for different metal-fill cases.

here follows Case 1 (Case 2 was considered post tapeout) and is 3.4 dB worse than an antenna without any metal density rules (Case 3) at 360 GHz.

3.2.2 Detector Design

The responsivity ($\Re$) and noise equivalent power (NEP) are important figure of merits for detector design. The responsivity in V/W is defined as the DC output voltage (due to even-order device non-linearity terms) divided by the available input power. The NEP (W/Hz$^{1/2}$) is defined as the equivalent input power level which results in a signal-to-noise ratio (SNR) of 1 at the detector output, in order words, the output noise voltage divided by the responsivity.

A conventional SiGe detector employs a notch filter such as series LC or a single capacitor at the collector node to filter out the fundamental signal [6,8,45]. In this work, a new detector topology is proposed which employs a $\lambda/4$ transmission line at the collector node to further increase the responsivity (Fig. 3.8). The transmission line results in a high impedance load (Z_L), which in turn, results in a larger Z_{IN} and a larger V_π. Assuming that the device nonlinearity is mostly due to the base-emitter junction impedance (C_π, r_π), then a higher responsivity is obtained for a larger voltage swing at V_π. The responsivity is calculated based on the equivalent circuit model of Fig. 3.8(c) and the BJT power-series non-linearity expansion, and is expressed as:

$$\Re = \frac{I_Q}{2V_T^2} R_L \frac{1}{Re(Y_{IN})} \frac{Re(Z_{IN})}{(r_b + Re(Z_{IN}))} \tag{3.1}$$

where

$$Z_{IN} = \frac{1 - \omega_0 C_\mu X_L}{-\omega_0 g_m C_\mu X_L + j(\omega_0 (C_\pi + C_\mu) - \omega_0^2 C_\pi C_\mu X_L)} \tag{3.2}$$

$$X_L = Z_0 \tan(\theta) \qquad r_\pi \gg \frac{1}{\omega_0 C_\pi} \tag{3.3}$$

For comparison purposes, both the conventional and proposed designs use HBT devices with $L_E = 2$ μm emitter length, and their input impedance is matched to 50 Ω using ideal components. Fig. 3.9(a) presents the simulated responsivity versus bias current (I_Q), and the proposed design results in approximately 30% higher responsivity. Since the output noise voltage (at low frequencies) for both designs is the same, the proposed design has therefore a lower NEP. Fig. 3.9(b) presents the simulated responsivity at I_Q = 100 μA versus the electrical length (θ) of the transmission line. As expected, a peak occurs at 90-105° since this results in the largest Z_{IN}.

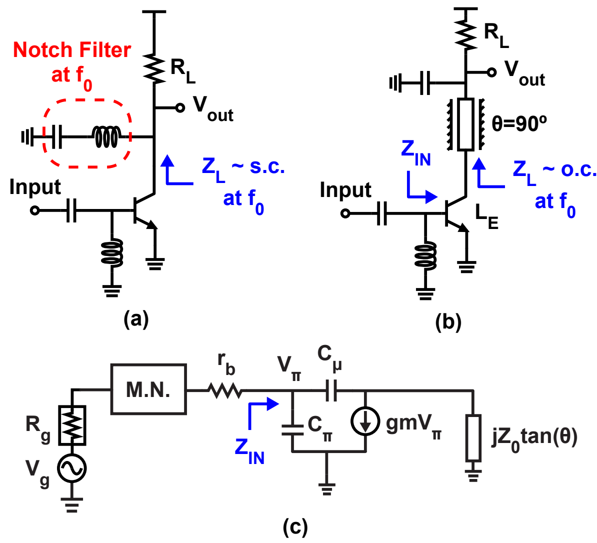


Figure 3.8: (a) Conventional and (b) proposed detector design, and (c) equivalent circuit model. Biasing circuit is not shown.

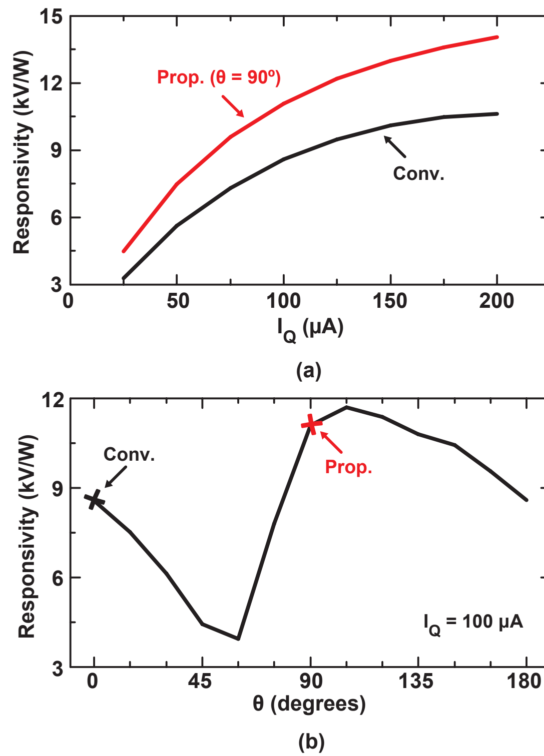


Figure 3.9: Simulated responsivity at 360 GHz versus (a) detector bias current (I_Q) for the conventional/proposed designs and (b) transmission line electrical length (θ) for the proposed design at I_Q = 100 μA.

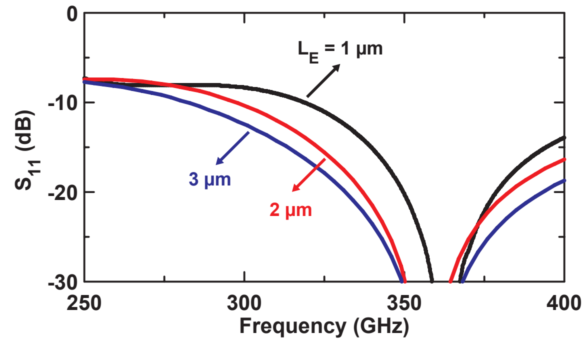


Figure 3.10: Simulated detector S_{11} versus frequency for different L_E at I_Q = 100 μA.

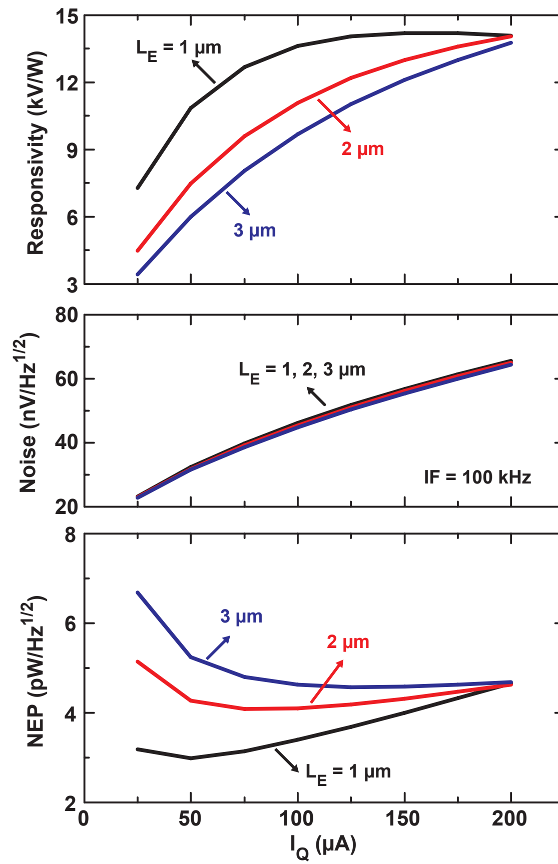


Figure 3.11: Simulated detector responsivity, noise and NEP at 360 GHz versus I_Q for different L_E.

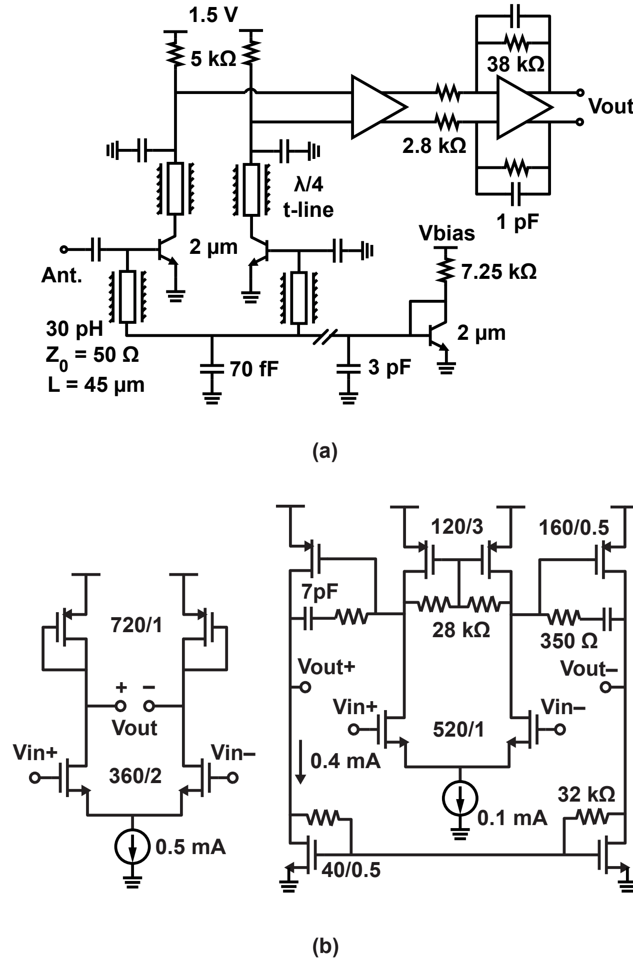


Figure 3.12: Schematic of the (a) complete detector, and (b) buffer and opamp.

Based on the proposed design, the detector is analyzed in Cadence in terms of S_{11} bandwidth, responsivity, output noise and NEP versus I_Q to determine the optimum emitter length and bias current (Figs. 3.10-3.11). Although $L_E = 1$ μm results in the best NEP, the associated S_{11} bandwidth is small. Therefore, $L_E = 2$ μm is chosen for its wider bandwidth at the expense of a slightly higher NEP at an optimum bias current of 50-150 μA.

3.2.3 Simulated System Response

Fig. 3.12(a) present the schematics of the complete detector. The single-ended antenna port is connected to one half of the detector, and the other half is used as a reference. For L_E = 2 μm, the simulated impedance at the base is Z_{IN} = 35–j32 Ω (including r_b in Fig. 3.8(c)), which can be matched using a shunt inductor of 30 pH (X = j68 Ω, Z_0 = 50 Ω and L = 45 μm). A

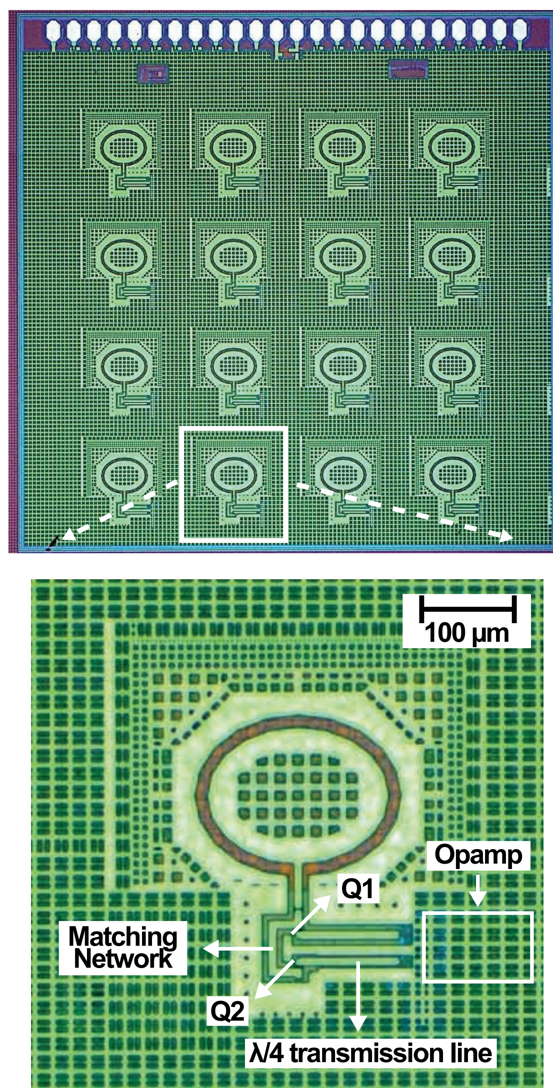


Figure 3.13: Microphotograph of the chip (2.6×2.6 mm^2) and a blow-up view of a single pixel (0.41×0.3 mm^2).

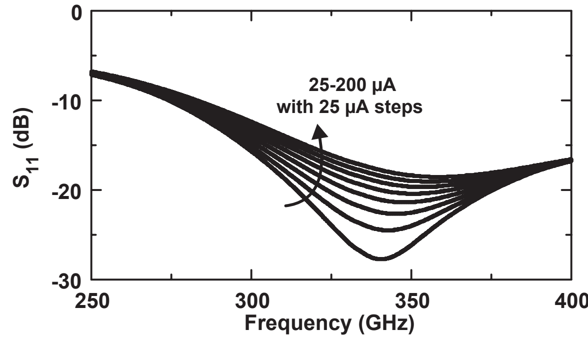


Figure 3.14: Simulated S_{11} of the detector and opamp.

similar circuit is placed at the reference detector for DC-matching purposes. A 70 fF capacitor with a series resonant frequency of 360 GHz (X $\approx$ 0 Ω) is used between the two transistors as an AC-short. This common AC-short node is also connected to a biasing network with an L_E = 2 μm transistor. The bias network creates a common-mode noise at the detector output which is attenuated by the differential buffer and opamp. The buffer is used to prevent any DC current flowing through the resistive network of the opamp stage. The buffer and opamp use large input transistors to result in a low 1/f corner frequency of less than 1 kHz with a gain of 22 dB and a 3-dB bandwidth of 3 MHz. The buffer/opamp input refered noise is 12 nV/Hz$^{1/2}$ (f $>$ 1 kHz) which is much less than the detector output noise of 35-55 nV/Hz$^{1/2}$ at I_Q = 50-150 μA. The opamp outputs are connected to a 16:1 and 16:4 differential multiplexers based on CMOS pass-gates. The multiplexers introduce insignificant loss and noise after the opamp and have no effect on the system responsivity and NEP.

The 4×4 SiGe imaging array and a blow-up of a single channel with the transmission-line matching network is shown in Fig. 4.3. Figs. 3.14-3.17 present the simulated S_{11}, responsivity and NEP versus frequency and bias current of a single channel including the RC extraction and EM models (using Sonnet [22]) of all transmission lines. The transistor input impedance is well matched with $S_{11} <$ -10 dB at 280-400$^+$ GHz for I_Q = 25-200 μA, and the responsivity has a broad peak of $\sim$90 kV/W and a 3-dB bandwidth of $>$ 150 GHz. The responsivity can also be defined at the antenna aperture, where the antenna effective area is taken as $A_e = \frac{\lambda^2}{4\pi}D$ (D = directivity). In this case, the antenna efficiency, ϵ, must be taken into account and the system responsivity is $\Re_s = \epsilon\Re$. The simulated $\Re_s$ is 24 $\pm$ 2 kV/W at 320-380 GHz.

The detector results in a simulated NEP of 8 pW/Hz$^{1/2}$ at 360 GHz for I_Q =50-150 μA, and the buffer/opamp 1/f noise corner frequency is $<$ 1 kHz (Fig. 3.16). The detector and system responsivity/NEP versus bias current is shown in Fig. 3.17. The design results in a system NEP

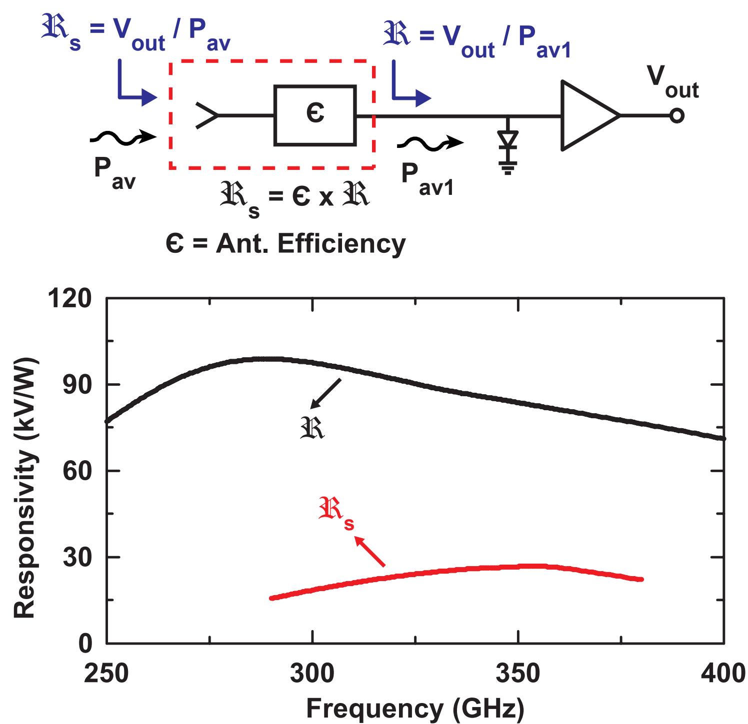


Figure 3.15: Simulated responsivity of the detector and opamp versus frequency at $I_Q = 100$ μA. System responsivity ($\Re_s$) including the antenna efficiency is also shown.

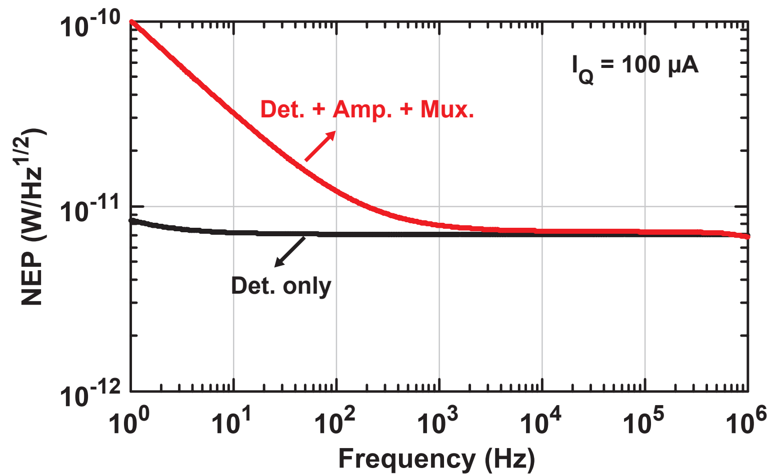


Figure 3.16: Simulated NEP of the detector alone and detector + amp. + mux. versus IF frequency at 360 GHz and I_Q = 100 μA.

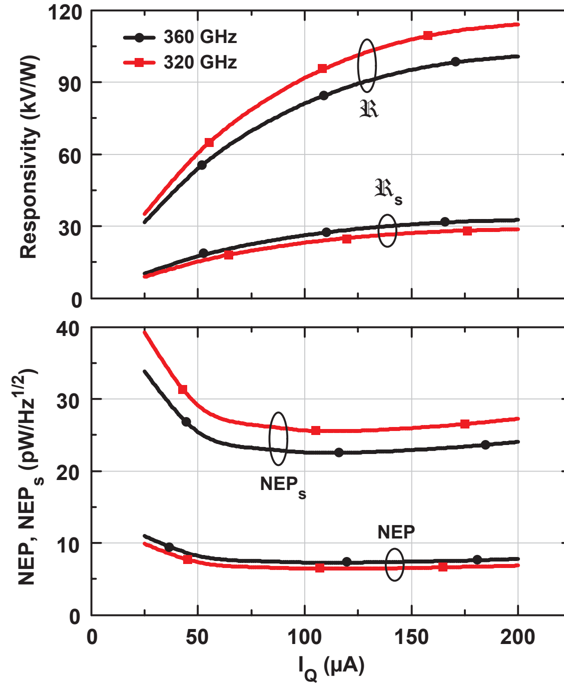


Figure 3.17: Simulated responsivity and NEP of the detector and opamp versus I_Q at 320 and 360 GHz. System responsivity/NEP including the antenna efficiency is shown with a subscript (i.e. $\Re_s$ and NEP$_s$).

of 26 ± 3 pW/Hz$^{1/2}$ at 320-360 GHz for I_Q = 50-150 μA.

3.3 Measurements

The 4x4 imaging array has been characterized using a far-field set-up as shown in Fig. 3.18. This ensures that a plane wave with a power density S is incident on the antennas, and the responsivity and NEP are defined as:

$$S = \frac{P_t G_t}{4\pi R^2} \tag{3.4}$$

$$P_{available} = S \times A_{physical} \tag{3.5}$$

$$\Re_s = \frac{V_{OUT}}{P_{available}} \tag{3.6}$$

$$NEP_s = \frac{V_n}{\Re_s} \tag{3.7}$$

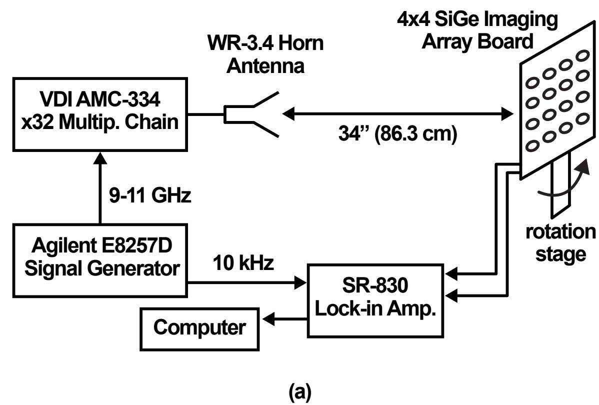
where P_t is the transmit power, G_t is the transmit antenna gain, R is the distance between the transmitter and the imaging array, and $A_{physical} = 0.35\lambda_0^2 = 0.243$ mm^2 at 360 GHz. Note that the antenna directivity also results in an effective aperture of $A_e = \frac{\lambda^2}{4\pi}D = 0.221$ mm^2 for a simulated directivity of D = 4.0 (6.0 dB) at 360 GHz, and is similar to the array cell size. It is better to use the physical array area for the available power since it takes into account all the power incident on the array.

The measurement system is based on a multiplier chain from Virginia Diodes, Inc. (VDI) capable of delivering 3-4 mW at 300-340 GHz from an Agilent source at 9-11 GHz [46]. The Agilent source is pulse modulated with 50 $\%$ duty cycle at 1-100 kHz, and the detected signal is sent to an SRS-830 lock-in amplifier. This eliminates the DC drifts in the system and results in accurate responsivity measurements. The measurement set-up is also used for pattern measurements, but with a rotation stage.

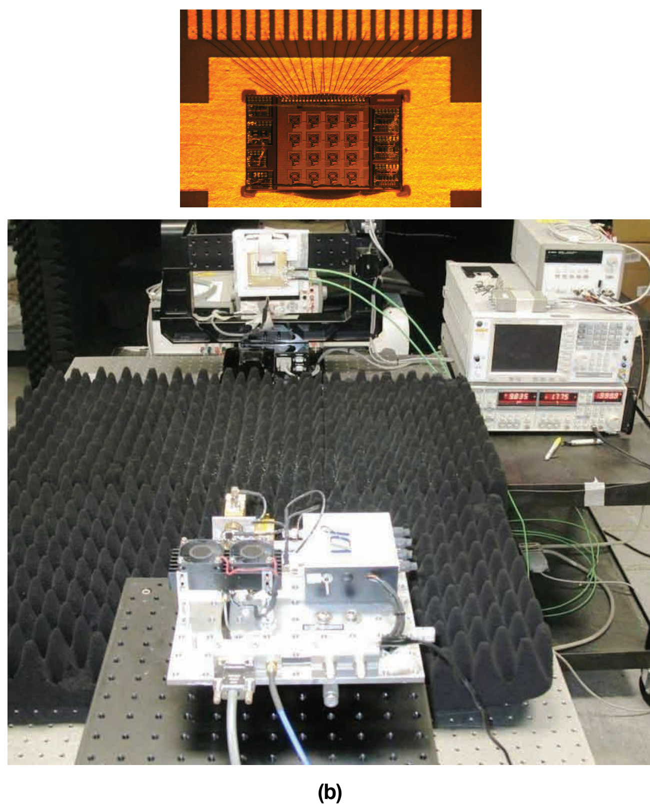
There are several sources of error in THz measurement setups, and these include: 1) accurate knowledge of the transmit power, 2) accurate knowledge of the transmit antenna gain, 3) ripple in the responsivity measurements versus distance and frequency due to standing waves in the measurement system, 4) variations across the array, and 4) ripple in the antenna patterns due to the finite ground-plane size. As will be seen below, these can contribute up to $\pm$ 2.1 dB of error to the measured responsivity and NEP values.

The measured transmit power and transmit antenna gain versus frequency are shown in Fig. 3.19(a). A difference of 0.5 dB exists between the measured transmit power values at UCSD and the values obtained from VDI. The transmit antenna gain was obtained using two identical antennas using the Friis transmission equation $P_r/P_t = (\lambda/4\pi R^2)G^2$ where P_t and P_r are measured using the same power meter. The measured antenna gain agrees well with the calculated values using horn antenna equations and as given by VDI [47]. Note that there is $\pm$ 0.5 dB ripple due to the standing waves in the measurement setup (Fig. 3.19(b)). In this experiment, the NEP values are based on the measured UCSD power as P_t and the calculated horn gain.

Fig. 3.20 presents the measured responsivity versus frequency at a detector bias current of 100 μA. The center frequency shifted to approximately 320 GHz with a 3-dB bandwidth of 308-333 GHz. Note the $\pm$ 0.9 dB ripple versus frequency at 100 MHz steps. This is not due to a low SNR at the detector (SNR $>$ 30 dB), but due to standing waves in the THz set-up. These standing waves are caused by the impedance mismatch between the antenna and the detector, and the large reflections from the ground plane (chip + FR-4 board). Similar standing waves



(a)



(b)

Figure 3.18: Measurement setup (a) block diagram and (b) photograph with inset of mounted imaging array chip on printed circuit board.

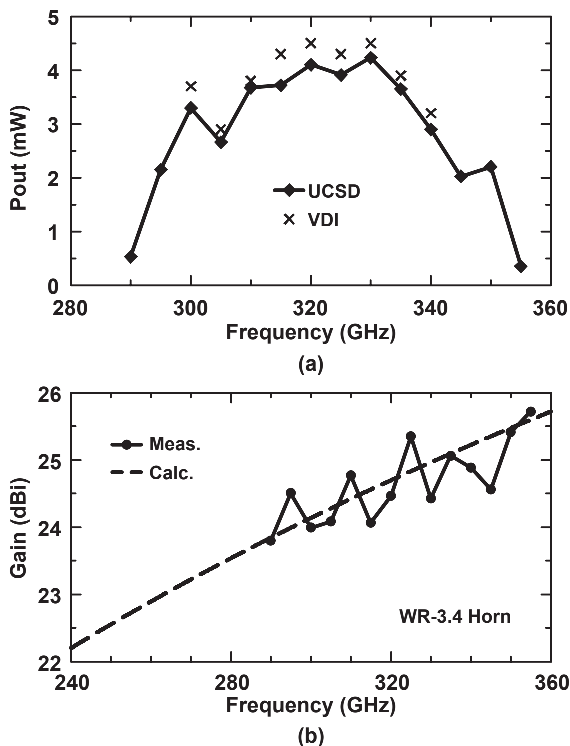


Figure 3.19: (a) Measured output power of VDI AMC-334 multiplier chain module, and (b) measured and calculated WR-3.4 horn antenna gain.

are observed if the frequency is kept constant and the transmit (or receive) antennas are moved in fractions of a wavelength using a micrometer. The quoted responsivity is obtained using a 16-point rolling average so as to reduce the effect of the standing waves.

Fig. 3.21 presents the measured low-frequency noise versus IF frequency. This is measured using an external low-noise amplifier with a 1/f corner frequency of a few Hz (SR-552 [48]) and an Agilent E4448A spectrum analyzer. The additional gain of the SR-552 amplifier has been calibrated out of Fig. 3.21. The measured noise includes the detector, operational amplifier and the 16:1 multiplexer, and agrees well with simulations. The additional 1/f noise below 10 kHz is due to the bias current noise and device mismatch in the buffer and opamp.

The measured H-plane patterns for three different antennas in the array also show a $\pm$ 1.2 dB ripple due to the finite ground plane and standing waves in the system (Fig. 3.22). The antennas show a cross-polarization component of $<$ -15 dB at 300-340 GHz. The quoted responsivity uses the average power at normal incidence and not the peak pattern values.

Fig. 3.23 presents the measured responsivity and NEP at 316 GHz and 100 kHz IF frequency versus bias current with and without a quartz superstrate. The NEP values are calcu-

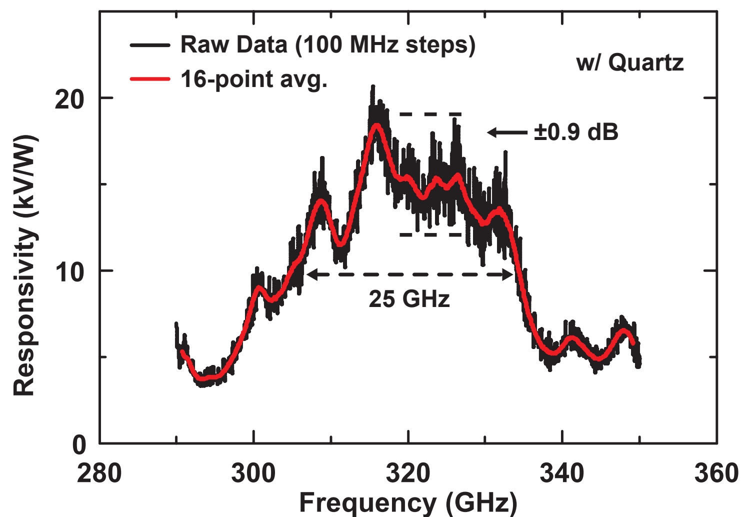


Figure 3.20: Measured responsivity versus frequency of a single pixel at $I_Q = 100\ \mu$A.

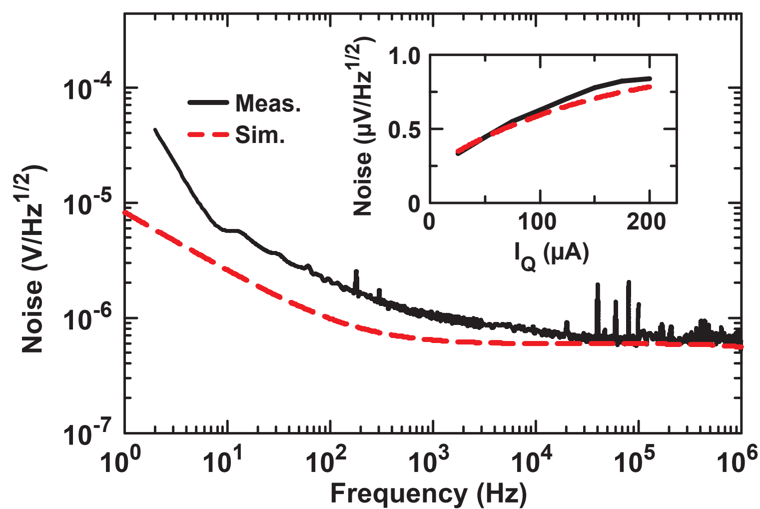


Figure 3.21: Measured and simulated output noise voltage versus freqeuency at $I_Q = 100\ \mu$A and versus I_Q at IF = 100 kHz.

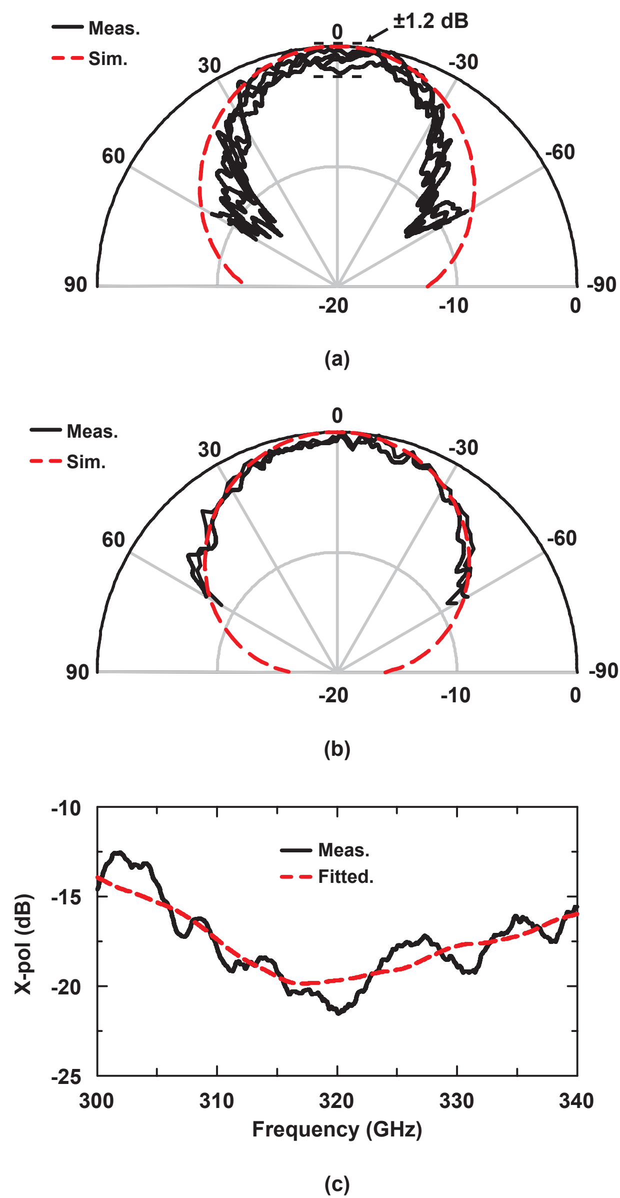


Figure 3.22: Measured and simulated H-plane antenna patterns at 315 GHz with (a) quartz (4 channels) and (b) without quartz (2 channels). (c) Measured X-pol of the slot-ring antenna with quartz versus frequency at $\theta = 0$.

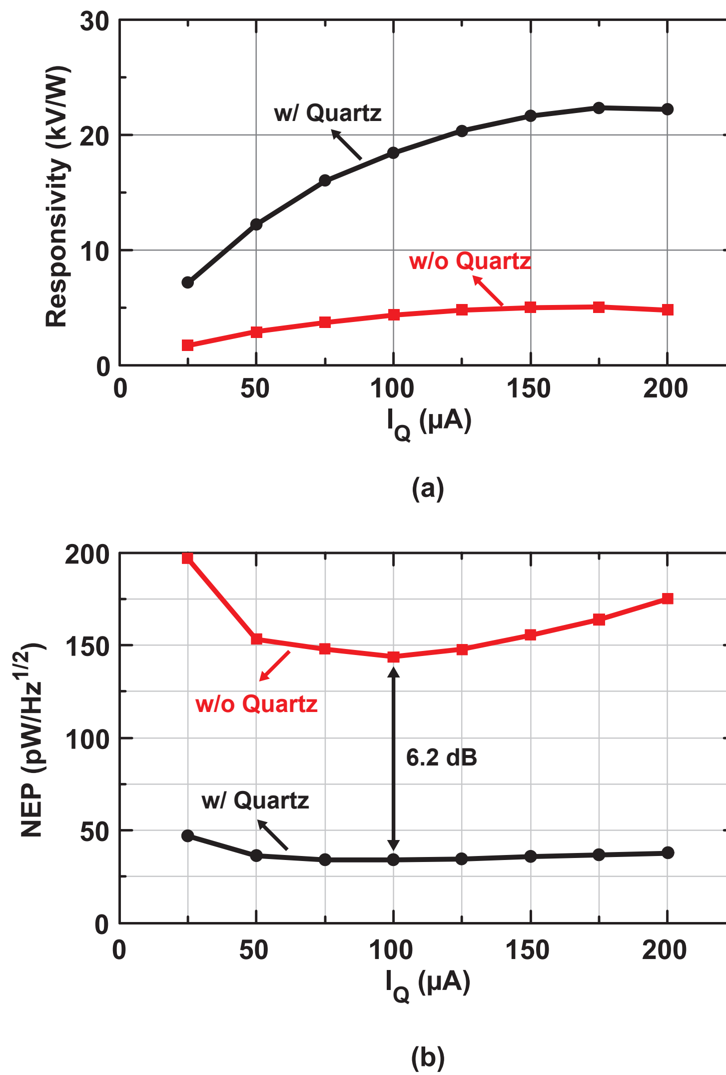


Figure 3.23: Measured (a) responsivity and (b) NEP versus I_Q with and without a quartz superstrate at 316 GHz (IF = 100 kHz).

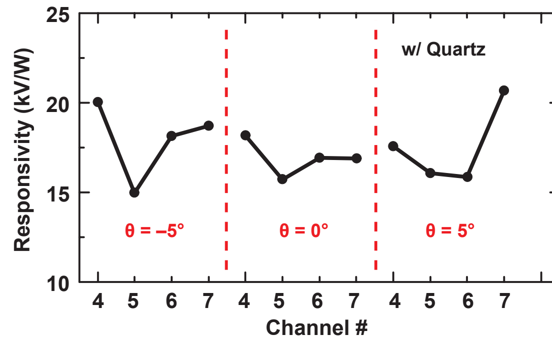


Figure 3.24: Measured responsivity versus channel and incidence angle at $I_Q = 100$ μA at 316 GHz for four detectors in a single row.

lated using (3.7). It is seen that the quartz superstrate results in ∼6 dB better performance than a standard on-chip slot-ring antenna (simulations indicate a 4.5 dB improvement at 320 GHz). A minimum NEP of 34-36 pW/Hz$^{1/2}$ is obtained over a bias current of 50-150 μA using the average values. The 3-dB bandwidth for the NEP is identical to the responsivity and is 308-333 GHz.

3.4 Discussion

As seen in the measurements, there is a $\pm$ 2.1 dB error in the measured responsivity and NEP values (Table 3.2). This is clearly seen in Fig. 3.24 where four detectors in a row in the 4×4 array are measured at slightly different angles from normal incidence, and result in $\pm$ 0.7 dB variation versus location and incident angle. This is due to the antenna pattern ripple versus angle which, in turn, is due to finite ground plane effects. The measured data shows that care should be used in describing the measurement system and all its errors. The published papers on THz imaging do not report such detail in their measurement set-ups and it is not clear if average or best values are used in their quoted NEP values.

The measured NEP values (Fig. 3.20) are based on a 16-point rolling-average versus frequency and also on the average value in the measured patterns at normal incidence. If peak values for the responsivity and antenna patterns are used, the minimum NEP would be 21 pW/Hz$^{1/2}$ (approximately 2.1 dB better). Also, note that the measured values were achieved while meeting the strictest metal-fill density rules (Case 1 in Fig. 3.5) with an antenna efficiency of about 30%. Several reported systems do not use any metal-fill which is acceptable for a small test chip, but is not acceptable for a production wafer which is full of imaging arrays. The exclusion of the

Table 3.1: Performance Summary

	[10]	[11]	[12]	This work
Technology	0.13-μm CMOS	0.25-μm CMOS	65-nm CMOS	0.18-μm SiGe BiCMOS
Frequency (THz)	0.28	0.65	0.86	0.32
Responsivity (V/W)	5k	80k	140k	18k
NEP (pW/Hz$^{1/2}$)	29	300	100	34^{a,b}
3-dB Bandwidth (GHz)	20	N/A	270	25
Metal-Fill	Excluded (0%)	N/A	N/A	30%
Antenna Type	Microstrip	Microstrip	Ring ant. + Lens	Slot-ring ant. w/ quartz superstrate
Power Consumption Detector Only (μW)	60	0^c	0^c	150
Power Consumption (mW/pixel)^d	1.3	5.5	2.5	2.4

^{a} NEP drops to 21 pW/Hz$^{1/2}$ if peak values for responsivity and antenna patterns are used.

^{b} If metal-fill below the antenna were omitted, average (best) NEP would be 16 (10) pW/Hz$^{1/2}$.

^{c} Cold-FET detector.

^{d} Power consumption of a single detector together with an opamp.

Table 3.2: Sources of Error in Measurements

Sources of Error	dB
Power Meter*	±0.3
Horn Gain**	±0.5
Resp. vs Freq.	±0.9
Pattern (θ)	±1.2
Sub-total	±2.1
Total	±2.9

*UCSD measured values are used.

**Calculated values are used.

metal-fill (case 3) increases the antenna efficiency to $\sim$60% and reduces the average system NEP values to 16 pW/Hz$^{1/2}$ and the best system NEP values to 10 pW/Hz$^{1/2}$.

3.5 Conclusion

A 0.32 THz 4×4 imaging array has been presented with state-of-the-art performance in the 0.2-0.6 THz range. Detailed measurements show that careful attention must be used in order to report accurate values for the system NEP. In particular, a $\pm$ 2.1 dB ripple in the NEP versus frequency and angle of incidence has been found due to standing waves in the THz measurement system and finite ground plane effects. In addition, it was found that metal-density rules drop the on-chip antenna efficiency by $\sim$3 dB, and therefore, it is important to report if the antennas used meet all the back-end processing rules or if exceptions are taken. The demonstrated array results in an average NEP of 34 pW/Hz$^{1/2}$ at 320 GHz using on-chip antennas meeting the strictest metal-density rules.

3.6 Acknowledgement

This work was supported by the DARPA GRATE program under a subcontract from Jazz Semiconductor, Inc., Newport Beach, CA. The authors would like to thank Quik-pak, San Diego, CA for board fabrication and Virginia Diodes, Inc., Charlottesville, VA for the multiplier-chain.

Chapter 3 is mostly a reprint of the material as it is submitted for publishing to IEEE Journal of Solid-State Circuits, 2013. Mehmet Uzunkol; Ozan D. Gurbuz; Fatih Golcuk; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4

60 GHz CMOS Amplifiers, Phase Shifters and Switches

4.1 Introduction

Silicon-based 60 GHz phased array systems using the All-RF architecture have been investigated for short-range Gbps communication links [49,50]. They have also been demonstrated at 35–85 GHz for satellite communications and automotive radars [51]. Two main designs have emerged for the phase shifter: The vector modulator [52] and switched-LC networks [53]. The vector modulator allows for design flexibility, but results in increased power consumption for high linearity and a high NF (larger than 12 dB) since it uses two amplifiers and a lossy I/Q network. On the other hand, the switched-LC approach suffers from high loss and NF due to the non-ideal CMOS switches in the 130 nm or 90 nm CMOS nodes, but has a power handling of 7–12 dBm depending on the CMOS node. Therefore, high-gain amplifiers are used in front of both phase shifter types, which results in either an input P_{1dB} of –30 to –20 dBm (for low power operation) or high power consumption for an input P_{1dB} of –15 to –10 dBm.

Millimeter-wave CMOS switches are used for 60 GHz high data rate communication systems for switched beam antennas, multi-band receivers on chip, built-in-self-test (BIST) circuits, and instrumentation systems [1, 54]. 45 nm CMOS SOI amplifiers, doublers and switches have been demonstrated with excellent performance up to 200 GHz [55, 56]. Previously, mm-wave single-pole multiple-throw switches have been demonstrated using 0.13-μm, 90-nm and 65-nm CMOS circuits, and have shown wideband performance [57–61]. Recently, a 60 GHz SPDT switch has been presented with excellent performance using metamorphic HEMTs [62].

However, the InGaAs process has lower integration complexity and yield than advanced CMOS nodes. As the channel length of CMOS transistor becomes smaller, R_{on} decreases and results in lower insertion loss, essentially resulting in a similar performance to pHEMT switches. Still, the power handling of pHEMT switches is better than CMOS switches due to higher voltage operation.

This chapter presents a 65 GHz CMOS SOI switched-LC phase shifter with low insertion loss, and shows that 65 GHz phased array front-ends can be designed with low power consumption and high linearity. This chapter also presents a high-performance 60 GHz SPDT switch realized in a standard 90-nm CMOS technology. The resulting SPDT switch shows state-of-the-art insertion loss and isolation from 50 to 70 GHz, and a IP_{1dB} of $\sim$ 13.5 dBm. The application areas are in 60 GHz CMOS transceivers for Gbps communications [1, 54], and in switched-beam antennas for wide-angle spatial coverage [63].

4.2 A 65-GHz LNA/Phase Shifter with 4.3-dB NF in 45 nm CMOS SOI

4.2.1 Design

The LNA and phase shifter are designed using the IBM 45 nm CMOS SOI process (Fig. 4.1). The inductors are implemented using G-CPW transmission lines except the 175 pH spiral inductor in the LNA, and the capacitors are standard IBM-library vertically stacked interdigitated metal finger caps (MFCs). The G-S-G RF pads, LNA and each phase shifter bit are designed with 50 Ω input and output impedances. A full-wave EM solver, Sonnet [22], is used to simulate all the transmission lines, interconnections and pads.

The LNA is a two-stage cascode amplifier with emitter degeneration for simultaneous noise and power matching (Fig. 4.1(a)). 30-μm wide floating-body transistors with 1-μm finger width are used. 10-Ω resistors are placed at the Vdd node for stability considerations, and do not affect the LNA, except the 60 mV voltage drop. A resistor of 250 Ω is used to result in a wide-band output impedance match. The measured LNA peak gain is 12.5 dB with a NF of 4.0 dB at 65 GHz [64]. The measured output 1dB power compression point (OP_{1dB}) is –2 dBm.

The 3-bit phase shifter consists of cascaded 180°, 45° and 90° phase shifting elements (Fig. 4.1(b)). The 180° phase shifter is designed using switched high-pass/low-pass networks [50]. The high-pass T-network results in a 90° phase lead, and consists of two series capacitors (53 fF) and a shunt transmission line (130 pH), whereas the low-pass π-network results in a 90°

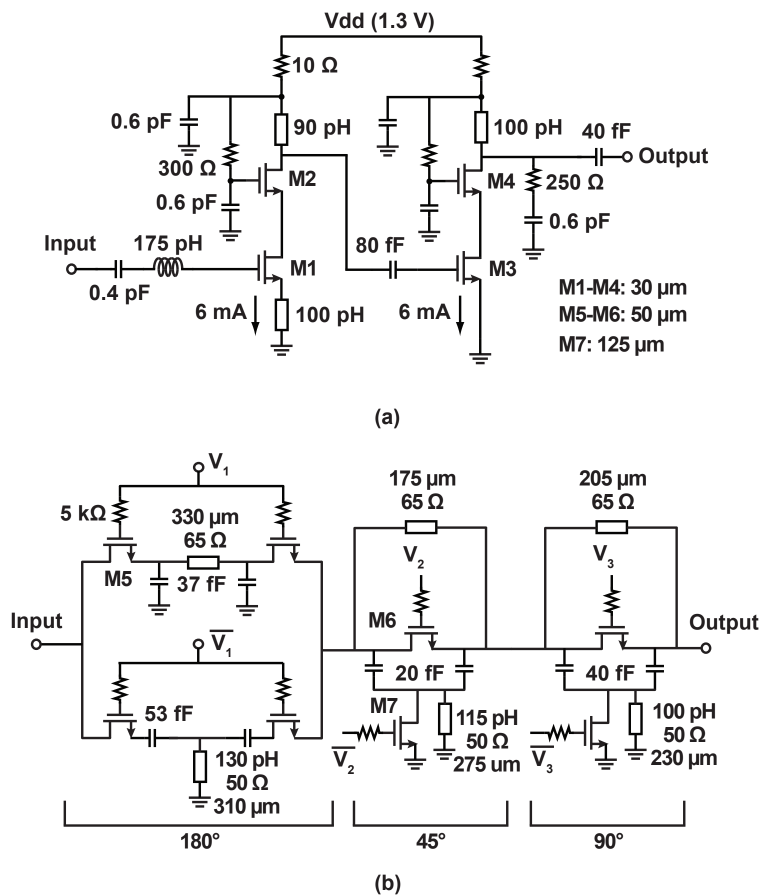


Figure 4.1: Schematic of the V-band (a) LNA and (b) 3-bit phase shifter.

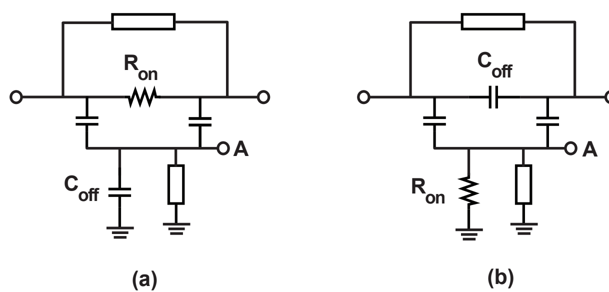


Figure 4.2: Equivalent circuit model of the 45°/90° phase shifters in the (a) bypass and (b) phase-delay states.

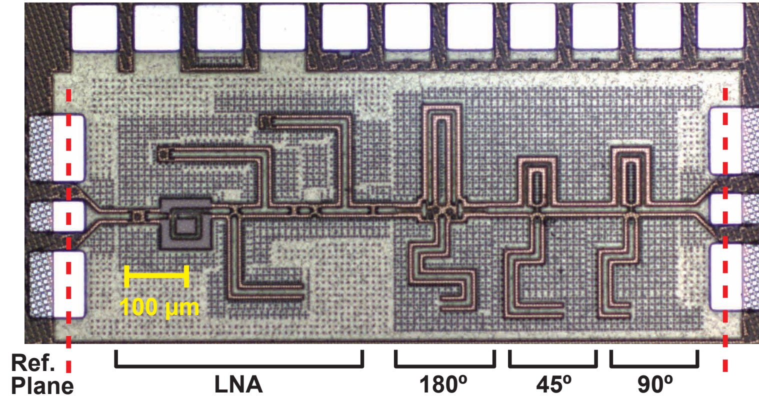


Figure 4.3: Microphotograph of the LNA/phase shifter.

phase lag and consists of an inductive transmission line ($Z_0 = 65\ \Omega$, $l = 330\ \mu$m) and two shunt capacitors (37 fF). The 90° and 45° phase shifters employ low-pass π-networks, and are based on switching between a phase delay and a bypass state. When M6 is on and M7 is off, the M7 off-state capacitance (C_{off}) resonates with the shunt transmission line and creates an open-circuit at node A (Fig. 4.2). The M6 on-resistance (R_{on}) therefore results in a bypass state. When M6 is off and M7 is on, the series transmission line together with the two shunt capacitors form a low-pass network, which results in a phase delay. Gate bias resistors of 5 kΩ are used for all switches in order to prevent the RF signal leakage through the gate bias lines.

A low R_{on} is desired for the shunt switch (M7) so that the CLC π-network in the phase-delay state results in low loss and accurate phase delay. At the same time, the impedance at node A needs to be high in the bypass state, and this is achieved by resonating M7 C_{off} with an inductor. A shunt switch transistor width of 125 μm (50 $\times$ 2.5 μm, $R_{on} = 2.8\ \Omega$ and $C_{off} = 62$ fF) is therefore chosen in this design. For the 90° and 45° phase shifters, the inductor values are 100 pH ($X = 38\ \Omega$) and 115 pH ($X = 43\ \Omega$) respectively, with a Q of 13 at 60 GHz. The loss in the 90° and 45° phase delay states is mostly determined by the transmission-line Q and two shunt capacitors, and is typically 1–1.5 dB at 60 GHz. In the bypass state, the loss is determined by the series switch loss, and is 2–3 dB at 60 GHz in a bulk CMOS technology. This creates a gain error between the bypass and phase delay states. However, in an advanced SOI CMOS process, the gain error could be minimized by choosing a wide series switch transistor without incurring a large substrate capacitance. Therefore, a transistor width of 50 μm (20 $\times$ 2.5 μm, $R_{on} = 7\ \Omega$ and $C_{off} = 25$ fF) is chosen for the series switch (M6) which results in a loss of 1–1.5 dB for the 45° and 90° phase states.

Fig. 4.3 presents the LNA/phase shifter chip photograph (0.55 $\times$ 1.2 mm^2 including the

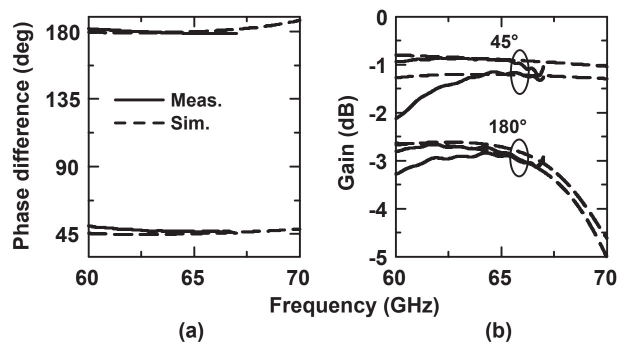


Figure 4.4: Measured and simulated (a) phase difference and (b) gain of 180° and 45° phase shifter test-cells.

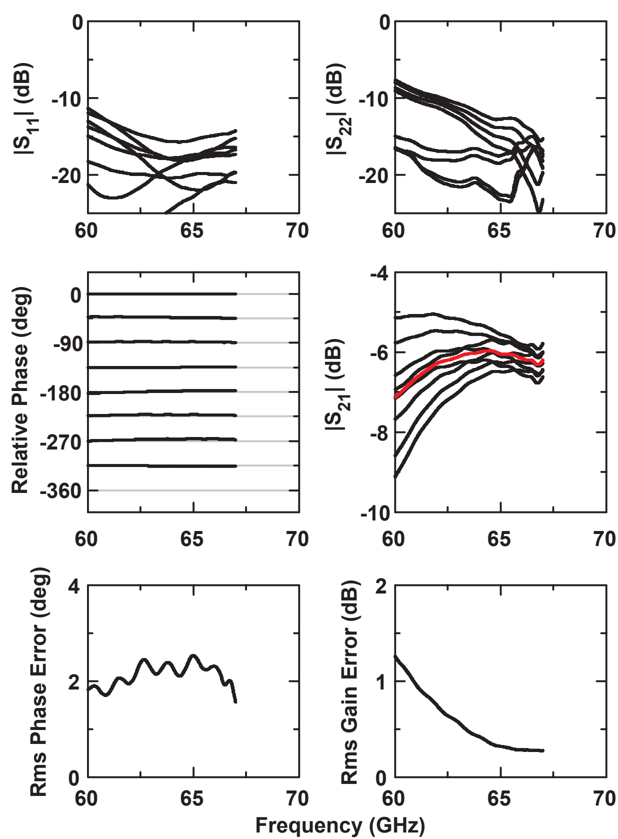


Figure 4.5: Measured S_{11}, S_{22}, S_{21}, relative phase, rms phase error and rms gain error of the 3-bit phase shifter.

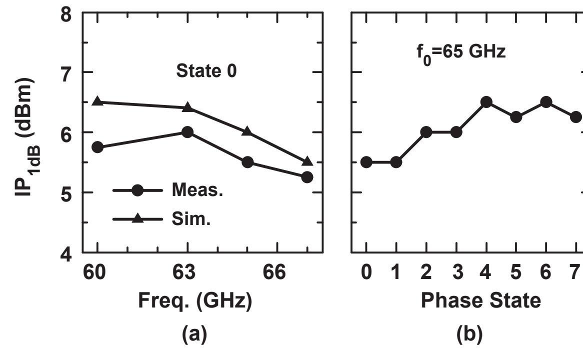


Figure 4.6: Measured and simulated input P_{1dB} of the 3-bit phase shifter versus (a) frequency and (b) phase state.

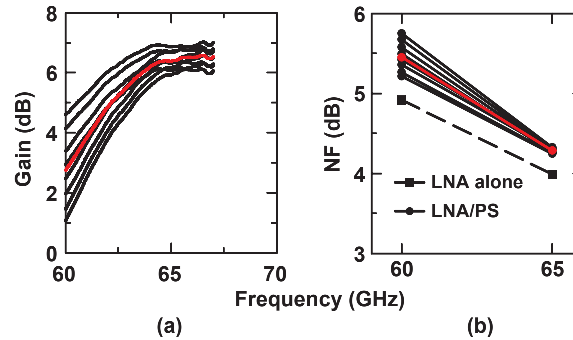


Figure 4.7: Measured (a) gain and (b) noise figure of the LNA/phase shifter for different phase states. The red curve is the average of all phase states.

pads).

4.2.2 Measurements

The 3-bit phase shifter was measured on-chip with an Agilent E8361 67 GHz PNA using SOLT calibration to the probe tips. Fig. 4.4 presents the simulated and measured phase difference and the insertion loss of individual 180° and 45° phase shifting cells. The measured insertion loss of the 45° and 180° phase shifters are 0.9–1.2 dB and 2.8–2.9 dB, respectively at 65 GHz.

Fig. 4.5 presents the measured 3-bit phase shifter. The input return loss is less than –10 dB at 60–67$^+$ GHz, and the output return loss is less than –8 dB at 60–67$^+$ GHz. The measured loss of the 3-bit phase shifter is 6.0±0.5 dB at 65 GHz, and the average loss is 6.0 dB (red curve in Fig. 4.5). The measured RMS gain error is 0.3 dB at 65 GHz and is less than 1.3 dB at 60–67$^+$ GHz. The measured RMS phase error is less than 2.5° at 60–67$^+$ GHz. The measured input

Table 4.1: LNA/Phase Shifter Comparison

	This Work	[52]	[49]*	[65]*
Technology Node	45-nm CMOS	90-nm CMOS	65-nm CMOS	65-nm CMOS
Frequency (GHz)	60–67^{+}	53–65	57–62	58–64
Rms gain error (dB)	$<$1.3	N/A	$<$1.7	$<$1.3
Rms phase error (degrees)	$<$3	N/A	$<$12	$<$8
Peak Gain (dB)	6.5	12.5	25	12
NF (dB)	$<$5.5	$<$7.5	N/A	$<$8.5
IP$_{1dB}$ (dBm)	–13.5	–13.3	–21.5	–16
Power Consumption (mW)	15	60	45	78
Phase Shifter Topology	3-bit passive	5-bit active	4-bit passive	4-bit active

*1-element of the receiver phased array.

P_{1dB} is about 6 dBm, and is relatively constant versus frequency and phase state (Fig. 4.6). The input P_{1dB} of the phase shifter is high enough so as not to limit the overall P_{1dB} when preceded by an LNA.

The measured average gain and NF of the LNA/phase shifter is 6.5 dB and 4.3 dB, respectively at 65 GHz (Fig. 4.7). The cascaded NF is only degraded by 0.3 dB since the phase shifter has low loss. The measured 3-dB bandwidth of the LNA/phase shifter is 59.5–61.6 (about 60.6) to 67^{+} GHz for different phase states. The overall input P_{1dB} is limited by the LNA, and is –13.5 dBm at 65 GHz.

The LNA and phase shifter were designed at 60 GHz, but the measured results show that the center frequency shifted to 65 GHz for both designs. Although parasitic RC extraction and full electromagnetic simulations were employed, this 8% frequency shift could be due to inaccurate transistor models since the CMOS models are mostly for digital designs. The results at 65 GHz are still state-of-the-art and show the validity of the design. Table 4.1 summarizes this work and compares the results with other LNA/phase shifter designs.

4.3 A Low-Loss 50–70 GHz SPDT Switch in 90 nm CMOS

4.3.1 Design

The schematic and cross section view of the SPDT switch are shown in Fig. 1. The IBM 9 RF technology is used with nMOS f_t/f_{max} of 130/140 GHz and 8 metal layers. The top two dielectric layers are 4 and 3 μm thick and allow relatively low-loss CPW lines at 60 GHz. A 50 Ω line is built using a 12/10/12 μm grounded CPW line with a simulated loss of 0.65 dB/mm at 60 GHz. This results in a Q of $\sim$17 for transmission line inductors. The switch is based on a $\lambda/4$ tuned transmission-line approach with a single 90-nm nMOS shunt transistor. In the off-state (V_c = 0 V), the transistor capacitances together with the substrate resistance transform into an equivalent RC network. An R_{sub} = 50 Ω, C_j = 46.5 fF and C_s = 65.8 fF (W = 250 μm FET) result in R_{eq} = 265 Ω and C_{eq} = 94.7 fF. For an R_{sub} of 100–150 Ω, one can obtain R_{eq} = 430–620 and C_{eq} = 90 fF. The high substrate resistance is realized using a small number of substrate contacts around the nMOS transistor [Fig. 1(b)].

The output matching network consists of a shorted stub with Z_s = 50 Ω in shunt with the transistor and cancels out the equivalent off-state capacitance. In the off-state, the shunt transistor with the shorted stub acts as a large resistance to ground. In the on-state (V_c = 1.2 V), the transistor acts as a small resistance to ground with R_{ch} = 2 Ω for W = 250 μm, and results in high isolation. The isolation can be further increased using very wide transistors. However, wide transistors have a high equivalent capacitance in the off-state and result in a reduced bandwidth. Fig. 2(a) presents the tradeoff between isolation, bandwidth, and insertion loss using a $\lambda/4$ transformer impedance of 50 Ω and the IBM models for the transistors and transmission lines. The stub loss is taken into account due to its finite Q ($\sim$ 17 at 60 GHz) and the bandwidth is defined at the –10 dB S_{11} values. A FET width of 250 μm is chosen for an isolation of 28 dB, insertion loss of 1.6 dB at 60 GHz, and results in 28 GHz bandwidth. The corresponding shunt inductor is 80 pH and is synthesized using a 200-μm-long CPW stub. The transmission lines are 610 μm long. The insertion loss is mostly determined by the Q of the shunt-stub and the $\lambda/4$ line.

The impedance transformation of a lossy $\lambda/4$ transmission line is given by

$$Z_{IN} = Z_0 \frac{Z_0 + Z_L \tanh(\alpha l)}{Z_L + Z_0 \tanh(\alpha l)} \tag{4.1}$$

where Z_0 is the characteristic impedance (50 Ω), Z_L is the load impedance, α is the loss of the line (0.075 Np/mm at 60 GHz), and l is the length of the $\lambda/4$ line (Fig. 3). Port 2 is specified as the signal path, whereas port 3 is the isolated port (R_{ch} = 2 Ω). The off-state resistance cannot

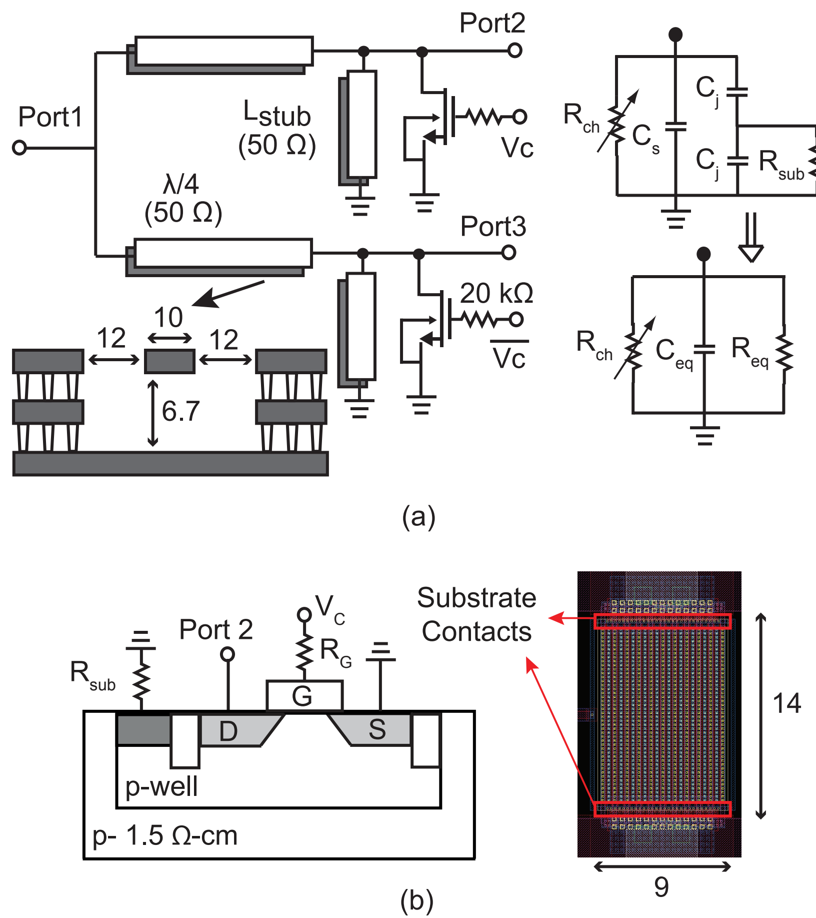


Figure 4.8: (a) Schematic of SPDT switch; (b) cross-sectional view and layout of the transistor. Dimensions are in micrometers.

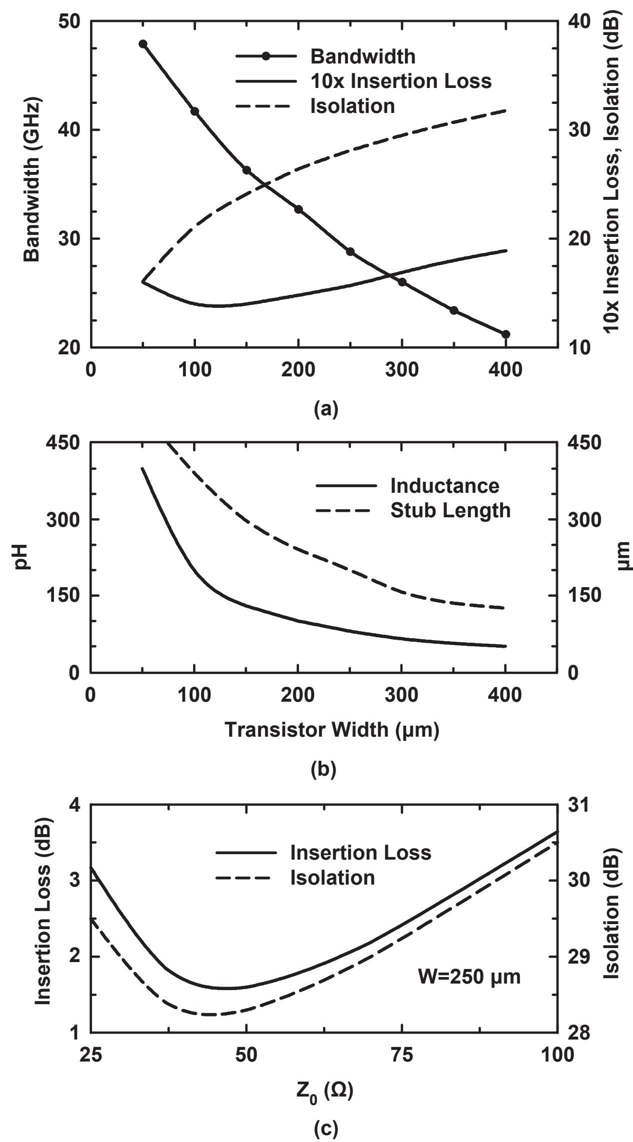


Figure 4.9: (a) Simulated insertion loss, isolation at 60 GHz and bandwidth versus transistor size; (b) inductance and stub length versus transistor size; (c) insertion loss and isolation at 60 GHz versus Z_0 of the $\lambda/4$ line.

be accurately calculated since it is layout dependent, but is usually larger than 500 Ω [66]. The equivalent resistance is $\sim$ 300 Ω including the shunt-stub Q. This results in $\sim$ 50 Ω at port 1 (57.5 Ω in parallel with 600 Ω), and S_{21} = –1.6 dB, S_{31} = –28 dB.

A transistor width of 125 μm results in an insertion loss of 1.4 dB but at the expense of a large shunt inductor (155 pH) and a larger stub (340 μm). A higher inductance results in more sensitivity in the resonant frequency ($f_0 = 1/2\pi\sqrt{LC_{eq}}$), and was not chosen due to the uncertainty in the transistor model and C_{eq}. The insertion loss and isolation for a transistor width of 250 μm and L_s = 80 pH are also simulated at 60 GHz using IBM models versus the $\lambda/4$ transformer impedance Z_0 [Fig. 2(c)]. It is seen that for 50 Ω input and output ports, 39 $\Omega < Z_0 <$ 58 Ω results in an insertion loss $<$ 1.8 dB with a broad minimum of 1.6 dB at Z_0 = 42–50 Ω.

4.3.2 Measurements

The SPDT switch is fabricated in a 90-nm CMOS process (Fig. 4). The transmission lines, T-junctions, and CPW pads are simulated using full EM methods (Sonnet [22]) so as to obtain accurate dimensions. The area bounded by the reference planes, as shown in Fig. 4, is EM-simulated in one piece including the transistor contacts. The coupling between the two shorted-stubs is $<$ –30 dB. The active chip area is 0.55 $\times$ 0.5 mm^2 and could be reduced by folding the $\lambda/4$ transmission lines. On-chip S-parameter measurements are done using a 67 GHz Agilent E8361A PNA. The pad loss is automatically taken out of the measurements using on-chip TRL calibration which includes open, thru and line sections built on the same wafer. The simulated pad-loss is 0.25–0.3 dB at 60 GHz, the insertion loss would increase by 0.5–0.6 dB at 60 GHz if the pads are taken into account.

The measured input and output reflection coefficients show a shift from 60 GHz to 54.6 GHz, and can be accurately fitted using an additional capacitance of 22 fF in parallel with the transistor model (R_{eq}, C_{eq}). It can also be fitted solely by an additional inductance of 21 pH to L_s, or a combination of two additional capacitances and inductances (10 fF, 10 pH). These values are low enough to be within the error of the EM simulations and the transistor model. Since R_{eq} is not well known, the impedance transformation through the $\lambda/4$ t-line causes a slight difference between the fitted and measured S_{11}. Still, the measured S_{11} and S_{22} are $<$ –8 dB from 50 to 67 GHz [Fig. 5(a)].

The measured insertion loss of SPDT switch is 1.5–1.6 dB at 53–60 GHz, and remains $<$ 2.0 dB from 50 to 67 GHz, showing very wide-band performance [Fig. 5(b)]. Ports 2 and

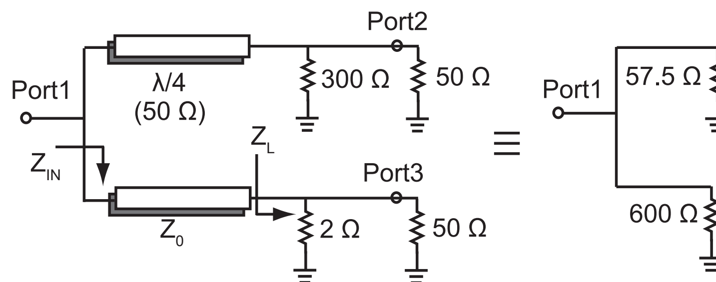


Figure 4.10: Impedance transformation of the $\lambda/4$-based SPDT switch.

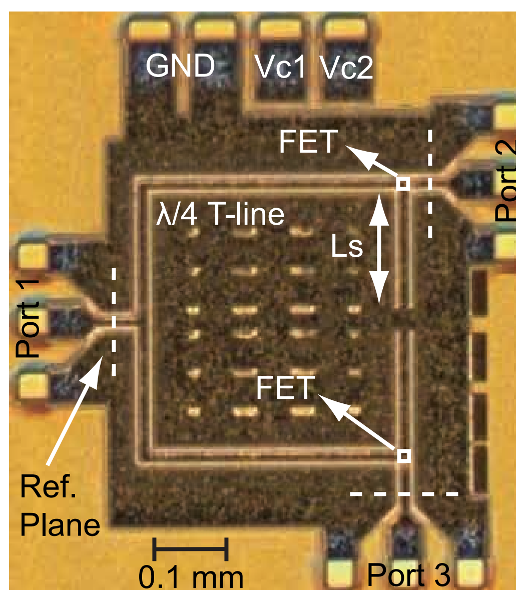


Figure 4.11: Microphotograph of SPDT switch. The size is 0.5×0.55 mm^2, not including the pads.

3 result in identical responses. The measured input-to-output (S_{31}) isolation is 25 dB and the measured isolation between the output ports (S_{32}) is $>$ 27 dB from 50 to 67 GHz and again both output ports result in almost identical response [Fig. 5(c)]. In the isolation measurements, one of the output ports is terminated with a fixed waveguide termination connected to the 1.85 mm CPW probe using a waveguide-to-coaxial adaptor (50–75 GHz). This results in the ripples especially below 50 GHz.

The SPDT switch has a simulated IP_{1dB} of 13.5 dBm, but this could not be measured due to power limitations at 60 GHz (compression is not observed up to an input power of 10 dBm). Fig. 6 presents the measured IIP3 which is 22.5 dBm at 60 GHz and agrees well with simulations. Power handling is limited mainly by the voltage swing at the gate node coupled from the drain through the junction capacitances [66]. When the power level increases, the off-state transistor starts to turn on and results in a degradation of the insertion loss (i.e., assuming V_{th} = 0.6 V and the junction capacitances are same, a 1.2 V peak amplitude swing at the drain would cause the transistor to turn on instantaneously).

The switching time of the SPDT switch is determined by the gate biasing resistor and the junction capacitance at the gate. The simulated switching time at 60 GHz is 0.15–3 ns for R_g = 1–20 kΩ (Fig. 7). The switching time could be improved to 0.15 ns using R_g = 1 kΩ at the expense of a 0.05 dB increase in loss (Fig. 8). Therefore, this switch could be used as a matched 5 Gbps ASK modulator [17, 18, 67] or for short-pulsed UWB automotive radars [68–70].

Table 4.2 summarizes the 90-nm SPDT switch design and compares with other state-of-the-art SPDT switches.

4.4 Conclusion

A 65 GHz 3-bit phase shifter with an integrated LNA is presented. The LNA/phase shifter achieves a gain of 6.5 dB, a noise figure of 4.3 dB and an input P_{1dB} of –13.5 dBm at 65 GHz with only 15 mW DC power consumption. The RMS phase and gain error is less than 2.5° and 1.3 dB at 60–67^{+} GHz. Also, this chapter has presented a wideband SPDT switch from 50 to 70 GHz with excellent insertion loss and isolation performance. The power handling is limited to 13–14 dBm which is sufficient for most short-range 60 GHz communication systems.

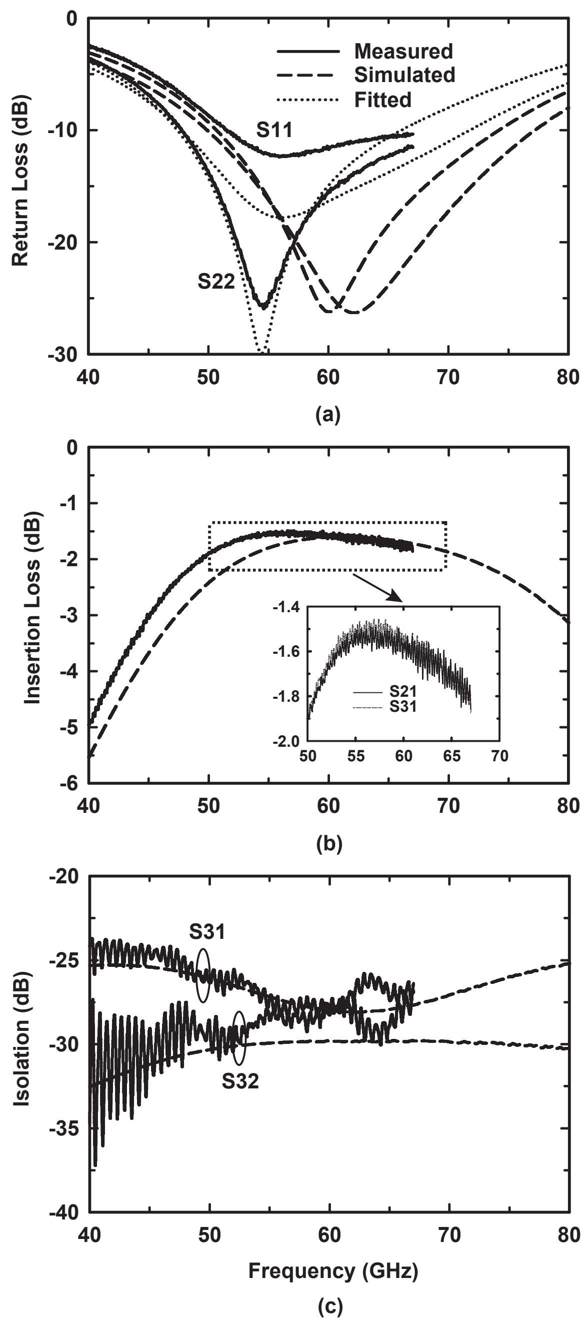


Figure 4.12: Measured and simulated (a) return loss, (b) insertion loss, (c) isolation of the SPDT switch.

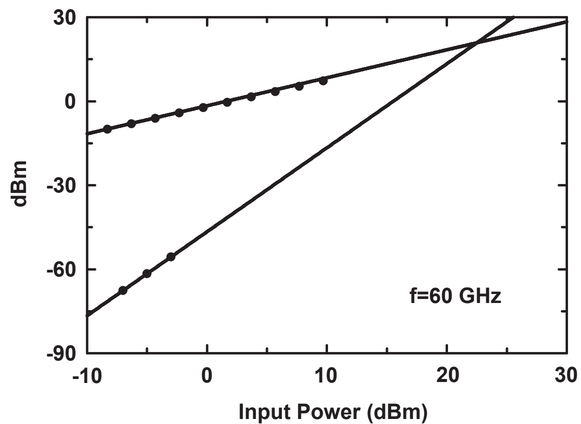


Figure 4.13: Measured IIP3 of the SPDT switch at 60 GHz.

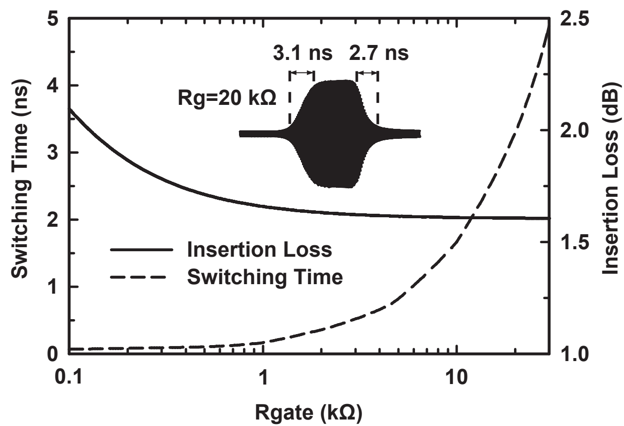


Figure 4.14: Simulated switching time performance of the SPDT switch versus R_gate at 60 GHz.

Table 4.2: SPDT Switch Comparison

	This Work	[58]	[59]	[60]	[62]	[6]	[71]	[72]*
Technology Node	90-nm CMOS	90-nm CMOS	65-nm CMOS	0.13-μm CMOS	100-nm CMOS	0.13-μm CMOS	90-nm CMOS	65-nm CMOS
Frequency (GHz)	50–70	50–94	70–94+	45–70	43–80	85–105	50	57–66
Min. IL (dB)	1.5	2.7	4.2	2.0	1.4	2.3	3.4	2.4
Isolation (dB)	>25	>27	>25	>30	>30	21	13.7	>21
Return Loss (dB)	<-8	<-10	<-10	<-10	<-9	<-10	<-10	<-10
IP_{1dB} (dBm)	13.5	15	N/A	13	>16	13	14	13
Size (mm^2)**	0.27	0.14	N/A	0.12	0.5	0.18	0.003	0.15

*: Simulation results.

**: Estimated size not including the pads.

4.5 Acknowledgement

This work was supported by the Intel Corporation and University of California (UC) Discovery program, Dr. Ian Young and Dr. Jad Rizk, program monitors. The authors thank Yusuf A. Atesal and Berke Cetinoneri for technical discussions.

Chapter 4 is mostly a reprint of the material as it appears in IEEE Microwave and Components Letters, 2012 and IEEE Journal of Solid-State Circuits, 2010. Mehmet Uzunkol; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 5

150–300 GHz Switches, Detectors and Imaging Arrays in 45 nm CMOS SOI

5.1 Introduction

Millimeter and terahertz applications circuits include passive and active imaging systems, and short-distance communications and sensing [7, 10, 73, 74]. It is also possible to integrate an efficient antenna in the CMOS backend above 100 GHz, thereby removing the need for transitions in and out of the wafer, which can be very lossy [10, 73, 75]. Some essential components are low-noise amplifiers, wideband mixers and efficient multipliers [55, 76, 77]. Other essential components are SPDT switches for transmit-receive functions, and SPST switches for signal routing and modulation. D-band (110–170 GHz) CMOS SPDT switches have been demonstrated with insertion loss of 3–4 dB [78, 79]. As in all designs, the CMOS switches must have low insertion loss, high isolation, and relatively high power handling capabilities so as to be used in mm-wave systems.

Silicon systems at $>$ 150 GHz are becoming more popular for active and passive imaging systems using advanced SiGe and CMOS technologies [7, 10–12]. Most of the work on imaging systems is based on SiGe detectors, Schottky diodes, or CMOS FETs using 0.25 μm and 0.18 μm technology, but little has been done to explore deep submicron CMOS transistors for low noise imaging systems. The 45 nm CMOS SOI technology offers a good platform for such systems due to its high f_t/f_{max}, and the possibility of integrating transmitters at $>$ 150 GHz using wideband multipliers arrays [80].

In this chapter, we investigate the use of advanced 45 nm CMOS SOI for high perfor-

mance switch designs at 140–220 GHz. It is seen that a shunt switch results in much better insertion loss and isolation than a series switch, and is therefore used in SPST and SPDT designs. The realized switches show state-of-the-art insertion loss and isolation. Also, this chapter presents the investigation of a biased 45 nm SOI transistor for active imaging systems in the 140–220 GHz band and the investigation of cold-FET 45 nm SOI transistors for active imaging systems at 300 GHz. The 45 nm detectors are coupled to high-efficiency on-chip slot-ring antennas with above-chip radiation. The on-chip antennas can be implemented with a) above-chip radiation, b) below-chip radiation, and c) below-chip with a dielectric lens. The dielectric-lens approach operates with full thickness chips, but the lens can be expensive for THz operation, and special mounting is required. The below chip radiation require thinning of the silicon chip to unacceptable levels ($\sim$50 μm) at 300 GHz and therefore is not robust. The above-chip radiation results in the lowest-cost since it operates with full thickness silicon chips which are placed on a low-cost FR-4 substrate.

5.2 140–220 GHz SPST and SPDT Switches in 45 nm CMOS SOI

5.2.1 Design

The IBM 12SOI 45 nm CMOS process is used with an nMOS f_t of 485 GHz and 11 metal layers (Fig. 3.3(a)) [81]. The f_t is referenced to the polysilicon layer and decreases to 220 GHz when the interconnect resistance and capacitances up to the top metal layer (LB) are included [55]. The IBM transistor models that come with the design kit are used in the S-parameters and P_{1dB} simulations.

Fig. 5.1(b) shows the cross section of the transistor in the 45 nm CMOS SOI process. The source/drain junction capacitances couple to substrate via the buried oxide (ϵ_r=4.1) instead of the silicon layer (ϵ_r=12). Therefore, this technology results in a significant reduction of junction capacitances as compared to bulk CMOS which is especially important in series switch design. For the same C_{ds} (equivalent isolation) in both technologies, the width of the CMOS SOI transistor is wider than the bulk CMOS transistor which results in a lower insertion loss. For a shunt switch design, C_{ds} imposes a trade-off between isolation and bandwidth [82], and the CMOS SOI design results in a wider bandwidth for the same transistor size, or a higher isolation for the same bandwidth.

An important figure of merit for switches is given by $R_{on}C_{off}$. In 65 nm bulk CMOS technology, $R_{on}C_{off}$ = 300 fs (R_{on} = 370 $\Omega\cdot\mu$m and C_{off} = 0.8 fF/μm) has been reported [83].

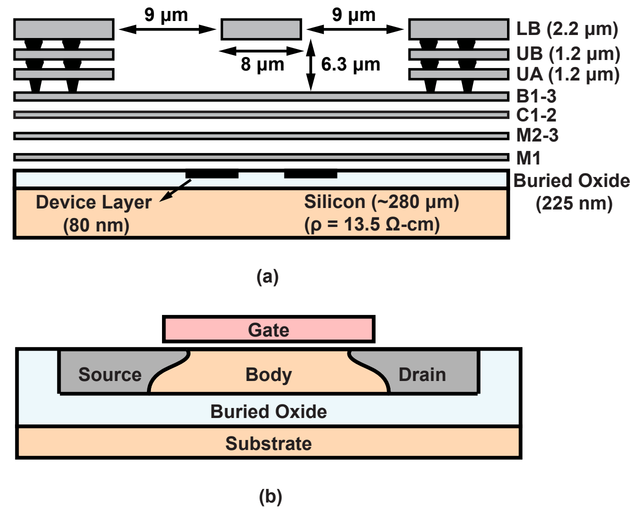


Figure 5.1: (a) Metal stack-up and 50 Ω grounded co-planar waveguide (GCPW) transmission line dimensions (not to scale), (b) Cross-section of the transistor in a 45-nm CMOS SOI process.

In the 45 nm CMOS SOI process, the transistor has a simulated R_{on} = 270 $\Omega\cdot\mu$m and C_{off} = 0.28 fF/μm. Once RC extraction is employed up to M2 (Fig. 5.2), the R_{on} and C_{off} values increase to 300 $\Omega\cdot\mu$m and 0.42 fF/μm. Sonnet full-wave EM simulation tool was then used to model the parasitics from the M2 metal layer up to LB (top metal layer) in order to capture the parasitic inductance and capacitance as well as the via resistances (Fig. 5.2). The final R_{on} and C_{off} values are 350 $\Omega\cdot\mu$m and 0.53 fF/μm including RC extraction and Sonnet simulations ($R_{on}C_{off}$=180 fs). It is seen that there is a significant difference in the C_{off} values between 65 nm bulk CMOS and 45 nm CMOS SOI. However, the R_{on} values are approximately the same which means that the isolation in a shunt switch in both technologies would be similar for the same device width. Also, the total via resistance from M1 to LB is 1–2 Ω independent of the technology node, and this creates an upper limit for the achievable isolation for the shunt switch (S_{21} = 2R/(Z_0+2R) = –28.3 to –22.6 dB for R = 1–2 Ω, independent of frequency).

The shunt switch inductance to ground, from the transistor source node (M1) to the ground metal layers (B3 and LB), must also be minimized since it further degrades the isolation at 180 GHz. Fig. 5.2 presents the zoomed view of the t-line and the transistor connections to the ground plane. Signal line (LB) is connected to the drain node of the transistor, and the source node is connected to t-line ground (B3) using multiple vias to minimize the inductance. The estimated additional source inductance using EM simulations is less than 1 pH and has virtually no effect in the isolation at 140–220 GHz.

Fig. 5.3 shows the simulated insertion loss and the isolation of series and shunt switches

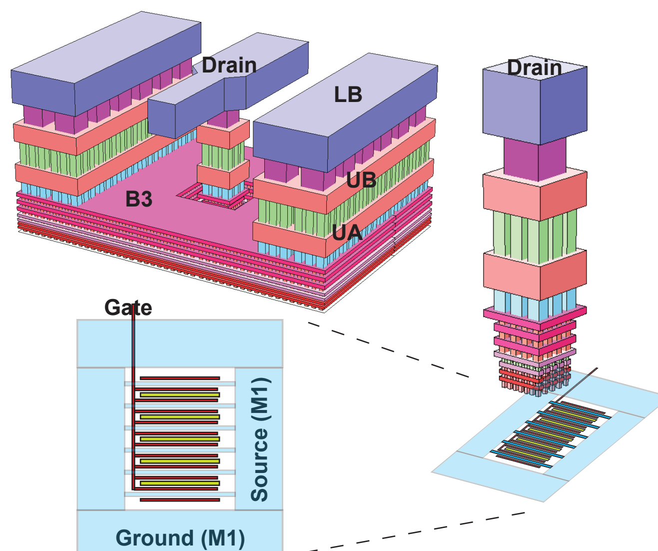


Figure 5.2: Transistor connections.

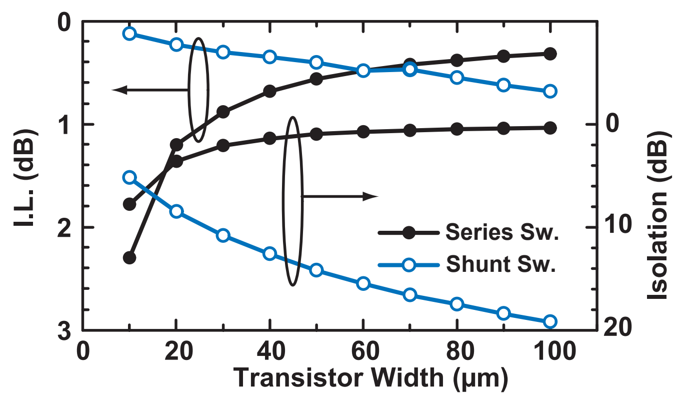


Figure 5.3: Simulated insertion loss and isolation of series and shunt switches vs. transistor width at 180 GHz.

vs. transistor width at 180 GHz. The main limitation of a series switch is the very low isolation at 180 GHz. Therefore, a shunt switch topology is chosen.

The schematic of several switches are shown in Fig. 5.4. The SS-SPST switch is based on a single-shunt nMOS transistor with a transmission-line stub to cancel the equivalent off-state capacitance of 36 fF for V_c = 0 V at 180 GHz. This design uses a wide transistor (W = 70 μm, W/L = 2800) which results in an on-resistance of 5 Ω for V_c = 0.9 V (includes RC extraction and Sonnet simulations) and an isolation of 16 dB at 180 GHz (Fig. 5.3). The insertion loss depends mostly on the shunt stub loss and drain contact resistance. The shorted stub, which has an equivalent inductance of 22 pH, and a simulated Q of 20 at 180 GHz, is realized using a 70-μm-long 50 Ω CPW line, and results in a simulated insertion loss of 1.2 dB at 180 GHz. A floating-body transistor with a 2.5 μm finger width is used in order to reduce the parasitic metallization capacitance.

The DS-SPST switch is based on two (double)-shunt nMOS transistors connected using an inductive transmission-line. In the off-state, this forms a CLC π-network and provides a wideband match. In the on-state, the circuit provides two resistances to ground, thereby improving the isolation. A width of 25 μm is chosen for each transistor (C_{off} = 13 fF and R_{on} = 14 Ω, includes RC extraction and Sonnet simulations). The series inductor is implemented with a 105μm-long 70 Ω grounded CPW line (11/4/11 μm) with a simulated Q of 17 at 180 GHz. The simulated isolation and insertion loss are 24 dB and 1 dB, respectively, at 180 GHz.

The SPDT switches are based on a tuned λ_g/4 design using SS- and DS-SPST switch cells where λ_g is reference to a 50 Ω shielded CPW transmission line. The 50 Ω λ_g/4 t-line at 180 GHz is 210 μm-long with a simulated loss of 0.3 dB. Port 3 of the SPDT switches is terminated with an on-chip 50 Ω load for measurement purposes.

The transmission lines, T-junctions, and CPW pads are then simulated using Sonnet [22] so as to obtain accurate dimensions, and take into account the connection between LB and M2. The SPST and SPDT switches have simulated IP_{1dB} of 9 and 10 dBm, respectively, at 180 GHz.

5.2.2 Measurements

On-chip S-parameter measurements are done using HP 8530 with OML Inc. WR-5 (140–220 GHz) frequency extenders and GGB Industries Inc. WR-5 probes. The system is calibrated using a SOLT probe-tip calibration and a GGB CS-15 calibration substrate. Therefore, the pad loss is included in the insertion loss measurements (0.2–0.3 dB for 2 GSG pads at 180 GHz). After calibration, the measured S_{21} of the thru-structure on CS-15 calibration substrate is

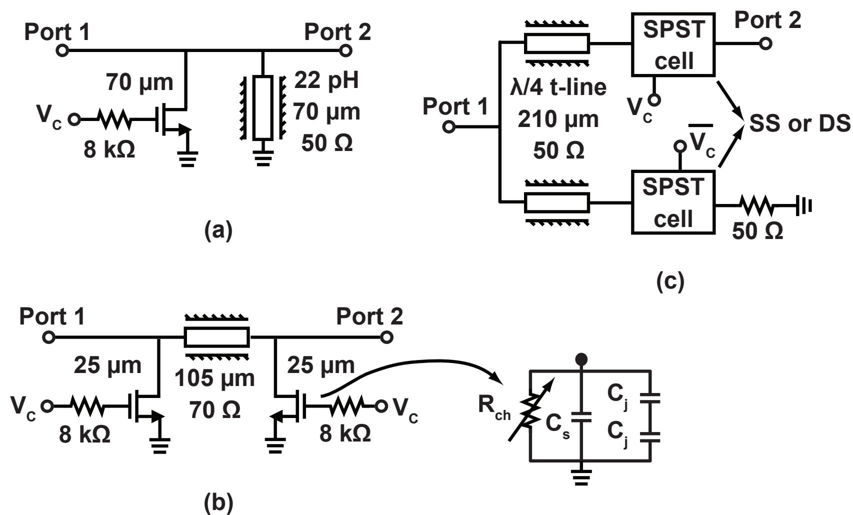


Figure 5.4: Schematic of (a) SS-SPST (b) DS-SPST and (c) SPDT switches.

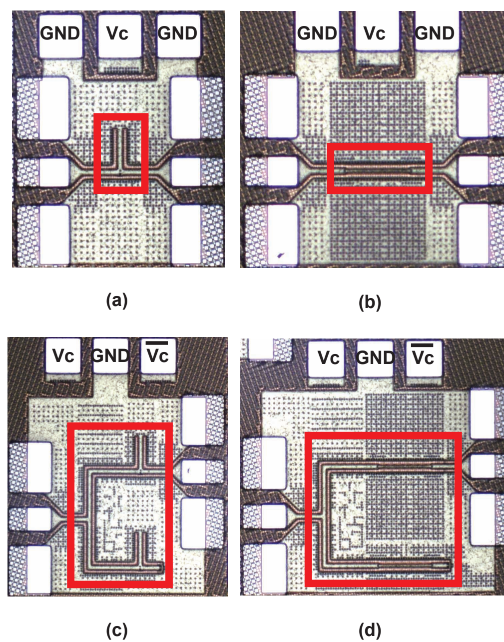
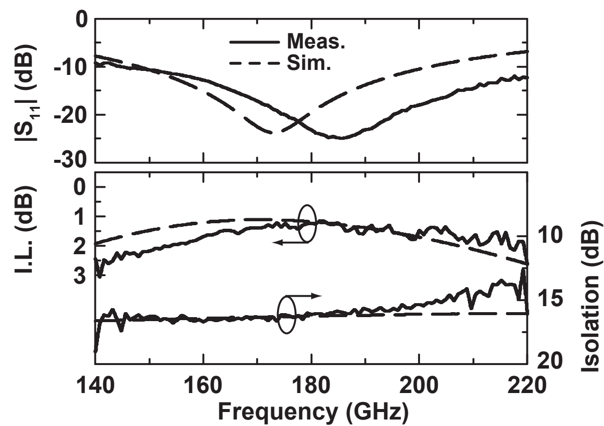


Figure 5.5: Chip photo of (a) SS-SPST (0.45×0.35 mm^2), (b) DS-SPST (0.45×0.45 mm^2), (c) SS-SPDT (0.55×0.45 mm^2), (d) DS-SPDT (0.53×0.55 mm^2) switches, all including the pads.



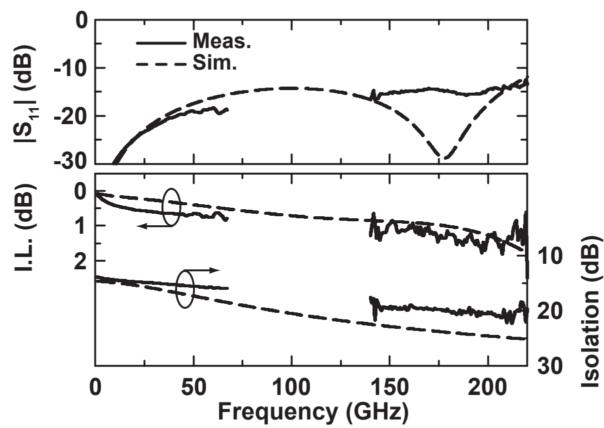


Figure 5.6: Measured and simulated return loss, insertion loss and isolation of (a) SS-SPST and (b) DS-SPST switches.

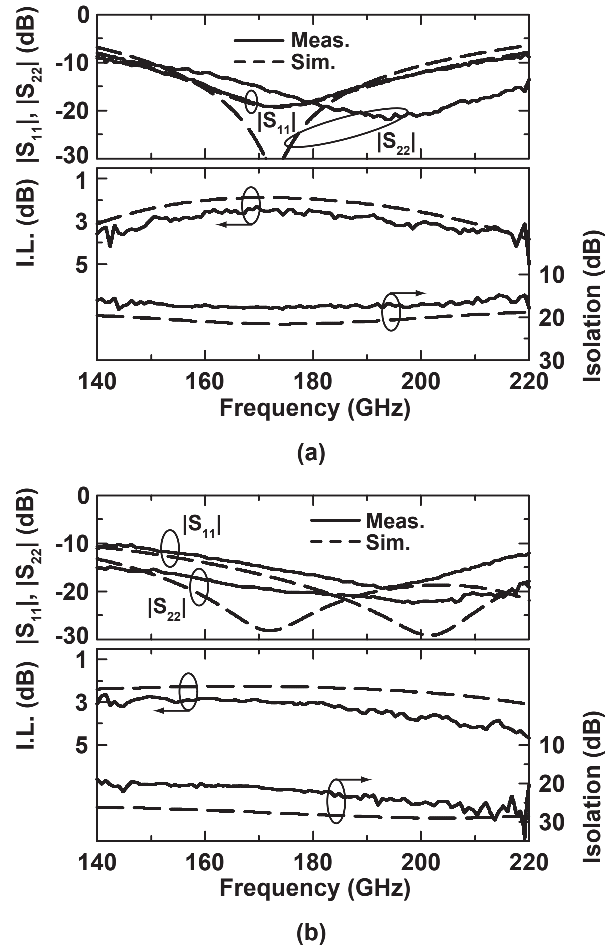


Figure 5.7: Measured and simulated return loss, insertion loss and isolation of (a) SS-SPDT and (b) DS-SPDT switches.

less than 0.2 dB at 140–220 GHz. The measured insertion loss of SS-SPST switch is less than 1.5 dB at 165–195 GHz with an isolation of 16 dB. By contrast, the DS-SPST switch results in an isolation of 20 dB with an insertion loss of 1.5 dB up to 220 GHz (1 dB at 180 GHz). The measured input-to-output isolation is larger than 15 dB and 20 dB at 140–220 GHz for the SPDT switches based on SS and DS designs, respectively. Both SPDT designs result in an insertion loss of less than 3 dB up to 195 GHz. The measured return loss for all switches are larger than 10 dB at 140–210 GHz. The power-level from the WR-5 extender is less than –10 dBm and was well below the P_{1dB} of the tested switches. As seen in Figs. 5.6-5.7, the measurements generally agree with simulations for all designs. The IP_{1dB} of the switches could not be measured due to source limitations at 180 GHz. However, the measured IP_{1dB} of the DS-SPST switch is 7–8 dBm at 50–65 GHz (2–3 dB lower than simulations).

5.3 A Low-Noise 150–210 GHz Detector in 45 nm CMOS SOI

5.3.1 Design

The G-band detector is shown in Fig. 5.8 and designed using the IBM 45 nm CMOS SOI technology with 11 metal layers (Fig. 5.9). This process has an n-type field-effect transistor (nfet) device with an f_t/f_{max} of $\sim$200/240 GHz once the parasitics from the transistor to the top metal layer are included [55]. The grounded coplanar waveguide (G-CPW) transmission lines with dimensions of 9/8/9 μm (Z_0 = 50 Ω) are implemented in the top 3 metal layers, with a measured loss of 2.0 dB/mm at 180 GHz [55]. Standard IBM nfet and vertically-stacked interdigitated metal-finger capacitor (MFC) models are used in the design. The stubs are implemented using G-CPW transmission lines and are modeled using a 2.5-D EM solver (Sonnet [22]). The transitions from the MFCs to the top metal layer, T-junctions and G-S-G pads are also simulated using Sonnet [22].

A detailed investigation shows that transistor widths of 5–25 μm biased at 5–20 μA/μm current density have almost the same NEP [84]. A transistor width of 15 μm is chosen for input matching considerations and the gate biasing is provided using a 5 kΩ resistor. The detector input impedance ($Z_{IN} = 10 - j50\ \Omega$) is matched to 50 Ω using a series and a shunt G-CPW transmission line with a DC block capacitor (150 fF) in between. A 180 GHz notch filter with L = 27 pH and C = 29 fF is used at the output to suppress the first harmonic of the input signal. The load resistor is set to 1 kΩ for DC biasing purposes which is the optimum value for the SR-552 amplifier used in detector noise measurements (see Section III).

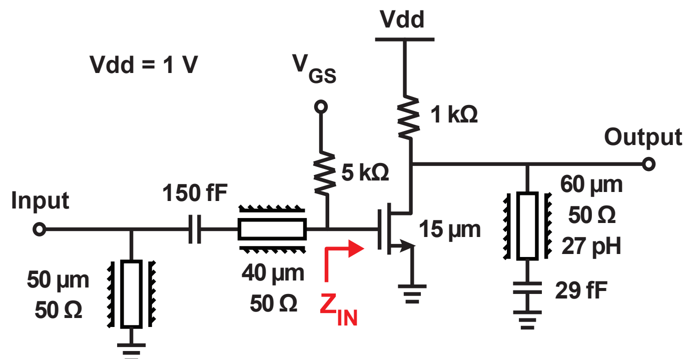


Figure 5.8: Schematic of the 150–210 GHz detector.

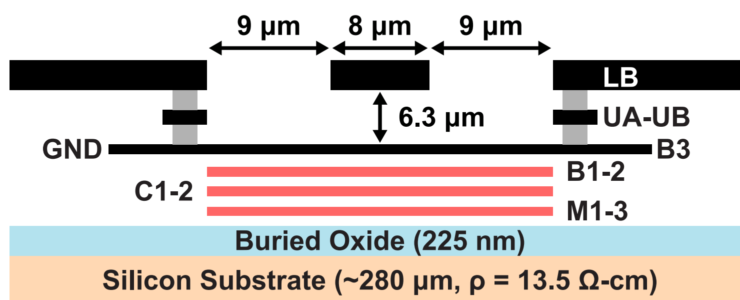


Figure 5.9: Cross-section of the 45 nm CMOS SOI process and 50 Ω G-CPW transmission line (dimensions are not to scale).

Fig. 5.10 presents the detector chip microphotograph (0.45 $\times$ 0.45 mm^2 including the pads). The detector is mounted on a board for noise measurements with a coaxial output in order to reduce the effect of surrounding noise.

5.3.2 Measurements

The on-chip S-parameters are measured using an HP 8530 VNA with OML Inc. WR-5 (140–220 GHz) frequency extenders and GGB Industries Inc. WR-5 probes. The system is calibrated using a SOLT probe-tip calibration and a GGB CS-15 calibration substrate. Fig. 5.11 presents the measured detector S_{11} and S_{21} at a bias current of 200 μA. The input return loss is $>$ 10 dB at 167–194 GHz and the notch filter characteristic is clearly seen in the S_{21} response which is $<$ –20 dB over the entire frequency range.

A W-band sixtupler together with a WR-5 VDI (Virginia Diodes, Inc.) doubler are used to generate the 140–200 GHz signals for responsivity measurements, followed by a WR-5 variable attenuator and a WR-5 10 dB directional coupler. The WR-5 probe loss (2.5 dB) is calibrated out of the measurements and all values are referenced to the GSG pads. Fig. 5.12 presents the measured and simulated detector responsivity versus gate bias voltage (V_{GS}) and DC bias current (I_{DC}) at 170 GHz for an input power of –26 dBm. The measured detector responsivity has a peak value of $\sim$3 kV/W at 170 GHz when the V_{GS} is close to the transistor threshold voltage (250 mV) where the device is highly nonlinear. The measured responsivity is $>$ 1.5 kV/W at 150–210 GHz for I_{DC} = 200 μA (Fig. 5.13). The detector responsivity versus input power is also measured and no compression is observed up to a power level of –18 dBm (not shown).

The detector output noise at low IF ($<$ 1 MHz) is measured using an external SR-552 amplifier which has an input impedance of 100 kΩ, a noise figure of 1 dB (1.9 nV/Hz$^{1/2}$) when driven by a 1 kΩ source impedance and a 1/f corner frequency of a few Hz (Fig. 5.14(a)) [48]. The measured noise includes the SR-552 amplifier noise which is negligible compared to the detector output noise voltage (30–300 nV/Hz$^{1/2}$), and the additional SR-552 amplifier gain has been calibrated out of the measurements. For noise measurements at high IF ($>$ 0.1 MHz), a DC-block and an SMA-tee together with a 50 Ω termination are placed right after the GSG probe in order to eliminate the standing waves in the long SMA cable to the Agilent E4448A spectrum analyzer (Fig. 5.14(b)). The spectrum analyzer internal preamp (0.1–3000 MHz) is turned on to reduce the noise-floor to –168 dBm/Hz. Fig. 5.14(c) presents the measured detector output noise voltage versus IF. The gate biasing resistor (5 kΩ) dominates the output noise at $>$ 1 MHz,

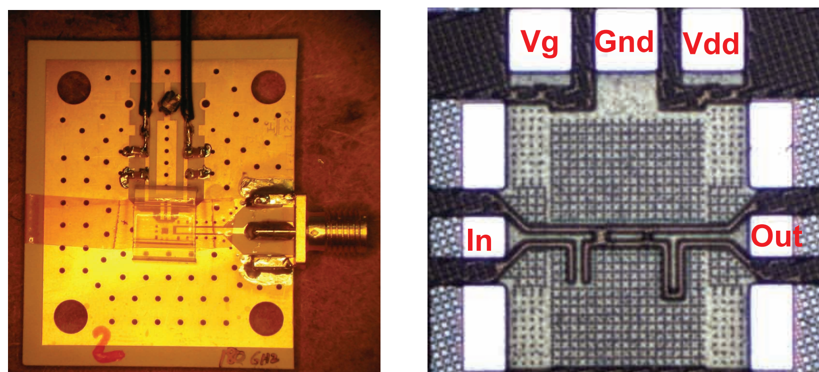


Figure 5.10: Microphotograph of the detector. The chip size is 0.45×0.45 mm^2 including the pads.

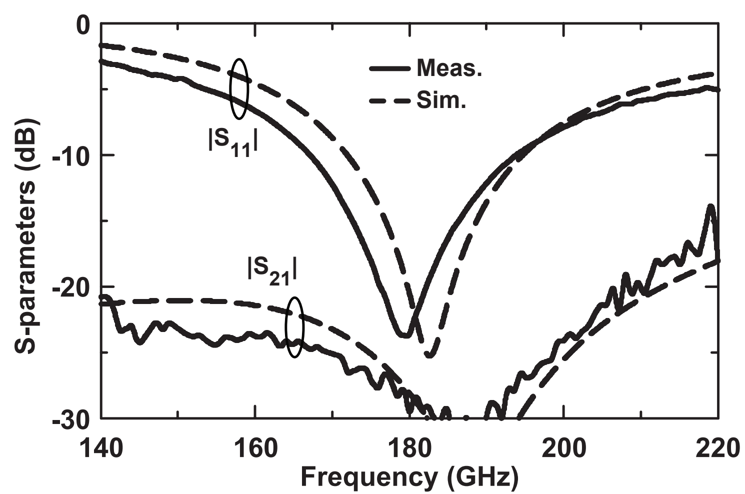


Figure 5.11: Measured and simulated detector S_{11} and S_{21} at I_{DC} = 200 μA.

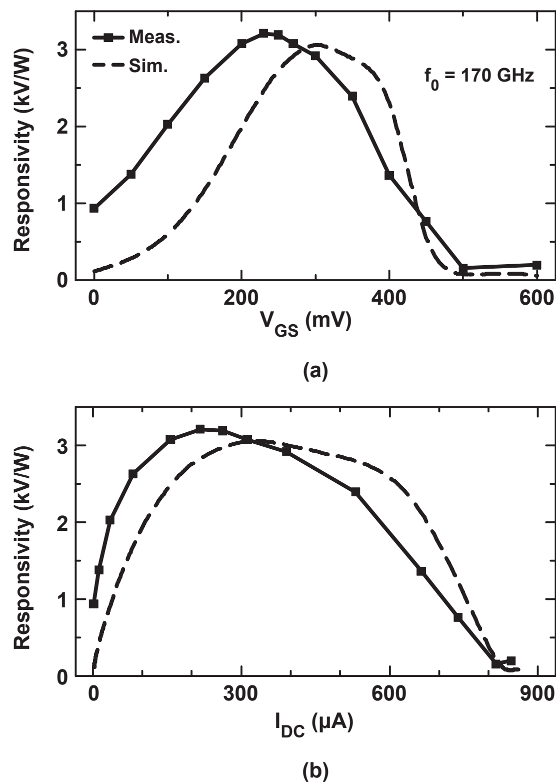


Figure 5.12: Measured and simulated detector responsivity versus (a) V_{GS} and (b) I_{DC} at 170 GHz.

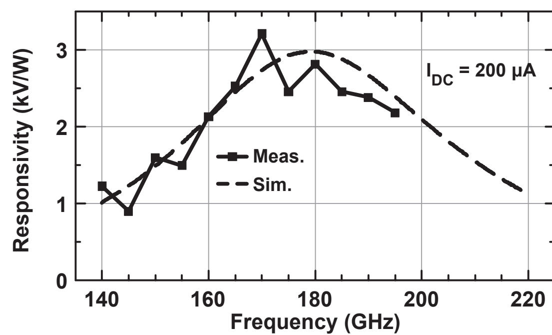


Figure 5.13: Measured and simulated detector responsivity versus frequency at I_{DC} = 200 μA.

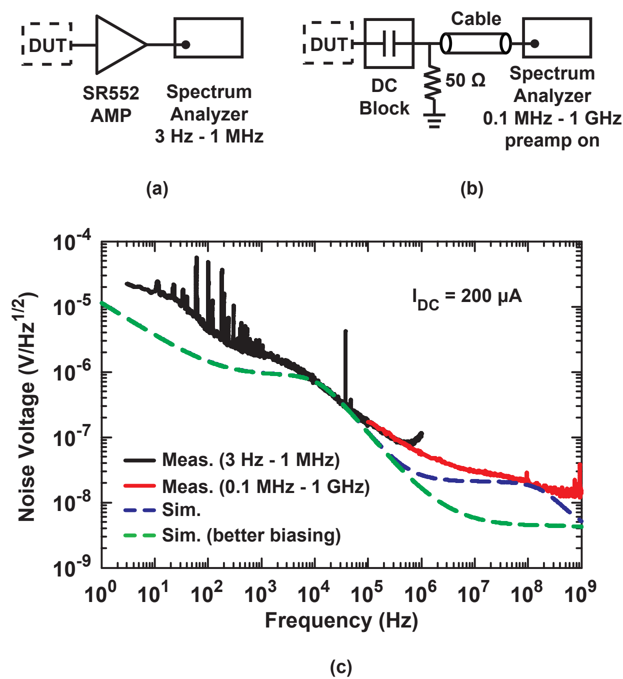


Figure 5.14: Noise measurement setup for (a) lower IF frequencies (< 1 MHz) and (b) higher IF frequencies (> 0.1 MHz). (c) Measured and simulated output noise voltage versus IF frequency at I_{DC} = 200 μA.

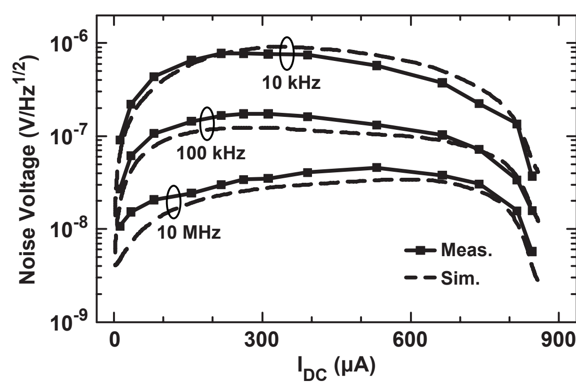
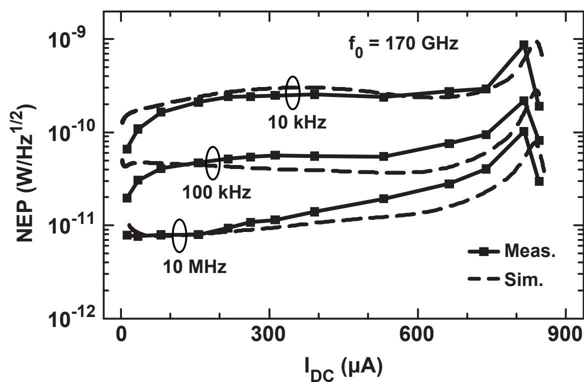
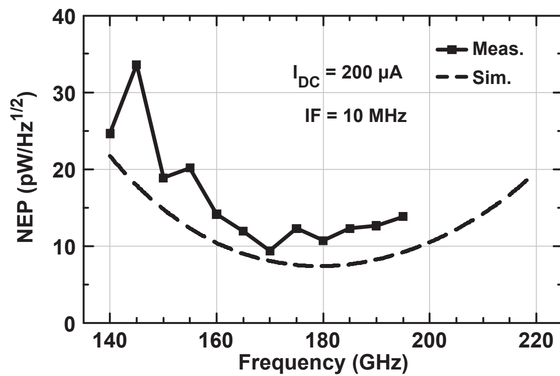


Figure 5.15: Measured and simulated detector output noise voltage versus I_{DC} at an IF frequency of 10 kHz, 100 kHz and 10 MHz.



(a)



(b)

Figure 5.16: Measured and simulated detector NEP versus (a) I_{DC} at an IF frequency of 10 kHz, 100 kHz and 1 MHz, (b) RF frequency at I_{DC} = 200 μA and an IF frequency of 10 MHz.

Table 5.1: Detector Comparison

	This Work	[7]	[10]*
Technology Node	45-nm CMOS	SiGe HBT	130-nm CMOS
Frequency (GHz)	170	165	280
Responsivity (kV/W)	3	11	0.32
NEP (W/Hz$^{1/2}$)	10	6	29
Power Consumption (μW)	200	1700	60

*Antenna efficiency ($\sim 50\%$) is included in the quoted values.

and this could have been avoided if the DC bias is applied through a shunt transmission-line as explained in [45]. The noise improves by 6 dB at 10 MHz if a better biasing were used. The measured detector output noise voltage is 760, 165 and 30 nV/Hz$^{1/2}$ at 10 kHz, 100 kHz and 10 MHz, respectively for I_{DC} = 200 μA (Fig. 5.15).

The measured output noise is then divided by the responsivity to calculate the noise equivalent power (NEP). The measured NEP is 30–50 pW/Hz$^{1/2}$ and 8–10 pW/Hz$^{1/2}$ at an IF of 100 kHz and 10 MHz, respectively for I_{DC} = 50–200 μA (Fig. 5.16(a)). The detector 3-dB NEP bandwidth is $>$ 45 GHz (150–195$^+$ GHz) and agrees well with simulations (Fig. 5.16(b)).

5.4 A 0.3 THz 4×4 Cold-FET Imaging Array using Differential High-Efficiency On-chip Antennas in 45 nm CMOS SOI

The 300 GHz imaging array is fabricated in a 45 nm CMOS SOI technology with 11 metal layers. This process has n-type field-effect transistor (nfet) device with an f_t/f_{max} of $200/240$ GHz [55]. The grounded coplanar waveguide (G-CPW) transmission lines with dimensions of 9/8/9 μm ($Z_0 = 50\ \Omega$) have a simulated loss of 2 dB at 300 GHz. Standard IBM nfet and vertically-stacked interdigitated metal-finger capacitor (MFC) models are used in the design. The G-CPW transmission lines, transitions from MFCs and nfet to the top metal layer, T-junctions and G-S-G pads are modeled using a 2.5-D EM solver, Sonnet [22].

5.4.1 Antenna Design

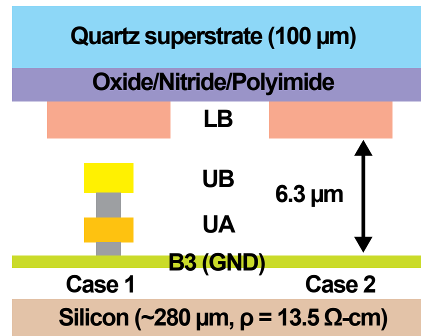
The 300 GHz differential slot-ring antenna is designed using a 100 μm quartz superstrate above the silicon chip. The antenna results in a 180° phase difference at the input of the two feeds. The slot-ring antenna uses the top metal layer (LB), and the ground plane is defined as B3. The quartz superstrate is not patterned and improves the antenna efficiency by equalizing the TEM mode in the dielectric underneath the top metal layer and the TM_0 mode in the quartz superstrate [42].

In this work, the antennas are implemented meeting the required minimum metal density rules although this results in a reduced efficiency due to increase of the effective ϵ_r. The minimum density requirement in the IBM12SOI process for the UA and UB metal layers is 20% which can seriously affect the antenna performance. Fig. 5.17 presents the different metal-fill cases under consideration (case 1: metal-fill, case 2: no metal-fill). The simulated S_{11} is shown in Fig. 5.18 for both cases (referenced to 100 Ω differential). The antenna without any dummy metal-fill (Case 2) results in a simulated efficiency of 45% and a gain of 3.6 dB at 270 GHz (Fig. 5.19). On the other hand, Case 1 (20% metal-fill) results in a simulated efficiency of 26% and a gain of 0.8 dB at 270 GHz. This is still 3.8 dB better than without a quartz superstrate (and metal fill).

5.4.2 Detector Design

Fig. 5.20 presents the schematic of a single element in the 4×4 CMOS imaging array. The differential slot antenna is connected to the cold-FET detector which drives a differential IF amplifier with a voltage gain of 32 dB. The cold-FET detector is based on resistive self-mixing by placing a 40 fF capacitor between the gate and drain nodes of the devices [11]. The drain nodes are connected together using G-CPW transmission lines (Z_0 = 50 Ω, $l = 35$ μm), creating a virtual ground at the intersection. The similar argument is also true for the source nodes due to the symmetrical structure. A device width of 10 μm is chosen in order to match the differential input impedance to 100 Ω together with the drain-to-gate capacitors and G-CPW transmission lines at the drain nodes.

The source bias voltage is applied to one input of the IF amplifier serving as a reference. When an RF signal is not present, both IF amplifier inputs are same, assuming V_{GS} is close to V_{TH} of the device. When an RF signal is present, the rectified voltage at the drain nodes due to the detector square-law characteristic is amplified by the differential IF amplifier. The source bias voltage is chosen as 0.7 V for proper operation of the IF amplifier, and the gate bias voltage



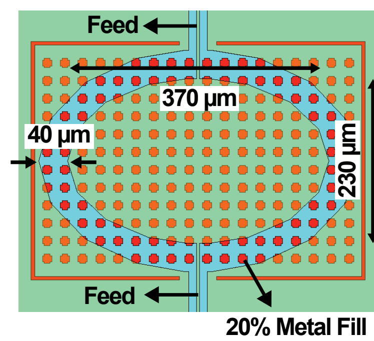


Figure 5.17: (a) Metal-fill cases and (b) on-chip differential slot antenna with the metal-fill underneath the antenna.

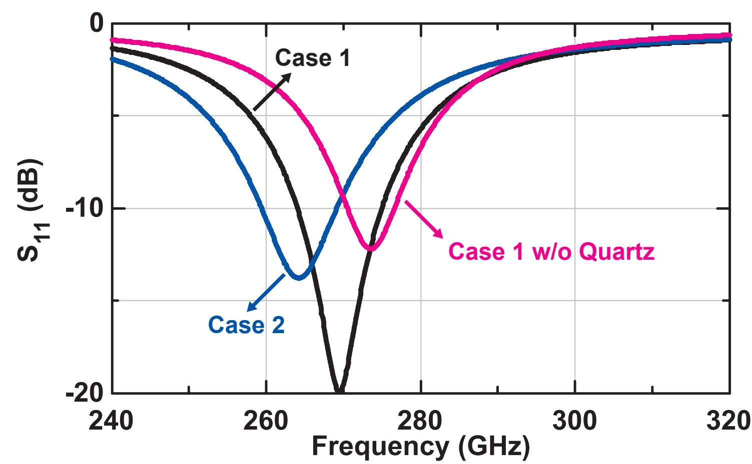
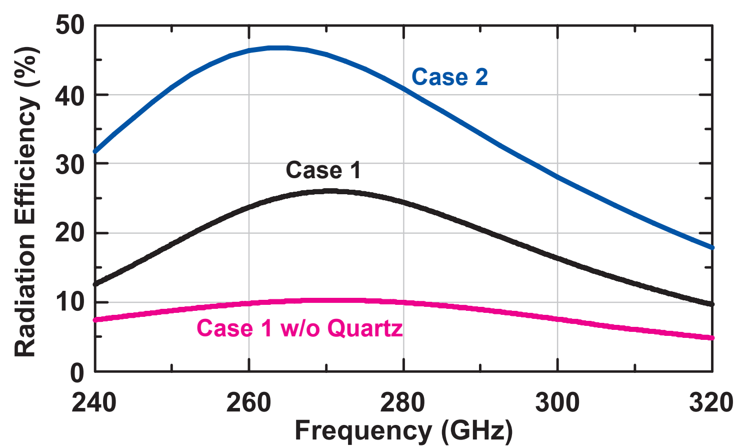
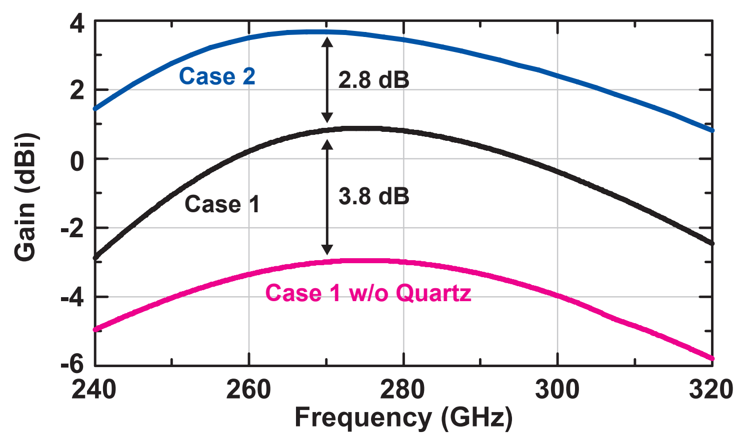


Figure 5.18: Simulated on-chip antenna S_{11} for different metal-fill cases.



(a)



(b)

Figure 5.19: Simulated on-chip antenna (a) efficiency and (b) gain for different metal-fill cases.

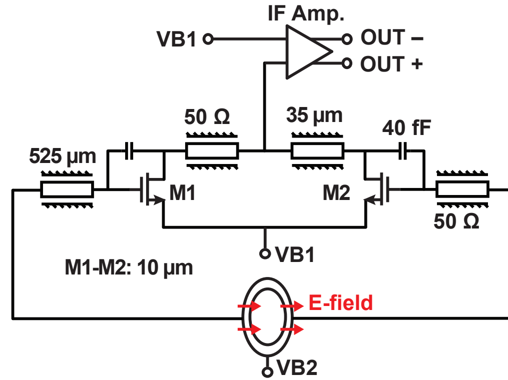


Figure 5.20: Schematic of the single element of 4×4 CMOS imaging array.

is V_{GS} + 0.7 V and is applied at the virtual ground of the differential slot-ring antenna. The G-CPW transmission lines from the antenna feed to the detector input are 525 μm long (Z_0 = 50 Ω) with a simulated loss of $\sim$1 dB at 300 GHz.

Since a cold-FET detector topology is used, the detector does not generate any 1/f noise. Therefore, the following IF amplifier determines the 1/f corner. A large device size (W/L = 540/2 μm) is chosen for the input differential pair of IF amplifier to obtain $<$ 100 kHz 1/f corner. The IF amplifier has a voltage gain of 32 dB with a current consumption of 2 mA from 1.8 V.

5.4.3 Measurements

The 4×4 imaging array has been characterized using a far-field set-up as shown in Fig. 5.22. The measurement system is based on 2 multiplier chains from Virginia Diodes, Inc. (VDI) capable of delivering 3-4 mW at 260–290 GHz (VDI AMC-333) and 290–340 GHz (VDI AMC-334) from an Agilent source at 9-12 GHz [46]. The Agilent source is pulse modulated with 50 $\%$ duty cycle at 1-100 kHz, and the detected signal is sent to an SRS-830 lock-in amplifier. This eliminates the DC drifts in the system and results in accurate responsivity measurements. The measurement set-up is also used for pattern measurements, but with a rotation stage. The responsivity is defined as:

$$\Re = \frac{V_{OUT}}{S \times A_{physical}} \tag{5.1}$$

$$S = \frac{P_t G_t}{4\pi R^2} \tag{5.2}$$

where S is the incident power density on the antennas, $A_{physical}$ is the cell size of a single antenna (0.36 mm^2), P_t is the transmitted power, G_t is the WR-3.4 horn antenna gain.

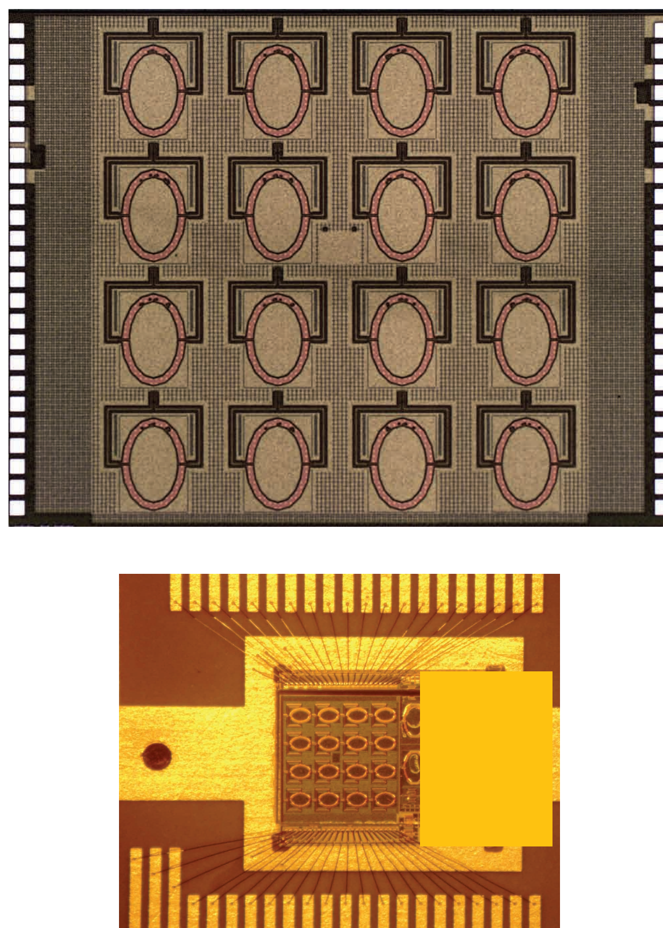


Figure 5.21: Microphotgraph of the 4×4 CMOS imaging array chip and zoomed view of the board showing the bondwires.

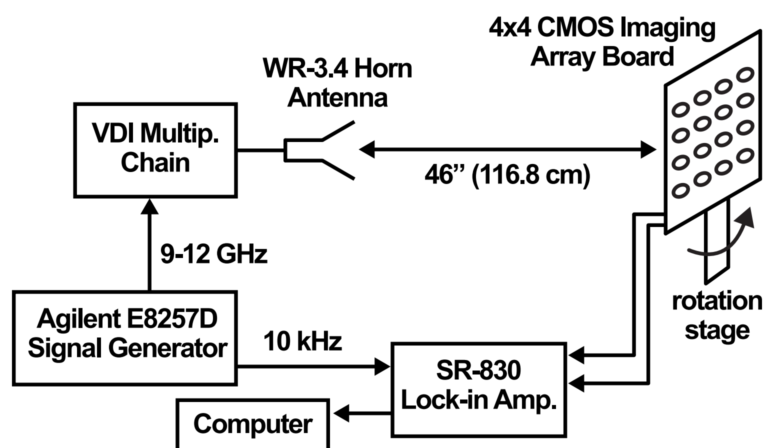


Figure 5.22: Block diagram of the responsivity and antenna pattern measurement setup.

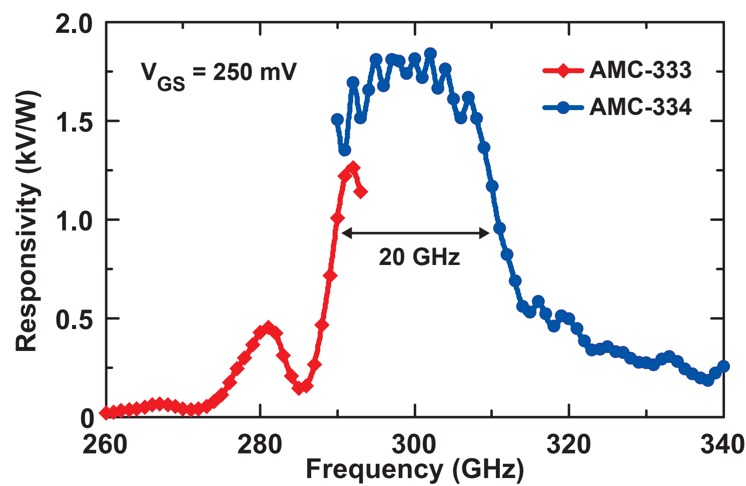


Figure 5.23: Measured responsivity versus frequency of a single pixel at $V_{GS} = 250$ mV.

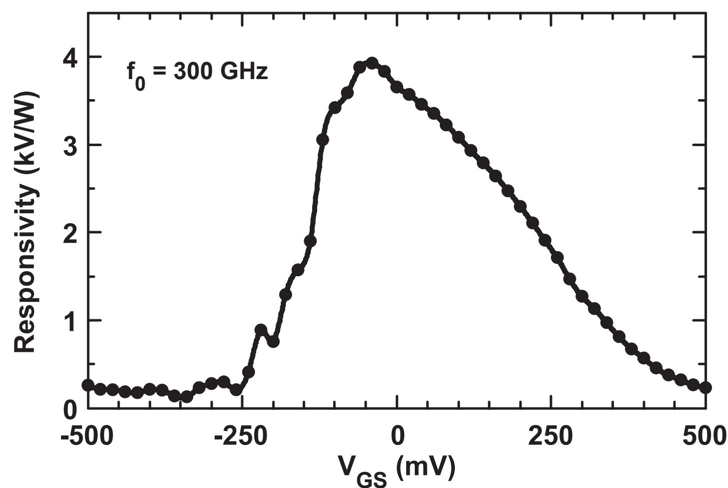


Figure 5.24: Measured responsivity versus V_{GS} of a single pixel at 300 GHz.

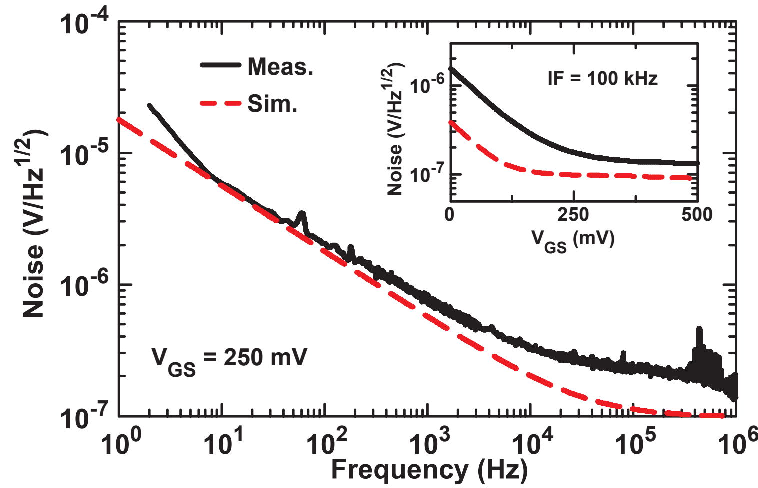


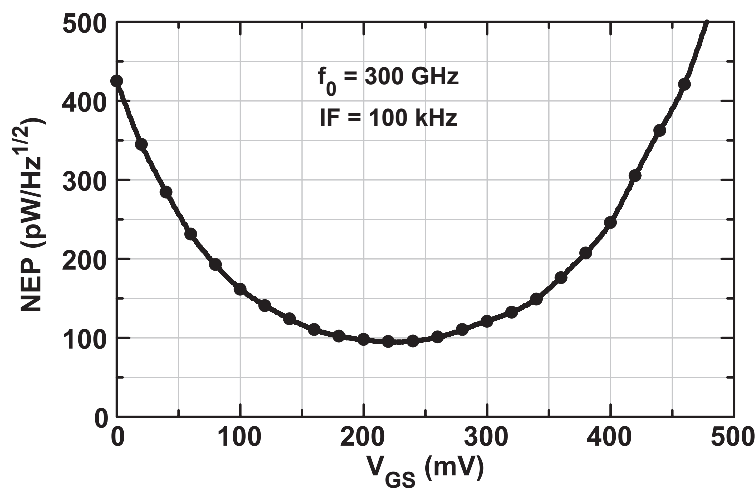
Figure 5.25: Measured and simulated output noise voltage of a single pixel versus frequency at $V_{GS} = 250$ mV and versus V_{GS} at IF = 100 kHz.

Note that the antenna directivity also results in an effective aperture of $A_e = \frac{\lambda^2}{4\pi}D = 0.32$ mm^2 for a simulated directivity of D = 4.0 (6.0 dB) at 300 GHz, and is similar to the array cell size. It is better to use the physical array area for the available power since it takes into account all the power incident on the array.

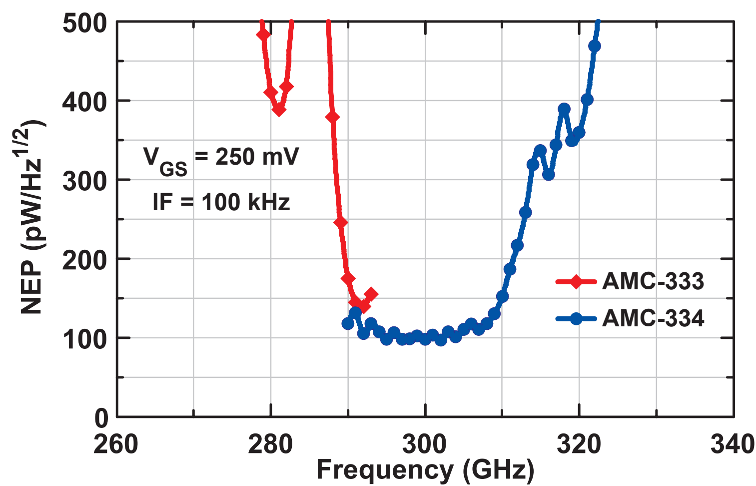
Fig. 5.23 presents the measured responsivity versus frequency at a detector gate bias of 250 mV. The peak responsivity is $\sim$1.8 kV/W with a 3-dB bandwidth of 20 GHz (290–310 GHz). The design was at 270–280 GHz, but shifted to 300 GHz. This 9% shift in frequency is perhaps due to inaccurate HFSS simulations which does not capture precisely the metal-fill effects and exact thickness of the dielectric layers. Fig. 5.24 presents the measured responsivity versus V_{GS} at 300 GHz, and the peak responsivity is $\sim$4 kV/W at V_{GS} close to 0 V.

Fig. 5.25 presents the measured low-frequency noise versus IF frequency. This is measured using an external low-noise amplifier with a 1/f corner frequency of a few Hz (SR-552 [48]) and an Agilent E4448A spectrum analyzer. The additional gain of the SR-552 amplifier has been calibrated out of Fig. 5.25. The measured noise includes the detector, operational amplifier and the external 16:1 multiplexer. The measured noise voltage is 0.18 nV/Hz$^{1/2}$ at V_{GS} = 250 mV and IF = 100 kHz. The noise equivalent power (NEP) is then calculated by dividing the measured noise to the responsivity. The 1/f noise below 100 kHz is due to the CMOS IF amplifier, and therefore the quoted NEP values are given at an IF of 100 kHz.

Fig. 5.26 presents the measured NEP versus RF frequency at V_{GS} = 250 mV and versus V_{GS} at 300 GHz. The minimum NEP occurs at V_{GS} of 200–250 mV and is $\sim$100 pW/Hz$^{1/2}$



(a)



(b)

Figure 5.26: Measured NEP of a single pixel versus frequency at $V_{GS} = 250$ mV and versus V_{GS} at 300 GHz, both for IF = 100 kHz.

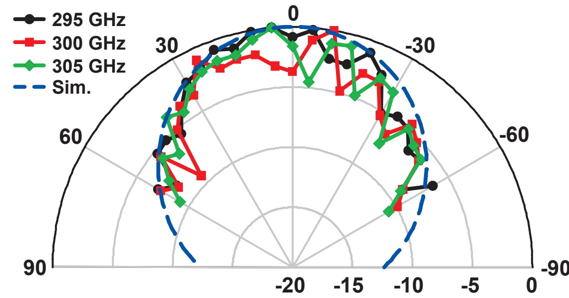


Figure 5.27: Measured and simulated H-plane antenna patterns of a single element at 295, 300 and 305 GHz with quartz superstrate.

with a 3-dB bandwidth of 20 GHz.

Fig. 5.27 presents the measured H-plane patterns of a single antenna pixel at 295, 300 and 305 GHz. Note that the ripples are due to the finite ground plane and standing waves in the measurement system. Overall, the measured patterns agree with simulations.

5.5 Conclusion

This chapter has presented a wideband SPST from DC to 220 GHz and SPDT switches at 140–220 GHz with low insertion loss and high isolation using 45 nm CMOS SOI process. Also, a G-band CMOS detector is presented with a measured responsivity of 3 kV/W at 170 GHz and an NEP of 8–10 pW/Hz$^{1/2}$ at an IF of 10 MHz. These values are comparable to the best SiGe detectors but at a higher IF due to the transistor 1/f noise. Additionally, a 0.3 THz 4×4 CMOS imaging array with above-chip radiation has been presented with a minimum NEP of 100 pW/Hz$^{1/2}$ and a 3-dB bandwidth of 20 GHz. The demonstrated array uses on-chip differential slot-ring antennas meeting the minimum metal-density rules which reduces the antenna efficiency by $\sim$3 dB. If the metal-density rules are excluded, the NEP would be $\sim$50 pW/Hz$^{1/2}$ which is competitive with the best reported values to date. Therefore, it is important to report if the antennas used meet all the back-end processing rules or if exceptions are taken. Also, it is important to report in detail the back-end technology since the 45 nm CMOS back-end has thinner dielectrics and thinner metals (which result in less antenna efficiency) than less advanced nodes such as 0.13 μm or 0.18 μm CMOS.

Table 5.2: Performance Summary

	[10]	[11]	[12]	This work
Technology	0.13-μm CMOS	0.25-μm CMOS	65-nm CMOS	45-nm CMOS SOI
Frequency (THz)	0.28	0.65	0.86	0.3
Responsivity (V/W)	5k	80k	140k	2k
NEP (pW/Hz$^{1/2}$)	29	300	100	100[b]
3-dB Bandwidth (GHz)	20	N/A	270	20
Metal-Fill	Excluded (0%)	N/A	N/A	20%
Antenna Type	Microstrip	Microstrip	Ring ant. + Lens	Slot-ring ant. w/ quartz superstrate
Power Consumption (mW/pixel)[a]	1.3	5.5	2.5	3.6

[a] Power consumption of a single detector together with an opamp.

[b] $\sim$50 pW/Hz$^{1/2}$ if 0% metal-fill is used.

5.6 Acknowledgement

This work was supported by the C2S2 Focus Center, one of six research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation entity. The authors thank Andy Fung from NASA Jet Propulsion Laboratory, Ozgur Inac, Fatih Golcuk and Ozan D. Gurbuz from University of California San Diego for their technical help.

Chapter 5 is mostly a reprint of the material as it appears in IEEE Microwave and Components Letters, 2012 and as it is submitted for publishing to IEEE Microwave and Components Letters, 2013. Mehmet Uzunkol; Jennifer M. Edwards; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 6

Conclusion

A low-power OOK receiver at V-band is developed in a commercial 0.12-μm SiGe BiCMOS process, and 3–6 Gb/s wireless communication link has been demonstrated with a BER $< 10^{-12}$ up to 105 °C. In depth analysis indicate that the OOK receiver operates best at low bias currents, and care should be taken to reduce the bias circuit noise, and to reduce the LO leakage from the transmitter. The OOK receiver, when well designed, can have an instantaneous dynamic range of 30 dB.

A 0.32 THz 4×4 imaging array has been presented with state-of-the-art performance in the 0.2-0.6 THz range. Detailed measurements show that careful attention must be used in order to report accurate values for the system NEP. In particular, a $\pm$ 2.1 dB ripple in the NEP versus frequency and angle of incidence has been found due to standing waves in the THz measurement system and finite ground plane effects. In addition, it was found that metal-density rules drop the on-chip antenna efficiency by $\sim$3 dB, and therefore, it is important to report if the antennas used meet all the back-end processing rules or if exceptions are taken. The demonstrated array results in an average NEP of 34 pW/Hz$^{1/2}$ at 320 GHz using on-chip antennas meeting the strictest metal-density rules.

A 65 GHz 3-bit phase shifter with an integrated LNA is demonstrated. The LNA/phase shifter achieves a gain of 6.5 dB, a noise figure of 4.3 dB and an input P_{1dB} of –13.5 dBm at 65 GHz with only 15 mW DC power consumption. The RMS phase and gain error is less than 2.5° and 1.3 dB at 60–67^{+} GHz. A wideband SPDT switch from 50 to 70 GHz with excellent insertion loss and isolation performance is presented. The power handling is limited to 13–14 dBm which is sufficient for most short-range 60 GHz communication systems.

A wideband SPST from DC to 220 GHz and SPDT switches at 140-220 GHz are pre-

sented with low insertion loss and high isolation using 45-nm CMOS SOI process. A G-band CMOS detector is presented with a measured responsivity of 3 kV/W at 170 GHz and an NEP of 8–10 pW/Hz$^{1/2}$ at an IF of 10 MHz. These values are comparable to the best SiGe detectors but at a higher IF due to the transistor 1/f noise. A 0.3 THz 4×4 CMOS imaging array with above-chip radiation has been presented with a minimum NEP of 100 pW/Hz$^{1/2}$ and a 3-dB bandwidth of 20 GHz. The demonstrated array uses on-chip differential slot-ring antennas meeting the minimum metal-density rules which reduces the antenna efficiency by $\sim$3 dB. If the metal-density rules are excluded, the NEP would be $\sim$50 pW/Hz$^{1/2}$ which is competitive with the best reported values to date. Therefore, it is important to report if the antennas used meet all the back-end processing rules or if exceptions are taken. Also, it is important to report in detail the back-end technology since the 45 nm CMOS back-end has thinner dielectrics and thinner metals (which result in less antenna efficiency) than less advanced nodes such as 0.13 μm or 0.18 μm CMOS.

Appendix A presents the SiGe detector open-circuit responsivity derivation based on Volterra series expansion. The theoretical and simulated detector responsivity are compared in Chapter 2 and the responsivity behaviour versus detector bias current is explained in detail. This is crucial for the detector operation and the optimum bias current for minimum NEP. Appendix B presents the theoretical BER equations for coherent and noncoherent OOK, and the difference between them is less than 0.5 dB to achieve a BER of 10^{-12}. Since the mathematics involved in noncoherent OOK analysis is tedious, the LO leakage effect on OOK detection, explained in Chapter 2, is analyzed using the coherent detection expression.

Appendix C compares the isolation performance of series and shunt switches with and without a matching inductor. For the inductorless case, it is proven that the shunt switch isolation is always better than the series switch when they have the same insertion loss. Using a matching inductor, it is shown that both switches have the same isolation given that they have the same insertion loss. However, a shunt switch is typically preferred if a wideband operation is desired. Finally, Appendix D investigates the single-shunt (SS) and double-shunt (DS) single-pole single-throw (SPST) switches. It is shown that the DS switch results in a better isolation than SS switch. This has been theoretically proven and also verified by the SpectreRF simulations. Additionally, 4S and 8S switch simulation results are presented, and 4S switch is considered to be the optimum switch topology considering the wideband return loss, insertion loss and high isolation. A 4S shunt switch could be a potential future work since the simulations predict superior performance compared to SS and DS switches.

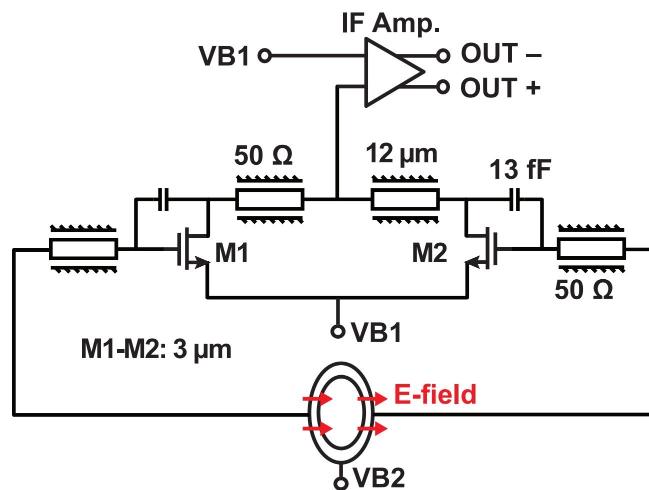


Figure 6.1: Schematic of the single element of the 1 THz 4 $\times$ 4 CMOS imaging array.

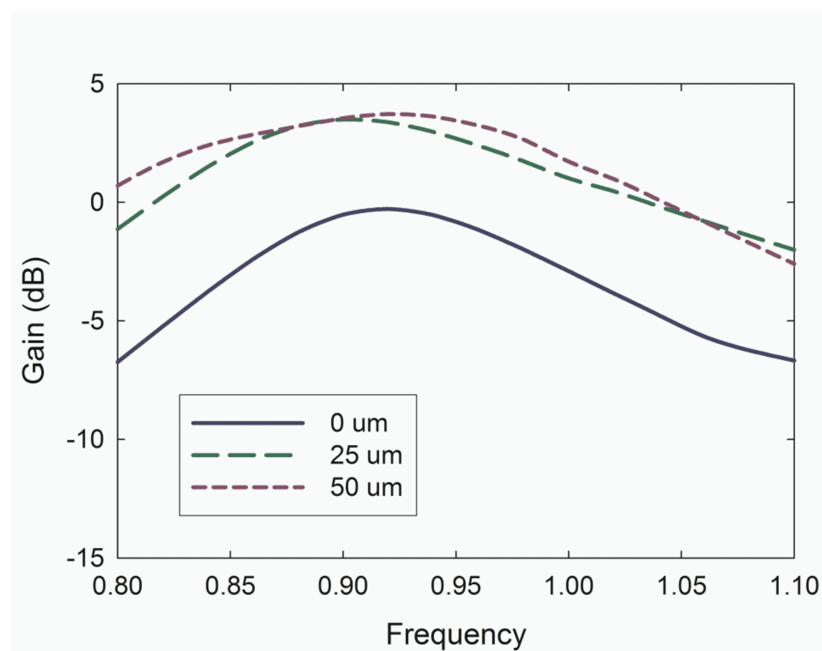


Figure 6.2: Simulated on-chip antenna gain for 3 different quartz superstrate thicknesses.

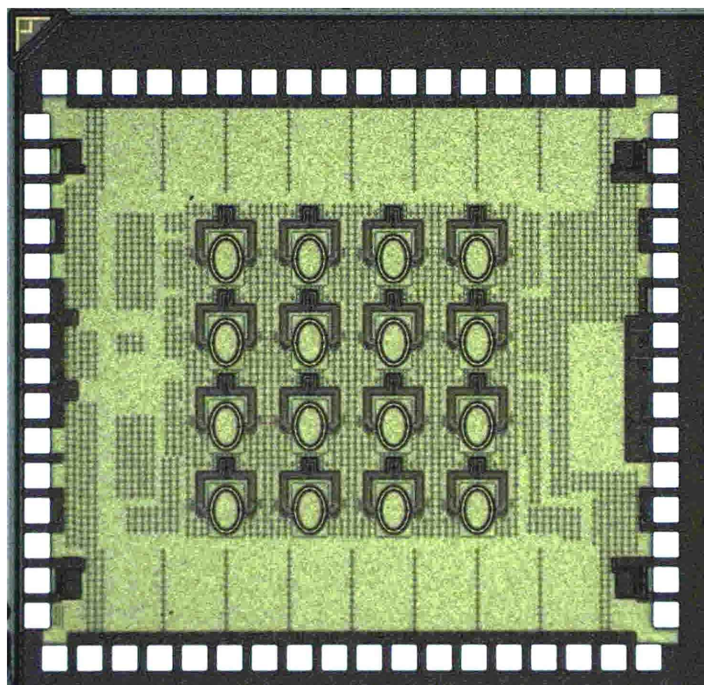
6.1 Future Work

In Chapter 3 and Chapter 5, 0.3–0.32 THz CMOS and SiGe imaging arrays have been demonstrated. As a future work, the operation frequency of an imaging array could further be increased. This will result in a higher resolution and therefore a much better image. On the other hand, the detector design and EM modeling of the interconnections and matching networks become more challenging.

A 1 THz 4 $\times$ 4 imaging array has been designed using 45 nm CMOS SOI technology and the schematic of a single element of the array is presented in Fig. 6.1. The design methodology is similar to the 300 GHz imaging array presented in Chapter 5. The differential slot antenna is connected to the cold-FET detector which drives a differential IF amplifier with a voltage gain of 32 dB. The cold-FET detector is based on resistive self-mixing by placing a 13 fF capacitor between the gate and drain nodes. The drain nodes are connected together using G-CPW transmission lines (Z_0 = 50 Ω. l = 35 μm), creating a virtual ground at the intersection. A device width of 3 μm is chosen for the differential detector. Note that all the detector design parameters (device size, gate to drain capacitor and transmission line lengths) are divided by 3.3 compared to the 300 GHz detector design. The main reason behind this methodology is the inaccurate models for transistors and passive structures at 1 THz. Therefore, no simulations have been done for the 1 THz detector.

Fig. 6.2 presents the simulated on-chip differential slot-ring antenna gain for 3 different quartz superstrate thicknesses. The simulated peak gain occurs at 0.92 THz and is 0 dB and 3 dB for a quartz thickness of 0 and 25 μm, respectively. Note that 50 μm quartz thickness results in almost the same gain as the 25 μm case. The simulated antenna radiation efficiency (not shown) also follows the same trend, and is 24% and 48% for a quartz thickness of 0 and 25 μm, respectively.

Fig. 6.3 presents the microphotograph of the fabricated 1 THz imaging array and the zoomed view of the board showing the bondwires. The imaging array occupies an area of 1.75 $\times$ 1.9 mm^2 and it is mounted on a low-cost FR-4 carrier. The measurements of the 1 THz imaging array will be conducted in the future. The measurement setup requires a transmitter at 1 THz and a WR-1.0 waveguide horn antenna.



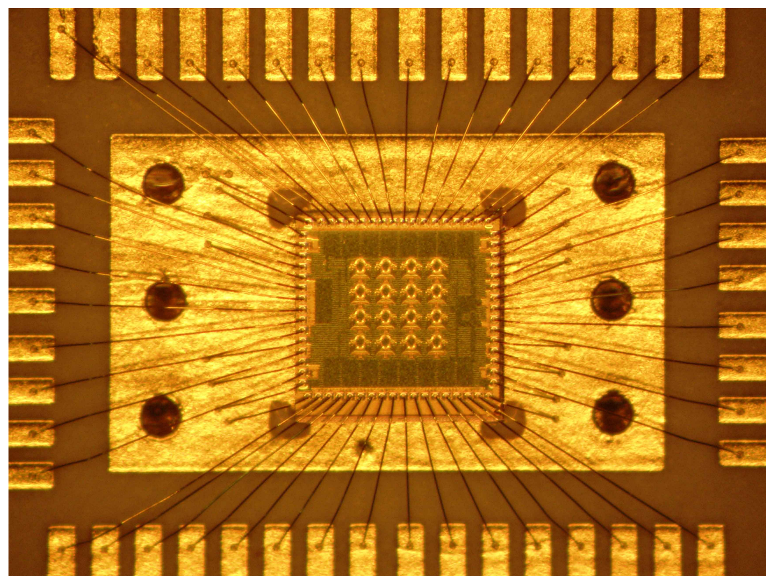


Figure 6.3: Microphotograph of the 1 THz 4 $\times$ 4 CMOS imaging array and zoomed view of the board showing the bondwires.

Appendix A

Derivation of the Detector Responsivity

Using the large-signal BJT model shown in Fig. 2.4(a), the collector current can be described by a Volterra series expression with an applied voltage V_s and expressed as

$$I_c = A_1(s) \circ V_s + A_2(s_1, s_2) \circ V_s^2 + ... \tag{A.1}$$

The first two volterra kernels are derived for a common-emitter BJT in [85]. To find the DC response due to 2nd order nonlinearity, $A_2(s_1, s_2)$ is obtained by setting s_1 = $-s_2$ = s and shown below:

$$A_1(s) = \frac{g_m}{1 + g_m Z_e(s) + sC_\pi Z(s)} \tag{A.2}$$

$$A_2(s, -s) = A_1(0)A_1(s)A_1(-s)\frac{V_T}{2I_Q^2} \tag{A.3}$$

where $Z_e(s) = R_e + sL_e$, $Z_b(s) = R_s + R_b + sL_b$, $Z(s) = Z_e(s) + Z_b(s)$, $C_\pi = C_{je} + \tau g_m$. R_e is the emitter resistance including the finite Q of the L_e. R_s is the source resistance (50 Ω), R_b is the base resistance of the device. L_e and L_b are the matching inductors at the emitter and the base, respectively. C_{je} is the depletion capacitance, and τg_m is the diffusion capacitance of the device. V_s is the input voltage source and is equal to $V_p \cos(\omega_0 t)$. The responsivity is defined as the output DC voltage due to non-linearity divided by the available input power and can expressed as

$$\Re = \frac{V_{OUT,DC}}{P_{avs}} = \frac{\frac{V_p^2}{2} A_2(s, -s) R_L}{\frac{V_p^2}{8R_s}} \tag{A.4}$$

Considering the input impedance match condition,

$$R_s = R_b + R_e + \frac{g_m}{C_\pi} L_e \tag{A.5}$$

$$s(L_e + L_b) + \frac{1 + g_m R_e}{s C_\pi} = 0 \tag{A.6}$$

Substituting (A.2), (A.3), (A.5) and (A.6) into (A.4) yields

$$\Re = \frac{g_m}{1 + g_m R_e} \frac{R_L}{2 w_0^2 C_\pi^2 R_s V_T} \tag{A.7}$$

Appendix B

Derivation of the BER for a Non-ideal OOK Modulation

In a binary scheme where symbols are transmitted every T_b seconds, let $p(t)$ and $q(t)$ be the two pulses used to transmit bit 1 and 0. In an ideal on-off keying $q(t)$ = 0, but there is a residual signal in the OOK modulator due to the LO leakage, and $q(t) \neq 0$. The BER for an optimum binary receiver has been derived in [23], and is

$$BER = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_p + E_q - 2E_{pq}}{4N_0}}\right) \tag{B.1}$$

where

$$\text{erfc}(x) = \frac{2}{\sqrt{\pi}}\int_x^\infty e^{-y^2}\,dy \tag{B.2}$$

E_p and E_q are the energies of $p(t)$ and $q(t)$, respectively, and

$$E_{pq} = \int_0^{T_b} p(t)q(t)\,dt \tag{B.3}$$

Let $q(t) = \alpha p(t)$, then

$$E_q = \alpha^2 E_p \qquad E_{pq} = \alpha E_p \tag{B.4}$$

The BER can be expressed in terms of a more basic parameter E_b, the energy per bit. Assuming bit 1 and 0 are equally likely, E_b is the mean of E_p and E_q. Hence,

$$E_b = \frac{E_p + E_q}{2} \tag{B.5}$$

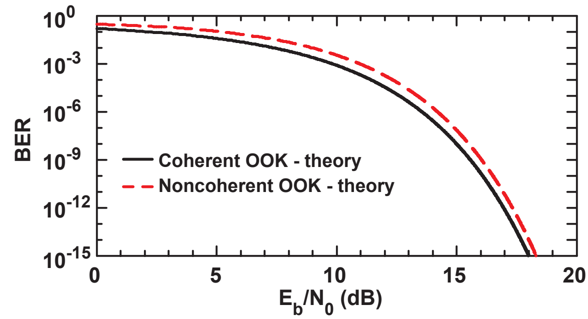


Figure B.1: BER versus E_b/N_0 for coherent and noncoherent OOK modulation.

Substituting (B.4) and (B.5) into (B.1) yields the BER for a coherent OOK detection, and it is expressed as

$$BER = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{2N_0}\frac{(1-\alpha)^2}{1+\alpha^2}}\right) \tag{B.6}$$

For the case of a noncoherent OOK receiver, the BER is derived in [86], and is

$$BER = \frac{1}{2}e^{-\frac{1}{2}\frac{E_b}{N_0}} \tag{B.7}$$

Fig. B.1 shows the BER versus E_b/N_0 for theoretical coherent OOK (Eq. 2.4) and noncoherent OOK (Eq. B.7). The difference between the coherent and noncoherent OOK to achieve the same BER of 10^{-12} is $<$ 0.5 dB, virtually they are same for all practical purposes. Since the mathematics involved with the noncoherent OOK analysis (especially for the LO leakage) is tedious, all the analysis presented in Chapter 2 are based on the coherent OOK.

Appendix C

Isolation Comparison of Series and Shunt Switches

C.1 Without an Inductor

The series and shunt switch isolation performance is compared for the condition that both switches have the same insertion loss. Assuming the transistor can be modeled as a resistor (R) in the on-state and a capacitor (C) in the off-state (Fig. C.1(a)), S_{21} for both switches can be expressed as

$$S_{21} = \frac{2Z_0}{2Z_0 + Z_{series}} \qquad \text{and} \qquad S_{21} = \frac{2Z_{shunt}}{Z_0 + 2Z_{shunt}} \tag{C.1}$$

for the series and shunt switches, respectively. (Fig. C.1(b)-(c)).

The $R_{on}[\Omega \cdot \mu m]$ and $C_{off}[fF/\mu m]$ are the two important figure of merits for switches. Let W_1 and W_2 be the widths of the series and shunt transistor switches, respectively. The insertion loss ($1/S_{21}$) can be expressed using

$$Z_{series} = \frac{R_{on}}{W_1} \qquad \text{and} \qquad Z_{shunt} = \frac{1}{j\omega W_2 C_{off}} \tag{C.2}$$

and is equal to

$$IL_{series} = \frac{2Z_0 + \dfrac{R_{on}}{W_1}}{2Z_0} \qquad \text{and} \qquad IL_{shunt} = \frac{2 + j\omega W_2 C_{off} Z_0}{2} \tag{C.3}$$

$$|IL_{series}|^2 = \left(1 + \frac{R_{on}}{2Z_0 W_1}\right)^2 \qquad \text{and} \qquad |IL_{shunt}|^2 = 1 + \left(\frac{\omega W_2 C_{off} Z_0}{2}\right)^2 \tag{C.4}$$

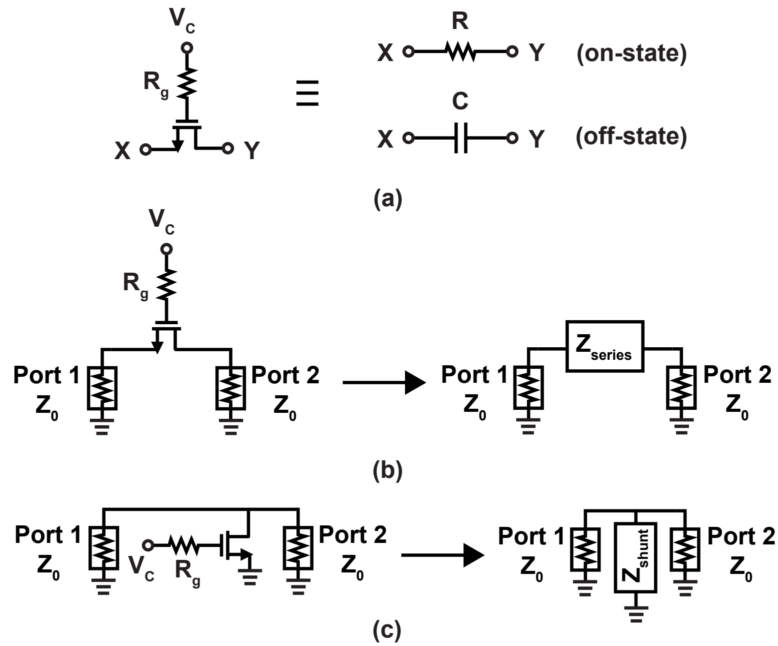


Figure C.1: (a) Equivalent simple model for a transistor switch in the on and off states; (b) Series switch; (c) Shunt switch.

Using the same procedure, the isolation (S_{21}) can be expressed using

$$Z_{series} = \frac{1}{j\omega W_1 C_{off}} \qquad \text{and} \qquad Z_{shunt} = \frac{R_{on}}{W_2} \tag{C.5}$$

and is equal to

$$ISO_{series} = \frac{j2\omega W_1 C_{off} Z_0}{1 + j2\omega W_1 C_{off} Z_0} \qquad \text{and} \qquad ISO_{shunt} = \frac{\frac{2R_{on}}{W_2}}{Z_0 + \frac{2R_{on}}{W_2}} \tag{C.6}$$

$$\frac{1}{|ISO_{series}|^2} = 1 + \left(\frac{1}{2\omega W_1 C_{off} Z_0}\right)^2 \qquad \text{and} \qquad \frac{1}{|ISO_{shunt}|^2} = \left(1 + \frac{Z_0 W_2}{2R_{on}}\right)^2 \tag{C.7}$$

Let A, B, X, Y be equal to

$$A = \frac{R_{on}}{2Z_0 W_1} \qquad \text{and} \qquad B = \frac{Z_0 W_2}{2R_{on}} \tag{C.8}$$

$$X = \frac{\omega W_2 C_{off} Z_0}{2} \qquad \text{and} \qquad Y = \frac{1}{2\omega W_1 C_{off} Z_0} \tag{C.9}$$

Note that $AB = XY$.

The isolation of the switches is then compared when both switches have the same insertion loss. Substituting (C.8) and (C.9) into (C.4) and (C.7) yields

$$|IL_{series}|^2 = (1+A)^2 = |IL_{shunt}|^2 = 1 + X^2 \tag{C.10}$$

$$\frac{1}{|ISO_{series}|^2} = 1 + Y^2 \qquad \text{and} \qquad \frac{1}{|ISO_{shunt}|^2} = (1+B)^2 \tag{C.11}$$

The goal is to show that $|ISO_{shunt}|^2 < |ISO_{series}|^2$ when both switches have the same insertion loss. Considering (C.10), (C.11) and $AB = XY$ and knowing that A, B, X and Y are all positive real numbers such that $(1+A)^2 = 1 + X^2$ and $AB = XY$, it is shown that $1 + Y^2 < (1+B)^2$ is true.

$$(1+A)^2 = 1 + 2A + A^2 = 1 + X^2 \Rightarrow X > A \tag{C.12}$$

$$X > A \quad \text{and} \quad AB = XY \Rightarrow Y < B \tag{C.13}$$

$$Y < B \Rightarrow Y^2 < B^2 \Rightarrow 1 + Y^2 < 1 + B^2 < 1 + 2B + B^2 \tag{C.14}$$

$$\Rightarrow 1 + Y^2 < (1+B)^2 \tag{C.15}$$

It can be concluded that the isolation of the shunt switch is always better than the series switch when they have the same insertion loss.

C.2 With an Inductor

The above analysis do not include the matching networks. An inductor could be placed between the source and drain nodes of the transistor to cancel the off-state capacitance which results in a better isolation for the series switch and an improved return loss for the shunt switch at high frequencies (Fig. C.2). Therefore, it is of interest to analyze the effect of this inductor. For the series switch (transistor width of W_1), L_1 is used and R_1 $(= Q\omega L_1)$ represents the parasitic resistor due to the finite inductor Q. Likewise, W_2, L_2 and R_2 are used for the shunt switch.

When the series transistor is on, the insertion loss is determined by the equivalent impedance of $\frac{R_{on}}{W_1} \parallel j\omega L_1 \parallel R_1$ which is mostly dominated by the on-resistance. The isolation is determined by R_1 since L_1 cancels the off-state capacitance $(W_1 C_{off})$.

The shunt switch insertion loss is determined by the R_2 since L_2 and $W_2 C_{off}$ cancel each other. Its isolation is determined by $\frac{R_{on}}{W_2} \parallel j\omega L_2 \parallel R_2 \approx \frac{R_{on}}{W_2}$. Therefore, the insertion loss and isolation for both switches can be expressed as

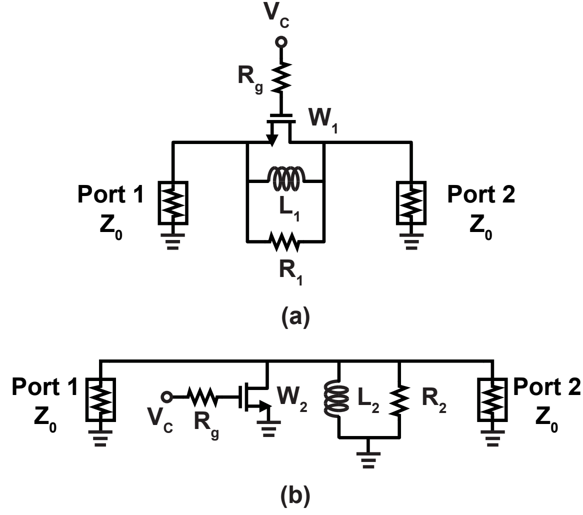


Figure C.2: (a) Series switch with an inductor for isolation and (b) shunt switch with an impedance matching inductor. R_1 and R_2 are the parasitic resistances due to inductor Q.

$$IL_{series} = 1 + \frac{R_{on}}{2Z_0W_1} \quad \text{and} \quad IL_{shunt} = 1 + \frac{Z_0}{2R_2} \tag{C.16}$$

$$\frac{1}{ISO_{series}} = 1 + \frac{R_1}{2Z_0} \quad \text{and} \quad \frac{1}{ISO_{shunt}} = 1 + \frac{Z_0W_2}{2R_{on}} \tag{C.17}$$

R_1 and R_2 can be expressed as

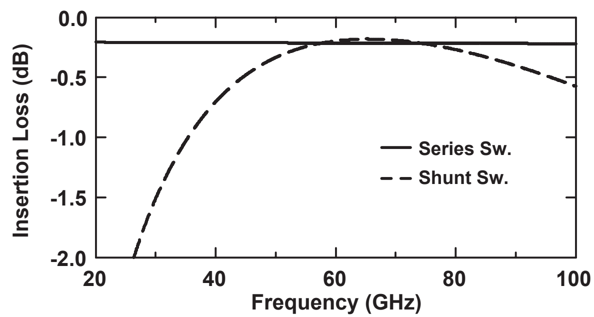
$$R_1 = Q_1\omega L_1 = \frac{Q_1}{\omega W_1 C_{off}} \quad \text{and} \quad R_2 = Q_2\omega L_2 = \frac{Q_2}{\omega W_2 C_{off}} \tag{C.18}$$

Subsituting C.18 into C.16 and C.17 yields

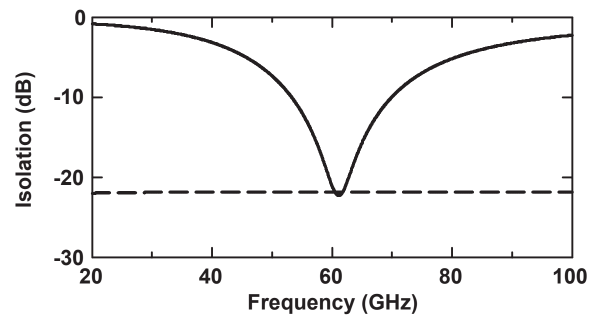
$$IL_{series} = 1 + \frac{R_{on}}{2Z_0W_1} \quad \text{and} \quad IL_{shunt} = 1 + \frac{\omega W_2 C_{off} Z_0}{2Q_2} \tag{C.19}$$

$$\frac{1}{ISO_{series}} = 1 + \frac{Q_1}{2\omega W_1 C_{off} Z_0} \quad \text{and} \quad \frac{1}{ISO_{shunt}} = 1 + \frac{Z_0W_2}{2R_{on}} \tag{C.20}$$

Assuming $Q_1 = Q_2$, C.19 and C.20 state that both switches will also have the same isolation given that they have the same insertion loss. This is quite an interesting result. To verify this result, shunt and series switches are simulated in 45-nm CMOS SOI process with $W_1 = W_2 = 130$ μm and $L_1 = L_2 = 201$ pH ($Q = 15$) at 60 GHz. The W_1 and W_2 values are chosen to satisfy $IL_{series} = IL_{shunt}$ in (C.19). Fig. C.3 presents the simulated insertion loss and isolation of the switches and both switches have the same insertion loss and isolation at $\sim$60 GHz, as expected. However, a shunt switch could be preferred if a wideband operation is desired since the series switch isolation is narrowband. Also, the drain and source contact resistances



(a)



(b)

Figure C.3: Simulated (a) insertion loss and (b) isolation of the series and shunt switches with inductors.

from the bottom metal to top metal should be considered. The shunt transistor source node can be connected to a large M1 (bottom metal) ground plane, therefore only the drain contact resistance will effect the overall performance. However, the series switch will suffer from both drain/source contact parasitics.

Appendix D

Single-Shunt and Double-Shunt Switches

The isolation performance of single-shunt (SS) and double-shunt (DS) switches will be analyzed in this section. An SS switch includes a single shunt transistor and an inductor (L_1) which resonates its off-state capacitance; whereas a DS switch consists of two (double) shunt transistors and an inductor (L_2) which form a π-network. For a fair comparison, the transistor width in the SS switch should be two times larger than the DS switch. Therefore, the off-state capacitance and on-resistance are represented by $2C$ and R for the SS switch; whereas they are C and $2R$ for the DS switch (Fig. D.1).

The inductors in the SS and DS switches are chosen so as to resonate out the capacitances at the operating frequency (ω_0). Therefore, L_1 and L_2 can be expressed as

$$L_1 = \frac{1}{\omega_0^2 2C} \qquad \text{and} \qquad L_2 = \frac{2CZ_0^2}{1+\omega_0^2 C^2 Z_0^2} \tag{D.1}$$

The isolation of the SS and DS switches are calculated using the on-state equivalent models in Fig. D.1 and are expressed as

$$\frac{1}{|ISO_{SS}|^2} = \left(1+\frac{Z_0}{2R}\right)^2 + \left(\frac{Z_0}{2\omega L_1}\right)^2 \tag{D.2}$$

$$\frac{1}{|ISO_{DS}|^2} = \left(1+\frac{Z_0}{2R}\right)^2 + \left(\frac{\omega L_2(2R+Z_0)^2}{8R^2 Z_0}\right)^2 \tag{D.3}$$

It is apparent that $|ISO_{SS}| = 0$ ($-\infty$ dB) at DC ($\omega = 0$) since L_1 is short, and $|ISO_{DS}| = 0$ ($-\infty$ dB) at $\omega = \infty$ since L_2 is open. Also $|ISO_{SS}|$ (at $\omega = \infty$) is equal

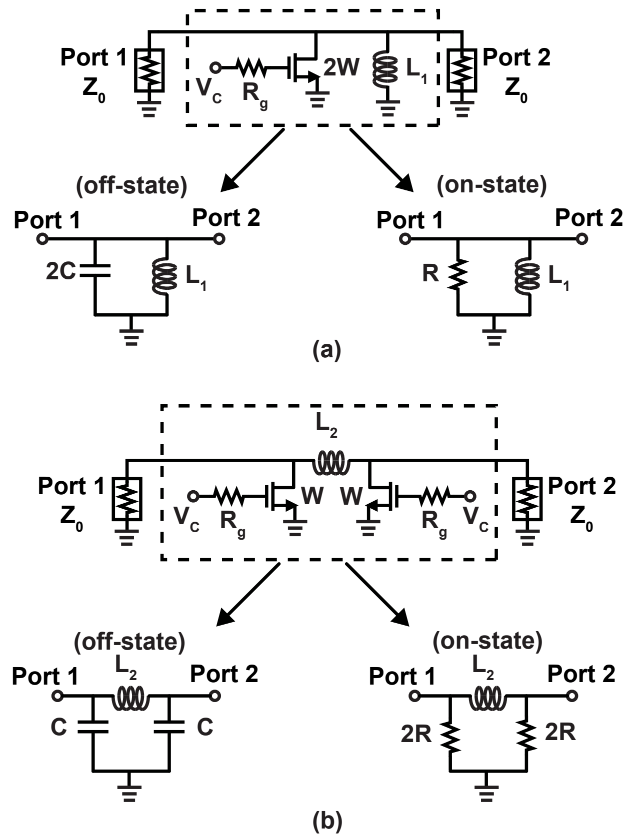


Figure D.1: (a) Single-shunt switch and its on/off-state equivalent models; (b) double-shunt switch and its on/off-state equivalent models.

to $|ISO_{DS}|$ (at $\omega = 0$). Therefore, the isolation versus frequency curves will intersect at a certain frequency, and it will be shown that this intersection point (ω_i) is lower than the operating frequency (ω_0). At ω_i, $|ISO_{SS}|^2 = |ISO_{DS}|^2$ and substituting D.1 into D.2 and D.3 yields

$$\omega_i = \omega_0 \sqrt{\left(\frac{2R}{2R + Z_0}\right)^2 + \left(\frac{\omega_0}{\omega_{RC}}\right)^2 \left(\frac{Z_0}{2R + Z_0}\right)^2} \tag{D.4}$$

where $\omega_{RC} = 2RC$ is the multiplication of the transistor on-resistance and off-state capacitance. The ω_{RC} value depends on the technology (i.e. $2\pi(880)$ GHz for 45-nm CMOS SOI and $2\pi(530)$ GHz for 65-nm bulk CMOS), but most of the time it is much higher than the operating frequency (ω_0). Assuming $\omega_0 \ll \omega_{RC}$ and $2R + Z_0 \approx Z_0$, D.4 can be simplified to

$$\omega_i \approx \omega_0 \frac{2R}{Z_0} \tag{D.5}$$

where $2R$ is typically less than 5-10 Ω. Therefore, the isolation of a DS switch is better than an SS switch at $\omega > (0.1 - 0.2)\omega_0$. It should also be noted that the drain contact resistance from the bottom metal to the top metal has less effect on the performance of the DS switch since there are 2 transistors.

What happens if the number of shunt transistors is increased to 4 or even 8? The analysis will be undoubtedly tedious, but can be simulated easily using SpectreRF in Cadence. Fig. D.2 presents the schematic of the SS, DS, 4S and 8S switches and the transistor widths are 200, 100, 50 and 25 μm, respectively. The drain contact resistance is also included in the simulations (R_d = 1.5 Ω) and the Q of all inductors is 15 at 60 GHz. The simulations are done in a 45-nm CMOS SOI process and do not include the RC extraction of the transistors. Fig. D.3 presents the simulated S_{11}, insertion loss and isolation of the switches. The switch performance is better as the number of shunt transistors is increased. However, the difference between 4S and 8S switches is insignificant. Therefore, 4S switch is the optimum one considering the performance and area.

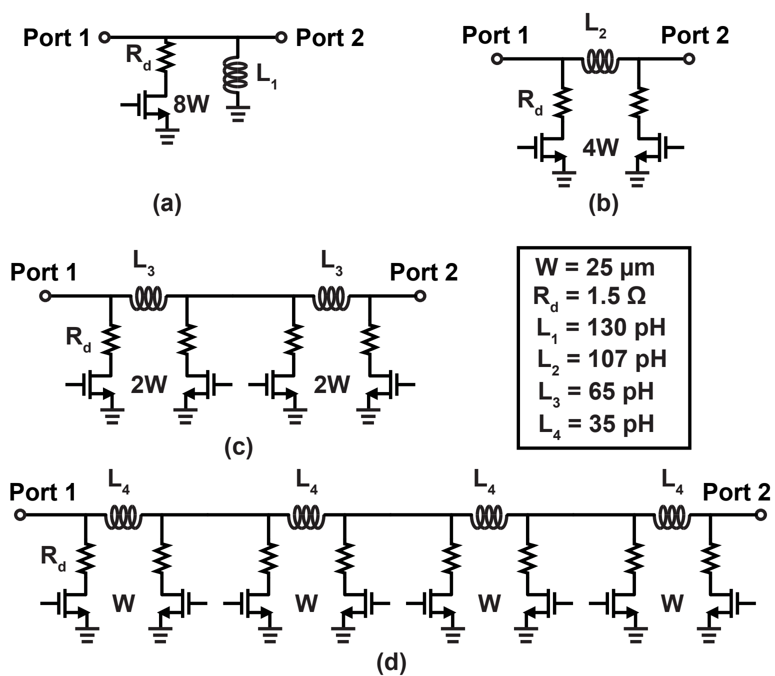
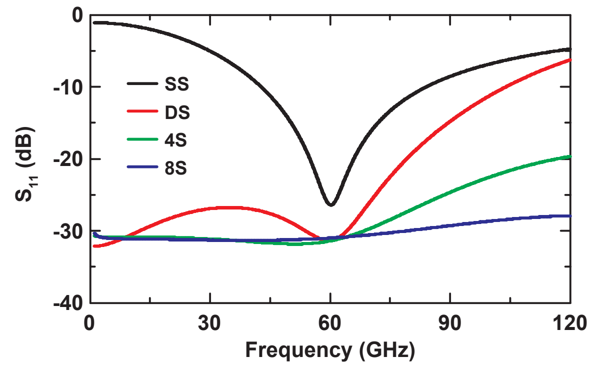
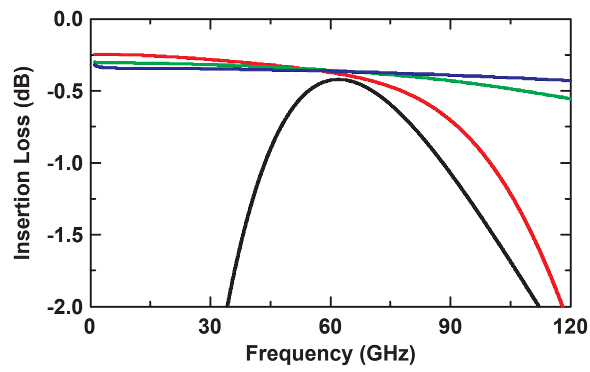


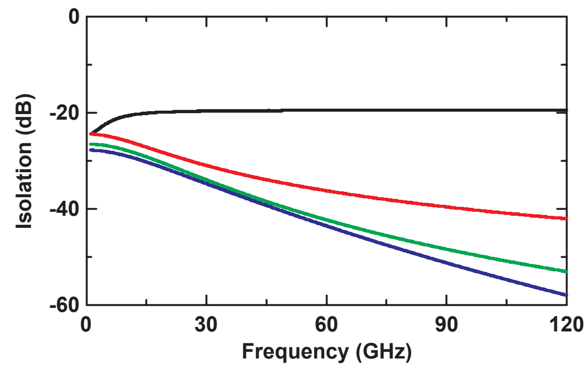
Figure D.2: Schematic of (a) SS, (b) DS, (c) 4S and (d) 8S switches.



(a)



(b)



(c)

Figure D.3: Simulated (a) S_{11}, (b) insertion loss and (c) isolation of the SS, DS, 4S and 8S switches.

Bibliography

[1] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2820–2831, December 2006.

[2] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, S. D. Yamamoto, R. Pilard, P. Busson, A. Cathelin, D. Belot, and P. Vincent, "A 65-nm CMOS fully integrated transceiver module for 60-GHz wireless HD applications," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 3005–3017, December 2011.

[3] K. Okada, K. M. N. Li, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2988–3004, December 2011.

[4] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, and S. P. Voinigescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2085–2099, August 2009.

[5] E. R. Brown, "Fundamentals of terrestrial millimeter-wave and THz remote sensing," *Int. J. High Speed Electron. Syst.*, vol. 13, pp. 995–1097, 2003.

[6] J. W. May and G. M. Rebeiz, "Design and characterization of W-band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory Tech.*, vol. 58, pp. 1420–1430, May 2010.

[7] E. Dacquay, A. Tomkins, K. H. K. Yau, E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "D-band total power radiometer performance optimization in an SiGe HBT technology," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 813–826, March 2012.

[8] L. Gilreath, V. Jain, and P. Heydari, "Design and analysis of a W-band SiGe direct-detection-based passive imaging receiver," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2240–2252, October 2011.

[9] Z. Chen, C.-C. Wang, H.-C. Yao, and P. Heydari, "A BiCMOS W-Band 2$\times$2 focal-plane array with on-chip antenna," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2355–2371, October 2012.

[10] R. Han, Y. Zhang, Y. Kim, D. Y. Kim, H. Shichijo, E. Afshari, and K. O, “280 GHz and 860 GHz image sensors using schottky-barrier diodes in 0.13 μm digital CMOS,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, February 2012, pp. 254–256.

[11] E. Ojefors, U. R. Pfeiffer, A. Lisauskas, and H. G. Roskos, “A 0.65 THz focal-plane array in a quarter-micron CMOS process technology,” *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 1968–1976, July 2009.

[12] H. Sherry, J. Grzyb, Y. Zhao, R. A. Hadi, A. Cathelin, A. Kaiser, and U. Pfeiffer, “A 1kpixel CMOS camera chip for 25fps real-time terahertz imaging applications,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, February 2012, pp. 252–254.

[13] R. A. Hadi, H. Sherry, J. Grzyb, N. Baktash, Y. Zhao, E. Ojefors, A. Kaiser, A. Cathelin, and U. Pfeiffer, “A broadband 0.6 to 1 THz CMOS imaging detector with an integrated lens,” in *IEEE Int. Microwave Symp. Dig.*, June 2011.

[14] K. Kang, F. Lin, D.-D. Pham, J. Brinkhoff, C.-H. Heng, Y. X. Guo, and X. Yuan, “A 60-GHz OOK receiver with an on-chip antenna in 90 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1720–1731, September 2010.

[15] W. Shin, M. Uzunkol, and G. M. Rebeiz, “Ultra low power 60 GHz ASK SiGe receiver with 3-6 Gbps capabilities,” in *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2009, pp. 1–4.

[16] M. F. Karim, Y.-X. Guo, M. Sun, J. Brinkhoff, L. C. Ong, K. Kang, and F. Lin, “Integration of SiP-based 60-GHz 4×4 antenna array with CMOS OOK transmitter and LNA,” *IEEE Trans. Microw. Theory Tech.*, vol. 59, pp. 1869–1878, July 2011.

[17] W. Shin, M. Uzunkol, R. A. Alhalabi, and G. M. Rebeiz, “60 GHz low power 1.5 Gb/s ASK transmitter in 90 nm CMOS with on-board Yagi-Uda antenna,” in *IEEE European Microwave Conference*, September 2010, pp. 272–275.

[18] J. Lee, Y. Chen, and Y. Huang, “A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly,” *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 264–275, February 2010.

[19] E. Juntunen, M. C.-H. Leung, F. Barale, A. Rachamadugu, D. A. Yeh, B. G. Perumana, P. Sen, D. Dawn, S. Sarkar, S. Pinel, and J. Laskar, “A 60-GHz 38-pJ/bit 3.5-Gb/s 90-nm CMOS OOK digital radio,” *IEEE Trans. Microw. Theory Tech.*, vol. 58, pp. 348–355, February 2010.

[20] W.-H. Chen, S. Joo, S. Sayilir, R. Willmot, T.-Y. Choi, D. Kim, J. Lu, D. Peroulis, and B. Jung, “A 6-Gb/s wireless inter-chip data link using 43-GHz transceivers and bond-wire antennas,” *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2711–2721, October 2009.

[21] *BiCMOS-8HP model reference guide*, V1.2.1.0hp ed., Compact Model Development CL4V Dept., IBM Microelectronics Division, June 2011.

[22] *Sonnet v12*, www.sonnetsoftware.com, Sonnet Software Inc., Syracuse, NY.

[23] B. P. Lathi, *Modern digital and analog communication systems*, 3rd ed. Oxford, 1998.

[24] http://pdfserv.maxim-ic.com/en/an/AN2815.pdf.

[25] http://www.markimicrowave.com/menus/datasheets/M9-0765.pdf.

[26] R. J. Dengler, A. Skalare, and P. H. Siegel, "Passive and active imaging of humans for contraband detection at 640 GHz," in *IEEE Int. Microwave Symp. Dig.*, June 2004, pp. 1591–1594.

[27] K. B. Cooper, R. J. Dengler, N. Llombart, B. Thomas, G. Chattopadhyay, and P. H. Siegel, "THz Imaging Radar for Standoff Personnel Screening," *IEEE Trans. Terahertz Science Tech.*, vol. 1, pp. 169–182, September 2011.

[28] P. H. Siegel, "THz technology," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 910–928, March 2002.

[29] J. J. Lynch, H. P. Moyer, J. H. Schaffner, Y. Royter, M. Sokolich, B. Hughes, Y. J. Yoon, and J. N. Schulman, "Passive millimeterwave imaging module with preamplified zero-bias detection," *IEEE Trans. Microwave Theory Tech.*, vol. 56, pp. 1592–1600, July 2008.

[30] D. T. Petki, F. C. D. Lucia, C. Castro, P. Helminger, E. L. Jacobs, S. K. Moyer, S. Murrill, C. Halford, S. Griffin, and C. Franck, "Active and passive millimeter- and sub-millimeter-wave imaging," *Proc. SPIE*, vol. 5989, 2005.

[31] R. Appleby and H. B. Wallace, "Standoff detection of weapons and contraband in the 100 GHz to 1 THz region," *IEEE Trans. Antenna Propag.*, vol. 55, pp. 2944–2956, November 2007.

[32] H. Kazemi, C. Nguyen, B. Brar, G. M. Rebeiz, G. Nagy, L. Tran, A. Young, and E. R. Brown, "Low cost modular integrated horn antenna array using heterojunction barrier diode detectors," in *IEEE Int. Microwave Symp. Dig.*, June 2008, pp. 297–300.

[33] D. M. Sheen, T. E. Hall, R. H. Severtsen, D. L. McMakin, B. K. Hatchell, and P. L. J. Valdez, "Active wideband 350 GHz imaging system for concealed-weapon detection," *Proc. SPIE*, vol. 7309, 2009.

[34] L. Yujiri, M. Shoucri, and P. Moffa, "Passive millimeter-wave imaging," *IEEE Microwave Magazine*, vol. 4, pp. 39–50, September 2003.

[35] F. Friederich, W. von Spiegel, M. Bauer, F. Meng, M. Thomson, S. Boppel, A. Lisauskas, B. Hils, V. Krozer, A. Keil, T. Loffler, R. Henneberger, A. Huhn, G. Spickermann, P. Bolivar, and H. Roskos, "THz active imaging systems with real-time capabilities," *IEEE Trans. Terahertz Science Tech.*, vol. 1, pp. 183–200, September 2011.

[36] F. Ulaby, R. Moore, and A. Fung, *Microwave Remote Sensing: Active and Passive, Volume I: Fundamentals and Radiometry*. Artech House, Norwood, MA, 1991.

[37] S. S. Gearhart and G. M. Rebeiz, "A monolithic 250 GHz Schottky diode receiver," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2504–2511, December 1994.

[38] S. Raman, S. Barker, and G. Rebeiz, "A W-band dielectric-lens-based integrated monopulse radar receiver," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2283–2288, December 1998.

[39] G. Gauthier, J.-P. Raskin, and G. Rebeiz, " 140-170 GHz low-noise uniplanar suhbharmonic Schottky-receiver," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1416–1419, August 2000.

[40] *Design application note for the SBC18H3 process*, Jazz Semiconductor, Inc., Newport Beach, CA, 2010.

[41] W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou, and G. M. Rebeiz, "A 108-114 GHz 4×4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE Journal of Solid-State Circuits*, submitted for publication.

[42] J. M. Edwards and G. M. Rebeiz, "High-efficiency elliptical slot antennas with quartz superstrates for silicon RFICs," *IEEE Trans. Antenna Propag.*, vol. 60, pp. 5010–5020, November 2012.

[43] I. Sarkas, J. Hasch, A. Balteanu, and S. P. Voinigescu, "A fundamental frequency 120-GHz SiGe BiCMOS distance sensor with integrated antenna," *IEEE Trans. Microwave Theory Tech.*, vol. 60, pp. 795–812, March 2012.

[44] R. A. Alhalabi and G. M. Rebeiz, "Design of high-efficiency millimeter-wave microstrip antennas for silicon RFIC applications," in *IEEE Antennas Propag. Symp.*, July 2011, pp. 2055–2058.

[45] M. Uzunkol, W. Shin, and G. M. Rebeiz, "Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance," *IEEE Trans. Microwave Theory Tech.*, vol. 60, pp. 3263–3271, October 2012.

[46] http://www.vadiodes.com.

[47] http://www.vadiodes.com/images/stories/AppNotes/ vdi feedhorn summary 2011_10_31.pdf.

[48] *Model SR550/552: Voltage Pre-Amplifier*, Stanford Res. Syst., Sunnyvale, CA, 2001.

[49] J.-L. Kuo, Y.-F. Lu, T.-Y. Huang, Y.-L. Chang, Y.-K. Hsieh, P.-J. Peng, I.-C. Chang, T.-C. Tsai, K.-Y. Kao, W.-Y. Hsiung, J. Wang, Y. A. Hsu, K.-Y. Lin, H.-C. Lu, Y.-C. Lin, L.-H. Lu, T.-W. Huang, R.-B. Wu, and H. Wang, "60-GHz four-element phased-array transmit/receive system-in-package using phase compensation techniques in 65-nm flip-chip CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 743–756, March 2012.

[50] E. Cohen, C. G. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four-element phased array at 60 GHz with RF-IF conversion block in 90-nm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 58, pp. 1438–1446, May 2010.

[51] D.-W. Kang, J.-G. Kim, B.-W. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Tech.*, vol. 57, pp. 3534–3543, December 2009.

[52] K.-J. Kim, K. H. Ahn, T. H. Lim, H. C. Park, and J.-W. Yu, "A 60 GHz wideband phased-array LNA with short-stub passive vector generator," *IEEE Microwave and Wireless Comp. Lett.*, vol. 20, pp. 628–630, November 2010.

[53] C. F. Campbell and S. A. Brown, "A compact 5-Bit phase-shifter MMIC for K-band satellite communication systems," *IEEE Trans. Microw. Theory Tech.*, vol. 48, pp. 2652–2656, December 2000.

[54] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60 GHz CMOS receiver front-end with frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1030–1037, April 2008.

[55] B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170-200 GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 692–701, March 2012.

[56] M. Uzunkol and G. M. Rebeiz, "140-220 GHz SPST and SPDT switches in 45 nm CMOS SOI," *IEEE Microwave and Wireless Comp. Lett.*, vol. 22, pp. 412–414, August 2012.

[57] ——, "Ultra low-loss 50–70 GHz SPDT switch in 90 nm CMOS," in *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2009, pp. 1–4.

[58] S.-F. Chao, H. Wang, C.-Y. Su, and J. Chern, "A 5094 GHz CMOS SPDT switch using traveling-wave concept," *IEEE Microwave and Wireless Comp. Lett.*, vol. 17, pp. 130–132, February 2007.

[59] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imager in 65 nm bulk CMOS," in *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2008, pp. 1–4.

[60] Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-loss 0.13-μm CMOS 50–70 GHz SPDT and SP4T switches," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 43–46.

[61] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC–70 GHz SP4T switch in 0.13-μm CMOS," in *IEEE Int. Microwave Symp. Dig.*, June 2009, pp. 1093–1096.

[62] I. Kallfass, S. Diebold, H. Massler, S. Koch, M. Seelmann-Eggebert, and A. Leuther, "Multiple-throw millimeter-wave FET switches for frequencies from 60 up to 120 GHz," in *IEEE European Microwave Conference*, October 2008, pp. 1453–1456.

[63] R. A. Alhalabi and G. M. Rebeiz, "High-gain yagi-uda antennas for millimeter-wave switched-beam systems," *IEEE Trans. Antennas and Propagation*, vol. 57, pp. 3672–3676, November 2009.

[64] O. Inac, B. Cetinoneri, M. Uzunkol, Y. A. Atesal, and G. M. Rebeiz, "Millimeter-wave and THz circuits in 45-nm SOI CMOS," in *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2011, pp. 1–4.

[65] Y. Yu, P. G. M. Baltus, A. de Graauw, E. van der Heijden, C. S. Vaucher, and A. H. M. van Roermund, "A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1697–1709, September 2010.

[66] B.-W. Min and G. M. Rebeiz, “Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS,” *IEEE Trans. Microw. Theory Tech.*, vol. 56, pp. 1364–1371, June 2008.

[67] Y. Nakasha, M. Sato, T. Tajima, Y. Kawana, T. Suzuki, and T. Takahashi, “W-band transmitter and receiver modules for 10-Gb/s impulse radio,” in *IEEE Int. Microwave Symp. Dig.*, June 2009, pp. 553–556.

[68] T. M. Hancock and G. M. Rebeiz, “Design and analysis of a 70 ps differential SiGe RF switch,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 2403–2410, July 2005.

[69] V. Jain, F. Tzeng, L. Zhou, , and P. Heydari, “A single-chip dual-band 22-to-29 GHz/ 7781 GHz BiCMOS transceiver for automotive radars,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, February 2009, pp. 308–309.

[70] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, N. Kinayman, N. Jain, R. Anderson, F. Kolak, R. Wohlert, S. P. Bawell, J. Bennett, and J.-P. Lanteri, “Ultra-wideband radar sensors for short-range vehicular applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 52, pp. 2105–2122, September 2004.

[71] E. Adabi and A. M. Niknejad, “A mm-wave transformer based transmit/receive switch in 90 nm CMOS technology,” in *IEEE European Microwave Conference*, September 2009, pp. 389–392.

[72] J. He and Y. P. Zhang, “Design of SPST/SPDT switches in 65 nm CMOS for 60 GHz applications,” in *IEEE Asia-Pacific Microwave Conference*, December 2008, pp. 1–4.

[73] E. Ojefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, “A 820 GHz SiGe chipset for terahertz active imaging applications,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, February 2011, pp. 224–226.

[74] A. Hirata, T. Kosugi, H. Takahashi, J. Takeuchi, H. Togo, M. Yaita, N. Kukutsu, K. Aihara, K. Murata, Y. Sato, T. Nagatsuma, and Y. Kado, “120-GHz-band wireless link technologies for outdoor 10-Gbit/s data transmission,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 881–895, March 2012.

[75] Y. A. Atesal, B. Cetinoneri, M. Chang, and G. M. Rebeiz, “Millimeter-wave wafer-scale silicon BiCMOS power amplifiers using free-space power combining,” *IEEE Trans. Microw. Theory Tech.*, vol. 59, pp. 954–965, April 2011.

[76] Z. Xu, Q. J. Gu, and M.-C. F. Chang, “A three stage, fully differential 128-157 GHz CMOS amplifier with wide band matching,” *IEEE Microwave and Wireless Comp. Lett.*, vol. 21, pp. 550–552, October 2011.

[77] O. Inac, A. Fung, and G. M. Rebeiz, “Double-Balanced 130-180 GHz passive and balanced 145-165 GHz active mixers in 45 nm CMOS,” in *IEEE Custom Integrated Circuits Conf.*, September 2011, pp. 1–4.

[78] E. Laskin, M. Khanpour, S. T. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, and S. P. Voinigescu, “Nanoscale CMOS transceiver design in the 90-170 GHz range,” *IEEE Trans. Microw. Theory Tech.*, vol. 57, pp. 3477–3490, December 2009.

[79] U. Yodprasit, R. Fujimoto, M. Motoyoshi, K. Takano, and M. Fujishima, "D-band 3.6-dB-insertion-loss ASK modulator with 19.5-dB isolation in 65-nm CMOS technology," in *IEEE Asia-Pacific Microwave Conference*, December 2010, pp. 1853–1856.

[80] F. Golcuk, J. M. Edwards, B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A 163-180 GHz 2×2 amplifier-doubler array with peak EIRP of +5 dBm," *submitted to IEEE Radio Frequency Integrated Circuits Symp.*, June 2013.

[81] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," in *IEEE Int. Electron Devices Meeting*, December 2007, pp. 255–258.

[82] M. Uzunkol and G. M. Rebeiz, "A low-loss 50-70 GHz SPDT switch in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2003–2007, October 2010.

[83] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A 94GHz SPST switch in 65nm bulk CMOS," in *IEEE Compound Semiconductor Integrated Circuits Symp.*, October 2008, pp. 1–4.

[84] ——, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1981–1991, October 2010.

[85] K. L. Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 548–555, April 1998.

[86] L. W. Couch, *Digital and analog communication systems*, 5th ed. Prentice-Hall, 1997.