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Theta Phase-Specific Closed-Loop Stimulation in Implantable Neuromodulation Devices

Author
ALZUHAIR, AHMED FAHAD A

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Theta Phase-Specific Closed-Loop Stimulation in Implantable Neuromodulation Devices

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical and Computer Engineering

by

Ahmed Fahad A Alzuhair

2019

ABSTRACT OF THE DISSERTATION

Theta Phase-Specific Closed-Loop Stimulation

in Implantable Neuromodulation Devices

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Ahmed Fahad A Alzuhair

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2019

Professor Dejan Marković, Chair

Deep brain stimulation (DBS) is increasingly used to mitigate a variety of brain disorders, which is driving the interest in understanding and creating the optimal conditions for delivery of stimulation pulses. Generally, therapeutic DBS is open loop, with limited sensing in epilepsy devices. Epilepsy monitoring is a welcoming clinical environment to study science of human memory, where encoding and retrieval of information occur at a specific phase of Theta-band brain waves. Beside treating epilepsy, there is a growing interest in using DBS for memory restoration. Stimulation could be more efficacious if we incorporate knowledge of the memory encoding or recall state to inform the stimulation decision process [1]. It was shown

that DBS enhances or inhibits memory when delivered at specific phases of the Theta rhythm [2-4].

Early Theta phase-locked (PL) (or phase-specific) experiments were fully supervised in the lab, and methods inaccuracies were overcome by repeated experiments. Later, efforts were made to realize real-time PL in software; these methods are supervised, requiring subject-specific complex optimization and manual settings, in addition to the high computational complexity [5, 6]. This work enables unsupervised, implantable size and power, phase-specific stimulation, closing the gap between implantable analog front-ends (AFE) and stimulation engines for smarter closed-loop control. Furthermore, compared to continuous stimulation, delivering stimulation pulses only when it matters results in an overall system power savings. This is crucial to implantable devices, since it translates to a smaller battery-size requirement or less frequent surgery for battery replacement.

To facilitate clinical studies and accelerate IC validation towards an implantable system, the PL IC was integrated with an AFE and a stimulation IC's in a small-scale hand-held portable platform. The closed-loop platform functionality was verified in-vitro in preparation for clinical studies, which have been recently approved by the UCLA institutional review board.

The platform features a graphical user interface for clinicians to design the closed-loop stimulation protocol parameters, such as targeted phase and the stimulation intensity for Theta-synchronized stimulation delivery. Therefore, facilitating a wide range of experiments that can, hopefully, bring us a step closer to restoring and enhancing memory.

The dissertation of Ahmed Fahad A Alzuhair is approved.

Gregory J. Pottie

Nanthia A. Suthana

Jonathan Chau-Yan Kao

Dejan Marković, Committee Chair

University of California, Los Angeles

2019

To My Parents, Hessah and Fahad…

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VITA

2006 – 2011 B.S. in Electrical Engineering, King Fahd University, Dharan, KSA.

2012 – 2013 Teaching Assistant, Department of Electrical Engineering, King Saud University, Riyadh, KSA

2013 – 2015 M.S. in Electrical Engineering, University of California, Los Angeles, USA.

2019 Engineering PhD Intern, Google Cloud Platforms, Sunnyvale, California.

AWARDS

2011 Prince Muhmmed bin Fahd prize for academic distinction, Dharan, KSA.

2011 MOHE undergraduate research accolade, Riyadh, KSA.

PUBLICATIONS

A. Alzuhair and D. Marković, "A 216 nW/Channel DSP Engine for Triggering Theta Phase-Locked Brain Stimulation," in *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS'17)*, Oct. 2017, pp. 1-4

1 | Introduction

1.1 Therapeutic Brain Stimulation

Since at least the beginning of the Anno Domini era, people have been fascinated with using electrical shocks for curation or pain relief as an alternative when traditional medicine techniques failed. In the 40's AD, Scribonius Largus, a physician of the Roman emperor Claudius, used torpedo fish (Figure 1.1) to deliver cranial electrical shocks to mitigate headaches [7]. Ibn-Saidh, an Andalusian scholar in the eleventh century, indicated that electric catfish could help with epilepsy when placed on the forehead [8]. In the hundreds of years that followed, numerous experiments studied the effects of cranial and intracranial stimulation when applied to both animals and humans. Surprisingly around thousand years ago - when only

Figure 1.1: Image of a Pacific electric ray or torpedo fish, courtesy of the U.S. National Oceanic and Atmospheric Administration.

primitive techniques were available - scholars were headed in the right direction of utilizing electrical shocks in brain therapy.

As surgical techniques to probe deeper brain regions took longer to mature, it was not until 1987 that deep brain stimulation (DBS) was shown to lessen tremor [9, 10]. Nowadays, implanted stimulation devices have allowed thousands of patients around the globe, who suffered from life-disrupting seizures, to lead better lives with

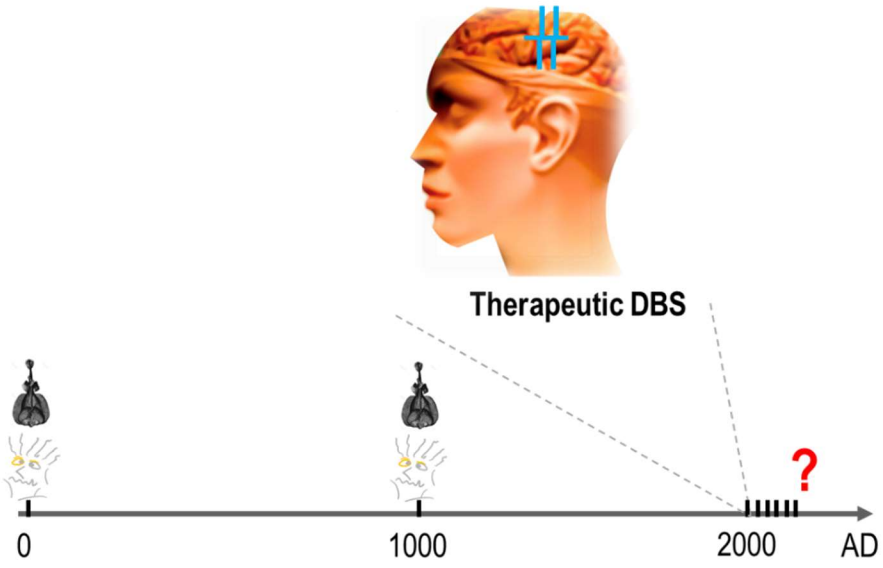

Figure 1.2: Recent years have seen increased application of electrical stimulation for therapy. At this accerlating pace, it is expected to see major technologicial and research breakthroughs in the few coming years.

66% reduction in seizures [11]. Only 40% reduction was reported in the first year - with NeuroPace RNS implantable device in [11] - suggesting that full potential of therapeutic stimulation may only be observed gradually.

The success in mitigating epilepsy has encouraged more efforts (Figure 1.2) to use stimulation to treat other brain-related illness such as Alzheimer disease. Although the mechanisms of memory encoding and recall in the brain are not well understood, it was shown recently that stimulating certain brain regions could improve memory [1,12].

1.2 Epilepsy: A Welcoming Environment to Study Brain Science

Since performing life-threating surgery is unjustified except for serious medical conditions, volunteering patients undergoing surgery for epilepsy device implantation have and continue to play a major role in advancing scientific research studying the human brain and the effects of different DBS protocols. The clinical experiments take place just after electrode implantation, in the hospitalization few-days-long period to localize the epilepsy source, and before the final surgery for device implantation.

1.3 Open-Loop Brain Stimulation

The applied DBS protocols are generally open loop, which could be a potential limitation on DBS effectiveness for therapy. For example, in memory experiments (Figure 1.3), the volunteering patients are typically shown a series of images to be encoded and later tested for recall with stimulation applied relative to an external stimulus such as prior to the image presentation. Therefore, stimulation is applied irrespective of the internal brain state, which could be a major limitation on stimulation effectiveness for therapy.

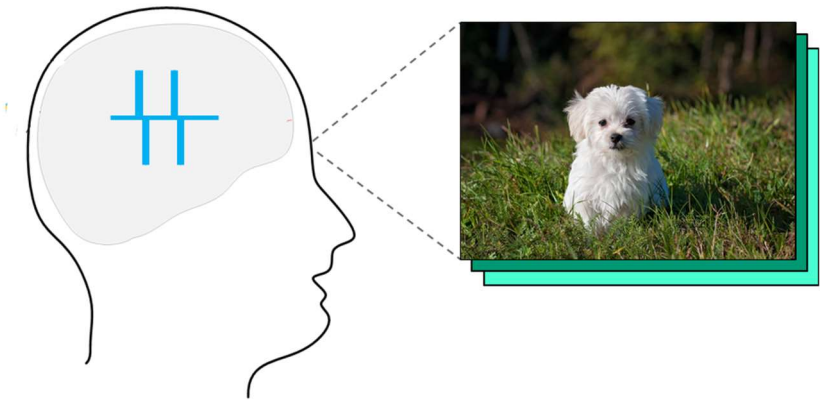

Figure 1.3: Stimulation in clinical experiments is generally applied in open-loop subject to an external stimulus such as image presentation in memory experiments.

1.4 Brain Stimulation Systems

Depending on the clinical experiment stage and patient needs, brain stimulation systems can be divided into four main classes that are summarized in Table 1.1. Compared to the outdated class I systems, class II systems - due to the compact form - offer freedom of movement, enabling more realistic setups mimicking normal everyday activity. Therefore, Class II systems are particularly suitable for integrated circuit validation and algorithm tuning before implantation.

Beyond applying stimulation in controlled clinical setups, Class III and IV offer long term brain therapy solutions. For example, NeuroPace RNS epilepsy system is a class IV system with a fully implantable platform for seizure onset detection and closed-loop seizure termination. Class IV eliminates external units that might be inconvenient and bothersome to wear - perhaps except for the occasional programming, battery recharging, and routine checks.

The majority of neuroscience laboratories use the outdated class I systems and bulky setups due to the limited offered options. Neurotechnology research must strive to advance neuromodulation systems to support studying the human brain and brain therapy research.

Table 1.1: Summary of brain stimulation systems classes

System Class	Highlights
I. Bedside-wired setups	Immobilized patient. Limited experiment duration & risk of infection
II. Portable devices	Compact form factor Freedom of movement Limited experiment duration & risk of infection
III. Implanted device + external stim control and processing unit	Long-term solution Inconvenient wearable supporting device Always-on power-hungry wireless transmission
IV. Fully implanted device	Compact form on-board closed-loop processing. All-in-one long-term solution

1.5 Challenges in Implantable Devices

Many challenges related to the implantable device energy and form factor restrict the on-board electronics design. Implantable device energy is a scarce commodity and efficient energy use could be as critical as lifesaving, since it reduces the frequency of surgery for battery replacement - a very dangerous procedure that may result in infection. This limited budget imposes strict constraints on the electronics within to achieve the lowest possible energy consumption. Moreover, maximum heat conduction to the surrounding tissue [17] sets the maximum power density

limits of the device. Finally, since devices are typically implanted just above the dura - after a small skull section is removed - the device size is another major constraint.

1.6 The Need for Closed-loop Algorithms

Compared to open-loop setups, closed-loop stimulation offers substantial benefits. Firstly, it allows delivery of brain-state informed stimulation. Secondly, compared to continuous or periodic stimulation, delivering stimulation pulses only when it matters results in an overall system power savings. As discussed previously, this is crucial to implantable devices, since it translates to a smaller battery-size requirement or less frequency of surgery for battery replacement. Moreover, less frequent DBS helps in mitigating DBS related side effects. Furthermore, having the unsupervised closed-loop processing chain fully implanted, the need for an always-on, power demanding wireless transmission is eliminated, in addition to the inconvenient external wearable supporting devices.

1.7 State-of-the-Art Closed-loop DBS Protocols

Beside NeuroPace RNS epilepsy system, another successful example of closed-loop DBS application is the 2018 work by Arlotti and colleagues [13]. The study investigated applying adaptive DBS to patients with Parkinson's disease (PD) subject to the local field potential (LFP) oscillation Beta (11-35 Hz) power activity. The experiment was performed for a day using a class II portable device where the adaptive DBS strength was changed linearly with Beta power. The results showed that adaptive DBS is effective in controlling PD symptomatic motor disturbances.

We note that compared to clinical settings where patients are tied to the bed, using the portable device enabled more flexibility allowing the patient to perform normal everyday life activity. The offered freedom and the duration of the experiments are incomparable to implantable solutions; however, it serves as an important step towards that direction. Since the employed device [26] consists of commercial discrete component electronics that are not implantation grade, it might take several years before transitioning to an implantable solution assessing long-term effectiveness of the therapy.

1.8 Proposed work: Theta Phase-Specific Stimulation in Implantable Neuromodulation Devices

Similar to suppressing epilepsy episodes and controlling Parkinson's disease motor disturbances, DBS for memory enhancement could be more efficacious if we incorporate knowledge of the memory encoding or recall state to inform the stimulation decision process. Theta band (3-8 Hz) has been linked to various memory functions such as encoding, recall and navigation [14-15]. Some theories suggest that the ongoing Theta phase could be employed by the brain to facilitate memory recall in sequential order [16]. Moreover, it was shown that DBS enhances or inhibits memory when delivered at specific phases of the theta rhythm [2-4].

Figures 1.5-1.8 show sample spectrograms of theta band activity in recorded local field potential data during verbal memory experiments from intracranial depth electrodes located in the hippocampal region of the human brain. We observe the following: 1) these oscillations are present typically for a short duration 2) Multiple oscillations can coexist simultaneously (multimodality) in the Theta band and 3) The oscillations are non-stationary.

We would like to detect these short temporal events without any subject-specific parameters in an unsupervised manner; in other words, without a human in the loop. After successful Theta activity sensing, we would like to predict when the requested

Theta phase is going to occur next. The algorithm should always monitor Theta band, and when an activity is present, it wakes up the stimulation engine to generate a pulse that is synchronized with the requested Theta phase.

The dissertation presents the algorithm design, architecture design and optimization, chip realization, and the design of a class II portable phase-specific (ps) DBS device towards closed-loop ps-DBS stimulation in implantable neuromodulation devices (Figure 1.4).

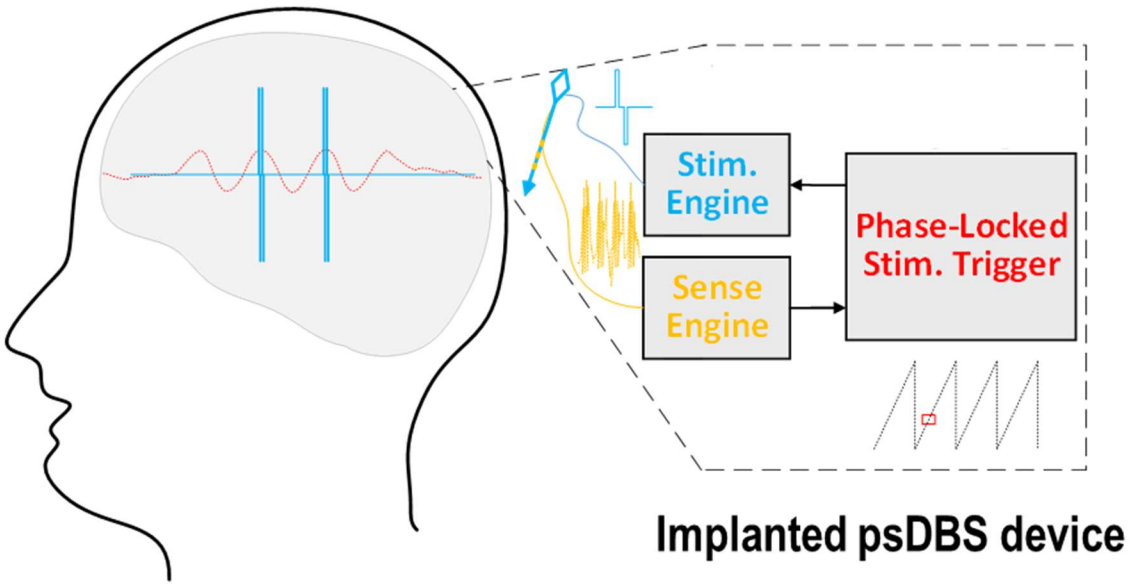

Figure 1.4: Phase-specific Stimulation in an implantable device.

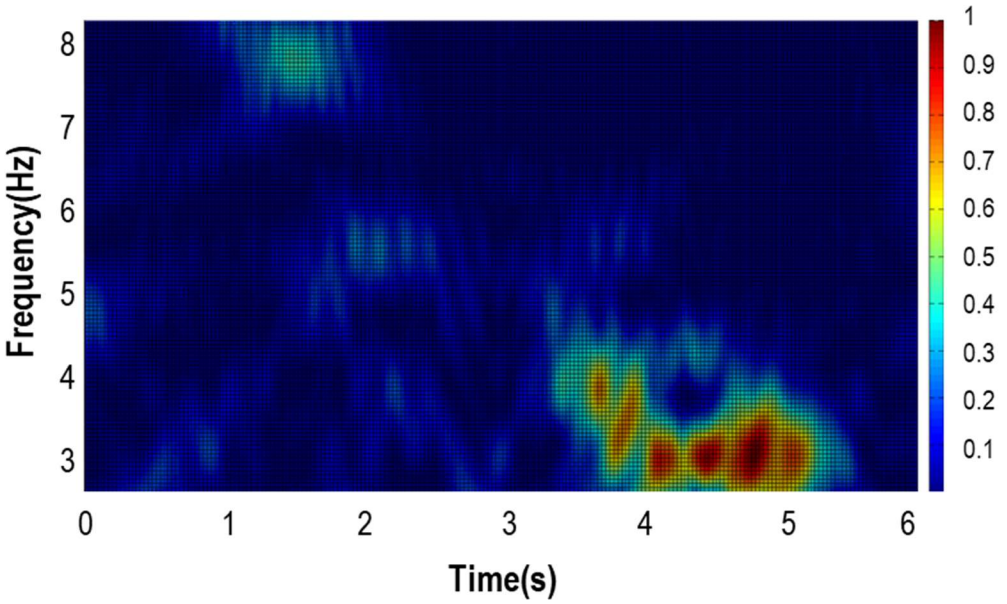

Figure 1.5: Sample spectrogram with normalized power spectral density.

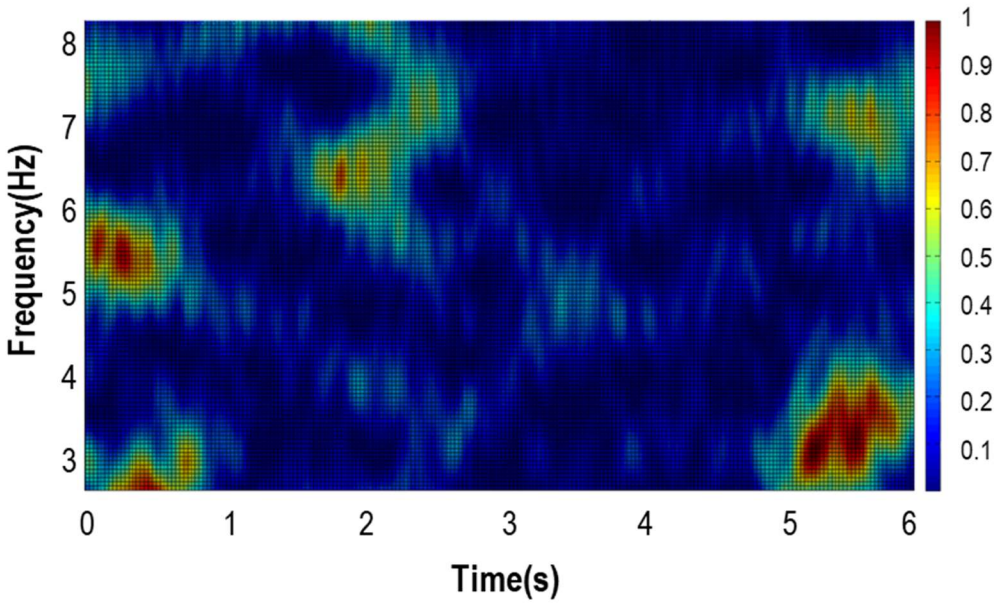

Figure 1.6: Sample spectrogram with normalized power spectral

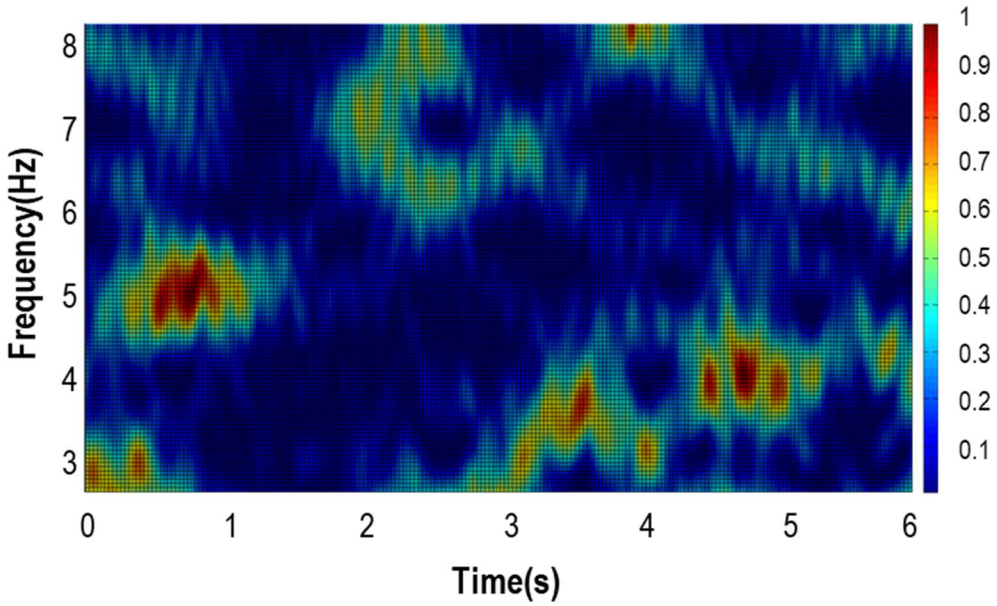

Figure 1.7: Sample spectrogram with normalized power spectral density.

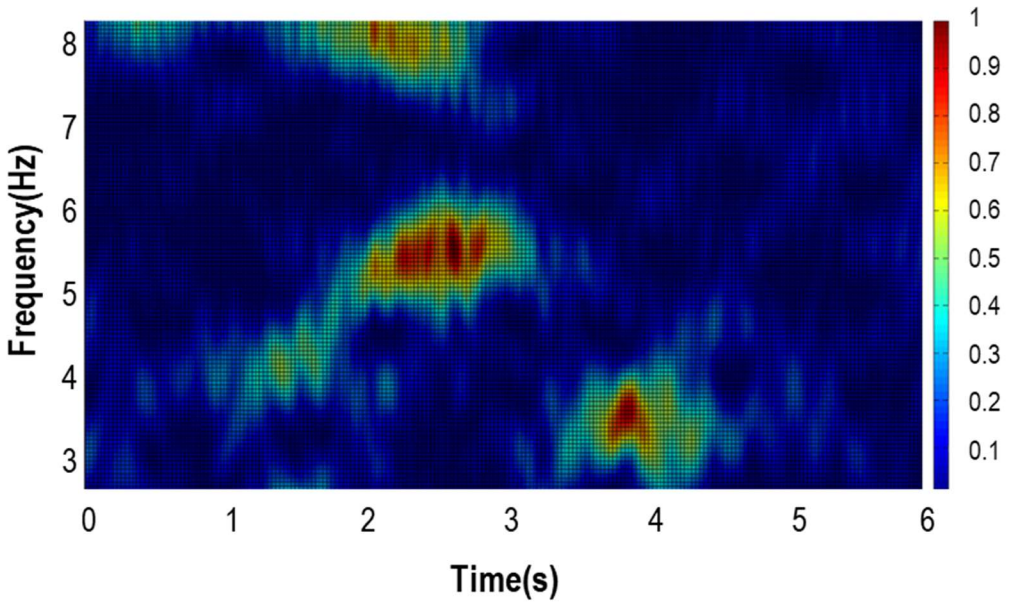

Figure 1.8: Sample spectrogram with normalized power spectral density.

1.9 Life of an Implantable Device

Having discussed the different brain stimulation systems, and motivated closed-loop ps-DBS in implantable neuromodulation devices, this section elaborates on the followed strategy to transition from theoretical evidence to practice throughout the developmental life of the proposed solution and how the different system classes come at play.

Early supporting evidence is typically found in laboratory research experiments that are performed on animals and humans using class I systems (Figure 1.9). As was observed in the case of epilepsy reduction, suggested therapy may only reach its maximum healing potential in the long term which requires implantation. Due to the previously discussed strict requirements on implantable devices, new hardware-efficient algorithms need to be designed and architected in ultra-low power integrated circuit implementation. Class IV systems additionally require algorithms to be automated or unsupervised for the loop to be fully closed on-board. As the implantable device undergoes the lengthy federal drug administration (FDA) approval process, an intermediate class III compact and portable device is developed in parallel to facilitate integrated circuit validation and algorithm tuning. After implantation, we may choose to unlock the algorithm when needed to carry on the laboratory and implant informed long term experiment that optimizes configuration parameters and reaches the maximum healing potential.

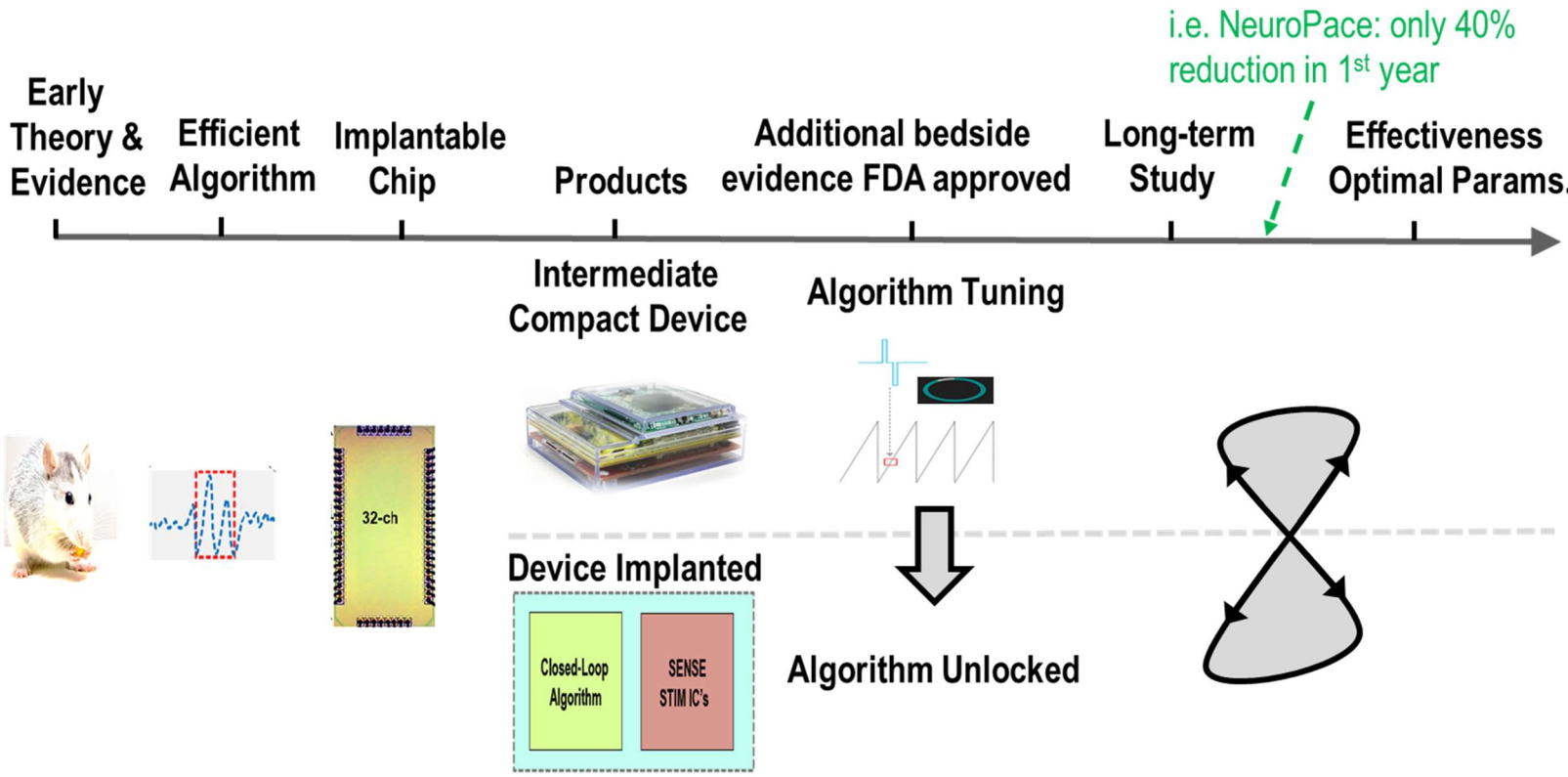

Figure 1.9: Life of an implantable device

1.10 Dissertation Outline

Chapter 2 reviews two existing methods to trigger a phase-specific stimulus in closed-loop. Next, the chapter presents the design of the unsupervised hardware-friendly algorithm to trigger phase-specific stimulation in implantable neuromodulation devices.

Chapter 3 presents the hardware design and the performed architectural optimizations to meet the implantable device area and power constraints. Specifically, at the block-level, details of the band-pass filter optimization are discussed. At the system level, the chapter discusses the design interleaving depth optimization that shares hardware resources for improved area and energy efficiency,

Chapter 4 presents details of the taped-out architecture in TSMC 40 nm low power technology. It also presents the in-isolation chip measurement results using a simulated real-time setup to verify chip functionally and measure the average power consumption

Chapter 5 presents the designed ps-DBS and stimulation protocol development platform. The handheld platform integrates the ps-DBS chip, analog sensing front-end, and stimulation engines in a compact and portal platform (Class II system). In preparation for clinical experiments, the chapter also presents details of the

conducted in-vitro measurement results of the proposed system. Finally, the chapter discusses design challenges encountered at the system-level.

Chapter 6 concludes the dissertation and presents our plans to test the platform in-vivo on human patients, in addition to future research directions.

2 | Algorithm Design

Closed-loop neural signal processing algorithms must be computationally inexpensive for a small hardware area and power footprint that meets the strict requirements of implantable neuromodulation devices. Moreover, it is desired that algorithms feature unsupervised or fully automated processing. Therefore, enabling compact all-in-one-device implantable solutions with no manual intervention beyond occasional parameters configuration.

The phase specific stimulation or locking (PL) algorithms predict the next occurrence of a desired theta phase. It is predicted rather than detected because of the inevitable preprocessing delays introduced by filtering, used to reject out-of-band neural oscillations. Theta phase extraction is another source of latency. To maximize the prediction accuracy, it is essential to account for and minimize algorithmic and the closed-loop system latencies. Not only the mean latency needs to be minimized but also the latency variance. The randomness in latency cannot be accounted for by the algorithm, therefore it adds to the uncertainty of phase prediction which degrades accuracy.

This chapter reviews two existing methods to trigger phase-specific stimulus in closed-loop. Next, the chapter presents the design of our unsupervised hardware-friendly algorithm to trigger ps-DBS in implantable neuromodulation devices.

2.1 Review of Existing Software Methods

Early Theta phase-locked (or phase-specific) stimulation experiments were fully supervised in the lab, and methods inaccuracies were overcome by repeating experiments to exclude missed trials. Later, efforts were made to automate the process and realize real-time PL in software. Here, two classes of methods are reviewed.

2.1.1 Method 1: Supervised

An interesting system was designed in [6] for presenting animals with a phase-specific visual stimulus in closed-loop. The system includes three networks of computers: 1) the data acquisition subsystem 2) the processing subsystem and 3) the visual stimulation subsystem.

The experiment consists of selecting a processing band of interest, manually setting a detection threshold, and finally inducing an oscillation. The presented visual stimulus is aligned to the requested phase. The software realization and network-distributed nature of the system resulted in a non-negligible latency variance. For example, the system (non-algorithmic) latency has a standard deviation of more than 20ms for a single channel processing.

Internally the system utilizes computationally expensive block filtering in the forward and backward direction to equalize the non-linear phase response. Due to the computational complexity and the supervised processing, the method is unsuitable for implantable devices.

2.1.2 Method 2: Semi-supervised

Another example is the work in [5] which designed a MATLAB simulated system that consists of a tracking filter, followed by future time-series prediction to estimate phase. The method follows a similar block filtering with non-linear phase equalization approach as in 2.1.1, in addition to requiring computationally very expensive autoregressive (AR) models that are used in the tracking filter and time series prediction modules. The method is semi-supervised as the AR model coefficients are optimized in patient-specific manner. Although oscillation tracking is suitable for non-stationary signals, it cannot handle multimodal oscillations. Moreover, since this is a MATLAB simulated system, it is unclear how practical aspects at the system level, such as the latency, might affect performance. Due to the inability to handle multimodal oscillation, and the very expensive high computational complexity, the algorithm is also unsuitable for implantation.

2.2 The Algorithm

While previous work involves supervised theta phase prediction and complex processing, our algorithm is based on an unsupervised divide-and-conquer approach, where we wait on sub-bands to sense Theta activity. When an activity is detected, relative to a running window that continuously estimates the average power baseline, we attempt to hit the target phase. By monitoring all the bands simultaneously, the algorithm can track multimodal oscillations, in addition to non-stationary signals as they traverse in time and frequency across all the sub-bands. This fully unsupervised and computationally inexpensive approach is suitable for implantation in neuromodulation devices.

Details of the algorithm are presented in Figure 2.1. Theta band (3-8 Hz) is divided into five 1-Hz sub-bands. The isolated oscillation is transformed to its analytical form, prior to phase extraction. Next, the phase is differentiated to obtain a frequency estimate. In parallel to phase extraction, the power of the signal is estimated over a running window and the mean power is calculated over multiple windows to establish a power level reference. Comparing the signal power against a running mean ensures unsupervised algorithm, that is insensitive to the baseline signal strength variations, seen across patients, different electrode contacts, or over time.

The algorithm takes the desired stimulation phase as input and makes the prediction of the real-time occurrence of that phase if the following decision criteria are met: 1) the equivalent-desired phase (EDP) is detected in any of the monitored bands, 2) the frequency estimation falls within the band, 3) the oscillation power over the running window exceeds a configured constant multiple of the running average power window.

There is a one-to-one relationship per sub-band between the EDP and the ongoing real-time phase. This relationship is calculated based on the center frequency of each sub-band and the processing delay, with the implicit assumption that the oscillation is sustained longer than the processing delay. The second decision criterion ensures no spectral leakage from adjacent sub-bands as to prevent impermissible violations of the one-to-one phase relationship. Moreover, only one stimulation decision is triggered if an activity is detected simultaneously in two adjacent bands. Finally, by comparing the signal power to the past running average, we can control the precision of the predictions around the target phase. This makes sense, since a stronger oscillation is more likely to sustain, leading to a more reliable phase prediction.

Beside unsupervised, it's also essential for algorithms to be hardware efficient to satisfy stringent power and area requirements of implantable devices. The employed block and system-level architecture optimization techniques are discussed in the next chapter

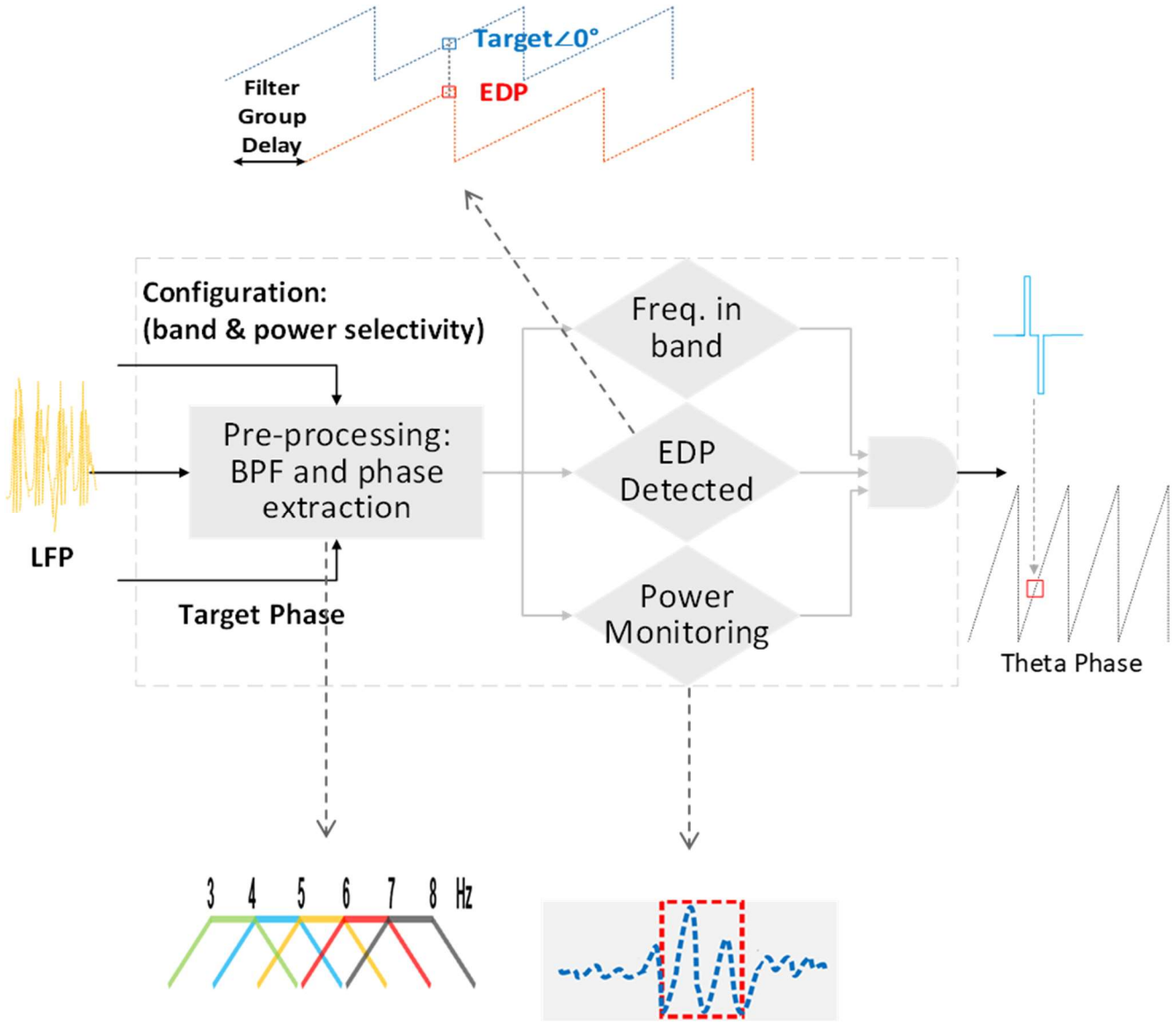

Figure 2.1: Algorithm flow chart. Digitized raw LFP from the analog front-end is preprocessed by filtering and phase extraction which is, next, fed to phase prediction.

3 | Architecture optimization and chip design

The chapter discusses the hardware design of the algorithm, in addition to the employed block and system-level architectural optimization techniques to arrive at an implant-scale power and size chip for neuromodulation devices.

3.1 Algorithm Hardware Realization and Block-Level Optimization

The implemented 4-channel interleaved architecture is shown in Figure 3.1. Input raw data, coming from the analog front end at 6 kHz, is decimated to 100 Hz for efficient subsequent processing.

A major hardware bottleneck is the configurable band-pass filter. Prior methods used block processing of the incoming data and utilized filtering in both forward and backward direction to equalize the non-linear phase response. To avoid performing the computationally expensive filtering twice, we used the more hardware efficient sample processing and employed different techniques for a linear phase response .IIR filters are sharp and relatively cheap but cannot be used because of their non-linear phase response, which would destroy the phase information that is critical for the algorithm operation .FIR filters have a linear phase response (LPR) but require a much larger number of taps. To reduce the number of taps, frequency masking is employed [18]. Figures 3.2-3 shows our two-stage realization of the masking technique, where a configurable low-order FIR filter is used as the first stage and a

fixed IIR filter is used as the second stage. We start by relaxing the filter requirements by a factor of 4, which reduces the number of taps by the same factor (Figure 3.3b). To meet the original response (Figure 3.3a), we transform the response as shown in Figure 3.3c. Since the frequency response of a discrete time signal is periodic, the shrinking of the frequency axis introduces extra images that need to be attenuated. An IIR filter performs this image attenuation (Figure 3.3d). The trick is, working as the masking stage, the IIR filter needs only to eliminate the extra images and can be designed to a have an approximately LPR over the band of interest. Using this approach, the number of the FIR filter registers remains the same, while a 4x reduction in the number of taps is achieved. Only the relaxed first stage needs to be configurable, which results in area and power savings. Finally, the symmetric FIR filter taps are folded reducing the number of taps by 50%.

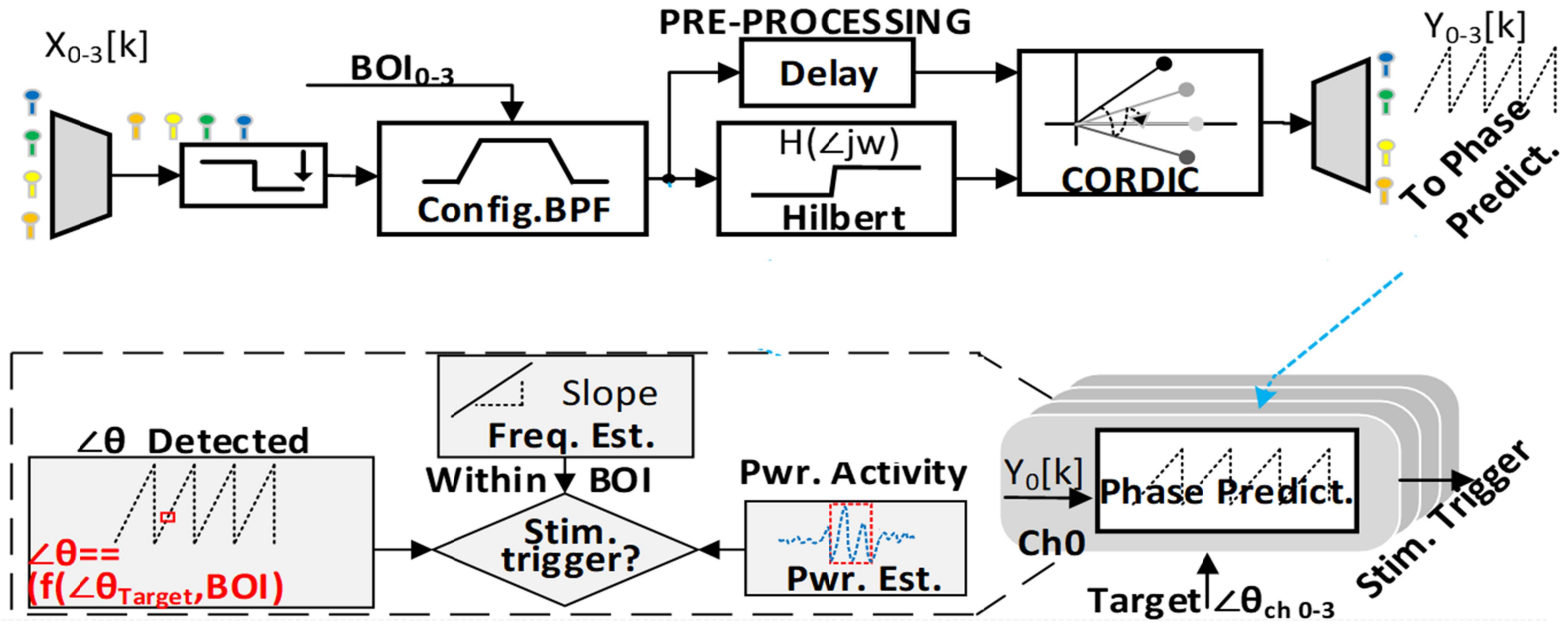

Figure 3.1: Block-level architecture of a 4-channel interleaved core.

Next, a FIR filter is used to approximate the Hilbert transform, followed by a CORDIC [19] engine for efficient phase extraction (Figure 3.1). Since CORDIC rotations only depend on the current sample, it is clocked at a faster rate to minimize the processing latency. Frequency is obtained by calculating the difference between phase samples, averaging to reduce noise, then multiplying by the sampling frequency. For power estimation, we observe that the band is narrow and use the maximum amplitude in half a period as an effective power indicator instead of the expensive squaring operation

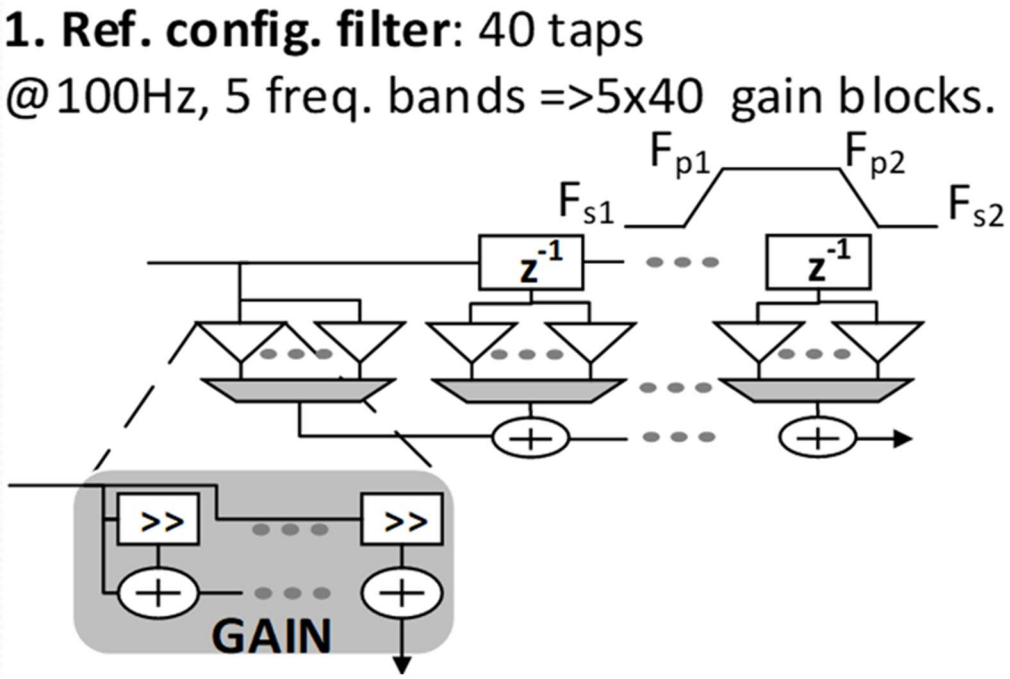

Figure 3.2: Reference FIR filter design; the multiplexers select the desired Theta band. Constant multiplication is implemented in its canonical form for hardware efficiency.

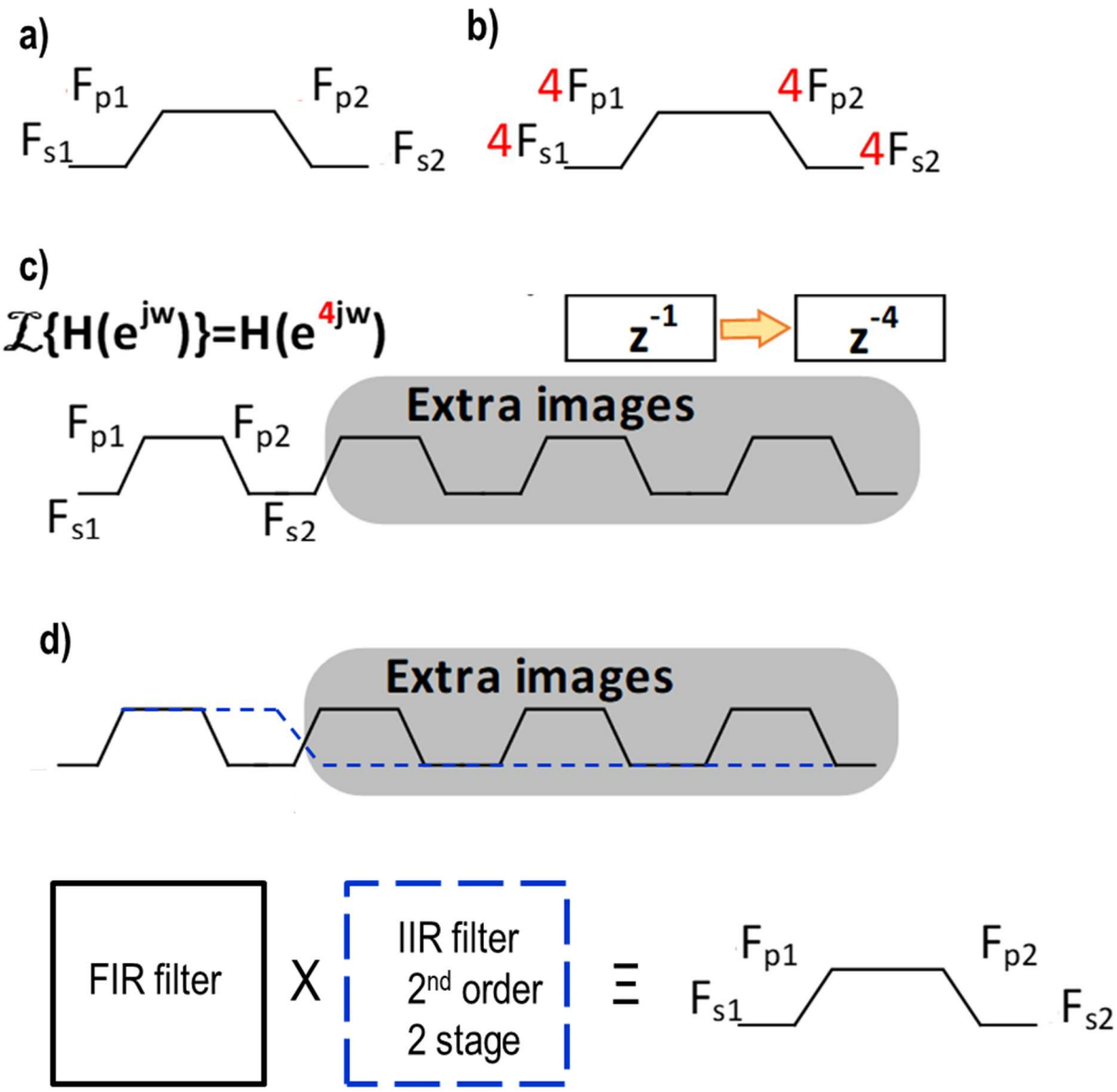

Figure 3.3: The configurable bandpass filter number of taps optimization a) the desired filter response b) relaxing the filter reduces the number of taps by 4 c-d) Filter transformation to arrive at the desired response. Folding the symmetric FIR filter reduces the number of taps by an additional 2x (not shown)

3.2 System-Level Optimization

Finally, at the chip-level we applied clock gating and multi-channel interleaving optimization [20, 21]. Substantial energy and area savings can be achieved through time-sharing of hardware resources. Deeply interleaved designs are unattractive as the individual channels can't be power-gated. As shown in Figure 3.4, energy is minimized at interleaving depth of 4-8 channels. Depth 4 was chosen to provide a balance between energy, area savings, and modularity for system integration.

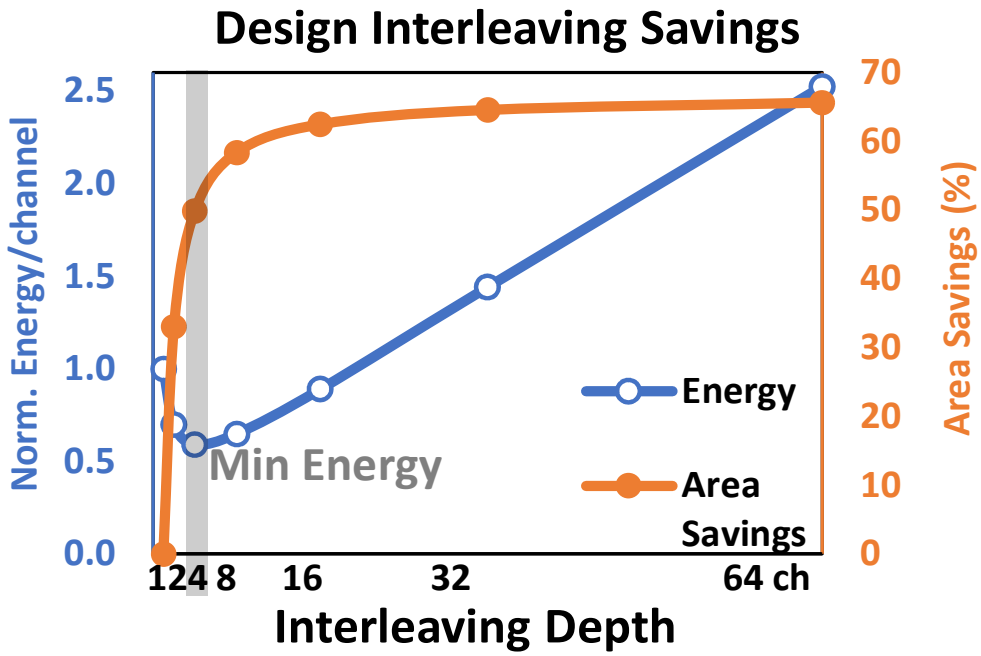

Figure 3.4: Energy (left) and area savings (right) vs. interleaving depth. Depth of 4 offers a reasonable tradeoff between savings and design modularity.

4 | Chip Measurements

The designed architecture was fabricated in TSMC 40 nm low power technology. This chapter presents the in-isolation chip measurement results using a simulated real-time setup to verify chip functionally and measure the average power consumption.

4.1 Simulated Real-time Test Setup

The chip was evaluated on local-field-potential (LFP) data recorded from intracranial depth electrodes located in hippocampal region of the human brain during memory tasks. Hippocampus is chosen due to its importance in memory function and for consistency with studies in [2-4]. To stimulate online data acquisition, we feed the quantized data in real-time at 6kHz. After the stimulation-trigger time stamps are collected online (Figure 4.1-2), phase prediction triggering performance is evaluated offline.

The offline analysis consists of the following steps: 1) sharply filter theta for each band, 2) extract the phase, 3) remove all the processing delays by shifting the phase by the amount of processing delay, thus, we can tell at any point in time the true phase of theta oscillation, 4) output true phase information based on stimulation time stamps.

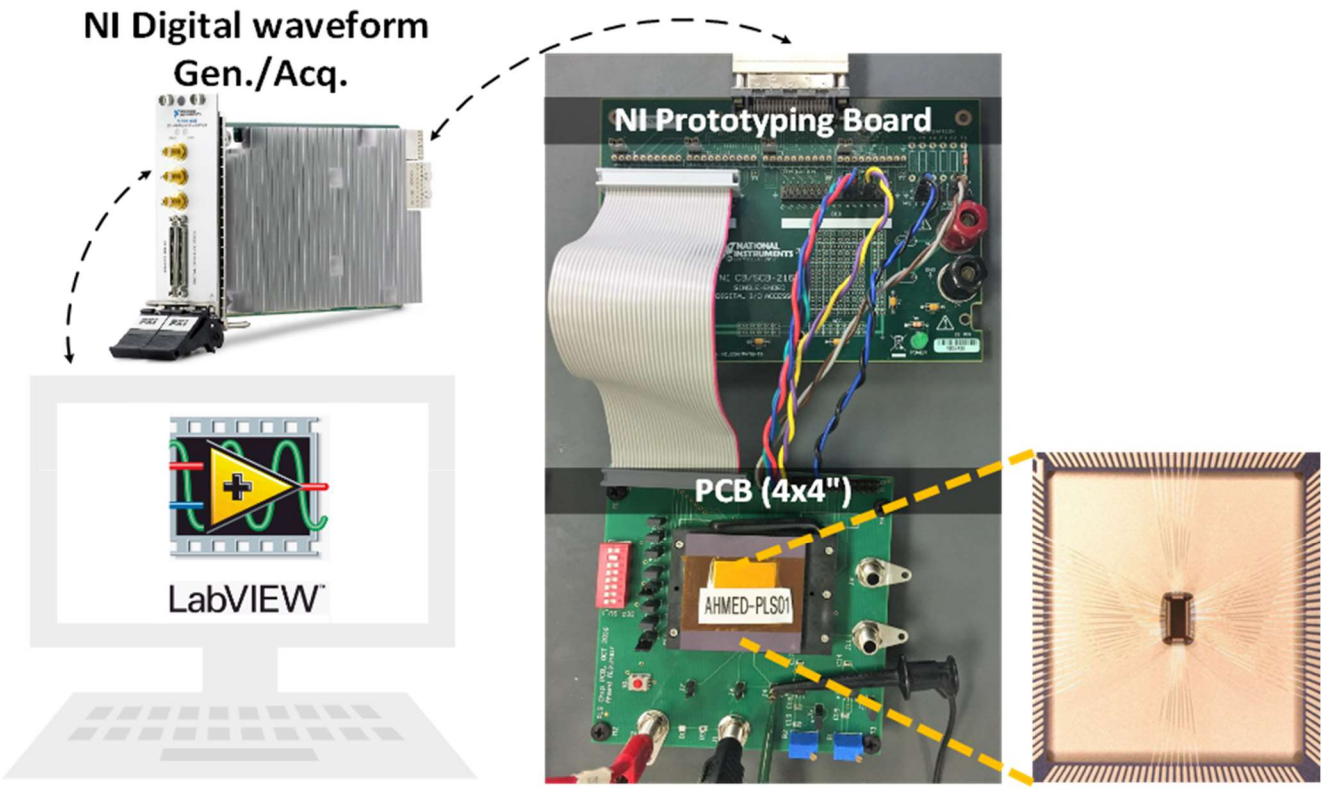

Figure 4.1: Use of NI PXIe-6555 for real-time digital data generation and acquisition (left). NI prototyping board and the designed printed circuit board hosting the packaged dies (right).

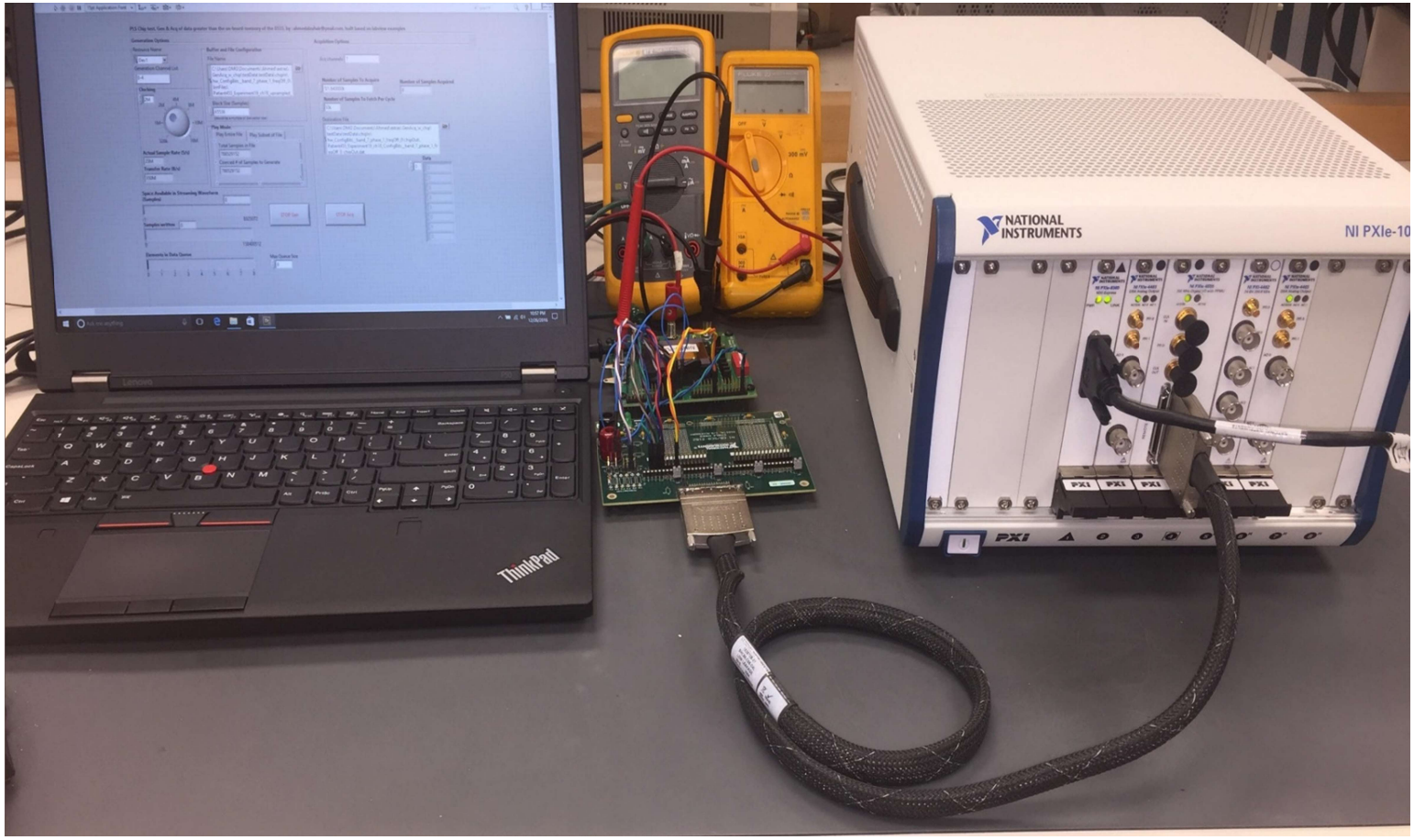

Figure 4.2: Photo of the Simulated Real-time test setup. The designed Labview GUI is used to select the desired chip configuration, the input data, and output data logging.

4.2 Performance

Performance of five patient data sets is shown in Figure 4.3. The three sections of each bar (Figure 4.3a) represent the number of degrees away from the target phase, 25%, 50% or 75% of our predictions have fallen. Figure 4.3b shows that we maintain a similar performance with different targets. Finally, we can control the variance of the predictions around the target phase by using different power configurations relative to the moving power average (Figure 4.3c).

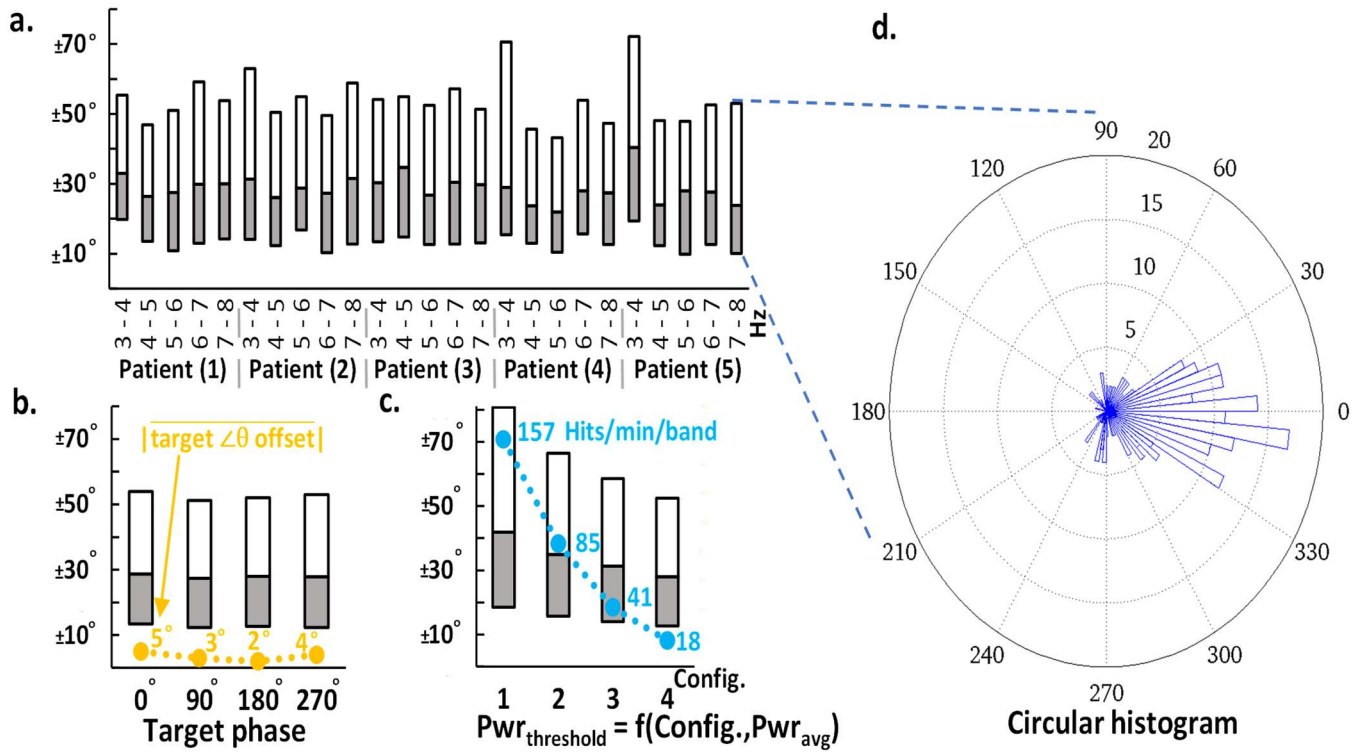

Figure 4.3: Measured Performance: a) Modified boxplot for target ∠0 (peak) (e.g. in highlighted bar, 25%, 50%, and 75% of the predictions are within ±10,˚ ±24,˚ and ±53 ˚of the target ∠0, respectively). b) Consistency in targeting different phases. c) Controlling variance by using different levels relative to Pwr_{avg} (b and c are the mean of all patients and bands). d) Circular histogram of the highlighted bar (dashed circles represent the bin count).

Comparisons with prior work are presented in Table 3.1. The circular variance takes values in the range of [0,1], with lower values indicating a tighter data spread [22]. Both [5-6] use block-based IIR filtering, in both directions to equalize the phase response. The approach truncates the input signal. While long signal padding might help, it is computationally expensive to pass each frame twice through the filter.

Table 4.1: Comparison with prior work.

Ref.	Method 1 [6]	Method 2 [5]	This Work
Signal	LFP	iEEG	LFP
Band	[0,40] Hz	Theta	Theta
Platform	Network of 3 computer subsystems	MATLAB (Simulated)	Chip
Unsupervised	No	No	Yes
Implantable	No	No	Yes
Mean offset	9°	12.2°	3.5°
Circular σ^2	NA	0.58	0.31
70th Percentile	$\pm 90^{\circ}$	NA	$\pm 46^{\circ}$

4.3 Chip Measurements

The chip (Figure 4.4-5), implemented in a 40nm LP TSMC technology, occupies an area of 1.2 mm^2, leaks 3.6 μW at 0.75V, and has a total power consumption of 6.9 μW. It features a programmable target phase over [0, 2π). It can also be configured to monitor different theta sub-bands simultaneously from single or multiple electrodes up to 32 channels. Monitoring different theta sub-bands simultaneously is particularly useful when prior knowledge of the activity patient-dependent the ta frequency is unavailable.

Table 4.2: Summary of chip specifications.

Technology	TSMC 40nm LP
Number of Channels	32
Power	216 nW/channel
Area	1.1 mm^2
Supervised	No
Circular Variance	0.3

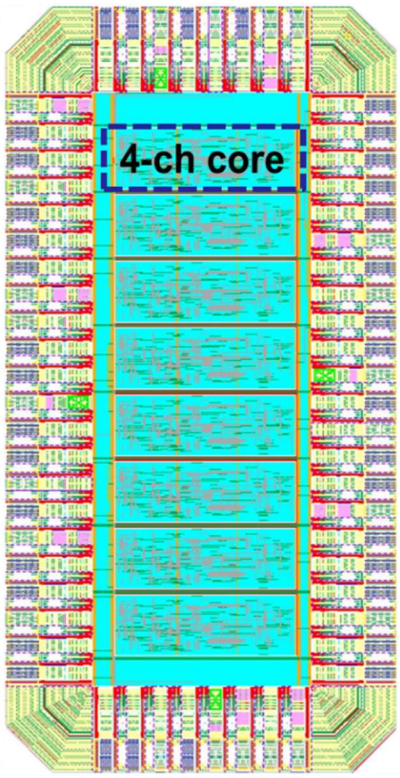

Figure 4.4: Layout snapshot of the chip.

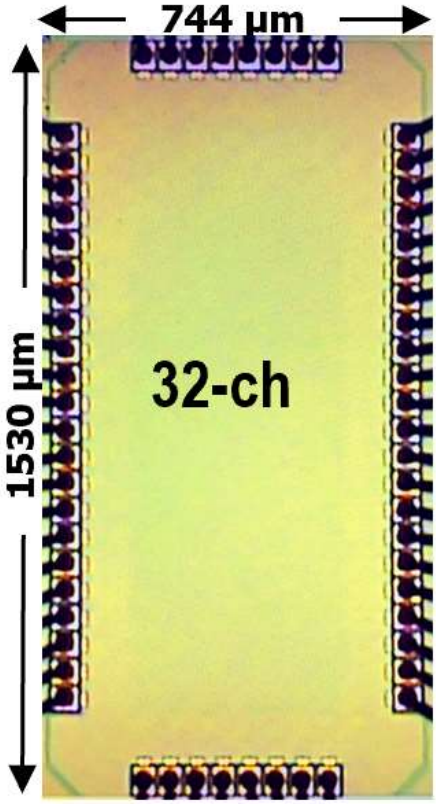

Figure 4.5: Die photo.

5 | System-Level Design

The phase-specific stimulation chip was integrated with an AFE and the electrical stimulation engines in a compact hand-held platform (class II brain stimulation system). This chapter discusses the platform, its graphical user interface, and finally presents the in-vitro measurements results that has been conducted in preparation for clinical experiments.

5.1 Motivation

The stimulation protocol development (SPD) platform, depicted in Figure 5.1, facilitates clinical studies and accelerated algorithm, and integrated circuit verification towards the implantable system. It also allows rapid algorithm tuning to experiment with the various configurable platform and algorithm parameters. After designing the desired phase-specific stimulation parameters on the hand-held SPD platform, the updated protocol can be downloaded and unlocked in the implanted counterpart.

Compared to existing commercial fridge-size systems, the SPD platform's compact form-factor not only allows more convenient non-bulky bed-side setups but enables more realistic experiments where patients could be moving around. The latter is potentially crucial for phase-specific stimulation experiments of Theta band, which has been extensively linked to navigation in animal studies in the neuroscience literature [14].

Moreover, the SDP platform provides scientists and clinicals the freedom in designing new algorithms or higher-level protocols that may employ the readily available phase information. The new algorithms and protocols can be integrated with the closed-loop system in software, as well as hardware in the platform's field programmable gate array (FPGA).

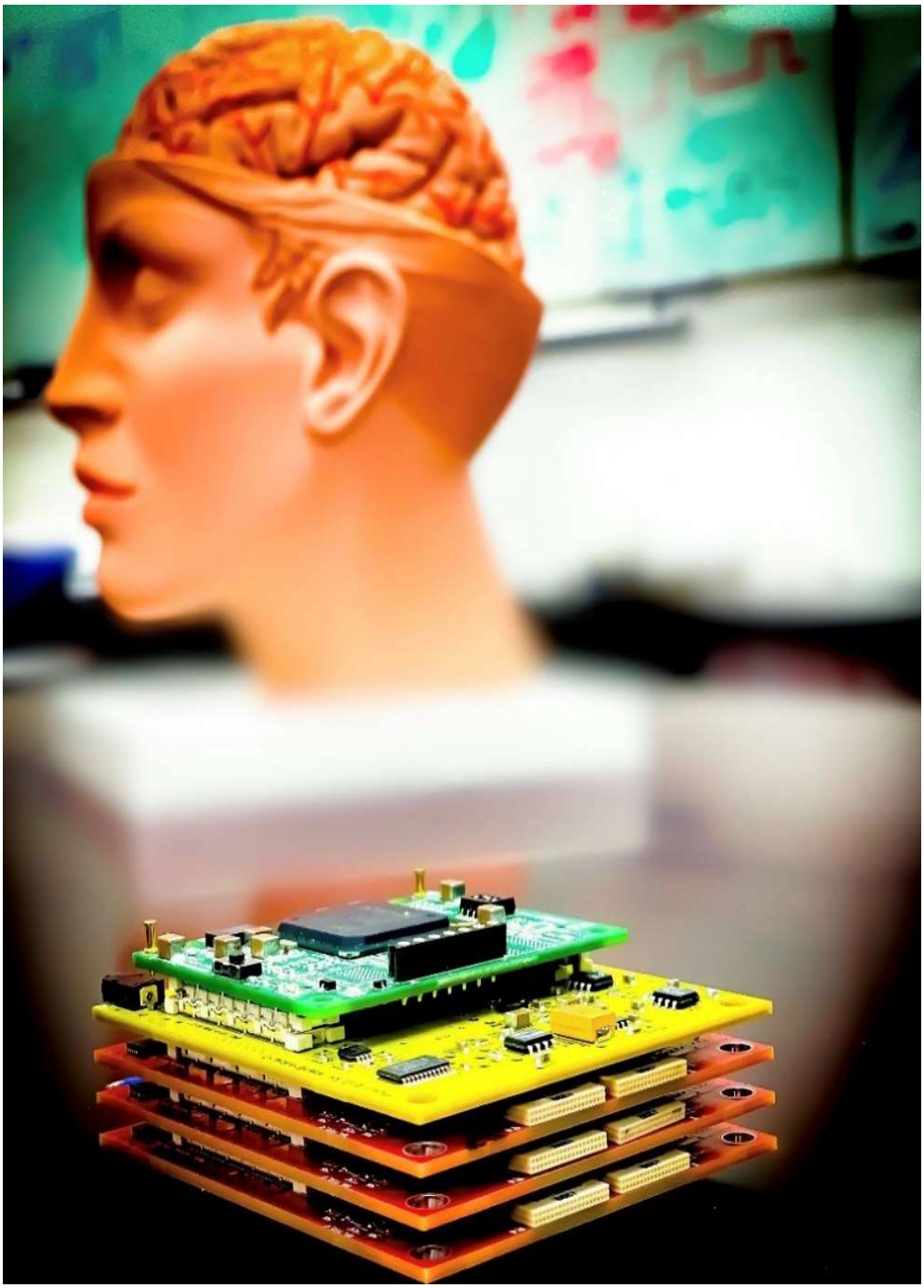

Figure 5.1: The hand-held stimulation protocol development (SPD) platform.

5.2 Platform Overview

The SPD platform (Figure 5.2) aims to provide clinicals a complete set of flexible and configurable tools for stimulation protocol design and application. The modular design readily supports rapid channel count expansion by vertically stacking the printed circuit boards that host the integrated circuits.

The platform offers real-time recording and configurable stimulation capability that can be delivered synchronously in closed loop to a desired Theta phase. For experimentation and the deployment of new real-time closed-loop algorithms -- that may incorporate the phase-specific stimulation algorithm -- the platform offers two options:1) software implementation 2) Hardware accelerated realization on the field programmable gate array (FPGA)

The system features a graphical user interface for clinicians to design the closed-loop stimulation protocol parameters, such as the targeted phase and the stimulation intensity for Theta-synchronized stimulation delivery. Therefore, facilitating a wide range of experiments that can, hopefully, bring us a step closer to restoring and enhancing memory.

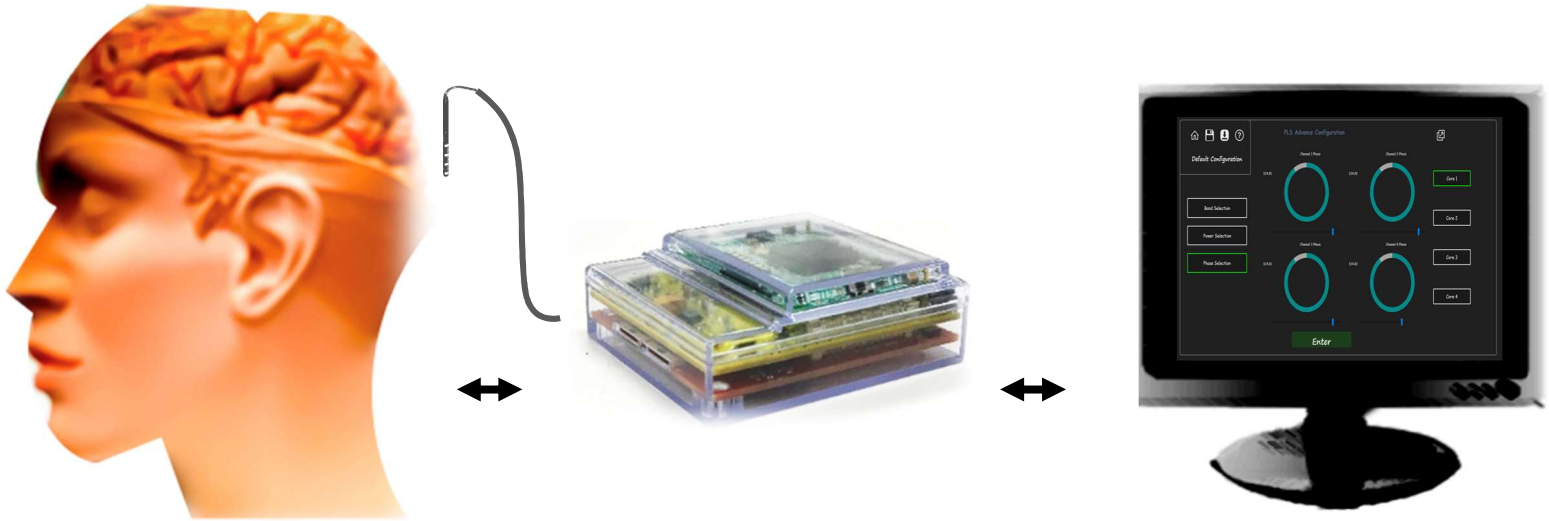

Figure 5.2: Platform Overview.

5.3 Main Specifications

At the analog front-end interfacing with the neural probes, the 64-channel neural sensing integrated circuit offers a wide dynamical range of 80 dB [23], and the 8-engine stimulation integrated circuit features a programable electrical current intensity and a configurable stimulation waveform of any shape [24]. The number of sensing and stimulation channels can be quadrupled by vertically stacking the printed circuit board layers.

On the digital signal processing side, any of the 256 recording channels can be multiplexed to the 32-channel phase-specific stimulation integrate circuit [25] for ps-stimulation on any electrode site. Refer to Table 5.1 for a summary of the main platform specifications.

Table 5.1: Main functional properties of the platform.

Number of Electrodes	4 (layers) x 64 = 256
Sensing Sampling Frequency	6 kHz
Sensing Dynamical Range	80 dB
Max. Stimulation Current	5.1 mA (resolution 20 μA)
Number of ps-stim Channels	32
ps-stim Phase Range	[0, 2π)
ps-stim Frequency Range (Hz)	[3,8]

Physically, the platform consists of three main groups of layers (see Figure 5.3 and Table 5.2): 1) Field Programable Gate Array (FPGA) layer (green) which is responsible of the integrated circuit interfacing and the data communication with a PC; The FPGA also features free resources, as summarized in Table 5.3, that could potentially host algorithms requiring hardware acceleration 2) Analog layers (red) host the analog front-end and stimulation engine integrated circuits (up to four layers can be stacked) 3) The DSP layer (yellow) hosts the phase-specific stimulation integrated circuit (Figure 5.4), USB communication module, and the voltage regulation modules.

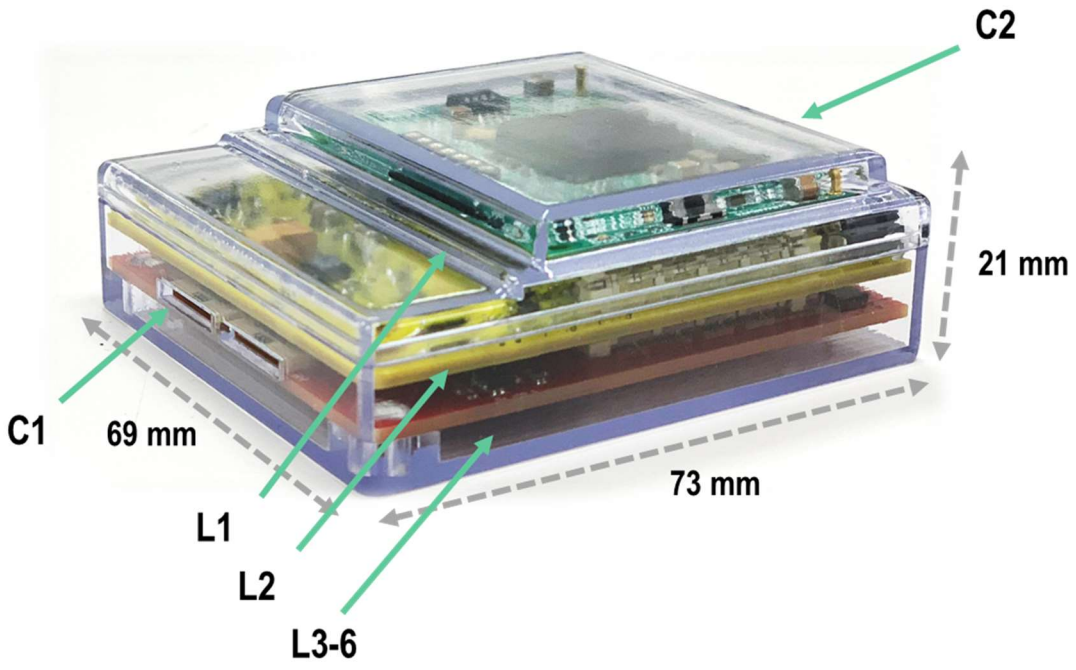

Figure 5.3: Platform layers and connectors.

Table 5.2: Platforms layers and component key.

L1	FPGA layer
L2	DSP and communication layer
L3-6	Analog layers (up to 4 stacked layers)
C1	64-channel omnetics connectors to neural probes
C2	USB mini port and power socket for the external battery option
L x W x H (mm)	69 x 73 x 21

Table 5.3: Utilization summary of Xilinx FPGA resources. Future optimized firmware updates are expected to further lower LUT resource utilization.

Resource	**Used**	**Available**	**Utilization**
Number of registers slices	5k	184k	2%
Number of DSP slices	0	180	0%
Number of LUT slices	47k	92k	51%

The platform supports two power delivery options: 1) using the USB power/data 2) supplying power externally using 6 Volts batteries. The latter option is included to facilitate conducting longer experiments, and to support our future plans of adding wireless data transmission to the portable platform.

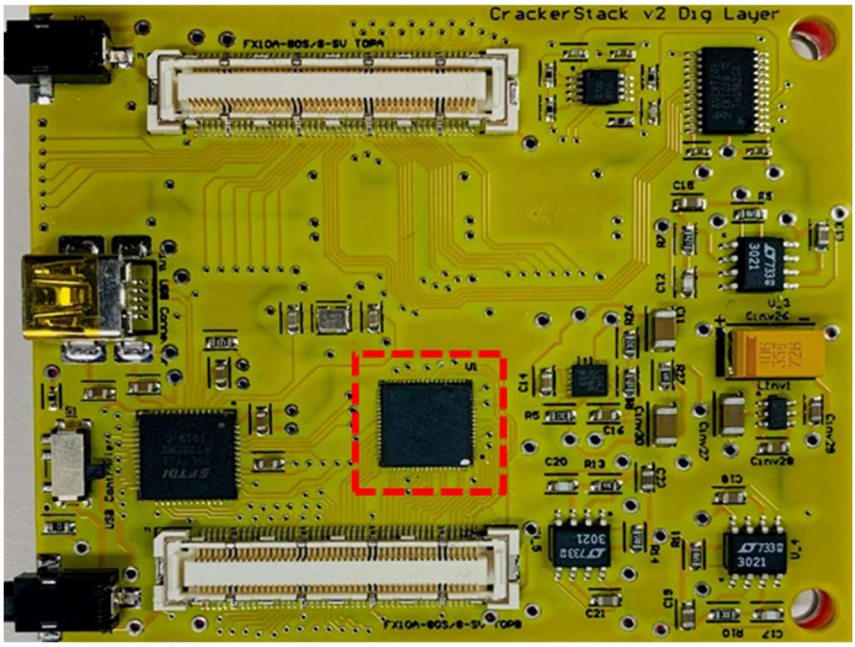

Figure 5.4: The DSP printed circuit board layer hosting the phase-specific stimulation, with the chip's QFN package highlighted.

5.4 Platform Block-Level Connectivity

Figure 5.5 shows the connectivity diagram of the different functional blocks in the ps-stim closed-loop system. In this beta firmware version - for compatibility with the open-loop stimulation commands that originate from software, and safety consideration that are discussed in section 5.8 - the closed-loop phase-specific stimulation protocol includes software in the loop. i.e. every time the ps-stim IC sends a trigger signal, it is only forwarded to the stimulation engine if the USB cable is connected and software flag is set by the operating clinician.

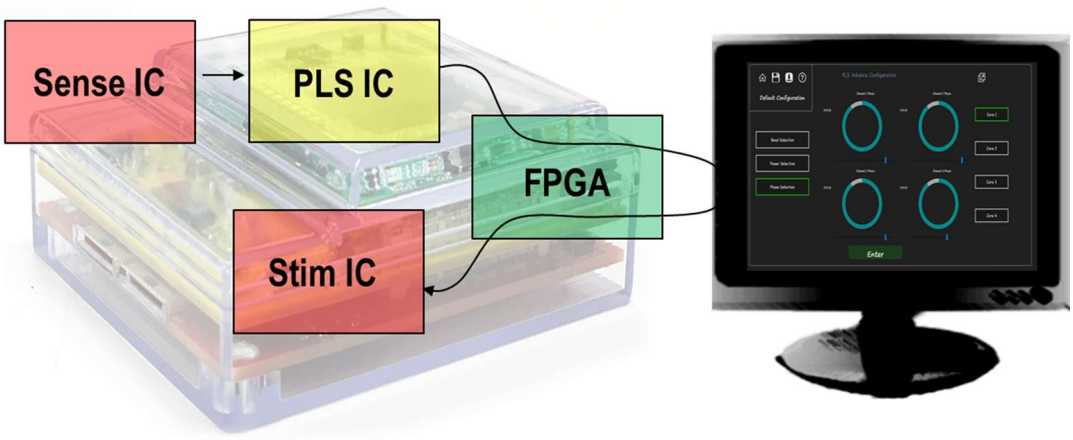

Figure 5.5: Block-level connectivity diagram of the ps-stim closed-loop system

5.5 Graphical User Interface

To ease stimulation protocol design and clinical experiments, the platform features a highly configurable GUI that is responsible of controlling the operation of the various chips as well as the real-time data logging. For example, the ps-stim engines configuration parameters are set as shown in figure 5.6 (also see Table 5.4 for a summary of the configurable parameters). The sensing and stimulation engines are configured similarly in dedicated configuration windows. After the platform is configured, real-time recording and the optional ps-stim may be enabled in the main GUI window (Figure 5.7).

Table 5.4: Configurable ps-stim parameters.

Target phase	The stimulation pulse is delivered at a desired phase in the range [0, 2π)
Power threshold	Relative to a running mean; controls sensitivity of the algorithm to the signal power variations
Band of interest	Could be a single band or multiple bands that are simultaneously monitored
Stimulation Waveform	Shape and periodicity of the pulse to be delivered
Sense/Stim Sites	Stim can be delivered on the same sensing site or to a different brain region for phase synchrony at the network scale

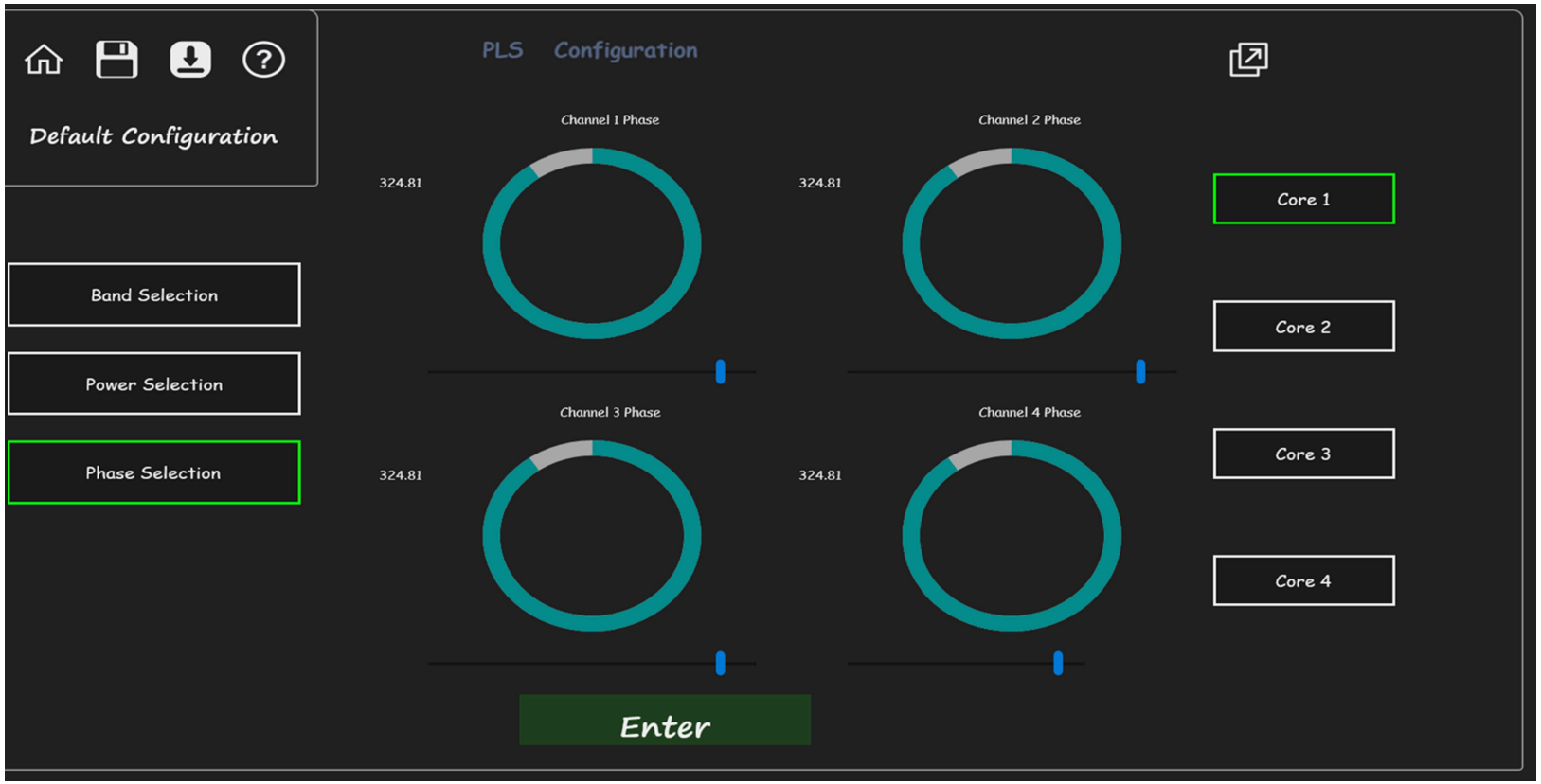

Figure 5.6: GUI window for ps-stim configuration

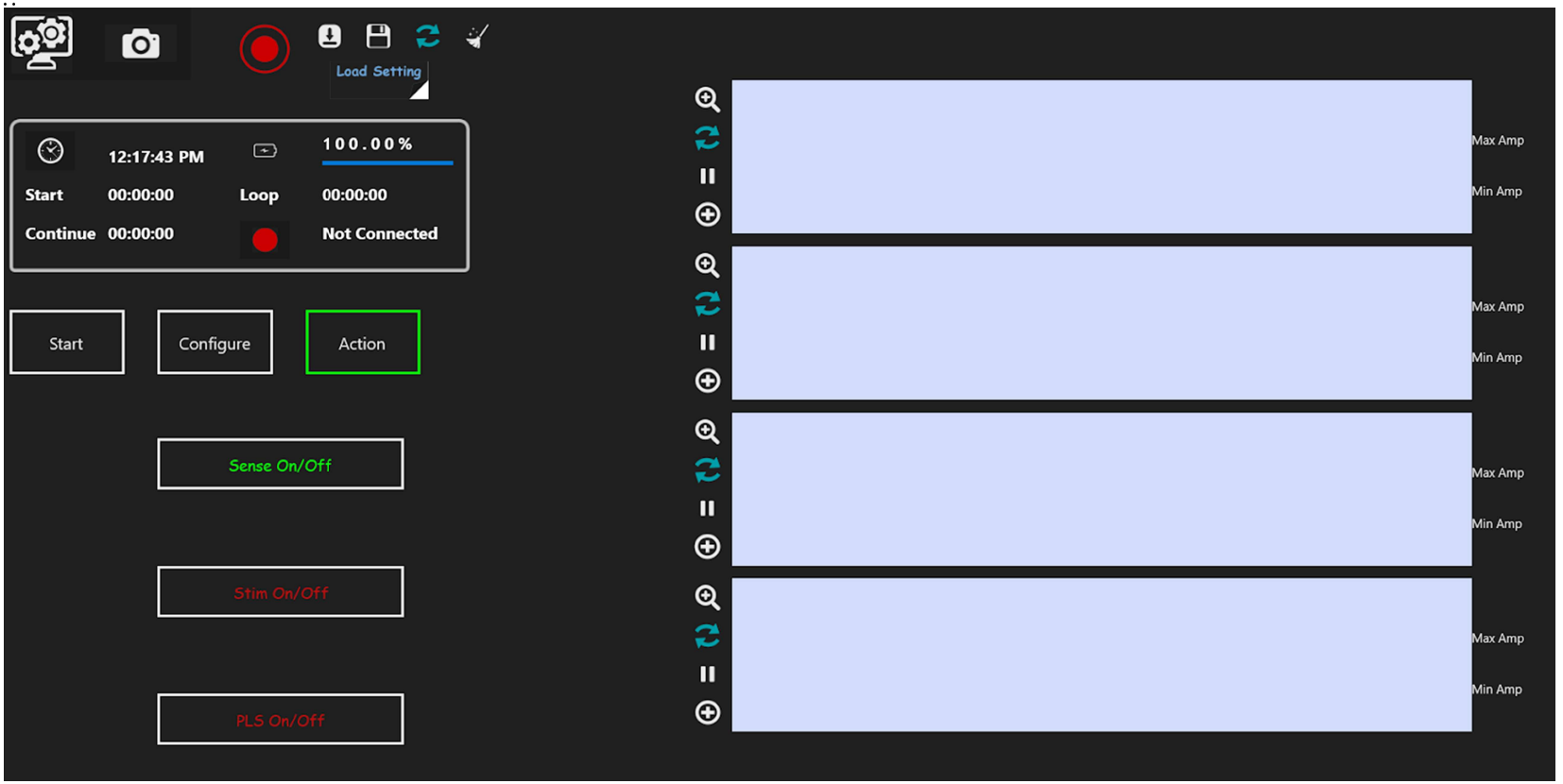

Figure 5.7: Main GUI window to start the experiment and to enable the ps-stim after the configuration paramters are set.

5.6 In-Vitro Measurements Setup

5.6.1 Input Data

To conduct the in-vitro experiment as close as possible to real experiments, we used previously recorded human local filed potential (LFP) signal. The neural signal has been recorded using depth electrodes in the hippocampal region of human patients during verbal memory experiments. The digitized signal is converted back to the analog domain before it is injected in the saline solution.

5.6.2 Electrodes and Becker setup

Electrodes setup in the saline solution is shown in Figure 5.8. We used two tablets of SIGMA P4417-50TAB, in 400 mL deionized water for concentrations: 0.01 M

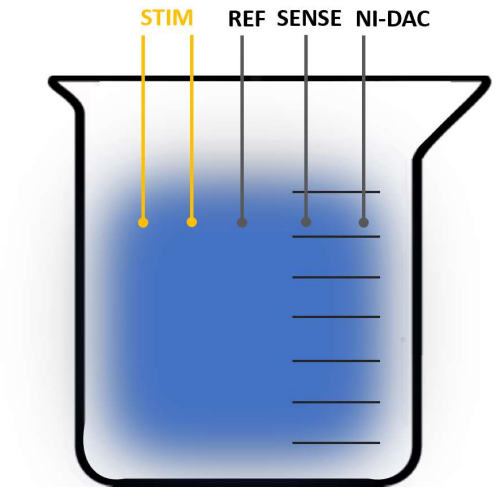

Figure 5.8: Electrode setup in the Saline solution.

phosphate buffer, 0.0027 M potassium chloride and 0.137 M sodium chloride, and pH of 7.4. The neural LFP signal is injected into the saline solution by the electrode connected to the National Instruments digital to analog converter (NI-DAC). Electrical stimulation is applied through electrodes adjacent to the sensing sites.

5.6.3 The In-Vitro Real-time Experiment

Image of the running real-time closed-loop ps-stim system is shown in Figure 5.9. The GUI was configured to deliver one (non-periodic) phase-specific stimulation pulse at the onset of PLS chip trigger and aligned with the sensed Theta activity peak (0 degrees). The NI PXIe-4463 digital to analog converter injects the neural LFP in the Saline solution, while the platform's AFE continuously samples the electrical potential in the solution at 6 kHz. The system wakes up the stimulation engine upon the detection of an opportunity to deliver ps-stim aligned with the requested phase. The software saves a local copy of the recorded data that is used for analysis of the system's performance.

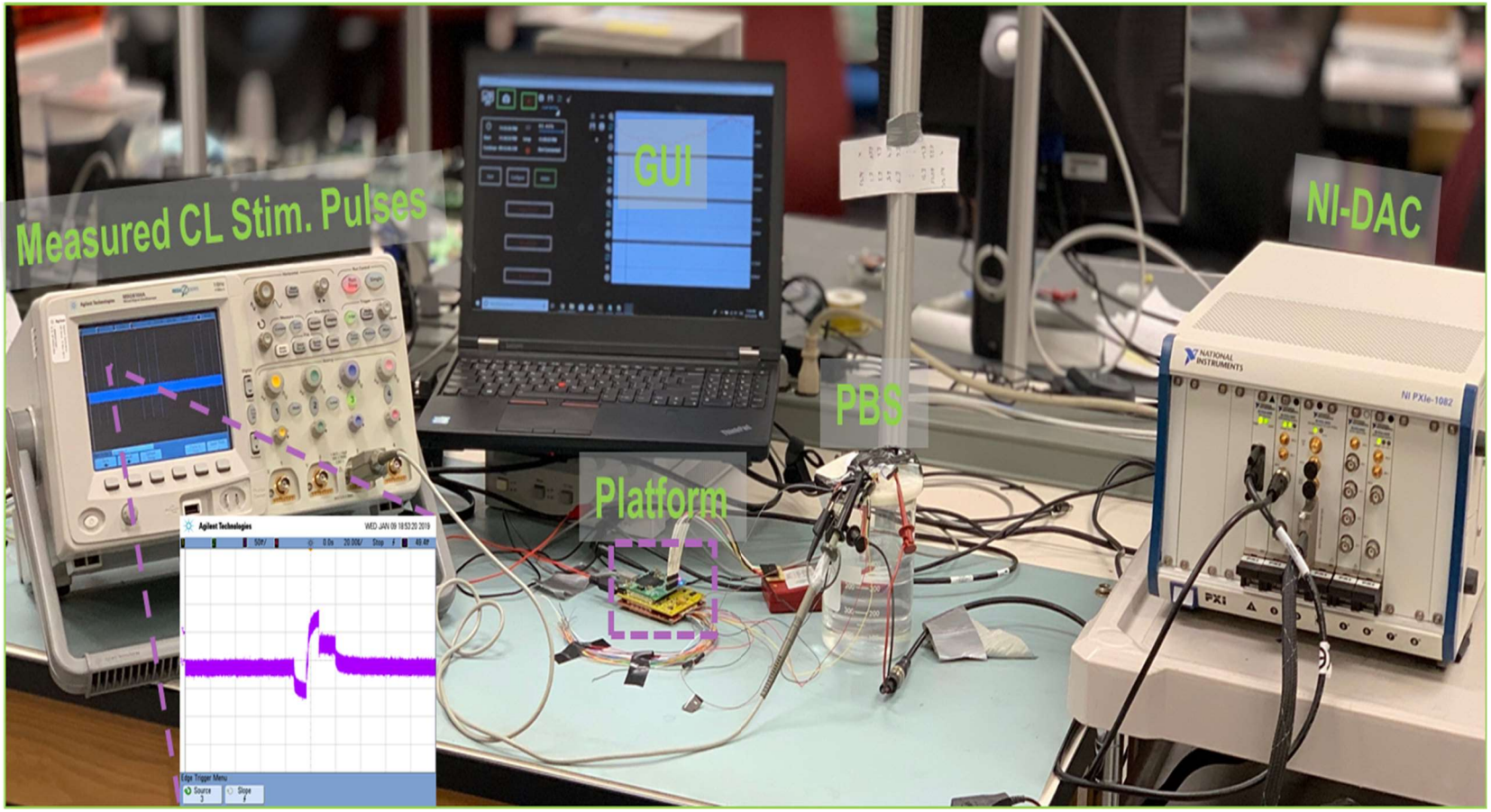

Figure 5.9: In-Vitro Measurement Setup.

5.7 In-Vitro Measurements Results

The experiment's recorded data is used for post-processing to assess the closed-loop ps-stim platform's performance. Figure 5.10 shows a sample recorded LFP trace with the stimulation pulse delivered in closed loop to the ongoing theta activity peak, and the circular phase histogram of the 400 delivered stimulation pulses throughout the experiment. Overall, measurements results show a circular variance of 0.3 in the direction of the requested phase. Figures 5.11-14 show the LFP sample spectrograms, that were presented in the introduction chapter, and the filter bank outputs overlaid with the timestamps of the in-vitro-measured ps-stim pulses.

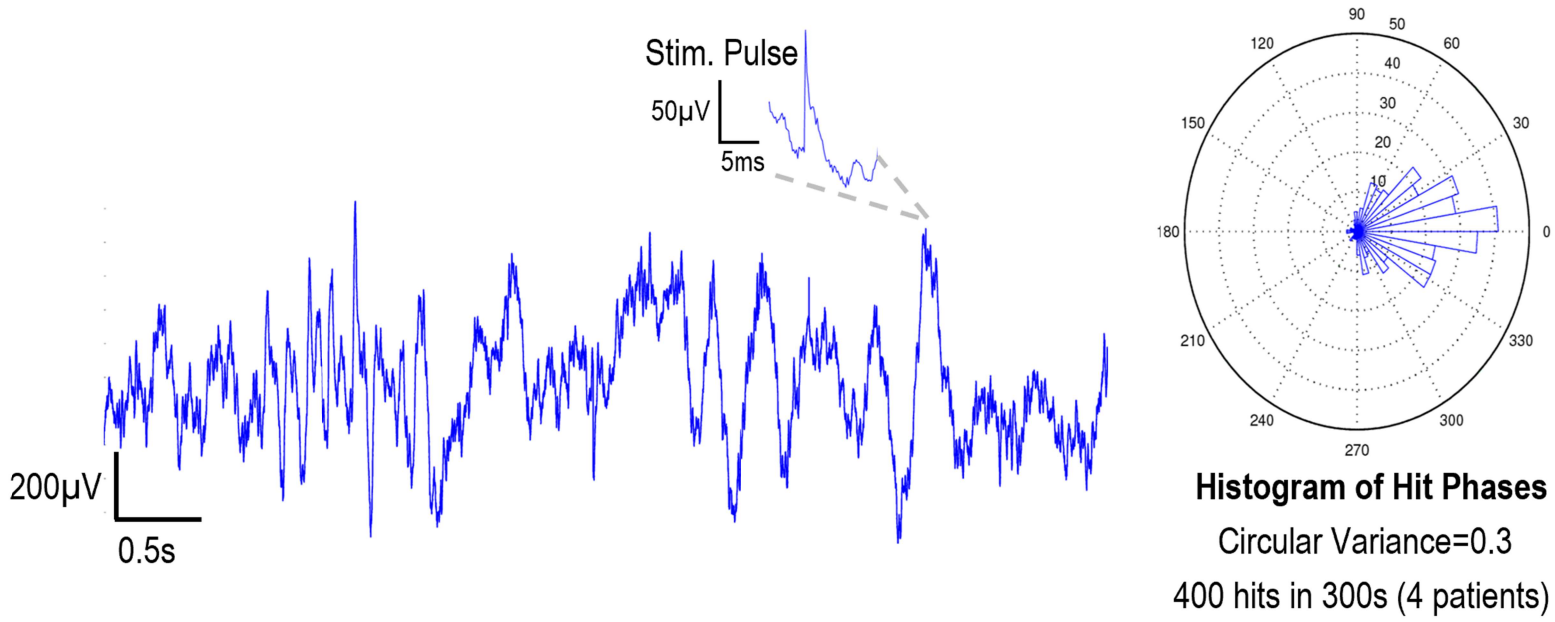

Figure 5.10: Raw LFP trace with stimulation applied in closed loop (left). Rose plot of the hit phases during the experiment.

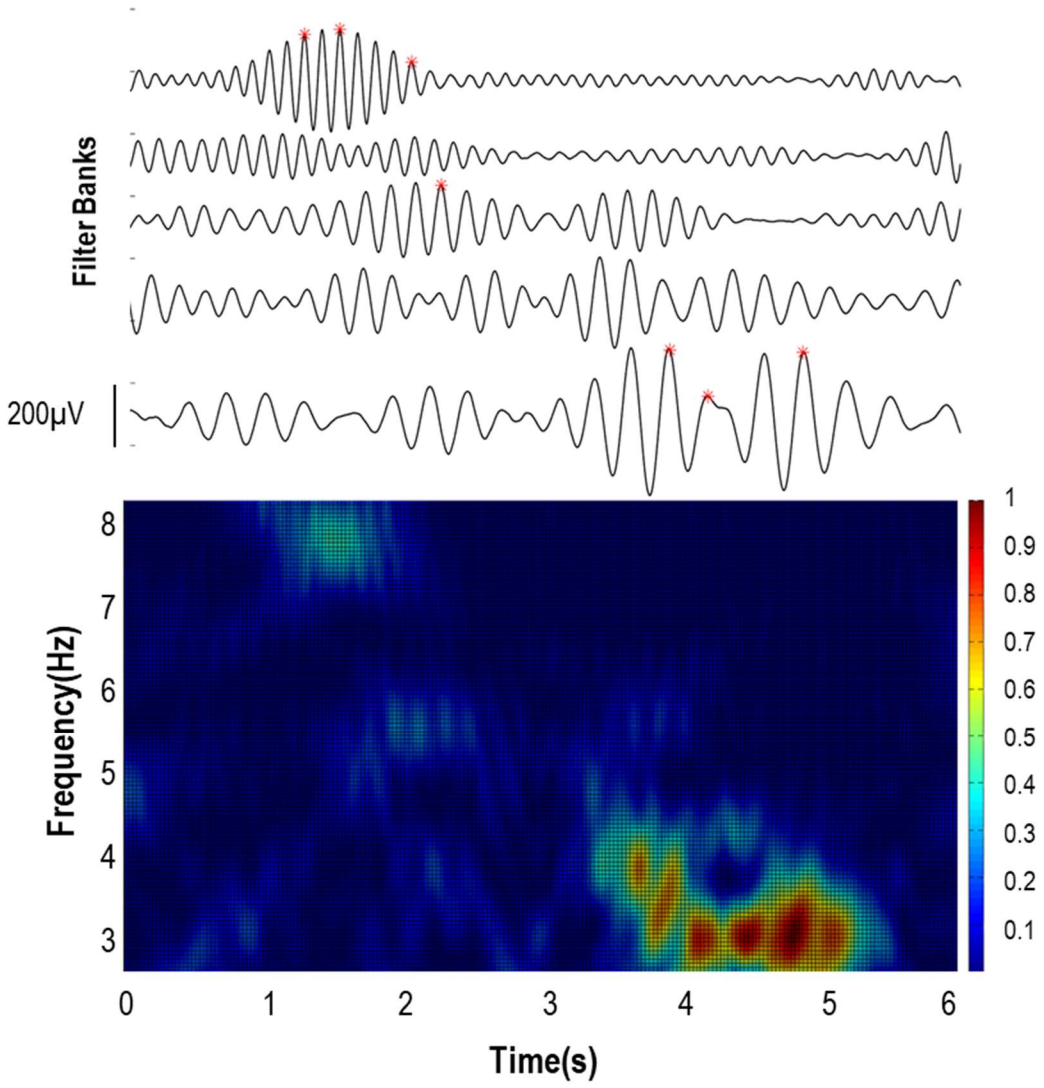

Figure 5.11: Sample measured stimulation timestamps and signal spectrogram.

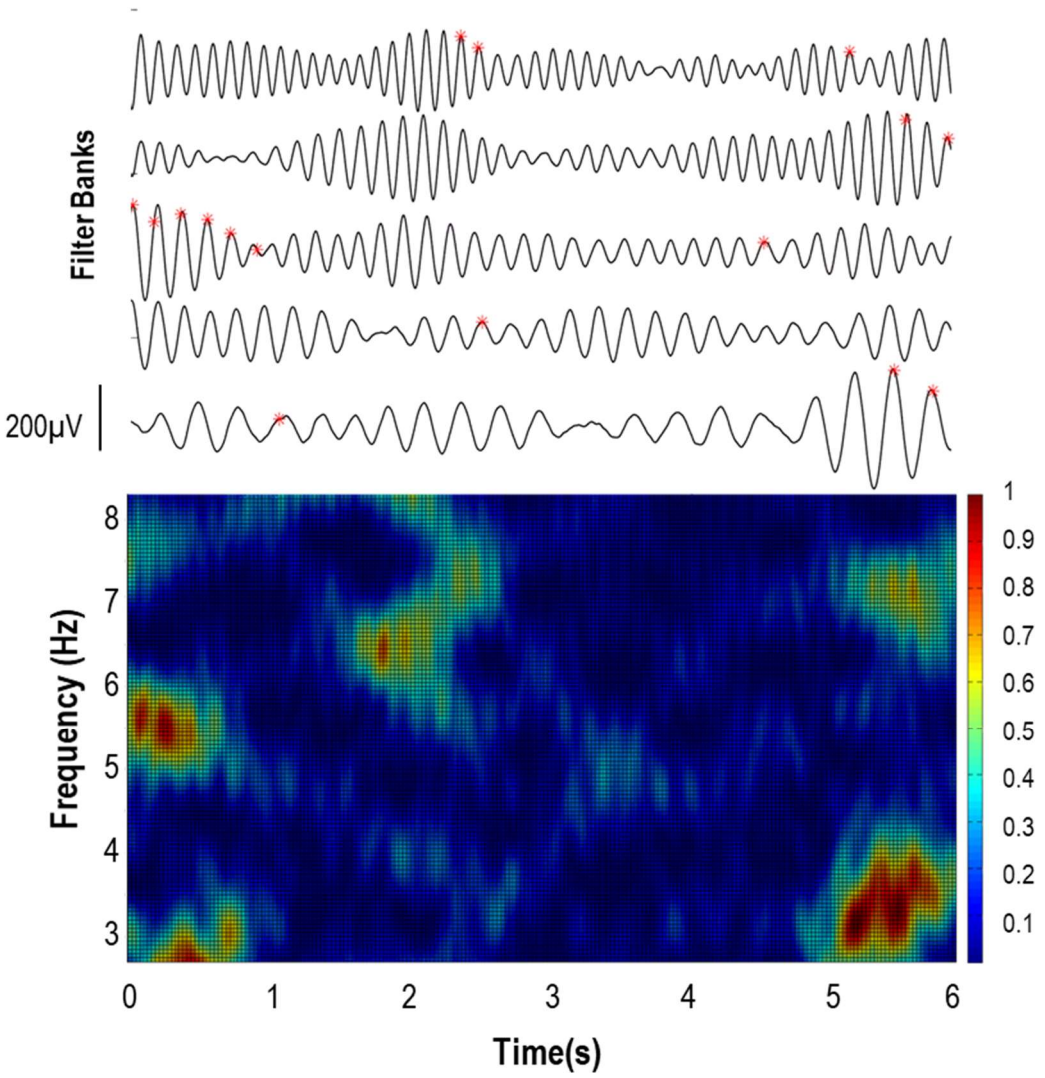

Figure 5.12: Sample measured stimulation timestamps and signal spectrogram.

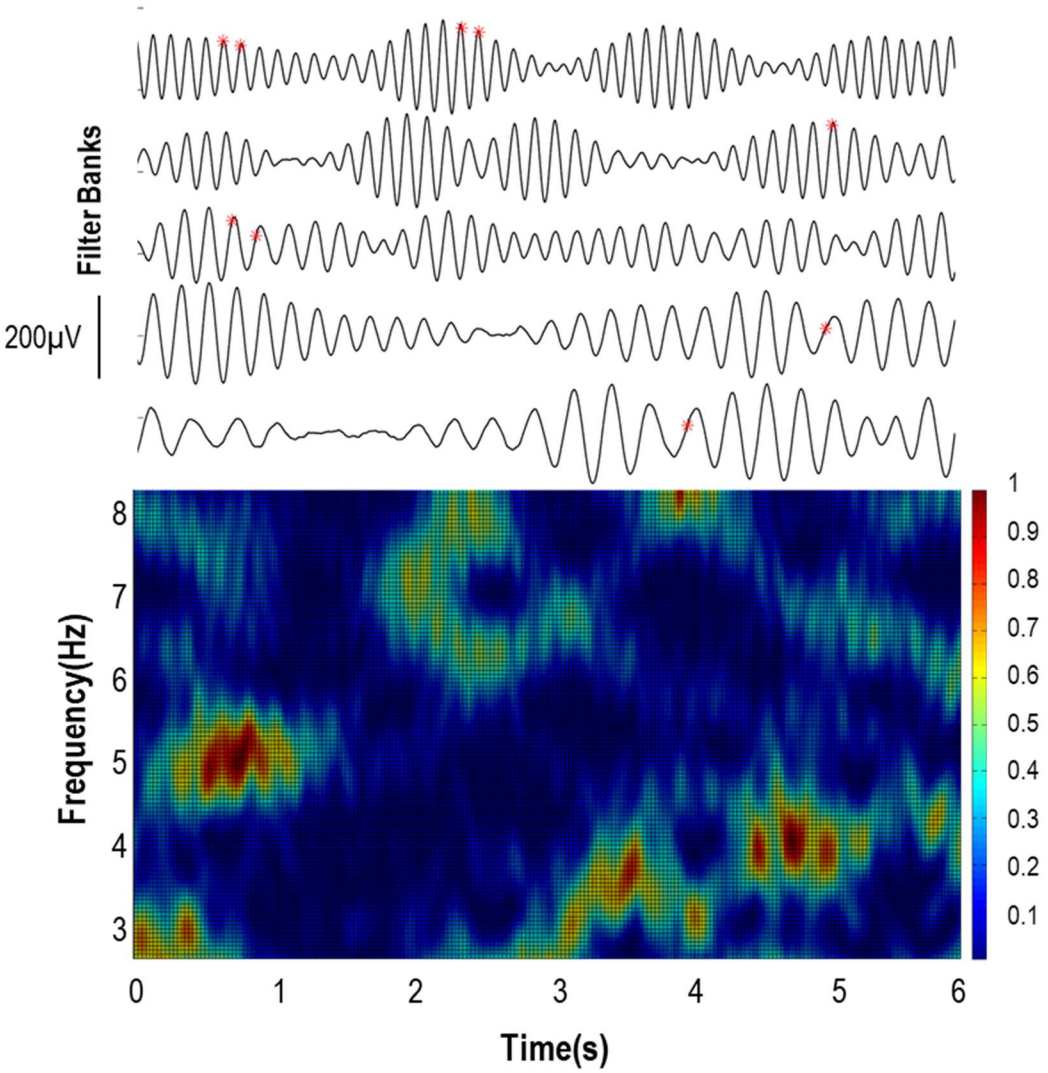

Figure 5.13: Sample measured stimulation timestamps and signal spectrogram.

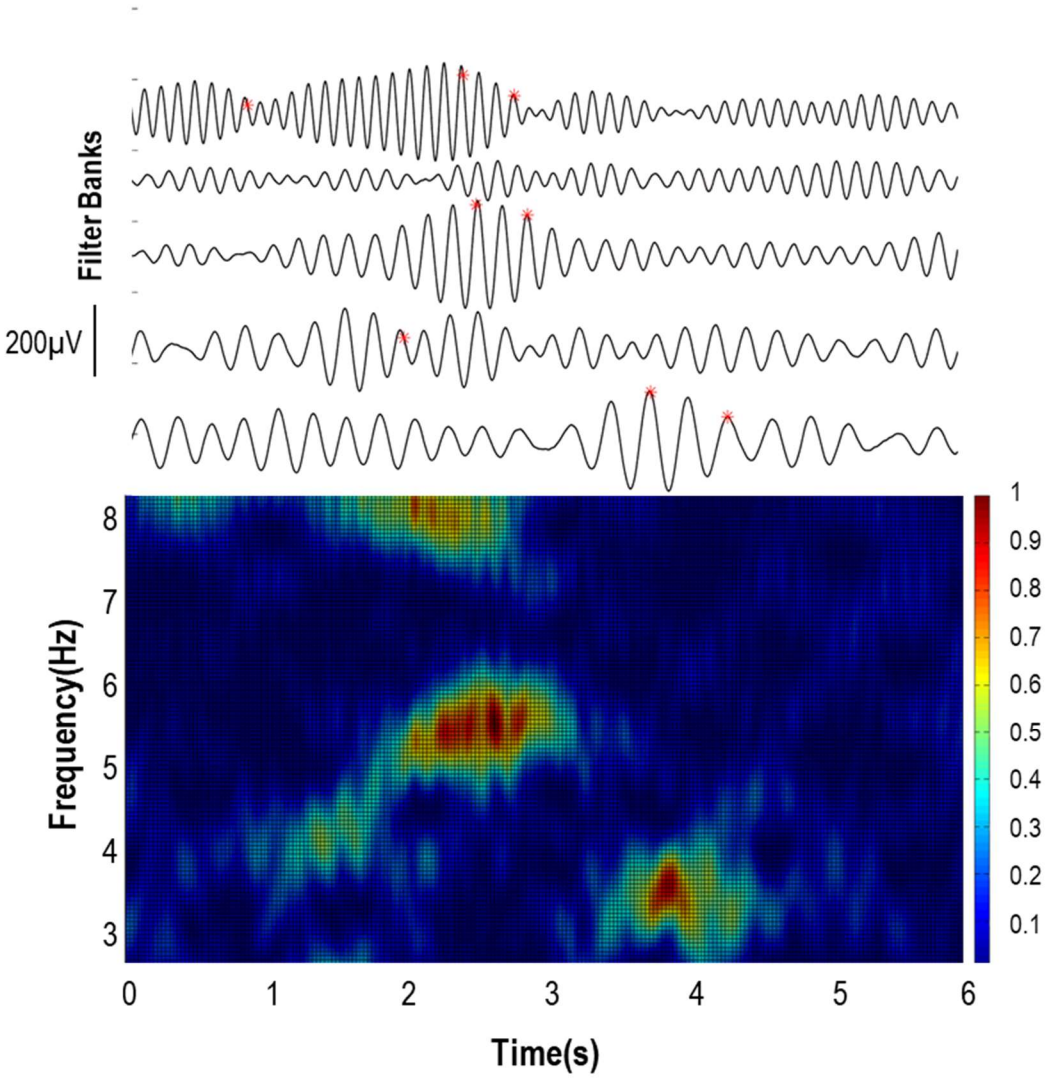

Figure 5.14: Sample measured stimulation timestamps and signal spectrogram.

5.8 Discussion

The chapter presented the design of a configurable platform for stimulation protocol development with on-board closed-loop ps-stim capability that has been verified in-vitro in preparation for clinical experiments. System-level aspects as well design considerations for implementing new algorithms and stimulation protocols are discussed in this section.

5.8.1 ps-stim closed loop latency

Controlling the loop latency was critical in achieving the accuracy and precision in the direction of the requested phase. Generally, closed-loop systems' loop latency consists of two main components:

1) Algorithmic latency: This is application dependent; in the case of ps-stim on Theta we require a Theta epoch to be able to predict the phase accurately.

2) System latency: These include system control logic, the communication up and down links, and software latency.

Table 5.5: ps-stim closed-loop system latency summary.

Latency	Mean (ms)	STD (ms)
Sense + PLS	0.1	0
PLS trigger to Stim.	1.6	0.3
Total	1.7	0.3

Not only the total latency is critical to the closed-loop system performance, but the latency variance around the mean. Algorithmic latencies are generally fixed with zero variance, while system latencies are nondeterministic. Unlike fixed delays, random delays cannot be accounted for by the algorithm and can affect its performance substantially. All necessary measures were taken at the chip, FPGA, and software levels to ensure limited and controlled closed-loop latency.

To ease assessing the system latency of the closed-loop ps-stim (see Figure 5.15 and Table 5.5), we divided the loop latency into two major sections:

1) Sense to PLS trigger:

This includes system delay of the sense and PLS IC.

2) PLS trigger to stimulation pulse delivery:

The latency of this path was estimated in a 40-trial experiment (Figure 5.16) where the actual delay between the ps-stim trigger and the delivery of the stimulation pulse was measured in the laboratory.

Due to the communication link and having the software in loop, the system latency was observed to vary around the mean. By assigning the closed loop stimulation commands the highest software priority, and by limiting all the signal

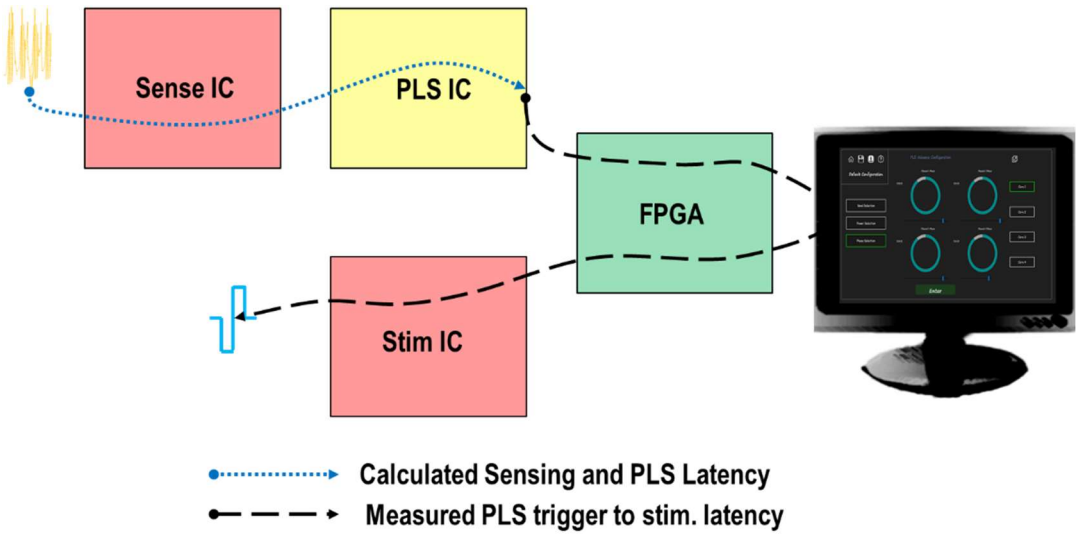

Figure 5.15: Illustration of the closed-loop system latency

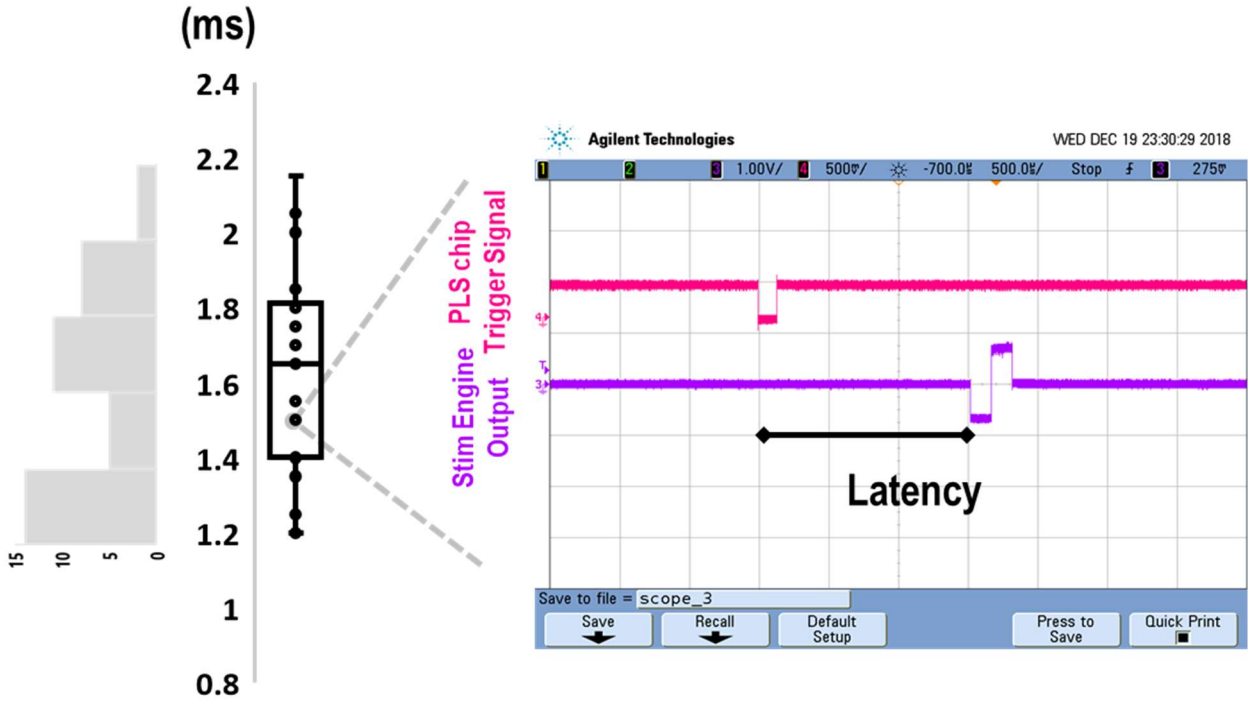

Figure 5.16: 40-trial Boxplot of the measured activation latency (from the ps-stim chip trigger onset to the delivery of the stimulation signal). The Closed-loop system features a small latency mean and variance. Low uncertainty in the loop delay is critical to the algorithm performance.

processing to the onboard chips, an extremely low variance was achieved. The limited and controlled system latency ensures the ps-stim algorithm operates at the maximum rated performance.

5.8.2 Closed-Loop ps-stim Safety Measures

A phase-specific stimulation opportunity generated by the ps-stim chip is only forwarded to the stimulation engine if and only if phase-specific stimulation is enabled in the GUI by the operating clinician and the USB cable is connected. In the unlikely and unforeseen circumstances such as a software freeze, we designed the ps-stim shutdown strategy to simply be unplugging the USB cable, which is guaranteed to terminate ps-stim regardless if the device was USB or battery powered. This was achieved by requiring software approval for every ps-stim trigger signal.

Alternatively, for the battery-powered scenario, we could have instructed the platform operator to unplug the battery and eliminated the PC from the loop. However, the latter strategy was avoided for two reasons: first, having two closed-loop stimulation termination options – depending on how the device is powered – could be confusing and error-prone, secondly, all the necessary steps were taken to ensure negligible additional latency. It should also be noted that some USB modules feature USB cable connectivity sensing, however, we choose not to rely on third-party interrupt for closed-loop ps-stim termination.

5.8.3 Higher-Level ps-stim Protocols

The platform not only offers configurable parameters at the algorithm level, but also powerful system flexibility if accompanied with the former could enable a wide range of phase-synchronized experiments.

Example ps-stim protocol:

Brain oscillations are believed to play an important role at the network-level in coordinating brain functions across its different regions. The platform allows sensing in one site and delivering phase-synchronized stimulation pulses simultaneously on up to 8 sites, anywhere on the 64-site electrodes. As mentioned previously, the number of sensing/stimulation channels on the platform could be quadrupled by stacking 3 more analog layers. It is also possible to introduce a phase shift - by setting the appropriate target phase for each engine - between the stimulation pules delivered to sites spanning distant brain regions.

5.8.4 Hosting Future Algorithms

The device has additional resources that support integrating new closed-loop algorithms. As discussed in section 5.8.1, the closed-loop link was designed carefully to ensure limited and controlled system-latency. The achieved latency is

on par with the fundamental neural processing event - the single unit spiking activity which has a period of around 2ms.

There are two available options to host future algorithms 1) Software 2) accelerated hardware realization on the available FPGA resources. Due to the parallel processing nature offered by the second option, it's particularly suitable for computationally expensive and closed-loop-latency critical application.

6 | Conclusion and Future Work

6.1 Conclusions

Implantable therapeutic brain stimulation devices must meet stringent area and power requirements and provide automated stimulation protocols to minimize human intervention. The dissertation presented an unsupervised theta phase-specific stimulation algorithm and chip, which has a very low area compared to state-of-the-art sensing and stimulation engines, with implant-scale power consumption. Therefore, it offers a prospect for more controlled memory enhancement, in addition to potential system energy savings and reduced DBS side effects, when integrated in an implantable device.

As a step towards enabling phase-specific – and higher-level – stimulation protocols development in clinical environments, and to support the implantable solution design efforts, the chip was integrated with an AFE and a stimulation engine in a hand-held class II brain stimulation system. The platform hosts the entire closed-loop neural processing and modulation chain, starting from the neural signal sensing, to real-time bio-marker processing, and finally, the stimulation pulse generation. Moreover, the platform offers free hardware resources and software support to design higher-level stimulation protocols that may embed the ps-stim capability.

To ease rapid stimulation protocol evaluation and development, the platform features a graphical software interface to the hardware platform. Configurable software features include the stimulation pulse strength and period, electrode-site, in addition to the desired target phase for Theta-synchronized stimulation delivery. Therefore, facilitating a wide range of experiments that can, hopefully, bring us a step closer to restoring and enhancing memory.

6.2 Future Work

At the time of the dissertation writing, all the necessary UCLA institutional review board (IRB) approvals were received to use the SPD platform on human patients. We are excited to soon be conducting closed-loop experiments that include studying the phase-specific stimulation in-vivo in human.

The software, hardware flexibility, and the ultra-low closed-loop latency – just below a spike period (the brain processing resolution or fundamental unit) - offer limitless possibilities to develop stimulation protocols studying the human brain. In the near future, we wish to explore phase-specific stimulation not only locally but - as was discussed earlier - at the network-level. Moreover, we are working to include the necessary modification to target other brain oscillations outside Theta band, and higher-level protocols employing broadband neural signal coherence. Since synchrony at the network-level - at the offered data rate and channel count - can be

difficult to coordinate for a successful stimulation decision, machine learning techniques are potential closed-loop protocol candidates for the platform.

The handheld platform features implantation-ready compact and ultra-low power chips, that readily support the future effort to transition to class IV implantable stimulation system for a long-term therapy solution.

6.3 Research Contributions

The dissertation aims to provide clinicals and scientists with a closed-loop low latency phase-specific stimulation and protocol development hand-held platform, that features implantation-ready ps-stim chip for long-term implantable therapy solutions. Towards that end, the dissertation made the following main research contributions:

- Developed a new closed-loop unsupervised hardware-efficient algorithm to adaptively trigger phase-specific brain stimulation. Offering a prospect for more controlled memory enhancement, reduced DBS side effects and increased battery life in implantable devices.

- Conducted algorithm and system-level optimization to arrive at a hardware-efficient architecture realization.

- Designed and taped-out an implantation-ready ultra-low power and small area chip in TSMC 40nm low power technology.

- Integrated the chip in a hand-held closed-loop stimulation protocol development platform, that capitalizes on the platform many electrodes to deliver brain-network-level ps-stim. The platform design includes a clinician friendly ps-stim configuration GUI.

- Demonstrated in-vitro measurements of the closed-loop platform in preparation for human experiments.

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