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POSITRON EMISSION TOMOGRAPHY

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ABSTRACT

The scintillation photon detection and event selection subsystem for the high spatial resolution Donner 600-channel positron emission tomograph is described. The tomograph spatial resolution of better than 3.0 mm, FWHM, is obtained by using 600 closely-packed bismuth germanate 3 mm thick scintillation detectors. Each detector has its own 13.5 mm diameter photomultiplier and event selection channel, consisting of two fast pulse amplifiers, a charge integrator, a differential pulse height discriminator and precision time delay for event strobing. The event selection channel is capable of starting a timing cycle from the first photoelectron emitted from the photocathode. It is also capable of discriminating between true events and noise and of eliminating events occurring simultaneously in two adjacent channels. Adjustments of the event strobing time and two discriminator levels are performed by a computer.

INTRODUCTION

In many recently developed positron emission tomographic systems small scintillators and small diameter photomultipliers are used as detectors to obtain a high spatial resolution and sampling density¹. Minimizing the coincidence resolving time to reduce the number of random coincidences is an important factor in the design of such systems. Generally, such a system requires a large number of fast scintillators and high time resolution photomultipliers².

In this paper a new scintillation detection and event selection subsystem for the high spatial resolution Donner 600-channel positron emission tomograph is described. The high spatial resolution is achieved by using 600 closely-packed bismuth germanate scintillation detectors. Each detector has its own photomultiplier and event selection channel². Detectors, including the photomultipliers, are arranged in a close packed single layer ring having a diameter of 60 cm. The dimensions of an individual detector are 3 mm x 10 mm x 25 mm. The inner diameter of the ring is 30 cm.

SCINTILLATION PHOTON DETECTION

The major time resolution limitations of a tomographic system are due to variations of the location of the scintillation events in the scintillators, fluctuations in the light collection process, and the time resolution capabilities of the photon detector.

Several photon detectors, such as silicon PIN and avalanche photodiodes as well as high gain photomultipliers, were initially considered for the scintillation detection subsystem. In the first part of 1982 when a decision was due on the selection of the system's 600 photon detectors, the silicon PIN and avalanche photodiodes did not have a capability for the first photoelectron detection. (The first photoelectron detection gives the highest time resolution needed for coincidence detection in positron emission tomography⁴). These devices, when operated at room temperature, did not have gain bandwidth product, low noise level, gain-quantum efficiency uniformity, and long term stability necessary for the detection subsystem. Although the energy resolution of the solid state photon detector can be significantly increased by their operation at cryogenic temperatures⁵ it was unlikely that device adequate time performance could ever be achieved for 511 keV annihilation photons. Consequently, the solid state photon detectors were eliminated from further consideration for possible application in the 600-channel positron emission tomograph. Efforts were directed toward selection of the most suitable high-gain photomultiplier having a small diameter photocathode and to determine its optimum operating conditions^{6,7}. From several candidates, of which some were in the experimental stage of development, Hamamatsu R647-01 photomultiplier was finally selected for scintillation detection subsystem on basis of its performance, cost and availability.

The R647-01 is a 13.5 ± 0.5 mm-diameter, 10-stage, head on, flat-face plate type photomultiplier with a bialkali photocathode having a S-11 response. Because of its small size, the photomultiplier is particularly suitable for high spatial resolution tomography systems. The photocathode has a peak response of 420 nm and a useful photocathode diameter of 9 mm. The multiplier utilizes a box type in-line dynode structure.

Our measurements have shown that the photomultiplier has a gain of 1 to 1.2 × 10⁶ at 1000 V and average dark current at this voltage of 350 pA. The average quantum efficiency was found to be 28% at 410 nm for five photomultipliers. Furthermore, the photomultiplier operating at 1000 V, which corresponds to a gain of 10⁶, has measured the dark pulse count:

$$\begin{aligned} &16 \text{ photoelectrons} \\ \sum &= 54 \text{ counts per second} \\ &1/8 \text{ photoelectron} \end{aligned}$$

Time resolution capabilities of the photomultiplier are essentially determined by the random deviations in the transit time of electrons traveling from photocathode to collector.

The electron transit time spread is mainly caused by fluctuations of individual times of flight of photoelectrons and secondary electrons due to their different trajectories and their initial velocity differences. The factors that contribute to the transit time spread are differences in trajectory lengths and in electrical field strengths in different portions of the photocathode-first-dynode region, and between various dynode sections. In addition, the transit time spread depends upon the number of photoelectrons released from the photocathode since the time spread varies approximately inversely as the square root of the number of photoelectrons. The time behavior information of single photoelectrons can be used for predicting the transit time spread for an arbitrary number of photoelectrons. Consequently, the best characterization of the photomultiplier electron transit time spread is given by the single photoelectron time performance³.

The R647-01 single photoelectron pulse response, using a modified manufacturer voltage divider to achieve a better match to the 50 Ohm external load, and the single photoelectron time spread with full photocathode illumination, are shown in Fig. 1 and 2, respectively. The 10-90% rise time of a single photoelectron pulse of the photomultiplier was found to be 2 ns $\pm$ 0.3 ns at 1000 V. The single photoelectron time spread was 1.22 ns, FWHM⁶.

ANALOG PROCESSING OF EVENTS

The detector photomultiplier output contains many unwanted signals. Each detector is served by an individual analog processing channel, and this circuit should pass only events meeting required preset criteria and eliminate all others as early as possible. The criteria for elimination of the "nonevents" are preset and each channel is individually matched to its assigned detector for best performance. In order to compensate for the detector aging, the critical parameters are individually controlled by computer, allowing remote alignment and test of the whole system.

Each of the system's 600 detectors requires an individual analog processing channel. The detector signal is brought in directly from the photomultiplier by a 50-ohm cable. Since the signal level received across the matching termination resistor is in the millivolt range, great care was taken to minimize noise pick-up and crosstalk between the channels.

The analog processing channels are organized in groups of eight, each group mounted on a single 19" x 10" printed circuit board. There are 75 such boards in the system. Each board also contains digital circuits for the control of individual channels by the computer. Stable on-board power regulators were designed to maintain a constant supply voltage such that the analog circuits are independent of changes in the bus voltage and variations in contact resistance. These regulators also reduce noise on the power lines, which in turn results in a stable and jitter-free performance of the analog circuits. Special care has been taken to keep power dissipation at a minimum.

A general block diagram of an 8-channel analog processing subsystem is shown in Fig. 3. Each channel (No. 0 to No. 7) can be remotely controlled by three 8-bit digital-to-analog converters (D/A 1 to D/A 3) with data latches. D/A 1 controls the strobing time of the event being processed, and D/A 2 and D/A 3 control the lower and upper discriminator levels of the single channel pulse height analyser monitoring the event's charge. All 24 D/A converters on the board have a common Data bus (D0 to D7). Each converter is strobed by one of the corresponding decoder outputs (D1 to D3). The three decoders are in turn controlled by three Crystal Number bus lines (A0 to A2) and strobed one at a time by a Function Decoder (D). The fourth decoder function controls an octal Veto 3 latch (L). When a latch is set, the corresponding analog channel is out of operation. The decoder (D) is addressed by two Function lines (F0 and F1). A 13-bit word is thus needed to define the command controlling any of the 24 D/A converters and 8 veto latches. The command is executed upon the receipt of a Strobe pulse. All vetoes can be removed simultaneously by resetting the veto latches with a Global Clear pulse.

Each analog channel also responds to two additional veto inputs. The function of these vetoes is to block certain analog functions in the processing of events which will be discussed later. The eight pairs of corresponding veto inputs are bussed and control all eight analog channels simultaneously.

The photomultipliers, signals from which are brought to the analog channel inputs, are labelled PMT No. 0 to PMT No. 7. An event that meets all the preset conditions will produce a fast, precisely timed ECL pulse at the channel output (Event Out). The eight event outputs are fed by 100-ohm microstrip transmission lines to the pins of an edge connector. From there the signals are transferred to the central fast logic processor.

A group of fast logic gates (G1 to G3), provided the Veto 1 signal is not applied, is designed to inhibit the event output of any channel if either its left or right neighbor channel is also processing an event at the same time. This means that probably the same gamma ray has hit two adjacent detectors and the event should be aborted. The end channel on either side of each board has a provision for controlling of the end channel of the adjacent card. Of course its end channels can be controlled by the adjacent boards. All 600 analog channels thus are daisy chained, making a circle where each one controls its left and right hand neighbor and is being in turn controlled by them.

Analog Processor Description

The photomultipliers generate random signals of various magnitude and duration. The purpose of analog processing is to examine all signals and immediately eliminate those not meeting the required amplitude level and time duration. The selection takes a very short time, allowing the processor to sort out all incoming signal pulses in search for a potential event. Analog processing channel block diagram is shown in Fig. 4. Detailed schematic diagram is given in Fig. 5.

Referring to Fig. 4, an input signal is immediately and evenly split upon its arrival between two wide-band amplifiers, separating two parallel lanes of analog processing. The gain of timing amplifier (TA) is high and a few millivolts of signal amplitude

is sufficient to drive the output to saturation. The leading edge of the output pulse is thus made very sharp and it serves as a time reference marking the start of an event. The second half of the signal is amplified by a fast linear amplifier (CA) and further integrated in a fast gated charge integrator (CI). The integrator is enabled when a clocked event latch (EL) is set by the leading edge of the timing portion of the signal passing TA.

Selection of signals of various amplitude and duration is illustrated by the timing diagram in Fig. 6. The upper sequence shows two short random "noise" signals, each having sufficient level to saturate the timing amplifier (line A). Event latch is set immediately, which in turn starts integration of the charge defined by the magnitude and waveform of the signal (line Ap). A delay timer is also started by EL, preset to produce a pulse fed back to its own clock input 50 ns later (lines C and D). The trailing edge of the clock checks the status of the latch D input, tied also to the signal A. Since both "noise" signals have already decayed below the triggering threshold at this time, the latch is reset by the clock and the integrator quickly discharged. Only a few nanoseconds are required for the recovery before a new signal can be tested.

If the signal duration exceeds 50 ns, the latch remains set and the charge integration continues (Event Cycle portion of Fig. 6). Bold lines A and Ap show a signal lasting several hundred nanoseconds, and the integrator output increases accordingly (line L). A precision 500 ns timer was started when the latch EL was set. The purpose of this timer is to produce a clock pulse exactly 500 ns after the start of the event. Each of the 600 processing channels must have this identical delay and be very stable. Small adjustments in delay of up to ± 30 ns due to the system time propagation differences can be made by the computer. An 8-bit D/A converter controls the delay in 0.25 ns steps (Fig. 4).

During the 500 ns integration time the integrator output is monitored by two discriminators (LD and UD). Each discriminator is controlled by an 8-bit D/A converter, which allow each to be set by the computer to any level within the range of the integrator. When the charge exceeds the lower discriminator level (Fig. 6, line M), the first criterion for recording an event is satisfied. The D input of the event latch timer (ET, Fig. 4) is armed through a gate G3 and set by the delay clock exactly 500 ns after the event started. A short time delay circuit resets the latch 30 ns later. The latch thus generates a 30 ns wide event pulse (Fig. 6, line N) which is sent to the tomograph coincidence circuits in search of a matching pulse that may result in confirming the occurrence of a real event.

If the charge integrated during the 500 ns period exceeds the expected level, the upper discriminator fires (dash-dot lines L and S), closing the anticoincidence gate G3 which prevents the firing of the event latch. No event pulse is sent out in this case.

The remote control of discriminator levels can turn each analog processor into a multichannel pulse height analyzer. When using an appropriate radioactive calibrating source, the computer scans the discriminators automatically through the integrator range. The gain of each charge amplifier is then adjusted and discriminator levels are set to center

the energy band of interest into the desired amplitude range. Valid events are those falling within the range.

Although the processing is completed after the event pulse is sent out and event latch timer reset, the processor must remain paralyzed to prevent retriggering by photons in the tail of the scintillator light pulse. The end of the 500 ns delay starts a second, 1.5 μ s deadtime timer. A pulse is generated at the end of 1.5 μ s which clears the latches and discharges the integrator. The processor is then immediately ready for a new event.

There is a large category of signals long enough to pass the 50 ns duration test. Their amplitude however may be too small to produce charge sufficiently large to exceed the lower discriminator threshold. Since this condition can be detected early, the processing cycle deadtime can be made shorter than 1.5 μ s (dotted lines in Fig. 6). The signal lasts long enough to pass the 50 ns duration test (lines A and D). At this moment an amplitude discriminator LL is tested which clocks the charge amplifier signal (Fig. 4). If the signal level at the 50 ns point is below the preset threshold, the discriminator does not fire (line E in Fig. 6) and thus does not enable the deadtime delay timer. The consequence is that the deadtime is reduced to 0.1 μ s instead of the normal duration of 1.5 μ s. The processing rate of signals is therefore substantially increased.

When processing a regular event the signal amplitude is sufficiently large to set the LL latch (line E) and enable the deadtimer to full 1.5 μ s delay. Also, a 40 ns wide pulse is generated at this moment by a left/right veto timer (lines F and G). This pulse enables gates G1 and G2 for a short time (Fig. 3). The gate G1 is controlled by the veto timer of the processing channel on the left and the gate G2 by the processing channel on the right. Should the neighbors produce an overlapping pulse, the gate G3 passes this coincidence back to the analog processor setting a left/right veto latch (lines Q and R). This latch in turn keeps reset the event timer. The signal processing continues, but the event will be aborted regardless. How effective this method is can be tested by applying an external Veto 1. The veto timer will be disabled and all events can be processed regardless of possible overlap between adjacent channels. When applied, Veto 1 affects all 600 analog channels.

Veto 2 controls also all analog processors of the tomograph. When applied, the noise elimination feature is disabled, allowing the processing of all signals as though all were potential events. These vetos are useful in testing the effectiveness of the event filtering procedure.

Veto 3 prevents the operation of the whole processing channel. Since each channel has an individual Veto 3 latch, addressable by computer, any combination of the tomograph detectors can be temporarily shut down when running test routines.

A number of test points throughout the analog processing channel makes alignment and monitoring easy. The timing and levels of all parameters discussed above can be individually preset so that all channels can be made identical. The adjustment range is sufficiently wide to permit realigning any parameter, if required, without the need to change circuit components.

CONCLUSION

Reliability was the principal consideration in designing the analog processing circuits serving the 600 photodetectors of the tomograph. The potential statistical failure of a system comprising such a large number of electronic components was a major concern. The building blocks of each of 600 analog processing channels are two wide band amplifiers, a fast gate charge integrator, two computer controlled level discriminators, a precision computer controlled time delay, a programmable deadtimer, three fast pulse generators, a fast amplitude discriminator, a fast time discriminator and logic circuits including fast coincidence circuits and gated latches.

Analog processors are combined in groups of eight mounted on a single printed circuit card, including a total of 24 D/A converters and digital computer interface logic. All analog circuits use only +5V and -5.2V power lines in order to minimize power dissipation. Precision regulators maintain these voltages stable and noise free, requiring only 6V supplies. The system cost was kept low by using inexpensive standard integrated circuits and discrete components.

A test station was designed and an alignment procedure devised to ensure that all 600 channels can be made identical. The procedure, aided by Hewlett-Packard 86 computer, includes the adjustment of 13 controls per channel for proper setting of the timers and discriminators and includes the trimming of the D/A converters for optimum tracking.

Final adjustment of gain and threshold is required in order to match each channel to its assigned detector as was described earlier. Once aligned, the analog processors have exhibited excellent stability. No measurable drift of preset parameters was found so far when random channels were rechecked. The photomultiplier drift and aging is the only potential source of need for periodic adjustment.

Only a few analog channel failures were reported so far (during the first thousand hours of operation). They were caused by a couple of failed integrated circuit chips and some capacitors shorting the power lines. In the system comprising over 7,500 integrated circuits, 7,500 discrete semiconductors, 63,000 resistors and 26,000 capacitors the number of failures was surprisingly low. The performance of the tomograph system is summarised in Ref. 8.

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Fig. 5. Analog processing channel schematic diagram.

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Fig. 4. Analog processing channel block diagram.

Fig. 6. PET timing diagram.

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