Title

Gate-All-Around Nanowire Field-Effect Transistors: A Historical Perspective

Journal

Nano Letters, 26(15)

ISSN

1530-6984

Authors

Tang, Lei

Yang, Peidong

Publication Date

2026-04-22

DOI

10.1021/acs.nanolett.6c00466

Gate-All-Around Nanowire Field-Effect Transistors: A Historical Perspective

Lei Tang[1] and Peidong Yang[1,2,3,4*]

[1]Department of Chemistry, University of California, Berkeley, Berkeley, California 94720, United States;

[2]Department of Materials Science and Engineering, University of California, Berkeley, Berkeley, California 94720, United States;

[3]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States;

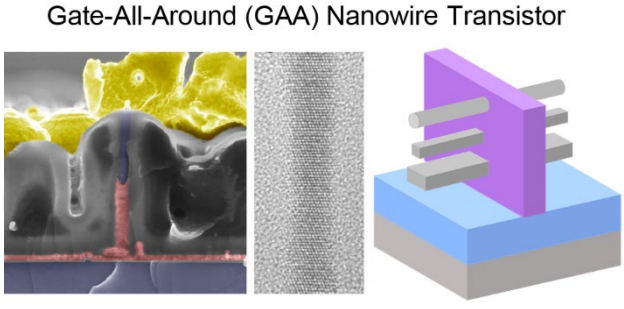
[4]Kavli Energy NanoScience Institute, Berkeley, California 94720, United States;

*Email: p_yang@berkeley.edu

ABSTRACT

The development of transistor architectures, evolving from 2D planar metal-oxide-semiconductor field-effect transistors (MOSFETs) to FinFETs and then to gate-all-around nanowire (GAANW) FETs, plays a crucial role in downscaling technology nodes in the semiconductor industry. This perspective reviews the concept of MOSFETs and summarizes this historical development, with particular emphasis on GAANW transistors due to their importance in next-generation technology for nodes below 3 nm. Specifically, the concept of GAANW transistors and their advantages over planar and FinFET devices for further scaling are presented, along with a discussion of their transition from early conceptual ideas to laboratory demonstrations and, ultimately, to industrial adoption. Furthermore, potential solutions, such as complementary FETs (CFETs) and 2D semiconductor-based FETs, and their associated challenges for the future generation, known as the Angstrom Era, are discussed in a technological roadmap. This perspective may inspire both industry and academia in future research directions for realizing the Angstrom Era.

Keywords: gate-all-around transistors, nanowire transistors, technology evolution, transistor scaling, sub-3 nm technology nodes.



TOC graphic

The metal-oxide-semiconductor field-effect transistor (MOSFET), which functions as either a switch or an amplifier, is the core component of modern integrated circuits used in many electronic devices for a wide range of applications, including computing and memory.[1, 2] The downscaling of MOSFETs is crucial for achieving faster switching response and lower resistance, thereby enabling more energy-efficient electronic devices. Over the past six decades, the general trend in semiconductor technology has largely followed Moore's law, which states that the number of transistors on an integrated circuit doubles every two years. Modern circuits now contain hundreds of billions of transistors, and this number continues to grow as MOSFET design advances, despite the challenges of high-cost fabrication.

With the rapid increase in transistor density, the technology node has been used to characterize the progression of semiconductor fabrication technology. The technology node typically corresponds to the minimum physical dimension, or gate length, achievable with manufacturing equipment until the mid-1990s, during which 2D Planar MOSFETs dominated the semiconductor industry. In the late 2000s, especially after the introduction of FinFETs,[3] node names largely decoupled from gate length, as gate length could no longer directly indicate transistor performance.[4] The so-called Gate, Metal, Tier (GMT) method, which involves the concepts of gate/metal pitch and the number of tiers, has been used to characterize the current technology node.[4]

The 3D FinFET has demonstrated improved electrostatic control because its fin-structured channel is surrounded on three sides by the gate, thereby overcoming many challenges of conventional planar MOSFETs, such as severe current leakage caused by short-channel effects, and enabling its use in the 3-nm node. Although powerful, FinFETs are approaching their practical limit for further scaling. Gate-all-around nanowire (GAANW) transistors are promising solutions and are now leading the next era of semiconductor technology, with nodes smaller than 3 nm.[5]

This perspective will briefly review the concept and historical development of MOSFETs, with particular emphasis on GAANW transistors, and discuss the future evolution of technological nodes below 3 nm and their associated challenges, while highlighting the latest emerging research needs in semiconductor node scaling. Unlike recently published review articles,[6-10] this perspective will provide the latest information on current transistor technologies and offer a more detailed and precise summary of the historical development of GAANW transistors.

EVOLUTION OF EARLY MOSFET STRUCTURES

Fundamental Theories Driving Transistor Evolution. The evolution of transistor architectures has been driven mainly by theories including semiconductor physics and scaling theory.[2,11] From a semiconductor physics perspective, the gate voltage modulates the energy band structure and, consequently, the charge carriers in the channel underneath the gate, thereby controlling the current flow from the source to the drain, which is the fundamental operating principle of MOSFETs. Therefore, device performance can be improved by enhancing carrier properties. This has led to the introduction of strain in silicon to modify its band structure, as well as the use of high-dielectric-constant (k) materials, both of which enhance carrier mobility and ultimately device performance.[6] As device dimensions continue to shrink, limitations such as leakage current, short-channel effects, and electrostatic control issues arise,[12,13] which degrade performance and drive the development of new architectures. From scaling theory,[11] improved electrostatic control and mitigation of short-channel effects can be achieved by providing gate control from multiple

directions. Consequently, MOSFET architectures have evolved from planar structures to FinFETs and eventually to GAA devices. This evolution is discussed in detail in the following sections.

Planar MOSFET: Above 25 nm Nodes. The MOSFET was first demonstrated at Bell Labs in 1960,[14] and its 2D planar structure subsequently dominated the semiconductor industry until 2011. Specifically, the planar MOSFET is the conventional device structure consisting of a source, a drain, and a metal gate stacked on top of a thin oxide layer that electrically isolates the gate from the substrate, as depicted in Fig. 1a. Such a device is called planar because its channel lies essentially in the same plane as the substrate surface. The gate controls current flow in the channel region. When a voltage is applied to the gate, a depletion layer forms at the channel region, which can be manipulated to regulate the current flow from the source to the drain. The source/drain structure can thus be switched between conducting (on) and nonconducting (off) states, depending on whether the applied gate voltages exceed the threshold voltage. Two primary types of transistors, p-MOSFETs and n-MOSFETs, with different charge carriers (holes or electrons), have been used together to enable the development of modern integrated circuits, including both digital and analog circuits.

The dimensions of the planar MOSFET, particularly the gate length L_g, have been reduced significantly, mainly due to improvements in lithography and shallow junction formation, as well as the introduction of technologies such as silicide contacts (e.g., Ni-silicide on top of poly Si gate to reduce contact resistance), channel strain engineering, and high-dielectric-constant (k) metal gate (HKMG).[15-20] These combined efforts enabled the technology node scaling from 90 nm to 65 nm and then to 32 nm (see Fig. 1b), which correspond to transistor gate lengths (L_g) of approximately 45 nm, 35 nm, and 30 nm, respectively.[16, 17, 19] For instance, a 32-nm node with HKMG technology was first manufactured and commercialized by Intel in 2009.[19] However, as the gate length decreases, it introduces numerous challenges, including short-channel effects.[12, 13] Such effects can lead to many problems, such as sub-channel leakage, direct-source-to-drain tunneling, mobility degradation, and loss of threshold control, resulting in performance degradation and reliability issues. To overcome these challenges, transistors have been advanced to various designs, such as FinFETs, particularly for technology nodes below 25 nm.

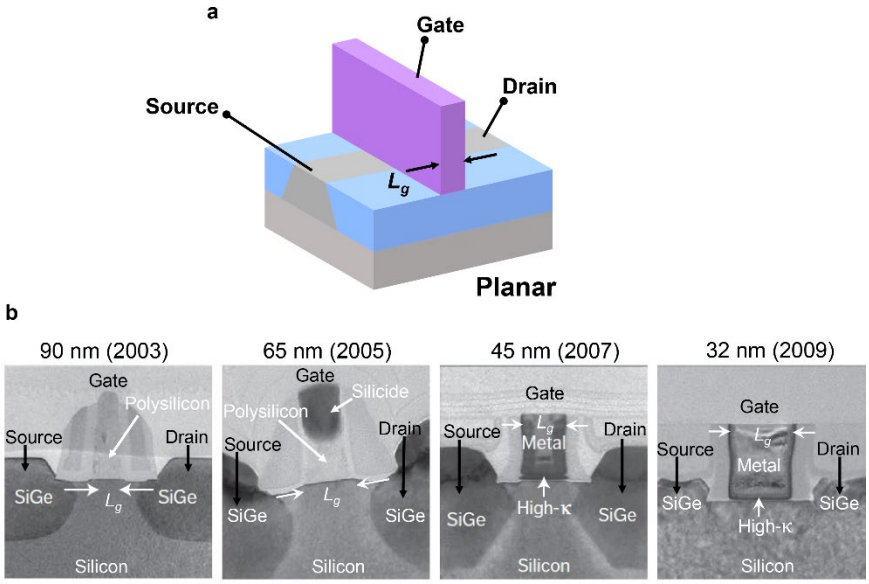


Fig. 1. (a) Schematic of the classic planar MOSFET and (b) its evolution. Adapted with permission from Bohr and Young.[20]

3D FinFET: 25-3 nm Nodes. The three-dimensional structured FinFET is a novel design and represents a significant technological advance, offering clear advantages over the planar case. As depicted in Fig. 2a, the FinFET has a vertical, thin Si fin extending above the substrate, allowing the gate to wrap around three sides of the fin. Compared with the conventional planar MOSFET, the FinFET gate controls the channel from multiple directions, thereby reducing current leakage and suppressing short-channel effects by exerting stronger electrostatic control, which enables continued transistor scaling.

The FinFET was first demonstrated by Chenming Hu's group[3, 21] in 1999, and it has been seriously considered for industrial production since 2004. The first mass production of a 22-nm node using FinFETs was achieved by Intel in 2011 (see Fig. 2b)[20], and other major foundries, such as TSMC and Samsung, have since adopted the technology. Although the concept of this design was proposed more than two decades ago, it has proven effective, enabling transistor technology nodes to scale down to 3 nm. However, as we enter a new era of technology, FinFETs face increasing challenges in scaling further, particularly at nodes below 3 nm. The drawbacks of FinFETs, such as width quantization, interference with interconnect layers, and current leakage from the bottom channel, pose challenges for continued scaling.[7] As such, a more advanced design that wraps the gate around all sides, called the gate-all-around (GAA) structure, has become a key solution for the next technology generation beyond 3-nm nodes because it provides much better electrostatic control without suffering the limitations of FinFETs.

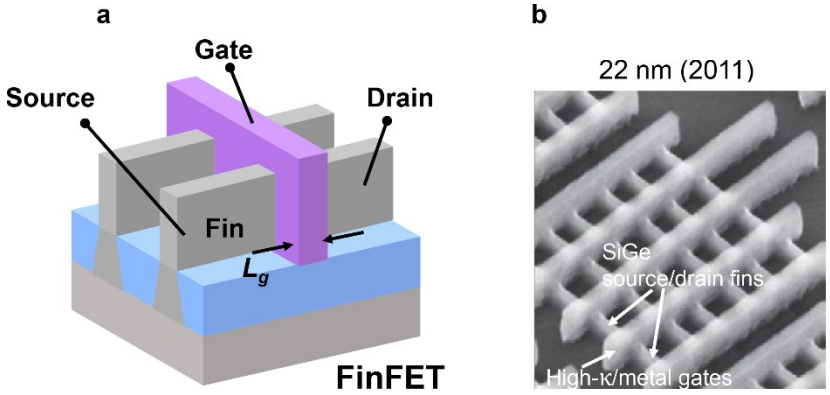


Fig. 2. Schematic of (a) a double-gate FinFET and (b) the first commercial tri-gate FinFET at the 22-nm node. Adapted with permission from Bohr and Young.[20]

CONCEPT OF IDEAL MOSFET: BEYOND 3 NM NODES

Structures. The concept of the ideal MOSFET was formulated and proposed by the International Technology Roadmap for Semiconductors (ITRS) back in 1998, which further noted that improvements in materials and device architectures are as crucial as geometric shrinking for continued technological scaling (i.e., "equivalent scaling").[22, 23] This has subsequently stimulated the development of new technologies, such as the aforementioned channel strain engineering and HKMG, but the invention of the FinFET, a key innovation in device structure, has played the most important role in sustaining Moore's Law through the 3-nm node. Furthermore, progress toward

the ideal MOSFET continues with the introduction of a novel gate-all-around device architecture for nodes below 3 nm.

As depicted in Fig. 3, the most critical feature of the ideal MOSFET is a gate wrapping around all sides of the channel (i.e., gate-all-around), in contrast to planar and FinFET devices, in which the channel is only partially enclosed by the gate. Other aspects of the ideal MOSFET include a metal gate, a high-*k* gate insulator, and low-resistance source/drain contacts. To achieve this ideal concept, the most important development was to incorporate semiconductor nanowires (NWs) into devices, since they enable a fully surrounding-gate structure and can support high-density circuits,[24, 25] making them essential building blocks for the next era of transistor technology. Although GAA nanosheet and nanoribbon transistors were proposed later,[26-29] they can be regarded as extensions of earlier nanowire architectures. Since nanosheets and nanoribbons are essentially a wider, laterally expanded version of nanowires, we will use the term "GAA nanowire" to represent both nanowire-, nanosheet-, and nanoribbon-based GAA transistors for brevity. Therefore, the gate-all-around nanowire (GAANW) transistor is the most realistic CMOS device architecture used today for technology nodes below 3 nm and represents one of the most significant advances toward realizing the ideal MOSFET proposed more than two decades ago.

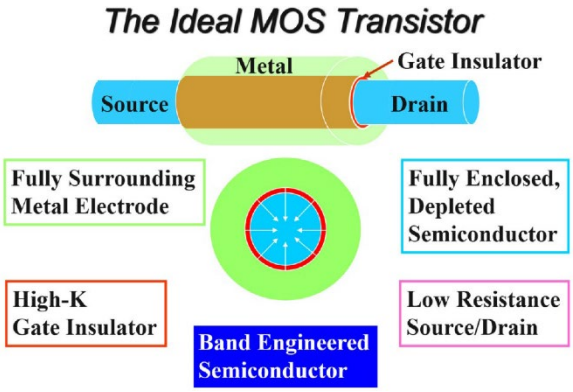


Fig. 3. The ideal MOSFET proposed in the 1998 ITRS. Reproduced from ref. 23, Applied Sciences, © 2021, Gargini et al., licensed under CC BY 4.0.

Key Performance and Advantages. GAANW transistors exhibit superior performance compared to FinFETs. The key difference between GAANW transistors and FinFETs lies in their device geometry, which, in turn, results in distinct electrical properties and overall performance. Because all sides of the channel are enclosed by the gate, the GAANW design provides an unprecedented level of electrostatic control.[30] As such, it can further suppress short-channel effects, reduce current leakage, and enable a lower threshold voltage. For instance, compared to the FinFET, the GAANW transistor has shown reduced off-current and an enhanced subthreshold slope, which can ultimately enable faster switching between the on and off states and lower power consumption in the devices.[31]

From a practical standpoint, the scalability of sub-3 nm nodes is a significant advantage of the GAA transistor architecture. The number and size of the NWs can be adjusted accordingly to achieve smaller nodes without the geometric limitations, unlike FinFETs, where the fin width and height can be restricted.[7, 26] This is also key to precisely controlling the transistor's power and performance, thereby enabling solutions for a range of applications, from low-power mobile devices to high-performance computing processors, which are not possible with FinFETs. In

addition, the GAA design enables the growth of multiple devices along the vertical direction, thereby achieving higher transistor density per unit area. For example, previous work has demonstrated that multiple nanowires can be vertically stacked and provide much larger drive current within the same footprint, marking a major advance in sub-3 nm scaling.[26] All of these benefits have led the industry to consider using GAANW transistors for nodes below 3 nm. More importantly, large improvements in the device performance using GAANW structures have already been reported by the big three semiconductor foundries, namely Samsung, Intel, and TSMC, with the details explained in a later section on industry adoption.

Fabrication Challenges. To realize GAANW architectures, a key challenge is to grow high-quality NWs, which are the core components of GAA transistors. NWs are difficult to fabricate because they typically require highly precise processes and advanced control. In the early 2000s, traditional top-down methods faced challenges in fabricating NWs because they relied heavily on Deep Ultraviolet (DUV) light sources, which had a limited resolution of 193 nm, as noted in the 2001 ITRS.[22] To address this, researchers initially employed bottom-up approaches to fabricate GAANW transistors, enabling precise control of the NWs' size and orientation.[32] Bottom-up techniques have often been used first for proof-of-concept devices, as they generally achieve higher resolution in at least one critical dimension than standard lithography processes,[32] thereby enabling future commercialization via top-down fabrication methods. Therefore, we will focus on discussing GAANW transistors fabricated through bottom-up techniques in the early 2000s.

The most well-established method for synthesizing bottom-up nanowires is relatively straightforward and based on the conventional catalyzed vapor-liquid-solid (VLS) process. After Wagner and Ellis successfully grew silicon whiskers using VLS with an Au catalyst,[33] the VLS mechanism has been adopted and further developed to produce various types of nanowires since the early 2000s, with early contributions from researchers such as the groups of Lieber,[34] Yang,[35] and Samuelson.[36] While the growth of Si, Ge, and other III-V nanowires, as well as nanowire heterostructures, using the bottom-up method has been reported since then,[37-40] several early studies have focused on incorporating these nanowires into transistor devices.[41-43] These nanowire-based transistors have either bottom- or top-gate configurations, in which the nanowire is not fully enclosed by the gate. Nanowire-based transistors with a top-gate geometry are often referred to as omega-gate transistors, as the gate shape resembles the Greek letter Omega,[44] and they represent the closest structures to the GAA case in the early stages of development. The fabrication of GAANW transistors was thus a significant challenge in the late 1990s and early 2000s. As such, it's essential to summarize their historical development, and especially to show how they evolved from conceptual ideas to laboratory demonstrations, and were eventually adopted by the industry. Such a transition is described in detail in the following section.

HISTORICAL DEVELOPMENT OF GAANW TRANSISTORS

Early Conceptual Ideas (before 2000). The first attempt to achieve a GAA transistor was made by a team from Toshiba in 1988,[45] who fabricated a vertical pillar silicon island surrounded by a poly-Si gate. The pillar silicon island had a width of 4 μm and a length of 0.8 μm and was defined by using the conventional top-down method. Two years later, instead of fabricating a vertical structure, an IMEC team[46] adopted an alternative orientation of the silicon island, yielding a horizontal GAA transistor. They first defined a silicon active region with a length and width of 3 μm by creating a cavity beneath the center of the silicon island using conventional lithography-

based wet etching. A poly-Si gate material was then grown on all sides of the suspended silicon to form a surrounding gate. Both Toshiba's and IMEC's vertical and horizontal designs have reported improved performance than their planar counterparts, including smaller threshold slopes by using GAA structures through better electrostatic control. Still, they are not suitable for industrial applications due to limitations, including non-metallic gates and, more importantly, relatively large micro-sized silicon source/strain structures that hinder scalability. Smaller structures, specifically NWs, are the key to realizing high-density GAA transistors and thus play the most important role in advancing current semiconductor technology to nodes below 3 nm as aforementioned.

Despite the limitations of prior GAA designs, the ITRS proposed the ideal MOS transistor with the GAANW architecture and urged its further development in 1998,[22, 23] as discussed in the previous section. Although such a metal GAA structure was predicted to eventually dominate semiconductor technology, it was uncertain at the time how to realize it or whether it would function properly. This has thus required substantial work from both university research and industry to advance the concept and implement it in the next era of technology. These efforts, along with their timelines, are discussed below.

Laboratory Demonstrations (2006-). Although the microelectronics industry has recognized since 1998 that the GAANW design concept could enable more energy-efficient transistors with improved performance at extremely small scales below 3 nm, initial challenges in traditional top-down lithography, such as limited resolution,[22] have hindered their fabrication and early development. As aforementioned, bottom-up approaches can be used to initially validate device concepts before large-scale integration since they offer molecular-level control of material composition and structure, as well as providing insights into intrinsic material properties including quantum effects, metal-semiconductor interface contact resistance at the source and drain, and ultimate scaling and performance limits, thereby enabling the discovery of novel architectures and materials, such as 2D semiconductors (e.g., graphene and MoS_2), for future transistor technologies.[38, 47-49] With rapid progress in bottom-up nanowire synthesis beginning in the early 2000s, nanowire-based transistors have been increasingly fabricated to explore their electrical properties. The nanowire-based transistors reported in early work typically had a horizontal layout with either a back or a top-gate geometry,[41-43, 50, 51] and thus were not GAA devices.

The first prototype of GAANW transistor was realized by Goldberger et al. from the Yang group at UC Berkeley in 2006, published in Nano Lett.[24] In this work, they fabricated vertical silicon nanowire GAA transistors (see Fig. 4) primarily using the bottom-up VLS epitaxial growth mechanism in a chemical vapor deposition (CVD) reactor. Specifically, vertical silicon nanowires were first grown by CVD using an Au catalyst, and subsequent thermal oxidation produced high-aspect-ratio structures with channel lengths of 1.0-1.5 μm and diameters as small as sub-5 nm, which are challenging to achieve via conventional top-down lithography. Then, the silicon nanowires were coated with an ultrathin Cr metal gate and embedded in silicon dioxide. Finally, 70 μm^2 Ni drain contact pads were defined, each covering 8-269 nanowires, demonstrating the feasibility of high-density circuits built on nanowires. While these vertical GAANW devices were first-generation and not yet optimized, they already showed promising performance comparable to that of standard transistors at the time. Although ZnO and CuSCN vertical nanowire transistors were also demonstrated at a similar timeframe,[52, 53] Goldberger et al.'s work is particularly

important because Si is more relevant to industrial applications. Therefore, this work has shed light on transistor development by validating the GAANW concept at the laboratory scale for the first time. In addition, an IBM team[54] and Bryllert et al.[55] from the Samuelson group both reported a conceptually similar nanowire device (see Fig. 5) around the same time as Goldberger et al. Specifically, the IBM team fabricated vertical wrap-gated transistors consisting of 10^4-10^5 silicon nanowires with 400-nm lengths and 40-nm diameters, while the Samuelson group characterized gate-all-around devices comprising 120 indium arsenide nanowires with 4-μm lengths and 80-nm diameters. Both devices demonstrated promising performance, further supporting the GAANW concept. Subsequently, numerous studies on bottom-up GAANW transistors have followed,[56-63] culminating in industry adoption.

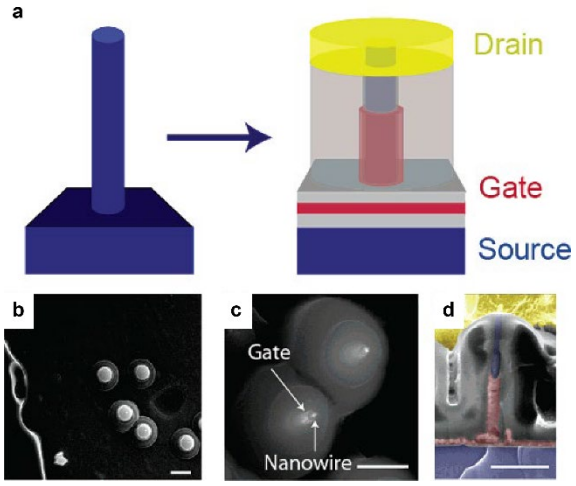


Fig. 4. First GAANW transistor prototype, developed by the Yang group at UC Berkeley in 2006. The scale bars are 2 μm, 1 μm, and 500 nm for b, c, and d, respectively. Reproduced with permission from Goldberger et al.[24]

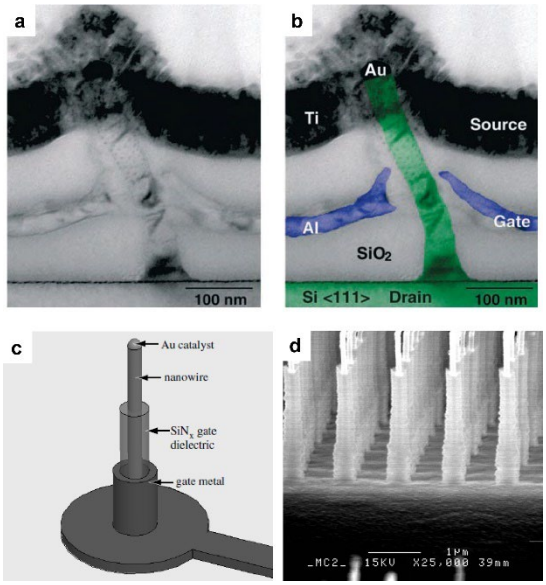


Fig. 5. (a, b) 40-nm silicon and (c, d) 80-nm InAs nanowire GAA transistors proposed by the IBM team[54] and the Samuelson[55] group, respectively. Reproduced with permission from Schmidt et al.[54] and Bryllert et al.[55]

Industry Adoption (2025-). Commercial GAANW transistors are now being produced by the semiconductor industry using top-down methods, building on earlier laboratory demonstrations of bottom-up concepts. Top-down fabrication is used by the industry because bottom-up techniques are not yet compatible with current CMOS processes for large-scale, commercial production due to their limitations in nanowire density, transfer, alignment, and uniformity.[64, 65]

Samsung announced the industry's first production using a GAANW structure in mid-2022.[66] The company's 3-nm MBCFET (Multi Bridge Channel FET) technology (see Fig. 6), based on the GAANW architecture, enabled unprecedented device performance. For instance, Samsung's 3 nm node based on GAANW transistors can reduce power consumption by 34%, improve performance by 22%, and reduce area by 21%, compared with its previous 4 nm process with FinFET technology.[66]

Intel has its own design of GAANW transistors. They initially called it 20A in 2021 and later renamed it 18A, which they previously expected to enter risk production in 2025, with improvements ongoing.[67] The 18A node showed up to 25% higher iso-power performance and 30% greater transistor density scaling compared to their previous FinFETs.[67] It's also worth noting that Intel incorporated a technology called PowerVia in its 18A node, making it the industry's first to implement a backside power delivery method to optimize performance.[67]

While TSMC pushed FinFET technology to its limits for use in their current 3 nm node, they recognized the early proof-of-concept silicon nanowire devices from the Yang group in 2014[44] and are now implementing GAANW transistors in their next N2 technology at the 2 nm node. For instance, TSMC announced its plans to mass-produce the 2 nm node based on GAANW transistors in 2026.[28] Similarly, their N2 technology demonstrated up to 15% higher performance and 30% lower power consumption than their previous N3 technology, which was based on FinFETs.[68] It's also worth noting that TSMC theoretically realized a 1 nm GAA tin nanowire transistor with well-behaved electrical characteristics due to a metal-to-semiconductor transition in 2014,[44] demonstrating the promising scalability of GAA-based structures, as shown in Fig. 7.

Besides the big three foundries, other research organizations, such as IBM and IMEC, further developed the GAA concept by employing a vertically stacked nanowire architecture,[26, 69] enabling faster industry adoption of the technology. For instance, Rapidus mentioned their partnership with IBM to develop their own 2 nm node, with mass production targeted for 2027.[70] Their 2 nm process was built on their early work on stacked nanosheet GAA devices.[26]

Typically, industrial GAANW transistors consist of multiple nanosheets with widths of ~8-24 nm and gate lengths of ~14 nm.[71] In these industrial devices, the gate length is smaller, while the channel width is comparable to the diameter of previously bottom-up synthesized nanowires (e.g., channel diameter ~5 nm, as reported by Goldberger et al.).[24, 54, 55] While industry is now implementing GAANW transistors through traditional top-down lithography, the Yang group and the IBM team fabricated the first prototype bottom-up silicon nanowire device[24, 54] by creating

these complex structures using chemical synthesis. It confirmed the concept nearly 20 years ago.[72] Despite using different names, the semiconductor industry is entering a new era with GAANW transistors for technology nodes below 3 nm, beginning in 2025.

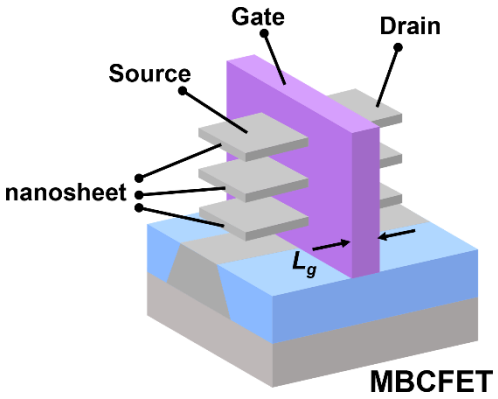


Fig. 6. Schematic of MBCFET technology, as discussed, for example, in Jeong et al.[66]

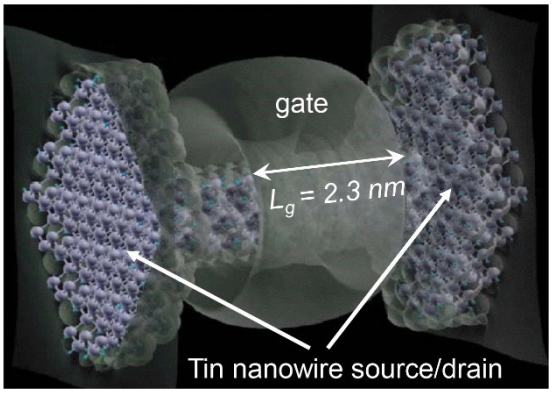


Fig. 7. A 1 nm tin GAANW transistor proposed by TSMC in 2014. Adapted with permission from Colinge et al.[44]

FUTURE EVOLUTION AND PERSPECTIVE: THE ANGSTROM ERA

Technology Roadmaps from the Big Three Foundries. Currently, the big three foundries are shifting from FinFETs to GAANW transistors to accelerate technology node scaling, although their timelines differ slightly. GAANW devices are now in mass production at 2 nm nodes and are expected to begin delivering in 2025/2026, after which they will be fully adopted. In addition, according to their roadmaps,[73-75] the big three foundries are now all heading in the same direction and aim to use GAA architectures to advance nodes down to 1.4 nm by 2028. While GAA transistor technology is powerful and shows improved device performance, there are still many improvements that need to be made for the next phase of Moore's Law – the Angstrom Era.

Future Technology Node and Challenges. The current technology node does not refer to any critical dimensions of the device; rather, it is used by industry to describe its technology generation. The GMT method, which accounts for contacted gate pitch, metal pitch, and number of tiers, is

typically used to characterize current technology nodes. The contacted gate pitch and metal pitch, respectively, represent the minimum distances between two transistors' gates and between two horizontal interconnects, while the number of tiers denotes the number of vertically stacked layers of transistors in an integrated circuit.[4] For instance, the 3 nm node equates to a 16-18 nm gate length, a 48 nm gate pitch, and a 24-32 nm metal pitch. It typically has a single layer of transistors, according to the IEEE International Roadmap for Devices and Systems (IRDS),[5] the successor to the ITRS. As we are about to enter the 2-nm era, it was further expected that the technology node would be scaled down to ~1 nm by 2028 (see Fig. 8).[4] Afterwards, we will be moving to an unprecedented generation era, the Angstrom Era, which will be full of uncertainties and challenges. Fabricating sub-1 nm nodes is not trivial, as we will reach lithography-limited dimensions at that point.[4]

As shown in Fig. 8, some potential solutions for further scaling are presented, as highlighted in IMEC's roadmap.[76] Current silicon CMOS technology employs a single transistor layer, with transistors connected to circuits via more than a dozen metal interconnect layers, resulting in limited transistor density.[4] Therefore, researchers have developed multiple layers of n- and p-type GAA transistors stacked on an integrated circuit. Such multilayer structures are generally referred to as complementary FETs (CFETs) and can enable larger transistor densities (e.g., several billion transistors per square millimeter can be realized with CFETs[7]). Although CFETs are expected to take over in the next phase of development, they are projected to operate for only another 10 years, as specified in the roadmap.

Beyond that, more advanced technologies employing sophisticated fabrication processes and innovative materials will be necessary to sustain Moore's Law. The fabrication processes for future transistors are complicated, as they involve many steps, including multiple thin-layer depositions, lithography, etching, doping, and planarization.[77] Each of these steps is crucial to realizing scaled-down devices. As device dimensions shrink, it becomes increasingly difficult to control their critical feature sizes and minimize variability.[77] In addition, integrating novel materials such as high-*k* dielectrics, metal gates, and emerging channel materials faces issues with thermal stability, interface quality, material defects, and process compatibility.[78-80] Consequently, manufacturing high-yield devices at production scale involves substantial technical difficulties.[81, 82] Nevertheless, these challenges are expected to be addressed through various strategies. For instance, according to the IRDS,[83] current Extreme Ultraviolet (EUV) systems will transition to high-numerical-aperture (High-NA) and hyper-numerical-aperture (Hyper-NA) EUV in the future to achieve better lithography resolution and support continued transistor scaling. Furthermore, novel materials, such as 2D semiconductors,[48, 49, 84-89] could drive future evolution, although large-scale, high-quality synthesis remains challenging.[90, 91] Other emerging materials, such as III-V compounds (e.g., InAs and InGaAs),[55, 58, 59, 92, 93] 1D Van der Waals crystals,[94, 95] carbon nanotubes,[96, 97] and quantum dots,[98-100] may also be used to fabricate ultrasmall transistors; however, they remain at the laboratory scale and require further development. Thus, it will require researchers and scientists from industry and academia to lead future breakthroughs in semiconductor technology to realize the Angstrom Era.

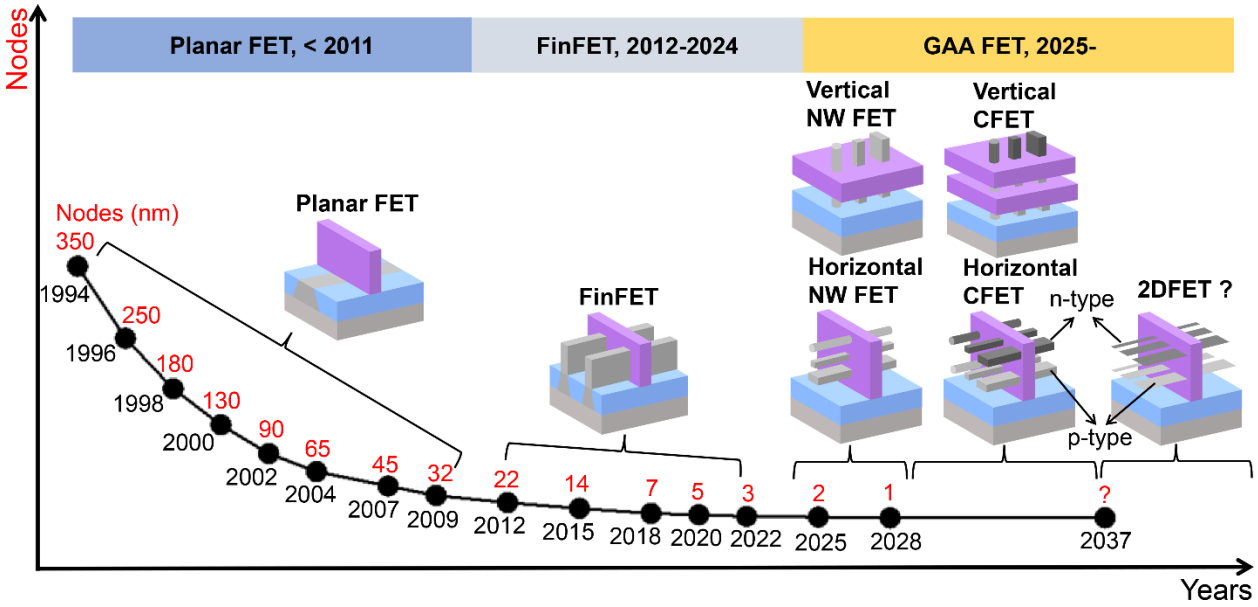


Fig. 8. The evolution of future technology nodes and a potential technological roadmap. Device structures evolve from planar to FinFET and GAA transistors, with corresponding evolution of channel materials from Si/SiGe to 2D materials and fabrication technology from DUV to High-NA/Hyper-NA EUV lithography.[4, 76, 83]

The technology nodes were scaled down from nearly a hundred nanometers to a few nanometers over the past two decades. These accomplishments were primarily due to rapid advances in device architectures, transitioning from 2D planar to fin- and, eventually, GAA-based structures. The first radical shift occurred in 2011 when the FinFET, developed by Chenming Hu's group,[3, 21] was commercialized at the 22-nm node by Intel.[20] The FinFET has clearly demonstrated better electrostatic control and lower power consumption than conventional planar transistors, thereby enabling its use down to 3 nm nodes.

Although powerful, FinFETs have reached the limit of further scaling. With the channel being entirely surrounded by the gate, GAA transistors can further suppress short-channel effects through superior electrostatic control, ultimately allowing nodes below 3 nm with enhanced performance. While the industry planned to mass-produce 2-nm nodes using GAANW transistors via traditional top-down lithography in 2025, marking another major shift, the Yang group demonstrated the potential of this concept by employing an unconventional bottom-up approach to fabricate these complex structures nearly 20 years ago.[24, 72]

Looking ahead, the implementation of GAANW transistors will eventually lead us to the next generation, the Angstrom Era. CFETs are improved GAA structures comprising multiple layers of n- and p-type GAA transistors stacked on top of one another. They were expected to play an important role in this era and support semiconductor technology for at least ten years. The microelectronics industry also recognized that innovative materials, such as 2D semiconductors, may be essential for the future evolution of technological nodes. However, these emerging materials still face challenges in high-quality synthesis and large-scale production, which must be addressed to enable further development. Despite these challenges, we anticipate that

semiconductor technology will continue to evolve toward even denser, more energy-efficient transistor architectures through future contributions from both industry and academic research investigating new materials. For example, the 2D material MoS_2 has already been explored and demonstrated as a promising candidate for future ultra-small technology nodes by the semiconductor industry, such as Samsung, Intel, TSMC, and IMEC.[84-87] Similar studies have also been conducted in academic research.[48, 49, 88, 89] Due to these combined efforts, this field is expected to continue expanding and evolving for transistor downscaling. Other emerging materials, such as III-V compounds (e.g., InAs and InGaAs),[58, 58, 59, 92, 93] 1D Van der Waals crystals,[94, 95] carbon nanotubes,[96, 97] and quantum dots,[98-100] might play an important role in the fabrication of next-generation ultra-small transistors as well. Therefore, further improvements in the synthesis and large-scale integration of such materials are also likely to enable continued transistor scaling.

AUTHOR INFORMATION

Corresponding Author

Peidong Yang – *Department of Chemistry and Department of Materials Science and Engineering, University of California, Berkeley, California 94720, United States; Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States; Kavli Energy Nano Science Institute, Berkeley, California 94720, United States;* orcid.org/0000-0003-4799-1684; Email: p_yang@berkeley.edu

Author

Lei Tang – *Department of Chemistry, University of California, Berkeley, California 94720, United States;* orcid.org/0000-0003-3796-1174

Notes

The authors declare no competing financial interest

ACKNOWLEDGMENTS

This work was primarily supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, Materials Sciences and Engineering Division, under contract DE-AC02-05-CH11231 within the Nanowire Fundamentals Program (KCPY23).

References:

(1) Hu, C. MOSFETs in ICs—Scaling, leakage, and other topics. *Modern Semiconductor Devices for Integrated Circuits*, 1st ed. New York, NY, USA: Pearson, **2009,** pp. 263–269.

(2) Sze, S. M.; Li, Y.; Ng, K. K. Physics of Semiconductor Devices; John Wiley & Sons, 2021.

(3) Hisamoto, D.; Lee, W.C.; Kedzierski, J.; Takeuchi, H.; Asano, K.; Kuo, C.; Anderson, E.; King, T.J.; Bokor, J.; Hu, C. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Transactions on Electron Devices* **2000,** *47*(12), 2320-2325.

(4) Moore, S. K. The node is nonsense. *IEEE Spectrum* **2020,** *57*(8), 24-30.

(5) More Moore: Technology requirements — logic technologies. *IEEE International Roadmap for Devices and Systems*, 2024.

(6) Cao, W.; Bu, H.; Vinet, M.; Cao, M.; Takagi, S.; Hwang, S.; Ghani, T.; Banerjee, K. The future transistors. *Nature* **2023,** *620*(7974), 501-515.

(7) Kalinin, S. V.; Ostertak, D. I.; Poteryaev, D. A.; Kuznetsov, M. A. A new revolution in logic silicon IC technology: GAA FETs are replacing FinFETs. In *2023 IEEE XVI International Scientific and Technical Conference Actual Problems of Electronic Instrument Engineering* **2023,** 160-165.

(8) Zhang, Q.; Zhang, Y.; Luo, Y.; Yin, H. New structure transistors for advanced technology node CMOS ICs. *National Science Review* **2024,** *11*(3), nwae008.

(9) Soma, U. Transistor Evolution: A Comprehensive Overview from TFT to TFET and Beyond. *Proceedings of the National Academy of Sciences, India Section A: Physical Sciences* **2025,** *95*(2), 113-125.

(10) Thapaswini, P.P. Gate-all-around structures for low-power applications. In *2D Nanomaterials and Devices for Flexible Electronics* **2026,** 258-294, CRC Press.

(11) Yan, R.H.; Ourmazd, A.; Lee, K.F. Scaling the Si MOSFET: From bulk to SOI to bulk. *IEEE Transactions on Electron Devices* **2002,** *39*(7), 1704-1710.

(12) Ieong, M.; Doris, B.; Kedzierski, J.; Rim, K.; Yang, M. Silicon device scaling to the sub-10-nm regime. *Science* **2004,** *306*(5704), 2057-2060.

(13) Taur, Y.; Ning, T. H. Fundamentals of Modern VLSI Devices. Cambridge University Press: Cambrige, UK, 2021.

(14) Atalla, M.; Kahng, D. Silicon-silicon dioxide field induced surface devices. *IRE-AIEE Solid State Device Research Conference*, Pittsburgh, PA, June 1960.

(15) Dennard, R. H.; Gaensslen, F. H.; Yu, H. N.; Rideout, V. L.; Bassous, E.; LeBlanc, A. R. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE J. Solid State Circuits* **1974,** *9*(5), 256-268.

(16) Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; McIntyre, B. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In *IEEE International Electron Devices Meeting* **2003,** 978–980 (IEEE, 2003).

(17) Tyagi, S.; Auth, C.; Bai, P.; Curello, G.; Deshpande, H.; Gannavaram, S.; Golonzka, O.; Heussner, R.; James, R.; Kenyon, C.; Lee, S.H. An advanced low power, high performance, strained channel 65nm technology. *IEEE Int. Electron Devices Meet. Tech. Digest* **2005,** 245–247.

(18) Mistry, K.; Allen, C.; Auth, C.; Beattie, B.; Bergstrom, D.; Bost, M.; Brazier, M.; Buehler, M.; Cappellani, A.; Chau, R.; Choi, C.H. A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging. In *IEEE International Electron Devices Meeting* **2007,** 247–250.

(19) Jan, C.H.; Agostinelli, M.; Buehler, M.; Chen, Z.P.; Choi, S.J.; Curello, G.; Deshpande, H.; Gannavaram, S.; Hafez, W.; Jalan, U.; Kang, M. A 32nm SoC platform technology with 2 nd generation high-k/metal gate transistors optimized for ultra low power, high performance, and high density product applications. In *IEEE International Electron Devices Meeting* **2009,** 1-4.

(20) Bohr, M. T.; Young, I. A. CMOS scaling trends and beyond. *IEEE Micro* **2017,** *37*(6), 20-29.

(21) Huang, X.; Lee, W.-C.; Kuo, C.; Hisamoto, D.; Chang, L.; Kedzierski, J.; Anderson, E.; Takeuchi, H.; Choi, Y.-K.; Asano, K., , et al. Sub 50-nm FinFET: PMOS, In *1999 IEEE International Electron Devices Meeting (IEDM)*, 5–8 Dec. 1999; IEEE: Washington, DC, USA, 1999; pp 67– 70.

(22) International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: https://www.itrs2.org/

(23) Gargini, P.; Balestra, F.; Hayashi, Y. Roadmapping of nanoelectronics for the new electronics industry. *Applied Sciences* **2021,** *12*(1), 308.

(24) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. Silicon vertically integrated nanowire field effect transistors. *Nano Letters* **2006,** *6*(5), 973-977.

(25) Beckman, R.; Johnston-Halperin, E.; Luo, Y.; Green, J. E.; Heath, J. R. Bridging dimensions: Demultiplexing ultrahigh-density nanowire circuits. *Science* **2005,** *310*(5747), 465-468.

(26) Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.W.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J.; Young, A., , et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In *2017 Symposium on VLSI Technology* **2017,** T230-T231.

(27) Bae, G.; Bae, D.I.; Kang, M.; Hwang, S.M.; Kim, S.S.; Seo, B.; Kwon, T.Y.; Lee, T.J.; Moon, C.; Choi, Y.M.; Oikawa, K., , et al. 3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications. In *2018 IEEE International Electron Devices Meeting (IEDM)* **2018,** 28-7.

(28) Yeap, G.; Lin, S.S.; Shang, H.L.; Lin, H.C.; Peng, Y.C.; Wang, M.; Wang, P.W.; Lin, C.P.; Yu, K.F.; Lee, W.Y.; Chen, H.K., , et al. 2nm Platform Technology featuring Energy-efficient Nanosheet Transistors and Interconnects co-optimized with 3DIC for AI, HPC and Mobile SoC Applications. In *2024 IEEE International Electron Devices Meeting (IEDM)* **2024,** 1-4.

(29) Wang, X.; Kim, Y.; Baek, G.H.; Bannore, K.G.; Dave, K.; Joushaghani, A.; Kang, N.; Ko, M.; Pillai, A.M.; Movva, H.C.P.; Park, G., , et al. 29.2 A 0.021μm^2 High-Density SRAM in Intel-18A-RibbonFET Technology with PowerVia-Backside Power Delivery. In *2025 IEEE International Solid-State Circuits Conference (ISSCC)* **2025,** 68, 494-496.

(30) Colinge, J. P. In *FinFETs and Other Multi-Gate Transistors*; Colinge, J. P., Ed. Springer: New York, 2008; p 14.

(31) Nagy, D.; Indalecio, G.; Garcia-Loureiro, A. J.; Elmessary, M. A.; Kalna, K.; Seoane, N. FinFET versus gate-all-around nanowire FET: performance, scaling, and variability. *IEEE Journal of the Electron Devices Society* **2018,** *6*, 332-340.

(32) Lu, W.; Xie, P.; Lieber, C. M. Nanowire transistor performance limits and applications. *IEEE Transactions on Electron Devices* **2008,** *55*(11), 2859-2876.

(33) Wagner, R. S.; Ellis, W. C. Vapor-liquid-solid mechanism of single crystal growth. *Applied Physics Letters* **1964,** *4*(5), 89-90.

(34) Lu, W.; Lieber, C. M. Semiconductor nanowires. *Journal of Physics D: Applied Physics* **2006,** *39*(21), R387.

(35) Yang, P. 30 years of semiconductor nanowire research: A Personal Journey. *Israel Journal of Chemistry* **2025,** *65*(2).

(36) Samuelson, L.; Thelander, C.; Björk, M.T.; Borgström, M.; Deppert, K.; Dick, K.A.; Hansen, A.E.; Mårtensson, T.; Panev, N.; Persson, A.I.; Seifert, W., , et al. Semiconductor nanowires for 0D and 1D physics and applications. *Physica E: Low-dimensional Systems and Nanostructures* **2004,** *25*(2-3), 313-318.

(37) Lauhon, L. J.; Gudiksen, M. S.; Lieber, C. M. Semiconductor nanowire heterostructures. *Philosophical Transactions of the Royal Society of London. Series A: Mathematical, Physical and Engineering Sciences* **2004,** *362*(1819), 1247-1260.

(38) Zhang, A.; Zheng, G.; Lieber, C.M. Emergence of nanowires. In *Nanowires: Building Blocks for Nanoscience and Nanotechnology Cham: Springer International Publishing* **2016,** 1-13.

(39) Yang, P.; Yan, R.; Fardy, M. Semiconductor nanowire: what's next?. *Nano Letters* **2010,** *10*(5), 1529-1536.

(40) Yang, P. Semiconductor nanowire, what's next II?. *Next Materials* **2023,** *1*(2), 100014.

(41) Cui, Y.; Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **2001,** *291*(5505), 851-853.

(42) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. High performance silicon nanowire field effect transistors. *Nano Letters* 2003, *3*(2), 149-152.

(43) Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. High-performance thin-film transistors using semiconductor nanowires and nanoribbons. *Nature* **2003,** *425*(6955), 274-278.

(44) Colinge, J. P. Multigate transistors: pushing Moore's law to the limit. In *2014 International Conference on Simulation of Semiconductor Processes and Devices* **2014,** 313-316.

(45) Takato, H.; Sunouchi, K.; Okabe, N.; Nitayama, A.; Hieda, K.; Horiguchi, F.; Masuoka, F. High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs. In *Technical Digest., International Electron Devices Meeting* **1988,** 222-225.

(46) Colinge, J. P.; Gao, M. H.; Romano-Rodriguez, A.; Maes, H.; Claeys, C. Silicon-on-insulator'gate-all-around device'. In *International Technical Digest on Electron Devices* **1990,** 595-598.

(47) Lu, W.; Lieber, C.M. Nanoelectronics from the bottom up. *Nature Materials* **2007,** *6*(11), 841-850.

(48) Liu, Y.; Duan, X.; Huang, Y.; Duan, X. Two-dimensional transistors beyond graphene and TMDCs. *Chemical Society Reviews* **2018,** *47*(16), 6388-6409.

(49) Dai, C.; Liu, Y.; Wei, D. Two-dimensional field-effect transistor sensors: the road toward commercialization. *Chemical Reviews* **2022,** *122*(11), 10319-10392.

(50) Wang, D.; Chang, Y. L.; Wang, Q.; Cao, J.; Farmer, D. B.; Gordon, R. G.; Dai, H. Surface chemistry and electrical properties of germanium nanowires. *Journal of the American Chemical Society* **2004,** *126*(37), 11602-11611.

(51) Goldberger, J.; Sirbuly, D. J.; Law, M.; Yang, P. ZnO nanowire transistors. *The Journal of Physical Chemistry B* **2005,** *109*(1), 9-14.

(52) Chen, J.; Klaumünzer, S.; Lux-Steiner, M. C.; Könenkamp, R. Vertical nanowire transistors with low leakage current. *Applied Physics Letters* **2004,** *85*(8), 1401-1403.

(53) Ng, H. T.; Han, J.; Yamada, T.; Nguyen, P.; Chen, Y. P.; Meyyappan, M. Single crystal nanowire vertical surround-gate field-effect transistor. *Nano Letters* **2004,** *4*(7), 1247-1252.

(54) Schmidt, V.; Riel, H.; Senz, S.; Karg, S.; Riess, W.; Gösele, U. Realization of a silicon nanowire vertical surround-gate field-effect transistor. *Small* **2006,** *2*(1), 85-88.

(55) Bryllert, T.; Wernersson, L. E.; Löwgren, T.; Samuelson, L. Vertical wrap-gated nanowire transistors. *Nanotechnology* **2006,** *17*(11), S227.

(56) Zhang, L.; Tu, R.; Dai, H. Parallel core− shell metal-dielectric-semiconductor germanium nanowires for high-current surround-gate field-effect transistors. *Nano Letters* **2006,** *6*(12), 2785-2789.

(57) Rosaz, G.; Salem, B.; Pauc, N.; Potié, A.; Gentile, P.; Baron, T. Vertically integrated silicon-germanium nanowire field-effect transistor. *Applied Physics Letters* **2011,** *99*(19).

(58) Tomioka, K.; Yoshimura, M.; Fukui, T. A III–V nanowire channel on silicon for high-performance vertical transistors. *Nature* **2012,** *488*(7410), 189-192.

(59) Storm, K.; Nylund, G.; Samuelson, L.; Micolich, A. P. Realizing lateral wrap-gated nanowire FETs: controlling gate length with chemistry rather than lithography. *Nano Letters* **2012,** *12*(1), 1-6.

(60) Lee, J. H.; Kim, B. S.; Choi, S. H.; Jang, Y.; Hwang, S. W.; Whang, D. A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope. *Nanoscale* **2013,** *5*(19), 8968-8972.

(61) Oh, J. Y.; Park, J. T.; Jang, H. J.; Cho, W. J.; Islam, M. S. 3D-transistor array based on horizontally suspended silicon nano-bridges grown via a bottom-up technique. *Adv. Mater.* **2014,** *26*(12), 1929-1934.

(62) Chen, L.; Cai, F.; Otuonye, U.; Lu, W. D. Vertical Ge/Si core/shell nanowire junctionless transistor. *Nano Letters* **2016,** *16*(1), 420-426.

(63) Liao, W.; Qian, W.; An, J.; Liang, L.; Hu, Z.; Wang, J.; Yu, L. High-Performance Gate-All-Around Field Effect Transistors Based on Orderly Arrays of Catalytic Si Nanowire Channels. *Nano-Micro Letters* **2025,** *17*(1), 154.

(64) Hobbs, R.G.; Petkov, N.; Holmes, J.D. Semiconductor nanowire fabrication by bottom-up and top-down paradigms. *Chemistry of Materials* **2012,** *24*(11), 1975-1991.

(65) Ghazali, N.A.B.; Ebert, M.; Ditshego, N.M.; de Planque, M.R.; Chong, H.M. Top-down fabrication optimisation of ZnO nanowire-FET by sidewall smoothing. *Microelectronic Engineering* **2016,** *159*, 121-126.

(66) Jeong, J.; Lee, S.H.; Masuoka, S.A.; Min, S.; Lee, S.; Kim, S.; Myung, T.; Choi, B.; Sohn, C.W.; Kim, S.W.; Choi, J., , et al. World's first GAA 3nm foundry platform technology (SF3) with novel multi-bridge-channel-FET (MBCFET™) process. *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* **2023,** 1-2.

(67) Fischer, K.; Abboud, F.; Aggarwal, R.; Amin, P.; Anand, S.; Asoro, M.; Atay, C.; Auth, C.; Aykol, M.; Badmaev, A.; Bains, B., , et al. Intel 18A platform technology featuring RibbonFET (GAA) and PowerVia for advanced high-performance computing. *Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* **2025,** 1-3.

(68) Morsy, M.; Znid, F.; Farraj, A. A critical review on improving and moving beyond the 2 nm horizon: Future directions and impacts in next-generation integrated circuit technologies. *Materials Science in Semiconductor Processing* **2025,** *190*, 109376.

(69) Mertens, H.; Ritzenthaler, R.; Chasin, A.; Schram, T.; Kunnen, E.; Hikavyy, A.; Ragnarsson, L.Å.; Dekkers, H.; Hopf, T., Wostyn, K.; Devriendt, K., , et al. Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates. In *2016 IEEE International Electron Devices Meeting (IEDM)* **2016,** 19-7.

(70) Armstrong, S.; Solís, M.; Urata, S. Economic security and new industrial policy. *Asian Economic Policy Review* **2025,** *20*(2), 265-275.

(71) Pal, A.; Bazizi, E.M.; Colombeau, B.; Alexander, B.; Ayyagari-Sangamalli, B. Nanosheet width investigation for gate-all-around devices targeting SRAM application. *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)* **2021,** 19-22.

(72) Duque, T.; Hatt, A. *Early research demonstrated novel approach to Next-Generation transistor design*. Berkeley Lab News Center. 2025. [Online]. Available: https://newscenter.lbl.gov/2025/09/22/early-berkeley-lab-research-demonstrated-novel-approach-to-next-generation-transistor-design/ (accessed April 6, 2026).

(73) Shilov, A. Samsung's new roadmap unveils its 2nm process nodes and outlines backside power delivery plans. *Tom's Hardware*. 2024, June 13. [Online]. Available: https://www.tomshardware.com/tech-industry/samsungs-new-roadmap-unveils-its-2nm-process-nodes-and-outlines-backside-power-delivery-plans (accessed April 6, 2026).

(74) [Online]. Available: https://www.intel.com/content/www/us/en/foundry/process.html (accessed April 6, 2026).

(75) Morris, M. TSMC 2025 Technology Symposium. *Nomad Semi*. 2025, May 2. [Online]. Available: https://www.nomadsemi.com/p/tsmc-2025-technology-symposium (accessed April 6, 2026).

(76) *2D-material based devices in the logic scaling roadmap | imec*. 2025. IMEC. [Online]. Available: https://www.imec-int.com/en/articles/introducing-2d-material-based-devices-logic-scaling-roadmap (accessed April 6, 2026).

(77) Londhe, P.U.; Chaure, N.B. Field-effect transistors: Advances, challenges, and future prospects. *Nanoelectronics* **2025,** 204-239.

(78) He, G.; Zhu, L.; Sun, Z.; Wan, Q.; Zhang, L. Integrations and challenges of novel high-k gate stacks in advanced CMOS technology. *Progress in Materials Science* **2011,** *56*(5), 475-572.

(79) Das, S.; Sebastian, A.; Pop, E.; McClellan, C.J.; Franklin, A.D.; Grasser, T.; Knobloch, T.; Illarionov, Y.; Penumatcha, A.V.; Appenzeller, J.; Chen, Z., , et al. Transistors based on two-dimensional materials for future integrated circuits. *Nature Electronics* **2021,** *4*(11), 786-799.

(80) Schram, T.; Sutar, S.; Radu, I.; Asselberghs, I. Challenges of wafer-scale integration of 2D semiconductors for high-performance transistor circuits. *Advanced Materials* **2022,** *34*(48), 2109796.

(81) Suman, J.V.; Priya, A.S.; Priyadarshini, G.A.; Krishnamraju, K.; Gangadhar, A.; Hema, M. Integration challenges and opportunities for Gate-All-Around FET (GAA FET) in next-generation electronic devices. *International Conference on Computational Innovations and Emerging Trends* **2024,** 1361-1368.

(82) Noh, C.; Han, C.; Won, S.M.; Shin, C. Vertical gate-all-around device architecture to improve the device performance for sub-5-nm technology. *Micromachines* **2022,** *13*(9), 1551. Atlantis Press.

(83) Lithography and Patterning. *IEEE International Roadmap for Devices and Systems*, 2023.

(84) Kim, K.; Kuzumoto, Y.; Jung, C.; Heo, S.; Zou, T.; Byeon, G.; Kang, H.; Kim, H.; Lim, Y.; Shin, J.; Lim, S.J., , et al. Intrinsically stretchable 2D MoS_2 transistors. *Nature Communications* **2026,** *17*, 1796.

(85) Neilson, K.; Mokhtarzadeh, C.; Jaikissoon, M.; Bennett, R.K.; Buragohain, P.; Verma Penumatcha, A.; Kumar Pinnepalli, S.S.; Rogan, C.; Kozhakhmetov, A.; Maxey, K.; Clendenning, S., , et al. Threshold Voltage Control through Solvent Doping of Monolayer MoS_2 Transistors. *Nano Letters* ***2025*****,** *25*(19), 7778-7784.

(86) Wu, W.C.; Hung, T.Y.; Sathaiya, D.M.; Chen, E.; Hsu, C.F.; Yun, W.; Hu, H.C.; Liu, B.H.; Lee, T.Y.; Kei, C.C.; Chang, W.H., , et al. On the extreme scaling of transistors with monolayer MoS_2 channel. *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* **2024,** 1-2.

(87) Xi, F.; Sharma, H.; Wu, X.; Verreck, D.; Cott, D.; Grubbs, R.K.; Ngo, T.D.; Kumar, P.; Morin, P.; Groven, B.; de Marneffe, J.F., , et al. High-Performance Monolayer-2D Stacked Nanosheet FETs with High $I_{ON} \sim 451$ μA/μm and $I_{ON}/I_{OFF} > 10^9$. *IEEE International Electron Devices Meeting (IEDM)* **2024,** 1-4.

(88) Wu, F.; Tian, H.; Shen, Y.; Hou, Z.; Ren, J.; Gou, G.; Sun, Y.; Yang, Y.; Ren, T.L. Vertical MoS_2 transistors with sub-1-nm gate lengths. *Nature* **2022,** *603*(7900), 259-264.

(89) Ravel, V.M.; Evans, S.R.; Holmes, S.K.; Doherty, J.L.; Rahman, M.S.; Roy, T.; Franklin, A.D. Impact of Contact Gating on Scaling of Monolayer 2D Transistors Using a Symmetric Dual-Gate Structure. *ACS Nano* **2026,** *20*(8), 7127-7136.

(90) Zhang, L.; Dong, J.; Ding, F. Strategies, status, and challenges in wafer scale single crystalline two-dimensional materials synthesis. *Chemical Reviews* **2021,** *121*(11), 6321-6372.

(91) Wang, Y.; Sarkar, S.; Yan, H.; Chhowalla, M. Critical challenges in the development of electronics based on two-dimensional transition metal dichalcogenides. *Nature Electronics* **2024,** *7*(8), 638-645.

(92) Ram, M.S.; Svensson, J.; Skog, S.; Johannesson, S.; Wernersson, L.E. Low-frequency noise in vertical InAs/InGaAs gate-all-around MOSFETs at 15 K for cryogenic applications. *IEEE Electron Device Letters* **2022,** *43*(12), 2033-2036.

(93) Shao, Y.; Pala, M.; Tang, H.; Wang, B.; Li, J.; Esseni, D.; Del Alamo, J.A. Scaled vertical-nanowire heterojunction tunnelling transistors with extreme quantum confinement. *Nature Electronics* **2025,** *8*(2), 157-167.

(94) Liu, X.; Liu, J.; Antipina, L.Y.; Hu, J.; Yue, C.; Sanchez, A.M.; Sorokin, P.B.; Mao, Z.; Wei, J. Direct fabrication of functional ultrathin single-crystal nanowires from quasi-one-dimensional van der Waals crystals. *Nano Letters* **2016,** *16*(10), 6188-6195.

(95) Choi, K.H.; Lee, B.; Kang, J.; Jeong, B.J.; Cho, S.; Lee, S.H.; Kim, D.; Kim, Y.H.; Chang, J.; Oh, H.S.; Kim, J.H.; Lee, J.H.; Yu, H.K.; Choi, J.Y. High-Performance Field-Effect Transistors and Phototransistors Array Based on Solution-Processed Quasi-1D Van der Waals $Ta_2Pd_3S_8$ Crystals. *Advanced Functional Materials* **2025,** 2507081.

(96) Tans, S. J.; Verschueren, A. R.; Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **1998,** *393*(6680), 49-52.

(97) Zhang, K.; Gao, N.; Zhang, J.; Li, Y.; Zhao, J.; Zhou, D.; Wang, X.; Liu, P.; Lin, X.; Xu, H.; Peng, L.M.; Zhao, W. Boosting carbon nanotube transistors through γ-ray irradiation. *Nature Communications* **2026,** *17*, 1896.

(98) Kastner, M. A. The single-electron transistor. *Reviews of Modern Physics* **1992,** *64*(3), 849.

(99) Klein, D. L.; Roth, R.; Lim, A. K.; Alivisatos, A. P.; McEuen, P. L. A single-electron transistor made from a cadmium selenide nanocrystal. *Nature* **1997,** *389*(6652), 699-701.

(100) An, J.; Hu, Z.; He, Z.; Li, S.; Song, X.; Zhao, L.; Wang, J.; Yu, L. Lithography-free, site-controlled germanium quantum dots in silicon nanowires for single-hole transistors operating up to 50 K. *Science Advances* **2026,** *12*(7), eaed0335.