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# Two Dimensional Transistors with Non-volatile Functionalities

By

Zhongyuan Lu

A dissertation submitted in partial satisfaction of the

Requirement for the degree of

Doctor of Philosophy

in

Physics

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Sayeef Salahuddin, Co-Chair

Professor Irfan Siddiqi, Co-Chair

Professor Feng Wang

Professor Jie Yao

Spring 2017

Abstract

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Doctor of Philosophy in Physics

University of California, Berkeley

Professor Sayeef Salahuddin, Co-Chair

Professor Irfan Siddiqi, Co-Chair

Two dimensional (2D) materials have gained much attention these years for their intrinsic physical properties and promising applications in the field of electronics, optics and mechanics. Those materials, especially the 2D transition metal dichalcogenides (TMD), are regarded as a potential replacement plan for silicon in the next generation semiconductor technology. The combination of 2D semiconductors and epitaxial grown single crystalline ferroelectrics enables the development of next generation emerging ferroelectric memory devices, and supplies a polarization controlled system to explore the fancy physical phenomena in the 2D crystals under high carrier density doping at the same time.

This thesis talks about the researches on two dimensional transistors with non-volatile functionalities originating from different mechanisms. Chapter 1 briefly introduced the research topics as well as motivations. Chapter 2 and 3 discussed details of two main components in the research: lead zirconate titanate (PZT) and molybdenum disulfide ($MoS_2$) respectively. The $MoS_2$ flakes were integrated with single crystalline PZT films directly and trap related hysteresis loops were observed in chapter 4. In chapter 5, methods to minimize the effects of interface states in the 2D ferroelectric structure were carried out. Correct handedness hysteresis loops were detected, with large loop size (>20V) and high ON/OFF ratio (>$10^6$), exhibiting the promising future of 2D ferroelectric devices. The switchable metal-insulator phase transitions of $MoS_2$ controlled by ferroelectric polarization were also detected. In chapter 6, the clockwise hysteresis loops induced by interface states in the $MoS_2$ 2D dielectric transistor were investigated. Then a pulse gating technique with self-designed pulse sequences was developed, which effectively minimized the hysteresis loops induced by adsorbates and the intrinsic electrical properties of tested devices were eventually extracted.

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# Chapter 1. Introduction

## 1.1 Introduction and Motivation

Semiconductor transistors, as the building block of integrated circuits (IC), are the most important unit of hardware products existing everywhere in our daily lives. Silicon (Si) has been taking over the world of semiconductor technology for decades based on its advantages in process development, process integration and electrical characteristics. According to the Moore's law [1], the number of components per integrated circuit would get doubled every year (later modified as 18 months) to keep the improvement of chip performance. So transistor scaling is the core task of semiconductor industries. However, nowadays the scaling of silicon reaches its bottleneck after going down to nanometers, where problems like bad gate control, high leakage currents and reliability issues emerge. To solve them, some potential replacement plans including two dimensional (2D) materials attract much attention these years. The 2D transistors, with atomic thin semiconductor channel, have better gate control and lower OFF current, which could improve the ON/OFF performance and reduce standby power consumption at the same time. Moreover, different from three dimensional (3D) materials, 2D semiconductors are expected to exhibit better in-plane carrier transport performance with strong vertical quantum confinement as well as absence of dangling bond on the surface [2].

Ferroelectric materials have been researched for the potential applications in electronic devices for many years. With nonlinear and spontaneous polarization, ferroelectrics could be used in both logic and memory fields, like negative capacitance field effect transistor (NCFET) [3] and ferroelectric random access memory (FeRAM) [4]. However, the integration of epitaxial grown single crystalline ferroelectrics and conventional semiconductor materials (silicon or III-V compounds) is always challenging owing to the huge lattice mismatch in between. Researchers have explored several methods for integration, including adding a buffering layer in between [5] or using polycrystalline (sometimes even amorphous) materials [6, 7]. But then the quality of either the ferroelectric crystal (remnant polarization, retention, etc) or the semiconductor (like mobility) will be sacrificed. For the emerging 2D single crystal semiconductors, their layered structure provides a good chance for the integration with high quality single crystal ferroelectric films via Van der Waal's force rather than chemical bonding.

Two dimensional transition metal compounds with strong vertical confinement are expected to have some interesting physical phenomena inside, especially under high carrier densities when electrons or holes could strongly correlate with each other. The ferroelectric crystal could just supply a large amount of carriers to the 2D semiconductor by polarization-induced doping once they are coupled together. So generally speaking, the two dimensional ferroelectric transistor structure provides us with a system in which both potential applications of memory devices and interesting physical mechanisms could be explored at the same time.

Hysteresis loops are always existing in the transfer curves of devices, resulting from different mechanisms like phase transition, interface states, mobile ions, fixed traps or ferroelectric polarization. In the loop, there are two discrete states (could be defined as “1” and “0”) existing in different sweep directions, which make information storable, retrievable and erasable inside the device. For memory applications, stable and repeatable hysteresis loops are desirable, and the corresponding devices are called “non-volatile memories”. While in logic devices, the loops are harmful to the reliability since they account for the threshold voltage shifts. So in different cases, we shall decide whether and how to improve (or minimize) the non-volatile functionalities based on the specific applications.

## 1.2 Focus of This Study

In this study, I mainly focused on fabrication and characterization of two dimensional transistors with different gate oxides (ferroelectric and dielectric) and investigated the hysteresis loops in those structures. For 2D ferroelectric transistors, I analyzed the robust interface states which screened channel doping from polarization and figured out methods to annihilate them fundamentally to get large and intact hysteresis loops in the correct handedness. Then phase transitions in a 2D system were explored. Investigations on the interface states of 2D dielectric devices were also carried out to analyze the trapping mechanisms and develop methods to minimize those effects eventually.

# Chapter 2. Physics of Lead Zirconate Titanate

## 2.1 Ferroelectric Materials

Ferroelectric materials are insulators exhibiting an electric dipole moment intrinsically which is reversible by the application of an external electric field. Those properties were firstly discovered by Joseph Valasek in 1921 [8]. Then after the discovery of a robust ferroelectric material $BaTiO_3$ (BTO) [9], technologies related to ferroelectrics have been developed rapidly and nowadays ferroelectric materials are widely used in plenty of aspects, including mechanical sensors [10], steep switching transistors [11, 12], and non-volatile memories [13, 14].

Non-centrosymmetry of the crystal structure plays the main role in creating the electric dipole inside. In the non-centrosymmetric crystals, the center of positive charges doesn't coincide with the center of negative charges. So an electric dipole moment exists even in the absence of external electric field, called "spontaneous polarization". Among all 32 crystallographic point groups, 21 of them don't have centrosymmetric center. Those groups (except for group 432, where the piezoelectric charges along the 111 polar axes will cancel each other) exhibit "piezoelectric" properties, which means that applied mechanical force will generate a charge separation on the faces of the crystal and will undergo internal mechanical strain when subjected to an electric field. 10 of those piezoelectric point groups (1, 2, 3, 4, 6, m, 2mm, 3m, 4mm, 6mm) represent the polar crystal classes, which show a spontaneous polarization without mechanical stress due to a unique axis of symmetry (polar). Those polar crystals are named as pyroelectrics, since the spontaneous polarization inside is temperature dependent. Ferroelectric is a subgroup of pyroelectric, with spontaneous polarization that could be reversed by externally electric field stronger than the intrinsic coercive electric field. Here the strong external electric field changes the relative values of different energy states of the crystal through coupling with the polarization. The piezoelectric, pyroelectric and ferroelectric material relationships are outlined in Figure 2.1.

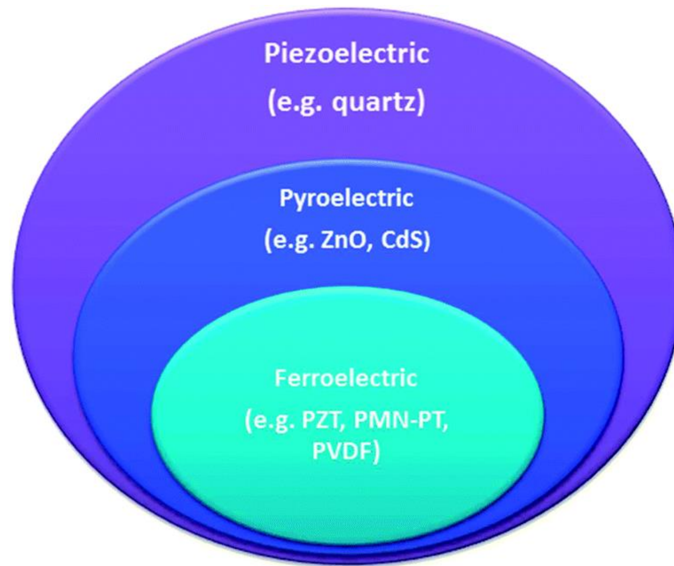



Figure 2.1. Piezoelectric, pyroelectric and ferroelectric material relationships [15].

In the family of ferroelectrics, there are various materials with different crystal structures, like corner sharing octahedra, compounds containing hydrogen bonded radicals, organic polymers and ceramic polymer composites (Figure 2.2). The perovskite oxides in the oxygen octahedron group, with the chemical formula $ABO_3$ (A, B are metal cations and O is oxygen), are most frequently used in research since they have high remnant polarization amplitudes and stable chemical properties in the tetragonal phase.

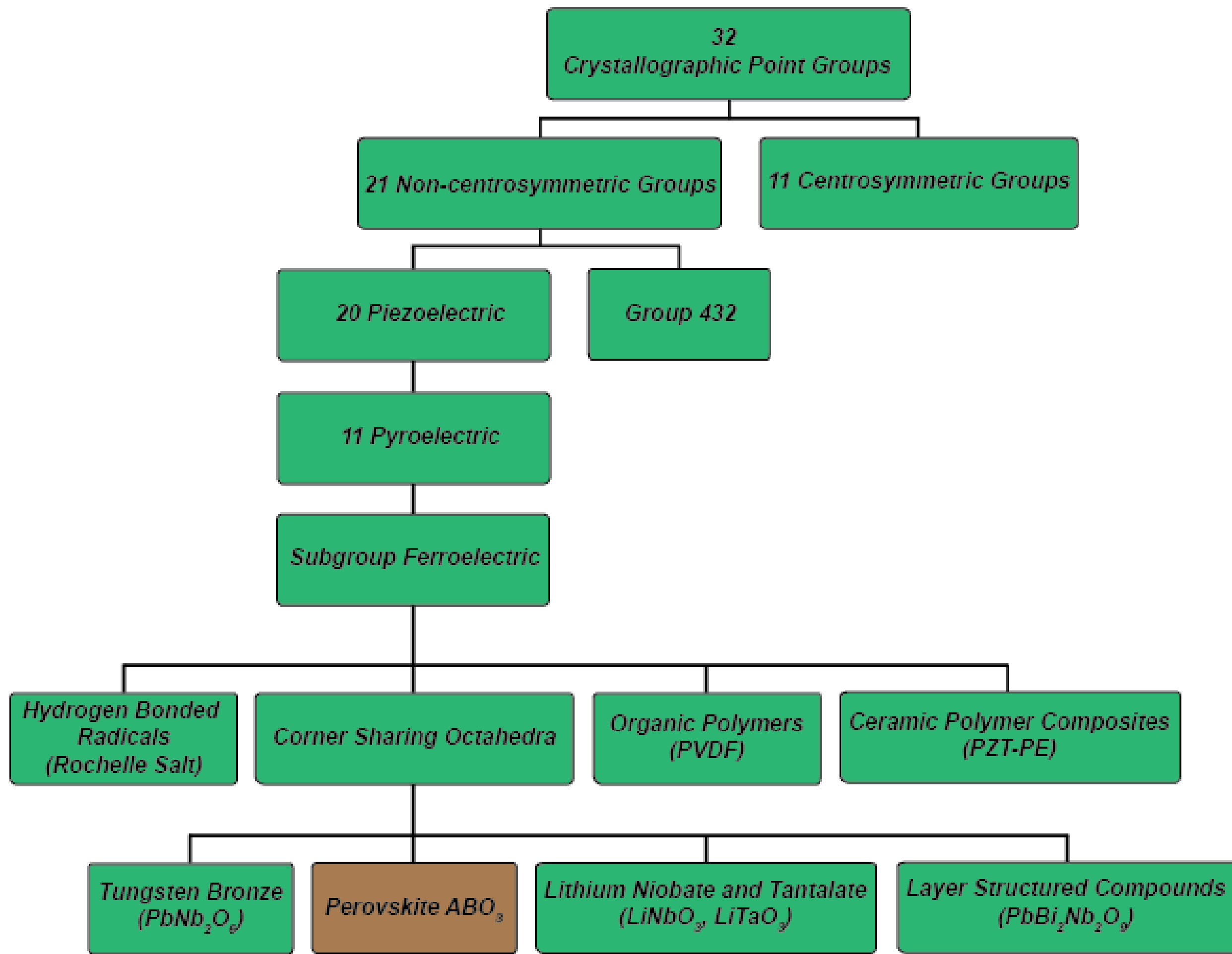



Figure 2.2. Relationships of ferroelectric compounds within 32 point groups.

Our research is mainly focusing on the ferroelectric properties of lead zirconate titanite (PZT), a most popular ceramic material with a perovskite structure, based on its high polarization amplitude (40μC/cm$^2$ or more) and high Curie temperature ($T_c$, always above 350 ℃). It has the common chemical formula: $Pb[Zr_{1-x}Ti_x]O_3$. Here $x \in [0, 1]$ represents the proportion of Ti in the total amount of tetravalent metal ions, and it equals to Ti/(Zr + Ti). The schematic structure of PZT unit cell in the tetragonal phase is shown in Figure 2.3, in which the displacement of Ti or Zr atom near the cubic center induce the polarization in the c axis. The lattice parameters of that tetragonal unit cell are: $a = b = 3.93$Å and $c = 4.13$Å.

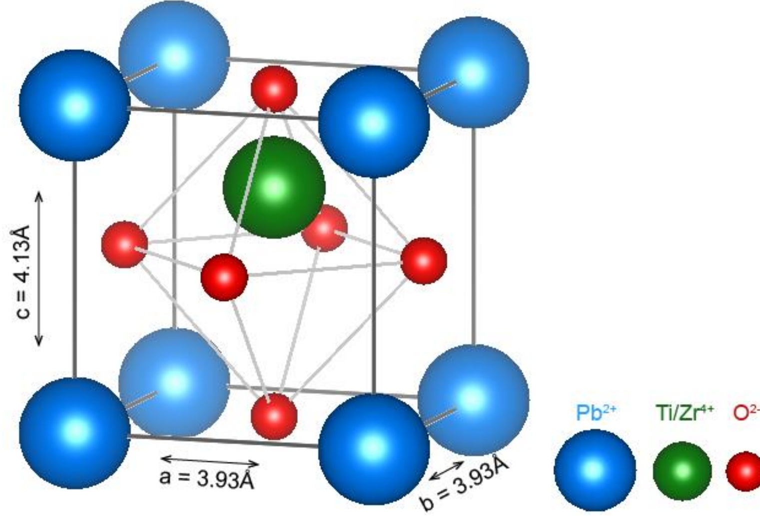



Figure 2.3. The unit cell structure of tetragonal PZT crystal.

## 2.2 Landau's Theory and Phase Transition

Since the first report in 1920s [8], many articles have been published to explain and estimate the properties of ferroelectrics at different conditions. The characteristics of ferroelectrics include several aspects, such as the spontaneous polarization amplitude $P_s$, the external electric field $E$, the Curie temperature $T_c$ (at which the ferroelectric-parasitic phase transition occurs). Landau theory, a general theory of continuous phase transitions, expressed a thermo dynamic potential as a function of an order parameter, its conjugated electric field and the temperature of the system. In 1940s, V.L.Ginzburg developed the first theoretical model [16] for the ferroelectrics based on Landau theory, where the order parameter is exactly the polarization vector $P$. The Landau-Ginzburg polynomial expansion of the Gibbs free energy of the ferroelectric system is as follows:

$$G = F - EP = F_0 + \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - EP \tag{1}$$

here $E$ is the electric field, $F_0$ is the free energy density of the paraelectric phase when $E = 0$. Coefficients $\alpha$, $\beta$, $\gamma$ are anisotropic constants, where α is temperature-dependent:

$$\alpha = \frac{1}{\varepsilon_0 C_0}(T - T_0) \tag{2}$$

in which $T_0$ represents the Curie temperature and $C_0$ is the Curie-Weiss constant. $\beta$ and $\gamma$ depend on the intrinsic properties of specific materials. Without external electric field ($E = 0$), the equilibrium conditions correspond to the minimum of $F$, which is:

$$\frac{\partial F}{\partial P} = 0, \frac{\partial^2 F}{\partial P^2} > 0 \tag{3}$$

In $Pb[Zr_{1-x}Ti_x]O_3$, $C_0$, $\beta$, $\gamma$ and $T_0$ are all related to the coefficient $x$ [17]:

$$C_0 = [\frac{2.8339}{1+126.56(x-0.5)^2} + 1.4132] \times 10^5 \tag{4}$$

$$\beta = 4 \times (10.612 - 22.655x + 10.955x^2) \times \frac{10^{13}}{C_0} \tag{5}$$

$$\gamma = 6 \times (12.026 - 17.296x + 9.179x^2) \times \frac{10^{13}}{C_0} \tag{6}$$

$$T_0 = 462.63 + 843x - 2105.5x^2 + 4041.8x^3 - 3828.2x^4 + 1337.8x^5 \tag{7}$$

Based on those equations, $P$ is much smaller than the coefficients $\alpha$, $\beta$ and $\gamma$. So derived from Eq. (1) and (3), the spontaneous polarization value ($P_s = P$ when $E = 0$) could be expressed as:

$$P_s = \pm\sqrt{\frac{T_0 - T}{\varepsilon_0 C_0 \beta}}, T < T_0 \tag{8}$$

The phase diagram of PZT is shown in Figure 2.4. Depending on compositions and temperatures PZT could have different properties. In our research, $x$ was always set as 0.8, which means that the composition of $PbTiO_3$ in the compound was 80% and the chemical formula was written as $Pb(Zr_{0.2}Ti_{0.8})O_3$. That composition corresponds to a most robust ferroelectric material with almost the largest spontaneous polarization ($P_s \approx 70\mu C/cm^2$) in the family of PZT compounds. As shown in the PZT phase diagram (Figure 2.4), at a temperature below around 450℃, $Pb(Zr_{0.2}Ti_{0.8})O_3$ unit cell is tetragonal and the crystal is ferroelectric.

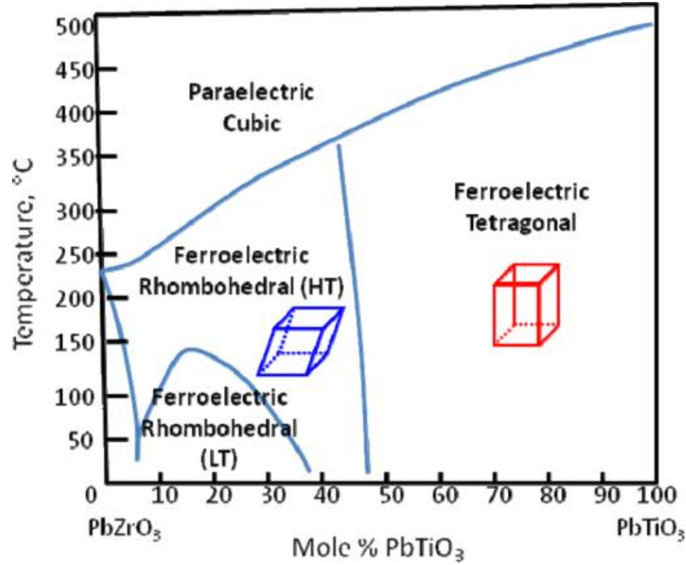



Figure 2.4. The phase diagram of PZT at different temperatures and different compositions of $PbTiO_3$ [18].

From Eq. (8), the spontaneous polarization amplitude is calculated to be around 69.9 μC/cm$^2$ at room temperature, very close to previously reported experimental results [19, 20]. The simulated spontaneous polarization amplitudes of $Pb(Zr_{0.2}Ti_{0.8})O_3$ at different temperatures are plotted in Figure 2.5. At high temperatures, $P_s = 0$, meaning $Pb(Zr_{0.2}Ti_{0.8})O_3$ is in the paraelectric phase; and when $Pb(Zr_{0.2}Ti_{0.8})O_3$ is ferroelectric, $P_s$ could reach as high as 80μC/cm$^2$. The Curie temperature ($T_c$), where the ferroelectric-paraelectric phase transition occurs, is around 732K (459°C), matching the $T_c$ value for $x = 0.8$ depicted in Figure 2.4. The phase transition is first-order since the change of $P_s$ at $T_c$ is discontinuous.

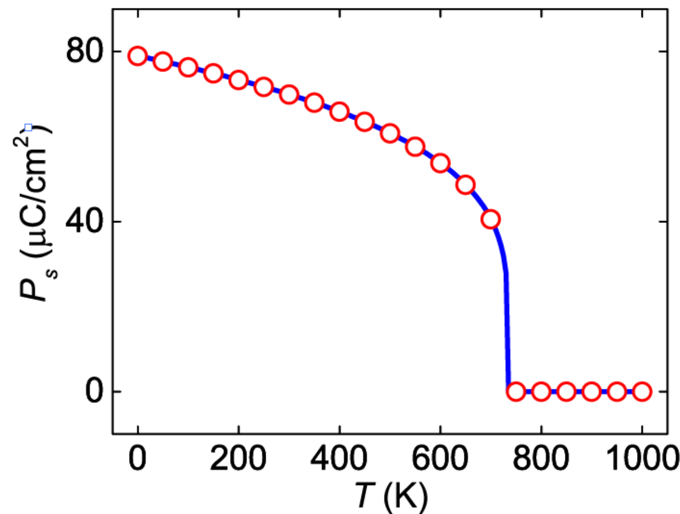



Figure 2.5. The polarization amplitude of $Pb(Zr_{0.2}Ti_{0.8})O_3$ at different temperatures.

## 2.3 PZT Growth and Structure Characterization

Pulsed laser deposition (PLD) is the most widely used technique to grow epitaxial oxide thin films. It's a typical physical vapor deposition (PVD) process in which a high-power laser is focused on the target of the material to be deposited in a high vacuum environment or with the presence of inert (including $N_2$ or Ar) or reactive (such as $O_2$) background gases. The schematic diagram of the PLD chamber is depicted in Figure 2.6, where the rotator is designed to improve the uniformity of grown films. The incident beam source is 248nm KrF excimer laser.

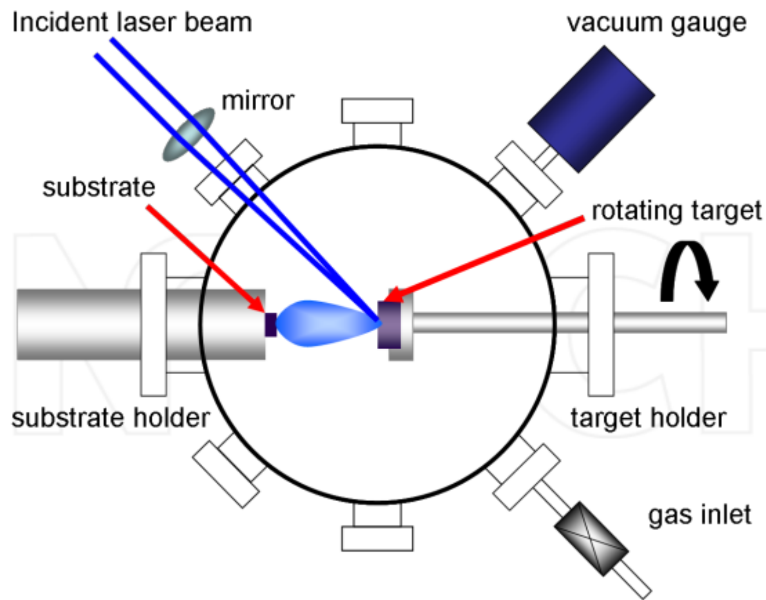



Figure 2.6. PLD chamber for PZT growth.

To grow high quality $Pb(Zr_{0.2}Ti_{0.8})O_3$ crystals, $O_2$ was used as the background gas to fully oxidize the deposited films. The substrate to deposit PZT on was 5 μm thick single crystal (001) oriented strontium titanate ($SrTiO_3$, STO), since its in-plane lattice constant ($a = b = 3.905$Å) is very close to that of PZT ($a = b = 3.93$Å). A conductive thin strontium ruthenate ($SrRuO_3$, SRO) buffering layer with lattice constant 3.95Å was grown prior to PZT as a back electrode, based on its low resistivity of ~ 225μΩ·cm. The cross section of grown heterostructure is depicted in Figure 2.7. Since the in-plane lattice constants of those three crystals are almost the same, the effects of lattice mismatch on the interfaces could be neglected.

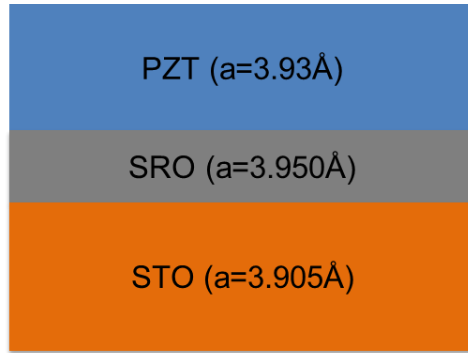



Figure 2.7. The cross section of PLD grown PZT film on STO substrate.

In our PLD steps, the PZT and SRO are grown at 600°C and 700°C respectively. After the film growth, the sample was cooled down to room temperature in 1atm pressure of $O_2$ at a rate of 10°C per minute.

After PLD, the grown heterostructure (PZT/SRO/STO) was tested by X-ray diffraction (XRD), a non-destructive analytical technique where the incident X-rays were diffracted into multiple directions by crystalline atoms. In the XRD spectrum (Figure. 2.8), crystal structures of different materials in the sample could be determined by the peaks and corresponding X-ray incident angles (θ).

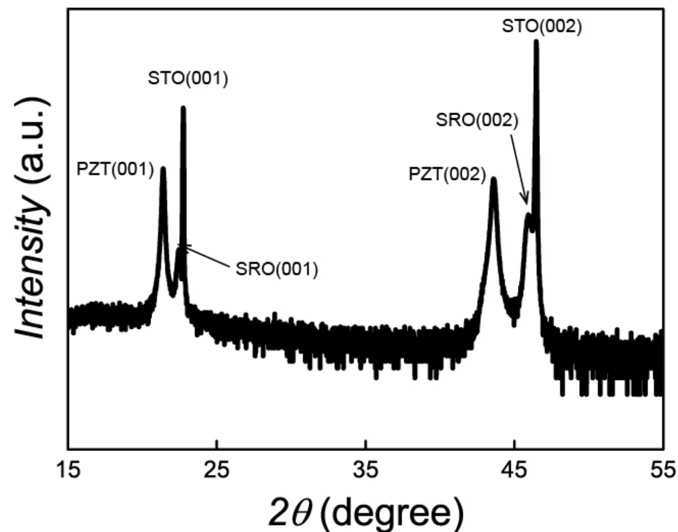



Figure 2.8. XRD spectrum of PZT/SRO/STO heterostructure grown by PLD.

Since every detected peak had a very narrow full-width-at-half-maximum (FWHM), the grown SRO and PZT layers were both convinced to be single crystalline. The out of plane (001) lattice constants could be derived by Bragg's law:

$$2d\sin\theta = n\lambda \tag{9}$$

where $d$ is the out of plane lattice constant, $\theta$ is the incident angle, $\lambda$ is the wavelength of X-ray (0.154nm here, with Cu source) and n is any integer. Based on those $x$-axis coordinates of peaks in Figure 2.8 and Eq. (9), the out of plane lattice constants of grown PZT, SRO and the STO substrate could be calculated as 4.15Å, 3.95Å and 3.903Å respectively. Those results are very close to the values mentioned before (labelled in Figure 2.3).

## 2.4 Electrical Characterization of PZT Films

After PZT film growth, several testing techniques were carried out to check its electrical performance, including hysteresis loops and capacitance-voltage (CV) characteristics. For the electrical tests, a metal-insulator-metal (MIM) ferroelectric (FE) capacitor was fabricated on the grown PZT film. As mentioned in chapter 2.3, a thin conductive SRO buffering layer was grown under PZT as the back electrode. Top electrodes were patterned by photolithography and e-beam evaporation. Voltage bias was added between those two electrodes (Figure 2.9).

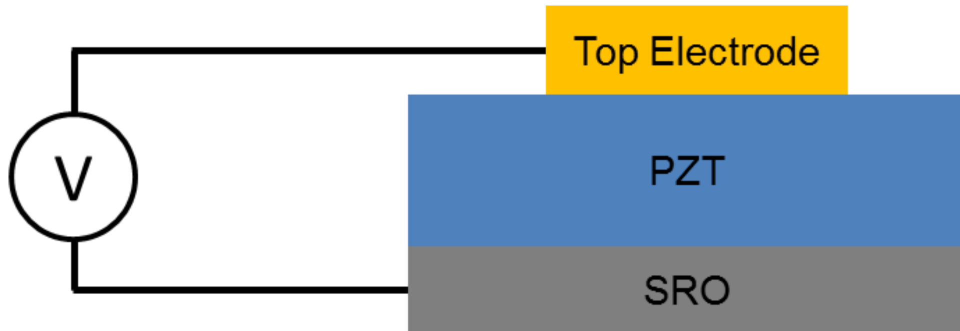



Figure 2.9. The schematic structure of PZT ferroelectric capacitor with voltage biased on the electrodes.

An external electric field generated by the voltage bias pointed vertically across the film. If the external electric field in the opposite direction to the spontaneous polarization ($P_s$) was larger than the coercive electric field ($E_c$) of PZT, the film would get switched and its spontaneous polarization would change to the same direction as the electric field (Figure 2.10). During the voltage sweeping, those parameters of the PZT capacitor, like polarization amplitude ($P$), coercive electric field ($E_c$), capacitance ($C$) and conductance ($G$) were recorded.

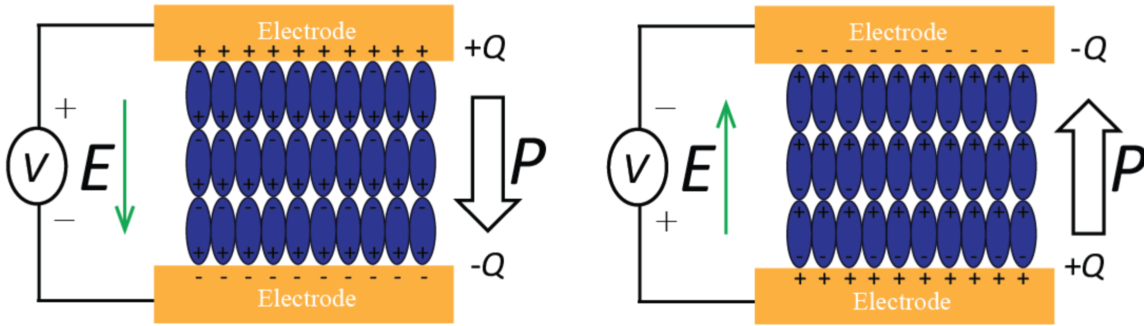



Figure 2.10. Switching of FE capacitor by external electric fields.

The Radiant Precision Multiferroic Analyzer was used to test the polarization properties of PLD grown PZT films. The mechanism of polarization measurement is generating a triangle pulse sequence (Figure 2.11) and capturing all the electrons that move into or out of the capacitor during the stimulus waveform. The polarization amplitude ($P$) is exactly the same as the counted charge ($Q$) moving into the capacitor per unit area since the beginning.

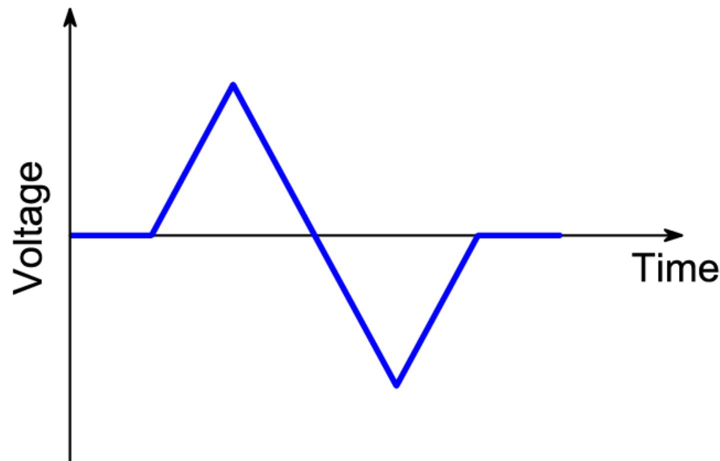



Figure 2.11. Voltage changes in the Radiant Precision Multiferroic Analyzer during a polarization measurement period.

As shown in Figure 2.12, the counterclockwise polarization hysteresis loop of our PZT film is intact and have steep slopes when switching, meaning that it has excellent ferroelectric properties. The coercive electric field $E_c$ is around 0.18MV/cm and the remnant polarization amplitude $P_r$ is about 70 μC/cm$^2$.

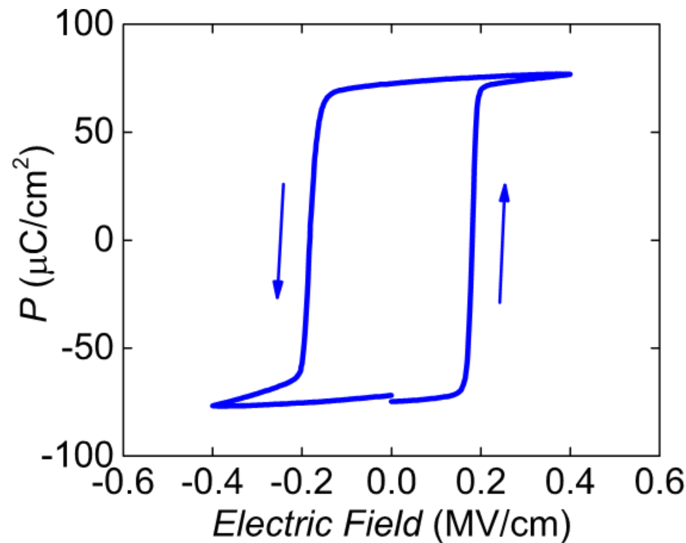



Figure 2.12. The PE loop of the PZT capacitor.

Another commonly used technique in characterizing the electrical properties of ferroelectric films is CV measurement. In our lab that task was done by Agilent B1500A Device Analyzer. The effective circuit model of CV testing in Agilent B1500A is drawn in Figure 2.13.

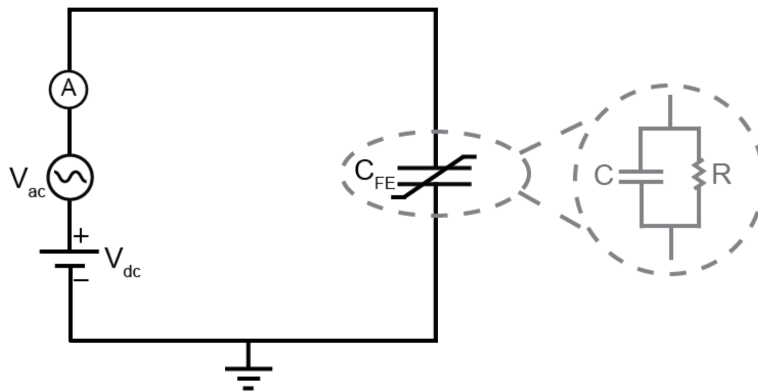



Figure 2.13. The effective circuit in the CV measurement of our PZT capacitor by Agilent B1500A Device Analyzer.

At each measurement point, the capacitor was biased at DC voltage, and an AC voltage source connected in series with the DC source generated a small AC signal. Simultaneously the ampere meter read the current changes in the circuit to calculate the capacitance value ($C$). In the meantime, the capacitor's conductance ($G = 1/R$) could be captured. The admittance angle of that PZT film, $\theta$, which is defined as the phase angle of the PZT film's admittance, is an important parameter to evaluate the electrical properties of PZT. The admittance angle could be calculated as follows:

$$Z = R \parallel \frac{1}{j(2\pi fC)} \tag{10}$$

$$Y = \frac{1}{Z} = \frac{1}{R} + j(2\pi fC) \tag{11}$$

$$\theta = \arctan(2\pi fCR) = \arctan(2\pi fC / G) \tag{12}$$

where $Z$ is the impedance, $f$ is the frequency of the AC signal, $R = 1/G$ is the resistance and $Y$ is the admittance of the capacitor. If $\theta$ is large (close to 90°), the imaginary part of admittance is much larger than the real part, meaning that the resistance $R$ is large enough so that the film is not leaking; while if $\theta$ has the small value (< 85°), the film is regarded as not resistive enough and the leakage current under voltage bias will be high.

After measurement, the admittance angles and $c$-axis oriented (001) relative dielectric constant ($\varepsilon_r$) values could be calculated by Eq. (12) and (13):

$$\varepsilon_r = C \times \frac{t}{\varepsilon_0 S} \tag{13}$$

where $C$ is the measured capacitance value, $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of vacuum, t is the thickness of PZT film and $S$ is the area of the PZT capacitor. Figure 2.14 depicts the calculated relative dielectric constant and admittance angle values at different biased voltages, in which the curves have a "butterfly" shape, corresponding to the hysteresis and retention properties of ferroelectric crystals. The relative dielectric constant was similar to those results measured from high quality films before [21-23], and admittance angles were kept at a high level, confirming the good electrical quality of our PLD grown PZT film.

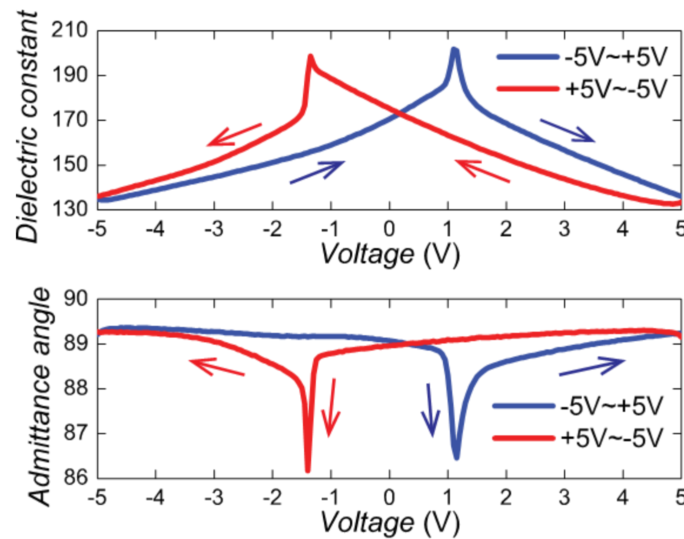


Figure 2.14. The dielectric constant and admittance angle values of the measured PZT capacitor.

# Chapter 3. Molybdenum Disulfide

## 3.1 Intrinsic Properties of $MoS_2$

Transition metal dichalcogenides (TMDs) are popular nowadays for their potential to enable the development of new and highly efficient two-dimensional (2D) electrical and optical devices [1, 24-32]. It is a kind of two-dimensional atomically thin semiconductor materials with the type $MX_2$, where M is the transition metal (like Mo, W) and X represents a chalcogen element (S, Se or Te). TMD compounds have strong in-plane bonding and weak Van der Waals out-of-plane interactions. The simple structure of TMD is a layer of metal atom sandwiched by two layers of chalcogenide atom, and its top view is honeycomb [24].

Unlike graphene, TMDs always have finite band gaps in the 2H phase (i.e. hexagonal symmetry, two layers per repeat unit, and trigonal prismatic coordination) [24, 25]. This is critical for transistor applications. Indeed, excellent switching behavior with high ON/OFF ratio has been demonstrated for a number of different TMD compounds. Schematics of a 2H TMD crystal structure are shown in Figure 3.1.

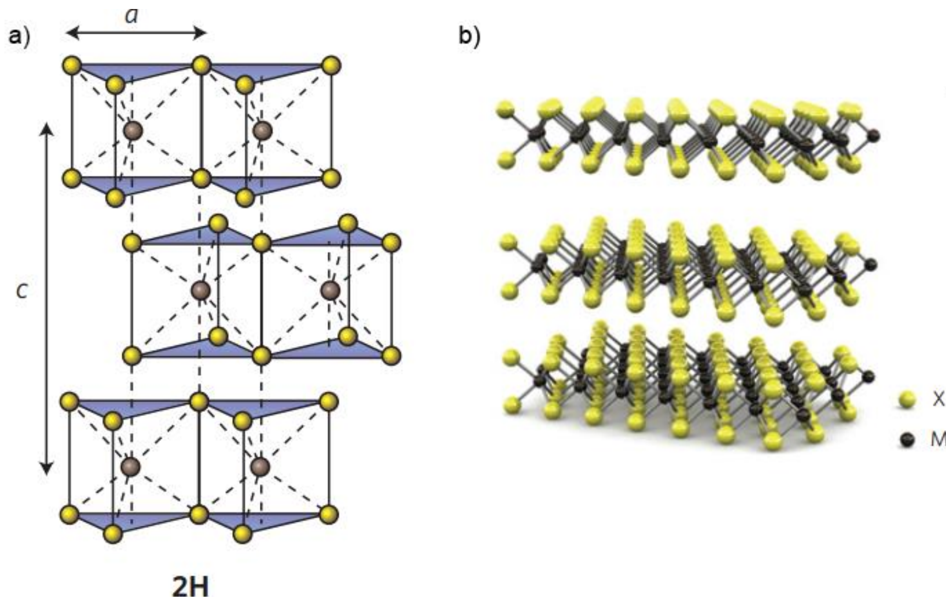



Figure 3.1 [24]. a) Schematic of the 2H TMD compound structure. b) 3-dimensional schematic of TMD, with the chalcogen atoms (X) in yellow and the metal atoms (M) in black.

Molybdenum disulfide ($MoS_2$) is the most widely used material in the family of TMDs, based on its sizable band gap (monolayer ~ 1.8eV, multilayer ~ 1.3eV), stable chemical properties and high growth yield. The monolayer $MoS_2$ is around 0.65nm in thickness. As a finite band gap 2D semiconductor, $MoS_2$ is regarded as a potential replacement of silicon (Si) in the semiconductor industry in the coming future. $MoS_2$ is always n-type doped by sulfur vacancies [33-35] or screening environment [36]. Plenty of works have been reported on $MoS_2$ transistors with electron mobility values ranging from 0.1 to $150cm^2V^{-1}s^{-1}$ [27, 30, 37] at room temperature, which depended on the intrinsic properties of $MoS_2$ crystals (layer thickness, defects), environment (ambient or vacuum) and device structures (encapsulated by 2D insulators or not, top-gate or back-gate).

## 3.2 $MoS_2$ Transistor Fabrication

To fabricate a $MoS_2$ transistor, the first step is always preparing a 2D semiconductor film with ideal thickness. Tape exfoliation, chemical vapor deposition (CVD) [38, 39] and liquid phase preparations [40] have all been tried before for 2D film preparation. Among them, tape exfoliation is always regarded as the most convenient and efficient method to get single crystal $MoS_2$ flakes. That technique, making use of the weak interlayer Van der Waals interaction of 2D crystals, has been developed since the very beginning [41]. In the tape exfoliation process, $MoS_2$ flakes are exfoliated from a bulk crystal purchased from companies (SPI Supplies) by scotch tape and then transferred onto the target substrate. Since large quantities of thick flake byproducts will be generated in the meantime, a silicon substrate with around 285nm thermal oxide on the top is always selected as the substrate to exfoliate $MoS_2$ on because of good color contrast [42] under optical microscope, to help identify the monolayer/multilayer flakes effectively. The color contrast of $MoS_2$ on the $SiO_2$/Si substrate is plotted in Figure 3.2. Atomic force microscopy (AFM) or Raman spectroscopy could be used afterwards to get the precise thickness of a selected flake.

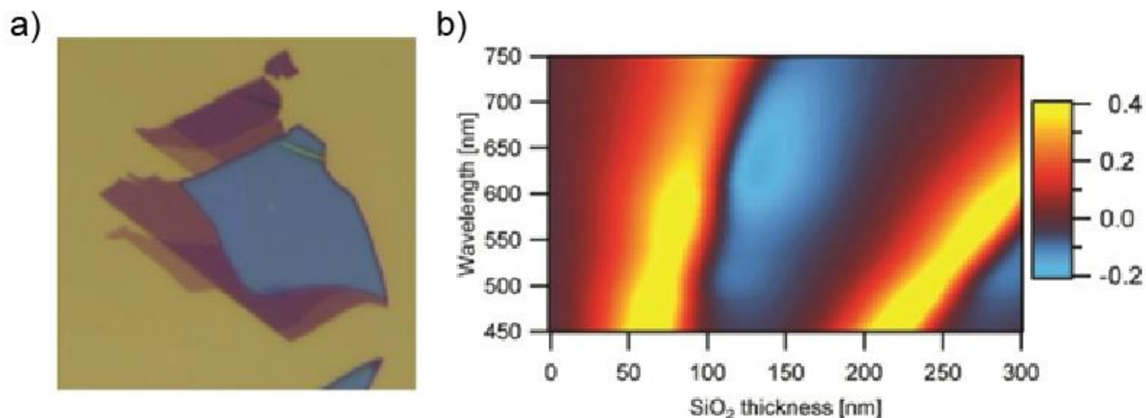
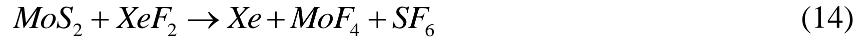



Figure 3.2 [42]. a) The optical image of exfoliated $MoS_2$ thin films. b) Color contrast of $MoS_2$ on $SiO_2$/Si substrate with different $SiO_2$ layer thickness and incident light wavelength.

The Si substrate was always heavily doped by boron (B) or phosphorus (P), making it conductive to perform as the back electrode in the back-gate transistor structure. After mechanical exfoliation and thickness identification, photolithography or e-beam lithography was used to pattern the channel, followed by dry etching to etch away the extra parts. Here the etchant is xenon difluoride ($XeF_2$), and the chemical reaction equations are [43]:



$$MoS_2 + XeF_2 \rightarrow Xe + MoF_4 + SF_6 \quad (14)$$

$$MoF_4 \rightarrow MoF_3 + F_2 \quad (15)$$

All the eventual products of these reactions are gases at room temperature, so after dry etching the surface of $MoS_2$ will be ultra clean.

After etching, lithography was carried out again to define source/drain (S/D) regions and e-beam evaporation was used to evaporate the contact metal stacks, which are Au/Ti or Au only in different cases. Those two terminals could get integrated with the back electrode (heavily doped Si) to constitute a back-gate transistor structure (Figure 3.3a). Sometimes atomic layer deposition (ALD) was used afterwards to deposit a top-gate dielectric layer, followed by gate electrodes patterning and deposition to eventually fabricate a top-gate transistor (Figure 3.3b).

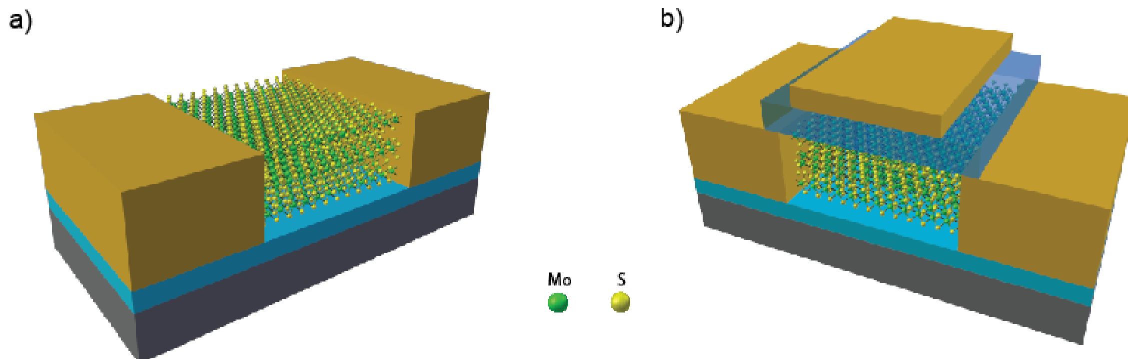



Figure 3.3. 3D schematic structure of $MoS_2$ a) back-gate transistor b) top-gate transistor on the $SiO_2$/Si substrate.

The intact process flow of fabricating a $MoS_2$ back-gate transistor on a heavily doped p-type Si chip is listed in Figure 3.4. Acetone and isopropyl alcohol (IPA) were used in lift-off and chip washing steps (all at room temperature).

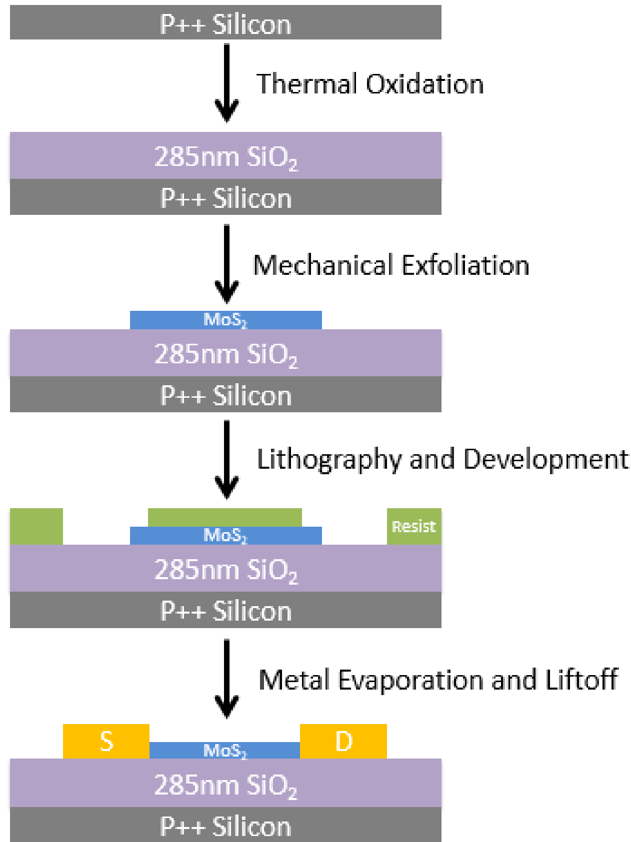



Figure 3.4. Fabrication process flow of a standard $MoS_2/SiO_2$ back-gate dielectric transistor.

## 3.3 $MoS_2$ Phase Transition

Other than the semiconductor-metal phase transformation induced by intralayer atomic plane gliding (from 2H trigonal prismatic $D_{3h}$, to 1T octahedral $O_h$) [44], there are some types of phase transitions in the 2H $MoS_2$ crystal itself, such as metal-insulator transition (MIT) and superconductor-insulator transition (SIT), at specific conditions. Those phase transitions result from the interactions among electrons, phonons and localization states inside the crystal.

Metal-insulator transition (MIT) is a phase transition from metal with good electrical conductivity to insulator with quickly suppressed charge conductivity. That phenomenon has been discovered in several kinds of materials with different mechanisms. Some compounds (such as $VO_2$) show metal-insulator phase transition with changes of composition, voltage, temperature or pressure [45, 46]. Those materials, called Mott insulators, have strong electron-electron interactions inside, which change the band structures and cause phase transitions when specific conditions change [47]. While in $MoS_2$, localized states from defects or ions play the main role in phase changes. As shown in Figure 3.5a, with low electron density, the electrons in $MoS_2$ are

mainly localized and could only transport via hopping through different localized states, called in an "insulating phase". So at a higher temperature, the higher kinetic energy of electrons will improve hopping efficiency and increase the conductance of $MoS_2$. Whereas with high electron density, the interactions between electrons screen the localized states so that electrons could transport smoothly. Then phonon scattering plays the dominant role in limiting the conductance, and $MoS_2$ is in the "metallic phase" where its conductance decreases with temperature increasing. Gate-induced carrier doping, where the target material is made as the channel of a transistor and doped electrons (or holes) are from the displacement of gate oxide induced by gate voltage bias, is a commonly used method in materials' phase transition analysis, since it is reversible and could change the channel doping density easily by gate voltage sweeping. In the 2D transistor structure, the gate oxide layer could supply enough carrier changes (~ $6\times10^{12}cm^{-2}$) for MIT [48]. In Figure 3.5b, there is a crossover point in the transfer curves at different temperatures, regarded as the phase transition point. On the left side of the crossover point, the conductance of $MoS_2$ is higher at higher temperature, corresponding to the insulating phase; while on the right side the channel's conductance decreases with temperature increasing, meaning that $MoS_2$ is in the metallic phase.

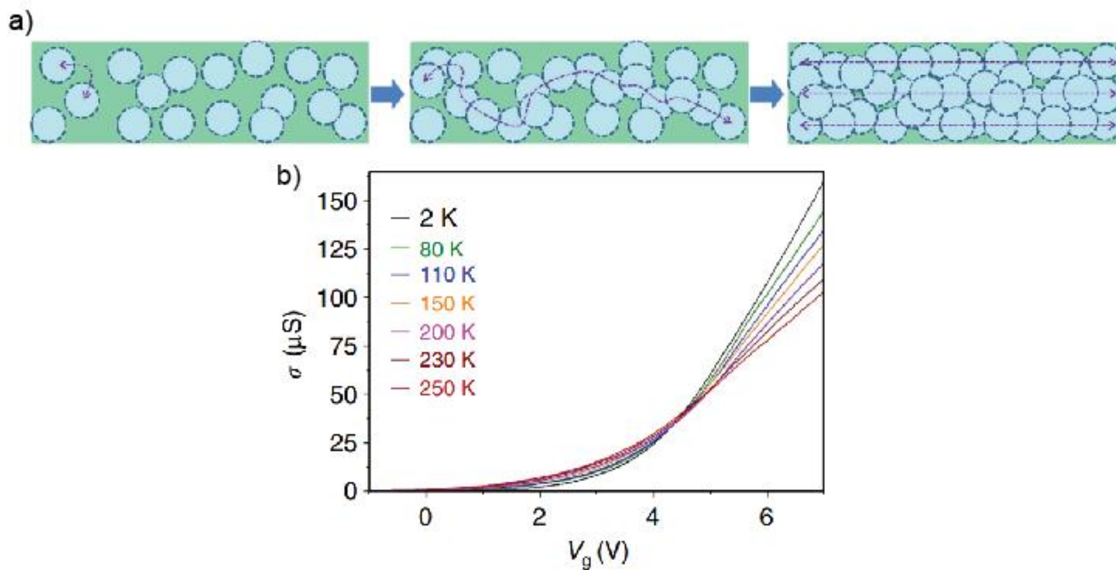



Figure 3.5 [48]. a) Electron transport mechanisms in $MoS_2$ at different carrier densities. b) The conductance changes of $MoS_2$ with gate voltage sweeping at different temperatures.

$MoS_2$ has also been discovered to be a 2D superconductor at low temperature [49-53]. The Berezinskii-Kosterlitz-Thouless (BKT) transition, which is a phase transition from in-plane bound vortex-antivortex pairs at low temperatures to unpaired vortices and anti-vortices at some critical temperature [54, 55], is regarded as the model to explain superconductor-insulator transitions (SIT) in 2D systems. Similar to MIT, the BKT transition could also be triggered by carrier density changes inside the semiconductor. To get SIT, large amount of carriers (> $5\times10^{13}cm^{2}$) are in need, which couldn't be supplied by common dielectric materials. Chemical doping used to be popular in generating enough carriers (electron or hole) in the film for

superconductivity [56-58]. But that process is irreversible and the doping density couldn't be changed conveniently afterwards, limiting the analysis of phase transitions. Recently researchers have developed a new electrostatic doping technique [49, 50, 59-61] for high crystalline 2D superconductors, in which ionic-liquid electrolyte was used as the dielectric layer (Figure 3.6) to supply high electron density ($> 1\times10^{14}cm^{-2}$) to the semiconductors, based on the ultrathin effective dielectric layer existing in the electrolyte (~ 1nm).

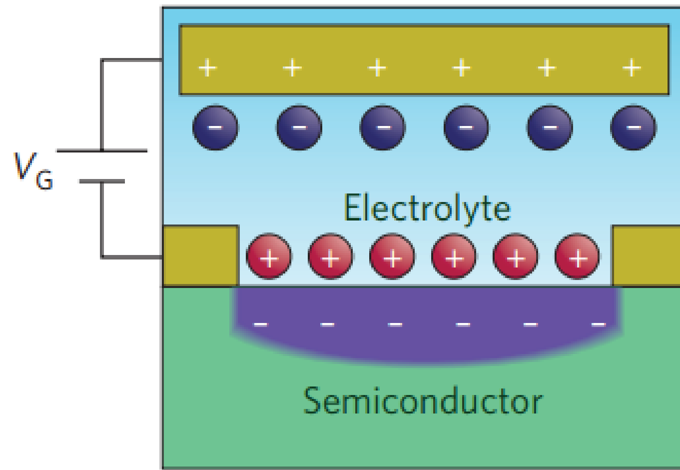



Figure 3.6. The schematic structure of ionic liquid gating [61].

Figure 3.7 depicts the phase diagram of $MoS_2$ with different electron densities. The Curie temperature $T_c$ for superconductivity is as high as 10.5K. At an electron density of around $5\times10^{13}cm^{-2}$, metal-insulator transition occurs. To get those phase transitions, especially SIT, in $MoS_2$, a high range of electron density changes is critical. In expectation, PZT is a good candidate in supplying a large amount of carriers from its high spontaneous polarization amplitude ($\sim70\mu C/cm^2$), which means that it could generate (or deplete) electrons with a density of $4.4\times10^{14}cm^{-2}$ in the $MoS_2$ channel in a 2D ferroelectric transistor structure without continuous gate voltage bias. In chapter 4, I will emphasize on the ferroelectric transistor fabrication and some initial analysis.

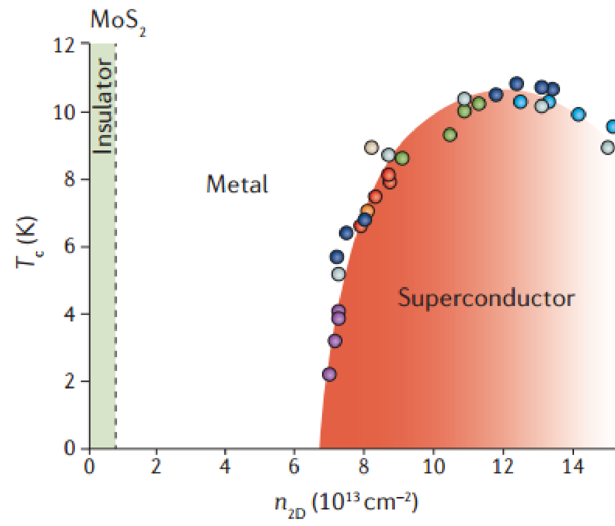



Figure 3.7. Phase diagram of $MoS_2$ with different electron densities inside [62].

# Chapter 4. Two Dimensional Ferroelectric Transistors

## 4.1 Device Preparation

After PZT film growth and polarization testing, a 2D ferroelectric transistor with $MoS_2$ as the channel material was fabricated on it. As mentioned in chapter 3.2, $MoS_2$ flakes on 285nm $SiO_2$ could be prepared directly by mechanical exfoliation, since the color contrast of those flakes there is good. However, for an epitaxial grown PZT film, $MoS_2$ flakes don't have good color contrast on its surface, making it difficult to identify monolayer or multilayer films after direct exfoliation. Moreover, the cost of growing high quality single crystalline PZT films, which is much more expensive than bulk Si wafers, prompts us to find a more efficient way of $MoS_2$ film preparation. So an effective transfer technique was developed, in which the $MoS_2$ flakes were firstly exfoliated on a Si chip with 285nm $SiO_2$ on. After thickness identification of $MoS_2$ films under the optical microscope, a thick PMMA layer was spin-coated on the chip and got hard baked to work as a polymer stamp to carry the selected $MoS_2$ flake during the transfer process. Then the stamp with the flake underneath was mechanically lifted up and moved onto the target PZT film. Eventually after annealing and chemical washing, the selected $MoS_2$ flake was entirely on the PZT film. The whole process flow is in Figure 4.1.

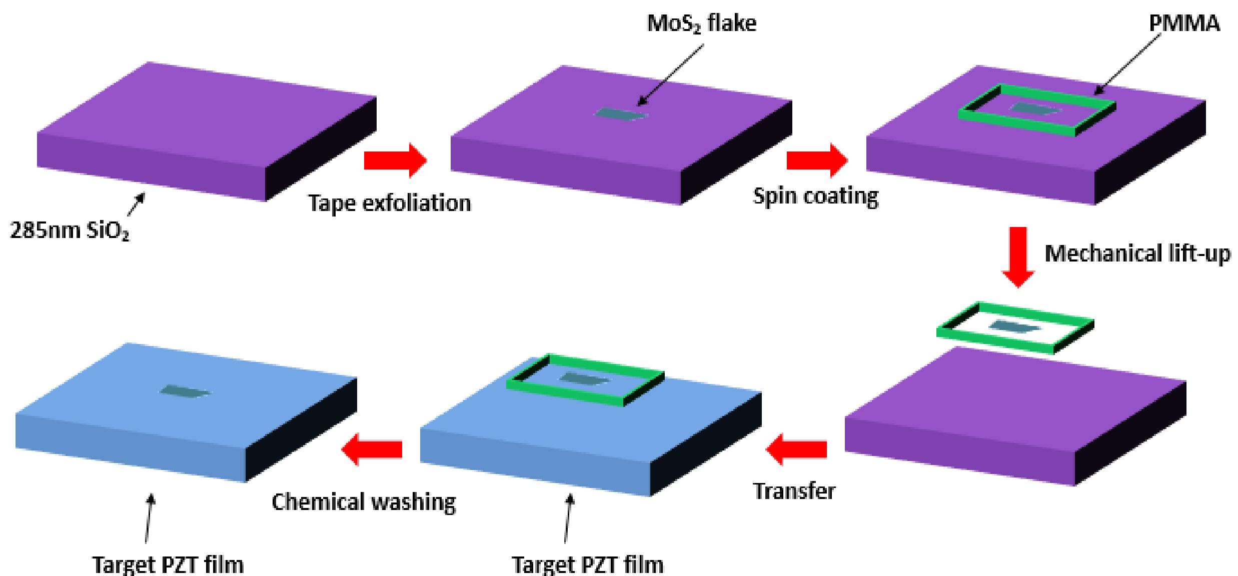



Figure 4.1. The process flow of $MoS_2$ transfer in 2D ferroelectric transistor fabrication.

Optical images of the $MoS_2$ flakes before/after transfer are in Figure 4.2, in which the color contrast difference of $MoS_2$ on those two substrates is obvious. From those images, the high

efficiency of the transfer technique could be identified since both of the flakes were kept intact during the whole process.

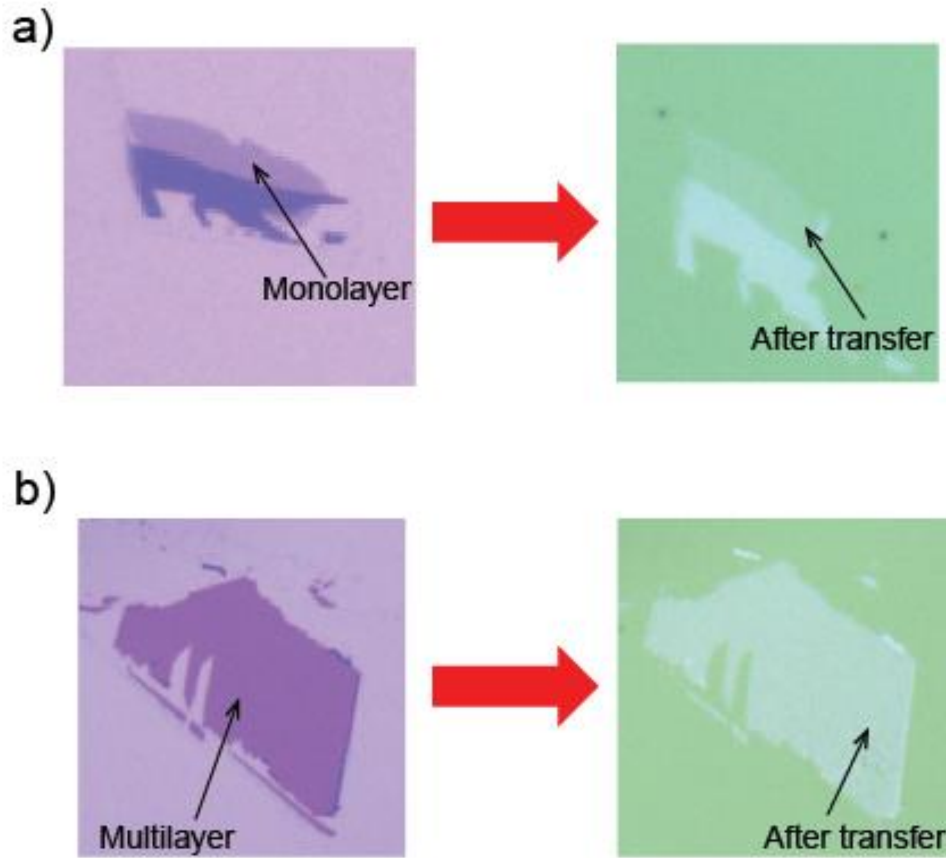



Figure 4.2. Optical images of $MoS_2$ a) monolayer b) multilayer flake before and after transfer.

After transfer, lithography and evaporation steps (same as those in chapter 3.2) were done to make a back-gate 2D ferroelectric transistor, whose schematic structure is in Figure 4.3. The gate oxide is the PZT ferroelectric flim, with SRO underneath as the back-gate electrode. The $MoS_2$ flake is the semiconductor channel, and source/drain electrodes were always made by gold (Au).

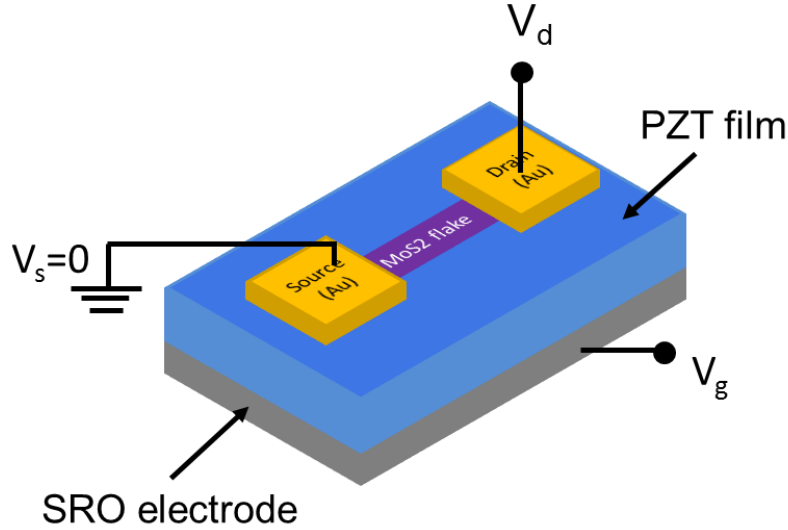



Figure 4.3. Schematic structure of $MoS_2$/PZT ferroelectric back-gate transistor.

## 4.2 Hysteresis Loops of Ferroelectric Devices

In the metal-oxide-semiconductor field effect transistor (MOSFET) structure, applying a voltage across the gate oxide electrostatically dopes the channel via capacitive coupling. Conventional oxides can only exhibit polarization proportional to the applied voltage. In FeFETs, however, the ferroelectric maintains a remnant polarization that switches directions when an opposing electric field is applied with magnitude greater than the coercive electric field $E_c$ (Figure 4.4a and 4.4b). This results in a large hysteresis loop. In the ferroelectric transistor, with electron doping/depletion from the polarization of PZT gate oxide, the threshold voltage ($V_t$) will shift to specific directions (Figure 4.4), based on the following equation:

$$\Delta V_t = -\frac{\Delta Q}{C_{ox}} \tag{16}$$

where $\Delta V_t$ is the threshold voltage shift, $\Delta Q$ is the changes of charge induced by ferroelectric polarization, $C_{ox}$ is the effective capacitance of PZT gate oxide. If the polarization is pointing into the channel (Figure 4.4a), there will be more electrons gathering in $MoS_2$ and enhancing the channel current, so $V_t$ will shift in the positive direction (the blue curve in Figure 4.4c); otherwise, once the polarization is switched to the direction pointing out of the channel (Figure 4.4b), the electrons inside the channel will get depleted, so $\Delta Q > 0$ and $\Delta V_t < 0$, meaning that $V_t$ will shift to the negative side (the red curve in Figure 4.4c). In summary, there should be a counterclockwise hysteresis loop (the green arrows in Figure 4.4c) in the transfer curve of a 2D n-type $MoS_2$ ferroelectric transistor.

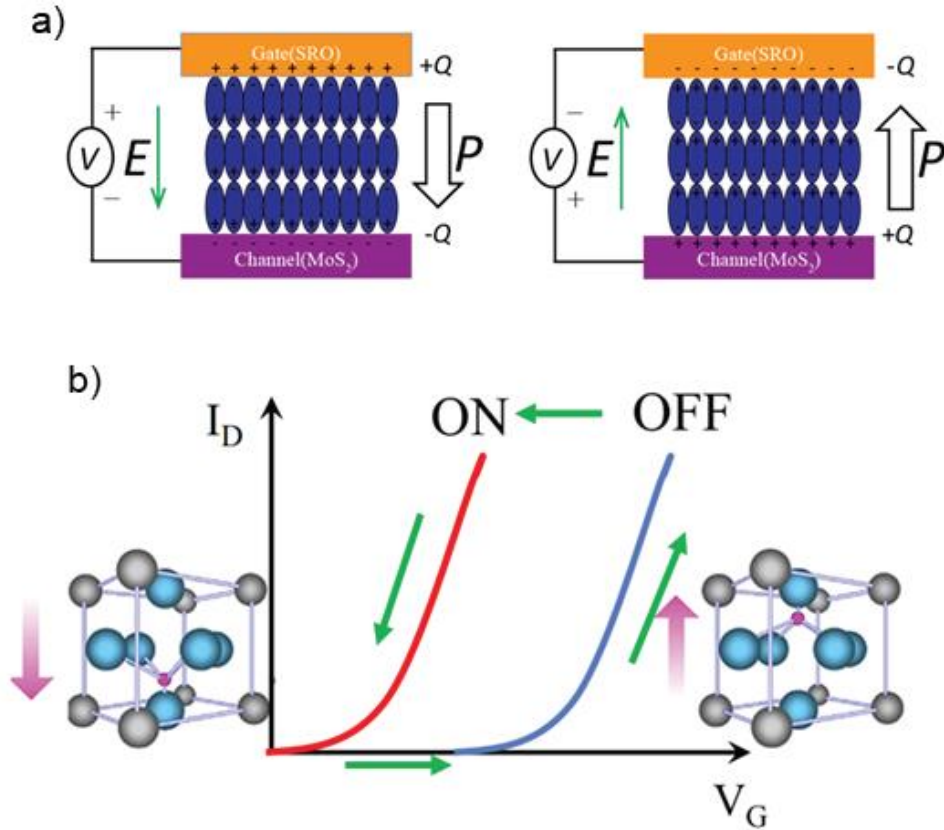



Figure 4.4. a) The schematic of $MoS_2$/PZT/electrode heterostructure showing the doping/depletion mechanism of PZT polarization in the $MoS_2$ film. b) Expected hysteresis loop in the n-type $MoS_2$ ferroelectric transistor.

## 4.3 Trap Related Hysteresis Loops

In expectation, the hysteresis loops of the transfer curves in the n-type 2D $MoS_2$ ferroelectric transistor should be in counterclockwise direction. However, in our first trials, the loops were in the opposite direction (clockwise, Figure 4.5), in which threshold voltage shifts to the negative side in forward sweep and to the positive side in reverse sweep.

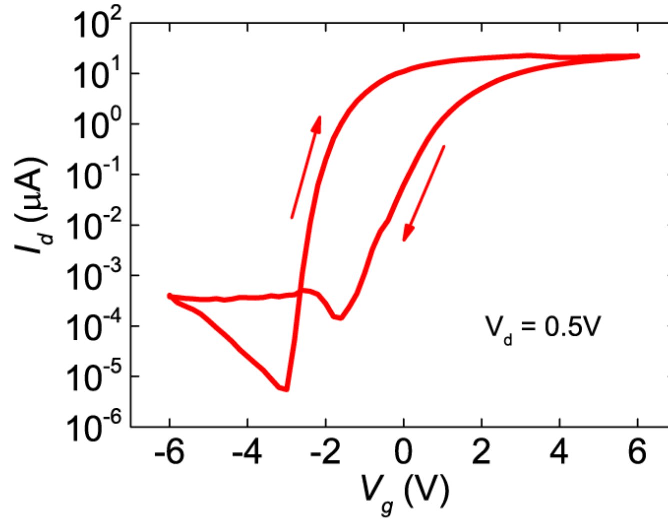



Figure 4.5. The transfer curve of fabricated $MoS_2$/PZT transistor with a hysteresis loop the wrong direction.

Clockwise hysteresis loops have been reported in some previously published works, not only on 2D ferroelectric transistors [63-67], but also on dielectric ones [68-70]. The loops in 2D dielectric transistors are attributed to adsorbates from ambient environment (like $O_2$ or vapor) which create trapping states on the interface between dielectric and 2D materials. More details about the trapping mechanism will be discussed in chapter 6. Some researchers also used adsorbates trapping mechanism to explain the clockwise hysteresis phenomenon in n-type ferroelectric transistors [63, 65, 67], while no convincing experiment evidence has been provided yet. To totally avoid effects from molecules in air, a high vacuum probe station (Lakeshore TTPX) was used, of which the pressure in the chamber could reach as low as $2\times10^{-6}$Torr. At such a low pressure, the molecules from ambient should have already been pumped away. However, in the measurement, robust clockwise hysteresis loops still existed (Figure 4.6), in which the loops had no relationship with the sweep scales or sweep voltage intervals, totally different from the results induced by adsorbates trapping mechanism (more details in chapter 6). So the detected clockwise hysteresis loops didn't origin from adsorbates.

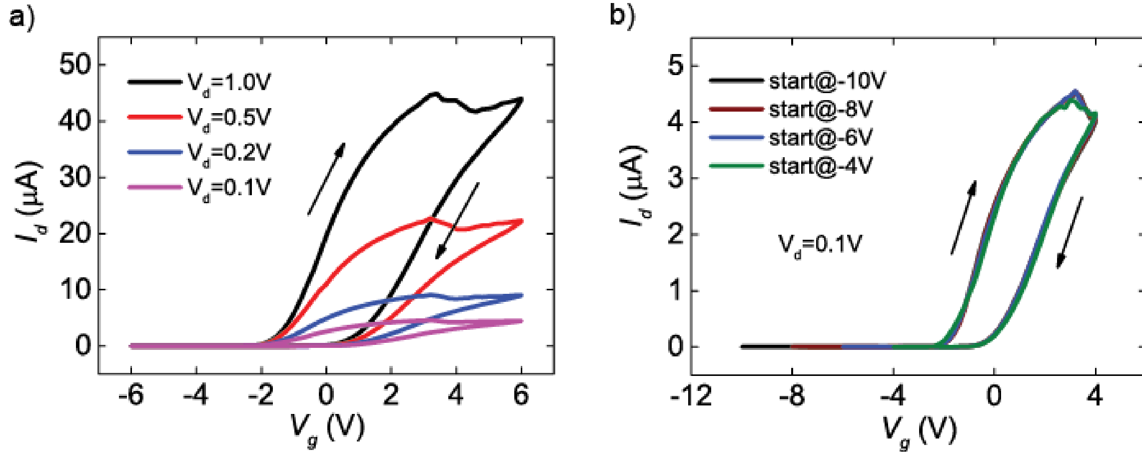



Figure 4.6. Transfer curves of $MoS_2$/PZT transistor a) with different drain voltage values; b) with different gate voltage sweep starting points. Measurements were in vacuum.

There is another explanation [71] claiming that the surface quality of the grown ferroelectric film is the main reason of the trapping states between ferroelectric and 2D layers. Those interface states, different from molecule traps, are generated by the coupling between polarization and surface defects of the ferroelectric film. So the density of trapping states is mainly determined by the polarization and doesn't change with band bending (or shifting) related to gate voltage scales. Figure 4.7a depicts the whole trapping mechanism in a graphene ferroelectric (PTO/STO heterostructure) back-gate transistor. When the ferroelectric film was polarized towards graphene, more electrons got trapped on the interface, causing $V_t$ shifting to the negative side (red curves in Figure. b); once the film was polarized out of graphene, the trapped electrons went back to the channel, so $V_t$ decreased and the transfer curve shifted left (black curves in Figure 4.7b). That model matched our results in vacuum, and the as-grown film used previously in the transistor fabrication was defective indeed (Figure 4.7c). To fully verify the mechanism, more detailed analysis is still in need.

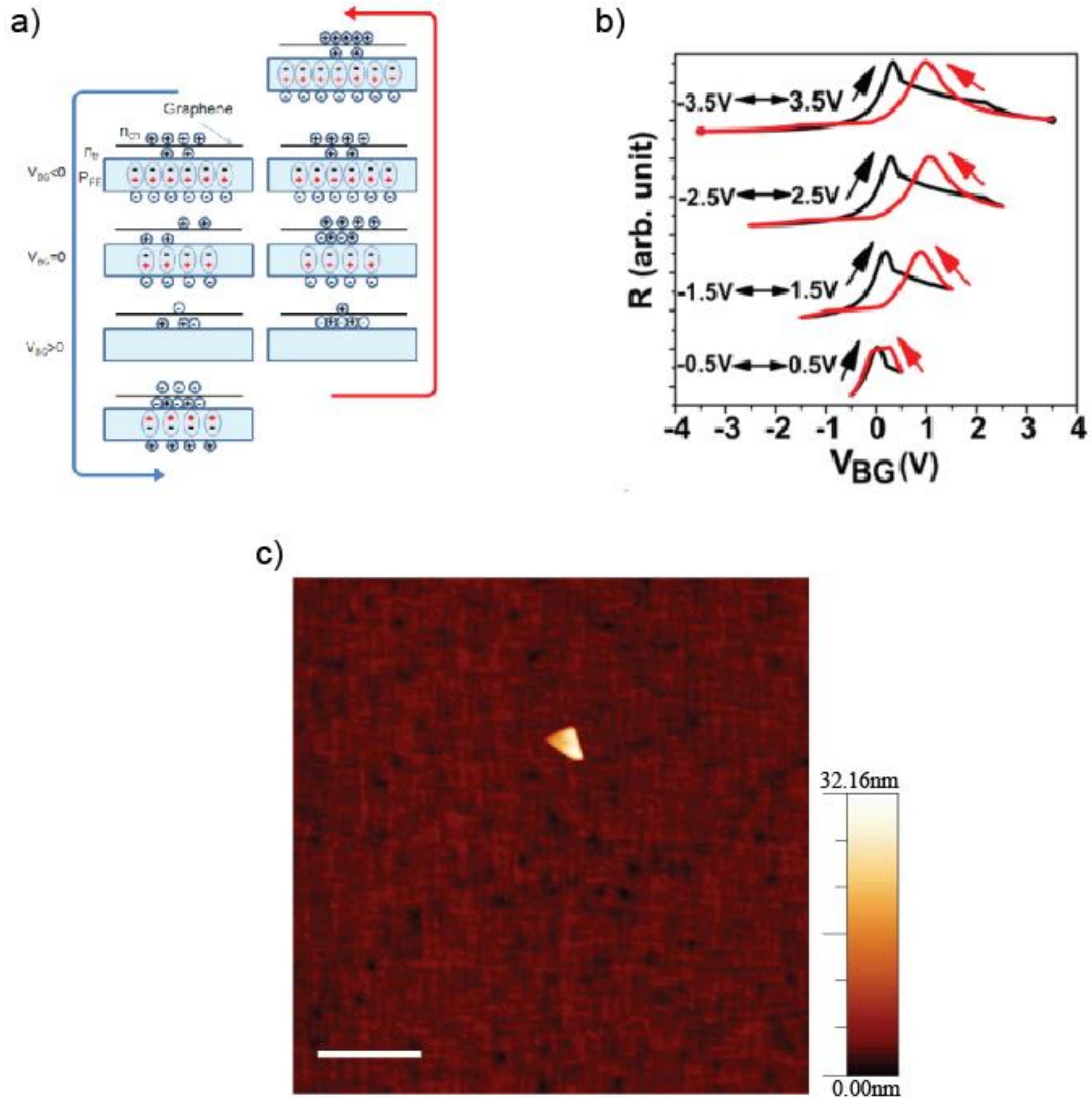



Figure 4.7. a) The polarization – induced trapping dynamics [71]. b) Simulated results of graphene sheet resistance with respect to gate voltages in based on the polarization trapping model [71]. c) The defective surface under AFM of our as-grown PZT film used in the ferroelectric transistor fabrication. The scale bar is 1μm.

To avoid those robust interface states, there are mainly two choices: 1) improving the surface quality of grown PZT films to minimize the amount of surface defects; 2) avoiding the direct contact between 2D and ferroelectric materials so that no interface coupling will exist. Chapter 5 discusses the results got via those two methods in details.

# Chapter 5. Two Dimensional Ferroelectric Transistors with Correct Handedness Hysteresis Loops

## 5.1 Ultra Smooth Ferroelectric Gate Oxide

To reduce the amount of defects on the ferroelectric surface, an ultra-smooth PZT film was produced after the optimization of PLD growth condition. Different from the defective film in chapter 4.3, the optimum PZT film has a much better surface (Figure 5.1a) with the root mean square (RMS) roughness of 4.78Å, almost the same as the out of plane lattice constant of PZT (4.13Å), and no defect on the surface. After evaporating testing electrodes on PZT, the polarization-voltage loops were measured for different voltage scales (Figure 5.1b). The closed loops, high polarization amplitude and excellent sharp switches indicate good electrical quality of that film.

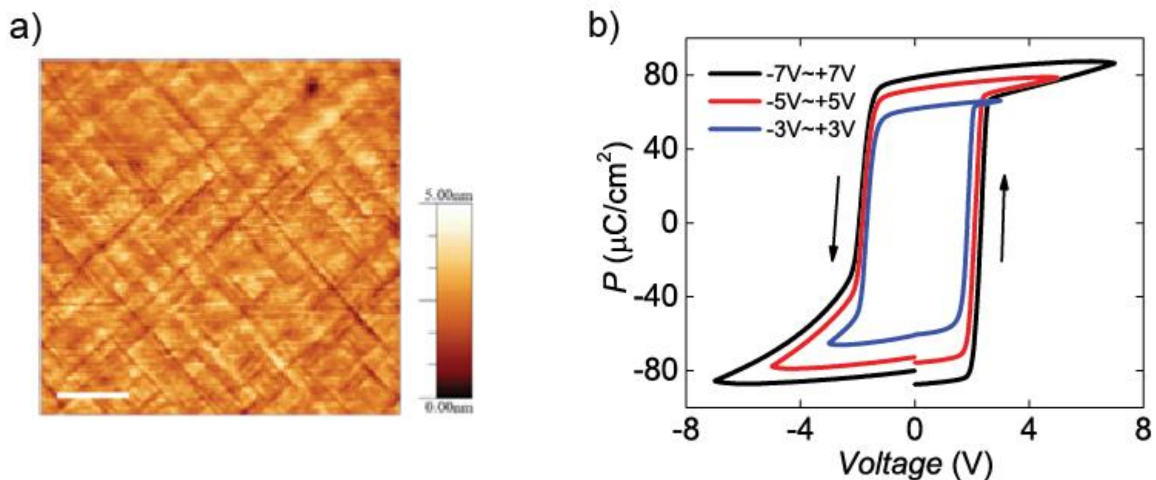



Figure 5.1. a) PZT film surface AFM topography. The scale bar is 1 μm. b) PZT film polarization-voltage loops for different voltage sweep ranges.

$MoS_2$ flakes were mechanically exfoliated from bulk crystals onto a 285nm $SiO_2$/Si substrate (Figure 5.2a). Multilayer $MoS_2$ flakes were chosen for high channel current. The selected $MoS_2$ flake was transferred onto PZT substrates via the dry cutting transfer process mentioned in chapter 4.1. AFM was used to measure the thickness and uniformity of the flake after transfer. As shown in Figure 5.2b, no ripples or ruptures were found, indicating the high fidelity of our transfer process. The measured film thickness is ~ 6.81nm (Figure 5.2c), meaning the layer number is about 10.

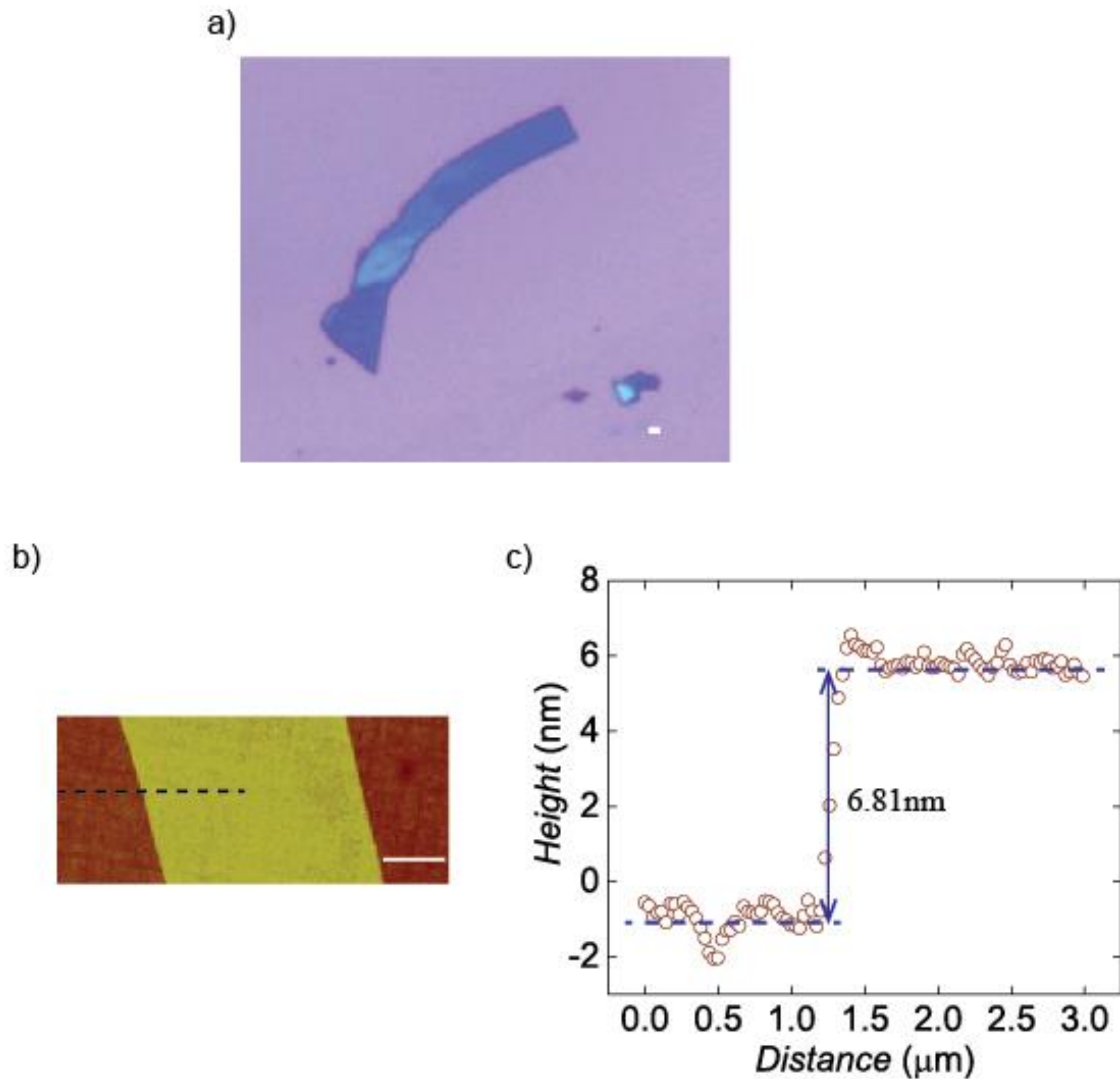



Figure 5.2. a) Optical image of $MoS_2$ flake exfoliated onto 285nm $SiO_2$/Si substrate prior to transfer. b) AFM image of $MoS_2$ flake. The scale bars are both 1μm. c) AFM result of $MoS_2$ flake thickness measurement.

Figure 5.3a depicts the 3D schematic of the back-gate $MoS_2$ transistor. E-beam lithography and metal evaporation were used to pattern 100nm Au film as the source/drain electrodes. The photo of the fabricated multilayer 2D ferroelectric transistor is in Figure 5.3b, where the blue rectangle enclosed by white dashed lines is the $MoS_2$ channel and the yellow patterns are Au electrodes. The channel is 3μm in width and 5μm in length. After lift-off, the device was annealed at 200 ℃ in vacuum for 1 hour to reduce contact resistance [33, 72]. Agilent B1500A Device Analyzer was used for current-voltage measurements carried out in the Lakeshore TTPX high vacuum chamber (pressure below $2\times10^{-6}$Torr). Note that we define the polarization is in the positive direction when it points into the channel; and when it points out of the channel, its polarization

direction is negative.

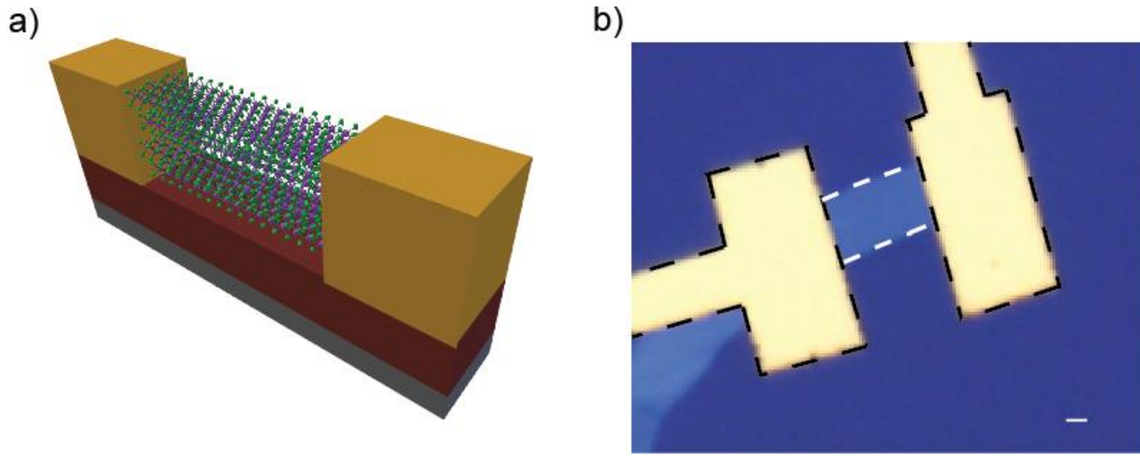



Figure 5.3. a) Schematic of multilayer $MoS_2$/PZT/SRO back-gate transistor. b) Optical image of the back-gate transistor. The scale bar is 1μm.

In the transistor transfer curves (Figure 5.4a), the ON current reached as high as 19μA/μm. Current saturation and a distinct counterclockwise hysteresis window were detected at positive gate voltages. Curves in different scales are overlapping each other. In the reverse sweep direction, the saturation current induced by positive polarization increases with wider sweep ranges. This indicates that the polarization amplitude increases with increasing voltage across the ferroelectric, matching the polarization-voltage results in Figure 5.1b. As depicted in Figure 5.4b, the ON/OFF ratio and subthreshold swing (*SS*) of the transistor reached ~$10^7$ and 92mV/dec respectively, which are comparable to those of previously reported high-quality $MoS_2$ devices [2, 29, 73]. Unlike conventional FeFETs, there is no forward shift in $V_t$, implying that the PZT film's negative polarization was screened. This is likely due to the lack of free electrons in the $MoS_2$ channel's depletion region, resulting in a weaker electric field across the ferroelectric film that is not strong enough to switch the polarization. The red curves in Figure 5.4a show changes in channel current as the gate voltage is swept from −3V to +3V. When the drain voltage $V_d$ is 1V, the hysteresis loop is partially clockwise and partially counterclockwise due to differing polarization states along the channel. This occurs because the maximum voltage across the ferroelectric at the drain side can only reach $V_g - V_d = 2$V while the coercive voltage to switch the PZT film is larger than that value (Figure 5.1b). Consequently, the electric field is not strong enough to switch the ferroelectric at the drain side. In contrast, when $V_d = 0.2$V, the hysteresis loop is counterclockwise because the ferroelectric polarization state is the same at both the source and drain sides. Based on that analysis, we can conclude that the coercive voltage for polarizing the PZT film in the positive direction is between 2.0V and 2.8V. These values are slightly higher than the values obtained in polarization-voltage measurements (about 2.0V from Figure 5.1b), likely due to work function difference between the $MoS_2$ (~ 4.7eV, [74]) channel of the transistor and the Au (~ 5.1eV) electrodes used in the testing PZT capacitor.

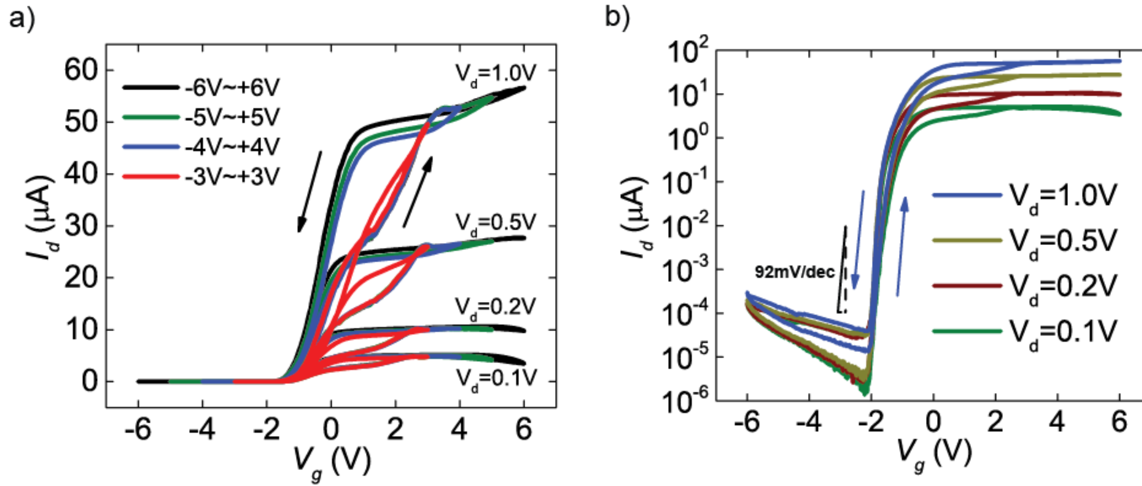



Figure 5.4. a) $I_d$-$V_g$ curves of $MoS_2$/PZT transistor with linear *y*-axis. b) $I_d$-$V_g$ curves of $MoS_2$/PZT transistor with logarithmic *y*-axis.

To characterize the channel current changes and retention in response to gate voltage pulses, a time-resolved two terminal source/drain current measurement with a series of gate voltage pulses from a Keithley 2612B Sourcemeter was carried out. The red curve in Figure 5.5 corresponds to a diagram of the pulse sequence, which has the amplitude of 5V, pulse width $t_{on}$ = 100ms, and pulse period $t_{off}$ = 1s. The resultant drain current over time is shown as the blue curve of Figure 5.5. The pulse-off current after the positive gate voltage pulse was kept at the same level as that when the gate voltage pulse was on, which shows the memory retention from the positive polarization. While after the negative voltage went to zero, the channel current got changed right away, meaning the negative polarization of the PZT was not stable, corresponding to the transfer curves in Figure 5.4a where the threshold voltages didn't shift to the positive side in those forward sweeps.

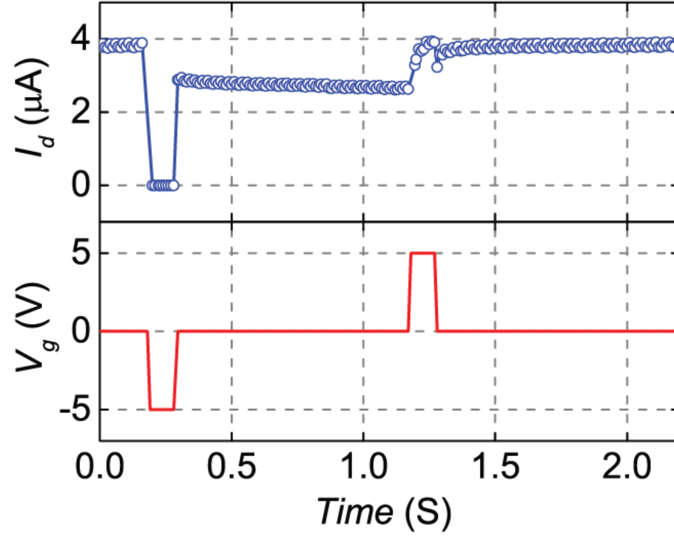



Figure 5.5. Time-resolved channel current changes in response to gate voltage pulse sequences. $V_d = 0.1V$.

Based on the metal-insulator phase transition in $MoS_2$ mentioned in chapter 3.3, since our PZT sample has a large effective dielectric constant (~ 200) and stable positive remnant polarization, we expected a metallic phase after applying a large enough positive voltage pulse to the gate, which will polarize the ferroelectric and dope the channel. +8V voltage pulses ($t_{on}$ = 1ms) generated by an Agilent 81150A function generator were used to fully polarize the ferroelectric gate oxide at different temperatures, and then the source/drain output performance was measured with gate floating. In Figure 5.6a, the linear output curves represent ohmic contacts between source/drain and the channel even at 77K. This implies that contact resistance is negligible and the channel resistance is nearly equal to the source/drain resistance. So the channel conductance could be directly calculated by:

$$G_{MoS_2} = \frac{I_d}{V_d} \tag{17}$$

where $I_d$ and $V_d$ are the channel current and the drain voltage bias (the source was grounded) respectively. In Figure 5b, the channel conductance increases with decreasing temperature, meaning that $MoS_2$ is in the metallic phase after positive polarization.

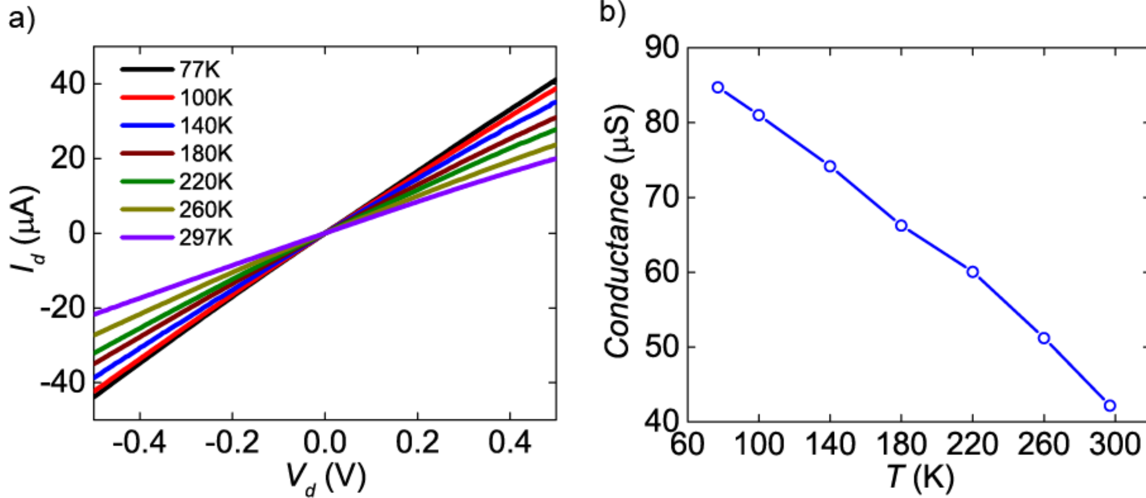



Figure 5.6. a) 2-terminal source/drain current at different temperatures after applying 8V positive gate voltage pulses. b) Channel conductance at different temperatures.

As a brief summary, our multilayer $MoS_2$/PZT n-type ferroelectric transistor shows great electrical performance and several other advantages compared to that of traditional 2D MOSFETs. PZT polarization dominates and results in a repeatable counterclockwise hysteresis loop. When the PZT is positively polarized, it dopes the channel, enhancing electron density and improving retention, then turning $MoS_2$ metallic. These results show the potential of TMD for using in next-generation memory devices. Moreover, the 2D ferroelectric structure can be a better device system for analyzing certain phase transition materials because they can be electrostatically doped without the need for a continuous voltage bias.

## 5.2 External PZT Capacitor Connection

Furthermore, to totally avoid robust trapping states on the interface between a ferroelectric layer and a 2D material and get intact correct handedness hysteresis loops, a combined system was designed in which an $MoS_2$ top-gate transistor was externally connected to a ferroelectric metal-insulator-metal (MIM) capacitor via probe tips and a cable (Figure 5.7). This structure prevents direct contact between the $MoS_2$ channel and the PZT oxide so that there will be no interface trap generated by direct coupling between 2D and ferroelectric materials at all.

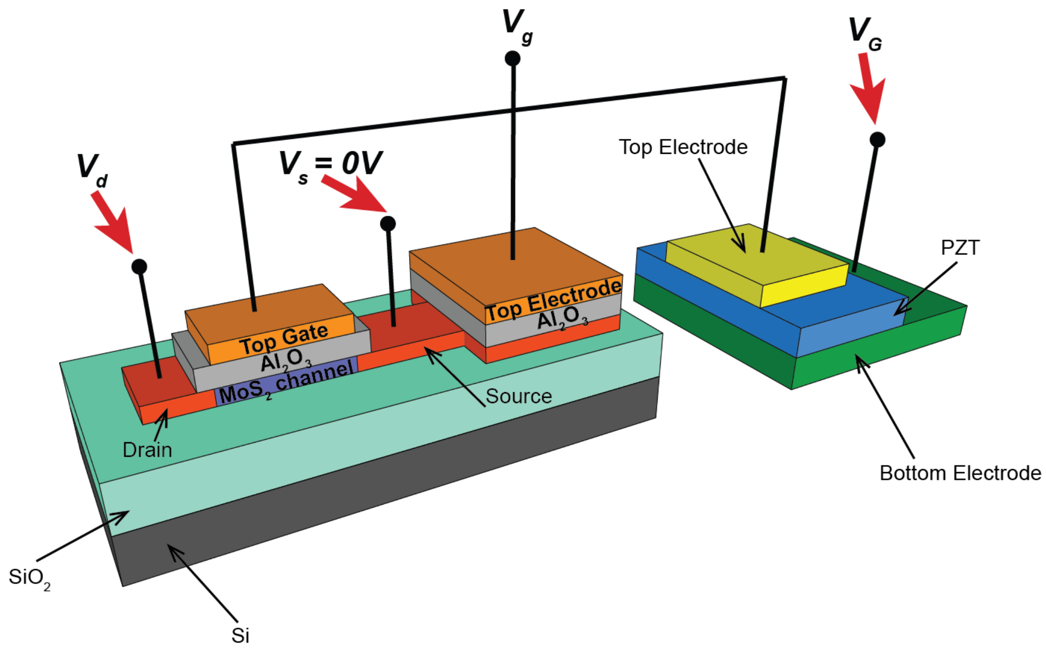



Figure 5.7. 3D schematic of the transistor and a parallel dielectric capacitor externally connected with an external PZT capacitor.

First of all, an $MoS_2$ top-gate dielectric transistor was fabricated on a 285nm $SiO_2$/Si chip. Optical microscopy was used after flakes exfoliation to locate the optimum ones (Figure 5.8a). Then atomic force microscopy (AFM) was used to measure the precise thickness of the selected flake (2.1nm, corresponding to a trilayer $MoS_2$ flake) (Figure 5.8b). A mesa region was defined as the transistor's channel and the remaining parts were etched away by $XeF_2$ gas.

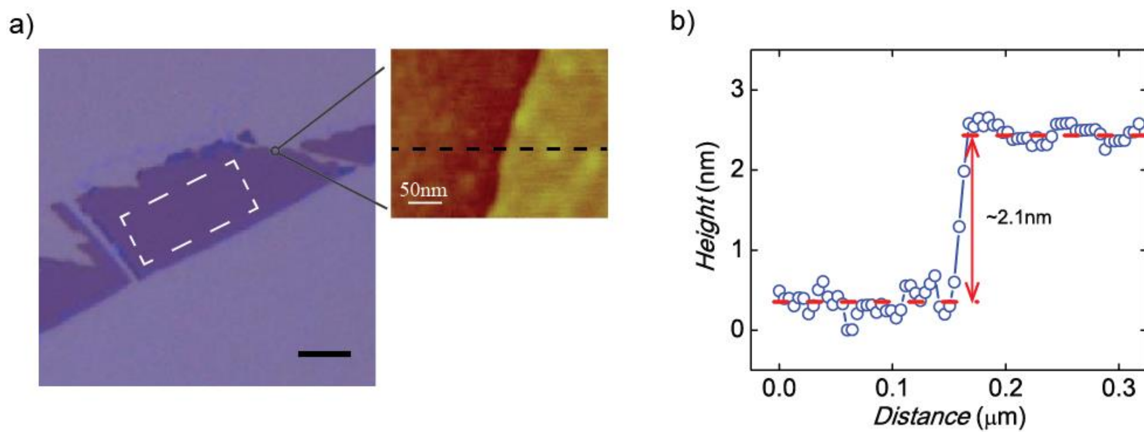



Figure 5.8. a) The optical image and AFM topography of the $MoS_2$ flake. The region enclosed by dashed lines is the remaining channel area after dry etching. The black scale bar is 5μm. b) The step height of the $MoS_2$ flake is ~ 2.1nm.

Au(50nm)/Ti(10nm) source/drain electrodes were evaporated after e-beam lithography patterning (Figure 5.9a), together with probes (P1 and P2) on the channel for the 4-point sensing later. The channel length $L_{total}$ is 8μm, and the width $W$ is 5μm. 20nm $Al_2O_3$ layer was deposited over the $MoS_2$ channel via 200 ℃ thermal atomic layer deposition (ALD) to form the gate dielectric with 1 nm of evaporated $SiO_x$ as the nucleation layer [75]. Finally, the top-gate electrode was defined ($L_g$ = 5 μm) and patterned with an Au(50nm)/Ti(10nm) metal stack. A 40μm×40μm $Al_2O_3$ dielectric capacitor was added in parallel during the transistor fabrication process, with pads connected to the source and gate separately (Figure 5.7 and Figure 5.9a). The capacitor was designed to increase the total capacitance of the transistor to the same order of magnitude as that of the ferroelectric capacitor (FE) used later. The total capacitance of the entire baseline system (the transistor combined with the parallel capacitor) was measured as 4.4pF (Figure 5.9b). This value did not vary with gate bias at a low excitation frequency (100kHz), implying that the parallel capacitor dominates in this system since its area is much larger than the channel's. The redielectric constant of $Al_2O_3$ here was calculated as 6.22, which is lower than its real value (~ 7.6, [29]) because the 1 nm $SiO_x$ ($\varepsilon_{SiOx} < 3$) nucleation layer increases the effective oxide thickness (EOT).

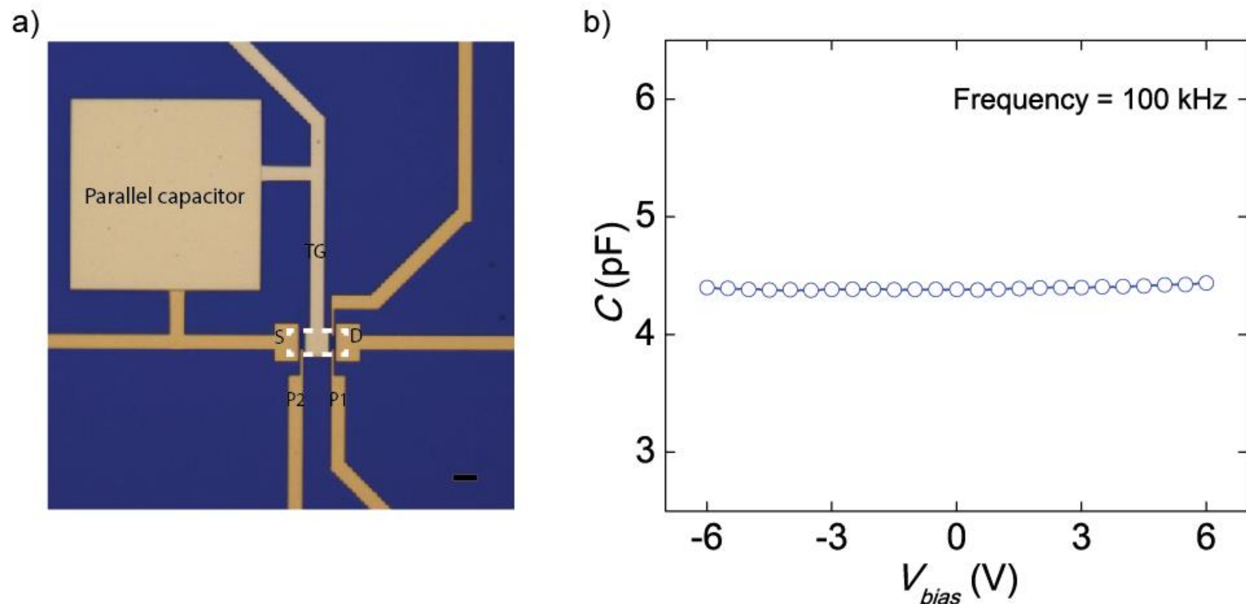



Figure 5.9. a) Optical image of fabricated top-gate transistor. The channel is outlined with dashed lines, and the scale bar is 5μm. b) The baseline system's total capacitance measured at 100 kHz.

The baseline transistor's electrical properties were characterized by an Agilent B1500A Device Analyzer in Lakeshore TTPX (~ $2\times10^{-6}$Torr) at room temperature (300K). As shown in Figure 5.10a, the transistor has reasonable subthreshold swing ($SS$ = 166mV/dec) and high ON/OFF ratio (> $10^6$). The clockwise hysteresis loops in the transfer curves originate from interface trapping states [76].

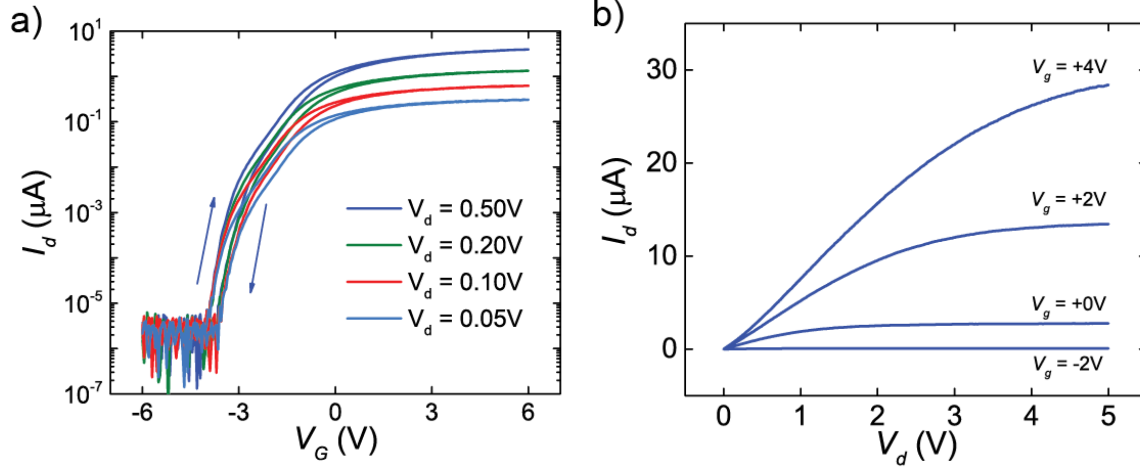



Figure 5.10. a) Transfer curves b) Output characteristics of the of the baseline top-gate transistor.

In the output curves (Figure 5.10b), the ON current $I_{on}$ could reach 28.5 μA, which is similar to those of previous reports [77, 78]. The sub-linear increase in channel current ($I_d$) with drain voltage ($V_d$) in the low drain voltage region confirmed the existing of Schottky barriers between $MoS_2$ and Au/Ti contacts, which result from Fermi level pinning [31]. To exclude the effects of Schottky contacts, 4-point sensing was used to get the channel conductance. Based on the measured drain current $I_d$ and the voltage difference $V_{12}$ between probe 1 and 2 on the channel, the channel conductance $G$ is:

$$G = \frac{I_d}{V_{12}} \tag{18}$$

In the linear region of Figure 5a, the slope $dG/dV_g$ was calculated to be 3.32 μS/V. Then the field effect mobility $\mu_{FE}$ was computed as ~ 14.5cm$^2$V$^{-1}$s$^{-1}$ using the equation:

$$\mu_{FE} = \left(\frac{L_{12}}{W}\right) \times \frac{dG/dV_g}{c_g} \tag{19}$$

where $c_g$ = 0.275 μF/cm$^2$ is the gate capacitance per unit area, $G$ is the channel conductance, and $L_{12}$ = 6 μm and $W$ = 5 μm represent the probe separation distance and the channel width respectively. The mobility value is limited by Coulomb scattering from ions, defects, and interface trapping states in addition to the dominant phonon scattering effect. To explore more details about the dominate mechanism limiting the mobility values, the 4-point sensing was carried out repeatedly at different temperatures. Figure 5.11b shows the channel conductance values extracted at different temperatures. There is a well-defined crossover point at $V_g$ = 2.61V, which represents the transition from an insulating phase to a metallic phase. In the low gate voltage region, $MoS_2$ is in the insulating phase in which electrons are primarily localized by impurities or localized states and transport through variable range hopping [33]. As temperature increases, thermal excitation enhances the hopping transport, resulting in higher channel conductance. With large enough gate voltage, the carrier density becomes high enough to result in strong Coulomb interactions between electrons to screen the localization states—phonon scattering becomes the primary scattering mechanism, and the phase becomes metallic. Hence at

lower temperatures, the phonon energies decrease, and the conductance increases. The critical carrier density at which MIT occurs for this trilayer $MoS_2$ flake is $n_c \approx 5.64\times10^{12}cm^{-2}$, which was calculated from:

$$n_c = \frac{c_g(V_g - V_t)}{q} \tag{20}$$

where $V_g = 2.61V$ is the gate voltage at the crossover point, $V_t = -0.67V$ is the threshold voltage (captured from Figure 5.11a), and $q = 1.6\times10^{19}C$ represents the charge of an electron. This carrier density value is similar to those in previous reports [48, 79].

And the temperature dependent mobility changes are plotted in Figure 5.11c. The slope here is the damping factor $\gamma$. At room temperature, optical phonon scattering dominates the mobility damping. Due to the quenching of homopolar phonon modes by the encapsulated structure, monolayer $MoS_2$ is expected to have a $\gamma$ of around 1.52 [80]. Our result $\gamma \sim 1.8$ is similar to that of some reports about multilayer films [30, 81], implying that thin film $MoS_2$ still behaves much like a 2D system. At 77K, as the device is cooled, thermal vibrations inside $MoS_2$ become weaker, resulting in the mobility to gradually increase to its maximum value of $59cm^2V^{-1}s^{-1}$. Here most optical phonons are frozen, allowing acoustic phonons ($\gamma = 1$) [80] and variable-range hopping ($\gamma = 1/3$) [82] to play leading roles in limiting the mobility and contributing to our measured result $\gamma \sim 0.8$.

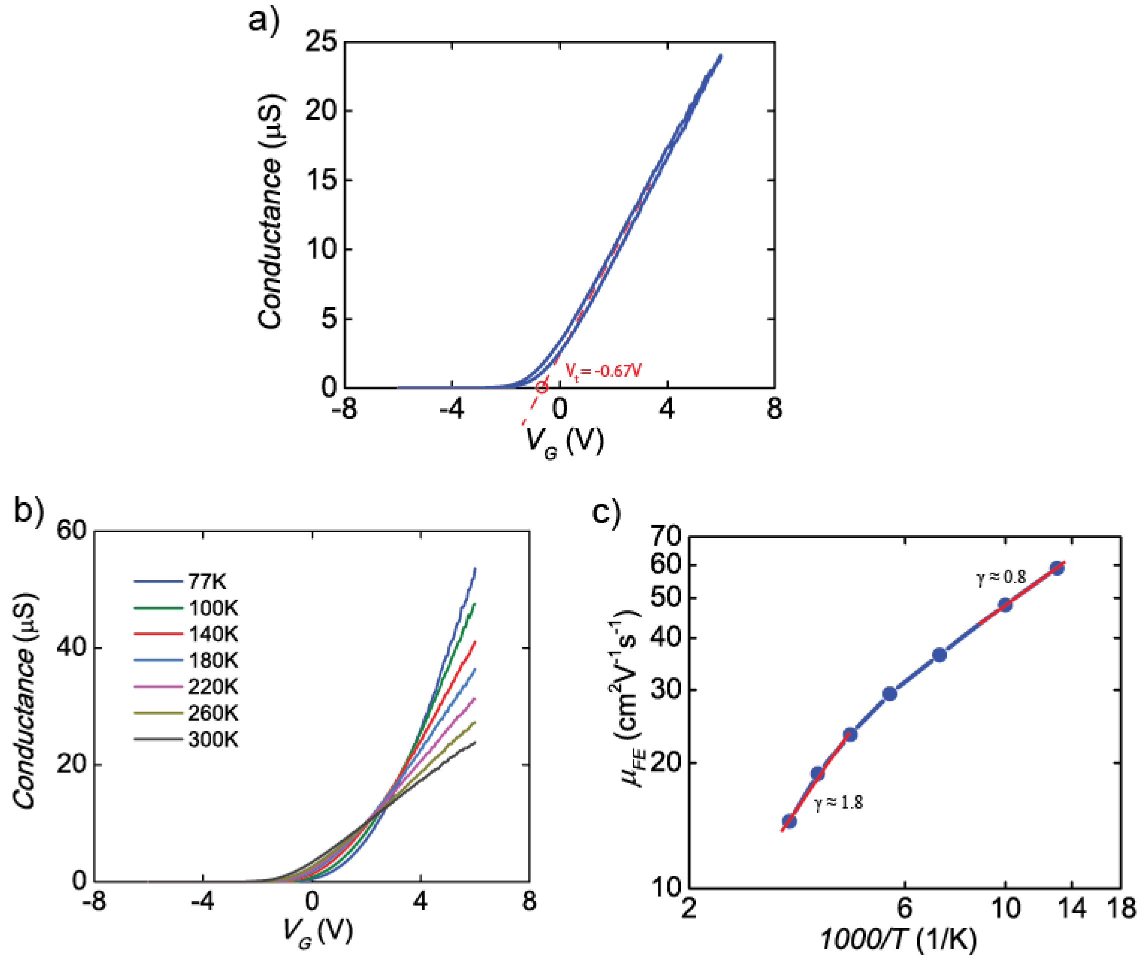



Figure 5.11. a) Conductance versus gate voltage. The threshold voltage is marked as -0.67V. b) Temperature-dependent conductance measurement. c) Log-log plot of field-effect mobility $\mu_{FE}$ versus inverse temperature 1000/*T*.

To avoid the interface states between $MoS_2$ and the ferroelectric layer, instead of direct contacting, a $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) ferroelectric capacitor was externally connected to the transistor (Figure 5.7). The capacitor was made by patterning a square Platinum (Pt) electrode pad on the surface of PLD grown PZT/SRO/STO heterostructure and connecting it to the bottom electrode (SRO) (Figure 5.12a). The FE capacitor has a size of 30 μm × 30 μm (Figure 5.12b).

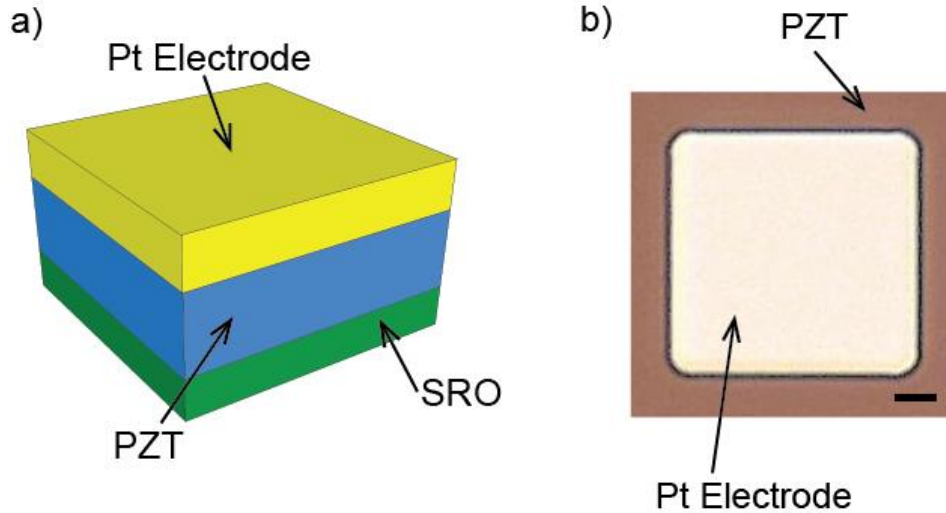



Figure 5.12. a) The 3D schematic structure of Pt/PZT/SRO ferroelectric capacitor. b) The optical image of the PZT capacitor. The scale bar here is 5μm.

The PZT film's CV characteristics are shown in Figure 5.13a. The measurements were performed at 100 kHz with the Agilent B1500A Device Analyzer. The effective dielectric constant varied between 65 and 110 at different voltages, corresponding to the nonlinear polarization of the PZT film. Those measured admittance angles were all nearly 90 ° in the non-switching regions, indicating that the film has excellent insulating capability. The polarization characteristics of PZT at different temperatures are depicted in Figure 5.13b. Those closed hysteresis loops signify low leakage current at all the temperatures. The remnant polarization magnitude reached a maximum of ~ 65 $\mu C/cm^2$, and remains virtually unchanged with temperature changes, while the coercive voltage increases as the temperature decreases. These temperature-dependent properties have been reported for other ferroelectric materials as well [83]. Since the remnant polarization is approximately constant at different temperatures, the corresponding electron doping density induced by it can also be regarded as independent of temperature.

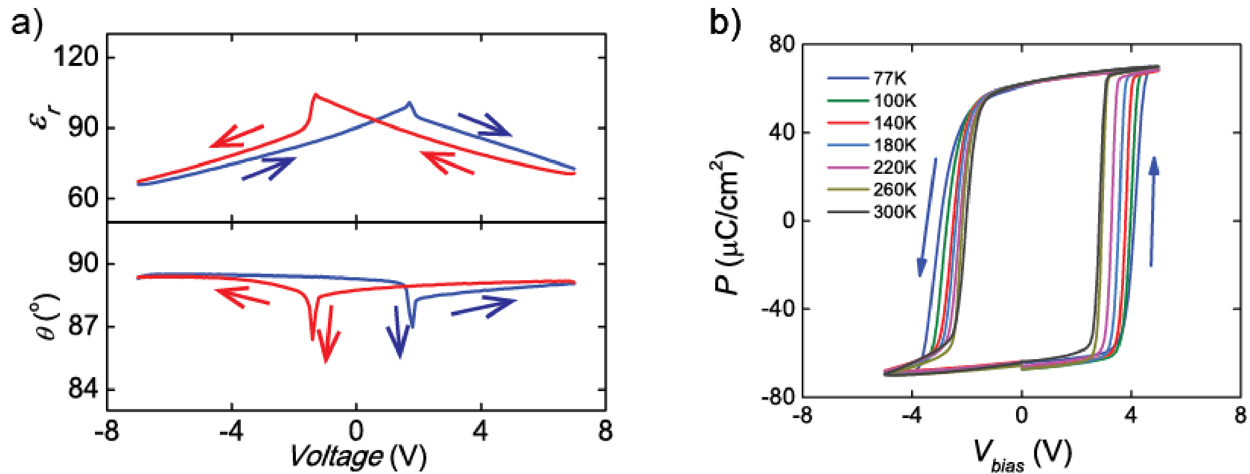



Figure 5.13. a) Dielectric constant $\varepsilon_r$ and admittance angle $\theta$ versus voltage. b) Hysteresis loop of the PZT capacitor at different temperatures.

In the equivalent circuit model (Figure 5.14a), the charge $Q_{FE}$ on the ferroelectric capacitor should be the same as the charge $Q_{DE}$ stored in the baseline system ($|Q_{FE}| = |Q_{DE}| = |Q_{ox}| + |Q_{parallel}|$). Thus, the carrier density in the $MoS_2$ channel can be tuned by switching the FE capacitor. As mentioned in Figure 5.9b, the total capacitance of the baseline transistor combined with the parallel dielectric capacitor was $C_{DE}$ = 4.4pF. And the capacitance of the FE capacitor was regarded as a constant value of 6.5pF in order to simplify the analysis. The transfer characteristics of the combined system (with the external FE capacitor connected) are shown in Figure 5.14b. The intact counterclockwise hysteresis loops correspond to the ferroelectric switching [11]. The loops at different drain voltages have the same window size and start/end points, which mean that the switch-induced doping mechanism is stable. Comparing the transfer curve with that without external FE capacitor connection (Figure 5.14c) emphasized the effects of ferroelectric polarization in determining the hysteresis loop direction. Shifts in $V_t$ follow the switches of the FE capacitor. When sweeping in the forward direction, $V_t$ is shifted positive relative to that of the baseline transistor, implying that the ferroelectric polarization is pointing out of the transistor and depleting the channel of electron carriers. At the end of the forward sweep (i.e. after reaching the coercive voltage), the ferroelectric polarization switches to point into the transistor, enhancing the electron carrier density in the channel. Thus, when sweeping in the reverse direction, $V_t$ is shifted negative relative to that of the baseline transistor. The system's large ON/OFF current ratio (~ $10^7$) and large hysteresis loop demonstrate the system's potential for use in next-generation ferroelectric memory units.

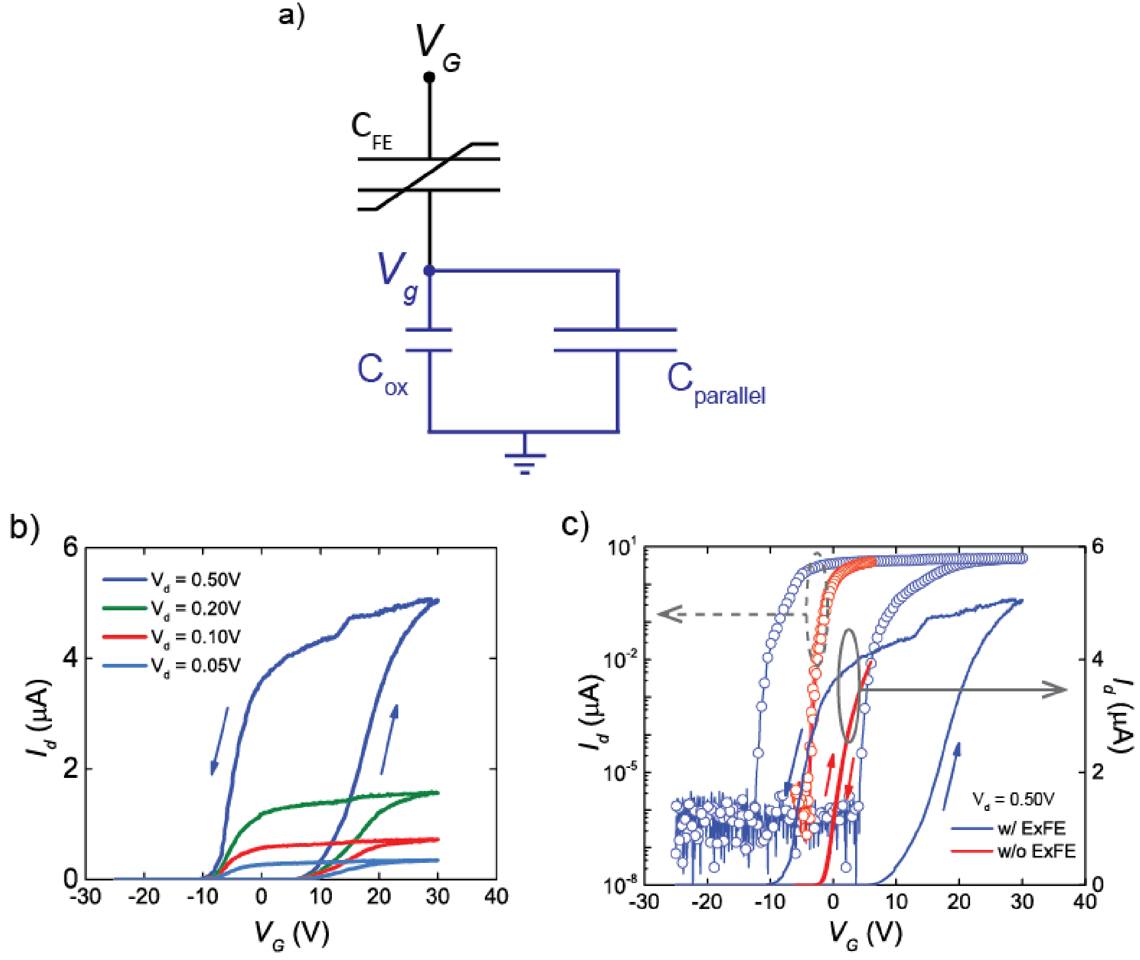



Figure 5.14. a) Equivalent circuit model of the overall system. b) Transfer characteristics for different drain voltages when the system is connected to an external PZT capacitor. c) Transfer characteristics of the $MoS_2/Al_2O_3$ transistor with and without the external PZT capacitor connection.

The effective gate voltage shift $\Delta V_{geff}$ in the baseline $MoS_2$ transistor is 10.2V, derived by:

$$\Delta V_{geff} = \Delta V_G \left(\frac{C_{FE}}{C_{FE} + C_{DE}}\right) \tag{21}$$

in which $\Delta V_G$ is read out from Figure 5.14a as the width of the hysteresis loops there. The doping density induced by the ferroelectric switching is $\Delta n_{doped} = \frac{1}{2}\left(\frac{c_{ox}\Delta V_{geff}}{q}\right) \approx 7.8\times10^{12}\text{cm}^{-2}$, which is larger than the critical charge density $n_c = 5.64\times10^{12}\text{cm}^{-2}$ needed to trigger the phase transitions [48]. This indicates that it is feasible to control the MIT with a series FE capacitor. Figure 5.15a shows the temperature-dependent changes in conductance for our combined system. Notice that the counterclockwise hysteresis loops consistently remain intact, and there is a crossover point in the forward sweep direction. This crossover voltage is shifted in the positive direction significantly more than the baseline transistor's original value from Figure 5.11b. This is because the ferroelectric polarization is oriented out of the channel, resulting in a depletion effect. In the

reverse sweep, the system retains its metallic conducting behavior, especially at the "gate voltage off-state" ($V_G$ = 0V). This could be due to the varying shifts in threshold voltage from temperature-dependent interface trapping [84]. At lower temperatures, the interface states in the top-gate transistor freeze out and do not have enough energy to interact with the channel carriers. If we compare the trends of the forward and reverse sweep directions at a specific voltage below the crossover point (e.g. 13V as in Figure 5.15b), then we find that $MoS_2$ can be in either of two phases at the same voltage. This implies the existence of switchable phases in our $MoS_2$/external FE capacitor system similar to those described in superconductors [85, 86].

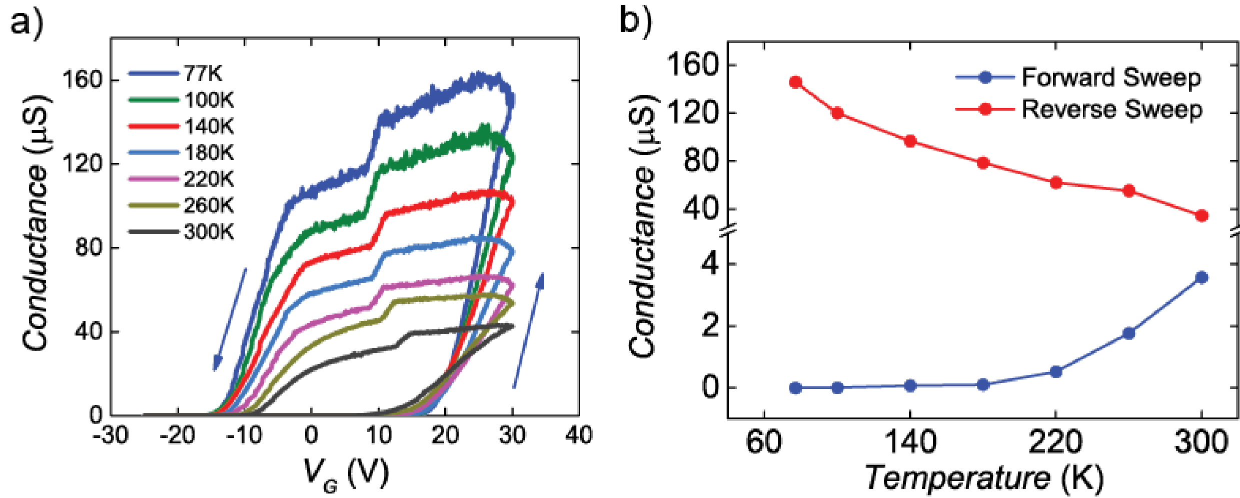



Figure 5.15. a) Conductance versus gate voltage at different temperatures with the external PZT capacitor connected. b) Conductance versus temperature at the same gate voltage (+13 V) when $V_G$ is swept in the forward and reverse directions.

In summary, we designed an electrical system combining an $MoS_2$ dielectric transistor with a ferroelectric capacitor that finally exhibits an intact hysteresis loop with correct handedness in its transfer curves, convincing the promising future of that combined system in the application of next generation memory unit development. Moreover, the temperature-dependent measurements reveal a metallic off-state as well as a switchable metal-insulator transition in the system.

# Chapter 6. Hysteresis Loops in Two Dimensional Dielectric Transistors and Pulsed Measurement

## 6.1 The Trapping States in 2D Dielectric Transistors

As mentioned previously in chapter 4.3, when the 2D dielectric transistors are characterized under typical ambient conditions, molecules such as oxygen, water vapor, etc. can adsorb at the interface between the channel and the gate oxide. This typically results in the formation of trapping centers at the interface. Those interface states will participate in trapping/detrapping electrons from the semiconductor channel, causing the counterclockwise hysteresis loops in the transfer curves of n-type $MoS_2$ transistors.

The trapping mechanism can be understood from the schematics shown in Figure 6.1. The thermal average occupancies of these interface states are described by the Fermi-Dirac distribution:

$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}} \tag{22}$$

Consequently, interface states with energies above the Fermi level are less likely to trap electrons while states with energies below the Fermi level are mostly full of trapped electrons. When a negative voltage is applied to the gate, the energy bands in the channel bend upwards near the oxide-channel interface as depicted in Figure 6.1a. This results in previously occupied states to rise in energy above the Fermi level, resulting in detrapping of electrons and increased channel current. On the other hand, when a positive gate bias is applied (Figure 6.1b), states previously unoccupied will decrease in energy below the Fermi level, resulting in trapping of electrons and reduced channel current.

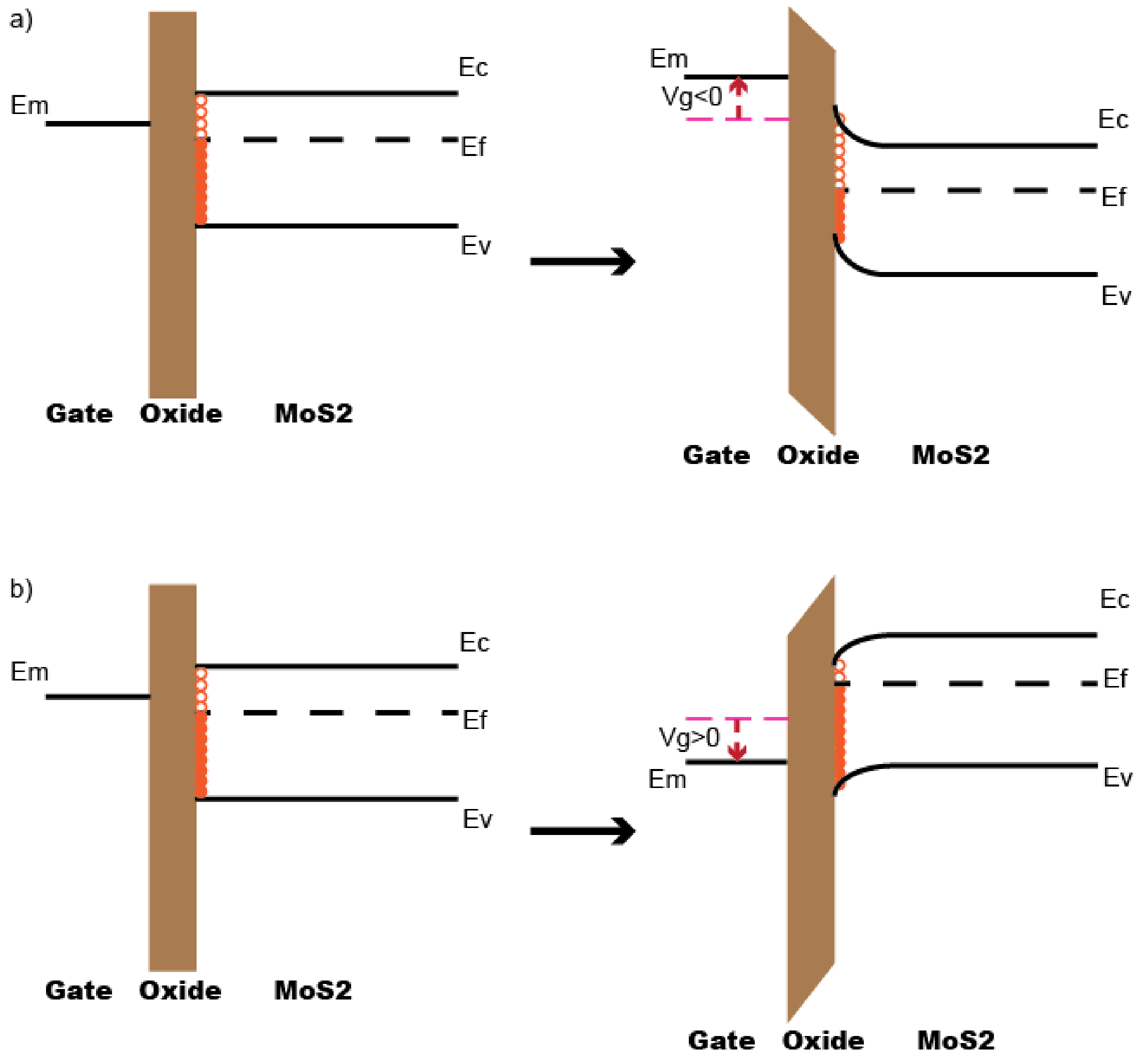



Figure 6.1. Schematics of interface trapping states changing occupancy when a gate bias is applied in the a) negative direction and in the b) positive direction.

As a result, nearly all experiments consisting of a DC sweep of the gate voltage show large hysteresis in the transfer curve.

The non-volatile functionalities in the 2D dielectric transistors are highly undesirable. For example, the traps can continuously change the threshold voltage as a function of gate bias, and they can also significantly reduce ON current. Furthermore, the two branches of the hysteresis loop are typically different and usually depend on the initial condition, sweep rate, etc. Therefore, critical parameters such as mobility—which is extracted from the slope of the transfer characteristic ($I_d$-$V_g$)—can no longer be reliably estimated. When it comes to memory, as mentioned before (chapter 1.1), the hysteresis loop sizes in the 2D dielectric transistors could be

easily changed by several external factors, like sweep scales and sweep intervals, degrading the reliability and endurance performances.

Later in chapter 6.2, we will show that the hysteresis depends on different parameters that can be exploited to quantify the nature and density of the trap states. Such information can provide important insight for engineering the oxide-channel interface to optimize device performance. We will then show that by applying carefully designed pulses to the transistor gate, the effect of the trap states can be completely removed. This eliminates the hysteresis and reveals the intrinsic nature of the material itself.

## 6.2 Hysteresis Analysis Depending on Different Parameters

To analyze the interface states, a monolayer $MoS_2$ dielectric transistor was fabricated on a 72nm $Al_2O_3$/Si substrate. $Al_2O_3$ (deposited on heavily doped p-type Si by ALD) with that specific thickness was chosen here since 1) the relative constant ($\varepsilon_0$) of $Al_2O_3$ (~ 7.6 [29]) is higher than that of $SiO_2$ (~ 3.5), which could help reduce the back-gate voltage sweep scales; 2) the color contrast of $MoS_2$ on 72nm $Al_2O_3$ was convinced to be great derived by the model in [42], so direct exfoliation could provide visible monolayer films under the optical microscope. Then the conventional back-gate transistor fabrication steps (in chapter 3.2) were carried out and the source/drain stacks were Au(60nm)/Ti(10nm). The schematic structure of the fabricated transistor is in Figure 6.2a, and the images of the exfoliated monolayer $MoS_2$ flake before/after fabrication are in Figure 6.2b and 6.2c respectively.

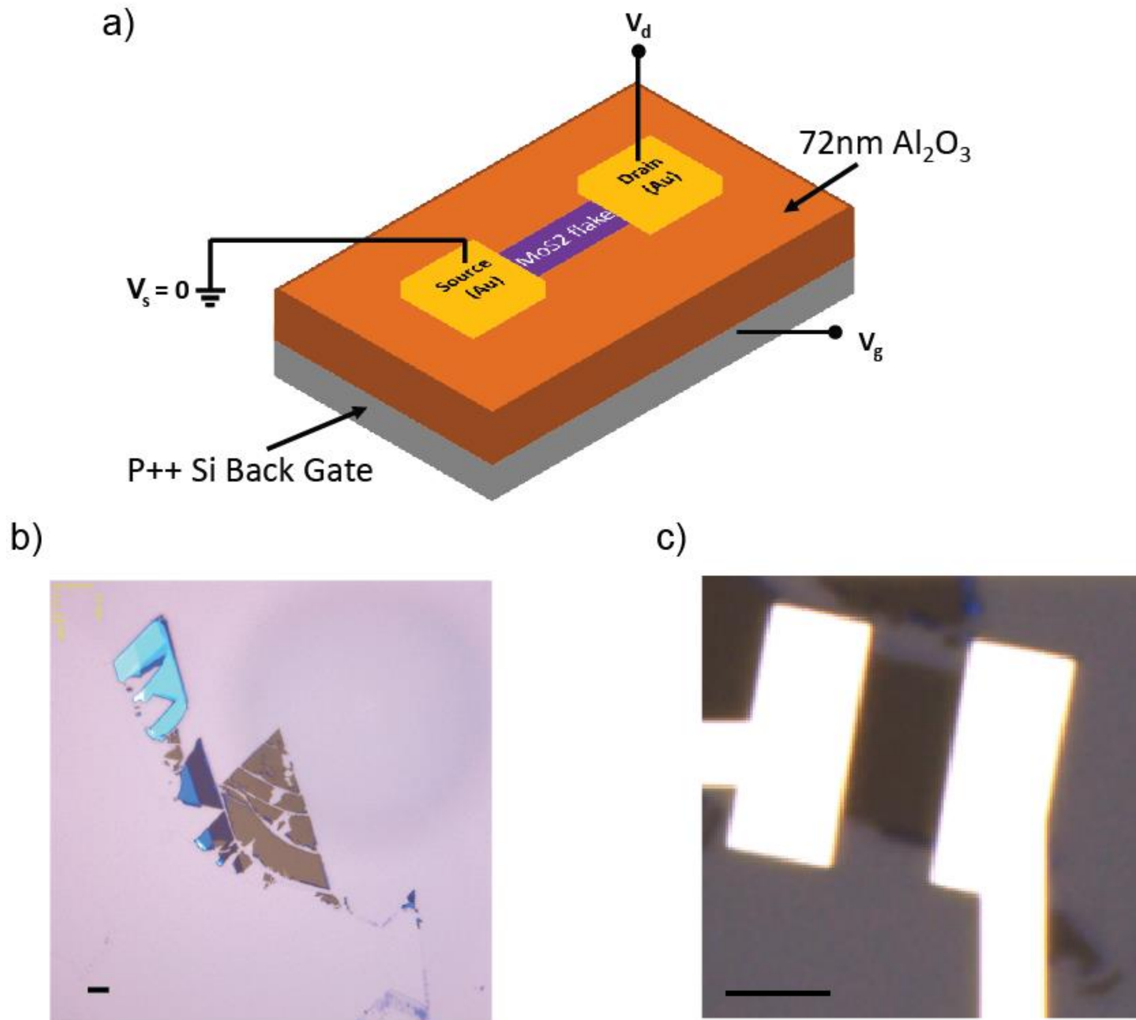



Figure 6.2 a) The schematic structure of $MoS_2$ back-gate dielectric transistor used in the interface states analysis. b) The optical image of exfoliated monolayer $MoS_2$ flakes. c) The optical image of the monolayer $MoS_2$ back-gate transistor. The scale bars are both 5 μm.

All the electrical characterizations were done in dark condition and ambient environment. As the gate voltage is swept back and forth, a clear hysteretic behavior is observed (Figure 6.3). We have characterized this hysteresis by varying different test parameters. Figure 6.3a shows the $I_d$ - $V_g$ behavior when gate voltage is swept from -20V to +20V and then back to -20V with different sweep intervals. Notice that with higher sweep interval values (i.e. fewer sweep points), the hysteresis window is narrower, and the ON current at 20V is higher. Figures 6.3b and 6.3c show the transfer characteristics for different starting voltages while keeping the sweep interval unchanged. It is clear that a more negative starting voltage leads to a negative shift in threshold voltage. We can now use this observation to understand the nature and distribution of the trap centers.

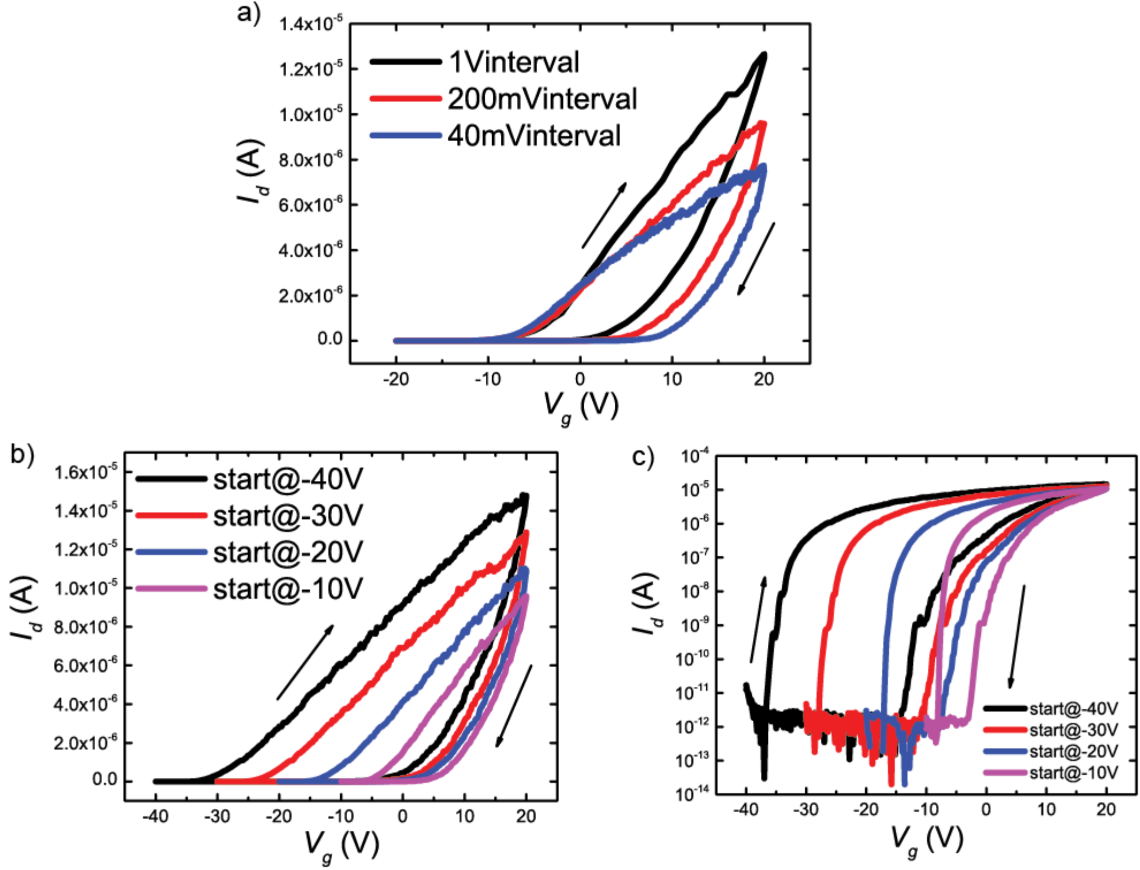



Figure 6.3. a) $I_d$-$V_g$ curves with different sweep intervals. b) & c) $I_d$-$V_g$ curves in linear axes (b) and in log y axis (c) with different starting voltages from -40V to -10V, with the same ending voltage (+20V). The sweep interval is kept unchanged at 200mV. Drain voltages are all 1V.

Note that once the trapping/detrapping occurs, a reasonably long relaxation period is needed before the interface states can return to their initial conditions, even after the gate bias has been removed. This is responsible for the speed-dependent and scale-dependent hysteresis seen in Figures 6.3a and 6.3b.

From Figure 6.3c, we see that the subthreshold swing (*SS*) degrades as the DC sweeps are started at increasingly negative voltages (Table 1). This observation allows us to estimate the effective density of interface states from [87]:

$$SS = \ln(10)\left(\frac{kT}{q}\right)\left[1+\frac{q}{C_{ox}}\left(\sqrt{\frac{\varepsilon_{ch}N_a}{4\varphi_B}}+qD_{it}\right)\right] \tag{23}$$

Here we neglect the effect of channel depletion capacitance since the changes in *SS* value due to different starting voltages are significantly larger than the ideal *SS* value of 60mV/dec. Table 1 considers the *SS* at a fixed channel current of 10nA for different sweep parameters while keeping all other channel conditions constant.

|  | **$SS$@10nA(V/dec)** |
|---|---|
| **-40V start** | **1.50** |
| **-30V start** | **1.36** |
| **-20V start** | **1.12** |
| **-10V start** | **0.653** |

Table 1. *SS* values at 10nA channel current for different starting voltages.

The calculated interface state density ($D_{it}$) results are shown in Table 2. The interface traps are found to have an energy-dependent distribution; there are more interface states at higher energies. Our results are consistent with those of previous studies that used optical techniques [76].

|  | **$D_{it}$@10nA($10^{12}$/cm$^2$.eV)** |
|---|---|
| **-40V start** | **17.3** |
| **-30V start** | **15.7** |
| **-20V start** | **12.9** |
| **-10V start** | **7.53** |

Table 2. Density of interface states for different starting voltages.

## 6.3 Pulsed Measurement

Pulsed measurement was introduced to analyze the transistor's $I_d$-$V_g$ characteristics. Instead of applying DC voltages to the gate, a sequence of voltage pulses with equal durations but different amplitudes was applied. The delay between pulses provided a relaxation period during which trapping/detrapping states could recombine. By varying parameters such as pulse width ($t_{on}$) and pulse period ($t_{off}$), the hysteresis loop induced by adsorbates was minimized, and the ON-current

was optimized. A Keithley 2612B SourceMeter controlled by a LabVIEW program was used to generate a series of $V_g$ and $V_d$ bias voltages while simultaneously measuring $I_d$.

Two different pulse series were used for the measurement. In the "normal" pulse series (Figure 6.4a), the pulse amplitude gradually decreases or increases in magnitude, but the polarity only switches after half the waveform period [88]. In contrast, in the "zigzag" pulse series (Figure 6.4b), each voltage pulse is followed by a pulse of equal amplitude and duration but opposite polarity to offset trapping/detrapping effects [89, 90]. The pulses of opposite polarity help to equilibrate the interface states. For example, electrons detrapped by a negative $V_g$ pulse are retrapped by the subsequent pulse of opposite polarity (a positive $V_g$ pulse). Thus, the two effects cancel each other to let the channel "forget" the previous history and the hysteresis loops disappear.

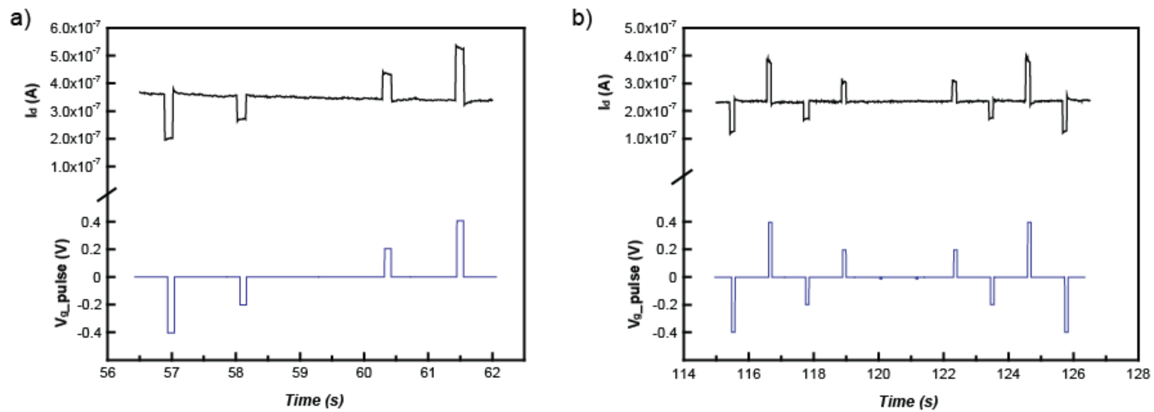



Figure 6.4. a) Part of the normal pulse series and the corresponding $I_d$-*Time* curves. b) The zigzag pulse series setup and the corresponding $I_d$-*Time* curves.

To detect the time-resolved response of the channel current to the voltage pulses generated in the pulsed measurement, a function generator (Agilent 81150A) was combined with a semiconductor device analyzer (Agilent B1500A). The setup is shown schematically in Figure 6.5. The device analyzer connects the source/drain terminals of the transistor and records changes in current induced by changes in gate voltage. The function generator and device analyzer are started simultaneously controlled by a LabVIEW program.

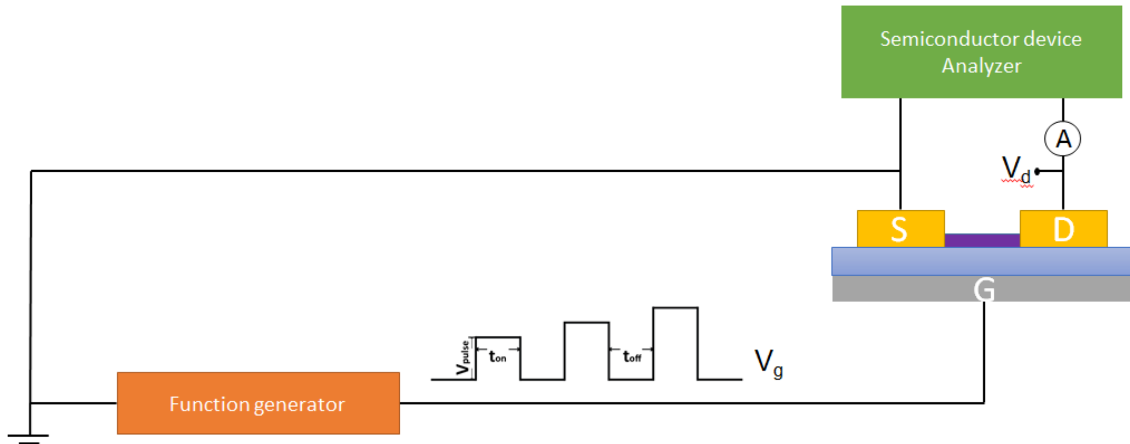



Figure 6.5. Setup for time-resolved detection of changes in channel current induced by pulsed gate voltage.

## 6.4 Result Analysis

For the normal mode pulse series, the time-resolved changes in current versus sweeping gate bias are shown in Figure 6.6a. The current clearly decays after each pulse, corresponding to the trapping/detrapping mechanism. In Figure 6.6b, the normal pulsed measurement mode results are compared with the DC transfer curve for the same sweep scale (-20V → +20V) and interval (200mV). The time needed to capture one point in DC measurement is about 100ms without any relaxation period between consecutive points. With 100ms pulse width and 100ms relaxation period, the effects of interface trapping are dramatically reduced, and the ON current increases. When reducing the pulse width to 1ms—thereby decreasing the time during which trapping/detrapping can occur—the interface effects are further minimized, leading to an enhancement of channel current by nearly 4 times compared to that of the DC mode. 1ms pulse width and 100ms relaxation period appear to be the optimal measurement parameters. No further enhancement was observed for longer relaxation periods within the limit of our measurement instruments. This indicates that time needed for detrapping is significantly long.

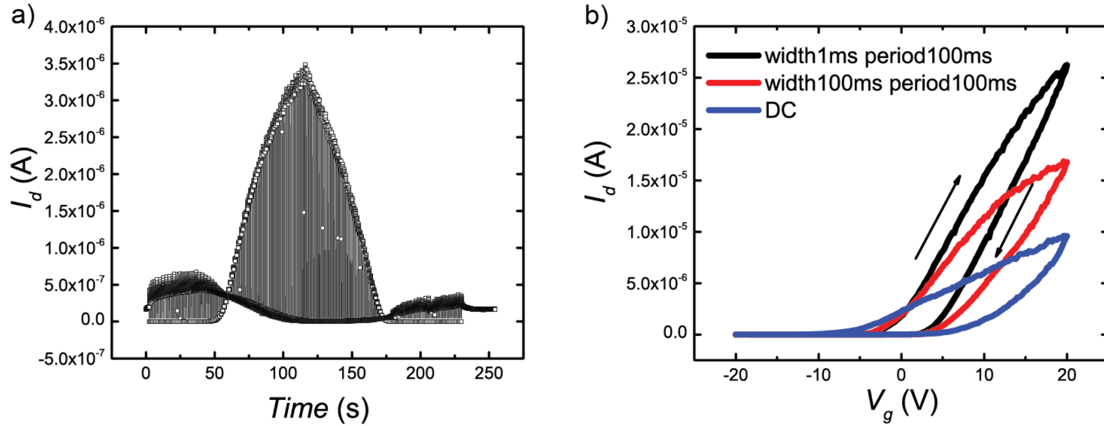



Figure 6.6. a) Complete $I_d$-*Time* curve produced by the normal pulse series. b) Normal pulsed measurement $I_d$-$V_g$ curves compared with DC mode. Drain voltages are all 1V.

Next, the zigzag pulse series was set up in which a voltage pulse follows another one with the same amplitude but opposite polarity (e.g. -20V, 20V, -19V, 19V, …, 19V, -19V, 20V, -20V). Figure 6.7a shows the time domain behavior of the drain current. The result is fairly symmetrical, especially in the low voltage region (100s ~ 150s). Figure 6.7b shows a comparison of the $I_d$-$V_g$ behavior measured by the normal pulse mode and the zigzag pulse mode. Notably, for the zigzag mode, the hysteresis is significantly smaller. In fact, the hysteresis completely disappears in the linear region (0V → 10V). Moreover, the curves with 1ms pulse width and 100ms relaxation period nearly overlap each other. The curves with different sweep scales ranging from ±10V to ±30V also nearly overlap each other as shown in Figure 6.7c. The threshold voltage stays at around -1.5V for all measurements done in the zigzag mode, showing a lightly n-doped $MoS_2$ property. Thus, the zigzag pulse mode is a robust method for measuring the transfer characteristics. It eliminates the negative effects of the trap states for the most part and reveals the intrinsic nature of the material itself.

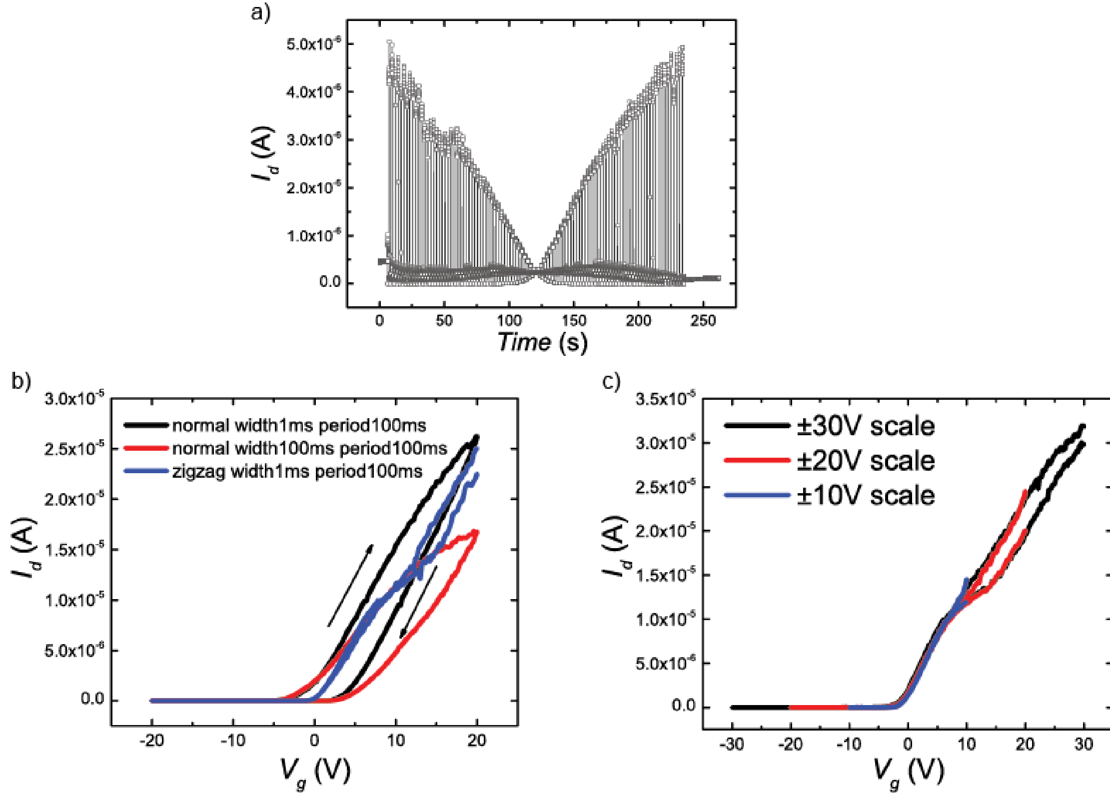



Figure 6.7. a) Complete $I_d$-*Time* curve generated by the normal pulse series with 10V amplitude and 200mV sweep interval. b) Zigzag pulsed measurement $I_d$-$V_g$ result compared with normal pulse series mode. c) Zigzag pulsed measurement with different sweep scales. Drain voltages are all 1V.

The mobility extracted from the DC sweeps is $1.74 cm^2V^{-1}s^{-1}$ for the forward sweep and $3.14 cm^2V^{-1}s^{-1}$ for the reverse sweep, based on the equation:

$$\mu_{FE} = [I_d / (V_g - V_t)] / (\frac{W}{L} c_{ox} V_d) \tag{24}$$

where $I_d$ is the drain current; $V_g$ is the gate voltage; $V_t$ is the threshold voltage; $W$ and $L$ are the channel width and length respectively; $c_{ox}$ is the gate oxide capacitance per unit area; $V_d$ is the drain bias voltage. Therefore, there is nearly a 100% difference between the results from the two branches of the hysteresis loop. By contrast, mobility extracted from the zigzag pulse mode data is almost identical for both branches ($5.91 cm^2V^{-1}s^{-1}$ for the forward sweep and $5.59 cm^2V^{-1}s^{-1}$ for the reverse sweep). Note that even in the presence of pulsed gating, some of the states can be filled/empty in the steady state (pulsed gating only removes the dynamic trapping/detrapping), which can adversely affect the mobility.

In summary, we have explored the interface states in a monolayer $MoS_2$ transistor. We have shown that the hysteresis in the DC sweeps can be exploited to quantify the nature and density of the interface trap states that are created by adsorption of various contaminant molecules. Such trap states severely affect device behavior such as ON current and mobility. By applying

carefully designed pulses to the gate, the effects of the trap states can be removed, revealing the intrinsic properties of the channel material. The techniques shown here are applicable in general to all other emerging channel materials.

# Chapter 7. Conclusion and Potential Future Work

## 7.1 Conclusion

In conclusion, we have fabricated and electrically characterized the $MoS_2$ transistors with non-volatile functionalities from multiple mechanisms.

We managed to integrate the 2D $MoS_2$ semiconductor with the single crystalline PZT crystal via transfer technique. Several methods were developed to avoid the effects induced by interface states which could screen the polarization mechanism in the 2D ferroelectric structure. Some FE transistors were fabricated on the ultra-smooth PZT film to minimize the number of traps induce by surface defects, in which correct handedness hysteresis loops were achieved. Moreover, with external ferroelectric connection, large counterclockwise hysteresis loops (~20V hysteresis window) with high ON/OFF ratio ($>10^6$) were detected. Electron doping/depletion with the density of around $7.8\times10^{12}cm^{-2}$ could be induced by the polarization of external FE capacitor, leading to the switchable metal insulator phase transitions in the system. Those non-volatile properties confirm a promising future of the combination of single crystalline perovskite materials and 2D semiconductors to be applied for the next generation FeRAM technology development.

At the same time, the interface trapping states from adsorbates in the monolayer $MoS_2$ dielectric transistor in ambient were investigated. Effects from interface states with the density of $>10^{13}/(cm^2{\cdot}eV)$ were convinced to be minimized by pulse gating with self-designed pulse sequences. The pulse gating technique provides a convenient method to analyze the intrinsic electrical characteristics of 2D devices in the ambient environment.

## 7.2 Potential Future Work

Since the promising future of 2D ferroelectric transistors in the application of emerging memory technology have been confirmed by the detected large and intact hysteresis loops, now we can consider how to simplify the model and characterize more properties. In the next step, instead of external connection, the integration of $MoS_2$ transistor and PZT capacitor could be done directly by the floating gate structure (shown in Figure 7.1), in which an $MoS_2$ back-gate floating gate (FG) transistor is fabricated on the PZT substrate. The floating gate could couple with the SRO back electrode to constitute a ferroelectric capacitor with PZT in between. And in the FG/dielectric/$MoS_2$ stack, the floating gate is designed to deliver the ferroelectric field effect to the $MoS_2$ channel based on the relationship $Q_{FE} = Q_{DE}$. That overall structure is similar to the

system with external connection in chapter 5.2, but here the cable is replaced by an electrode, so the whole system's size could be minimized and the parameters related to the memory performance, like retention and endurance, could be extracted easily.

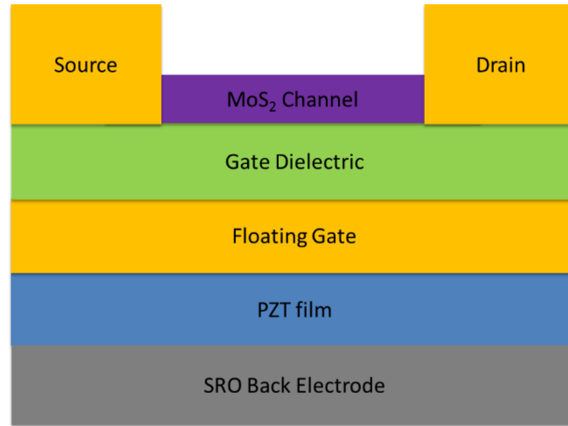



Figure 7.1. The cross section of designed $MoS_2$ ferroelectric floating gate transistor.

Moreover, even though we have already got metal-insulator transition in the previous work, the electron density for getting superconductivity of $MoS_2$ ($\geq 7\times10^{13}cm^{-2}$) is still hard to reach by the external connection technique, likely because of the dissipation of charge in the cable and tips used there. Integrating the two parts ($MoS_2$ transistor and PZT capacitor) directly on the same chip is expected to help improve the coupling efficiency in between and let us get switchable superconductor-insulator transition (SIT) phenomenon in the future.

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