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Spread Spectrum Based Digital-Intensive CMOS Radar System

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Spread Spectrum Based Digital-Intensive CMOS Radar System

A dissertation submitted in partial satisfaction of the

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in Electrical and Computer Engineering

by

Rulin Huang

2022

ABSTRACT OF THE DISSERTATION

Spread Spectrum Based Digital-Intensive CMOS Radar System

by

Rulin Huang

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2022

Professor Mau-Chung Frank Chang, Chair

CMOS radar is a promising technique enabling applications like ground penetrating, weather observing, and even autonomous driving with its high integration level and cost effectiveness in mass production. Under an analog type waveform, performance of conventional linear frequency-modulated continuous-wave (FMCW) radar is heavily degraded by AM (envelop fluctuation) and FM (chirp non-linearity) distortions. In this dissertation, digital-intensive CMOS radar with digital modulated and coded waveform is proposed instead of using an analog chirp. Additionally, spread spectrum technique is adopted to expand radar signal across a wide bandwidth and therefore achieve good radar range resolution. Two digital-intensive radar systems and the fabricated CMOS implementations will be shown to demonstrate the proposed approaches.

First, an 89-93 GHz frequency hopping spread spectrum (FHSS) based FHCW radar with 4-GHz bandwidth / 3.75-cm range resolution is developed and implemented for automotive application to tolerate multi-user interference. To effectively mitigate the radar interference under an multi-user scenario, frequency hopping technique with one-coincidence codes is used to achieve multiplexing in the code domain. The unique orthogonal property of these one-coincidence codes prevent different users from occupying the same frequency channel at the same time. A cost-effective TX/RX module with the 28-nm CMOS chip and a Rogers patch antenna is developed for over-the-air verification, whose results demonstrate the multi-user capability of this FHCW radar.

Second, a 0.1-4.0 GHz direct sequence spread spectrum (DS/SS) based all-digital radar SoC is proposed and fabricated in 28-nm CMOS for ground-penetrating application. A time-domain digital correlation-based time-of-flight measurement is employed for radar ranging instead of a chirp or pulse. The SoC offers complete programmability over frequency and bandwidth due to the nature of inductor-less design, which allows the ground-penetrating radar (GPR) to be adopted to various sub-surface conditions. In-field GPR test with actual rover prototype validates the capability of the DS/SS radar. The 28-nm prototype radar SoC achieves a fine resolution of 3.75 cm and consumes 46.2 mW, which makes it suitable for low power applications.

The dissertation of Rulin Huang is approved.

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Yuanxun Wang

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2022

DEDICATION

To my dear parents

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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SELECTED PUBLICATIONS

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CHAPTER 1

Introduction

1.1. Fundamentals of Radar System

Radar (radio detection and ranging) is a detection system that transmits and receives electromagnetic waves to resolve the range, velocity and angle information of targets. Since invented during World War II, radars have been widely used in many different applications in our daily life, such as automotive driving [1-6], weather detection [7], [8] and ground-penetration [9], [10]. Among different radar implementations, CMOS radar is a promising technique due to its high integration level, robustness, and cost effectiveness in mass production [11-13].

As shown in Fig. 1.1, radars acquire the ranging information of targets through resolving the time-of-flight (*ToF*) of propagating waves between different targets placed within a scene. Assuming there are two different targets in front of the radar. Target1 is distance d away from the radar while target2 is distance Δd further away from target1. By the definition of wave propagation, the distance of target 1 from the radar can be calculated by the following equation

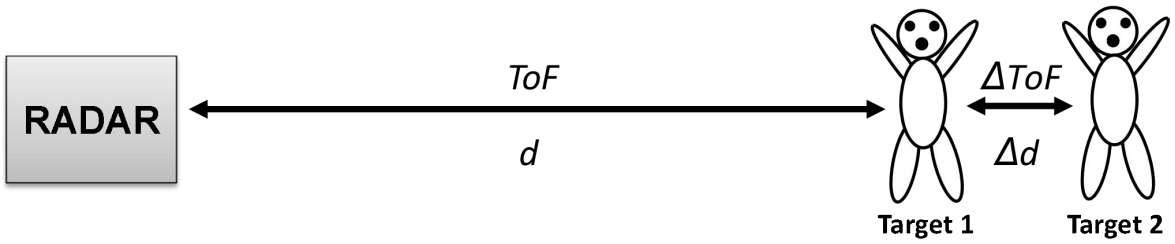


Fig 1.1 Diagram showing how radars acquire ranging information

$$d = ToF \times c/2 \quad (1\text{-}1)$$

where c is the speed of light. Moreover, in order to resolve target1 and target2 that are spaced Δd ($\Delta d = \Delta ToF \times c/2$) away from each other, the adopted radar will need a Nyquist bandwidth of

$$B_N = 1/\Delta ToF \quad (1\text{-}2)$$

This equation applies regardless of the radar waveform type (pulse, chirp, spread waveform). Assuming the bandwidth of the adopted radar signal is BW, we know $BW \geq B_N$. Therefore, from (1-1) and (1-2), the fundamental radar range resolution equation can be derived as

$$\Delta d \geq c/2BW \quad (1\text{-}3)$$

Equation (1-3) shows that the achievable radar range resolution is only determined by the overall radar signal bandwidth. A larger bandwidth will promise a smaller range resolution [14].

1.2. Motivation

With a constant envelop and low-complexity implementation, linear frequency-modulated continuous-wave (FMCW) radar is used in the majority of automotive radars [15], [16]. Time domain and frequency domain waveforms of an FMCW radar are shown in Fig. 1.2(a) and (b), respectively. As illustrated in Fig. 1.2(b), a chirp (red curve) with an average slope of SL is transmitted and the received time-shifted echo signal (green curve) is demodulated against the same chirp to produce a beat frequency f_{beat}, which is proportional to the time-of-flight (ToF) of the target, formulating the FMCW ranging principle

$$f_{beat} = SL \times ToF = SL \times 2d/c \quad (1\text{-}4)$$

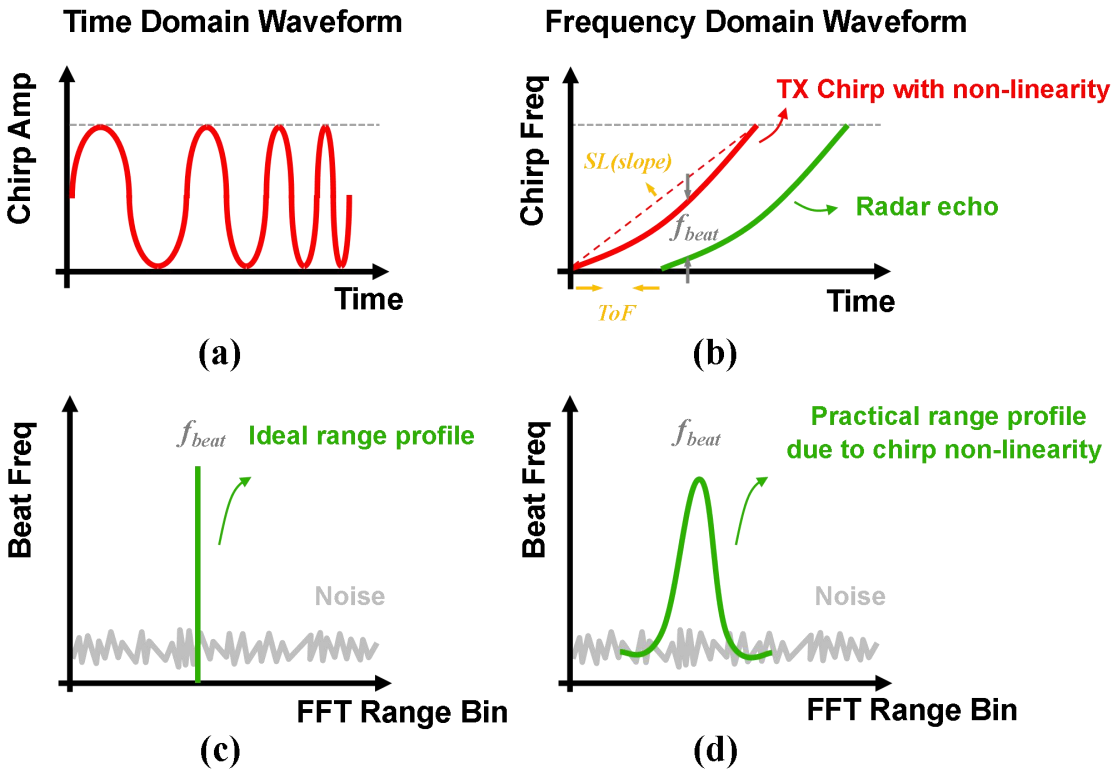


Fig 1.2 (a). FMCW radar time domain waveform. (b). FMCW radar frequency domain waveform with chirp non-linearity. (c). Ideal FMCW radar range profile after FFT. (d). Practical FMCW radar range profile after FFT due to chirp non-linearity

However, there are two practical impairments that limit the performance of FMCW radar. Under an analog type waveform, AM (envelop fluctuation) and FM (chirp non-linearity) distortions will introduce significant performance degradation in an FMCW radar. With these non-ideal effects, the beat frequency f_{beat} will spread out over the entire spectrum, which is called tone splitting after baseband FFT [17].

In order to obtain a good range resolution, FMCW radars need to chirp across a large bandwidth. Therefore, the envelop fluctuation could be induced by the non-constant amplitude

frequency response of practical RF and millimeter-wave (mm-Wave) circuits. In addition to the AM distortion, there is also FM distortion induced by chirp non-linearity, which is even more severe in an FMCW radar. From [18], chirp non-linearity is the key limiting factor in FMCW radar systems.

Phase-locked loop (PLL) with a wide tuning range voltage-controlled oscillator (VCO) usually serves as the chirp generator in an FMCW radar. As shown in Fig. 1.2(b), due to the nonlinear nature of VCO tuning characteristic and the PLL loop dynamic change induced from K_{VCO} variation, the generated FMCW chirp inevitably suffers from non-linearity. Fig. 1.2(c) and (d) compare the FMCW radar range profile, which is the intermediate frequency (IF) spectrum after baseband FFT without and with chirp non-linearity, respectively. Rather than a fixed beat frequency, under an non-linear chirp, the beat frequency becomes an frequency modulated signal and its energy will spread out. As a result, radar sensitivity is degraded and inaccurate detection may occur [2].

To relieve chirp non-linearity effect, segmentation technique is used for VCO varactor design in [2]. Varactors with three segmented bias is adopted to reduce the variation of the effective K_{VCO} across VCO control voltage and therefore extend the linear region of the generated chirp. The design achieves a chirp from 77 to 81 GHz with a rate of 340 MHz/us and the corresponding peak chirp non-linearity is +/- 0.2%. This technique works well for slow chirp, but for fast chirp generation, it can not satisfy the stringent requirement of ultra-short-range radar (USRR), which requires +/- 0.05% chirp non-linearity. In [18], a digital PLL with two point modulation (TPM)

and digital pre-distortion (DPD) is presented for fast and linear chirp generation. 208 MHz-BW chirp centered at 23 GHz is achieved with a maximum rate of 173.3MHz/us and +/- 0.06% RMS chirp non-linearity. This work could barely satisfy the chirp linearity requirement of USRR, but the overall chirp bandwidth is limited and the required DPD background calibration consumes a lot of power. Therefore, developing new types of CMOS radars that are able to tolerate chirp non-linearity remains an active research topic.

From the history of communication system, we know that digital communication offers lots of benefits over traditional analog communication. Actually, it is very similar in a radar system. In comparison of analog type waveform, digital modulated waveform is more robust to circuit impairments and non-ideal effects. Moreover, a digital-intensive CMOS radar is more scaling-friendly with advanced CMOS technologies.

Fig. 1.3 shows the concept of new CMOS radars that adopt digital modulated/coded waveform instead of analog frequency chirp to overcome the AM (envelop fluctuation) and FM (chirp non-linearity) impairments. However, one follow-up question is how to preserve the required range resolution of the radar. Based on the fundamental radar resolution equation (1-3), in order to maintain range resolution, the radar signal bandwidth BW has to be the same as previous. Therefore, spread spectrum technique can be used in radar digital signal coding to expand radar signal over a certain bandwidth and maintain the required radar range resolution. Furthermore, spread spectrum technique also offers some interesting characteristics to the radar system, such as diversity.

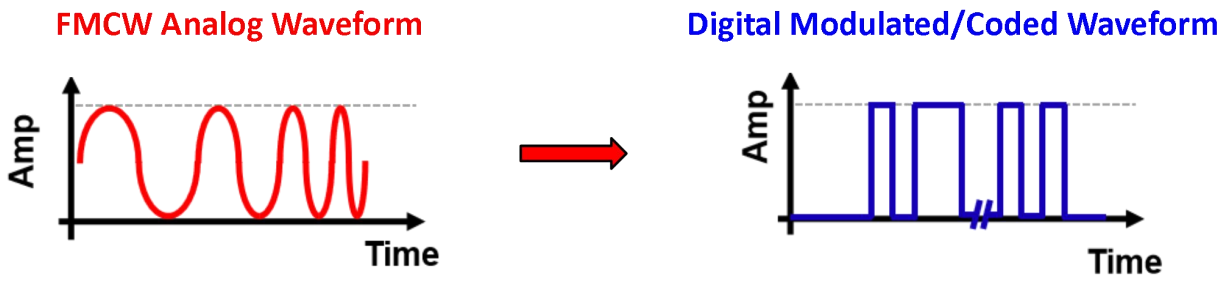


Fig 1.3 Concept of radars adopting digital modulated/coded waveform instead of conventional analog FMCW chirp

In this dissertation, I report two new digital-intensive CMOS radar systems based on spread spectrum technique. First, I introduce an 89-93 GHz frequency hopping spread spectrum (FHSS) based multi-user interference-tolerant radar for automotive application in 28-nm CMOS process. In order to effectively mitigate radar interference in an multi-user scenario, one-coincidence codes spreading out of a 4-GHz bandwidth are developed. The unique orthogonal property of these one-coincidence codes prevent different users from occupying the same frequency channel at the same time. Thereafter, I propose a 0.1-4 GHz direct sequence spread spectrum (DS/SS) based all-digital radar SoC for ground-penetrating application in 28-nm CMOS process. With software defined carrier frequency and bandwidth, the DS/SS based inductor-free radar SoC can be adapted to any encountered sub-surface conditions, so as to overcome the penetration and resolution trade-off. Moreover, the DS/SS approach does not require a baseband FFT processing as the ranging information is naturally produced in time-domain, allowing for much lower power.

1.3. Dissertation Organization

The rest of the dissertation is organized as follows. Chapter 2 introduces a new concept of frequency hopping one-coincidence codes and presents an 89-94 GHz FHSS based multi-user radar for automotive application. Code domain multiplexing is obtained from the orthogonality of the one-coincidence codes and offers interference-tolerant capability to the radar system. Radar architecture, interference analysis under multi-user scenario, CMOS building blocks design and measurement results are also described in this chapter. Chapter 3 demonstrates a 0.1-4 GHz DS/SS based all-digital radar SoC for ground-penetrating application. Without using a single inductor, the proposed radar offers complete programmability over frequency and bandwidth. SoC architecture, radar ranging principle, dynamic range analysis, key building blocks design and a practical in field radar test are presented in this section. Finally, chapter 4 concludes the dissertation.

CHAPTER 2

An 89-93 GHz Frequency Hopping Spread Spectrum (FHSS) Multi-User Interference-Tolerant Radar for Automotive Application in 28-nm CMOS

This chapter will present an 89-93 GHz interference-tolerant frequency hopping continuous-wave (FHCW) radar capable of supporting simultaneous operations of multiple users over a 4-GHz bandwidth [19]. To effectively mitigate radar interference resulted from concurrent transmissions of multiple users, frequency hopping with corresponding one-coincidence codes is employed on each user. The unique orthogonal property of the one-coincidence codes prevent different users from occupying the same frequency channel at the same time, thus achieving multiplexing in code domain.

2.1. State-of-the-art CMOS Automotive Radar Systems

In the early 1970s, millimeter-wave (mm-Wave) radar system has been used for automotive application [11]. Since then, several generations of automotive radar system have been developed by different research institutes and automotive companies. Compared with its counterpart LiDAR and camera, mm-Wave radar provides superior robustness against bad weather conditions, such as rain, fog and snow [20]. Meanwhile, as an integration-friendly technology, CMOS process gradually dominates the market of low cost mm-Wave automotive radar over SiGe and other III-V technologies [21-23]. Regarding to the operation frequency,

Short range radar (SRR) locals near 24 GHz while long range radar (LRR) locals near 77 GHz [24], [25]. The antenna size and form factor of a 77 GHz radar are much more smaller than those of a 24 GHz radar.

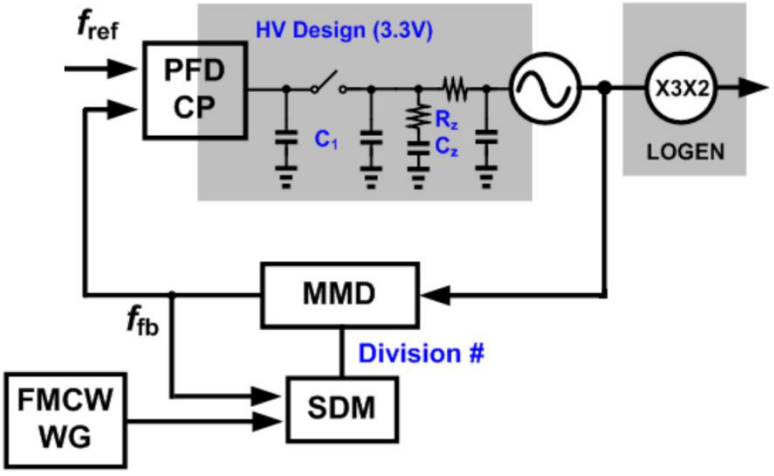


Fig 2.1 Block diagram of the FMCW radar transmitter in [2]

In order to achieve better range resolution, recent published state-of-the-art CMOS automotive radar extends the overall bandwidth up to 4 GHz from 77 GHz to 81 GHz. In [2], MediaTek reported a 77-81 GHz FMCW automotive radar in 65-nm CMOS process, targeting at ultra-short range sensing and 360-degree surround view for parking assistance. The block diagram of the radar transmitter is shown in Fig 2.1. Direct frequency modulation architecture is used for chirp generation with a 13 GHz fractional-N PLL and an ×6 frequency multiplier. Since there is no mixing operation, the transmitter linearity performance is superior. However, under a 4-GHz BW, chirp non-linearity does degrade the radar overall performance. Even with varactor segment-biasing technique to reduce the variation of the effective K_{VCO} and therefore extend the linear region of the generated chirp, the radar still can not satisfy the stringent requirement of

ultra-short-range radar, which requires +/- 0.05% chirp non-linearity. For fast chirp generation with a rate of 340 MHz/us, the FMCW radar's reported peak chirp non-linearity of is +/- 0.2%. Furthermore, a large PLL chirping bandwidth degrades the overall phase noise performance.

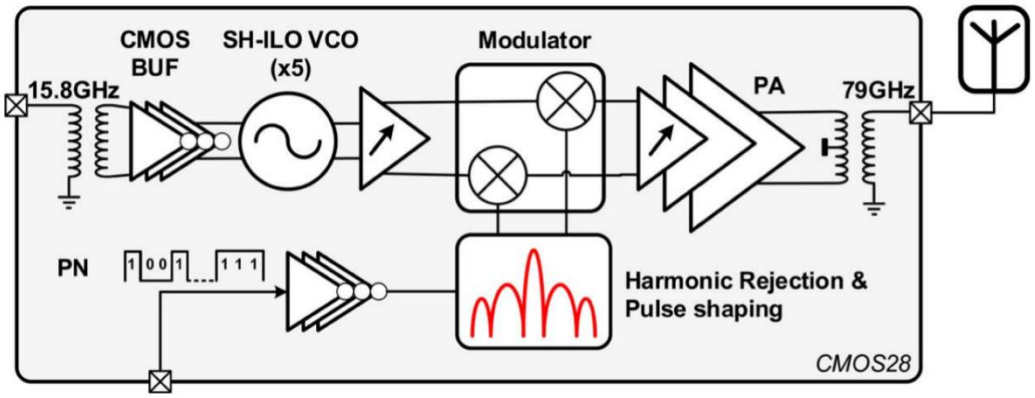


Fig 2.2 Block diagram of the PMCW radar transmitter in [3]

To overcome the FMCW radar chirp non-linearity issue and obtain better range resolution profile, CMOS phase-modulated continuous wave (PMCW) radar is first introduced in [3] for pedestrian detection. Fig 2.2 shows the block diagram of the PMCW automotive radar. Direct conversion architecture is used here, where a pseudo-noise (PN) sequence directly modulates the differential output of a 79 GHz sub-harmonically injection locked oscillator (SH-ILO). Binary phase-shift keying (BPSK) is used for modulation and the ×5 SH-ILO VCO is injection locked to a 15.8 GHz external local oscillator (LO). The PMCW radar offers quite a lot advantages over conventional FMCW radar. First, there is no chirp non-linearity consideration anymore. Second, superior phase noise performance can be achieve for a fixed LO frequency. Third, the PN sequence offers diversity to the radar system, which is used for multiple-input-multiple-output (MIMO) radar operation to resolve angular information of the target in [3].

However, there are two factor that may limit the practical operation of a PMCW radar. Regarding to the implementation, the locking range of ×5 SH-ILO is very limited since it relies on the fifth-order harmonic of the 15.8 GHz LO. PVT variation could cause trouble to the normal operation of the ×5 SH-ILO as well. Moreover, from the system point of view, the instantaneous phase jumps from BPSK modulation introduce discontinuities in the time-domain waveform, which results in spectrum regrowth and poor sidelobe rejection. Additional harmonic rejection and pulse shaping circuits have to been implemented to suppress the sidelobe in [3].

2.2. New FHCW Radar with Interference-Tolerance Capability for Multi-User Application

2.2.1. FHCW Radar System

A new frequency hopping continuous-wave (FHCW) radar system is introduced in [19], which is able to support simultaneous operation of multiple users with its interference-tolerance capability.

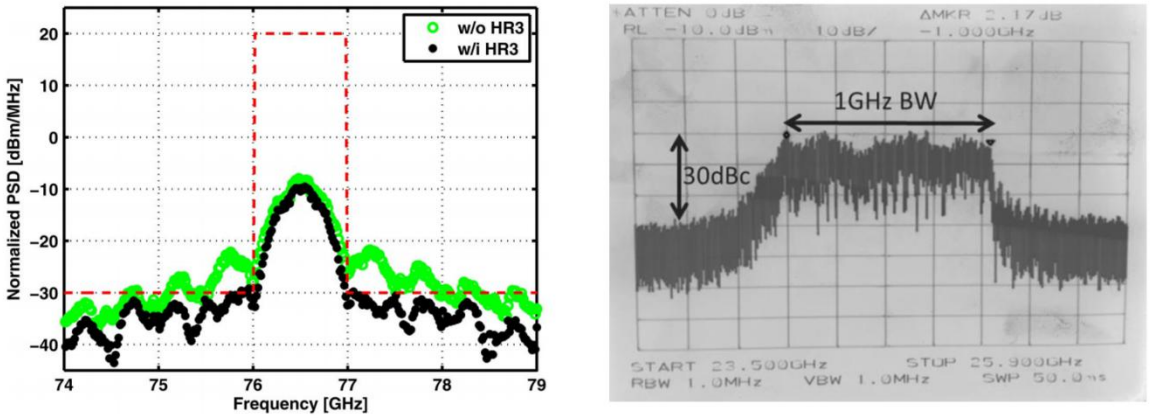


Fig 2.3 (a). 1GHz-BW PMCW radar spectrum. (b). 1GHz-BW FHCW radar spectrum

Other than BPSK modulation used in a PMCW radar, frequency hopping spread spectrum (FHSS) is adopted in an FHCW radar to suppress the spectrum sidelobes. Fig 2.3 shows the spectrum comparison between PMCW and FHCW radar. For a PMCW radar under 1GHz-BW, the sidelobe rejection is 13dBc without cancellation technique, and it goes up to 20dBc by utilizing harmonic rejection circuit [3]. For an FHCW radar under 1GHz-BW, the sideband rejection is naturally 30dBc at 500MHz offset. It is obvious that FHCW radar has better sideband rejection performance in comparison with PMCW radar. Because phase discontinuity only occurs when the instantaneous frequency hops from one to another under FHSS, while it could occur for each symbol under BPSK modulation.

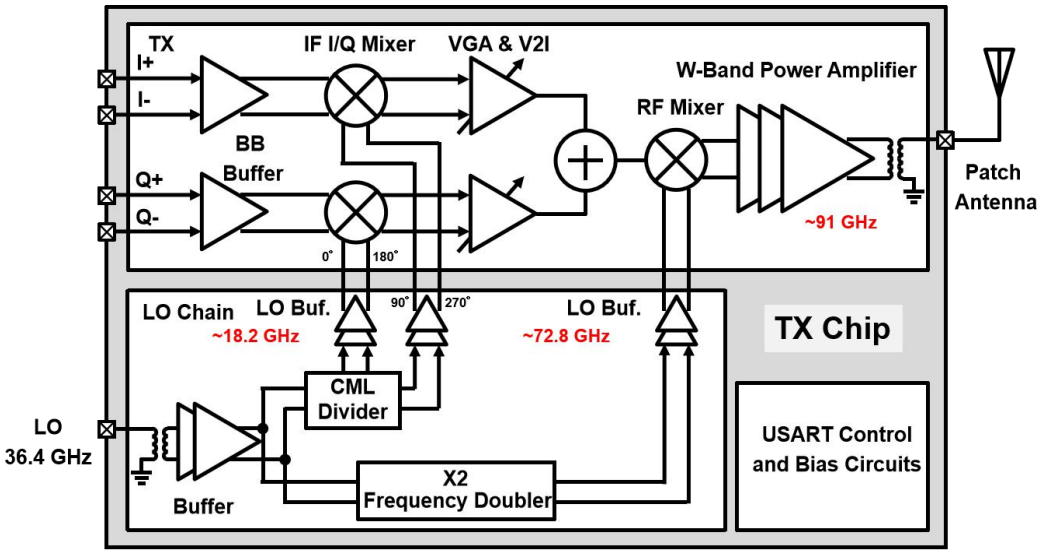


Fig 2.4 Block diagram of the proposed FHCW radar transmitter

Block diagram of the proposed 89-93 GHz FHCW radar transmitter is shown in Fig 2.4. Two-step conversion architecture is adopted with an external 36.4 GHz LO and an on-chip LO

chain, which consists of an I/Q divider and a frequency doubler. This specific LO plan gets rid of the PVT-sensitive ×5 SH-ILO used in [3], promises a robust transceiver design. With a fixed LO frequency, phase noise performance can be further optimized.

Similar to a PMCW radar, with a digital coded waveform, there is no more chirp non-linearity issue in an FHCW radar. Meanwhile, because FHSS is used in baseband signaling for radar ranging, different frequency hopping orders naturally provide diversity to the FHCW radar system. This diversity property can be used to obtain interference-tolerance capability for multi-user automotive application, which is presented in the following sections.

2.2.2. Radar Interference Analysis under Multi-User Scenario

In practical autonomous driving applications that normally involve multiple vehicles, transmissions from adjacent vehicle radars inevitably cause interference, which may adversely affect the radar functionality and accuracy [26], [27]. In an FMCW radar, the chirp is not robust against interference in a multi-user scenario [2]. Take the two-car scenario depicted in Fig. 2.5 as an example, chirp B (from FMCW radar of car B) actually becomes an interference to chirp A (from FMCW radar of car A). If the rates (frequency ramp slopes) of chirp B and chirp A are the same, a ghost target will appear at the radar IF spectrum of car A. If these two chirp rates are different but have the same sign (positive or negative), the interference from chirp B will spread out as a strong narrowband signal. If these two chirp rates have opposite signs (one positive and one negative), the interference from chirp B will spread out as in-band noise. In all aforementioned cases (shown in Fig. 2.5(b), (c) and (d)), the interference may significantly

degrade the performance of an FMCW radar. Although bandpass filtering can be applied to mitigate FMCW radar interference, it only deals with the out-of-band interference; the ghost target or receiver sensitivity degradation caused by the in-band interference still remain [2].

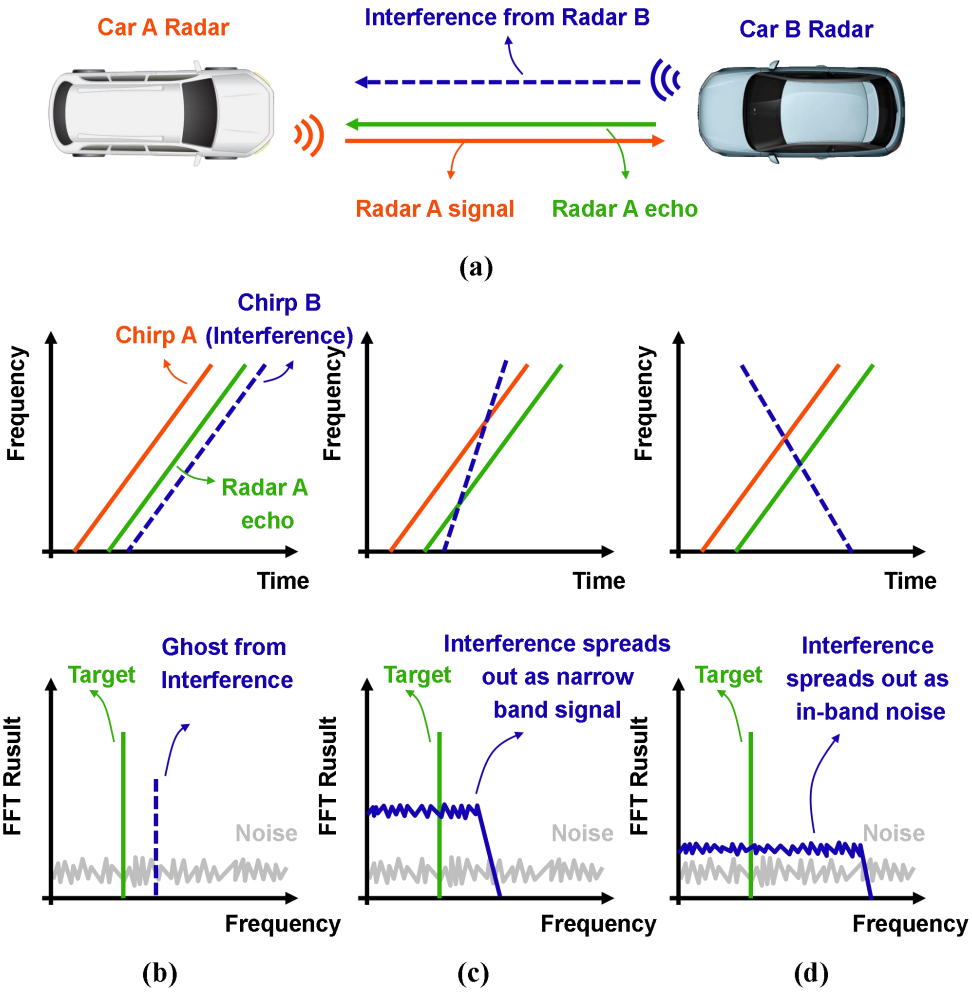


Fig 2.5 (a). FMCW radar interference issues under a two car scenario. When (b). chirp A and chirp B have the same rate; (c). two chirp rates are different but with the same polarity; (d). two chirp rates are different and with opposite polarity

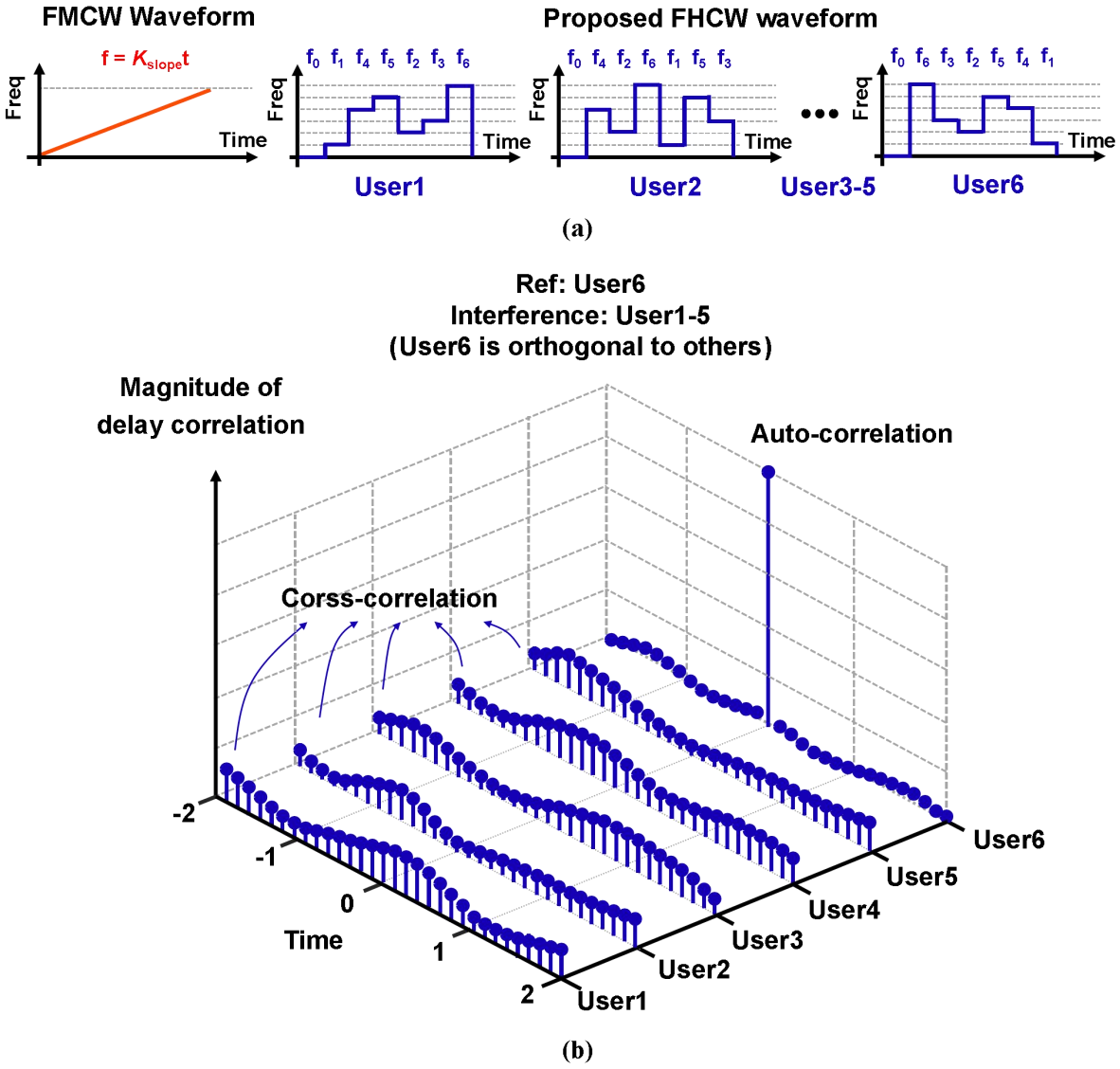


Fig 2.6 (a). Comparison of the FHCW radar and FMCW radar waveform. (b). Delay correlation and interference tolerance property of the adopted one-coincidence codes for the FHCW radar

In order to effectively mitigate radar in-band and out-of-band interference in a multi-user scenario and overcome range accuracy challenge due to chirp non-linearity while providing fine

resolution, this work adopts the extended hyperbolic congruential (EHC) one-coincidence codes [27] and extends the radar bandwidth to 4 GHz to construct a W-band 89-93 GHz FHCW radar. The unique orthogonal property of these one-coincidence codes prevent different users from occupying the same frequency channel at the same time, thus supporting multiple users simultaneously. Moreover, wideband operation induced from frequency hopping enables a radar range resolution of 3.75 cm, which is equal to $c/2BW$ where c is the light speed and BW is the radar bandwidth.

As shown in Fig. 2.6, rather than a linear frequency chirp used in FMCW radar, the waveform of an FHCW radar is a sequence of frequencies that hop with time. Frequency hopping spread spectrum technique is used here to provide multi-user multiplexing. Therefore, multiple radar users can be involved. For every user, a specific frequency hopping order is applied. When different users occupy the same frequency channel at the same time, the coincidence or a hit happens, causing interference to each other. One-coincidence code set has the property that the maximum number of hits between any different users is one [28], which minimizes the mutual interference among various users.

2.2.3. Code-domain Orthogonality with One-Coincidence Frequency Hopping Codes

The adopted one-coincidence frequency hopping code set for multi-user application is explained as follows: a total bandwidth BW is occupied by N frequency steps with a sub-channel bandwidth of BW/N. All the frequencies are non-repeating and the entire signal length is T

seconds. At the k-th time slot, the instantaneous frequency f_k is frequency modulated with respect to the carrier frequency f_0 by

$$f_k = f_o + y_i(k) \times (BW/N) \tag{2-1}$$

$$y_i(k) \in \{0, 1, \cdots, N-1\} \tag{2-2}$$

In the equation, i is the user identification number and $y_i(k)$ is the placement operator, which is a sequence of integers. Each user owns a unique $y_i(k)$. In order to provide a consistent interference tolerance performance, a well-defined code $y_i(k)$ is created for each user by optimizing cross-correlation [29]. For two user X and Y, the cross-correlation can be defined as

$$H_{XY}(\tau) = \sum_{i=0}^{N-1} h\,(X_i\,, Y_{i+\tau})\,, \quad 0 \le \tau \le N-1$$

$$where \quad h(X_i\,, Y_{i+\tau}) = \begin{cases} 0\,, & X_i \neq Y_{i+\tau} \\ 1\,, & X_i = Y_{i+\tau} \end{cases} \tag{2-3}$$

Note when (2-3) applies to the same radar user X, $H_{XX}()$ becomes auto-correlation function for itself. The one-coincidence code set [27] with optimum orthogonality and cross-correlation is adopted for this FHCW radar. For this code set, the maximum non-trivial correlation is then given by

$$H_{cross\_max} = max\{H_{XY}(\tau), \tau = 0, 1, \cdots, N-1\} = 1 \tag{2-4}$$

$$H_{auto\_max} = max\{H_{XX}(\tau), \tau = 1, 2, \cdots, N-1\} = 0 \tag{2-5}$$

which means only one coincidence or frequency hit happens between different users so as to minimize their mutual interference, while a thumbtack like auto-correlation function can be

maintain to avoid range-Doppler ambiguity [30]. The adopted one-coincidence code set can be obtained using congruential equation. For a total number of p-1 users, where p is a prime number > 2, the placement operator $y_i(k)$ is then defined as.

$$y_i(k) \equiv \begin{cases} (i \times k)^{-1} mod(p), & k = 1, 2, \cdots, p-1 \\ 0, & k = 0 \end{cases} \quad (2\text{-}6)$$

By choosing the total frequency steps $N = p$, N-1 orthogonal one-coincidence codes can be obtained to accommodate N-1 users concurrently. For example, if $N = 7$, the radar waveform and interference tolerance property are shown in Fig. 2.6 (a) and (b), respectively. Each code $y_i(k)$ has 7 different frequency steps occupying 7 continuous time slots. Following are those 6 one-coincidence codes $y_i(k)$ for the 6 users, respectively.

$$\begin{aligned} &User(i=1):\{0,1,4,5,2,3,6\};\ User(i=2):\{0,4,2,6,1,5,3\}; \\ &User(i=3):\{0,5,6,4,3,1,2\};\ User(i=4):\{0,2,1,3,4,6,5\}; \\ &User(i=5):\{0,3,5,1,6,2,4\};\ User(i=6):\{0,6,3,2,5,4,1\}; \end{aligned} \quad (2\text{-}7)$$

2.2.4. System Analysis and Link Budget

To mitigate radar interference from different users while maintaining a good radar range resolution, an one-coincidence frequency hopping code set with a chip rate R_C of 4 Gsps and sequence length L_C is developed for the FHCW radar centered at 91 GHz. The finest achievable radar range resolution R_{res} is 3.75 cm, given by.

$$R_{res} = c/2R_c \quad (2\text{-}8)$$

where c is the speed of light. The sequence length is chosen to have a maximum unambiguous range R_{max} more than 30 m. With a sequence length L_C of 800, R_{max} is 30.45 m according to

$$R_{max} = cL_c/2R_c = R_{res}L_c \tag{2-9}$$

To fully utilize the 4 GHz radar bandwidth, 29 frequency steps with a sub-channel bandwidth of 138 MHz is allocated for the frequency hopping operation, which can accommodate 28 different users. System parameter for the W-band FHCW radar is summarized in Table 2.1.

Parameter	**Symbol**	**Value**	**Unit**
Carrier frequency	F_C	91	GHz
Chip rate	R_C	4	Gsps
Range resolution	R_{res}	3.75	cm
Max. Unambiguous range	R_{max}	30.45	m
Number of users	N_{user}	28	
Total frequency steps	p	29	
Sequence length	L_C	800	chips
RX baseband total integration time	T_{int}	10	ms

Table 2.1 System parameter for the W-band FHCW radar

A link budget is then calculated based on the well-known radar equation [31]

$$P_R = G_R G_T P_T \sigma \lambda_c^2 / (4\pi)^3 R^4 \tag{2-10}$$

where P_T and P_R are the transmitted power and received power, respectively, G_T and G_R are the antenna gain of the radar transmitter and receiver, respectively, σ is the radar cross section (RCS) of the target, λ_c is the wavelength at radar operation frequency and R is the target distance. From the results in [11], the RCS of an ordinary car is assume to be 0 dBsm in this paper. At 91 GHz, based on our research [32], [33], 3 dBi transmit and receiver antenna gain with the feeding loss considered can be achieved using low loss substrate material such as Rogers 4003C. Maximum unambiguous range R_{max} is used for path loss calculation. Based on these parameters, with 10 dBm transmitted power, the received power P_R = -126 dBm given by (2-10), which is very low. However, because the radar signal is correlated to itself while noise is totally uncorrelated by its nature, digital processing gain resulted from correlation and integration at the receiver baseband can help improve the overall SNR [3]. With a total integration time T_{int} = 10 ms. The digital processing gain is G_{int} is 76 dB, according to

$$G_{int} = 10\log_{10}(T_{int}/T_C) \tag{2-11}$$

When arriving at the receiver input, the received signal power needs to be higher than the receiver sensitivity, of which is defined in the following equation in decibel meters [34]

$$P_{sen} = -174\ dBm/Hz + NF + 10\log_{10} B + SNR - G_{int} \tag{2-12}$$

where -174 dBm/Hz is thermal noise floor at room temperature, NF is the receiver noise figure in decibels, B is the radar bandwidth in hertz. With an estimate receiver NF of 10 dB, the calculated noise power refer to the receiver input P_N = -68 dBm. Consider the 76 dB baseband processing

gain, the overall $SNR = P_R - P_N + G_{int}$ = 18 dB, which fulfill the 16 dB *SNR* requirements for 99% detection probability and 10^{-10} false alarm ratio [31]. Table 2.2 summarizes the link budget analysis for the W-band FHCW radar.

Parameter	**Symbol**	**Value**	**Unit**
Transmitted power	P_T	10	dBm
Antenna gain	G_T, G_T	3	dBi
Target RCS	σ	0	dBsm
Path loss	$\lambda_c^2/[(4\pi)^3 R^4]$	-142	dB
Received power	P_R	-126	dBm
Receiver noise figure	*NF*	10	dB
Radar bandwidth	*B*	4	GHz
Noise power refer to RX input	P_N	-68	dBm
RX baseband processing gain	G_{int}	76	dB
Signal-to-noise ratio	SNR	18	dB

Table 2.2 Link budget analysis of the W-band FHCW radar

Doppler effect induced by the moving target can also be detected under the frequency-hopping scheme. Delay correlation is performed to acquire the range profile of the target at the radar receiver, which is a linear function in terms of signal processing. Therefore, all the information related to Doppler-induced frequency shift will still remain after the delay correlator. If an FFT engine is placed after the delay correlator, the Doppler profile of the moving target can be detected from the spectrum after FFT. Furthermore, to minimize the phase

coherence disturbance and therefore the velocity detection disturbance in a Doppler detection, two approaches are used during the implementation: First, minimize the phase discontinuous of the one-coincidence frequency hopping code waveform (with smooth transitions during frequency hopping) when the waveform is generated. Second, the same LO is provided to the radar transmitter and receiver to keep the phases of the up-converted and down-converted radar signals coherent.

For a typical radar system, where transmitter (TX) and receiver (RX) operate at the same time, the TX-to-RX leakage is a severe practical problem [4], [35]. Leakage can occur through coupling either on-chip or on printed circuit board (PCB). Limited isolation between TX and RX antenna will also introduce leakage. The TX-to-RX leakage can be modeled as a large target at very short distance. With the effect of TX LO phase noise, radar RX sensitivity will be heavily degraded. For demonstration purpose, we design the radar TX and RX on separate dies and assemble them on dedicated PCBs.

2.3. W-Band FHCW Radar Architecture and Circuit Design

2.3.1. FHCW Radar Top Level Architecture

Block diagram of the W-band FHCW radar is shown in Fig. 2.7. The conventional direct frequency modulation architecture is not used here because in general the phase locked loop settling time significantly limits the frequency hopping rate. Therefore, a fast settling frequency synthesizer with highly linear slope is no longer required. Superheterodyne (two step conversion)

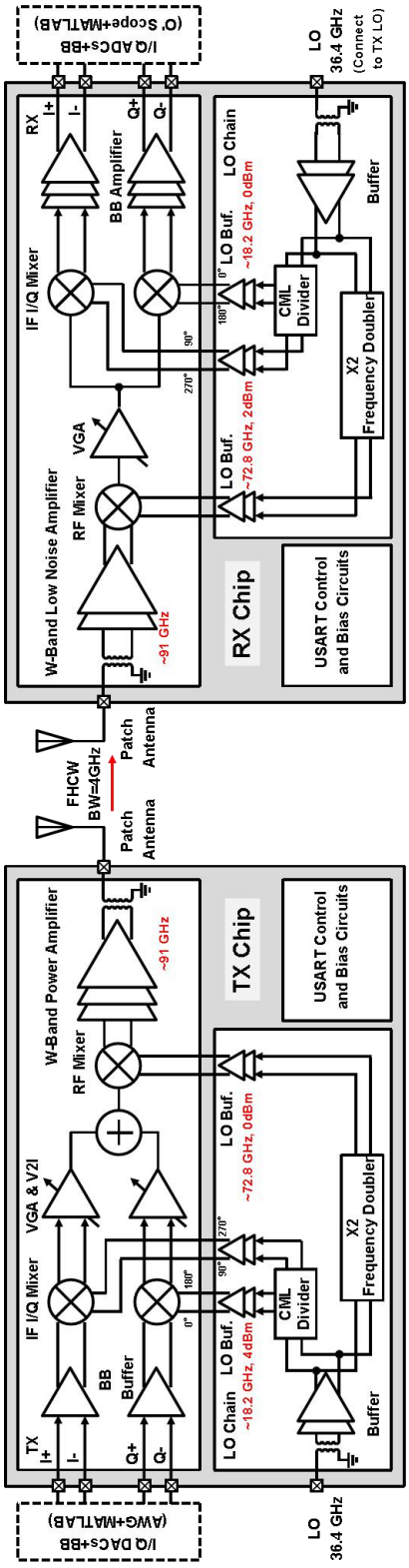


Fig 2.7 Block diagram of the W-band FHCW radar

architecture with two step conversion is adopted for the transmitter (TX) and receiver (RX) to achieve better performance in terms of I/Q imbalance and in-band LO leakage, which is essential for the frequency hopping operation. On the TX side, an I/Q mixer up-converts the baseband I/Q signal to an IF centered at 18.2 GHz. A second RF mixer up-converts the IF signal to W-band through a 72.8 GHz LO, while a power amplifier (PA) further amplifies the RF radar signal. A series patch antenna is designed on Rogers substrate to serve as TX and RX antenna. On the RX side, a low-noise amplifier (LNA) amplifies the received radar signal prior to the two-step down-conversion, from W-band to IF centered at 18.2 GHz and from IF to I/Q baseband, respectively. Delay correlation is performed at baseband (BB) to get the target range profile. A common 36.4 GHz LO is fed to the TX and RX chip externally, while a current-mode logic (CML) based divider further provides 18.2 GHz quadrature LO signal for the IF mixer and a frequency doubler further provides 72.8 GHz LO signal for the RF mixer. USART (universal synchronous/asynchronous receiver/transmitter) serves as the on-chip digital control interface.

2.3.2. LO Chain Design

The radar TX and RX share the same LO chain design. As shown in Fig. 2.8(a), an LO buffer is designed to amplify the external 36.4 GHz LO signal and provide enough input swing for the CML divider and frequency doubler. A transformer based input balun is employed to realize single-ended to differential conversion. Ultra-thick metal M7 is used for transformer primary coil while thick metal M6 is used for secondary coil to reduce insertion loss. In order to make the differential signal on the transformer secondary side more symmetrical, the overlap between the

primary and secondary coils is reduced to minimize the parasitic capacitance induced from overlapping, which causes odd-mode coupling [36]. An 8-bit R-2R based digital-to-analog converter (DAC) controlled by USART provides the bias voltage for the input common-source pair M0A/M0B. On each sides of the loading transformer, a 3-bit thermometer coded switched-capacitor bank is added to fine tuning the resonator frequency of the tank, therefore providing gain control for the LO buffer. The schematic of the switched-capacitor unit is shown in Fig. 2.8(b), the switch consists of 3 transistors in π-configuration (MS1, MS2 and MS3) and they are designed to balance R_{ON} and C_{OFF}. 8 fF Metal-Oxide-Metal (MOM) capacitor from M3 to M5 is used for CS1/CS2.

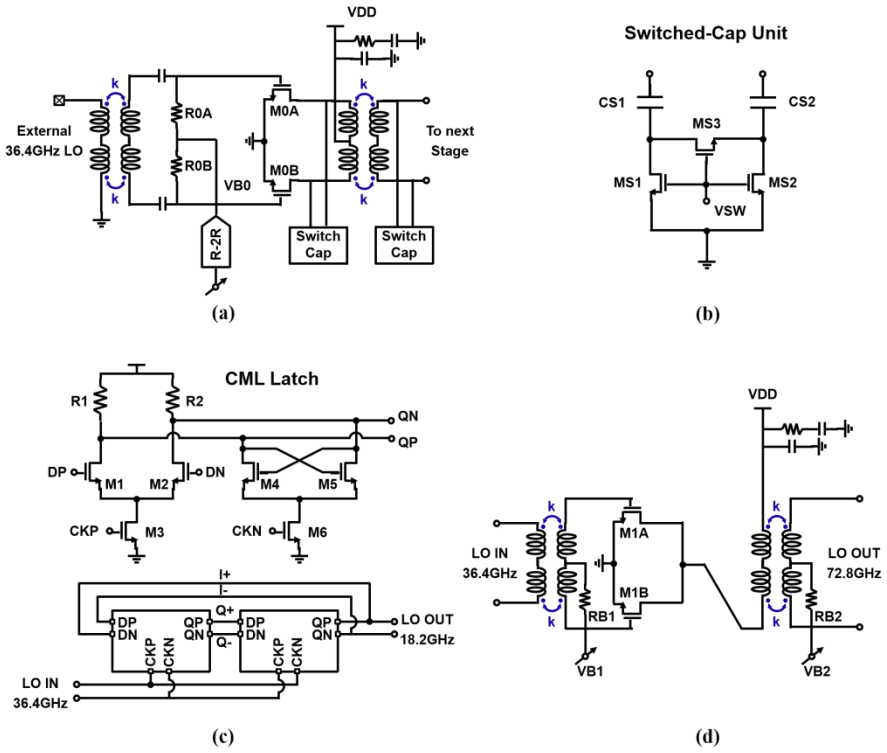
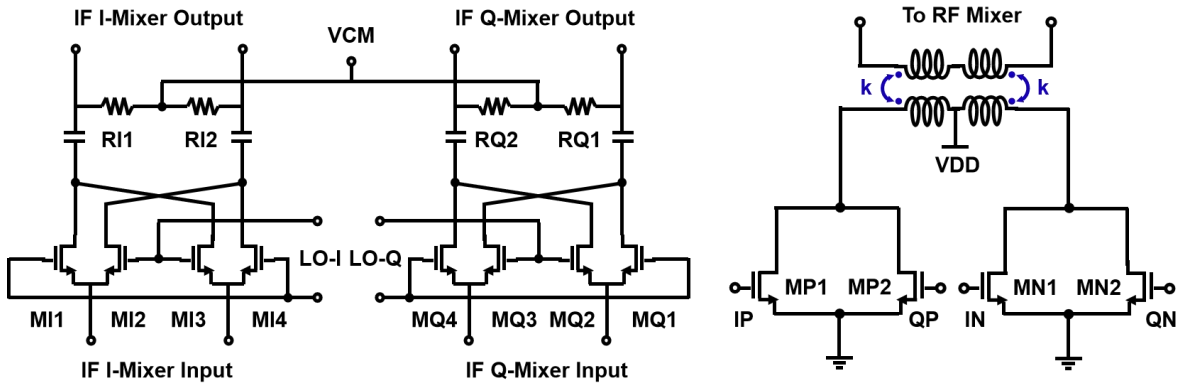


Fig 2.8 Detail of the LO chain, including schematic of (a). LO input buffer; (b). The switched-capacitor unit; (c). CML latch and frequency divider; (d). Frequency doubler

The CML divider's schematic is shown in Fig. 2.8(c), which consists of two identical CML latches. 18.2 GHz quadrature signal is obtained at the output of each latch. Inductor peaking is not needed to divide down from 36.4 GHz to 18.2 GHz with advanced technology node. The divider's minimum required differential input swing over different process corner is 80 mV in simulation, which can be sufficiently supported by the LO buffer. The schematic of the frequency doubler is shown in Fig. 2.8(d). The second order harmonic current is generated by the push-push pair M1A/M1B, and then injected into the transformer-based resonator tank. DC bias of the push-push pair can be adjusted to obtain the strongest second order harmonic over PVT variations.

2.3.3. Transmitter Design

The radar TX consists of source follower based baseband buffers, a passive IF quadrature up-converting mixer, an IF voltage-to-current converter for I/Q combining, an RF active mixer, and a 3-stage differential PA.



(a) (b)

Fig 2.9 Schematic of (a) The TX IF I/Q up-converting mixer; (b). The TX I/Q combiner

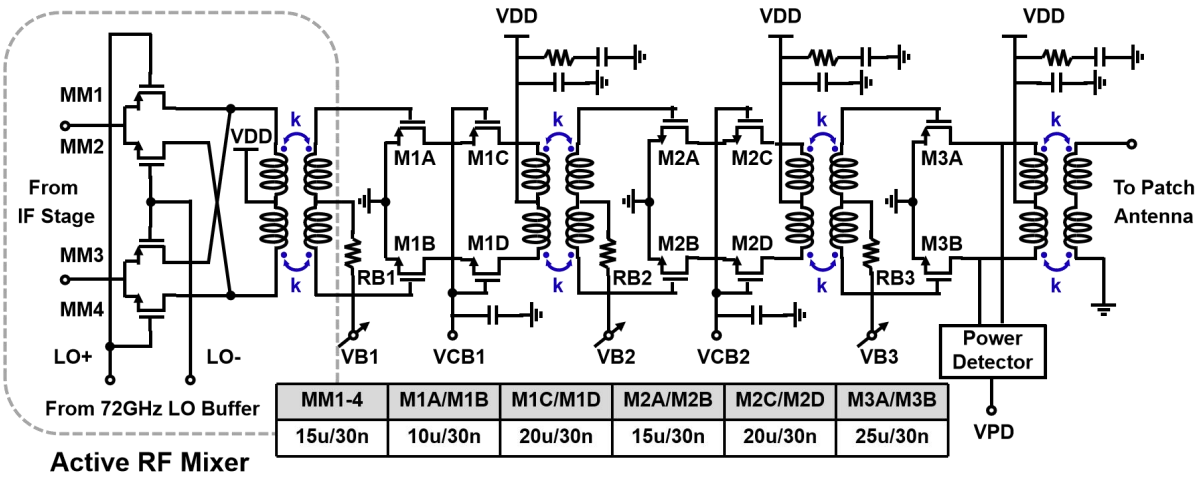
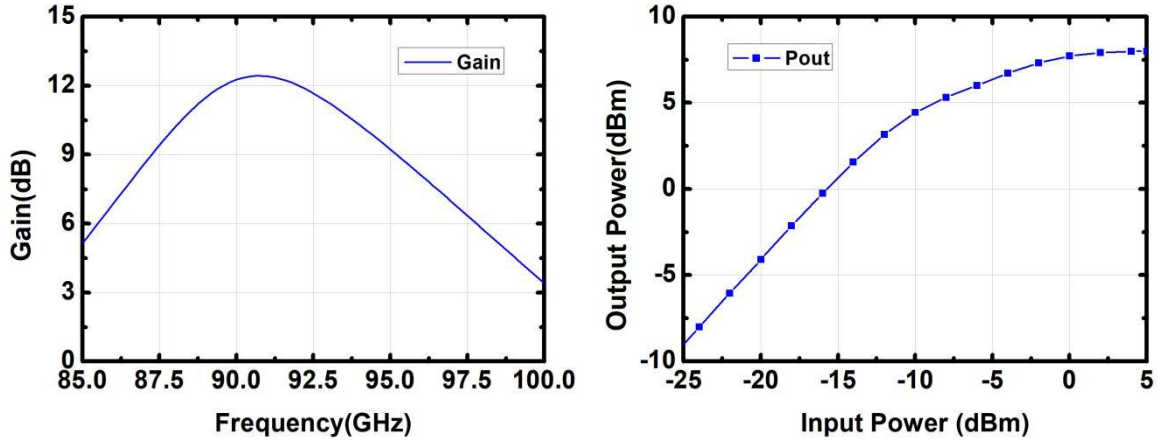


Fig 2.10 Schematics of the RF up-converting mixer and PA



(a) (b)

Fig 2.11 (a) Simulated gain plot of the PA. (c) Simulated P_{in}-P_{out} curve of the PA

Schematic of the TX IF I/Q up-converting mixer is shown in Fig. 2.9(a), it is a passive voltage-mode double-balanced quadrature mixer with AC coupling to the next stage, which is a transformer loaded variable gain amplifier (VGA) providing IF gain control. An I/Q combiner is

implemented after the VGA. As shown in Fig. 2.9(b), transistor pairs MP1/MP2 and MN1/MN2 convert the voltage in both I-path and Q-path into current with the desired polarity.

Fig. 2.10 shows the schematics of the RF up-converting mixer and the differential PA. Transformers are used for PA inter-stage and output matching. Before physical layout and EM simulation, a transformer lumped model is first parameterized to accelerate the design procedure, which includes transformer conductive resistance R_S, parasitic capacitance between the differential feeding traces C_P, primary coil inductance L_1 and secondary coil inductance L_2 [37]. The 1st and 2nd stages of the PA adopt a cascode topology to provide gain, while the 3rd stage adopts a common-source topology for headroom and linearity enhancement. A power detector is placed at the PA's 3rd stage to assist bias control. The PA output power can be reconfigured depending on target range by controlling the bias voltage of the input differential pair.

In simulation, the overall PA achieves 12.3 dB maximum gain at 91 GHz and a 3-dB bandwidth from 87.5 GHz to 95 GHz, as shown in Fig. 2.11(a). The simulated P_{in}-P_{out} curve of the PA is shown in Fig. 2.11(b), the PA OP_{1dB} is 3.5 dBm and P_{sat} is 7.6 dBm. For the radar TX, dynamic range is limited by the PA. However, since the frequency-hopping radar waveform has a constant envelope, the PA does not need to be backed off deeply and can operate in a region close to saturation.

2.3.4. Receiver Design

The radar RX consists of a 2-stage differential low noise amplifier, a passive RF down-converting mixer followed by a transformer-based VGA, an IF quadrature down-converting mixer, and 3-stage CML-based differential baseband amplifiers.

Fig. 2.12(a) shows the schematic of the RX IF I/Q down-converting mixer, which is an active Gilbert-cell-based double-balanced quadrature mixer with resistive load. For the RX baseband amplifier, a 3-stage CML-based differential amplifier is used. Digitally controlled current sources is embedded in the CML amplifier using R-2R DACs to provide baseband gain control, as shown in Fig. 2.12(b).

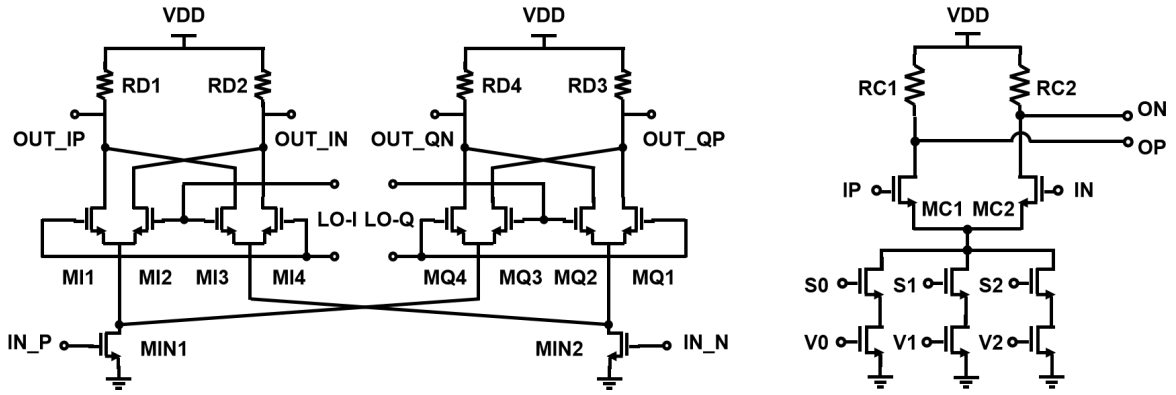
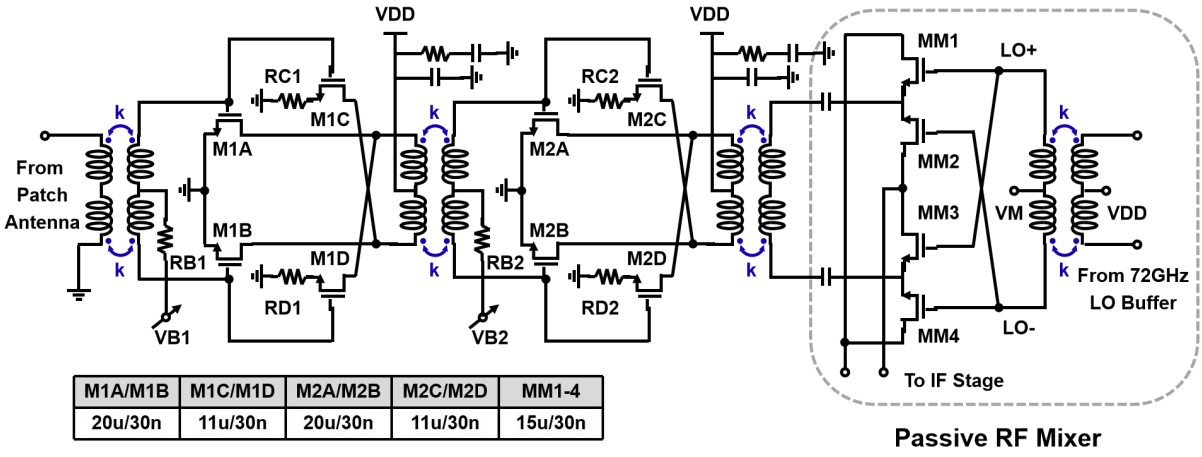


Fig 2.12 Schematic of (a) The RX IF I/Q down-converting mixer; (b). The RX CML-based differential baseband amplifier

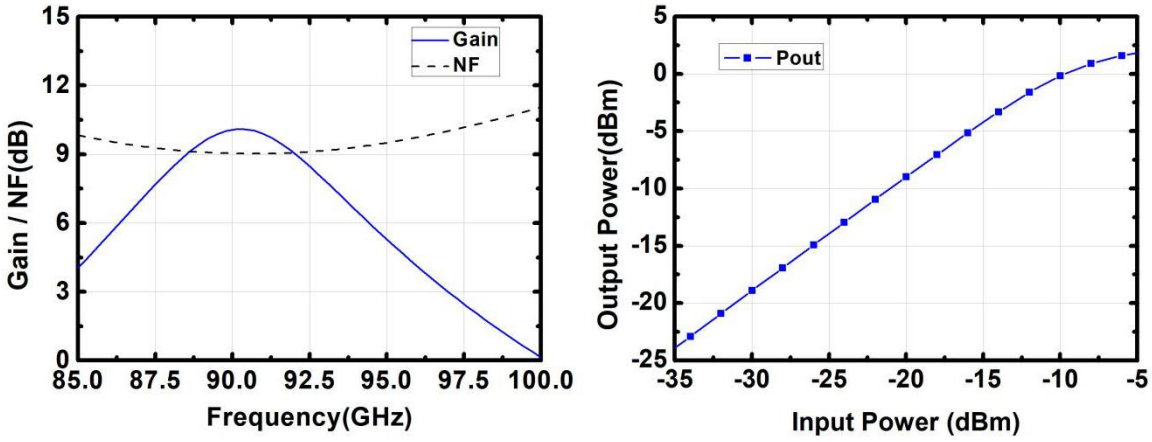
The schematics of the LNA and RF down-converting mixer are shown in Fig. 2.13. An on-chip balun converts the received radar signal from a patch antenna into a differential signal, and offers

ESD protection for the LNA. To avoid desensitization resulted from TX-RX leakage and coupling as well as other unexpected reflections, the LNA is designed to trade off between linearity and noise figure. The C_{gd} of the g_m device (M1A/M1B) is neutralized by M1C/M1D to improve gain and stability, and M1C/M1D is more robust against process variation than an MOM capacitor.



M1A/M1B	M1C/M1D	M2A/M2B	M2C/M2D	MM1-4
20u/30n	11u/30n	20u/30n	11u/30n	15u/30n

Fig 2.13 Schematics of the LNA and RF down-converting mixer



(a) (b)

Fig 2.14 (a) Simulated LNA gain and RX NF. (b) Simulated P_{in}-P_{out} curve of the LNA

Simulated LNA gain and RX NF are given in Fig. 2.14(a), 9.8 dB LNA gain is achieved at 91 GHz with a 3 dB bandwidth of 6.5 GHz. NF of the overall RX is less than 10 dB from 85 GHz to 97.5 GHz, and the minimum NF is 9 dB at 91 GHz. The simulated P_{in}-P_{out} curve of the LNA is shown in Fig. 2.14(b), IP_{1dB} of the LNA is -12 dBm. A passive RF down-converting mixer is employed in this design to enhance linearity. To properly receive a significantly varying echo signal, the gains of the LNA, the RF and baseband amplifiers can be tuned through the on-chip adjustable bias currents and voltages, which are controlled externally through the on-chip digital control interface (USART).

2.3.5. Antenna Design

In order to perform over-the-air measurement and validate the radar system performance, a W-band series patch antenna is designed using High-Frequency Structural Simulator (HFSS). Rogers 4003C with a dielectric constant of 3.55 is adopted as the TX and RX antenna substrate. Under 200um dielectric layer thickness and 18um copper layer thickness, an 1 × 4 patch antenna array with optimized element length of 0.915 mm and width of 0.75 mm is designed. As shown in Fig. 2.15(a), -10 dB return loss S_{11} is achieved across the radar bandwidth from 89 GHz to 93 GHz. The simulated antenna gain is 10.5 dBi, as illustrated in the XZ plane gain plot (Fig. 2.15(b)) and 3-D antenna radiation pattern (Fig. 2.15(c)). Detail of the series patch antenna model in HFSS is shown in Fig. 2.15(d).

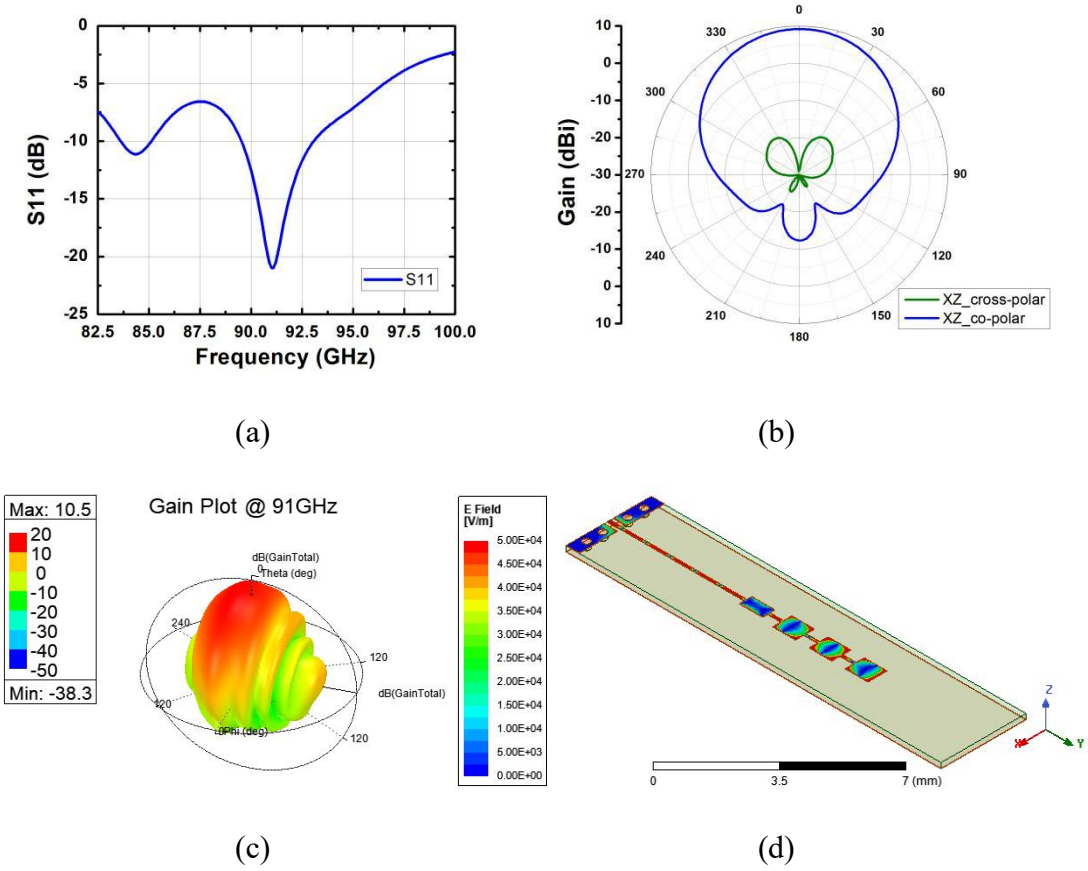
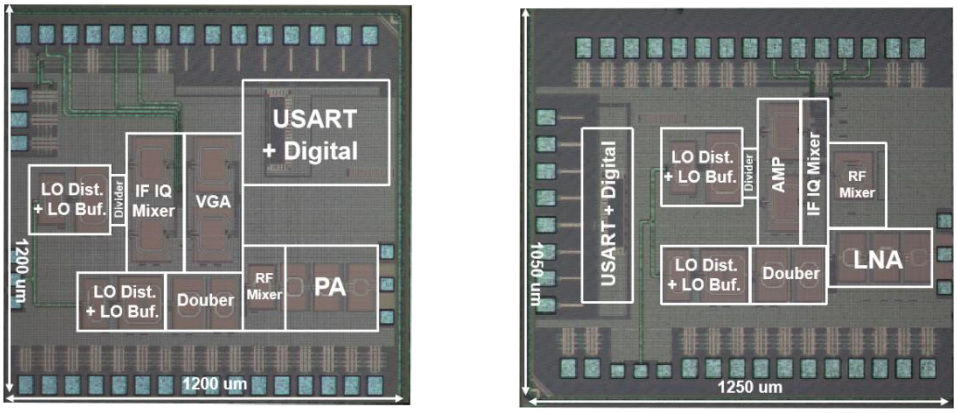


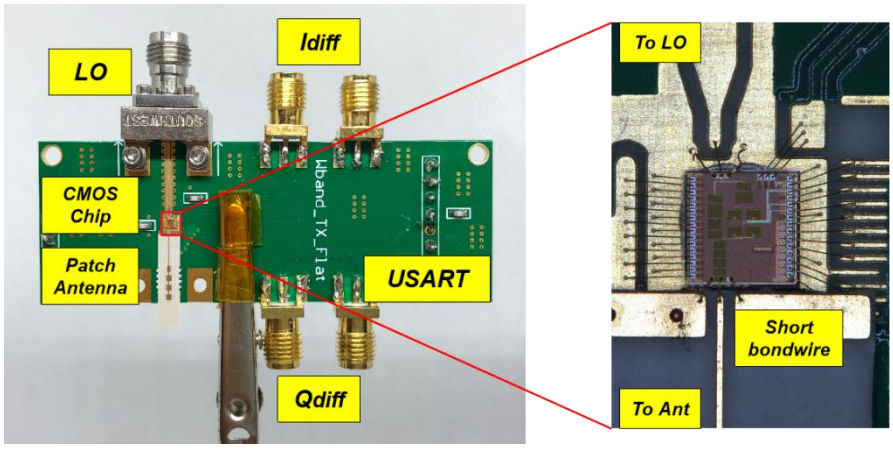
Fig 2.15 (a) Simulated return loss S11 of the antenna. (b) Simulated XZ plane gain plot. (c). Simulated 3-D antenna radiation pattern. (d). Series patch antenna HFSS model

2.4. Measurements and Discussions

The W-band FHCW radar TX and RX chips are fabricated in 28-nm CMOS technology with seven metal layers and an ultra-thick top metal of 3.5 um. Fig. 2.16(a) and (b) show the TX and RX chip micrographs, respectively. The chip area including pads is 1.44mm^2 for the TX chip and 1.31mm^2 for the RX chip.



(a) (b)



(c)

Fig 2.16 Chip micrographs of (a) the radar TX chip; (b) the radar RX chip. (c) TX (RX) module with the TX (RX) chip and a Rogers patch antenna

The typical conversion gains of the TX and RX are 9 dB and 30 dB, respectively. Under a 0.9-V supply, the TX and RX chips consume 145 mW and 128 mW, respectively. Power breakdown between circuit blocks in the TX and RX is summarized in Table 2.3. As depicted in Fig. 2.16(c), a cost-effective TX (RX) module with the TX (RX) chip, a Rogers patch antenna, and FR4 substrate is designed and fabricated with wire-bonding assembly. For chip-to-antenna

interconnection, the length of bondwires are kept below 200 um to reduce insertion loss and maintain decent impedance matching at the operation frequency.

	Circuit Block	Power (mW)
TX	IF Chain	27.2
	RF Mixer	8.5
	PA	43
	TX LO and other buffer stages	66.3
RX	LNA and RF Mixer	23.1
	IF Chain	19.6
	Baseband Amplifier	16.2
	RX LO and other buffer stages	69.1
	Total	273

Table 2.3 Summary of the radar TX/RX power consumption

2.4.1. Radar TX/RX Measurement

The over-the-air (OTA) measurement is conducted with the TX and RX modules to authentically characterize the overall performance of the FHCW radar. First, a Keysight N9041B UXA signal analyzer with a horn antenna is used to capture an 89.5-90.5 GHz FHCW signal transmitted by the TX module. Fig. 2.17(a) shows the captured 1-GHz spectrum. Second, to avoid the equipment's relatively high noise floor at W-band for better characterizing the radar signal, an 89-93 GHz FHCW signal (transmitted by the same TX module) is first down-converted by an Eravant 88-GHz mixer and then sampled by a Keysight MSOS054A Oscilloscope. Fig. 2.17(b) shows the captured 4-GHz spectrum in a Keysight 89600 vector signal analyzer (VSA).

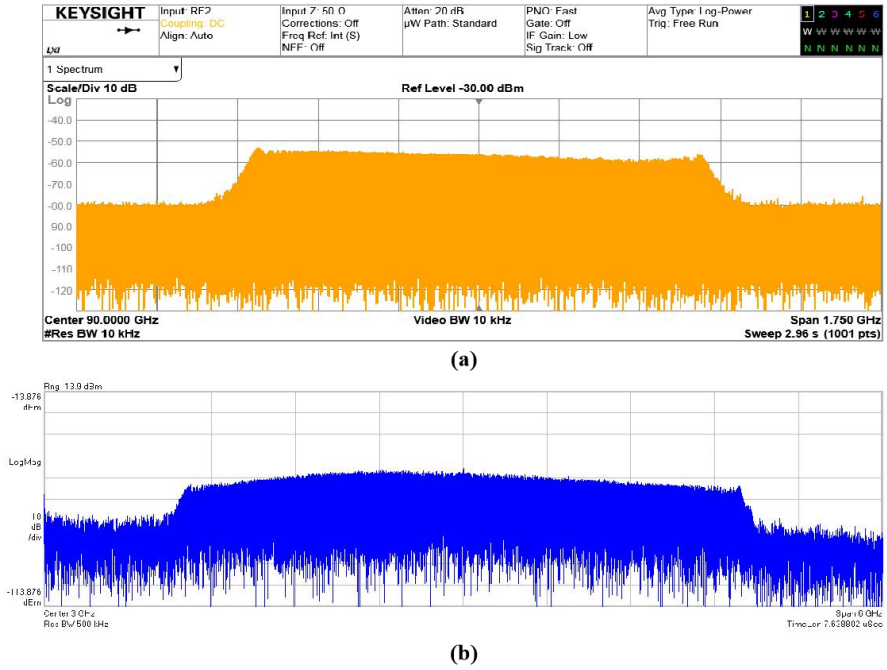


Fig 2.17 Spectrum of the transmitted FHCW radar signal (a) 89.5-90.5 GHz (1-GHz BW) captured by a Keysight N9041B UXA signal analyzer; (b) 89-93 GHz (4-GHz BW) shown in Keysight 89600 VSA (down-conversion through an Eravant 88-GHz mixer)

Phase noise (PN) profile of the transmitted FHCW radar signal is shown in Fig. 2.18. The measured PN is less than -110.0 dBc/Hz at 1MHz offset from a 91-GHz carrier frequency. This superior phase noise performance is obtained mainly from a clean external LO source and the carefully designed LO circuits. The transmitted output power is measured to be 7.1 dBm, the measured TX LO leakage is less than -25 dBm, and image rejection ratio (IRR) is larger than 28.3 dBc. The RX NF is 10 dB and IP_{1dB} is -12 dBm over 89-93 GHz.

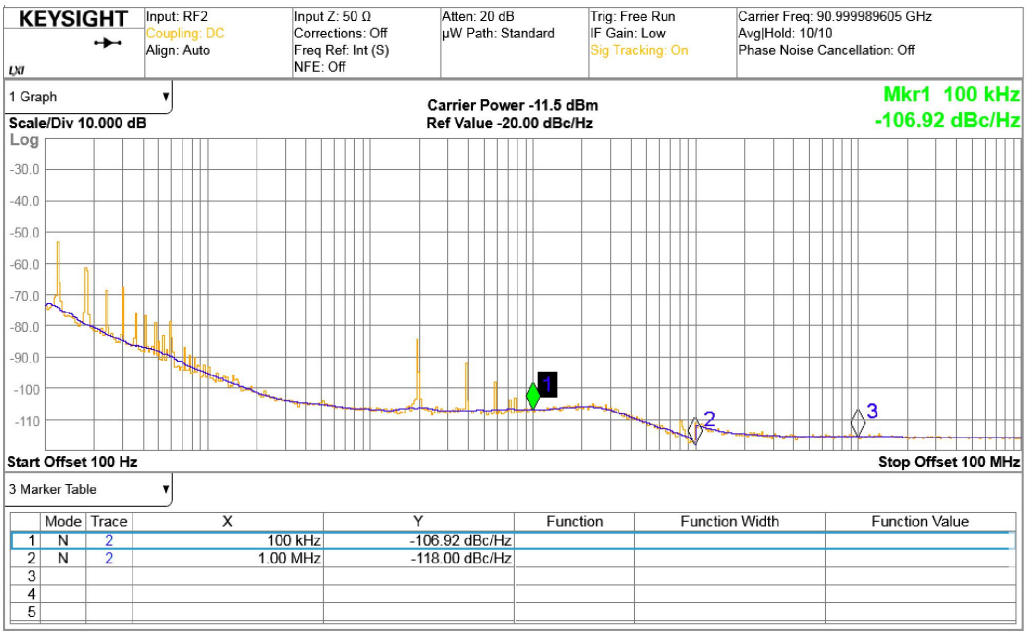


Fig 2.18 Phase noise profile of the transmitted FHCW radar signal

2.4.2. Radar Demonstration

As shown in Fig. 2.19(a), a single user OTA radar test is first conducted to characterize the FHCW radar end-to-end system performance. Second, a multi-user OTA radar test is performed so as to verify interference-tolerant capability of the FHCW radar, which is shown in Fig. 2.19(b).

The setup for multi-user OTA radar test is depicted in Fig. 2.20, with two different transmitter (TX1, TX2) and one receiver (RX1) involved. TX1 and RX1 serve as the radar device under test (DUT) while TX2 is configured as another user injecting the interference to RX1. Two different frequency hopping codes are used for TX1 and TX2, respectively, and their corresponding signals are generated by a 4-channel arbitrary waveform generator (AWG) M9502A. TX1 and TX2 simultaneously point to the same target, which is a metallic plate 0.5 m

away. RX1 receives the two 89-93 GHz FHCW signals from TX1 and TX2 at the same time, respectively. Baseband output data stream of RX1 is sampled by a Keysight MSOS054A Oscilloscope and then decoded by a FHCW decoder realized in MATLAB.

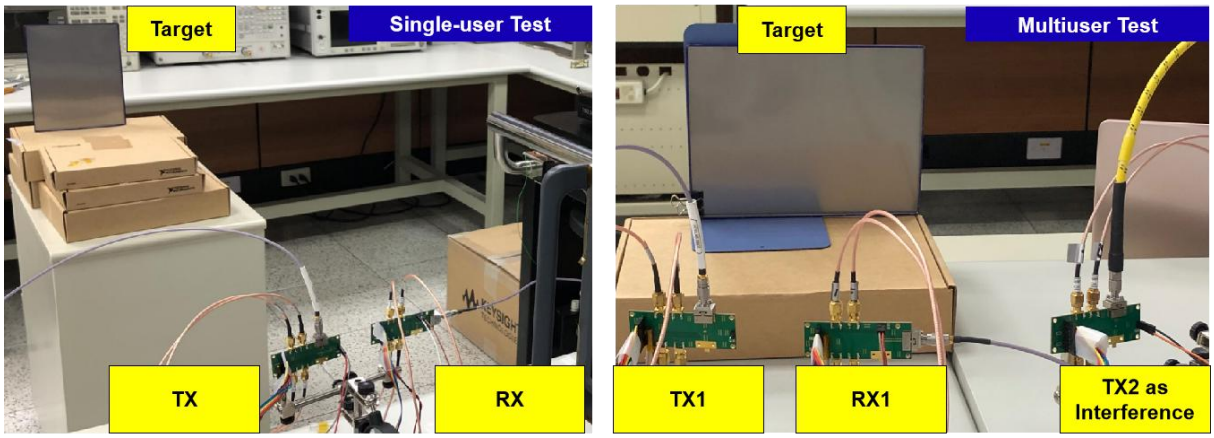


Fig 2.19 Radar demo setup: (a) Single-user test scenario; (b) Multiuser test scenario

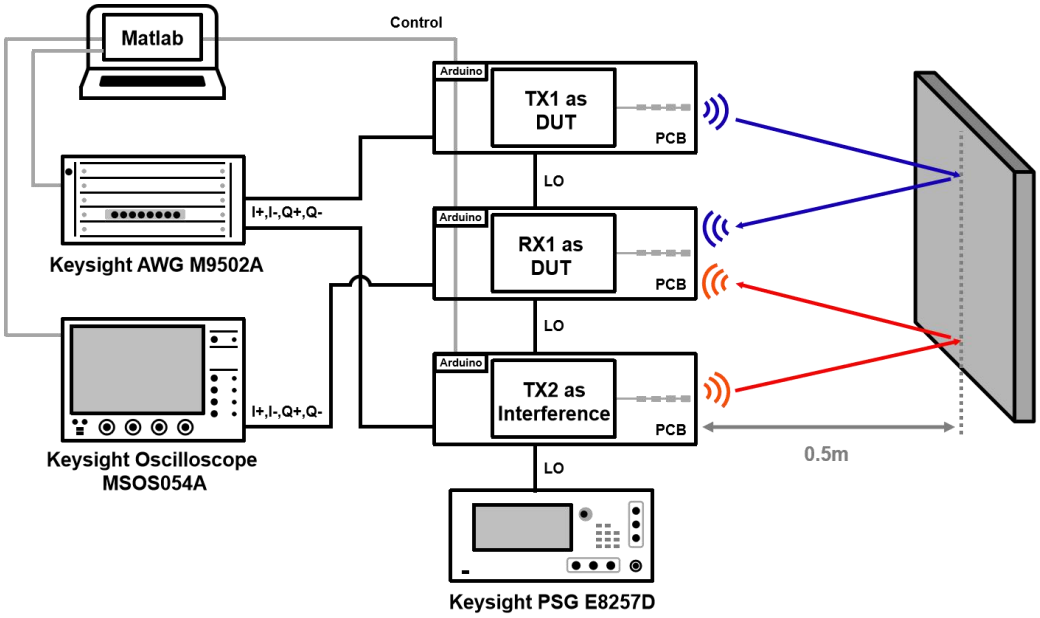


Fig 2.20 Diagram of the setup used for the W-band FHCW radar multiuser interference avoidance OTA test with patch antennas

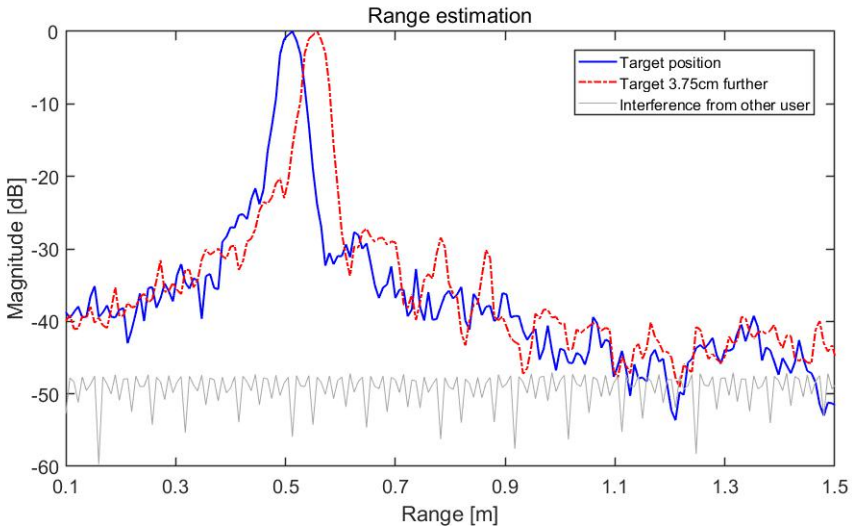


Fig 2.21 Captured range profile from the interference avoidance test with two 89-93 GHz FHCW radars employing two different one-coincident codes, respectively

Fig. 2.21 presents the results of the multi-user OTA test. Two measurement cases are conducted. First, the distance is measured in the reference position (blue curve). Second, the target is moved 3.75 cm (range resolution corresponding to 4-GHz BW) further away from the radar (red curve). Under both cases, clear peaks at 0.5 m are visible, and the interference from the other user (gray curve) is effectively eliminated in the code domain, causing no detection performance degradation.

The promising results demonstrate the multi-user interference avoidance feature provided by the chosen one-coincidence frequency hopping codes. Measured performance in comparison with prior reported state-of-the-art mm-Wave CMOS radars is summarized in Table 2.4. This unique work provides the first interference-tolerant solution for multi-user radar scenario with low chip area (2.75 mm^2) and the lowest power consumption (273 mW) per TRX.

	This work	[1]	[2]	[4]	[5]	[6]
Technology	28nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	45nm CMOS	28nm CMOS
Radar Type	FHCW	FMCW	FMCW	PMCW	FMCW	GMSK PMCW
Multi-user Capability	**Yes**	No	No	No	No	No
Center Frequency (GHz)	91	77	79	79	77/79	77/79
Mod BW (GHz)	4	1.93	4	2	4	2
TX P_{out} (dBm)	7.1	13.2	13	8.5	10.8	8.8[1]
PN (dBc/Hz) @ 1 MHz	**-118**	-87	-91	-85	-91	-110
LO Source	IQ Div+Doubler Ext. Sig. Gen.	Internal PLL	Internal PLL	Internal PLL	Internal PLL	Ext. PLL
RX NF (dB)	10	5	13	12	18	13
RX IP_{1dB} (dBm)	-12	–	-7.5	–	-7	-6.7
Chip Area / #TRX (mm^2)	**2.75**	4.64	2.3	3.95	22 (3TX+4RX)	14 (12TX+8RX)
Power Cons. / #TRX (mW)	**273**	343	700	500	3500[2] (3TX+4RX)	9500[3] (12TX+8RX)
Ant Gain (dBi)	10.5	–	2	–	–	–
Antenna Type	1x4 Patch	–	in-Package	4x4 Patch	–	–
Antenna Size (mm^2)	4x10	–	6x6	20x40	–	–

[1]Total chip output power for 12 TX is 19.6 dBm.
[2]The power is measured for full chip (3TX+4RX) under full duty cycle operation.
[3]The power is measured for overall SoC (12TX+8RX) under full duty cycle operation.

Table 2.4 Performance summary of the FHCW radar and comparison with previous state-of-the-art mm-Wave CMOS radars

CHAPTER 3

A 0.1-4 GHz Direct Sequence Spread Spectrum (DS/SS) Based All-Digital Radar SoC for Ground-Penetrating Application in 28-nm CMOS

This chapter will propose a 0.1-4.0 GHz broadband serial direct-sequence spread-spectrum (DS/SS) based inductor-free ground-penetrating radar (GPR) system-on-chip (SoC). A time-domain digital correlation-based time-of-flight measurement is employed for radar ranging instead of a frequency chirp or pulse [9], which allows a higher degree of flexibility. With no conventional RF up/down conversion present, the radar offers complete programmability over frequency and bandwidth up to 4.0 GHz. Additionally, since the power hungry FFT processing is no longer required, the DS/SS GPR is highly suitable for low power applications such as planetary exploration.

3.1. Introduction

Ground-penetrating radar (GPR) is a long established technology that can penetrate beneath the ground and help investigate sub-surface environments. It has many applications from surveying construction sites for detecting hazardous buried objects to archaeological excavation for detecting buried artefacts. Moreover, GPR is also an indispensable tool for NASA, ESA and others to explore the remote planetary bodies. Two recent examples are the RimFax GPR launched on NASA's Mars Perseverance Rover and the Wisdom GPR on ESA's ExoMars Rover

mission [38], [39]. GPR allows scientists to peer beneath the surface of planetary bodies and even detect possible water deposits under sub-surface. These space missions present several challenges for GPR implemented with conventional RFIC-style circuitry (with inductor based filters and up/down-converters), most notably that the frequency and bandwidth of the radar must be committed to at the design time. This means that the penetration and resolution trade-off [40] (bigger λ for more penetration / smaller λ for better resolution) must also be committed to prior to the launch time. This is extremely problematic as little is known about the sub-surface conditions that may be encountered before the GPR measurement. In addition, power consumption is another constrain for applications like planetary exploration. Without much sunlight, power will be extremely limited, so a very low power GPR system is required.

Comparing with automotive and other radar systems, GPR is very unique regarding to its operation frequency and the target property [10]. In order to penetrate most surface materials, GPR usually operates at low frequency, for example in the range of 0.5-5 GHz. However, wide fractional bandwidth is still required to get a good range resolution based on equation (1-3). Moreover, since GPR penetrates beneath ground, the typical detection range is 0.1-10 m, and the round-trip loss can be more than 50 dB [10]. For the GPR target property, static scenes with no scatterer in motion is usually considered. Therefore, Doppler related effects is typically neglect in a GPR system. These unique considerations, including a low carrier frequency and a relative high fractional bandwidth actually pose a challenge to the design of conventional FMCW radar. Meanwhile, it is highly motivated to develop a new GPR system and make it more suitable to

applications where the scene is static and no constraint is placed on acquisition time.

To address the above issues, a 0.1-4 GHz energy efficient direct-sequence spread-spectrum (DS/SS) based inductor-free GPR SoC is proposed. As shown in Fig. 3.1, the DS/SS GPR transmits and receives a DS/SS sequence for ranging instead of conventional FMCW chirp. DS/SS sequence is essentially a random bit sequence with equal probably of 0 and 1. At the receiver, delay correlation is performed in analog domain to get the target range information, and therefore a high-speed ADC is no longer required. Without the use of inductor, carrier frequency and bandwidth of the DS/SS radar is software programmable, so that the GPR can be adapted to any encountered sub-surface conditions. Additionally, the DS/SS approach does not require a baseband FFT as the ranging information is naturally produced in time-domain, allowing for much lower power and making the DS/SS radar highly suitable for low power applications such as planetary exploration.

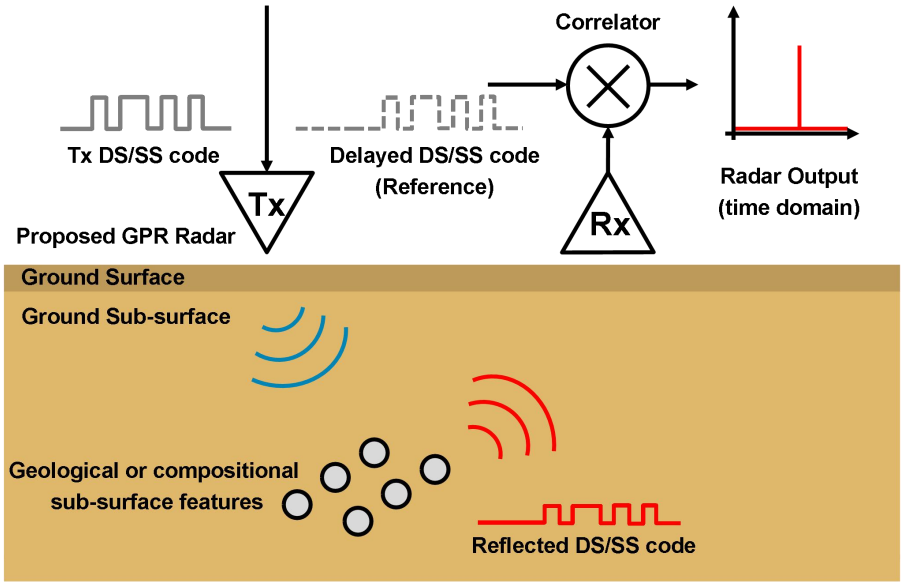


Fig 3.1 Proposed DS/SS based delay-correlating GPR

3.2. New DS/SS Based Delay-Correlating Radar SoC for GPR Application

3.2.1. DS/SS Radar System-on-chip

The block diagram of the proposed radar SoC is shown in Fig. 3.2. The transmitter (TX) consists of a wide tuning range phase-locked loop (PLL) providing programmable carrier frequency, a digital DS/SS sequence generator, a modulator and a wideband power amplifier (PA). The output of the digital DS/SS sequence generator directly modulates the output of the carrier PLL under on-off keying (OOK). A second global PLL provides digital clock for both TX and RX sequence generators.

A non-coherent receiver (RX) is implemented with an envelope detector (ED) after a wideband low noise amplifier. The ED output is correlated against the reference DS/SS sequence through an analog multiplier-based correlator. The reference DS/SS sequence is obtained by digitally delaying the TX sequence. For simplicity and more precise delay control, the same DS/SS sequence generator is duplicated in both transmitter and receiver rather than distributing the signal between them. Two generators start the same DS/SS sequence when the positive edge of each external trigger arrives. However, the trigger for the reference DS/SS sequence generator is delayed by a programmable delay block further controlled by a digital counter. The counter counts the number of triggers received, causing each DS/SS sequence to be incrementally delayed and therefore implementing the time-swept behavior of the reference DS/SS sequence. As the RX system only interrogates the received envelope not the phase, the phase noise requirements of the TX PLL are relaxed [37], allowing the use of a wide tuning range ring-VCO.

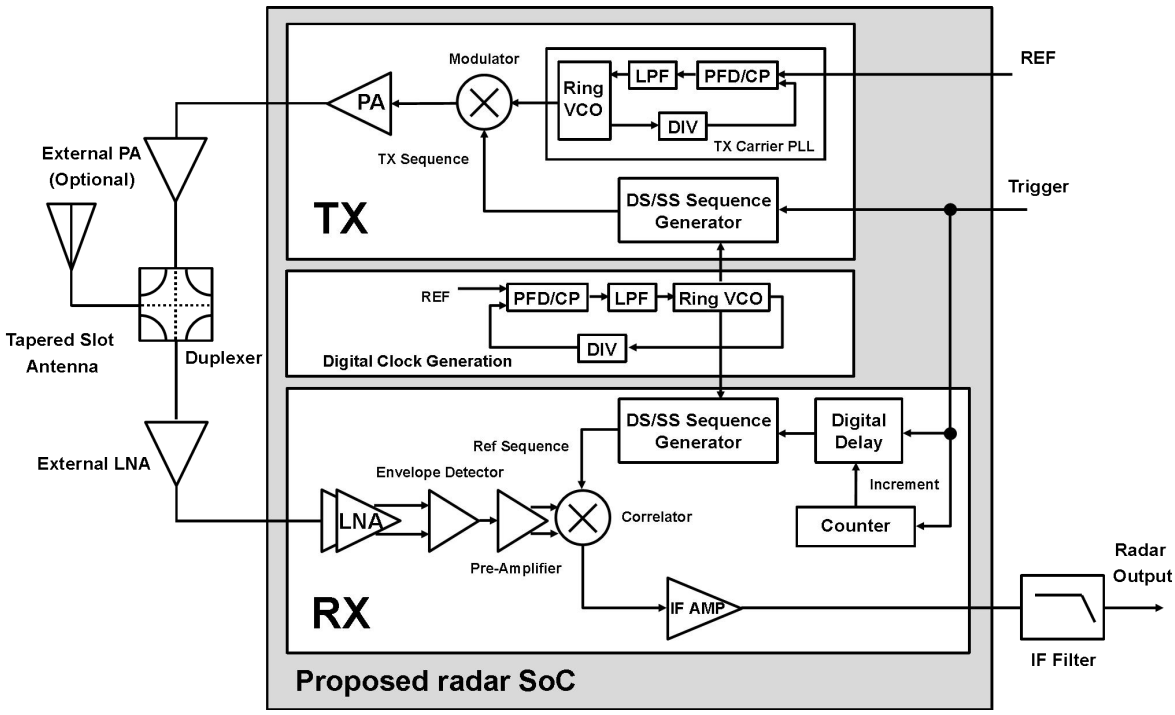


Fig 3.2 Block diagram of the DS/SS radar SoC

As shown in Fig. 3.2, external PA and LNA can be used to further extend penetration range of the proposed GPR SoC. With the use of a duplexer, only one tapered slot antenna is adopted for the radar system. In the radar IF path, time domain radar range information can be read out after an off-chip low-pass filter. There are many advantages to use this DS/SS approach for GPR ranging. First, it allows a higher degree of flexibility as a transmitter DAC and associated anti-alias filters are not required, while still offering the duty cycle benefits of continuous wave operations. Second, with no conventional RF up/down conversion present, the radar offers complete programmability over frequency and bandwidth. Third, without the use of a high speed ADC and baseband FFT, the DS/SS radar architecture lends itself well to low power consumption, which is crucial for low power GPR applications like planetary exploration.

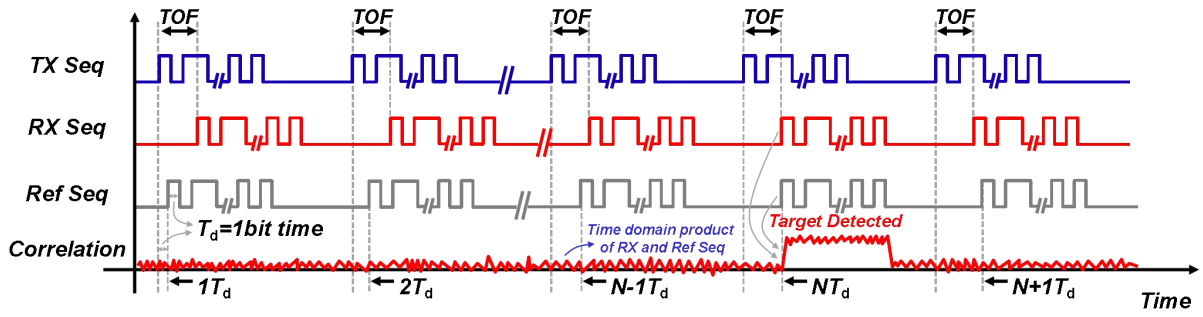


Fig 3.3 Key time-domain waveform showing how the target is detected when the round-trip time-of-flight (*ToF*) matches counter delay of the receiver reference DS/SS sequence

3.2.2. DS/SS Radar Ranging Principle

Fig. 3.3 illustrates the key time-domain waveform of the proposed radar system and demonstrates the DS/SS radar ranging scheme. The generated DS/SS codes are essentially a random bit sequence with equal counts of 0s and 1s. The length of the DS/SS sequence is designed to be programmable to tradeoff among acquisition time and effective signal-to-noise ratio (SNR), and maximum unambiguous range. The default sequence length is 32767 bits.

Assume there is one target at distance d away from the radar. The round-trip time-of-flight (*ToF*) will be $2d/c$, where c is the speed of light. DS/SS radar TX keeps transmitting a DS/SS bit sequence (transmitted sequence). The radar RX captures the reflected signal from the object (received sequence), which is actually a time-shifted version of the transmitted sequence and the time-shift is equal to *ToF*. At the same time, the radar RX generates a tunable delayed copy of the transmitted sequence (reference sequence). The time delay of the reference DS/SS sequence is incremented by 1-bit time $T_d=1/BW$ at each repetition. The reference sequence is repeatedly

correlated against the received sequence through the RX correlator. When the reference sequence and received sequence are not lined up, their correlation result will be low because the DS/SS sequence is a random bit sequence with equal probably of 0 and 1, and therefore it is uncorrelated with the time-shifted version of itself. When the reference sequence and received sequence are lined up (in the case where the time delay is NT_d in Fig. 3.3), their correlation result will be high since the DS/SS sequence is correlated with itself, indicating a target existing at the range where *ToF* is equal to NT_d.

3.2.3. DS/SS Radar Range Bin

The correlation results from each shifted reference sequence is a "range bin" as it indicates if a target exists at the range with *ToF* equal to the time shifted. The bit-rate (bandwidth) of the DS/SS sequence sets the minimum time delay T_d that the reference sequence can shift and therefore sets the range resolution of the proposed radar. In actuality, the returns often occur at times between two different range bins and their correlated energy is spread between them, still allowing the target to be detected with no SNR degradation.

Since the unit bits of the DS/SS code is a rectangular function, its auto-correlation can be calculated as (3-1) and (3-2), where T_d is the chip time (1-bit time T_d=1/BW), N is the sequence length and $s_c(t)$ is the DS/SS code.

$$R_{xx}(\tau) = \frac{1}{NT_d}\int_0^{NT_d} s_c(t) \times s_c(t-\tau)dt \qquad (3\text{-}1)$$

$$R_{xx}(\tau) = \begin{cases} 1 - |\tau|(N+1)/NT_d, & |\tau| \le T_d \\ -1/N, & |\tau| > T_d \end{cases} \quad (3\text{-}2)$$

Fig. 3.4(a) shows the auto-correlation functions of 3 continuous DS/SS code, which are triangle functions. As shown in Fig. 3.4(b), if the received DS/SS code is misaligned within $1T_d$ from two continuous reference code, bin splitting behavior will happen [41]. Misaligned DS/SS code will spread into 2 range bins, and detection amplitude of the two range bins will be proportional to the overlaps portion with the captured code. Under very high SNR case, range information can be further estimated beyond c/2B based on misalignment weighting.

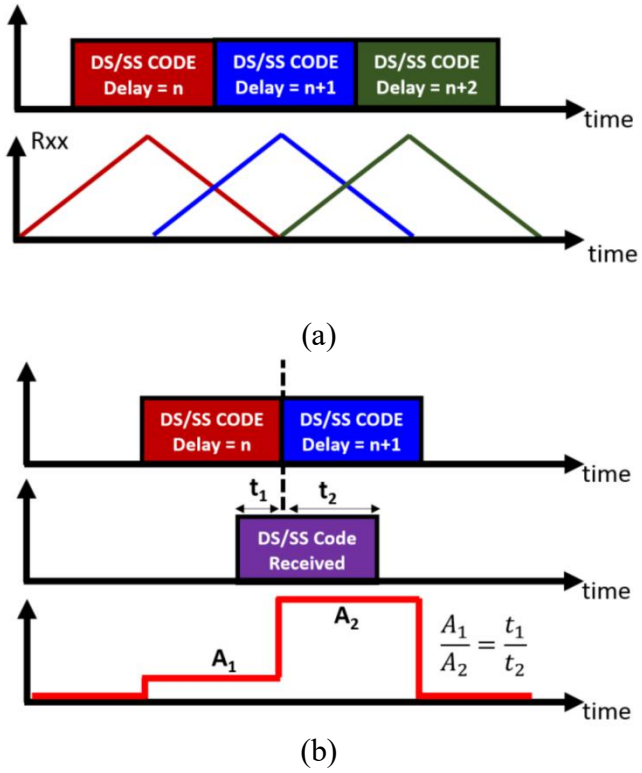


Fig 3.4 (a) 3 continuous DS/SS codes and their auto-correlation functions. (b) Bin splitting behavior resulted from a misaligned captured DS/SS code [41]

Based on the auto-correlation function, radar robustness to clock jitter can also be analyzed. For a 1 GHz digital clock, the chip time T_d=1ns, and the simulated ring-VCO based PLL rms jitter is less than 300fs. This tells us that the rms jitter only occupies 0.03% of T_d and it almost does not affect the overall auto-correlation value. Therefore, DS/SS radar is very robust to clock jitter, which promises the use of ring-VCO in the clock PLL for an inductor-less design.

In the proposed DS/SS radar system, the bandwidth of the sequence is fully programmable up to 4GHz. With a 2GHz bandwidth, the range resolution is 7.5cm. Since the default sequence includes 32767 bits, each DS/SS sequence takes 16.4us to complete. 255 successive range bins have been implemented to cover a maximum range swath of 19m, which is enough for ground-penetrating application. Longer detection range can be achieved through reducing radar bandwidth. To further reduce the total measurement time, the reference delay can be programmed to sweep from iT_d to jT_d (i, j are programmable) instead of starting from 0 to $255T_d$. This works in the case when it is only interested in examining targets over a small range swath rather than the entire detecting range starting from the radar system's position. The maximum acquisition time for a 50-bin range swath is 0.82ms.

3.2.4. DS/SS Radar Dynamic Range Analysis

As shown in Fig. 3.5, there are two major noise sources in the radar receiver that can limit the receiver overall dynamic range: thermal noise and the noise coming from the uncorrelated DS/SS code. Let's calculate the contribution of thermal noise first. Assuming the receiver noise figure is 5dB under 1GHz-BW, with a non-coherent detection penalty of 5dB, thermal noise

power at the receiver input in decibel meters can be calculated from

$$P_{therm} = 10\log_{10} kTBW + NF \tag{3-3}$$

where kT is thermal noise floor at room temperature, and P_{therm}=-74 dBm. Because the radar signal is correlated to itself and noise is totally uncorrelated by its nature, correlation at the receiver baseband can help improve the overall SNR by

$$G_{corre} = 10\log_{10}(T_{corre}/T_d) \tag{3-4}$$

T_{corre} is overall correlation time for a DS/SS sequence (assume T_{corre}=1ms, which means the bandwidth after correlator BW_{after}=1/T_{corre}=1kHz), and T_d=1/BW_{before}=1ns is the chip time of the 1 GHz-BW DS/SS code. With these parameters, G_{corre}=60 dB. Therefore, the thermal noise induced DR is given by

$$DR_{therm} = P_{in} - P_{therm} + G_{corre} = P_{in} + 134\ dB \tag{3-5}$$

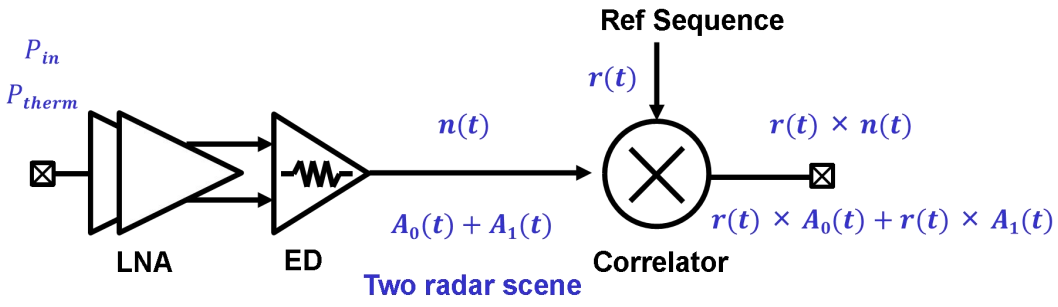


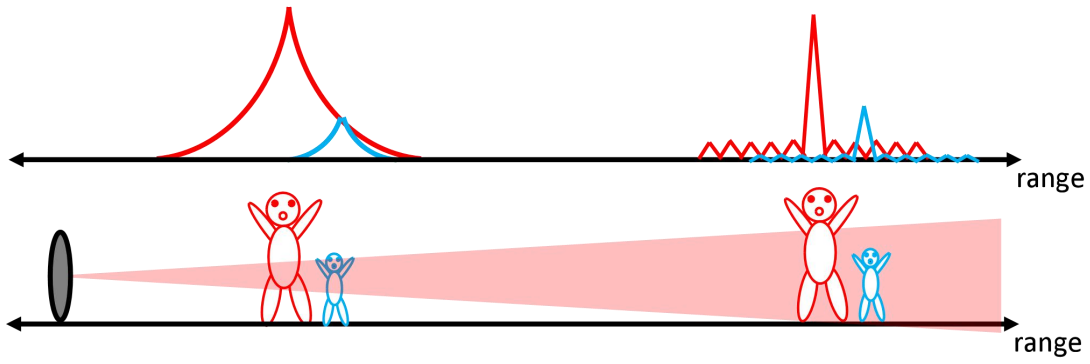
Fig 3.5 Thermal noise and the noise from uncorrelated code in the radar receiver

Regarding to the noise from the uncorrelated DS/SS code, since the bandwidth before and after correlator is 1GHz and 1KHz respectively, the DS/SS noise suppression or uncorrelated code induced DR can be calculated by

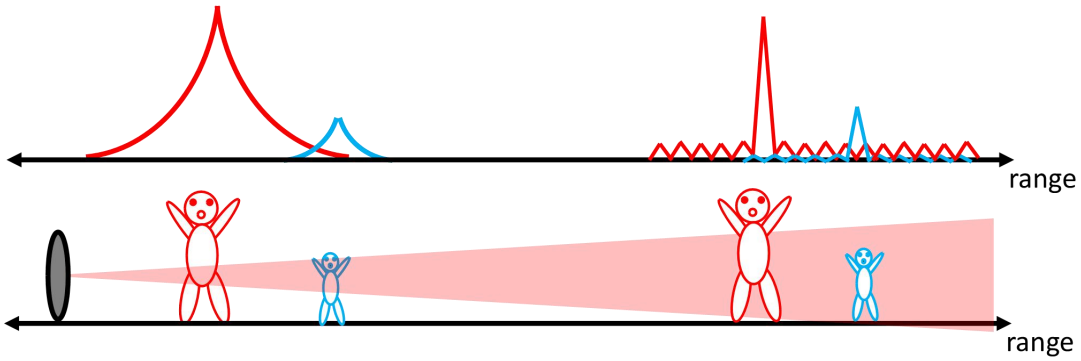
$$DR_{corre} = 10\log_{10}(BW_{before}/BW_{after}) = 60\ dB \qquad (3\text{-}6)$$

For typical GPR case, P_{TX}=10 dBm, path loss L_{path}=50 dB, P_{in}=-40 dBm, the resulted DR_{therm}= 94dB and DR_{corre}= 60dB. Therefore, for a DS/SS radar, dynamic range is usually limited by the uncorrelated code.

Furthermore, DS/SS radar can be considered reconfigurable because the uncorrelated code induced dynamic range is set by the time-length of the DS/SS sequence. The longer the sequence length, the lower the auto-correlation of the misaligned sequences will be. However, in such case the radar integration time will be longer. To sum up, it is a trade off between time and accuracy. For typical GPR application, where the radar scenes is static, DS/SS radar with a reconfigurable sequence length could be a suitable candidate to obtain high accuracy under the cost of more time.



(a)



(b)

Fig 3.6 Dynamic range comparison between DS/SS and FMCW radar: (a) When two targets are very close to each other. (b) When two targets are far away from each other

Dynamic range of a DS/SS radar system in comparison to state-of-the-art FMCW radar system is explained here:

As shown in Fig. 3.6(a), when two targets are very close to each other, conventional FMCW radar struggles in-close because the phase noise skirt can hide weak signals. The DS/SS waveform has lower auto-correlation at small range offsets compared to phase noise skirt levels, so it's easier to see targets close together with different amplitudes.

When two targets are far away from each other in Fig. 3.6(b), as range diversity increases between two targets, FMCW radar dynamic range improves while that of DS/SS radar stays the same.

In summary, for GPR application where the targets are stationary and close to each other, a DS/SS radar system can be a good alternative to state-of-the-art FMCW system with its robustness against phase noise skirt, as well as its superior power efficiency.

3.3. Radar Building Blocks and Key Circuit Design

3.3.1. Radar Transmitter

Fig. 3.7 shows the key circuits in the DS/SS radar TX chain. No inductor is used for the TX building blocks. A 1.0-4.0 GHz ring-VCO based Type-II PLL is designed for TX carrier generation, with 0.1-1.0 GHz available in the PLL-bypass mode. The envelope detector in the radar receiver removes the phase information prior to correlator, so the phase noise is less critical. An eight-stage inverter-based ring oscillator with a 2-bit programmable forward-interpolating buffer is adopted. Interpolating between phases that are nominally 90 degree apart with varying strength servers as a compact, low noise coarse-tuning alternative to switched capacitors and current-starving [42]. Small varactors are added at each stage for a reasonable K_{VCO}.

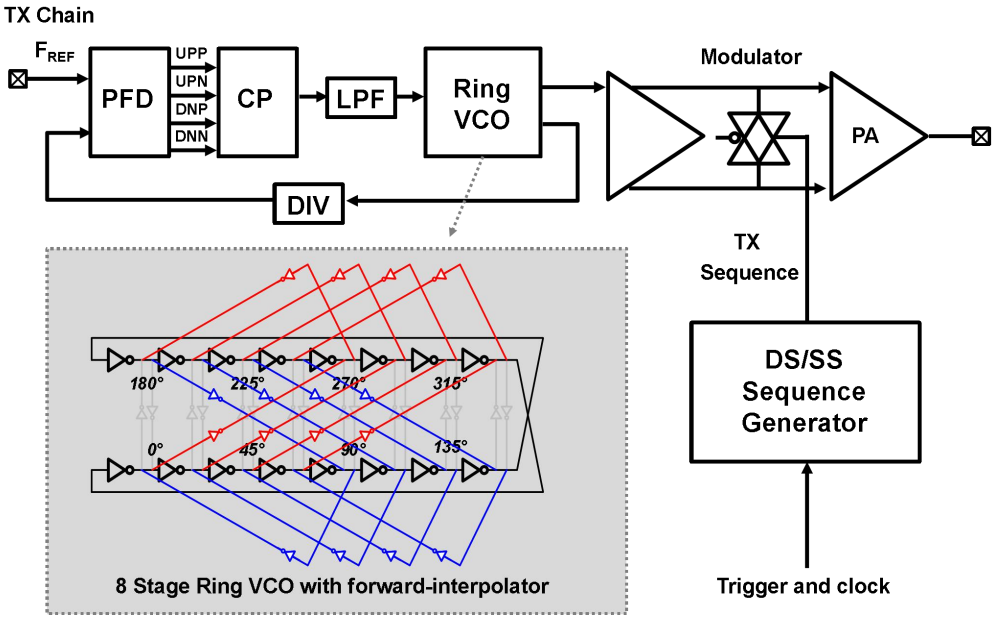


Fig 3.7 Building blocks of TX chain, and circuit implementation of the ring VCO

Deferential switch-based modulator is adopted for OOK modulation and to suppress the baseband to RF leakage. A resistor loaded wideband PA offers 4.9-5.2 dB gain from DC up to 4.0 GHz. The output power of the PA is 0 dBm. Additionally, this PA could work in standalone mode or serve as a pre-driver if external PA is used.

3.3.2. Clock PLL and DS/SS DSP

The digital sequence PLL provides digital clock for the DS/SS radar DSP (digital signal processor) and offers programmability for the radar bandwidth. It shares the same wide-tuning scheme as TX PLL through the use of ring VCO.

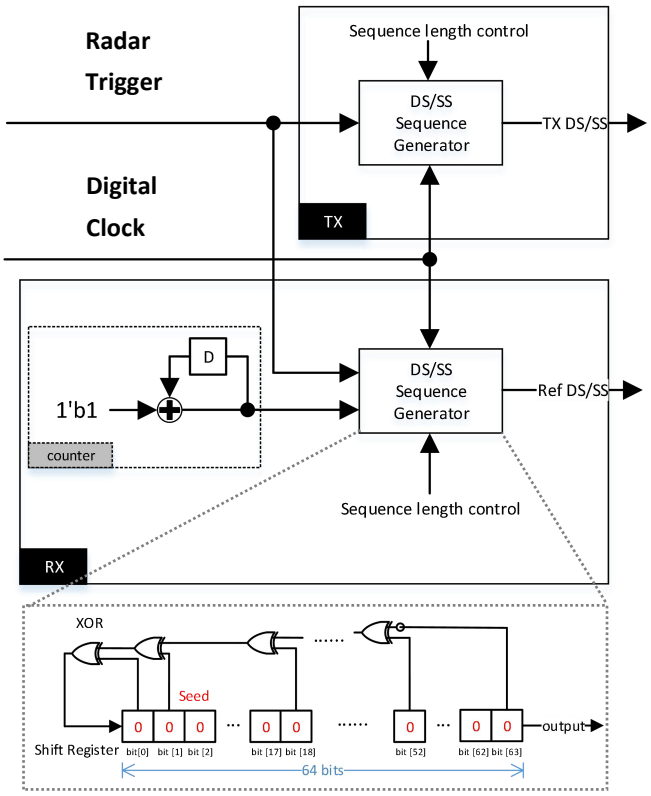


Fig 3.8 DS/SS radar DSP, and detail of the DS/SS sequence generator

As shown in Fig. 3.8, once the radar trigger signal goes up from 0 to 1, indicating the start of DS/SS radar operation, the TX/RX DSP starts to provide periodical DS/SS codes. The DS/SS sequence generator is essentially a pseudo-random binary sequence (PRBS) generator implemented through a 64-bit linear-feedback shift register (LFSR). There is flexibility to tune the effective DS/SS code length by reducing the LFSR number of bits. A 64-bit counter controls the delay of reference DS/SS code in the RX DSP, and the exact counter value is read out to calculate the target range information once the correlation peaks.

After digital synthesis and APR (automatic place & route) in 28-nm CMOS technology, the overall bound area for the DS/SS radar DSP is 9000 um^2 with an utilization rate around 50%. The radar DSP can work up to 4GHz clock rate and it consumes 26.2 mW power under 1 GHz clock rate.

3.3.3. Radar Receiver

On the RX side, as shown in Fig. 3.9, a 2-stage resistor loaded differential LNA offers 12.2 dB gain up to 4.0 GHz with 4.7 dB NF. The LNA is designed to trade between linearity and NF, and -5.9 dBm IP_{1dB} is achieved to mitigate TX-RX leakage and coupling. A resistor-feedback based TIA converts the output current of the envelop detector into voltage and extracts the amplitude information of the received radar signal. The bandwidth of the TIA is tunable through the feedback resistor. Differential outputs of the pre-amplifier are fed into the correlator to correlate against the reference DS/SS sequence. Thereafter, correlator output is further amplified by a resistor loaded IF amplifier and then sent out of chip as radar output. The DC operation

points of all the differential amplifiers in the RX are monitored through an Op-Amp-based sensor for DC offset cancellation.

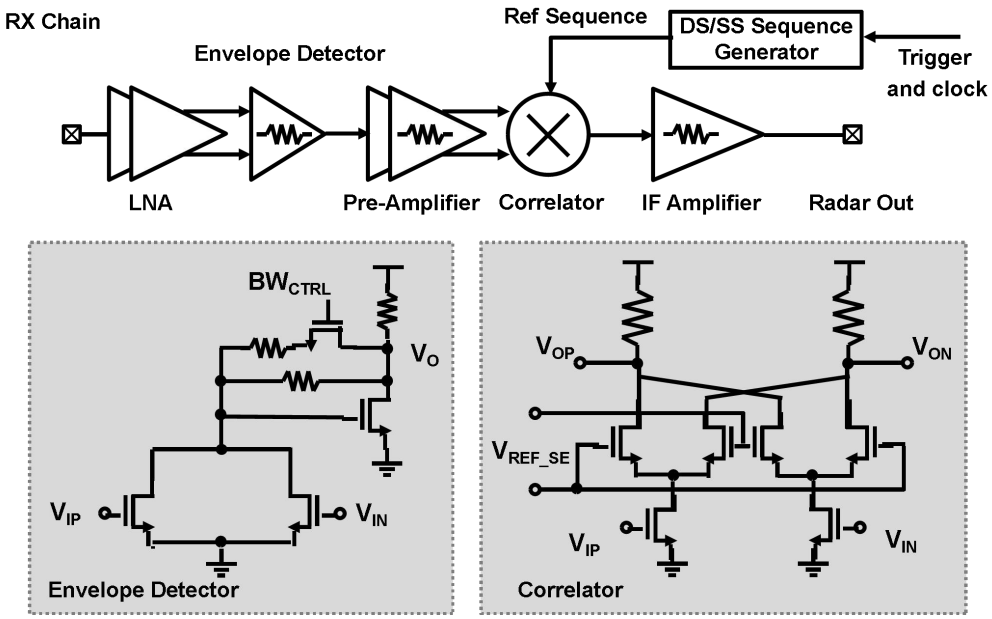
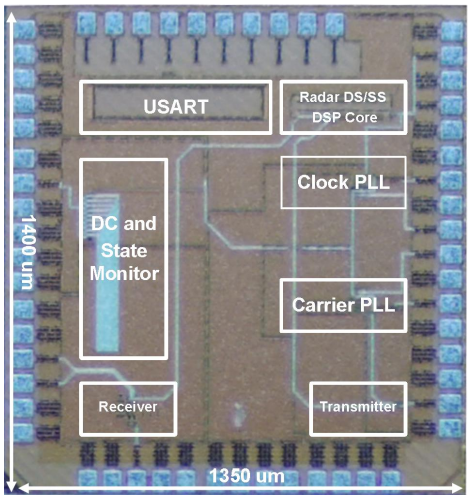


Fig 3.9 Building blocks of the radar RX chain, and circuit implementation of the envelope detector and correlator

3.4. Measurements and Discussions

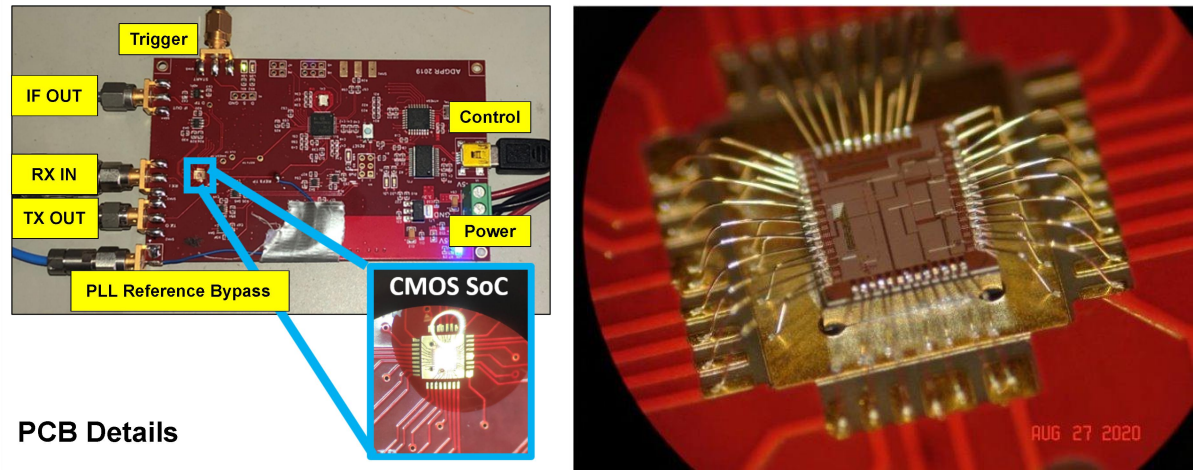
The prototype DS/SS radar SoC is fabricated in 28-nm 1P7M HPC CMOS process. Fig. 3.10(a) shows the chip micrograph. The total chip area is 1.89 mm^2 including pads (1350 um by 1400 um), while the core area is only 0.42 mm^2. From the chip die photo, it is clear that no inductor is used for the SoC design. Under a 1-V supply, the chip consumes 46.2 mW. The power break down of the radar SoC is summarized in Fig. 3.10(b).



DS/SS Radar SoC Power Breakdown	
Transmitter	4.2 mW
Receiver	13.3 mW
Clock PLL	2.5 mW
DS/SS DSP	26.2 mW
Total	46.2 mW

(a) (b)

Fig 3.10 (a) Chip micrograph. (b) Power breakdown of the DS/SS radar SoC



(a) (b)

Fig 3.11 (a) DS/SS GPR PCB detail. (b) DS/SS GPR SoC assembled to PCB

As shown in Fig. 3.11(a), a custom-made printed circuit board (PCB) provides DC power, PLL reference, radar trigger, and control signals for the radar chip. Wire bond is used for SoC-PCB interconnect as shown in Fig. 3.11(b).

3.4.1. Radar Loopback Test

Time domain radar TX output waveform is first measured with a Keysight Oscilloscope DSO6034A. Fig. 3.12(a) and (b) show the TX output waveforms for a 1.0 GHz-BW DS/SS sequence with a carrier frequency of 1.5 and 2.5 GHz, respectively.

(a) (b)

Fig 3.12 (a) Measured time-domain TX waveform with F_C=1.5 GHz and BW=1.0 GHz. (b) Measured time-domain TX waveform with F_C=2.5 GHz and BW=1.0 GHz

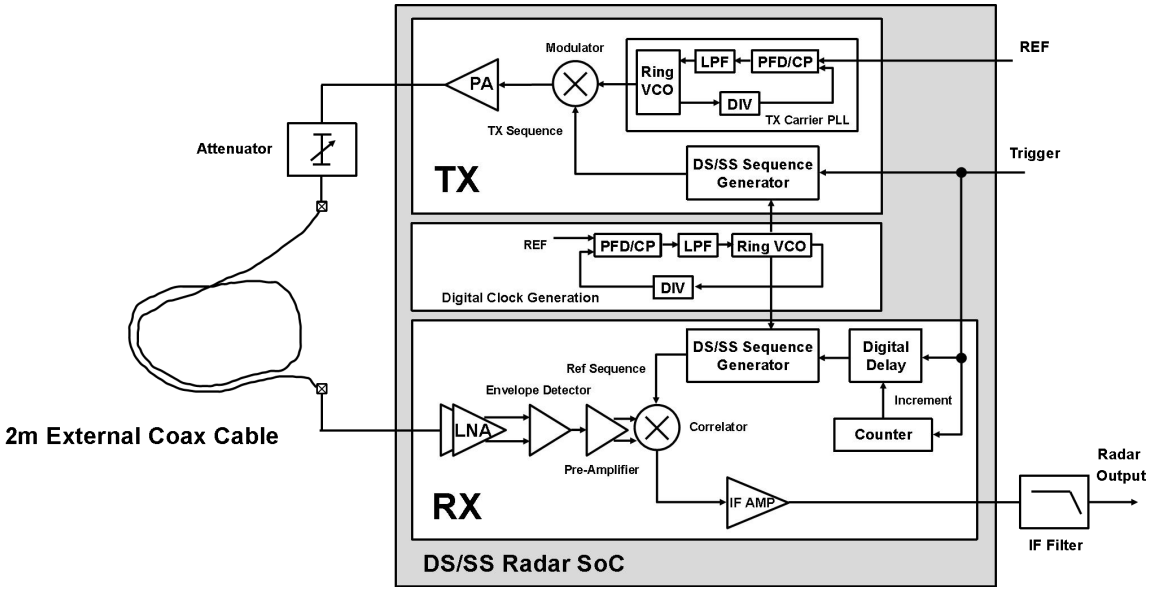


Fig 3.13 TX to RX loopback test with a 2-meter external coaxial cable

To characterize the DS/SS radar function, a direct TX to RX loopback test is done by connecting the TX and RX with a 2-meter long coaxial cable. Fig. 3.13 shows the setup for the loopback the test. The loopback test result is shown in Fig. 3.14, where the radar produces a step signal in the range bin associated with the cable length. Double bounce along the length of the cable is visible as well due to the imperfect matching.

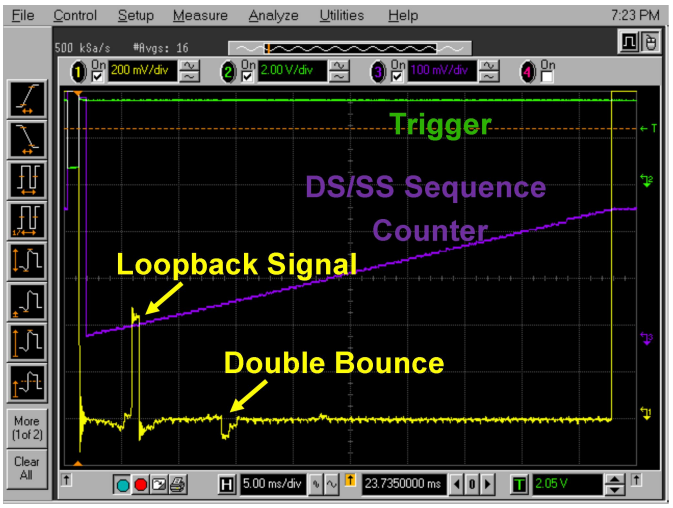
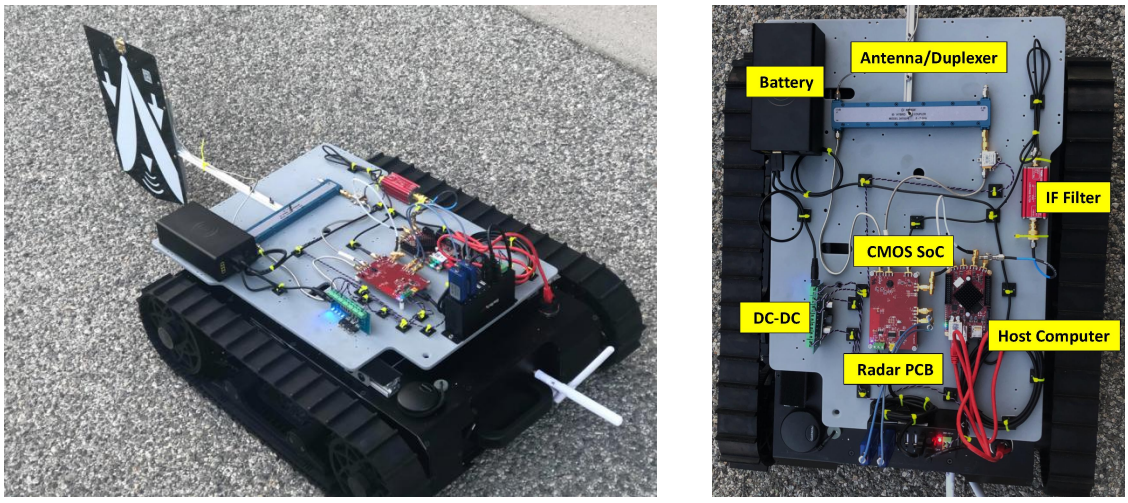


Fig 3.14 DS/SS GPR SoC TX to RX loopback test result

3.4.2. In Field GPR Test

The capability of the DS/SS GPR has been validated for the actual ground penetrating operation. As shown in Fig. 3.15(a), the PCB that contains the GPR SoC is mounted onto a test rover which carries an embedded host computer with a 100 KS/s sampling ADC, an external LNA ZVA-183+ with 3 dB NF and 20 dB gain, a Krytar duplexer with 20dB isolation, and a 10dBi PCB tapered slot antennas (detail shown in Fig. Fig. 3.15(b)).



(a) (b)

Fig 3.15 (a) DS/SS GPR rover prototype. (b) Detail of the DS/SS GPR rover prototype

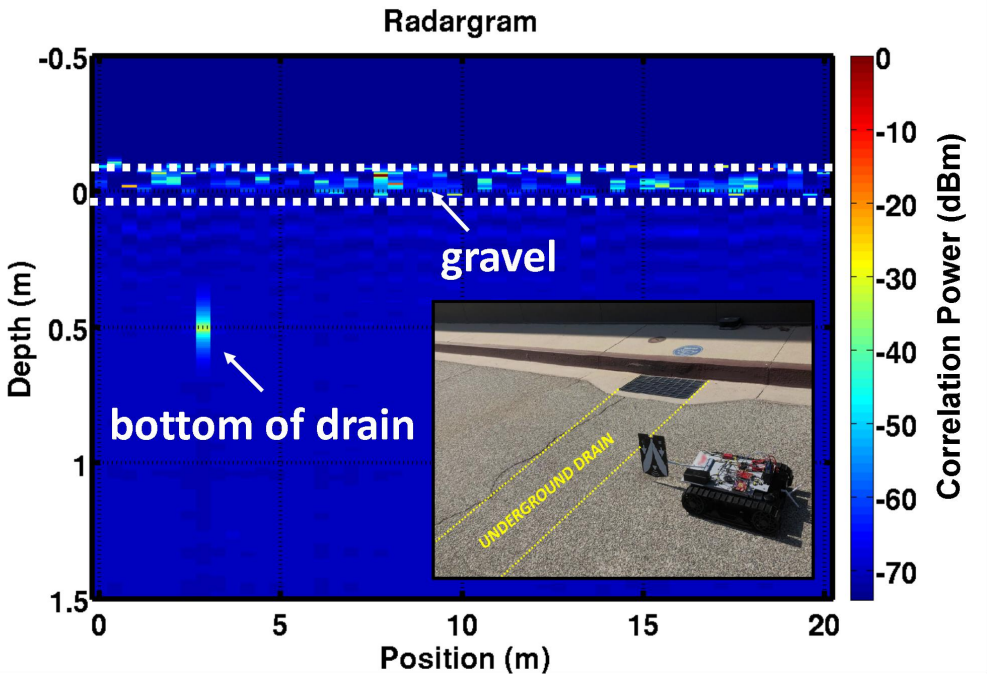


Fig 3.16 Measurement result of the DS/SS GPR with a testing rover over a roadway containing a sub-surface drainage conduit. The road surface, the gravel underneath and the bottom of the drain structure around 0.5m below the road surface are clearly visible

The rover ran over a roadway with a storm drain passing beneath it. From the captured GPR data in Fig. 3.16 (DS/SS correlation power for different depth), it is evidenced that the GPR can clearly resolve the road surface, the gravel layer beneath it, and the bottom surface of the storm drain approximately 0.5m below the roadway surface. This scan has been consistently performed with the same 2.5 GHz carrier / 1.0 GHz bandwidth settings as in the loopback test.

Due to limited number of CMOS GPR reported, Table. 3.1 compares the DS/SS radar with the prior arts operating at similar frequencies for various applications [43-45]. Among all, this presented radar SoC achieves the largest fractional bandwidth due to its inductor-less nature, as well as its superior efficiency in both area (1.89 mm^2) and power consumption (46.2 mW).

	[43] Andersen, JSSC' 17	[44] Chu, ISSCC' 11	[45] Lou, ISSCC' 18	**This work**
Technology	55nm	130nm	65nm	28nm
Frequency	7.2-8.5GHz	2-5GHz	10GHz	0.1-4GHz
Modulation	Impulse	Impulse	FMCW	**DS/SS Code**
Mod. BW	1.4GHz	0.9GHz	1GHz	1GHz (tunable)*
BW/F_c	17.8%	25.7%	10%	**40%****
TX P_{OUT}	0.7dBm	N.A.	10dBm	0dBm
Die Area	8.6mm^2	11.9mm^2	7.8mm^2	**1.89mm^2**
Power Consumption	118mW	695mW	141mW/Ch	**46.2mW*****

*Radar BW can be programmed up to 4.0 GHz. 1.0 GHz BW is used for in-field GPR prototype measurement in Fig. 7.
**Calculated under in-field GPR measurement setup with 2.5 GHz carrier / 1.0 GHz BW. ***SoC power only.

Table 3.1 Performance summary of the DS/SS GPR SoC and comparison with previous state-of-the-art radars

CHAPTER 4

Conclusion and Future Work

This dissertation focused on spread spectrum based digital-intensive radar system design in advanced CMOS processes for automotive and ground-penetrating applications. Specifically, two digital modulated/coded CMOS radars based on frequency hopping spread spectrum and direct sequence spread spectrum have been devised, realized and demonstrated to overcome the conventional analog radar's performance degradation from AM/FM distortions.

First, practical impairments that limit the performance of analog FMCW radars are carefully analyzed. Envelop fluctuation induced AM distortion and chirp non-linearity induced FM distortion introduce significant performance degradation in an FMCW radar, causing the beat frequency f_{beat} to spread out over the spectrum and resulting in tone splitting after FFT. To avoid these limitations from the conventional analog type FMCW radar, two newly proposed digital modulated/coded CMOS radar is presented in this dissertation.

Second, a W-band 89-93 GHz multi-user interference-tolerant FHCW radar with 4-GHz bandwidth / 3.75-cm range resolution is demonstrated for automotive application. Frequency hopping technique with one-coincidence codes is used to achieve multiplexing in the code domain, which can effectively mitigate the radar interference in an multi-user environment. A prototype radar module with the 28-nm CMOS TX/RX chip, a Rogers patch antenna and FR4

substrate is developed for the OTA verification, whose results validate the orthogonality property of the chosen one-coincidence codes and demonstrate the multi-user support capability of the radar.

Finally, a 0.1-4.0 GHz broadband DS/SS based all-digital radar SoC is developed for ground-penetrating application. Radar ranging is accomplished in code domain rather than through a chirp or pulse, which allows a higher degree of flexibility and programmability. Without conventional up/down conversion, the SoC offers complete programmability over frequency and bandwidth, allowing it to be adopted to various sub-surface conditions. In-field GPR test with actual rover prototype validates the capability of the DS/SS radar. The 28-nm prototype radar SoC achieves a fine resolution of 3.75 cm and consumes 46.2 mW, which makes it suitable for low power applications such as planetary exploration in the future.

To sum up, comparing with conventional analog radar, digital modulated/coded radar is more robust to circuit impairments and chirp non-linearity. It's also more scaling-friendly with advanced CMOS technologies. In addition, flexibility and programmability obtained from a digital-intensive radar does benefit a lot for many practical applications.

For future work, a lot of research can be carried out to further improve the performance of these digital modulated/coded radars. For example, TX-RX leakage cancellation with calibration algorithm and hardware implementation, coherent GPR TRX design for receiver sensitivity improvement. Furthermore, a reconfigurable radar that combines the functions of analog FMCW radar and digital modulated/coded radar can be realized in a single CMOS chip.

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