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Novel Channel Materials for Field-Effect Devices:
Barium Stannate and Cadmium Arsenide

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Materials

by

Omor Faruk Shoron

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May 2021

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Barium Stannate and Cadmium Arsenide

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by

Omor Faruk Shoron

This thesis is dedicated to my family.

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1. **O. F. Shoron**, M. Goyal, D. A. Kealhofer, T. Schumann, and S. Stemmer, “Enhanced carrier control in Cd₃As₂ thin films”
2. **O. F. Shoron**, T. Schumann, M. Goyal, D. Kealhofer and S. Stemmer, “Transverse

negative magnetoresistance and robust surface states in Cd_3As_2 thin films”

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2. **O. F. Shoron**, D. Kealhofer, M. Goyal, T. Schumann, L. Galletti, S. Stemmer, "Electrostatic Gating and Transport Studies of Thin Films of the 3D Dirac Semimetal Cd_3As_2 ", **APS Spring Meeting**, 2018, Los Angeles, USA
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ABSTRACT

Novel Channel Materials for Field-Effect Devices: Barium Stannate and Cadmium Arsenide

Omor Faruk Shoron

Novel materials with unique electronic properties are required to meet the demands of next-generation electronic systems. This dissertation discusses the use of novel materials, such as the perovskite oxides barium titanate (BaTiO_3) and barium stannate (BaSnO_3), and the three-dimensional Dirac semimetal cadmium arsenide (Cd_3As_2), for field-effect devices with distinctive transistor characteristics.

Integration of ultrathin epitaxial ferroelectric thin films on semiconductor channels is of great interest for novel low power switching and memory applications. The first section of this dissertation covers $\text{BaTiO}_3/\text{SrTiO}_3$, a ferroelectric-semiconductor heterostructure. The electronic properties of this heterostructure confirm that the BaTiO_3 thin film is ferroelectric. An anti-clockwise hysteresis is observed in $\text{BaTiO}_3/\text{SrTiO}_3$ -based capacitors and the characteristics of field-effect transistors are also consistent with the ferroelectric nature of the BaTiO_3 thin films. Furthermore, the BaTiO_3 thin films are under biaxial compressive stress, which enhances the ferroelectricity and increases the Curie temperature. This section also discusses the epitaxial growth of a high mobility perovskite oxide, BaSnO_3 , and reports the highest mobility in BaSnO_3 thin film – $215 \text{ cm}^2/\text{Vs}$.

The second part of this dissertation covers Cd_3As_2 , a three-dimensional Dirac semimetal with topologically non-trivial electronic states. Quantum capacitance measurements exhibit zero-energy Landau level, confirming Dirac surface states on the Cd_3As_2 thin films. Due to topologically nontrivial energy states, Cd_3As_2 thin films display interesting

magnetotransport characteristics. Berry phase effects lead to a negative transverse magnetoresistance in Cd_3As_2 thin films. The effect of the Berry phase can be tuned by altering film thicknesses or shifting Fermi level. Moreover, Cd_3As_2 based field effect transistors have the potential to operate in the THz regime, owing to the high Fermi velocity. Additionally, theoretical analysis shows linearity in transistor performance. This study demonstrates the first field-effect transistor with a Cd_3As_2 channel. Cd_3As_2 devices exhibit extraordinarily high current densities (10 A/mm) and ultra-low contact resistance ($< 2 \times 10^{-9} \Omega\text{cm}^2$). Improvements in the fabrication process and transistor structure enhance the current modulation ($> 50\%$) and transconductances (120 mS/mm) of a Cd_3As_2 field-effect transistor. There is a potential for a $10\times$ improvement in transconductance by reducing trap densities. Preliminary results demonstrate the vast potential of Cd_3As_2 field-effect transistors for high-speed THz electronics.

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Chapter 1

Introduction

Modern electronic devices and systems face significant challenges that need to be addressed to enable next-generation electronic systems. For instance, slowed-down voltage scaling in recent years makes thermal management in microprocessors challenging [1-4]. Poor electrostatics in power transistors limits the breakdown voltage in power ICs [5]. Due to the density-of-states constraints of high-mobility semiconductors, it is difficult to bridge the THz gap with conventional semiconductors [6]. Neuromorphic and quantum computing need new materials and device structures to make these technologies feasible [7-14]. To address these challenges, we need to approach them from different directions. We need to investigate new materials with novel electronic properties, which can offer new functionalities in electronic devices and systems. Furthermore, we should study new device structures to overcome the limitation of current technologies and to meet the requirements of next-generation electronic systems.

The main goal of this thesis is to investigate few novel electronic materials with exceptional electronic properties, which can potentially address some of the challenges facing current electronic devices. The first part of this thesis will cover different perovskite oxides and related electronic transistors. It will discuss ferroelectric-semiconductor heterojunctions, which can enable all-oxide electronics, memory devices, and negative capacitance field-effect transistors.

Additionally, this thesis covers epitaxial growth and electrical characterization of high mobility perovskite oxide, BaSnO_3 . The second half of this thesis discusses the electronic properties and potential electronic applications of a novel material, Cd_3As_2 . Cd_3As_2 is a 3D topological Dirac semimetal with unique electronic properties. This chapter provides a brief introduction into these materials. Moreover, we discuss different experimental methods used in this thesis.

1.1 Perovskite Oxides

Perovskite oxides is a fascinating class of materials with the chemical composition ABO_3 , where A and B are cations and O is oxygen. The tilt or the relative displacement of the cations can be tuned by choosing appropriate A and B cations. The combination of different cations determines the details of the crystal and electronic structure and leads to a broad spectrum of unique electronic and material properties [15-21], such as ferromagnetism, superconductivity, strong electron correlation, Mott insulators, ferroelectricity, and large dielectric response [188]. Although perovskite oxides are widely used for different applications, their use in electronic devices is minimal. One of the major reasons behind this lack of perovskite oxide-based electronic devices is poor room temperature carrier mobility in most perovskite oxides. There are only very few perovskite oxides that are semiconductors and allow controlled doping [188]. This thesis will discuss two such perovskite oxide semiconductors – SrTiO_3 and BaSnO_3 . While SrTiO_3 has low room temperature mobility, its large density-of-states allows a wide range of doping concentrations. BaSnO_3 , however, is a high-mobility perovskite oxide. Its excellent conductivity could be interesting for all-oxide transparent and power electronics. This thesis will also examine BaTiO_3 , a ferroelectric perovskite oxide. Ferroelectric-semiconductor heterojunction is a central component of different novel electronic devices.

Chapter 2 & 3 will discuss these perovskite oxides and their heterostructures for different electronic applications.

1.1.1 SrTiO₃

SrTiO₃ is a perovskite oxide with a cubic unit cell. It has a lattice parameter of 3.905 Å [22]. It is a relatively wide bandgap semiconductor with an energy gap of 3.2 eV [23]. Unlike most of the common semiconductors, SrTiO₃ does not have valence band maxima at Γ point. The conduction band of SrTiO₃ is derived from Ti d-states, which leads to a heavy effective mass ($1.17 - 4.2 m_0$) [24,25]. Consequently, SrTiO₃ has a large density-of-states, which allow a wide range of controlled doping. There are several ways to dope SrTiO₃:

1. Substitute Sr with a trivalent rare-earth ion, such as La or Gd [26].
2. Substitute Ti with a pentavalent ion, such as Nb [27].
3. Introduce oxygen vacancies [28].
4. Electrostatic or remote doping by interfacing with a polar perovskite oxide to introduce a two-dimensional electron liquid in the SrTiO₃ layer. Examples of such polar-nonpolar heterostructures are LaAlO₃/SrTiO₃ [29], GdTlO₃/SrTiO₃ [30], SmTiO₃/SrTiO₃ [31], etc.

SrTiO₃ has a very low room temperature electron mobility ($\sim 10 \text{ cm}^2/\text{Vs}$) due to optical phonon scattering [27,32,33], though very high mobility can be achieved at low temperatures [34,35]. Besides, this material exhibits a strong dielectric response with a room temperature relative permittivity of 300 [36] at low electric field. The permittivity of SrTiO₃ is electric field

dependent. Additionally, extremely high permittivity ($\sim 10,000$) is achievable by alloying SrTiO_3 , which can be used as tunable RF circuit component [37].

1.1.2 BaTiO_3

BaTiO_3 is a perovskite oxide that exhibits ferroelectric behavior at room temperature. It has a bandgap of ~ 3.2 eV [38] with a Curie temperature around 120-130 °C [39]. Below the Curie temperature, BaTiO_3 stabilizes in a low-symmetry tetragonal phase. In this tetragonal unit cell, the Ti atom moves to an off-center position. This displacement is the origin of the ferroelectricity in BaTiO_3 . The displacement of the Ti atom is along the c-axis (the longest axis) of the unit cell. There are two equivalent displacement states of the Ti atom which minimize the free energy of the system. The polarization direction of BaTiO_3 depends on which state the Ti atom is occupying. The polarization direction can be altered by switching the state of the Ti atom. At the Curie temperature, BaTiO_3 goes through a phase transition and a high-symmetric cubic phase emerges. This cubic unit cell contains random Ti displacement [40], which creates a random local dipole moment, leading to ferroelectricity when the system transforms into a low-symmetry phase below the Curie temperature [41].

1.1.3 BaSnO_3

BaSnO_3 has gathered significant attention for its high room temperature mobility in recent years compared to other perovskite oxides. BaSnO_3 has a cubic crystal structure with a lattice parameter of 4.116 Å [42]. It is also a wide-bandgap semiconductor with a bandgap of about 3 eV [43,44].

The electronic bandstructure of BaSnO₃ was first studied in 1991 to investigate the lack of superconductivity in this material [45]. That study predicted that the conduction band of BaSnO₃ consists of Sn 5s-orbitals, which is also confirmed by recent theoretical calculations [46-48]. **Figure 1.1(b)** shows a calculated band structure of BaSnO₃. Because of delocalized s-orbital, the conduction band exhibits strong dispersion, which leads to a low effective mass ($m^* = 0.20 m_e$). This low effective mass is the origin of high room temperature electron mobility in BaSnO₃.

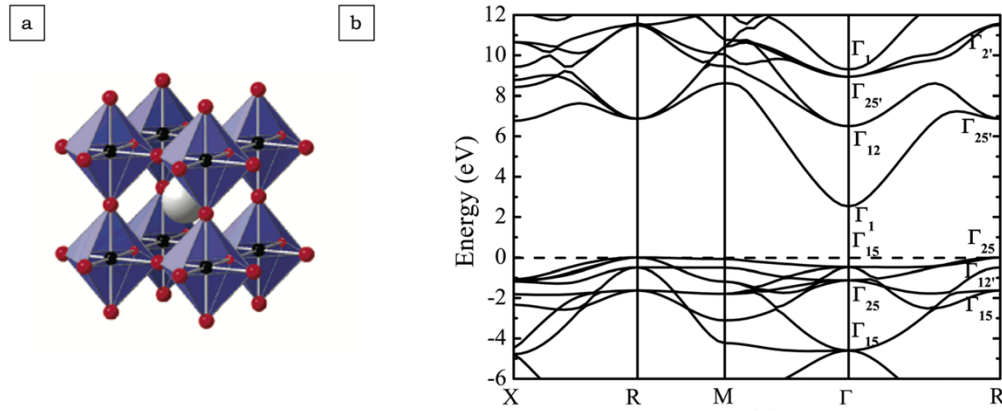


Figure 1.1: High mobility perovskite oxide BaSnO₃. (a) Unit cell of BaSnO₃. *Reprinted with permission from H. Mizoguchi et al. Inorg. Chem. 2004, 43, 5, 1667–1680. Copyright 2004 American Chemical Society [49].* (b) Electronic band structure of BaSnO₃. *Reprinted from H.-R. Liu et al. Appl. Phys. Lett. 102, 112109 (2013), with the permission of AIP Publishing.[46]*

Kim *et al.* reported BaSnO₃ single-crystal with room temperature mobility of $>300 \text{ cm}^2/\text{Vs}$ at La-doping densities around 10^{20} cm^{-3} , as shown in **Fig. 1.2** [50]. Among all semiconductors, BaSnO₃ exhibits the highest electron mobility at such high doping densities. Typically, electron mobility collapses at this doping level in most of the semiconductors. Most of the high

mobility semiconductors exhibit mobility below $100 \text{ cm}^2/\text{Vs}$ when doping density exceeds 10^{20} cm^{-3} [51].

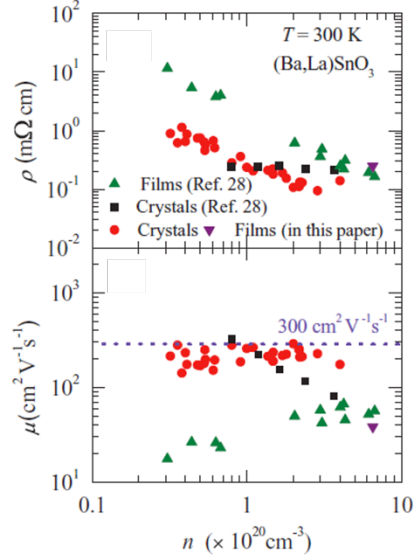


Figure 1.2: Transport properties of BaSnO₃. Resistivity (**top**) and electron mobility (**bottom**) of single-crystal BaSnO₃. Reprinted with permission from H. J. Kim *et al.* *Phys. Rev. B* 86, 165205, 2012. Copyright 2012 by the American Physical Society.[50]

N-type doping of BaSnO₃ is possible by either substituting Ba-site with La [52] or substituting Sn-site with Sb [53]. Only La-doping of BaSnO₃, however, has produced single-crystal material with high electron mobility. Kim *et al.* [50] showed that the electron mobilities in single-crystal BaSnO₃ are independent of the doping density, as shown in **Fig. 1.2**. This doping density-independent mobility in single-crystal BaSnO₃ hints that a different scattering mechanism, such as electron-phonon scattering, other than ionized impurity scattering is limiting the mobility in single-crystal BaSnO₃ [50].

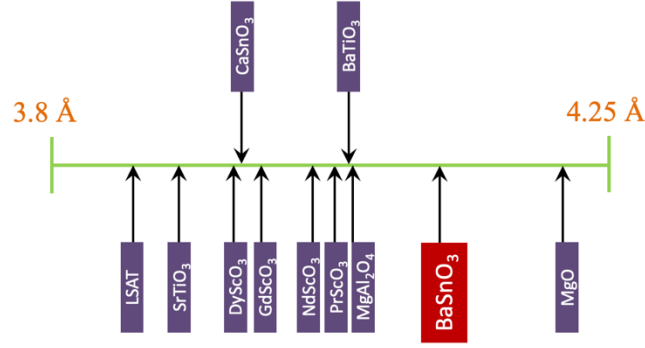


Figure 1.3: Lattice parameters of commercially available substrates. Lattice parameters of different commercially available substrates compared to BaSnO₃. There is no substrate available with lattice mismatch below 2%.

High-quality BaSnO₃ thin films are required to translate these excellent electronic properties into feasible electronic applications. BaSnO₃ thin films exhibit much lower electron mobilities. The main reason behind this poor transport properties in thin films is attributed, at least partially, to the lack of lattice-matched substrates. **Figure 1.3** shows the lattice parameters of various commercially available substrates compared to BaSnO₃. It is evident from the figure that there is no substrate available, which has a lattice mismatch with BaSnO₃ below 2%. As a result, BaSnO₃ thin films are grown with huge lattice mismatch. This huge lattice mismatch introduces a high density of dislocations at the film-substrate interface. Because of the scattering from these dislocations and associated grain boundaries, the electron mobilities in BaSnO₃ thin films follow $n^{1/2}$ dependence [51,54]. It should be noted that there is no report of mobility in lightly doped BaSnO₃ bulk single-crystal or thin film. Several factors, such as carrier compensation, non-stoichiometry, defects, dislocations, vacancies etc., could be behind the collapse in electron mobility at lightly doped BaSnO₃.

1.2 Mobility Limiting Mechanisms in Perovskite oxides

Several scattering mechanisms limit the mobility in a perovskite oxide. A brief introduction of these scattering mechanisms is discussed below.

1.2.1 Electron-Phonon Interactions

One of the leading mobility-limiting mechanisms in perovskite oxides is electron-phonon interaction. When charged carrier moves in a perovskite oxide, it interacts with the vibration of the lattice ions. Also, the Coulomb interactions between carriers and ions displaces the ions, further enhancing electron-phonon interactions. The electron-phonon scattering has a strong dependence on temperature since phonon distribution changes with temperature.

1.2.1.1 Acoustic Phonon Scattering

The acoustic phonon limited mobility can be written as [56] –

$$\mu_{ac} = \frac{2e\hbar\rho v_s^2}{3\pi n_{3D}m_e^*a_c^2} \ln(1 + e^{E_F/k_B T}) \dots \dots \dots (1.1)$$

where e is the charge of an electron, $\hbar$ is the reduced Planck constant, ρ is mass density, v_s is the sound velocity in the medium, n_{3D} is the 3D doping density, m_e^* is the effective mass of the electron, a_c is acoustic deformation potential, E_F is the Fermi energy, k_B is the Boltzmann constant, and T is the temperature.

1.2.1.2 Longitudinal Optical Phonon Scattering

LO phonon limited mobility for SrTiO₃ can be written as [26] –

$$\mu_{LO} = \frac{1}{2K_{ep}\omega} \frac{e}{m_p} \left(\frac{m_e^*}{m_p}\right)^2 f(K_{ep}) (e^{\hbar\omega/k_B T} - 1) \dots\dots\dots (1.2)$$

where ω is the phonon frequency, $f(K_{ep})$ is a dimensionless function and is ≈ 1 . m_p is the polaron quasiparticle mass and can be written as –

$$m_p = m_e^* \left(1 + \frac{K_{ep}}{6}\right) \dots\dots\dots (1.3)$$

and the dimensionless electron-phonon coupling constant, K_{ep} can be expressed as –

$$K_{ep} = \frac{e^2}{\hbar} \sqrt{\frac{m_e^*}{2\hbar\omega}} \left(\frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_0}\right) \dots\dots\dots (1.4)$$

where ϵ_∞ is the high-frequency dielectric constant, and ϵ_0 is the static dielectric constant. This formalism assumes that τ_{LO} is independent of the wave vector, k . This assumption works for semiconductors like SrTiO₃, which has large effective mass. Conversely, this formalism is not valid for a material like BaSnO₃ that has a small effective mass.

1.2.1.3 Transverse Optical Phonon Scattering

TO phonon limited mobility in a perovskite oxide can be calculated using the following analytical model [56] –

$$\mu_{TO} = \frac{\sqrt{2}\pi\hbar^3 \rho v_s^2 (e^{\hbar\omega_{TO}/k_B T} - 1)}{(m_e^*)^{5/2} \omega_{TO} d_0^2 \sqrt{E + \hbar\omega_{TO}}} \dots\dots\dots (1.5)$$

where ω_{TO} is the frequency of TO phonon mode, d_0 is optical phonon deformation potential, and E is the energy of the electron. Most of the evidence indicates that TO phonon scattering is not a dominating mechanism in SrTiO₃ and BaSnO₃.

1.2.2 Electron-Electron scattering

The quadratic dependence of resistivity on temperature is a signature of electron-electron scattering in a material. The mechanism of electron-electron scattering can be explained using Fermi liquid theory. Electron-electron scattering limited mobility of a material system can be approximated as –

$$\mu_{TO} \propto T^{-2} \dots\dots\dots (1.6)$$

Although electron-electron scattering is reported in two-dimensional electron liquid of SrTiO₃ [57,58], there is no similar report for BaSnO₃.

1.2.3 Ionized Impurity Scattering

Unlike electron-phonon, and electron-electron scatterings, ionized impurity scattering in a degenerately doped semiconductor is independent of temperature. The ionized impurity limited mobility in a degenerately doped semiconductor can be modeled as [59] –

$$\mu_{II} = \frac{3(\epsilon_r \epsilon_0)^2 h^3}{Z^2 m_e^* e^3} \frac{n}{N_i} \left[\ln(1 + \xi) - \frac{\xi}{1 + \xi} \right]^{-1} \dots\dots\dots (1.7)$$

where ϵ_r is the relative dielectric constant, Z is the effective charge of these impurities, N_i is the density of ionized impurity, and ξ can be written as –

$$\xi = (3\pi^2)^{1/3} \frac{\epsilon_r \epsilon_0 h^2 n^{1/3}}{m_e^* e^2} \dots\dots\dots (1.8)$$

Since ionized impurity scattering depends on the doping densities, electrostatic or modulation doping where carriers and ionized dopants are spatially separated should reduce ionized impurity scattering.

1.2.4 Neutral Impurity Scattering

Usually, neutral impurity scattering is very weak compared to ionized impurity scattering. Nevertheless, there are few cases when neutral impurity scattering could be significant in BaSnO₃. Neutral impurity scattering limited mobility can be written as –

$$\mu_{NI} = \frac{2\pi e}{10a_B h} \frac{1}{N_N} \dots\dots\dots (1.9)$$

where N_N is the density of neutral impurity and a_B can be written as –

$$a_B = \frac{\epsilon_r \epsilon_0 \hbar^2}{\pi m_e^* e^2} \dots \dots \dots (1.10)$$

1.2.5 Dislocation Scattering

As BaSnO₃ thin films are grown on a substrate with a huge lattice mismatch, there are significant dislocation densities in the BaSnO₃ films. Dislocation scattering limited mobility can be written as [60] –

$$\mu_{DIS} = \frac{8ea^2}{\pi \hbar N_{DIS}} \left(\frac{3n}{\pi} \right)^{2/3} (1 + \xi_0)^{3/2} \dots \dots \dots (1.11)$$

where a is the lattice parameter, N_{DIS} is the dislocation density, and ξ_0 can be written as –

$$\xi_0 = \frac{\epsilon_r \epsilon_0 \hbar^2}{m_e^* e^2} (3\pi^2 n)^{1/3} \dots \dots \dots (1.12)$$

1.3 Cd₃As₂

Cd₃As₂ is a three-dimensional (3D) topological Dirac semimetal. There are two Dirac nodes in the first Brillouin zone of Cd₃As₂. Along with time-reversal symmetry, Cd₃As₂ has a 4-fold rotational symmetry that prevents bandgap opening at the Dirac nodes' band crossings. The unit cell of Cd₃As₂ can be described as a superstructure of distorted antiferroite subcells. The Fermi velocity in a Cd₃As₂ Dirac node is $\sim 1.5 \times 10^6$ m/s [61]. The Fermi velocity of Cd₃As₂ is

much higher than that of any other topological semimetal. Furthermore, the electron mobility in single-crystal Cd_3As_2 could be as high as $9 \times 10^6 \text{ cm}^2/\text{Vs}$ at low temperatures [62]. Detailed structural and electronic properties of Cd_3As_2 are discussed in **Chapter 4**.

1.4 Magnetotransport

One of the best ways to probe the topological nature of the Cd_3As_2 sample is to conduct magnetotransport experiments. This measurement can reveal different electronic properties of the material. For example, quantum hall effect or Shubnikov-de Haas oscillations can reveal whether an energy state is 2D or 3D. Negative magnetoresistance can reveal the topological phase of the material [63]. In this study, we used magnetotransport studies to investigate the evolution of the electronic bandstructure of Cd_3As_2 .

1.4.1 Classical Hall Effect

When a magnetic field is applied perpendicular to the path of moving charged particles, due to the Lorentz force, an electric field is induced in the conductor, which is perpendicular to both the current direction and the applied magnetic field. This electric field results in a transverse voltage. This effect is called the Hall effect, named after E. H. Hall, who first discovered this effect [64]. Hall effect is used to study different electronic transport properties of a material, such as a carrier density, carrier mobility, etc. In a classical single-carrier system, the transverse voltage (also known as Hall voltage, V_H) can be written as –

$$V_H = -\frac{I B}{n e w} \dots \dots \dots (1.13)$$

where e is the charge of an electron, I is current, B is the applied magnetic field, n is the sheet carrier density, and w is the width of the conductor. In the classical regime, Hall resistance ($R_{xy} = \frac{V_H}{I}$) has a linear dependence on the magnetic field. Hall coefficient can be calculated from the slope of this linear dependence and can be written as –

$$R_H = -\frac{1}{n e} \dots\dots\dots (1.14)$$

This Hall coefficient is used to measure the carrier density and their mobilities. The sign of the Hall coefficient indicates the charge of the carriers (-ve for electrons and +ve for holes).

1.4.2 Magnetoresistance

The magnetoresistance resistance demonstrates how the conductivity of a material changes with the magnetic field, and thus, reveals different macroscopic classical and quantum mechanical properties of a material.

Cd₃As₂ thin films have two types of electronic states – bulk and surface states. Furthermore, the type of carriers in these two states could be different (electrons and holes) and could exhibit ambipolar transport. Therefore, a nonlinearity in Hall resistance is expected. Moreover, the magnetoresistance of Cd₃As₂ could exhibit a large non-saturating magnetoresistance [65-68]. The large non-saturating magnetoresistance can be explained using carrier compensation.

To understand the effect of carrier compensation, we need to understand the conductivity of a two-carrier system with n- and p-type carriers. The conductivity tensor elements of such a system can be written as –

$$\sigma_{xx} = \frac{|e|n_e\mu_e}{1 + \mu_e^2 B^2} + \frac{|e|n_h\mu_h}{1 + \mu_h^2 B^2} \dots\dots\dots (1.15)$$

$$\sigma_{xy} = \frac{e_e n_e \mu_e^2 B}{1 + \mu_e^2 B^2} + \frac{e_h n_h \mu_h^2 B}{1 + \mu_h^2 B^2} \dots\dots\dots (1.16)$$

where e_e (e_h) is the charge of an electron (hole), n_e (n_h) is the density of electrons (holes), and μ_e (μ_h) is the mobility of the electrons (holes). The resistivity tensor component of this two-carrier system can be derived by inverting the conductivity tensor –

$$\rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx} + \sigma_{xy}} = \frac{(n_e\mu_e + n_h\mu_h) + (n_e\mu_e\mu_h^2 + n_h\mu_h\mu_e^2)B^2}{(n_e\mu_e + n_h\mu_h)^2 + \mu_h^2\mu_e^2(n_h - n_e)^2 B^2} \cdot \frac{1}{e} \dots\dots\dots (1.17)$$

$$\rho_{xy} = \frac{\sigma_{xy}}{\sigma_{xx} + \sigma_{xy}} = \frac{(n_h\mu_h^2 - n_e\mu_e^2) + \mu_h^2\mu_e^2(n_h - n_e)^2 B^2}{(n_e\mu_e + n_h\mu_h)^2 + \mu_h^2\mu_e^2(n_h - n_e)^2 B^2} \cdot \frac{B}{e} \dots\dots\dots (1.18)$$

From **Eqn. 1.17** it is clear that when $n_h = n_e$, ρ_{xx} does not saturate and exhibits a B^2 dependence [65-67].

1.4.3 Landau Quantization

Landau levels are the quantized eigen states of a charged carrier under an applied strong magnetic field. Due to the quantum mechanical nature of the carriers, only certain discrete

cyclotron orbits are allowed for the carriers under a magnetic field. As a result, a carrier can only occupy an orbit with a quantized energy value, known as the Landau level.

The Landau energy level of a system depends on the energy dispersion and topological nature of the system. For a 2D parabolic band, the allowed Landau energy levels can be written as –

$$\varepsilon_n = \left(n + \frac{1}{2}\right) \hbar \omega_c \dots \dots \dots (1.19)$$

where n is the index of the Landau level. In a parabolic band, Landau levels are equidistant.

The Landau energy level of a 2D Dirac band can be written as –

$$\varepsilon_n = v_F \text{sgn}(n) \sqrt{2e\hbar|B||n|} \dots \dots \dots (1.20)$$

where v_F is the Fermi velocity. Unlike a parabolic band, Landau levels in a 2D Dirac band are not equally spaced. Furthermore, in a 2D Dirac state, zero-energy Landau level is accessible.

For a 3D Dirac semimetal, the allowed Landau levels are –

$$\varepsilon_n = v_F \text{sgn}(n) \sqrt{2e\hbar|B||n| + (\hbar k_z)^2} \dots \dots \dots (1.21)$$

where k_z is the crystal momentum along z -direction. 3D Dirac state exhibits magnetic field independent zeroth Landau level.

1.4.4 Shubnikov-de Haas Oscillations

Shubnikov-de Haas (SdH) oscillations are an example of the quantum mechanical nature of the carriers. As explained in previous section, the magnetic field forms Landau levels, and when the magnetic field is varied, Fermi level crosses the Landau levels. When the Fermi level crosses the Landau levels, it results in an oscillation in conductivity. This oscillation in conductivity is known as SdH oscillation.

As SdH oscillations are quantum mechanical phenomena, quantum coherence must be maintained to observe the oscillations. Therefore, thermal broadening should be smaller than the spacing between the Landau levels. Additionally, scattering time (τ) should satisfy the condition $\omega_c \tau > 1$, where ω_c is the cyclotron frequency. As a result, SdH oscillations can only be observed at a very low temperature (low thermal broadening) and high magnetic field (large ω_c). SdH oscillation is used to calculate the sheet carrier densities of a system. The frequency of the SdH oscillations depends on the external cross-sectional area (A_{cross}) of the Fermi surface, and this area depends on the carrier densities. The frequency of the SdH oscillations can be expressed as follows -

$$F = \frac{\hbar A_{cross}}{2\pi e} \dots\dots\dots (1.22)$$

This frequency of the SdH oscillations can be calculated by plotting the conductivity as a function of $1/B$. If there are multiple types of carriers, Fourier transformation is used to differentiate between them. For a 2D state, the sheet carrier density can be calculated from the oscillation frequency using the following relation –

$$n_{2D} = \frac{e}{h} F \dots \dots \dots (1.23)$$

1.5 Experimental Methods

1.5.1 Hall and Magnetotransport Measurements

We have used two different geometries to measure magnetotransport – Van der Pauw and Hall bar geometries. Here, we discuss how these devices are used to probe different transport properties of a material.

For a Van der Pauw geometry, 4 contacts are deposited at four corners of a square sample, as shown in **Fig. 1.4**. Two different resistances (R_v and R_h) are measured to calculate the sheet resistance. The electrical connections of these measurements are shown in **Fig. 1.4(b,c)**. R_v and R_h can be calculated using the following relations –

$$R_v = R_{13,24} = \frac{V_{24}}{I_{13}} \dots \dots \dots (1.24)$$

$$R_h = R_{34,12} = \frac{V_{12}}{I_{34}} \dots \dots \dots (1.25)$$

Now, the sheet resistance, R_S can be calculated using the following relation [69] –

$$e^{-\frac{\pi R_h}{R_S}} + e^{-\frac{\pi R_v}{R_S}} = 1 \dots \dots \dots (1.26)$$

For an isotropic material, **Eqn. 1.32** can be simplified to –

$$R_S = \frac{\pi R_h}{\ln 2} = \frac{\pi R_v}{\ln 2} \dots \dots \dots (1.27)$$

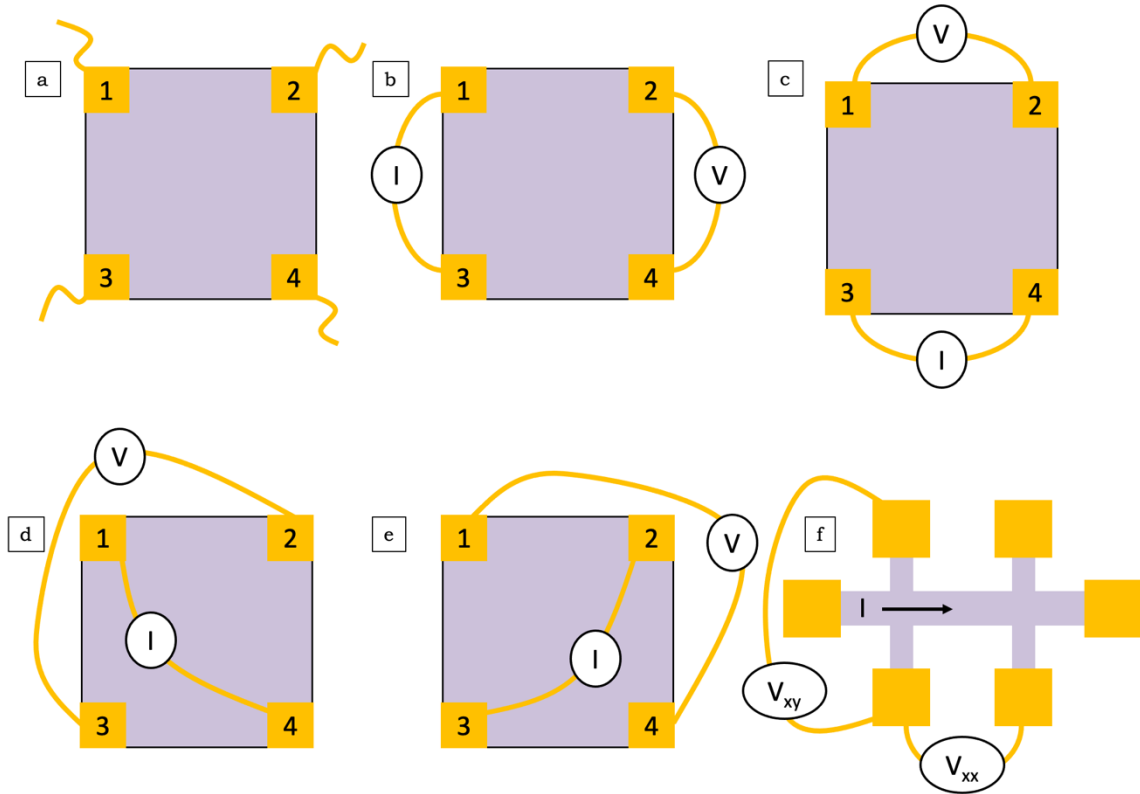


Figure 1.4: Hall and magnetotransport measurements. (a) Van-der Pauw geometry. Connection for **(b)** R_v and **(c)** R_h measurements. **(d-e)** Connection for Hall resistance measurements. **(f)** Hall bar geometry.

Hall resistances can be measured using the connection shown in **Fig. 1.4(d,e)** and the following relations –

$$R_{H,1} = R_{14,23} = \frac{V_{23}}{I_{14}} \dots\dots\dots (1.28)$$

$$R_{H,2} = R_{32,14} = \frac{V_{14}}{I_{32}} \dots\dots\dots (1.29)$$

So, the Hall resistance, R_{xy} of the system is –

$$R_{xy} = \frac{R_{H,1} + R_{H,2}}{2} \dots\dots\dots (1.30)$$

For an isotopic single-carrier system, $R_{xy} = R_{H,1} = R_{H,2}$. R_{xy} is calculated for different magnetic fields, and the sheet carrier density, n , is calculated from the slope (R_H) of the R_{xy} vs. B curve and using **Eqn. 1.14**. The mobility is calculated using the following relation –

$$\mu = \frac{1}{n e R_s} \dots\dots\dots (1.31)$$

Figure 1.4(f) shows the schematic diagram of a Hall bar structure. R_{xx} and R_{xy} of the geometry can be measured using the following relations -

$$R_{xx} = \frac{V_{xx}}{I} \dots\dots\dots (1.32)$$

$$R_{xy} = \frac{V_{xy}}{I} \dots \dots \dots (1.33)$$

Now, R_S can be calculated using **Eqn. 1.13**. Sheet carrier density and carrier mobility can be calculated following the same procedure described above. All the magnetotransport measurements reported in this thesis were carried out using a Quantum Design Dynacool Physical Properties Measurement System. Matlab and Python codes to extract data from Dynacool measurements are attached in **Appendix**.

1.5.2 Transmission Line Measurements

Transmission line measurements (TLM) are used to measure the contact resistances and the sheet resistances of a sample. TLM structure consist of series of rectangular ohmic contacts where the distances between two adjacent contact pads are gradually increased, as shown in **Fig 1.5(a)**. Also, the structure is isolated by etching to control the width of the current path.

The total resistance between two adjacent contacts, R_T can be written as –

$$R_T = \frac{2R_C}{w} + R_S \frac{l}{w} \dots \dots \dots (1.34)$$

where R_C is the contact resistance, R_S is the sheet resistance, l is the distance between two consecutive contacts, and w is the width of the structure. After measuring R_T for different spacings, they are plotted as a function of l , as shown in **Fig. 15(b)**. 4-probe measurements are

used to exclude the probe resistance. The sheet resistances and contact resistances can be calculated from this plot. The slope of the plot gives the sheet resistance –

$$R_S = \text{Slope} \times w \dots \dots \dots (1.35)$$

The contact resistance, R_c , can be calculated from y-interception –

$$R_c = \frac{y - \text{intercept} \times w}{2} \dots \dots \dots (1.36)$$

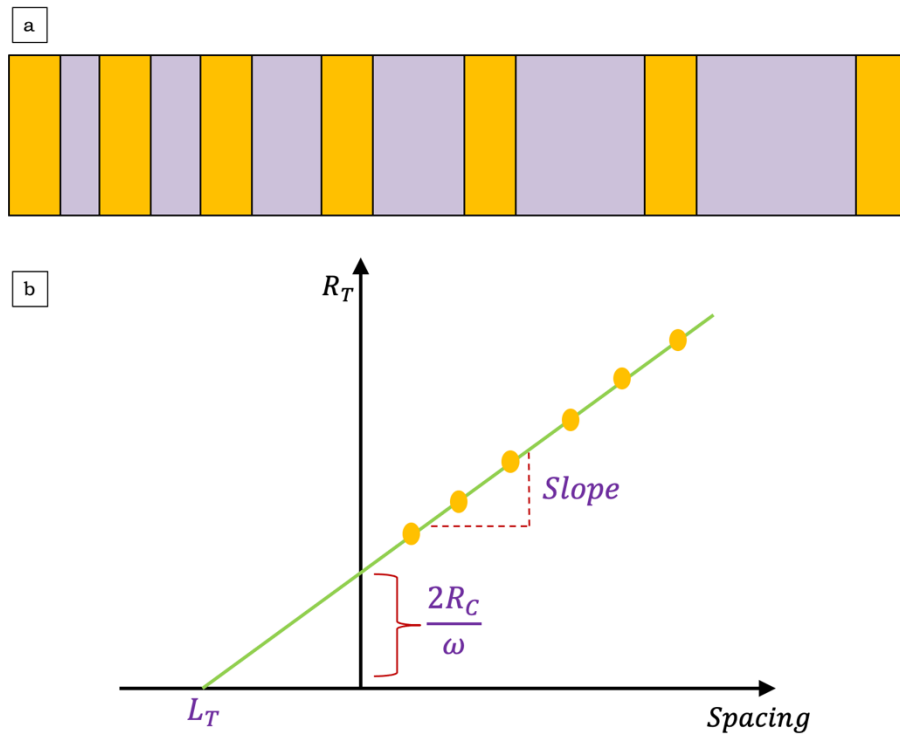


Figure 1.5: Transmission line measurement. (a) TLM structures. **(b)** Calculation of sheet and contact resistances from TLM data.

The specific contact resistance, $R_{c,sp}$ can be calculated from x-intercept, $L_T -$

$$R_{c,sp} = R_S L_T^2 \dots \dots \dots (1.37)$$

1.5.3 Capacitance-Voltage Measurement

A small AC voltage is superimposed on a DC voltage to measure the capacitance-voltage ($C-V$) characteristics. This combined voltage is applied at a high current terminal (H_{cur}). The low current terminal (L_{cur}) measures the current that passes through the testing device. The function of the low (L_{pot}) and the high potential (H_{pot}) terminals is to detect the voltage drop across the device. This measurement gives both amplitudes and phases of the voltage and current signals, which are used to measure the capacitance and resistance (or conductance) of the system.

Figure 1.6 shows a schematic diagram of a $C-V$ measurement system.

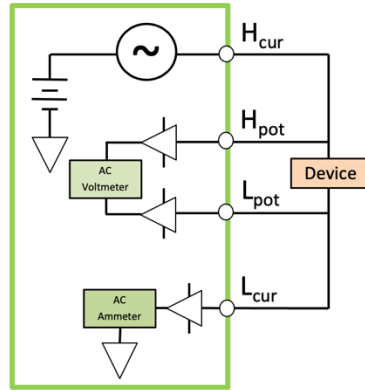


Figure 1.6: Capacitance-voltage measurements. Circuit diagram of an impedance analyzer used to measure $C-V$ characteristics.

There are two different C - V measurement models. The most common one is the parallel model where the parallel capacitance (C_P) and the parallel conductance (G_P) are measured. The other one is the series model, which measures the series resistance (R_S) and the series capacitance (C_S). All the C - V characteristics reported in this thesis were measured using the parallel model. The quality factor, the ratio between imaginary and real part of the impedance, for a parallel model is calculated using the following relation -

$$\text{Quality Factor, } Q = \frac{2\pi f C_P}{G_P} \dots\dots\dots (1.38)$$

where f is the frequency of the applied AC voltage.

1.6 Thesis Organization

Chapter 2 discusses the electrical characterization of BaTiO₃/SrTiO₃ heterojunction. Additionally, it demonstrates different two- and three-terminal devices based on BaTiO₃/SrTiO₃ heterostructures.

Chapter 3 details the growth of BaSnO₃ by molecular beam epitaxy. This chapter examines different growth conditions to optimize electrical and structural quality of BaSnO₃ thin films.

Chapter 4 gives a detail description of electrical and structural properties of Cd₃As₂ single-crystal and thin films.

Chapter 5 explains electronic band structure and magnetotransport characteristics of Cd₃As₂ thin films.

Chapter 6 demonstrates the first Cd₃As₂ channel field-effect transistors. Moreover, it will explore different performance-limiting factors of Cd₃As₂ channel field-effect transistors.

Chapter 7 details different modifications in fabrication process and device structures to improve transistor performance of Cd₃As₂ channel field-effect transistors.

Chapter 8 will give a summary of this work. Furthermore, it discusses future research directions based on the results shown here.

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Chapter 2

Ferroelectric-Semiconductor Heterostructures for Novel Field-Effect Transistors

Novel electronic devices are needed to meet the requirements of next-generation electronic systems. For example, modification in field-effect transistors (FETs) is warranted to allow aggressive voltage scaling necessary to keep up with “*Moore’s Law*.” Likewise, new two- and three-terminal devices are necessary to make neuromorphic architecture feasible to complement existing slower von Neumann architecture. One of the significant components of most of these new device structures is ferroelectric-semiconductor heterojunction. Epitaxial growth of single-crystal ferroelectric-semiconductor heterojunction is always challenging. This chapter describes how a single-crystal epitaxial ferroelectric layer can be integrated into a semiconducting channel using molecular beam epitaxy. The first section of this chapter discusses several applications of ferroelectric-semiconductor heterojunctions and explains why single crystal epitaxial structures are necessary for those applications. The second part details different types of all-perovskite oxides ferroelectric-semiconductor systems, such as $\text{SmTiO}_3/\text{BaTiO}_3/\text{SrTiO}_3$ and $\text{BaTiO}_3/\text{SrTiO}_3$ heterojunctions. And, finally, the last section covers electronic properties of $\text{BaTiO}_3/\text{SrTiO}_3$ heterojunctions. Furthermore, this section explains the electrical characteristics of parallel plate capacitors and field-effect transistors fabricated on $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructure.

Most of the results presented in this chapter have been published in OF Shoron et al. [86] and S Raghavan et al. [80].

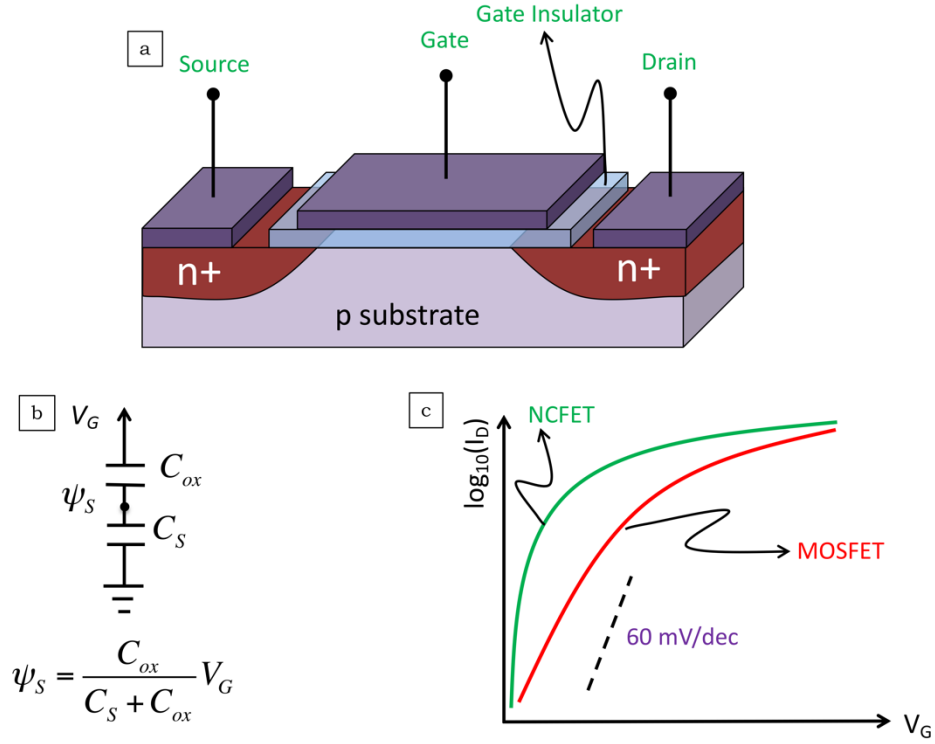


Figure 2.1: Subthreshold swing of a field-effect transistor. (a) Schematic diagram of an n-channel planar MOSFET. (b) Gate capacitances of a field-effect transistor. There are two components in gate capacitances – gate oxide capacitances (C_{ox}) and channel capacitances (C_s), which are in series. The equation shows the voltage drops across these capacitors. (c) I_D - V_G characteristics of a typical MOSFET (Red) and an NCFET (Green) in logarithmic scale. The theoretical lower limit of the subthreshold swing of a MOSFET is 60 mV/dec. That means the slope of the I_D - V_G curve of a MOSFET cannot be steeper than 60 mV/dec (black dashed line). Due to ferroelectric negative capacitance-induced voltage amplification at the gate, NCFETs can overcome this limit and can exhibit a much steeper slope in I_D - V_G characteristics.

2.1 Electronic Applications of Ferroelectric–Semiconductor Heterojunction

There is a renewed interest in ferroelectric–semiconductor heterojunctions for their unique electronic properties. Electrostatically switchable polarization charges of ferroelectric thin films make these heterostructures suitable for low power electronic devices, such as negative capacitance FETs [70], and memory devices, such as ferroelectric gated synaptic FETs [71] and ferroelectric tunnel junction [72]. The following section will provide a brief overview of these ferroelectric–semiconductor heterojunction-based electronic devices.

2.1.1 Negative Capacitance Field-Effect Transistors (NCFETs)

Metal oxide semiconductor field-effect transistor (MOSFET) (**Fig. 2.1(a)**) is the basic building block of modern electronic systems. The scaling of MOSFETs has primarily been propelling rapid technological advancements of the last few decades. The scaling of MOSFETs has enabled the drastic improvement of speed and functionality of the microchips. This scaling, however, has been slowed down in recent years. One of the significant challenges to continue this scaling to keep up with “Moore’s Law” is thermal management [1-4]. The supply voltage needs to be scaled accordingly to lower the chip's power density and heating. Moreover, voltage scaling is necessary to improve the reliability of the ultra-scaled MOSFETs. The scaling of the supply voltage is limited by the subthreshold swing (SS) of the transistor. SS defines how much change in supply gate voltage is needed to change the current in the channel by one order. SS of a conventional MOSFET can be written as –

$$SS = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \frac{\partial V_G}{\partial \psi_s} \frac{\partial \psi_s}{\partial(\log_{10} I_D)} \dots \dots \dots (2.1)$$

where V_G is the gate voltage, I_D is the channel current, and ψ_s is the surface potential of the MOSFET channel.

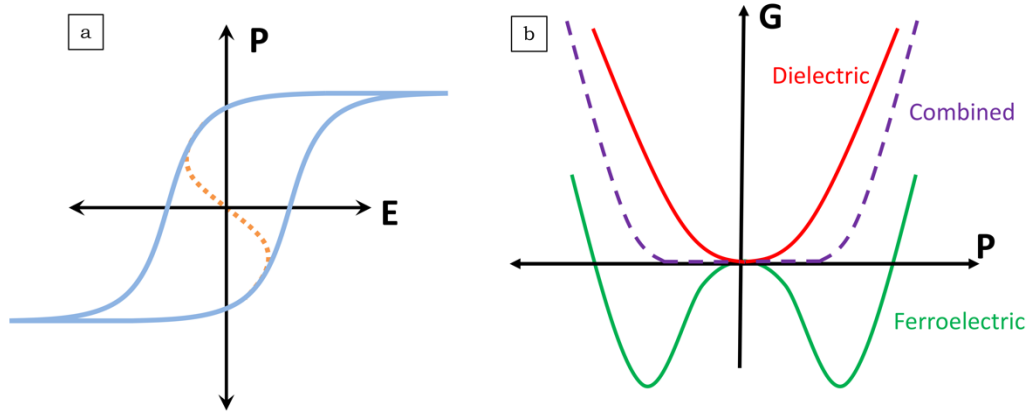


Figure 2.2: Stabilization of negative differential capacitance in a ferroelectric layer. (a)

Polarization vs. electric field (P-E) curve of typical ferroelectric material. The hysteresis in the P-E curve is due to the polarization switch in the ferroelectric materials. A hysteresis free polarization switch is possible (orange dashed line), but the path is thermodynamically unstable. **(b)** Gibbs free energy of a dielectric (red) and a ferroelectric (green) material as a function of polarization charge. In a standalone ferroelectric material, only two ferroelectric charge states are stable – the two minima in the Gibbs free energy. By combining a ferroelectric with a dielectric, the polarization charge between two charge minima can be made accessible while keeping the combined system's Gibbs free energy at its minima (purple dashed line). Thus, the orange dashed line of the P-E curve can be accessed, keeping the overall system thermodynamically stable.

The Boltzmann transport mechanism and Fermi-Dirac statistics set the lower limit for

$\frac{\partial \psi_s}{\partial (\log_{10} I_D)}$, 60 mV/dec at room temperature. ψ_s of a MOSFET can be written as –

$$\psi_s = \frac{C_{ox}}{C_s + C_{ox}} V_G \dots \dots \dots (2.2)$$

where C_{ox} is the capacitance due to the gate insulator and C_s is the capacitance of the channel.

Figure 2.1(b) shows how the gate voltage is divided between these two capacitors. From **Eqn.**

2.2, it is evident that the minimum value of $\frac{\partial V_G}{\partial \psi_s}$ for a conventional MOSFET cannot be below

1. Consequently, the theoretical lower limit of SS for a traditional MOSFET is 60 mV/dec at room temperature. This fundamental limit of SS makes the scaling of the supply voltage of a MOSFET challenging. Moreover, a larger SS means a higher off-current, which increases the passive power dissipation and heating of the chip. One solution to this problem is negative capacitance FET (NCFET), which requires a modification of conventional MOSFET [70]. In NCFET, a ferroelectric layer is used as a gate insulator. Consider the polarization-electric field (P - E) curve of a typical ferroelectric (**Fig. 2.2(a)**) and a path with a negative slope (orange dashed line). This negative slope path is not accessible in a standalone ferroelectric capacitor because this path is thermodynamically unstable. **Figure 2.2(b)** shows the Gibbs free energy of a ferroelectric and a dielectric material. The negative slope region of **Fig. 2.1(a)** corresponds to the free energy region of a ferroelectric between two minima that is not thermodynamically accessible. Even though this negative slope region is not accessible in an isolated ferroelectric layer, combining it with a suitable dielectric layer makes it possible to access this negative slope region, keeping the overall system thermodynamically stable [70,73], as shown in **Fig.**

2.2(b). A negative differential capacitance across a ferroelectric layer can be achieved by stabilizing this negative slope path. According to **Eqn. 2.2**, a negative gate capacitance allows $\frac{\partial V_G}{\partial \psi_s}$ to be below 1. Therefore, SS below 60 mV/dec can be achieved in an NCFET without changing the transport mechanism. Here, the ferroelectric gate is acting as a voltage amplifier. Although ψ_s and I_D still obey the limit imposed by the Boltzmann transport mechanism, voltage amplification at the gate permits a larger change in ψ_s with a smaller change in V_G . This mechanism effectively lowers the SS of an NCFET, as shown in **Fig. 2.1(c)**.

One of the fundamental challenges of NCFETs is the proper integration of the ferroelectric layer on a semiconducting channel. NCFETs need to be hysteresis-free, and the gain of the device should be uniform [74]. The ferroelectric layer needs to be a single crystal to fulfill these requirements. It is challenging to integrate an epitaxial ferroelectric layer on a semiconducting channel. There are several reports of epitaxial layers of ferroelectrics on semiconductors. Nonetheless, typically, those required an additional buffer layer to stabilize ferroelectricity [74-77]. Moreover, detailed analysis of NCFETs shows that the semiconducting channel's carrier density must match the ferroelectric layer's polarization [73,78,79]. This carrier matching is difficult to achieve using traditional semiconductors, as the relatively low density of states of conventional semiconductors prevents them from accommodating a large amount of free charge to balance polarization charge. This mismatch leads to depolarization of the ferroelectric layer grown directly on the semiconductors. To make NCFETs a viable technology, this issue of integrating the epitaxial ferroelectric layer on the semiconducting channel needs to be resolved.

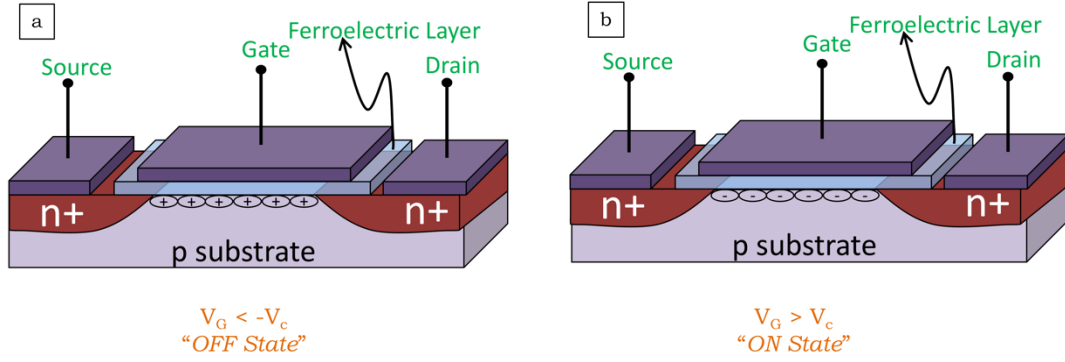


Figure 2.3: Operation principle of ferroelectric field-effect transistor. (a) “OFF state” of a Ferroelectric FET (FeFET). When the gate voltage is sufficiently negative, the polarization of the ferroelectric layer is along the out-of-plane. The polarization charge depletes the channel and induces an “OFF state” in the device. (b) “ON state” of the FeFET. When the gate voltage is sufficiently positive, the polarization of the ferroelectric layer is reversed. This reversal in polarization causes the accumulation of free carriers in the channel and induces an “ON state” in the device.

2.1.2. Ferroelectric Field Effect Transistor (FeFET)

FeFET is essentially a MOSFET with a ferroelectric gate insulator. The FeFET can be used for ferroelectric random-access memory (FRAM). The resistivity of the channel of the FeFET can be altered by switching the polarization of the ferroelectric layer, as shown in **Fig. 2.3**. When the gate voltage, V_G , is larger than a positive critical voltage, V_c , the polarization, P , is directed toward the channel. This polarization direction accumulates electrons at the channel and lowers the resistance between source and drain. This state is called “ON state” or “1”. On the other hand, if V_G is smaller than $-V_c$, P is directed toward the opposite direction. This reversal of polarization direction depletes the electrons of the channel and increases the channel resistance. This state is called “OFF state” or “0”. No additional capacitors are needed to design a RAM

using FeFET. Therefore, FeFET can offer compact cell design, non-volatile memory, and non-destructive readout.

To improve the retention time of a FeFET, charge traps at the channel–ferroelectric interface need to be reduced [7-9]. This can be achieved by lowering lattice mismatch between the channel and ferroelectric layer, reducing the dangling bonds at the interface, avoiding the formation of the low- k dielectric at the interface, and making the ferroelectric layer pinhole-free [7]. All of these requirements can be achieved by choosing an appropriate channel and ferroelectric materials and growing an epitaxial heterojunction.

2.1.3 Ferroresistive Devices

Ferroelectric-based, two-terminal devices can be used for memory applications, as shown in **Fig. 2.4(a)**. These devices are called ferroresistive devices. The coexistence of band conductance and ferroelectricity can make it possible to alter the resistance between two terminals by switching the polarization direction [7]. This device shows two resistive states (“*ON*” and “*OFF*”) logically represented by “*1*” and “*0*”. Ferroresistive devices offer non-destructive readout. Moreover, the gigabit range is possible because these devices require relatively low remnant polarization [7]. Another alternative approach of ferroresistive device is ferroelectric tunnel junctions (FTJs). Carrier can be tunneled through a very thin ferroelectric layer. The tunneling current depends on the polarization state of the ferroelectric layer [7] that gives rise to two distinct resistive states (“*0*” and “*1*”), as shown in **Fig. 2.4(b,c)**. These types of ferroresistive devices can be an alternative to FeRAM. Parasitic effects such as local

conductivity and electrochemical variations have to be reduced to take full advantage of these types of devices, which can be ensured by epitaxial ferroelectric-semiconductor heterojunctions [7,10,11].

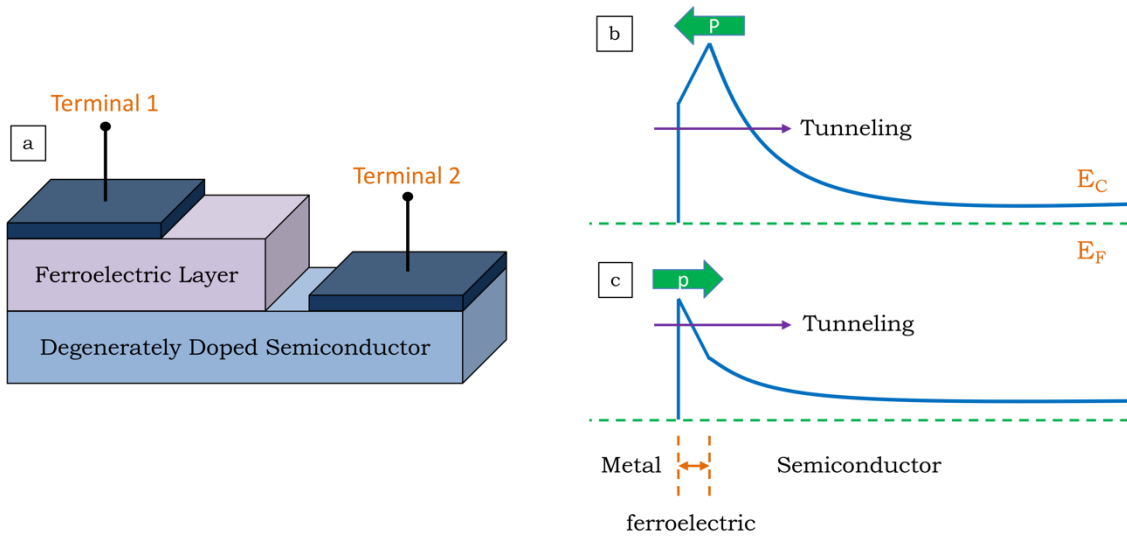


Figure 2.4: Ferroresistive devices. (a) Schematic diagram of a two-terminal ferroresistive device.

The resistivity between the two terminals of the device depends on the polarization direction of the ferroelectric layer. **(b) & (c)** Schematic band diagram of a ferroelectric tunnel junction. The width of the tunneling barrier changes depending on the polarization direction (green arrow). When the polarization is along the out-of-plane, the depletion layer widens and lowers the tunneling current. When the polarization points toward the semiconductor, the tunneling current increases due to the thin depletion layer.

2.2 Ferroelectric–Semiconductor Heterostructures

As discussed in the previous section, an excellent interface between the ferroelectric layer and the semiconductor channel is essential for different electronic applications. The ferroelectric layer should be single-crystal, and the interface must be trap-free. Moreover, there should be a

charge matching between ferroelectric polarization and the semiconductor channel's free carriers. Considering all these requirements, epitaxial BaTiO₃/SrTiO₃ heterostructures emerge as a potential candidate for different electronic applications discussed earlier. The ferroelectric polarization of BaTiO₃ is 0.15 C/m² that corresponds to a sheet carrier density of $\sim 10^{14}$ cm⁻² [20]. The high density-of-states due to the large effective mass of electrons in SrTiO₃ makes such carrier densities achievable in a SrTiO₃ channel. SrTiO₃ can be doped over a vast range with La or Sm. Moreover, both SrTiO₃ and BaTiO₃ are perovskite oxides, making epitaxial growth easier and providing an excellent interface quality. The following sections discuss the electronic properties of BaTiO₃/SrTiO₃ heterostructures. Moreover, these sections detail the electrical characteristics of different two- and three-terminal devices based on these heterostructures.

2.2.1 Critical Thickness of Ferroelectric BaTiO₃

Polar discontinuity can introduce a large two-dimensional electron gas (2DEG) at the interface of a polar (i.e., SmTiO₃, GdTiO₃, etc.) and a nonpolar (i.e., SrTiO₃) perovskite oxides [30]. The electronic transport properties of these 2DEGs can be altered by introducing a ferroelectric layer at the interface. Conversely, the transport characteristics of these 2DEGs can reveal the nature of the ferroelectric layer. To study that, our group member Santosh Raghavan grew SmTiO₃/BaTiO₃/SrTiO₃ heterostructures using molecular beam epitaxy (MBE) [80]. The thicknesses of the BaTiO₃ layer were varied from 1 BaO layer ($\frac{1}{2}$ u.c.) to 14 BaO layers (13 u.c.). The schematic diagram of the heterostructure is shown in **Fig. 2.5(a)**. Santosh Raghavan has observed a ferroelectricity-induced metal-to-insulator transition in these heterostructures. As shown in **Fig. 2.5(b)**, all the samples show similar sheet carrier density - around 3×10^{14} cm⁻². This sheet carrier density is around $\frac{1}{2}$ electron per unit cell at the interface, consistent

with the 2DEG introduced by polar discontinuity. **Figure 2.5(c)** shows the sheet resistance of the samples as a function of temperature. When the BaTiO₃ layers contain up to 4 BaO layers, the slopes of the sheet resistance curves are non-negative ($\frac{\partial R_s}{\partial T} > 0$), indicating the metallic behavior of the 2DEGs. Nonetheless, above this critical thickness, the sheet resistance curves display negative slopes ($\frac{\partial R_s}{\partial T} < 0$) below 125 K. These negative slopes reveal an insulating behavior of the channel.

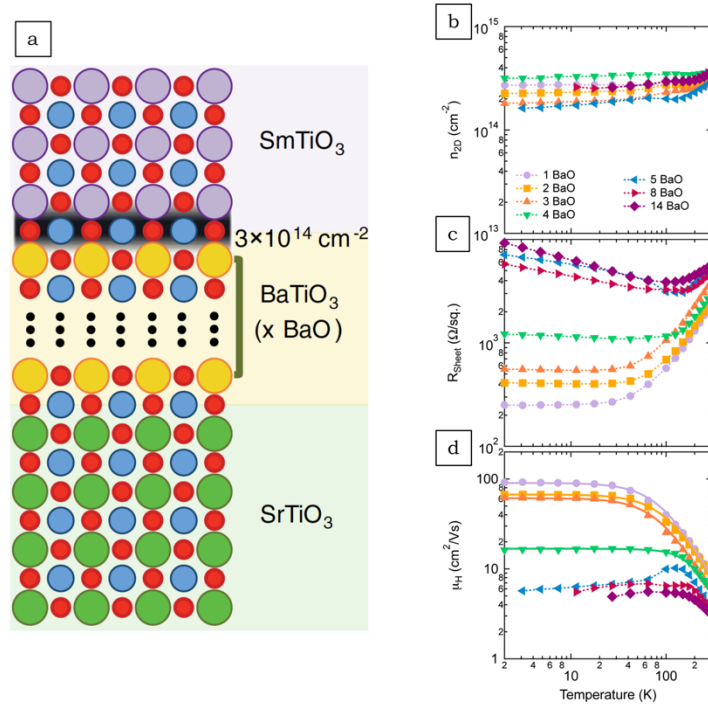


Figure 2.5: Electronic transport properties of SmTiO₃/BaTiO₃/SrTiO₃ heterostructures. (a)

A schematic diagram of a SmTiO₃/BaTiO₃/SrTiO₃ heterostructure. The thickness of the BaTiO₃ layer is varied from 1 BaO layer ($\frac{1}{2}$ u.c.) to 14 BaO layers (13 u.c.). **(b)** Sheet carrier densities, **(c)** Sheet resistances, and **(d)** Hall mobilities of the 2DEGs in SmTiO₃/BaTiO₃/SrTiO₃ heterostructures. The transport properties show a ferroelectricity-induced metal-to-insulator transition in the 2DEGs of the heterostructures. *Reprinted from [80] with permission from American Physical Society, Copyright 2016.*

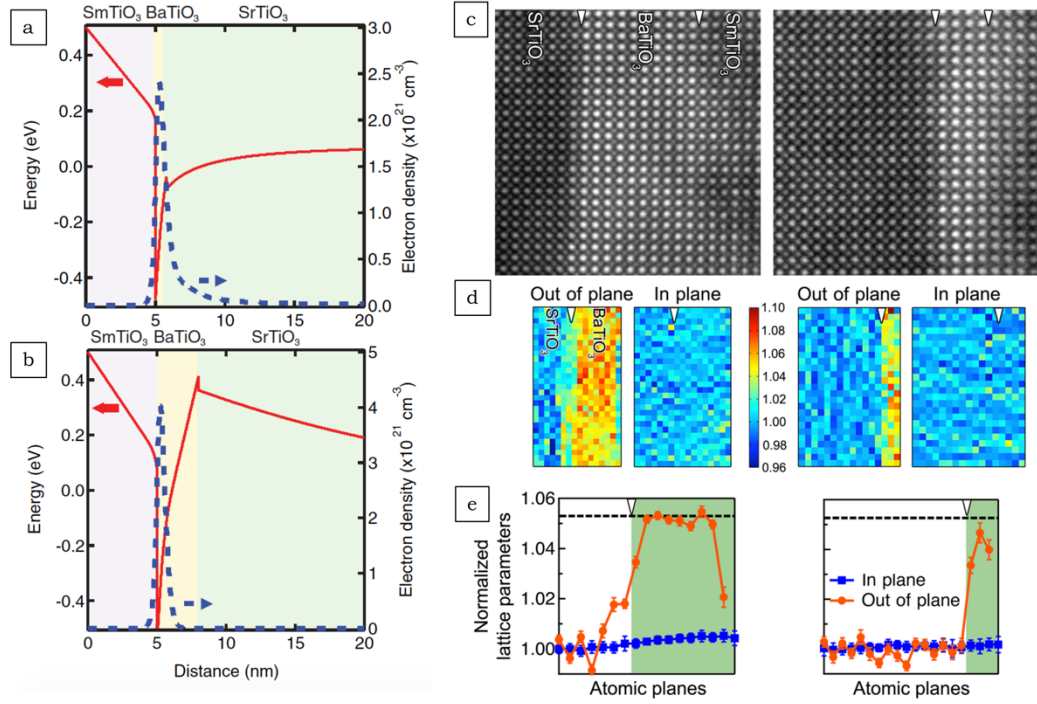


Figure 2.6: Suppression of ferroelectricity in thin BaTiO₃ films. The calculated band diagram and 2DEG distribution of SmTiO₃/BaTiO₃/SrTiO₃ heterostructures with **(a)** 2 u.c. (3 BaO layer) and **(b)** 7 u.c. (8 BaO layers) of the ferroelectric BaTiO₃ layers. The calculation was carried out using a 1D Poisson-Schrodinger solver [81]. **(c)** HAADF TEM cross-section images of the heterostructures with two u.c. (right) and seven u.c. (left) of the BaTiO₃ layer. **(d)** Maps of in- and out-of-plane lattice parameters of the samples with two different BaTiO₃ thickness normalized to SrTiO₃ lattice parameter. **(e)** Average normalized in- and out-of-plane lattice parameters for those two samples. The out-of-plane lattice parameter of BaTiO₃ is slightly smaller when BaTiO₃ thickness is below a critical thickness. This structural distortion in BaTiO₃ induces a suppression in ferroelectricity when BaTiO₃ thickness is below a critical thickness. *Reprinted from [80] with permission from American Physical Society, Copyright 2016.*

Transmission electron microscopy (TEM) images reveal the reason behind this metal-to-insulator transition, as shown in **Fig. 2.6(c-e)**. **Figure 2.6(d,e - left)** show in-plane and out-of-plane lattice parameters of the sample with 8 BaO layers, normalized to SrTiO₃ lattice parameter. The lattice parameters are calculated from TEM images (**Fig. 2.6(c)**). The out-of-plane lattice parameter of the sample is consistent with the ideal c-axis lattice parameter of BaTiO₃, indicated by the black dashed line. When the BaTiO₃ layer is below a critical thickness, the out-of-plane lattice parameter is lower than the ideal c-axis lattice parameter of BaTiO₃, as shown in **Fig. 2.6(d,e - right)**. This lattice distortion suppresses the ferroelectricity of the BaTiO₃ layer and BaTiO₃ behaves like paraelectric. Therefore, when BaTiO₃ layer contains 4 BaO layers or less, the 2DEGs do not experience any intrinsic electric field due to ferroelectric polarization. As a result, the 2DEGs can spread in both BaTiO₃ and SrTiO₃ layers, as shown in **Fig. 2.6(a)**, and they can move freely. That is why the samples with 4 BaO layers or less exhibit metallic behavior. When BaTiO₃ crosses a critical thickness, the ferroelectricity of the BaTiO₃ kicks in, and the 2DEGs experience an intrinsic electric field due to ferroelectric polarization, as shown in **Fig. 2.6(b)**. Consequently, 2DEGs are confined only in the BaTiO₃ layers. Because of dipole-electron scattering in the ferroelectric BaTiO₃ layer, the mobilities of the 2DEGs are suppressed when the BaTiO₃ layer is above this critical thickness, as shown in **Fig. 2.5(d)**. Subsequently, the sheet resistances increase, and the samples become insulating.

This experiment provides few critical insights about BaTiO₃/SrTiO₃ heterostructures. The key findings can be summarized as follows –

1. It is possible to integrate the ferroelectric BaTiO₃ layer on the semiconducting SrTiO₃ channel without any buffer layer.

2. Lattice distortion can suppress ferroelectricity in the BaTiO₃ layer. The critical thickness for this ferroelectric to paraelectric transition in BaTiO₃ is 4 BaO layer or 3 u.c. (equivalent to around 1.2 nm). Therefore, BaTiO₃ thickness should be above 1.2 nm to use as a ferroelectric layer.
3. Metal-to-insulator transition can be introduced by tuning the ferroelectricity of the BaTiO₃ layer. Dipole-electron interaction can suppress the carriers' mobility, and this interaction can be tweaked by regulating the ferroelectricity of the BaTiO₃ layer.
4. **Figure 2.5(c)** shows that the samples' sheet resistances are not very high even after the metal-to-insulator transition. This result suggests that finite conductivity and ferroelectricity can coexist, which could help ferroresistive devices, as discussed in the previous section.

2.2.2 BaTiO₃/SrTiO₃ Heterostructures

After successfully integrating ferroelectric BaTiO₃ with a semiconducting SrTiO₃ layer, we have grown BaTiO₃/SrTiO₃ heterostructures to fabricate and characterize different electronic devices. We used MBE for the epitaxial growth of these heterostructures. BaTiO₃ thickness is chosen to be 10 nm to be a ferroelectric layer while reducing gate leakage. Moreover, in these heterostructures, there is no 2DEG from polar discontinuity. Therefore, the SrTiO₃ layer is doped with La to make the channel conducting. **Figure 2.7(a)** shows a schematic diagram of the heterostructure. **Figure 2.7(b)** show the reflection high energy electron diffraction (RHEED) images along $\langle 100 \rangle$ and $\langle 110 \rangle$ direction after the growth of SrTiO₃ (right) and BaTiO₃ (left) layers. Nice streaky RHEED images with surface reconstruction indicate the good surface and interface quality of the films. **Figure 2.7(c)** shows a typical wide range 2 θ -

ω x-ray diffraction (XRD) scan of a BaTiO₃/SrTiO₃ heterostructure. The XRD displays both BaTiO₃ and SrTiO₃ peaks, suggesting good structural quality of the film. In the next section, we discuss the electrical characteristics of different BaTiO₃/SrTiO₃ based electronic devices.

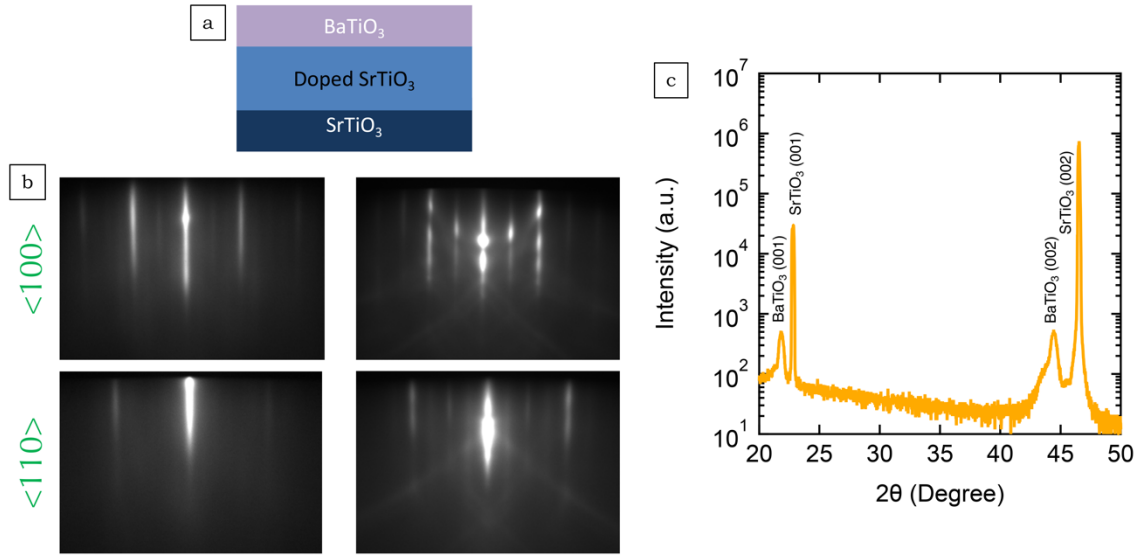


Figure 2.7: Epitaxial BaTiO₃/SrTiO₃ heterostructure. (a) Schematic diagram of MBE grown epitaxial BaTiO₃/SrTiO₃ heterostructure. The heterostructure is grown on insulating SrTiO₃ substrate. (b) In-situ RHEED images of the sample after the growth of SrTiO₃ (right) and BaTiO₃ (left) layers along <100> (top) and <110> (bottom) directions. The RHEED images show nice streaky pattern with surface reconstruction. (c) Wide range 2θ- ω x-ray diffraction scan of BaTiO₃/SrTiO₃ heterostructure showing both BaTiO₃ and SrTiO₃ peaks.

2.3 BaTiO₃/SrTiO₃ Devices

We have studied the parallel plate capacitors and heterojunction FETs with ferroelectric BaTiO₃ layers grown epitaxially on the La-doped SrTiO₃ channel. A reference sample was also

grown where the ferroelectric BaTiO₃ layer is replaced with an undoped dielectric SrTiO₃ cap layer. By comparing the electrical characteristics of BaTiO₃/SrTiO₃ devices with the reference sample, the effect of ferroelectric polarization on the channel and device characteristics can be isolated.

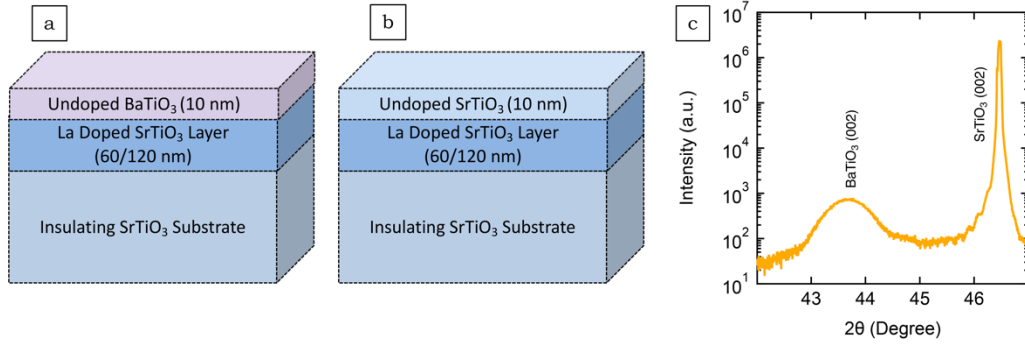


Figure 2.8: Integration of epitaxial ferroelectric layer on semiconducting channel. Schematic diagrams of the epitaxial structures of **(a)** BaTiO₃/doped SrTiO₃ heterostructures and **(b)** reference sample. The channels of the BaTiO₃ capped heterostructures are either 60 nm or 120 nm thick, while La doping density varies from $1 \times 10^{19} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. The BaTiO₃ cap layer is replaced with an undoped SrTiO₃ layer in the reference sample. **(c)** 2θ-ω x-ray diffraction scan of BaTiO₃/SrTiO₃ heterostructure showing both BaTiO₃ and SrTiO₃ peaks.

The schematic diagrams of the BaTiO₃/SrTiO₃ heterostructure and the SrTiO₃-capped reference sample are shown in **Fig. 2.8(a,b)**. All of these samples were grown using MBE on insulating SrTiO₃ (001) substrates. Special surface treatment was carried out to flatten the substrate surfaces and improve the films' quality grown on the substrates (detail in **Appendix**). BaTiO₃ cap layers are 10 nm thick to ensure ferroelectricity and reduce gate leakages. The undoped SrTiO₃ cap layer of the reference sample is of similar thickness. La-doped SrTiO₃

channel layers were grown in two different thicknesses – 60 nm and 120 nm. La doping densities were varied between $1 \times 10^{19} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. SrTiO₃ channel thickness for the reference sample is 60 nm, while La doping concentration is $1 \times 10^{19} \text{ cm}^{-3}$. All these samples were annealed at 900 °C in a rapid thermal annealing chamber at an oxygen ambient to remove any oxygen vacancies. References [80,82,83] detail the MBE procedure of epitaxial growth of SrTiO₃ and BaTiO₃ and electrical properties of La-doped SrTiO₃ for a wide range of doping densities. **Figure 2.8(c)** shows the high resolution XRD scan of a BaTiO₃/SrTiO₃ heterostructure and confirms epitaxial single-crystal BaTiO₃ film.

We fabricated and characterized parallel plate capacitors and heterojunction FETs to understand the effect of ferroelectric polarization on the underlying semiconducting channels. Parallel plate capacitors with different sizes were fabricated, varying from $90 \times 90 \mu\text{m}^2$ to $150 \times 300 \mu\text{m}^2$. Optical lithography was used to pattern Schottky contacts, and subsequently, Au/Pt (150 nm/ 50 nm) metal stacks were deposited by electron-beam (e-beam) evaporation as Schottky contacts. 1 eV Schottky barrier height between Pt and BaTiO₃ acts as a negative bias while reducing gate leakage. To form Ohmic contacts, the top BaTiO₃ cap layers were patterned and etched using chlorine-based inductive coupled plasma (ICP) etching to access the underneath doped SrTiO₃ channel, which acts as a back contact of the parallel plate capacitors. Then Au/Ti (150 nm/ 50 nm) metal stacks were deposited in the etched region using e-beam evaporation to form Ohmic contacts with the La-doped SrTiO₃ channel. A schematic

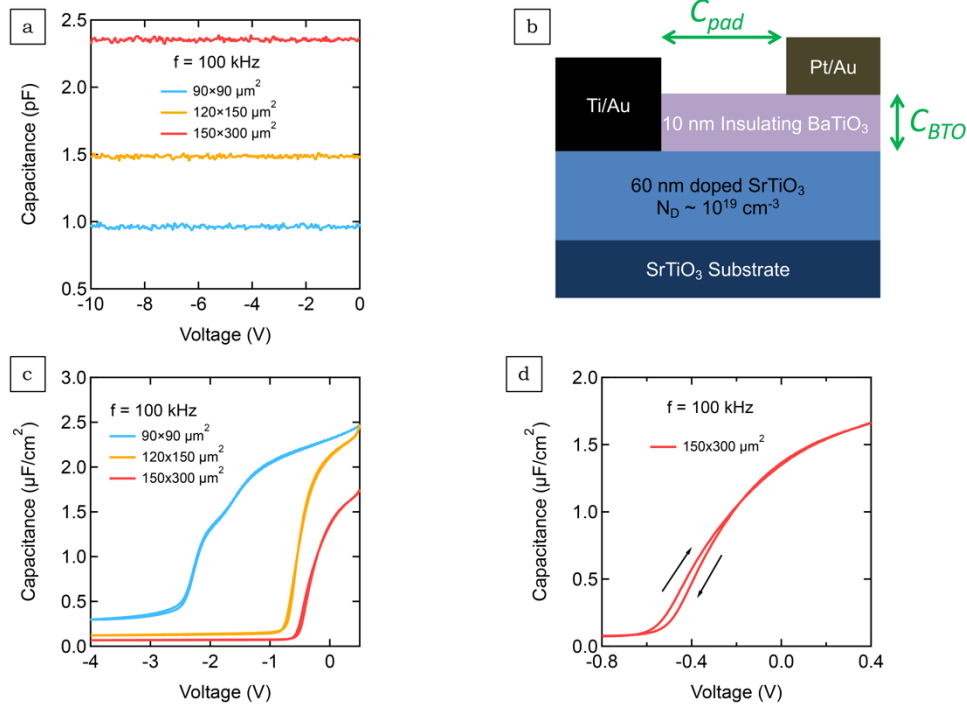


Figure 2.9: Ferroelectric polarization-induced depletion in SrTiO₃ channel. (a) Capacitance-voltage characteristics of a BaTiO₃/SrTiO₃ heterostructure. Capacitances were measured at 100 kHz for three different sizes of the capacitors. **(b)** Schematic diagram of a parallel plate capacitor. As shown in the schematic diagram, there are two components (C_{pad} and C_{BTO}) that contribute to the measured capacitances. C_{pad} is scaled with perimeter, while C_{BTO} is scaled with the area. The perimeter-dependent C - V characteristics suggest a complete depletion of the channel due to ferroelectric polarization. **(c)** Capacitance-voltage characteristics of the reference sample were measured at 100 kHz for three different sizes of the capacitors. **(d)** A close-up of the capacitance-voltage characteristics of the reference sample shows no significant hysteresis.

diagram of the parallel plate capacitor is shown in **Fig. 2.9(b)**. Ferroelectric-gated heterojunction FETs were fabricated on the sample where SrTiO₃ channel thickness is 60 nm with La doping concentration of $3 \times 10^{19} \text{ cm}^{-3}$. A thinner channel heterojunction was selected to improve SS. Circular FETs were fabricated as they do not require any mesa isolation. So,

this type of device structure should not have any etching-induced leakages and damages. It will help to eliminate any fabrication-related secondary effects. To form Ohmic contacts, the same BaTiO₃ etching process was used. Moreover, the same Schottky and Ohmic metal stacks were deposited using e-beam evaporation to make gate and source/drain contacts, respectively. **Figure 2.14(a)** shows a picture of a circular FET. The gate length and the source-drain spacing of this circular FET are 15 μm and 55 μm , respectively. The square pad in the gate contact is used to probe the devices. Though these large square pads introduce non-uniformity in electrostatics and current flow, that should not affect any characteristics we study here. Current-voltage (I - V) and capacitance-voltage (C - V) characteristics were probed using an Agilent B1500A parameter analyzer and an Agilent 4294A impedance analyzer, respectively.

2.3.1 Capacitance–Voltage (C - V) characteristics

Figure 2.9(a) shows the C - V characteristics of a parallel plate capacitor fabricated on BaTiO₃/SrTiO₃ heterostructure, measured at 100 kHz. The SrTiO₃ channel is 60 nm thick with a La doping concentration of $3 \times 10^{19} \text{ cm}^{-3}$. This figure displays tiny capacitance, only a few pF. Intriguingly, the measured capacitance is scaled with the perimeters of different capacitor pads. The ratio of the perimeters of the capacitors with different Schottky contact areas is 1:1.5:2.5. The measured capacitances shown in **Fig. 2.9(a)** follow the same ratio. This similarity implies that instead of measuring the vertical capacitance across the BaTiO₃ layer (C_{BTO}), this measurement is probing the horizontal capacitance between two pads (C_{pad}), as shown in **Fig. 2.9(b)**. As C_{pad} depends on the edge of the capacitors, the measured capacitances show a linear dependence on the perimeter. We can compare these results with the reference sample's C - V characteristics, as shown in **Fig. 2.9(c)**. The reference sample has similar channel

thickness and doping density. Unlike BaTiO₃/SrTiO₃ heterostructure, the C - V characteristics of this reference sample show very high capacitance density. The reference sample's large capacitance density is due to the sizeable low-field permittivity of SrTiO₃ ($\sim 300\epsilon_0$) at room temperature [36]. Negative gate voltage depletes the channel and increases the depletion width. The fall in capacitance at negative gate voltage is due to this increased depletion width, which increases the distance between two conductive plates of a parallel plate capacitor. Moreover, electric field tunable permittivity associated with SrTiO₃ [84,85] further amplifies the decrease in capacitances at negative gate voltage region. Unlike BaTiO₃/SrTiO₃ devices' capacitances, these measured capacitances show no correlation with the capacitors' perimeters. These capacitances are not scaled with the area of the capacitors either. When the size of the capacitor increases, it increases both series resistances and gate leakages. These contribute to lower capacitance densities in capacitors with a larger area. Furthermore, as both BaTiO₃ and SrTiO₃ have very high permittivity, fringing capacitance contribution should be significant, and it should bump the capacitance densities in the smaller devices. A comparison between the capacitances measured in both samples reveals that the BaTiO₃/SrTiO₃ sample's capacitances are not the vertical capacitance of the BaTiO₃ layer, C_{BTO} , but the horizontal capacitance between Ohmic and Schottky pads, C_{pad} . Moreover, the comparison suggests that the parallel plate capacitor's back contact (doped SrTiO₃ layer) is not acting as a conductive equipotential layer in the BaTiO₃/SrTiO₃ sample. To understand the reason behind this unusual capacitance characteristic of the BaTiO₃/SrTiO₃ sample, the current-voltage (I - V) characteristics of the Schottky contacts of BaTiO₃/SrTiO₃ and reference samples were measured, as shown in **Fig. 2.10(a)**. These results show that the device fabricated on BaTiO₃/SrTiO₃ exhibits a much lower current density. There is at least a six-order difference between the Schottky contact current

densities of these two samples. This low current density indicates the lack of Ohmic contact formation between doped SrTiO₃ layer and Au/Ti metal stacks. There are two possible reasons behind this lack of Ohmic contact formation –

1. The insulating BaTiO₃ layer is not entirely etched, leading to a bad Ohmic contact.
2. The doped SrTiO₃ channel is wholly depleted due to ferroelectric polarization.

At first, we need to confirm whether or not this unusual C - V characteristic is a consequence of bad Ohmic contacts stemmed from the under-etching of the insulating BaTiO₃ layer. Chlorine-based ICP etching described earlier has an etch rate of 10 nm/min for BaTiO₃. To ensure that the BaTiO₃ layer is not under-etched, we fabricated parallel plate capacitors on two different pieces of the same BaTiO₃/SrTiO₃ sample where the BaTiO₃ layer is etched for 1.5 and 2.5 minutes before metal deposition. Capacitors were fabricated on the reference sample with similar cap layer etch time, too. This over-etching should ensure the successful formation of ohmic contact with the underneath SrTiO₃ layer if the layer is conductive. **Figure 2.10(c,d)** shows the Schottky current characteristics of the devices with 1.5 minutes and 2.5 minutes cap layer etching. Even after over-etching, BaTiO₃/SrTiO₃ sample shows several orders lower Schottky currents. These results eliminate the possibility of bad Ohmic contact due to the under-etched BaTiO₃ layer and confirm that the unusual C - V characteristics stem from the fully depleted SrTiO₃ layer due to ferroelectric polarization. A fully depleted insulating channel prevents a good Ohmic contact required to form an equipotential back contact, and thus the capacitor structure fails to function as a parallel plate capacitor. That is why the measured capacitance in the BaTiO₃/SrTiO₃ sample is C_{pad} instead of C_{BTO} . The polarization direction of the BaTiO₃ can be deduced from this fully depleted channel. As the ferroelectric polarization

depletes negative carriers from the channel, the polarization direction must be pointed perpendicular outward of the sample plane, as shown in **Fig. 2.10(b)** with a black arrow.

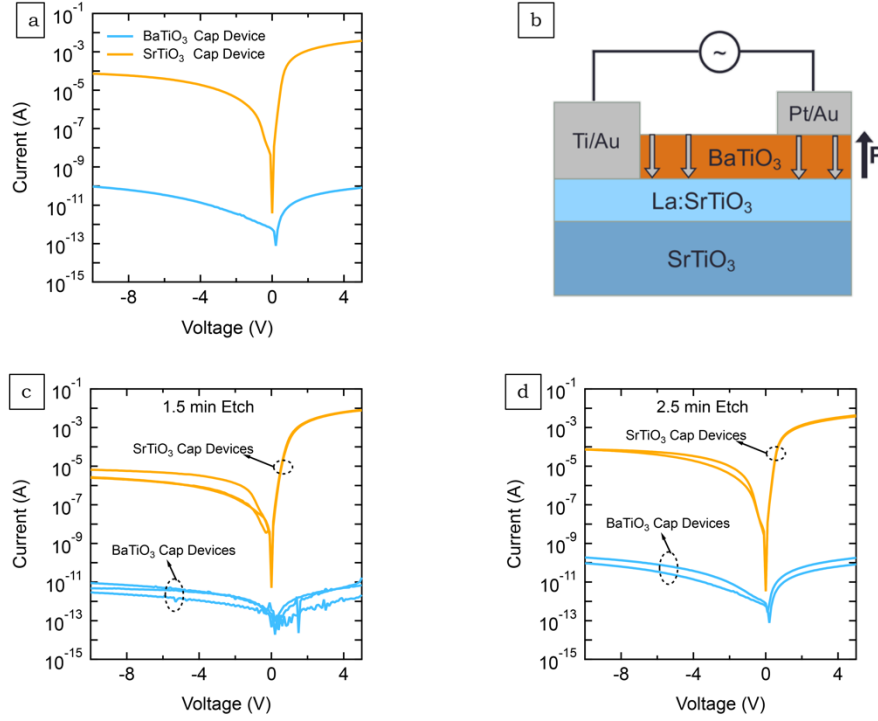


Figure 2.10: Out-of-plane ferroelectric polarization in BaTiO₃/SrTiO₃ heterostructure. (a) I - V characteristics of the Schottky contacts of BaTiO₃/SrTiO₃ (blue) and reference (orange) samples. BaTiO₃ capped sample shows at least six orders lower current density. **(b)** Schematic diagram of a parallel plate capacitor fabricated on BaTiO₃/SrTiO₃ sample. Lower current density in BaTiO₃ capped sample is due to complete depletion of the channel, indicating polarization direction along out-of-plane of the sample, as shown with a black arrow. *Reprinted from [86] with permission from AIP Publishing.* I - V characteristics of the same samples where cap layer is etched for **(c)** 1.5 minutes and **(d)** 2.5 minutes to verify that lower current density is due to ferroelectricity, not bad Ohmic contacts.

To avoid complete depletion of the SrTiO₃ channel, we grew two additional BaTiO₃/SrTiO₃ samples with higher sheet carrier densities. Both of these samples have a 120 nm thick SrTiO₃ channel with La doping densities of $2 \times 10^{19} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$. Thicker channels accompanied by higher doping densities should increase sheet carrier densities in the channels and prevent complete depletion. Afterwards, parallel plate capacitors were fabricated in both samples following the fabrication process described earlier, and then their C - V characteristics were investigated. **Figure 2.11(a)** shows the C - V characteristics of the sample with higher doping density ($5 \times 10^{19} \text{ cm}^{-3}$) for two different sizes of capacitors measured at 100 kHz. **Figure 2.11(b)** displays the capacitances and quality factors of the same devices as a function of frequency. C - V characteristics show a drop in capacitance at a negative voltage. This drop is associated with increased depletion width in the channel and field tunable permittivity of SrTiO₃, as explained earlier for the reference sample. Moreover, both capacitance and quality factor drop at a higher frequency. SrTiO₃ has very low electron mobility at room temperature ($\sim 10 \text{ cm}^2/\text{Vs}$). This low mobility leads to the high sheet resistance of the back contact and increases the capacitor's series resistance. The fall in capacitance and quality factors at high frequency is a result of this high series resistance. Moreover, the larger capacitor shows lower capacitance density due to larger series resistance and higher gate leakage. Due to the channel's large sheet carrier density, the channel cannot be completely depleted even at a large negative gate bias. 120 nm channel with $5 \times 10^{19} \text{ cm}^{-3}$ doping density should contain sheet carrier density of $6 \times 10^{14} \text{ cm}^{-2}$ without any depletion due to ferroelectric polarization. As the polarization charge of BaTiO₃ is equivalent to low 10^{14} cm^{-2} , a huge sheet carrier density should remain in the channel even after ferroelectricity-induced depletion. Electrostatic gating

is unable to modulate this huge number of carriers [84,85]. That is why the C - V characteristics of this higher doped sample do not show complete depletion.

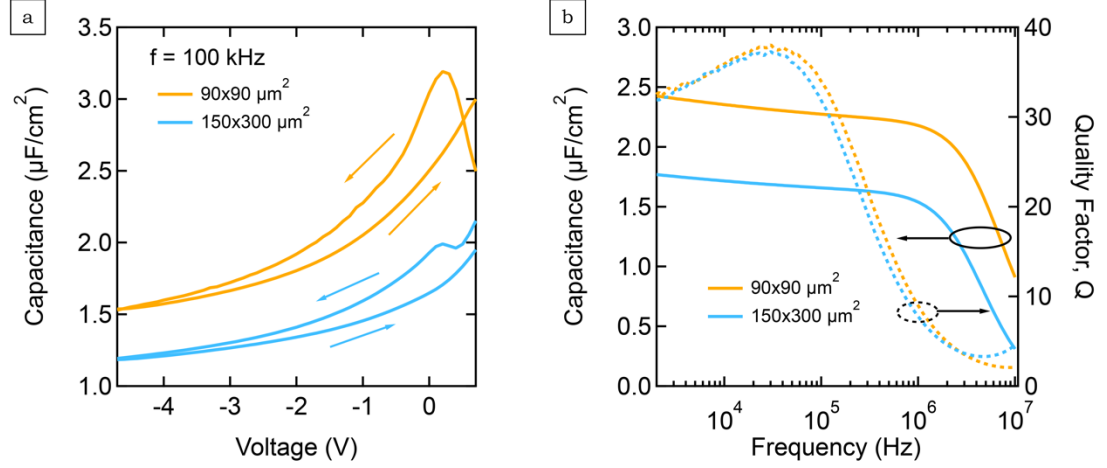


Figure 2.11: Capacitance-voltage characteristics of $\text{BaTiO}_3/\text{La-doped SrTiO}_3$ heterostructure with a doping density of $5 \times 10^{19} \text{ cm}^{-3}$. (a) Capacitance-voltage and (b) Capacitance-frequency and quality factor-frequency characteristics of a $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructure. SrTiO_3 channel is 120 nm thick with a doping density of $5 \times 10^{19} \text{ cm}^{-3}$. The C - V characteristics show anti-clockwise hysteresis due to ferroelectric gating. Due to high sheet carrier density, the channel cannot be completely depleted using electrostatic gating.

Figure 2.12(a) shows the sample's C - V characteristics with lower doping density ($2 \times 10^{19} \text{ cm}^{-3}$) for two different sizes of capacitors measured at 10 kHz. **Figure 2.12(b)** displays the same devices' capacitances and quality factors as a function of frequency. Like the higher doped sample, these C - V characteristics also exhibit a fall in capacitance at negative gate bias. Additionally, these C - V characteristics demonstrate a complete depletion of the channel at -3 V due to lower sheet carrier density. In addition, the peak capacitances of these capacitors are smaller than those of the higher doped sample. Zero bias depletion width is wider for a lower

doped sample, and this is the reason behind these slightly smaller peaks in C - V characteristics. The lower doping density also causes a faster fall in capacitances at negative gate bias than higher doped devices. Additionally, the lower doping density also raises the capacitors' series resistances, resulting in an early degradation in capacitances and quality factors at a higher frequency than the higher doped devices.

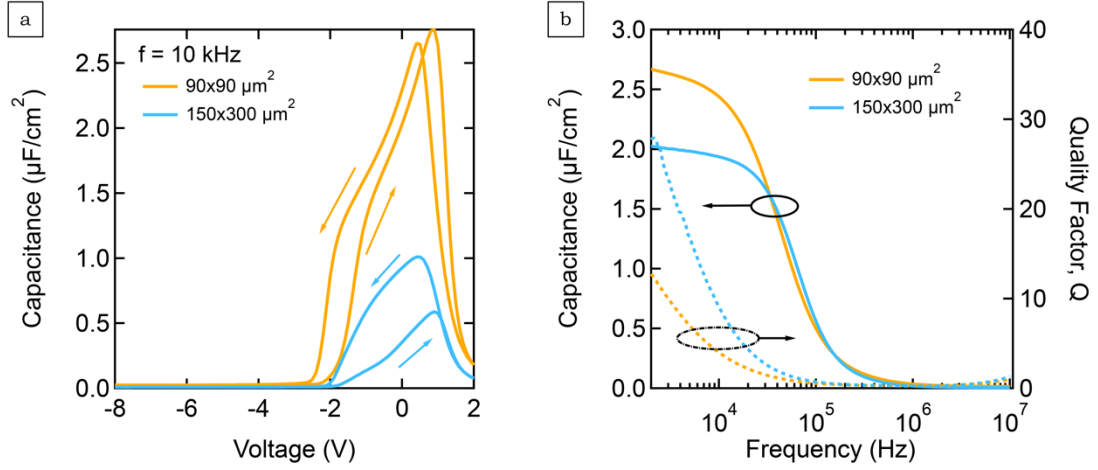


Figure 2.12: Capacitance-voltage characteristics of $\text{BaTiO}_3/\text{La-doped SrTiO}_3$ heterostructure with a doping density of $2 \times 10^{19} \text{ cm}^{-3}$. (a) Capacitance-voltage and (b) Capacitance-frequency and quality factor-frequency characteristics of a $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructure. SrTiO_3 channel is 120 nm thick with a doping density of $2 \times 10^{19} \text{ cm}^{-3}$. Due to the channel's low sheet carrier density, the pinch-off voltages of the devices are $\sim -3 \text{ V}$.

Most notably, both samples exhibit anti-clockwise hysteresis in their C - V characteristics. In contrast, the reference sample shows no significant hysteresis in the C - V characteristics (**Fig. 2.9(d)**). Anti-clockwise hysteresis is a signature of a shift in the threshold voltage due to switching in ferroelectric polarization direction. Moreover, anti-clockwise hysteresis differentiates itself from clockwise hysteresis, usually associated with charge trappings [76,

87-89]. A negative gate voltage aligns the polarization with favoring the depletion of the electrons from the channel. Subsequently, it requires a higher positive gate voltage to accumulate electrons in the channel than the absence of any ferroelectric polarization. Sufficient positive voltage switches the ferroelectric layer's polarization direction and favors a large electron accumulation. So, a larger negative gate voltage is necessary to deplete the channel. This polarization-induced asymmetry is the reason behind anti-clockwise hysteresis in the C - V characteristics.

By integrating the C - V characteristics of **Fig. 2.12(a)**, it is possible to calculate the carrier densities in the channel during the downward (positive to negative) and upward (negative to positive) sweeps of the gate voltage. The calculated sheet carrier densities are $2.3 \times 10^{13} \text{ cm}^{-2}$ and $1.6 \times 10^{13} \text{ cm}^{-2}$ during downward and upward voltage sweeps, respectively. 120 nm channel with $2 \times 10^{19} \text{ cm}^{-3}$ doping density should exhibit sheet carrier density of $2.4 \times 10^{14} \text{ cm}^{-2}$ in the absence of any ferroelectric polarization. By comparing these carrier densities, it is clear that BaTiO₃ film has a ferroelectric polarization charge equivalent to $\sim 2 \times 10^{14} \text{ cm}^{-2}$, slightly higher than that of bulk BaTiO₃. As BaTiO₃ has a marginally larger lattice parameter than SrTiO₃, BaTiO₃ is under compressive stress. This compressive stress could be the reason behind this enhancement in polarization charge. Moreover, the difference in sheet carrier densities during upward and forward voltage sweeps suggests that the amount of switchable polarization charge is equivalent to $7 \times 10^{12} \text{ cm}^{-2}$, much smaller than the ferroelectric polarization charge of BaTiO₃. There is no significant conduction band offset between BaTiO₃ and SrTiO₃. This lack of conduction band offset makes applying a positive gate voltage complicated in BaTiO₃/SrTiO₃ devices, which is necessary for the complete switching of the

polarization of the BaTiO₃ layer. That is why parallel conductance and quality factors of the capacitors degrade sharply after applying positive bias. Additionally, this lack of conduction band offset limits the amount of switchable polarization charge.

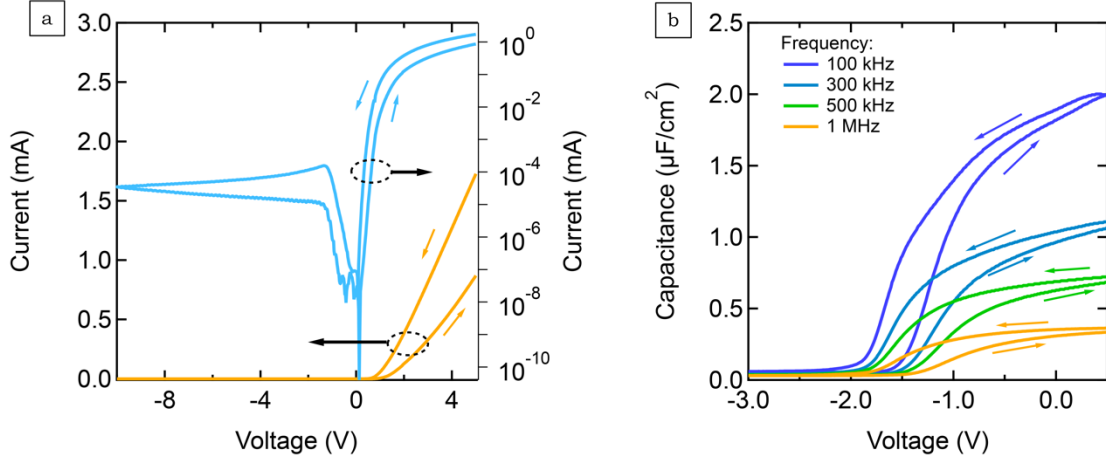


Figure 2.13: Gate contact characteristics of the BaTiO₃/SrTiO₃ FETs. (a) Gate leakage of a BaTiO₃/SrTiO₃ FET in linear (orange) and logarithmic (blue) scale. The gate leakage shows anti-clockwise hysteresis as an effect of ferroelectric gating. Moreover, the I - V characteristics show ferroresistive characteristics with a resistance ratio over 20 between high and low resistive states. **(b)** Gate capacitances of the FET are measured at different frequencies. A significant frequency dispersion is visible due to a considerable series resistance.

2.3.2 Ferroelectric Gated Field-Effect Transistors

This section discusses how ferroelectric BaTiO₃ can affect the FET characteristics. To investigate BaTiO₃ gated FETs, we fabricated circular FETs (**Fig. 2.14(a)**) using the fabrication process described earlier. The FETs were fabricated on a BaTiO₃/SrTiO₃ sample with a 60 nm thick SrTiO₃ channel with a La doping density of $\sim 3 \times 10^{19} \text{ cm}^{-3}$. The thinner

channel is used for FETs to improve SS. Furthermore, the doping density level is selected so that the channel is neither fully depleted due to ferroelectric polarization nor contains too many carriers to deplete by electrostatic gating.

Figure 2.13(a) shows the gate leakage characteristics of a circular FET in both linear and logarithmic scales. This figure shows more than four orders of magnitude rectification in gate leakage. Moreover, as there is no conduction band offset between BaTiO₃ and SrTiO₃, gate leakage increases significantly when gate voltage exceeds 1 V. The gate leakage is very small (< 100 nA) within the range used for polarization switching and thus plays no significant role in our findings. As expected, the gate leakage shows anti-clockwise hysteresis associated with a shift in threshold voltage due to polarization switching. Additionally, ferroelectricity-induced hysteresis switches the resistivity of the gate-channel junction during upward and downward voltage sweeps. These types of two-terminal devices could be used as ferroresistive devices in neuromorphic systems. The ratio of low resistive state and high resistive state is around 20. This ratio can be further improved by controlling the gate leakage.

Figure 2.14(b) shows the gate capacitances of the FET at different frequencies. The anti-clockwise hysteresis continues to persist for the entire range of the frequencies. This figure also indicates similar degradation in capacitances at higher frequencies due to high series resistances associated with high resistivity of the SrTiO₃ channel. At 100 kHz, the C - V characteristics show carrier modulation of $2.2 \times 10^{13} \text{ cm}^{-2}$ and $1.8 \times 10^{13} \text{ cm}^{-2}$ during downward and upward voltage sweeps, respectively. This is equivalent to a switchable polarization charge of $4 \times 10^{12} \text{ cm}^{-2}$, slightly lower than the previous C - V analysis. The circular FET's Gate area is

larger than smaller parallel plate capacitors, and capacitances were measured at a higher frequency in the FET device. As explained in the previous section, both of these factors are responsible for degradation in capacitances. These factors could be the reason behind this lower switchable polarization charge in FET devices.

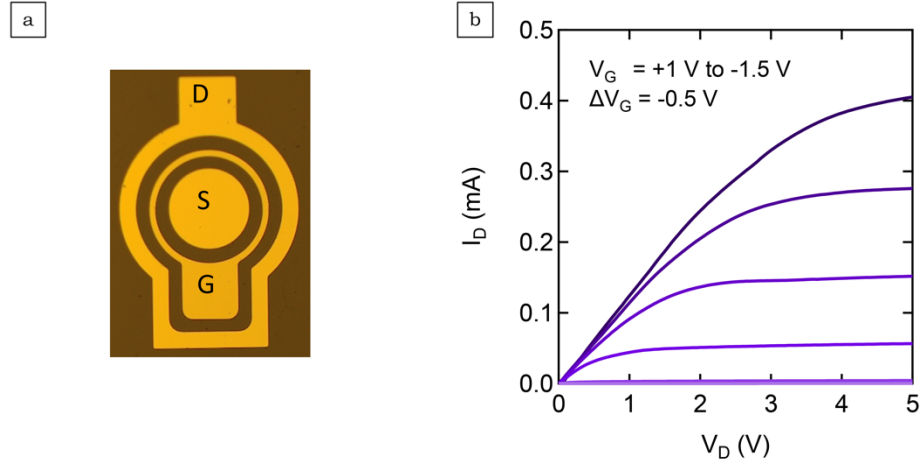


Figure 2.14: Output characteristics of BaTiO₃/SrTiO₃ FET. (a) An image of a BaTiO₃/SrTiO₃ circular FET. The inner ring is the gate. The device's gate length is 15 μm , while source-to-drain spacing is 55 μm . *Reprinted from [86] with permission from AIP Publishing.* **(b)** The I_D - V_D characteristics of the circular FET. The pinch-off voltage of the device is -1 V.

The drain current vs. drain-to-source voltage (I_D - V_D) characteristics of BaTiO₃/SrTiO₃ circular FET is shown in **Fig. 2.14(b)**. The output characteristics of the FET show good transistor performance with a pinch of voltage around -1 V. Since the gate length of the transistor is 15 μm , the output characteristics exhibit expected long channel behavior with no output conductance. The current density of the device is extremely low, compared to the previous SrTiO₃ based FETs [84,85], because of the low sheet carrier density due to ferroelectric

polarization-induced depletion in the channel. Additionally, a long source-to-drain distance (55 μm) is also responsible for this low current density. The device exhibits no degradation of electron mobility in the SrTiO₃ channel, indicating that apart from the carrier depletion, BaTiO₃ does not affect the electronic transport properties of the SrTiO₃ channel.

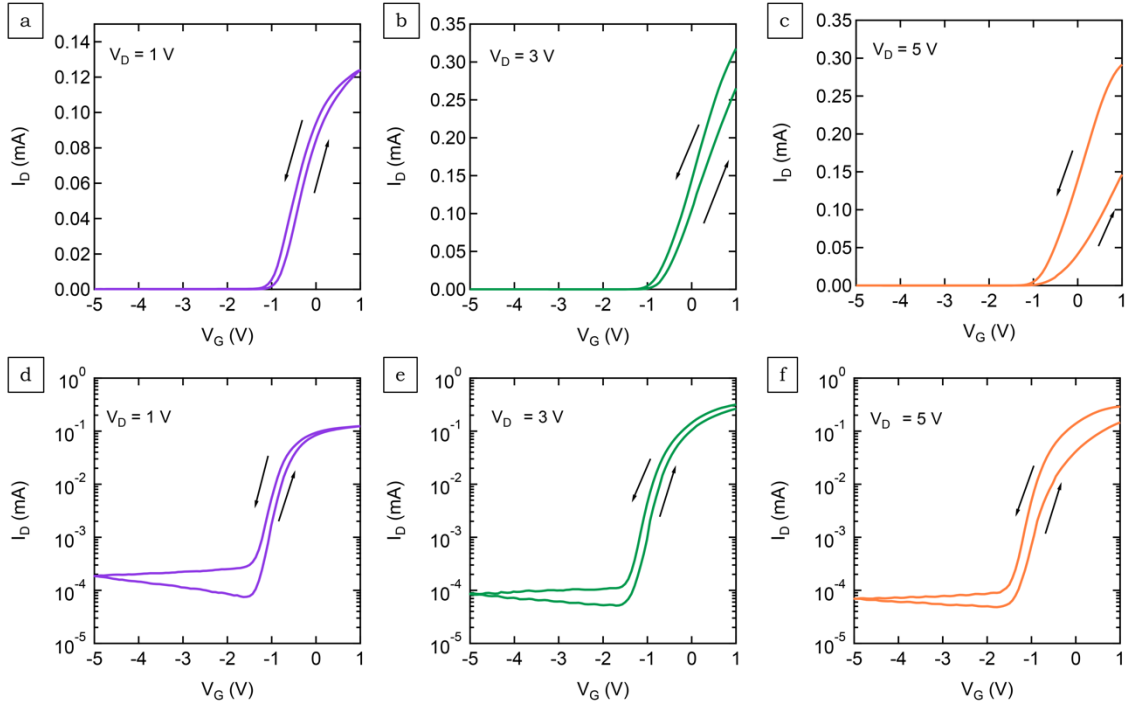


Figure 2.15: Transfer characteristics of BaTiO₃/SrTiO₃ FET. I_D - V_G characteristics of a BaTiO₃/SrTiO₃ circular FET for different drain voltages in (a,b,c) linear and (e,f,g) logarithmic scale. The I - V characteristics show anti-clockwise hysteresis, a signature of ferroelectric gating.

Figure 2.15 shows the drain current vs. gate voltage (I_D - V_G) characteristics at different drain voltages ranging from 1 V to 5 V, both in linear and logarithmic scales. All the transfer curves show anti-clockwise hysteresis due to ferroelectric polarization-induced shift in threshold voltage. The change in threshold voltage depends on the drain voltage, and when the drain

voltage is 5 V, the transistor exhibits around 0.5 V shift in threshold voltage. I_{on}/I_{off} ratio of the transistor is about 10^4 . **Figure 2.16** shows the device's SS at different drain voltages during upward and downward gate voltage sweeps. The transistor shows very high SS with a minimum SS of 200 mV/dec. There are several reasons behind this poor SS performance of the BaTiO₃/SrTiO₃ FETs. Using **Eqn. 2.1-2.2** and Boltzmann transport equation, SS of a FET can be rewritten as [90] -

$$SS = \frac{2.3 kT}{q} \left(1 + \frac{C_s}{C_{ox}} \right) \dots \dots \dots (2.3)$$

where k is the Boltzmann constant, T is the temperature, and q is the charge of an electron.

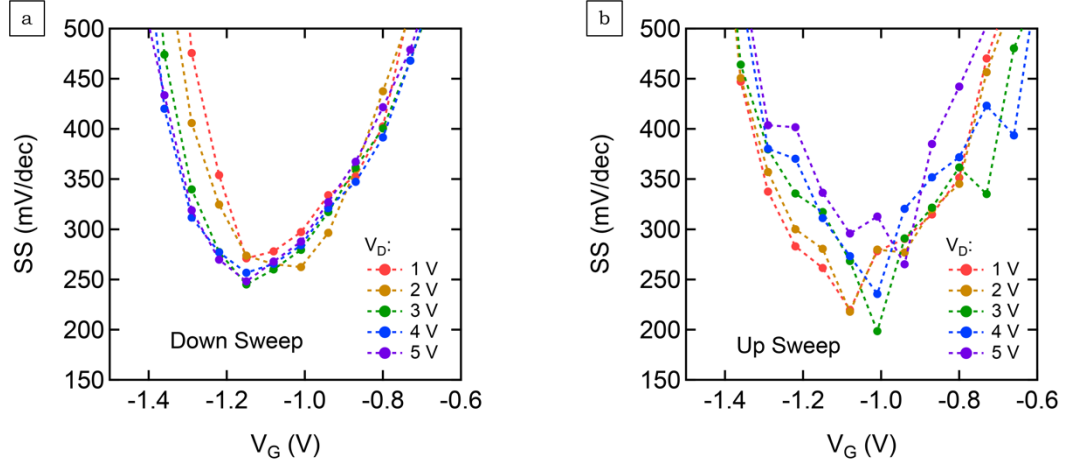


Figure 2.16: Subthreshold swing of a BaTiO₃/SrTiO₃ FET. SS during (a) downward and (b) upward gate voltage sweeps for different drain voltages. As channel capacitances, C_s decreases with negative voltages, subthreshold swing drops with negative gate voltage. At large negative gate voltage, the gate leakage starts to dominate drain current, and subthreshold swing starts to degrade.

As mentioned earlier, C_s is the channel's capacitance, and if C_s is high, that will degrade SS. In BaTiO₃/SrTiO₃ FETs, a depletion region is formed in the channel that contributes to C_s . As SrTiO₃ has a large permittivity, C_s contribution is significant in BaTiO₃/SrTiO₃ FETs. This high C_s is the reason behind high SS in these devices. Depletion capacitances decrease with increased depletion width. Moreover, the higher electric field in the SrTiO₃ layer lowers the permittivity of the channel. That also results in lower depletion capacitances. That is why **Fig. 2.16** shows a fall in SS when negative gate voltages are applied. Nonetheless, SS starts to increase again due to large gate leakages when the gate voltage is below -1 V. As the deep subthreshold region is dominated by gate leakage, we could not observe any negative capacitance effect in BaTiO₃/SrTiO₃ devices.

2.3.3 Temperature-Dependent Device Characteristics

Bulk BaTiO₃ has a Curie temperature of 400 K. We have characterized FETs and capacitors at higher temperatures to investigate the Curie temperature of our epitaxial BaTiO₃ films. Moreover, this study should reveal the effect of ferroelectric-to-dielectric transition of BaTiO₃ on device characteristics. This study was carried out in a vacuum MMR probe station that has a temperature range of 77 K to 500 K and an Agilent B1500A parameter analyzer.

Figure 2.17 shows the I_D - V_G characteristics of the BaTiO₃/SrTiO₃ circular FET measured at 300 K to 420 K. The orange curves indicate the gate leakage of the device. The gate leakage of the device increases significantly at a higher temperature, especially when the gate voltage is below the pinch-off voltage. This degrades the I_{on}/I_{off} ratio of the device significantly at a higher temperature. The transistor demonstrates anti-clockwise hysteresis for this entire

temperature range, suggesting that the ferroelectricity of BaTiO₃ persists even at 420 K. This temperature is above the Curie temperature of bulk BaTiO₃. This enhancement in Curie temperature could be the result of compressive stress on the BaTiO₃ layer. Compressive stress-induced ferroelectric enhancements have already been reported in the literature [91].

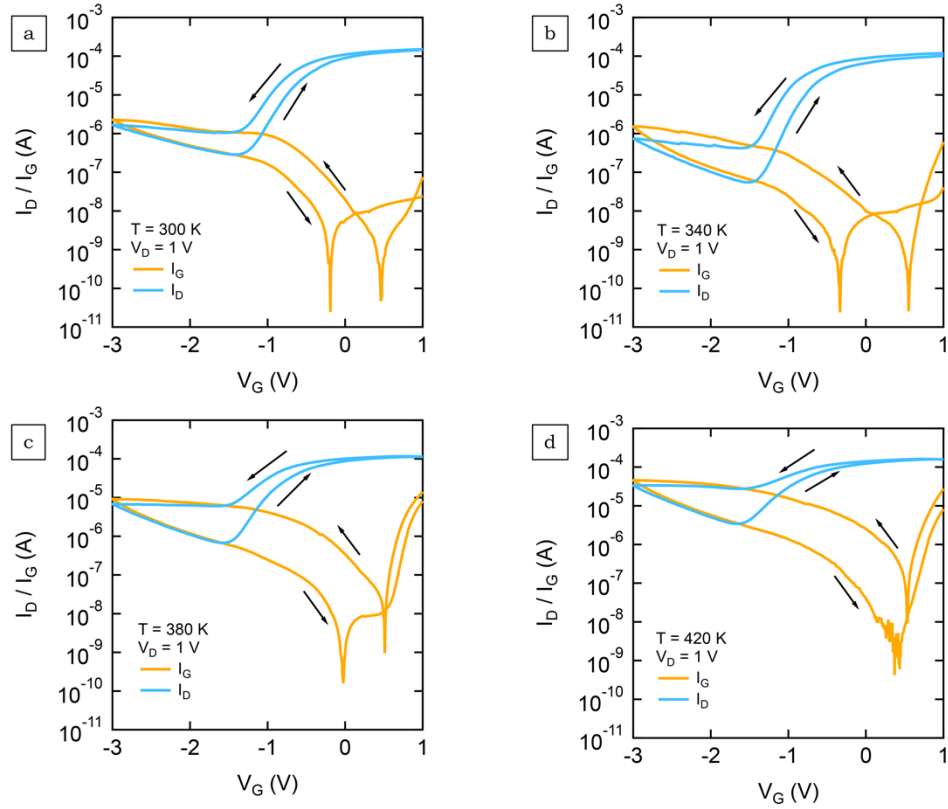


Figure 2.17: Temperature-dependent BaTiO₃/SrTiO₃ FET characteristics. I_D - V_G characteristics and gate leakages of BaTiO₃/SrTiO₃ FET measured at **(a)** 300 K, **(b)** 340 K, **(c)** 380 K, and **(d)** 420 K. Anti-clockwise hysteresis persists for the whole range of the temperature. Moreover, gate leakage degrades significantly at a higher temperature, especially at subthreshold regions.

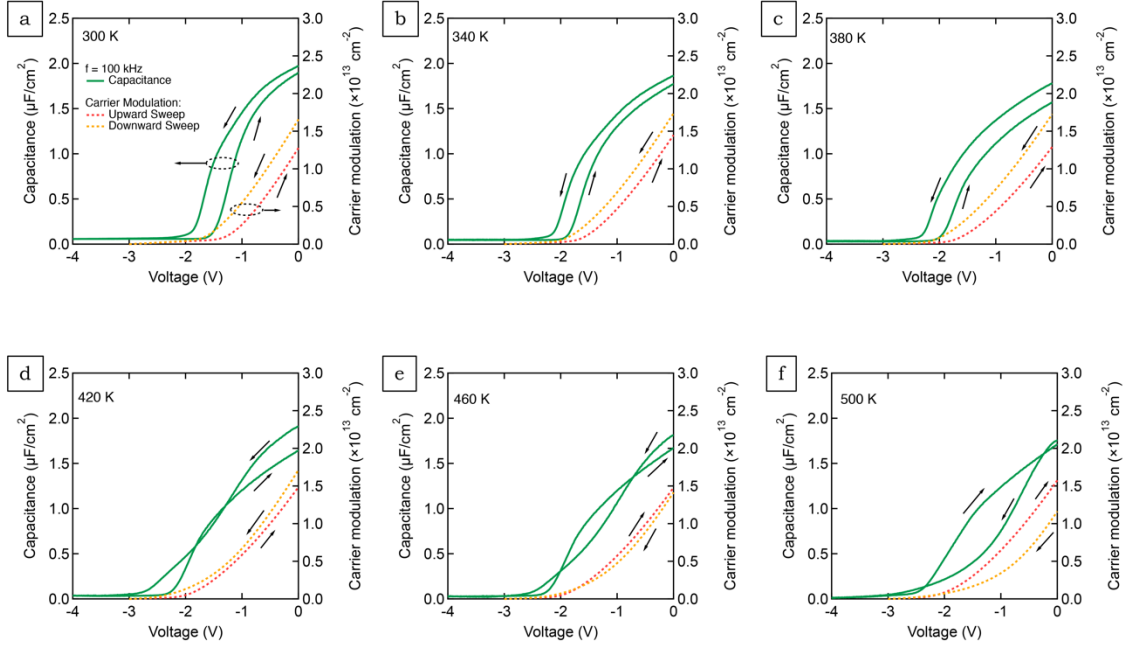


Figure 2.18: Temperature-dependent capacitance-voltage characteristics of $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructure. $C-V$ characteristics of $\text{BaTiO}_3/\text{SrTiO}_3$ heterojunction measured at (a) 300 K, (b) 340 K, (c) 380 K, (d) 420 K, (e) 460 K, and (f) 500 K. From 420 K, the $C-V$ characteristics start to exhibit a mixture of clockwise and anti-clockwise hysteresis, indicating suppression of ferroelectricity. At 500 K, the hysteresis is completely clockwise, suggesting a complete ferroelectric to the dielectric transition of BaTiO_3 thin film. The orange and red dashed lines show the charge modulation during downward and upward voltage sweeps, respectively.

Figure 2.18 shows the $C-V$ characteristics of a $\text{BaTiO}_3/\text{SrTiO}_3$ parallel plate capacitor measured at 300 K to 500 K. Up to 380 K; the $C-V$ characteristics exhibit consistent anti-clockwise hysteresis. At 420K, the device displays the first sign of anomaly in hysteresis. Above 450 K, the clockwise hysteresis starts to dominate, indicating weak ferroelectricity, and at 500 K, the $C-V$ characteristics exhibit completely clockwise hysteresis, suggesting a non-ferroelectric BaTiO_3 layer. These temperature-dependent $C-V$ characteristics indicate a

ferroelectric-to-dielectric transition in the BaTiO₃ layer. Besides, these characteristics do not indicate a sharp change in ferroelectricity in the BaTiO₃ layer. Furthermore, C - V characteristics exhibit an enhancement in Curie temperature.

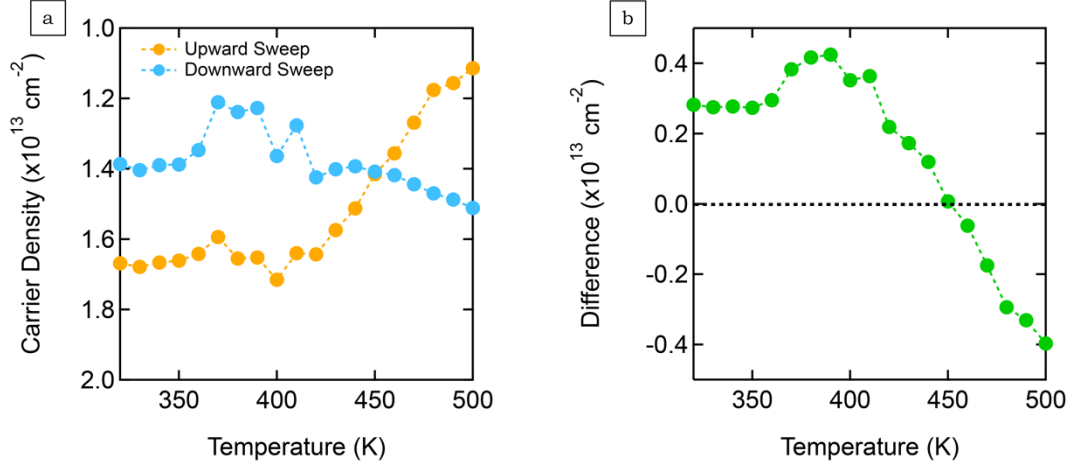


Figure 2.19: Ferroelectric-to-dielectric transition of BaTiO₃ thin films. (a) Charge modulation during downward and upward voltage sweeps as a function of temperature. **(b)** The difference in charge modulation during upward and downward sweeps as a function of temperature. Up to 400 K, the C - V characteristics are completely anti-clockwise. Above 400 K, the hysteresis shows a mixture of clockwise and anti-clockwise hysteresis and results in a smaller charge modulation difference. Above 450 K, clockwise hysteresis starts to dominate, and at 500 K, the hysteresis is entirely clockwise, suggesting a Curie temperature between 450 K and 500 K.

By integrating the C - V curves, we can calculate the carrier modulation, as shown in **Fig. 2.18** with dashed lines. **Figure 2.19** summarizes the carrier modulation during upward and downward voltage sweeps and their differences as a function of temperature. Up to 450 K, the anti-clockwise hysteresis dominates, and that is why we can see higher carrier modulation during downward voltage sweep. Above this temperature, the effect of ferroelectric gating

wanes out, and clockwise hysteresis due to traps starts to dominate. That is why we cannot observe any switchable polarization charges above 450 K. This study suggests that the Curie temperature of our epitaxial BaTiO₃ films is between 450 K and 500 K. Further study is needed to understand the impact of compressive stress-induced ferroelectricity enhancement in BaTiO₃ thin films on FET characteristics.

2.4 Conclusion

In summary, we demonstrated that switchable polarization can be stabilized in a thin, epitaxial BaTiO₃ film. Moreover, we have successfully integrated ferroelectric BaTiO₃ on a high density-of-state semiconductor. The ferroelectricity of BaTiO₃ depletes the carriers from the SrTiO₃ channel. BaTiO₃/SrTiO₃ devices, such as capacitors and FETs, exhibited anti-clockwise hysteresis, a signature of the ferroelectric nature of BaTiO₃. Moreover, experiments suggest that compressive strain not only enhances ferroelectricity but also increases Curie temperature. Lack of conduction band offset and low carrier mobility in the SrTiO₃ channel limit the performances of BaTiO₃/SrTiO₃ FETs. Although SrTiO₃ channel can match the polarization charge because of its high density-of-states, the channel fails to match the capacitance, which is necessary for a NCFET. Moreover, polarization switching is essential to achieve negative capacitance across the ferroelectric layer. The conduction band alignment of BaTiO₃/SrTiO₃ heterostructure prevents applying a large positive gate voltage required for polarization switching. This study demonstrates that BaTiO₃/SrTiO₃ heterostructure is not suitable for NCFET operation. Channel with high electron mobility and higher electron affinity should allow BaTiO₃ gated FETs to drive high on-current and complete switching of polarization direction necessary for NCFET operation. BaSnO₃ is such a material with higher

electron mobilities and a large conduction band offset with BaTiO₃. In the next chapter, we discuss the epitaxial growth of BaSnO₃ and the integration of BaTiO₃ on the BaSnO₃ channel.

Chapter 3

Epitaxial Growth of High Mobility Perovskite Oxide Barium Stannate for Power Devices

The previous chapter detailed the electronic properties and different electronic applications of $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructures. From the device engineering point of view, this particular heterostructure has several issues. For example, a doped SrTiO_3 layer was used as a conductive channel. The extreme low room temperature electron mobilities of the SrTiO_3 channel make this heterostructure impractical for high-performance electronic applications. The low carrier mobilities result in low current densities and high series resistances, which are undesirable properties for any electronic device. Furthermore, the lack of a conduction band offset between BaTiO_3 and SrTiO_3 , which results in a significant gate leakage at positive gate bias, makes the design of the electronic device very challenging. Large positive voltage is essential to switch the polarization of the BaTiO_3 layer in the FeFETs and NCFETs. To overcome these issues, new channel materials with high carrier mobilities and favorable conduction band offset with BaTiO_3 are needed to design all-perovskite oxide heterostructure-based electronic devices for different logic and memory applications. BaSnO_3 is an excellent example of such a material, which fulfills both of these requirements. As mentioned in **Chapter 1**, bulk single-crystal BaSnO_3 has a carrier mobility over $300 \text{ cm}^2/\text{Vs}$. Moreover, density functional theory calculations show that the conduction band offset between BaSnO_3 and SrTiO_3 (or BaTiO_3) is around 1 eV [92].

Prof. Susanne Stemmer's group at UCSB has been working on the epitaxial growth of BaSnO_3 thin films using molecular beam epitaxy (MBE) for several years. Prior to my involvement in this project, Santosh Raghavan and Timo Schumann developed a process of epitaxial growth of BaSnO_3 thin films using MBE. They reported electron mobility of $150 \text{ cm}^2/\text{Vs}$ in BaSnO_3 thin film at room temperature, the highest for any BaSnO_3 thin film at the publication time [93]. While their studies focused on the growth of BaSnO_3 thin films on SrTiO_3 and PrScO_3 substrates, this study focuses on the growth of BaSnO_3 thin films on DyScO_3 substrates. This chapter delves into the epitaxial growth conditions of BaSnO_3 thin films and their impact on the morphology and electrical properties of the films. In addition, it discusses BaSnO_3 -based heterostructures for different device applications.

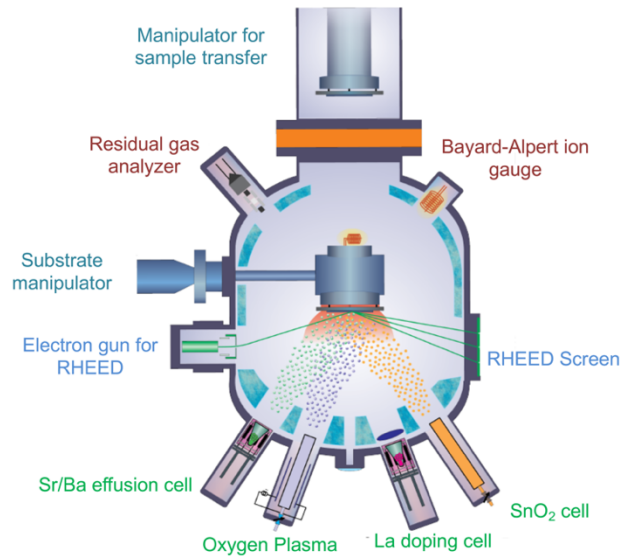


Figure 3.1: Schematic diagram of a molecular beam epitaxy chamber. The system is equipped with Ba, SnO_2 cells, and oxygen plasma source to grow BaSnO_3 thin films. The system has a La effusion cell to dope the films. An RHEED system is also installed for an *in-situ* characterization.

3.1 Plasma Assisted Modified MBE Growth of BaSnO₃ Thin Films

This study examines the stoichiometry of BaSnO₃ thin films that are grown in MBE. A schematic diagram of the MBE system used for this study is shown in **Fig. 3.1**. The setup of the MBE system is as follows. In this system, highly pure Ba and SnO₂ (Sigma Aldrich) are evaporated using solid source cells. The SnO₂ cell temperature is varied from 1070 °C to 1285 °C to achieve a beam equivalent pressure (BEP) of $\sim 5 \times 10^{-7}$ Torr. The Ba cell temperature is varied from 560 °C to 620 °C to achieve desired Ba flux. Typical BEP of Ba flux is low 10^{-8} Torr. Activated oxygen is provided during the growth using an oxygen plasma source. RF plasma power of 300 W is used to supply oxygen plasma during the growth with BEP $\sim 1 \times 10^{-5}$ Torr. The substrates are annealed under this oxygen plasma condition for 20 minutes at the growth temperature before the growth. Likewise, the samples are cooled down under the very same oxygen plasma condition after the growth. Furthermore, highly pure La (Sigma Aldrich) is evaporated from a solid source effusion cell to provide n-type dopants in the films. For all the samples of this study, the La cell temperature is kept at 1275 °C. Substrate temperatures are monitored using an IR pyrometer (Iacon Modline-3), and the flux BEPs are measured using a beam flux measurement system. 350 nm Mo is deposited at the back surfaces of the substrates to have an excellent thermal contact between the substrate heater and the substrates. Usually, Ta back metal is used for the epitaxial growth of other perovskite oxides, such as SrTiO₃, GdTiO₃, etc. Since BaSnO₃ films are grown under high oxygen plasma BEP, Mo back metal is used in this study for its better resistance against oxidation. Nonetheless, the back metal still oxidizes during growth and makes it challenging to maintain a constant substrate temperature. Consequently, the substrate heater is kept at constant output power mode, instead of constant temperature mode, during the growths to mitigate this issue. The stoichiometry, morphology,

and structural quality are studied using *in-situ* monitoring of reflection high-energy electron diffraction (RHEED) and *ex-situ* x-ray diffraction (XRD). Moreover, Physical Property Measurement System (Quantum Design Dynacool) is used to extract the transport properties of the samples.

Although highly pure metals are usually evaporated to supply cations in conventional MBE, in this study, SnO₂ is used instead of Sn metal. At an earlier phase of this project [93, 188], our group used Sn to grow BaSnO₃. Due to the low melting point of Sn (232 °C), sufficient vapor pressure was achievable by evaporating solid Sn in an effusion cell. Nonetheless, a fraction of the Sn flux consumed all activated oxygen to form volatile Sn and the rest of the Sn that was not oxidized formed droplets at the surface [93, 94]. One solution to this problem is to increase the concentration of activated oxygen by increasing the RF power of the plasma source or using ozone [93]. Such an increase in activated oxygen, however, leads to a significant reduction of the lifetime of the filaments and gauges in the MBE chamber due to high rate of oxidation. Besides, high concentration of the activated oxygen also increases the oxidation of the back metal. Another solution is to increase substrate temperature. Although substrate temperature prevents the formation of Sn droplets, it also reduces the incorporation of Sn into the films [93]. A similar problem has already been observed and reported for SnO₂ growths [94,95]. Our group has also tried a metal-organic precursor, tin tetra-butoxide (SnTB), to provide pre-oxidized Sn [188]. Nevertheless, SnTB decomposed into SnO₂ and other organic byproducts even before reaching the MBE growth chamber [188].

All these challenges led to our current modified MBE approach where we supply pre-oxidized Sn from a SnO₂ powder source to mitigate droplet or decomposition issues. This approach also helps to keep the growth temperature and the oxygen pressure reasonable. At a sufficiently high effusion cell temperature (mentioned above), SnO₂ powder sublimates in the form of SnO_x [93] with a reasonable BEP $\sim 5 \times 10^{-7}$ Torr. SnO_x flux coupled with activated oxygen allows the oxidation of Sn to Sn⁺⁴ [188] and thus leads to the epitaxial growth of BaSnO₃.

3.2 MBE Growth of BaSnO₃ Thin Films on DyScO₃ Substrates

As discussed in **Chapter 1**, no substrate that has lattice mismatch with BaSnO₃ below 2% is commercially available. Therefore, BaSnO₃ thin films have to grow with a significant lattice mismatch. Prior to my involvement, the focus of this project was to grow BaSnO₃ thin films on SrTiO₃ and PrScO₃ substrate. SrTiO₃ is a cubic perovskite oxide with a lattice parameter of 3.905 Å [22] that results in a lattice mismatch of 5.1% with bulk single-crystal BaSnO₃. PrScO₃ has an orthorhombic crystal structure with a pseudo-cubic lattice parameter of 4.02 Å, which results in a 2.3% lattice mismatch with BaSnO₃. Despite these significant lattice mismatches, our group has demonstrated relatively high electron mobility in BaSnO₃ thin films. The reported room-temperature electron mobilities were 125 cm²/Vs and 150 cm²/Vs grown on SrTiO₃ and PrScO₃ substrates, respectively [93]. Nonetheless, the lack of availability and twinning issue of PrScO₃ and significant lattice mismatch of SrTiO₃ make these substrates unsuitable for stoichiometric growth studies of BaSnO₃ thin films. As a result, this study, DyScO₃ substrates (MTI) are used to understand the growth stoichiometry of BaSnO₃ thin films.

DyScO₃ has an orthorhombic crystal structure with $a=5.44$ Å, $b=5.71$ Å, and $c=7.89$ Å [96]. DyScO₃ substrates have smaller lattice mismatch with BaSnO₃ compared to SrTiO₃ and are readily available. Two different DyScO₃ substrates have been used– DyScO₃ (001) and DyScO₃ (110) substrates. DyScO₃ (001) forms a pseudo-cubic unit cell with two edges at the substrate surface along orthorhombic $\langle 110 \rangle$ and $\langle \bar{1}10 \rangle$. This pseudo-cubic unit cell has a lattice parameter of 3.938 Å, which results in a lattice mismatch of 4.3%. The angle between orthorhombic $\langle 110 \rangle$ and $\langle \bar{1}10 \rangle$ is 87.22°, slightly lower than 90°. The DyScO₃ (110) substrate has orthorhombic pattern at the surface with edges along $\langle 001 \rangle$ and $\langle \bar{1}10 \rangle$, with lattice parameters of 3.945 Å and 3.938 Å along with these directions, respectively.

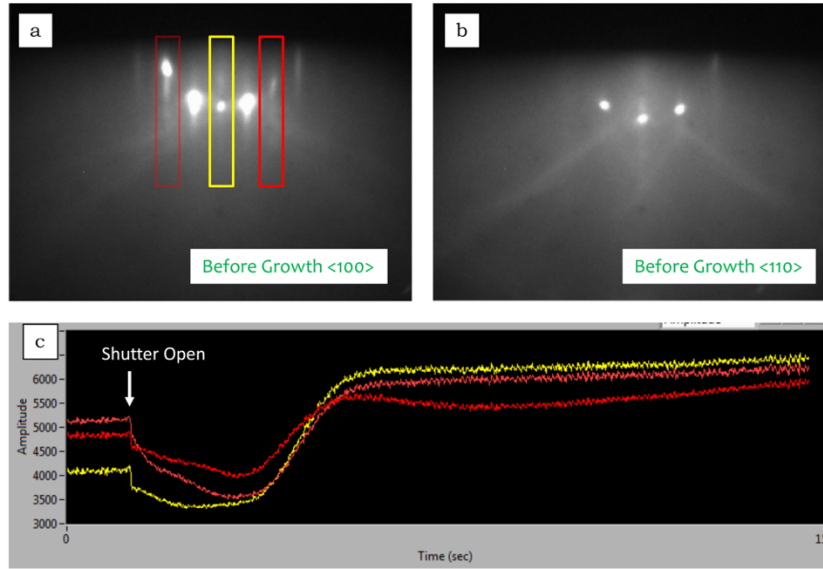


Figure 3.2: *In situ* RHEED characterization. Pre-growth RHEED images taken along (a) $\langle 100 \rangle$ and (b) $\langle 110 \rangle$ directions. (c) RHEED intensities of different diffraction peaks indicated by colored boxes in (a) as a function of time. The drop in intensities immediately after the opening of the shutter is due to island growth mode. The intensity increases when those islands or domains coalesce. Lack of RHEED oscillation indicates no layer-by-layer growth mode.

3.2.1. BaSnO₃ Thin Films on DyScO₃ (001) Substrates

First, we investigated the epitaxial growth of BaSnO₃ thin films on DyScO₃ (001) substrates. BaSnO₃ thin films were grown on DyScO₃ (001) substrates in MBE using the same growth process described in **Section 3.1**. All the films were grown for 90 minutes. The first 30 minutes of the growths were undoped, whereas the La effusion cell shutter was open for later 60 minutes. A schematic diagram of a BaSnO₃ thin film is shown in **Fig. 3.4(a)**.

Figures 3.2 and **3.3** show the RHEED images of a typical BaSnO₃ thin film during different stages of growth. **Figures 3.2(a)** and **3.2(b)** present the RHEED images just before the start of the growth along $\langle 100 \rangle$ and $\langle 110 \rangle$ directions, respectively. Nice streaky RHEED patterns suggest a smooth surface quality of the substrate. *Ex-situ* surface treatment and annealing were carried out on the substrates to ensure stepped and smooth surface of the substrates. The detailed procedure of the surface treatment is discussed in the **Appendix**. Additionally, the substrate was *in-situ* annealed at the growth temperature and oxygen plasma ambient for 20 minutes just before the growth, as discussed earlier. These *in-situ* and *ex-situ* treatments ensure excellent surface quality suitable for epitaxial growth, evident in the RHEED images. **Figure 3.2(c)** displays the intensities of three Laue diffraction peaks, indicated by three rectangular boxes in **Fig. 3.2(a)**, as a function of time. The RHEED intensities drop immediately after the growth starts. After around 1 minute, the intensities start to increase. Besides, this image exhibits no time-dependent RHEED oscillations, confirming the absence of layer-by-layer growth. **Fig. 3.3** reveals the reason behind the collapse in RHEED intensities at the beginning of the growth. **Figure 3.3(a)** and **3.3(b)** illustrate the RHEED images along $\langle 100 \rangle$ direction taken 1 minute and 2 minutes into the growth, respectively. Immediately after the growth starts,

the RHEED pattern became slightly spotty, as shown in **Fig. 3.3(a)**. This spottiness reduces the RHEED intensities. Spotty RHEED pattern immediately after the start of the growth suggests a 3D growth mechanism. These 3D islands coalesce quickly and form a smoother surface, verified by a streaky RHEED pattern shown in **Fig. 3.3(b)**. As shown in **Fig. 3.3(c,d)**, post-growth RHEED images exhibit streaky patterns, suggesting the excellent surface quality of the BaSnO₃ thin film.

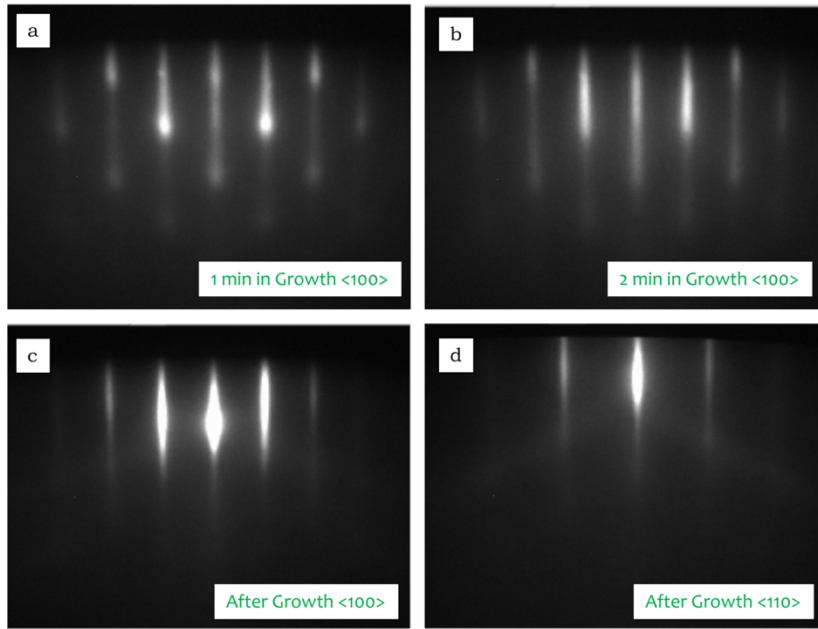


Figure 3.3: Evolution of RHEED during growth. RHEED images of $\langle 100 \rangle$ direction taken at **(a)** 1 minute and **(b)** 2 minutes into the growth. Spotty RHEED indicates initial island growths. The RHEEDs, however, become streaky within 2 minutes, suggesting a smoother surface. Steaky post-growth RHEED along **(c)** $\langle 100 \rangle$ and **(d)** $\langle 110 \rangle$ directions.

To understand the growth mechanism of BaSnO₃ thin films, several growth parameters were varied to alter the growth conditions. One of the critical variables is the ratio of SnO_x and Ba fluxes. Although SnO_x flux was kept constant for all the growths, there was slight day-to-day variation in SnO_x flux. The Ba cell temperature was adjusted to vary SnO_x/Ba flux ratio, and beam flux measurement was used to determine Ba flux. Moreover, the growth temperature was also varied to figure out an optimum growth condition. Nonetheless, due to back metal oxidation, maintaining a constant substrate temperature during the growth of BaSnO₃ was challenging. Due to the high-temperature growth and significant oxygen plasma pressure, the back metal oxidizes during the growth and makes a poor thermal contact. As a result, there is a gradual fall in the actual substrate temperature during the growth. Therefore, heater filament was kept at a constant output power mode instead of constant output temperature to address this issue. This study has used two different output powers – 432 watts (36% output power) and 456 watts (38% output power).

Figures 3.4(b) and 3.4(c) present the 2θ-ω XRD scans for different BaSnO₃ thin films growth with substrate heater output power of 36% and 38%, respectively. The number printed with each scan indicates the corresponding SnO_x/Ba flux ratio. All of the XRD scans exhibit both substrate (DyScO₃) (004) and BaSnO₃ (002) peaks. Additionally, the XRD scans show nice thickness fringes, signifying excellent interface quality and uniform thicknesses of the films. Thickness fringes change with the SnO_x/Ba flux ratio. This variation in thickness fringes suggests that even though all films were grown for the same amount of time, the film thicknesses are dependent on the SnO_x/Ba flux ratio.

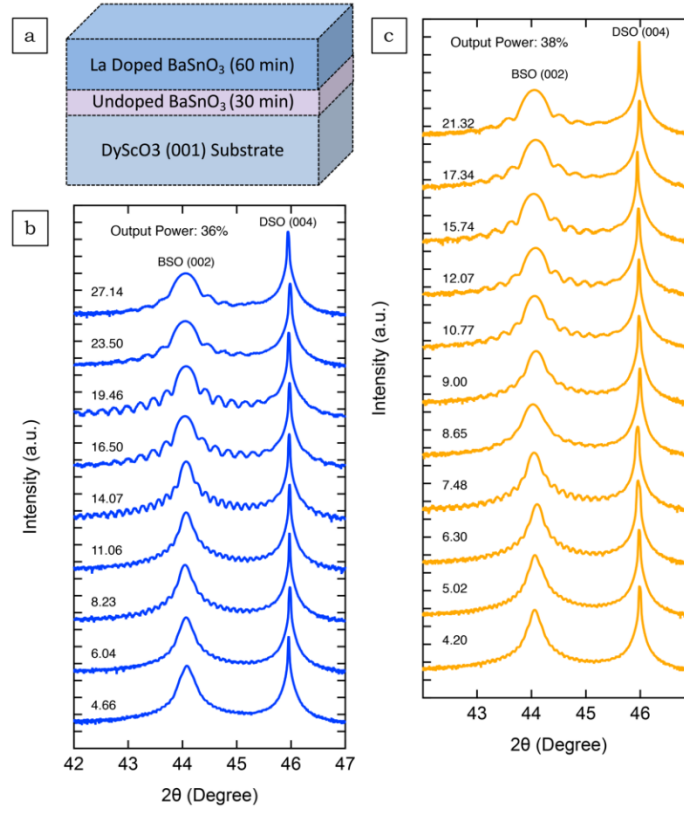


Figure 3.4: X-ray diffraction of BaSnO₃ thin films grown on DyScO₃ (001) substrates. (a) A schematic diagram of epitaxial structures of BaSnO₃ thin films grown on DyScO₃ (001) substrates. The films were grown for 90 minutes, where the first 30 minutes were grown undoped, followed by 60 minutes La-doped layers. High-resolution 2θ-ω x-ray diffraction scans of BaSnO₃ (BSO) films grown on DyScO₃ (DSO) substrates with substrate filament power of **(b)** 36% and **(c)** 38%.

3.2.2 Ba Flux-Limited Growth of BaSnO₃ Thin Films

From the thickness fringes of the XRD scans shown in **Fig. 3.4(b,c)**, the thicknesses of the BaSnO₃ thin films can be calculated using the following equation –

$$Thickness = \frac{\lambda}{\Delta(2\theta)\cos(\theta_m)} \dots \dots \dots (3.1)$$

where λ is the wavelength of the x-ray (1.54 Å for Cu K- α x-ray), $\Delta(2\theta)$ is the periodicity of the thickness fringes, and θ_m is the half of the angle where the BaSnO₃ (002) peak occurs.

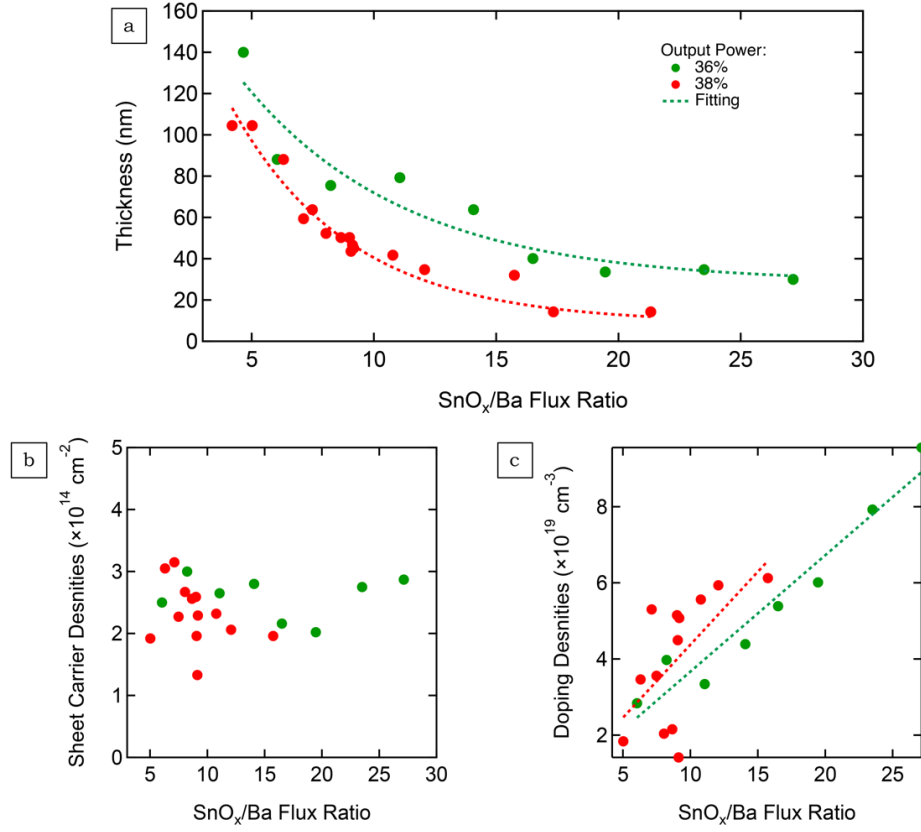


Figure 3.5: Ba flux-limited growth of BaSnO₃ thin films. (a) Thicknesses of BaSnO₃ thin films as a function of SnO_x/Ba flux ratio. The drop in film thicknesses at a higher flux ratio suggest Ba flux-limited growth of BaSnO₃ thin films. (b) 2D sheet carrier densities and (c) 3D doping densities as a function of SnO_x/Ba flux ratio. Flux ratio-dependent growth rate and constant La flux increase 3D doping densities in the films. The red and green data points indicate the sample grown with a filament output power of 38% and 36%, respectively.

The thicknesses of the BaSnO₃ thin films grown at different growth conditions are extracted using **Eqn. 3.1**, and are shown in **Fig. 3.5(a)**, as a function of the SnO_x/Ba flux ratio. The green and red data points indicate the substrate heater power of 36% and 38%, respectively. The figure shows an exponential decay in film thicknesses with flux ratio. As the SnO_x flux was kept almost constant, lower thickness at a higher flux ratio indicates Ba flux-limited growth. Higher SnO_x/Ba flux ratio means lower Ba flux, and as the growth is Ba flux-limited, the growth rate declines at a higher flux ratio. Moreover, the samples grown at higher output power show smaller thicknesses for a similar flux ratio. This could be due to a higher decomposition rate at a higher growth temperature associated with higher output power. As La flux was not changed during the growths and all films were grown for 90 minutes, there are no significant variations in 2D sheet carrier densities, as shown in **Fig. 3.5(b)**. Sheet carrier densities of most of the films stay between $2 \times 10^{14} \text{ cm}^{-2}$ to $3 \times 10^{14} \text{ cm}^{-2}$. Since the film thicknesses decrease with SnO_x/Ba flux ratio, 3D doping densities increase linearly with the flux ratio, as shown in **Fig. 3.5(c)**.

Figure 3.6(a) illustrates the transport characteristics of the BaSnO₃ thin films grown on DyScO₃ (001) substrates. The figure shows the electron mobilities in BaSnO₃ thin films as a function of SnO_x/Ba flux. The green and red data points indicate the substrate heater output power of 36% and 38%, respectively. Both data sets follow dome-shaped curves, highlighted by the dashed fitting curves. Although this dome-shaped curve may look like a growth window, a deeper analysis reveals something different. At a lower flux ratio (Ba-rich regime), the mobility is low, suggesting that the Ba-rich growth condition is far from being suitable for transport in BaSnO₃ films. At a very high flux ratio regime, mobilities fall again, but not

because of the stoichiometry of the films. As discussed earlier, the film thicknesses decrease with the flux ratio, and this fall in film thicknesses results in a drop in mobility at a very large flux ratio. As the films grown at higher temperatures have lower thicknesses for a similar flux ratio, the fall in mobility strikes earlier in those films. Nonetheless, the samples grown at higher temperatures exhibit higher carrier mobilities. Higher substrate power (temperature) gives the adatoms higher mobility, which usually results in a better film quality. This might be a reason behind higher carrier mobilities in the sample grown with higher filament output power.

3.2.3 Non-stoichiometric Growth of BaSnO₃ Thin Films

From the BaSnO₃ (002) XRD peaks shown in **Figure 3.4**, we calculate the out-of-plane lattice parameter of BaSnO₃ in the thin films using Bragg's condition for diffraction -

$$2d \sin(\theta_m) = n\lambda \dots \dots \dots (3.2)$$

where λ is the wavelength of the x-ray, θ_m is the half of the angle where the BaSnO₃ (002) peak occurs, d is the distance between (002) planes, and n is the order of reflection ($n = 2$ for (002) planes). **Figure 3.6(b)** presents the lattice parameters of BaSnO₃ in the thin films grown at different growth conditions extracted from the XRD scans. The dashed line indicates the bulk lattice parameter for BaSnO₃. The figure shows a considerable variation in out-of-plane lattice parameters. This variation suggests a lack of self-limiting stoichiometry in the BaSnO₃ films. Nevertheless, this non-stoichiometry does not correlate with carrier mobility. This lack of correlation implies the presence of other dominating mobility-limiting mechanisms in BaSnO₃ thin films.

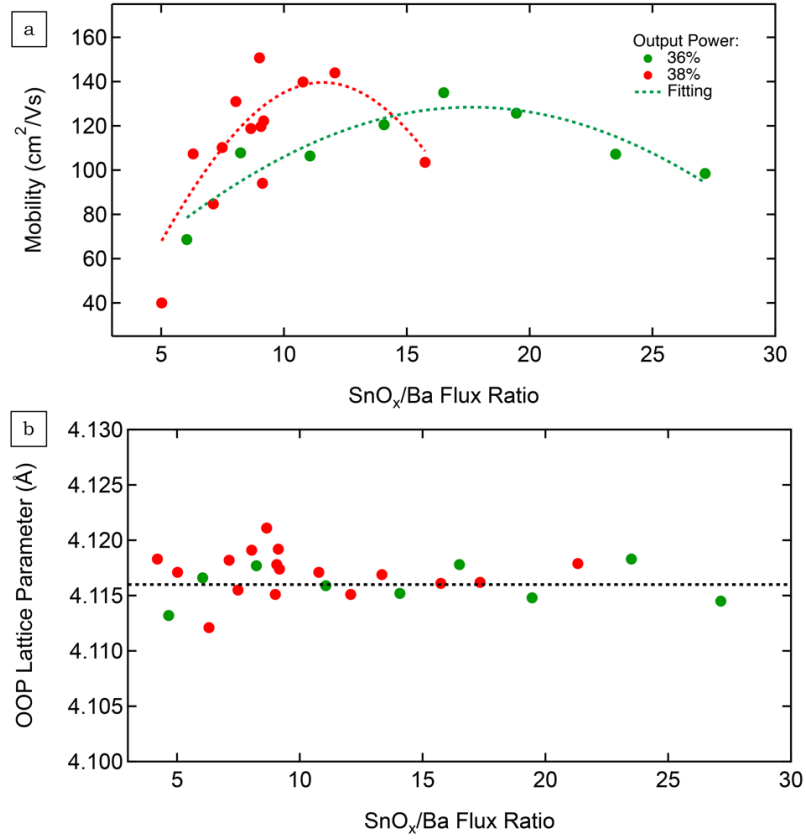


Figure 3.6: Electronic transport and stoichiometry of BaSnO₃ thin films. (a) Electron mobility in BaSnO₃ thin films. Lower growth rate and pits in samples grown at a high flux ratio degrade electron mobilities. Moreover, Ba-rich samples exhibit lower electron mobilities. Higher substrate temperature enhances electronic transport in BaSnO₃ thin films. **(b)** Out-of-plane lattice parameters of BaSnO₃ thin films. The measured lattice parameters are scattered around the bulk lattice parameter of BaSnO₃ (black dashed line). Lack of constant lattice parameters suggests non-stoichiometric growth of epitaxial BaSnO₃ thin films.

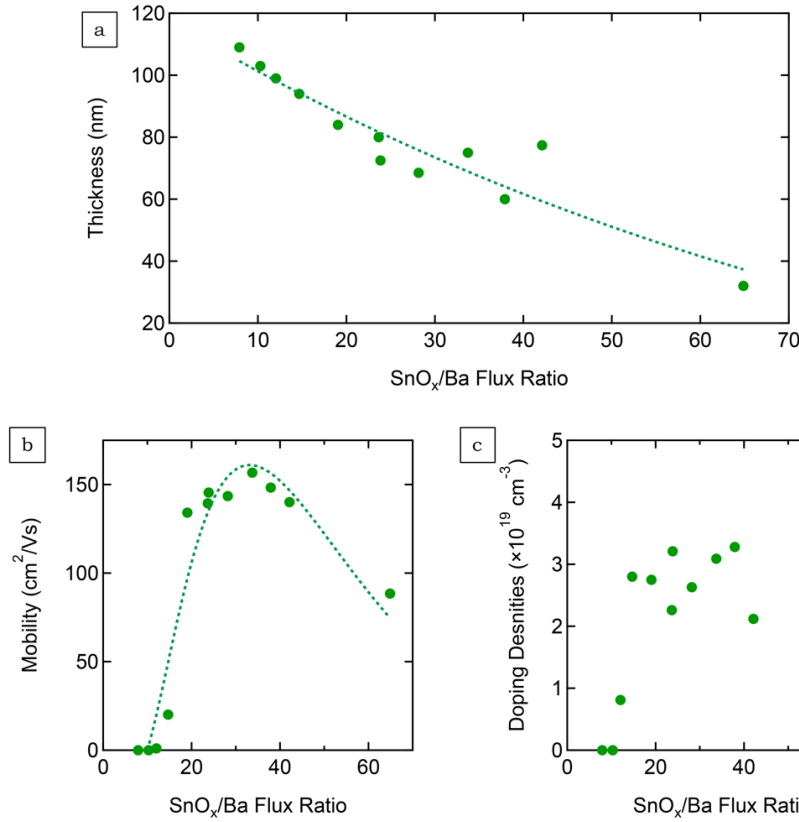


Figure 3.7: Non-linear growth rate of BaSnO₃ thin films. (a) Thicknesses of BaSnO₃ thin films as a function of SnO_x/Ba flux ratio. The growth times were adjusted to make all the films of similar thickness. Yet, there is a significant variation in film thicknesses due to the non-linear growth rate. (b) Electron mobility and (c) 3D doping densities of the films.

3.2.4 Non-linear Growth Rate of BaSnO₃ Thin Films

In this study, there are too many variables that can affect carrier mobilities, such as – film thicknesses, doping densities, flux ratio, among others. To reduce the number of variables, our group member Christopher Freeze has studied a growth series where he has adjusted the growth time to keep the film thicknesses constant. He has used the growth study described earlier to estimate the growth time for his experiments. By keeping the film thickness constant,

the effect of variations in both film thickness and doping density can be eliminated. Even after adjusting the growth time, the thicknesses of the films drop with SnO_x/Ba flux ratio, as shown in **Fig. 3.7(a)**. Because of the extended growth time, the drop in thicknesses is much slower than the previous study. This drop in film thicknesses, even after adjustment of growth times, indicates a non-linear growth rate during a single growth. The growth rate of BaSnO_3 slows down over time during a growth. This non-linear growth rate might be due to the back metal oxidation during the growth. The back metal oxidation changes the substrate temperature gradually and may result in a non-linear growth rate. As the variation in film thicknesses is smaller in this study, these films exhibit dome-shaped mobility curve with a broader region of high mobility (**Fig. 3.7(b)**), and less variation in doping densities (**Fig. 3.7(c)**).

3.2.5 Strain Compensation in BaSnO_3 Thin Films on DyScO_3 (001) Substrates

Figure 3.8(a) shows the plane-view transmission electron microscopy (TEM) image of a BaSnO_3 film grown on a DyScO_3 (001) substrate. The TEM image shows few dark spots. **Figure 3.8(b)** zooms into one of these dark spots, showing the Burger's circuit around the spot. The Burger's circuit indicates that these spots are due to threading dislocations. As explained earlier, RHEED images show island formation at the beginning of the growth and later they coalesce. Those merging could result into these threading dislocations. The TEM analysis demonstrates that the density of these threading dislocations is $3 \times 10^{11} \text{ cm}^{-2}$, which is consistent with literature [97].

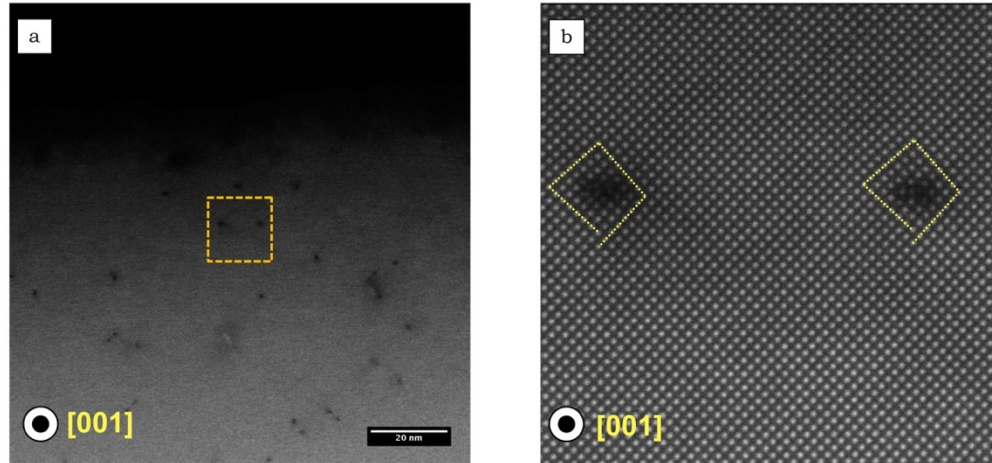


Figure 3.8: In-plane transmission electron microscopy of BaSnO₃ thin films. (a) In-plane TEM images of a BaSnO₃ film show dislocation densities. The TEM image shows a density of threading dislocation of $3 \times 10^{11} \text{ cm}^{-2}$. (b) A zoomed-in TEM image showing Burger circuit around the dislocations. (Image courtesy – Dr. Honggyu Kim)

As discussed earlier, DyScO₃ (001) forms a pseudo-cubic unit cell, with an angle between two edges (corresponding to $\langle 110 \rangle$ and $\langle \bar{1}10 \rangle$ directions) of 87.22° . When the growth initiates with nucleation, some nucleation sites align with $\langle 110 \rangle$, while other sites align with $\langle \bar{1}10 \rangle$. When these nucleation sites merge, there is slight angular misalignment ($\sim 2.7^\circ$) between them. Cross-section TEM images corroborate this hypothesis, as shown in **Fig. 3.9**. These TEM images show multiple domains of BaSnO₃ with different brightness. A domain becomes brighter when the alignment is perfect. The contrast in brightness confirms a small angular misalignment between the domains.

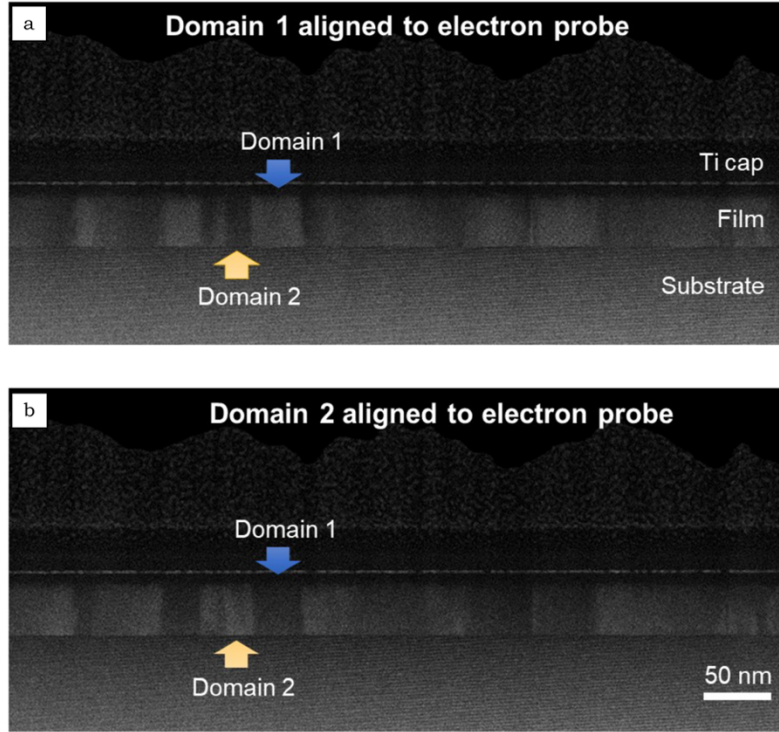


Figure 3.9: Cross-section transmission electron microscopy of BaSnO₃ thin films. Cross-section TEM images of BaSnO₃ films. Because of sheer stress introduced by pseudo-cubic substrates, BaSnO₃ films show different domains with a slight angle between them. The contrast between these domains indicates an angular mismatch. (*Image courtesy – Dr. Honggyu Kim*)

It is worth mentioning that the growth mode of BaSnO₃ is different on DyScO₃ (001) substrates compared to PrScO₃ and SrTiO₃ substrates. On DyScO₃ (001) substrates, the growth mode is island nucleation and merging. In contrast, on PrScO₃ and SrTiO₃ substrates, BaSnO₃ films relax by forming misfit dislocations at the interface [93]. 4.3% lattice mismatch along with 2.7° sheer mismatch might be the origin of this different growth mode on DyScO₃ (001) substrates.

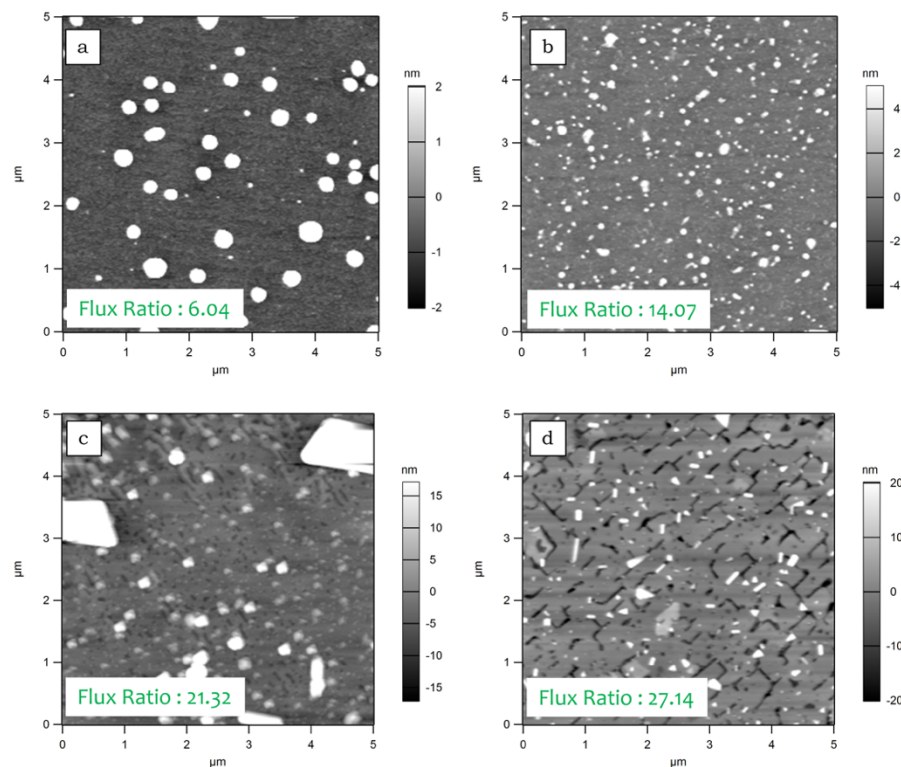


Figure 3.10: Surface morphology of BaSnO₃ thin films. Atomic force microscopy of different BaSnO₃ thin films grown with different flux ratios. Samples grown at a lower flux ratio shows Sn droplets at the surfaces. While a higher flux ratio can eliminate those droplets, it introduces pits in the films.

3.2.6 Surface Morphology of BaSnO₃ Films Grown on DyScO₃ (001)

Substrates

The surface morphology of the BaSnO₃ films grown on DyScO₃ (001) is characterized using atomic force microscopy (AFM). **Figure 3.10** shows the AFM images of BaSnO₃ films grown with different SnO_x/Ba flux ratios and filament output power of 36%. The surfaces of the films grown at a low flux ratio contain Sn droplets (**Fig. 3.10(a,b)**). The density of droplets reduces when the sample is grown at a higher flux ratio (**Fig. 3.10(c,d)**). A higher flux ratio, however,

introduces pits in the films. These pits might be another reason behind the fall in mobility at the higher flux ratio observed in **Fig. 3.6(a)**. The pits can be eliminated by growing the samples at a higher temperature. This might explain the higher carrier mobility observed in the films that were grown with a filament output power of 38%.

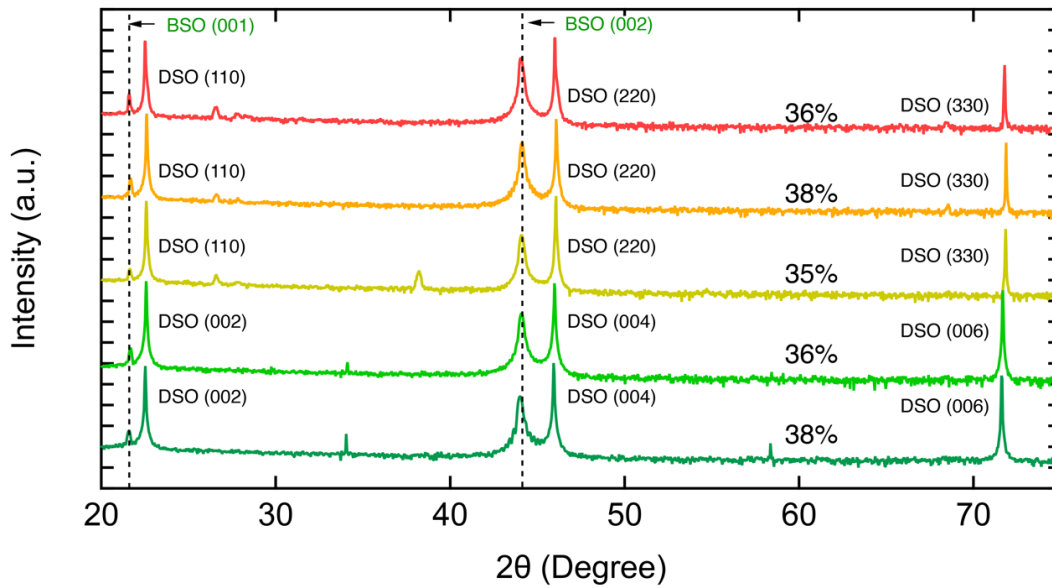


Figure 3.11: Long x-ray diffraction scans of BaSnO_3 thin films. Long 2θ - ω XRD scans of BaSnO_3 (BSO) thin films grown on DyScO_3 (DSO) (001) and (110) substrates with different substrate filament powers.

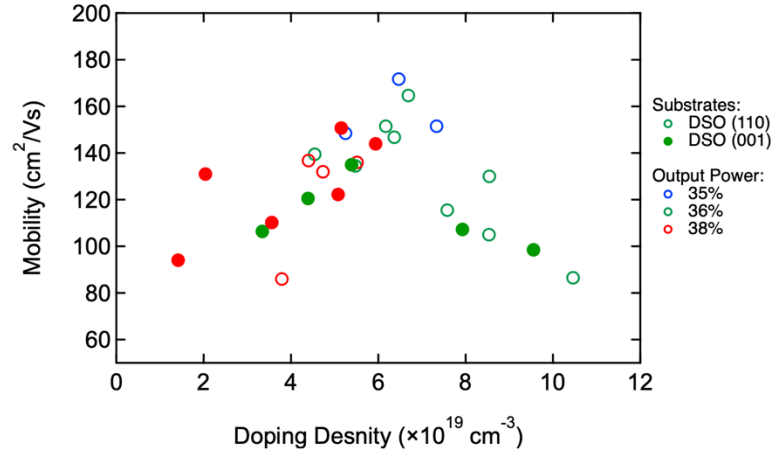


Figure 3.12: Electron mobilities in BaSnO₃ thin films grown on DyScO₃ substrates. Electron mobilities in BaSnO₃ films grown on DyScO₃ (001) and (110) substrates as a function of doping densities. Lack of sheer stress enhances mobilities in samples grown on DyScO₃ (110) substrate. Because of better screening, increased doping densities initially improve the carrier mobilities. Lower film thicknesses degrade the mobilities in the films with very high doping densities.

3.2.7 BaSnO₃ Thin Films on DyScO₃ (110) Substrates

As a part of this experiment, we have also explored the transport properties of BaSnO₃ thin films grown on DyScO₃ (110) substrates. Substrate output power and SnO_x/Ba flux ratio have been varied to improve carrier mobility in BaSnO₃ thin films. **Figure 11** shows the long XRD scans of BaSnO₃ films grown on DyScO₃ (001) and (110) substrates with different filament output power. All the samples show BaSnO₃ (001) and (002) peaks, where (002) peaks are more prominent than (001) peaks. These XRD scans hint about the good structural quality of the films. **Figure 12** summarizes the carrier mobilities of the BaSnO₃ films grown on DyScO₃ (110) substrates and compares them with the films grown on DyScO₃ (001) substrates. The carrier mobilities are plotted as a function of doping densities. Initially, the carrier mobilities increase with doping densities. This dependence of mobility on doping densities is consistent

with the literature [52, 97-102]. Higher doping densities provide better screening from charged defects. The drop in mobilities at higher doping densities is due to the lower thicknesses of the films. Furthermore, the films grown on DyScO₃ (110) substrates show slightly higher carrier mobilities. This enhancement in carrier mobilities might come from the absence of sheer mismatch in DyScO₃ (110) substrates. The maximum mobility measured in a BaSnO₃ thin film is 172 cm²/Vs, grown on DyScO₃ (110) substrate.

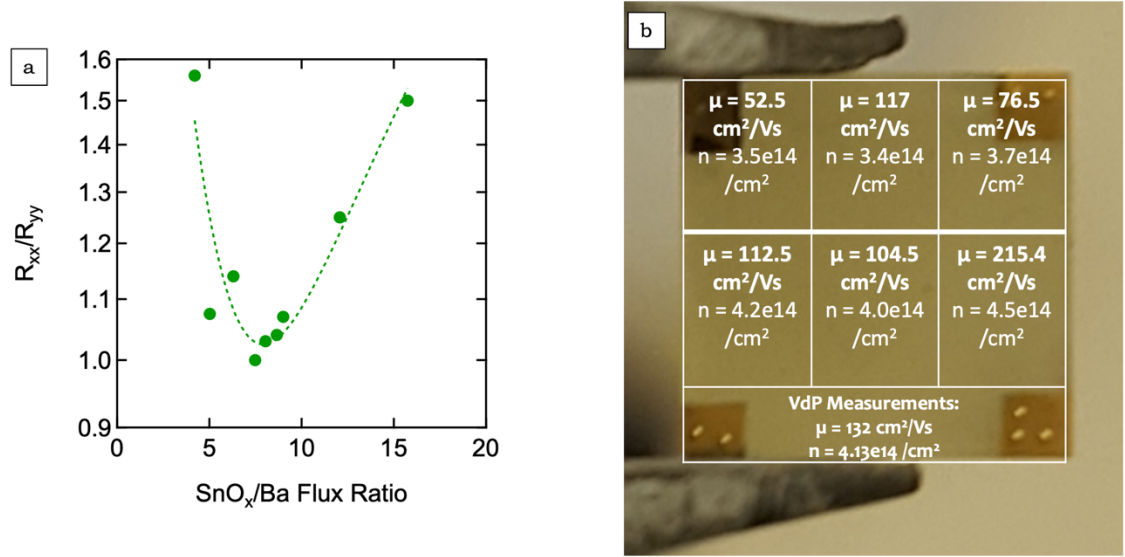


Figure 3.13: Non-uniform electronic transport in BaSnO₃ thin films grown on DyScO₃ substrates. (a) The ratio of R_{xx} and R_{xy} as a function of flux ratio. This plot shows significant variation in R_{xx} and R_{xy} . This variation enhances when the flux ratio is either too low or too high. **(b)** Mobilities and sheet carrier densities measured at different regions of a film using Hall bar structures. The data exhibits a huge variation in carrier mobilities.

3.2.8 Non-uniform Transport in BaSnO₃ Thin Films

Van der Pauw method was used to measure the mobilities in BaSnO₃ films. In the Van der Pauw method, four large metal contacts were deposited at four corners of the square samples.

This method probes the average transport properties of the films. From TEM and AFM analyses, it is evident that BaSnO₃ films grown on DyScO₃ substrates exhibit huge structural non-uniformity. Therefore, a reasonable assumption would be that electronic transport might also display similar non-uniformity. **Figure 3.13(a)** illustrates the ratio of R_{xx} and R_{yy} measured using Van der Pauw. It demonstrates significant non-uniformity in R_{xx} and R_{tt} , especially when SnO_x/Ba flux ratio is either too low or too high. This particular result correlates strongly with the surface morphology and mobilities of the films that have been discussed earlier. To understand more about this non-uniformity in electronic transport, we have fabricated Hall bar structures at different areas of a BaSnO₃ thin film. Afterward, we have measured Hall mobility and sheet carrier densities using these Hall Bar devices. **Figure 3.13(b)** shows a sample with transport data measured at different parts of the sample. The mobility of the sample measured using the Van der Pauw method is 132 cm²/Vs. The mobilities measured using Hall bar structures display a huge non-uniformity and vary from 52 cm²/Vs to 215 cm²/Vs. Non-uniformity in structural quality might have caused this considerable non-uniformity in transport properties. There is, however, no significant variation in sheet carrier densities, suggesting a uniform incorporation of doping atoms.

Figure 3.14 summarizes the carrier mobilities of this study and compares them with the same in the existing literature [52,93,97-102]. The highest mobilities observed in this study are 172 cm²/Vs and 215 cm²/Vs using Van der Pauw and Hall bar methods, respectively. 215 cm²/Vs is the highest carrier mobility measured in any BaSnO₃ thin film.

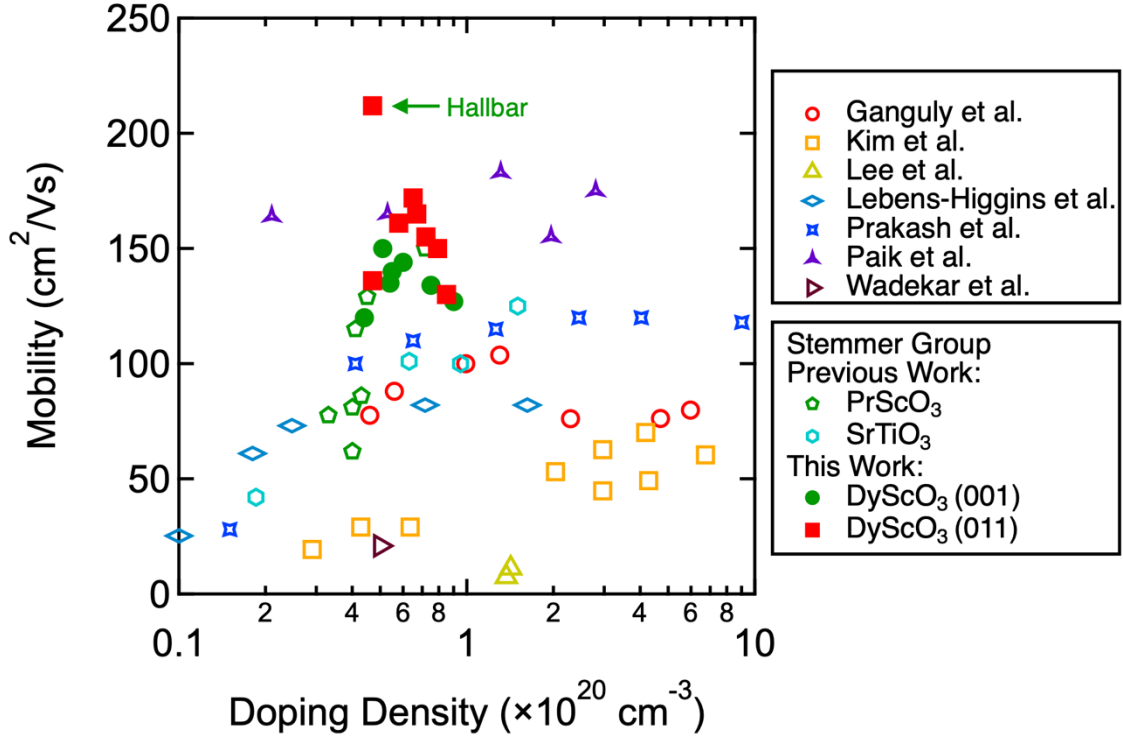


Figure 3.14: Electron mobilities in BaSnO₃ thin films. Summary of electron mobilities in BaSnO₃ thin films. This plot compares our results with other mobilities reported in the literature [52, 93, 97-102].

3.3 BaTiO₃/BaSnO₃ Heterostructure

The focus of the experimental work then shifted to grow BaTiO₃/BaSnO₃ heterostructures for different device applications after optimizing the MBE growth of BaSnO₃ thin films. BaTiO₃/BaSnO₃ heterostructures were grown on SrTiO₃ substrates. **Figure 3.15(a)** presents a schematic diagram of a BaTiO₃/BaSnO₃ heterostructure. **Figure 3.15(b)** and **3.15(c)** show short and long XRD scans, respectively. Both figures exhibit BaSnO₃ and BaTiO₃ peaks, along with substrate peaks. **Fig. 3.15(b)** reveals a right shift in BaTiO₃ (002) peaks, compared to the bulk lattice parameter indicated by red dashed lines. This right shift indicates biaxial tensile

stress on BaTiO₃ films. As BaTiO₃ has smaller lattice parameters ($a = b = 3.992 \text{ \AA}$, $C = 4.036 \text{ \AA}$) compared to that of BaSnO₃ ($4.116 \text{ \AA}$), a large tensile stress is expected.

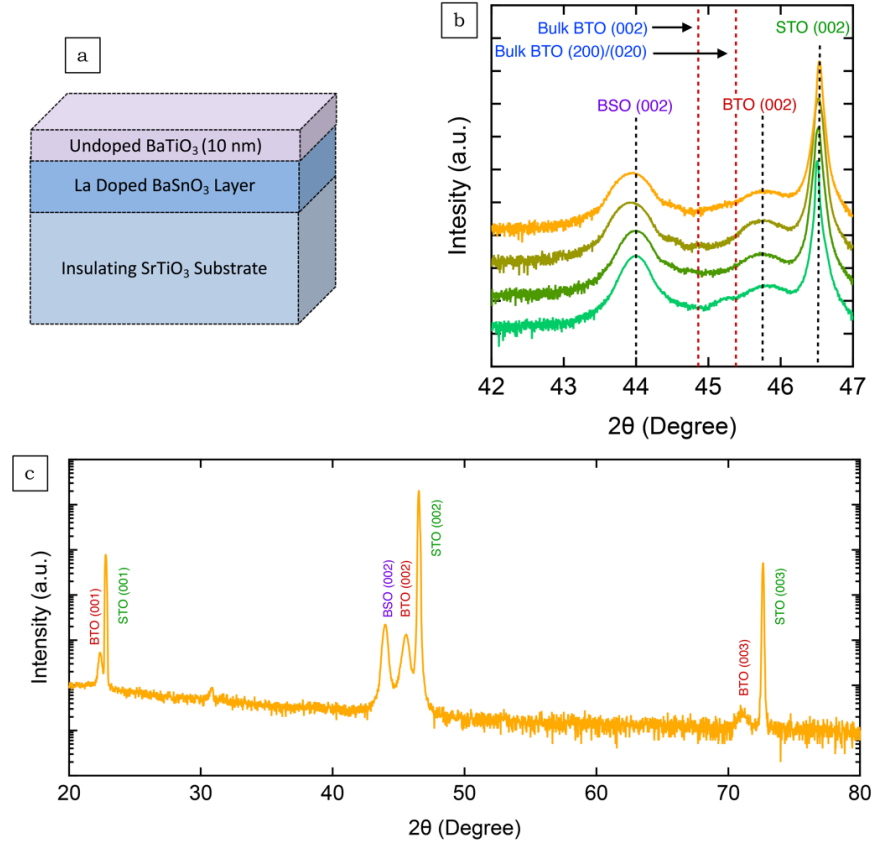


Figure 3.15: BaTiO₃/BaSnO₃ heterostructure. (a) A schematic diagram of the epitaxial structure of BaTiO₃/BaSnO₃ heterostructure. (b) High-resolution short and (c) Long 2θ - ω XRD scans of the heterostructures. High-resolution XRD scans show tensile stress on BaTiO₃ layers.

3.3.1 Current-Voltage and Capacitance-Voltage Characteristics in BaTiO₃/BaSnO₃ Heterostructure

Besides growing and characterizing BaTiO₃/BaSnO₃ heterostructures, we fabricated and studied two-terminal devices to characterize current-voltage (I - V) and capacitance-voltage (C -

I-V characteristics of the BaTiO₃/BaSnO₃ heterostructures. The BaSnO₃ channel was 35 nm thick with a doping density of $6 \times 10^{19} \text{ cm}^{-3}$, while the BaTiO₃ cap layer was 10 nm thick. Moreover, a reference SrTiO₃/BaSnO₃ heterostructure was also grown and fabricated for comparison. Due to the significant lattice mismatch between BaSnO₃ and SrTiO₃ (>5%), the gate leakage was extremely high in 10 nm SrTiO₃ capped devices. So, another SrTiO₃/BaSnO₃ reference sample was grown with a SrTiO₃ capped layer of 60 nm. Agilent B1500A semiconductor parameter analyzer was used for *I-V* and *C-V* characterizations. A similar process recipe, discussed in **Chapter 2**, was used to fabricate the devices.

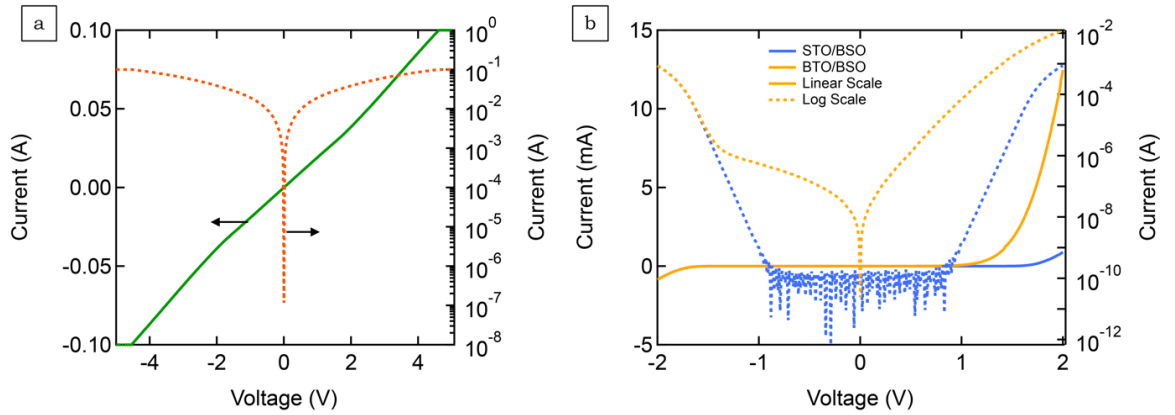


Figure 3.16: Current-voltage characteristics in BaTiO₃/BaSnO₃ heterostructure. (a) Ohmic and (b) Schottky *I-V* characteristics of BaTiO₃/BaSnO₃ (BTO/BSO) heterostructures.

Figure 3.16(a) shows the *I-V* characteristics between two Ohmic contacts, and it shows a linear *I-V* characteristic with large current densities. **Figure 3.16(b)** presents the Schottky currents of the devices fabricated on BaTiO₃/BaSnO₃ and reference samples. As the SrTiO₃ cap layer was thicker in the reference sample, devices in the reference sample exhibit a lower leakage current.

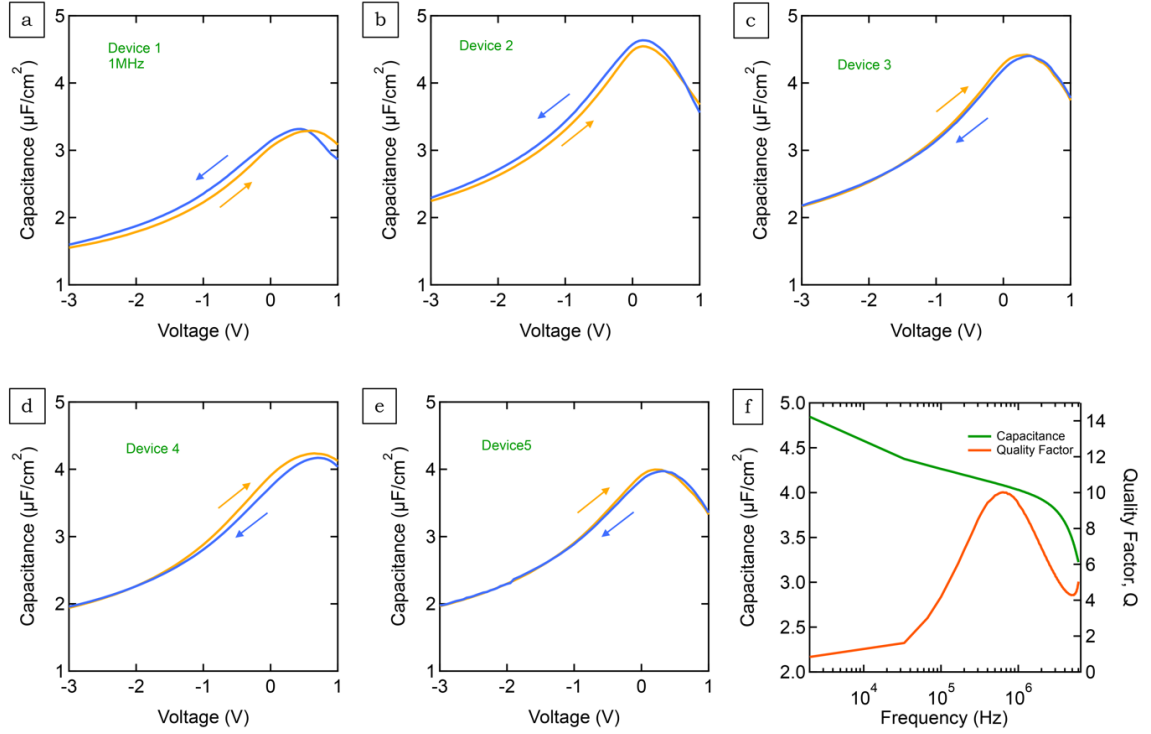


Figure 3.17: Capacitance-voltage characteristics in BaTiO₃/BaSnO₃ heterostructure. (a)-(e) C - V characteristics of different devices fabricated on BaTiO₃/BaSnO₃ (BTO/BSO) heterostructures. The C - V characteristics exhibited no consistent hysteresis. **(f)** Capacitance and quality factors measured at different frequencies. High gate leakages limit the performances at the low-frequency regime.

Figure 3.17(a-e) shows the C - V characteristics of different capacitor devices fabricated on BaTiO₃/BaSnO₃ heterostructure measured at 1 MHz. Surprisingly, unlike BaTiO₃/SrTiO₃ devices, there is no consistent anti-clockwise hysteresis in devices fabricated on BaTiO₃/BaSnO₃ heterostructures. These C - V characteristics exhibit both clockwise and anti-clockwise hysteresis. This inconsistency in hysteresis suggests that the ferroelectric polarization is not aligned along the out-of-plane direction. As the lattice parameter of BaSnO₃ is much larger than the long side of the BaTiO₃ unit cell, the ferroelectricity of the BaTiO₃

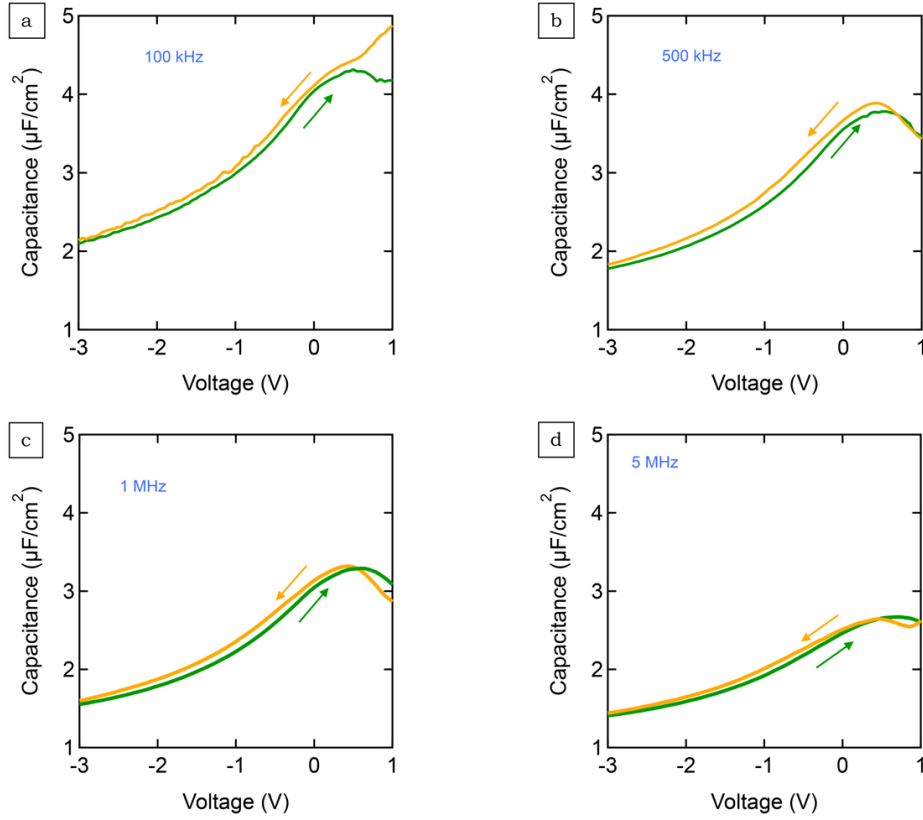


Figure 3.18: Capacitance-voltage characteristics in control SrTiO₃/BaSnO₃ heterostructure. C - V characteristics of device fabricated on SrTiO₃/BaSnO₃ heterostructures measured at **(a)** 100 kHz, **(b)** 500 kHz, **(c)** 1 MHz and **(d)** 5 MHz.

layer is likely to align along parallel to the plane. The suppression of ferroelectricity due to sizeable tensile stress might be another possibility. **Chapter 2** discusses how the lattice deformation of BaTiO₃ suppresses ferroelectricity and induces a ferroelectric to paraelectric transition. The further structural study is required to understand the ferroelectric nature of the BaTiO₃ layer in the BaTiO₃/BaSnO₃ heterostructures. **Figure 3.17(f)** shows the frequency dependence of capacitance and quality factor. The poor quality factor at a low-frequency regime (<100 kHz) is due to the gate leakage. BaTiO₃/BaSnO₃ devices exhibit better high-frequency performance than BaTiO₃/SrTiO₃ devices discussed in the previous chapter. This

improvement is due to higher mobility and sheet carrier density in BaTiO₃/BaSnO₃ heterostructures. The reference sample capacitors exhibit expected small clockwise hysteresis, suggesting a low density of traps at the interface (**Fig. 3.18**).

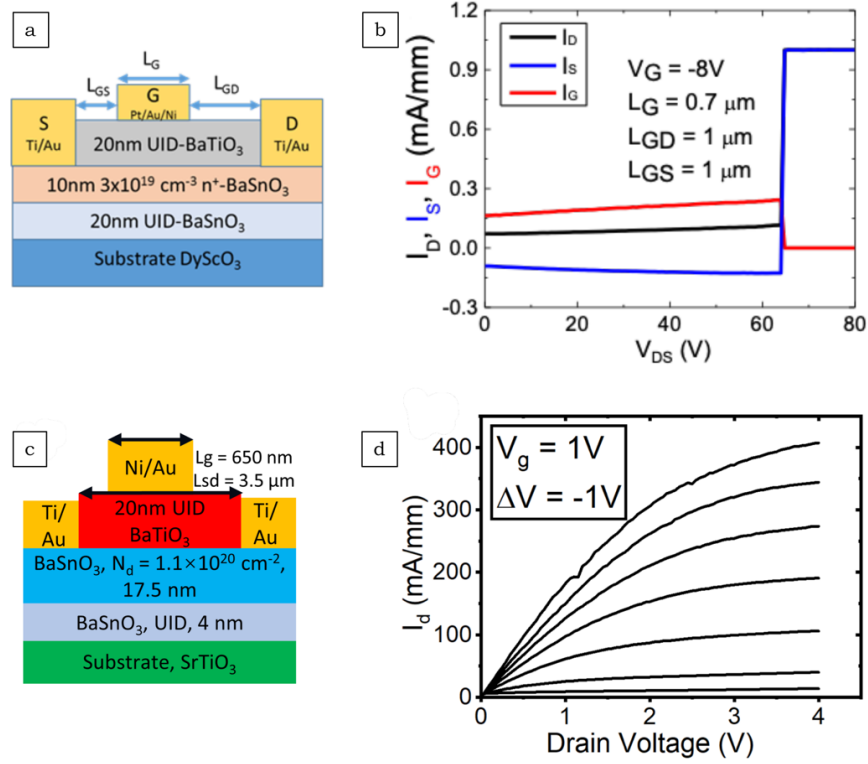


Figure 3.19: BaTiO₃/BaSnO₃ heterojunction field-effect transistors. BaTiO₃/BaSnO₃ HFETs (a) shows breakdown voltage over 60 V (b). Image Courtesy – Prof. Siddharth Rajan’s Group at The Ohio State University. Channel with higher sheet carrier densities (c) exhibits higher drain current (d). Reprinted from Junao Cheng et al. *Appl. Phys. Lett.* 118, 042105 (2021) with permission from IEEE. Copyright 2021 IEEE [103].

3.3.2 Field-Effect Transistor Using BaTiO₃/BaSnO₃ Heterostructure

Although BaTiO₃ does not display any sign of ferroelectricity in C - V characteristics, BaTiO₃/BaSnO₃ heterostructure could still help power transistors. The high permittivity of

BaTiO₃ lowers the lateral electric field in the channel of a field-effect transistor (FET). This low lateral electric field can increase the breakdown voltage in power FET [5,104]. Our collaborator, Prof. Siddharth Rajan's group at Ohio State University, has fabricated FETs in the BaTiO₃/BaSnO₃ heterostructures. In a narrow channel (10 nm) BaTiO₃/BaSnO₃ FET (**Fig. 3.19(a)**), they have demonstrated breakdown voltage over 60 V, as shown in **Fig. 3.19(b)**. Moreover, moderately high drain current can be achieved in BaTiO₃/BaSnO₃ FET by increasing BaSnO₃ channel thickness and doping density (**Fig. 3.19(c)**), as shown in **Fig. 3.19(d)** [103].

3.4 Conclusion

In summary, we have studied the growth mechanism of BaSnO₃ thin films on DyScO₃ substrates. This study reveals that the epitaxial growth of BaSnO₃ thin films in MBE is Ba flux-limited, and the growth is always non-stoichiometric [105]. Moreover, TEM and RHEED analyses demonstrate that the growth mode is island nucleation and coalescence. Besides, this study confirms significant non-uniformity in structural and transport properties of BaSnO₃ thin films. The highest mobilities measured in this study are 172 cm²/Vs and 215 cm²/Vs using Van der Pauw and Hall bar methods, respectively. Due to significant lattice mismatch, BaTiO₃/BaSnO₃ devices demonstrate no sign of ferroelectricity. Nonetheless, the high permittivity of BaTiO₃ can enhance the breakdown voltage of the power FETs.

Chapter 4

Cadmium Arsenide (Cd_3As_2) – a Three-Dimensional Topological Dirac Semimetal

In recent years, topological Dirac semimetals have gathered substantial attention because of their unique electronic properties. Dirac semimetals have Dirac nodes, which are created by the crossing of the linearly dispersive bands around the Fermi energy. Depending on the nature of the Dirac nodes, these new class of electronic material can exhibit a wide range of interesting electronic properties, such as – high Fermi velocity [61], negative or linear magnetoresistance [62,106-108], ambipolar transport [109], high electron mobilities [62], chiral anomaly [106,108,110-115], and Fermi arcs on the surface [116]. Moreover, by breaking the crystal symmetry and tuning the spin-orbit coupling, the topological phase of a Dirac semimetal can be altered [117]. These unique electronic properties have also made Dirac semimetals promising for next-generation electronic and photonic devices.

This chapter discusses a recently discovered three-dimensional (3D) Dirac semimetal – cadmium arsenide (Cd_3As_2). This chapter details crystal and electronic structures of Cd_3As_2 . Moreover, it reviews Cd_3As_2 thin films grown in molecular beam epitaxy (MBE). Furthermore, it describes several possible electronic and photonic applications of Cd_3As_2 thin films.

4.1 Three-Dimensional Topological Dirac Semimetal

Topological semimetals have topologically protected states that can accommodate relativistic fermions. One of the subclasses of topological semimetal is Weyl semimetal. Weyl semimetals are characterized by Weyl nodes that can host massless chiral fermions. A topological semimetal becomes a Weyl semimetal when the crystal lacks inversion and/or time-reversal symmetry. The low energy excitation of a massless fermion in a Weyl node can be described using the Hamiltonian [118-119] –

$$H = \pm v \vec{\sigma} \cdot \vec{k} \dots \dots \dots (4.1)$$

where $\vec{\sigma}$ is the Pauli matrix, v is the velocity of the fermion (also known as the Fermi velocity), $\vec{k}$ is the crystal momentum of the fermion, and the sign indicates the chirality of the Weyl node.

Imposing both time-reversal and inversion symmetry, Weyl semimetal can be transformed into a 3D Dirac semimetal. In simple terms, this type of material can be considered as a 3D analog of graphene [120]. Graphene has Dirac nodes with linear energy dispersion along with two momentum directions, while 3D Dirac nodes exhibit linear energy dispersion along with all three momentum directions. The additional symmetry in a 3D Dirac semimetal results in a two-fold degeneracy. This two-fold degeneracy of a 3D Dirac semimetal can be explained as the superimposing of two copies of Weyl nodes on each other in the momentum space, and thus the low energy excitation of fermions in a Dirac node can be expressed using the following Hamiltonian [121]–

$$H = \begin{pmatrix} v\vec{\sigma} \cdot \vec{k} & 0 \\ 0 & -v\vec{\sigma} \cdot \vec{k} \end{pmatrix} \dots \dots \dots (2.2)$$

Additional symmetry needs to be imposed to stabilize the band crossing in a Dirac node. One possible way to stabilize a Dirac node is to introduce an n-fold rotational symmetry in the crystal [122]. A 3D Dirac semimetal with a rotational symmetry is called a 3D topological Dirac semimetal.

4.2 Cd₃As₂ – A 3D Topological Dirac semimetal

3D topological Dirac semimetal is a new class of material first proposed in 2012 [123]. After this proposal, Cd₃As₂ [61,124,125] and Na₃Bi [117,126] are the two materials that were identified and experimentally verified as 3D topological Dirac semimetals. Unlike Na₃Bi, Cd₃As₂ is chemically stable at room temperature and atmospheric pressure. This chemical stability gathered immense attention to Cd₃As₂. Along with time-reversal symmetry, Cd₃As₂ has a 4-fold rotational symmetry that protects the band crossings in Dirac nodes.

Cd₃As₂ has a very complex crystal structure. The unit cell of Cd₃As₂ is a superstructure of distorted antiferite (M₂X) subcell. In an antiferite unit cell, the M atoms sit at eight tetrahedral interstitial sites while the X atoms form a face-centered cubic structure. In the distorted Cd₃As₂ antiferite subcell, **As** anions sit in the X sites whereas **Cd** cations occupy the M sites that form a distorted cube with two **Cd** vacancies at the vertices, as shown in **Fig. 4.1(b)**. Cd₃As₂ has a very large unit cell at room temperature consisting of 16 distorted antiferite subcells, as shown in **Fig. 4.1(a)**. An earlier x-ray diffraction (XRD) study [127],

reported lack of inversion symmetry in Cd_3As_2 . But, recent studies [120,128,129] have confirmed the inversion symmetry in Cd_3As_2 .

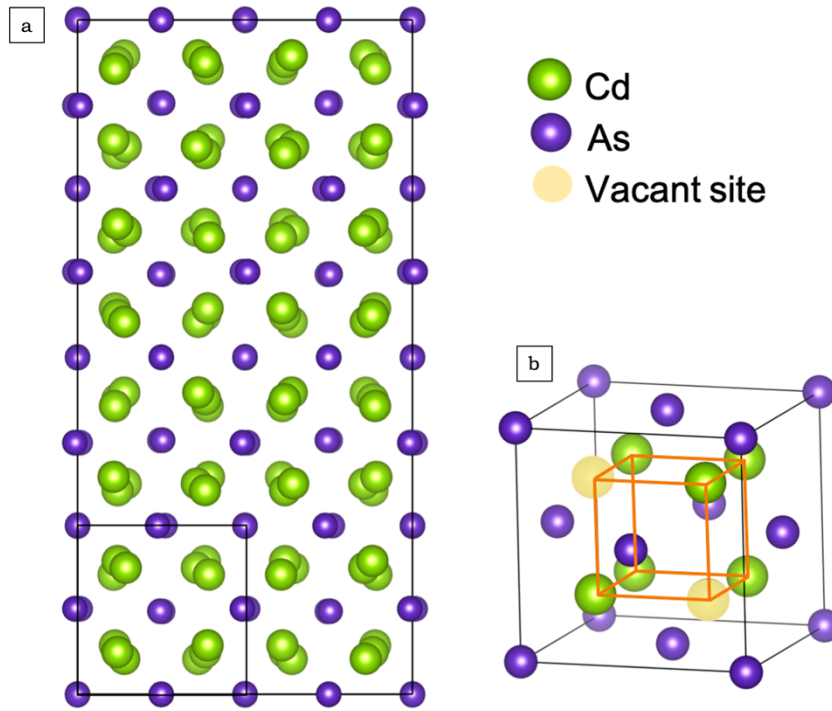


Figure 4.1: Crystal structure of Cd_3As_2 . (a) A unit cell of Cd_3As_2 consists of 160 atoms and 16 distorted antiferroite subcells. (b) Distorted antiferroite subcell of Cd_3As_2 . This subcell consists of tetrahedral interstitial Cd, face-centered As, and two Cd vacancies. *Image Courtesy – Manik Goyal*

There are several studies to calculate the band diagram of Cd_3As_2 . In earlier studies, the Cd_3As_2 band structure was calculated using Kane models [130]. These models, however, fail to incorporate **Cd** vacancy ordering. To incorporate **Cd** vacancy ordering in the calculation, Bodnar [131] included field splitting parameters in the band calculation of Cd_3As_2 . Recent first-principle calculations [124,132] show the presence of the band crossing in Cd_3As_2 band

structure along Γ -Z direction (**Fig. 4.2**). This band crossing gives two Dirac nodes in the first Brillouin zone, as shown in the figure. A four-fold rotational symmetry protects this band crossing, and prevents any bandgap opening. The calculation shows large anisotropy in the Dirac nodes. Also, the Dirac node exhibits a linear energy dispersion near the Fermi level. As the Dirac nodes of Cd_3As_2 are along the Γ -Z direction, the surface projections of the bulk nodes on the (001) crystallographic plane should overlay on each other. All other surface states should be created by Fermi arcs, as shown in **Fig. 4.3**.

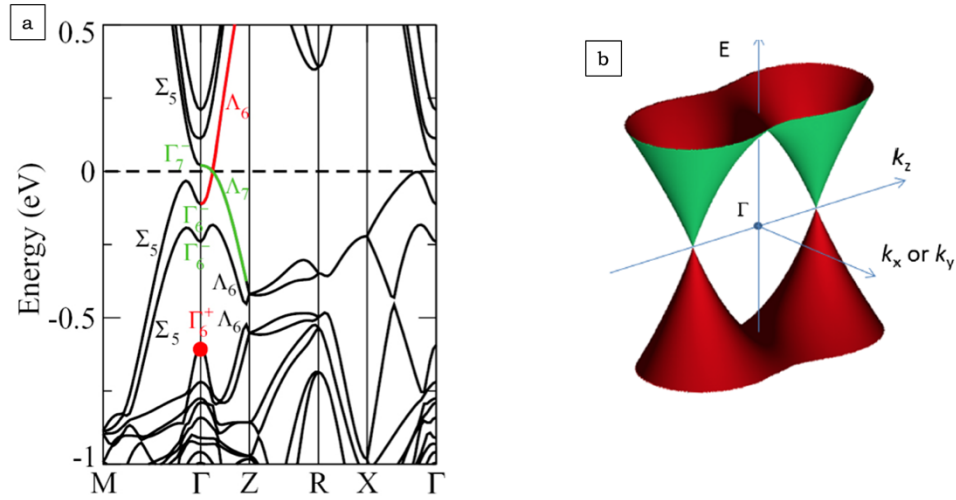


Figure 4.2: Electronic band structure of Cd_3As_2 . (a) Calculated Band Structure of Cd_3As_2 . 4P As states create Dirac nodes along k_z direction. The Dirac node is protected by C_4 rotational symmetry. *Reprinted with permission from Zhijun Wang et al. Phys. Rev. B 88, 125427, 2013 [124]. Copyright 2013 by the American Physical Society.* (b) Schematic diagram of Dirac nodes in Cd_3As_2 . Two copies of Dirac nodes (two-fold degeneracy) exist due to inversion symmetry. *Reprinted with permission from Sergey Borisenko et al. Phys. Rev. Lett. 113, 027603, 2014 [125]. Copyright 2014 by the American Physical Society.*

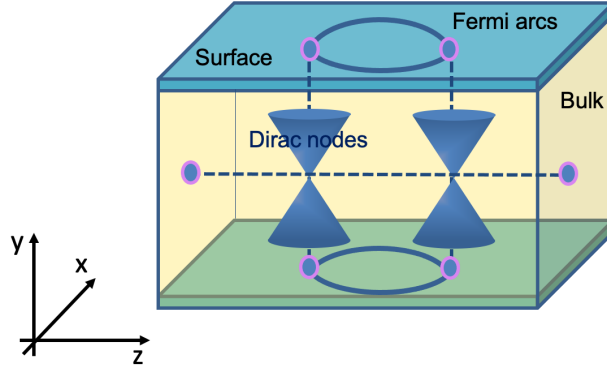


Figure 4.3: Surface states in Cd_3As_2 . Surface states are created by connecting the surface projections of the Dirac nodes. Along z-direction, the projections of both Dirac nodes coincide. That is why surface states are point-like on (001) surface. On any other surface, the surface states are created by Fermi arcs.

Cd_3As_2 has been considered as a low bandgap high mobility semiconductor for a long time [133]. Cd_3As_2 was first predicted as 3D Dirac topological semimetal in 2013 [124]. In 2014, angle-resolved photoemission spectroscopy (ARPES) measurements verified the presence of the Dirac nodes in Cd_3As_2 and confirmed the predictions made earlier [61,125]. **Figure 4.4** shows the ARPES measurement of single-crystal Cd_3As_2 with a nice Dirac node. The ARPES image shows linear energy dispersion for an energy range of ~ 250 meV. This study also shows that the Fermi velocity in a Cd_3As_2 Dirac node is $\sim 2 \times 10^6$ m/s. The Fermi velocity of Cd_3As_2 is much higher than that of any other topological semimetals (**Table 4.1**). Moreover, the electron mobility in single-crystal Cd_3As_2 could be as high as 9×10^6 cm^2/Vs at low temperatures [62].

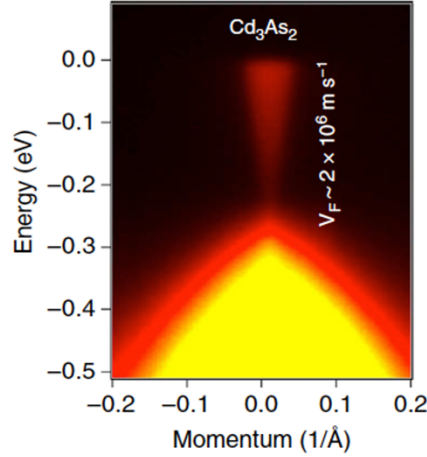


Figure 4.3: Angle-resolved photoemission spectroscopy of Cd_3As_2 . ARPES measurements verify the existence of Dirac nodes in Cd_3As_2 . ARPES measurements showed a Fermi velocity of 1.5×10^6 m/s in Cd_3As_2 . *Reprinted from Madhab Neupane et al. Nature Communications volume 5, 3786 (2014) with permission from Springer Nature, Copyright 2014 [61].*

4.3 Cd_3As_2 Thin Films Grown in Molecular Beam Epitaxy

The best way to study any new electronic material, to understand its physics and to explore different applications is to grow epitaxial thin films of that materials. MBE is a process to grow high-quality epitaxial single-crystal thin films. Our group has developed an MBE process to grow high-quality single-crystal Cd_3As_2 thin films. Timo Schumann and Manik Goyal led this project where they varied different growth parameters to grow high-quality Cd_3As_2 thin films with excellent structural quality and electronic transport properties [134].

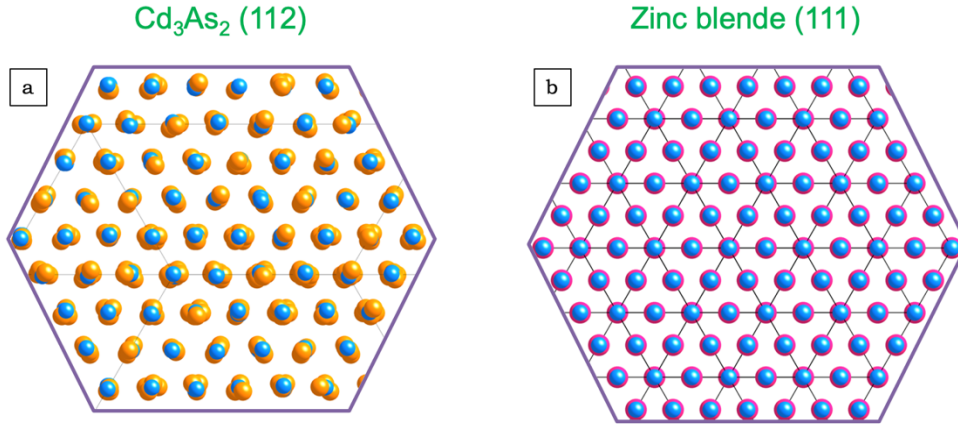


Figure 4.5: Substrates for epitaxial growth of Cd_3As_2 thin films. Atomic arrangement of (a) Cd_3As_2 (112) and (b) Zincblende (111) surfaces. Both surfaces show a similar hexagonal arrangement of As atoms. *Image Courtesy – Prof. Susanne Stemmer.*

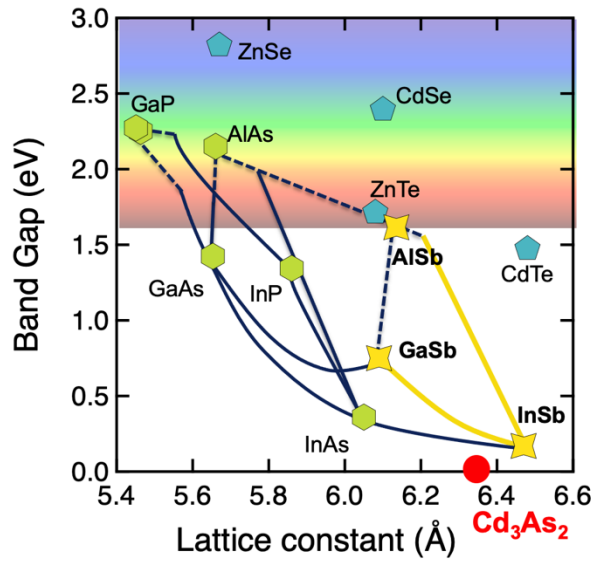


Figure 4.6: Lattice parameters of zincblende substrates for epitaxial growth of Cd_3As_2 . As antimonides have lattice parameters close to that of Cd_3As_2 , Cd_3As_2 is grown with an antimonides buffer layer to reduce defects. *Image Courtesy – Prof. Susanne Stemmer.*

Single crystal studies of Cd_3As_2 have shown that (112) is the preferred growth plane for Cd_3As_2 [120,135]. That is why the epitaxial growth of Cd_3As_2 (112) thin films in MBE was first optimized in our lab. The first step of the epitaxial growth of any thin film in MBE is to select the correct substrate. Several factors need to be considered to select a suitable substrate. The substrate and the thin film should have similar crystallographic structures or similar atomic arrangements at the surfaces. Moreover, to grow a coherently strained film, the lattice parameter of the substrate should be close to that of the thin film. **Figure 4.5** shows the atomic arrangements of the Cd_3As_2 (112) and *zincblende* GaAs (111) planes. Both surfaces show similar hexagonal arrangements of As atoms. Because of the similar atomic arrangements, GaAs (111) substrate was chosen for epitaxial growth of Cd_3As_2 (112) films. **Figure 4.6** shows the lattice parameters of different *zincblende* semiconductors and Cd_3As_2 . Antimonides have lattice parameters close to that of Cd_3As_2 . Therefore, growing an antimonide buffer layer reduces structural defects introduced by lattice mismatch. Furthermore, the biaxial stress on the Cd_3As_2 thin films can be tuned by alloying AlSb, InSb, and GaSb [136].

Figure 4.7(a) shows a schematic diagram of a typical Cd_3As_2 thin film grown in MBE. Atomic force microscopy (**Fig. 4.7(b)**) shows the excellent surface quality of the films. **Figure 4.7(c)** shows out-of-plane XRD of a typical Cd_3As_2 film grown in the MBE system. The long XRD scan exhibit peaks only from GaAs and GaSb {111} and Cd_3As_2 {112} planes. This XRD scan confirms the excellent structural quality of the Cd_3As_2 film. Additionally, **Fig. 4.7(d)** shows the high-resolution XRD scan with thickness fringes. Thickness fringes suggest great surface and interface quality. Cd_3As_2 films grown in the MBE system exhibit good structural quality

and demonstrate outstanding electronic transport properties. The Cd_3As_2 films routinely exhibit room temperature mobilities of $20,000 \text{ cm}^2/\text{Vs}$ [134].

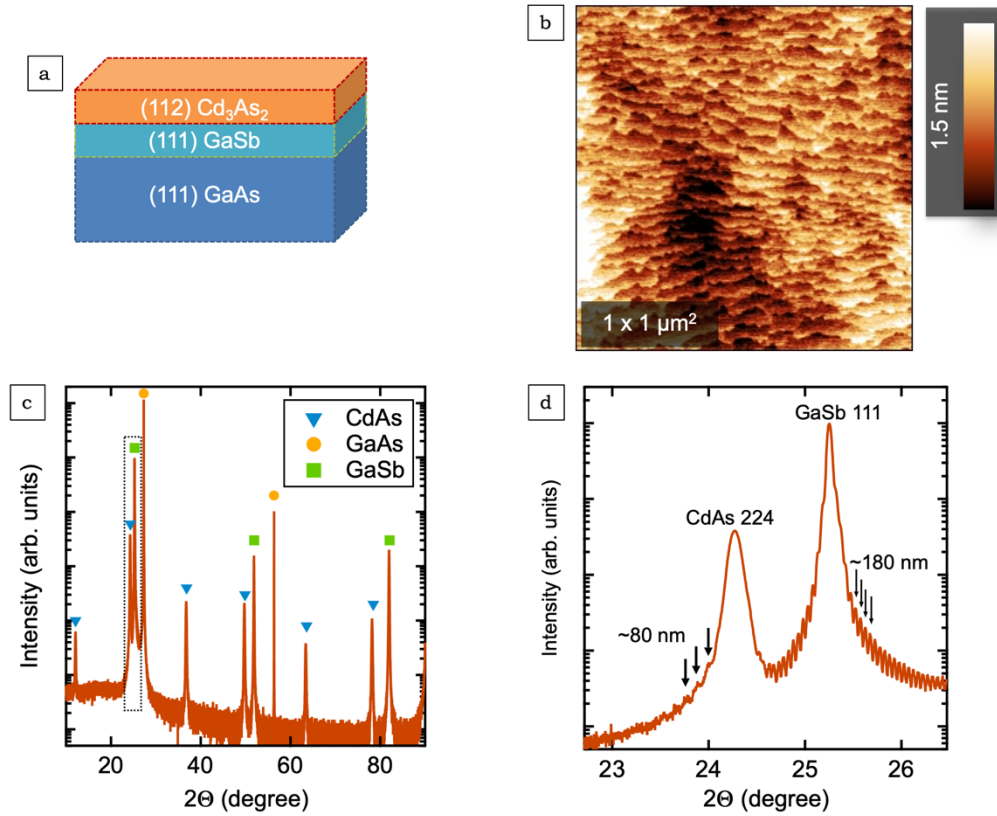


Figure 4.7: Epitaxial thin films Cd_3As_2 grown in molecular beam epitaxy. (a) Schematic diagram of Cd_3As_2 thin films grown on GaAs substrate with GaSb buffer layer. (b) Atomic force microscopy of a surface of a typical Cd_3As_2 film. (c) Long and (d) Short x-ray diffraction scan of a Cd_3As_2 thin film. Long XRD scan shows GaAs and GaSb $\{111\}$ planes and Cd_3As_2 $\{112\}$ planes. A high-resolution short XRD scan exhibits nice thickness fringes, indicating a smooth interface. *Image Courtesy: Timo Schumann and Manik Goyal.*

Table 4.1: Fermi and Drift Saturation Velocities of Semimetals and Semiconductors

Material Type	Material	Fermi/Saturation Velocity ($\times 10^6$ m/s)
2D Dirac Semimetal	Graphene	1.05 [137]
3D Dirac Semimetal	Cd ₃ As ₂	2 [61]
	Na ₃ Bi	0.425 [117]
Weyl Semimetal	TaAs	0.36 [106]
Topological Insulator	Bi ₂ Se ₃	0.54 [138]
	Bi ₂ Te ₃	0.4 [139]
Semiconductor	InAs	0.8 [140]
	GaAs	0.1 [141]
	InP	0.2 [142]
	GaN	0.2 [143]

4.4 Cd₃As₂ Transistors to Bridge the “Terahertz Gap”

To bridge the "terahertz gap," electronic devices will require new materials that exhibit higher carrier velocity and offer a relatively high density-of-states (DOS). Traditional high mobility semiconductor suffers from low DOS due to small effective mass, known as "DOS bottleneck" [6]. As mentioned earlier, Cd₃As₂ has a high Fermi velocity, higher than the Fermi velocity of any other topological semimetals or the saturation velocities of any semiconductors. **Table 4.1** compares the Fermi velocity of electrons in Cd₃As₂ with the Fermi velocities and the saturation velocities of some common semimetals and semiconductors. Additionally, Cd₃As₂ thin films can accommodate relatively high sheet carrier densities due to valley degeneracy (two Dirac cones in the Brillouin zone) and linear energy dispersion. Extremely high Fermi velocity and relatively large DOS make Cd₃As₂ a suitable candidate for THz transistors.

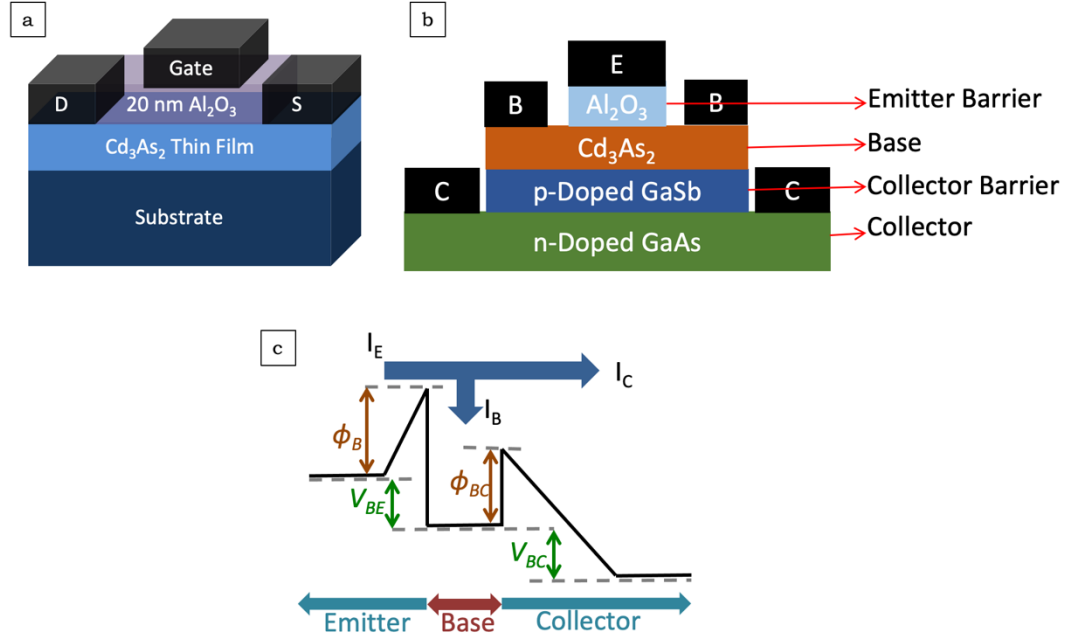


Figure 4.8: Transistors using Cd_3As_2 thin films. (a) Field-effect transistor with Cd_3As_2 channel. (b) Hot electron transistor with Cd_3As_2 base layer. (c) Operating principle of a hot electron transistor.

4.4.1 Cd_3As_2 Channel Field-Effect Transistors

Cd_3As_2 thin film can be used as the channel of a planar field-effect transistor (FET) (**Fig. 4.8(a)**). High Fermi velocity will reduce channel transit time. Moreover, large DOS will increase drain current and internal transconductance of the device. Large DOS, along with high carrier mobilities, will reduce contact and access region resistances. Low transit time, high current density, and transconductance, and low contact and access region resistances should significantly boost the RF performances of the Cd_3As_2 channel FETs. Theoretical calculation (**Chapter 6**) shows that ultra-scaled Cd_3As_2 FET can potentially achieve the current cut-off frequency, f_T , over 1.5 THz. As the carrier velocity is independent of the Fermi level or sheet carrier densities in the Dirac states, Cd_3As_2 FET should provide better protection against any droop in f_T or transconductance at high current density. First-generation Cd_3As_2 FETs exhibit

very low contact resistance and extremely high current densities while showing current modulation similar to monolayer graphene FET. **Chapter 6 and 7** will cover detail of Cd_3As_2 channel FETs.

4.4.2 Hot Electron Transistor

Hot electron transistor (HET) is a vertical unipolar electronic device that has the potential to offer THz performance. Like a bipolar junction transistor (BJT), HET has three terminals – emitter, base, and collector, as shown in **Fig. 4.8(b)**. By applying a bias between base and emitter, the carrier is injected from the emitter. As the injected carriers have very high energy, most of them cross the base region ballistically. The collector barrier prevents the thermalized electron from reaching the collector. All the electrons that reach the base-collector junction with energy more than the collector barrier should reach the collector. **Figure 4.8(c)** shows the basic operation principle of a HET. HET has been demonstrated using different materials. Nevertheless, all of those devices suffer from different design trade-offs. For example, III-Nitride-based HET suffers from low carrier velocity [144,145]. Though base transit time can be reduced in a monolayer graphene-based HET, this device suffers from high base contact resistance [146]. On the other hand, the multilayer graphene base drastically increases the base transit time due to vertical hopping transport. Additionally, lack of chemical bonding between graphene and other layers increases electron reflection at collector junction. Carrier velocity can be improved using high mobility III-V semiconductors; however, close upper valley increases base relaxation. Considering all these, Cd_3As_2 could be a suitable option for this type of transistor. Cd_3As_2 can be used as the base of a HET (**Fig. 4.8(b)**). High Fermi velocity will reduce base transit time, while the semimetallic nature of Cd_3As_2 will reduce base resistance,

even for a very thin base layer. Moreover, epitaxial integration of Cd_3As_2 with other III-V materials gives flexibility in design. For example, high mobility III-V materials can be used as collector barriers, which can lower the collector transit time for a thicker barrier that is necessary to lower the charging time.

Chapter 5

Electronic Transport in Cd_3As_2 Thin Films

Chapter 4 discussed the electronic band structure and the transport properties of the 3D topological Dirac semimetal Cd_3As_2 . Those properties are either calculated or measured for bulk single crystalline Cd_3As_2 . The electronic properties of Cd_3As_2 , however, may change significantly when they are synthesized as thin films. Because thin films are required for different electronic and photonic applications discussed in the previous chapter, a deeper understanding of the electronic properties of Cd_3As_2 thin films is essential. This chapter first discusses how the electronic band structures of Cd_3As_2 thin films evolve with thickness. This chapter also presents the electronic properties of the topologically non-trivial surface states of Cd_3As_2 thin films. The second half of this chapter details how film thickness affects the electronic transport properties, and especially magnetotransport, of Cd_3As_2 thin films.

Some of the results presented in this chapter have been published in L Galletti et al. [187]

5.1 Electronic Band Structure of Cd_3As_2 Thin Films

5.1.1 Energy Gap in Cd_3As_2 Thin Films

To probe the electronic band structure of a Cd_3As_2 thin film, a 30 nm Cd_3As_2 (112) film was grown on a GaAs (111) substrate with a GaSb (111) buffer layer using molecular beam epitaxy (MBE). Afterwards, Hall bar structures were fabricated to study electronic transport properties of the film. Details of the fabrication process are discussed in **Chapter 6**. Physical Property

Measurement System (Quantum Design Dynacool) was used to measure temperature-dependent transport characteristics.

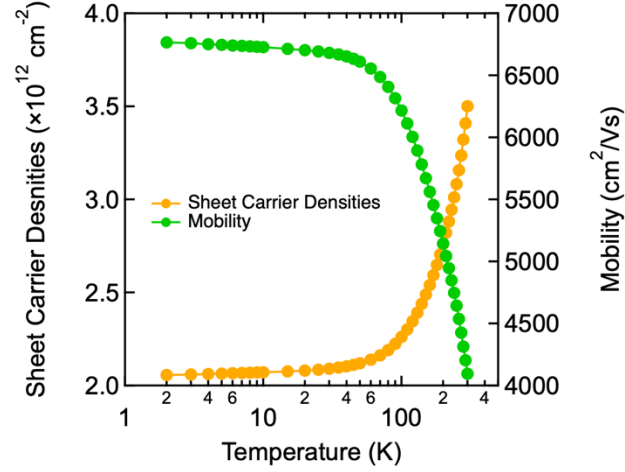


Figure 5.1: Energy gap in Cd_3As_2 thin films. Temperature-dependent sheet carrier densities and electron mobilities of a Cd_3As_2 thin film. Carrier freeze-out indicates the existence of an activation energy in Cd_3As_2 thin film.

Figure 5.1 shows the temperature-dependent sheet densities and the mobilities of the electrons in the film. Below room temperature, the sheet carrier density starts to decrease. The sheet carrier density is somewhat independent of temperature below 80 K. Initial carrier freeze-out indicates the presence of an activation energy in the thin film. Furthermore, the temperature-independent sheet carrier density below 80 K hints at the existence of a gapless state. So, the temperature-dependent sheet carrier density, n_s , of a Cd_3As_2 thin film can be written as -

$$n_s(T) = n_0 + n_1 e^{-\frac{E_A}{kT}} \dots \dots \dots (5.1)$$

where n_0 is temperature independent sheet carrier density, n_1 is a constant, E_A is the activation energy, k is the Boltzmann constant, and T is the temperature.

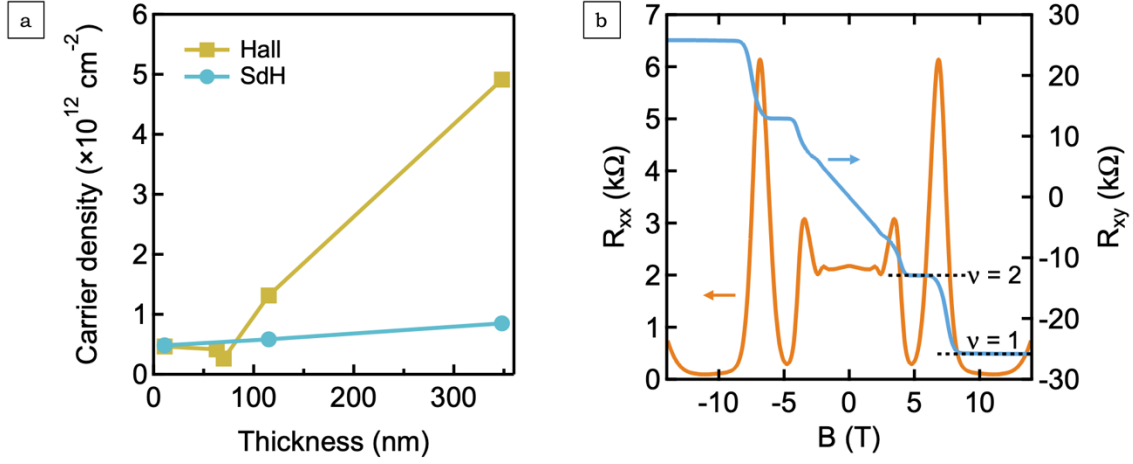


Figure 5.2: 2D transport in Cd_3As_2 thin films. (a) Sheet carrier densities of Cd_3As_2 films with different thicknesses measured at 2 K. Sheet carrier densities were measured using the Hall effect and Shubnikov-de Hass methods. Both methods show similar sheet carrier densities when the film thickness is below 60-70 nm, indicating 2D transport. *Reprinted from M. Goyal et al. APL Materials 6, 026105 (2018) with the permission from authors [147].* (b) Quantum Hall effect in a Cd_3As_2 thin film, clear evidence of a pure 2D transport in very thin Cd_3As_2 films. *Reprinted with permission from T Schumann et al. Phys. Rev. Lett. 120, 016801, 2018. Copyright 2018 by the American Physical Society [148].*

Fitting experimental data with **Eqn. 5.1** gives an activation energy of about 50 meV. Although the temperature-independent sheet carrier density is expected for the 3D Dirac semimetal, the presence of an activation energy is a strong indication of the opening of an energy gap in Cd_3As_2 thin films. Although one theoretical study predicted that quantum confinement could

open up a small bandgap in very thin Cd_3As_2 films [124], further study is needed to understand the origin of activation energy in relatively thicker films.

5.1.2 Two-Dimensional Transport in Cd_3As_2 Thin Films

Thickness-dependent, low-temperature transport studies of Cd_3As_2 reveal purely 2D transport in Cd_3As_2 thin films. Manik Goyal *et al.* [147] measured the sheet carrier densities of Cd_3As_2 thin films at 2 K for different thicknesses, as shown in **Fig. 5.2(a)**. Thicknesses of Cd_3As_2 were varied from 10 nm to 350 nm. Sheet carrier densities were measured using two different methods: the Hall effect method and the Shubnikov–de Haas (SdH) method. The Hall effect method needs a very small magnetic field, and this method reveals the total sheet carrier densities in a film. A high magnetic field is needed for the SdH method to separate different 2D and 3D energy states by forming different Landau levels. The carrier densities in these different energy states can be calculated from their corresponding oscillations in conductivity. In addition, angle-dependent SdH oscillations can distinguish 2D energy states from 3D energy states. Therefore, in **Fig. 5.2(a)**, the sheet carrier densities measured using the Hall method include contributions from both 2D and 3D energy states. The sheet carrier densities measured using the SdH method represent only 2D carriers. This experiment shows that the 2D carriers measured using the SdH method are independent of the film thicknesses. These thickness independent 2D carriers suggest that the 2D energy states are not in the bulk regions, instead at the surfaces. Moreover, when the Cd_3As_2 film thickness is below 60-70 nm, both methods give similar sheet carrier densities, confirming only 2D transport behavior in thin Cd_3As_2 films. In a very thin film, the quantum confinement effect widens the bandgap, leading to a smaller carrier contribution from the gapped states. Due to the absence of the carriers in the gapped

states, the electronic transport mechanism is 2D in a very thin Cd_3As_2 film. Furthermore, Timo Schumann *et al.* have observed the quantum Hall effect in a very thin Cd_3As_2 film [160], as shown in **Fig. 5.2(b)**. As the quantum Hall effect can only be observed in a 2D system, this report is clear evidence of 2D transport in thin Cd_3As_2 films.

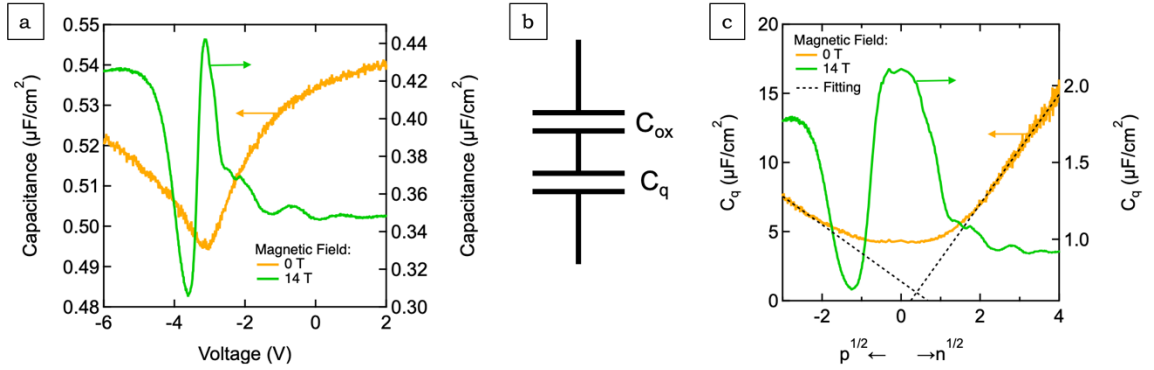


Figure 5.3: 2D Dirac nodes at the surfaces of Cd_3As_2 thin films. (a) Capacitance-voltage characteristics of a Cd_3As_2 device measured at a magnetic field of 0 T (Orange) and 14 T (Green). The measurement was carried out at 40 mK. **(b)** Capacitance components of the device. Oxide and quantum capacitances are in series in the device. **(c)** Extracted quantum capacitances show a linear dependence on $n^{1/2}$ or $p^{1/2}$ at 0 T (Orange) and exhibit zero-energy Landau level at 14 T (Green).

5.1.3 Dirac Nodes in Surface States

From **Section 5.1.2**, it is evident that Cd_3As_2 thin films have 2D electronic states. Nonetheless, the nature of this 2D state is not well understood. Is this 2D state such as the quantum confined subband states in semiconductor quantum wells or is it a 2D Dirac surface state? To answer these questions, an experiment was designed to extract the quantum capacitance of a Cd_3As_2 thin film and to probe the nature of the electronic states of a Cd_3As_2 thin film. For this experiment, Timo Schumann grew Cd_3As_2 (112) films on a GaAs (111) substrate with a GaSb

(111) buffer layer. The thickness of the Cd₃As₂ film was 38 nm. Parallel plate capacitors were fabricated using a standard fabrication process that is discussed in the next chapter. Al₂O₃ was used as a gate insulator layer. Capacitance-voltage (C - V) characteristics were measured at 40 mK using a Keithley 4300A parameter analyzer. An Oxford Triton dilution refrigerator was used to achieve this ultra-low temperature. This dilution refrigerator can apply a magnetic field up to 14 T.

Figure 5.3(a) shows the C - V characteristics of the device measured at the magnetic field of 0 T and 14 T. The measurement frequency of the C - V characteristics is 60 kHz. The quality factor is above 20 for the entire range of the measurements. The measured capacitances have two series components— oxide capacitance (C_{ox}) and quantum capacitance (C_q), as shown in **Fig. 5.3(b)**. The overall capacitance, C , of the device can be written as –

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_q} \dots \dots \dots (5.2)$$

C_{ox} of this device is 0.55 $\mu\text{F}/\text{cm}^2$, and by removing this contribution from the overall capacitance, it is possible to extract the C_q of the device. Extracted C_q is shown in **Figure 5.3(c)**. C_q reflects the density of states, D , at the Fermi energy, E_F , and can be written as –

$$C_q(E_F) = e^2 D(E_F) \dots \dots \dots (5.3)$$

Moreover, the density of states of a 2D Dirac state, which has linear energy dispersion, can be written as –

$$D(E_F) = \frac{gE_F}{\pi\hbar^2v_F^2} = \frac{g\sqrt{n_s}}{\sqrt{\pi}\hbar v_F} \dots \dots \dots (5.4)$$

where g is the valley degeneracy (number of Dirac nodes in the material, 2 for Cd₃As₂), $\hbar$ is the reduced Planck constant, v_F is the Fermi velocity of the Dirac nodes, and n_s is the sheet carrier density in the 2D states. From **Eqn. 5.4** it is evident that C_q should depend linearly on Fermi energy. Moreover, C_q should have a linear dependence on $\sqrt{n}$ (or $\sqrt{p}$ if E_F is below the charge neutrality point (CNP)). **Figure 5.3(c)** presents the C_q as a function of $\sqrt{n}$ (or $\sqrt{p}$), where n and p are the density of electrons and holes, respectively. n and p are calculated by integrating the C - V profile, assuming that number of electrons and holes are zero at the CNP. The minimum of the C - V characteristics is considered the CNP as the density-of-states (and C_q contribution) is minimum at the CNP. At 0 T, C_q shows a linear dependence on $\sqrt{n}$ and $\sqrt{p}$. This linear dependence is a clear indication of the existence of the 2D Dirac states in Cd₃As₂ thin films. The flat C_q near the CNP is due to electron-hole puddles [149]. Similar puddles were observed in similar experiments in graphene [149].

Another definite signature of a 2D Dirac state is the zero-energy Landau level (**Eqn. 1.26**). Nonetheless, this signature is difficult to detect from transport measurements, even for a very high-quality Dirac material. This zero-energy Landau level is easy to probe in a C - V measurement. C - V characteristics exhibit quantum oscillations due to the formation of the

Landau levels under an applied magnetic field. **Figure 5.3(c)** illustrates the C_q with an applied magnetic field of 14 T. Due to the formation of the Landau levels, C_q demonstrates oscillations. More importantly, the zero-energy Landau level (the peak at the CNP) can easily be detected from this C_q . This detection of the zero-energy Landau level gives additional evidence of the presence of 2D Dirac states in Cd_3As_2 thin films.

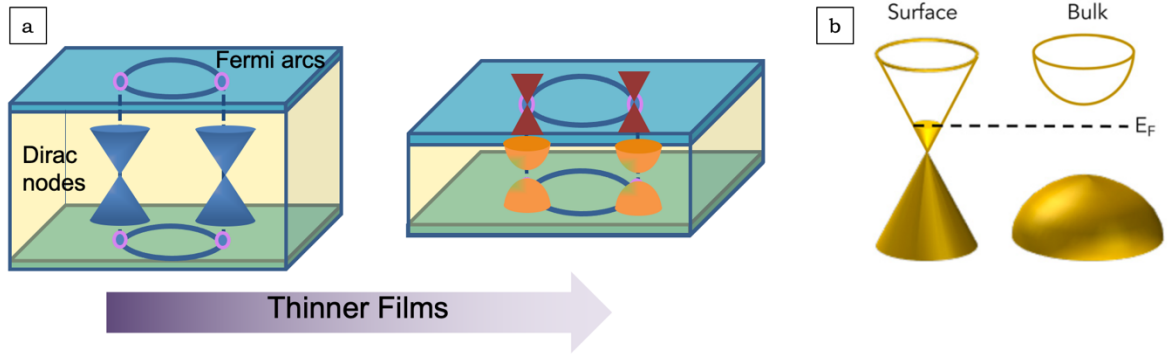


Figure 5.4: Electronic band structure of Cd_3As_2 thin films. (a) Evolution of the band structure in Cd_3As_2 with film thicknesses. (b) A small bandgap opens up in the bulk region in a thin film due to quantum confinement. A 2D Dirac state exists on the surfaces. *Reprinted from [109] with permission from AIP Publishing.*

5.1.4 Electronic Band Structure of Cd_3As_2 Thin Films

All the experiments discussed so far can be combined to obtain a clear picture of how the electronic band structure of Cd_3As_2 thin films evolve with thickness. This is illustrated schematically in **Fig. 5.4**. Towards the bulk limit, quantum confinement effects are negligible. As a result, 3D Dirac nodes exist in thick Cd_3As_2 films. As the film thickness is decreased, quantum confinement effects start to dominate, and a small bandgap opens up in the bulk region. Topologically non-trivial 2D Dirac states exist on the surfaces. The energy band

diagram of a very thin Cd_3As_2 film is illustrated in **Fig. 5.4(b)**. The band diagram shows parabolic bands and a small energy gap at the bulk region. Furthermore, it contains a linearly dispersive, topologically non-trivial 2D Dirac node at the surface.

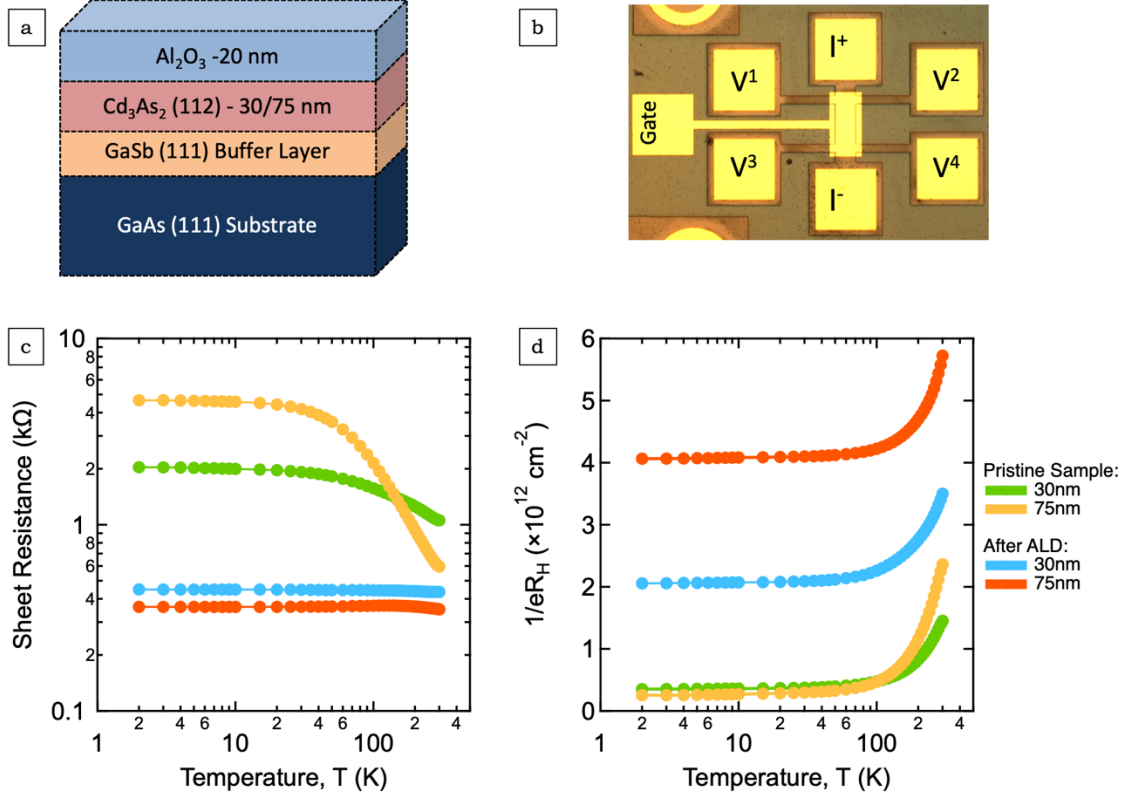


Figure 5.5: Temperature-dependent transport characteristics of Cd_3As_2 films before and after Al_2O_3 deposition. (a) Schematic structure of Cd_3As_2 (112) thin film grown on GaAs (111) substrate with a GaSb buffer layer. Cd_3As_2 films with two different thicknesses (30 nm and 75 nm) were grown in MBE. **(b)** A gated Hall bar structure fabricated on a Cd_3As_2 thin film. **(c)** Sheet resistance and **(d)** The inverse of the Hall resistance before and after ALD as a function of temperature for these two Cd_3As_2 films.

5.2 Thickness Dependent Magnetotransport in Cd_3As_2 Thin Films

From earlier discussion, it is clear that the band structures of Cd_3As_2 thin films evolve with the thicknesses of the films. This thickness-dependent electronic bandstructure should directly affect the electronic transport in Cd_3As_2 thin films. This section discusses how the film thickness affects magnetotransport in Cd_3As_2 thin films.

Two Cd_3As_2 (112) thin films with different thicknesses (30 nm and 75 nm) were grown for this experiment. The schematic structures of the films are shown in **Fig. 5.5(a)**. The thicknesses of the films were chosen based on the other experiments discussed earlier. 30 nm film should have a significantly wider energy gap in the bulk region compared to a 75 nm film. This should result in a different bulk carrier contribution in the films, and the effect of these bulk carriers on transport characteristics can be revealed by comparing the transport of these two films. Gated Hall bar structures were fabricated on the samples. 20 nm Al_2O_3 layers were deposited on the films for electrostatic gating. The detail of the fabrication is discussed in the next chapter. An optical image of a fabricated gated Hall bar structure is shown in **Fig. 5.5(b)**. The transport characteristics of the films were measured using Quantum Design physical property measurement system, which has a temperature range of 2 K to 400 K and can apply a magnetic field up to ± 9 T. A Keithley 2400 source meter was used to control the gate voltage of the Hall bars.

Figure 5.5(c) presents the sheet resistances of the films before and after atomic layer deposition (ALD) of Al_2O_3 . The sheet resistances of the films decrease after Al_2O_3 deposition

due to the elevation of the Fermi level. This elevated Fermi level increases the sheet carrier densities in the films and thus reduces the sheet resistances. **Figure 5.5(d)** shows the $(eR_H)^{-1}$ of the films as a function of temperature, where R_H is the Hall coefficient. When there is only one type of carrier, $(eR_H)^{-1}$ is the sheet carrier density of the film. At low temperatures, both pristine films accommodate both electrons and holes. Due to the presence of two types of carriers, it is difficult to measure the exact sheet carrier densities at low temperatures. The origin of the two types of carriers will be explained later. After Al_2O_3 deposition, the films are entirely n-type due to the elevated Fermi levels. So, $(eR_H)^{-1}$ plots after Al_2O_3 deposition represent the sheet carrier densities of the films. Both films show carrier freeze-out at lower temperatures due to the existence of energy gaps in the bulk regions, as explained earlier. After Al_2O_3 deposition, the thicker film shows higher sheet carrier density because of higher bulk carrier contributions. In both samples, whether pristine or post-ALD, there are several types of carriers with different mobilities: Dirac fermions, bulk electrons, bulk holes. Because of these different types of carriers with different dependencies on temperature, it was difficult to extract their mobilities.

Figure 5.6 presents the magnetotransport of both pristine films. **Figure 5.6(a,c)** shows the magnetoresistance (MR) of 30 nm and 75 nm Cd_3As_2 films, respectively. The MR was calculated using the following equation:

$$MR(H) = \frac{R_{xx}(H) - R_{xx}(H=0)}{R_{xx}(H=0)} \times 100 \dots \dots \dots (5.5)$$

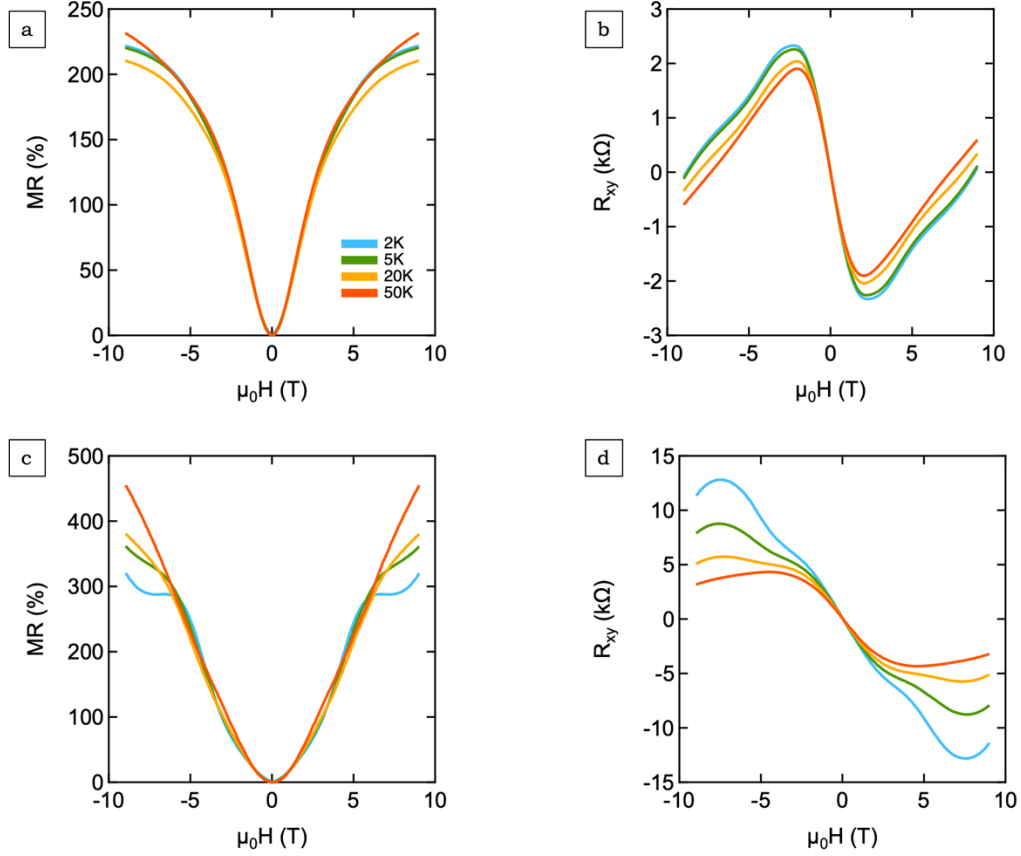


Figure 5.6: Effect of film thickness on magneto-transport of pristine Cd_3As_2 thin films. (a) Magnetoresistance and **(b)** Transverse resistance of pristine 30 nm Cd_3As_2 film as a function of applied magnetic field for different temperatures. **(c)** Magnetoresistance and **(d)** Transverse resistance of pristine 75 nm Cd_3As_2 film as a function of applied magnetic field for different temperatures.

Longitudinal resistance, R_{xx} , was measured using the Hall bar structures. Even though both films exhibit positive MR, the magnetic field dependence of the MR is different in thick and thin films. The thinner film displays saturating MR at a high magnetic field, whereas the thicker film exhibits classic quadratic dependence ($\sim H^2$) on the magnetic field. This different magnetic field dependence of MR indicates a longer carrier lifetime in thicker films [150]. This finding

is consistent with the previous observation of higher electron mobilities in thicker films. Moreover, MR in thicker film exhibits quantum oscillations, another piece of evidence of a higher quantum lifetime of fermions in a thicker film. These quantum oscillations diminish at higher temperatures because of quantum decoherence due to thermal vibration. **Figure 5.6(b,d)** illustrates the Hall resistance, R_{xy} , of 30 nm and 75 nm Cd_3As_2 films, respectively. At a low magnetic field, both films exhibit negative slopes in R_{xy} , indicating electron-dominated transport. Slopes became positive at a higher magnetic field in both films. These changes in the sign of the slopes of R_{xy} at a high magnetic field indicate the coexistence of electrons and holes in the films. R_{xy} of the thicker film demonstrates oscillations, and this might be due to quantum oscillations observed in the MR of the same film. Moreover, the thinner film exhibits a relatively steeper positive slope in R_{xy} at a higher magnetic field. This could be due to lower electron mobilities or higher hole contribution in the thinner films.

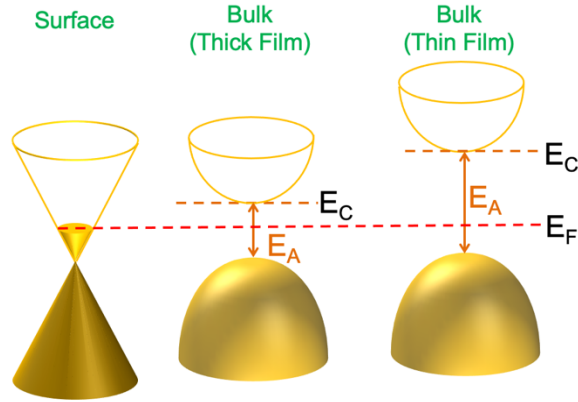


Figure 5.7: Electronic band structures of pristine Cd_3As_2 thin films. Schematic energy band diagram of thick and thin Cd_3As_2 films showing Dirac surface states and gapped bulk states. Thinner film has a wider bulk energy gap due to more prominent quantum confinement.

The coexistence of electrons and holes in the pristine films can be explained using the band structure. **Figure 5.7** illustrates the schematic electronic band structures of these two pristine films. Both films have two states, 2D Dirac state at the surface and gapped parabolic state at the bulk region, as shown in this figure. The energy gap of the bulk state is wider in the thinner film due to a stronger quantum confinement effect. In a pristine sample, the Fermi level, E_F , is slightly above the CNP of the surface Dirac state. These surface states contribute to electrons in the films. Nevertheless, in the bulk region, E_F is close to the bulk valance band. As a result, bulk states contain holes. The ratio of electrons and holes in the film depends on several factors, such as the position of E_F , band bending, and the electric field near the surface. As the films are not intentionally doped, these factors are mostly determined by the film quality and growth conditions. Surface roughness, dislocation densities, and vacancies in the film can alter the position of E_F , band bending, and the electric field near the surface. Furthermore, quantum confinement can move the relative position of the bulk states. Sample-to-sample variation can result in a variation in electron/holes ratio. That is why the early onset of the positive slope of R_{xy} in thinner films may not be due to differences in film thicknesses, but instead due to a slight variation in unintentional “doping density.”

Figure 5.8 demonstrates the magnetotransport of 30 nm and 75 nm thick Cd_3As_2 films after Al_2O_3 deposition. **Figure 5.8(a)** presents the MR of the thinner film. The post-ALD film shows positive MR with SdH oscillations. Moreover, unlike the pristine film, the post-ALD film displays non-saturating MR. The quadratic magnetic field dependence of MR and SdH oscillations suggest an improvement in the quantum lifetime of the Dirac fermions. This change in MR after Al_2O_3 deposition is due to an elevated E_F in the film. In the post-ALD thin

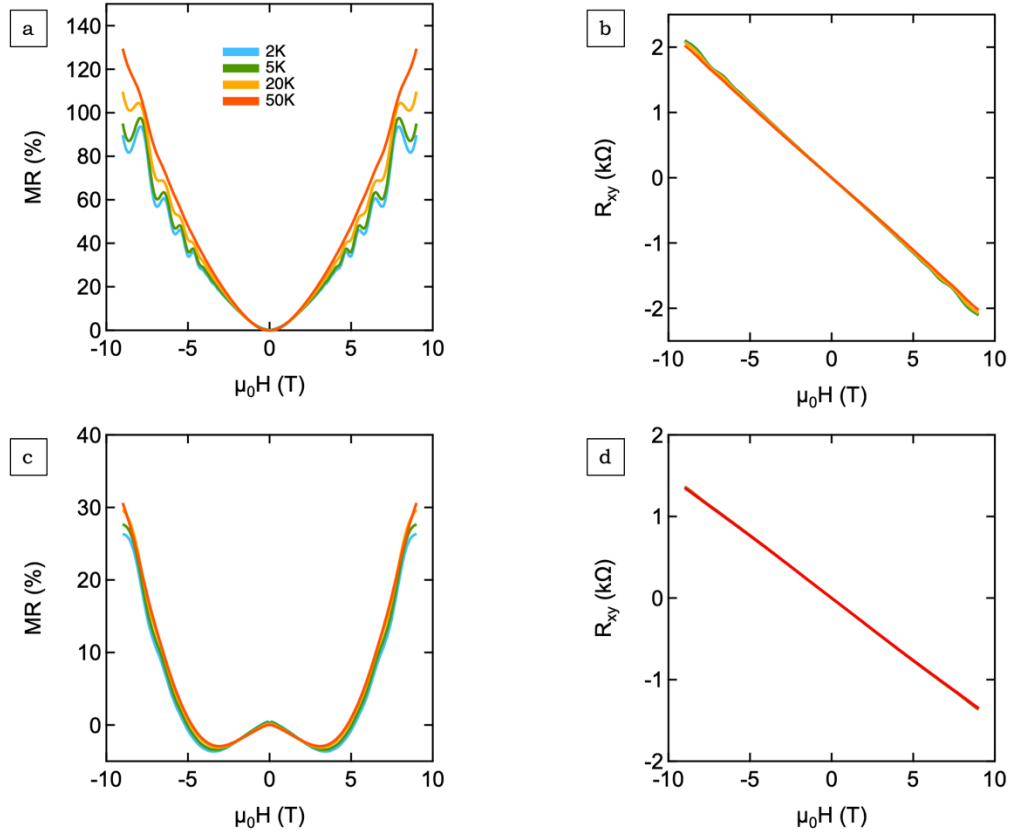


Figure 5.8: Effect of film thickness on magneto-transport of Cd₃As₂ thin films with Al₂O₃ cap layer. (a) Magnetoresistance and (b) Transverse resistance of 30 nm Cd₃As₂ film after Al₂O₃ deposition as a function of applied magnetic field for different temperatures. (c) Magnetoresistance and (d) Transverse resistance of 75 nm Cd₃As₂ film after Al₂O₃ deposition as a function of applied magnetic field for different temperatures.

film, E_F resides around the middle of the bulk bandgap. This change in E_F reduces the carrier contribution from the bulk region and makes the surface Dirac fermions the only dominating carriers in the film. That is why the electronic transport exhibits 2D transport characteristics, displaying SdH oscillations. Additionally, Al₂O₃ deposition increases the carrier densities in the surface Dirac states. High carrier densities provide higher screening in the film and, thus,

improve carrier lifetime. **Figure 5.8(b)** illustrates the Hall resistance of the thinner Cd_3As_2 film. Because the post-ALD thinner film has negligible hole contribution from the bulk region, R_{xy} displays a negative slope for the whole range of the magnetic field. Moreover, as the sheet carrier density is very high ($\sim 2 \times 10^{12} \text{ cm}^{-2}$), R_{xy} does not display any clean quantum hall plateaux. Although few less prominent higher filling factor plateaux are visible at a high magnetic field.

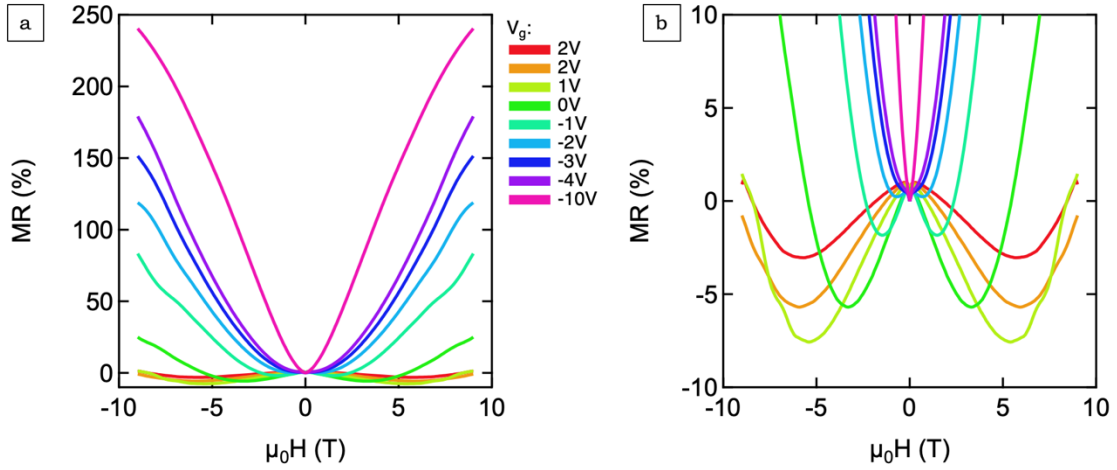


Figure 5.9: Electrostatic gating of 75 nm Cd_3As_2 thin film and its effect on magneto-transport.

(a) Magnetoresistance of Cd_3As_2 thin film for different gate voltage. **(b)** Magnification of the magnetoresistance near the negative magnetoresistance region.

Figure 5.8(c) shows the MR of the 75 nm thick Cd_3As_2 film. The MR of the post-ALD thicker film is different from post-ALD thinner film or pristine films. The post-ALD thicker film demonstrates negative MR at a low magnetic field, and it becomes positive above 5 T. In all of these measurements, magnetic field direction is perpendicular to the film surface. Negative

longitudinal MR (the magnetic field is parallel to the plane) has been reported for Dirac semimetals. Chiral anomaly [106,108,110-115], current jetting [151], and the contribution of the Berry phase [152] are reported as the origin of negative longitudinal MR in Dirac semimetals. Nonetheless, there are very few reports on negative transverse MR (NTMR) in Dirac semimetals. Our hypothesis is - the origin of this NTMR is the electrons of the bulk states. In the thicker film, the bulk energy gap is small. Therefore, when Al_2O_3 deposition elevates E_F , it resides inside the bulk conduction band, as shown in **Fig. 5.10(b)**, which results in a massive contribution of electrons from the gapped bulk state. These bulk carriers are the reason behind NTMR in post-ALD thicker film. In addition, due to these bulk carriers, the transport becomes 3D. Consequently, the MR exhibits no SdH oscillations. As the post-ALD thicker film contains only n-type carriers and the transport mechanism is 3D, R_{xy} presents a linear dependence on the magnetic field with a negative slope (**Fig. 5.8(d)**).

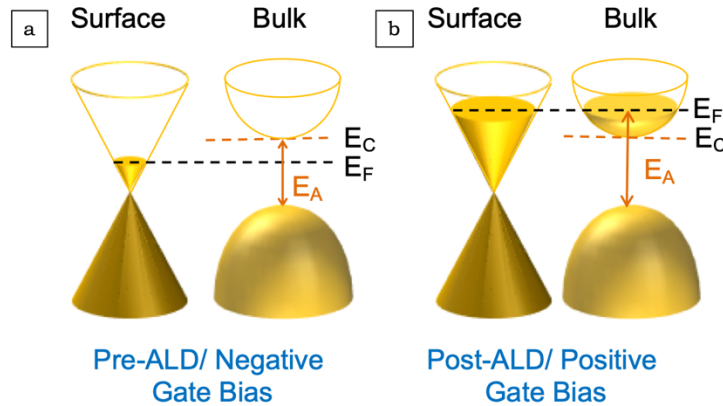


Figure 5.10: Position of the Fermi level in Cd_3As_2 thin films. Schematic of energy band diagram showing activation energy, E_A , for different Fermi levels. (a) When Fermi level resides inside the bulk bandgap, E_A is equivalent to the bulk bandgap. (b) If the Fermi level is inside the bulk conduction band, E_A is the difference between the Fermi level and the top of the bulk valence band.

One way of validating our hypothesis is to study the effect of the position of the Fermi level on MR. By electrostatic gating, it is possible to move the Fermi level inside the film and confirm whether or not the position of the Fermi level and bulk electrons are the reason behind NTMR. **Figure 5.9(a)** shows the gated MR of the thicker film measured at 2K, where the gate voltage is varied from +2 V to -10 V. **Figure 5.9(b)** zooms in on the negative MR region of **Fig. 5.9(a)**. This figure displays negative MR if the gate voltage is -2 V or above. MR becomes positive for the entire range of the magnetic field when the gate voltage is below -2 V. This experiment is consistent with our initial hypothesis. When the gate voltage is -2 V or above, E_F resides inside the bulk conduction band and increases bulk electron density. These bulk electrons lead to an NTMR in the thicker film. On the other hand, when the gate voltage is below -2 V, E_F dropped into the bulk energy gap, and thus MR became positive. This change in Fermi level and bulk electron contribution is demonstrated in **Fig. 5.10**. The activation energies are also extracted from temperature-dependent sheet carrier densities at different gate voltages, as shown in **Fig. 5.11**. When E_F is inside the conduction band, activation energy is the difference between E_F and the top of the bulk valence band. Therefore, at a higher gate voltage, activation energy is larger than the bulk bandgap, as shown in **Fig. 5.10(b)**. Nevertheless, if E_F is inside the bulk energy gap, activation energy is determined by the bulk energy gap, as shown in **Fig. 5.10(a)**. **Figure 5.11(b)** shows that activation energy initially reduces with negative gate voltage and later flattens to a specific value, equal to the bulk energy gap. This gate voltage-dependent activation energy confirms that when thicker film exhibits NTMR, the Fermi level is inside the bulk conduction band.

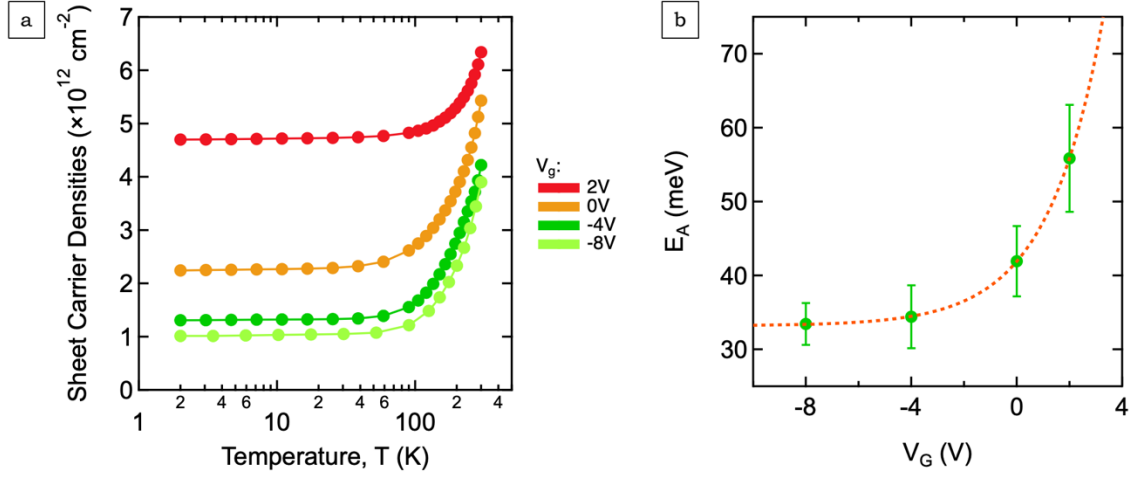


Figure 5.11: Gate voltage-dependent activation energy in Cd_3As_2 thin film. (a) Sheet carrier density of the film as a function of temperature for different gate voltages. (b) The activation energy of the film for different gate voltages extracted from temperature-dependent sheet carrier density.

From thickness-dependent and gated magnetotransport experiments, it is evident that the electrons of the gapped bulk states are the reason behind NTMR in Cd_3As_2 films. These experiments, however, do not reveal the mechanism or physics of this NTMR. There are several possible mechanisms behind negative MR in a topological material:

First, the chiral anomaly can exhibit negative MR in a Dirac semimetal. The magnetic field breaks the time-reversal symmetry of the Dirac material and makes it a Weyl semimetal. This topological phase transition can introduce negative MR through the chiral anomaly. Nonetheless, that can only happen for a longitudinal magnetic field, which is not the case here.

Second, there are few reports of NTMR in topological insulators introduced by disorder [153]. Disorder can introduce charge puddles, which leads to NTMR. Although the disorder in an MBE-grown Cd_3As_2 thin film should be very low. Furthermore, the effect of the disorder should be more prominent in thinner films. Contrarily, we observe NTMR in a thicker film and when the sheet carrier densities are high. Higher sheet carrier densities should further minimize the effect of disorder.

And last but not least is the effect of the Berry phase. The Berry curvature diverges near the band edges. Therefore, when E_F is inside or near the bulk conduction band, Berry curvature can introduce negative MR. This picture is consistent with our experiments. **Figure 5.9(b)** shows that MR becomes more negative when the gate voltage is lowered from 2 V to 0 V. Below this gate voltage, the negative MR component starts to reduce, and below -2 V, MR became completely positive. This change in negative MR implies that when E_F moves toward the band edge, NTMR became more pronounced due to the divergence in Berry curvature. Furthermore, when the MR transitions from negative to positive, the figure shows that the critical magnetic field is reduced when the gate voltage is lowered. This gradual change in the critical magnetic field is due to the lower contribution of the bulk electrons at a lower gate voltage.

5.3 Conclusion

In summary, both electronic band structure and electronic transport properties of Cd_3As_2 thin films vary with film thickness. Although bulk Cd_3As_2 is a 3D Dirac semimetal, a bandgap opens up in the bulk region of epitaxial films due to quantum confinement. Nonetheless, a

topologically non-trivial 2D Dirac state exists on its surfaces. Due to these topologically non-trivial energy states, Cd_3As_2 films display interesting magnetotransport characteristics. The Berry phase effect leads to a negative transverse magnetoresistance in Cd_3As_2 thin films. The effect of the Berry phase can be tuned by altering the film thicknesses or shifting the Fermi level.

Chapter 6

Cd₃As₂ Channel Field-Effect Transistors for Terahertz Applications

Transistors operating in the terahertz (THz) frequency regime are required for future communication, sensing, and imaging applications. THz transistors have the potential to be the central component of the progress of next-generation mobile wireless systems and autonomous vehicles. THz transistors, however, impose extreme requirements on the electronic properties of the channel material. As RF transistors are ultra-scaled to ensure low carrier transit time, THz performances of these transistors are limited by intrinsic carrier velocities and not by low-field carrier mobilities. Additionally, these transistors are required to drive high drain current to minimize charging and discharging time. Therefore, a good channel material should accommodate high sheet carrier densities with high carrier velocities. These requirements will enhance the gain of the transistor, reduce the R-C delay and ensure THz performance. Although high mobility semiconductors can provide high carrier velocities and low contact resistance, they have a low density-of-states (DOS). As a result, the THz field-effect transistor (FET) warrants a new type of channel material with a unique energy band structure. One such material is graphene, which is a 2D material with high Fermi velocity. Nonetheless, the performances of graphene-based FETs are severely limited by high contact resistances and defect scattering. Another suitable candidate for THz FET are 3D topological Dirac semimetals, such as Cd₃As₂. The previous two chapters discussed the electronic

properties of Cd_3As_2 thin films, such as electronic transport and electronic band structures of thin films. The unique electronic properties of Cd_3As_2 , such as high Fermi velocity, high electron mobility, and high density-of-states, fulfill all the requirements of a THz FET. This chapter explores the prospect of Cd_3As_2 as a channel of a THz FET. Moreover, this chapter details the first experimental demonstration of Cd_3As_2 channel FET.

Some of the results presented in this chapter have been published in OF Shoron et al. [109] and OF Shoron et al. [155].

6.1 Comparison of the Electronic Properties of Cd_3As_2 and High Electron Mobility Semiconductors

To take full advantage of Cd_3As_2 FETs, it is important to understand the fundamental differences in transport properties between Cd_3As_2 and high electron mobility semiconductors. Cd_3As_2 has linear energy dispersion, whereas traditional semiconductors exhibit near-parabolic energy bands. This difference in energy dispersion alters several key transport characteristics. These differences should be taken into account to examine the prospect of Cd_3As_2 FETs for THz applications. This section compares the relevant properties of Cd_3As_2 and high electron mobility semiconductors.

6.1.1 Average Forward Velocity of Carriers

Figure 6.1 illustrates the forward momentum components of a 2D Fermi circle. Each point of this semi-circle represents a state of an electron that has a specific positive (or forward) velocity. The average of all these velocities determines the average forward velocity ($v_{avg,Fwd}$)

of the carriers in a channel. $v_{avg,Fwd}$ determines the current of a planar FET. $v_{avg,Fwd}$ of a 2D state can be calculated using the following equation –

$$v_{avg,Fwd} = \frac{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} v(k) k \cos\theta dk d\theta}{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} k dk d\theta} \dots\dots\dots (6.1)$$

where k is the crystal momentum, k_F is the crystal momentum at the Fermi energy, $v(k)$ is the carrier velocity of the state k , and θ is the angle between the velocity and x-axis.

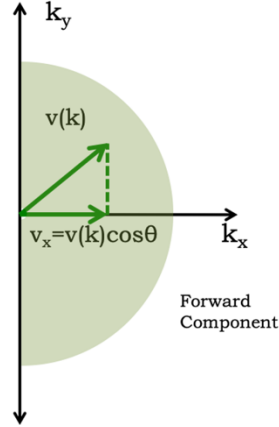


Figure 6.1: Average forward velocity. Fermi semi-circle with only forward crystal momentum.

Average forward velocity can be computed by averaging the velocities of all these states.

In a semiconductor, assuming a parabolic energy band, the velocity of the carriers can be written as -

$$v(k) = \frac{\hbar k}{m^*} \dots\dots\dots (6.2)$$

where $\hbar$ is the reduced Planck constant, and m^* is the effective mass of the carriers. $v_{avg,Fwd}$ of a 2D state with a parabolic band can be calculated by combining **Eqn. 6.1 & 6.2** –

$$v_{avg,Fwd} = \frac{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} \frac{\hbar k}{m^*} k \cos\theta \, dk \, d\theta}{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} k \, dk \, d\theta} = \frac{4}{3\pi} v_F \dots \dots \dots (6.3) \quad (2D \text{ Parabolic Band})$$

where $v_F (= \frac{\hbar k_F}{m^*})$ is the velocity of the carrier at the Fermi energy, also known as the Fermi velocity.

Cd₃As₂ thin films have 2D Dirac nodes at the surface, which exhibit linear energy dispersion. Additionally, unlike semiconductors, the velocity of a Dirac fermion is independent of crystal momentum. These differences give a different $v_{avg,Fwd}$ for a 2D Dirac state as follows -

$$v_{avg,Fwd} = \frac{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} v_F k \cos\theta \, dk \, d\theta}{\int_{-\pi/2}^{\pi/2} \int_0^{k_F} k \, dk \, d\theta} = \frac{2}{\pi} v_F \dots \dots \dots (6.4) \quad (2D \text{ Dirac Band})$$

In a 2D Dirac band, all the carriers have the same velocity - v_F . From **Eqn. 6.2 & 6.4**, it is evident that carriers in a 2D Dirac band can achieve a 50% higher average forward velocity compared to a parabolic band for the same Fermi velocity. Consequently, a Dirac semimetal channel has the potential to drive a higher current density. Furthermore, higher average forward velocity should significantly lower the carrier transit time. High current density along with lower carrier transit time should boost the RF performance of a FET. As Cd₃As₂ surface has 2D Dirac states, Cd₃As₂ FETs have the potential to exhibit excellent RF performances.

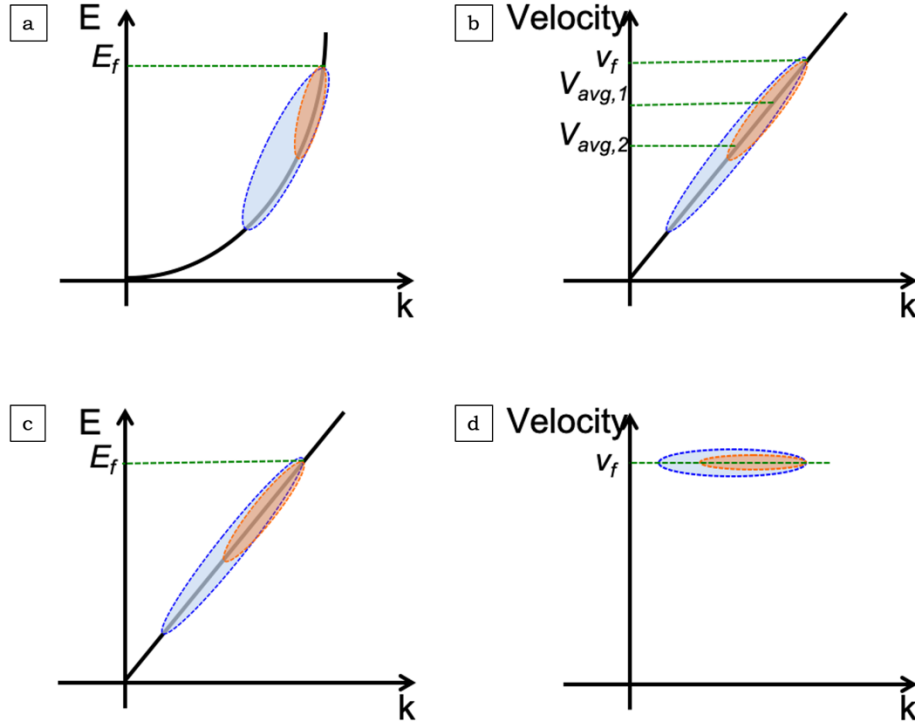


Figure 6.2: Density dependent average carrier velocity. (a) E - k dispersion diagram [155] and (b) crystal momentum-dependent velocity in a parabolic band [155]. (c) E - k dispersion diagram and (d) crystal momentum-dependent velocity in a Dirac (linearly dispersive) band. In a parabolic band, average velocity is lower for higher sheet carrier densities. Contrarily, velocity is independent of the crystal momentum, energy, and sheet carrier density in a Dirac band.

6.1.2 Sheet Carrier Density Dependent Average Carrier Velocity

The room temperature saturation velocity of a material is generally limited by optical phonon scattering. Therefore, the highest possible Fermi energy of a material is determined by the optical phonon energy associated with that scattering. **Figure 6.2(a)** illustrates two different sheet carrier densities in a parabolic energy band at a large lateral electric field. The highest

energy and velocity of the carriers are set by optical phonon energy. When sheet carrier densities are small (red circle), most carriers occupy the states near the Fermi energy. Hence, they exhibit higher average saturation velocity. When sheet carrier density is high, carriers are more scattered in the momentum space, and this lowers their average saturation velocity. These phenomena are illustrated in **Fig. 6.2(b)**. Because of this sheet carrier density-dependent average velocity, FETs based on high mobility semiconductors display their best RF performances near the threshold voltage. Just above the threshold voltage, the channel contains a small number of carriers and thus exhibits a higher carrier velocity. A higher drain current, however, degrades the RF performance due to lower carrier velocity in the channel. This drain current-dependent RF performance introduces significant non-linearity in the performance of the transistors, which leads to a significant amount of complexity in the circuit design.

The sheet carrier density-dependent saturation velocity in semiconductors can also be derived analytically. If the maximum and minimum crystal momentum of a sheet carrier density in a 2D parabolic band are k_F and k_i , respectively, the saturation velocity for that sheet carrier density can be written as –

$$v_{sat} = \frac{\int_{-\pi/2}^{\pi/2} \int_{k_i}^{k_F} \frac{\hbar k}{m^*} k \cos\theta dk d\theta}{\int_{-\pi/2}^{\pi/2} \int_{k_i}^{k_F} k dk d\theta} = \frac{4\hbar}{3\pi m^*} \frac{k_F^3 - k_i^3}{k_F^2 - k_i^2} = \frac{4\hbar}{3\pi m^*} \frac{k_F^2 + k_i^2 + k_F k_i}{k_F + k_i} \dots\dots (6.5)$$

Equation 6.5 implies that saturation velocity increases with k_i . That means when minimum crystal momentum is close to k_F , which means a smaller sheet carrier density, the saturation velocity is maximized. In a Dirac band, all the carriers have the same velocity, irrespective of

the momentum, the Fermi level, or the energy. Because of this, the saturation velocity is independent of the sheet carrier densities in a 2D Dirac band. These phenomena are illustrated in **Fig. 6.2(c,d)**. As the saturation velocity of a 2D Dirac band is independent of the sheet carrier densities, the Cd_3As_2 channel is expected to provide better linearity in FET performance.

6.1.3 Density-of-States of the Channel

Figure 6.3(a) presents the electron mobilities of different semiconductors as a function of effective mass. The figure shows that all the high electron mobility semiconductors have low effective mass. DOS of electrons in a 2D parabolic band can be expressed as –

$$DOS = \frac{g_v m^*}{\pi \hbar^2} \dots \dots \dots (6.6)$$

where g_v is the valley degeneracy. As DOS is proportional to the effective mass of the carriers, the low effective mass of electrons in a high electron mobility semiconductor results in a low DOS (**Fig. 6.3(a)**). Additionally, the DOS is independent of the energy in a 2D parabolic band. Therefore, tuning the DOS using an external bias becomes challenging. Furthermore, most high electron mobility semiconductors are direct bandgap semiconductors, featuring only one valley in the first Brillouin zone, which also leads to a low DOS. This phenomenon is called the "DOS bottleneck" of the high electron mobility semiconductors [168]. This bottleneck results in low internal transconductance, high contact and access region resistances, and low drain current, which severely limit the RF performance of traditional FETs.

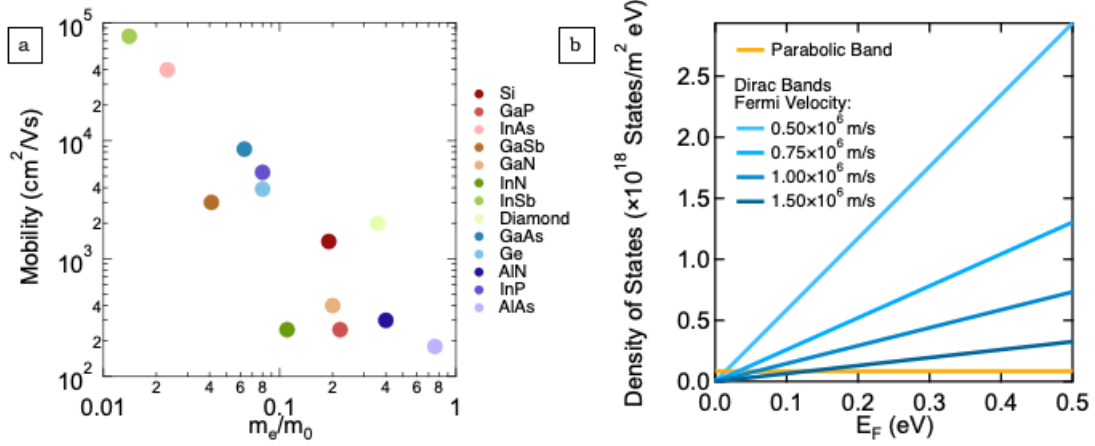


Figure 6.3: Density-of-states bottleneck in high electron mobility semiconductors. (a) Room temperature mobility vs. effective mass of different semiconductors [141,156-167]. High mobility semiconductor exhibits low effective mass, resulting in a low density-of-states. **(b)** The calculated density-of-states of a 2D Dirac band and a 2D parabolic band for different Fermi energies. 2D Parabolic band shows a flat and low density-of-states, whereas 2D Dirac band displays a tunable density-of-states. Different Fermi velocities are considered for this calculation.

The fermions in a 2D Dirac state follow a linearly dispersive energy-momentum relation –

$$E(k) = \hbar v_F k \dots \dots \dots (6.7)$$

The 2D sheet carrier density, n_s of a Dirac semimetal with 2D Dirac nodes at the surface is formulated as follows –

$$n_s(E_F) = \frac{g_v E_F^2}{2\pi \hbar^2 v_F^2} \dots \dots \dots (6.8)$$

where g_v is the number of Dirac nodes of the Dirac semimetal, and E_F is the Fermi energy.

Therefore, the DOS of a 2D Dirac state can be written as follows –

$$DOS(E_F) = \frac{dn_s}{dE_F} = \frac{g_v E_F}{\pi \hbar^2 v_F^2} \dots \dots \dots (9)$$

Unlike the parabolic energy band, the DOS of a 2D Dirac state is a linear function of E_F .

Figure 6.3(b) demonstrates the DOS of a Dirac semimetal with two Dirac nodes (like Cd_3As_2) as a function of E_F with respect to Dirac point (DP) for different v_F . The plot also shows the DOS of a 2D parabolic band, assuming an effective mass of $0.02m_0$. This calculation reveals that the 2D Dirac states have a DOS much higher than traditional high electron mobility semiconductors. Moreover, the valley degeneracy enhances the DOS in a Dirac semimetal. Besides, the DOS of a 2D Dirac state can be adjusted by tuning E_F . Consequently, a Cd_3As_2 channel should accommodate relatively high sheet carrier density. The experimental section of this chapter discusses Cd_3As_2 thin films with relatively high sheet carrier densities. It also details how a high DOS translates into high current density and low contact resistances in Cd_3As_2 devices. High current density and low contact resistances might play a vital role in the designing of THz transistors using a Cd_3As_2 channel.

6.2 Prospect of Cd_3As_2 for THz applications

Two important parameters of a MOSFET for RF applications are the current gain cutoff frequency (f_T) and the external transconductance ($g_{m,ext}$). f_T ensures high operating frequency while $g_{m,ext}$ boosts both f_T and the gain of the MOSFET. This section details an analytical

model to explore the prospect of RF performances of Cd_3As_2 FET (**Fig. 6.4(a)**) for THz application. Moreover, this section explains how the unique band structure and the transport properties of Cd_3As_2 can lead to a linearity in Cd_3As_2 FET.

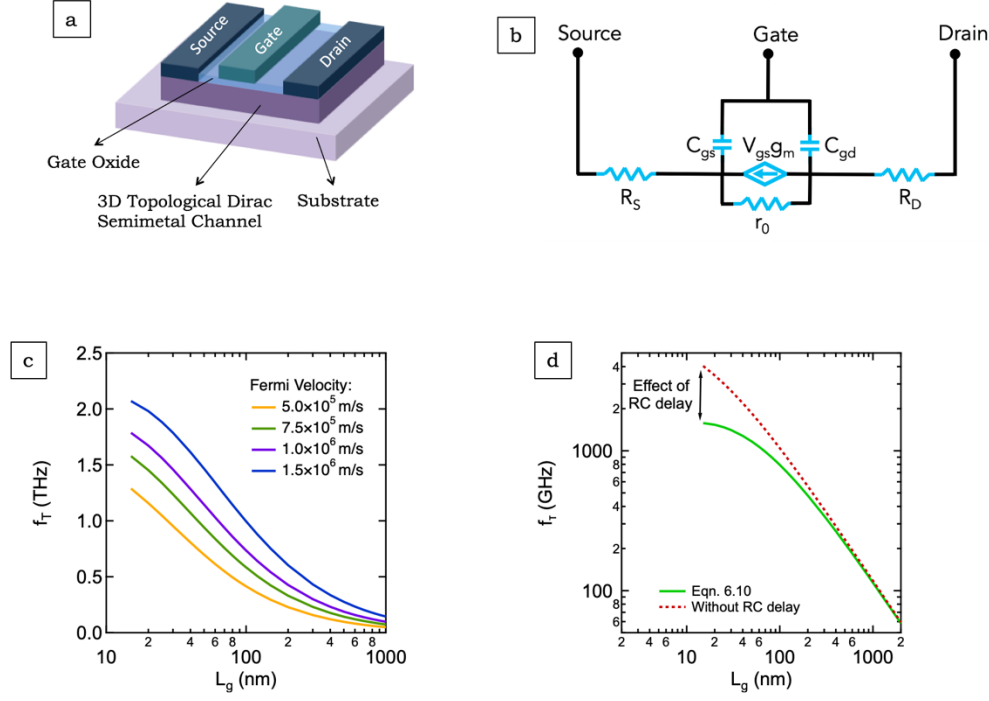


Figure 6.4: Cd_3As_2 field-effect transistors for thz applications. (a) Schematic diagram of a Cd_3As_2 FET. (b) Small-signal circuit model of a FET. (c) Calculated current cutoff frequencies of a Cd_3As_2 FET as a function of the gate length. Four different Fermi velocities are used for the calculations. (d) The calculated current cutoff frequency of a Cd_3As_2 FET using a Fermi velocity extracted from current-voltage characteristics. Ultra-scaled Cd_3As_2 has the potential to achieve a cutoff frequency over 1 THz. Moreover, R-C delays are more significant in ultra-scaled FETs.

6.2.1 RF Performance of Cd_3As_2 FETs

The analytical expression of f_T of a MOSFET is derived from a small-signal circuit model shown in **Fig. 6.4(b)**. The analytical expression of f_T can be written as:

$$\frac{1}{2\pi f_T} = \frac{C_{gs}}{g_{m,i}} \left(1 + \frac{R_S + R_D}{r_0}\right) + \frac{C_{gd}}{g_{m,i}} \left(1 + \frac{R_S + R_D}{r_0}\right) + C_{gd}(R_S + R_D) \dots \dots \dots (6.10)$$

where C_{gs} and C_{gd} are the capacitances between gate-to-source and gate-to-drain, respectively, R_S , R_D , and R_g are the source, drain and gate resistances, respectively, $g_{m,i}$ is the intrinsic transconductance, and r_o is the output resistance of the MOSFET. RF performance of any MOSFET can be estimated by inserting device and material parameters in **Eqn. 6.10**.

C_{gs} has three different components – gate oxide capacitance (C_{ox}), capacitance due to the DOS (C_{DOS}), and fringing capacitance ($C_{gs,f}$). C_{ox} and C_{DOS} are in series and form the channel capacitance, and $C_{gs,f}$ is parallel with the channel capacitance. C_{gd} has only a fringing component ($C_{gd,f}$). C_{gs} of a transistor can be written as –

$$C_{gs} = \frac{C_{ox} + C_{DOS}}{C_{ox}C_{DOS}} + C_{gs,f} \dots \dots \dots (6.11)$$

C_{ox} of a transistor depends on the permittivity and the thickness of the gate oxide and is expressed as –

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \dots \dots \dots (6.12)$$

C_{DOS} depends on the DOS of the channel material and can be written as –

$$C_{DOS} = q^2 DOS \dots \dots \dots (6.13)$$

As shown in **Eqn. 6.9**, the DOS of a Dirac semimetal like Cd₃As₂ is different from a traditional semiconductor. C_{DOS} of a Cd₃As₂ channel of a MOSFET can be expressed as –

$$C_{DOS}(E_f) = q^2 \frac{g_v E_F}{\pi \hbar^2 v_F^2} \dots \dots \dots (6.14)$$

The intrinsic transconductance, $g_{m,i}$ of a MOSFET can be calculated by differentiating the drain current, I_D with respect to the internal gate voltage, $V_{g,i}$ [168]-

$$g_{m,i} = \frac{dI_D}{dV_{g,i}} = q\Gamma(E_F) \frac{I_D(E_F + \Delta E_F) - I_D(E_F)}{\Delta E_F} \dots \dots \dots (6.15)$$

where

$$\Gamma(E_F) = \frac{\Delta E_F}{q\Delta V_{g,i}} = \frac{C_{ox}}{C_{ox} + C_{DOS}(E_F)} = \frac{\frac{v_F^2}{E_F}}{q^2 \frac{g_v}{\pi \hbar^2 C_{ox}} + \frac{v_F^2}{E_F}} \dots \dots \dots (6.16)$$

where q is the charge of an electron. To calculate $g_{m,i}$, I_D needs to be known, and the I_D of a MOSFET can be calculated by using the following equation –

$$I_D(E_F) = q v_{avg,FWD} n_s(E_F) \dots \dots \dots (17)$$

where $v_{avg,FWD}$ is the average forward velocity of the 2D sheet carrier density. Therefore, $g_{m,i}$ can be rewritten as -

$$\begin{aligned}
g_{m,i} &= q^2 v_{avg,FWD} \frac{\frac{v_F^2}{E_F}}{q^2 \frac{g_v}{\pi \hbar^2 C_{ox}} + \frac{v_F^2}{E_F}} \frac{n_s(E_F + \Delta E_F) - n_s(E_F)}{\Delta E_F} = q^2 v_{avg,FWD} \frac{\frac{v_F^2}{E_F}}{q^2 \frac{g_v}{\pi \hbar^2 C_{ox}} + \frac{v_F^2}{E_F}} DOS \\
&= q^2 v_{avg,FWD} \frac{\frac{v_F^2}{E_f}}{A + \frac{v_F^2}{E_F}} \frac{g_v E_F}{\pi \hbar^2 v_F^2} \dots \dots \dots (6.18)
\end{aligned}$$

$v_{avg,FWD}$ of a Dirac semimetal is derived in **Eqn. 6.4**. Carriers in a Dirac node have 1.5 times higher average velocity compared to a traditional semiconductor with a similar v_F . Moreover, unlike traditional semiconductors, v_F of a Dirac node is independent of E_F or n_s . As a result, a Cd₃As₂ channel FETs should exhibit better RF performance for a wide range of I_D and E_F (or V_g). The final expression of $g_{m,i}$ of a Cd₃As₂ FET can be written as –

$$g_{m,i} = \frac{\frac{v_F^2}{E_f}}{A + \frac{v_F^2}{E_f}} \frac{8g_v E_F q^2}{\pi^2 \hbar^2 v_F} = \frac{2g_v q^2}{\pi^2 \hbar^2} \frac{1}{\frac{A}{v_F} + \frac{B}{\sqrt{n_s}}} \dots \dots \dots (6.19)$$

where

$$A = q^2 \frac{g_v}{\pi \hbar^2 C_{ox}} \dots \dots \dots (6.20)$$

$$B = \left(\frac{g_v}{2\pi} \right)^{1/2} \dots \dots \dots (6.21)$$

Additionally, $g_{m,ext}$ of a Cd₃As₂ FET can be estimated by using the following relation –

$$g_{m,ext} = \frac{g_{m,i}}{1 + R_S g_{m,i}} \dots \dots \dots (6.22)$$

The values of f_T and $g_{m,ext}$ for Cd₃As₂ FETs are calculated by inserting the material and device parameters in **Eqn. 6.10-6.22**. The device and material parameters used in these calculations are shown in **Table 6.1**. The device parameters that are not channel material-dependent are consistent with traditional highly scaled RF MOSFETs reported in the literature [169]. Our own experimental data extracted from Cd₃As₂ thin films and devices are used as material parameters. Moreover, the calculations are carried out for different Fermi velocities. Therefore, the discussion of this section is valid for any Dirac semimetal or topological insulator with 2D Dirac nodes at the surface. Unless mentioned otherwise, the gate length of the device used in this calculation is 15 nm.

Table 6.1: Values of different structural and material parameters (* used for **Fig. 6.4(c,d)**)

C_{barrier}	C_{WF}	$C_{\text{gs,f}}$	$C_{\text{gd,f}}$	R_S	R_D	n_s^*
(F/m ²)	(F/m ²)	(F/m)	(F/m)	(Ωm)	(Ωm)	(m ⁻²)
0.085	0.576	2.5×10^{-10}	1×10^{-10}	1.5×10^{-4}	1.5×10^{-4}	4.5×10^{16}

Figure 6.4(c) presents the calculated f_T of Cd₃As₂ FETs as a function of gate length for a wide range of v_F . The calculations reveal that ultra-scaled Cd₃As₂ FET can be operated in the THz frequency regime for a wide range of v_F . According to **Eqn. 6.19**, $g_{m,i}$ increases with both v_F and n_s . According to **Eqn. 6.8**, high values of v_F lower n_s . Therefore, $g_{m,i}$ of a Cd₃As₂ FET is less sensitive to v_F . Lower v_F , however, can increase contact and access region resistances

and thus increase the RC delays of the FETs. **Figure 6.4(d)** shows the effect of RC delay on f_T of a Cd₃As₂ FET. RC time delay becomes significant in the highly scaled devices where RC time delay is a significant fraction of the total transit time. Same resistance values are used for calculating f_T with different v_F . As this is not the case in reality, the effect of v_F on f_T might be more significant than the effect shown in **Fig. 6.4(c)**.

As Cd₃As₂ has no bandgap in the surface states, r_o of a Cd₃As₂ FET should be very low. Therefore, a smaller value of r_o is used for the calculations. In the calculation, the values of r_o are assumed a function of gate length – $2.5 \times 10^4 L_g$ [Ωm], where L_g is the gate length. For a 15 nm gate length device, r_o is $3.75 \times 10^{-4} \Omega\text{m}$, almost equal to R_S and R_D . These assumed values of r_o are very conservative compared to III-V MOSFETs, where r_o is almost one order higher than the assumed values used in this calculation [169]. Besides, this calculation shows that f_T could be above 1 THz even if r_o is three times lower. The transport experiment that is discussed in the next chapter reveals that v_F is over 1.2×10^6 m/s in a Cd₃As₂ thin film. Assuming this v_F , the calculation predicts that Cd₃As₂ FET has the potential to exhibit extremely high current density (over 5 A/mm) with an f_T around 1.6 THz, as shown in **Fig. 6.4(d)**. Furthermore, the calculation expects Cd₃As₂ FET performances to be quite robust against any variation in the device and material parameters.

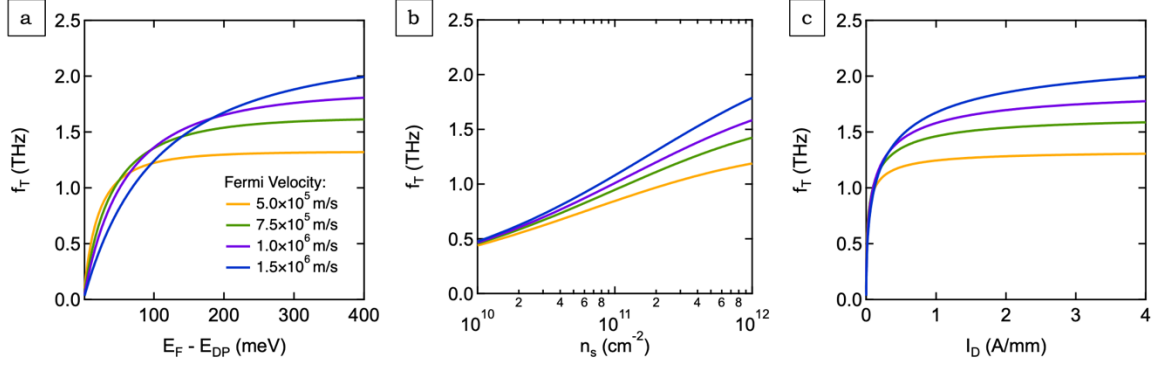


Figure 6.5: Current cutoff frequency of a Cd₃As₂ field-effect transistor. Current cutoff frequency as a function of **(a)** Fermi level **(b)** Sheet carrier densities and **(c)** Drain current. The gate length of the device is 15 nm, and four different Fermi velocities were used for the calculation. The calculation shows robust RF performance of Cd₃As₂ for a wide range of Fermi velocities. Moreover, the calculation shows no drop in f_T at high current density.

6.2.2 Linearity in f_T and $g_{m,ext}$

Linearity of f_T and $g_{m,ext}$ are important factors to design an RF system with low cost and complexity while improving output signal quality. Linearity of these parameters is defined by no roll-off of these parameters with increased gate voltage or drain current. Traditional semiconductor-based RF MOSFETs suffer from non-linearity in f_T and $g_{m,ext}$ [170-172]. The non-linearity in traditional MOSFETs stems from density-dependent carrier velocity in a parabolic energy band, as explained in **Section 6.1.2**. This non-linearity not only reduces the operating frequency but also introduces distortion in output signals. System-level measures need to be taken to mitigate this issue that increases both the cost and the complexity of the systems. According to our analytical model, a Cd₃As₂ channel can offer linearity in both f_T and $g_{m,ext}$.

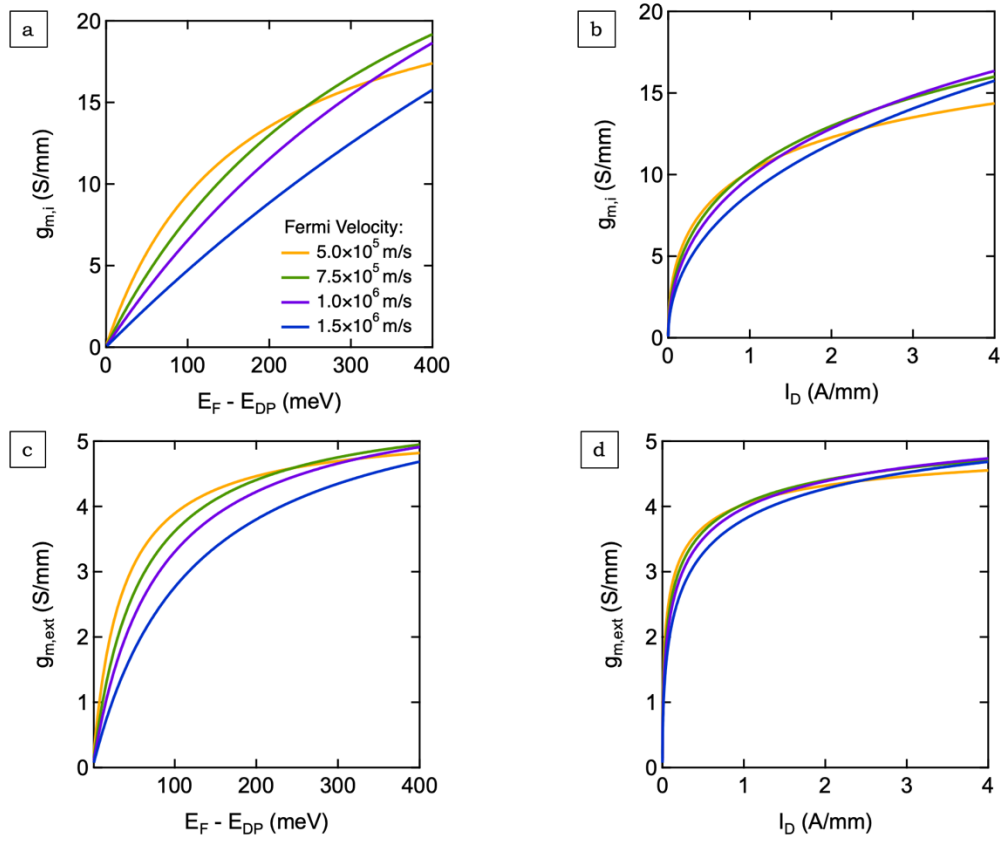


Figure 6.6: Transconductance of a Cd_3As_2 field-effect transistor. Intrinsic transconductance as a function of (a) Fermi level and (b) Drain current. Extrinsic transconductance as a function of (c) Fermi level and (d) Drain current. The gate length of the device is 15 nm, and four different Fermi velocities are used for the calculation.

Figure 6.5 presents the calculated f_T of a Cd_3As_2 FET as a function of the Fermi level, the sheet carrier densities, and the current density. The calculation is carried out for a wide range of v_F . This calculation demonstrates no roll-off in f_T of a Cd_3As_2 FET at a higher Fermi level (gate voltage) or a higher drain current, indicating linearity in f_T . Moreover, **Fig. 6.5(c)** shows that f_T could be above 1 THz even for a lower current density, relaxing the requirement of operating the FET at a higher current density to achieve better RF performance. A low drain

current ensures better thermal management in the devices and improves reliability. Nonetheless, the low sheet carrier density increases access and contact resistances and degrades RF performances. This issue can be quickly resolved by selective area doping in the access and contact regions or by using a gate-recessed FET structure.

High f_T of a Cd_3As_2 FET results from a high internal transconductance, as shown in **Fig. 6.6(a,b)**. **Figure 6.6(c,d)** shows the calculated $g_{m,ext}$ of a Cd_3As_2 EFT as a function of the Fermi level and the drain current. These plots reveal two crucial features. Firstly, calculated $g_{m,ext}$ exhibits linearity, displaying no roll-off at the high gate voltage and drain current. Secondly, the variation in v_F has minimal effect on $g_{m,ext}$. Though high $g_{m,ext}$ depends on high v_F and high DOS, high v_F decreases the DOS, making $g_{m,ext}$ less sensitive to v_F .

It is evident from the calculations based on our analytical model that Cd_3As_2 channel FET can offer THz performances and provide linearity in f_T and $g_{m,ext}$. Taken together, the results presented here suggest that Cd_3As_2 FET could be a central component of future THz technology. These results also warrant further effort to design and develop devices and circuits using Cd_3As_2 FET to explore the full potential of this material. The rest of this thesis describes different experimental techniques to realize functional Cd_3As_2 FETs.

6.3 Cd_3As_2 Field-Effect Transistors

We have developed a process to fabricate FETs on MBE-grown Cd_3As_2 thin films. **Figure 6.7(a)** shows a schematic diagram of an epitaxial structure of a typical Cd_3As_2 (112) thin film used for FET fabrication. Unless stated otherwise, the thickness of the Cd_3As_2 film is 30 nm.

Figure 6.7(b) presents a schematic diagram of a fabricated FET. The fabrication process starts with the Ohmic metal deposition. Optical lithography is used to define the Ohmic contact regions, and e-beam evaporation is used to deposit Au/Pt/Au (200 nm/50 nm/50 nm) metal layers to form Ohmic contacts with the Cd_3As_2 channel. Ar-ion milling is used to isolate the active device areas. 20 nm Al_2O_3 layer is deposited using atomic layer deposition (ALD) to facilitate electrostatic gating. Immediately before the Al_2O_3 deposition, the Cd_3As_2 surface is treated using trimethylaluminum precursor and N^* plasma. This surface treatment lowers the gate leakage and improves carrier mobilities. Detail of this surface treatment is discussed in the next chapter. As the structural quality of Cd_3As_2 degrades at high temperature, Al_2O_3 is deposited at 120 °C. This low-temperature deposition degrades the quality of the gate oxide and the performances of the Cd_3As_2 FETs. After gate oxide deposition, gate regions are defined using optical lithography, and Au/Pt/Au (200 nm/50 nm/50 nm) metal layers are deposited using an e-beam evaporator as gate contacts. **Figure 6.7(c)** illustrates the fabrication process.

A Physical Properties Measurement System (Quantum Design Dynacool) was used for temperature-dependent Hall and FET measurements. Temperature-dependent current-voltage (I - V) characteristics were measured using a Keithley 4200A-SCS parameter analyzer. Room temperature I - V and capacitance-voltage (C - V) characteristics were measured using a HP 4155B and an Agilent B1500A, respectively.

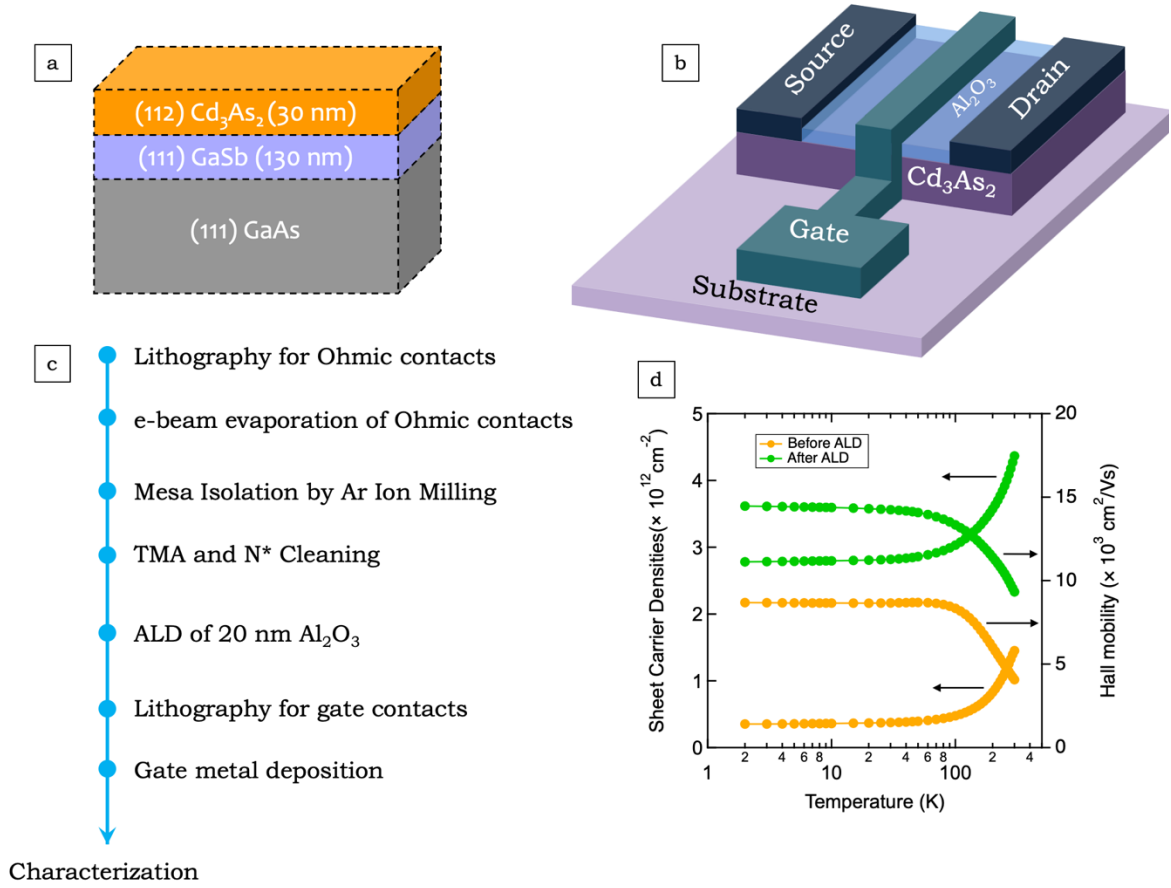


Figure 6.7: Fabrication of Cd₃As₂ field-effect transistor. (a) Epitaxial structure of a Cd₃As₂ thin film, which was used to fabricate FET. (b) Schematic diagram of a Cd₃As₂ FET. (c) Process flow of a Cd₃As₂ FET fabrication. (d) Temperature-dependent sheet carrier densities and electron mobility of the Cd₃As₂ film before and after ALD Al₂O₃ deposition.

6.3.1 Effect of Al₂O₃ on the Transport of Cd₃As₂ Film

Figure 6.7(d) presents the temperature-dependent sheet carrier densities and the carrier mobility in Cd₃As₂ film before and after Al₂O₃ deposition. At room temperature, the pristine sample exhibits sheet carrier density of $1.5 \times 10^{12} \text{ cm}^{-2}$ with Hall mobility of $4,000 \text{ cm}^2/\text{Vs}$. Besides, room temperature sheet carrier density increases after ALD. This is due to the elevation of the Fermi level in post-ALD Cd₃As₂ films, as discussed in **Chapter 5**. Post-ALD

sample exhibits room temperature sheet carrier density of $4.5 \times 10^{12} \text{ cm}^{-2}$. Due to an energy gap in the bulk state, carrier freeze-out is observed in the sample, both before and after ALD, upon lowering the temperature. As 2D Dirac states have higher DOS than parabolic bands, most of the excess carriers introduced by ALD reside in the surface states. Moreover, Al_2O_3 deposition improves the mobility of the film, displaying room temperature mobility of 9,000 cm^2/Vs . As the ALD process increases the fraction of carriers accommodated by high mobility surface states, increased mobility after ALD is expected. Furthermore, surface cleaning also contributes to mobility enhancement.

6.3.2 Ohmic Contacts of Cd_3As_2 Devices

Figure 6.8(a) illustrates the transmission line measurement (TLM) data of two pre-ALD samples with two different Cd_3As_2 film thicknesses. The thicknesses of the films are 30 nm and 65 nm. Although TLM data of a 65 nm film shows a low contact resistance (R_c) of 0.34 $\Omega\cdot\text{mm}$, contact resistance increases in 30 nm film (1.15 $\Omega\cdot\text{mm}$). Thinner films have low sheet carrier densities with low carrier mobilities, which lead to higher contact resistances in thinner films. **Figure 6.8(b)** demonstrates the contact resistance of a post-ALD 30 nm thick Cd_3As_2 film. The TLM data gives contact resistance and specific contact resistance of 4.7 $\text{m}\Omega\cdot\text{mm}$ and $1.9 \times 10^{-9} \Omega \text{ cm}^{-2}$, respectively. Ultra-low contact resistances after ALD are due to the enhancement in sheet carrier densities and carrier mobilities. These contact resistances are comparable to the best III-V RF transistors, which have gone through decades of optimization. More notably, specific contact resistance below $10^{-8} \Omega \text{ cm}^{-2}$ is required for THz application [173,174].

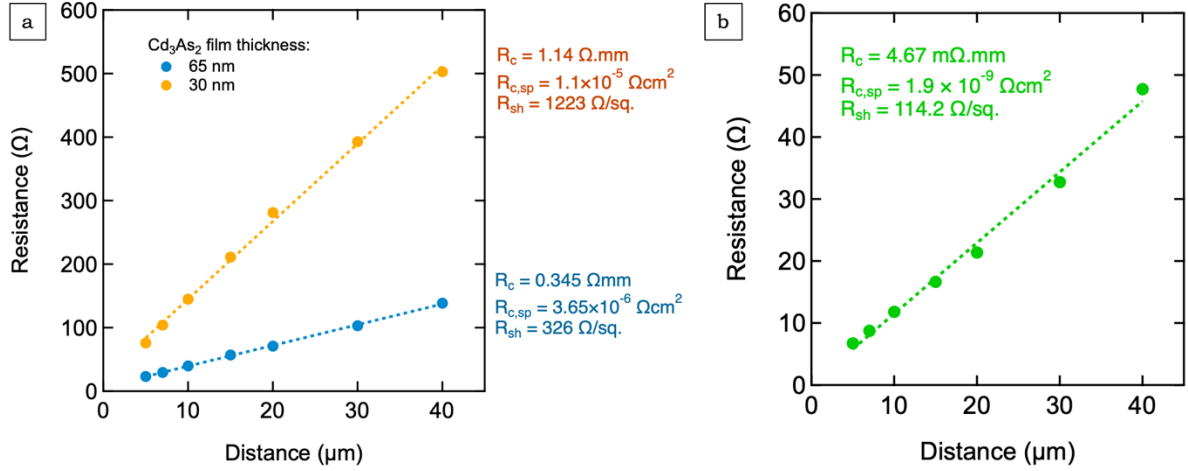


Figure 6.8: Contact resistance of Cd_3As_2 field-effect transistor. (a) TLM measurements of pristine Cd_3As_2 films with the film thickness of 30 nm and 65 nm. (b) TLM measurements of a 30 nm Cd_3As_2 film after Al_2O_3 deposition. The Post-ALD sample shows extremely low contact resistance.

6.3.3 I - V Characteristics of Cd_3As_2 Field-Effect Transistor

Figure 6.9(a) shows an optical image of a Cd_3As_2 FET. It is a narrow channel FET with the channel width, the gate length, and the source-to-drain distance of 2 μm , 3 μm , and 8 μm , respectively. The room temperature drain current vs. gate voltage (I_D - V_G) characteristics of the device for a drain voltage of 2 V are presented in **Figure 6.9(b)**. The I_D - V_G characteristics display a current density of 0.5 A/mm. As the transistor is still operating in a linear regime, increasing the drain voltage should further increase the drain current. Nonetheless, the transistor exhibits very poor current modulation at room temperature. The I_D - V_G characteristics show only 10% current modulation in this particular device.

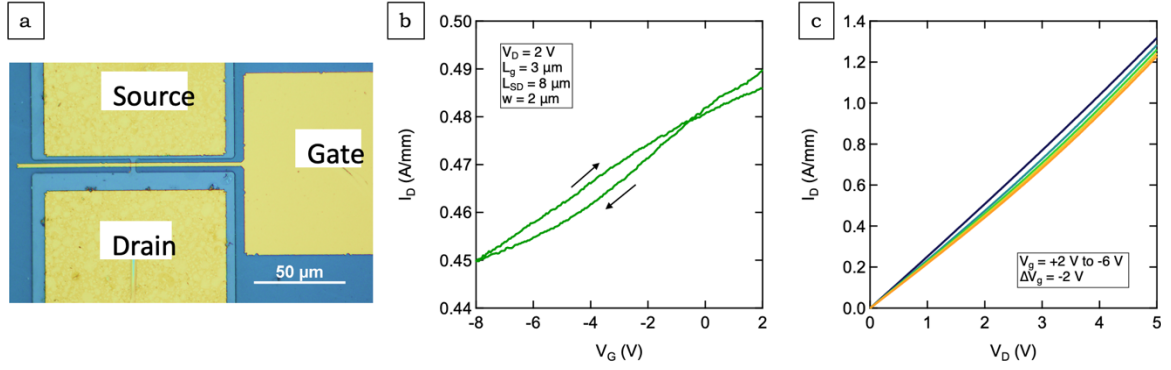


Figure 6.9: First demonstration of Cd₃As₂ field-effect transistor. (a) An optical image of Cd₃As₂ FET. Reprinted from [109] with permission from AIP Publishing. (b) I_D - V_G and (c) I_D - V_D characteristics of the FET.

6.4 Limiting Factors of The Current Modulation in Cd₃As₂ Field-Effect Transistors

There are several factors in the material and the transistor design that contribute to poor room temperature performances of Cd₃As₂ FETs. This section explains different factors that limit the current modulation in a Cd₃As₂ FET.

6.4.1 Screened Bulk Carriers

To understand the factors that limit current modulation in a Cd₃As₂ FET, transistor characteristics are measured of a very long channel ($L_g = 300$ μm) device. As the effect of access and contact resistances is negligible in a very long channel FET, this device might help to unveil the intrinsic limitations of a Cd₃As₂ FET. **Figure 6.10 (a,b)** presents the drain current vs. drain voltage (I_D - V_D) characteristics of this long FET measured at 300 K and 2 K, respectively. These I_D - V_D characteristics reveal that the current modulation improves significantly at low temperatures. Moreover, the I_D - V_D characteristics measured at 2 K

demonstrate the onset of the current saturation at negative gate bias. This result suggests that the current saturation in Cd_3As_2 FET is achievable, even though the surface Dirac states are gapless. **Figure 6.10(c)** shows the I_D - V_G characteristics of the transistor measured at different temperatures (2 K to 300 K). The I_D - V_G characteristics also exhibit improvement in the current modulation at lower temperatures.

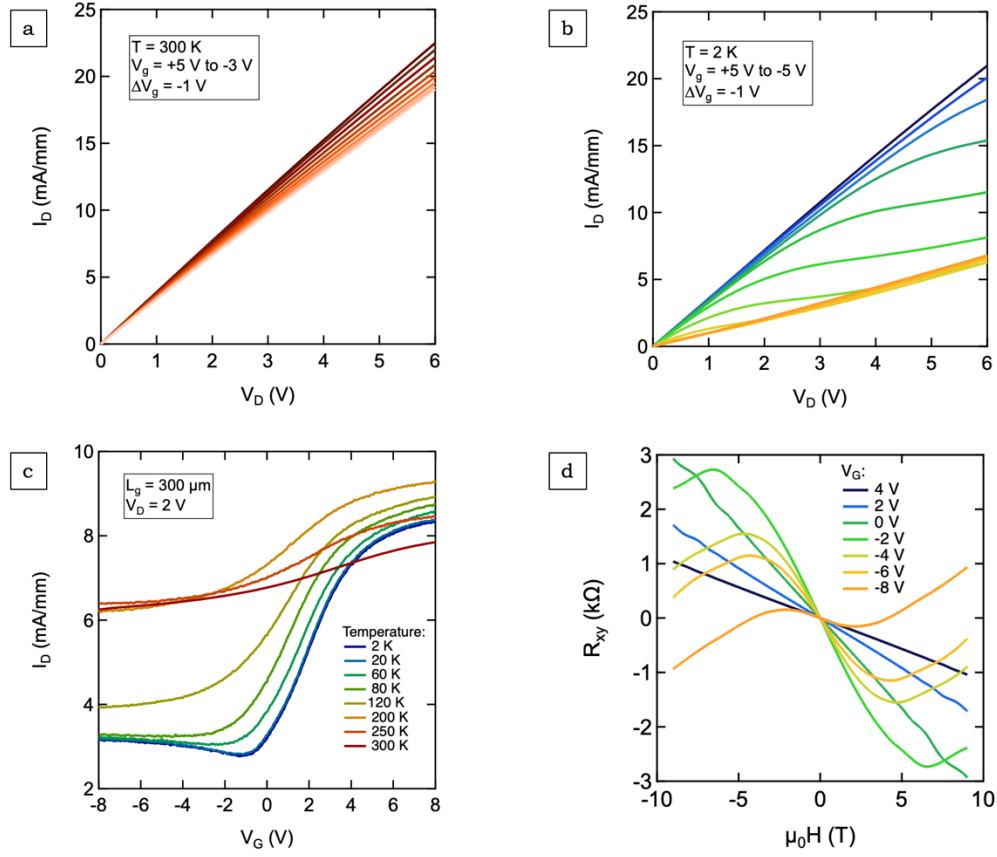


Figure 6.10: Ambipolar transport in Cd_3As_2 field-effect transistor. I_D - V_D characteristics of a 300 μm gate length Cd_3As_2 FET measured at **(a)** 300 K and **(b)** 2 K. **(c)** I_D - V_G characteristics of the transistor measured for a temperature range of 2 K to 300 K. The transistor shows an upturn in the drain current at negative gate voltage, exhibiting ambipolar transport. **(d)** Hall resistance at different gate voltage measured at 2 K. Below -2 V, the Hall measurements exhibit the co-existence of holes and electrons in the channel. *Reprinted from [109] with permission from AIP Publishing.*

Furthermore, low-temperature I_D - V_G characteristics demonstrate an upturn in the drain current when the gate voltage is below -1 V. If the gate voltage is sufficiently negative, the Fermi level goes below the charge neutrality point of the surface Dirac nodes, and the surface states accumulate holes. Accumulation of low mobility holes is the origin of this slight upturn in the I_D - V_G characteristics. **Figure 6.10(d)** exhibits the Hall resistances at different gate voltage measured at 2 K. When the gate voltage is -2 V or below, the sign of the slopes of the Hall resistances switches at a high magnetic field. This change in the sign of the slope is a clear indication of the accumulation of holes at the negative gate bias.

Figure 6.11(a) summarizes the current modulation of two Cd₃As₂ FETs of different gate lengths (10 μm and 300 μm) as a function of temperature. The current modulation is calculated using the following equation –

$$\text{Current Modulation} = \frac{I_{max} - I_{min}}{I_{max}} \times 100 \dots \dots \dots (6.23)$$

Although both devices exhibit flat current modulation at low temperatures, their current modulations start to degrade at 80 K, the same temperature when the bulk carriers start to reappear. This result strongly suggests that one of the limiting factors of the room temperature current modulation in a Cd₃As₂ FET is the thermally activated bulk carriers. The carriers of the surface Dirac states screen most of the transverse electric field, and thus prevent the bulk carriers from being modulated by the gate voltage. As the bulk carrier contribution is negligible in the Cd₃As₂ film below 80 K, the Cd₃As₂ FETs show high current modulation at this temperature regime. The current modulation in a very long channel device is as high as 70%

at a low temperature and it drops from 70% to only 20% at room temperature due to the unscreened bulk carriers.

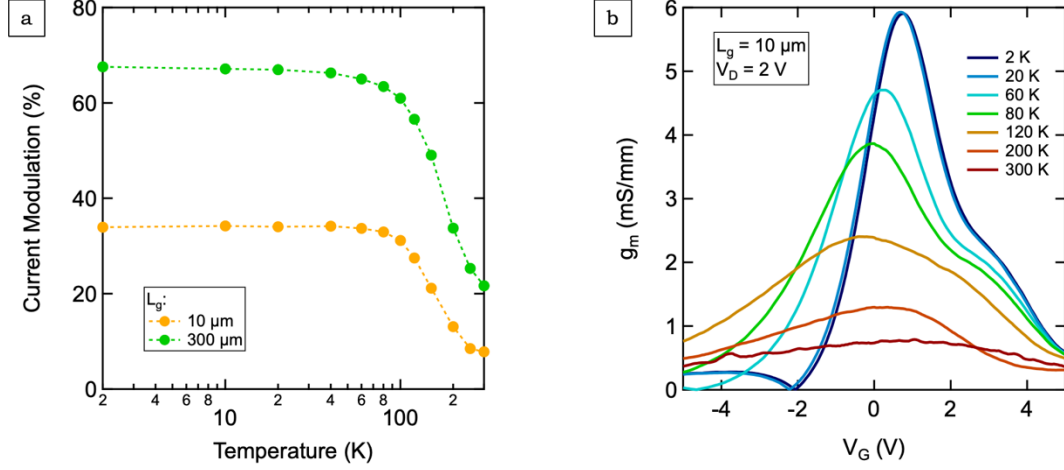


Figure 6.11: Bulk carrier-limited current modulation in Cd_3As_2 field-effect transistor. (a)

Current modulation as a function of temperature. The long channel device shows higher current modulation than a shorter channel device. The current modulation collapses when the temperature is above 80 K. This is due to the accumulation of the carriers in the bulk state. **(b)** The transconductance of a Cd_3As_2 FET measured at different temperatures ranging from 2 K to 300 K.

The shorter channel device exhibits worse performance in terms of current modulation. The 10 μm gate length FET displays a current modulation of 35% and 10% at low temperature and room temperature, respectively. There are two reasons behind the poor current modulation in the shorter channel FETs— the effect of the access and contact resistances and the poor gate control due to trap densities. **Figure 6.11(b)** presents the temperature-dependent transconductances of the 10 μm gate length FET. Transconductance decreases at a higher

temperature. As both current modulation and carrier mobilities degrade near room temperature, lower transconductance near room temperature in a Cd_3As_2 FET is expected.

To improve the room temperature current modulation and transconductance of a Cd_3As_2 FET, the Cd_3As_2 channel should be very thin. The thinner channel has a wider bulk energy gap due to an enhanced quantum confinement effect. The wider bulk energy gap lowers the amount of thermally activated bulk carriers. Furthermore, the thinner channel has a smaller region to accommodate bulk carriers, further reducing bulk carrier contribution at room temperature.

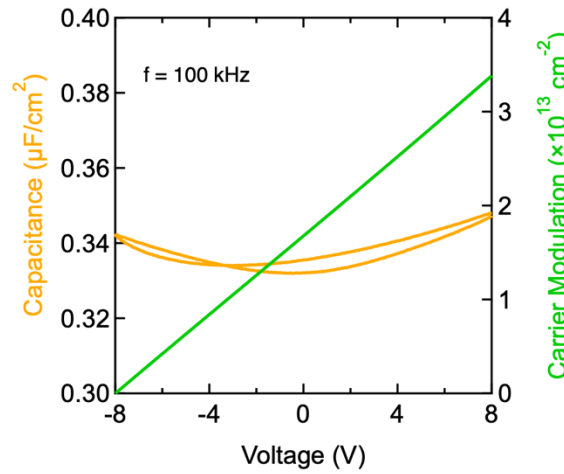


Figure 6.12: Capacitance-voltage characteristics of a Cd_3As_2 field-effect transistor. C - V characteristics exhibit large hysteresis, indicating huge trap densities. The C - V characteristics show much higher charge modulation than the sheet carrier densities.

6.4.2 Interface Trap Densities

As mentioned earlier, Al_2O_3 is deposited in the ALD chamber at 120°C to maintain the structural integrity of the Cd_3As_2 films. The low-temperature Al_2O_3 deposition compromises

the gate oxide quality of Cd₃As₂ FET. This low-quality gate oxide introduces huge trap densities in Cd₃As₂ devices. **Figure 6.12** illustrates the C - V characteristics of a Cd₃As₂ FET. The C - V characteristics exhibit huge hysteresis, indicating large trap densities. Moreover, the plot presents the carrier modulation of the device. Carrier modulation is calculated by integrating the C - V profile. This figure reveals that the number of carriers modulated during the C - V measurements is much higher than the sheet carrier densities of the Cd₃As₂ film. The I_D - V_G characteristics exhibit much lower carrier modulation than the C - V measurements. These discrepancies strongly suggest that most of the gate voltage is employed to fill up or empty immobile trap states instead of modulating the mobile carriers of the channel. These traps have several adverse effects on the transistor performances - poor gate control, lower transconductance, hysteresis in the I - V characteristics, and smaller current modulation. All of these affect both the DC and RF performances of the transistors.

6.4.3 Effect of The Gate Length

The current modulation gives the total change of resistance between the source and the drain with gate voltage. Electrostatic gating only changes the resistance of the region of the channel that is below the gate contact. Other resistances, such as contact resistances and access region resistances, are not altered by gate bias. Therefore, the overall current modulation depends on the gate length. If the gate length is small, other resistances are much higher than the modulated resistance of the channel, which translates into a low current modulation of the transistor.

In the linear regime, the maximum and minimum current of a Cd₃As₂ FET can be written as-

$$I_{D,max} = \frac{V_D}{R_C + R_{access} + (R_{s,ch} - \Delta R_{s,ch})L_g} \dots \dots \dots (6.24)$$

$$I_{D,min} = \frac{V_D}{R_C + R_{access} + R_{s,ch}L_g} \dots \dots \dots (6.25)$$

Here, R_C = contact resistances, R_{access} = resistance of the access regions, $R_{s,ch}$ = sheet resistance of the channel below the gate contact. Therefore, current modulation can be written as –

$$\begin{aligned} \text{Current Modulation} &= \frac{I_{D,max} - I_{D,min}}{I_{D,max}} = \frac{\Delta R_{s,ch}L_g}{R_C + R_{excess} + R_{s,ch}L_g} \\ &= \frac{\text{Resistance Modulation}}{\frac{R_{Add,norm}}{L_g} + 1} \dots \dots \dots (6.26) \end{aligned}$$

where,

$$\text{Resistance Modulation} = \frac{\Delta R_{s,ch}}{R_{s,ch}} \dots \dots \dots (6.27)$$

and

$$R_{Add,norm} = \frac{R_C + R_{excess}}{R_{s,ch}} \dots \dots \dots (6.28)$$

Equation 6.26 indicates that the current modulation increases with the gate length. To verify this hypothesis, we have fabricated Cd_3As_2 FETs with the same source-to-gate and gate-to-drain spacings (5 μm each), whereas the gate length is varied from 5 μm to 40 μm . **Figure 6.13(a)** presents the normalized I_D - V_G characteristics of these devices, and **Fig. 6.13(b)** summarizes the current modulation calculated from the I_D - V_G characteristics. This is quite

evident from this experiment that the current modulation increases significantly in longer channel devices.

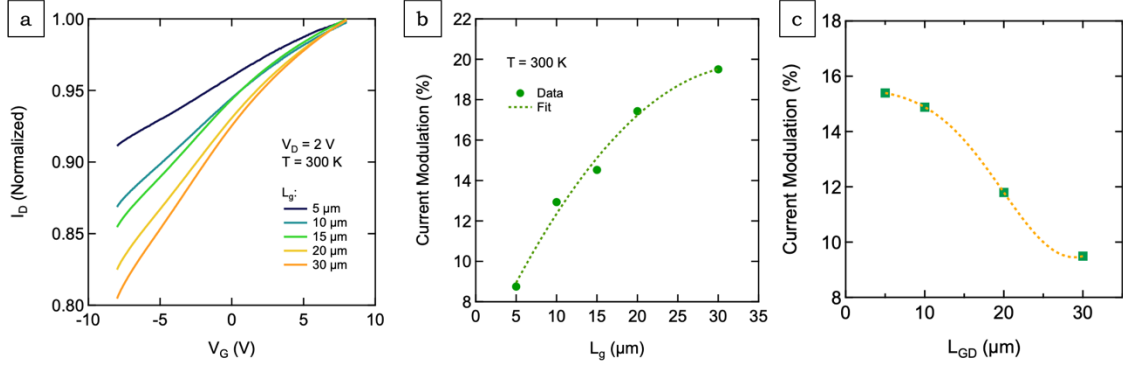


Figure 6.13: Effect of access resistance on current modulation. (a) Normalized I_D - V_G characteristics and (b) Current modulation of Cd_3As_2 FET for different gate lengths. As access region length is the same for all the devices, the effect of access region resistance should be negligible in a longer channel FET. Moreover, longer gate length devices show better gate control, and hence improved current modulation. (c) Current modulation decreases with increased gate-to-drain distance, as it increases access region resistance.

Another takeaway is that the current modulation of a shorter channel device can be improved by lowering the contact and access region resistances. To verify that, we have fabricated FETs where the gate lengths are unchanged, but the gate-to-drain distances (L_{GD}) are varied from 5 μm to 30 μm . The current modulations of those devices are demonstrated in **Fig. 6.13(c)**. This figure exhibits lower current modulation in the devices with a longer L_{GD} . A longer L_{GD} increases the access region resistances, which leads to a lower current modulation.

6.4.4 Effect of Channel Width

Figure 6.14(a) shows the two-terminal current densities as a function of the channel width of Cd_3As_2 FETs for two source-to-drain distances ($8\ \mu\text{m}$ and $10\ \mu\text{m}$). The channel widths of the devices are varied from $2\ \mu\text{m}$ to $100\ \mu\text{m}$. The narrow channel devices exhibit higher current densities. Conducting surface states of the sidewalls, which are intrinsic characteristics of topological semimetals, might have caused higher current densities in narrower channel devices. The effect of sidewall conducting states is more significant in narrow channel devices than a wider channel one. Moreover, sidewall surface states increase the fraction of surface state carriers compared to the bulk carriers, resulting in a higher current modulation in a narrower channel device, as shown in **Fig. 6.14(b)**.

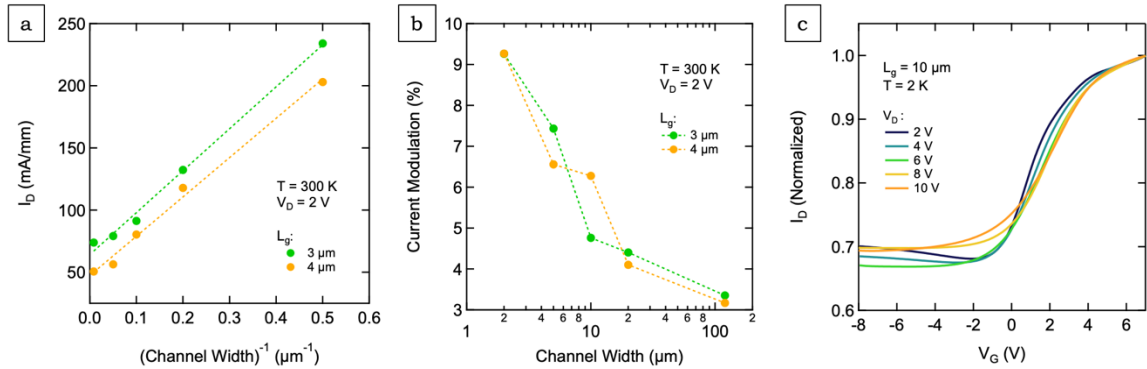


Figure 6.14: Effect of channel width and lateral electric field on Cd_3As_2 field-effect transistor.

(a) Current density and **(b)** Current modulation of Cd_3As_2 FETs for different channel widths. **(c)** The low temperature ambipolar transport of a Cd_3As_2 FET vanishes at higher drain voltage.

6.4.5 Effect of Lateral Electric Field

The performance of a Cd_3As_2 FET depends on the lateral electric field in the device. Due to large trap densities and screened bulk states, the gate has poor control over the channel.

Because of this, the lateral electric field plays a vital role in the device performances. **Figure 6.14(c)** exhibits the normalized I_D - V_G characteristics for different drain voltages measured at 2 K. At a lower drain voltage, the I_D - V_G characteristics show an upturn at a negative gate voltage. This upturn, however, vanishes at a higher drain voltage due to the injection of electrons into the channel at the high lateral field. These excess electrons overwhelms the effect of accumulated holes. The lateral electric field effect can be minimized by reducing trap densities and making the channel thinner.

6.5 Conclusion

As Cd_3As_2 is a Dirac semimetal, there are several vital differences in transport properties between Cd_3As_2 and traditional semiconductors. Unlike traditional semiconductors, Cd_3As_2 can offer higher Fermi velocity, higher average forward velocity, sheet carrier-independent carrier velocity, and higher DOS. All of these properties can be exploited to design Cd_3As_2 channel FETs to achieve excellent RF performances. We have developed an analytical model, which predicts that Cd_3As_2 FET has the potential to achieve f_T over 1 THz. We have also demonstrated the first FET using Cd_3As_2 thin film as a channel. We have also investigated different factors that limit the performance of a Cd_3As_2 FET. Screened bulk carriers, trap densities, access region resistances, channel width, and lateral electric field affect the transistor characteristics of Cd_3As_2 FETs. We believe that novel device structures and material and fabrication engineering are needed to minimize the effect of these performance-limiting factors.

Chapter 7

Enhanced Carrier Control in Cd_3As_2 Field-Effect Transistor

High trap densities are one of the limiting factors of the performance of a Cd_3As_2 field-effect transistor (FET). In addition, device parameters such as contact and access region resistances, gate length, channel width, and channel thicknesses also play a vital role in the device performances. This chapter discusses fabrication techniques that can improve these performance-limiting factors. Moreover, it covers a modified FET structure that can improve current density, transconductance, and current modulation in a Cd_3As_2 FET.

A Physical Properties Measurement System (Quantum Design Dynacool) was used for temperature-dependent Hall measurements. Room temperature current-voltage (I - V) and capacitance-voltage (C - V) characteristics were measured using an HP 4155B and an Agilent B1500A, respectively.

Some of the results presented in this chapter have been published in OF Shoron et al. [155].

7.1 Improved Cd₃As₂-Gate Insulator Interface

Since trap densities severely limit the Cd₃As₃ FET performance, several modifications were made to the Cd₃As₂ FET fabrication process to improve the interface quality between the Cd₃As₂ channel and the gate insulator. This section discusses how these modifications affect transport in the Cd₃As₂ channel and the overall device performance. Unless stated otherwise, all the films used for these experiments are 30 nm Cd₃As₂ (112) films.

7.1.1 Effect of Surface Treatment

Different surface treatment procedures were employed immediately before Al₂O₃ deposition to obtain a cleaner interface between the Cd₃As₂ channel and the gate dielectric (Al₂O₃). Different pieces of the same sample were used for this experiment. Two different surface treatment techniques were carried out to improve interface quality. In one *in-situ* treatment, the surface was cleaned using alternating tetramethyl-aluminum (TMA) and N⁺ plasma pulses in an atomic layer deposition (ALD) chamber and in the other *ex-situ* treatment, the surface was cleaned using N⁺ plasma in an ion beam deposition chamber (IBD). These surface treatments should passivate the surface and remove the native oxide layer that forms upon air exposure [175]. Moreover, these treatments should clean any contaminants deposited on the Cd₃As₂ surface during the fabrication process. A control sample was also fabricated, which underwent no surface treatment, to isolate the effect of these surface treatments. After the surface treatment 20 nm of Al₂O₃ was deposited using ALD at 120 °C. The epitaxial structure of the test sample is shown in **Fig. 7.1(a)**. Hall bar structures were fabricated to study the effect of the surface treatments on the electronic transport of Cd₃As₂ thin films.

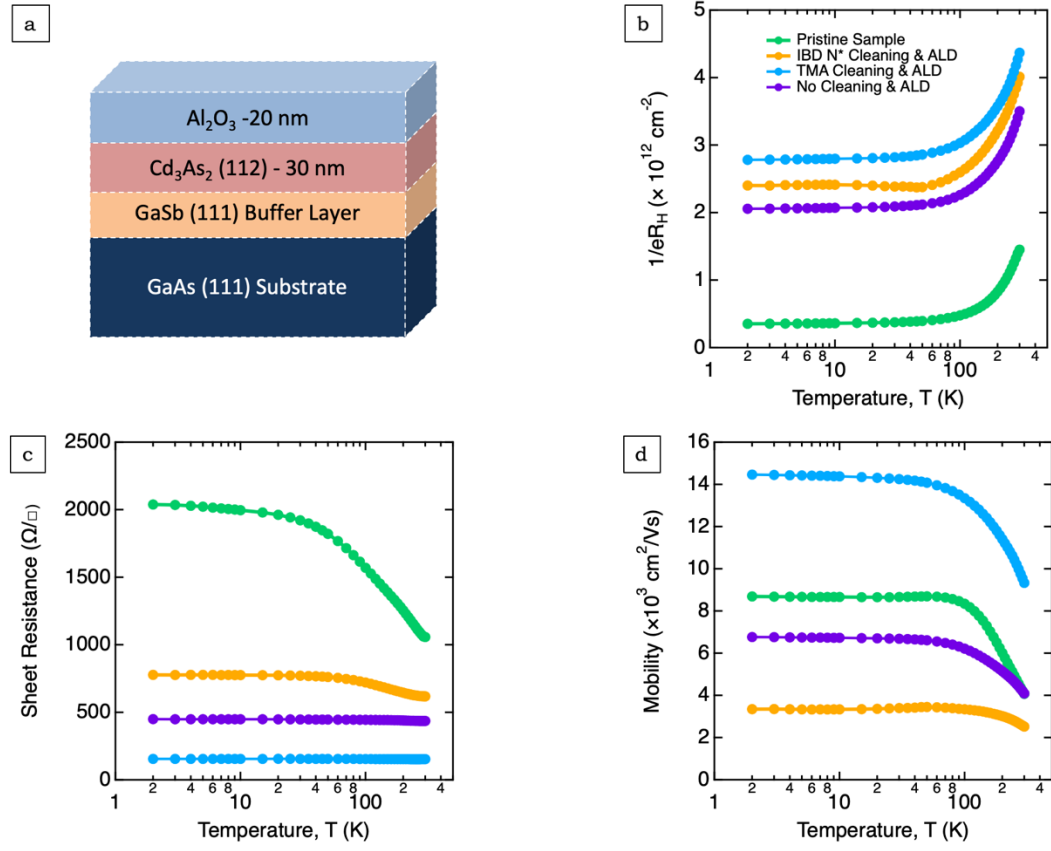


Figure 7.1: Effect of surface treatment on the transport in a Cd₃As₂ channel. (a) Epitaxial Structure of Cd₃As₂ (112) thin film grown on GaAs (111) substrate with a GaSb buffer layer. ALD Al₂O₃ layer is used as the gate insulator. **(b)** The inverse of Hall resistance, **(c)** Sheet Resistance and, **(d)** Electron mobility as a function of temperature for pristine (green) and Al₂O₃ capped samples with and without surface treatments.

Figure 7.1(b) presents the sheet carrier densities as a function of temperature for pristine, surface treated, and control samples. All samples show the expected temperature dependence – bulk carrier freeze-out at about 80 K and a temperature-independent flat sheet carrier density below this temperature. This confirms that the surface treatment and Al₂O₃ deposition processes do not alter the basic electronic structure of Cd₃As₂. Furthermore, post-ALD

samples, whether surface treated or not, exhibit higher sheet carrier densities than surfaces not covered with the dielectric. The surface of a pristine Cd_3As_2 film captures electronegative OH^- species which pulls the Fermi level of a Cd_3As_2 film down [176]. Because of this low Fermi level, Cd_3As_2 films without any surface treatment exhibit relatively low sheet carrier densities. There are several ways to lift the Fermi level. For instance, the N^* plasma treatment utilized in the two surface treatments discussed above reduce the OH^- species on Cd_3As_2 surfaces by passivating surface dangling bonds that otherwise capture OH^- species [176]. Alternatively, OH^- species can be removed by low-temperature thermal annealing of the Cd_3As_2 film in vacuum, which occurs during the deposition of Al_2O_3 at 120 °C. Removal of OH^- species by either method should lift the Fermi level in the Cd_3As_2 films resulting in the observed larger sheet carrier densities, compared to the pristine sample. As the surface treated samples experienced both N^* plasma treatment and annealing, these samples should have the least OH^- species at the Cd_3As_2 surface, which leads to higher sheet carrier densities in the surface treated samples. Nonetheless, surface passivation due to N^* plasma treatment or annealing is not permanent because, in ambient conditions the Cd_3As_2 surface starts to accumulate OH^- species again. That might be a possible reason behind slightly lower sheet carrier densities in IBD N^* treated sample compared to N^* and TMA treated sample since the sample was exposed to atmosphere during transfer from the IBD chamber to the ALD chamber. Exposure to the ambient condition might slightly degrade the surface passivation.

Figure 7.1(c,d) illustrates the temperature-dependent sheet resistance and carrier mobilities of the pristine, surface-treated, and control samples. The IBD N^* plasma-treated sample displays the lowest carrier mobilities. N^* plasma treatment in the IBD chamber is a relatively high-

energy process, which damages the Cd_3As_2 film and leads to low carrier mobilities. In contrast, the TMA and N^* plasma-treated sample demonstrates the highest carrier mobilities. This enhancement in carrier mobilities is due to a combination of surface passivation and surface cleaning. Furthermore, as the vacuum was not broken between surface treatment and Al_2O_3 deposition, this sample should have the minimum native oxide. Additionally, high sheet carrier densities in the TMA and N^* plasma-treated sample might play a role in improving carrier mobilities by reducing scattering.

Higher sheet carrier densities ($4.5 \times 10^{12} \text{ cm}^{-2}$ at room temperature) along with high carrier mobilities ($9,000 \text{ cm}^2/\text{Vs}$ at room temperature) suggest a cleaner interface between Cd_3As_2 and Al_2O_3 after TMA and N^* plasma treatment. This surface treatment also reduces sheet resistances to a very value of only $150 \text{ } \Omega/\text{sq}$ at room temperature. This low sheet resistance is essential to achieve lower contact and access region resistances, which is one prerequisite to operate Cd_3As_2 FETs in the THz frequency range.

TMA and N^* plasma treatment of Cd_3As_2 sample also improves the magnetotransport of Cd_3As_2 thin films. **Figure 7.2** presents the magnetotransport data of the TMA and N^* plasma-treated sample and the control sample. Both samples exhibit a transition from an entirely n-type channel to the coexistence of electrons and holes in the channel with changing gate voltage (**Fig. 7.2(b,d)**). Only the surface-treated sample shows pronounced Shubnikov-de Hass (SdH) oscillations for the whole range of gate voltages, indicating a long quantum lifetime of the carriers. In contrast, the control sample demonstrates SdH oscillations only at a large positive gate bias when sheet carrier densities are high. High sheet carrier densities provide better

screening against scattering to improve quantum lifetime. Therefore, surface treatment of Cd_3As_2 samples is essential not only for improving transistor performance but also for probing the low energy physics of this novel topological material.

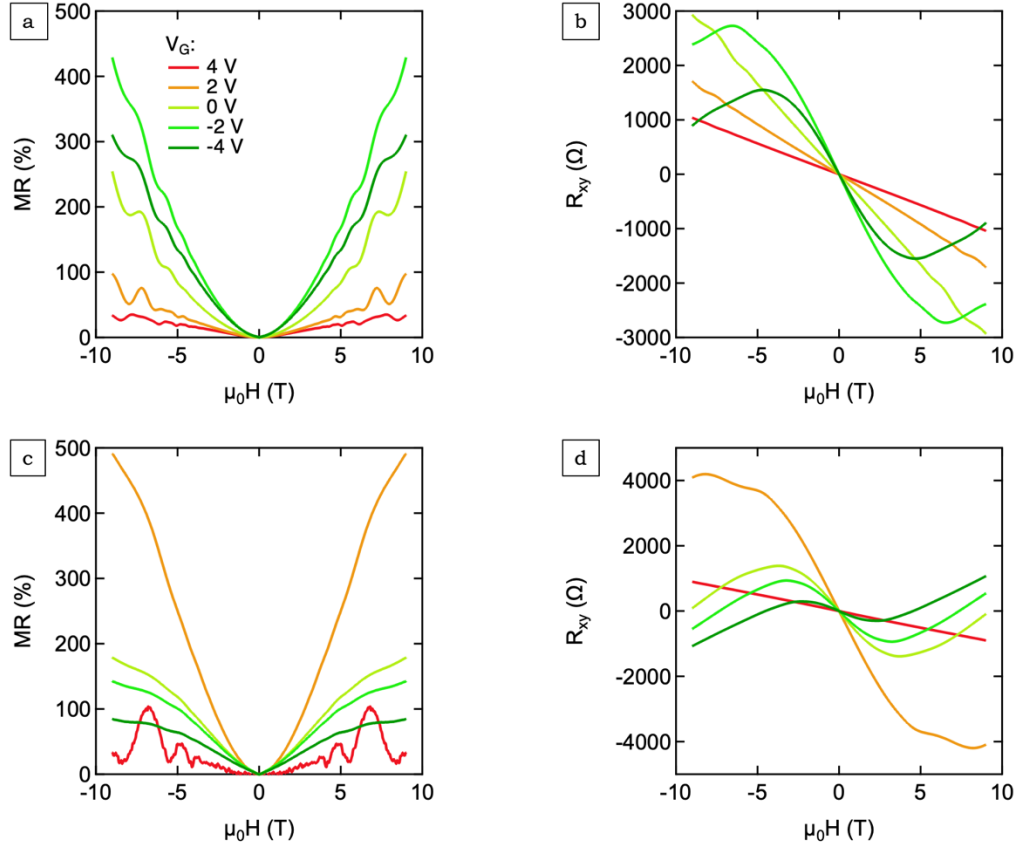


Figure 7.2: Effect of TMA and N^* cleaning on magneto-transport of Cd_3As_2 film. (a) Magnetoresistance and **(b)** Hall resistance of Al_2O_3 capped Cd_3As_2 film with TMA and N^* cleaning as a function of applied magnetic field for different gate voltages. **(c)** Magnetoresistance and **(d)** Hall resistance of Al_2O_3 capped Cd_3As_2 film without any surface treatment as a function of applied magnetic field for different gate voltages.

Table 7.1: Al₂O₃ deposition conditions in ALD (FG = Forming Gas, NA = Not Applicable)

Sample No.	Al Precursor	O Source	Deposition Temperature	Post-ALD Annealing
A	TMA	H ₂ O	120 °C	NA
B	TMA	H ₂ O	120 °C	200 °C in FG
C	TMA	O* Plasma	120 °C	NA
D	TMA	O* Plasma	120 °C	200 °C in FG
E	TMA	H ₂ O	200 °C	NA
F	TMA	O* Plasma	200 °C	NA

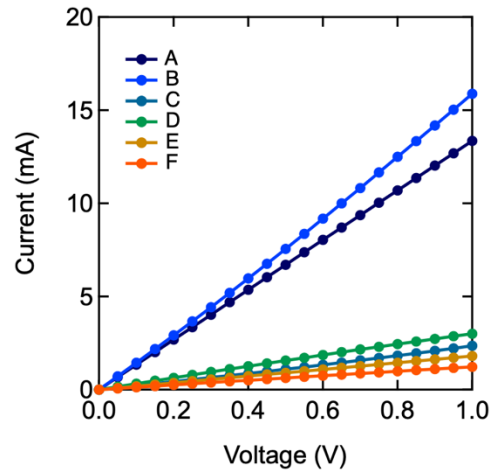


Figure 7.3: Variation in Al₂O₃ deposition method in atomic layer deposition chamber. Current-voltage characteristics of two-terminal devices fabricated on different samples with Al₂O₃ layers. Al₂O₃ layers were deposited and annealed at different conditions, as mentioned in **Table 7.1**. A collapse in current is observed when the Al₂O₃ layer was deposited using O* plasma and/or deposition temperature was 200 °C.

7.1.2 Variation in Al₂O₃ Deposition Method in ALD

Although surface treatment provides a cleaner interface, it cannot resolve the trap density issue as shown in **Chapter 6**. The origin of these traps is the low-temperature deposition of the Al₂O₃ layer. In all the Cd₃As₂ devices discussed so far, Al₂O₃ layers were deposited using TMA and H₂O pulses at 120 °C in the ALD chamber. In this experiment, different Al₂O₃ deposition methods are explored in ALD to find the best Al₂O₃ deposition condition. Table 7.1 shows the deposition conditions of different Al₂O₃ layers. All the sample surfaces were cleaned with TMA and N⁺ plasma treatments.

Figure 7.3 shows the I - V characteristics of the two-terminal devices fabricated on these samples. The samples where Al₂O₃ layers were deposited using O⁺ plasma and/or deposition temperature was 200 °C exhibit almost one order lower current. This collapse in current indicates that O⁺ plasma and high-temperature deposition degrade the transport properties of Cd₃As₂ films. High energy O⁺ plasma damages Cd₃As₂ films. As the Cd₃As₂ structural quality is compromised at high temperatures, the degradation of Cd₃As₂ films at 200 °C depositions is not surprising. Post-ALD 200 °C annealing, however, improves transport characteristics. As explained in **Section 7.1.4**, post-ALD annealing improves not only current densities but also enhances current modulation. Furthermore, this experiment shows that the Cd₃As₂ layer can withstand high-temperature processes if Cd₃As₂ is covered with a protection layer.

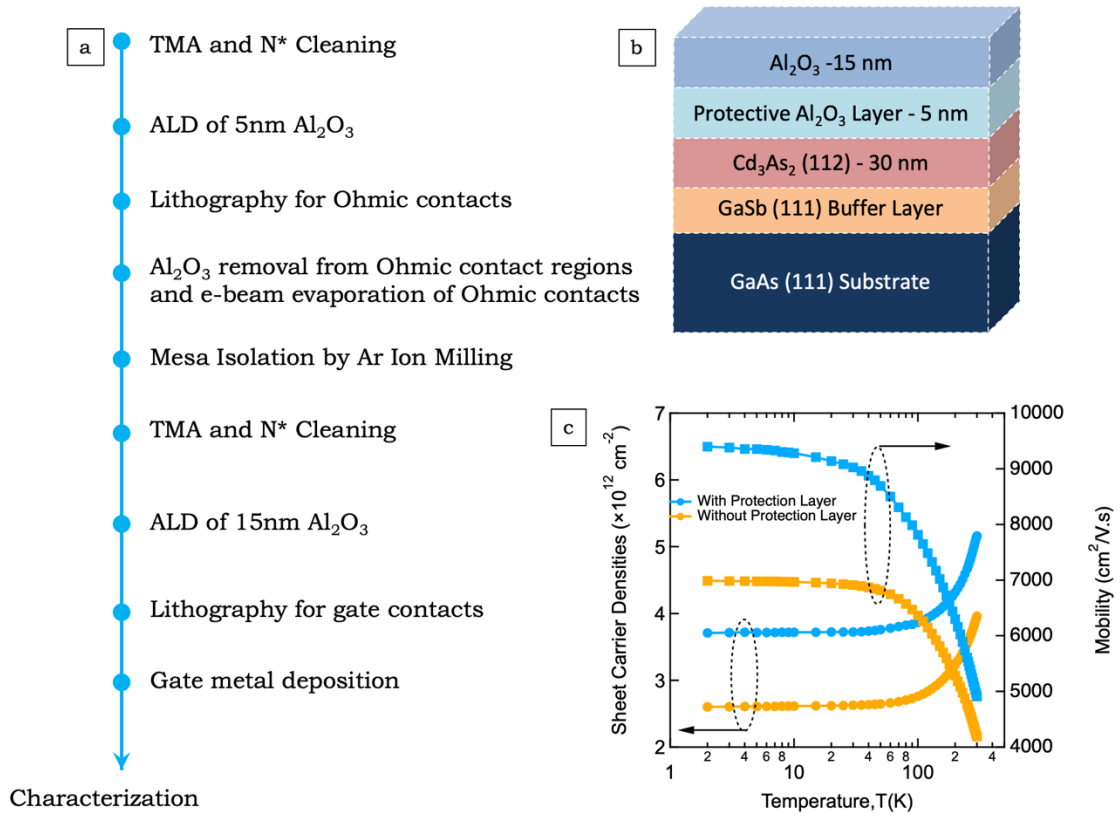


Figure 7.4: Cd₃As₂ fabrication process with Al₂O₃ protection layer. (a) Process flow of modified fabrication process of Cd₃As₂ devices. **(b)** Epitaxial structure with the modified fabrication process. **(c)** Sheet carrier density and electron mobility of Cd₃As₂ thin film with (blue) and without (Orange) protection layer.

7.1.3 The Effect of Protection Layer

A typical fabrication process of a Cd₃As₂ FET starts with the lithography for Ohmic regions. Ohmic metal deposition and mesa isolation etching take place before Al₂O₃ deposition. All of these steps potentially introduce damage and contamination of the channel. For example, photoresists are stuck on Cd₃As₂ surfaces and difficult to remove completely. Contamination and damage needs to be minimized to improve the interface quality between Cd₃As₂ and Al₂O₃.

To ensure a cleaner interface, we modified the fabrication process. The modified process starts with 5 nm of Al_2O_3 deposition, which protects the Cd_3As_2 channel during the fabrication. The detail of the modified fabrication process is shown in **Fig. 7.4(a)**. **Figure 7.4(b)** shows the epitaxial structure used in this experiment. To aid in identifying the effect of the protection layer, a control sample was fabricated using the standard process and no protection layer. **Figure 7.4(c)** presents the sheet carrier densities and carrier mobilities of the samples with and without the protection layer. The protection layer improves the carrier mobilities in the channel indicating a cleaner interface. In addition, the protection layer increases sheet carrier densities, which suggests that fabrication-related damage and contamination lower the Fermi level in the Cd_3As_2 channel.

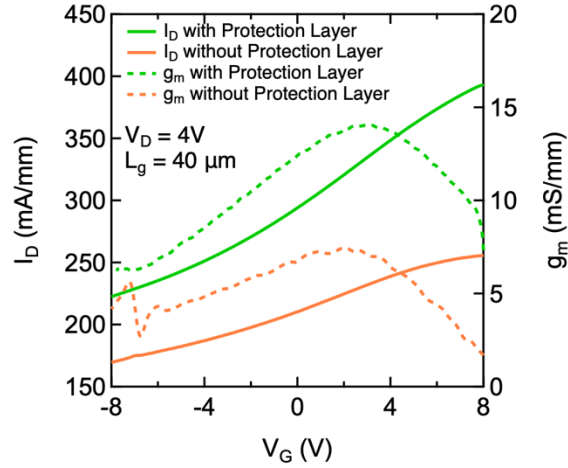


Figure 7.5: Effect of protection layer on current and transconductance of Cd_3As_2 field-effect transistors. Drain current (solid) and transconductance (dashed) characteristics of Cd_3As_2 field-effect transistors with (green) and without (orange) the protection layer.

Figure 7.5 illustrates the drain current – gate voltage (I_D - V_G) and transconductance characteristics of the Cd₃As₂ FETs with and without the protection layer. The protection layer improves current densities, current modulation, and transconductance. As this sample has higher sheet carrier densities and carrier mobilities, higher current density and transconductance are expected in this sample. Moreover, higher sheet carrier densities lower access region and contact resistances and reduce their impact on transistor performance, resulting in a higher current modulation in the FET with the protection layer. Furthermore, a cleaner interface establishes better gate control, which also increases current modulation.

Figure 7.6 presents the drain current – drain voltage (I_D - V_D) characteristics of Cd₃As₂ FETs with different gate lengths. Irrespective of the gate length, the FETs with the protection layer exhibit higher current densities and higher current modulation. **Figure 7.7(a)** summarizes the current modulation of Cd₃As₂ FETs for different gate lengths. Longer channel devices demonstrate higher current modulation, consistent with the discussion of **Section 6.4.3**. Long channel Cd₃As₂ FET with the protection layer shows current modulation of 45%. To examine the limit of the current modulation in Cd₃As₂ FETs, FETs with an extremely long gate length of 300 μm were fabricated. In these extreme channel length devices, the effect of access and contact resistances are negligible. Additionally, long channel devices have a low lateral electric field and thus can provide better gate control. **Figure 7.7(b)** shows the I_D - V_G characteristics of 300 μm gate length FETs. The FET with the protection layer exhibits a current modulation over 55%, comparable to graphene FETs [177-180], whereas the control sample has a current modulation of 35%. This large current modulation further confirms that low current modulation in shorter channel devices is not due to material limitations. **Figure 7.8** shows the transconductance characteristics of Cd₃As₂ FETs for different gate lengths. Surprisingly,

longer channel devices display higher transconductances and have better gate control and thus exhibit higher current modulation. Although the current density is lower in a longer channel device, higher current modulation improves transconductance of long channel FETs. These results indicate that high current modulation and transconductance are achievable in a shorter channel Cd_3As_2 FET by establishing a better gate control.

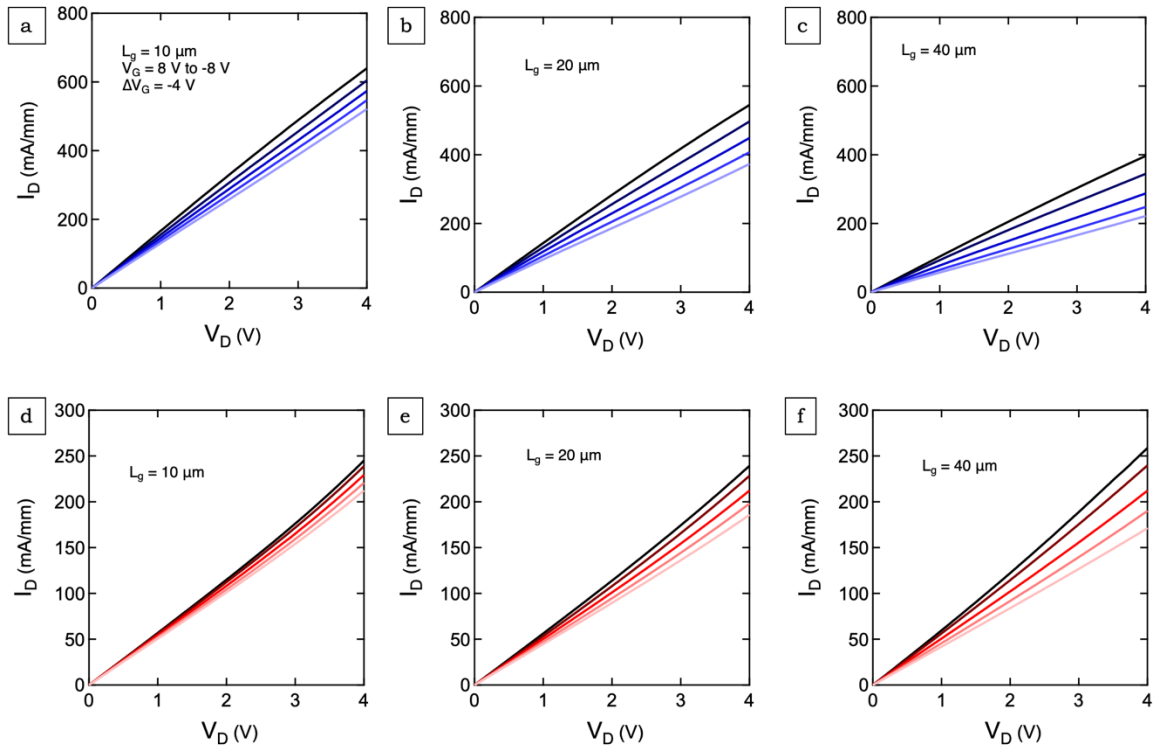


Figure 7.6: Effect of protection layer on I_D - V_D characteristics of Cd_3As_2 field-effect transistor.

I_D - V_D characteristics of Cd_3As_2 FET (a-c) with and (d-f) without protection layer for different gate lengths.

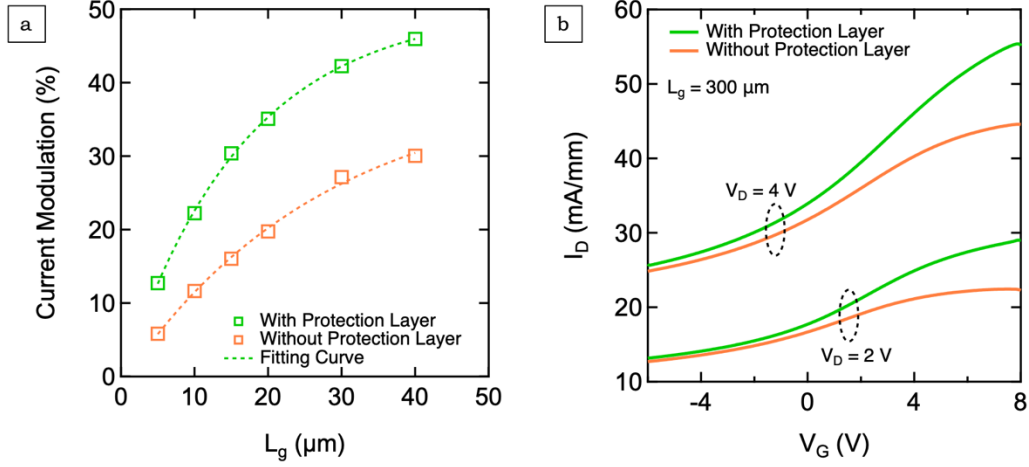


Figure 7.7: Effect of gate length on the carrier control of Cd_3As_2 field-effect transistor. (a) Gate modulation of Cd_3As_2 FETs as a function of the gate length. Longer gate length devices show better gate control and hence improved current modulation. **(b)** I_D - V_G characteristics of Cd_3As_2 FETs with a highly long gate length of $300 \mu\text{m}$.

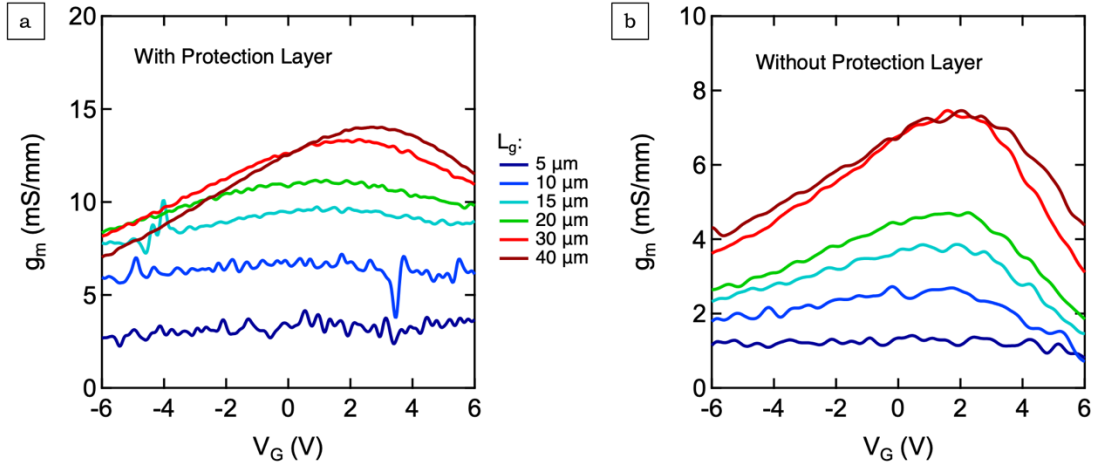


Figure 7.8: Effect of protection layer on the g_m - V_G characteristics of Cd_3As_2 field-effect transistor. (a) g_m - V_G characteristics of Cd_3As_2 FETs **(a)** with and **(b)** without protection layer for different gate lengths. Due to better gate control, longer channel FET with protection layer exhibits higher transconductance.

Although the protection layer improves Cd_3As_2 FET performance, it did not lower the trap densities significantly. **Figure 7.9** presents the C - V characteristics of devices with and without a protection layer. Charge trapping introduces hysteresis in the C - V characteristics [181] and there is no significant difference in terms of hysteresis between these devices. These results suggest large trap densities in Cd_3As_2 FETs, even with surface treatment and a protection layer. As the Al_2O_3 layer was deposited in two steps in the sample with the protection layer and the vacuum was broken between those two steps, gate leakage is slightly higher in this sample. That is why there is a slight degradation in quality factors in the devices with the modified fabrication process.

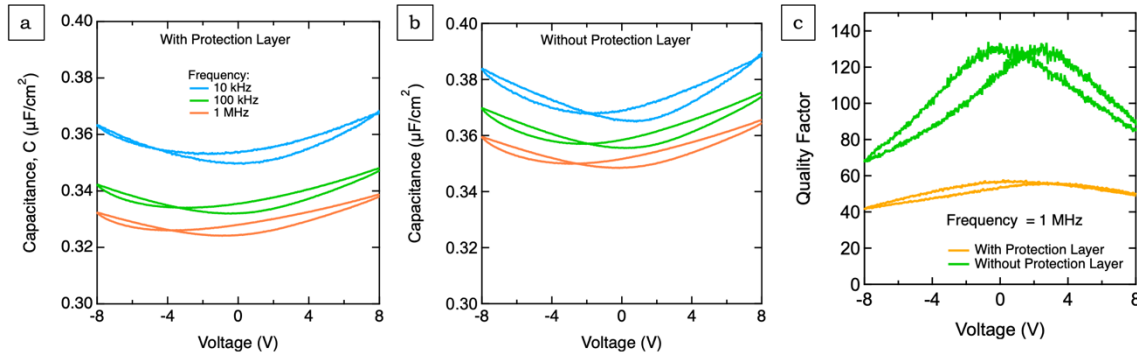


Figure 7.9: Effect of protection layer on the gate capacitances of Cd_3As_2 field-effect transistor.

Capacitance-voltage characteristics of Cd_3As_2 devices **(a)** with and **(b)** without protection layer for different frequencies. **(c)** As the Al_2O_3 layer was deposited at two steps in the sample with the protection layer, the devices with the protection layer exhibited slightly higher gate leakage and lower quality factor.

7.1.4 Effect of Post Al₂O₃ Deposition Annealing

As mentioned in **Section 7.1.2**, post-ALD annealing improves the transport of Cd₃As₂ films. This section discusses two different annealing experiments to understand the effect of annealing on Cd₃As₂ devices. In the first experiment, Cd₃As₂ devices (FETs and capacitors) were fabricated with a protection layer. The sample was annealed in forming gas (FG) at 200 °C after the first Al₂O₃ layer (5 nm protection layer) deposition. Afterward, the rest of the processing steps were carried out to finish the fabrication. This high-temperature annealing improves the transport properties (sheet resistances, carrier mobilities, etc.) of the sample. As a result, the FET with post-ALD annealing exhibits higher current modulation, as shown in **Fig. 7.10(a)**. Nonetheless, the C - V characteristics (**Fig. 7.10(b)**) show no significant improvement in hysteresis.

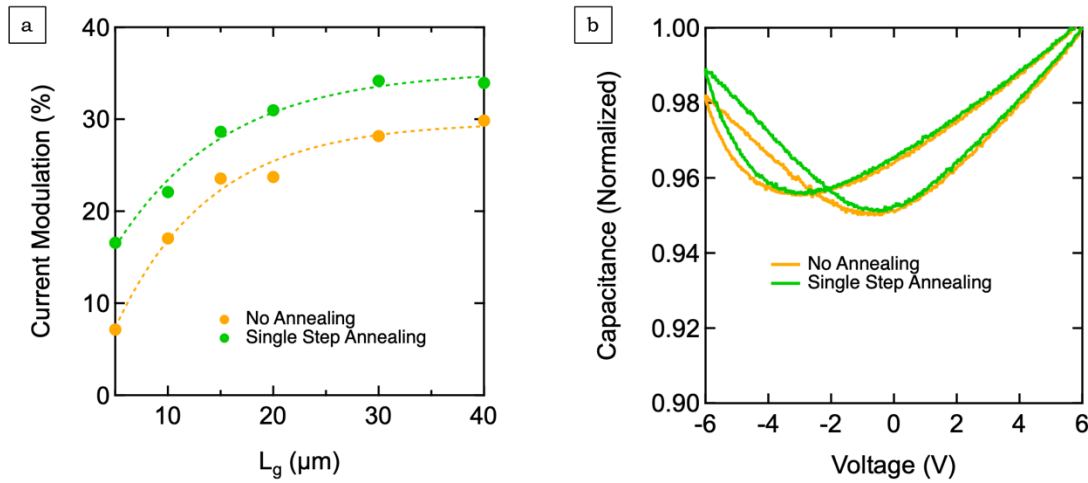


Figure 7.10: Effect of annealing on Cd₃As₂ FETs with protection layer. (a) Current modulation as a function of the gate length. The annealing after the deposition of the protection layer improves current modulation. **(b)** Normalized C - V characteristics of the devices with and without annealing. The annealing shows no improvement in hysteresis.

In this annealing experiment, the top Al_2O_3 layer did not experience any annealing. Therefore, this layer might be the source of traps observed in the devices. To test this hypothesis, a new experiment was designed where the whole Al_2O_3 layer was annealed in FG at 200 °C. **Figure 7.11** illustrates the C - V characteristics of Cd_3As_2 devices with and without annealing. Unfortunately, post-ALD annealing displays no significant improvement in trap densities. The quality factor, however, improves after annealing, indicating that the Al_2O_3 layer is better quality. This annealing study suggests that most of the traps, if not all, resides at the interface.

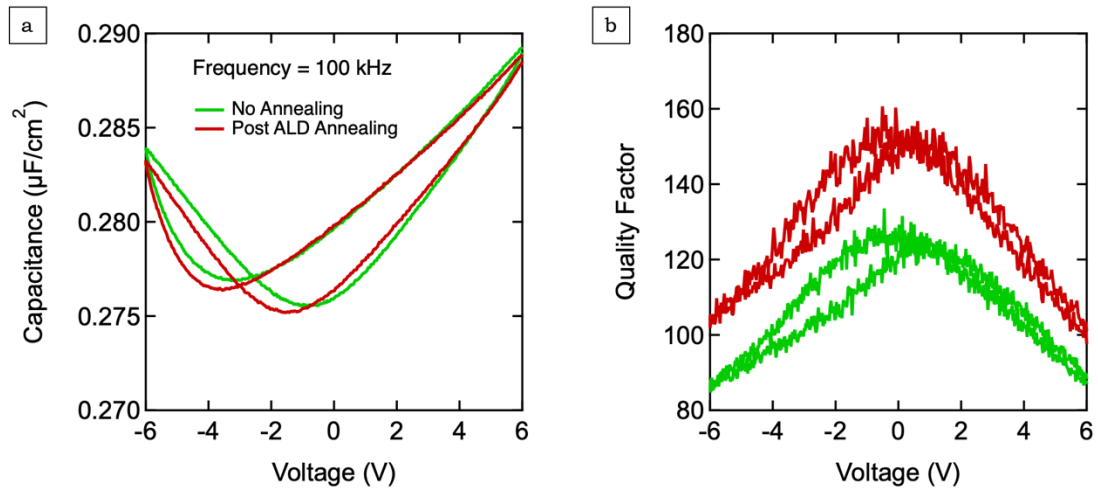


Figure 7.11: Effect of post-ALD annealing on Cd_3As_2 devices. (a) C - V characteristics and (b) Quality factor of Cd_3As_2 devices with and without post-ALD annealing. The Al_2O_3 layer was deposited in a single step, and then the sample was annealed. Even though annealing improves quality factors, it does not reduce trap densities.

7.1.5 Thermally Evaporated Gate Metal

Another vital factor that affects gate oxide quality is the gate metal deposition technique. E-beam evaporation causes more damage to the gate oxide compared to thermal evaporation

[182]. **Figure 7.12** shows the C - V characteristics of a Cd_3As_2 device where the gate contact was deposited by thermally evaporating Ni. Even though C - V characteristics exhibit a large hysteresis, thermal evaporation shows a significant improvement in the quality factor. There is more than a two-fold improvement in quality factor compared to the e-beam evaporated gate contact. This result suggests that, although thermal evaporation does not reduce trap densities, it significantly reduces the damage to the gate oxide introduced by e-beam evaporation.

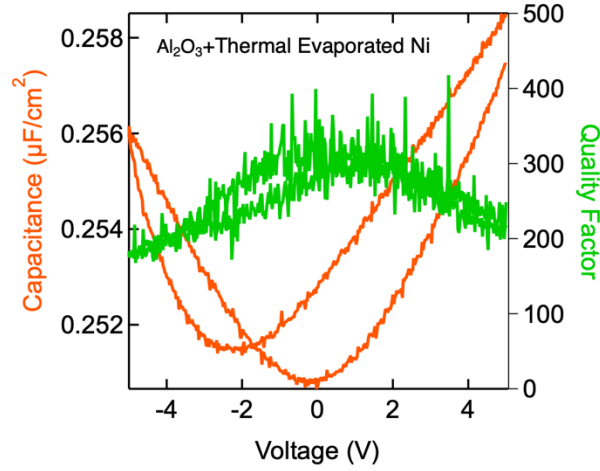


Figure 7.12: Effect of thermally evaporated gate metal. C - V characteristics and quality factor of Cd_3As_2 devices with thermally evaporated gate metal

7.1.6 Hexagonal Boron Nitride (h-BN) as Gate Insulator

To mitigate trap issues in Cd_3As_2 devices, we used 2D h-BN as a gate insulator. The h-BN film was grown by Prof. Jing Kong's group at MIT using chemical vapor deposition [183]. Afterward, h-BN film was transferred on Cd_3As_2 film and Al_2O_3 was deposited on top of the h-BN to lower gate leakage. As h-BN is a 2D material without any dangling bonds, it was speculated that it could reduce interface traps. Moreover, as h-BN was grown at high

temperature and then transferred on Cd_3As_2 sample, the material quality of h-BN should be better than the low-temperature ALD gate dielectric. The schematic diagram of the epitaxial structure is shown in **Fig. 7.13(a)**.

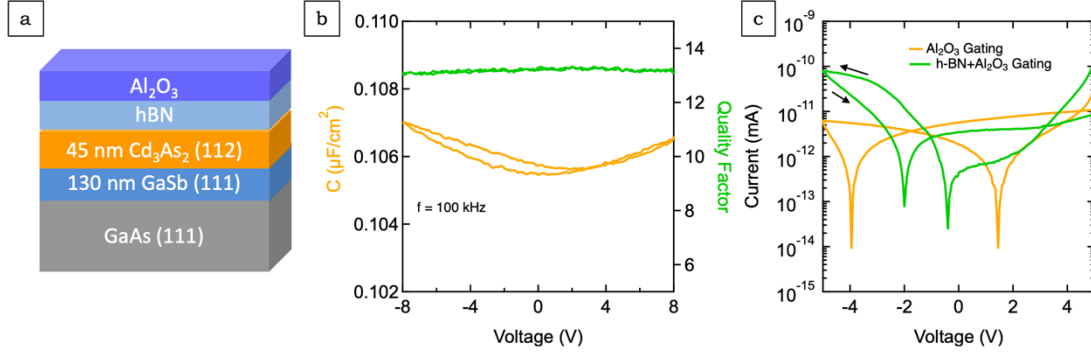


Figure 7.13: Hexagonal-BN gated Cd_3As_2 field-effect transistors. (a) Epitaxial structure of h-BN gated FETs. (b) C - V characteristics of h-BN gated Cd_3As_2 device. (c) Gate leakage of h-BN gated devices. The h-BN gated device shows smaller hysteresis compared to Al_2O_3 gated device.

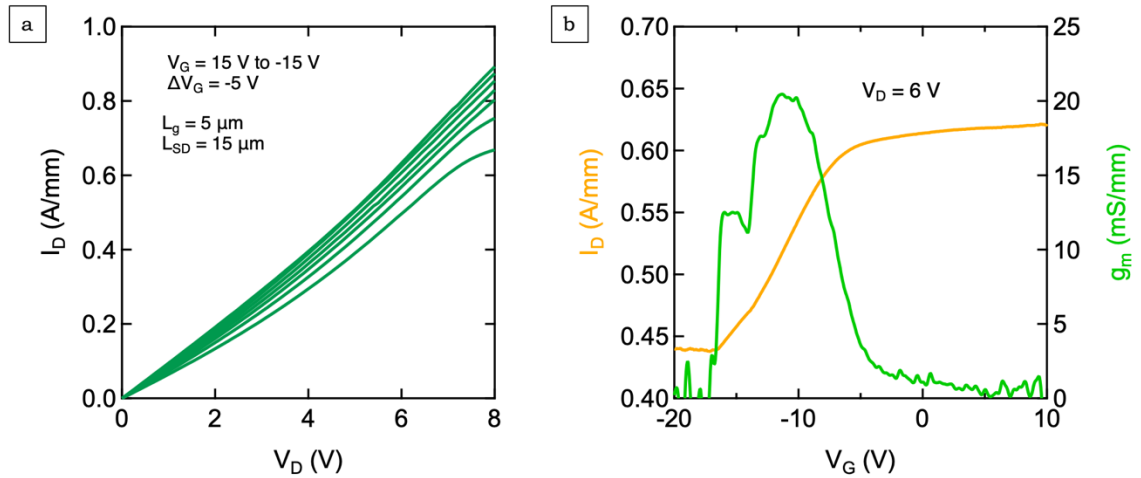


Figure 7.14: Effect of h-BN gating on Cd_3As_2 transistor characteristics. (a) I_D - V_D (b) I_D - V_G and g_m - V_G characteristics of an h-BN gated Cd_3As_2 FET.

Figure 7.13(b) presents the C - V characteristics of the Cd_3As_2 devices with an h-BN gate insulating layer. The data show slightly lower hysteresis compared to Al_2O_3 gated devices. Moreover, due to the lower permittivity of h-BN and thicker gate insulator layer, this device has only about $1/3^{\text{rd}}$ of the capacitance density. Additionally, the gate current shows significant improvement in hysteresis. **Figure 7.13(c)** shows that hysteresis in the gate leakage reduced from 5 V to below 2 V after using h-BN as a gate insulator. **Figure 7.14** demonstrates the I_D - V_D , I_D - V_G , and g_m - V_g characteristics. The I_D - V_D characteristics show the onset of current saturation at negative gate voltage. This onset of current saturation implies that h-BN gating offers better gate control. Additionally, this result confirms that with better gate control and lower trap densities, current saturation is achievable in a Cd_3As_2 FET even without any bandgap in the surface states. h-BN gated FETs exhibit significant improvement in transconductance compared to Al_2O_3 gated devices with similar dimensions (20 mS/mm compared to 5 mS/mm). Therefore, h-BN gated FETs demonstrate about one-order improvement in transconductance after taking the difference in gate capacitances into account. Furthermore, h-BN gating improves current modulation from 12% to 25%. This improvement further confirms that most of the traps of an Al_2O_3 gated Cd_3As_2 FET are at the interface. Although h-BN gating offers a huge improvement in transistor characteristics, there are still significant trap densities in the FETs. There are two possible origins of these traps – top Al_2O_3 layer and native oxide layer. Cd_3As_2 FETs with only h-BN gate insulator, instead of bilayer gate insulator, should eliminate any effect of the low quality Al_2O_3 layer. Moreover, surface treatment of Cd_3As_2 just before h-BN transfer should remove any native oxide.

7.2 Modified Cd₃As₂ Field-Effect Transistor Structures

Terahertz (THz) FETs require high current densities. To drive a high current in a FET, the carrier velocity in the channel should be high. To estimate the carrier velocity in the Cd₃As₂ channel, two-terminal devices with different channel widths, varied from 2 μm to 100 μm , were fabricated. **Figure 7.15(a)** presents the I - V characteristics of those two-terminal devices. The 2 μm wide device exhibits extremely high current density, around 10 A/mm. At such extremely high current densities, heating plays an important role. The non-linearity observed in the 2 μm wide device at current densities above 6 A/mm is due to heating. Because of the smaller free surface/volume ratios in wider channel devices, the effect of heating is worse in those devices. 10 μm and 20 μm wide devices failed below 3 V due to poor thermal management and 50 μm and 100 μm wide devices hit the current compliance of the parameter analyzer below 2 V. A lower limit of the average carrier velocity in Cd₃As₂ can be estimated from I - V characteristics before the onset of any heating effect. A 6 A/mm current density with a sheet carrier density of $4.5 \times 10^{12} \text{ cm}^{-2}$ translates to an average carrier velocity of $7.5 \times 10^5 \text{ m/s}$. We can also estimate the Fermi velocity in Cd₃As₂ thin films using **Eqn. 6.4**. The I - V characteristics indicate that the Fermi velocity in Cd₃As₂ thin film is above $1.2 \times 10^6 \text{ m/s}$. This estimated Fermi velocity is very close to the value measured by angle-resolved photoemission spectroscopy ($2.0 \times 10^6 \text{ m/s}$) [61].

The I - V characteristics also exhibit a surprising result. The current density is much higher in narrower channel devices. For a better illustration, resistances of the devices are shown in **Fig. 7.15(b)** as a function of the inverse of the channel widths. Deviation from linear behavior

confirms that narrow channel devices have lower resistivities. Several factors can lead to this unusual trend in resistivity:

1. One possible factor is the effect of series resistances. There are two sources of series resistances – contact resistances and probe resistances. All the devices have similar large contact pads so contact resistances are the same for all the devices. Probe resistances should also be similar for all the devices. As the wider devices have low channel resistances, series resistances in these devices are comparable to the channel resistances. As a result, a relatively large voltage drops at the contacts and probes in a wider channel device, and the device exhibits lower current density. The effect of contact resistances is more pronounced in wider channel devices and the resistances of the wider channel devices deviate from linear behavior, as shown in **Fig. 7.15(c)** with red dashed lines. In **Fig. 7.15(b)**, 2-probe measurements show a similar trend at a wider channel regime. Because of large series resistances, the channel resistances exhibit a plateau for wider channel devices. The plateau, however, vanishes during 4-probe measurements. This difference between 2- and 4-probe measurements suggest that series resistance is dominated mainly by probe resistances. Thus series resistances cannot explain the deviation of device resistances in a narrow channel regime.

2. Another possible factor is conducting surface states at the edges of the devices. These surface states are an intrinsic feature of a topological insulators [124,148,184]. These surface states act as a parallel resistance and lower the overall resistance of the channels. Their impact is more prominent in narrower channel devices, as shown in **Fig. 7.15(c)** with a green line.

That is why narrow channel devices exhibit higher current densities and their resistances depart from linear behavior.

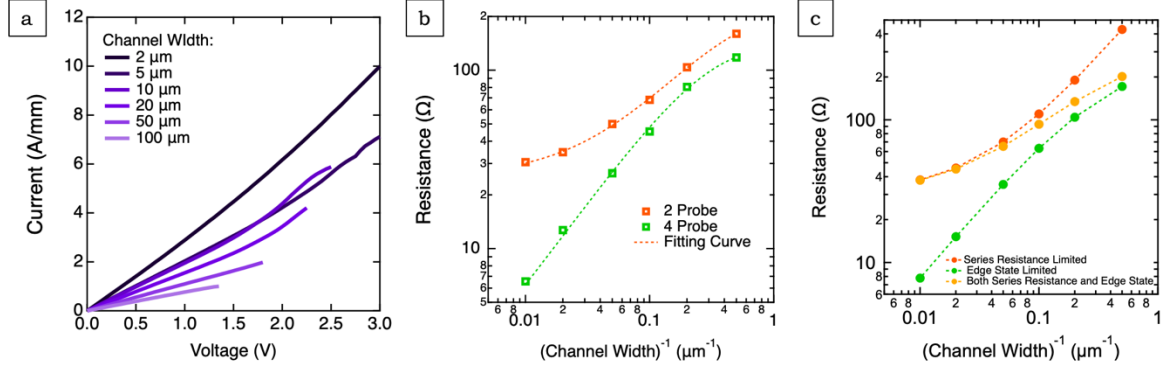


Figure 7.15: Effect of channel width on the transport of Cd_3As_2 channel devices. (a) 2-terminal I - V characteristics of Cd_3As_2 devices with different channel widths. Narrow channel devices exhibit higher current densities and better thermal management. (b) Measured resistance of the devices as a function of channel width. Two-probe measurements show a plateau in resistance at wider channel devices. This indicates that probe resistances limit the current of the wider channel devices. (c) Calculated resistance of the devices as a function of channel width. Edge states lower the resistances of narrow channel devices, whereas series resistance (probe resistance or contact resistance) increases the resistances of wider channel devices. Comparison between (b) and (c) suggest that I - V characteristics of Cd_3As_2 devices are affected by both edge states and probe resistances.

From the experiments discussed in this thesis; we have learned the following information about Cd_3As_2 FETs:

1. Surface cleaning improves interface quality and transport properties of Cd_3As_2 channels.

2. The protection layer improves current densities, current modulation, and transconductances.
3. Contact and access region resistances should be low to improve current modulation and transconductances.
4. Narrow channel devices exhibit higher current densities and better thermal management.
5. Most of the traps resides at the $\text{Cd}_3\text{As}_2\text{-Al}_2\text{O}_3$ interface.

Armed with this knowledge, we have modified the fabrication process and designed a new Cd_3As_2 FET structure to probe the intrinsic characteristics of Cd_3As_2 FETs. A top view of this new FET structure is shown in **Fig. 7.16(a)**. This new device structure has much wider contacts and access regions (100 μm) than the channels. This should make the effect of contact and access region resistances negligible. Besides, a very narrow channel (2 μm) ensures higher current densities and better gate control. Because of these modifications, a relatively shorter gate length (4 μm) device exhibits improved transistor characteristics.

Figure 7.16(b) presents the drain current vs. gate voltage ($I_D\text{-}V_G$) characteristics and transconductance vs. gate voltage ($g_m\text{-}V_g$) characteristics of the modified Cd_3As_2 FET. The $I_D\text{-}V_G$ characteristics exhibit extremely high current densities of 4 A/mm for a drain voltage of 1 V. This current density is much higher than state-of-the-art III-V MOSFETs [172,185]. The average velocity derived from this current density is 4×10^5 m/s. This velocity is slightly lower than the velocity derived from two-terminal $I\text{-}V$ characteristics. The drain current vs. drain voltage ($I_D\text{-}V_D$) characteristics show that the device is still in a linear regime. So, higher current

density should be attainable by applying higher drain voltage. I_D - V_D characteristics exhibit current modulation over 25%. This is a considerable improvement in current modulation in a shorter channel device. Also, the FET exhibits a maximum transconductance of 120 mS/mm. The average velocity derived from this transconductance (Velocity = g_m/C_{ox}) is 4×10^4 m/s, which is one order smaller than the velocity derived from I_D - V_G characteristics. This difference in average velocity is due to the trap densities. These results suggest that by reducing the trap densities, the transconductance of a Cd₃As₂ FET can be improved by a factor of 10.

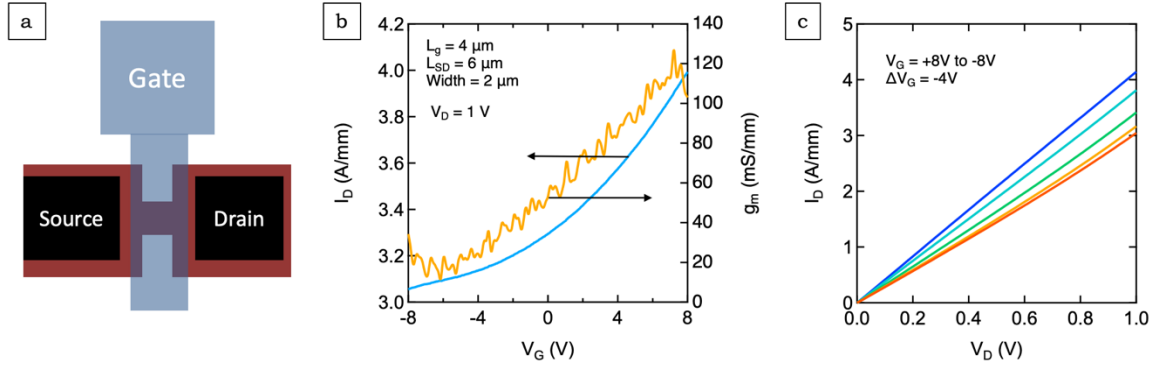


Figure 7.16: Modified Cd₃As₂ field-effect transistor. (a) Schematic diagram of a modified Cd₃As₂ FET with wide contact and access regions and narrow channel. (b) I_D - V_G , g_m - V_G , and (c) I_D - V_D characteristics of the modified FET.

7.3 Conclusion

In summary, the protection layer along with N^{*} plasma-based surface treatment improves interface quality and carrier transport in a Cd₃As₂ channel. These modifications in the fabrication process lead to an improved room temperature current modulation and high transconductance in Cd₃As₂ channel FETs. Furthermore, a longer channel FET exhibits a

current modulation over 55%, which is reasonable for a gapless semimetallic channel. This result also demonstrates that the low current modulation in shorter channel FETs is not a fundamental material issue of Cd_3As_2 . Instead, it stems from relatively high access resistance and large trap density. Furthermore, h-BN gating offers a better gate control and improved transistor characteristics. Finally, a modified FET structure demonstrates higher current density and transconductance in a shorter channel device. This study also suggests that a massive improvement in transconductance is possible by reducing the trap densities.

Chapter 8

Summary and Outlook

8.1 Summary

8.1.1 Perovskite Oxide Based Electronics

We demonstrated the successful integration of epitaxial ferroelectric thin films on semiconductor channels with high density-of-states. Ferroelectricity of BaTiO_3 can be stabilized in a thin film above a critical thickness (~ 1.2 nm). The ferroelectric polarization charge depletes the carriers from the channel. Electronic devices, such as capacitors, and field-effect transistors (FETs), based on $\text{BaTiO}_3/\text{SrTiO}_3$ heterostructures exhibit anti-clockwise hysteresis in their characteristics consistent with expectations from the ferroelectric nature of the BaTiO_3 thin films. Furthermore, biaxial compressive stress enhances ferroelectricity and increases the Curie temperature of BaTiO_3 thin films. Nevertheless, $\text{BaTiO}_3/\text{SrTiO}_3$ FETs are negatively affected by the low electron mobility in the SrTiO_3 channel and lack of conduction band offset between BaTiO_3 and SrTiO_3 . Consequently, we developed the epitaxial growth of high electron mobility perovskite oxide, BaSnO_3 , in molecular beam epitaxy (MBE). This thesis details the growth of BaSnO_3 thin films on DyScO_3 substrates. All BaSnO_3 films were found to be non-stoichiometric and the growth was Ba flux-limited. The growth of BaSnO_3 on DyScO_3 substrate starts with island formation, and those islands merge afterward, forming domains. There are slight misalignments between these domains due to the pseudo-cubic nature of the DyScO_3 (001) substrates. This work also reveals significant non-uniformity in

structural and transport properties of the BaSnO₃ thin films. The highest electron mobilities in BaSnO₃ thin films observed in this study are 172 cm²/Vs and 215 cm²/Vs using Van der Pauw and Hall bar methods, respectively. BaTiO₃/BaSnO₃ devices were found to be not affected by the ferroelectricity in their characteristics because of large biaxial tensile stress on BaTiO₃ thin films, which aligns the polarization in-plane. Yet, the high permittivity of BaTiO₃ can be exploited to enhance the breakdown voltage of BaTiO₃/BaSnO₃ FETs.

8.1.2 Cd₃As₂ for Electronic Applications

The electronic band structure and the transport properties of Cd₃As₂ thin films evolve with the film thicknesses. A thick Cd₃As₂ film is a 3D Dirac semimetal, whereas quantum confinement and/or strain opens up a small bandgap in the bulk region of a thin film. In these films, topologically non-trivial 2D states exist on the surfaces. Furthermore, the Berry phase introduces a negative transverse magnetoresistance in the Cd₃As₂ thin films. The effect of the Berry phase can be modified by tuning the quantum confinement or shifting the Fermi level.

Due to the topological nature of the energy states, Cd₃As₂ thin films exhibit interesting transport characteristics, such as extremely high Fermi velocity, high electron mobility, sheet carrier density-independent higher average forward velocity, and large density-of-states. All of these unique electronic properties make Cd₃As₂ a suitable candidate for THz transistors. We have presented an analytical model that evaluates the prospect of Cd₃As₂ FETs for THz application. The model predicts excellent RF performances along with linearity in current cutoff frequency and transconductance.

This thesis also demonstrated the first FETs with a Cd_3As_2 channels. Bulk carriers, trap densities, access region resistances, channel width, and lateral electric field affect room temperature performances of Cd_3As_2 FETs. A protection layer along with N^* plasma-based surface treatment was shown to improve the interface quality and carrier transport of Cd_3As_2 FETs. Moreover, these modifications in the fabrication process improve current density, current modulation, and transconductances of the FETs. Because traps are the major performance-limiting factors of a Cd_3As_2 FET, replacing gate insulator with 2D h-BN may offer better gate control and improved transistor characteristics. Finally, this thesis developed a modified FET structure, which demonstrated higher current density (4 A/mm) and transconductance (120 mS/mm) in a shorter channel device. Experimental data also implied that a massive improvement in transconductance ($\sim 10\times$) is possible by reducing the trap densities.

8.2 Future Work

8.2.1 Modulation Doping in BaSnO_3

To realize all-oxide electronic devices, high electron mobilities, such as those afforded by BaSnO_3 thin films, are required. One of the ways of achieving high electron mobility in any heterostructure is modulation doping, which has been a key factor in achieving high mobility in III-V systems. Modulation doping isolates the doping atoms from the channel, which leads to low ionized impurity scattering and high electron mobility in the channel. Furthermore, the efficiency of the modulation doping can be improved by a delta doping near the channel. There are two possible heterostructures that can be explored for modulation doping – $\text{SrTiO}_3/\text{BaSnO}_3$ and $\text{SrSnO}_3/\text{BaSnO}_3$. Both SrSnO_3 and SrTiO_3 have the conduction band offset of about 1 eV

with BaSnO₃. 1 eV conduction band offset is sufficient to achieve reasonable sheet carrier densities in the BaSnO₃ channel. SrSnO₃ has a smaller lattice mismatch with BaSnO₃, which can offer a smoother interface and better structural quality of the barrier layer. On the other hand, the high permittivity of SrTiO₃ could be beneficial to modulate high sheet carrier densities in the BaSnO₃ channel.

8.2.2 Reduce Trap Densities for Cd₃As₂ Field-Effect Transistor

One of the major performance-limiting factors of a Cd₃As₂ channel FET are the trap densities at the interface with the gate dielectric. One way of reducing the traps could be high temperature post-ALD annealing. It is possible to anneal Cd₃As₂ films at a high temperature (> 500 °C) without sacrificing the structural quality of the films [186]. Cd₃As₂ film needs to be covered with a thick cap layer (~ 1 µm) to apply this high-temperature annealing. Several modifications and optimizations in the fabrication process are needed to accommodate this high-temperature post-ALD annealing. High temperature annealing could be helpful to passivate the dangling bonds at the interface, which could reduce interface trap densities. Moreover, this annealing should improve the structural quality of the Al₂O₃ layer, which should lower bulk traps of the Al₂O₃ layer. Another possible solution could be using h-BN as a gate insulator. This thesis discussed preliminary results of Cd₃As₂ FET with a hybrid h-BN gate insulator. Although h-BN gating improved transistor performances and reduced interface trap densities, there are still significant trap densities in the h-BN gated Cd₃As₂ FETs. This study confirmed that although interface traps are the most dominating traps in the Cd₃As₂ FETs, there are few other factors that contribute to high trap densities in these FETs. Low structural quality of Al₂O₃ can introduce traps at the bulk region of the gate oxide. Furthermore,

native oxide of Cd_3As_2 may further increase interface trap densities. Cd_3As_2 FETs with h-BN as gate insulator, where h-BN layers are transferred immediately after surface treatment, can reduce both interface and bulk trap densities.

8.2.3 Hot Electron Transistor with Cd_3As_2 Base

One of the interesting applications of Cd_3As_2 thin films to achieve THz performance could be hot electron transistor (HET). HET is a BJT-like three-terminal device. However, unlike BJT, the transport mechanism is unipolar in a HET. Though HET has the potential to be operated in THz frequency, the base region needs to be both thin and highly conductive, which traditional semiconductors fail to offer, to achieve THz performances. Cd_3As_2 thin films can meet all these requirements. As Cd_3As_2 is a semimetal, a very thin layer should be sufficient to achieve reasonable conductivity in the base region. Furthermore, high Fermi velocity should reduce the base transit time. Additionally, because Cd_3As_2 can be grown epitaxially on different III-V semiconductors, there is flexibility in transistor design.

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Appendix

A1. Surface Treatment of DyScO₃ Substrates

1. Mix HNO₃ and HCl (Volume ratio 1:3). Make the Solution 30 minutes before using.
2. Soak the substrates into hot water for 15 mins.
3. Make the substrates dry using N₂ blow.
4. Use the mixture to etch the surfaces of the DyScO₃ substrates for 5 minutes
5. Mix 0.5 M NH₃ and 0.1 M HCl.
6. Use NH₃/NH₄Cl mixture to soak the substrates for 5 mins.
7. Soak the substrates into water and make them dry using N₂ blow.
8. Anneal at 1000 °C for 2 hours. Cover the substrates with sapphire wafer during the annealing.

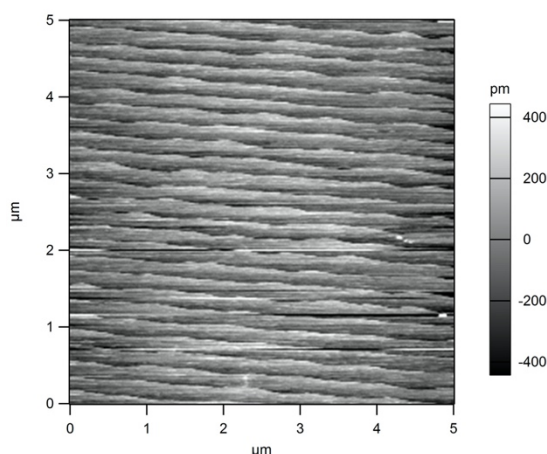


Figure: Surface morphology of DyScO₃ (001) substrate after surface treatment

A2. Surface Treatment of SrTiO₃ Substrates

1. Mix HNO₃ and HCl (Volume ratio 1:3). Make the Solution 30 minutes before using.
2. Soak the substrates into hot water for 15 mins.
3. Make the substrates dry using N₂ blow.
4. Use the mixture to etch the surfaces of the DyScO₃ substrates for 5 minutes
5. Mix 0.5 M NH₃ and 0.1 M HCl.
6. Soak the substrates into water and make them dry using N₂ blow.
7. Anneal at 1000 °C for 2 hours. Cover the substrates with sapphire wafer during the annealing.

B1. MATLAB Code for Extracting Mobility of VdP Devices

MATLAB Code for Quantum Design Dynacool Physical Property Measurement System

```
clc
clear all
close all

factor = 1; % To adjust connection error
HDP = 5; % Hall Data point at each Temperature

%% Import Data
cd('/Adress of the folder')
Q = csvread(['Resistivity Data.dat'],31,1);
P = csvread(['Hall Data.dat'],31,1);

%% Calculate Sheet Carrier Density
[m,p] = size(P);
l = m/HDP; % No. of Temperature points

for i = 1:l
    T(i) = P(1+(i-1)*HDP,3);
    B = P(1+(i-1)*HDP:HDP+(i-1)*HDP,4)/1e4;
    Rxy_1 = P(1+(i-1)*HDP:HDP+(i-1)*HDP,6+(1-1)*2)*factor;
    [aa,bb,R_calc,RH] = HallCoefficient(B,Rxy_1);
    n_1(i) = aa;
    r2_1(i) = bb;
    Rxy_2 = P(1+(i-1)*HDP:HDP+(i-1)*HDP,6+(3-1)*2)*factor;
    [aa,bb,R_calc,RH] = HallCoefficient(B,Rxy_2);
    n_2(i) = aa;
    r2_2(i) = bb;
    n(i) = mean([n_1(i) n_2(i)]);
end

%% Calculate Sheet Resistance and Mobility
Rx = flip(Q(:,6));
Ry = flip(Q(:,10));

for i = 1:l
    [Rs_1(i),Rs_2(i),Rs(i)] = SheetResistance(Rx(i),Ry(i));
    mu_1(i) = 1/n_1(i)/1.6e-19/Rs_1(i);
    mu_2(i) = 1/n_2(i)/1.6e-19/Rs_2(i);
    mu(i) = 1/n(i)/1.6e-19/Rs(i);
end

%% Plotting
figure(1)
set(gcf, 'Position', [0, 1600, 1600, 1600])
subplot(2,2,1)
```

```

semilogx(T,n,'-
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','r')
hold on
semilogx(T,n_1,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','g')
hold on
semilogx(T,n_2,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','b')
xlabel('T(K)')
ylabel('Sheet Carrier Density (cm-2)')
if (1 < 2)
    xlim([.9*T 1.1*T])
else
    xlim([1 300])
end
set(gca,'FontSize',20,'Box','on','LineWidth',2)
legend('Avg','Ch1','Ch3')
grid on

subplot(2,2,2)
semilogx(T,r2_1,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','g')
hold on
semilogx(T,r2_2,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','r')
xlabel('T(K)')
ylabel('R2')
if (1 < 2)
    xlim([.9*T 1.1*T])
else
    xlim([1 300])
end
set(gca,'FontSize',20,'Box','on','LineWidth',2)
grid on

subplot(2,2,3)
semilogx(T,Rs,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','r')
hold on
semilogx(T,Rs_1,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','g')
hold on
semilogx(T,Rs_2,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','b')
xlabel('T(K)')
ylabel('R_s_h_e_e_t (Ohm/sq.)')
if (1 < 2)
    xlim([.9*T 1.1*T])
else
    xlim([1 300])
end
set(gca,'FontSize',20,'Box','on','LineWidth',2)
legend('Avg','Ch1','Ch3')

```

```

grid on

subplot(2,2,4)
semilogx(T,mu,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','r')
hold on
semilogx(T,mu_1,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','g')
hold on
semilogx(T,mu_2,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','b')
xlabel('T(K)')
ylabel('Mobility (cm^2/V-s)')
if (l < 2)
    xlim([.9*T 1.1*T])
else
    xlim([1 300])
end
set(gca,'FontSize',20,'Box','on','LineWidth',2)
legend('Avg','Ch1','Ch3')
grid on

function [n, r2, R1_calc, RH_1] = HallCoefficient(B,R1)
fit_1 = polyfit(B,R1,1);
RH_1 = -1*(fit_1(1));
R1_calc = fit_1(1)*B+fit_1(2);
R2_1 = 1 - sum((R1 - R1_calc).^2)/sum((R1 - mean(R1)).^2);
n = 1/RH_1/1.6e-19/1e4;
r2 = R2_1;

function [Rs_1,Rs_2,Rs] = SheetResistance(Rx,Ry)
Rs0 = pi/log(2)*1/2*(Rx+Ry); %Initial guess for solver
Rs_1 = pi/log(2)*Rx; %Sheet resistance of Channel 1
Rs_2 = pi/log(2)*Ry; %Sheet resistance of Channel 2

F = @(Rs) 1-(exp(-Rx*pi/Rs)+exp(-Ry*pi/Rs));
Rs = fzero(@(Rs) F(Rs),Rs0);

```

B2. MATLAB/Python Code for Extracting Mobility of Hallbar Devices

MATLAB Code for Quantum Design Dynacool Physical Property Measurement System

```
clc
clear all
close all

%% Import Data
AR = 2; % Aspect ratio of Hall Structure, L/W
HDP = 5; % Hall Data point at each Temperature
Res_Ch = 1; % Rxx measured at this channel
Hall_Ch = 3; % Rxy measured at this channel
pol1 = 1; % 1 = right connection, -1 = reverse connection Hall
pol2 = 1; % Rxx polarity

name = 'Data File Name;
cd('/Address of the Folder)
P = csvread([name '.dat'],31,1);
[m,p] = size(P);
l = m/HDP; % No. of Temperature points

for i = 1:l
    T(i) = P(1+(i-1)*HDP,3);
    B = P(1+(i-1)*HDP:HDP+(i-1)*HDP,4)/1e4;
    Rxy = P(1+(i-1)*HDP:HDP+(i-1)*HDP,6+(Hall_Ch-1)*2)*pol1; %
    Careful about - sign
    [aa,bb,R_calc,RH] = HallCoefficient(B,Rxy);
    n(i) = aa;
    r2(i) = bb;
    Rxx(i) = P(round(HDP/2)+(i-1)*HDP,6+(Res_Ch-1)*2);
    Rsh(i) = Rxx(i)/AR*pol2;
    mu(i) = 1/n(i)/1.6e-19/Rsh(i);
end

figure(1)
set(gcf, 'Position', [0, 1600, 1600, 1600])
subplot(2,2,1)
semilogx(T,n,'--
rs','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','b')
xlabel('T(K)')
ylabel('Sheet Carrier Density (cm^-2)')
xlim([1 300])
set(gca, 'FontSize',20, 'Box', 'on', 'LineWidth',2)
grid on
subplot(2,2,2)
semilogx(T,r2,'--
ks','MarkerSize',15,'linewidth',4,'MarkerEdgeColor','g')
xlabel('T(K)')
ylabel('R^2')
```

```

xlim([1 300])
set(gca, 'FontSize', 20, 'Box', 'on', 'LineWidth', 2)
grid on
subplot(2,2,3)
semilogx(T,Rsh, '--
gs', 'MarkerSize', 15, 'linewidth', 4, 'MarkerEdgeColor', 'r')
xlabel('T(K)')
ylabel('R_s_h_e_e_t (Ohm/sq.)')
xlim([1 300])
set(gca, 'FontSize', 20, 'Box', 'on', 'LineWidth', 2)
grid on
subplot(2,2,4)
semilogx(T,mu, '--
bs', 'MarkerSize', 15, 'linewidth', 4, 'MarkerEdgeColor', 'k')
xlabel('T(K)')
ylabel('Mobility (cm^2/V-s)')
xlim([1 300])
set(gca, 'FontSize', 20, 'Box', 'on', 'LineWidth', 2)
grid on

function [n, r2, R1_calc, RH_1] = HallCoefficient(B,R1)
fit_1 = polyfit(B,R1,1);
RH_1 = -1*(fit_1(1));
R1_calc = fit_1(1)*B+fit_1(2);
R2_1 = 1 - sum((R1 - R1_calc).^2)/sum((R1 - mean(R1)).^2);
n = 1/RH_1/1.6e-19/1e4;
r2 = R2_1;

```

Python Code for Quantum Design Dynacool Physical Property Measurement System

```

import numpy as np
import matplotlib.pyplot as plt
from sklearn.linear_model import LinearRegression

q = 1.6e-19;

# Device and measurement parameters
AR = 2          # Aspect Ratio
HDP = 5         # Hall data points
Res_ch = 1
Hall_ch = 3
Pol_Res = 1
Pol_Hall = 1

# Initialize extracted arrays
T = []
B = []
R1 = []
R3 = []
Slope = []
R_sq = []

```

```

# Read data from input file
with open("/File and Address.dat") as f:
    d = f.readlines()

data = d[31:]

for line in data:
    A = line.split(',')
    T.append(float(A[3]))
    B.append(float(A[4]))
    R1.append(float(A[6+(Res_ch-1)*2]))
    R3.append(float(A[6+(Hall_ch-1)*2]))

Temp = np.array(T[1:HDP])
Rxx = np.array(R1[int((HDP+1)/2):HDP])/AR*Pol_Res
B = np.array(B)/1e4
Rxy = np.array(R3)*Pol_Hall

# Calculating mobility and Sheet Resistance
for i in range(0,len(Temp)):
    model = LinearRegression(fit_intercept=True)
    B1 = np.copy(B[i*HDP:(i+1)*HDP]).reshape(-1,1)
    R1 = Rxy[i*HDP:(i+1)*HDP]
    reg = model.fit(B1,R1)
    R_sq.append(model.score(B1,R1))
    Slope.append(reg.coef_)

R_sq = np.array(R_sq)
Slope = np.array(Slope)
n = -1/Slope/q/1e4
mu = 1/q/np.multiply(n,Rxx.reshape(-1,1))

# Plotting
#fig0 = plt.figure(0,dpi=300)
plt.figure(dpi=1000)
plt.subplot(221)
plt.rcParams.update({'font.size': 12})
plt.plot(Temp,n,marker='.', c = 'blue', alpha=1,
markersize=12,linewidth=2)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.gca().set_xscale('log')
plt.xlim((1,500))
plt.ylim((3e12,6e12))
plt.xlabel('Temperature (K)',fontsize=12)
plt.ylabel('$n_s$ $(cm^{-$$^2})$',fontsize=12)
plt.grid(True)

#fig1 = plt.figure(1,dpi=300)

```

```

plt.subplot(222)
plt.plot(Temp,Rxx,marker='.', c = 'orange', alpha=1,
markersize=12,linewidth=2)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.gca().set_xscale('log')
plt.xlim((1,500))
plt.ylim((170,250))
plt.xlabel('Temperature (K)',fontsize=12)
plt.ylabel('$R_s$$_h$ $$(\Omega/sq.)$',fontsize=12)
plt.grid(True)

#fig2 = plt.figure(2,dpi=300)
plt.subplot(223)
plt.plot(Temp,mu,marker='.', c = 'green', alpha=1,
markersize=12,linewidth=2)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.gca().set_xscale('log')
plt.xlim((1,500))
plt.ylim((4000,10000))
plt.xlabel('Temperature (K)',fontsize=12)
plt.ylabel('$\mu_e$ $(cm^2/V-s)$',fontsize=12)
plt.grid(True)

#fig3 = plt.figure(3,dpi=300)
plt.subplot(224)
plt.plot(Temp,R_sq,marker='.', c = 'red', alpha=1,
markersize=12,linewidth=2)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.gca().set_xscale('log')
plt.xlim((1,500))
#plt.ylim((3e12,6e12))
plt.xlabel('Temperature (K)',fontsize=12)
plt.ylabel('$R^2$',fontsize=12)
plt.grid(True)

plt.tight_layout()

```


B3. MATLAB Python Code to Analyze Magnetotransport

MATLAB Code for Quantum Design Dynacool Physical Property Measurement System

```
clc
clear all
close all

AR = 2; % Aspect ratio of Hall Structure, L/W

%% Import Data
name = 'Data File Name';
cd('/Adress of the Folder')
A = csvread([name '.dat'],31,1);

Res_Ch = 3; % Rxx measured at this channel
Hall_Ch = 1; % Rxy measured at this channel
n = 61;
m = 0;

B = A(:,4)/1e4;
Rxx = A(:,6+(Res_Ch-1)*2)/AR;
Rxy = A(:,6+(Hall_Ch-1)*2);

l = round(length(B)/2);
B_n = B(l-n:l+n);
R_n = Rxy(l-n:l+n);

[n, r2, R_calc, RH_1] = HallCoefficient(B_n,R_n);
R = interp1(B_n,R_calc,B,'linear','extrap');
mu = 1/1.6e-19/Rxx(l+m)/n;

%% Plotting
figure(1)
set(gcf, 'Position', [0, 1800, 1800, 1600])

subplot(2,2,1)
plot(B,Rxx,'linewidth',4,'Color','r')
set(gca,'FontSize',20,'Box','on','LineWidth',2)
xlabel('B (T)','fontsize',20)
ylabel('R_x_x (\Omega/sq.)','fontsize',20)

subplot(2,2,2)
plot(B,Rxy,'LineWidth',4,'Color','b')
hold on
plot(B,R,'--','LineWidth',2,'Color','r')
set(gca,'FontSize',20,'Box','on','LineWidth',2)
xlabel('B (T)','fontsize',20)
ylabel('R_x_y (\Omega)','fontsize',20)
text(2,0,sprintf('n = %.2fx10^1^2 \n r^2 = %.4f \n\mu = %.2f \nR_s = %.2f',n/1e12,r2,mu,Rxx(l+m)), 'fontsize',18, 'color','b')
```

```

%% Symmetry Anti-Symmetry

Rxx_rot = flip(Rxx);
Rxx_sym = (Rxx+Rxx_rot)/2;
Rxx_anti = (Rxx-Rxx_rot)/2;

Rxy_rot = flip(Rxy);
Rxy_sym = (Rxy+Rxy_rot)/2;
Rxy_anti = (Rxy-Rxy_rot)/2;

subplot(2,2,3)
plot(B,Rxx_sym,'linewidth',4,'Color','b')
set(gca,'FontSize',20,'Box','on','LineWidth',2)
xlabel('B (T)','fontsize',20)
ylabel('R_x_x (\Omega/sq.)','fontsize',20)

subplot(2,2,4)
plot(B,Rxy_anti,'linewidth',4,'Color','r')
set(gca,'FontSize',20,'Box','on','LineWidth',2)
xlabel('B (T)','fontsize',20)
ylabel('R_x_y (\Omega)','fontsize',20)

function [n, r2, R1_calc, RH_1] = HallCoefficient(B,R1)
fit_1 = polyfit(B,R1,1);
RH_1 = -1*(fit_1(1));
R1_calc = fit_1(1)*B+fit_1(2);
R2_1 = 1 - sum((R1 - R1_calc).^2)/sum((R1 - mean(R1)).^2);
n = 1/RH_1/1.6e-19/1e4;
r2 = R2_1;

```

Python Code for Quantum Design Dynacool Physical Property Measurement System

```

import numpy as np
import matplotlib.pyplot as plt
from sklearn.linear_model import LinearRegression

q = 1.6e-19;

# Device and measurement parameters
AR = 1      # Aspect Ratio
HDP = 5     # Hall data points
Res_ch = 1
Hall_ch = 3
Pol_Res = -1
Pol_Hall = -1
TDP = 7     # Temperature data point

# Initialize extracted arrays

```

```

T = []
B = []
R1 = []
R3 = []
Temp = []

with open("/Address and File.dat") as f:
    d = f.readlines()

data = d[31:]
for line in data:
    A = line.split(',')
    T.append(float(A[3]))
    B.append(float(A[4]))
    R1.append(float(A[6+(Res_ch-1)*2]))
    R3.append(float(A[6+(Hall_ch-1)*2]))

l = int(len(T)/TDP)
B_field = np.array(B[0:l])/1e4
Rxx = np.zeros((TDP,l))
Rxy = np.zeros((TDP,l))

for i in range(TDP):
    Temp.append(round(T[i*l]))
    Rxx[i,:] = R1[i*l:i*l+l]
    Rxy[i,:] = R3[i*l:i*l+l]

fig0 = plt.figure(0,dpi=300)
plt.rcParams.update({'font.size': 20})
for i in range(TDP):
    plt.plot(B_field,Rxx[i,:]/1e3, c = [.5,i/TDP,.7],
alpha=1,linewidth=3)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.xlim((-10,10))
plt.ylim((0,20))
plt.xlabel('$\mu_0 H$ (T)',fontsize=20)
plt.ylabel('$R_x$ $R_y$ $(k\Omega/sq.)$',fontsize=20)
plt.grid(True)

fig1 = plt.figure(1,dpi=300)
plt.rcParams.update({'font.size': 20})
for i in range(TDP):
    plt.plot(B_field,Rxy[i,:]/1e3, c = [.5,i/TDP,.7],
alpha=1,linewidth=3)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:

```

```

plt.gca().spines[axis].set_linewidth(2)
plt.xlim((-10,10))
plt.ylim((-30,30))
plt.xlabel('$\mu_0$H (T)',fontsize=20)
plt.ylabel('$R_x$ $R_y$ $(k\Omega)$',fontsize=20)
plt.grid(True)

Rxx_sym = (Rxx+np.fliplr(Rxx))/2
Rxy_asym = (Rxy-np.fliplr(Rxy))/2

fig2 = plt.figure(2,dpi=300)
plt.rcParams.update({'font.size': 20})
for i in range(TDP):
    plt.plot(B_field,Rxx_sym[i,:]/1e3, c = [.5,i/TDP,.7],
alpha=1,linewidth=3)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.xlim((-10,10))
plt.ylim((0,20))
plt.xlabel('$\mu_0$H (T)',fontsize=20)
plt.ylabel('$R_x$ $R_y$ $(k\Omega/sq.)$',fontsize=20)
plt.legend(("2K","5K","10K","20K","50K","120K","300K"),fontsize=12)
plt.grid(True)

fig3 = plt.figure(3,dpi=300)
plt.rcParams.update({'font.size': 20})
for i in range(TDP):
    plt.plot(B_field,Rxy_asym[i,:]/1e3, c = [.5,i/TDP,.7],
alpha=1,linewidth=3)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:
    plt.gca().spines[axis].set_linewidth(2)
plt.xlim((-10,10))
plt.ylim((-30,30))
plt.xlabel('$\mu_0$H (T)',fontsize=20)
plt.ylabel('$R_x$ $R_y$ $(k\Omega)$',fontsize=20)
plt.grid(True)

fig4 = plt.figure(4,dpi=300)
plt.rcParams.update({'font.size': 20})
for i in range(TDP):
    plt.plot(B_field,(Rxx_sym[i,:]/1e3-Rxx_sym[i,int((1-1)/2)]/1e3)/(Rxx_sym[i,int((1-1)/2)]/1e3), c = [.5,i/TDP,.7],
alpha=1,linewidth=3)
plt.gca().tick_params(axis="x", which='both', direction="in")
plt.gca().tick_params(axis="y", which='both', direction="in")
for axis in ['top','bottom','left','right']:

```

```

plt.gca().spines[axis].set_linewidth(2)
plt.xlim((-10,10))
plt.ylim((0,10))
plt.xlabel('$\mu_0$H (T)',fontsize=20)
plt.ylabel('MR',fontsize=20)
#plt.grid(True)

```