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An IC-Compatible Detector Process

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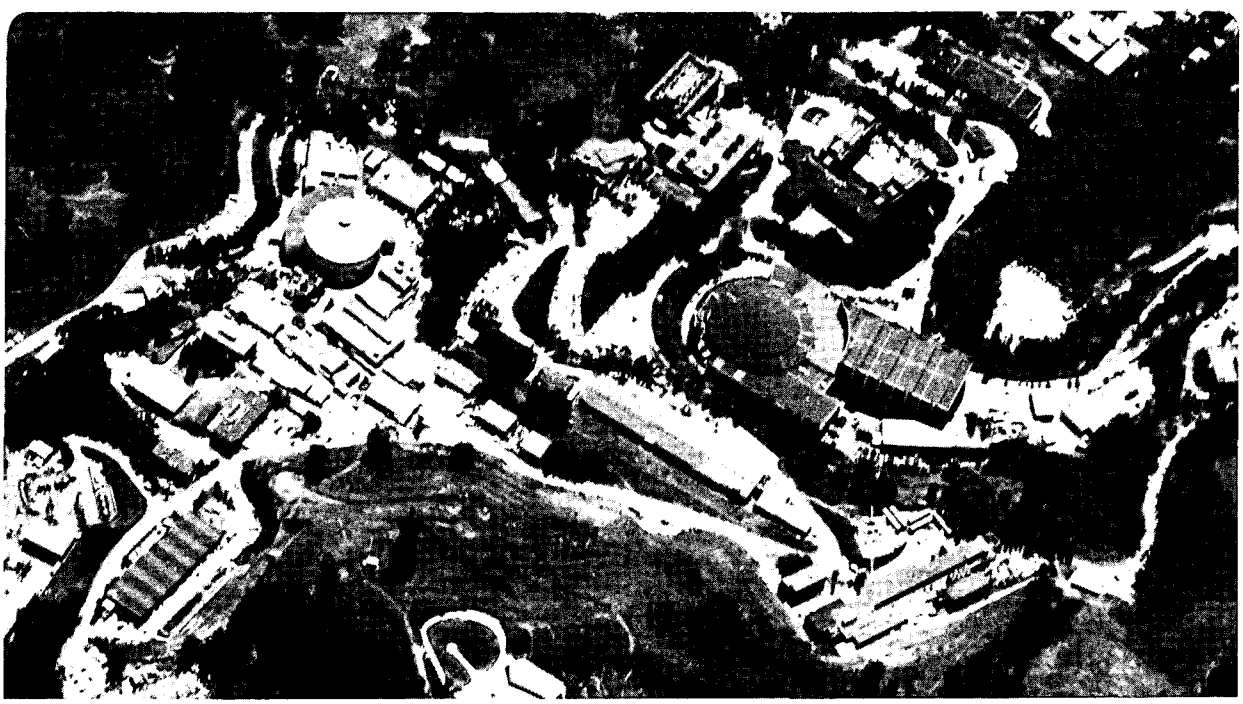

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ABSTRACT

A silicon radiation-detector fabrication process which exploits the excellent gettering properties of a backside layer of phosphorus-doped polysilicon has been developed and characterized. 2 mm diameter p-i-n diodes have been fabricated with typical reverse-bias current densities of approximately 1 nA/cm^2. In addition, a strip detector with 128 strips of 6 mm length on a 55 μm pitch has been successfully fabricated with better than 10% uniformity in the diode reverse-bias currents. The process is compatible with conventional integrated-circuit fabrication technologies, and p-channel enhancement and depletion-mode MOSFETs with associated inter-device isolation have been fabricated simultaneously on detector-grade silicon with p-i-n radiation detectors.

1. Introduction

The monolithic integration of semiconductor radiation detectors and electronic readout circuitry offers substantial benefits for many types of detectors. In configurations that need to minimize stray capacitance, integration of the detecting element with front-end circuitry is essential for optimum performance. In large-scale systems the resulting simplification could reduce cost and improve reliability.

A new process for the fabrication of silicon p-i-n diodes for use as radiation detectors was recently developed at the Lawrence Berkeley Laboratory and is described elsewhere [1]. The process utilizes a backside layer of in-situ doped polysilicon which acts as a sink for detrimental impurities that can cause excessive reverse-bias leakage currents. These detrimental impurities, which are typically metals such as gold, iron, copper, etc. are fast diffusers in silicon [2-3] and can be gettered by the backside polysilicon layer during normal annealing steps in the fabrication process. Once the impurities are removed from the sensitive depletion region, reverse-bias leakage current densities of approximately 1 nA/cm^2 can be achieved even after annealing steps at 900C [1], whereas similarly processed devices without a backside gettering layer have leakage currents two to three orders of magnitude larger than this value [1,4].

In this work, further results regarding silicon p-i-n diode fabrication using the gettering process are described, including the effect of the post-metallization anneal on the reverse-bias current and the fabrication of a strip detector. In addition, a process that monolithically integrates p-i-n diodes and p-channel enhancement and depletion-mode MOSFETs on the same wafer is described along with the observed device characteristics.

2. Detector fabrication and experimental results

The details of the detector process were described previously [1]. All of the devices used in this study were fabricated on high-resistivity (≈ 10kΩ–cm) float-zone refined silicon substrates. The crystalline orientation was <100> and the substrates were n-type. The key step to obtaining low reverse-leakage currents is the formation of the backside gettering layer, which is an approximately 1 μm thick layer of in-situ phosphorus-doped polysilicon. The polysilicon is doped during the deposition by adding phosphine to the silane gas flow in the low-pressure chemical vapor deposition reactor. In addition to gettering the layer serves as the backside contact of the p-i-n structure.

Polysilicon has been extensively used as a gettering layer in conventional integrated-circuit process technologies [5-10]. The effectiveness of phosphorus as a gettering agent was first recognized in 1960 [11], and has been extensively studied [12-18]. By the use of in-situ doped polysilicon, both polysilicon and phosphorus are present on the back side of the wafer for gettering. The in-situ doping process eliminates a high temperature step that would otherwise be necessary to diffuse phosphorus into the polysilicon layer.

In addition to the backside gettering, various steps are taken during the processing to minimize contamination. The wafers are cleaned before all furnace operations with the exception of the final post-metallization anneal in the following sequence: Initially the wafers are cleaned in 5 to 1 $H_2SO_4 : H_2O_2$ solution at 120C followed by a dilute HF etch. The wafers are then cleaned in a 5:1:1 solution consisting of $H_2O : NH_4OH : H_2O_2$ at 65C, with a dilute HF etch before cleaning in 5:1:1 $H_2O : HCl : H_2O_2$ at 65C. The wafers are rinsed between cleans in deionized water. The HCl-based etch is particularly suited for removal of metallic contamination from the wafer surface given the high affinity of chlorine for metallic elements. In addition to wafer cleaning, the furnace tubes are cleaned whenever possible prior to the furnace step by flowing trichloroethane (TCA) mixed with oxygen at 1100C where again the chlorine present in the TCA acts to remove metallic contaminants from the furnace tube.

Figure 1 shows the distribution of reverse-bias current densities at 100V before and after the post-metallization anneal in forming gas (80% N_2, 20% H_2) at 400C. The devices used in these measurements were circular diodes with a 2 mm diameter surrounded by a p^+ guard ring to collect surface currents and minority carriers from outside the active area of the diode. The 100V bias is sufficient to completely deplete the approximately 250 μm thick lightly-doped region between the front-side p^+ contact and the backside n^+ contact. In Figure 1a the passivating oxide was grown in dry oxygen with TCA, whereas a steam-grown oxide was used for Figure 1b.

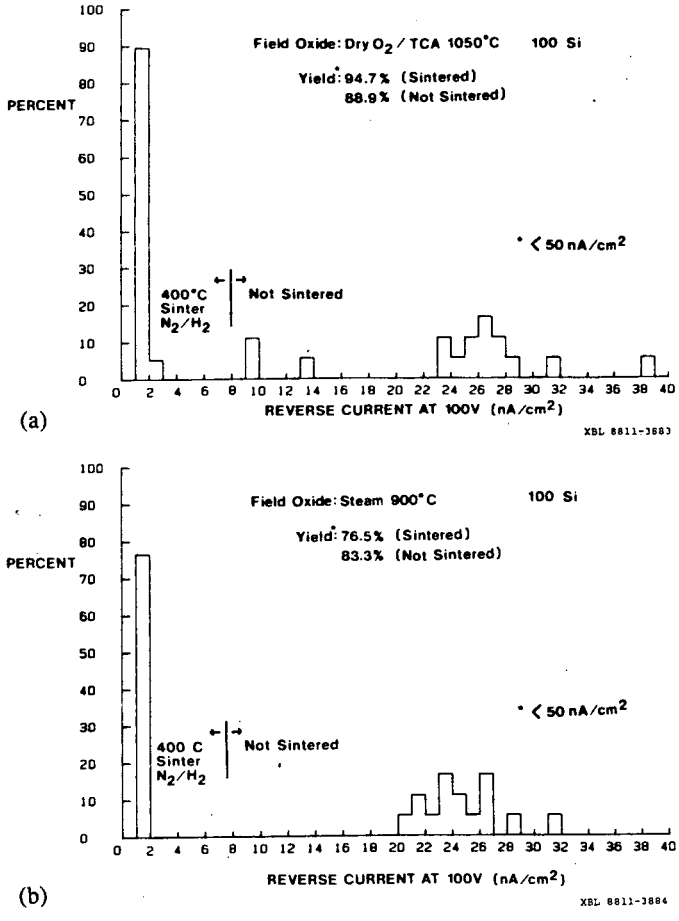


Figure 1. The distribution of reverse-bias leakage currents for 2 mm diameter diodes before and after sintering in forming gas at 400C for 20 minutes. The detector bias voltage was 100V.

(a) Passivating oxide grown in dry oxygen with TCA at 1050C.

(b) Passivating oxide grown in steam at 900C.

As can be seen, before the 400C sintering process the distribution of reverse-bias currents is rather broad and the observed currents are much larger than the 1-2 nA/cm^2 values observed after sintering. This is an indication of currents arising from electrically active interface states at the silicon-silicon dioxide interface, as the forming gas anneal is well known to reduce interface state densities in metal-oxide-semiconductor (MOS) devices and hence would be expected to reduce the component of current arising from the surface [19].

One also notices a significantly lower yield when the passivating oxide is grown in steam as opposed to dry oxygen with TCA (76.5% versus 94.5% after sintering). In this case yield is defined as the percentage of diodes with leakage current less than 50 nA/cm^2 at 100V bias. Although the statistics are somewhat limited in that approximately 20 devices were tested for each grouping in Figure 1, the effect does appear to be significant and will require further study. The one difference in the two oxidation conditions is the injection of silicon interstitials into the silicon substrate when the oxide is grown in steam, and interstitials have been shown to nucleate into defects in float-zone silicon under certain conditions [20-21]. However, more work is necessary to determine if this is the cause of the lower yield for the steam-grown devices.

In addition to the 2 mm diameter diodes, a strip detector was also fabricated. This device consists of 128 strip-like junctions, each 15 μm wide and 6 mm long, with a 55 μm pitch (the distance between the centers of adjacent diodes). The entire device is surrounded by a guard ring. Figure 2 shows the reverse-bias current at 100V bias for each diode in the detector. The bias voltage was applied to the substrate and the diode under test was grounded, along with the guard ring and the two adjacent diodes on either side of the diode under test. The remaining diodes were floating. The cause for the increased current on the edge diodes is believed to be due to the fact that the guard ring is spaced 150 μm from the edge diodes and hence the volume over which the edge diodes collect minority carriers is larger than that for the inner strips. Figure 3 shows the distribution of reverse-bias leakage currents. Neglecting the edge devices, the standard deviation in the current is less than 1 pA and the uniformity is 8.1% where uniformity is defined as

$$\text{Uniformity} = \frac{\text{Max} - \text{Min}}{2 \times \text{Mean}} \times 100 \ \% \qquad (1)$$

The passivating oxide for the strip detector was grown in dry oxygen/TCA.

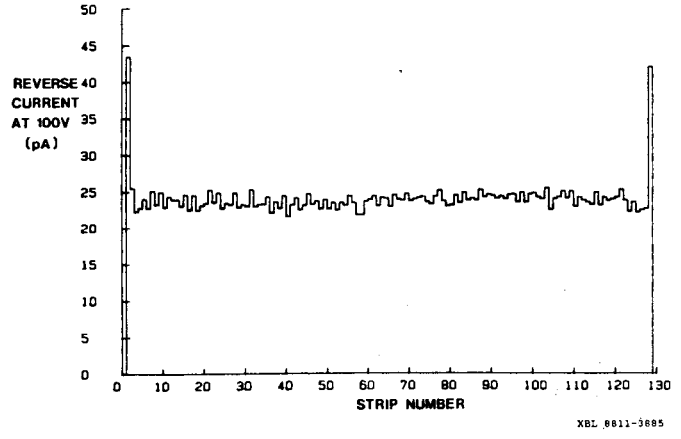


Figure 2. The reverse-bias current at 100V bias for the strip detector described in the text versus the strip number.

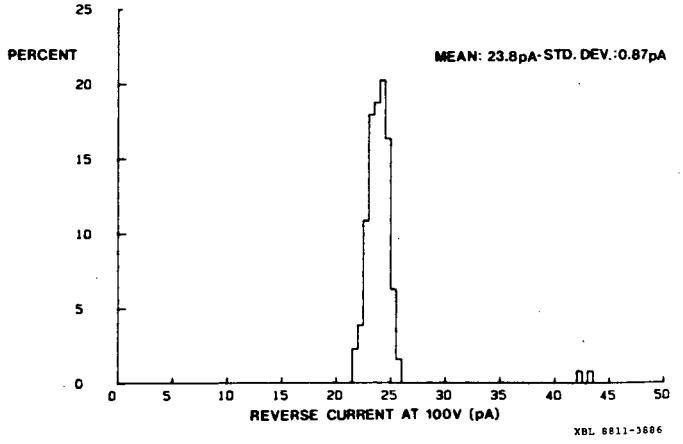


Figure 3. The distribution of reverse-bias currents for the strip detector from Figure 2. The statistics do not include the edge strips.

As the previous results show, the use of backside gettering does consistently yield low-leakage p-i-n diodes suitable for use in particle detection. A key point is that the gettering process allows reduced sensitivity to harmful contaminants in that the gettering will be effective as long as the impurities have sufficient time to diffuse and be trapped, and as long as the concentration of impurities does not exceed that of the gettering sites. In addition, the process used is compatible with conventional integrated-circuit processing technologies. In the next section a process which combines active devices on the same substrate with p-i-n diodes is described.

3. IC-Compatible Detector Process

Given the good performance of the process, an investigation was begun to determine the compatibility of the process with active device fabrication. The ability to integrate electronics on the same substrate as the detector could potentially yield great benefits in terms of performance and reliability in that the number of external connections to the detector could be minimized. For certain applications, most notably the silicon drift chamber [22], the performance inherent in the detector can only be exploited with the use of monolithically-integrated electronics.

The approach taken has been to attempt to integrate active devices on the same substrate with the detector using standard, conventional processing technologies. P-channel MOSFET technology has been chosen for the investigation. The main driving force for this technology choice is that this is the simplest technology from a processing point of view that allows integration of the detector p-i-n diodes with active devices while still maintaining the in-situ doped polysilicon gettering layer on the backside of the wafer. The main drawbacks of this technology are the lower hole mobility when compared to electron mobility in n-channel MOSFETS [23] and the fact that the source and drain junctions of the transistors will also collect charge generated in the substrate. This will be of less concern for applications involving a collimated radiation source or for those applications where some "dead area" is acceptable. In addition, the devices must be designed to withstand the detector bias which in general must be large enough to completely deplete the substrate. Another drawback is the inability to cascode load devices in order to increase the output impedance of integrated amplifiers as is possible in the significantly more complex CMOS or bipolar technologies [24]. However, the work reported here forms a subset for the integration of CMOS devices on high-resistivity silicon as many of the problems addressed here apply to CMOS as well.

In the previous report on the detector process, p-channel MOSFETs were fabricated simultaneously with detector diodes on high-resistivity silicon while maintaining low reverse-bias currents in the detector diodes [1]. In other reported work MOS devices were fabricated on high-resistivity silicon [25]. In reference [1] the p-channel devices did not receive a threshold-adjusting ion implantation, nor was there any provision to inhibit inversion of the field region between transistors. Both of these features are essential if these devices are to be usable in integrated circuitry. In the discussion that follows, a more realistic process is described that includes these features.

The process used in this work is based on the the conventional local-oxidation of silicon process (LOCOS) [23, 26]. The

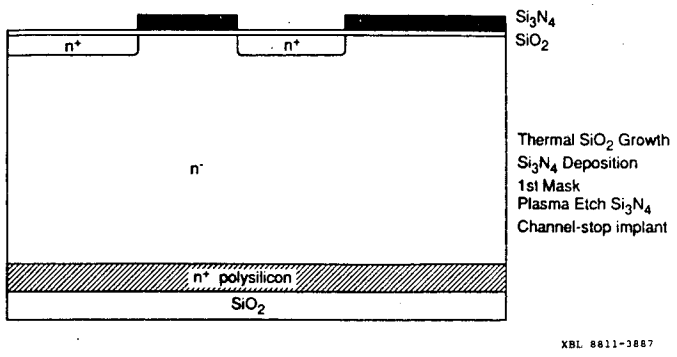


Figure 4. Device cross-section after P^+ implantation for the IC-compatible detector process.

cross-section of a device after the first mask is shown in Figure 4. Initially, an oxide is thermally grown on a substrate prepared with the backside gettering layer present. The purpose of this oxide is to minimize defects that could be generated in the silicon substrate due to the differing thermal expansion coefficients of silicon and silicon nitride. A 1000A layer of silicon nitride is then deposited by low-pressure chemical vapor deposition at 800C. The nitride is then masked and etched in a plasma reactor operating at 50W and 225 mTorr using SF_6 as the reactant gas. After etching of the silicon nitride the wafers are implanted with P^+ ions in order to increase the doping density in the region between the transistors. After this step the nitride is removed in the regions where detector p-i-n diodes are desired. This requires an additional mask when compared to the standard MOS process. The function of this additional step is to prohibit implantation into the sensitive diode area where the damage resulting from implantation could degrade the reverse-leakage current of the detector diodes.

With the nitride still in place in the transistor regions, the wafers are placed in an oxidizing ambient and a relatively thick field oxide is grown. The resulting device cross-section after nitride removal is shown in Figure 5. The patterned nitride film blocks diffusion of oxygen resulting in field oxide growth only in those regions where the nitride is not present. Since silicon is consumed during the oxidation process (44% of the final thickness of the silicon dioxide) the final oxide is recessed into the silicon as shown in Figure 5 [23].

After the field oxidation the oxide which was underneath the silicon nitride is removed by etching, and another nonstandard

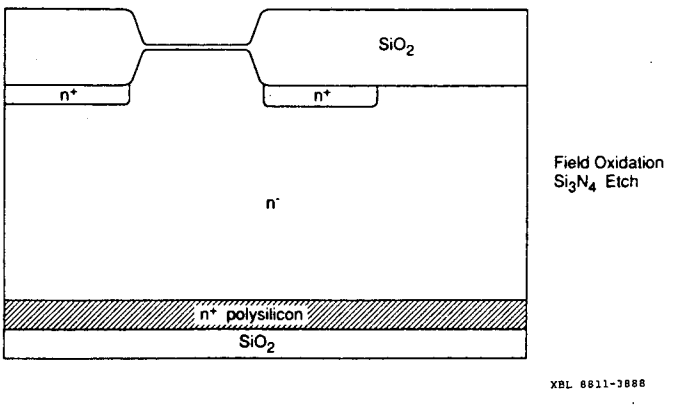


Figure 5. Device cross-section after the field oxidation.

mask is used to etch openings in the field oxide for the p^+ contact of the detector p-i-n diodes. At this step a sacrificial gate oxide for the MOS transistors is grown in steam at 800C to a nominal thickness of 20 nm. BF_2^+ or As^+ ions are then implanted into selected transistor channel regions (the region defined by the silicon nitride mask) using photoresist as a mask to block the implants where they are not desired. The function of this implant is to set the turn-on or threshold voltage of the MOS transistors. Again, the implants are not allowed in the sensitive diode regions.

The sacrificial gate oxide is then etched and the gate oxide is regrown as before. Undoped polysilicon is subsequently deposited, masked and plasma etched to form the gate area of the transistors. The gate oxide in the regions not covered by the polysilicon (including the detector diode regions) is etched and boron is diffused from a B_2O_3 source simultaneously doping the source and drains of the transistor, the gate polysilicon, and the detector diode. The cross-section after this step is shown in Figure 6. The structure to the left is the MOS transistor and the structure on the right forms a p-i-n diode with the backside contact. The remainder of the processing is conventional.

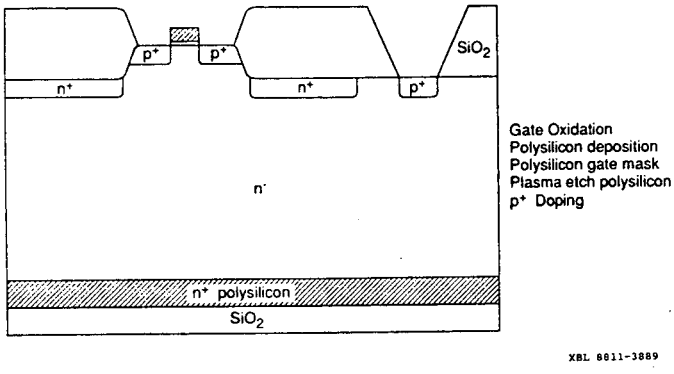


Figure 6. Device cross-section after boron doping. The device on the left is a p-channel MOS transistor while the device on the right forms a p-i-n diode.

Figure 7 shows the linear region current-voltage (I-V) characteristics of p-channel devices fabricated on the same wafer. The channel width is 25 μm and the channel length is 5 μm. As can be seen, the device receiving the As^+ implant turns on at a gate voltage of approximately - 0.5V, while the BF_2^+ implanted device is conducting at zero gate-source voltage and is hence a depletion-mode device. The unimplanted device turns on at a gate voltage of approximately 0V. Note that the unimplanted device is not suitable for digital CMOS because the threshold voltage is near 0V and hence turning off this device for logic applications would be difficult. Hence a CMOS technology on high-resistivity silicon will likely require implanted p-channel MOSFETs and therefore the work reported here is a component of CMOS technology development on high-resistivity silicon.

The implanted dopants used in this study are somewhat nonstandard, i.e. B^+ and P^+ would be more typical. The choice of As^+ and BF_2^+ is due to their larger mass when compared to the typical dopants. As a result one obtains shallower implants [27], typically 300-500A at the implant energies used in this study. The use of shallow implants is necessary in order to minimize the body effect, which is the variation of the transistor threshold

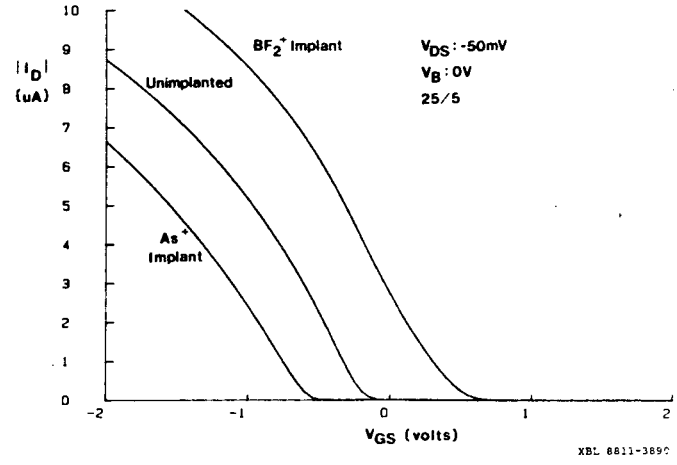
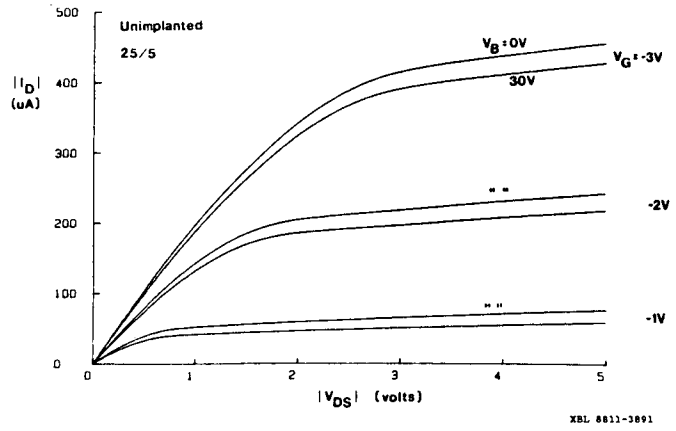


Figure 7. Linear region current-voltage characteristics for p-channel devices fabricated on high-resistivity silicon.

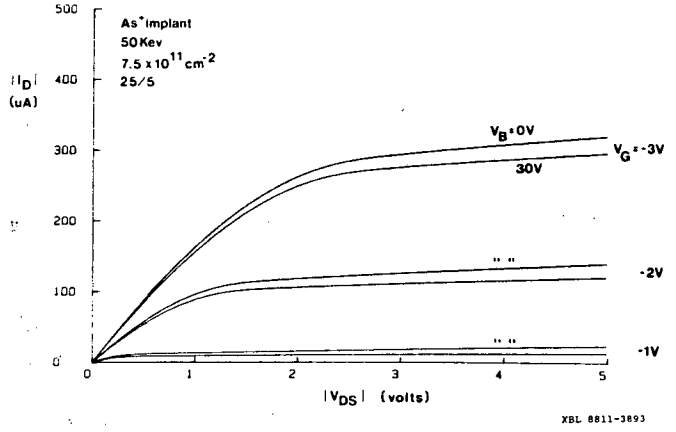
voltage with substrate bias [23]. This problem is particularly acute in this technology where the devices must withstand the detector bias voltage. For the resistivity (≈ 10 kΩ–cm) and thickness (≈ 250 μm) of silicon used in this work the required bias voltage to achieve full depletion of the substrate is on the order of 20V, which is much larger than the typical supply voltage in conventional integrated circuits. In fact, a tradeoff between process complexity and device design exists. The relatively simple processing necessary to make p-channel transistors results in more stringent demands on the device design since the devices must withstand the detector bias, and this problem is magnified when lower resistivity and/or thicker substrates are used (which result in higher bias voltages and electric fields when the substrate is completely depleted). Devices in wells which are biased separately from the substrate would have a large advantage in this case, although at the expense of additional process complexity.

Figure 8 shows the effect of the substrate bias on the output I-V characteristics for all three types of transistors. As can be seen, the effect of a bias of 30V on the substrate (which is sufficient to overdeplete the substrate) is to reduce the output current slightly, on the order of 10% at a gate voltage of -3V. Nevertheless, the transistors still behave normally even with the substrate overdepleted.

With the availability of a depletion-mode device, it is possible to achieve higher gain in amplifiers for the same silicon area than is possible when only enhancement-mode devices are present, particularly when the body effect is minimized [28]. This is due to the fact that the small-signal output impedance looking into the source of a depletion-mode device with gate shorted to source is simply the output impedance of the transistor itself if the body effect is negligible [24]. However, for enhancement-mode devices the small-signal impedance looking into the source of a saturated device is the inverse of the device transconductance, again assuming negligible body effect [24]. Thus enhancement-mode load devices will necessarily require small width to length ratios in order to achieve high impedances. This will, however, typically result in much larger areas necessary for the load devices when comparing enhancement-mode devices to depletion-load devices biased at the same current [28].



(a)



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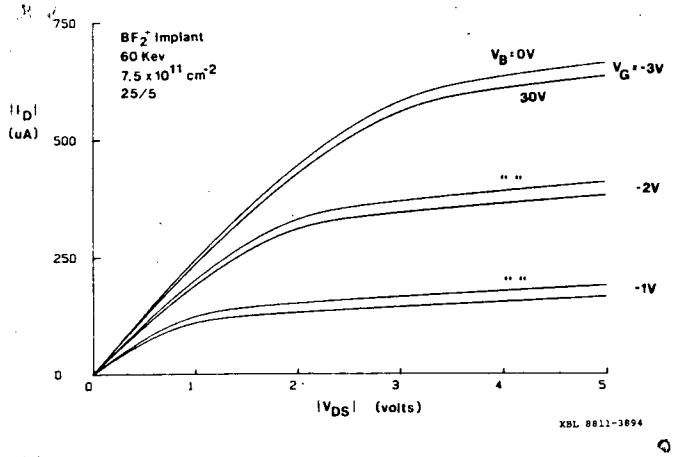

(c)

Figure 8. Output current-voltage characteristics for p-channel devices fabricated on high-resistivity silicon showing the effect of the detector bias on the output current. The bias of 30V results in an overdepleted detector.

(a) Unimplanted device.

(b) As^+ implanted at an energy of 50 Kev and a dose of 7.5×10^{11} cm^{-2}.

(c) BF_2^+ implanted at an energy of 60 Kev and a dose of 7.5×10^{11} cm^{-2}.

Figure 9 shows the transfer characteristic of a common-source amplifier using an unimplanted input device and a depletion-mode load. The amplifier achieves a small-signal gain of approximately 40 with the substrate overdepleted at a substrate bias of 30V. For the device geometries used, the quiescent current when the amplifier is biased in the active region is approximately 1-2 μA. Improvements in gain can be achieved by cascoding the amplifier and adding a device to inject current into the input device to increase its transconductance while keeping the bias current in the load devices low enough to maintain high output impedance [22,28]. By virtue of the demonstration of an amplifier on high-resistivity silicon, this p-channel technology with depletion-mode devices could in fact be a viable technology for certain applications. In any event, the p-channel device development is an essential step to CMOS technology development.

Measurements on 2 mm diameter diodes fabricated on the same substrate as the transistors yielded reverse-bias currents of less than 1 nA/cm^2 at a detector bias of 100V, i.e. the additional processing necessary for the fabrication of active devices did not degrade the detector diodes. However, an increase in current was observed on the guard ring of the detector diodes. This is believed to be due to punchthrough from p^+ regions at the edge of the die which, because of the layout and the mask aligner used, are biased at the substrate potential. A similar problem was observed on the initial attempt to fabricate the strip detector, and the problem was corrected with a simple layout change (after the layout correction the guard ring current for the strip detector referred to in Figure 2 was less than 10 nA).

4. Summary

The process described appears to be a good candidate for the fabrication of silicon p-i-n diodes to be used as radiation detectors. The backside layer of polysilicon efficiently getters unwanted impurities and reduces the sensitivity of the process to such impurities. Low reverse-bias leakage currents are consistently achieved, and good uniformity was observed in the reverse-bias

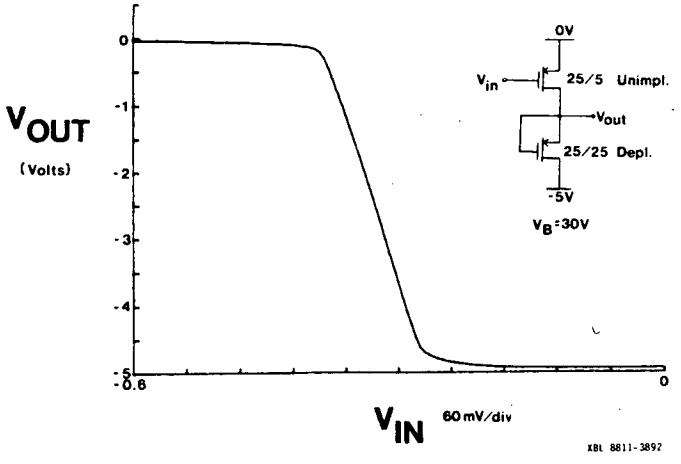

Figure 9. Transfer characteristics of the common-source amplifier shown in the inset. The 30V substrate bias is sufficient to overdeplete the substrate.

currents for a strip detector. A major point is that the process is compatible with conventional integrated-circuits fabrication technologies, and a viable technology for some applications which includes active devices integrated on the same substrate with the detector has been presented. The technology includes LOCOS isolation and ion-implanted p-channel MOSFETs. A simple amplifier made from devices on the high-resistivity silicon has been shown to achieve a small-signal voltage gain of 40 in an overdepleted substrate. Further work is necessary to explore the limitations of this technology in terms of compatibility with thicker and/or lower resistivity substrates. This demonstration of a realistic technology for the integration of active circuitry on high-resistivity silicon is an essential step toward more advanced technologies that include CMOS or JFET-based structures monolithically integrated with semiconductor radiation detectors.

5. Acknowledgements

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