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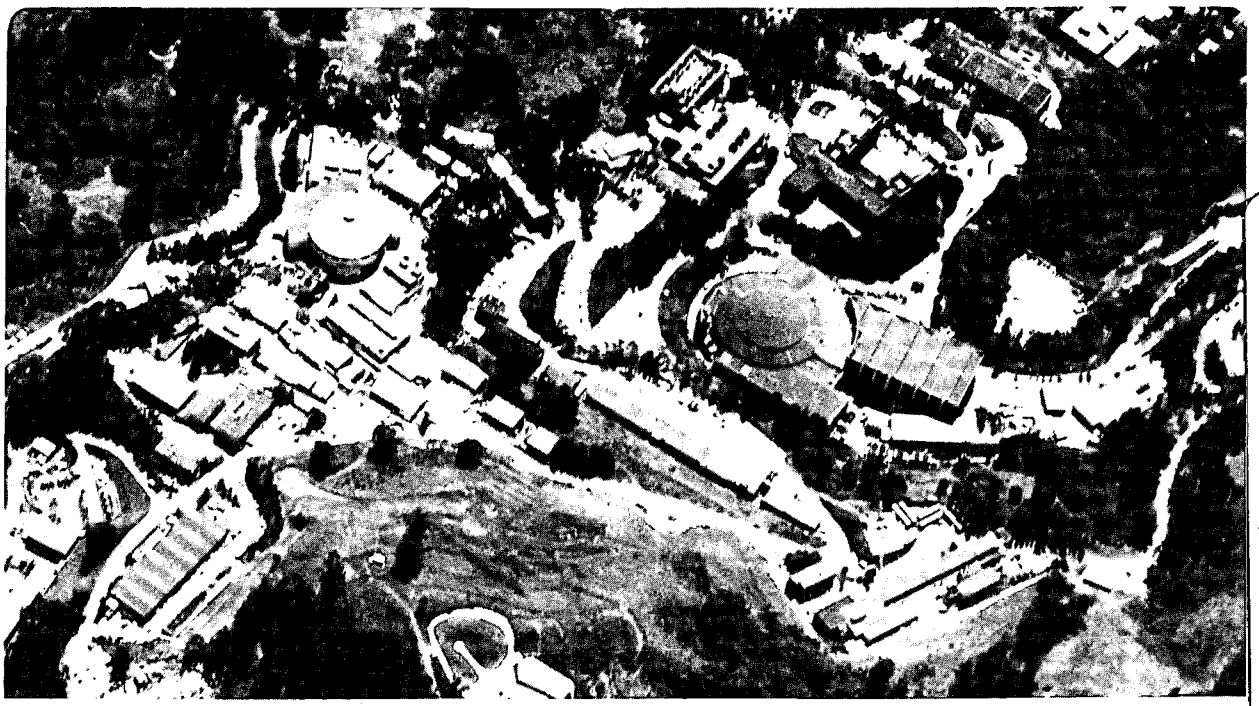



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## DISCLAIMER

# TFT Amplifiers for Amorphous Silicon PIXEL Particle Detectors

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*Abstract*

We have investigated the application of thin film electronics technology to making a signal amplifier and read-out circuit for amorphous silicon PIXEL particle detectors which can detect minimum ionizing particles. Characteristics of currently available TFTs are reviewed and preliminary designs of a-Si:H and poly-Si amplifiers for a 300 μm x 300 μm PIXEL array are proposed. Based on measurement of small signal parameters and noise spectrum of individual a-Si:H and poly-Si TFTs, the overall gain, time-response and signal-to-noise ratio are calculated.

## I. INTRODUCTION

Position sensitive radiation detectors have become an essential tool in many fields of scientific research. For example, good spatial resolution as well as a fast time response is very important in the tracking detectors and digital calorimeters for high energy physics experiments. The 511 KeV gamma ray detectors for PET also requires good spatial resolution, energy resolution and a fast time response. Real time x-ray digital imaging and *in vivo-* or *in vitro-*radioisotope tracer imaging for medical or biological applications usually require spatial resolution and energy resolution. Material science applications, such as, x-ray crystallography, x-ray microscopy and nondestructive x-ray imaging also require fine spatial resolution. Depending on the application, many different types of 1-D or 2-D detectors are used. For example, films for x-ray flux detection, scintillators with a photodetector or CCD for single x-ray detection[1], drift chambers or Si strip detectors for high energy particle tracking measurement, etc., are currently used[2,3].

In many applications, 2-D detectors are preferrable due to the unambiguous track determination and the high signal-to-noise ratio. However in the case of 2-D electronic detectors, signal read-out is more difficult than for 1-D detectors. A detector read-out system under study at LBL and other labs combines crystal silicon 2-D detectors and VLSI electronics by using an indium bump cold welding technique[4,5]. This method is expected to be expensive, especially when used over a large area.

An alternative solution for making cheap and large area 2-D radiation resistant pixel detectors with a relatively fast read-out scheme is to use hydrogenated amorphous silicon (a-Si:H) thin film techniques on substrates. This paper reviews the current status of a-Si:H thin film technology and proposes a simple design of 2-D a-Si:H detectors for single minimum ionizing particle (MIP) detection, together with integrated thin film amplifiers.

## II. A-Si:H THIN FILM TECHNIQUES

Currently a-Si:H is widely used for solar cells, light sensing diodes for electrophotography, and for switching TFTs of LCD drivers. The typical thickness of these devices is a few μm. When used as ionizing particle detectors, thick films are desirable in order to get a large signal size. A-Si:H is usually deposited as a film on various substrates in rf-discharge chambers. A typical growth rate is one μm per hour in 13.5 MHz rf discharge of silane gas and devices up to 50 μm thick have been produced. Higher growth rates have been reported at higher frequencies[6,7].

Table 1 is a summary of estimated and measured properties of several noncrystalline TFTs. We are primarily interested in 4 μm a-Si:H TFT technology as a candidate for pixel electronics because of the present industrial experience with it[8,9]. Properties of poly-silicon vary with annealing temperature and up to now the best poly silicon is known to be annealed at 900°C[10,11,12] which is far beyondthe a-Si deposition temperature of 250°C. In the case of using poly silicon electronics with a-Si:H detector, we need a high temperature substrate such as quartz and interconnection metals

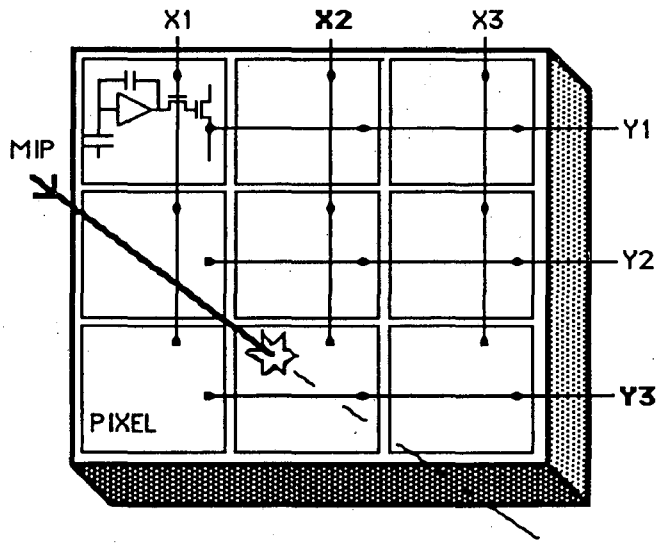


Fig. 1. 3x3 prototype 300 x 300 μm² pixel detector array with read-out scheme showing a MIP hiting a pixel (X2,Y3)

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Table 1 Estimated properties of various TFTs

| | L (μm) | W/L | $\mu_{fe}$ ($cm^2$/Vs) | $C_{in}$ (fF) | $g_m$ (μA/V) | Freq Limit (MHz) | Noise* ( rms in e) | Radiation Resistance |
|---|---|---|---|---|---|---|---|---|
| a-Si:H TFT | 8 | 1~60 | 0.3~0.8 | 6~600 | 1~5 | 1~5 | 90~900 | Excellent |
| a-Si:H TFT | 4 | 1~60 | 0.3~0.8 | 3~200 | 1~10 | 1~10 | 50~400 | Excellent |
| a-Si:H VTFT | 0.2~1 | NA | 0.3~0.8 | NA | 10~300 | 10~100 | > 1000 | Unknown |
| 900°C poly Si | 4 | 1~60 | 20~40 | 3~200 | 10~700 | 500 | 40~500 | Excellent |
| 400°C poly Si | 4 | 1~60 | 10~20 | 3~200 | 5~300 | 100 | > 500 | Unknown |
| SOI | 1~4 | 1~60 | ~700 | 1~200 | 200~2000 | ~10000 | same as c-Si | Excellent |

* Noise value given in the table is estimated when $C_D = C_{in}$.

with a high melting point. The poly-Si electronics should be fabricated on the substrate and then the a-Si:H detector deposited on top of the electronics.

## III. A-Si:H PIXEL DETECTOR

We have studied the feasibility of detecting minimum ionizing particles (MIP) with a-Si:H radiation detectors[13,14]. The specific ionization energy (W-value) in a-Si:H was estimated to be about 6 eV based on X-ray detection[15] which gives the linear ionization density of 60~70 electrons/μm. MIP measurement with betas seemed to give a little higher value than that[13]. For the calculation of the charge collection efficiency of the proposed pixel detector, we will assume that ionizaion density of MIP is about 70 electrons/μm in a-Si:H. Typical leakage current density of 20~40 μm thick pin diodes were less than $5x10^{-7}$ A/$cm^2$ up to a detector bias at which reversible microbreakdown starts to happen. The leakage current will induce noise current, *i*, in parallel with the signal current, $I_D$, which will be added to the amplifier noise.

$$i^2 = 2\,q\,I_D\,\Delta f \qquad (1)$$

The proposed detector is a 300 x 300 $\mu m^2$ 2-D pixel array which is shown in Fig. 1. When a MIP hits an element of the array the position information, for example, (X2,Y3) in Fig. 1, as well as the analog signal will be read out by external addressing circuitry through common bus lines. Figure 2-(a) shows a cross section of a direct ionizing pixel detector and the interdigitated electodes which are used to reduce the detector capacitance. Every component is proposed to be manufactured in sequence by deposition processes on a large thin substrate.

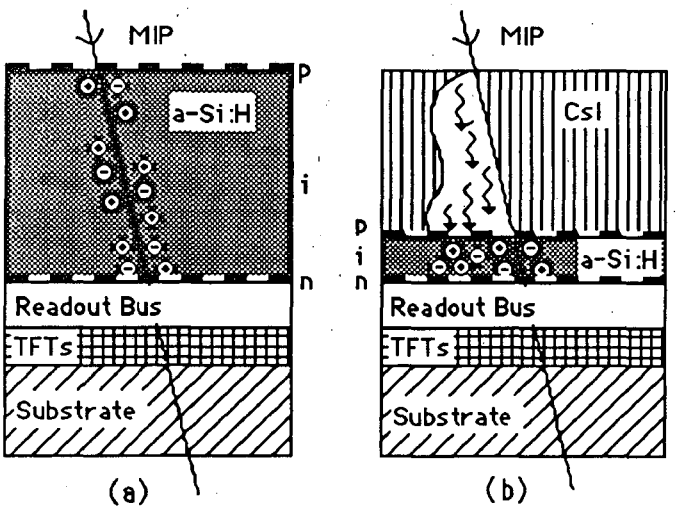



Fig. 2. Cross sectional views of (a) a direct ionizing pixel detector ; 50 μm thick pin diode and (b) a CsI scintillator coupled pixel detector ; 2 μm thick pin diode

The detector consists of a reverse biased pin diode having a thick i-layer in which e-h pairs generated by interactions between MIPs and Si atoms drift toward the p and n contact layers, inducing a signal current flowing and being integrated in the amplifer. The integrated signal current or collected charge is determined by the detector properties, thickness, and the integration time. Generally the collected charge, $Q_{col}$, is

$$Q_{col} = q \times \eta_{col} \times n \times t_D \qquad (2)$$

where n is the linear ionization density and $t_D$ is the detector thickness. The collection efficiency, $\eta_{col}$ is calculated as a function of detector thickness, bias, integration time and material parameters such as the ionized dangling bond density, $N_d^*$, mobilities and lifetimes of charge carriers with an assumption of uniform ionization in a-Si:H by single MIP comming perpendicularily to the detector. Table 2 shows the typical values of these material parameters measured by time-of-flight method[16]. Figure 3 shows the calculated chage collection efficiency in a 50 μm thick detector as a function of integration time (RC time when RC-CR shaper is used) at 1500 V which depletes the i-layer fully. Most electrons are collected within 10 nsec and one third of the holes are collected within 1 μsec. The collection efficiency saturates at 10 μs and is 0.77. The net equivalent signal charges collected in two shaping times, 0.2 μs and 1 μs are 1790 and 2220 electrons respectively. Based on these numbers we will calculate the signal size and signal-to-noise ratio.

Although this paper is concerned mainly with 50 μm thick direct ionizing pixel detectors, it is worthwhile to mention an alternative scheme: a scintillator coupled to a thin photo-detector shown in Fig. 2-(b). At present deposition of columnar structure CsI on a-Si:H films is under study at LBL. Due to the large photon yield from a thick CsI scintillator, signal size and signal-to-noise ratio (S/N) of this system can be much larger than the thick direct ionizing detector. Also due to the small thickness of diodes (~2 μm) collection efficiency would be more than 90 % and signal rise time will be less than a few nsec. An interdigitated electrode scheme is necessary to keep the detector capacitance small.

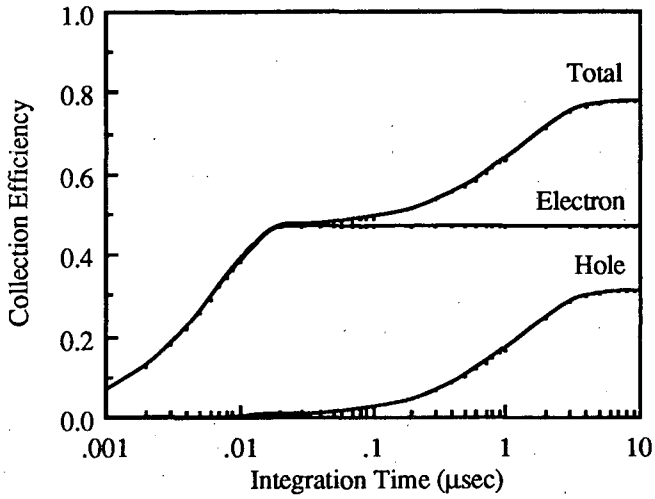



Fig. 3. Calculated charge collection efficiency for a 50 μm thick a-Si:H pixel detector at 1500 V

Table 2 Input parameters for collection efficiency calculation

| $N_d^*$ (#/cm$^3$) | $\mu_e$ (cm$^2$/Vsec) | $\mu_h$ (cm$^2$/Vsec) | $\tau_e$ (sec) | $\tau_h$ (sec) |
|---|---|---|---|---|
| 7 x $10^{14}$ | 1.2 | 0.004 | 1 x $10^{-7}$ | 4 x $10^{-6}$ |

## IV. MEASUREMENT OF TFT PROPERTIES

We have tested some a-Si:H and poly-Si TFTs made at XEROX PARC. Basically TFTs are field effect transistors with structures as shown in figure 4. Due to the higher deposition temperature of silicon nitride than that of amorphous silicon, a-Si:H TFTs are usually made as a staggered inverted type, ie. the gate is at the bottom. Dimensions of test TFTs are the following; (a) Channel length, L = 4 ~ 20 μm, (b) Channel width, W = 16 ~ 256 μm, and (c) Gate insulator ; silicon nitride for a-Si TFTs ($t_N$ = 0.3 μm) and silicon oxide for poly-Si TFTs ($t_O$ = 0.2 μm).

Figure 5 shows a typical I-V curve of a sample a-Si:H TFT (W/L = 256/4). A simple crystal Si MOSFET model of drain current, $I_d$, for saturation region ($V_{DS} > V_G - V_T$) [17],

$$I_d = \frac{\mu_{fe} C_i}{2} \times \frac{W}{L} \times (V_G - V_T)^2 \qquad (3)$$

fits the measurements very well up to 20 V at the gate. Similar curves are obtained for poly-Si NMOS and PMOS. The threshold voltage and the field effect mobilities are also measured. As shown in Table 3, the field effect mobility of a-Si:H is less than a half of the drift mobility shown in table 2.

The equivalent noise voltage (ENV) spectrum from a single TFT is analyzed as a sum of two different noise sources[18], Nyquist noise, due to the finite channel resistance, and flicker noise, due to the fluctuation of electron density in the channel.

$$v^2 = 4\,kT\left(\frac{2}{3\,g_m}\right)\Delta f + \frac{K_f}{C_i WL \times f^{\alpha}}\Delta f \qquad (4)$$

where $v^2$ is the ENV power at frequency, f. $C_iWL$ is the input capacitance of the TFT(=$C_{in}$) and α is the slope in log($v^2$) vs f plot. The noise spectrum is obtained by measuring the drain current fluctuations with a low noise amplifier in a shielded probe station[19]. Figure 6 is a measurement of ENV for a typical a-Si:H TFT. $K_f$ and α are material- and process-dependent constants and the measured values are listed in Table 3. For poly-Si TFTs, α is slightly lower than 1 and this causes the shaping time dependence of the flicker noise as explained below.

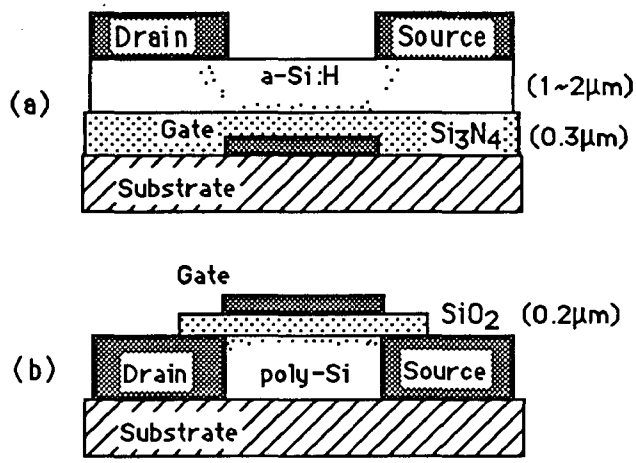



Fig. 4. (a) Schematic structure of an a-Si:H TFT (Staggered inverted type) (b) Schematic structure of a poly-Si TFT

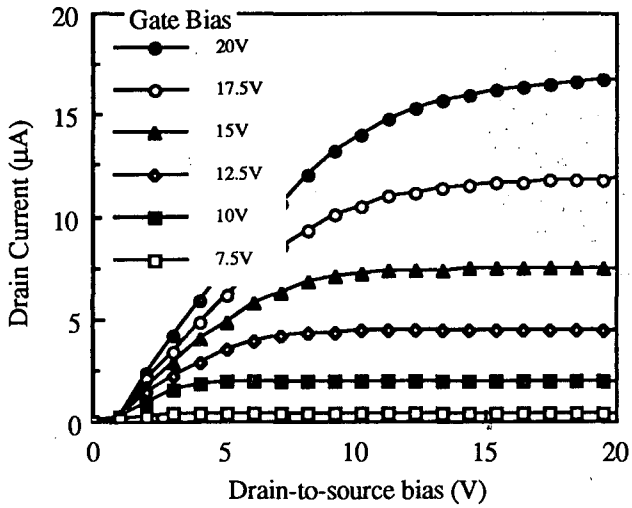



Fig. 5. Measured I-V curves of an a-Si:H TFT (W/L= 256/4 μm)

Table 3 Measured parameters of a-Si:H and poly-Si TFTs

| Type | Insulator (μm) | $V_T$ (V) | $\mu_{fe}$ (cm$^2$/Vs) | $K_f$ ($10^{-20}$ VC) | α |
|---|---|---|---|---|---|
| a-Si:H TFT | $Si_3N_4$ 0.2 ~ 0.3 | 2 ~ 3 | 0.25 ~ 0.35 | 1. ~ 2. | ~ 1.0 |
| poly-Si NMOS | $SiO_2$ 0.1 ~ 0.2 | 1 ~ 2 | 10 ~ 20 | 0.01 ~ 0.02 | ~ 0.78 |
| poly-Si PMOS | $SiO_2$ 0.1 ~ 0.2 | 1 ~ 2 | 10 ~ 20 | 0.007 ~ 0.01 | ~ 0.8 |

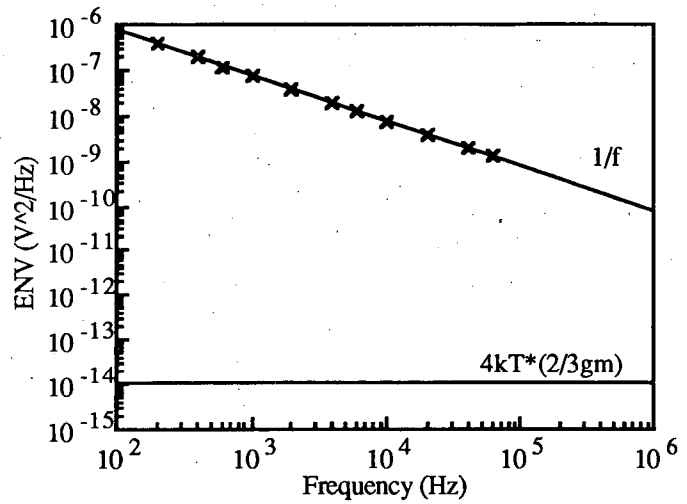



Fig. 6. Measured noise voltage spectrum of a typical a-Si:H TFT (L= 4 μm & W = 256 μm) at $V_{DS}$ = 20 V, Vg = 17.5 V ( x measurement data, __ estimated Nyquist noise ($g_m$ = 2.5 μA/V)

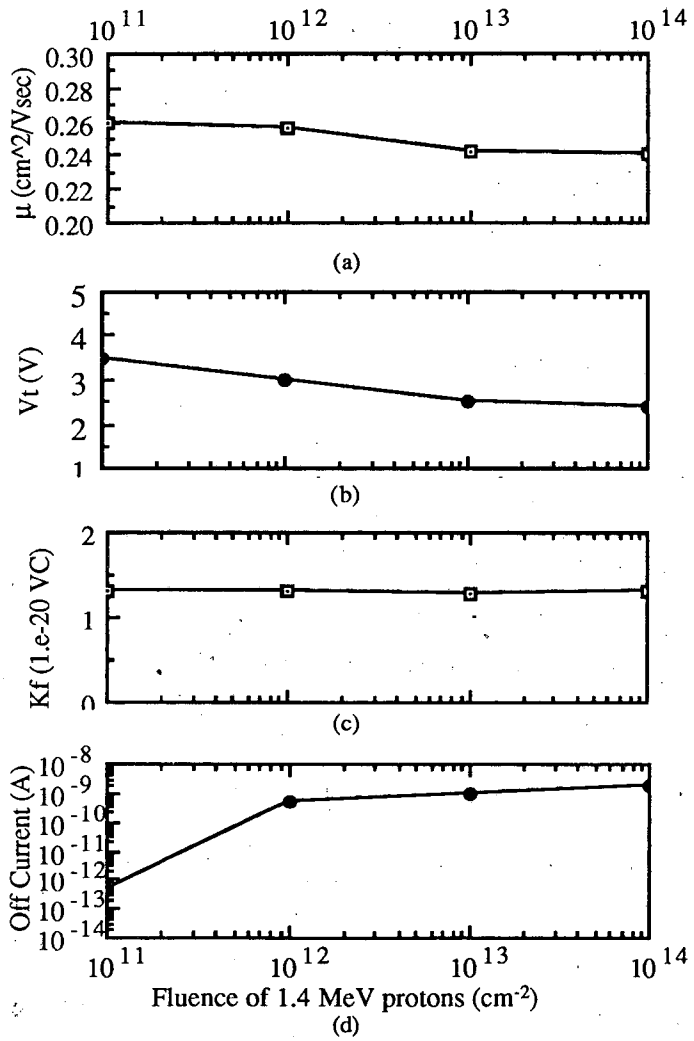



Fig. 7. Change of parameters of a typical a-Si:H TFT (L= 4 μm & W = 256 μm) due to radiation damage of 1.4 MeV protons; (a), (b) and (c) are meaured at $V_{DS}$ = 20 V, $V_G$ = 17.5 V and (d) is meaured at $V_{DS}$ = 20 V, $V_G$ = 0 V.

Sensitivity of a-Si:H TFTs to radiation damage was investigated by observing the variation of device parameters such as threshold voltage, mobility, $K_f$, α, and off current, etc. as a function of exposure to 1.4 MeV protons from a Van de Graaff accelerator. Except for off-current, the relative change of the values of these parameters were less than 10 % until the proton fluence exceeded $10^{14}$ /cm$^2$ as shown in Figure 7. Changes in $K_f$ and α, are even less. Similar measurements for poly-Si TFT are underway

## V. DESIGN OF A-Si:H AND POLY-Si TFT AMPLIFIERS

Since the signal from a MIP is small, a low noise amplifier is necessary before the signal is read out. Figure 8-(a) shows a conceptual block diagram of the proposed amplifier and read-out scheme. It consists of a charge sensitive preamplifier with a reset switch, linear amplifier stage, an addressing switch(x-bus) and a source follower output stage(y-bus). Figure 8-(b) shows a schematic circuit diagram of the proposed two-stage amplifier and read-out circuit made of resistors and a-Si:H TFTs or poly-NMOS TFTs. The first stage consists of a front-end TFT, $Q_1$, a load resistor, $R_L$, a cascode TFT, $Q_2$ and its bias circuit. Figure 8-(c) is a poly-CMOS amplifier with an active load which will give higher open loop gain at the same power dissipation than a passive load. Poly-Si PMOS TFT is used as the front end TFT because of its lower noise characteristics. The reset switch can be replaced with a high value resistor in the case of low event rate application. The linear gain of the second amplifier stage should be decided by considering the proximity and input impedence of the external circuitry. Here the second stage gain is arbitrarily chosen to be 10.

Optimum design of a charge sensitive amplifier requires the following; (a) small detector capacitance, (b) uniform and reliable feedback capacitance, (c) high value of open loop voltage gain, (d) wide bandwidth, (e) low power dissipation, and (f) high signal to noise ratio. Following are summaries of the state of art consideration on these subjects.

(a) Generally the input signal is

$$V_{in} = \frac{Q_{col}}{C_D} \qquad (5)$$

where $Q_{col}$ is the total collected charge and $C_D$ is the detector capacitance. In order to obtain a larger input signal, a lower detector capacitance is necessary. For example, a 50 μm thick 300 x 300 μm$^2$ pixel detector can have $C_D$ = 0.05 pF by using an interdigitated electrode configuration covering 25 % of the pixel area.

(b) The feedback capacitance can be implemented with or without cascode configuration. The benefit from using cascode is to make a small value of feedback capacitance with high reliability. The disadvantage is the complexity of fabrication and increase of power dissipation. In the proposed system the value of $C_f$ is 2 fF made by a thin insulator layer between two 3 x 3 μm$^2$ parallel electrodes. Amplifiers without cascode stage may use the gate-to-drain overlaping capacitance as a feedback capacitance and its value can be made less than 10 fF

by overlapping of 0.5 μm or less. Experiences of underlapping for Xerox high voltage TFT and 2-D simulation program[20] would give guide lines for the design and fabrication process in this case.

(c) Due to the low mobility of electrons in a-Si:H, the transconductance of a typical size of a-Si:H TFT is of the order of 1- 5 μA/V so it requires a high value of load resistance to give high gain and is constrainted by the power dissipation and pulse rise time. However poly-Si TFT due to their higher transconductances can achieve high gain and a fast RC rise time. The open loop voltage gain of the first stage is approximately

$$A_v = g_m \times R_L \tag{6}$$

where $g_m$ is the transconductance.

$$g_m = \left( 2 \mu_{fe} C_i \times \left(\frac{W}{L}\right) \times I_d \right)^{0.5} \tag{7}$$

and $R_L$ is the load resitance. In CMOS amplifier, $R_L$ represents the parallel sum of channel transconductances of $Q_1$ and $Q_3$. The closed loop gain of the first stage, $A_1$, is

$$A_1 = \frac{C_D}{C_f + (C_D + C_{in} + C_f)/A_v} \tag{8}$$

where $C_{in}$ is the input capacitance of the front end TFT, $Q_1$. If $A_v$ is large enough then $A_1$ would simply reduce to $C_D/C_f$ which is the gain of an ideal charge sensitive amplifiers. The final output voltage peak is

$$V_o = V_{in} \times A_1 \times A_2 \tag{9}$$

(d) The bandwidth of -3dB is

$$\omega_{-3dB} = \frac{1}{R_L \times C_L} \tag{10}$$

where $C_L$ is the total capacitance at this node which consists mainly of the input capacitance of the next stage and the stray capacitance through metal connections and load resistor. The stray capacitance effect is not considered in the calculation. The maximum gain-bandwidth product, $A_v\omega_{-3dB}$, is simply $g_m/C_L$ and the amplifier response time, $\tau_{RC}$, is a product of $R_L$ and $C_L$. This response time should be an order of magnitude smaller than the shaping time.

(e) For a 300 x 300 μm$^2$ pixel size, there are about 10 million pixels per m$^2$, so the reduction of power dissipation is a very important issue. The dominant power dissipation occurs in the first stage,

$$P = V_{dd} \times (I_1 + I_2 + \cdots) \approx 2 \times V_{dd} \times I_1 \tag{11}$$

where $V_{dd}$ is the amplifier bias and $I_i$ is the current flowing along loop i.

(f) For the proposed system, there are three main noise sources ; (1) Step noise : Shot noise from the detector leakage current given in Section III, (2) Delta noise : Thermal (Nyquist) noise from the channel resistance of the front end TFT, and (3) Flicker noise : 1/f noise from the TFT. Equations for (2) and (3) are given in Section IV. If these noise sources are not correlated, then net equivalent noise charge (rms in electrons) at the input in the case of a CR-RC shaper with shaping time, τ, is obtained by a convolution of the noise spectrum and the transfer function of the CR-RC shaper[21].

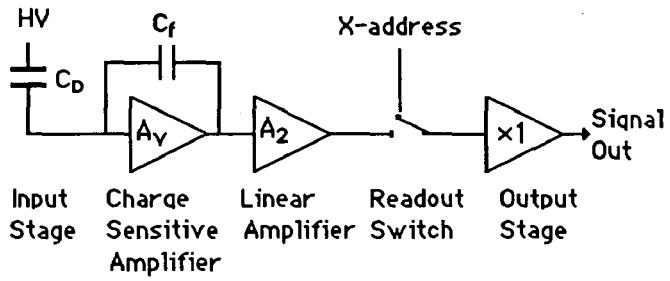
$$N^2 = N_S^2 + N_\Delta^2 + N_F^2 \tag{12}$$

$$= \frac{e^2 I_{det}}{4q}\tau + \left(\frac{e(C_{det}+C_{in})}{q}\right)^2 \frac{kT}{3g_m\tau} + \left(\frac{e(C_{det}+C_{in})}{q}\right)^2 \frac{K_f}{2C_{in}} F(\alpha,\tau)$$

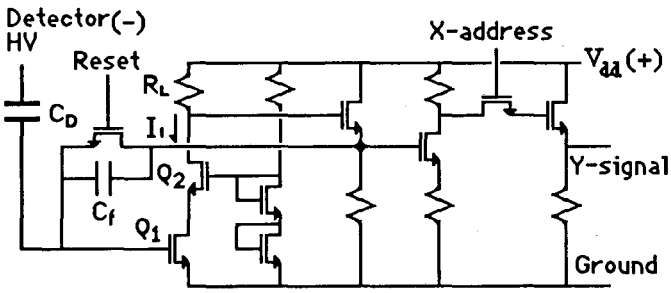
where $F(\alpha,\tau)$ is a correction function for $\alpha \neq 1$ in 1/f noise.

$$F(\alpha,\tau) = \frac{0.5\pi\times(\alpha-1)}{\sin(0.5\pi\times(\alpha-1))} \times (2\pi\tau)^{\alpha-1} \tag{13}$$

If $\alpha$ is 1 then F is 1. The dominant noise source is the 1/f noise of the front end TFT for the range of shaping time, $\tau$ = 0.2 - 20 μsec so in order to minimize the 1/f noise terms, the TFT size should be optimized to give the minimum 1/f noise, ie. $C_D = C_{in}$.




(a)

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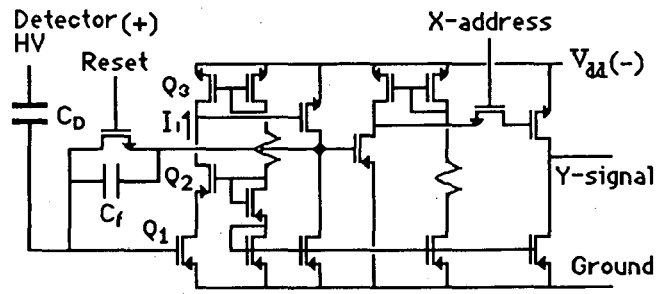


(c)

Fig. 8. (a) Schematic block diagram of pixel electronics (b) Circuit diagram of a a-Si:H TFT or a poly-NMOS amplifier and (c) Circuit diagram of a poly-CMOS amplifier

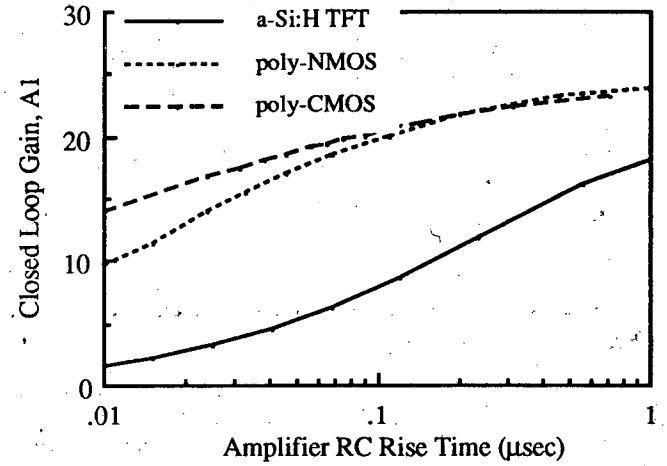


Fig. 9. Calculated closed loop gain ($A_1$) vs RC rise time of three amplifier configurations for a 50 μm thick 300 x 300 μm$^2$ pixel detector having $C_D$ = 0.05 pF

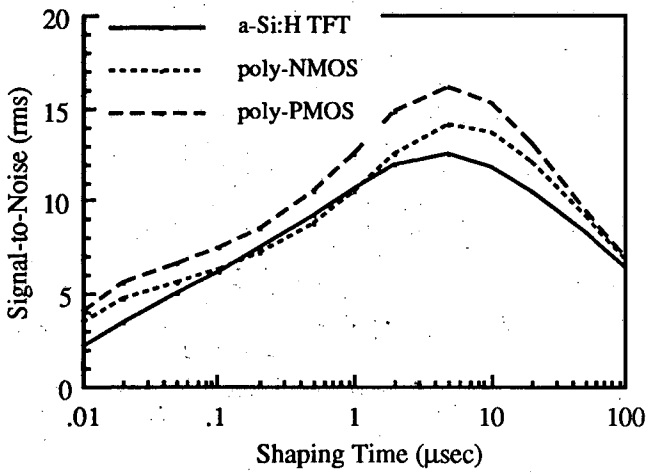


Fig. 10. Calculated signal to noise ratio of three amplifier configurations for a 50 μm thick 300 x 300 μm$^2$ pixel detector having $C_D$ = 0.05 pF as a function CR-RC shaping time

Table 4 Summary of estimated and calculated parameters of three amplifiers for a 50 μm thick pixel detector having $C_D$ = 0.05 pF

| Amplifier | $C_D$=$C_{in}$ (pF) | W/L [$Q_1$] | $V_{dd}$ (V) | $I_1$ (μA) | $g_m$ [μA/V] | $R_L$ (MΩ) | $\tau_{RC}$ (μsec) | $A_v$ | $A_1$ | $A_2$ | Noise (e) * / ** | S/N * / ** | $V_{out}$ (V) * / ** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| a-Si:H | 0.05 | 40/4 | 100 | 5 | 1.2 | 14 | 0.068 | 17 | 6.3 | 10 | 240 / 210 | 7.4 / 10.5 | 0.36/ 0.46 |
| poly-N | 0.05 | 53/4 | 50 | 10 | 11 | 4 | 0.015 | 43 | 11 | 10 | 250 / 210 | 7.2 / 10.5 | 0.63 / 0.78 |
| poly-C | 0.05 | 53/4 | 25 | 20 | 16 | 25 | 0.024 | 100 | 17 | 10 | 210 / 180 | 8.5 / 12.3 | 0.96 / 1.23 |

* Values are estimated at CR-RC shaping time, τ = 0.2 μsec.

** Values are estimated at CR-RC shaping time, τ = 1.0 μsec.

## VI. DISCUSSION

Based on a device with the values such as $C_D$ = 50 fF , $C_f$ = 2 fF, and constraining power dissipation to about 1 mW/pixel, we estimated the optimum circuit parameters for three cases of amplifiers ; a-Si:H TFT, poly-Si NMOS TFT and poly-Si CMOS TFT amplifiers with a poly-PMOS input stage. Among the design parameters two of the most important ones are (a) closed loop gain and (b) signal-to-noise ratio(S/N) of the first stage.

Figure 9 shows the closed loop gain, $A_1$, for the three proposed amplifiers as a function of the rise time, $\tau_{RC}$. Over the range of interest, a-Si:H TFT amplifiers have half the gain of poly-Si NMOS or CMOS TFT amplifiers. Figure 10 shows the signal-to-noise ratios (S/N) as a function of shaping time, τ. S/N values peak at about 5 μsec and drop at higher frequencies due to the rapid increase of shot noise from detector current and drops at lower frequencies due to increase of the thermal noise of the amplifier and loss of hole signal. A summary of estimated circuit parameters for these three amplifiers for a 50 μm thick 300 x 300 μm$^2$ pixel detector are shown in Table 4.

At present a-Si:H TFT technology is better developed. However the main limitations are low gain and low frequency response because of low field effect mobility. In the case of poly-Si NMOS or PMOS TFTs, noise at the input stage is not much better than with a-Si:H TFT although $K_f$ is smaller by an order of magnitude than that of a-Si:H TFTs because α is less than 1. This gives high noise in the frequency range of 1 ~ 5 MHz. However poly-Si TFT will give higher open loop gain which produces better stability for the charge-sensitive amplifier. Also the RC response time of poly-Si TFT amplifiers will be better than that of an a-Si:H TFT amplifier.

Among the various noise sources, the 1/f noise from the front end TFT is found to be the dominant one for the entire system. Its physical origin is considered to be the random trapping and detrapping of channel electrons at the interface traps between silicon and silicon nitride. One way to reduce the 1/f noise is to make use of advanced shaping techniques such as double correlated sampling[22]. Development of new gate insulators such as tantalium oxide may reduce 1/f noise as well as to increase the field effect mobility[23].

## VII. CONCLUSION

We have demonstrated the feasibility of building a-Si:H 2-D position sensitive pixel detectors by using a-Si:H thin film technology. The system would be very compact because it is composed of detector and amplifier circuit fabricated on the same substrate. For an amorphous silicon PIXEL particle detector, overall signal gain of more than 100 and response

time of less than 100 nsec can be achieved by a-Si:H TFT and poly-Si NMOS or CMOS technology. The estimated signal-to-noise ratio for both systems are about 10 in the range of shaping time of 0.2 ~ 1.0 μsec which would be adequate for our primary application of position detection of single MIP. Radiation damage measurement with up to $10^{14}$ $cm^{-2}$ fluence of 1.4 MeV protons on sample a-Si:H TFTs indicated that a-Si:H TFTs are highly radiation resistant.

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