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UNIVERSITY OF CALIFORNIA
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Soft Underlayers for Next Generation Magnetic Recording Media and Nano Electrostatic
Discharge Protection

A Dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy

in

Electrical Engineering

by

Chen Zhang

August 2013

Dissertation Committee:

Dr. Albert Wang, Chairperson
Dr. Sheldon Tan
Dr. Qi Zhu

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The Dissertation of Chen Zhang is approved:

Committee Chairperson

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ABSTRACT OF THE DISSERTATION

Soft Underlayers for Next Generation Magnetic Recording Media and Nano Electrostatic Discharge Protection

by

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Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, August 2013
Dr. Albert Wang, Chairperson

In this dissertation, two sections were included to present my work. The first section concerns about soft underlayers (SULs) in magnetic recording media, and the other section introduces electrostatic discharge (ESD) protection devices.

Hard disk drives (HDDs) are still being widely used in consumer electronics applications to store information. Due to the scaling down, higher capacity with smaller size HDDs are highly desired in market. Recently, perpendicular recording caused more attention to overcome some of the potential problems with longitudinal recording. The progress from the materials and techniques may make perpendicular recording more competitive. In this dissertation, a novel amorphous SUL CoFeTaZr is discussed for its superior magnetic properties.

ESD is one of the most important reliability problems for ultra-scaled integrated circuit (IC). Transient high voltage (up to tens of kilovolts) and current generated by ESD

in a very short time could introduce very high electric field and current across semiconductor devices, which may result in dielectric damage or melting of semiconductors and contacts, which may affect circuit performance, shorten product life time and increase manufacturing and assembling cost. Therefore, it's necessary to design a protection circuit that discharges the ESD. As the scaling down continues, ESD protection design is facing severe challenges.

This dissertation presented two novel ESD protection structures. One is a new nano crossbar array ESD protection device consists of the $\text{Si}_x\text{O}_y\text{N}_z$ composite, as dielectric layer between two metal electrodes. This device has extremely-low leakage current, fast response, good uniformity and robust ESD protection, ideal for mobile applications where power consumption is a great concern. The other one is a new non-volatile memory based ESD protection structure, two structures were introduced. One is with layers of nano crystal dots inside the floating gate film, the other one is with nitride floating gate layer in an MOSFET. Both structures has ultra-low leakage current, wide range of triggering voltage, ideal for multiple power domains.

In the last part, design and characterization of shallow trench isolation and poly-gated diode based ESD structures in a foundry 28 nm technology were reported. ESD-protected monitor circuits were used to evaluate chip-level ESD protection.

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Section 1 Soft Underlayers for Next Generation Magnetic Recording Media

Chapter 1.1 Introduction to Hard Disk Drives (HDDs)

Since the late 1950s IBM introduced random access method of accounting and control (RAMAC), hard disk drives (HDDs) have been used in computers. The first-generation HDDs were costly and bulky but advanced the random access feature for the main frame computers of that era. After improved over time, the HDDs entered the personal computer in the 1980s. Recently, HDDs are also being widely used in consumer electronics applications to store information, like iPods, video cameras, cell phones, game consoles etc. [1]. As the improvement of HDDs with larger capacity and smaller size over time, some analysts predict that more HDDs will be needed in the computers and consumer electronics market while the markets for other technologies such as flash memory and optical storage devices starts to grow.

Until recently, longitudinal recording technology is used to store information in the HDDs. In longitudinal recording technology, the magnetizations that lie longitudinally (parallel to the disk surface) are used for storing information. Alternative technologies such as perpendicular recording, in which magnetizations lie perpendicular to the disk surface, were proposed in the late 1970s to overcome some of the potential problems with longitudinal recording, especially the superparamagnetic limit faced by the longitudinal recording [2-4]. Efforts have been made to optimize the materials and introduce new techniques to produce better recording layers and soft underlayers (SULs) for the perpendicular recording media, which would provide comparable or superior performance

than the longitudinal recording media [5-9]. Significant improvements have also been made in the head design [10-11]. All these factors now make perpendicular recording more competitive.

1.1.1 Overview of Longitudinal Magnetic Recording

Paulsen invented magnetic recording a century ago, which relies on two basic principles: (i) Strong magnetic field at the poles which produced by the magnets can be used for reading information. (ii) The polarity of the magnets itself can be changed by applying external field, which provides the possibility of writing information. Therefore, a magnetic recording device would need to have the following key components: a recording medium to store information, a write head to produce localized magnetic fields which used for writing information, and a read sensor to convert the magnetic field from the media to electrical (voltage) signals for reading information. And there are many other components to position the head, to interpret the voltages into bits, and so on.

In the first few generations of HDDs, and in many tape storage devices, such as VCRs, a particulate medium (which is essentially a mixture of magnetic particles in a binder) was used [1]. The medium was primarily iron (III) oxide, however, this particulate medium cannot have a high saturation magnetization since the saturation magnetization of the magnetic material will be diluted by the binder. In the early days, a high saturation (or remanent) magnetization was required from the recording media, since the signal will be proportional to remanent moment and thickness of the media and the heads were not sensitive enough to detect weak signal. Another problem was that the

coercivity could not be tailored easily to meet the high-density requirements. Therefore, thin film media were considered as alternative in the HDDs, for their high saturation/remanent magnetization, high coercivity and also smooth surfaces. Therefore, particulate media were phased out from HDDs in the 1980s. In this section, some of the requirements of longitudinal recording media and the ways they were achieved are discussed.

1.1.1 Granular Media

Thin film media are usually deposited by DC or RF magnetron sputtering onto glass or aluminum substrate disks. Current recording media have several functional layers to achieve desired performance. However, it is the magnetic layer that stores the information. And the magnetic layer produced by sputtering is a polycrystalline material. Therefore the grains of the recording medium would have random orientations with respect to the film plane and the track direction as well. Moreover, they would also be arranged in random positions and sizes and may have a random easy axis orientation. Because of the randomness of the grains used in storing the information, a group of grains are used to store information. The group of grains which acts as a larger, single magnet, is called a “bit”. The bits are used to record binary code “0” and “1”. Information could be stored by aligning the net magnetization of the grains in a bit in one direction. Depends on the quality of the media, the read/write head and the overall technology of the hard disk drive, the group grain can vary from as few as 20 grains to several hundred. Older generations of HDDs will use more grains per bit than new generations. The borders of

these bits make up the “bit boundary”, which is one of several factors that determine the signal-to-noise ratio (SNR). Figure 1.1.1(a) is the TEM image of granular magnetic media. Figure 1.1.1(b) illustrates the randomness of easy-axis orientations and the bit boundary.

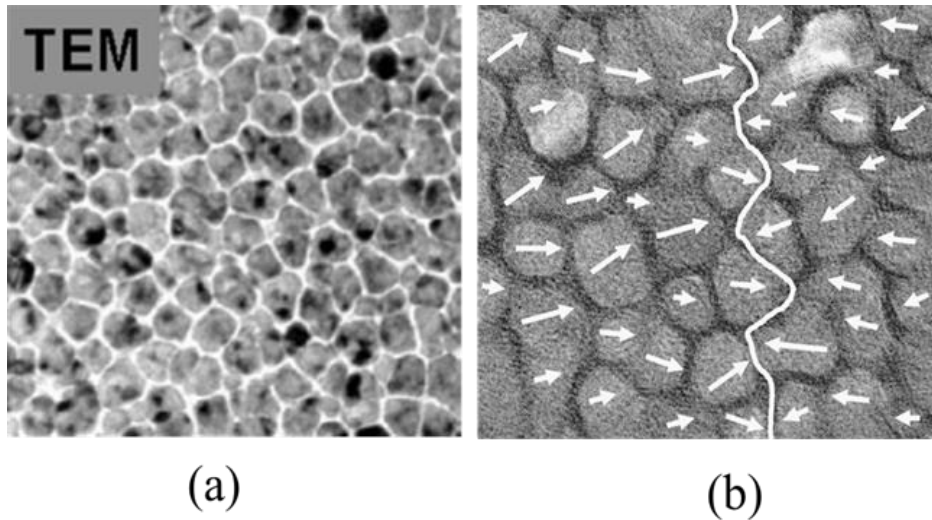


Figure 1.1.1 (a) TEM image of a granular medium. (b) Illustration of grains, the randomness of easy-axis orientations and the bit boundary.

The signal-to-noise ratio (SNR) is approximately given by the expression

$$\text{SNR} = 10 \log(N), \tag{1}$$

where N is the number of grains in a bit. To some extent, the SNR at a particular linear density is an indicator of how reliable the bits could be read out at that linear density. Therefore, SNR is a key indicator of the recording performance of a recording medium.

Equation (1) indicates that increasing the number of grains would help increase the SNR. Therefore, one way to increase the SNR of the recording medium is to reduce the

grain size and grain size distribution, which can increase the number of grains in the bit area. However, simply apply more grains in the bit area without reducing the grain size would also increase SNR while at the same time reduce the areal density of the recording medium. Grain size reduction can be achieved by the use of seedlayers and /or underlayers with small grain size or from the magnetic layer itself [12-22].

1.1.2 Orientation of Grains

According to Equation (1), which assumes the SNR is proportional to the number of grains because the randomness involved in the grain orientation and grain size. In the case of longitudinal media, the magnetization of the grains should lie parallel to the track direction. However, when the thin film media is sputter-deposited, the randomness of grain size and magnetization orientation occurs in order to minimize the energy of the film. One way to minimize the randomness is to improve the number of grains that have an easy axis along the film plane. Several underlayers such as Cr, CrTi, CrV, CrMo, or combinations of these have been used to improve the c-axis orientation parallel to the film plane [12][23-29]. It has also been reported that the use of intermediate layers helps to improve the easy axis orientation by improving the lattice matching between the Cr underlayers and the CoCrPt based magnetic layers [30]. In addition to using an underlayer and an intermediate layer to improve the in-plane easy-axis orientation, another way to minimize the randomness is to increase the number of grains that have an easy axis orientation parallel to the track direction. Figure 1.1.2 illustrates the magnetization orientation for different media configuration. A recording medium in which the magnetic

moments are randomly oriented with respect to the plane and the track [Figure 1.1.2 (a)] would have the lowest SNR. This is because, in such a recording medium, the component of magnetization that lies parallel to the disk surface or the track direction is low. This will lead to a reduction in the signal and an increase in the noise. The SNR can be increased by maximizing the number of grains that are oriented parallel to the disk surface [Figure 1.1.2 (b)]. This is typically achieved by the use of underlayers such as Cr, as discussed previously. Further increase of SNR can be obtained by aligning the magnetization of the grains along the track direction [Figure 1.1.2 (c)]. This could be achieved by the texturing process, which leads to an increased orientation ratio. Figure 1.1.2 (d) illustrates the ideal configuration for obtaining very high SNRs, though it is not possible to achieve such orientations experimentally.

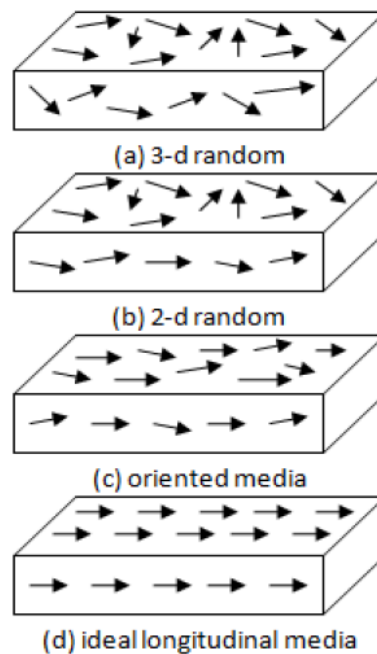


Figure 1.1.1.2 The randomness of easy axis orientation: (a) three-dimensional (3D) random, (b) two-dimensional (2D) random, (c) oriented media, and (d) ideal orientation.

1.1.3 Challenges of Longitudinal Magnetic Recording

From the recording media perspective, the improvement of the recording media is always focused on controlling exchange coupling between the grains. Even if the magnetic grains are very small, having high exchange coupling enlarges the magnetic domains of the media, which in turn increases the smallest possible bit size, which then reduces the areal density of the film. Some of the initial research work on the reduction of exchange coupling between the grains relied on the surface morphology of the underlayers. A rough surface was obtained by depositing very thick underlayers, which led to a physical separation between the magnetic layer grains [31], thus reduce the exchange coupling between the grains of the recording layer. However, thick underlayers also led to a larger grain size in the recording layer. Therefore, better methods were needed to separate the magnetic layer grains from each other. By compositional segregation at high temperatures, exchange decoupling could be obtained [24]. It is possible to sputter a recording medium that has two regions with different properties. The core of the grain would have magnetic properties and the grain boundary would have nonmagnetic properties. Thus, the nonmagnetic grain boundary would reduce the exchange coupling.

In magnetic recording, the energy barrier that prevents the magnetization of a particle from flipping is proportional to anisotropy energy $K_u V$, where K_u is the anisotropy constant of the material and V is the volume of the grain. It is this anisotropy

energy that helps to store the bit and make HDD a nonvolatile storage device. If the particle has to switch its magnetization from one direction to another, energy has to be supplied to overcome the energy barrier. An applied external field, which alters the energy barrier, is usually required to switch the direction of magnetization. In magnetic recording, this external field is applied using the write head, which is an electromagnet with nanometer scale gaps.

In the previous section, it was discussed that the mean grain size and the grain coupling in longitudinal recording media need to be reduced to increase the areal density. However, the reduction of these two parameters leads to a reduction in the grain volume and, therefore, a reduction in the energy barrier for magnetization reversal, since the K_u is intrinsic property of the material and fixed. When the anisotropy energy K_uV gets lower, the thermal energy ($k_B T$) starts to compete with the anisotropy energy and makes the magnetization thermally excited and reversed. This phenomenon, where the nano magnetic particles could flip their magnetization without any external field, is called superparamagnetism. Since a recording medium is composed of different size grains, some of the smaller grains would be more susceptible to thermal switching. And it has been reported that the data will be lost even if 5% of the magnetization reverses due to thermal excitations [32-33]. For a medium to be thermally stable, the above quantity K_uV should be substantially greater ($> \sim 40$) than the thermal energy $k_B T$, and this is also the scale limit of the grain [34]. The HDD industry was no longer able to increase the areal density by simply scaling down, new methods and technologies should be considered.

The superparamagnetic limit is the physical limit of longitudinal recording technology that enhanced the current interest in perpendicular recording. However, the bottleneck for longitudinal recording technology is still based on the available write head materials to write information. It is still possible to make longitudinal recording media that can provide thermal stability at higher areal densities than the present densities. However, writing and reading information from such a medium remains a challenge.

1.1.2 Overview of Perpendicular Magnetic Recording

Demagnetizing fields are experienced in any ferromagnetic or ferrimagnetic system and are expressed as

$$H_d = -NM, \quad (2)$$

where N is the demagnetization tensor which depends on the shape and direction of the magnet and M is the magnetization vector. The rule of thumb is that the demagnetization field is stronger when the magnetic charges or the magnetic poles are nearer. In longitudinal recording, as the linear density increases, the distance between the magnetic charges or the magnetic poles decreases, as seen in Figure 1.1.3. Strong forces are experienced between neighbor tracks. This leads to an increased demagnetizing field.

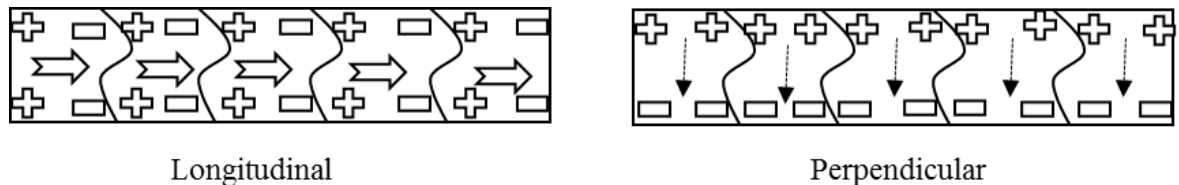


Figure 1.1.3 Illustration of magnetic charges and the associated demagnetizing fields for longitudinal and perpendicular recording.

However, in perpendicular recording technology, the demagnetization field would be reduced at high linear densities. Since they experience a much weaker force coming from the magnetic field of neighboring tracks.

Although several configurations for perpendicular recording have been proposed, the invention of double-layered perpendicular recording medium (CoCr recording layer and NiFe as SUL) and the single-pole head design are crucial for the superiority of perpendicular recording over longitudinal recording. Together, these inventions provide superior writing performance on perpendicular recording than is possible in longitudinal recording. Figure 1.1.4 illustrates the writing process in longitudinal and perpendicular recording. In longitudinal recording, if the fringing field from the head is higher than that of the coercivity of the grain, the magnetization will be reversed and writing will be achieved. In the recording medium, the grains have different energy barriers because of the distribution in the size and anisotropy constant. Therefore, in order to reverse all the grains at smaller time scales encountered in hard disk recording, the field from the head is made to be two to three times the coercivity of the material. In longitudinal recording, the maximum longitudinal recording field generated by a ring head (RH), the fringing field (H_f) is approximately $2\pi M_s$, where M_s is the saturation magnetization for the material [35]. For comparison, in perpendicular recording, the maximum recording field generated by a single pole head (SPH), the gap field (H_g) is $4\pi M_s$ [36-37]. Thus, in longitudinal recording, the weaker field is used to write the information. In perpendicular recording, the higher write field is achieved by the use of a soft underlayer and a single pole head, as illustrated in Figure 1.1.4 (b). Since SUL is highly permeable, it acts as a magnetic

mirror, which forms a closed loop for the magnetic flux of the pole head. It can be visualized that in perpendicular recording the media is virtually placed in the gaps of the poles and hence under higher writing fields. The direct consequence of higher writing field is the ability to write onto a higher anisotropy medium (higher K_u). The use of higher anisotropy media materials allows higher areal densities without compromising thermal stability of the recording data.

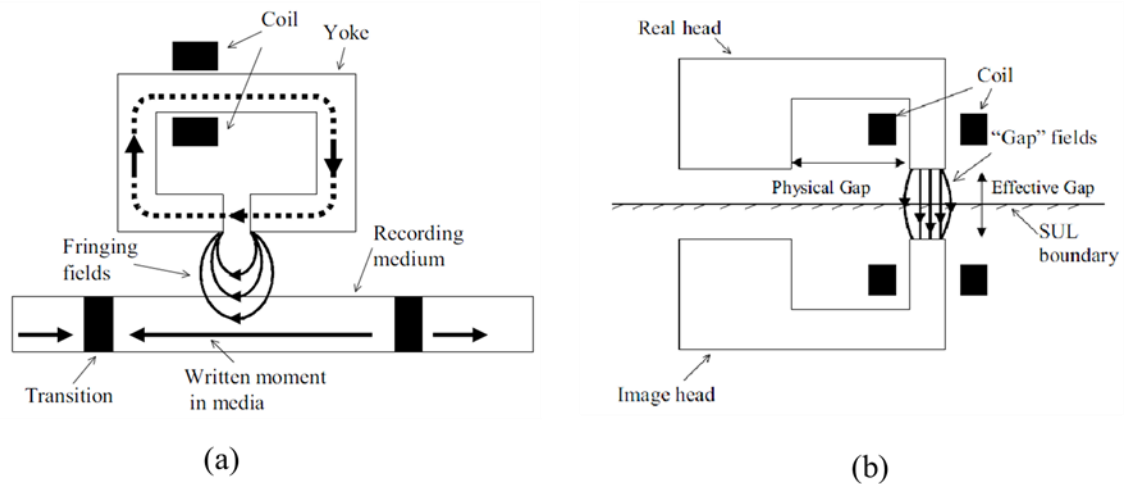


Figure 1.1.4 Writing process in (a) longitudinal and (b) perpendicular recording. In perpendicular recording technology, the medium is virtually placed in the pole gaps between the head and the mirror image in SUL.

In spite of several advantages that the perpendicular recording had over the longitudinal recording technology, the perpendicular was not given a serious thought until lately. The areal density demonstrations on perpendicular recording media were lagging behind that of longitudinal recording. One reason was that a smaller grain size could be achieved in longitudinal recording than the possible grain size in perpendicular recording. Also, in the early 2000s, in order to obtain the desired grain boundary segregation, higher

compositions of Cr was studied in perpendicular recording. However, the presence of more Cr also led to a reduction in the anisotropy constant of the grains. In such case, some grains may be more sensitive to thermally assisted switching and become a source of dc noise. In addition, the soft underlayer issues were also not solved, which led to an inferior performance of perpendicular recording. Despite all these setbacks, perpendicular recording became the most likely candidate for the technology to be implemented in the next generation HDDs when an areal density of 340 Gbits/in.² was reported. For the past five years or so, significant progress were made in the perpendicular recording. The progress came from the recording layer and soft underlayers of the recording media, and also writing heads, made perpendicular recording technology more promising [5][9][38-41].

1.1.3 Description of Various Layers and Their Functions

Figure 1.1.5 shows various functional layers, such as the soft underlayer, recording layer, etc., of a typical double-layered perpendicular recording medium. In the practical designs, there may be more than one layer involved for every function. The most advanced or exploratory designs may have a totally different structure than described. However, for the sake of simplicity, only a simple design is shown to illustrate the function of each layer.

The recording medium may be coated on an AlMg alloy precoated with a NiP layer or a glass substrate of a dimension suitable for its particular application. For example, an outer diameter of 3.5 in. or more disk substrates could be used in server and desktop

HDDs. Outer diameter of 2.5 in. disk substrate can be used for laptops. HDDs with a diameter range of 1-2 inches are used for small electronic devices such as MP3 players, etc. Most of the layers in a hard disk medium are deposited by the sputtering process. Prior to the deposition of any layer, the substrates are cleaned to remove chemical and particle contaminants. Then, the substrate is first coated with an adhesion layer or an interface layer, made of Ta, Ti, or an alloy of these materials. This layer helps in improving the adhesion of SUL and all the other layers with the substrate. The next layer deposited is a soft magnetic underlayer. The soft magnetic underlayer helps in conducting the flux from the writing pole of the head to the trailing pole, as previously discussed. On top of the SUL, some intermediate layers may be deposited with or without seed layers. The intermediate layers aim at least two functions in the recording layer. One is to eliminate the exchange-coupling of the SUL and recording layer. If the SUL and the recording layers are coupled, the recording medium may show a larger noise during readback. Another function of the intermediate layer is to provide epitaxial growth conditions for the recording layer to obtain perpendicular orientation with respect to the film plane. Intermediate layers have also been served to decrease the grain size of the recording layer [42]. Usually, a seed layer is deposited below the intermediate layer to enhance a preferred growth. The recording layer is used to store information for long periods of time (about 10 years) and to produce the signal when reading back the information. The disk will then be coated with carbon overcoat layer and lubricants to prevent the corrosions of the recording layer. Typically, an amorphous carbon layer and a diamond-like carbon (DLC) layer are used. While both serve to prevent failures, the DLC

layer also helps in the bonding of the lubricant layer to the disk. The lubricant layer is used to ensure a uniform fly-height of the recording head and to prevent wear and tear on the head, which can cause the head to crash onto the disk.

Overcoat/ Lubricant ~ 4 nm
Recording Layer ~ 15 nm
Intermediate Layer ~ 20 nm
Soft Magnetic Underlayer (SUL) ~ 80 nm
Adhesion Layer ~ 10 nm
Substrate ~ few mm

Figure 1.1.5 Different functional layers of perpendicular recording medium with approximate thickness (layers are not to scale).

1.1.3.1 Soft Magnetic Underlayers

As discussed previously, the soft magnetic underlayer in the perpendicular recording media is helpful during the writing of information. It is the presence of a soft magnetic underlayer in the recording medium that provides a significant advantage for

perpendicular recording technology. Higher writing fields can be achieved with a soft magnetic underlayer and a single-pole head, thus, materials with high K_u can be used as the recording media. Therefore, smaller grains can be used to store information in the recording medium. With smaller and stable grains, higher linear density could be achieved. Thus, soft magnetic underlayer is a significant part of perpendicular recording technology. The fact that the longitudinal media did not require a soft magnetic underlayer created a handful of new challenges in perpendicular recording, which are described below.

During the fabrication of a recording medium, all the layers except the lubricant are deposited by a sputtering process. The disk substrate (glass or Al-alloy) will pass from one sputtering chamber to another and finally leave the deposition system. During this process, each layer will be sputtered in a sputtering chamber that is isolated from the rest of the chambers. This helps to avoid contamination. The number of disks that can be produced by a system in 1 h throughput depends on the time that each disk spends in a particular chamber. The deposition of thicker layers needs longer time to sputter, which would reduce the throughput. It has to be noted that the thickness of SUL alone could equal the total thickness of longitudinal media, thus, the manufacturing efficiency is reduced. Another manufacturing problem that would arise because of thicker SULs is that higher deposition rates would be needed, which are usually achieved at higher powers. However, sputtering at higher power would cause spitting of particles, which would deteriorate the surface of the disk and make it unsuitable for the flying heads in a hard disk drive. Therefore, thicker layers are not desirable in the production. In order to avoid

the above problems, thicker layers are usually deposited in two or three chambers to increase the throughput. This leads to an increase in the number of sputtering stations, which will lead to a significant investment. However, if the performance of perpendicular recording media is significantly higher, investment will out of the concern. This was one reason why the industry did not choose perpendicular recording technology for a long time, as the longitudinal recording media provided significant performance and cost advantages.

The fact that the SUL is too thick compared to the recording layer and is also made of materials with a larger magnetization than that of the recording layer also leads to the problem of noise from the SUL. As early as 1984, it has been reported that the presence of SUL, such as Permalloy, can increase the noise from the formation of domains [43]. Three different kinds of noises contributed by the SULs were reported: spike noise, medium noise, and low noise [44]. Spike noise arises due to the domain walls of the SUL. The medium noise, which arises because of the interaction between the SUL and the residual magnetization of the head, was weaker than the spike noise but larger than the low noise.

In the absence of a field, a soft underlayer may form domains, such as stripe domains or 180° domains, as these are ways to minimize the magnetostatic energy. However, the formation of such domain walls would also generate strong magnetic fields, which will cause strong noise during the reading process. A 180° domain wall with the magnetization along the track direction can be considered similar to a transition in longitudinal recording. In longitudinal recording, the signal produced by such a transition

will be proportional to its $M_r\delta$. Therefore, if a thick SUL forms a 180° domain wall, the signal produced will be very high. Figure 1.1.6 illustrates such a situation. Therefore, a 180° domain wall of such a SUL will produce a signal (rather, it should be called noise, since SUL is not supposed to produce any signal during the reading) much stronger than that of longitudinal or perpendicular recording media. Therefore, the noise from the soft underlayer is a serious concern. If the domain walls formed in the SUL are fixed in one position, it would be possible to mark that position of the hard disk drive as a bad sector and still use perpendicular recording. However, the domains that cause the spike noise may move from one place to another [46]. Therefore, domain walls are a serious concern. Figure 1.1.7 shows MFM images of stripe domains formed in Permalloy thin films. Stripe domain periodicity is increased due to increasing film thickness. Even though the stripe domains are not as severe as the 180° domains, stripe domains also cause noise during the reading.

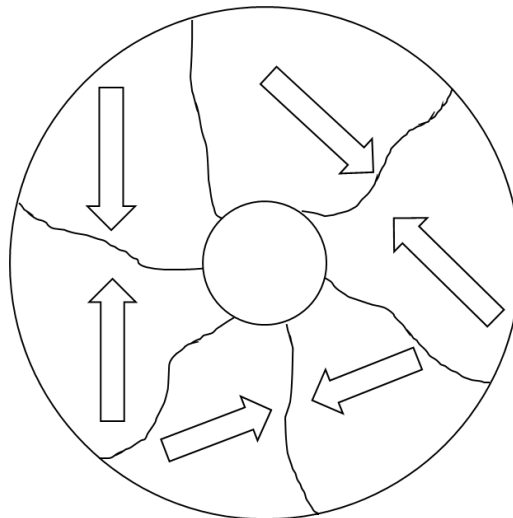


Figure 1.1.6. Illustration of 180° domain formation in SUL.

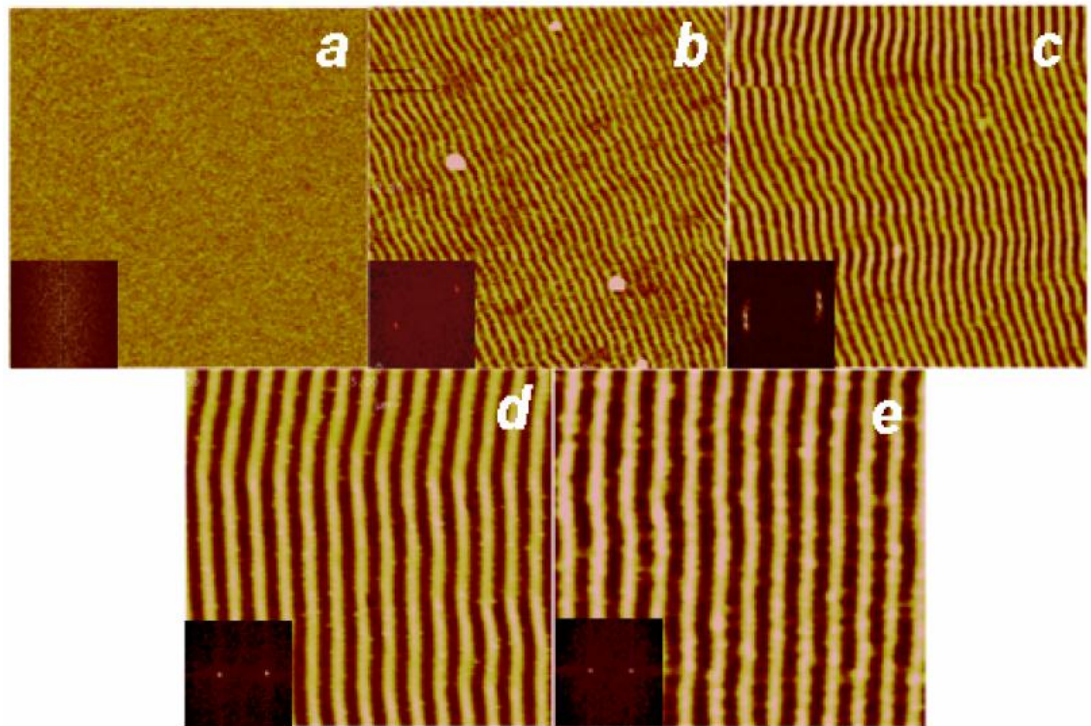


Figure 1.1.7 $5 \times 5 \mu\text{m}^2$ MFM images of Permalloy thin films representing the growth in stripe domain periodicity due to increasing film thickness: (a) lack of stripe domain structures, (b-e) increasing periodicity of stripe domains.

It has been reported that when the stripe domains were swept away by using external magnets (biasing) during the reading process, thus, no undesired stray field could be generated and the noise was much lower and the signal was higher. Figure 1.1.8 illustrates the spinstand-measured signal profiles along a track recorded into a perpendicular medium with and without external magnetic field.

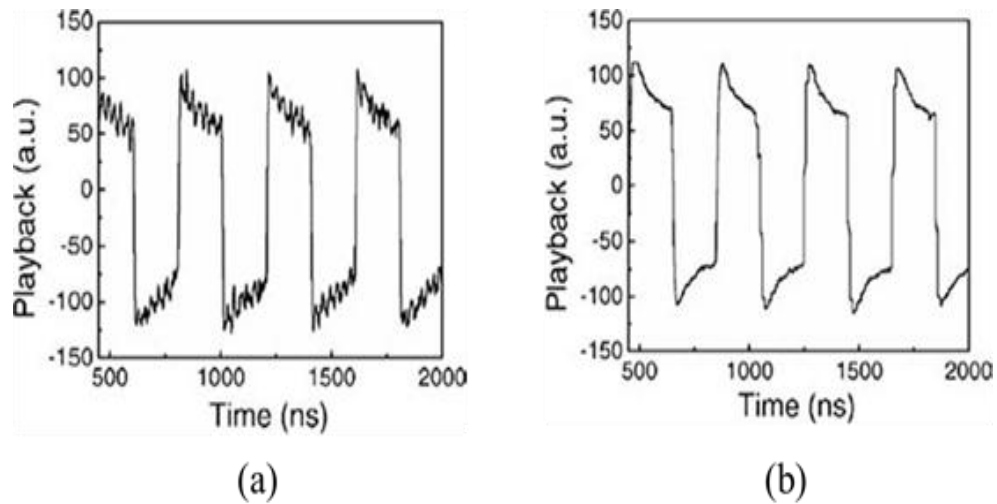


Figure 1.1.8 Spinstand-measured signal profiles along a track recorded into a perpendicular medium with (a) a non-biased SUL and (b) a biased SUL.

One approach is to use new materials that could probably show fewer domains and hence a lower spike noise. Another approach is to do laminations of SUL material to minimize the domain formation. A third approach is to combine new materials, laminations, and/or processes. However, an easier alternative to reduce the noise of soft magnetic underlayers is to use antiparallel coupled soft underlayers (APC SUL) through a thin Ru layer. In this case, two or more soft magnetic underlayers could be made to couple to each other antiferromagnetically during the reading, and theoretically the remanances of each layer should cancel each other, as in Figure 1.1.9. However, during the writing process, the Zeeman energy would overcome the antiferromagnetic coupling energy [47]. Therefore, the two layers are aligned in the same direction and would produce a high field during writing. Such an antiferromagnetic coupling has been reported to reduce the noise of the SUL.

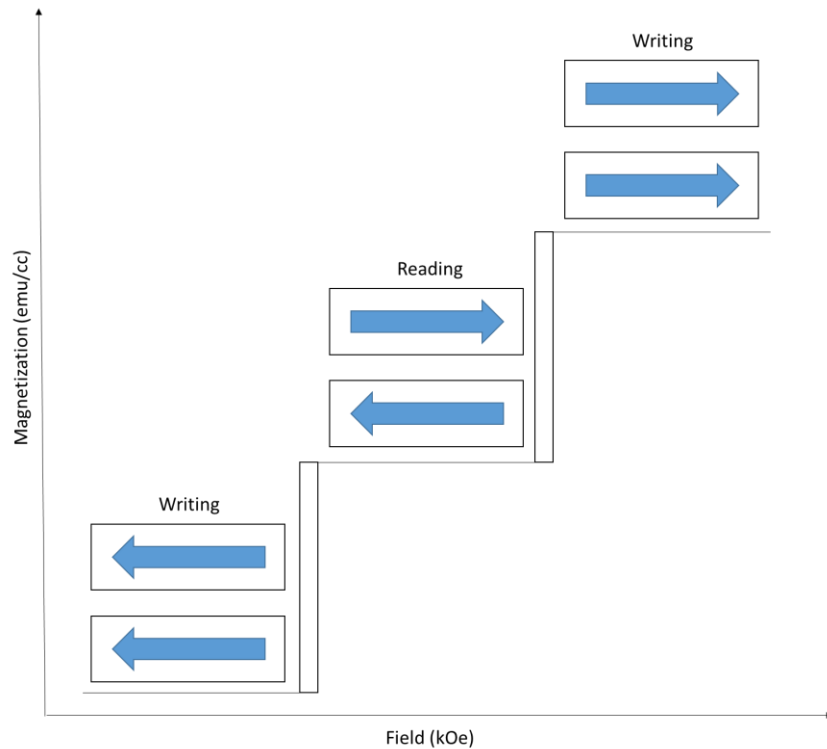


Figure 1.1.9 Magnetization of two layers of antiferromagnetically coupled SUL during the writing and reading (remanence).

Another problem with the use of a SUL is the difficulty in controlling its magnetic “softness.” Some experiments indicate that the “softness” of a SUL strongly depends on its thickness and the bit pattern in the recording layer above it. Figure 1.1.10 illustrates how MFM image may change depending on the “softness” of SUL. Permalloy was used as the SUL material. Figure 1.1.10 (a) and (b) images correspond to adequately “soft” and strongly biased (or “hard”) cases, respectively. The noticeable unidirectional orientation in Figure 1.1.10 (a) is due to the existence of an “easy axis” with an anisotropy field, H_k . Some effective “biasing” of SUL was predicted to take place in a thin layer of SUL close to the recording layer as the bit dimensions become smaller than the domain wall width

[48]. In the “hard” case, the SUL fails to screen off the demagnetized information in the recording layer or, in other words, loses its main purpose of being “soft.” These measurements indicate that there is some limiting or “dead” thickness value, below which the SUL could not further adequately function.

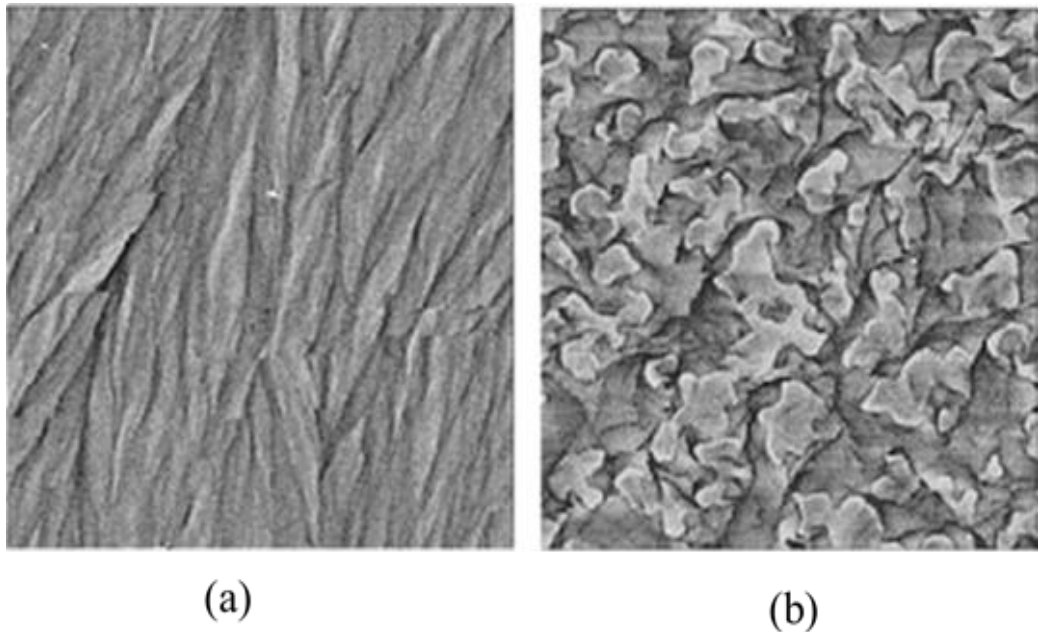


Figure 1.1.10 MFM images of a SUL corresponding to (a) the relatively “soft” and (b) strongly biased (“hard”) cases.

1.1.3.2 Intermediate Layers

When a magnetically soft underlayer and a hard layer are next to each other, their magnetic properties would change because of the exchange coupling interaction. Such an exchange interaction could reduce the coercivity of the recording layer and produce a larger noise during the readback. Thus, intermediate layers are inserted between the SUL and recording layer in perpendicular recording as an exchange breaking layer to reduce

the noise. Thus, the optimization of the intermediated layer thickness together with the noise of the SUL are crucial to perpendicular recording.

Another function of intermediate layers is to induce a perpendicular hcp (002) orientation for the Co-alloy-based recording layer. In Co-alloy-based perpendicular recording media, the easy axis (c axis of the hcp crystal) needs to be deposited with a perpendicular orientation with respect to the substrate. In the current design of perpendicular recording media, amorphous materials such as CoTaZr or FeCoB are considered as the SUL because they could provide a lower noise. Moreover, the amorphous SULs also exhibit a very low average roughness (closer to that of the substrate) of about 0.15 nm. When a Co alloy is deposited directly on top of the a -SUL, the hcp (002) texture would not easily developed. Therefore, it is essential to grow intermediate layers that would induce a hcp (002) orientation on the Co-alloy-based recording layer. Recently, intermediate layer has also been loaded with an additional role of producing the right morphology to control the segregation of grains in the recording layer.

1.1.3.3 Recording Layers

The material used for the recording layer of the perpendicular media has traditionally been a Co alloy. The CoCr alloy was the original media proposed in the late 1970s. Since then, modifications of Co alloys such as CoCrPt, CoCrTa, CoCrNb, CoCrPtNb, and CoCrPtB were used as the recording layer material [49-56]. One of the major problems of CoCr-alloy media materials was that the nucleation field (field required to switch 5% of

the magnetization) of the recording layer was seen in the first quadrant of the hysteresis loop [57]. This implies that at zero fields magnetization of several grains has already reversed. Such grains with reversed magnetization would exhibit a high dc noise. Figure 1.1.11 is an illustration to show the significance of nucleation field. The grains are magnetized into the plane of the paper with an applied field. When the field is removed, all the grains are expected to maintain the magnetization if they are thermally stable and their anisotropy energy is higher than that of the demagnetizing energy.

However, if the anisotropy constant of the media is not high, some grains (smaller ones) would reverse, as in Figure 1.1.11 (a). However, if the anisotropy is high enough, all the grains would maintain their magnetization in the applied field direction, as in Figure 1.1.11 (b). This could be seen as hysteresis loops with nucleation fields in the first quadrant and second quadrant for media with low K_u and high K_u , respectively (Figure 1.1.11 (c) and 1.1.11 (d)). Therefore, media with high anisotropy are needed to obtain a negative nucleation field. In the earlier days, it was difficult to obtain such media as Cr was used as an additive element to obtain the exchange decoupling. As a side effect, the presence of Cr led to media with lower anisotropy energy.

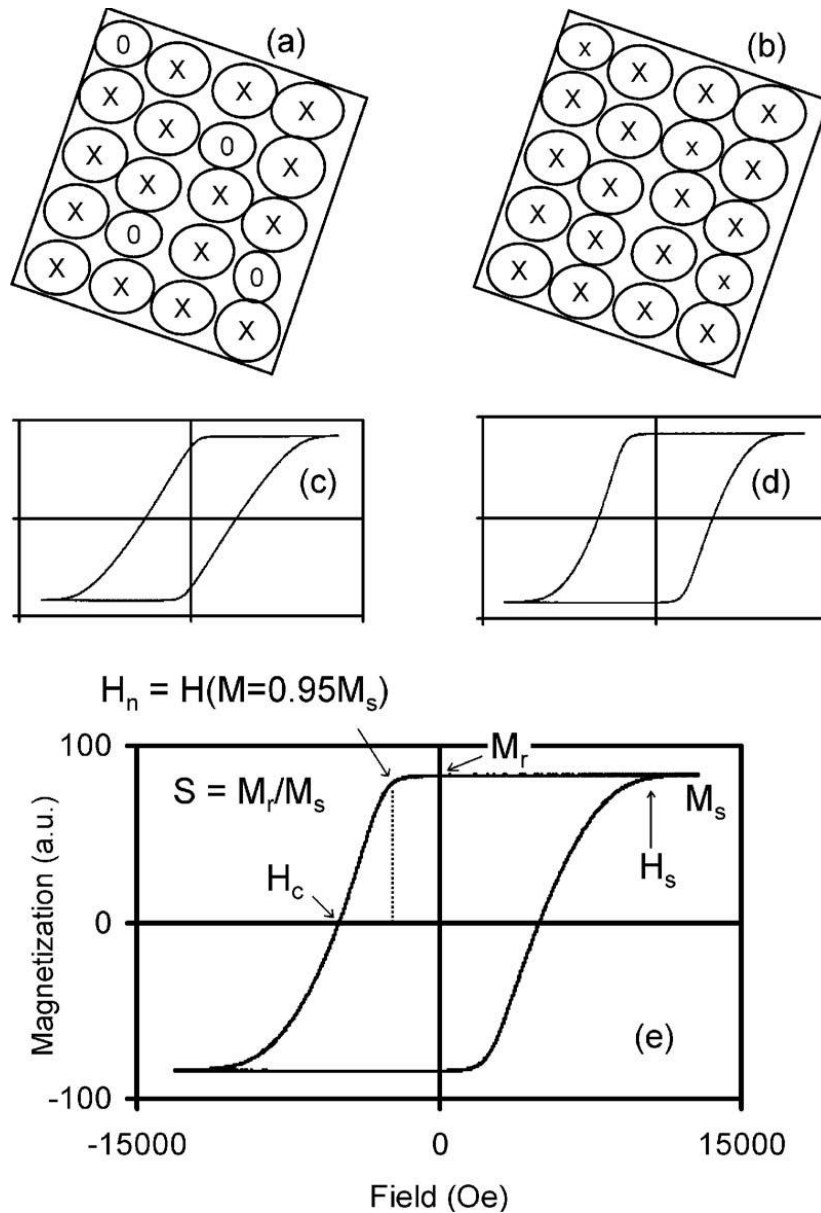


Figure 1.1.11 (Top) Illustration of remanence magnetization state of grains of perpendicular media after it was saturated with a field into the plane. (a) Grains with a lower anisotropy constant show a reversal with remanent magnetization out of the plane showing instability. (b) Grains with a higher anisotropy constant show stable magnetization. (Middle) Illustration of hysteresis loops of the respective media that show (c) a positive H_n and (d) a negative H_n (bottom) hysteresis loop with relevant parameters.

Recently, oxide-based CoCrPt materials have received attention of researchers. In these media, CoCrPt is sputtered together with an oxide such as Si-oxide or Cr-oxide. This oxide element can be present in the target or can be formed in the film during the reactive sputtering of target in an oxygen atmosphere [53][40-41][58-61]. As the oxide and Co do not mix well, Co alloy grain is surrounded by an oxide based grain boundary. In order to form this grain boundary the amount of Cr needed in the target material is not high. About 5–10 at. % of Cr is sufficient, as compared to 14–17 at. % of Cr needed in the CoCrPt media without oxides. Moreover, out of the 5–10 at. % of Cr available in the target, some of the Cr would oxidize and go to the grain boundary as well. As a result, the grain could have a low Cr in its core and a high anisotropy constant. Such grains would be thermally stable, and squareness close to one could be achieved. The oxide based grain boundary is also effective in reducing the grain size and in reducing the intergranular exchange interaction. Therefore, the noise can be reduced and sharper transitions are possible. Another advantage of oxide-based CoCrPt materials is that the manufacturing process will be more or less similar to that of longitudinal recording media. And, more importantly, small grain size, low noise, and good thermal stability could all be achieved with oxide-based media.

In order to continue the use of CoCrPt-oxide media, it will be necessary to identify suitable oxide materials as the recording layers or other methods that would form a narrow grain boundary but effectively decouple the grains. The new oxide materials should also help in achieving narrower grains and a narrower grain size distribution. The future media would also have a higher anisotropy constant to overcome the thermal

instability issues by reducing the Cr content or by increasing the Pt content. Reducing the grain size and distribution of the existing CoCrPt-oxide media using other methods is also possible.

Chapter 1.2 Magnetic Properties Optimization for Amorphous Soft Underlayers

1.2.1 Introduction

The study of amorphous soft magnetic thin films has been receiving great attention recently since they are a key component in modern magnetic recording technologies. Applications involving amorphous soft magnetic thin films include high frequency magnetic recording heads, soft magnetic underlayers (SULs) in perpendicular magnetic recording, soft magnetic underlayers and interlayers that could be potentially used in multilevel three-dimensional magnetic technologies [62-63]. Nowadays, double-layer perpendicular media are routinely used for high-density magnetic recording media; therefore, finding a soft magnetic underlayer with optimal properties is crucial [64]. In order to optimize the performance of the magnetic writing heads, SULs with low coercivity and large value of B_{st} (B_s is the saturation magnetic flux density, t is the thickness of the SUL) are required [65]. Adequately high magnetic anisotropy field (H_k) is also a necessary parameter of SULs to reduce the domain wall noise during the read back process [66].

In this paper, a study of amorphous CoTaZr and CoFeTaZr thin films for soft magnetic underlayers is presented. Iron (Fe) is added to the composition of CoTaZr to enhance both its magnetic and corrosion-resistance properties. Both type of SULs are

comparatively investigated. CoFeTaZr amorphous thin films are further analyzed due to their superior magnetic properties. Various sputtering conditions were used to fabricate CoFeTaZr amorphous thin films on glass, silicon and silicon oxide substrates. The importance of using pre-sputtering substrate Ar milling and the processing pressure dependence on the CoFeTaZr amorphous thin films are also studied. Furthermore, the effect of capping layers (Ta and Ru) and seed layers (Cu, Ta and Ru) on the magnetic properties of the CoFeTaZr amorphous thin films are examined.

1.2.2 Experiment

CoTaZr, CoFeTaZr, Ta and Cu layers were all deposited via DC-magnetron sputtering in an AJA 1600 system. The Ru layers were deposited via RF-magnetron sputtering to improve the control of the sputtering rate. All samples were sputtered at a common base pressure of $<2 \times 10^{-7}$ Torr. DC input power of 112.5 Watt for CoFeTaZr and CoTaZr SULs were used and the argon sputtering pressure was varied to achieve the desired sputtering rate. Ta capping layers and seedlayers were deposited under DC input power of 75 Watt and argon sputtering pressure of 10 mTorr with a sputtering rate of 0.831 Å/s. DC input power of 75 Watt, argon sputtering pressure of 5 mTorr, and a sputtering rate of 1.456 Å/s were used to fabricate the Cu seedlayers. Argon sputtering pressure of 5 mTorr was used for the Ru layers, with 60 Watt RF input power with a sputtering rate of 0.202 Å/s for the Ru capping layer and 22.5 Watt RF input power with a sputtering rate of 0.047 Å/s for the Ru seedlayer. Single crystal Si (100), silicon oxide and glass were used as the substrates for the thin films. The silicon oxide substrates were

made by growing a 200 nm oxide on the Si (100) substrates by chemical vapor deposition. Acetone and IPA were used to clean the substrates before loading them into the chamber of the sputtering system. Magnetic biasing was introduced in order to produce the easy-axis of magnetization.

The coercivity measurements were performed using Magneto Optical Kerr Effect (MOKE) microscopy with a field step of 0.1 Oe. Kerr rotation was used for easy-axis magnetization measurements and hard-axis magnetization measurements with Helmholtz coils.

The in-plane magnetic moment was measured using Vibrating Sample Magnetometry (VSM) system PPMS from Quantum Design, with the sensitivity of under 10^{-6} emu for the average measurement time of 1 s. All the measurements were carried out at room temperature with a field step of 15 Oe.

Sputtering rate and roughness characterization were carried out via AFM Dimension 3100 system in tapping mode. In order to calculate the sputtering rate, materials were deposited on photolithography-featured substrates. The photoresist was then lifted off to obtain the thickness and thus the sputtering rate of the materials. NSC 15/Si₃N₄/NoAl probes from MikroMasch were used for sputtering rate characterization and FMR probes from Nano world were used for roughness measurements.

1.2.3 Results and Discussions

1.2.3.1 The Role of Ar Ion Milling on Substrate

Amorphous CoTaZr and CoFeTaZr thin films were first prepared by sputtering under 5 mTorr Argon sputtering pressure and 112.5 Watt DC input power on glass, silicon and silicon oxide substrates. Films were prepared with and without the Ar pre-sputtering milling before sputtering in order to examine its effects both on the CoTaZr and CoFeTaZr thin films. It was observed that samples with the Ar pre-sputtering milling showed superior magnetic properties, as shown in Figure 1.2.1. Roughness measurements were also carried out on the glass, silicon and silicon oxide substrates with and without Ar pre-sputtering milling, but did not show any significant difference, the roughness are all between 0.2-0.3 nm. Ar pre-sputtering milling helps to remove particles and contaminants on the substrate surfaces before sputtering, thus, making the surface of the substrates much cleaner and smoother for film growth. Since Ar milling produced improved results, Ar milling was used before sputtering for all samples in this study.

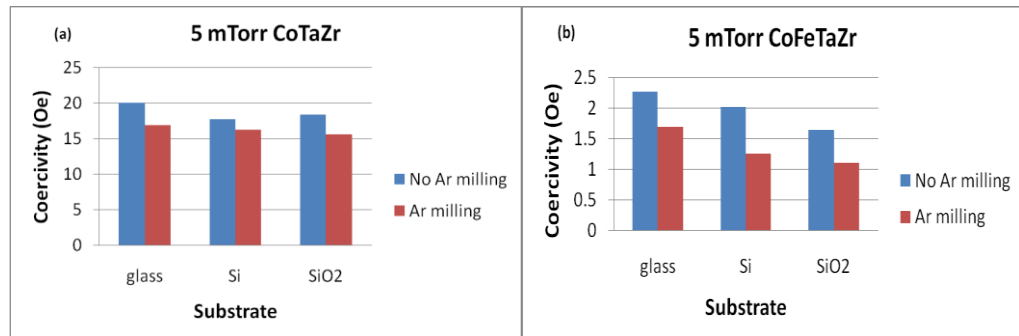


Figure 1.2.1 Ar ion milling effect on the magnetic properties of amorphous (a) CoTaZr and (b) CoFeTaZr thin films sputtered at 5 mTorr Ar processing pressure.

1.2.3.2 Comparison Between CoTaZr and CoFeTaZr Amorphous Thin Films

Recently, CoTaZr amorphous thin films have been intensively studied because of their importance as an SUL for perpendicular recording [67]. Considering the characteristics of SULs, CoTaZr amorphous thin film exhibits the best overall characteristics, like corrosion, thermal stability and abrasion resistance [68]. In this paper, the magnetic properties of CoTaZr and CoFeTaZr amorphous SULs were compared. They were all fabricated under the same sputtering conditions and thicknesses with Ar sputtering pressure of 5 mTorr and DC input power of 112.5 Watt. A comparison of the magnetic moment and coercivity of the CoFeTaZr and CoTaZr films on different substrates are shown in Figure 1.2.2, 1.2.3. The in-plane magnetic moment of CoFeTaZr and CoTaZr films are almost the same, and the magnetization of these two films are around 1150 emu/cm^3 . In perpendicular magnetic recording (PMR) media SUL is commonly used for providing the closed flux loop and thus increases recording field by approximately a factor of two from the write head due to the mirror effect [69]. However, due to magnetic domain walls in the SUL, SUL also increases the magnetic noise during the read back process. Hence, large uniaxial or unidirectional magnetic anisotropy field (H_k) is essential for SUL to reduce domain wall noise and exhibits improved field gradient and writing performance simultaneously [66]. In this study, the uniaxial or unidirectional magnetic anisotropy field (H_k) of CoTaZr and CoFeTaZr thin film is around 60 Oe. The CoFeTaZr films produced over 10 times lower coercivity than the CoTaZr films. The in-plane hysteresis loops of the hard-axis magnetization direction on

different substrates are presented in Figure 1.2.4. Adding Fe in the composition helps to reduce the coercivity while maintain the same magnetization.

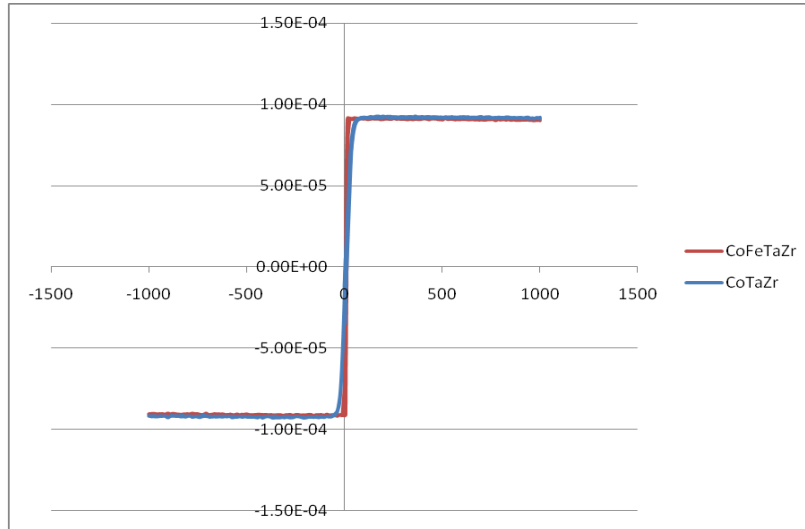


Figure 1.2.2 Magnetic moment comparison between CoTaZr and CoFeTaZr amorphous soft magnetic underlayers.

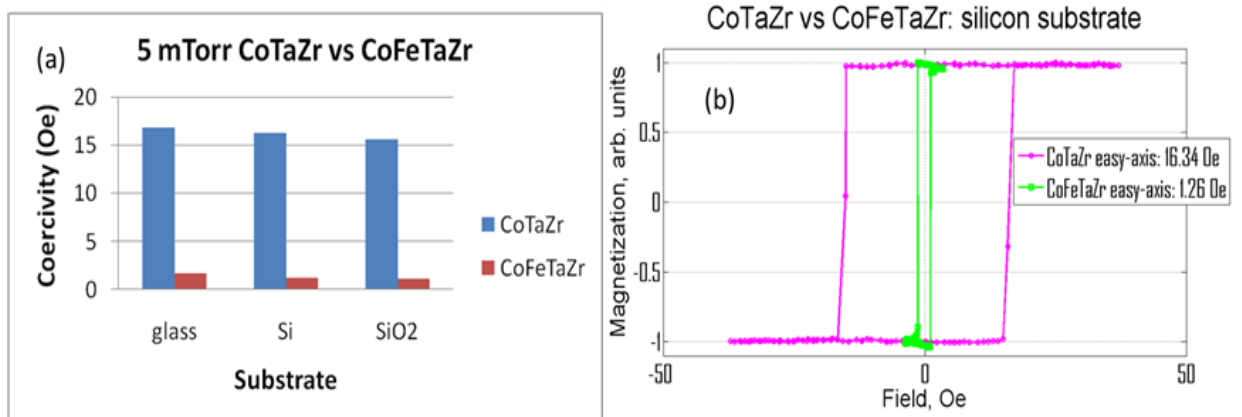


Figure 1.2.3 (a) Coercivity comparison between CoTaZr and CoFeTaZr amorphous soft magnetic underlayers fabricated under same sputtering conditions with 5 mTorr Ar sputtering pressure. (b) In-plane hysteresis loops of the hard-axis magnetization direction on silicon substrates.

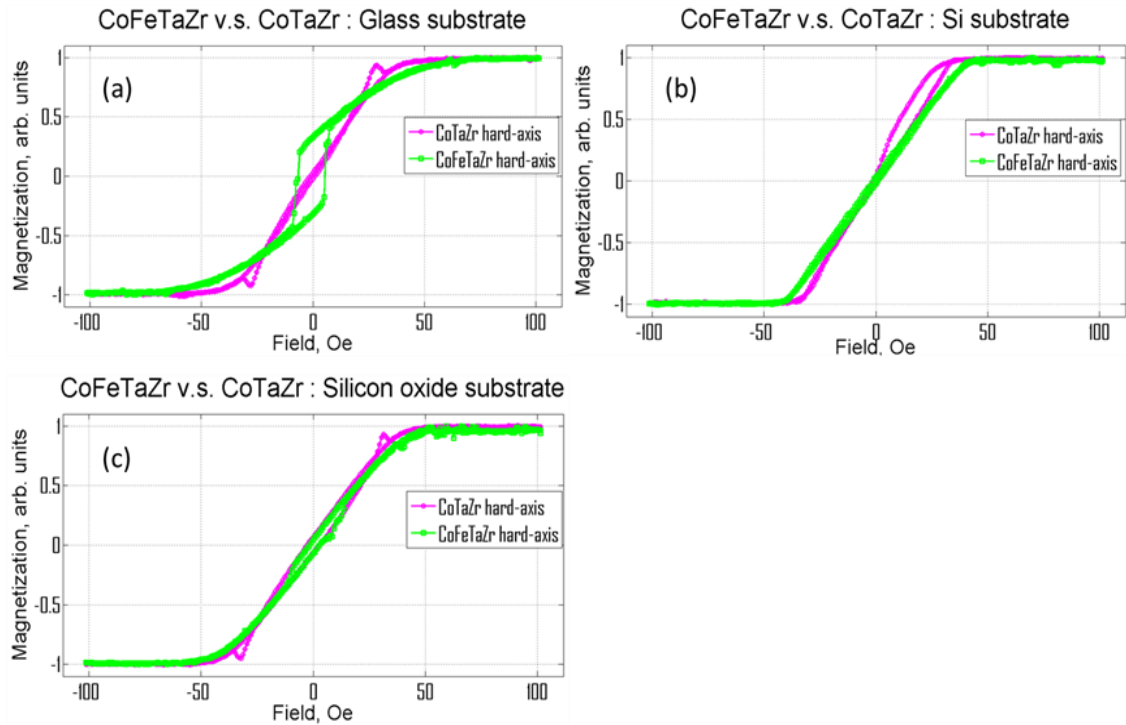


Figure 1.2.4 In-plane hysteresis loops of the hard-axis magnetization direction on (a) glass substrates, (b) silicon substrates, and (c) silicon oxide substrates.

1.2.3.3 Pressure Dependence of CoFeTaZr Amorphous Thin Film

The Ar sputtering pressure of the CoFeTaZr films was varied from 2 to 10 mTorr. Higher sputter pressure resulted in higher coercivity, as seen in Figure 1.2.5. This is due to the samples sputtered at higher pressure having higher roughness [67]. Lower Ar sputtering pressure also resulted in a higher sputtering rate, as seen in Figure 1.2.6. And thus, higher sputtering rate resulted in lower coercivity, as seen in Figure 1.2.7. Since a lower sputtering rate is easier to control the thin film growth, 5 mTorr processing Ar pressure was chosen over 2 mTorr processing Ar pressure for future experiments.

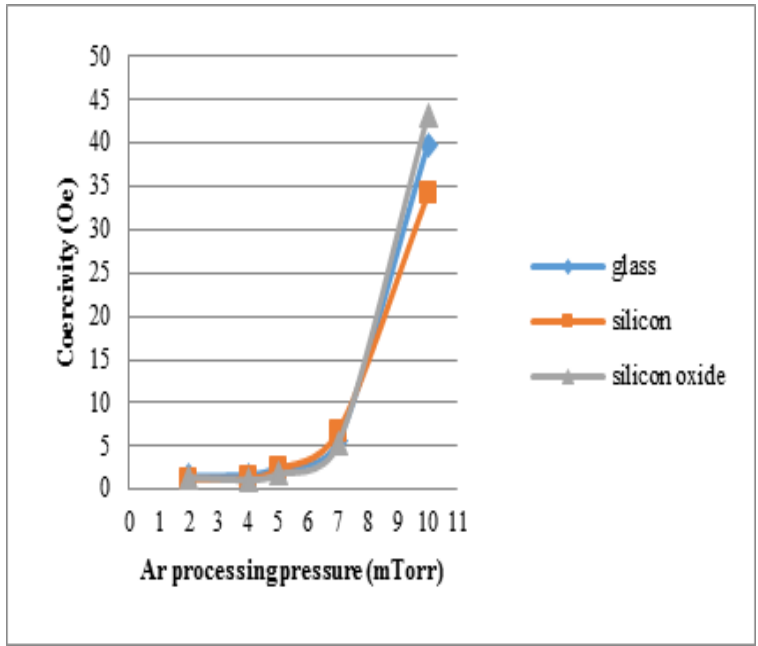


Figure 1.2.5 CoFeTaZr amorphous thin film coercivity dependence vs. processing Ar pressure sputtered on various substrates.

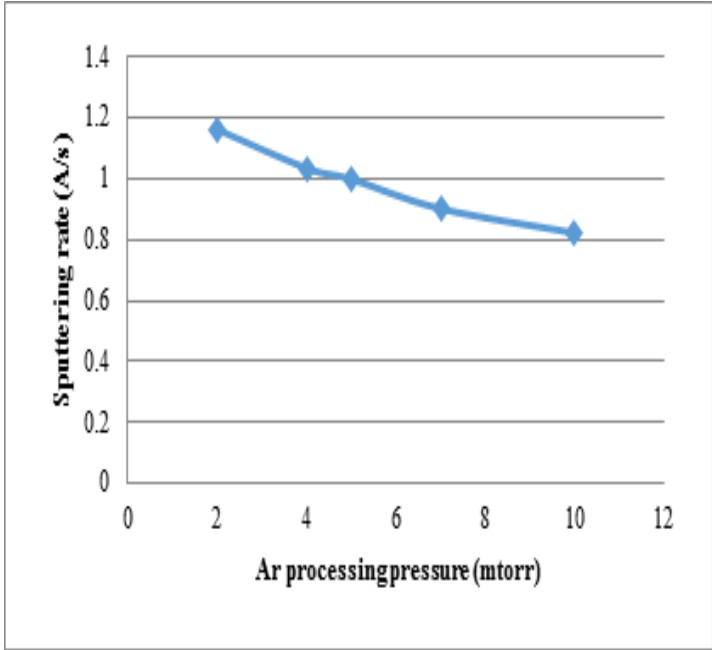


Figure 1.2.6 Sputtering rate vs. processing Ar pressure.

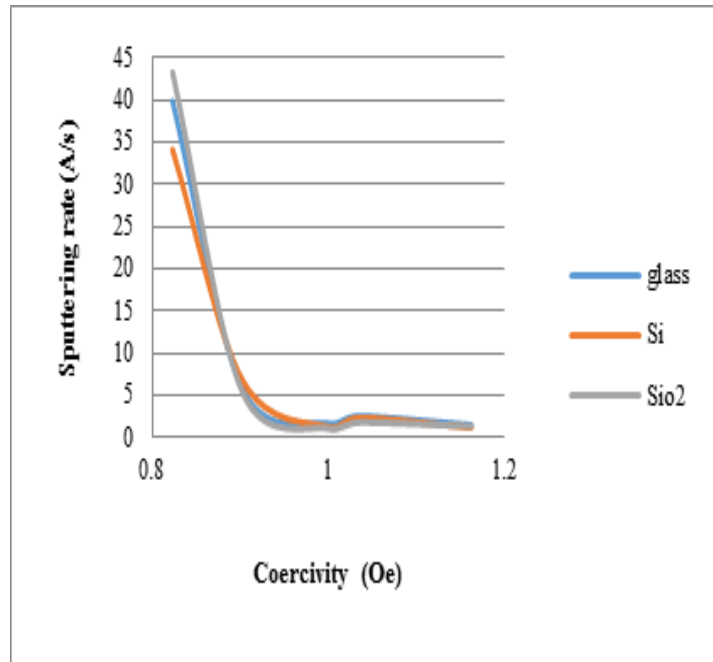


Figure 1.2.7 Sputtering rate vs. coercivity dependence.

1.2.3.4 Thickness Dependence of CoFeTaZr Amorphous Thin Film

SULs are used for conducting flux from the recording head for double-layer perpendicular recording. The pole dimensions, the write pole moment and the moment of SUL will affect the thickness of CoFeTaZr SUL which can vary from 10 to hundreds of nanometers. However in this range, magnetic domains are observed [5][53][70-72]. Media noise will increase under a certain critical thickness due to these magnetic domains [8].

CoFeTaZr amorphous thin films were prepared under the same sputtering conditions (Ar sputtering pressure 5 mTorr, DC input power of 112.5 Watt) with varying thicknesses to measure the thickness effect on coercivity. The coercivity of the CoFeTaZr SULs

decreased as the thickness increased, as seen in Figure 1.2.8. However, there was a sudden increase between 50 nm and 100 nm. The coercivity then decreased as the thickness increased from 100 nm to 400 nm.

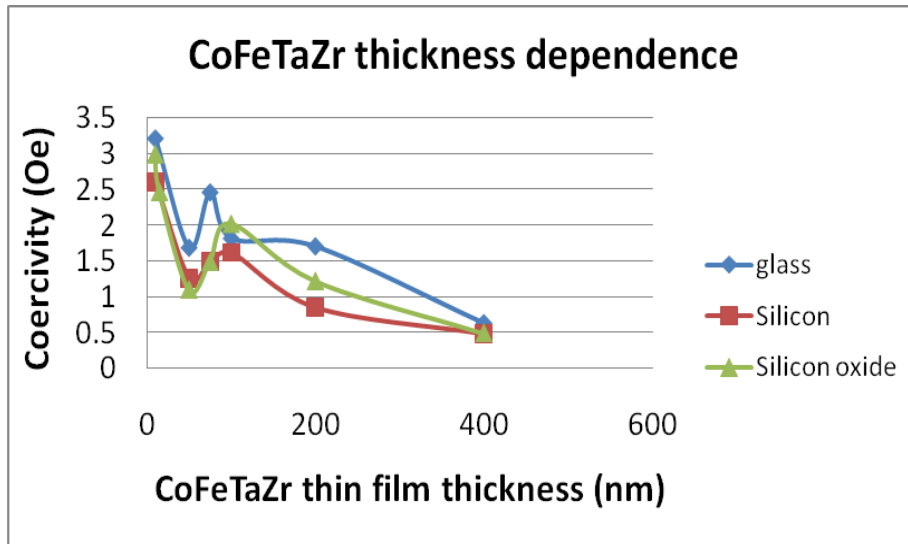


Figure 1.2.8 Coercivity vs. thickness dependence of CoFeTaZr amorphous thin films sputtered on different substrates.

1.2.3.5 Capping Layer Dependence of CoFeTaZr Amorphous Thin Films

Capping layers are used to protect the SULs from oxidation but can also affect the magnetic properties of the SULs. CoFeTaZr samples with a 5 nm Ru capping layer, a 5 nm Ta capping layer and no capping layer were prepared to study the effects of the capping layer on the magnetic properties of the SULs. Samples without a capping layer showed lower coercivity, as seen in Figure 1.2.9. The Ta capping layer produced lower coercivity compared with the Ru capping layer. The increase in coercivity due to the capping layers may be caused by the capping layers inducing a perpendicular (out-of-

plane) component in the SULs [66]. The in-plane hysteresis loops of easy-axis magnetization and hard-axis magnetization on different substrates are also presented in Figure 1.2.10-1.2.12.

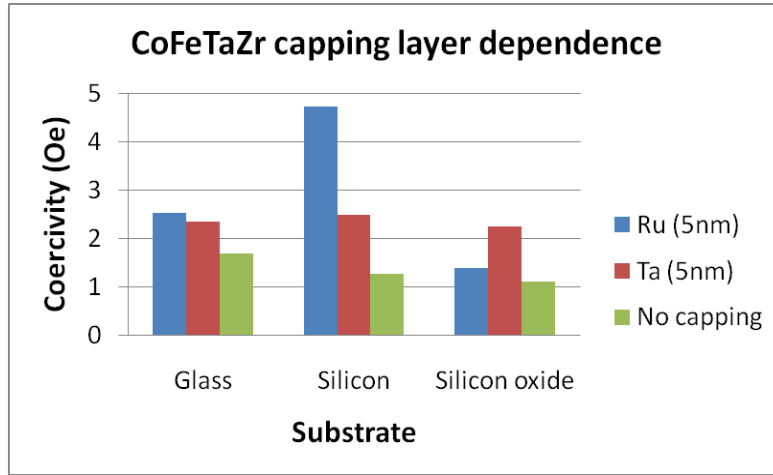


Figure 1.2.9 Coercivity vs. capping layer dependence of CoFeTaZr amorphous thin films deposited on different substrates.

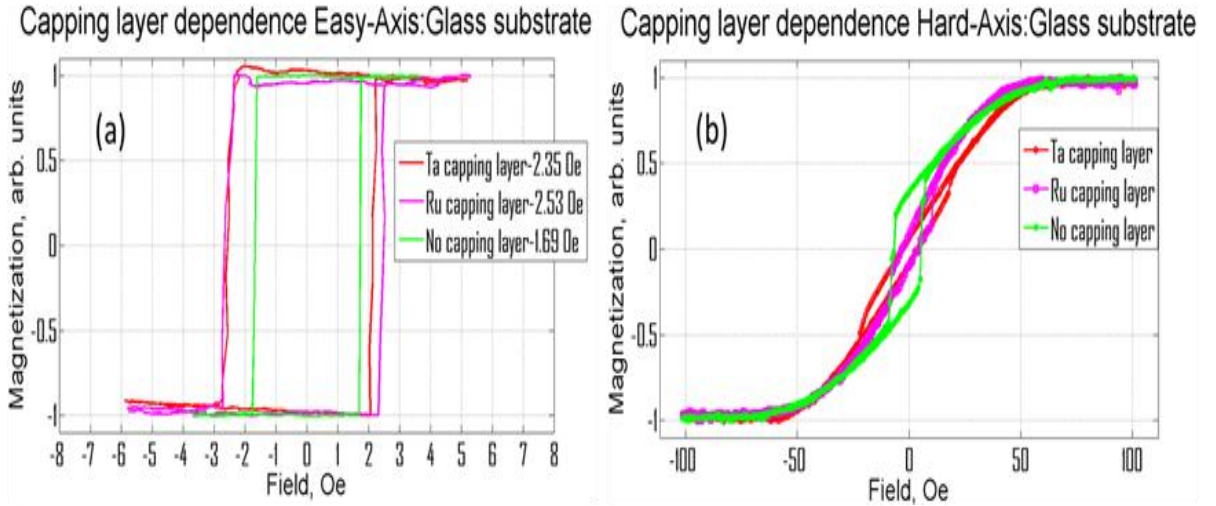


Figure 1.2.10 Hysteresis loops of capping layer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr amorphous thin films deposited on glass substrates.

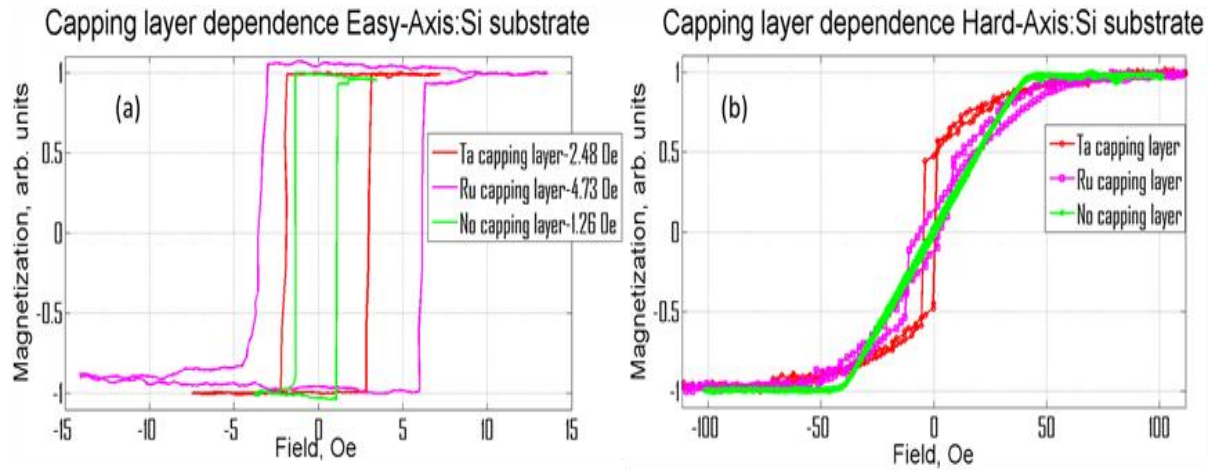


Figure 1.2.11 Hysteresis loops of capping layer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr amorphous thin films deposited on silicon substrates.

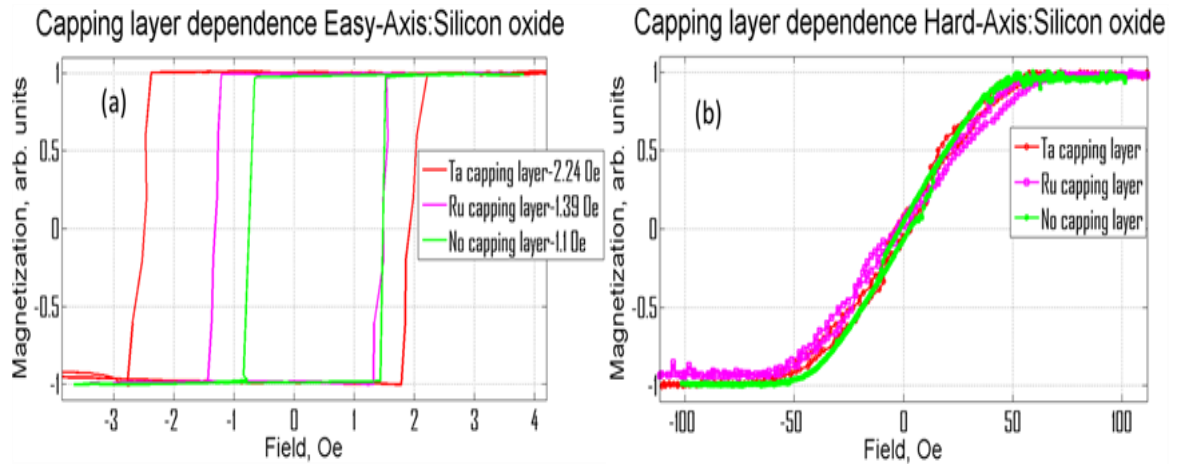


Figure 1.2.12 Hysteresis loops of capping layer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr amorphous thin films deposited on silicon oxide substrates.

1.2.3.6 Seed Layer Dependence of CoFeTaZr Amorphous Thin Films

Seed layers can help induce the amorphous structure of the CoFeTaZr thin films and with adhesion to the substrates and also resulting in a smoother surface for SULs to grow

[73]. In order to examine the effects of the seedlayer, four samples were prepared: 5 nm Ru seedlayer, 10 nm Cu seedlayer, 5 nm Ta seedlayer and no seedlayer. All the samples were capped with a 5nm Ta capping layer to protect the SUL from oxidation. As shown in Figure 1.2.13, samples with a Ru seedlayer exhibited the lowest coercivity while samples with a Cu seedlayer exhibited the highest coercivity. The main reason for this phenomena may be that the lattice structure of Ru helps to build the amorphous CoFeTaZr structure. On the contrary, the Cu seedlayer may cause a crystalline structure in the CoFeTaZr films around the interface between the SUL and seedlayer, thus, resulting in higher coercivity. The hysteresis loops of easy-axis magnetization and hard-axis magnetization on different substrates are also presented in Figure 1.2.14-1.2.16. The crystallographic properties were analyzed by X-ray diffraction (XRD) and the patterns are shown in Figure 1.2.17.

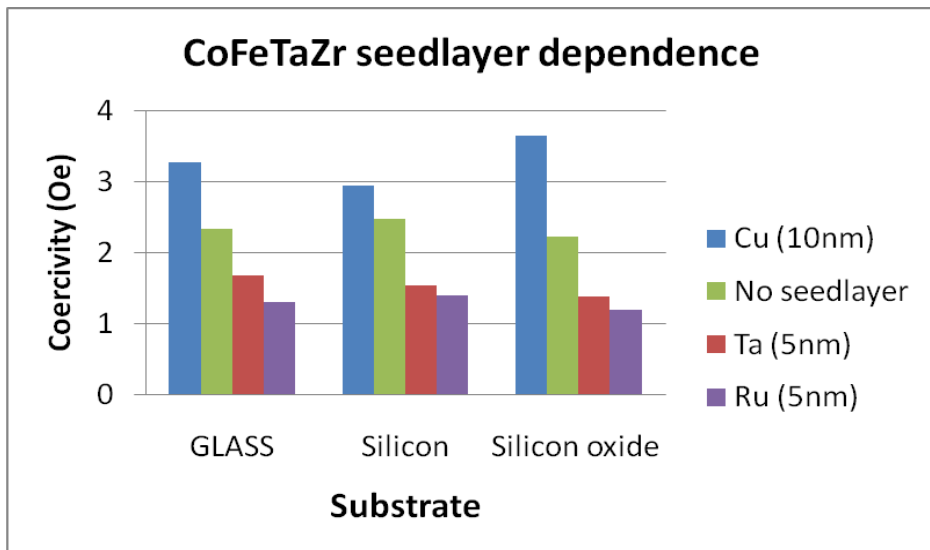


Figure 1.2.13 Coercivity vs. seedlayer dependence of CoFeTaZr amorphous thin films deposited on various substrates.

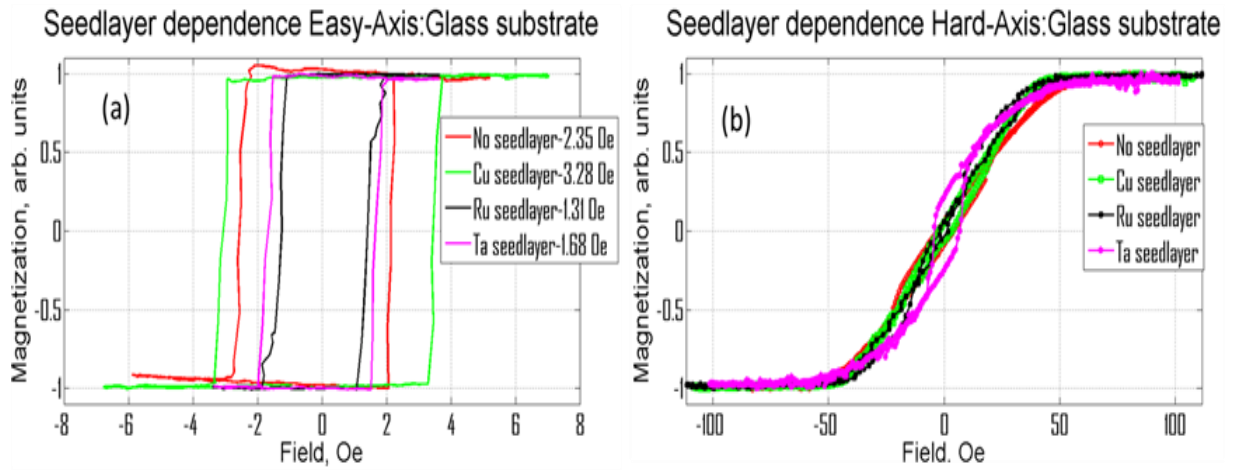


Figure 1.2.14 Hysteresis loops of seedlayer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr thin films deposited on glass substrates.

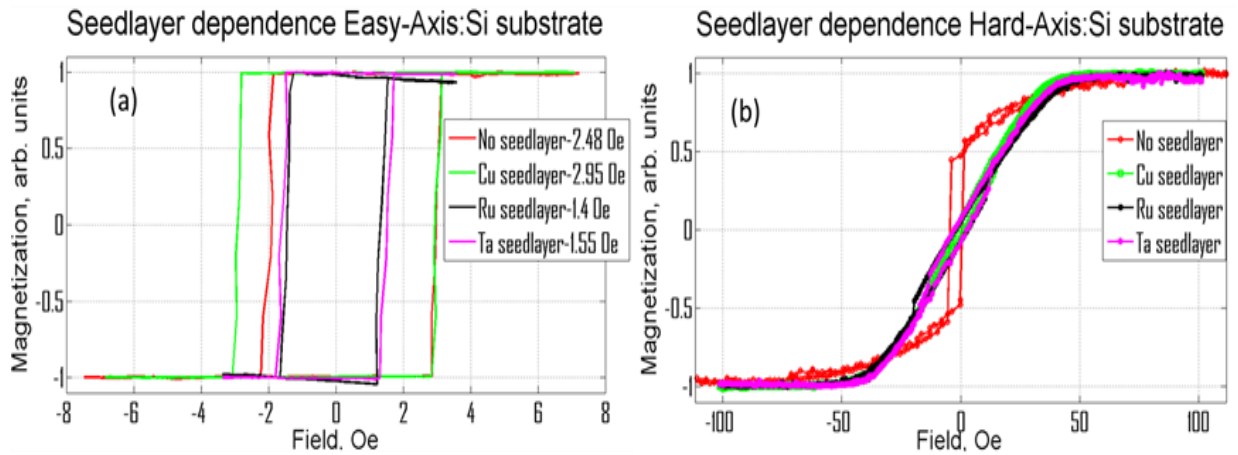


Figure 1.2.15 Hysteresis loop of seedlayer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr thin films deposited on silicon substrates.

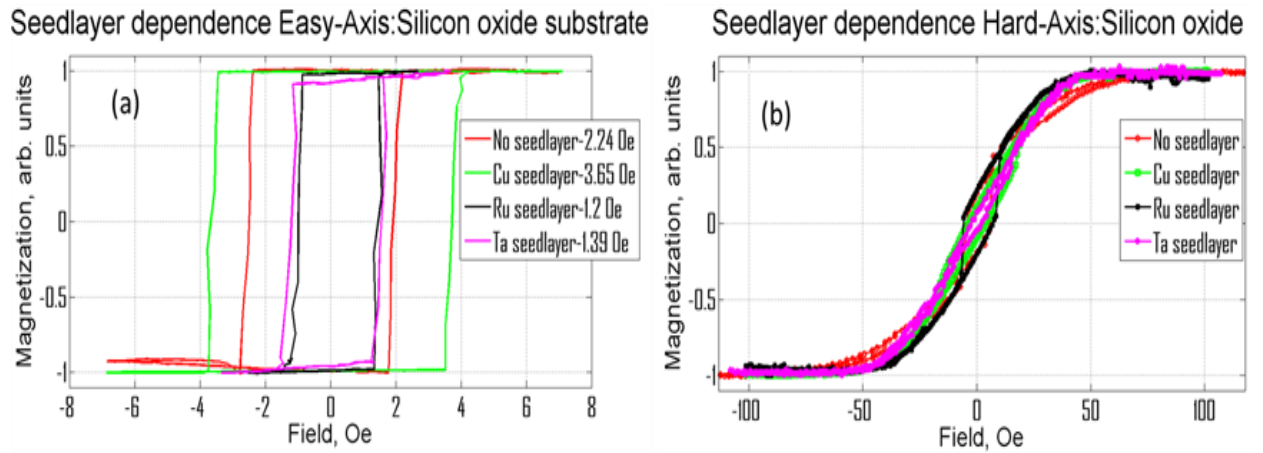


Figure 1.2.16 Hysteresis loop of seedlayer dependence of (a) easy-axis magnetization and (b) hard-axis magnetization of CoFeTaZr thin films deposited on silicon oxide substrates.

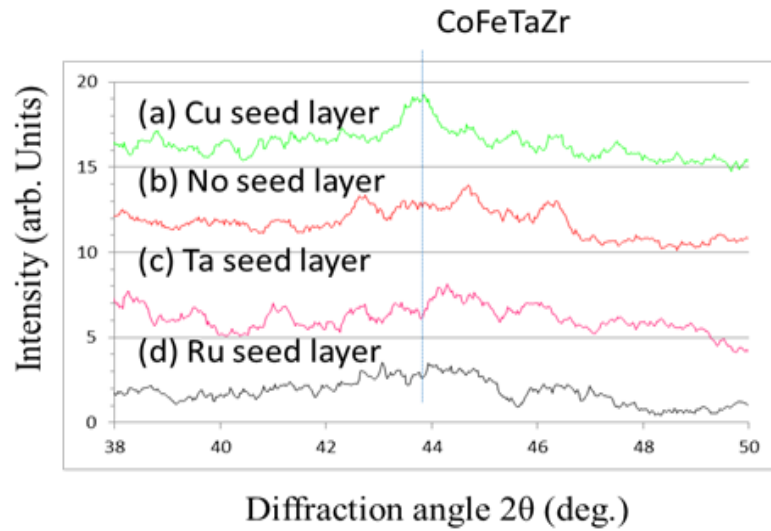


Figure 1.2.17 XRD patterns of (a) Cu seedlayer, (b) No seedlayer, (c) Ta seedlayer and (d) Ru seedlayer.

1.2.4 Conclusion

MOKE system measurements have been applied to investigate the relationship between different sputtering conditions, thicknesses, capping layers and seed layers of the amorphous thin film SULs and their magnetic properties. The following results were observed:

- 1) Ar ion milling played an important role in reducing the coercivity of the SULs, 30% reduction of the CoFeTaZr and 10% of CoTaZr thin films.
- 2) CoFeTaZr showed better magnetic properties than CoTaZr amorphous thin films, 10 times lower coercivity while remain the same magnetization.
- 3) Thicker SULs help to obtain better magnetic properties.
- 4) A Ta capping layer would be a suitable capping layer for CoFeTaZr amorphous thin film SULs rather than a Ru capping layer.
- 5) A Ru seedlayer helped to build the amorphous structure of CoTaZrFe SUL and improved the magnetic properties of the SUL.

Section 2 Nano Electrostatic Discharge Protection

Chapter 2.1 Introduction to Electrostatic Discharge (ESD) Protection

2.1.1 Overview of ESD and ESD Protection for IC

ESD, electrostatic discharge, is the sudden electricity flow between two objects when contacts. It is first documented by ancient Greeks by rubbing Amber with a piece of fur,

light weighted objects will be attracted to Amber, and electric sparks may also be observed if rubbing time is long enough. One cause for the ESD events is generated through tribocharging, by creating a difference of electrical potential. Another cause is through electrostatic induction, by creating an electrostatic field to redistribute electrical charges on the surface of a conductive object.

With the development of integrated circuit (IC) technologies, more and more electronic cells and functional circuits are incorporated on a small die on a silicon substrate, ESD protection is rapidly becoming a big interest both in academia and industry, since the ultra-small ICs are extremely sensitive and vulnerable to the high transient generated by ESD [74]. Common ESD failures are catastrophic, leading to immediate malfunction of IC chips by either thermal melting in silicon and/or interconnects due to high current or dielectric breakdown of gate oxide due to high voltage stressed in a very short time, as seen in Figure 2.1.1. It is reported that up to 35% of all IC field failures are associated with ESD damages [75-76].

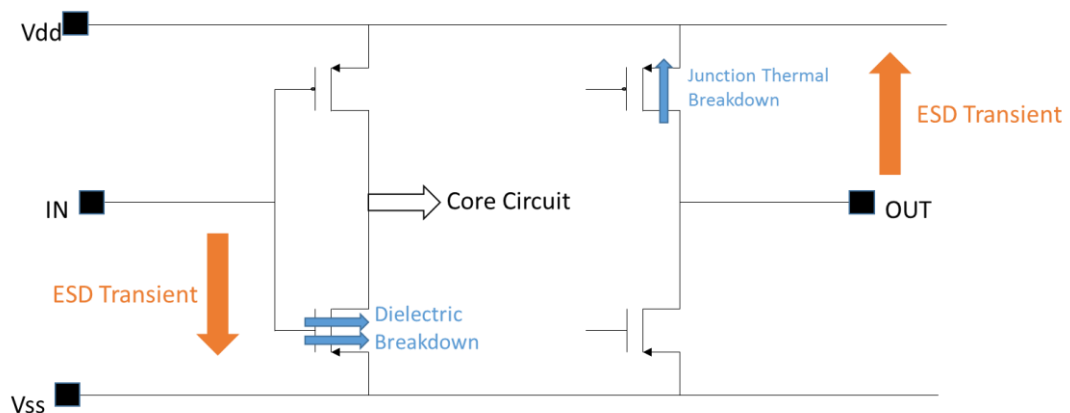
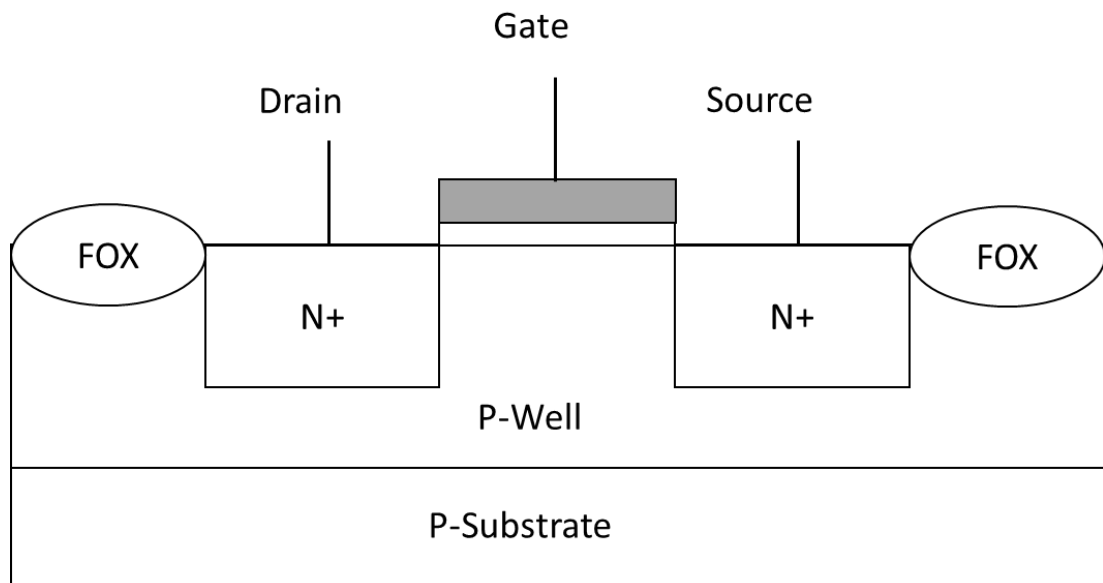
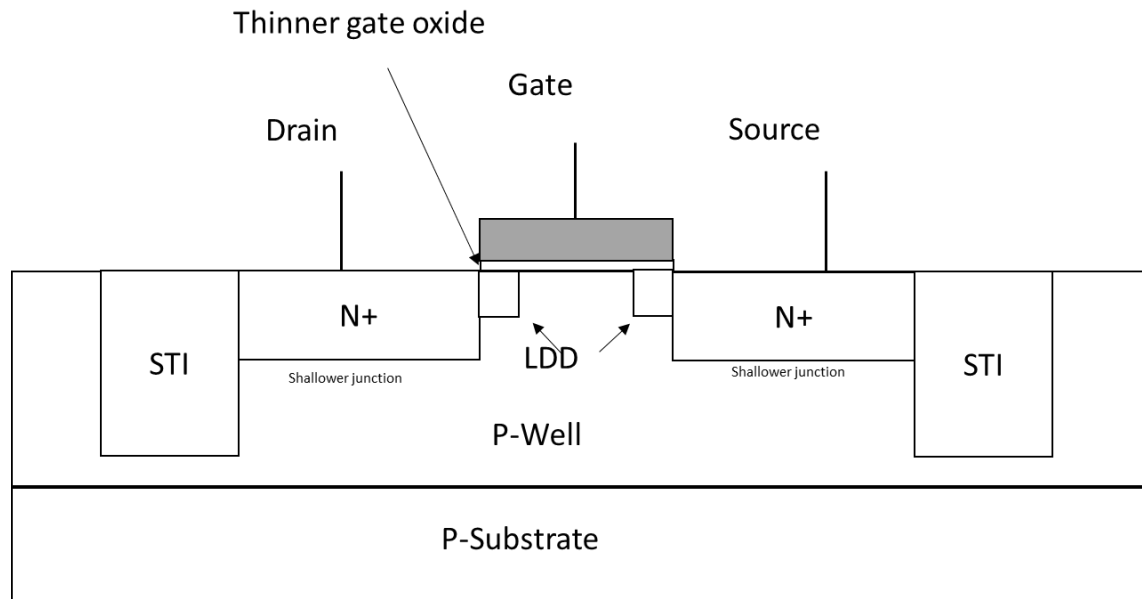


Figure 2.1.1 Possible ESD damages to IC circuits.

Different measures and means were set up and proposed in manufacturing, transportation and application fields to prevent electrostatic charging and provide a safe way for static discharging. In addition, various of on-chip and off-chip ESD protection structures were designed and applied in IC to handle ESD transient. As the ICs move into the deep-sub-micron level, ESD protection are facing many challenges: shallow trench isolation (STI) technology as well as light-doped drain (LDD) technology, may reduce the performance and reliability of some traditional ESD protection structures, as illustrated in Figure 2.1.2; shallower P+ and N+ junction may fail to conduct ESD transient to the deep substrate and cause heat crowding; thinner gate oxide results in lower robustness and make the gate oxide more susceptible to the ESD stress.



(a)



(b)

Figure 2.1.2 (a) Traditional MOSFET device. (b) New technology MOSFET device.

As the operating frequency of the chip being protected continues to increase, the parasitic components introduced by ESD, such as parasitic ESD capacitor (C_{ESD}), parasitic ESD resistor (R_{ESD}) and extra noise, starts to cause problems for RF operation [77].

2.1.2 ESD Protection Principles

2.1.2.1 ESD Protection Methods and Full-Direction ESD Protection

The principle of ESD protection is twofold: 1) provide a low-impedance discharging path to shunt the ESD currents, in order to prevent thermal damage of inner circuits causing by the high current ESD-induced; 2) clamp pin-voltage sufficiently low to a safe

level, in order to avoid dielectric breakdown, especially for the MOSFET gate oxide at the input node. Pin-voltage clamping also serves to avoid accidentally turn-on of internal devices. A good on-chip ESD protection should feature the following characteristics: 1) fast triggering to avoid premature ESD failure due to the accidental turn on of the internal parasitic structure; 2) high current handling capability, good heat dissipation capability, and low discharging impedance to boost the ESD robustness; 3) low parasitic effects to minimize the impacts on the function of the core circuits, especially for high-speed or high-frequency applications.

In practice, a complete full-direction ESD protection scheme is necessary to protect each pad against ESD surges come in from different formats [78]: positive ESD pulse from I/O pad to V_{dd} , which classified as PD mode; negative ESD transient from I/O pad to V_{dd} , which classified as ND mode; positive ESD stress from I/O pad to V_{ss} , which classified as PS mode; negative ESD pulse from I/O pad to V_{ss} , which classified as NS mode and positive ESD surge from V_{dd} to V_{ss} , which classified as DS mode. ESD protection structure must be designed accordingly to provide full-direction ESD protection between any two ports, as shown in Figure 2.1.3.

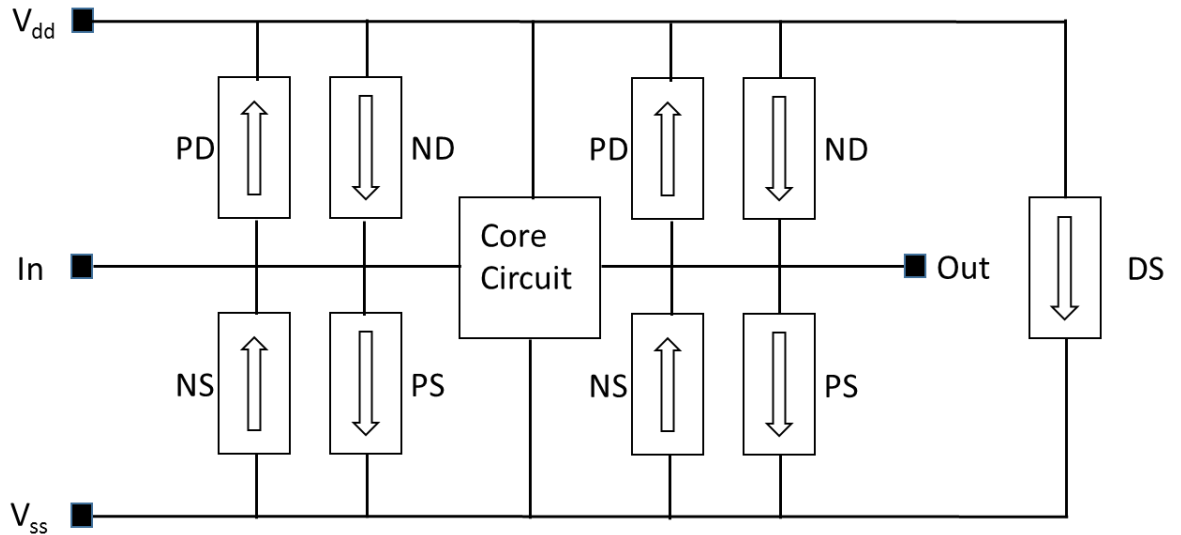


Figure 2.1.3 Full-direction ESD protection scheme.

2.1.2.2 ESD Protection Mechanisms and ESD Design Window

The two main ESD failures are: thermal breakdown and dielectric breakdown. And the principle of on-chip ESD protection solutions is two-fold: safely discharge the ESD currents via a low-impedance shunting path and clamp the pad voltage to a safely low level. There are two general means to classify the above ESD protection concepts, as illustrated in Figure 2.1.4. The first option is to use a protection device with a simple turn-on I-V characteristic as shown in Figure 2.1.4 (a). The protection unit will be simply turned on the triggering point (V_{t1} , I_{t1}) with I_{t1} being the triggering time, and forms a low-impedance shunting channel for the ESD currents. The discharging resistance of the I-V curve is defined as “on-resistance” R_{on} . The protection unit current handling capability, which reflects the ESDV level is limited by the thermal breakdown point (V_{t2} , I_{t2}).

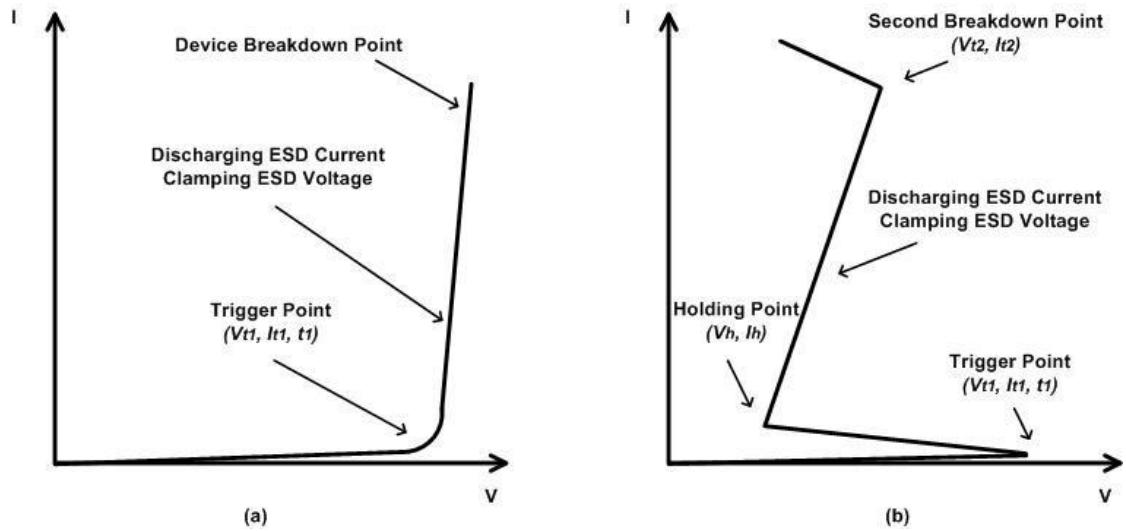


Figure 2.1.4 (a) Simply turn-on I-V characteristic. (b) Snapback turn-on I-V characteristic.

The other option is to use a protection unit based on snapback I-V characteristic, as depicted in Figure 2.1.4 (b). The protection element will be turned on at the triggering point (V_{t1} , I_{t1} , t_1), and then driven into a snapback region with low holding (V_h , I_h) to create the low impedance shunting path and clamp the ESD device to a safe level to avoid dielectric breakdown. The ESD protection performance level, i.e., ESDV level, is also represented by the second breakdown point (V_{t2} , I_2).

The ESD-critical parameters for any ESD protection structures include ESD triggering voltage and current (V_{t1} , I_{t1}), ESD triggering time (t_1), ESD holding voltage and current (V_h , I_h), ESD discharging on-resistance R_{on} , and ESD failure voltage and current (V_{t2} , I_2). Accurate and quantitative design for these ESD-critical parameters is a big challenge for ESD protection design optimization. As illustrated in Figure 2.1.5, practical on-chip ESD protection design must fit in the ESD Design Window, which is

defined by the supplies (V_{dd} , V_{ss}), breakdown voltage (V_{BR}), and total supply current (I_{dd}) with proper safety margins (at least 10%).

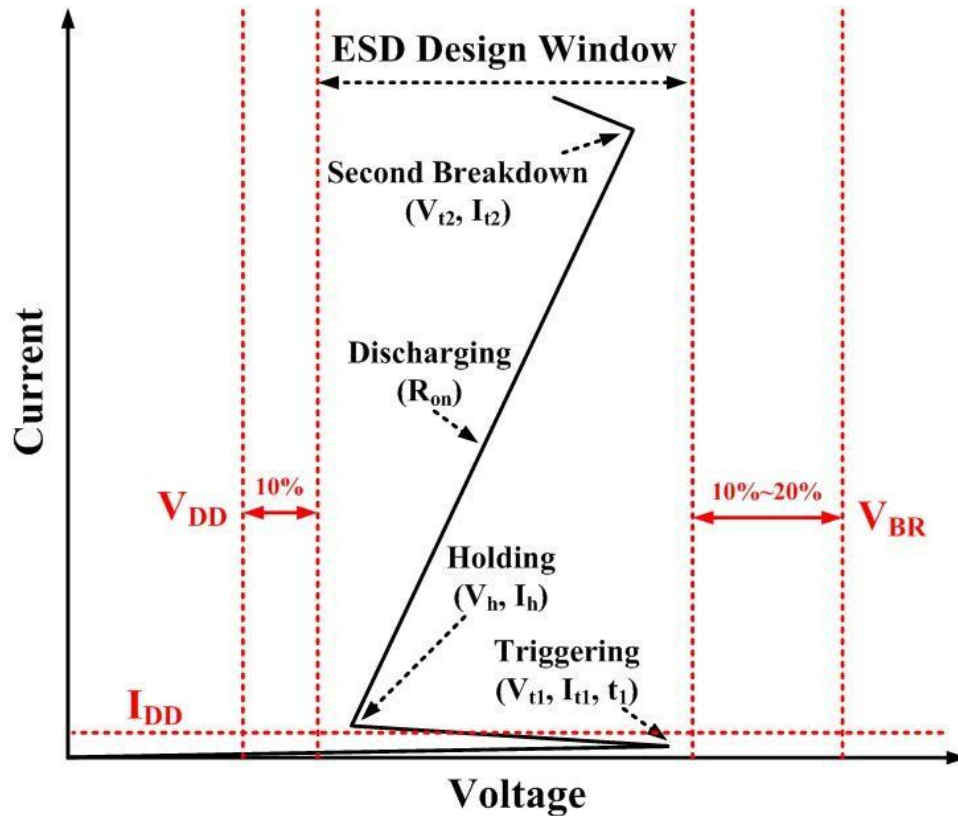


Figure 2.1.5 ESD Design Window.

In the ESD Design Window, triggering voltage (V_{t1}) of the protection element has to be less than V_{BR} to ensure the protection element will be turned on before the breakdown of the core circuits, while V_{t1} also needs to be higher than the supplies (V_{dd}) to avoid accidental turn-on of the protection element during normal operation. In addition, V_h and I_h ($I_h > I_{dd}$) must be carefully designed to avoid possible latch-up. Moreover, V_{t2} and I_{t2} , is the highest voltage and current the protection element can achieve, in a sense, represent the protection capability of the element. The higher the I_{t2} , the higher protection level the

element could achieve. The triggering time t_1 has to be smaller than the rising time t_r of the incoming ESD pulse waveforms per given testing standard, to ensure the protection element will be fast enough to turn on during the ESD event.

2.1.3 ESD Test Models

ESD is an extremely fast discharging phenomenon, occurring when two charged objects are brought into proximity. The corresponding high current (up to a few tens of Amps) and high voltage (up to a few tens of kilo Volts) transients may damage or degrade the performance of the IC parts. Different ESD test models are proposed according to its origins to simulate the ESD events, on-chip ESD protection are tested and valued upon those models.

2.1.3.1 Human Body Models (HBM)

Human body model (HBM), describes a discharge procedure that a charged human body contacts a device directly and electrostatic charges transfer from the human body into the device. This process usually lasts for several hundreds of nanoseconds (nS) and the peak current could reach to several Amps (A). The high current induced by ESD event in this extremely short time may damage the device if proper ESD protection is not provided.

One of the earliest and most widely accepted HBM test model is the military standard, MIL-STD-883E Method 3015.7, the simplified equivalent circuit is depicted in Figure 2.1.6 [79]. The equivalent circuit includes a 100pF capacitor C_{ESD} and a 1500 Ω series resistor R_{ESD} , represent the human body parasitic capacitance and resistance, respectively.

The ESD event is simulated by pre-charge capacitor C_{ESD} through resistor R_0 of 1~10 $M\Omega$, then it will discharge into an ESD DUT via R_{ESD} .

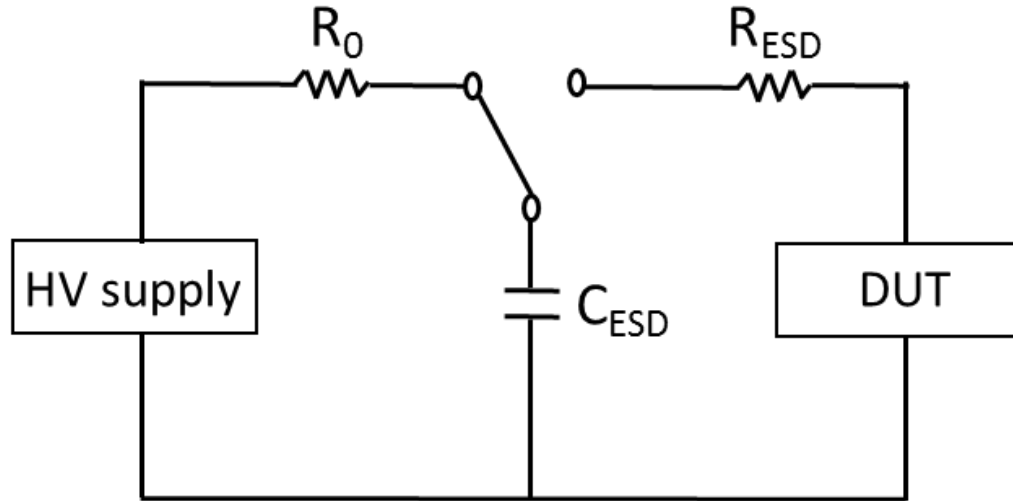


Figure 2.1.6 HBM model equivalent circuit.

However, parasitic parameters in a HBM tester may lead to significant deviation in the ESD tester waveform. To address these uncertainties, improved standard were proposed by several organizations. In Figure 2.1.7, a typical HBM discharging current waveform, defined in ESD Association HBM standard [80] is illustrated. The main parameters are defined as follows: pulse rising time (t_r) is between 2~10nS, pulse duration time (t_d) is around 150nS. A HBM tester must be able to deliver a discharging waveform fitting in the standard, and this verification has to be done before each HBM zapping begins.

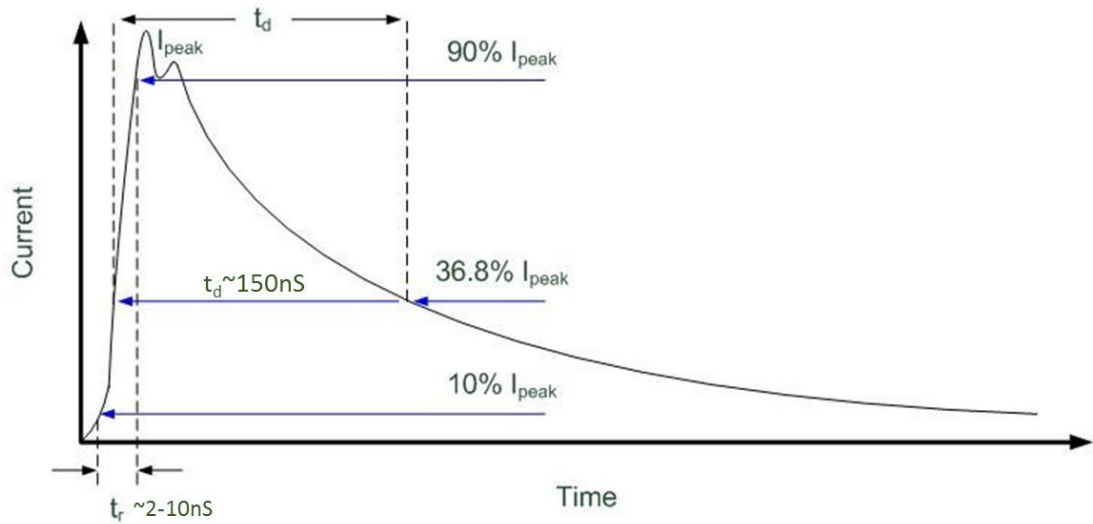


Figure 2.1.7 A typical HBM ESD discharging waveforms shows a typical rising time (2~10nS) and duration time (150nS).

2.1.3.2 Machine Model (MM)

Machine model (MM), describes the ESD events when metallic machinery contacts IC components in an IC manufacturing environment or automatic testing. Unlike in a HBM ESD case, the parasitic resistance is very low for metallic machinery. Therefore, the peak ESD current becomes much higher than that in a HBM event. A new ESD test model, MM was proposed and its equivalent circuit is shown in Figure 2.1.8, which is similar to that for HBM model [81]. This simplified circuit composed of a 200pF capacitor C_{ESD} and negligible R_{ESD} and L_{ESD} and produces an oscillatory discharging waveform with higher peak current and shorter rising time. A typical waveform is shown in Figure 2.1.9.

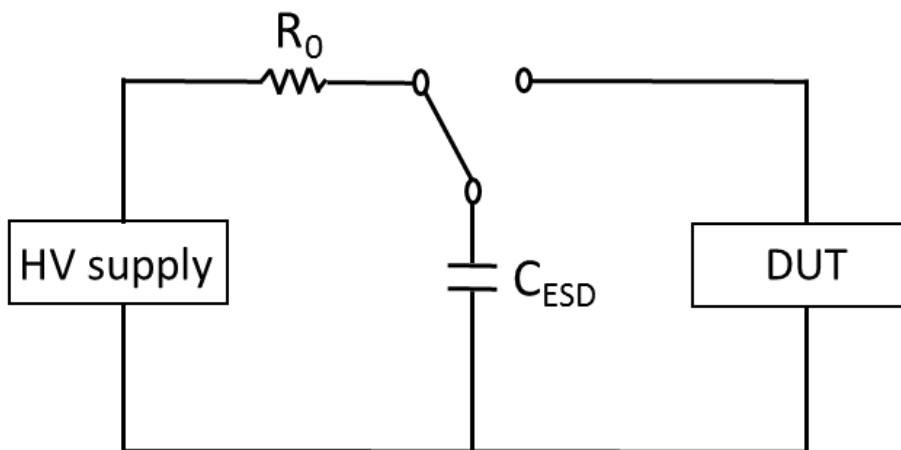


Figure 2.1.8 MM model equivalent circuit.

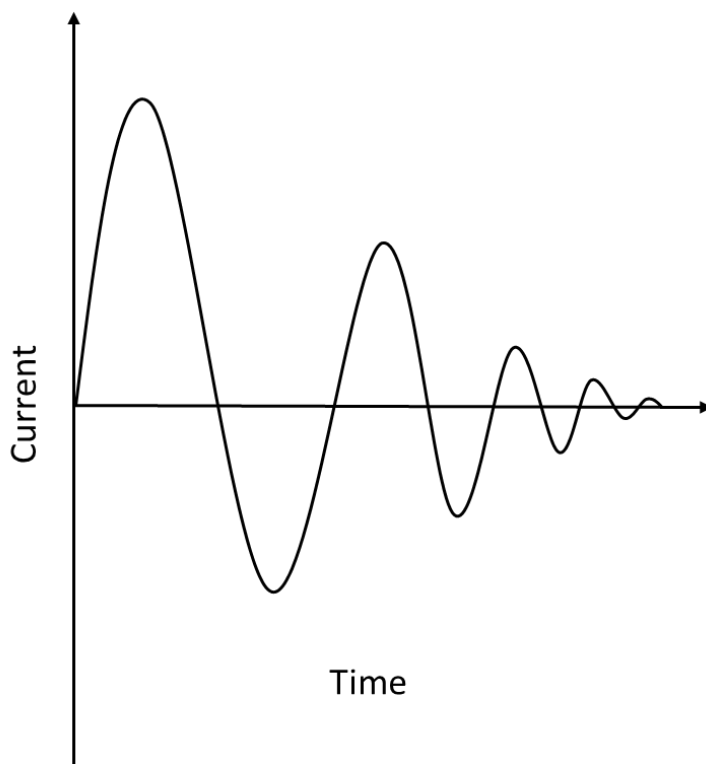


Figure 2.1.9 A typical MM ESD discharging waveforms shows its oscillating properties.

2.1.3.3 Charged Device Model (CDM)

Charged Device Model (CDM), depicts the ESD events where an un-grounded IC parts charged up during manufacturing or assembly and then discharges itself when a pin contacts a grounded object or conductive surface. Different from HBM model, since the CDM model is a self-discharge procedure. The CDM discharge is very rapid, featuring very short rising time, t_r ($\sim 1\text{nS}$), and very high peak current (up to several tens of Amps) due to the extremely low discharge resistance and inductance.

A typical CDM discharging waveform under a 3.5GHz bandwidth system is shown in Figure 2.1.10 based on the ESDA CDM standard [82]. In this standard with a 4pF verification module, the rising time has to be less than 200pS, duration time less than 400pS. It is reported that considering a maximum tolerable current of 7.5A the CDM protection level for a chip with the TQFP package is 750V. A CDM ESD event could be very deadly and attracts more attention as IC technologies advance, due to its impact on the even thinner gate oxide dielectric breakdown.

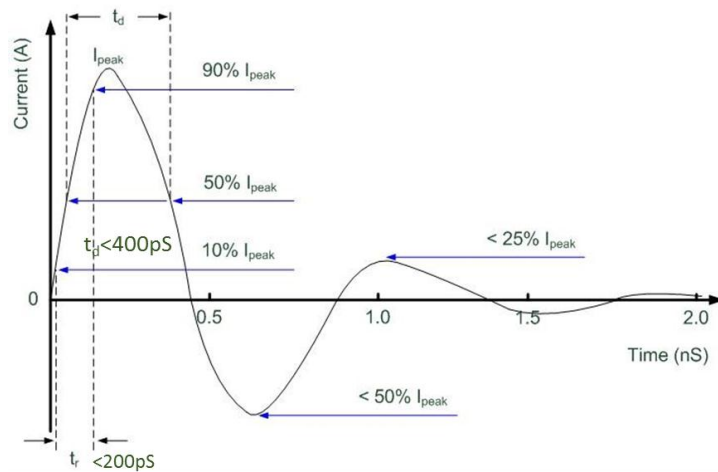


Figure 2.1.10 A typical CDM ESD discharging waveforms under 3.5GHz bandwidth system.

2.1.3.4 Transmission Line Pulse Model (TLP)

Transmission Line Pulse (TLP), unlike the HBM, MM and CDM, delivers more useful information by stressing IC parts with short square waveforms of varying heights, durations and rising times. Since its introduction into ESD protection design [83], the TLP technique has been increasingly accepted in practical ESD protection structure transient behavior.

A typical constant-impedance TLP set-up is illustrated in Figure 2.1.11 [84-85]. It contains a piece of transmission line cable which can be pre-charged to a specific voltage level, and produce a stable square waveform to stress the DUT; a matching constant resistance of 50Ω to discharge the ESD transient, provided by another transmission line cable; and an oscilloscope which collects the instantaneous current and voltage data. After each ESD stress, DC leakage current under operation power supplies is measured.

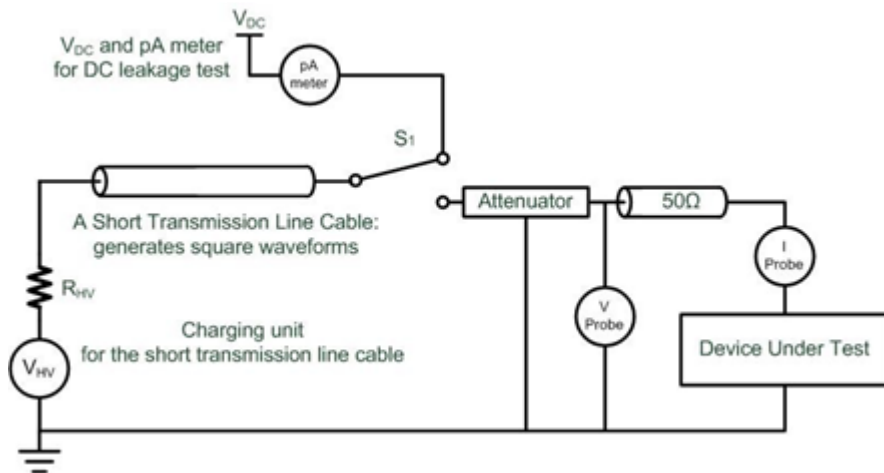


Figure 2.1.11 TLP testing system scheme.

Commercialized TLP tester will produce HBM-like pulses with various t_r (0.2, 2, 10nS) and t_d (50, 75, 100nS), to simulate HBM behavior of the ESD protection devices. Similarly, very-fast transmission line pulse (vf-TLP) is also introduced to evaluate the CDM behavior of the ESD protection devices [86].

2.1.4 ESD Protection Device Physics

As mentioned before, on-chip ESD protection units, being either single devices or sub-circuits, are placed at each port to protect it from ESD surges. And two typical I-V characteristics: simply turn-on and snapback are being adopted. Various ESD protection devices have been developed and applied into the industry, most of them are based on a few simple structures, which will be discussed in the following sections.

2.1.4.1 Diode and Diode Strings ESD Device

Diode, is a simple structure, as illustrated in Figure 2.1.12, with a N+ diffusion (Cathode) and P+/P-well diffusion (Anode), which defines as N diode; or a P+ diffusion (Anode) and a N+/N-well diffusion (Cathode), which defines as P diode. Due to its simplicity and efficiency, diodes are still widely used on IC chips.

Diodes can be used as ESD protection devices in either forward-biasing mode or reverse-biasing mode, typically the Zener diode. Either way, the simply turn-on I-V characteristic is in charge. In their forward-biasing mode, diodes will be turned on and start to form a low-impedance for the ESD currents, typically with a $V_{on} \sim 0.65V$ for silicon diodes. While in their reverse-biasing mode, diodes have a higher turn on voltage,

usually associated with their junction avalanche breakdown voltage, but a low current handling capability compared to the forward-biasing mode.

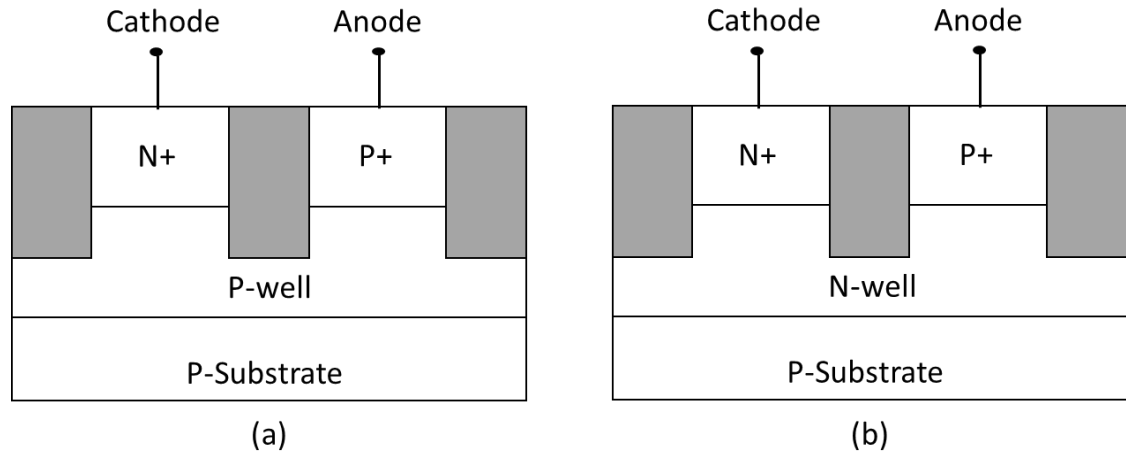


Figure 2.1.12 (a) N-type diode. (b) P-type diode.

Thus, diodes are commonly reverse-connected to the I/O ports as shown in Figure 2.1.13, to avoid accidentally turn on during normal operation. And a power clamp must be added between V_{dd} and V_{ss} to provide a full-direction ESD protection at all ports. During ESD zapping, for example, from I/O ports to V_{dd} (PD mode), D1 will be forwardly turned on and with the power clamp, form a PD shunting path; from V_{dd} to I/O ports (PS mode), D2 will be forwardly turned on and with the power clamp, form a ND shunting path. For PS mode, the current discharging path is similar to PD shunting path; and NS mode discharging channel is similar to PS shunting path. And the design must strictly follow the ESD Design Window, the voltage drop of the shunting path, equal to the voltage drop of the forward-on diode plus voltage drop of the power clamp, must be lower than the breakdown voltage of the core circuit.

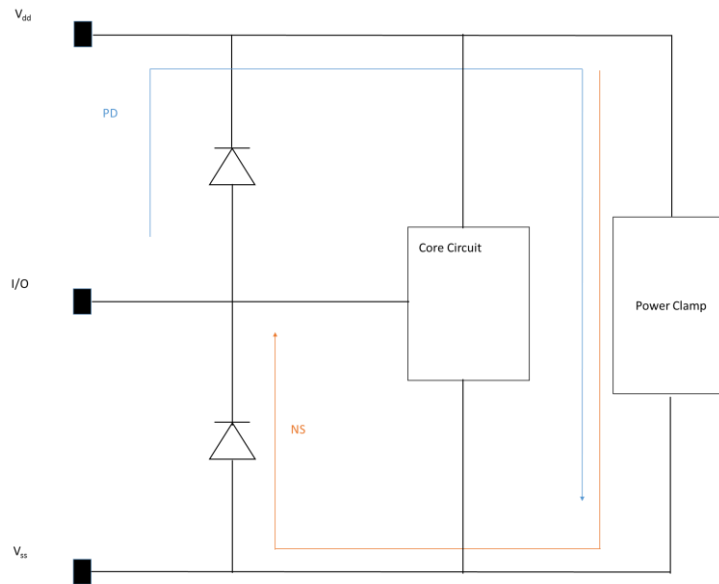


Figure 2.1.13 Diode ESD Protection Scheme.

However, the main disadvantage of diode protection device is associated with its fixed low turn-on voltage that limits its application in high V_{dd} case. Multiple diode strings may overcome the problem, as illustrated in Figure 2.1.14. One believes that the parasitic capacitance C_{ESD} is inversely proportional to the number of diodes (N), assuming the junction-induced capacitance is the only source for the parasitic capacitance. However, it is not true in real applications. First, some extra parasitic capacitance do not follow this trend, hence, simply increase N may not ensure continuous reduction in the total C_{ESD} . Second, increase N will result in larger layout area for the device. Third, extra noise figure may be increased as N increased. Therefore, N must be optimized to balance overall performance. It is reported N equals to 2 or 3 will provide optimal ESD protection [87].

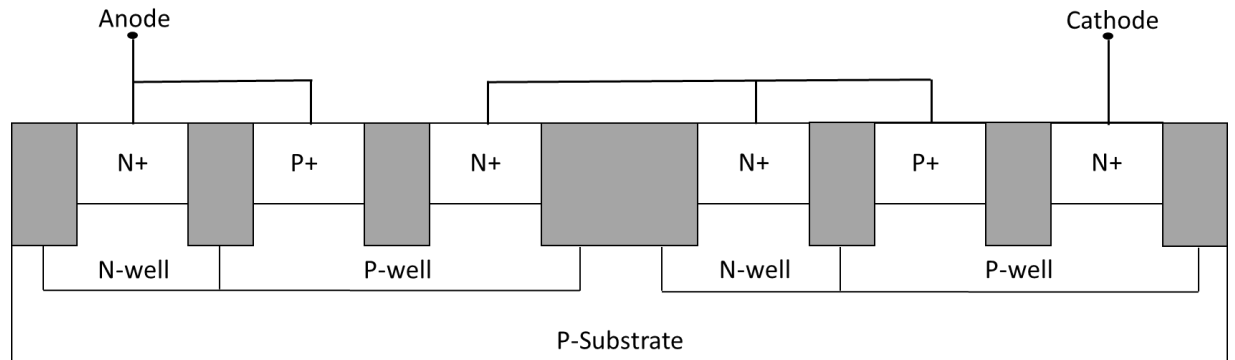
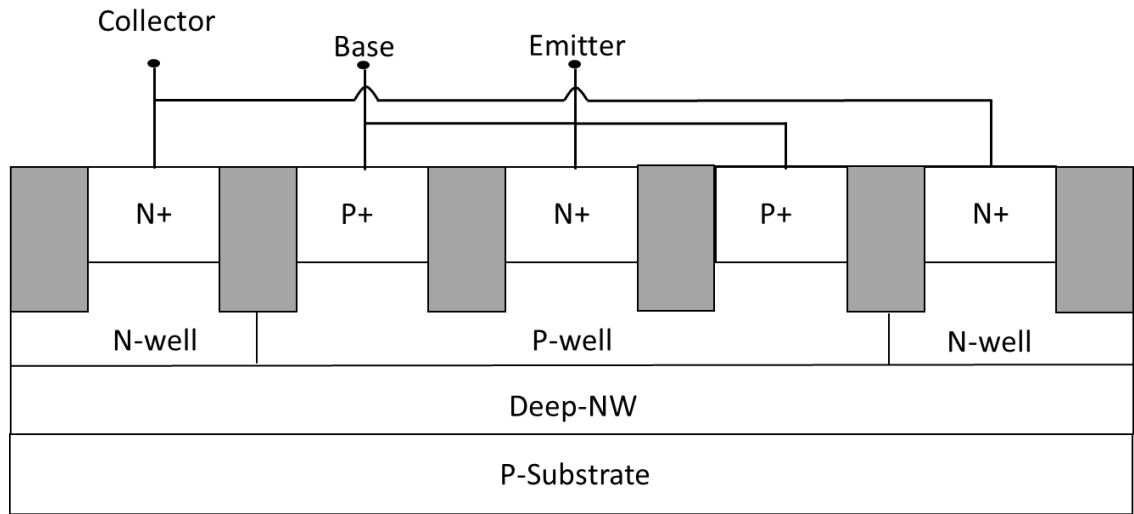


Figure 2.1.14 Diode String (N=2).

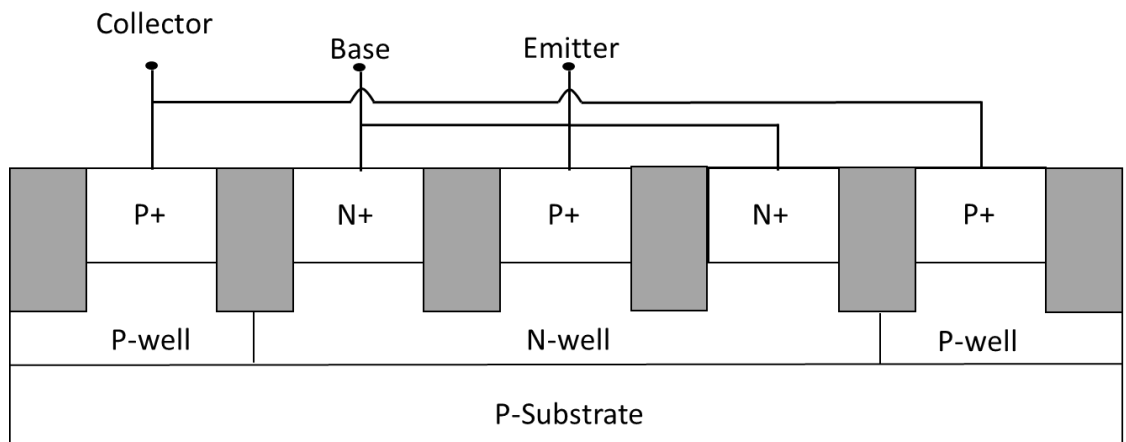
2.1.4.2 BJT ESD Device

Recently, vertical BJTs gradually take over lateral BJTs for their superior performance: shorter base width (higher β and faster speed) and smaller size with the same current handling capability as lateral BJTs.

A typical vertical NPN BJT cross section structure is shown in Figure 2.1.15 (a). The structure is composed of emitter (N+ diffusion in the middle), base (P+ diffusion in the P-well region) and collector (N+ diffusion in the N-well region). Similarly, a vertical PNP BJT is composed of emitter (P+ diffusion in the middle), base (N+ diffusion in the N-well region) and collector (P+ diffusion in the P-well region).



(a)



(b)

Figure 2.1.15 (a) Typical vertical NPN BJT cross section. (b) Typical vertical PNP BJT cross section.

BJT normally works in a snapback mode as an ESD protection device. The protection scheme is shown in Figure 2.1.16 [88]. In case (a), Q1 is off under normal operation, and when ESD appears at I/O pad, base potential V_B is designed to raise up to turn on Q1 and

form a shunting path for the ESD current. In case (b), BJT is connected on I/O pad with its base connected to emitter through R. Take Q2 as an example, when an ESD pulse appears at I/O with respect to V_{ss} , the collector-base junction is reverse-biased until reaches its avalanche multiplication, then the current flows to V_{ss} through R and builds up the voltage across the base-emitter junction. As V_{BE} becomes greater than V_{ON} , Q2 turns on. Then i_E will take over and maintain the multiplication. V_C starts to decrease and Q2 moves into snapback region. It will form a safe channel to shunt the ESD current as well as clamp the voltage to avoid possible dielectric breakdown of the core circuit. If a negative ESD pulse appears at I/O with respect to V_{ss} , the parasitic diode of Q2 together with R will form a shunting path for ESD current.

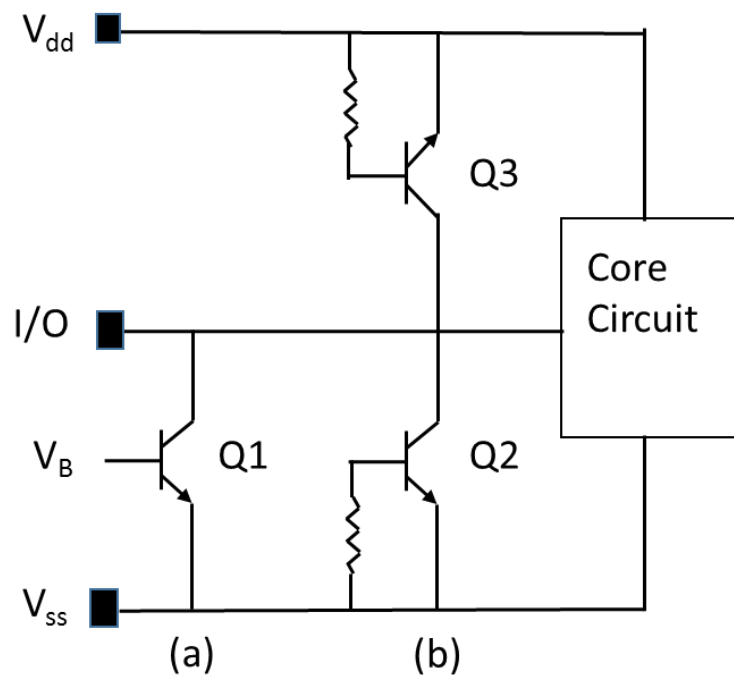
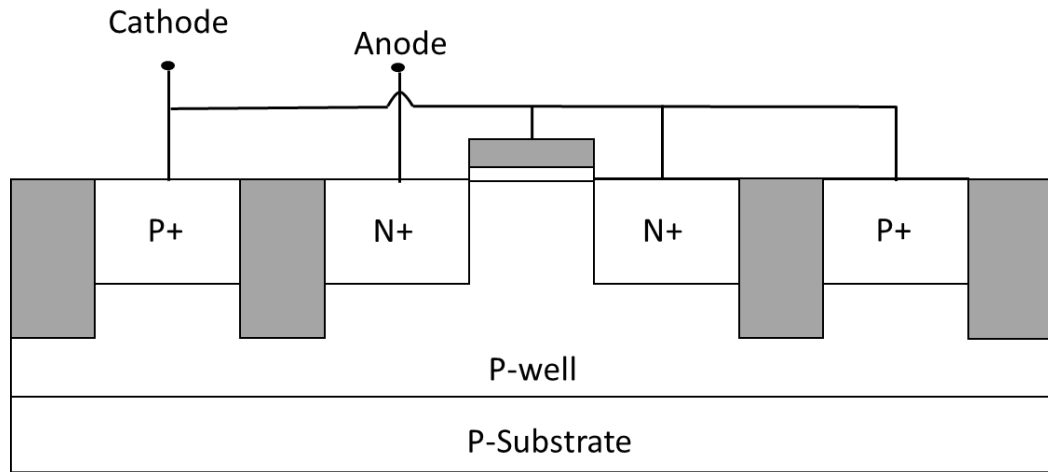


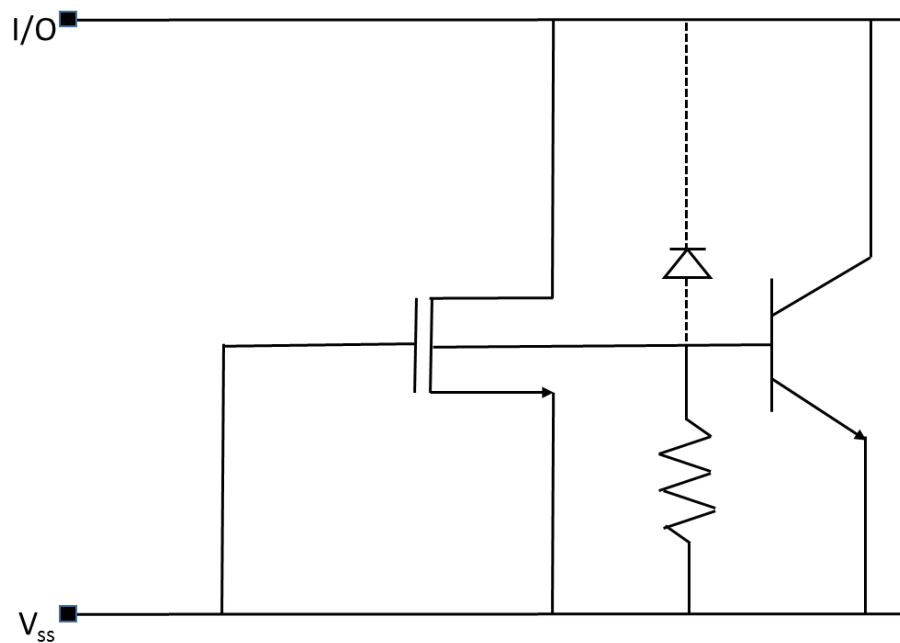
Figure 2.1.16 BJT ESD protection scheme.

2.1.4.3 MOSFET ESD Protection

Figure 2.1.17 illustrates the cross section and equivalent circuit of a commonly used grounded-gate NMOS (ggNMOS) ESD structure, where the drain is connected to the I/O pad, and the gate is grounded. When a positive ESD pulse appears at I/O pad with respect to V_{ss} , DG junction is reverse biased until the avalanche breakdown is reached. Then the multiplication will take place and builds up a voltage drop V_R across BS junction, as the voltage drop increases, the parasitic NPN BJT will be turned on, and the rest story will be the same as that told in BJT. After being turned on at the triggering point V_{t1} , ggNMOS will be driven into the snapback region and form a low-impedance path for the ESD currents. And when a negative ESD pulse appears at I/O pad with respect to V_{ss} , the parasitic diode will be forward-biased and turned on. The reason for grounding the gate is to ensure the ESD protection device is totally off during normal operation. ggNMOS is a natural option in CMOS technology, but due to the low current handling capability of the parasitic diode, its application is limited. And also due to the snapback characteristic, it could not be included in the SPICE simulation.



(a)



(b)

Figure 2.1.17 (a) Cross section of a typical ggNMOS. (b) Equivalent circuit of ggNMOS.

A typical ggMOS protection scheme is depicted in Figure 2.1.18, with Vdd connected to the gate of a ggPMOS and I/O pad connected to the drain of the ggPMOS. In this

scheme, ggPMOS is usually larger size than that of ggNMOS, since the parasitic PNP BJT of the ggPMOS is inefficient, and requires a much bigger size to achieve the same protection level as ggNMOS.

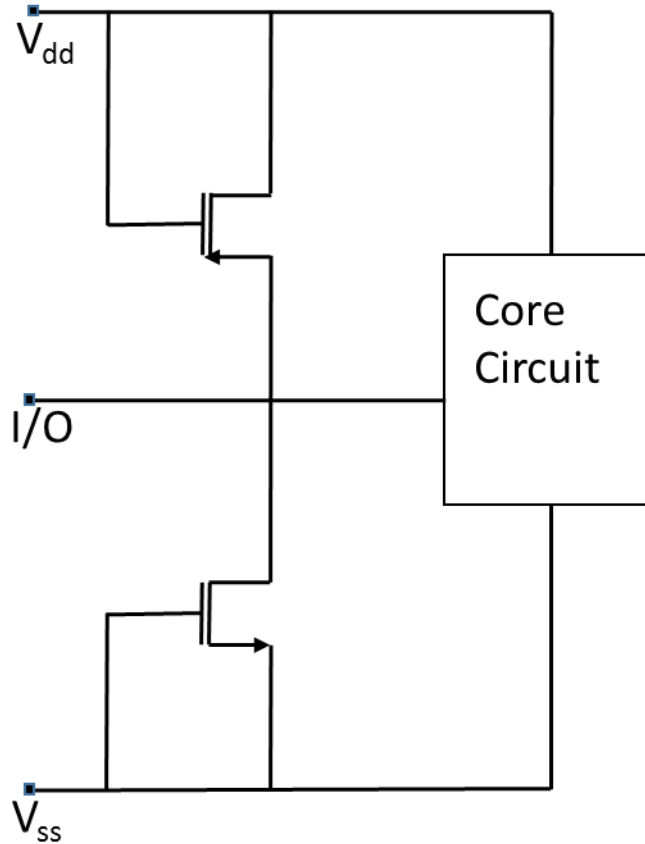


Figure 2.1.18 ggMOS ESD protection scheme.

In practical application, a multi-finger structure is required to achieve better performance. Many small ggMOS will be connected parallel to provide ESD protection. However, for ggNMOS, the thermal breakdown voltage V_{t2} is usually smaller than the triggering voltage V_{t1} . In that case, it is possible that failure may occur before all the

fingers participate in the protection process, and the protection level will be reduced. This problem is addressed by taking several actions. First, layout dimension is finely adjusted, for example, the drain contact to gate space (DCGS), gate length (L) and the source contact to gate space (SCGS). Second, inserting a ballasting resistor into each finger or using a gate-coupled structure to reduce the V_{t1} , the structure is shown in Figure 2.1.19. In principle, a coupling capacitor will lift up the gate voltage of NMOS and accelerates the V_{BE} building up for the parasitic NPN BJT, hence reduce V_{t1} . However, a careful design is needed to pick up a suitable value for R and C to avoid over-stressing the gate while reducing V_{t1} [89].

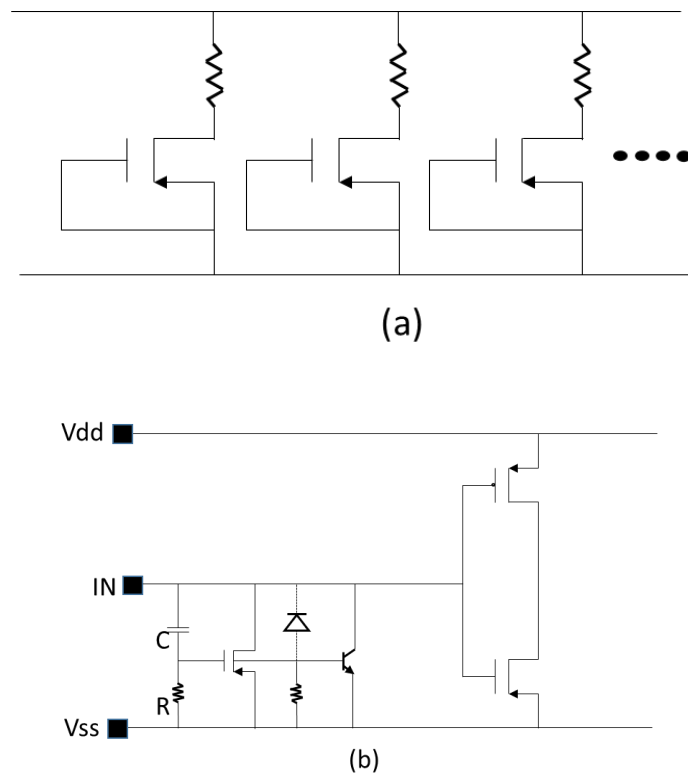
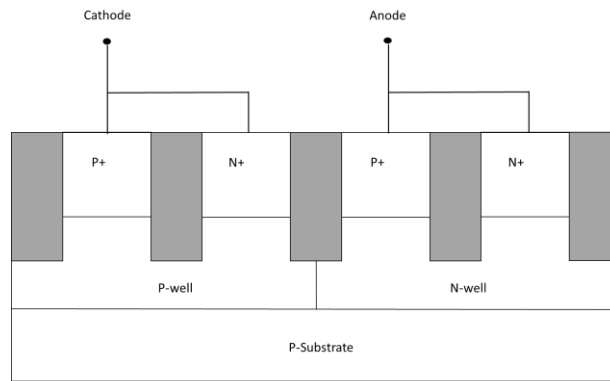


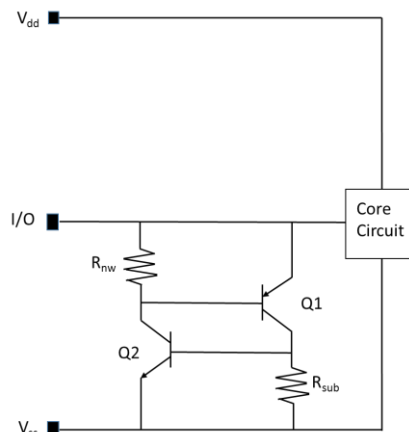
Figure 1.30 (a) Adding ballasting resistor to enhance uniformity. (b) A gate-coupled MOS ESD protection scheme.

2.1.4.4 SCR ESD Protection

Silicon controlled rectifier (SCR), may be one of the most efficient ESD protection structure due to its deep snapback I-V characteristic, that could be used to handle large current transients. As illustrated in Figure 2.1.20 (a), SCR is consisted of a N+ diffusion and a P+ diffusion in a N-well and a N+ diffusion and a P+ diffusion in P-well. Its equivalent circuit is shown in Figure 2.1.20 (b), which composed of one parasitic PNP BJT and one parasitic NPN BJT.



(a)



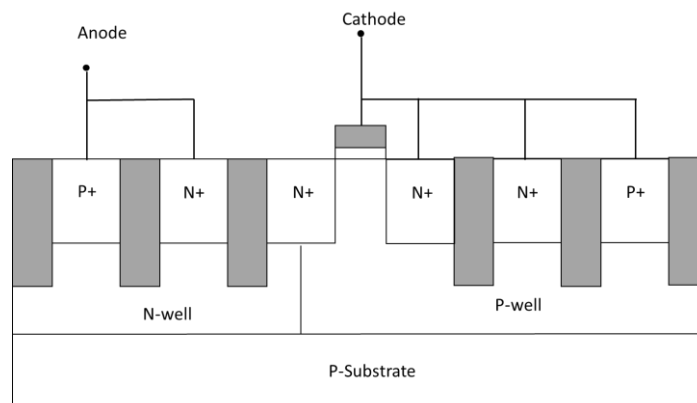
(b)

Figure 2.1.20 (a) Cross section of SCR. (b) Equivalent circuit and ESD protection scheme of SCR.

SCR could be connected as demonstrated in Figure 2.1.20 (b). When a positive ESD pulse appears at I/O with respect to V_{ss} , N-well/P-well junction is reverse-biased to its avalanche breakdown. And the multiplication takes place and builds up potential drop of V_{BE} of Q2 through parasitic R_{sub} . After Q2 turns on, its i_B serves as i_C for Q1, and in return, i_B of Q1 serves as i_C for Q2, these two parasitic BJT starts to feed each other. And SCR is on, a low-impedance active path is formed and the voltage between I/O and V_{ss} will be clamped to a safe low level.

However, cautions are needed to avoid possible latch-up effect due to the low holding voltage and relatively high V_{t1} outside the ESD Design Window. Its improved versions work in many fashions.

As shown in Figure 2.1.21, a LVSCR is introduced. A ggNMOS is placed over the N-well boundary [90]. When ESD event happens, ggNMOS turns on first and then helps to turn on the SCR. In this case, V_{t1} of SCR will be reduced, almost the same as ggNMOS in the same technology.



(a)

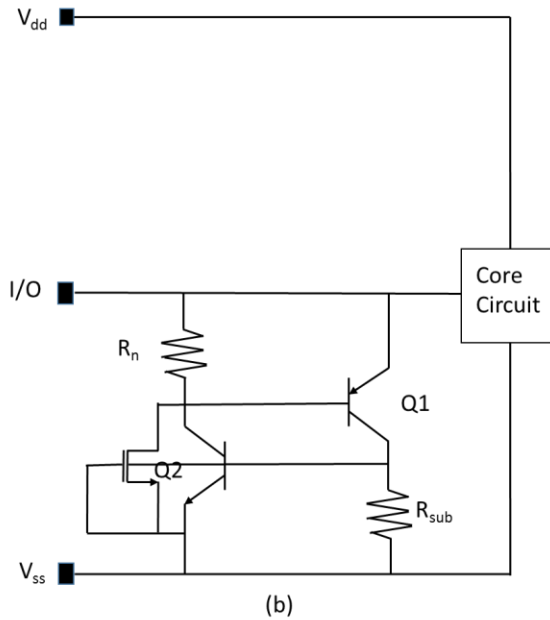


Figure 2.1.21 (a) Cross section of LVSCR. (b) Equivalent circuit and ESD protection scheme of LVSCR.

Another method is illustrated in Figure 2.1.22 [91]. DTSCR employs an external diode string to help injecting current to the base of parasitic PNP and NPN BJT. In case (a), diode string helps to forward bias BE junction of Q2 and further turns on SCR. SCR then clamps the voltage between I/O and V_{ss} to a safe level, the triggering voltage V_{t1} is determined by the number of the diodes in the diode string. In case (b), instead, the diode string helps to forward bias BE junction of Q1 and the rest is the same as case (a). One less diode could be used in this diode string to obtain the same triggering voltage as case (a), since the parasitic diode of PNP should be considered. In case (c), similar as case (b), a diode could be placed at the BE junction of Q1 to further increase the holding voltage of the DTSCR while maintaining the same triggering voltage.

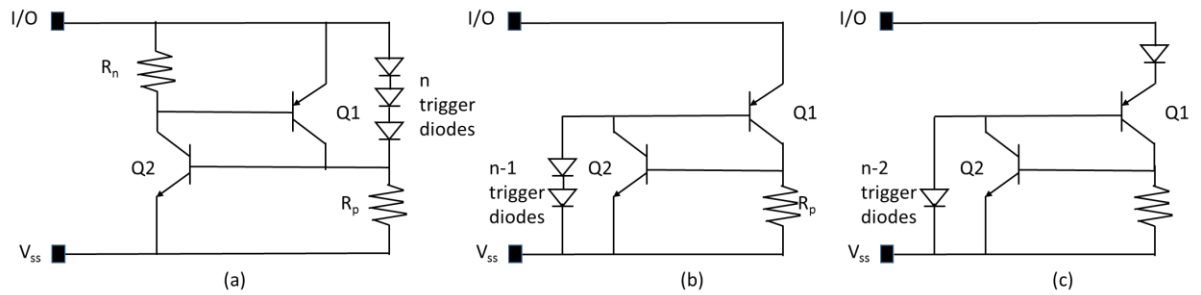


Figure 2.1.22 Equivalent circuit of DTSCR (a) Forward-biasing V_{BE} of Q2. (b) Forward-biasing V_{BE} of Q1. (c) Forward-biasing V_{BE} of Q1 and increase holding voltage at the same time.

Chapter 2.2 Novel ESD Protection Structures

2.2.1 Filed Programmable ESD Protection Structure

2.2.1.1 Introduction

ESD failure is a major reliability problem to ICs and on-chip ESD protection is mandatory to all ICs and electronic systems [77][88][92]. Accurate and quantitative design for ESD-critical parameters, including triggering voltage and current (V_{t1} , I_{t1}), triggering time (t_1), holding voltage and current (V_h , I_h), ESD discharging resistance (R_{on}) and thermal breakdown voltage and current (V_{t2} , I_{t2}), is an emerging challenge for ESD design optimization and prediction for complex mixed-signal ICs due to the ESD Design Window Shrinking Effect [89][92-95]. As the IC technologies advance, for example, BVD decreases rapidly while V_{dd} only reduces slightly, causing the ESD Design Window shrinks. Furthermore, complex mixed-signal ICs using multiple supplies require flexible V_{t1} in each power domain on a chip. In addition, emerging nano scale devices and circuits require a new nano ESD protection solution. Finally, multichip modules (MCMs) and

system boards utilize many different ICs fabricated in different IC processes and some ICs may be replaced over the time for certain products, which may require fine revision of ESD specs (e.g., V_{t1}) in field designs. Therefore, novel programmable post-Si ESD protection mechanisms and structures are needed to replace the existing ESD protection solutions that cannot address the above ESD protection challenges.

2.2.1.2 New Programmable ESD Protection Mechanisms

Field-programmable devices have been widely studied and used for nonvolatile memories [96-102]. Understanding that transistor threshold voltage could be changed by means of gate programming techniques, we devised two field-programmable ESD protection mechanisms to realize tunable ESD protection circuitry allowing IC designers to fine-tune the ESD protection structure V_{t1} in post-Si field designs, including NC-QD-based ESD protection structure and SONOS-based ESD protection structure. Both the NC-QD and SONOS ESD protection structures are CMOS-compatible.

2.2.1.2.1 NC-QD ESD Protection Mechanism

Figure 2.2.1 illustrates a conceptual new silicide-coated NC-QD ESD structure and its energy diagrams. In principle, an NC-QD ESD structure is an MOSFET incorporating layers of nanocrystal dots inside the floating gate layer, which is connected as an ESD protection unit, such as ggMOS, gdMOS. To program ESD protection structure, charging/de-charging function is utilized to adjust its ESD V_{t1} as needed. Traditional ggNMOS ESD protection structure relies on the drain breakdown to trigger ESD discharging under ESD stressing, where V_{t1} is determined by its BV_{DS} that is fixed by the

doping profile. In contrast, the new programmable NC-QD utilizes two possible tunneling-assist ESD triggering mechanisms. First, the programming of the nanocrystal dots can change the V_{th} , which alters the ESD V_{t1} . Second, varying the gate bias by design can change the maximum electric field (E_{max}) inside the gate oxide and channel, thus altering the BV_{DS} , which in return, changes the V_{t1} . This can be modeled by the following equation:

$$\Delta V_{th} \approx \frac{qn_{well}}{\epsilon_{ox}} (t_{ctl} + \frac{1}{2} \frac{\epsilon_{ox}}{\epsilon_{Si}} t_{well}) \quad (3)$$

Where t_{well} is nanocrystal well dimension, n_{well} is nanocrystal dot density, t_{ctl} is gate-oxide thickness and ϵ is dielectric constant. Several possible on-chip ESD protection schemes may be realized using our new NC-QD ESD protection structure, as illustrated in Figure 2.2.2. In scheme 1 (ESD-1), a typical ggNMOS ESD unit where the field-programming node allows designer to program the ESD V_{t1} . Alternatively, a typical gcNMOS ESD block can be constructed (ESD-2), which may be externally programmed to achieve the required ΔV_{t1} . The third type where the gate and drain can be tied together to form a unique gdNMOS (ESD-3) for a non-snapback I-V characteristic. ESD-3 can achieve a lower V_{t1} , which is not possible for traditional MOSFET structures due to the susceptibility of the thin gate. ESD-4 can be easily used as a power clamp or at I/O.

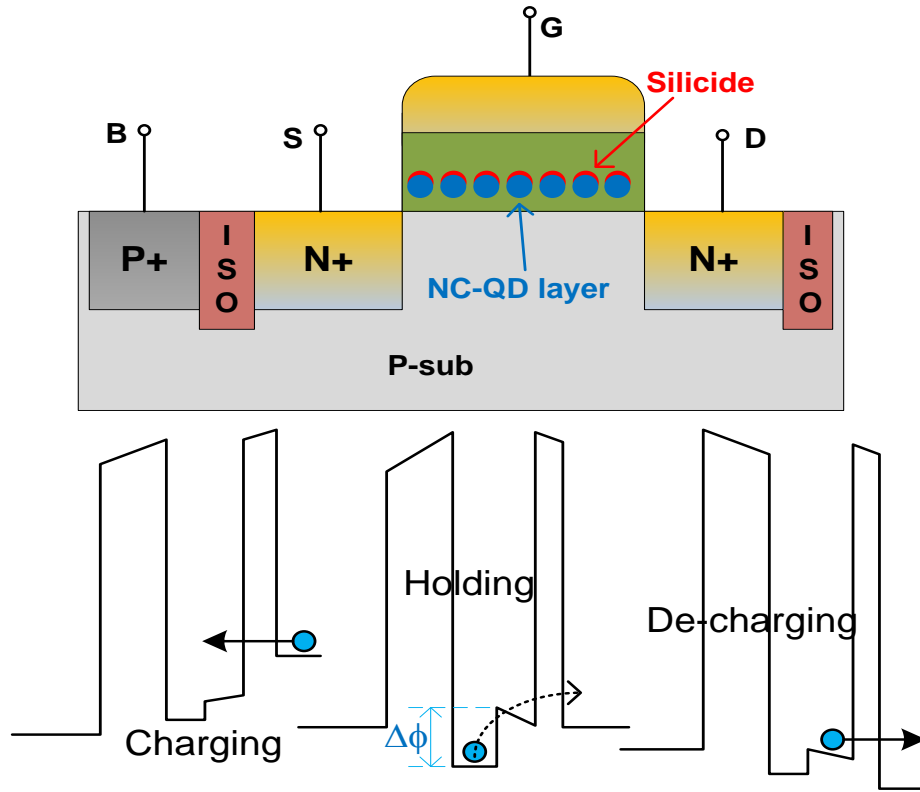


Figure 2.2.1 Cross-section and energy diagram for the new NC-QD ESD protection structure.

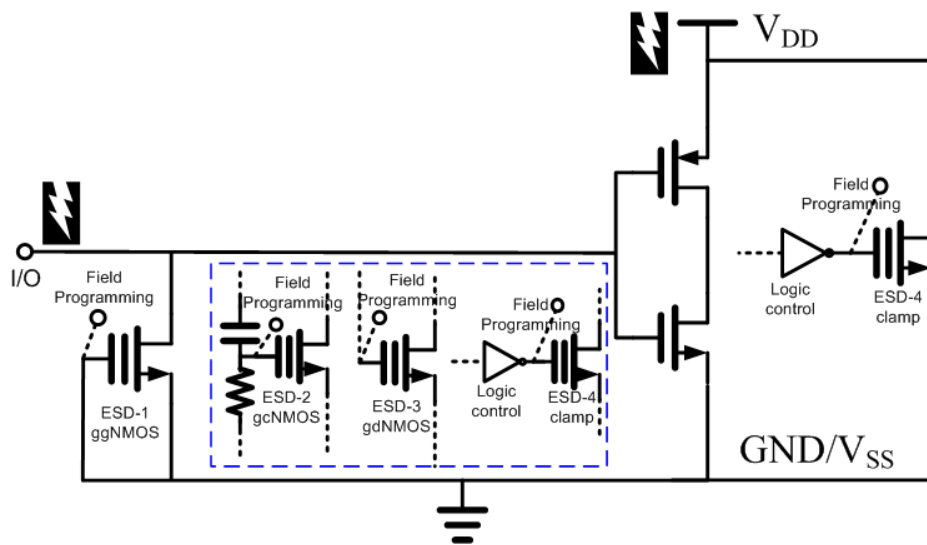


Figure 2.2.2 Possible chip-level ESD protection schemes using the new NC-QD ESD protection structure.

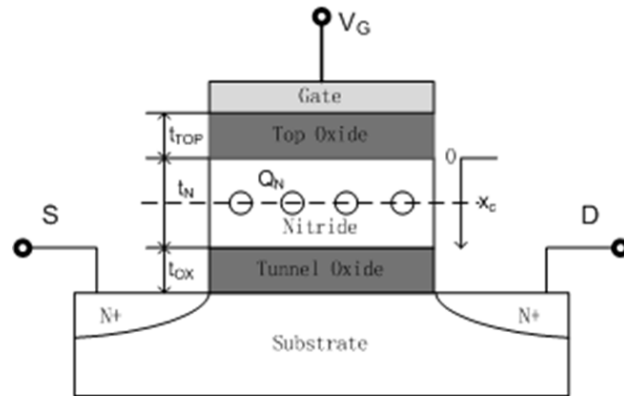
In real design, several techniques can be used to fine tune the ESD V_{t1} . First, the NC-QD ESD structure may be pre-programmed individually off-chip to adjust the V_{t1} for different IC blocks using different supplies. Second, on-chip digital programming circuitry may be used to locally program the nanocrystal dots for varying ESD V_{t1} . Third, on-chip V_G biasing can be programmed to adjust the V_{th} and thus control the ESD V_{t1} . Fourth, ESD V_{t1} can be adjusted by varying the nanocrystal dots density, as illustrated before in formula (3). In the future, multi-layer NC-QD arrays may be realized to achieve even wider ΔV_{t1} for more accurate and flexible on-chip ESD protection design in field applications.

2.2.1.2.2 SONOS ESD Protection Mechanism

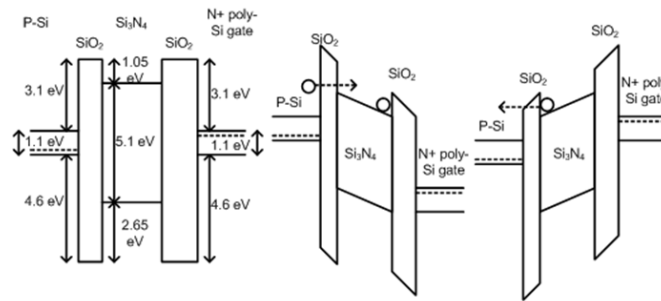
Figure 2.2.3 shows the conceptual SONOS ESD protection device and its bandgap structures under neutral, programming and erasing conditions. The new ESD mechanism is that the charges are stored inside a SONOS floating gate by programming an erasing, which modifies the threshold voltage (V_{th}) of the MOSFET, and thus varying the V_{t1} . The following equation describes the V_{th} variation behavior by charging and erasing:

$$\Delta V_{th} = -\frac{Q_N}{A} \cdot \frac{\tau_{TOP}}{\epsilon_{ox}} - \frac{1}{\epsilon_N} \int_0^{\tau_N} x \cdot q(x) dx = -\frac{Q_N}{A} \left(\frac{\tau_{TOP}}{\epsilon_{ox}} + \frac{X_C}{\epsilon_N} \right) \quad (4)$$

Where Q_N is the trapped charge in the floating gate layer, X_C is the centroid position, $q(x)$ is the charge density in nitride, ϵ_{ox} and ϵ_N are permittivity of SiO_2 and Si_3N_4 , respectively. τ_{TOP} and τ_N are thickness of top oxide and nitride [103].



(a)



(b)

Figure 2.2.3 Conceptual SONOS ESD protection. (a) Cross-section. (b) Bandgap diagrams under fresh, programming and erasing conditions.

Both channel hot electron (CHE) and Fowler-Nordheim (FN) programming can be used. The ESD V_{t1} programmability utilizes the tunneling-assist ESD triggering mechanism in SONOS enabled by gate programming and erasing. In practice, designer can also add a trigger-assisting circuit block on chip to change the gate bias (V_G), thus alter the channel status in an ESD event, and further modify the ESD V_{t1} . Smiliar to the NC-QD ESD protection, SONOS ESD protection can also be used in two main schemes. In scheme 1, an SONOS ESD protection device is triggered by ESD pulse and then driven into snapback region. In scheme 2, a SONOS device can be turned on by V_G to discharge

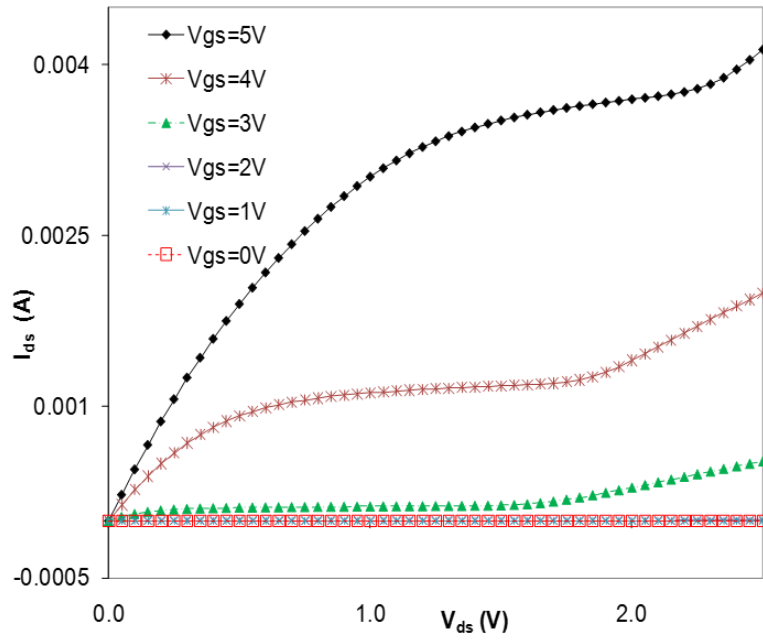
ESD surges in a nonsnapback saturation conduction mode, which has the advantage of allowing SPICE circuit simulation of the whole chip including ESD protection behaviors.

2.2.1.3 Measurements and Discussions

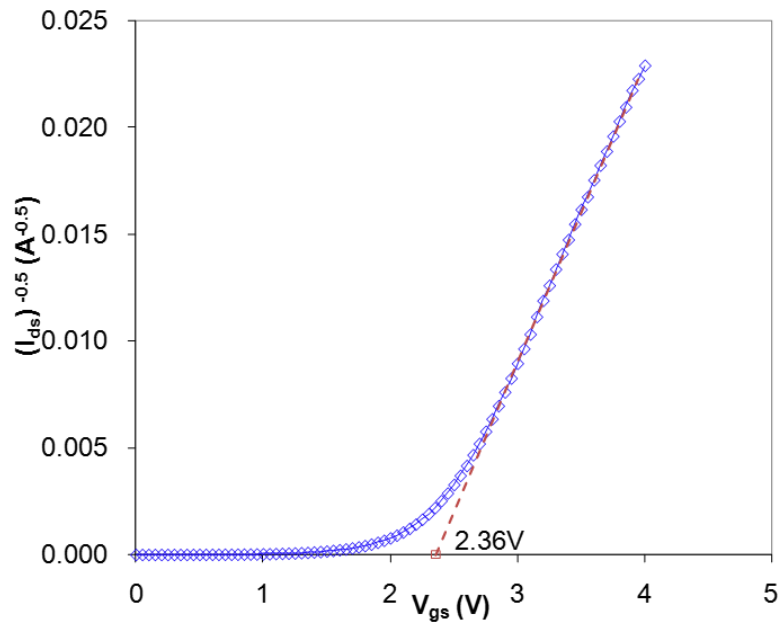
2.2.1.3.1 NC-QD ESD Protection Structure

NC-QD ESD protection structures of varying design matrix were fabricated in a CMOS-compatible process for heterogeneous integration. A 5nm tunneling oxide is grown on Si at 850°C, followed by Si NC dots deposited by LPCVD at 600°C. A 1nm cobalt film is then deposited and annealed to form CoSi₂. Unreacted Co is etched off, resulting in CoSi₂-coated NCQD array, covered by 20nm control oxide. The NC dot size is 10nm with a dot density of $4 \times 10^{11} \text{ cm}^{-2}$.

Both DC and TLP test were conducted. Typical NCQD programming requires $V_G \approx 20\text{V}$ for 5s and 50% duty cycle to charge the NCQD array. Figure 2.2.4 gives the DC measured $I_{DS} \sim V_{DS}$ and $\sqrt{I_{DS}} \sim V_{GS}$ curves for sample NCQD ESD protection devices for $L=1\mu\text{m}/W=100\mu\text{m}$ confirming the normal MOSFET I-V characteristics. The V_{th} values were extracted, which clearly shows the expected shift, from 2.36 to 3.46 V, before and after the programming process.



(a)



(b)

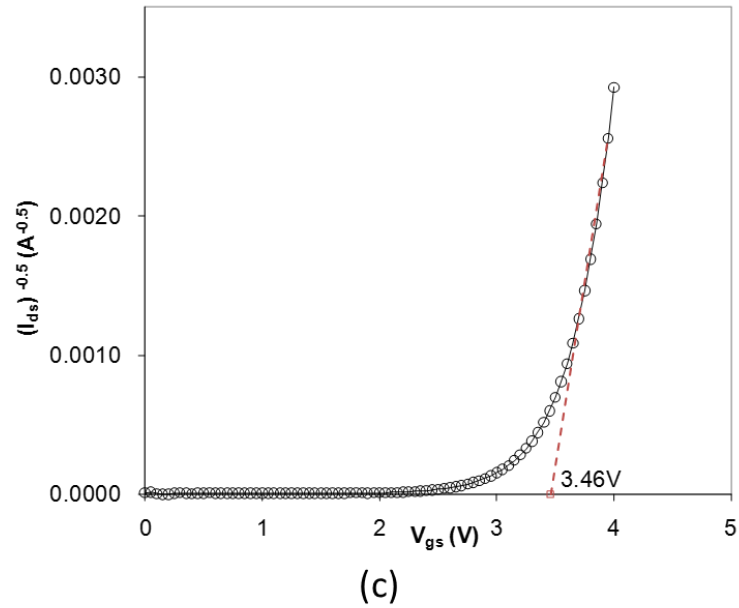


Figure 2.2.4 Measured DC I-V characteristics for NCQD ESD protection show the shift of threshold voltage by programming. (a) $I_{DS} \sim V_{DS}$ before programming. (b) $\sqrt{I_{DS}} \sim V_{GS}$ before programming. (c) $\sqrt{I_{DS}} \sim V_{GS}$ after programming.

Figure 2.2.5 and 2.2.6 show TLP results ($t_r=10\text{ns}$) under varying gate bias before and after programming. The extracted V_{t1} and V_h are summarized in Table 2.2.1 and $\Delta V_{t1} \sim \Delta V_G$ is illustrated in Figure 2.2.7. From Figure 2.2.5 and 2.2.6, it is observed that at lower V_G , the typical snapback I-V behavior occurs and when V_G increases to a certain level, V_{t1} is substantially reduced and results a non-snapback conduction. Our previous mechanism is confirmed that by varying V_G , we could obtain altered V_{th} . And we also observed that the non-snapback I-V characteristic occurs at $V_G=3\text{V}$ before programming and $V_G=4\text{V}$ after programming, which confirms that by programming, V_{t1} is changed accordingly.

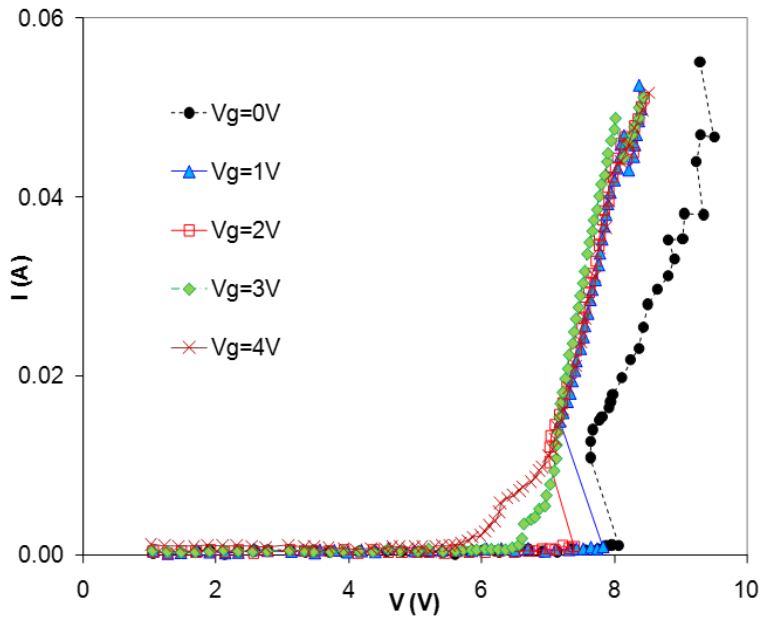


Figure 2.2.5 Measured ESD discharging I-V characteristics for the same sample by TLP before programming shows the desired ESD triggering variation, ΔV_{t1} , at different gate biasing V_G .

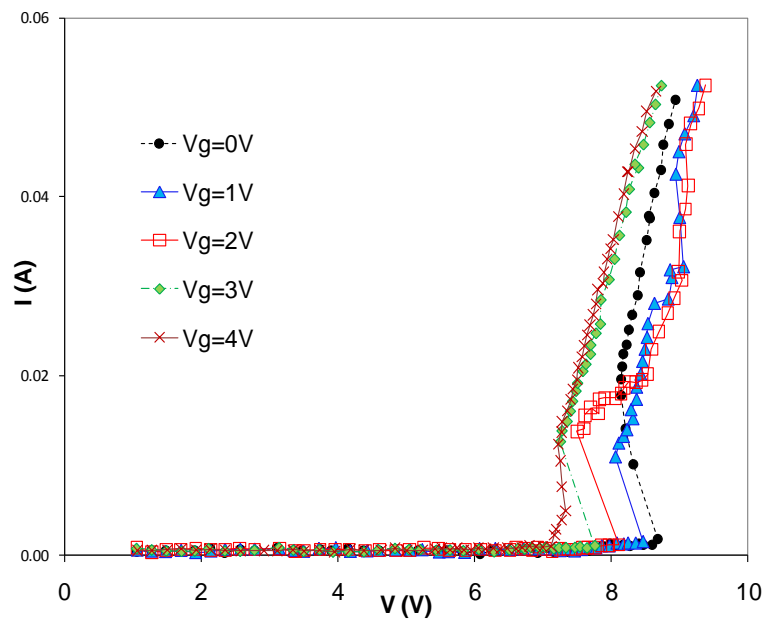


Figure 2.2.6 Measured ESD discharging I-V characteristics for the same sample by TLP after programming shows the desired ESD triggering variation, ΔV_{t1} , at different gate biasing V_G .

Table 2.2.1 V_{t1} and V_h for sample NCQD ESD protection structures at different gate biasing V_G by TLP.

	V_G (V)	0	1	2	3	4
Before Prog.	V_{t1} (V)	8.06	7.82	7.39	6.46	5.6
	V_h (V)	7.64	7.17	7.02		
After Prog.	V_{t1} (V)	8.68	8.11	7.76	7.12	6.29
	V_h (V)	8.06	7.5	7.25	7.22	

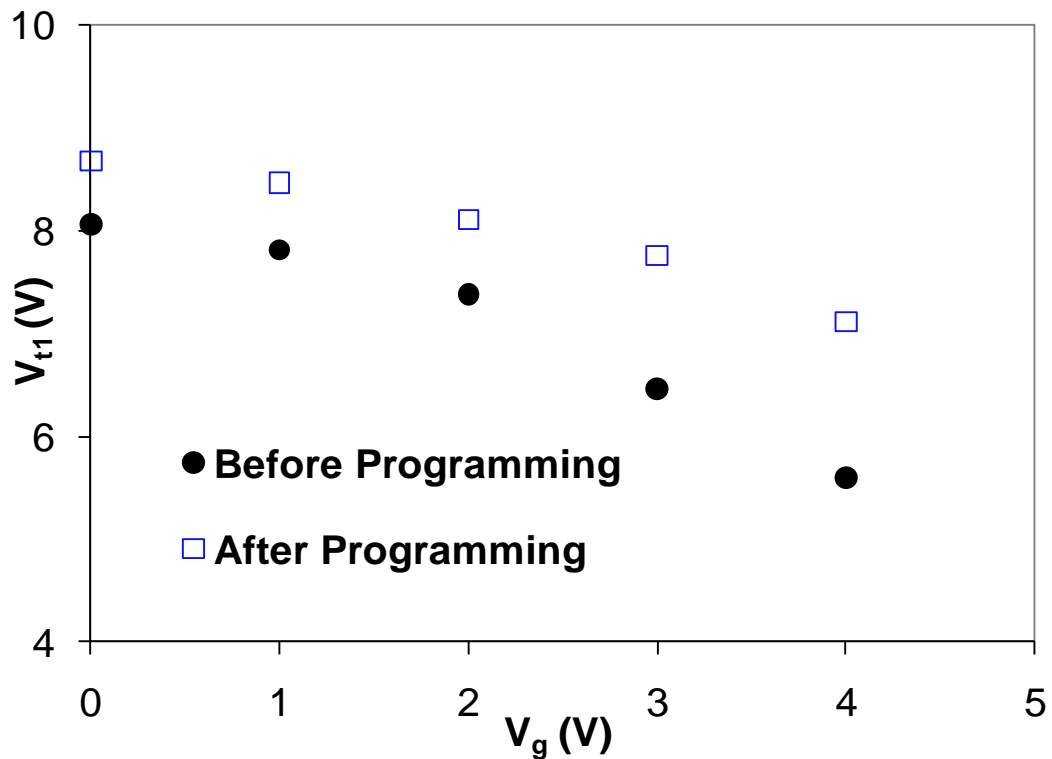


Figure 2.2.7 Measured $V_{t1} \sim V_G$ curves.

Figure 2.2.8 shows TLP test for an $L=2\mu\text{m}/W=100\mu\text{m}$ ggNMOS type NCQD ESD structure before and after programming. Very fast (VF)-TLP was conducted to examine the NCQD ESD protection structure response to ultrafast CDM surges. In Figure 2.2.9, I-V characteristic and leakage for an $L=1\mu\text{m}/W=1\mu\text{m}$ device featuring a ultrafast ESD

surge with $t_r=100\text{ps}$ and $t_d=1\text{nS}$, clearly, the device has a potential to react to a very fast ESD transient while achieving a very low leakage current of $I_{\text{leak}}\sim 14.6\text{pA}$ at a bias of 0.5V . Figure 2.2.10 and 2.2.11 present the full transient ESD discharging I-V curves for a sample $L=1\mu\text{m}/W=10\mu\text{m}$ structure by TLP and VF-TLP, respectively, which show the thermal breakdown threshold (I_{t2}) for the new structures. The achieved robustness levels are $I_{t2}\approx 25\text{mA}/\mu\text{m}$ for HBM and $I_{t2}\approx 400\text{mA}/\mu\text{m}$ for CDM ESD protection. The results strongly suggest that the new NCQD ESD protection structures may potentially be the first field-programmable on-chip ESD protection solution to complex mixed-signal ICs down to the nano nodes and shall allow fine-tune of ESD triggering in the electronic systems in post-Si design.

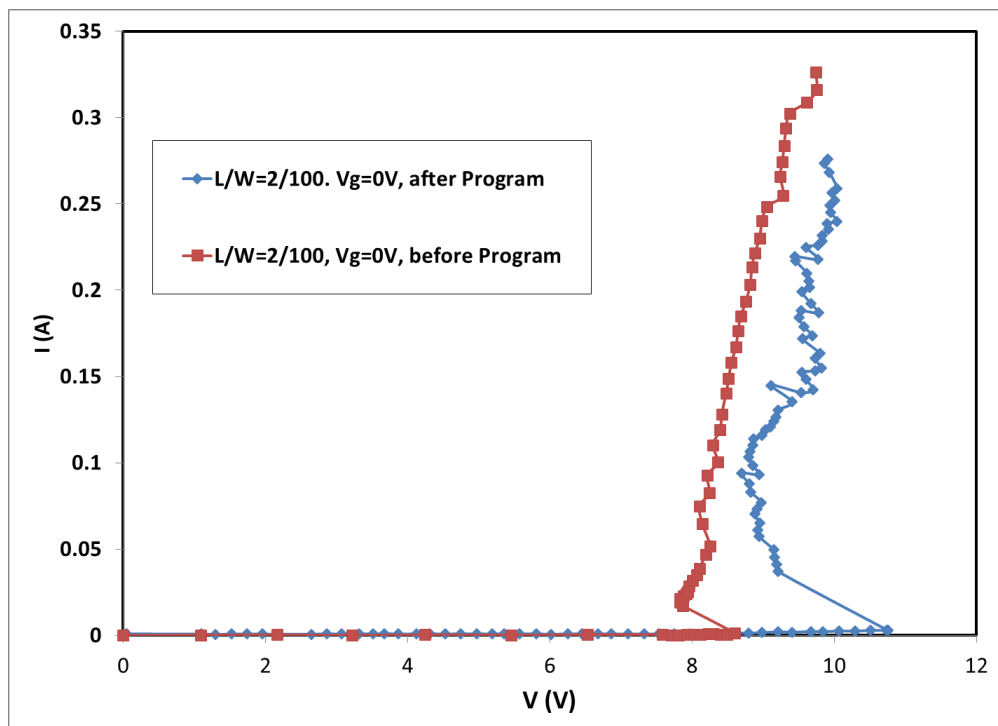


Figure 2.2.8 Measured I-V curves for a $W/L=100\mu\text{m}/1\mu\text{m}$ NCQD ESD structure in ggNMOS format before and after programming shows a ΔV_{t1} of $\sim 2\text{V}$.

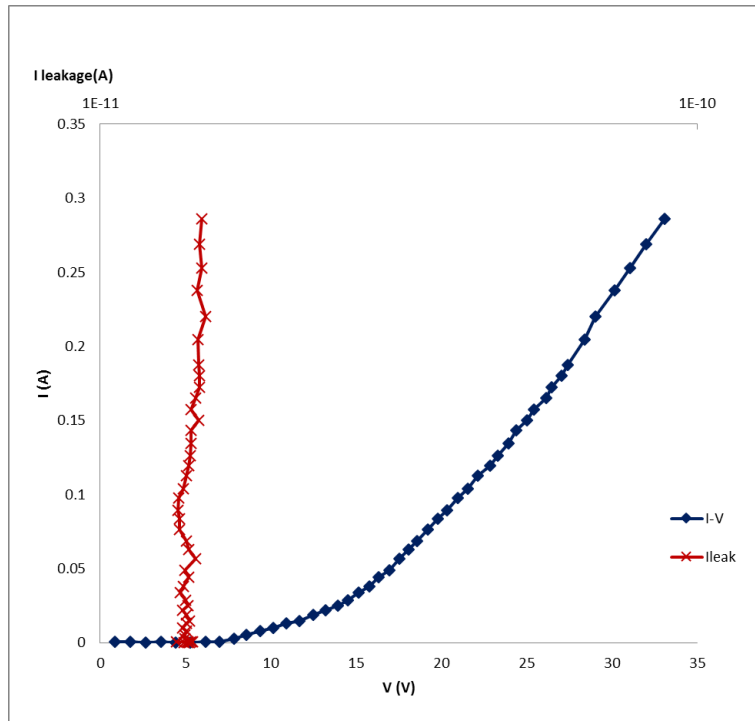


Figure 2.2.9 Measured I-V curves for a W/L=1 μ m/1 μ m NCQD ESD structure by VF-TLP shows very fast ESD discharging response time of 100pS and very low leakage \sim pA.

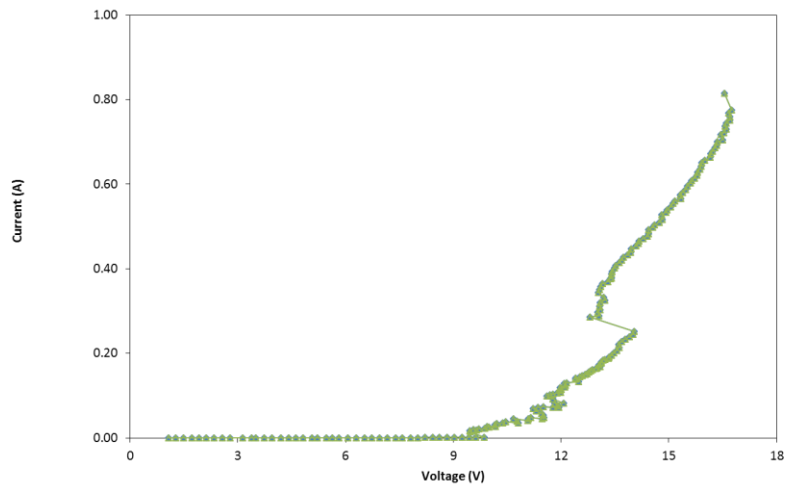


Figure 2.2.10 Measured full transient I-V curves for a W/L=1 μ m/10 μ m NCQD ESD structure by TLP shows its I_2 .

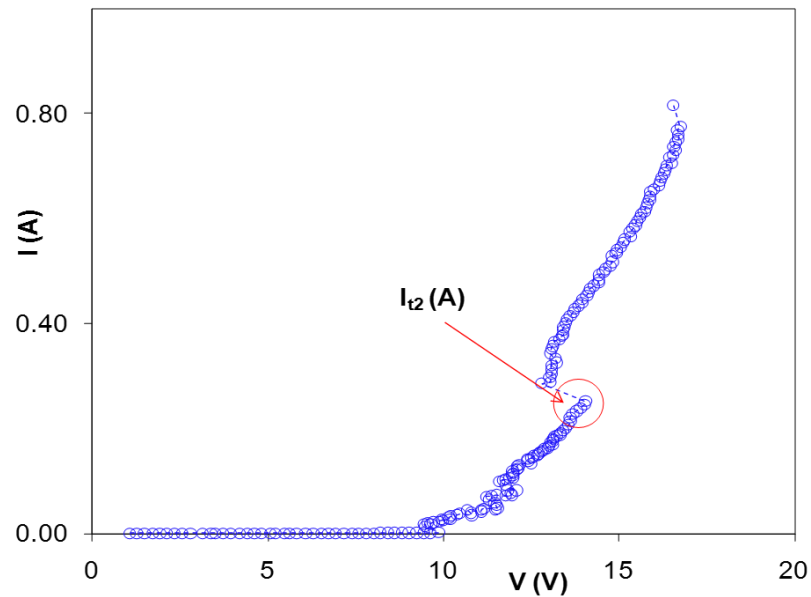
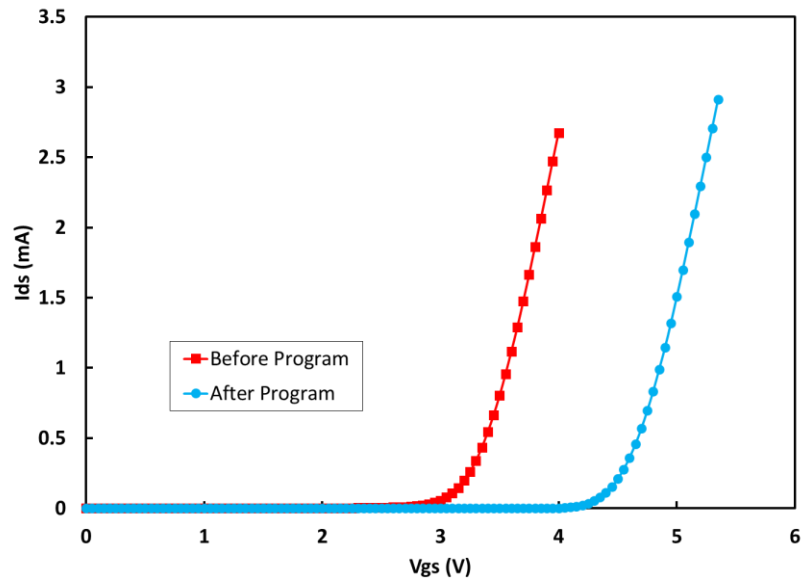


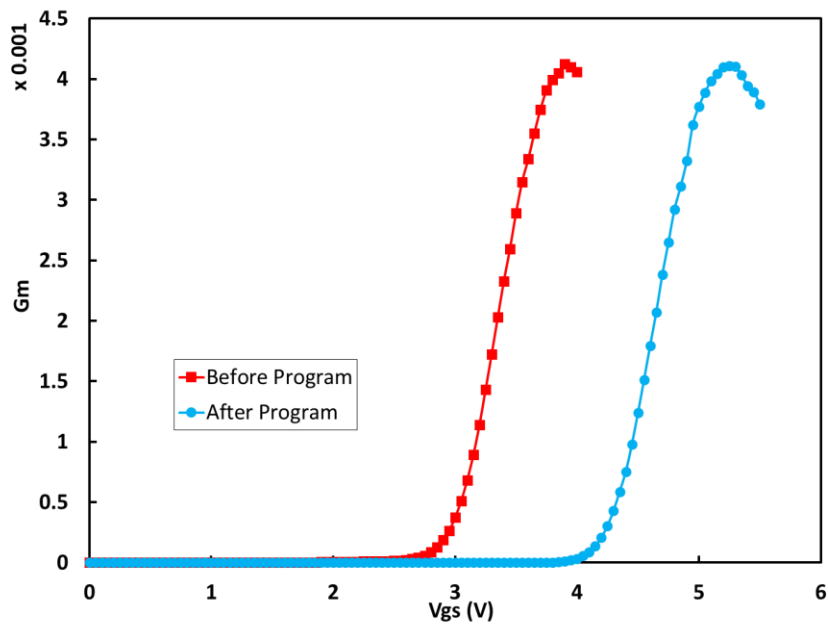
Figure 2.2.11 Measured full transient I-V curves for a W/L=1 μ m/10 μ m NCQD ESD structure by VF-TLP shows its I_{t2} .

2.2.1.3.2 SONOS ESD Protection Structure

New SONOS ESD protection structures were fabricated in a 130nm 1-poly/4-metal CMOS logic process. The ONO thickness is 14nm. An additional step is added to generate ONO floating-gate layer before normal gate oxidation. Figure 2.2.12 shows the measured I_{DS} - V_{GS} and G_m - V_{GS} curves for a sample SONOS ESD protection structure (L=0.18 μ m/W=50 μ m). A ΔV_{th} =1.17V was obtained after programming.



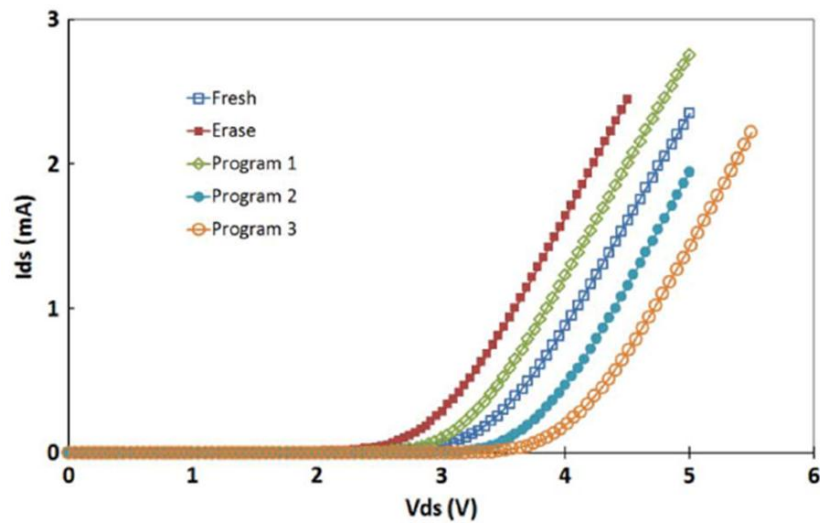
(a)



(b)

Figure 2.2.12 Measured (a) $I_{DS} \sim V_{GS}$ before programming. (b) $G_m \sim V_{GS}$ for a sample $W/L=50\mu\text{m}/0.18\mu\text{m}$ SONOS ESD structure by DC testing show ΔV_{th} by programming (17V, 2ms programming pulse at gate).

TLP testing for SONOS ESD structures were conducted. Figure 2.2.13 shows the measured ESD discharging I-V curves and DC testing for a ggNMOS type SONOS ESD protection structure of $L=0.15\mu\text{m}/W=10\mu\text{m}$ with the results summarized in Table 2.2.2. The testing step was first fresh, followed by deep erasing, and then multi-step gradual programming. It clearly shows the erasing process reduces the V_{t1} and programming increases V_{t1} as expected. And Figure 2.2.14 shows the I-V curve under the reverse sequence for a device of $L=0.16\mu\text{m}/W=10\mu\text{m}$, first with fresh device, then deep programming and multi-step gradual erasing, with the results shown in Table 2.2.3. Together with Table 2.2.2, reveals a clearly $V_{t1}\sim$ programming trend. Figure 2.2.15 shows monolithic $V_{t1}\sim V_{th}$ relationship by programming, which is attributed to the tunneling effect.



(a)

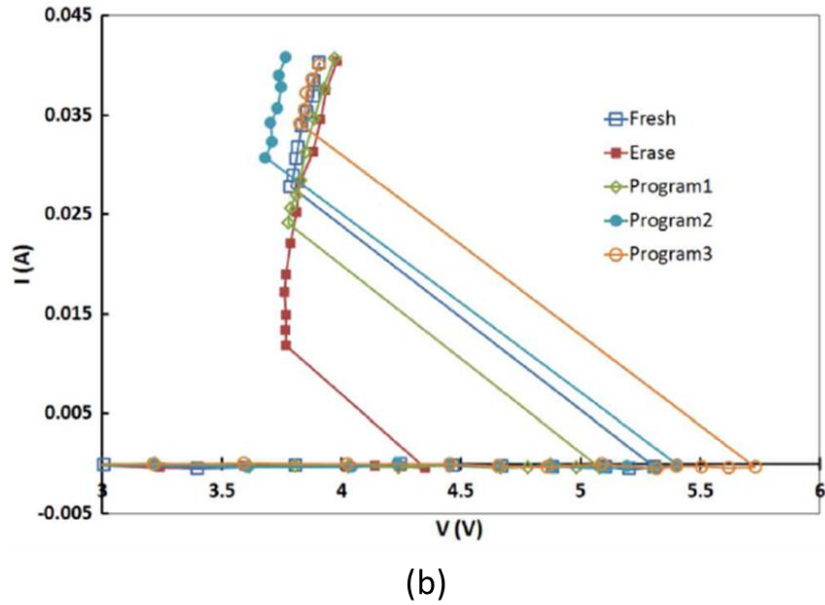
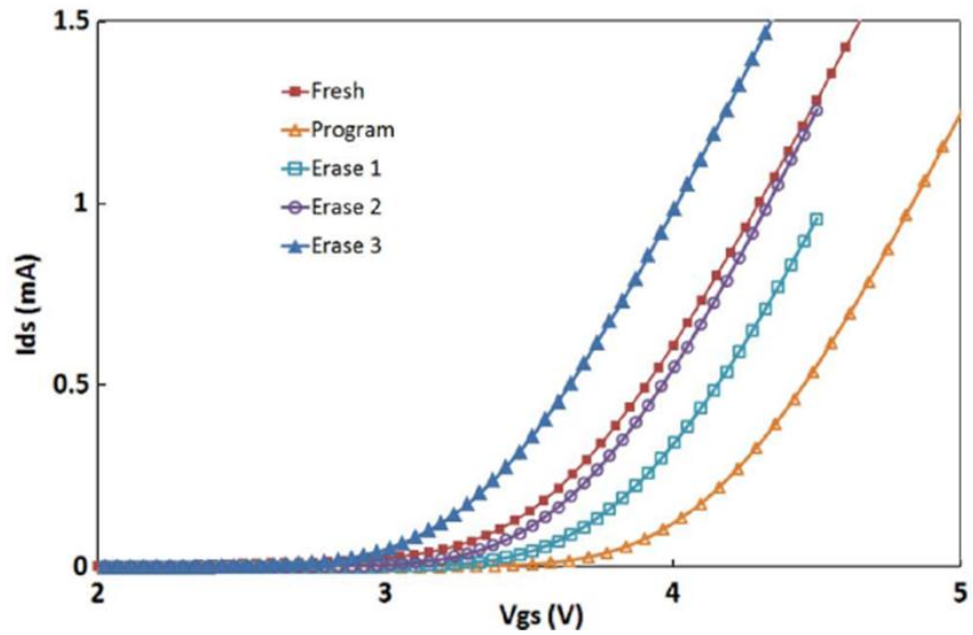


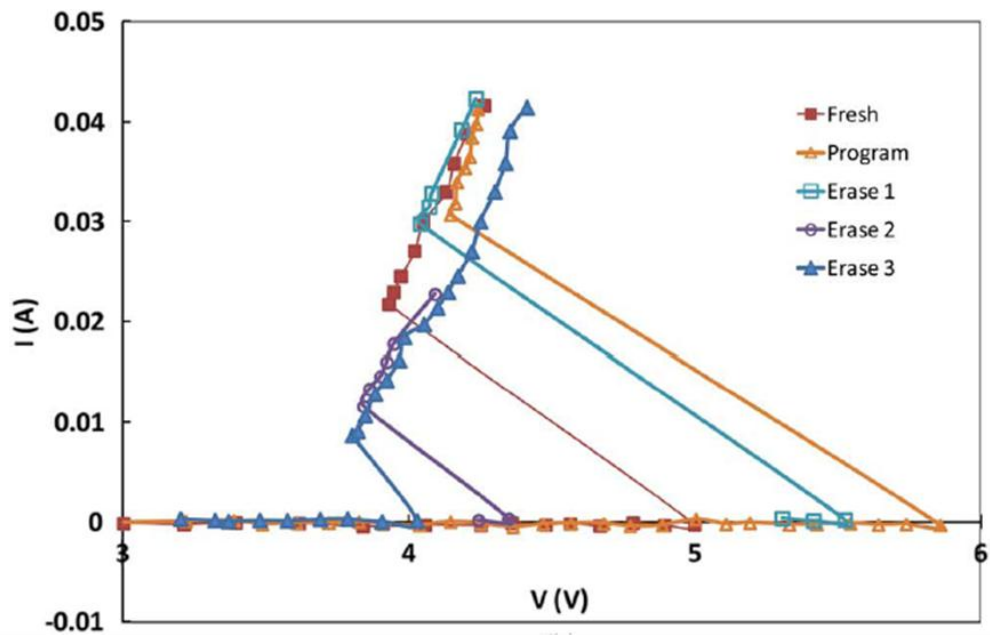
Figure 2.2.13 Measured I-V curves for a sample SONOS ESD structure, from fresh to one-step erase followed by multi-step programming, show ΔV_{th} and ESD triggering ΔV_{th} as designed. (a) DC testing. (b) TLP transient testing.

Table 2.2.2 Erasing/Programming Results for a W10 μ m/L0.15 μ m SONOS-based ESD Protection Structure.

ACTIONS	Conditions	$V_{TH}(V)$	$V_{TI}(V)$
Fresh	N/A	2.92	5.31
Erase	$V_{gs}=-10V$	2.44	4.35
Program-1	$V_{gs}=6.5V, V_{ds}=4V$	2.71	5.08
Program-2	$V_{gs}=7V, V_{ds}=4V$	2.98	5.33
Program-3	$V_{gs}=7.5V, V_{ds}=4V$	3.24	5.40
Program-4	$V_{gs}=8V, V_{ds}=4V$	3.52	5.73



(a)



(b)

Figure 2.2.14 Measured I-V curves for a sample SONOS ESD structure, from fresh to one-step program followed by multi-step erasing, show ΔV_{th} and ESD triggering ΔV_{th} as designed. (a) DC testing. (b) TLP transient testing.

Table 2.2.3 Programming/Erasing Results for a W10 μ m/L0.16 μ m SONOS-based ESD Protection Structure.

ACTIONS	Conditions (10mS)	V_{TH} (V)	V_{TI} (V)
Fresh	N/A	3.10	5.00
Program	$V_{gs}=V_{gd}=17V$	3.63	5.86
Erase-1	$V_{gs}=-7V, V_{ds}=4V$	3.36	5.53
Erase-2	$V_{gs}=-8V, V_{ds}=4V$	3.18	4.35
Erase-3	$V_{gs}=-9V, V_{ds}=4V$	3.02	4.25
Erase-4	$V_{gs}=-10V, V_{ds}=4V$	2.92	4.13
Erase-5	$V_{gs}=-11V, V_{ds}=4V$	2.85	4.03

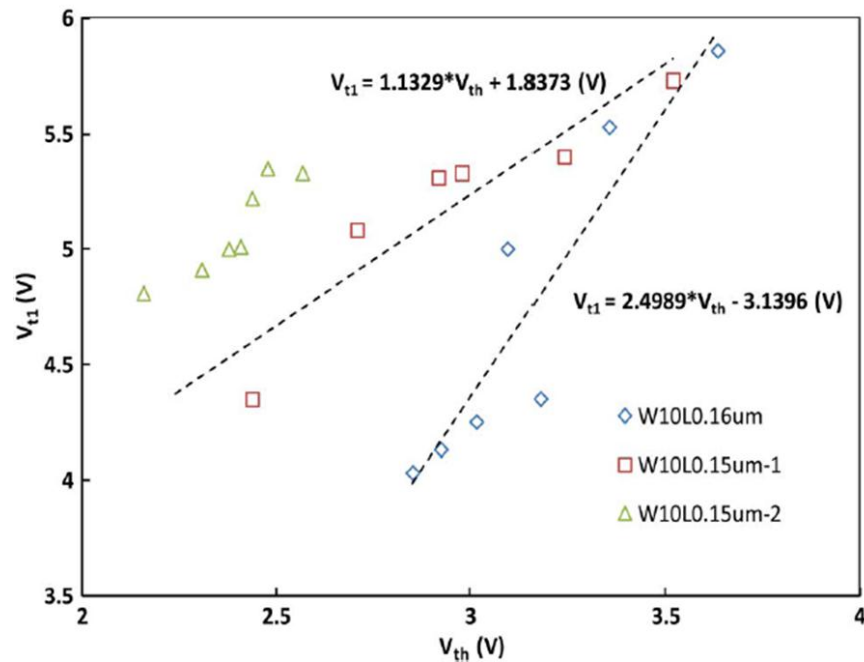


Figure 2.2.15 TLP testing shows the $V_{ti} \sim V_{th}$ monolithic variation trends by field programming, depicted by a fitting model.

Figure 2.2.16 shows the complete I-V and leakage by TLP testing for sample SONOS ESD protection structures ($L=0.18\mu\text{m}/W=10\mu\text{m}$). The measured SONOS ESD protection device achieved ultra-low leakage $<1.2\text{pA}$. Figure 2.2.17 shows the channel length of SONOS ESD structure also affects the ESD V_{t1} due to change in the electrical field and the punch-through effect. The measured sample SONOS ESD protection structures survived ESD transients of $I_{t2}\sim 94.9/96/102\text{mA}$, translating into the ESD protection capability of $\sim 14\text{V}/\mu\text{m}$. Figure 2.2.18 shows the temperature dependence of V_{t1} and V_{th} measured at $T=-50^\circ\text{C}/+100^\circ\text{C}$. A sizable $\Delta V_{t1}\sim 2\text{V}$ was obtained for the SONOS ESD structures by moderate field programming. Wider ΔV_{t1} tuning range may be achieved by design optimizations, including substrate doping profile and increasing both the thickness and number of mid-nitride layers.

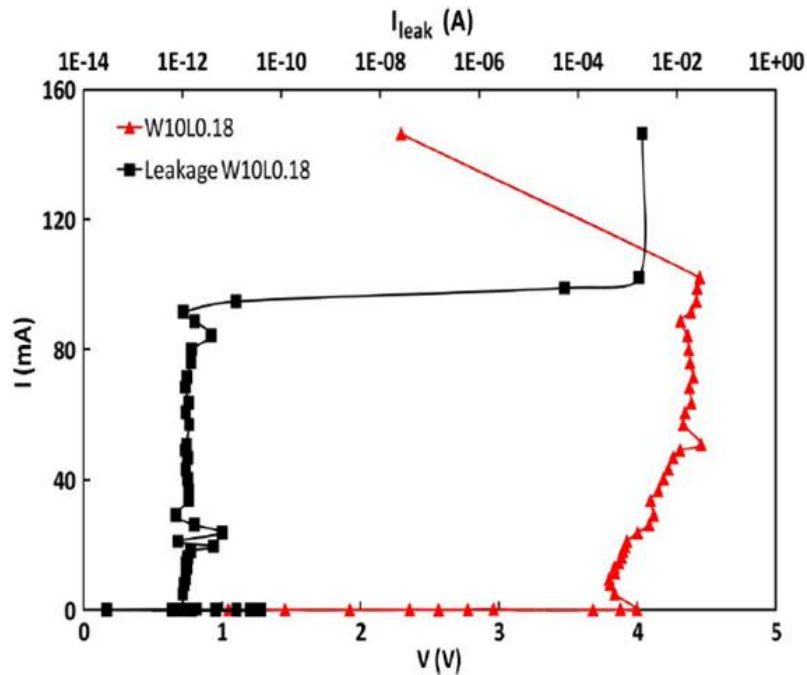


Figure 2.2.16 Measured full ESD I-V curve for a sample SONOS ESD structure by TLP shows the ESD I_{t2} and ultralow leakage I_{leak} .

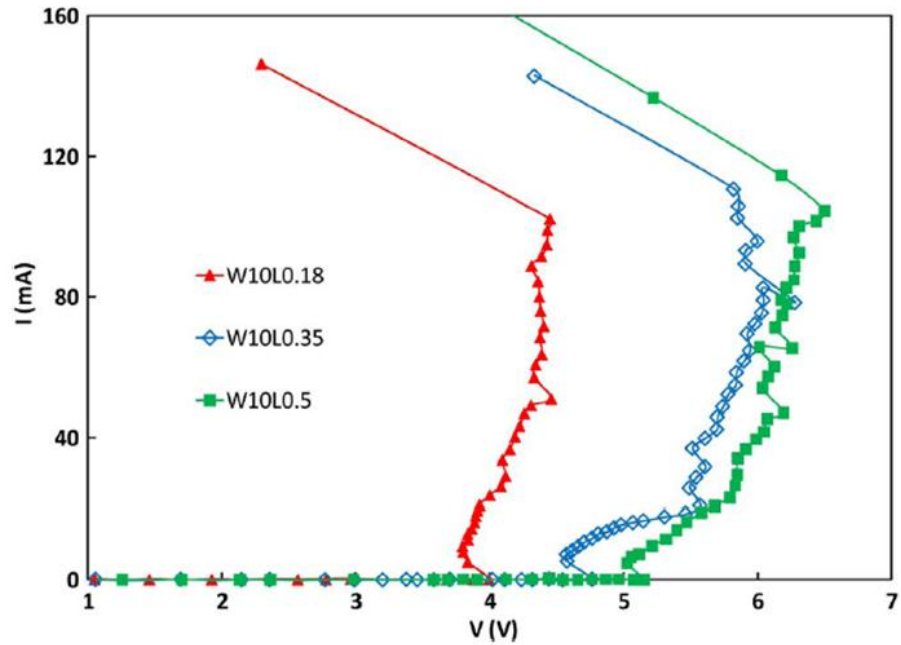


Figure 2.2.17 TLP testing of sample SONOS ESD structure shows clear influence of the channel length L on the ESD V_{t1} .

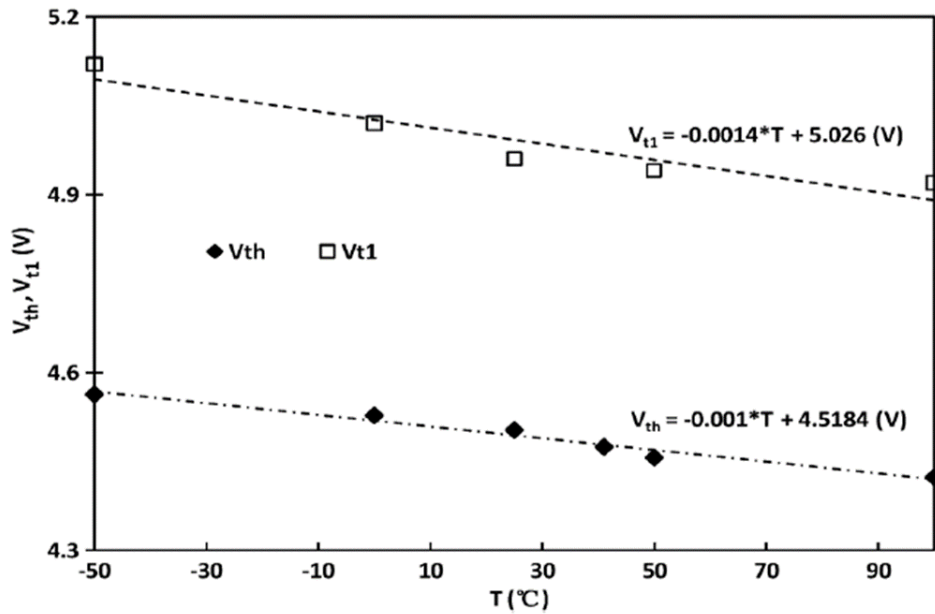


Figure 2.2.18 TLP testing of sample SONOS ESD structure shows clear influence of the channel length L on the ESD V_{t1} .

2.2.1.4 Conclusion

Two novel programmable ESD protection mechanisms and experimental results for complex mixed-signal ICs are reported. The new NCQD and SONOS-based ESD protection structures utilize tunneling-assist ESD triggering mechanisms to achieve programmable ESD ΔV_{t1} . Prototype designs fabricated in CMOS-compatible processes demonstrated full programmable- V_{t1} ESD operation. Sample NCQD and SONOS ESD protection structures achieve a wide ΔV_{t1} of $\sim 2V$, ultra-low leakage of $I_{leak} \sim 1.2pA$, ESD protection capacity of $>25V/\mu m$ for HBM and $\sim 400mA/\mu m$ for CDM. Several whole-chip programmable ESD protection circuit design schemes are proposed.

2.2.2 Dual-Direction Nanocrossbar Array ESD Protection Structures

2.2.2.1 Introduction

Low-leakage robust ESD protection design is a compelling reliability design challenge as IC technologies advance into sub-45nm regime. Traditional ESD protection has inherent problems associated with the conventional p-n junction structures, including unbearable ESD-induced leakage current (I_{leak}) and mistripping effect [77][104]. In addition, ESD discharging uniformity has always been a physical design challenge for whole-chip ESD protection designs. Novel non-PN-junction-triggering ESD protection mechanism is considered the future solution. We recently demonstrated a non-traditional nano crossbar phase switching ESD protection concept [105]. Previous reported phase switching memory structures cannot handle large ESD surge [106-113]. This paper

reports design and analysis of a novel dual-directional nano crossbar array ESD protection structure achieving ultra-low leakage, fast response, good uniformity and robust ESD protection in CMOS flows.

2.2.2.2 Nanocrossbar Array ESD Protection

Figure 2.2.19 shows the new dual-direction nanocrossbar array ESD protection structure, including a single-node nanocrossbar (a), a 5×5 nanocrossbar array ESD device (b), its cross-section (c), and its typical on-chip ESD protection scheme (d). The new nanocrossbar array consists of a Cu electrode (anode), a W/Cu back contact (cathode), and a unique nano-phase-switching dielectric in between. The dielectric layer eliminates ESD I_{leak} and possible mistriggering effect seen in p-n type devices. When the ESD surge comes, the large transient electric field instantly triggers nano-phase switching for ESD to discharge. It turns off after the ESD event is over.

Initial results for single-node nanocrossbar ESD devices of different sizes were reported [106], which is however not suitable for several reasons: First, a small nanowire crossbar device, good for low leakage, cannot handle large ESD surge. Second, if a large nanocrossbar area is used, it might suffer from non-uniformity, more leakage and slower ESD triggering. Third, too large a crossbar area might corrupt the new nano-phase switching ESD discharging mechanism. To address these problems, we devised new nanocrossbar array ESD structures where the small nano crossbar area ensures ultra-low I_{leak} and fast ESD triggering, while a large array structure allows robust ESD protection, uniform ESD discharging and fast nano-switching ESD triggering. The array structures

are also layout-friendly in practical IC designs.

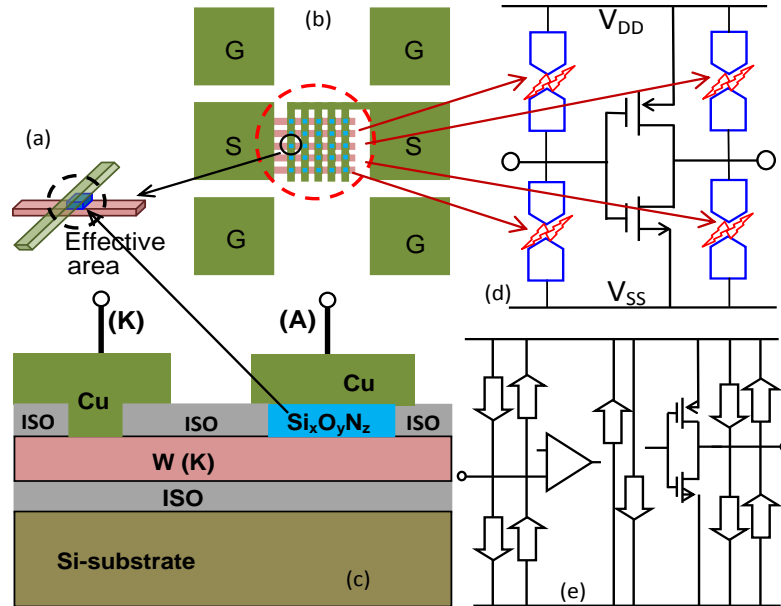


Figure 2.2.19 Nano crossbar array ESD concept: (a) single-node device, (b) 5x5 array device, (c) cross-section, (d) new on-chip ESD circuit scheme, (e) ESD protection using traditional single-polarity ESD devices. (ESD=symbols)

2.2.2.3 Experiments and Discussions

A CMOS-compatible flow was developed, a 100nm W layer was deposited on SiO₂/Si substrate. Lithography and RIE etching defined electrode K. A 50nm Si_xO_yN_z layer was then deposited by PECVD and tuned by reactive gas ratio of N₂O/SiH₄. Via is formed as bottom connection. Then, Cu was deposited by PVD followed by lift-off. A large group of nanocrossbar array ESD devices was fabricated with the design split matrix summarized in Table 2.2.4, including nanocrossbar insulator type, composition and thickness, node dimension, and array size. Pt was also used to compare with Cu. Figure 2.2.20 shows the expected nano phase switching predicted by TCAD simulation, which is explained by our new dispersed local ESD tunneling

(ESD-DLT) model. The $\text{Si}_x\text{O}_y\text{N}_z$ film is annealed at low temperature to prediffuse the disperse Cu (or Pt) ions into the dielectric where Cu is trapped by O/N atoms, but remains off. An ESD surge causes local electron tunneling between neighbor Cu ions dispersed throughout $\text{Si}_x\text{O}_y\text{N}_z$, resulting in low- R_{on} ESD discharging. After the ESD pulse, the ESD-induced tunneling stops, and the device turns off.

Table 2.2.4 Nanocrossbar ESD structure design matrix

Nano crossbar insulator media		Area(μm)		Nano crossbar array		
design matrix		Single-node ESD	1x1	Crossbar array ESD	Node	Array
Type	$\text{Si}_x\text{O}_y\text{N}_z$		2x2		area (μm)	ESD size
Thick-ness	50nm		5x5			
	20nm		10x10		2x2	8x8
Media	1:0.95:0.54		20x20		5x5	5x5
ratios	1:0.42:0.39		40x40		10x10	3x3
	1:1.93:0.08		60x60		20x20	2x2
Top metal	Cu (bottom W/Cu)		80x80			
	Pt (bottom W/Pt)					

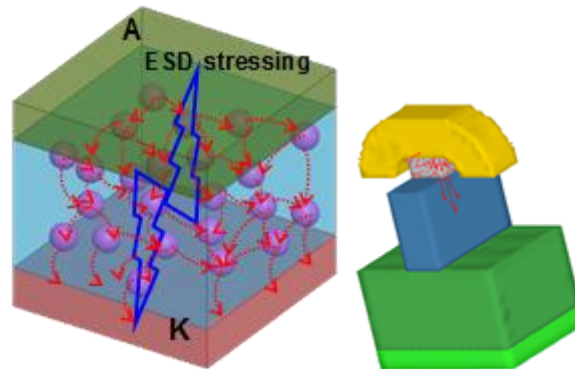


Figure 2.2.20 Nano crossbar array ESD discharging effect by simulation (Right) and the new dispersed local ESD tunneling model (Left).

Figure 2.2.21 shows the measured transient ESD I-V by TLP and VF-TLP for single-node devices. Figure 2.2.22 and 2.2.23 show ESD I-V curves for single-node and array (5×5) nanocrossbar ESD device ($5 \mu\text{m} \times 5 \mu\text{m}$ node area) by TLP testing. It is observed that a single-node ESD device has one single ESD triggering point, while for array, feature

multiple ESD triggering points, proportional to the array size, because local ESD tunneling may trigger the nanocrossbar nodes one by one sequentially per the new ESD-DLT model.

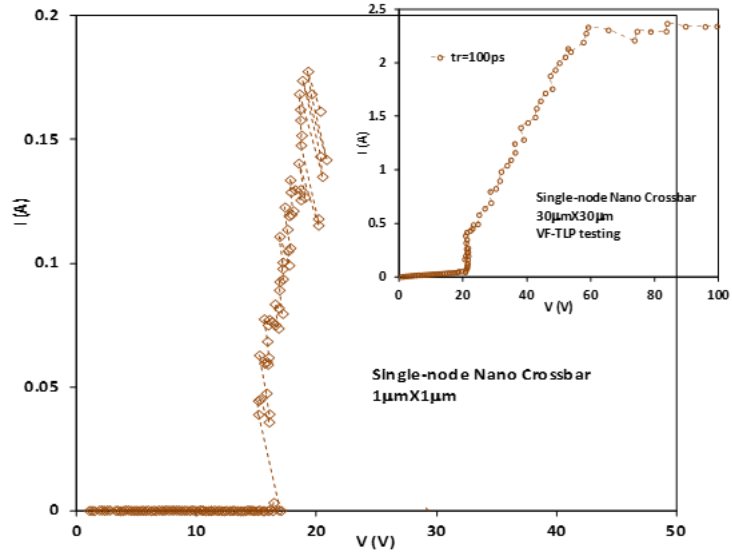


Figure 2.2.21 Measured I-V curves for different ESD devices by TLP (rising time $t_r \sim 10\text{nS}$, duration $t_d \sim 100\text{nS}$) and VF-TLP ($t_r \sim 100\text{pS}$, $t_d \sim 1\text{nS}$, Inset).

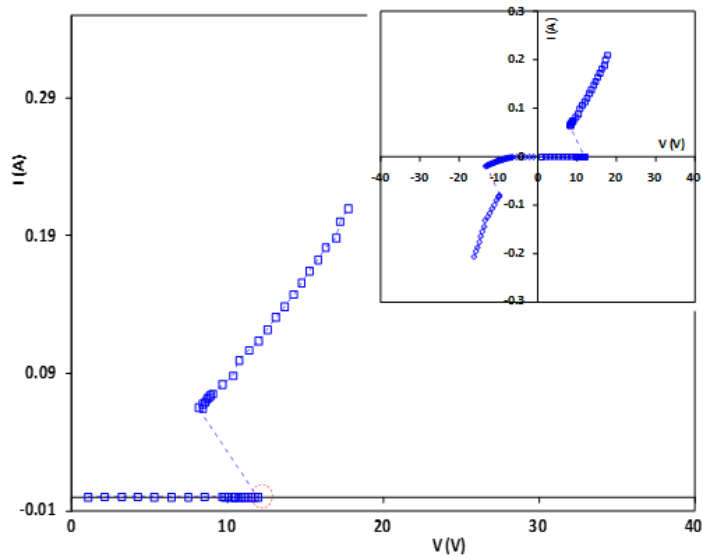


Figure 2.2.22 Measured I-V curve by TLP for single-node $5\mu\text{m} \times 5\mu\text{m}$ nanocrossbar ESD devices. The inset shows its dual-directional ESD discharging curve.

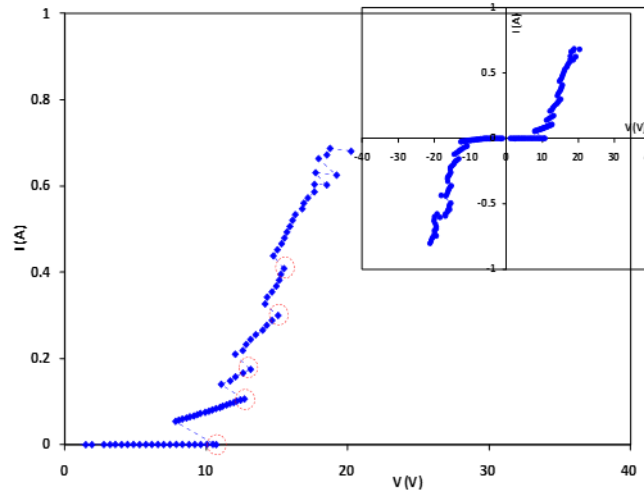


Figure 2.2.23 Measured I-V curve by TLP for $5\mu\text{m}\times 5\mu\text{m}$ 5×5 nanocrossbar array ESD devices. The inset shows its dual-directional ESD discharging curve.

Figure 2.2.24 shows that new ESD device have ultra-low leakage of $I_{\text{leak}} < 2\text{pA}$, measured at 0.1-3.3V. The new ESD-DLT model is different from the phase changing memory model (filament) reported because of the following: 1) It may be triggered by very fast ESD pulses of $t_r \sim 100\text{pS}$ (versus $\sim 5\text{-}50\text{ns}$ in phase changing memories), and 2) it features monotonic R_{on} against device sizes (Figure 2.2.25; versus a fixed R_{on} in memories due to limited numbers of conducting filaments) [107-113]. Figure 2.2.26 shows the measured ESD triggering voltage (V_{tl}) for various prototype nanocrossbar ESD devices with different design splits, showing a wide tunable ΔV_{tl} of 1.26-28.3V controlled by device design parameters such as $\text{Si}_x\text{O}_y\text{N}_z$ ratio and thickness. Figure 2.2.27 shows a comparison of devices using Cu and Pt as contact, which reveals that Cu contact is better than Pt in both ESD V_{tl} and V_{h} due to more efficient local ESD tunneling effect associated with Cu atoms. The VF-TLP testing confirms that the new nanocrossbar array ESD devices can respond to ultra-fast ESD surge with the pulse rising time down to

100ps. Figure 2.2.22 and 2.2.23 confirms that the new nanocrossbar array ESD devices can discharge ESD pulses in both directions. This is a highly desired feature because using dual-directional ESD devices can significantly simplify whole-chip ESD protection circuit design, and reduce ESD layout area and ESD-induced parasitic effects, which has been a key problem for using typical traditional one-directional ESD devices. The prototype devices do not show perfect I-V symmetry because of asymmetrical cross-section. Good ESD I_{t2} capability was obtained for prototype devices, not shown due to validity concern of thermal resistance effect at high current, e.g., at least $I_{t2} \sim 8.11A$ observed for a 5×5 array device by TLP.

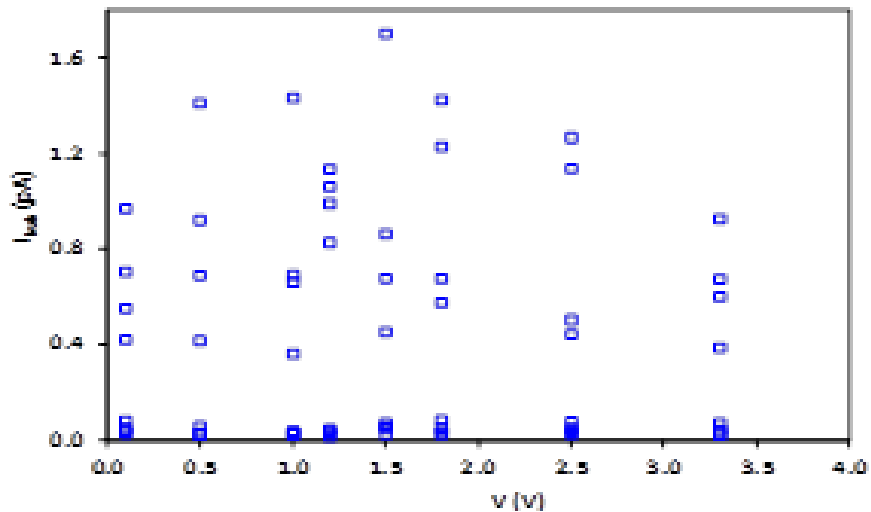


Figure 2.2.24 Measured leakages for a large group of new ESD devices at voltage bias of 0.1-3.3V shows very low leakage current down to $\sim 2pA$.

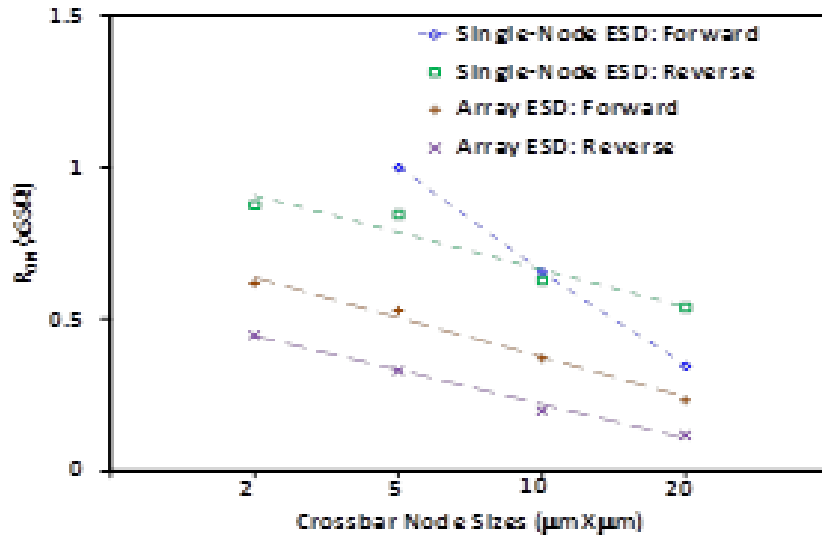


Figure 2.2.25 Measured ESD R_{ON} for new ESD devices show that as total device area increases, R_{ON} decreases monotonically, confirming the new dispersed local ESD tunneling mechanism. Traditional phase memories show a fixed R_{ON} regardless of the device size due to its fixed filament conduction model.

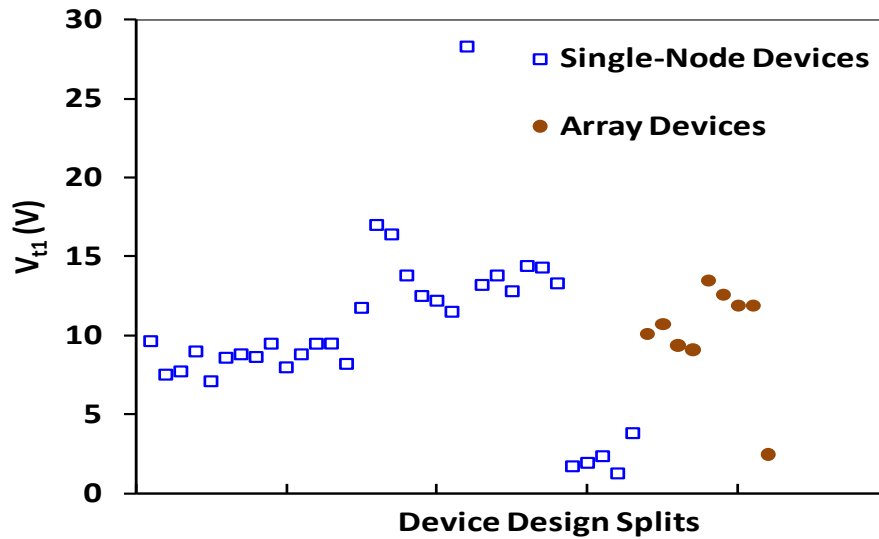


Figure 2.2.26 Testing shows wide ESD ΔV_{t1} among fabricated prototype devices with different design splits (Table 3.4). Hence, efficient ESD programmability can be readily achieved by careful physical design matrix in future.

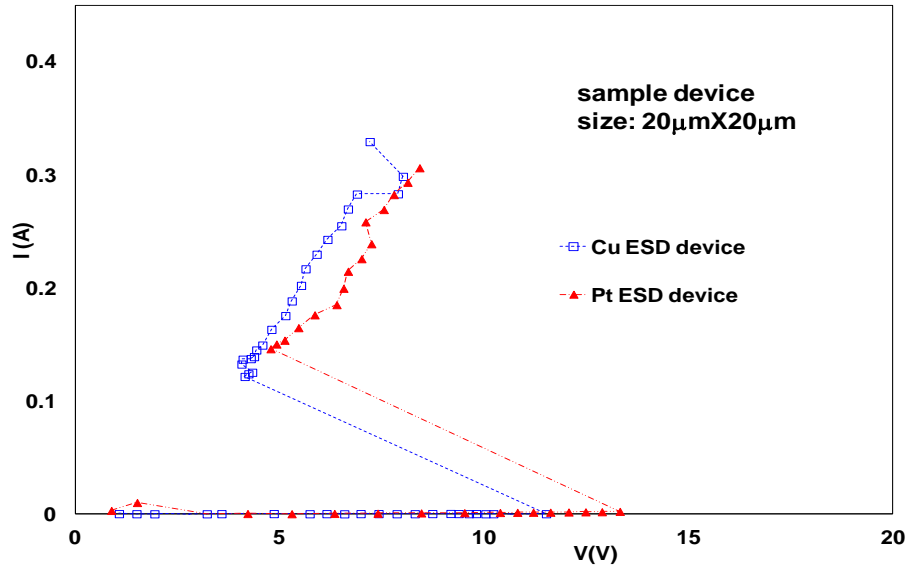


Figure 2.2.27 Cu ESD device shows lower V_{t1} and V_h than Pt device by TLP testing.

2.2.2.4 Conclusion

This section reports a new dual-directional nanocrossbar array ESD protection mechanism and functional structures. Experiment validates the new ESD concept and ESD-DLT model. Testing shows excellent ESD protection features including ultra-fast ESD response, ultra-low leakage of $<2\text{pA}$ and robust ESD protection level. This novel ESD protection concept is promising for future ICs at nano nodes.

Chapter 2.3 STI and Gated Diode ESD Protection in 28nm CMOS with Circuit Monitors

2.3.1 Introduction

ESD failure has become a major design barrier as semiconductor IC technologies advance into sub-32nm nodes. ESD protection capability, layout size and ESD-induced

parasitic effects are important design factors to consider. The popular ESD protection structures, such as, FET, SCR and diode, and their derivatives, may or may not be suitable for ESD protection at sub-32nm [77]. The key ESD design tasks are: First, accurate ESD protection design and optimization must be ensured by ESD simulation in design phase. Second, systematic ESD characterization is required to evaluate various ESD protection devices. Third, suitable ESD-protected I/O dummy monitor circuits are used to evaluate ESD protection capability and suitability for general ICs. In this work, we designed various simple diode ESD protection structures by mixed-mode ESD simulation and conducted comprehensive TLP ESD characterization for both individual ESD diodes and ESD-protected monitor circuit blocks. The goal is to provide practical design guidelines for robust ESD protection circuit design at 28nm node and beyond. ESD protection capability of about 47V/ μm , 48V/ μm and 64V/ μm are obtained for STI core, STI I/O and gated I/O diodes, respectively.

2.3.2 Diode ESD Protection in 28nm CMOS

While research is on-going to explore novel non-traditional ESD protection solutions for sub-32nm technologies [114-115], diode based ESD remains attractive to IC designers due to its capability and simplicity [116]. Based on its process features, a group of various diode ESD protection structures were designed in the 28nm CMOS in this work for comparison.

2.3.2.1 STI Core and I/O Diode ESD Structures

Shallow trench isolation (STI) is a standard feature in 28nm CMOS. STI diode can be readily designed for ESD protection. Figure 2.3.1 illustrates the cross-section of N+/P-well STI diode ESD structure designed in this work, where the N+ diffusion (Cathode) and P+/P-well diffusion (Anode) are separated by STI. In a typical on-chip ESD protection scheme, the STI diode ESD devices are used at I/O to discharge ESD surges in forward mode in combination of a power clamp structure [77]. Since STI has very short dimension, STI diode ESD structures can be made very small, hence reduce ESD-induced parasitic effects and alleviate ESD layout burden. On the negative end, with a narrow and sharp STI plug, the large ESD discharge current has to make sharp turns in conduction, resulting in severe current crowding at the bottom of a STI plug that affects ESD protection capability. This phenomenon is confirmed in simulation and testing. The foundry 28nm CMOS offers both core (0.85V) and I/O (1.8V) process modules. Accordingly, we designed STI diode ESD devices in both core and I/O processes for comparison studies.

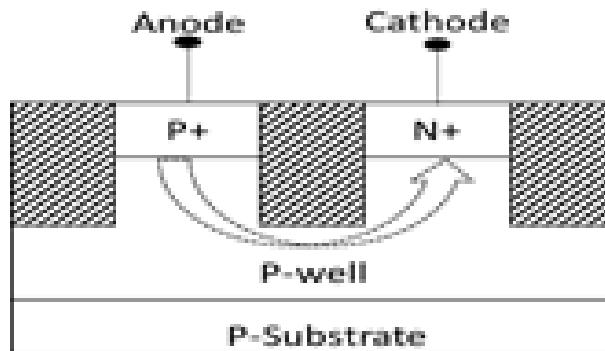


Figure 2.3.1 Cross-section and ESD discharge path for an N+/P-well STI diode ESD device. ESD current crowding at STI reduces ESD protection capability.

2.3.2.2 Poly-Gated Diode ESD Structures

Figure 2.3.2 depicts the cross-section of a gated diode ESD structure where a poly gate is used to isolate the cathode (N+) and anode (P+) instead of using a conventional STI plug. There are two main advantages for the gated-diode ESD device. First, the large ESD current can conduct straightly through the channel between the N+ and P+ without any sharp turning and current crowding as seen in an STI diode ESD device. Second, the ESD discharge is extremely short as defined by the 28nm CMOS channel. Hence, the ESD protection capability for a gated-diode ESD device shall be stronger than that of a STI diode ESD structure, which is confirmed in testing. In ESD design, the gate must be properly biased for a gated-diode ESD device in order to avoid unexpected channel turn-on in normal IC operation. Nevertheless, relatively higher leakage current may be expected for such gated-diode ESD protection devices.

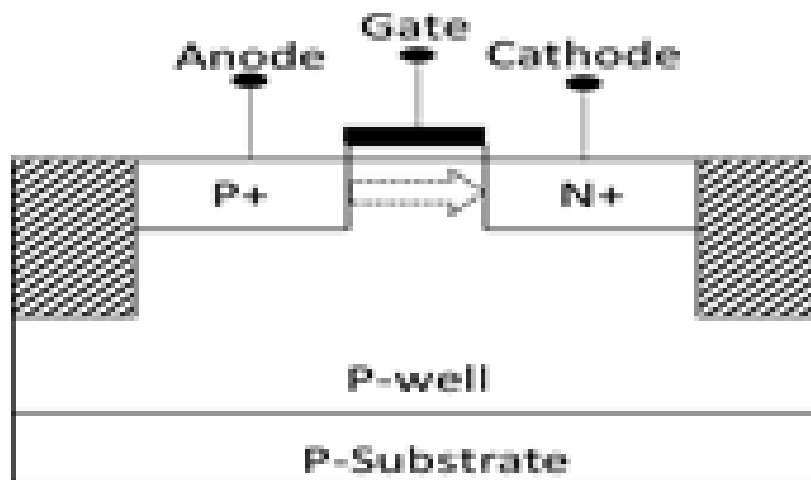


Figure 2.3.2 Cross-section and ESD current discharging path for a poly-gated diode ESD protection structure.

2.3.3 ESD Design by Mixed-Mode Simulation

2.3.3.1 Diode ESD Structure Design

Traditional trial-and-error approach should be replaced by simulation based predictive design method for ESD protection design at advanced nodes [77][114-115]. Particularly, at 28nm node, many traditional ESD design rules may not hold at all. It is essential to conduct mixed-mode ESD simulation design to fully understand the ESD behaviors inside an ESD structure, to optimize ESD performance, to minimize its parasitic effects and to predict ESD performance at chip level, which, in turn, not only ensures ESD design performance, but also reduce ESD design costs and shorten the ESD design cycles. In this work, comprehensive mixed-mode ESD simulation was conducted for individual ESD devices and I/O ESD monitor circuits in design phase. Mixed-mode ESD simulation design technique serves to accurately design the ESD devices, to explore ESD discharging current flow and heating details, to optimize ESD layout, to understand transient ESD discharging I-V behaviors, etc. [117]. Figure 2.3.3 depicts simulated cross-section, heating effect and temperature contours, and transient ESD discharging behaviors for the STI and gated diode ESD structures under the same ESD stresses. It is clearly observed that the ESD discharging current tends to crowd around the bottom of a STI plug, hence, more severe heating occurs in the STI diode than in the gated diode ESD device, which will affect ESD capability substantially. For selected ESD protection targets, ESD device sizes were selected by ESD simulation. Figure 2.3.4 shows transient ESD I-V curves for sample STI diode ESD devices with finger width of 60 μ m, 100 μ m

and 120 μm that passed 2kV, 3kV and 4kV ESD transients, respectively. All ESD-critical parameters, including triggering and thermal breakdown voltage and current (V_{t1} , I_{t1} , V_{t2} , I_{t2}), and discharging resistance (R_{ON}), are obtained in simulation, which allows accurate ESD protection designs for 28nm core and I/O CMOS process modules to meet the required ESD design window [114].

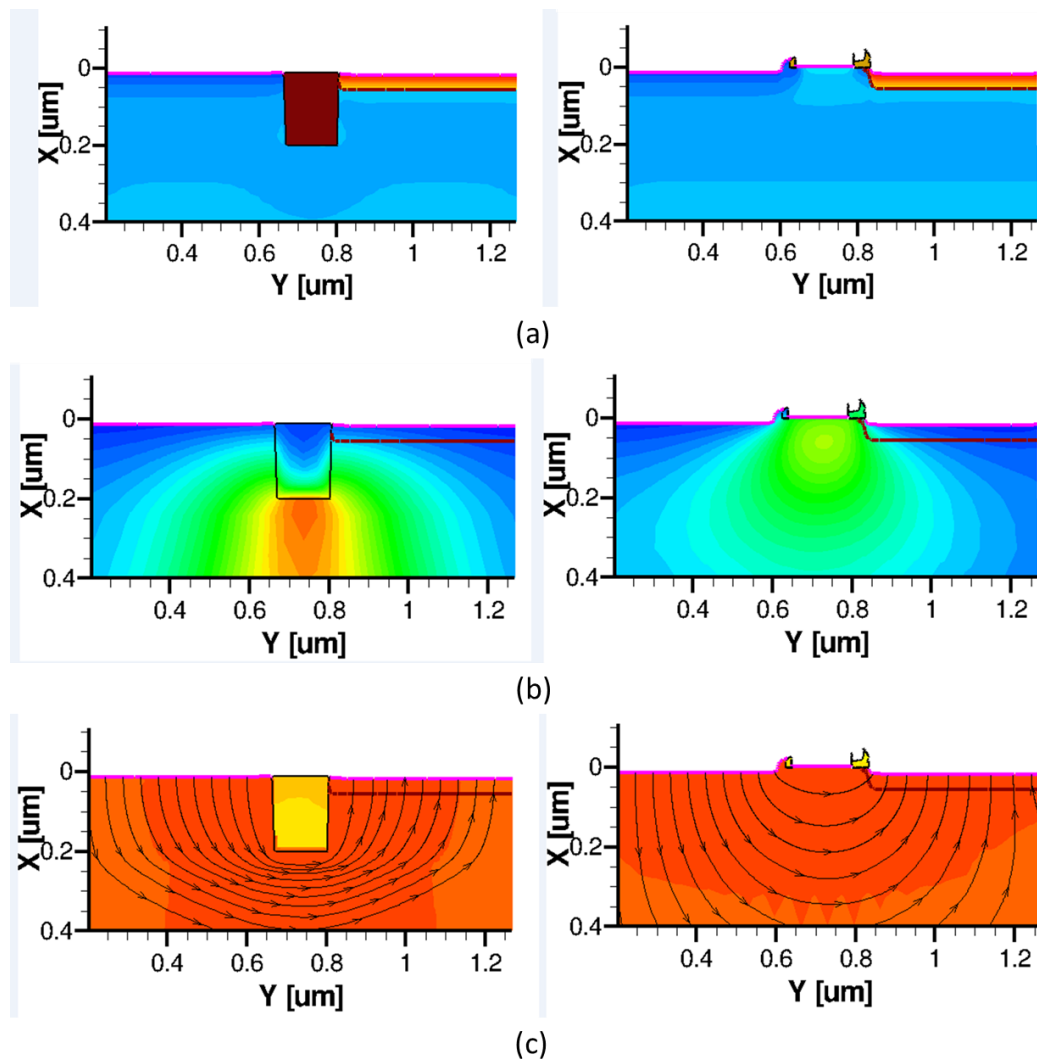


Figure 2.2.3 Simulated (a) cross-section, (b) temperature contours and heating effect, and (c) ESD discharging current flows for STI core diode (left) and poly-gated diode (right) ESD protection structures under same ESD stressing.

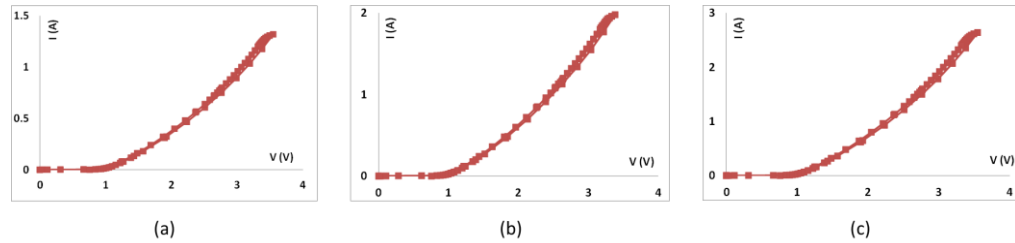


Figure 2.2.4 Simulated transient ESD discharging I-V curves for sample STI core diode ESD devices with different sizes: (a) 60 μm , (b) 100 μm and (c) 120 μm .

2.3.3.2 ESD Monitor Dummy Circuit Design

Practically, it is common that an ESD structure designed and tested as an individual ESD device works well, however, fails on chip. ESD-circuit co-design is critical for success of chip level ESD protection circuit design because complex ESD to circuit interactions exist [77]. Co-design becomes essential to 28nm ESD design due to more unexpected interaction effects. To ensure successful on-chip ESD protection for general circuit protection, we designed a couple of ESD monitor dummy circuit blocks in 28nm CMOS to evaluate ESD performance at chip level. While such dummy monitor circuits are not for any specific circuit, it considers critical CMOS gate breakdown risks for general circuits. Figure 2.3.5 illustrates the schematics for the two dummy ESD gate monitor circuit blocks. Figure 2.3.5 (a) is designed to evaluate ESD protection to the gate by ESD stressing test. The dummy monitor circuit in Figure 2.3.5 (b) allows both ESD protection testing and general MOSFET I-V characterization before and after ESD stressing, so that any potential ESD damage to the MOSFET may be evaluated in terms of its I-V behaviors. Figure 2.3.6 shows simulated ESD discharging I-V characteristics for one sample dummy ESD gate monitor circuit shown in Figure 2.3.5, which confirms the

designed ESD protection behaviors. Figure 2.3.7 gives the simulated ESD discharging voltage waveform in time domain under transient ESD stressing for the ESD gate monitor circuit, which should be carefully compared with the gate breakdown voltages of the core and I/O MOSFET in 28nm CMOS. This circuit level ESD simulation helps to determine if a given ESD diode device, though already being confirmed in ESD simulation for an individual ESD device, would provide required ESD protection at chip level. This is a critical ESD design aspect, which may often be ignored by IC designers in real world circuit designs.

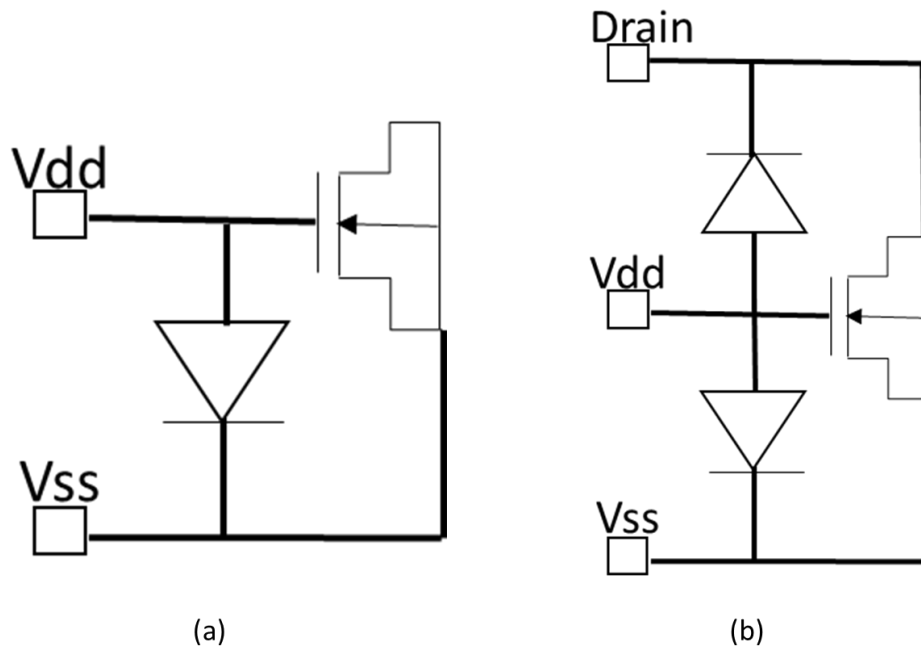


Figure 2.3.5 Schematics for ESD dummy gate monitor circuits: (a) gate ESD testing monitor only, and (b) gate ESD monitor and MOSFET I-V testing circuit.

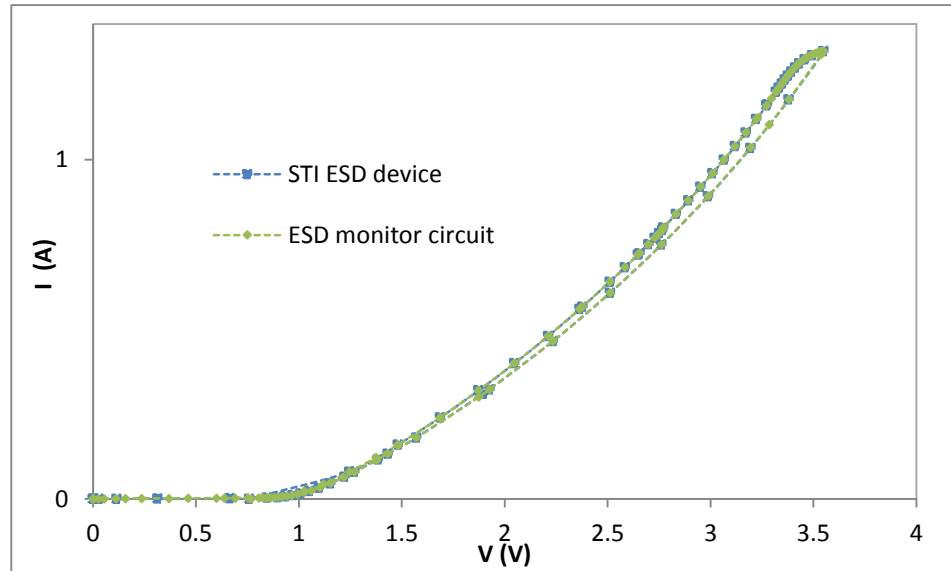


Figure 2.3.6 Simulated ESD I-V curve for a dummy ESD gate monitor circuit block shows transient ESD discharging behavior.

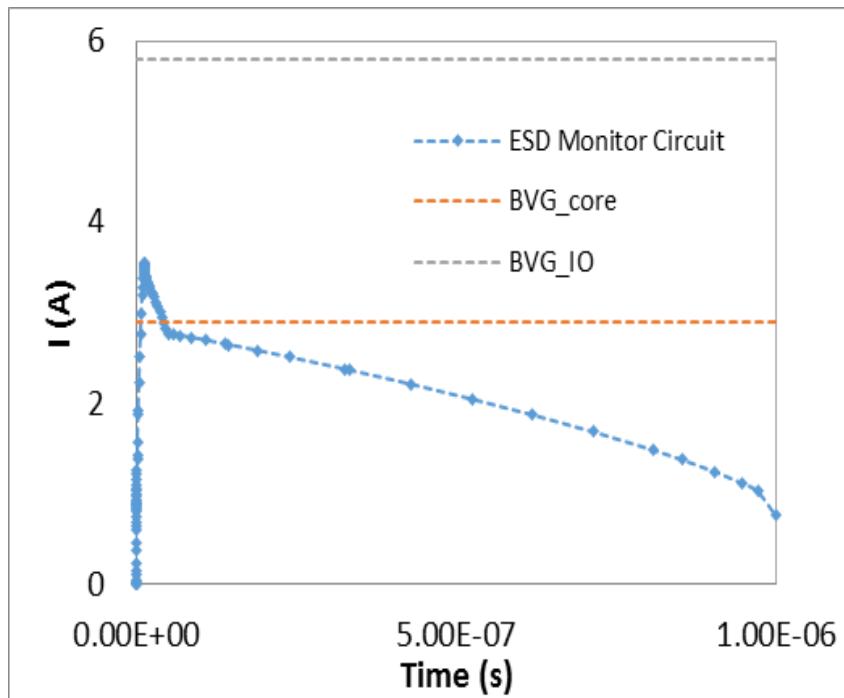


Figure 2.3.7 Simulated ESD discharging voltage in time domain for a dummy ESD gate monitor circuit shows ESD clamping voltage with respect to MOSFET gate breakdown voltage in core and I/O process sections.

2.3.4 Measurements and Analysis

2.3.4.1 Individual Diode ESD Characterization

A large set of diode ESD protection structures of various layout dimensions and connections, including STI diodes in core and I/O processes, as well as poly gated diodes, were designed and fabricated in a foundry 28nm high-performance CMOS technology. Comprehensive ESD characterization was conducted for all fabricated ESD structures using TLP tester (Barth Model 4002+) for transient ESD discharging evaluation, which provides all ESD-critical parameters (V_{t1} , I_{t1} , V_{t2} , I_{t2} , R_{ON}) and ESD-induced leakage current (I_{leak}). ESD-critical parameters must be accurately designed to ensure chip-level ESD protection performance, while the leakage must be evaluated to analyze possible ESD-induced negative impact on IC performance. Figure 2.3.8 shows the measured ESD I-V behaviors for sample STI core and I/O diode ESD structures with same finger width of $100\mu\text{m}$. Good ESD triggering and discharging behaviors are observed, which are predicted by mixed-mode ESD simulation. The two types of ESD devices have very similar ESD performance because they have similar ESD structures and ESD discharge current conduction paths. The main difference in doping density in the core and I/O process modules do not affect key ESD discharging behaviors as predicted by ESD simulation. The reverse diode breakdown voltages are different, which should be considered for ESD protection for different circuit sections using core and I/O processes in practical IC designs, because the gate and drain breakdown voltages of the protected circuits must be considered at chip level design in order to meet the ESD design window

to ensure whole-chip ESD protection performance. The ESD protection is reflected by the measured ESD thermal breakdown current, I_{t2} , which are about 3A and 3.2A for the STI core and I/O ESD diodes, equivalent to HBM ESD protection level of about 4.5kV and 4.8kV, respectively. The I_{t2} value was obtained conservatively at the threshold point where ESD I-V shows thermal breakdown and the ESD leakage current I_{leak} increases dramatically by several orders of magnitudes as shown in Figure 2.3.8. Figure 2.3.9 gives measured ESD discharging I-V curves for a sample poly-gated diode ESD structures with a finger width of 120 μ m, which clearly shows the desired ESD discharging behavior. It achieves $I_{t2} \sim 5A$, i.e., 7.5kV ESD protection level. The measured ESD-critical parameters for the different STI and gated diode ESD structures are summarized in Table 2.3.1. Figure 2.3.10 compares measured ESD I-V curves for three different types for ESD diode device samples of the same finger width (60 μ m). Several observations critical to practical ESD protection circuit designs were obtained readily. First, STI core and I/O diode ESD devices behave very similar for the same size ESD structures in terms of ESD triggering, discharging resistance, ESD capability and ESD induced leakage. This is because their ESD structures are very similar. Second, the poly-gated ESD diode can achieve much higher ESD protection level ($I_{t2} \sim 2.58A$ for 60 μ m) than the STI diode structures ($I_{t2} \sim 1.9A$ and 2A for 60 μ m). This was well predicted by ESD simulation as shown in Figure 2.3.3 where severe ESD current crowding was observed at the bottom of the STI plug in STI diodes, while the gated diode ESD structure enjoys a much smoother ESD discharging conduction. In ESD protection structures, any complex ESD discharging path that causes current crowding effect will inevitably lead to local ESD heating effect,

resulting severe micro hot spot inside an ESD device and, hence, reducing ESD protection capability. Third, it is also clearly observed in Figure 2.3.10 that a poly-gated ESD diode has higher leakage current compared to an STI diode. This may be attributed to the inevitable MOSFET gate leakage in the poly-gated ESD protection device. In addition, very short channel length in 28nm may cause leakage too. Although in this design, the gate of a gated diode ESD structure was properly biased to avoid possible channel inversion, it is clear that a gated diode ESD device will have more leakage current. Fortunately, the measured leakage current for a gated diode ESD device is well below nA level, which shall be no concern in practical IC designs.

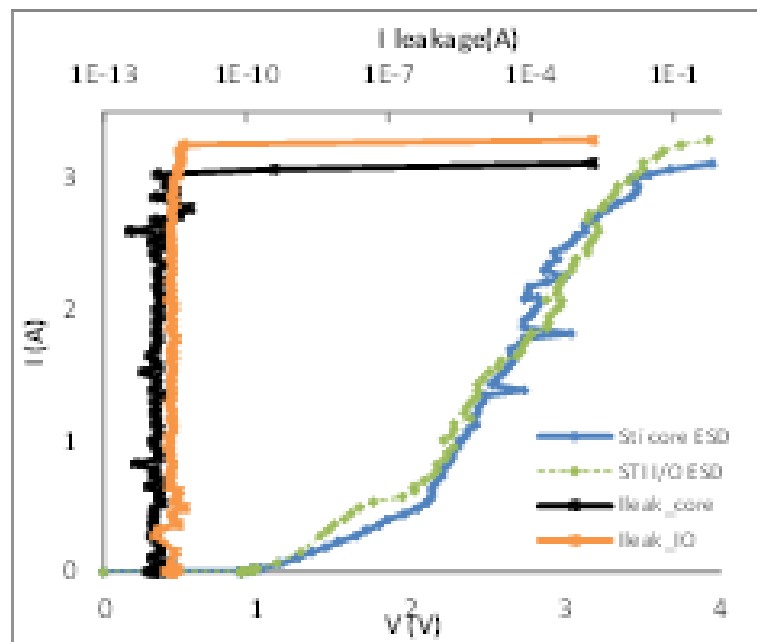


Figure 2.3.8 Measured ESD discharging I-V curves by TLP testing for STI diode ESD devices (100 μ m finger width) designed in core and I/O process modules achieve $I_2 > 3A$, translating into HBM ESD protection level of $> 4.5kV$ as predicted by ESD simulation.

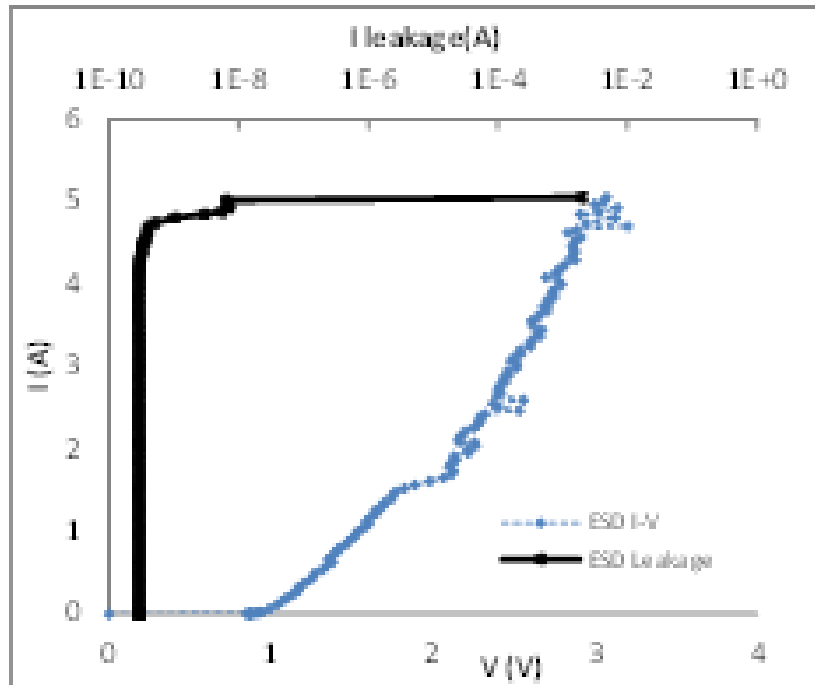


Figure 2.3.9 Measured ESD I-V curves for a sample N+/P-well poly-gated diode of 120µm show desired ESD discharging behaviors.

Table 2.3.1 Comparison of measured ESD-critical parameters for sample STI and gated diode ESD devices of different dimensions.

Devices		Vt1 (V)	It2 (A)	Vt2 (kV)
core_STI	60um	0.912	1.9	2.85
	100um	0.878	3.02	4.53
	120um	0.88	3.67	5.505
IO_STI	60um	0.924	2	3
	100um	0.889	3.25	4.875
	120um	0.878	3.84	5.76
Poly-gated	60um	0.875	2.58	3.87
	100um	0.878	4.23	6.345
	120um	0.869	5.02	7.53

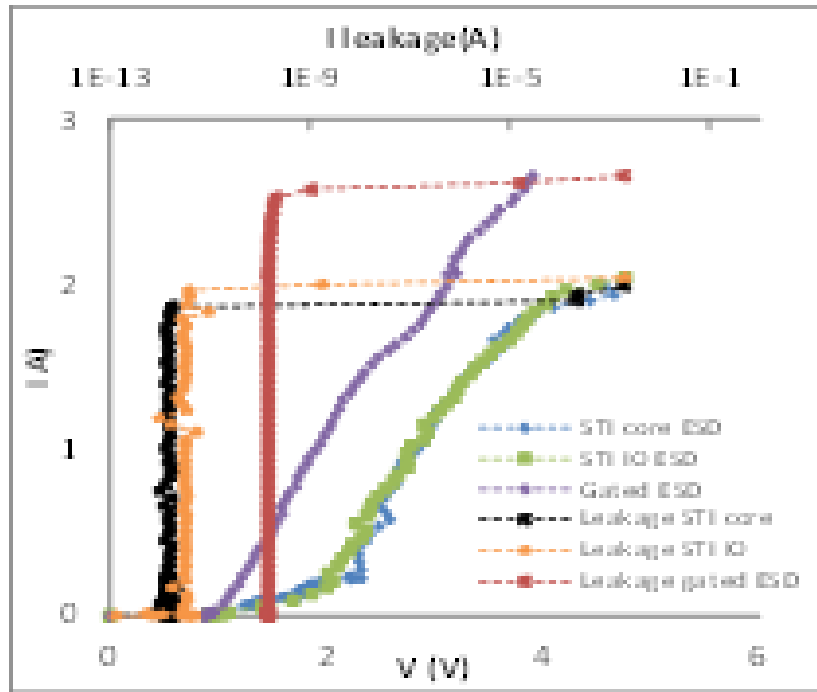


Figure 2.3.10 Measured ESD I-V curves for sample STI core and I/O diodes and gated diode of 60µm reveal details and differences in ESD performance.

2.3.4.2 ESD Monitor Circuit Characterization

As discussed before, to ensure whole-chip ESD protection, circuit level ESD characterization is required in addition to evaluating individual ESD protection devices. The dummy ESD gate monitor circuit blocks designed in this work were characterized by TLP testing. Figure 2.3.11 depicts the measured ESD I-V curves by TLP for a sample stand-alone STI core diode ESD device of 60µm and its corresponding dummy ESD gate monitor circuit as shown in Figure 2.3.5 (a). It is clearly observed that ESD protection was realized for individual STI ESD diode and the monitor circuit as predicted by ESD simulation. Due to extra gate leakage associated to the dummy MOSFET, relatively higher current was observed for the ESD gate monitor circuit in both ESD discharging I-

V curve and the leakage curve, which was expected. Such circuit level ESD protection analysis by both ESD simulation and measurement is important in practical ESD protection circuit design at 28nm to ensure whole-chip ESD protection. The measured ESD protection capability for the STI and gated diode ESD protection devices designed achieved good ESD protection level of about 47V/ μm , 48V/ μm and 64V/ μm for the STI core, STI I/O and gated I/O diodes fabricated, respectively.

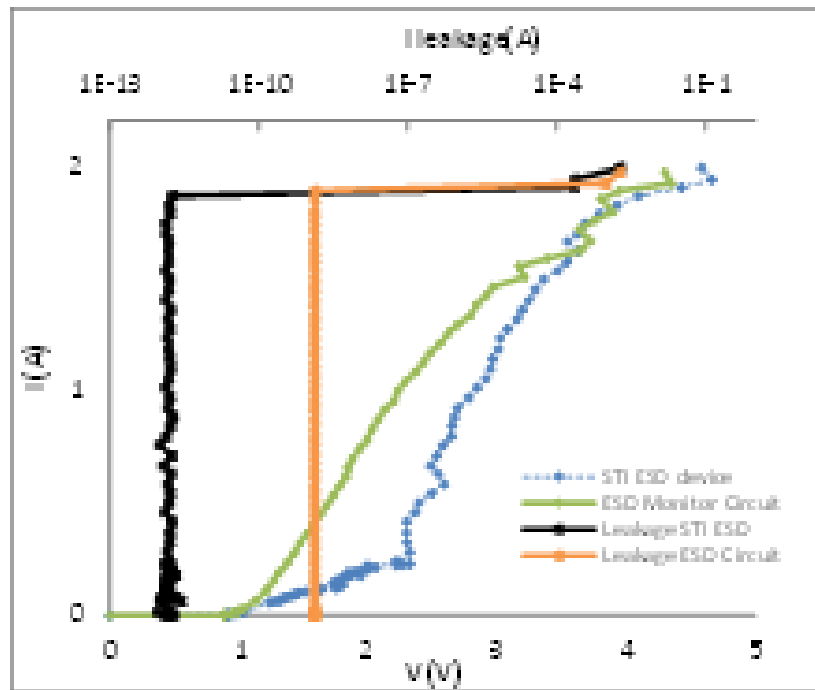


Figure 2.3.11 Measured ESD discharging I-V curves for a sample STI core diode ESD devices of 60 μm and its ESD gate monitor circuit confirms proper ESD protection at chip level.

2.3.5 Conclusion

We report a comprehensive design and analysis of STI and gated diode ESD protection structures in 28nm CMOS. Mixed-mode ESD simulation can predict chip level ESD protection performance, which is confirmed by ESD testing. The ESD protection design technique and results shall be useful to IC designs at 28nm node and beyond.

Section 3 Summary

In this dissertation, soft magnetic underlayers for next-generation magnetic recording media and ESD protection devices are introduced. In the magnetic recording section, basic concepts for hard disk drives were discussed, for example, the orientation of the grains and current challenges for the traditional longitudinal magnetic recording as well as the principles for perpendicular magnetic recording, and the functions for various layers in the perpendicular magnetic recording. SUL is a crucial part in the perpendicular recording technology to achieve higher writing field. However, it is really difficult to control the “softness”.

A comparison study between the novel CoFeTaZr SUL and conventional CoTaZr SUL was presented. Various optimization were also carried out on the novel CoFeTaZr SUL to achieve better performance. CoFeTaZr has a much lower coercivity compared to CoTaZr while remains the same magnetic moments, the fabrication process is simply by sputtering without heating process, which is highly desired for SUL in the perpendicular magnetic recording. Moreover, SUL behaviors with the seedlayer and capping layer

(intermediate layer in perpendicular magnetic recording) were also investigated. All these factors together, make CoFeTaZr SUL a superior SUL to replace the CoTaZr SUL.

Then the principles of ESD protection designs, ESD test models and basic ESD protection structures were studied. Due to the scaling, new challenges were brought to the ESD protection design, especially the shrinking effect on the “ESD Design Window”. To solve this problem, two novel ESD protection structures were introduced.

The first new structure is based on nonvolatile memory. By applying high DC voltage on the gate for a certain amount of time to “program” the devices, the V_{th} of the devices will be changed, and thus causing a V_{t1} variation. In this part, two structures were introduced. NC-QD ESD protection structure with layers of QD incorporated into the floating gate layer and SONOS-based ESD protection structure with an ONO floating gate layer. These two structures are both CMOS-compatible and could be connected as ESD protection unit. A wide programmable ESD $\Delta V_{t1} \sim 3V$ for NCQD ESD devices, $\Delta V_{t1} \sim 2V$ for SONOS-based ESD devices were achieved with ultra-low leakage current $I_{leak} \sim 15pA$ for NCQD ESD devices, $I_{leak} < 1.2pA$ for SONOS-based ESD devices. These two structures could be potential solutions to the “ESD Design Window” shrinking and ideal for the multiple power domains due to their programmability after fabrication.

Another novel ESD protection structure is the nanocrossbar array. Compared to previous work on single node nanocrossbar, the array could provide a high current handling capability as well as low leakage current $\sim 0.11pA$. The nanocrossbar array is also dual-direction ESD protection structure. This is a highly desired feature due to the

simplicity of the ESD protection circuit design, reduced layout area and ESD-induced parasitics.

Lastly, shallow trench isolation and poly-gated diode based ESD protection structures in a foundry 28nm are compared. STI core and STI I/O diodes behave similarly due to the similar structures. However, poly-gated diodes have a higher current handling capability compared to STI diodes. A higher leakage current due to the gate leakage was also observed from poly-gated diode. A dummy gate monitor was also studied to value the diode behavior on the whole chip protection.

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