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A Synchronous Boot-strapping Technique with Increased On-time and Improved Efficiency for High-side Gate-drive Power Delivery

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***Abstract*—In this work we demonstrate a synchronous boot-strap power delivery scheme applied to a high level count GaN-based flying capacitor multi-level (FCML) converter. The proposed approach is well suited for high-frequency operation as it eliminates conventional boot-strap diodes and allows for precise on-time control for a maximized conduction duration. Importantly, we note the synchronous boot-strapping scheme's capability for bi-directional energy transfer: Gate driver power can be injected into the chain from either a ground referenced supply, a high-side line referenced supply, or both simultaneously for further reduced voltage droop. A discrete 6-level FCML hardware prototype switching at 500 kHz (2.5 MHz effective) is designed and constructed to validate this approach. A maximum deviation in supply voltage of 156 mV throughout all 10 series stacked gate drivers for converter duty ratios spanning 15-85% is measured. Subsequently the need for local regulation throughout the gate-drive chain is eliminated, which in turn improves efficiency, simplifies design, and reduces cost.**

I. Motivation & Background

In the quest towards improved power density, efficiency and cost, industries continue to be receptive to improvements made in micro-assembly and co-packaging, in addition to monolithic solutions, with power electronics modules gaining a significant market share in recent years. To that end, there is a strong push to revisit and improve converter sub-systems that would not have been considered limiting in the recent past.

One essential, yet often trivialized aspect of power converter design is the power delivery scheme for the gate-drivers contained therein. While this circuitry is expected to leave a minimal footprint, improvements in this area have not kept pace with the rapidly developing power converter landscape in which higher order topologies eschew simplicity for dramatic performance improvements [1]–[3]; advanced control schemes and assistive circuitry minimize parasitic effects [4]–[6]; and advanced semiconductor devices, such as Gallium Nitride, consume significantly less area for the same switch conductivity while simultaneously boasting reduced parasitics. Subsequently, switching frequencies have been increased, resulting in the ordinarily dominant volume of passive components reducing considerably [7], [8].

Conventional gate-driver power delivery has historically employed isolated voltage supplies when dealing with topologies with complexity beyond the standard half-bridge structure (e.g. [9]). However, this approach tends to be expensive while consuming considerable converter volume, especially for converters with a high switch count, such as the flying capacitor multi-level (FCML) converter [10]–[12]. In response, in recent years there has been a push in the literature to promote and develop non-isolated gate-driver power delivery techniques with the promise of greatly increased overall converter density [13]–[16].

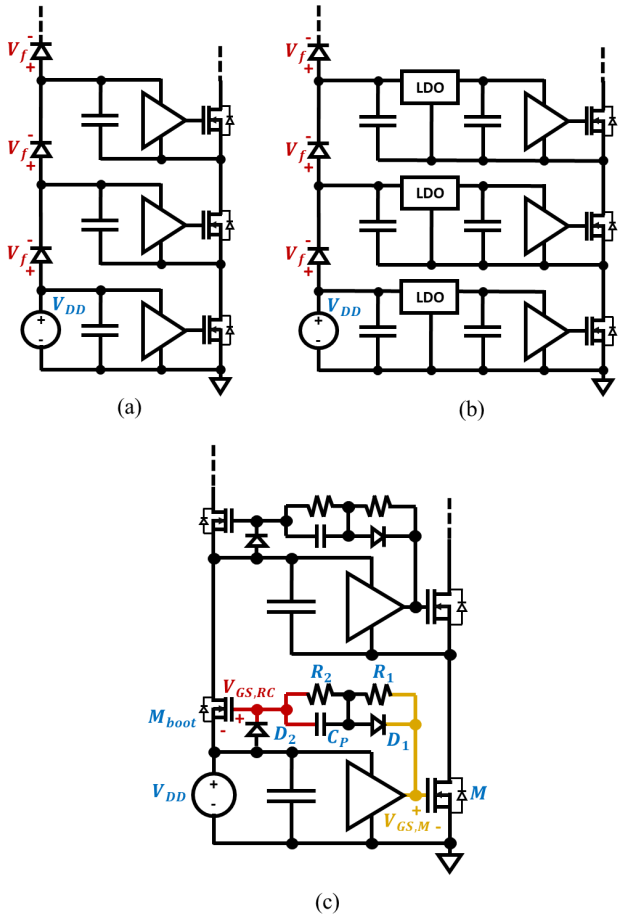

Fig. 1. Prior work on non-isolated gate driver power delivery. (a) Straightforward cascaded boot-strapping using diodes ([13], [14]); suffers from accumulating voltage droop due to repeated diode forward voltage drops. (b) Cascaded boot-strap with LDO regulation [16]; local regulation ensures correct voltage presented to each gate driver, albeit with poor efficiency. (c) RC-delayed synchronous boot-strapping [15], [17]; removes diodes drops, increasing efficiency and feasible switching frequency, although bootstrap conduction time is still limited by RC delay.

The commonly used boot-strap diode offers a simple and elegant solution for half-bridge structures, with many commercial products even integrating this element on-chip [18]. However, when applied over an increased number of switches, repeated diode drops leads to a significant decrease in voltage provided to each subsequent gate driver (Fig. 1 (a)). While [14] has described a voltage recovery scheme leveraging a finite dead-time duration, this approach is load and timing dependent and only applicable to switches that are subjected to reverse conduction as part of normal converter operation. In GaN-based converters where tight supply tolerances are required, this approach may be considered infeasible in practice.

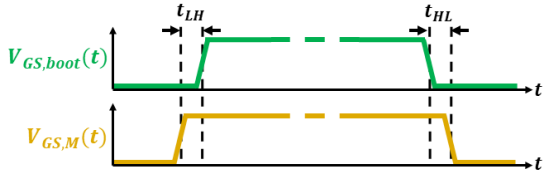

Fig. 2. Timing diagram of ideal V_{GS} waveforms in a synchronous bootstrap solution. Time durations t_{LH} and t_{HL} must be substantial enough to avoid shoot-through currents, but sufficiently short so as to maximize conduction through M_{boot}, reducing voltage droop in a cascaded array of gate drivers.

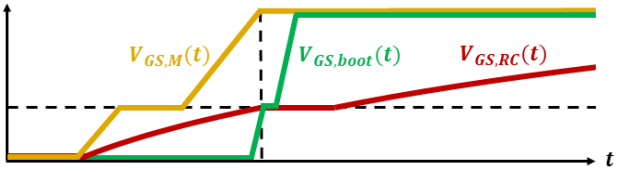

Fig. 3. Example V_{GS} waveforms occurring at the turn-on of primary switching device M (gold). Since the RC-delayed gate signal for M_{boot} (red) begins rising at the same time as $V_{GS,M}$, its slope must be greatly reduced such that M_{boot} does not turn on until $V_{DS,M} = 0V$. Conversely, the proposed buffered signal (green) may turn on sharply, allowing M_{boot} to reach minimum $R_{DS,ON}$ much sooner.

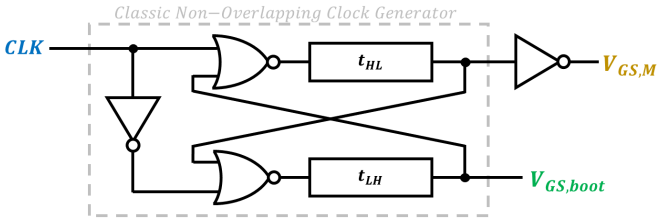

Fig. 4. Appropriate synchronous bootstrap signals may be synthesized locally using modified dead-time control circuitry, and can be easily integrated on-chip within existing gate driving solutions. Time delays t_{HL} and t_{LH} are kept as short as possible while avoiding shoot-through currents within the bootstrapping network.

In [16], this accumulating voltage droop is overcome by increasing the ground-referenced supply voltage (V_{DD}) and introducing local regulation within each gate driver (Fig. 1 (b)). Recognizing that this approach leads to significant LDO-incurred inefficiency, [16] further proposes splitting the power delivery path using gate driven charge pumps, reducing the path impedance and leading to reduced LDO losses. While both of these approaches offer compelling results, they still rely on lossy diodes and ultimately require local regulation.

Alternatively [17] improved on [15] by suggesting a gate-driven synchronous boot-strap using an RC delay network to provide an appropriate gate drive signal to a diode-replacing boot-strap FET (M_{boot} Fig. 1 (c)). Here, M_{boot} must only be turned on within the conduction period of primary FET, M (Fig. 2). To do otherwise risks unintended and potentially damaging large reverse current transients from a high-side bypass capacitor back down to the preceding low-side charge resevoir. In this solution, t_{LH} is defined by the RC time constant of R_1 and the intrinsic gate capacitance, C_{ISS}, of M_{boot}. Here, C_p is large and stores a DC offset equal to V_{DD}, effectively performing voltage level translation. D_1 acts to bypass R_1 during the falling edge and allows M_{boot} to rapidly turn off at the same time as M with a marginally acceptable t_{HL} of zero seconds. D_2 and R_2 are high impedance elements that act to bias C_p at V_{DD} in steady-state.

This approach eliminates diode voltage drops and alludes to the possible omission of local regulation stages [19], [20]. However, the slope of this rising RC-delayed gate signal ($V_{GS,RC}$ in Fig. 3) must be severely limited since it begins rising at the same time as the gate of the primary switching device, M, and must be designed such that M_{boot} does not turn on until after the V_{DS} of primary switch M has fully discharged to 0 V. As such, M_{boot} does not reach its minimum $R_{DS,ON}$ until much later. For high frequency converters this delayed turn-on can be detrimental and allows the aforementioned voltage droop issues to persist, as recorded in [16].

II. Synchronous Bootstrap with Maximized On-Time

Here we explore a synchronous boot-strapping technique that instead applies controlled timing delays such that a sharp buffered gate-drive signal can be quickly applied to M_{boot} as soon as $V_{DS,M}$ has reached 0V. This approach avoids the RC-settling observed in $V_{GS,RC}$ (Fig. 3) and enables M_{boot} to conduct for its full allowable duration ($V_{GS,boot}$ in Fig. 3), with minimum $R_{DS,ON}$. In turn, this results in maximum charge being transferred and extends the achievable frequency of operation while minimizing voltage droop on successive cascaded gate drivers.

There are several ways to generate the ideal $V_{GS,boot}$ signal depicted in Figures 2 and 3, such that it maintains precise timing relationships to $V_{GS,M}$, as defined by t_{HL} and t_{LH}. Here, rather than using separate level-shifted clock signals to control M and M_{boot} (with t_{XX} defined within the controller), instead $V_{GS,boot}$ is synthesized locally from the same single level-shifted signal destined for M. To do so, the classic non-overlapping clock generator (Fig. 4) may be modified to include one additional inverter on its output: The result is a $V_{GS,boot}$ waveform that exclusively overlaps with $V_{GS,M}$, thereby providing the desired ideal buffered waveforms depicted in Fig. 2.

To demonstrate this in hardware, existing integrated dead-time circuitry was leveraged, making this approach viable as a fully integrated circuit (IC) gate-drive solution. Figures 5 and 6 depict the gate-drive circuitry used to synthesize appropriate gate signals for both the primary switching device, M, and its associated boot-FET, M_{boot}. The internal dead-time circuitry of a high-speed commercial GaN gate-driver is used to provide tuned delays, with an additional gate-drive IC

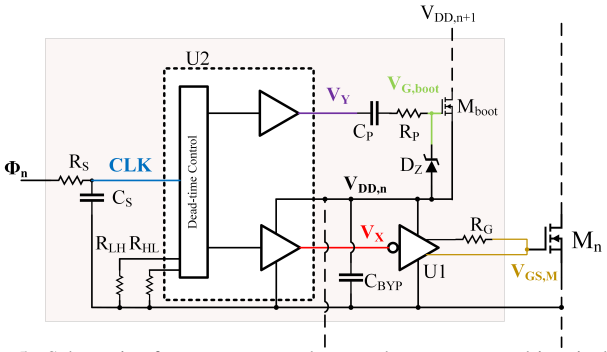

Fig. 5. Schematic of a prototype synchronous boot-strap gate-driver including a dead-time control IC, U_2; an output driver stage, U_1; and a level-shifting charge-pump to drive M_{boot}. The charge-pump may be omitted if M_{boot} is instead made depletion mode.

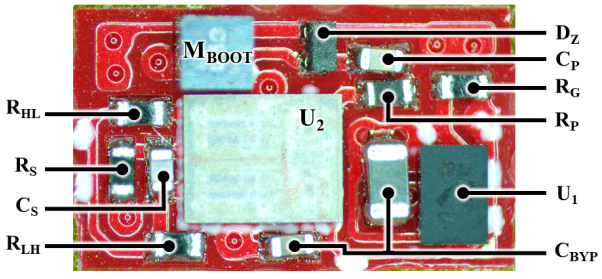

Fig. 6. Photograph of constructed daughter-board proof of concept, containing gate-driver and synchronous boot-strap circuitry.

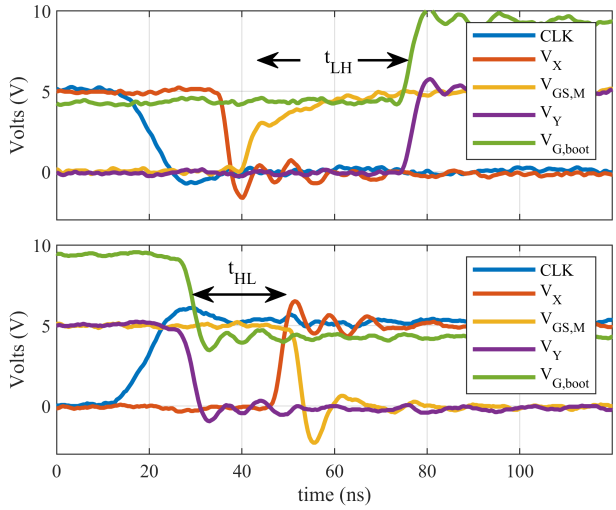

Fig. 7. Measured voltage waveforms demonstrating the correct synthesis of $V_{GS,boot}$ ($= V_{G,boot} - 5V$) with respect to $V_{GS,M}$. Top and bottom figures zoom in on rising and falling edges of $V_{GS,M}$ respectively. $V_{G,boot}$ only goes high after a programmed delay t_{LH}, and goes low before $V_{GS,M}$, avoiding any possibility of shoot-through currents while simultaneously maximizing the conduction window of M_{boot}.

TABLE I
DAUGHTERBOARD COMPONENTS

Component	Description
U_1	Gate Driver, LMG1020
U_2	Dual Gate Driver, PE29102
M_{boot}	100 V 73 mΩ, EPC2036
R_S	200 Ω 0201
C_S	50 pF 0201
R_{HL}	100 kΩ 0201
R_{LH}	750 kΩ 0201
D_z	5.6 V Zener 0201
C_P	10 nF 0201
R_P	10 Ω 0201
R_G	5.1 Ω 0201
C_{BYP}	0.1 μ F (0201), 2.2μF (0402)

providing a required signal inversion. Similar to C_P in Fig. 1 (c), here capacitor C_P maintains a 5V offset allowing a level-shifted drive signal to be applied to M_{boot}. However, we note that a depletion mode device may instead be used, eliminating the need for components C_P, R_P and D_Z (e.g. [21]). R_P is employed here to limit $V_{GS,boot}$ overshoot given that the gate driver producing V_Y is greatly oversized for this application. D_Z ensures that $\sim 5V$ is maintained on C_P and is a discrete alternative to D_2 and R_2 in Fig. 1 (c). R_s and C_s are optional noise filtering components. The time durations of t_{HL} and t_{LH} may be adjusted via R_{LH} and R_{HL}. Measured voltage waveforms validating intended operation are depicted in Figure 7 and the specific component values used are listed in Table I.

III. APPLICATION TO A 6-LEVEL FCML

The described synchronous boot-strapping circuitry was demonstrated within a 6-level FCML converter, depicted in Figures 8 and 9 and in which there are ten GaN switching devices connected in series (M_{1-10}). Consequently, these switches are controlled using ten copies of the daughterboard depicted in Fig. 6. Here, ten much smaller GaN-FETs, serving as M_{boot}, are used to replace the diodes used in a conventional cascaded bootstrap. While validating this boot-strapping approach in hardware, power and voltage levels were kept significantly lower than rated, while the converter was switched at 500 kHz, resulting in the FCML's output inductor seeing an effective 2.5 MHz switching frequency with a line voltage, V_{IN}, of 140V (Fig. 10). Table II lists the components used to construct the power stage.

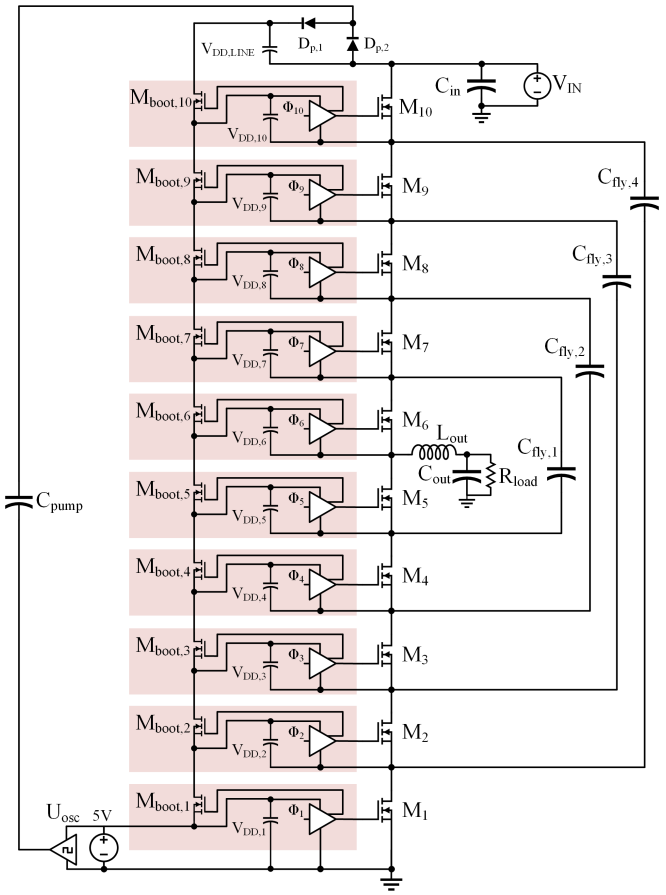

Fig. 8. Simplified schematic of the constructed 6-level FCML prototype using synchronous boot-strapping within each gate-driver. Ten copies of the previously described daughterboards are used to drive and provide power to ten series connected GaN devices, M_{1-10}. An additional charge pump, comprised of U_{osc}, C_{pump}, $D_{p,1}$, and $D_{p,2}$ is included to provide a 5V line referenced supply, $V_{DD,LINE}$, and allows power to be delivered from both ends of the boot-strapping network, further reducing voltage droop.

TABLE II
FCML COMPONENTS

Component	Description
L_{out}	7.92μH, 11A, 10.8mΩ
M_{1-10}	100V 3.2mΩ, EPC2218
$C_{fly,1,2,3,4}$	3.2μF, 4.2μF, 3.6μF, 3.2μF, X7R
C_{in}	4.2 μF, X7R
$Level\ Shift$	2EDF7275K
U_{osc}	Gate Driver, 1EDN7550U
$D_{p1,2}$	20V Schottky 0402
C_{pump}	47nF 450V X7T 0805

We note that this work serves as the first demonstration of bi-directional energy delivery throughout a cascaded bootstrapping network: Since M_{boot} can conduct in either direction when turned on, dissimilar to a diode, it follows that a gate driver may receive energy from the high-side driver immediately above it, provided it can access this energy. That is, this gate driver must possess sufficient initial charge to push the gate of its M_{boot} high, thereby enabling charge to flow down onto its local bypass capacitor[1]. This requirement that charge be stored locally in order to facilitate access to energy provided by gate drivers higher up the bootstrapping chain, necessitates an initial upward flow of energy from a ground referenced supply (5V in Fig. 8) at start-up, as is conventional.

[1]This was not the case in [20] where PMOS devices were instead used. In this case, M_{boot} is controlled by the high-side driver and may commence a downward flow of charge irrespective of the charge stored within gate drivers beneath it. However, with this approach appropriate generation of $V_{GS,boot}$ becomes significantly more challenging as it cannot be generally synthesized from the adjacent primary switching device.

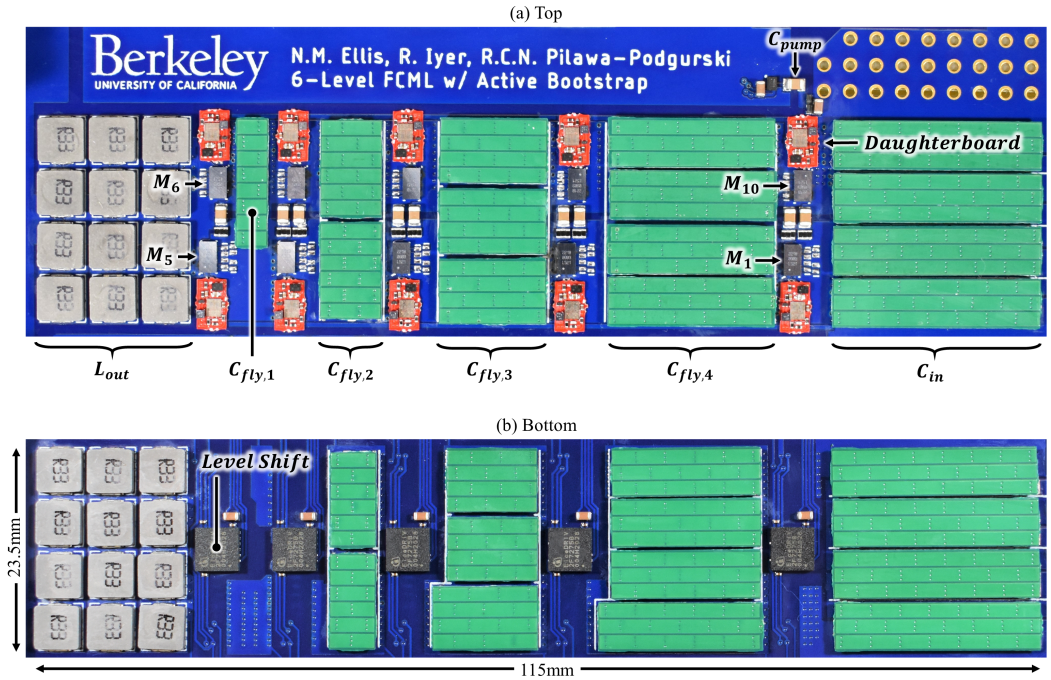

Fig. 9. Photograph of the constructed 6-level FCML prototype using the synchronous boot-strap power delivery on all 10 GaN-FETs.

However, once all gate drivers linked by synchronous boot-strapping are sufficiently charged, energy may be derived from a downward flowing line-referenced supply, labelled $V_{DD,LINE}$ in Fig. 8, in addition to the ground referenced upward flowing supply, $V_{DD,1}$. This essentially halves the impedance of the gate-drive power delivery path since charge may be delivered from both ends of the bootstrapping network. Alternatively, once a downward flowing charge path has been established, the ground referenced supply may be disabled with energy delivery from $V_{DD,LINE}$ self-sustaining, although this may not be desirable in practice. In this prototype, a simple charge-pump consisting of an oscillator, a pumping capacitor, and two diodes was used to produce $V_{DD,LINE}$, thereby allowing gate-driver energy to be fed into the chain via $M_{boot,10}$.

To validate the aforementioned concepts, the steady-state DC voltages stored on all 10 of the gate-driver's bypass capacitors was measured for FCML duty cycles of 15%, 50%, and 85% while switching at 500 kHz. For each of these operating points, gate-drive power was supplied either from the 5V low-side supply $V_{DD,1}$, the charge-pump generated high-side supply $V_{DD,LINE}$, or both simultaneously for minimal voltage droop throughout the chain. Figure 11 documents these results and illustrates that when the synchronous boot-strapping network is fed energy from both a ground-referenced and line-referenced supply, a worst-case maximum voltage droop of 156 mV is observed across a wide duty cycle range of 15-85%. This is a significant improvement over the RC-delayed synchronous approach which yielded a $\sim$ 1 V droop at a relaxed 75% duty cycle in [16].

IV. Conclusion

To conclude, this work demonstrates a synchronous gate-drive power delivery approach with a greatly reduced volume as compared to conventional fully isolated solutions. It performs significantly better than cascaded diode approaches due to the absence of any forward voltage drops, ultimately eliminating the need for local regulation. Additionally, the boot-strap conduction duration is maximized, making it well suited for high frequency converters. Furthermore, appropriate boot-strap control signals may be generated locally

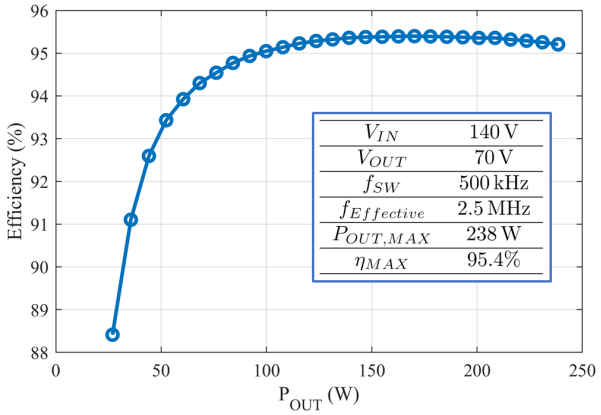

Fig. 10. Measured efficiency versus output power for a 6-level FCML prototype with $V_{IN} = 140V$ and a 50% duty cycle.

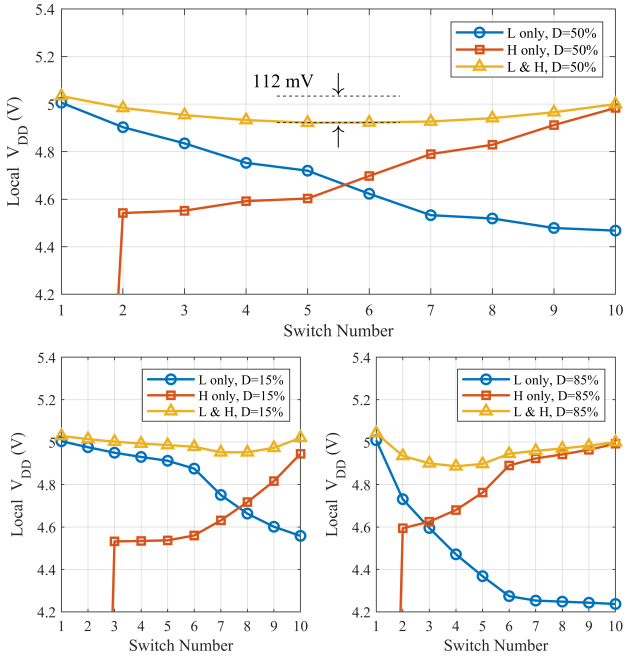

Fig. 11. Measured supply voltages across all 10 gate-drivers with varying duty cycle and three permutations of power delivery: low-side power only, high-side power only, and both simultaneously. At 50% duty cycle, applying power from both ends of the boot-strap network leads to a low voltage droop of 112 mV.

within a given gate-driver, with the majority of components suitable for complete monolithic integration. Moreover, we explore the possibility of bi-directional energy flow through a synchronous boot-strap network and demonstrate that voltage droop can be further reduced by applying power to both ends of the chain, approximately halving its impedance.

This approach was successfully demonstrated as part of a high level count FCML where power is delivered to ten series connected switches. A maximum voltage droop of 158 mV is observed across all switches over a wide conversion range of 15-85%, verifying that this approach is well suited for providing power to high-order GaN-FET networks which demand strict supply tolerances.

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