UNIVERSITY OF CALIFORNIA SAN DIEGO

Ultra-Low-Power Sensors and Receivers for IoT Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Haowei Jiang

Committee in charge:

Professor Drew A. Hall, Chair
Professor Gert Cauwenberghs
Professor Young-Han Kim
Professor Patrick P. Mercier
Professor Gabriel M. Rebeiz

2019

The Dissertation of Haowei Jiang is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

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Chair

University of California San Diego

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Haowei Jiang

La Jolla, CA

September 2019

VITA

EDUCATION

2014	Bachelor of Engineering in Electrical Engineering and Automation, Huazhong University of Science and Technology, Wuhan, China
2016	Master of Science in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego, La Jolla, USA
2019	Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego, La Jolla, USA

PUBLICATIONS

H. Jiang, P. H. Wang, L. Gao, C. Pochet, G. M. Rebeiz, D. A. Hall, P. P. Mercier, " A 22.3 nW, 4.55 cm^2 Temperature-Robust Wake-up Receiver Achieving a Sensitivity of -69.5 dBm at 9 GHz," *Journal of Solid-State Circuits (JSSC)*, In Press.

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FIELDS OF STUDY

Major Field: Electrical Engineering

Studied in Electronic Circuits and Systems

Professor Drew A. Hall

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Ultra-Low-Power Sensors and Receivers for IoT Applications

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Haowei Jiang

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The combination of ultra-low power analog front-ends and CMOS-compatible transducers enable new applications, such as environmental monitors, household appliances, health trackers, etc. that are seamlessly integrated into our daily lives. Furthermore, wireless connectivity allows many of these sensors to operate both independently and collectively. These techniques collectively fulfil the recent surge of internet-of-things (IoT) applications that have the potential to fundamentally change daily life for millions of people.

In this dissertation, the circuit and system design of wireless receivers and sensors is presented that explores the challenges of implementing long lifespan, high accuracy, and large coverage range IoT sensor networks. The first is a wake-up receiver (WuRX), which continuously monitors the RF environment to wake up a higher-power radio upon detection of a predetermined RF signature. This work both improves sensitivity and reduces power over prior art through a multi-faceted design featuring an impedance transformation network with large passive voltage gain, an active envelope detector with high input impedance to facilitate large passive voltage gain, a low-power precision comparator, and a low-leakage digital baseband correlator.

Although pushing the prior WuRX performance boundary by orders of magnitude, the first work shows moderate sensitivity, inferior temperature robustness, and large area with external lumped components. Thus, the second work shows a miniaturized WuRX that is temperature-compensated, yet still consumes only nano-watt power and millimeter area while operating at 9 GHz. To further reduce the area, a global common-mode feedback is utilized across the envelope detector and baseband amplifier that eliminates the need for off-chip ac-coupling components. Multiple temperature-compensation techniques are proposed to maintain constant bandwidth of the signal path and constant clock frequency. Both WuRXs operate at 0.4 V supply, consume near-zero power and achieve ~-70 dBm sensitivity.

Lastly, the first reported CMOS 2-in-1 relative humidity and temperature sensor is presented. A unified analog front-end interfaces on-chip transducers and converts the inputs into a frequency vis a high-linearity frequency-locked loop. An incomplete-settling switched-capacitor-based Wheatstone bridge is proposed to sense the inputs in a power-efficient fashion.

Chapter 1

Introduction

1.1 Motivation for Internet-of-Things Sensors

The combination of ultra-low power analog front-ends (AFEs) and CMOS-compatible transducers enable new applications, such as environmental monitors, household appliances, health trackers, etc. that are seamlessly integrated into our daily lives. Furthermore, wireless connectivity allows many of these sensors to operate both independently and collectively. These techniques collectively fulfil the recent surge of internet-of-things (IoT) applications that have the potential to fundamentally change daily life for millions of people.

The Internet-of-Things helps people live and work smarter as well as gain complete control over their lives. There are numerous real-world applications of the internet of things, ranging from consumer and enterprise to manufacturing and industrial [1]. In the consumer segment, for example, smart homes that are equipped with smart thermostats, smart appliances and connected

heating, lighting and electronic devices can be controlled remotely [2]. Wearable devices can collect, analyze and sending data to smartphones with the aim of making users' lives easier and more comfortable. In healthcare, IoT offers many benefits, including the ability to shift the centralized biomedical examinations towards the point-of-care to monitor patients more closely [3]–[8]. In agriculture, IoT-based smart farming systems can help monitor, for instance, light, temperature, humidity and soil moisture of crop fields using connected sensors. In a smart city, IoT sensors and deployments, such as smart streetlights and smart meters, can help alleviate traffic, conserve energy, monitor and address environmental concerns and improve sanitation.

Wireless connectivity and sensing are the two cornerstone technologies to the IoT [9]. We are giving the world a digital nervous system: location data using GPS sensors; eyes and ears using cameras and microphones, along with sensory organs that can measure everything from temperature to acceleration depending on what the applications require. These inputs are digitized and placed onto networks: from wide area networks (WAN) to local area networks (LAN) and even personal area networks (PAN). Therefore, as shown in Figure 1.1, an IoT sensor is the kind of node equipped with certain types of sensors and has communication capability. With an expectation of rapidly increased IoT sensors [1], there is a surging demand of developing wireless communication circuits and sensing circuits that are oriented for IoT usage.

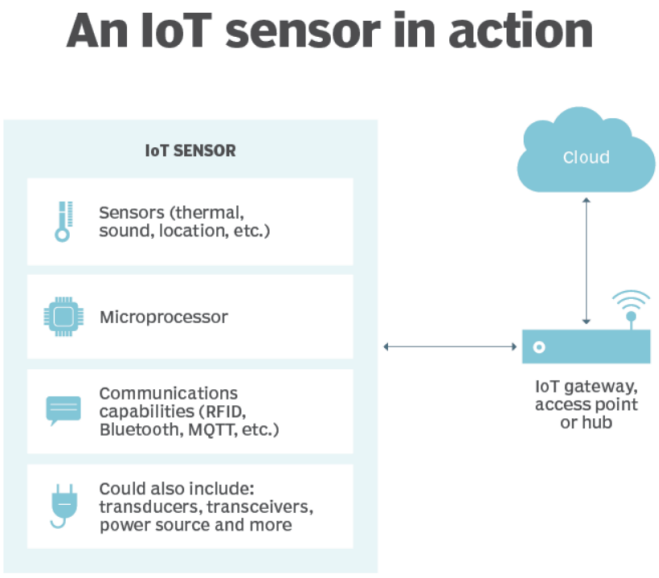


Figure 1.1. Illustration of an IoT sensor from [1].

1.2 Event-Driven Communication Using Wake-up Receiver

There is a growing class of event-driven devices that require instant-on wireless connectivity, but only use the radio to communicate intermittently throughout their lifetime. For example, smart homes equipped with smart sensors and automatic appliances, only use or need their radios when prompted by an event. In these applications, the energy spent synchronizing the radios, or maintaining a connected state, dominates, as opposed to the energy spent communicating, sensing, and processing data [10], [11].

Because of the intermittent nature of event-driven communication, IoT radios spend much of their time in a sleep state, where the radios are not capable of sending or receiving packets, in an effort to conserve energy and reduce their average power consumption. This creates a challenge when two radios need to establish communication with each other. Both radios need to wake up and communicate at the same time, which requires the radios to be synchronized with one

another. As shown in Figure 1.2(a), the conventional method to synchronize the IoT nodes is to periodically wake up their radios to check for wireless messages triggered by a random event. However, this doesn't solve the power problem of event-driven communication, since energy is wasted every time a radio wakes up to try and establish communication and it fails. Although the energy spent could be low by having a low duty cycle, it will inevitably increase the latency, which has a maximum value limited by the application. This tradeoff between power and latency is not ideal.

A wake-up radio (WuRX) can be used as a superior alternative to conventional method. The WuRX acts as a secondary receiver within an asynchronous protocol. While the other radios are conserving power in an ultra-low power sleep state, the WuRX continuously monitors the RF environment for events and enables the main communication radio when it detects another radio trying to communicate [Figure 1.2(b)]. Because the WuRX remains always-on, it must be ultra-low power, which is the main specification that drives WuRX design. This event-driven synchronization methodology is energy efficient because the high-power receiver remains off as long as possible and only wakes when communication is necessary. In sensor settings with low event activity, considerable extension (1 month → 10 years) of battery life can be achieved, as shown in Figure 1.3[12].

This is the motivation behind the Near-Zero Power (N-ZERO) program, which was founded by the US Defense Advanced Research Projects Agency (DARPA). This program aimed to develop a WuRX that consumes less than 10 nW power, corresponding to the self-discharge of a typical button cell battery sitting on a shelf unused [13]. The body of this dissertation's work is based on the outcome from the N-ZERO program.

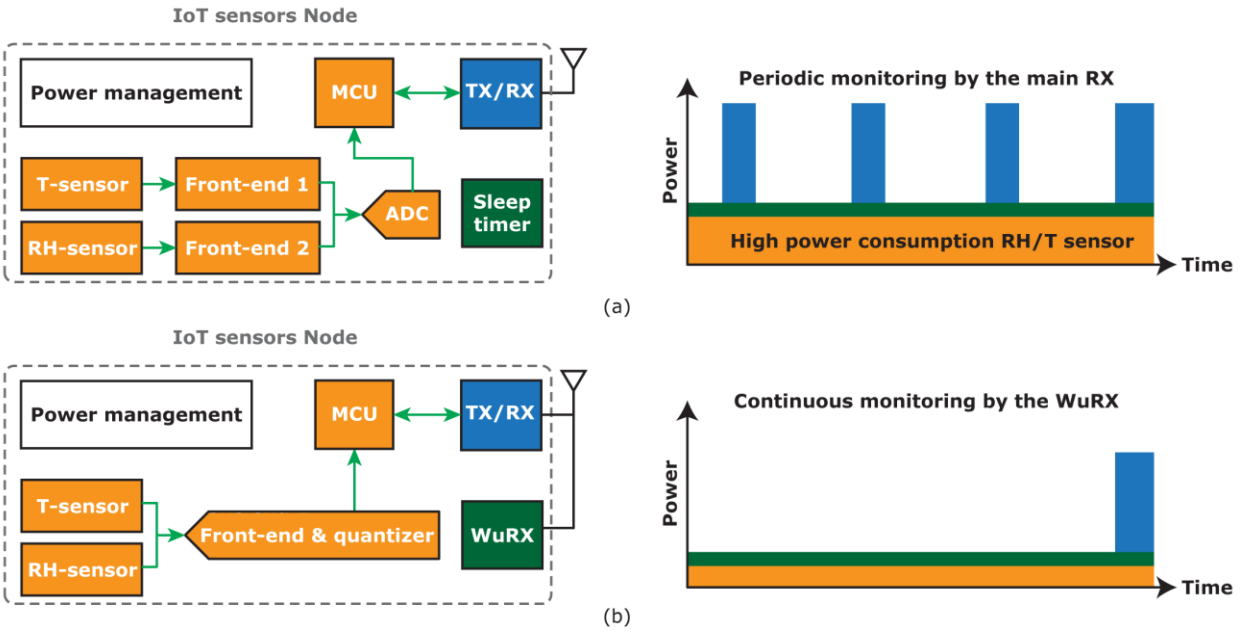


Figure 1.2. Diagram of (a) periodic wake-up and (b) employing a WuRX.

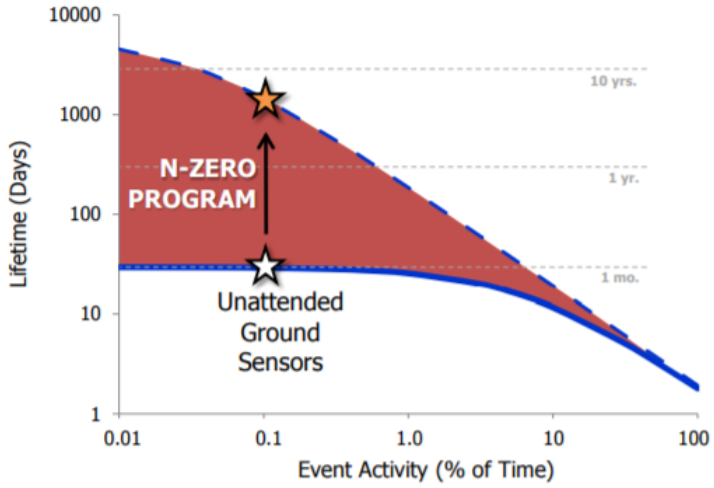


Figure 1.3. N-ZERO circuit power saving as a function of event activity from [12].

1.3 Compound Sensor Using Unified Analog Front-End

One IoT node typically consists of a cluster of sensors, which detect similar physical or chemical parameters to provide a comprehensive assessment. By sharing the micro-processer unit

and the radio, this approach is power- and cost-efficient. For example, an IoT node for surveillance purpose should be equipped with motion, vibration, and sound sensors; while a node for monitoring the food supply chain should be equipped with relative humidity and temperature (RH/Temp.) sensors.

A key challenge in this vision is to combine the sensors in a compact and power efficient manner as they utilize fundamentally different transduction mechanisms and therefore typically require different AFEs. Different mechanisms include voltage [14], current [15], [16], resistive [17], capacitive [18] and inductive [19] transduction. From the circuit perspective, a conventional way to integrate different sensing mechanisms is to convert multiple parameters into the voltage domain, and then use an analog-to-digital converter (ADC) to digitize them. As shown in Figure 1.2(a), this is commonly used architecture for the existing RH/Temp. environmental sensors [20], [21], which show inferior power efficiency and large area cost. Furthermore, the conventional architecture uses two-step data acquisition, *i.e.* an amplifier followed by an ADC, to repurpose the ADC in different modes. This architecture typically requires at least two high gain amplifiers, and hence higher power and complexity, and less gain accuracy [22].

To integrate more sensing mechanisms to a compound sensor more efficiently, this work demonstrates a unified AFE, which digitizes both resistive and capacitive information for RH/Temp. monitoring applications. As shown in Figure 1.2(b), both transducers interact with the AFE directly, and the AFE converts the inputs into a time information, which is then digitized by a built-in quantizer. By using this 2-in-1 approach, power, area, and circuit complexity can be improved significantly. Meanwhile, other design specifications such as linearity and process, voltage, and temperature (PVT) robustness have also been improved. Those specifications are crucial but oft overlooked in IoT applications, which typically are used under poorly regulated

power supply (from either batteries or power harvesters) and operate in uncontrolled environments (compared to a conventional laboratory setting).

1.4 Scope of Dissertation

This dissertation presents the development of the near-zero power WuRXs as well as the RH/Temp. sensor for environmental sensing. The WuRXs presented in this dissertation are categorized into two types: active ED based WuRX and passive ED based WuRX. Although being categorized by the ED types, the difference between them are more than the ED design. The active ED tends to have better driving ability and higher bandwidth, while inferior noise efficiency; on the contrary, the passive ED shows better noise efficiency, at the cost of no driving ability and ultra-high output impedance. Thus, the ED types also influence the BB circuit design, especially, the passive ED demands more stringent requirements on the BB circuits. In Chapter 2 and 3, the two generations of WuRXs, that evolve from the active ED based architecture to passive ED based architecture, are presented. Chapter 4 raises issues of temperature dependence in the WuRX and presents solutions to improve the temperature robustness. Chapter 5 covers the 2-in-1 RH/Temp sensor with a unified front-end that demonstrates state-of-the-art performance. Finally, Chapter 6 presents concluding remarks and future research directions.

Chapter 2

N-zero WuRXs with Active Envelope Detection

2.1 Introduction

WuRXs are low-power radios that continuously monitor the RF environment to wake up a higher power radio upon detection of a pre-determined RF signature. Prior-art WuRXs have 100s of kHz of bandwidth with low signature-to-wake-up-signal latency to help synchronize communication amongst nominally asynchronous wireless devices [23], [24]. However, applications such as unattended ground sensors and smart home appliances wake-up infrequently in an event-driven manner, and thus WuRX bandwidth and latency are less critical; instead, the most important metrics are power consumption and sensitivity, as the power of always-on WuRXs ultimately determines the battery life of low-activity devices, while sensitivity determines the communication distance and therefore deployment cost via the total number of nodes required to achieve a given network coverage. Typically, sensitivity and power consumption trade-off with

one another, making the design of WuRXs that simultaneously achieve both challenging. Fortunately, the relaxed wake-up latency and data rate requirements of low-average-throughput applications can help improve both power consumption and sensitivity by minimizing baseband bandwidth, as will be shown shortly.

There are two primary classes of applications where WuRXs can be useful: 1) high-average-throughput applications, where WuRXs are used to eliminate the need for precision watch-dog timers used to perform network synchronization; and 2) low-average-throughput applications where the network is largely idle, waiting for an event to occur (*e.g.*, infrastructure and perimeter monitoring). In high throughput applications it is important to minimize wake-up detection latency, set in part by the WuRX data rate, so as to not adversely affect the average network throughput. In low throughput applications, wake-up latency (and thus data rate), is less important, as long latency may not adversely affect the overall needed throughput. As an emerging research direction, this thesis focuses on the design of WuRXs used in low-average-throughput applications.

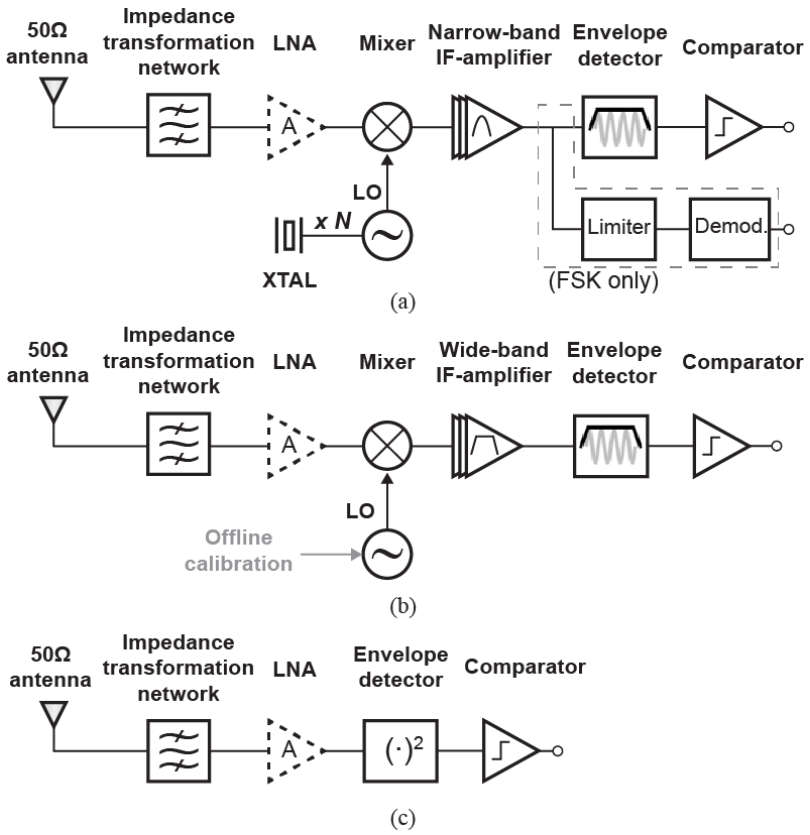


Figure 2.1. Wake-up radio architectures: (a) mixer-based low-IF, (b) mixer-based uncertain-IF, and (c) direct envelope detection.

2.2 Prior WuRX Architectures

Most low-power WuRXs demodulate non-coherent OOK or FSK using one of two general architectures illustrated in Fig. 2.1: a) mixer-based low-or b) uncertain-IF architectures, and c) direct envelope detection architectures.

2.2.1 Low-or Uncertain-IF Architectures

Most conventional radio architectures utilize a LO, often stabilized via a low-frequency crystal by means of injection locking or a PLL, to mix the incoming RF signal down to a known IF prior to demodulation via an ED or other means [Figure 2.1(a)]. Since it is much more power-

efficient to amplify and filter signals at a low IF than at RF, mixer-first low-IF architectures, where an LNA is not included, can consume relatively low power while achieving good sensitivity. For example, achieve -70 dBm and -87 dBm at 200 kbps and 50kbps, respectively. However, even though OOK and FSK are demodulated in a non-coherent manner, the generated LO must be frequency-stable in order to limit bandwidth (and therefore noise) at IF; this requires ~10s of μW when operating between 400-900 MHz, and even more at 2.4 GHz. Thus [25], [26] each consume 44 μW, which is higher than desired for many WuRX applications. For this reason, mixer-based low-IF architectures are typically reserved for WuRX applications operating below 1GHz, and/or where sensitivity is more important than power.

The power consumption of LO generation can be reduced substantially if the frequency stability specifications are relaxed. For example, by replacing a frequency-locked oscillator with a simple free-running digitally controlled ring oscillator, LO generation has consumed 13/20 μW at 2.0/2.45 GHz in prior work [23], [27], respectively. However, mixing an incoming RF waveform with a free-running oscillator whose precise frequency is not well controlled or known requires a large IF bandwidth to guarantee proper reception after envelope detection. Thus, such architectures are called "uncertain-IF" WuRXs. Since even far away interferers can potentially end up in the wideband IF, and these interferers would be demodulated to baseband via the ED, high-*Q* filtering at RF prior to down conversion is required. This can be accomplished using mechanical resonant structures (*e.g.*, BAW or FBAR filters), or via *N*-path filters [28]. Generally, uncertain-IF WuRXs should achieve lower power operation than conventional low-IF WuRXs with similar, though typically slightly worse, sensitivity due to increased noise bandwidth. Recent work on multi-stage *N*-path filters have improved sensitivity via enhanced filtering, albeit at higher power (*e.g.*, -97 dBm at 10 kbps and 99 μW). Thus, mixer-based uncertain-IF WuRXs are capable of

operating at lower power and higher frequencies than mixer-based low-IF WuRXs, with similar, though often slightly poorer, sensitivities.

2.2.2 Direct Envelope Detection Architectures

Many applications such as unattended ground sensor networks, smart home automation, and wearables demand sub-μW power consumption to enable ultra-long battery life. Since LO generation and IF amplification dominate the power consumption of mixer-based architectures, an impactful way to reduce power is to eliminate mixers altogether and directly demodulate to baseband via an envelope detector [Figure 2.1(c)]. Envelope detection can be performed passively by a rectifier [29], or actively via an amplifier biased to maximize second-order non-linearities [24]. The latter approach typically exploits the non-linear exponential *V-I* relationship of a subthreshold MOSFET.

Nominally a passive rectifier offers poor conversion gain; however, multi-stage charge pumps can be employed to achieve similar conversion gain as low-power active EDs, though they suffer from low input impedances, making large passive RF voltage gain structures difficult to implement. However, since EDs demodulate all energy present at their inputs to baseband, such architectures tend to accumulate significant noise and interference, making their sensitivity generally inferior to mixer-based architectures.

2.3 Proposed WuRX Architecture

The architecture of the proposed WuRX is shown in Figure 2.2. The primary optimization objective of this design was to minimize power. This motivated the use of a direct-ED WuRX architecture operating at a low supply voltage (0.4 V in this work). However, the secondary objective was to achieve sensitivity that approaches that of a mixer-based WuRX architecture,

while not significantly compromising tolerance to interferers. This was accomplished through a number of architectural and circuit design techniques described below.

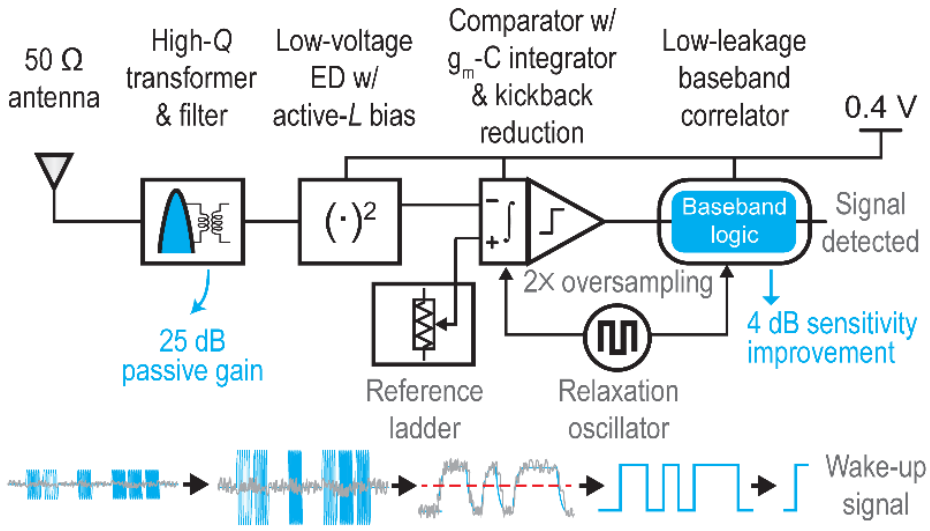


Figure 2.2. Overview of the proposed WuRX.

2.3.1 Direct-ED RF Front-End Optimization

Direct ED architectures demodulate all input RF energy to baseband, and thus any interferers within the input RF bandwidth can inhibit proper reception. In addition, the lack of an LNA together with very low-power demodulating circuits means that the baseband circuit noise often dominates, thereby ultimately limiting the WuRX sensitivity. Fortunately, these two problems, *i.e.* interference and baseband circuit noise, can be overcome via the following techniques:

1) Minimizing the influence of interference via high-Q filtering:

To reduce the impact of in-band blockers in direct-ED or uncertain-IF mixer-based architectures, a high-Q narrow-band filter is needed to minimize RF bandwidth and block

interferers. Most prior-art low-power radios accomplish narrow-band filtering by utilizing high-Q mechanical resonators, which offer attractive narrow filtering capabilities at 1-3 GHz [23]. In this design, however, to attain the highest possible Q for sharp filtering, and, as will be seen shortly, to achieve a large impedance transformation ratio from a 50 Ω source as well as wide communication range, a carrier frequency in the 100 MHz range was selected for use near the FM radio band. Therefore, a high- Q filter (and, as will be described shortly, transformer) was designed out of lumped components directly.

2) Minimizing baseband circuit noise via passive RF voltage amplification:

Envelope detectors are inherently non-linear elements. Unlike linear mixers used for down-conversion, the squaring operation of an ED converts pre-ED noise down to baseband via two mechanisms: self-mixing of noise and noise convolved with the input signal [30]. Since most ultra-low-power WuRXs forgo active gain before the ED, sensitivity is typically limited by baseband noise. Therefore, to improve sensitivity without a power penalty, most direct-ED WuRX designs strive to achieve as much passive voltage gain in the matching network as possible. This is typically achieved by designing the ED to have a large input impedance and matching this large impedance to 50 Ω via an impedance transformation network. Prior work has shown 5 dB and 12 dB of passive voltage gain which, when coupled to either a rectifier or an active ED, achieved sensitivities of -45.5 dBm and -41 dBm at 12.5 kbps and 100 kbps at powers of 116 nW and 98 nW, respectively [24], [29]. Thus, direct ED systems can achieve ultra-low-power operation, yet without large RF voltage gain and low-noise baseband circuits, do so at limited sensitivities.

To address the aforementioned issues, the proposed WuRX incorporates an ED with a high input impedance that, combined with a high-Q impedance transformer, facilitates up to 25 dB of passive voltage gain at RF before being demodulated by the ED, thus directly resulting in a 25 dB

improvement in sensitivity compared to the exclusion of this transformer. Furthermore, the ED is designed to support high conversion gain to further reduce the impact of baseband circuit noise (*i.e.* to increase SNR).

2.3.2 Baseband Bandwidth Consideration

In high throughput applications it is important to minimize wake-up detection latency, set in part by the WuRX data rate, so as to not adversely affect the average network throughput. In low throughput applications, wake-up latency (and thus the data rate of the WuRX), is less important, as long latency does not adversely affect the overall throughput needed. Most conventional WuRX designs target the first class of applications; this work instead focuses on the design of WuRXs used in low-average-throughput LPWAN applications. One of the key ideas of a LPWAN is to leverage the reduced data rate (and thus integrated baseband noise) to improve sensitivity and enable wide communication range. For example, LoRaWAN utilizes a 300 bps to 50 kbps data rate, whereas Sigfox is only 100 bps to 600 bps. Therefore, a 300 bps data rate was selected for this design.

2.3.3 Digital Baseband Processing

The received RF signal employed in this design is modulated with a custom designed 16-bit sequence. After envelope detection in the proposed architecture, the demodulated signal is 2× oversampled and digitized by a 1-bit regenerative comparator. The output of the comparator feeds a digital correlator that computes the Hamming distance between the received and stored sequence. When the Hamming distance is below a programmable threshold (H_{th}), a wake-up signal is generated. It will be shown later that the use of this wake-up sequence provides additional coding gain that improves the sensitivity of the proposed WuRX. Moreover, the correlator prevents false

alarms caused by unwanted jammers. An on-chip relaxation oscillator provides the required 600 Hz clock.

2.4 System Analysis & Modelling

2.4.1 Sensitivity Analysis

Due to the inherent nonlinearity of the direct-ED method, it is difficult and inconvenient to analyze the receiver sensitivity with a conventional noise figure (NF) based approach, which refers the all the noise to the RF input, with respect to the ambient thermal noise (*i.e.* -174 dBm/Hz at room temperature). A more convenient approach, as shown in [30], is referring both noise and signal to the baseband at voltage domain and computing the signal-to-noise ratio (SNR). Generally, there are four steps in calculating the sensitivity:

1) Computing the signal amplitude after the ED, using parameters such as the RF front-end voltage gain, A_V, and the ED scaling factor, k.

2) Computing the BB referred RF noise, $\sigma_{n,RF}$, including the ambient thermal noise floor and RF amplifier (optional) noise. Due to the nonlinear operating, those noise sources mix with either themselves or the signal. Thus, the RF noise shown in the BB is signal dependent if the signal is large or the RF bandwidth is narrow. The method to compute the BB referred RF noise is elaborated in [30].

3) Computing the BB noise, $\sigma_{n,BB}$, which includes the output referred ED noise and the input referred BB amplifier/comparator noise. Note, it is relatively easy to compute/simulate the ED output noise with its small-signal BB model by ignoring all the nonlinear effects [31].

4) Computing the sensitivity by comparing the SNR versus the minimum required SNR, SNR_{mim}, which is determined by the coding. If no coding is used, SNR_{mim} is 11 dB for a bit-error rate (BER) of 10^{-3}.

In the direct-ED method in this work, *i.e.* high-*Q* RF filtering and no active RF amplification, it is most likely always true that the BB noise is dominating. Thus, the step (2) shown above can be skipped for simplicity. The simplified direct-ED WuRX sensitivity is

$$P_{sen} = \frac{\sqrt{SNR_{min} \times \sum \sigma_{n,BB}^2}}{50kA_V^2}, \quad 2.1$$

whose unit is in milliwatt (mW). This equation works as a guidance to all WuRX design: higher RF gain, higher conversion gain, lower BB noise, and a longer code lead to better sensitivity collectively.

The noise and sensitivity breakdown of this work is shown in Table 2.1. It can be observed that the RF noise has nearly no effect on the overall sensitivity, while the BB referred ED noise dominates the noise, followed by the comparator.

Table 2.1. WuRX sensitivity breakdown

Noise @ Comparator Input Node	Sensitivity Limitation by Noise Source @ BER=10^{-3}
Signal ⊗ RF Noise	-126.7dBm
Self-Mixed RF Noise	-122.1dBm
ED Noise	-67.3dBm
Comparator Noise	-69.2dBm
Ref. Ladder Noise	-75.2dBm
Total Noise	-66.5dBm
Measurement Result	-65.0dBm

2.4.2 Simulink Behavior Model

To model the WuRX system behavior, a Simulink model was established (Figure 2.3). Signal sequence, ambient thermal noise and interference serve as the model inputs. The ED is modeled by a square function, followed by a 1st order low-pass filter. The BB noise is modelled as bandlimited white noise. A fast version was also built by using a stored rectified signal sequence as the input (Figure 2.4). Since RF noise is negligible, by removing the RF and conversion operations, only modelling the BB behavior, the simulation speeds up by ~10^6×. With the fast version, Monte Carlo simulation was applied to the system for a large run numbers (>10^4) to obtain the statistics of missed detection and false alarms.

This model validates some the sensitivity analysis shown above and the codeword effectiveness. It also helps to choose an appropriate sampling rate, *i.e.* 2× the data rate, which is a tradeoff between power and possibility of missing bits. Some nonidealities (difficult for analytical analysis), such as asynchronous operating, clock drift, and comparator threshold voltage drift have been applied to this model.

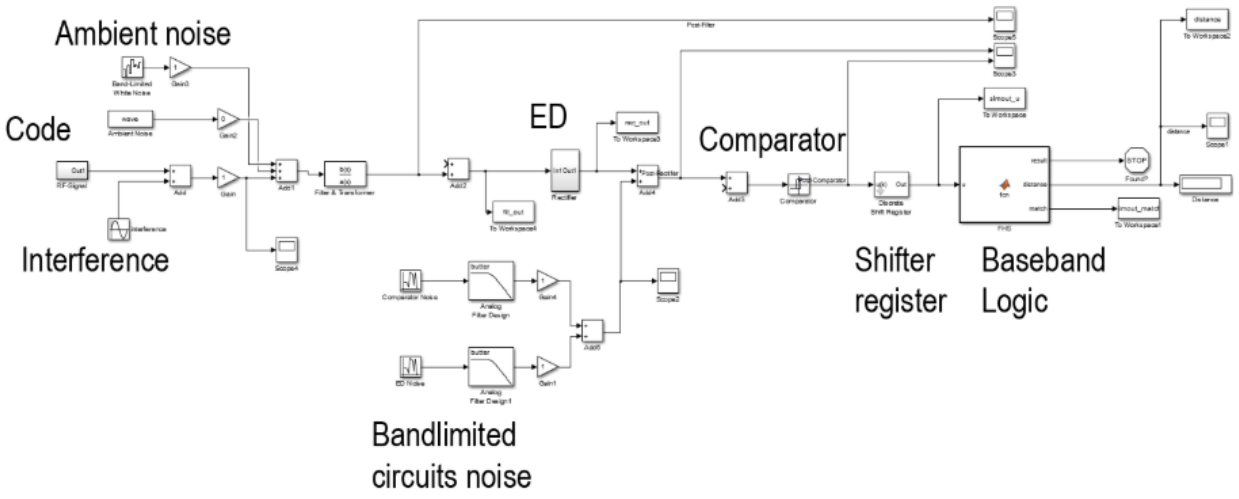


Figure 2.3. WuRX Simulink model.

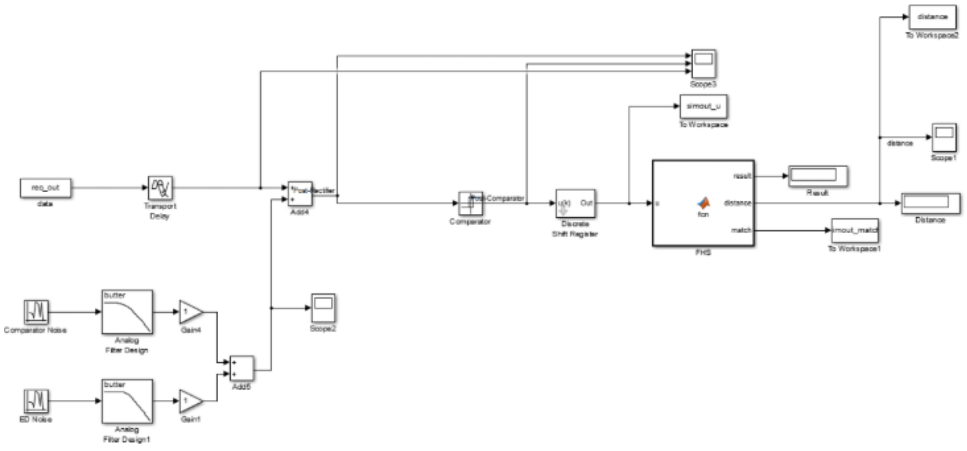


Figure 2.4. WuRX BB Simulink model.

2.5 Circuits Implementation

2.5.1 Transformer/Filter

The purposes of the transformer/filter is to impedance transform a 50 Ω source impedance to a much larger value to facilitate passive voltage gain, while also performing high-Q RF filtering. The schematic of the implemented transformer/filter is shown in Figure 2.5(a) were R_s is the 50 Ω source impedance. The primary stage resonator is formed by L_P and C_P, while the secondary stage is formed by L_S and C_S, with k denoting the coupling coefficient between L_P and L_S. C_{chip} and R_{chip} are the equivalent input impedance of the chip at the carrier frequency, which connects to the transformer/filter via a large ac-coupling capacitor, C_{BLK}, and a small parasitic inductor from the PCB trace and bondwire. The primary and secondary stage tanks both resonate at the same operating frequency, f_{RF}=113.5 MHz. Departing from a traditional 2-port RF filter, which has 50 Ω matching at both ports, the proposed transformer/filter not only provides a 2nd order filter response for interference rejection, but also realizes impedance transformation between the two

ports to achieve passive voltage gain. To analyze the circuit, an equivalent circuit model is derived as shown in Figure 2.5(b). L_M is determined by k and can be written as:

$$L_M = k\sqrt{L_P L_S} = kL_S\sqrt{\frac{1}{N}}, \quad 2.2$$

where N is the turn ratio between L_P and L_S. C_{SE} and R_{SE} are the equivalent capacitor and resistor of the secondary stage, with $C_{SE}=C_S+C_{chip}$ and $R_{SE}=R_{EQ,P}||R_{chip}$, where $R_{EQ,P}$ is due to the finite Q of L_S. Therefore, the maximum passive voltage gain the transformer/filter can achieve at f_{RF} is:

$$Gain_{max} = \sqrt{\frac{R_{SE}}{R_S}} = \sqrt{\frac{R_{EQ,P}\|R_{chip}}{R_S}}. \quad 2.3$$

To get large passive voltage gain, a large $R_{EQ,P}$ must be achieved by either increasing Q or L_S for a given C_{SE}. Since Q can only be pushed so high using practical inductors, L_S is the only practical tunable parameter. There are two things that limit the achievable value of L_S: 1) the chip input capacitance, C_{chip}, and 2) the self-resonant frequency of the inductor. With C_S=0 and C_{chip}=1.8 pF, the maximum L_S is 1.06 μH. Due to the size of the required inductor, it must be off-chip. For commercial inductors with high Q, self-resonance typically occurs when $\omega L\approx$1,400 Ω. To account for variation in C_{chip} and on-board parasitics, $\omega L\approx$520 Ω was chosen. From the datasheet [32], a Q of 150 can be obtained at 115 MHz, and thus $R_{EQ,P}$<78 kΩ.

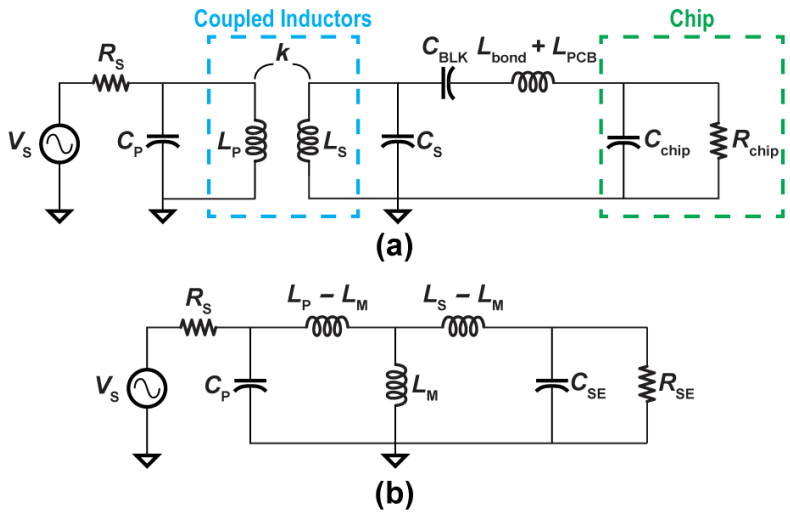


Figure 2.5. Schematic of (a) transformer/filter and (b) equivalent circuit model.

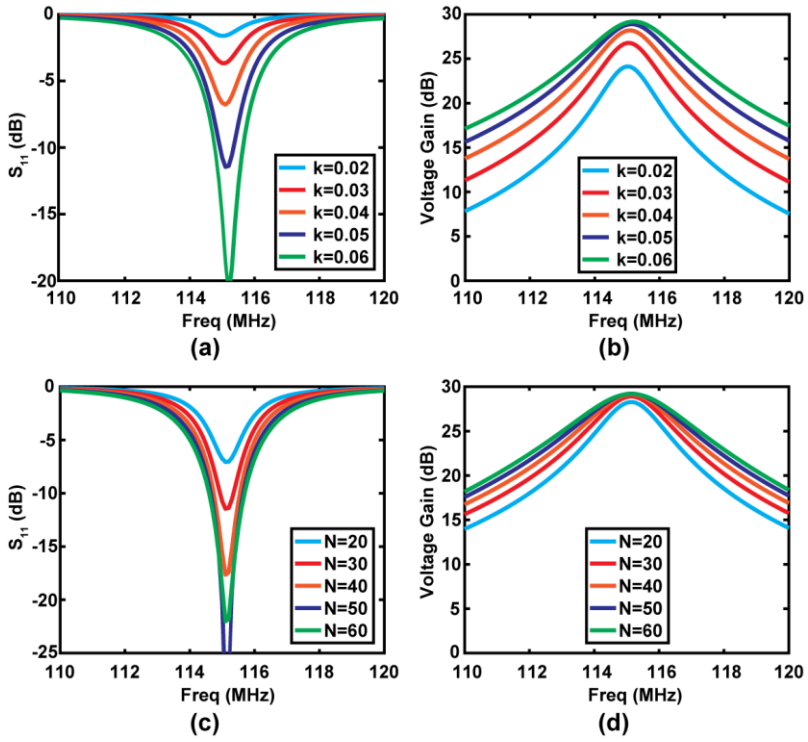


Figure 2.6. Plot of (a) S_{11} vs. k; (b) voltage gain vs. k; (c) S_{11} vs. N; (d) voltage gain vs. N.

After determining the value of L_S and C_S, we considered the coupling coefficient k and the turn ratio N, both of which affect the input matching and passive voltage gain. To have a sharper

filter response for out-of-band interference rejection, k should be small and Q should be large [33]. Figure 2.6(a) and (b) show calculated S_{11} and voltage gain of the transformer/filter varying k with N fixed to be 30. When k is increased from 0.02 to 0.06, the input matching gets better and the voltage gain increases. However, the filter bandwidth also increases. Figure 2.6(c) and (d) show calculated S_{11} and voltage gain varying N with k=0.05. When N is increased from 20 to 60, the voltage gain does not increase much, but with considerably larger filter bandwidth. Therefore, k=0.05 and N=30 were chosen as a compromise between input matching, voltage gain, and filter bandwidth. Calculations show that S_{11} is better than -10 dB with a passive voltage gain of 28.9 dB and a 3-dB bandwidth of 2.4 MHz.

The key challenge in implementing the proposed transformer/filter is to control the coupling despite the large difference in inductance (720 nH and 24 nH). Implementing the inductors using only lumped elements would make it very hard to control the coupling through positioning, whereas only distributed inductors would take too much area. As such, we used a combination of lumped inductors (220 nH and 160 nH from Coilcraft) and a distributed inductor to realize L_S and a distributed inductor to realize L_P, which has three advantages. First, L_S is realized by both distributed and lumped inductors, thus the value can be large. Second, the coupling is realized by the distributed parts of L_P and L_S, and thus k is determined by the length and gap of the coupling PCB traces. With modern PCB fabrication techniques, this coupling can be controlled precisely, which is crucial since k affects both passive gain and filter bandwidth. Third, the use of both lumped and distributed inductors provides more freedom to design the transformer. For example, the center frequency can be easily tuned by replacing lumped components, which is an advantage compared to mechanical resonators [23], [34].

Figure 2.7 shows the 3-D model of the transformer/filter. To reduce the dielectric loss, a Rogers RO4003C substrate was used (ε_r= 3.55, thickness of 20 mil, and a loss tangent of 0.0027). From HFSS simulations, we found that at 115 MHz, L_P and L_S are 28 nH and 756 nH, respectively, and k= 0.05. All of the component values are close to the desired values from calculation. The simulated voltage gain was 26.6 dB with a bandwidth of 2.2 MHz.

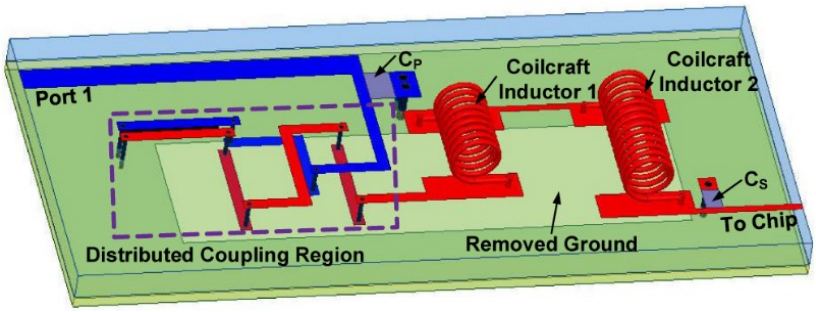


Figure 2.7. 3-D model of the transformer/filter.

2.5.2 Envelope Detector

To take full advantage of the gain provided by the transformer/filter, the ED must provide a large enough input resistance R_{chip} so as to not to degrade the corresponding $R_{EQ,P}$. Although a passive N-stage RF rectifier [24], [29] is a tempting choice (due to the zero power consumption), it is difficult to achieve high enough R_{chip}. Thus, in this work an active ED was selected. A transistor biased in the sub-V_t region can not only operate with a low supply voltage and low power consumption, but also provides an exponential voltage-current relationship. Assuming the transistor is operating in the sub-V_t saturation region (*i.e.* V_{DS}>100 mV) with negligible drain-induced barrier lowering (DIBL), the current can be written as [35]:

$$i_{DS} = \mu C_{ox} \frac{W}{L} (n-1) V_T^2 e^{\frac{v_{GS}-V_t}{nV_T}}, \quad 2.4$$

where μ is the mobility, C_{ox} is the oxide capacitance, W is the transistor width, L is the transistor length, n is the sub-V_t slope factor, V_T is the thermal voltage ($k_B T/q$), and v_{GS} is the gate-to-source voltage. This exponential relationship results in a 2nd order non-linearity used for the desired ED functionality.

The second order transconductance is given by:

$$g_{m2} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS}}{\partial v_{GS}^2} = \frac{I_{DS}}{2(nV_T)^2}. \quad 2.5$$

In an SOI process, the floating body can be connected to the gate directly without using deep n-well devices, commonly referred to as the DTMOS configuration [36], to achieve additional 2nd order non-linearity via threshold voltage modulation. The additional transconductance can be derived as:

$$g_{mb2} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS}}{\partial v_{BS}^2} = (n-1)^2 g_{m2}. \quad 2.6$$

For the process used in sub-V_t, n≈1.4, meaning that the DTMOS configuration provides an additional 16% transconductance compared to gate input only.

Conventional common source ED biasing schemes use either a diode-connected load or a resistive load. Unfortunately, the diode connected load results in a low output resistance (similar to a source follower ED) and only achieves high conversion gain with large input signals, while a resistive load has limited conversion gain with a 0.4 V supply voltage. Other techniques such as a cascode level shifter provide high output resistance, but require extra voltage headroom [24] not compatible with the employed 0.4 V supply.

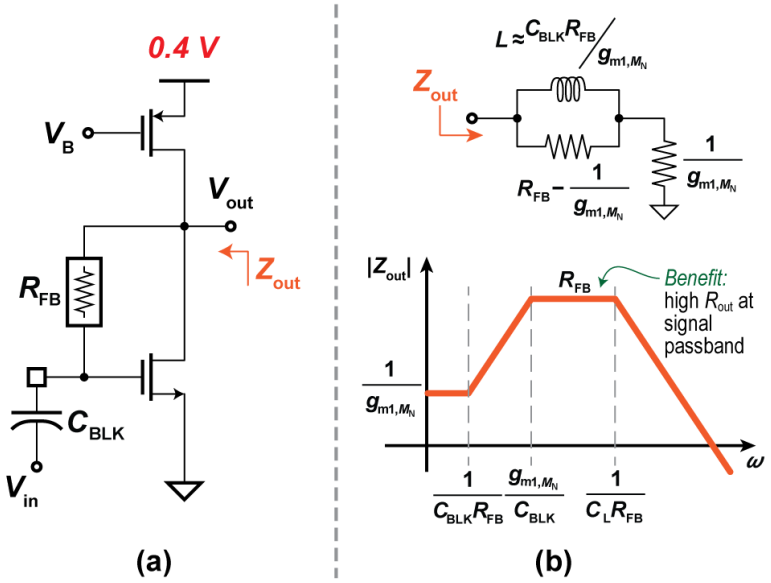


Figure 2.8. (a) Schematic of proposed active-L biased ED; (b) active-L biasing circuit model and Bode plot of ED output impedance.

To address the aforementioned issues, an active-L self-biased ED was designed [Figure 2.8(a)]. The feedback resistor sets the DC voltage for both the gate and drain nodes of the input transistor and serves as the output impedance. The output impedance can be written as:

$$Z_{\text{out}} = \left(\frac{g_{\text{m1}}+sC_{\text{BLK}}}{1+sC_{\text{BLK}}R_{\text{FB}}} + \frac{1}{r_{\text{o}}} + sC_{\text{L}}\right)^{-1}, \tag{2.7}$$

where g_{m1} is the transconductance of the NMOS, C_{BLK} is the AC-coupling capacitor, R_{FB} is the feedback resistor, r_{o} is the small-signal intrinsic output resistance of the transistor, and C_{L} is the capacitance at the output node. Assuming $r_{\text{o}} \gg 1/g_{\text{m1}}$ and R_{FB} because of the low current (5 nA in this design, which results in $r_{\text{o}} \approx$1 GΩ and $1/g_{\text{m1}} \approx$7 MΩ), $C_{\text{BLK}} \gg C_{\text{L}}$, and $C_{\text{BLK}}/g_{\text{m1}} \gg C_{\text{L}}R_{\text{FB}}$, thus it can be simplified to:

$$Z_{\text{out}} \simeq \frac{1}{g_{\text{m1}}} \cdot \frac{1+sC_{\text{BLK}}R_{\text{FB}}}{\left(1+s\frac{C_{\text{BLK}}}{g_{\text{m1}}}\right)(1+sC_{\text{L}}R_{\text{FB}})}, \tag{2.8}$$

which contains two poles and one zero. The equivalent circuit model and Bode plot of Z_{out} are shown in Figure 2.8(b). It can be seen that the output impedance is boosted to R_{FB} within the signal passband due to the active-L biasing, which leads to higher conversion gain. Since non-return-to-zero (NRZ) signaling is used, the high pass corner must be low enough to not attenuate the signal power and is set to 20 mHz in this design for < 0.01 dB SNR degradation from baseline wander. Therefore, an off-chip C_{BLK} was used as a DC block and incorporated into the bias network.

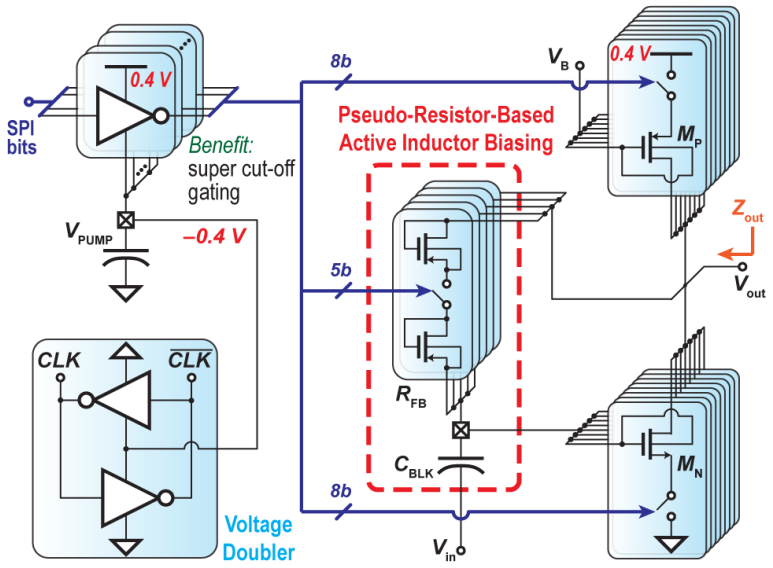


Figure 2.9. Full schematic of the proposed low-voltage active-L biased DTMOS ED with boosted binary-weighted SPI control.

The full ED schematic is shown in Figure 2.9. Due to significant process variation in sub-V_t circuits, both M_N and M_P were designed to have 8-bit binary-weighted tuning capability. To reduce the leakage of unused M_N via super-cutoff biasing, and to turn on M_P strongly, a voltage doubler [37] was designed to provide -0.4 V, saving up to 3 nA in simulation (at the TT corner). Because of the high required value of the feedback resistor, a MOS-bipolar-pseudo-resistor was used instead of a poly resistor to prevent high capacitive loading of the input node at RF, which

ultimately limits the achievable inductor value of the second stage of transformer/filter, and therefore passive voltage gain. For the same reasons as above, and to make the baseband bandwidth tunable, the pseudo-resistor was implemented with 5 binary-weighted bits. Since the baseband bandwidth is 300 Hz, all critical transistors were sized to trade-off the contributions of $1/f$ noise while minimizing parasitic capacitance at the output node, the latter of which ultimately limits the achievable R_{FB} to ~100 MΩ.

The demodulated output signal of the ED is:

$$v_{\mathrm{out}} = Conv_{\mathrm{Gain}} \cdot v_{\mathrm{in}} = \frac{k_{\mathrm{ED}}}{2} \cdot v_{\mathrm{in}}^2, \tag{2.9}$$

where $Conv_{\mathrm{Gain}}$ is the conversion gain of the ED, v_{in} is the input signal amplitude, and k_{ED} is the ED scaling factor (in units of $1/V$). Thus, the k_{ED} of the designed ED in the signal passband is given by:

$$k_{\mathrm{ED}} = (g_{\mathrm{m2}} + g_{\mathrm{mb2}}) \cdot Z_{\mathrm{out}} \approx [1 + (n-1)^2] \cdot \frac{I_{\mathrm{DS}}}{2(nV_{\mathrm{T}})^2} \cdot R_{\mathrm{FB}}, \tag{2.10}$$

which is only dependent on design parameters.

To compare the two conventional biasing schemes with the proposed active-L biasing scheme, the SNR at the ED output was calculated. Assuming all three biasing schemes use the same DTMOS configuration as the input stage, the SNR can be written as:

$$SNR = \frac{(g_{\mathrm{m2}}+g_{\mathrm{mb2}})^2 \cdot \frac{v_{\mathrm{in}}^4}{4} \cdot R_{\mathrm{out}}^2}{\overline{i_{\mathrm{n,ED}}^2} \cdot R_{\mathrm{out}}^2 + \overline{v_{\mathrm{n,comp}}^2}}, \tag{2.11}$$

where $\overline{i_{\mathrm{n,ED}}^2}$ is the total integrated noise current of the ED input transistor, R_{out} is the output resistance in the passband, and $\overline{v_{\mathrm{n,comp}}^2}$ is the total input-referred noise of the comparator. It can be shown that if the ED loading and comparator are noiseless, the SNR is independent of R_{out} and

all the biasing schemes would have the same SNR. However, if $\overline{v_{\mathrm{n,comp}}^2}$ is significant compared to the ED noise, higher R_{out}, and therefore higher k_{ED} lead to better SNR. Simulation with an ED current of 5 nA and a 3.2 mV input signal for these three bias schemes is depicted in Figure 2.10. If the comparator noise is large, the active-L self-biased scheme achieves the highest SNR.

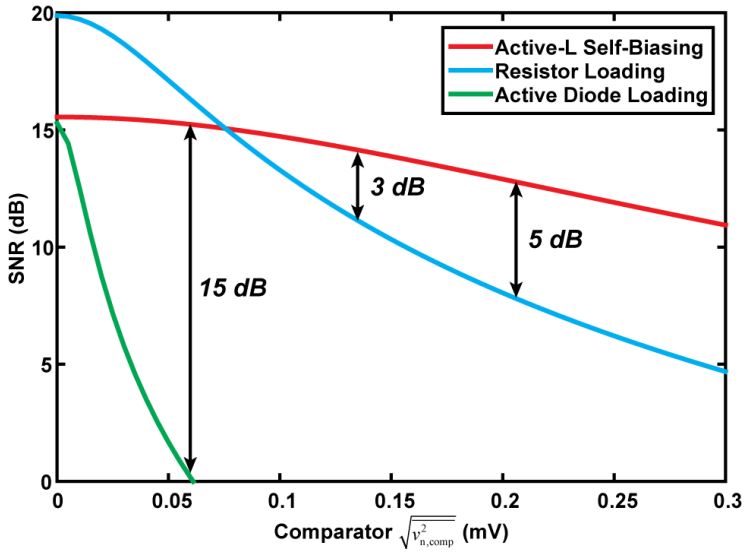


Figure 2.10. Simulated ED output SNR vs. integrated comparator noise voltage for different biasing schemes.

2.5.3 Comparator and S/H Stage

The output of the ED is digitized by a comparator, which serves as a 1-bit quantizer. Due to the 2× oversampling, the comparator operates at 600 Hz. As shown in Figure 2.11(a), the comparator is implemented with a $g_{\mathrm{m}}C$ integrator as a preamplifier followed by a regenerative latch [38]. The operation is as follows: 1) Once $\overline{\phi}$ goes low, a current determined by the inputs is integrated on C_{F} until 2) the voltage crosses the latch threshold voltage, $V_{\mathrm{threshold}}$, after which 3) the positive feedback latch regenerates producing complementary rail-to-rail outputs [Figure

2.11(b)]. The two-stage dynamic comparator is then reset by the other phase of the clock and ready for the next cycle.

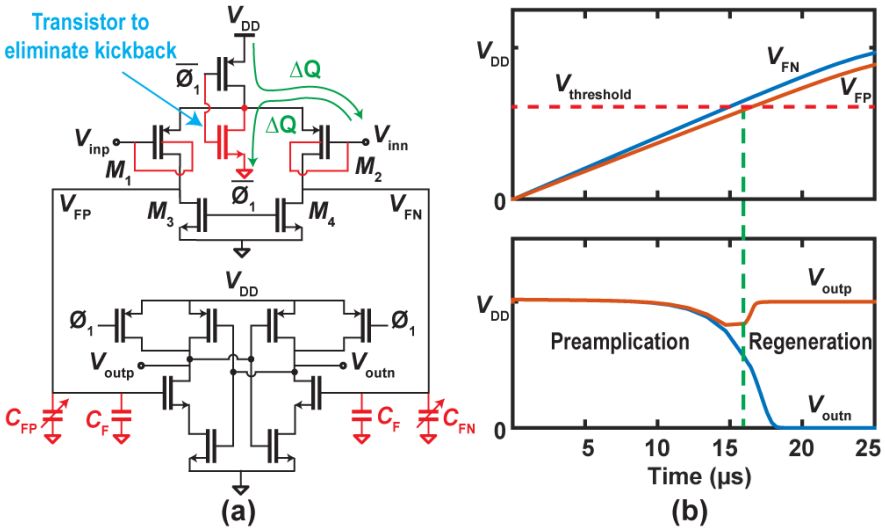


Figure 2.11. (a) Schematic of the dynamic two-stage comparator, and (b) simulation showing 1st/2nd stage output voltages.

This two-stage comparator has three dominant noise sources: 1) thermal noise from the input transistors $M_{1,2}$, 2) sampling noise from the reset switches $M_{3,4}$, and 3) the input-referred noise from the latch. If the input common-mode voltage of the preamplifier is mid-supply (200 mV), the input transistors operate in subthreshold. Therefore, the input-referred thermal noise of the input pair can be written as

$$\overline{v_{n1}^2} = 2\frac{2qn^2V_T^2}{I_{ds1}}NBW, \qquad 2.12$$

where I_{ds1} is the DC current of $M_{1,2}$, n is the subthreshold slope factor (typically ~1.4-1.6), V_T is the thermal voltage, and NBW is the noise bandwidth. The NBW is inversely proportional to the integration time T_{int} of the first stage [38], and given by

$$NBW = \frac{1}{2T_{\text{int}}} = \frac{I_{\text{ds1}}}{2V_{\text{threshold}}C_{\text{F}}}. \quad 2.13$$

Since the 1/*f* noise corner in subthreshold design is typically much lower than the *NBW,* it does not significantly contribute to the overall noise. When the differential input signal is small, $V_{\text{threshold}}$ is relatively constant at a fixed input common-mode voltage and can be extracted from simulation.

Transistors $M_{3,4}$ introduce sampling noise during the reset phase, and this input-referred noise is

$$\overline{v_{\text{n2}}^2} = \frac{1}{A_{\text{V}}^2}\frac{2k_{\text{B}}T}{C_{\text{F}}}. \quad 2.14$$

The differential gain A_{V} of the preamplifier is given by

$$A_{\text{V}} = \frac{g_{\text{m1}}T_{\text{int}}}{C_{\text{F}}} = \frac{V_{\text{threshold}}}{nV_{\text{T}}}, \quad 2.15$$

where $g_{\text{m1}}=I_{\text{ds}}/nV_{\text{T}}$ in subthreshold region. The gain is independent of C_{F} in the conventional G_{m}-*C* integrator.

Lastly, the latch also has noise, although the calculations require accounting for the significant nonlinearity and time-varying behavior. As such, the latch input-referred noise is expressed as

$$\overline{v_{n3}^2} = \frac{1}{A_{\text{V}}^2}\frac{2\alpha k_{\text{B}}T}{C_{\text{L}}}, \quad 2.16$$

where the scaling factor α depends on the latch sizing and C_{L} is the load capacitance [39]. Since $V_{\text{threshold}}$ is typically 200-300 mV, $\overline{v_{\text{n2}}^2}$ is always much smaller than $\overline{v_{\text{n1}}^2}$, and can be neglected.

The preamplifier is typically designed with a moderate integration gain of ~5 V/V to suppress the latch input-referred noise. Therefore, the preamplifier usually dominates the noise performance of the entire comparator. As can be observed, adding matched capacitance at the

preamplifier output prolongs the integration time and limits preamplifier noise bandwidth, which effectively reduces the comparator noise. In this design, a 480 fF MIM capacitor was used and placed in a common-centroid manner to ensure good matching. Compared to the same comparator without explicitly loading the preamplifier, the noise power is reduced by 8× while the power consumption increases by only 5× in simulation because of the $C_{\mathrm{F}}V_{\mathrm{DD}}^2$ energy. Since the comparator is operating at a low speed and the dynamic power of the preamplifier is minimal, loading the preamplifier results in a good noise versus power trade-off. Moreover, as shown in Fig. 2.10(a), the input pair also uses a DTMOS configuration, which increases the transconductance resulting in a lower input-referred noise at no power cost. Simulation shows that the effective transconductance increases by 51% and the noise power reduces by 66%. With the help of loading preamplifier and increased transconductance, the simulated comparator noise was suppressed from 505 $\mu\mathrm{V}_{\mathrm{RMS}}$ to 104 $\mu\mathrm{V}_{\mathrm{RMS}}$.

The comparison threshold voltage is tuned with a dual 5-bit binary weighted capacitor DAC (CDAC) in parallel with C_{F}. By changing the loading capacitance, the comparator offset voltage changes accordingly. Assuming the capacitance difference between the two outputs (ΔC_{F}) is much less than C_{F}, the comparison threshold voltage can be written as

$$v_{\mathrm{os,DAC}} = \frac{\Delta C_{\mathrm{F}}}{C_{\mathrm{F}}} \cdot n \cdot V_{\mathrm{T}}, \tag{2.17}$$

Thus, the threshold voltage increases linearly with ΔC_{F}, and is constant after the CDAC is configured. The CDAC is using MOM capacitors with a unit capacitance of 3.7 fF (C_{F}=0.65 pF), corresponding to ~200 μV resolution. A reference ladder provides a voltage reference to the negative terminal of the comparator. The reference ladder contains 64 diode-connected PMOS

transistors in series. A 5-bit mux selects the output node as the reference voltage, providing a tuning step size of 6.25 mV and a range of 200 mV.

The biggest challenge with this dynamic architecture is the comparator kickback via C_{gs}, C_{bs}, C_{gd}, and C_{bd}. Due to the unbalanced output impedances of the ED (~100 MΩ||1.7 pF) and the reference ladder (~2 GΩ||50 pF), the kickback charge introduces unequal voltage perturbations. This voltage difference would lead to a comparison error in subsequent cycles since the time constant at both nodes is much larger than one clock period. To eliminate this error, two techniques were implemented: 1) An additional reset transistor was placed at the source of the input pair, which insures that the V_{gs} always resets to V_{DD}, such that the same amount of charge is injected into the input when ϕ is asserted high and is removed when ϕ is deasserted [Figure 2.12(a)]. This results in zero net kickback charge into the ED and reference ladder during each cycle, preventing incomplete settling. 2) A S/H stage was added in front of the comparator that provides matched impedances for both inputs and temporarily stores the kickback charge. The sampling capacitor is 1.9 pF, much larger than the parasitic capacitance of the input transistor. Therefore, the only kickback effect is a ~2 mV common-mode spike at the comparator input, which does not lead to a comparison error. The sampling capacitor and the ED output capacitance limit the baseband bandwidth to 300 Hz.

An early-reset feedback was implemented to generate a two phase non-overlapping clock efficiently and save comparator dynamic power simultaneously. As illustrated in Figure 2.12, the comparator resets once the comparator output is latched, such that the dynamic power of the integrator is reduced from $2fC_{\mathrm{F}}V_{\mathrm{DD}}^2$ to $2fC_{\mathrm{F}}V_{\mathrm{threshold}}^2$. Since a large capacitance C_{F} is added, the power savings are significant. Simulation shows that 33% of total comparator power is saved when the WuRX RF input power is -69 dBm, or 0.7 mV at the comparator input. The early-reset

feedback was implemented as shown in Figure 2.12(c), where an SR-latch captures the rising edge of either $V_{\mathrm{outb+}}$ or $V_{\mathrm{outb-}}$ and asserts CLK to "low" to turn off the integration. The non-overlapping phases are generated with two inverter chains: one creates a pos-edge delay and the other creates a neg-edge delay. The pos-edge delay was created by four cascaded inverters, where the first was designed to be high-skewed followed by a low-skewed inverter with $W_{\mathrm{P}}/W_{\mathrm{N}}$ of 6 and 0.5, respectively. Similarly, the neg-edge delay was created by flipping the order of the skewed inverters. Compared to a conventional two-phase clock generator where cascaded latches are used, this method has lower power consumption with a 0.4 V supply.

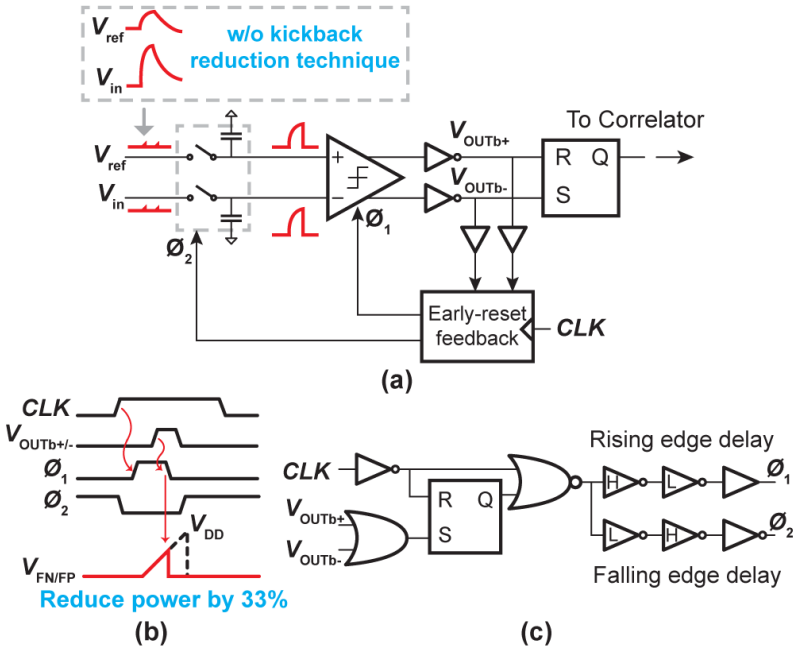


Figure 2.12. (a) Schematic of the comparator, S/H stage and clocking; (b) timing diagram of the of the early-reset feedback; (c) schematic of the early-reset feedback.

2.5.4 Digital Baseband

Figure 2.13. Digital correlator baseband logic with wake-up signal output driver. shows the digital baseband correlation logic that processes the incoming data from the comparator. With the

lack of a power hungry PLL for synchronization, the correlator provides an energy efficient way to overcome phase asynchronization by operating with a 2× oversampling rate to sample the incoming bits [40]. An optimal 16-bit code sequence (1110101101100010) was designed such that it has both a large Hamming distance from all of its shifted versions (D=9) and from the all-0 sequence (D=9). A family of codes also exists, but with slightly lower Hamming distances (D≤8). As the input sequence shifts along the D flip-flop chain, the correlator computes the Hamming distance between the sequence and the programmable 32-bit oversampled code book. Once the value is below a preset threshold, the desired pattern is declared detected and the correlator generates a wake-up signal. To drive the main receiver with a higher supply voltage, the output driver was designed to generate a >1 V signal with 5 ms duration assuming a 10 pF load. When the correlator sends a wake-up signal to the driver, it resets a 4-bit counter and the signal is latched to leave the cascode voltage doubler enabled until the counter rolls over. The charge pump and counter make the wake-up signal look like a ramp. Also, to use the same 0.4 V supply, the digital baseband operates in the sub-V_t region and a custom logic gate library using thick oxide device was designed. All the gates were designed using only inverters and transmission gates for the highest robustness in subthreshold [41].

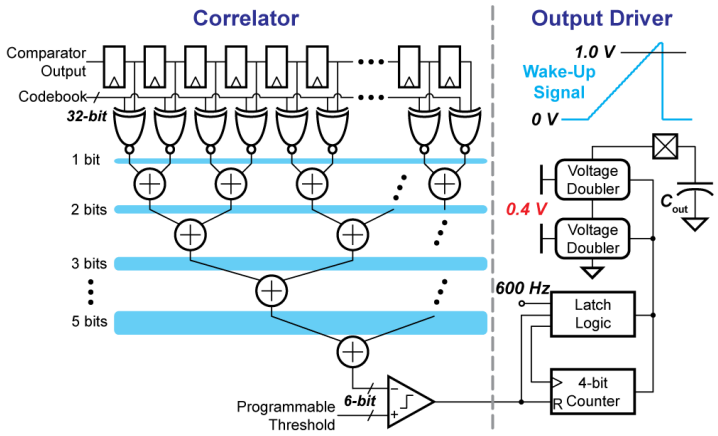


Figure 2.13. Digital correlator baseband logic with wake-up signal output driver.

From a static performance perspective, digital logic gates operating in the sub-V_t region need extra attention to the transistor sizing to overcome process variation. To see this, the inverting threshold V_M of an inverter with minimum width and length NMOS was simulated across the width of the PMOS at different process corners [Figure 2.14(a)], where the solid and dashed lines correspond to a 0.4 V and 1.0 supply voltage, respectively. For an ideal inverter with a negligible transition region, the noise margin is equal to the lower value of either V_M or $V_{DD} - V_M$. It can be seen that the inverter maintains larger than 30% V_{DD} noise margin when operating above-V_t across all corners, while it fails when operating in the sub-V_t region without proper sizing. Another important design consideration comes from power dissipation. For a digital circuit, it is well known that the power consumption can be written as:

$$P_{tot} = P_{leak} + P_{dyn} = V_{DD} I_{leak} + \alpha C_L V_{DD}^2 f, \tag{2.18}$$

where I_{leak} is the average leakage current, α is the activity factor, C_L is the load capacitor, and f is the clock rate.

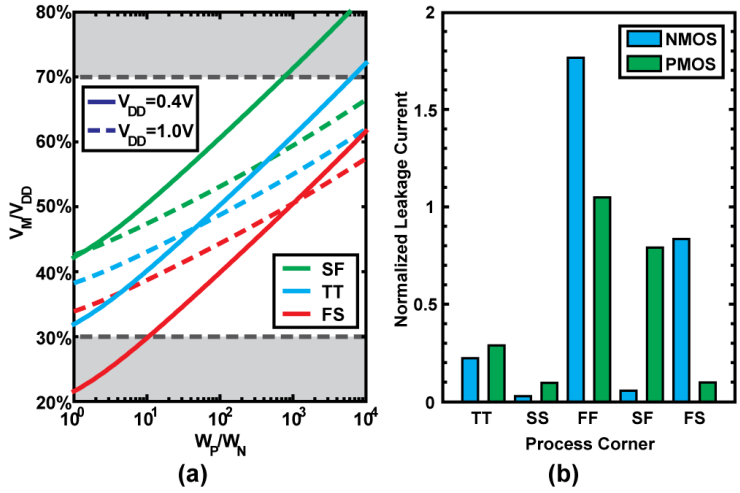


Figure 2.14. (a) Simulated switching threshold for inverter with minimum width and length across different corners and supply voltages; (b) simulated normalized leakage current of the designed inverter across corners.

In addition to the low clock rate, since ideally the correlator only computes when the signal pattern changes, α is nearly zero, both of which make leakage power dominant and thus the design target here. To equate the NMOS and PMOS leakage in this process where the PMOS has lower mobility and V_{t} is 90 mV higher than an NMOS in the TT corner, 5× NMOS devices are stacked. Moreover, the PMOS is re-sized to 1.6× larger width to achieve 30% V_{DD} noise margin even in the worst-case FS corner. Figure 2.14(b) shows the leakage current of the designed inverter across corners, which is normalized to the leakage current of a minimum size inverter at TT. The normalized I_{leak} is 0.26 in the TT corner and 1.41 in the FF corner.

2.5.5 Relaxation Oscillator

The system clock for the comparator, digital baseband, and charge pump is generated from a relaxation oscillator. As shown in Figure 2.15, the oscillator is composed of a reference generator, where one branch is shared with a pseudo-differential common-gate comparator, an inverter buffer chain, and a reset switch. The reference generator with all four transistors operating in the sub-V_{t} region, generates a reference current I_{REF} and a reference voltage V_{REF} through an off-chip resistor. I_{REF} is used to charge a MIM capacitor that is connected to a common-gate comparator (shown in the dashed box). The comparator output is pulled high after V_{INT} exceeds V_{REF}. Then the inverter chain is triggered to close the reset switch and reset the integration capacitor. The capacitor is charged and discharged periodically with a period of $\sim RC$. The clock buffer was implemented with current-starved inverters whose delay are determined by the I_{REF}, which has better energy efficiency than dynamic inverters (CV_{DD}^2). Since the power consumption is largely determined by the static power of the reference generator and comparator, the oscillator power consumption can be minimized by using a large bias resistor. The resistor was chosen to be

30 MΩ and I_{REF} to be ~0.5 nA. To compensate the variation of the capacitor value and comparator delay, the off-chip resistor is tuned to adjust the oscillation frequency to 1.2 kHz. The oscillator output is divided and buffered to a 600 Hz system clock with 50% duty cycle. The frequency varies from 617 Hz to 585 Hz, when the supply voltage changes from 0.35 V to 0.45 V. This corresponds to 5.3% frequency change when the supply changes by 25%. When the temperature changes by 10 °C, the frequency changes by 4.9%. The supply and temperature sensitivity are mainly caused by the comparator delay and digital buffer delay. The 2× oversampling scheme and short data sequence (53.3 ms) make the system insensitive to clock mismatch. Based on system level Monte Carlo simulations where the clock mismatch is modeled as normal distribution with 1.5% standard deviation *(i.e.* 99.7% samples are within +/-4.5% clock mismatch), the sensitivity deviation is less than 0.5 dB.

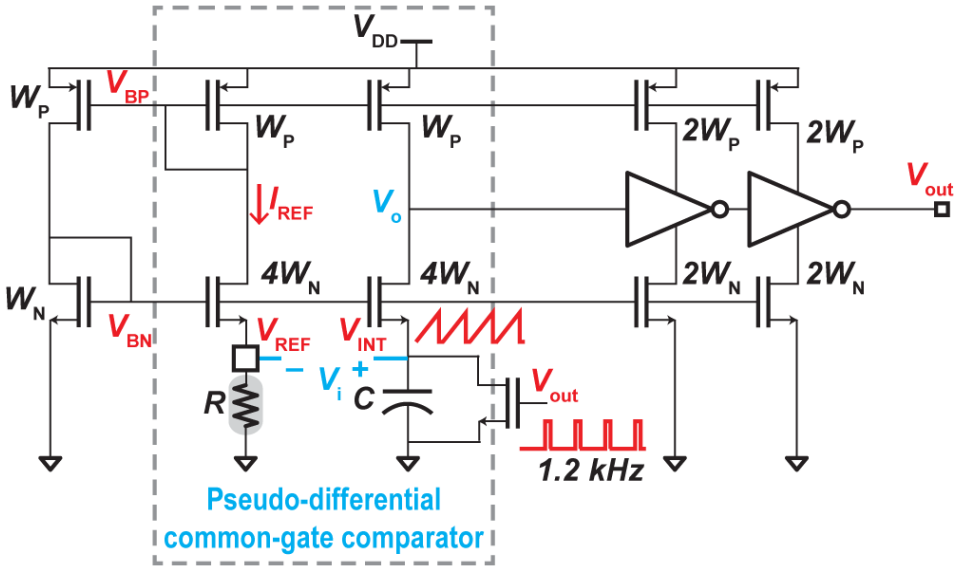


Figure 2.15. Schematic of the relaxation oscillator.

2.6 Measurement Results

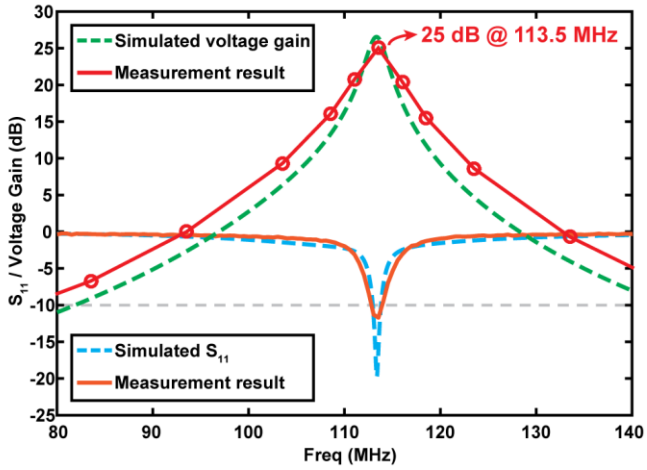


Figure 2.16. Simulated and measured transformer S_{11} and voltage gain.

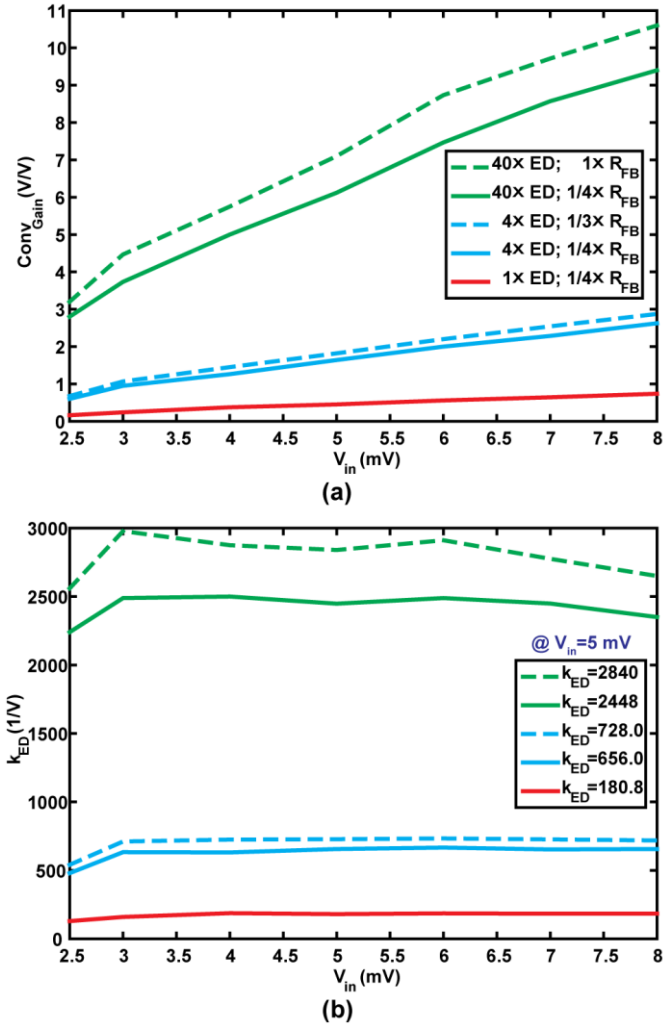


Figure 2.17. Measurement results of (a) ED conversion gain; (b) Scaling factor k_{ED}.

To characterize the passive voltage gain from the transformer/filter, a conventional 2 port measurement such as S_{21} using a vector network analyzer (VNA) is not possible due to the high (*i.e.* non-50 Ω) output impedance. Instead, we first characterized the ED by connecting a 50 Ω load at the input without the transformer to provide matching and measured the output voltage after applying a known input signal. We then replaced the 50 Ω resistor with the transformer and again measured the output voltage. The transformer gain was then calculated using

$$A_{\mathrm{V}} = \frac{V_{\mathrm{in},1}}{V_{\mathrm{in},2}} \cdot \sqrt{\frac{V_{\mathrm{out-ED},2}}{V_{\mathrm{out-ED},1}}}. \tag{2.19}$$

Using the above procedure, $A_{\mathrm{V}} = 25$ dB was measured, which is in agreement with simulation results (Figure 2.16). S_{11} measurements show excellent matching at the signal frequency (113.5 MHz), and is also in agreement with simulations.

The measured conversion gain, $Conv_{\mathrm{Gain}}$, and scaling factor, k_{ED}, versus $V_{\mathrm{in-ED},1}$ for different ED bias current settings are shown in Figure 2.17. While the $Conv_{\mathrm{Gain}}$ is proportional to $V_{\mathrm{in-ED},1}$ as shown in Figure 2.17(a), Figure 2.17(b) shows that k_{ED} is independent of $V_{\mathrm{in-ED},1}$, which is expected. When the ED is configured for 2 nW (*i.e.* 1× ED) with 4 parallel feedback units (*i.e.* 1/4× $R_{\mathrm{FB,unit}}$) to achieve a 300 Hz low pass corner, k_{ED} =180.8 (1/V). Using 1/3× $R_{\mathrm{FB,unit}}$ and 4× ED, the ED achieves k_{ED} =728 (1/V), which is ~ 4 × larger than the 1× ED configuration, as expected. At higher powers (*e.g.*, 40× ED), r_{o} dominates, and thus the improvement in k_{ED} saturates.

The comparator noise can be extracted from the distribution of "1" at comparator output versus the comparator input ΔV_{in}. Since the comparator noise is mainly white, the distribution curve can be fitted into the cumulative distribution function (CDF) of a Gaussian distribution, where the offset and noise can be obtained. Figure 2.18 shows the measurement results from four

different chips, and the offset from each chip has been removed. Nine chips were measured with the input-referred noise varying from 89 μV_{RMS} to 95 μV_{RMS}, slightly lower than the simulated value at the TT corner due to process variation. The measured offset varied from 0.69 mV to 1.16 mV, which is easily covered by the 5-bit tuning range of comparator CDAC.

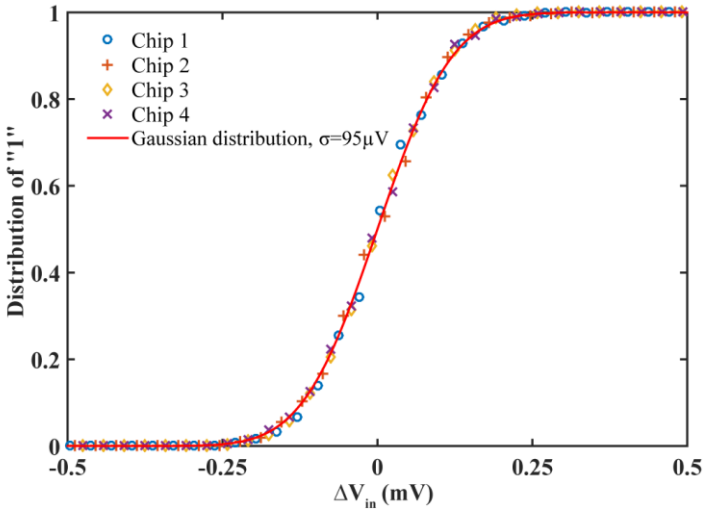


Figure 2.18. Measured comparator noise CDFs.

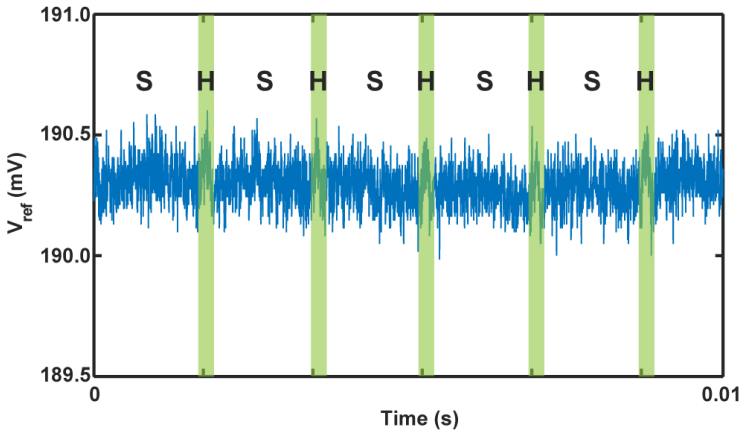


Figure 2.19. Measured reference ladder output voltage with S/H phases annotated.

The performance of the kickback reduction technique was validated by measuring the output voltage of the reference ladder, which connects to one of the comparator inputs, with the transmitted signal at the other input. Since this is a very high impedance node (~2 GΩ||50 pF), a

unity-gain buffer with low input bias current was used to buffer the voltage. The measured data are shown in Figure 2.19, where the sample (*S*) and hold (*H*) phases are annotated. Only small spikes appear during the *H* phase that are due to the leakage of the sampling switch since the switch off-resistance is not significantly larger than the reference ladder impedance. The spikes always settle before the beginning of the next cycle owing to the zero net charge kickback, and as such do not affect the following comparisons.

Figure 2.20(a) shows the measured power breakdown of the WuRX. The total power consumption is 4.5 nW when the ED is set to 2.0 nW. Transient waveforms shown in Figure 2.20(b) demonstrate correct detection when the correct code is transmitted.

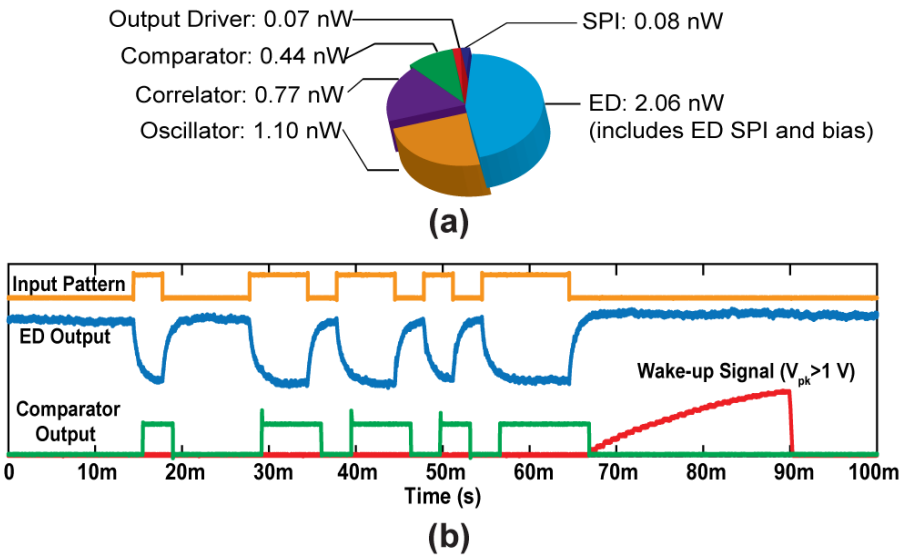


Figure 2.20. (a) System power breakdown; (b) transient waveforms.

Figure 2.21 shows the waterfall curves for conventional bit error rate (BER) measured at the comparator output, and the wake-up signal missed detection rate (MDR) measured after the digital BB logic. The BER was measured under the assumption of perfect synchronization between clock and input data, while the MDR was measured with random (*i.e.* not synchronized)

transmission. To achieve a BER $= 10^{-3}$, the input signal power $P_{\mathrm{IN}} = -65$ dBm. With the same comparator and correlator threshold, $P_{\mathrm{IN}} = -67.5$ dBm for MDR $= 10^{-3}$ with a false alarm rate of $\ll$ 1/hr. By adjusting the comparator threshold, $P_{\mathrm{IN}} = -69$ dBm was achieved for MDR $= 10^{-3}$ with a false alarm rate of $\approx$ 1/hr, which is where the sensitivity P_{SEN} is defined, and 4 dB coding gain is shown compared to the BER measurement. MDR measurements were also taken at higher power ED settings (Figure 2.22). For the 4× ED case, $P_{\mathrm{SEN}} = -71.5$ dBm and the power consumption is 9.5 nW. For the 40× ED case, $P_{\mathrm{SEN}} = -73.5$ dBm and the power consumption is 66.4 nW.

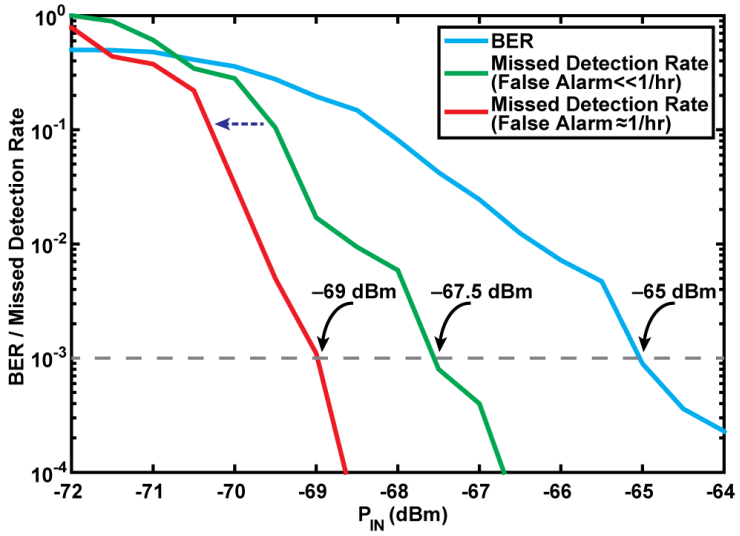


Figure 2.21. BER and MDR waterfall curves with a 300 bps data rate.

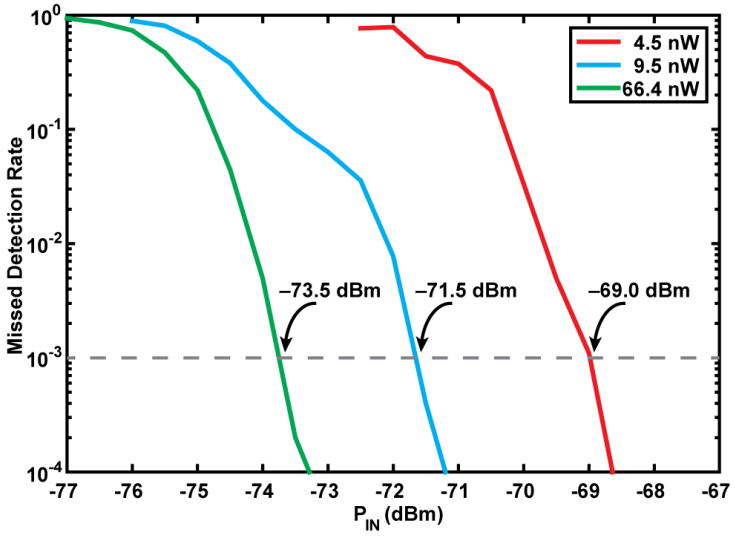


Figure 2.22. MDR waterfall curves for different power settings with a 300 bps data rate.

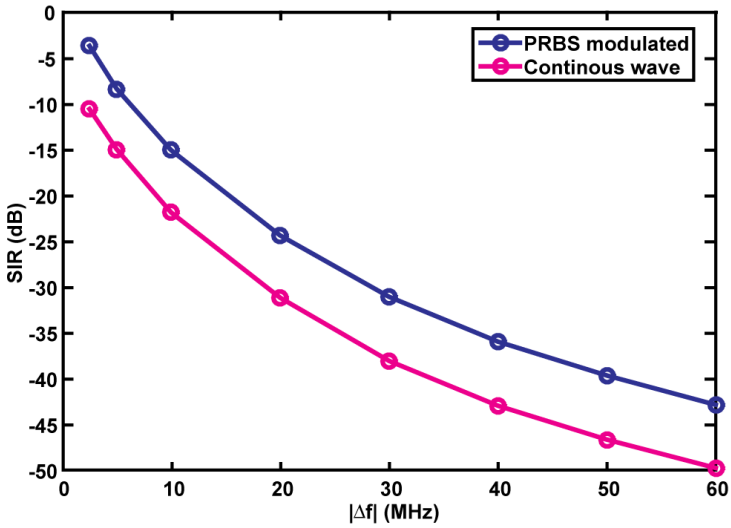


Figure 2.23. SIR curve vs. interferer frequency offset $|\Delta f|$ to carrier frequency for a worst-case 300bps PRBS-modulated jammer and a CW jammer.

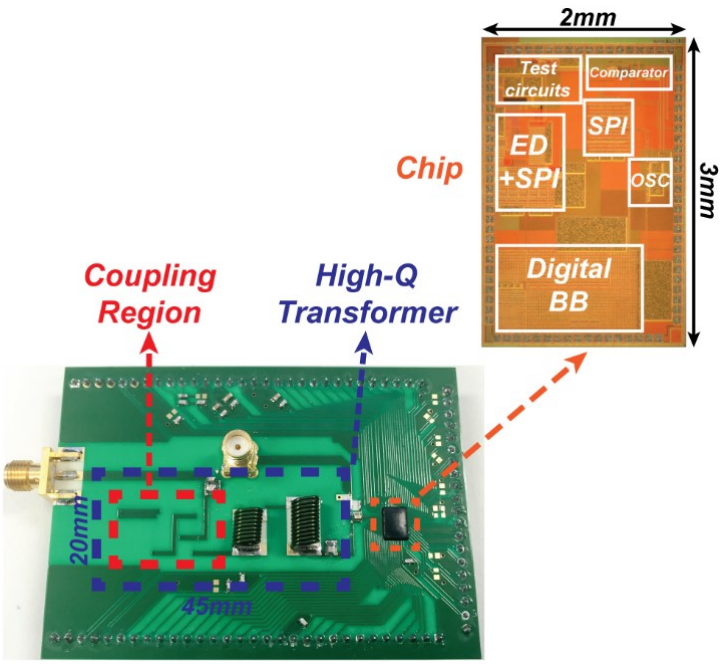


Figure 2.24. Picture of annotated die micrograph (top); whole WuRX (bottom).

A modulated signal tone along with a pseudo-random binary sequence (PRBS) modulated or continuous wave (CW) jammer at frequency offset Δf to the signal center frequency were used to test WuRX performance under interference. The input signal power was set to 1 dB higher than the power where BER $= 10^{-3}$ (*i.e.* at -64 dBm), and the interferer power at Δf was swept until BER$= 10^{-3}$. The signal to interferer ratio (SIR) vs. $|\Delta f|$ is depicted in Figure 2.23. Because of the high-Q nature of the transformer/filter, for PRBS jammer an SIR< -30 dB was achieved at $|\Delta f| = 30$ MHz. At the chosen FM band, since a narrow-band FM signal would look like a CW jammer and only causes a DC tone at the ED output, an additional 7 dB rejection compared to a PRBS jammer was achieved. Moreover, a CW jammer is unlikely to cause a false alarm due to the correlator. Therefore, by designing a longer-bit correlator, the code space can be increased, which not only improves interferer resilience further in terms of false alarms, but also enables more

WuRXs with different wake-up codes in the sensor network. The die micrograph along with the whole system photograph are shown in Figure 2.24.

2.7 Figure of Merit and Comparison

As discussed in Chapter 2.1, for WuRXs used in low-average-throughput applications, power consumption and sensitivity are the most important metrics, and thus the following FoM is defined:

$$FoM_{\mathrm{LAT}}(\mathrm{dB}) = -P_{\mathrm{SEN}} - 10\log\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}, \tag{2.20}$$

where P_{SEN} is the sensitivity in dBm and P_{DC} is the power consumption. For high-average-throughput applications, data rate is important. Therefore, the following FoM is used:

$$FoM_{\mathrm{HAT}}(\mathrm{dB}) = -P_{\mathrm{SEN,norm}} - 10\log\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}, \tag{2.21}$$

where $P_{\mathrm{SEN,norm}}$ is the sensitivity normalized to data rate and calculated using one of the following equations:

$$P_{\mathrm{SEN,norm}}(\mathrm{dB}) = P_{\mathrm{SEN}} + 5\log Latency, \tag{2.22}$$

$$P_{\mathrm{SEN,norm}}(\mathrm{dB}) = P_{\mathrm{SEN}} + 10\log Latency, \tag{2.23}$$

where $5\log Latency$ in (2.22) is used for designs with a non-linear squaring function for envelope detection [23], [24], [29], [30], [42]–[44], and $10\log Latency$ in (2.23) is used for designs with a linear operation to demodulate the signal [26], [28] or designs using a non-linear squaring function for envelope detection after high active pre-ED gain with sharp filtering [25], [27] (*i.e.* where convolution noise dominates [30]). A survey of prior-art WuRXs is shown in Figure 2.25 for both FoMs. The low baseband bandwidth and high passive RF gain afforded by the high input impedance ED and FM-band high-Q passives enabled the proposed design to achieve an

FoM_{LAT}=122.5 dB, which is over an order of magnitude higher than prior works. Table 2.2 summarizes the measurement results of the proposed WuRX design and compares the results to the state-of-the-art WuRXs.

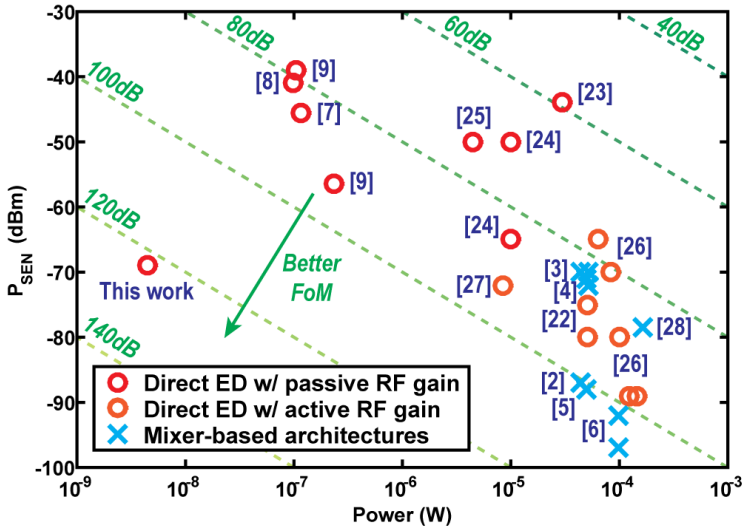


Figure 2.25. Sensitivity vs. power (FoM_{LAT})

Table 2.2. Comparison with State-of-the-Art WuRX prior 2017

	Plectcher ISSCC'08	Huang ISSCC'10	Pandey ISSCC'11	Oh CICC'13	Salazar ISSCC'15	Robert ISSCC'16		**This Work**
Technology	90nm	90nm	130nm	130nm	65nm	65nm		180nm
Carrier Frequency	2GHz	915MHz	402MHz	402MHz	2.4GHz	2.4GHz		113.5MHz
Modulation	OOK	OOK	FSK	OOK	OOK	OOK		OOK
Power Supply	0.5V	1V	1V	1.2/0.5V	0.5V	1/0.5V		0.4V
Digital Correlator?	No	No	No	31-bit	No	31-bit		32-bit[1]
Oscillator?	Ring osc.	No	Inj.-locked ring osc.	XTAL osc.	LC DCO	XTAL osc.		Relaxation osc.
Gain Stage(s)	IF[2]	RF/BB[2]	IF[2]	ED[2]	IF/BB[2]	ED[2]	ED/BB[2]	TF/ED/BB
Data Rate	100kbps	10kbps	200kbps	12.5kbps	10kbps	8.192kbps		0.3kbps
Energy/bit	520pJ	5100pJ	220pJ	9.3pJ	9900pJ	12.7pJ	28.8pJ	15.0pJ[1]
Sensitivity	-72dBm	-80dBm	-70dBm	-45dBm	-97dBm	-39dBm	-56.5dBm	-69dBm[3]
Normalized Sensitivity[4]	-84.6dBm	-87.6dBm	-98.2dBm	-53.1dBm	-112dBm	-46dBm	-63.7dBm	-69dBm
Power	52µW	51µW	44µW	116nW	99µW	104nW	236nW	4.5nW

[1] 16-bit code sequence with 2x oversampling.
[2] The front-end matching network also has modest passive gain.
[3] Defined with less than 10^{-3} miss detection rate.
[4] Calculated by normalizing the data rate to 0.3kbps.

2.8 Summary

In this chapter, a 0.4 V 113.5 MHz OOK-modulated WuRX that achieves -69 dBm sensitivity consuming only 4.5 nW in a 0.18 μm SOI CMOS process is presented. The WuRx was designed for emerging event-driven low-average-throughput applications to reduce system power. While conventional direct envelope detection architectures can achieve low power at moderate sensitivities, this design breaks the conventional trade-off to achieve ultra-low power with high sensitivity by: 1) reducing the baseband signal bandwidth to 300 Hz; 2) modulating OOK signal with a custom designed 16-bit code sequence to get 4 dB coding gain; 3) employing an off-chip high-*Q* transformer/filter with 25 dB passive voltage gain enabled by an ED with high input impedance; 4) achieving higher conversion gain using an active-*L* biased ED; 5) digitizing the ED output via a regenerative comparator with kickback elimination; 6) decoding the received OOK signal using a high-*Vt* subthreshold digital baseband correlator, operating with 2× oversampling to overcome phase asynchronization, where the clock is generated by a 1.1 nW relaxation oscillator.

Chapter 2, in part, is based on materials from Haowei Jiang, Po-Han Peter Wang, Li Gao, Pinar Sen, Young-Han Kim, Gabriel M. Rebeiz, Drew A. Hall, Patrick P. Mercier, "A 4.5nW wake-up radio with −69dBm sensitivity," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2017, and Po-Han Peter Wang, Haowei Jiang, Li Gao, Pinar Sen, Young-Han Kim, Gabriel M. Rebeiz, Patrick P. Mercier, Drew A. Hall, "A Near-Zero-Power Wake-Up Receiver Achieving −69-dBm Sensitivity," in *IEEE Journal of Solid-State Circuits*. June 2018. The dissertation author was the primary investigator and author of these papers.

Chapter 3

N-Zero WuRXs with Passive Envelope Detection

3.1 Introduction

Last chapter has shown has shown that through a combination of low carrier frequency operation (*i.e.* FM-band) and reducing the WuRX data rate, large passive RF voltage gain (at the expense of larger passive components) when combined with a high input impedance active ED results in improved sensitivity at extremely low power (*e.g.*, -69 dBm at 4.5 nW [45], [46]), with wake-up latencies that still support the needs of low-average throughput applications. Despite these improvements, WuRX sensitivity still lags that of most main radios, and must be further improved upon. Since the ED is the dominant noise source in a direct-ED receiver [46], recent work has shown that by implementing a multi-stage passive ED architecture, which, unlike active EDs, does not have any 1/*f* noise [47], high sensitivity at sub-10 nW is possible (*i.e.* -76 dBm at 7.6 nW [31]). Thus, it becomes increasingly appealing to adopt passive ED to achieve better sensitivity as shown in Figure 3.1. However, there are still many challenges in combining a passive into the existing WuRX architecture, most prominently, the difficulty to design the BB circuits.

The BB circuits in the new WuRX have to interface with a higher output impedance, 1/*f* noise free, DC floating ED, which imposes issues including biasing, offset and BB circuit 1/*f* noise, which potentially limits the WuRX sensitivity.

In addition to the power and sensitivity, other practical metrics have been overlooked. For example, at such low power levels, the battery volume may not be the limiting factor in overall device miniaturization. Instead, the size of the antenna, transformer, and other off-chip components often dominate, especially in size-conscious applications (*e.g.*, surveillance and tracking). For example, achieving 0.7 dBi peak gain at 433 MHz requires a 50 × 100 mm^2 patch antenna [48], which alone is on the same size as a 1.5 V, 90 mAh printed battery (72 × 60 mm^2) [49]. The area of the impedance matching network at such frequencies also occupies significant area (*e.g.*, >6 cm^2 in [50]). To make matters worse, such designs typically ac-couple the ED output to the baseband (BB) amplifier to ease biasing, and thus require either off-chip nF-size capacitors or suffer from ac-coupling distortion due to the low data rate (<1 kbps) [50]–[52].

This chapter presents the design of a WuRX architecture that arranges the passive ED in a pseudo-balun topology to perform single-ended to differential conversion and improve the conversion gain by 2× compared to a conventional single-ended passive ED for a given input capacitance under the same input signal level [29], [31]; 2) using higher V_t devices than in conventional passive EDs [29], [53] to increase the effective input resistance as well as a body-biasing technique to reduce the input capacitance, which enables the design of a passive voltage gain impedance transformer with high voltage gain at high frequency.

To minimize area and impart temperature-robust operation without a large compromise in power or sensitivity, this paper presents a WuRX operating at X-band, shown in Figure 3.2. The design utilizes a pseudo-balun passive ED with high input impedance at 9 GHz to facilitate the

design of a small microstrip line transformer with 13.5 dB of passive voltage gain at 9 GHz. To eliminate off-chip ac-coupling, a replica ED and autozeroing BB amplifier with CMFB loop is proposed. Temperature robustness is achieved using temperature compensation techniques applied to the ED, BB amplifier, and relaxation oscillator to maintain constant signal bandwidth. The proposed WuRX is implemented in a heterogenous stack of 65 and 180 nm CMOS directly mounted on a PCB with a custom antenna and microstrip line transformer. The entire design, including the antenna, fits within 4.55 cm^2.

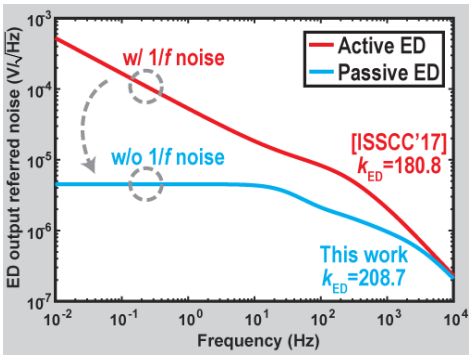


Figure 3.1. Active ED vs. passive ED

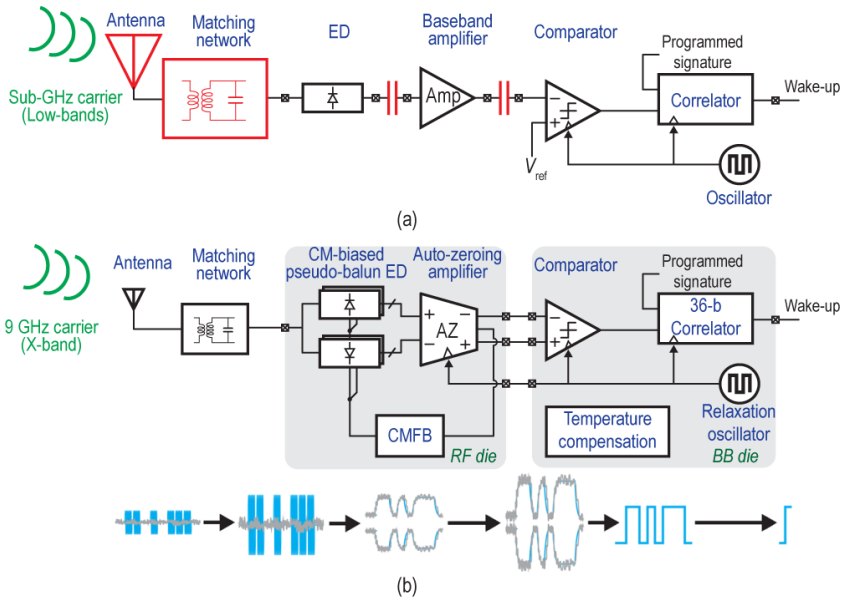


Figure 3.2. Block diagram of (a) a conventional ac-coupled WuRX and (b) the proposed WuRX.

3.2 System Design Consideration

3.2.1 Carrier Frequency and Architecture Selection

Recent WuRX work has greatly benefited from the combination of a passive direct ED architecture coupled to a passive impedance transformation network enabling high voltage gain with zero power [Figure 3.2(a)]. By operating at sub-500 MHz (*e.g.*, 109 MHz in [54] and 434 MHz in [52]), high voltage gain (>23 dB) and therefore high sensitivity (<-79 dBm) was achieved. However, the impedance transformer in such designs requires large, off-chip, high-Q inductors for high parallel resistance. For instance, a 1,320 nH inductor and a 50 nH inductor were used in the 109 MHz and 434 MHz designs, respectively. The antenna size also scales quadratically with the carrier wavelength [55]. The matching network (MN) and the antenna consume >50 mm^2 preventing use in area-constrained applications.

Operating at higher frequencies (*e.g.*, 2.4 GHz) can enable a dramatic area reduction, for example down to <2 cm^2 in [56], at the expense of reduced sensitivity (-61.5 dBm) due to low antenna and matching network gains. Alternatively, ultrasound can also enable miniaturization, but requires custom transducers that are not compatible with existing radios [57], [58]. Furthermore, ultrasound is easily blocked by obstacles, and thus only suitable for short range applications.

To enable miniaturization, this design targets X-band operation. However, any RF active amplification or LO generation at such frequency would consume several mWs – $10^6\times$ larger than the nW target. As such, a direct ED architecture is the only suitable architecture. A passive ED was chosen over an active or self-mixer due to its higher input-impedance, higher conversion gain, and $1/f$ noise-free nature.

3.2.2 RF Circuit Design Challenges

Moving to higher frequencies reduces the size of the antenna and MN, as illustrated in Figure 3.3. However, this comes with a tradeoff in the achievable passive gain. According to recent literature, the passive voltage gain scales monotonically with frequency, from 30.6 dB at 109 MHz to 2 and 3 dB at 5.8 GHz [59], [60]. Since the direct-ED WuRX sensitivity is typically set by the BB noise [61], every dB lost in the MN gain directly reduces the sensitivity. This indicates that simply moving a prior design from 109 MHz to 9 GHz would lose ~30 dB in sensitivity, which is unacceptable. Thus, the first challenge is to break the trend shown above and maintain high passive gain while moving to X-band. This requires co-design of a high-impedance ED and a high-Q MN at 9 GHz to maximize the RF and conversion gain.

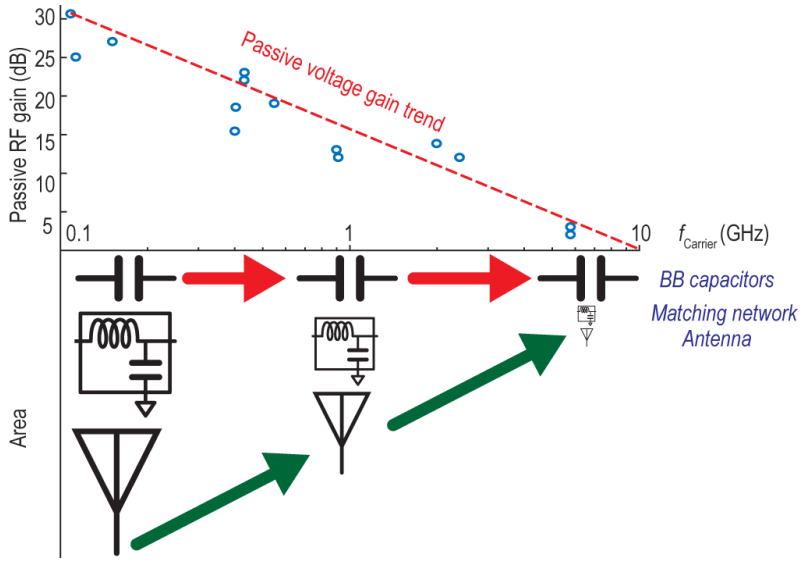


Figure 3.3. MN voltage gain and component size vs. carrier frequency.

3.2.3 BB Circuit Design Challenges

As described in [50], after fixing the architecture and frequency, the only design parameter that can be used to trade for sensitivity is latency. With 20 dBm output power from a transmitter,

better than -65 dBm sensitivity is required to achieve a reasonable coverage range (~50 m). To achieve this sensitivity, a low WuRX data rate (33.3 bps), low BB bandwidth (33.3 Hz), and a long code sequence (18 bit) are chosen. This results in a latency of 540 ms, which is acceptable in many, though not all, low-average throughput IoT applications.

However, the low data rate and long code sequence impose a challenge on the conventional ac-coupled BB amplifier [Figure 3.2(a)]. Prior work used either nF off-chip capacitors [7] or a 20 pF on-chip capacitor but incurred an SNR penalty [52]. While the RF components (*i.e.* antenna and MN) scale with the carrier frequency, the BB ac-coupling capacitors are unchanged and only possible with lumped components (Figure 3.3).

Figure 3.4(a) shows the effect on the signal distortion due to the ac-coupling. When a signal passes through the high-pass filter, its dc level shifts towards the bias voltage gradually, which manifests as a distortion. Since the comparator threshold voltage is preset to achieve the required false-alarm rate and is constant during the sequence, the signal amplitude with respect to the threshold voltage decreases with each "1" bit. The minimum signal amplitude (*i.e.* the maximum SNR loss) happens at the end of the last "1" bit. This distortion depends on the filter corner frequency, f_c, and the code (sequence and length). For example, consider the code consisting of repeating "10" for simplicity. The maximum SNR loss is plotted against f_c normalized to the data rate and code length in Figure 3.4(b) and (c), respectively. The plots show that the distortion is more serious when lower data rates and longer code sequences are used assuming a fixed f_c. To bound the distortion to less than 1 dB, f_c must be $<0.001\times$ data rate. A similar conclusion has been drawn in [62]. Thus, the 33.3 bps data rate needs $f_c \leq 33.3$ mHz, which is not possible to reasonably implement on-chip.

To address this challenge, dc-coupling should be used between the ED and BB amplifier. However, this leads to issues around biasing (*i.e.* the preceding stage sets the following stage's operating point) and offset. Chapter 3.3 proposes an ED-amplifier co-design scheme where a global CMFB, autozeroing network, and a replica ED are used to address this collectively.

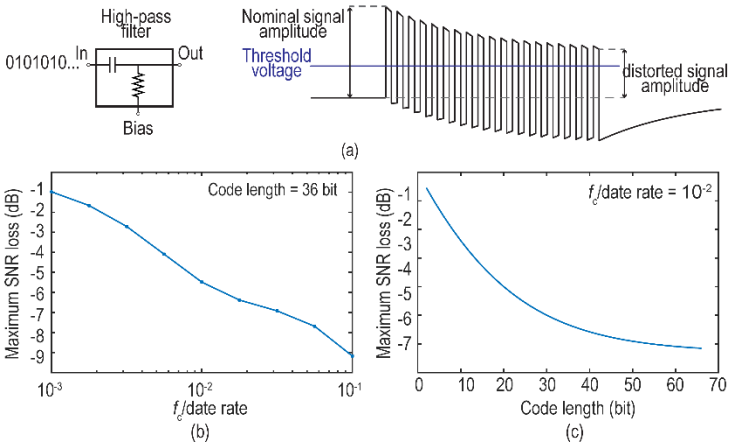


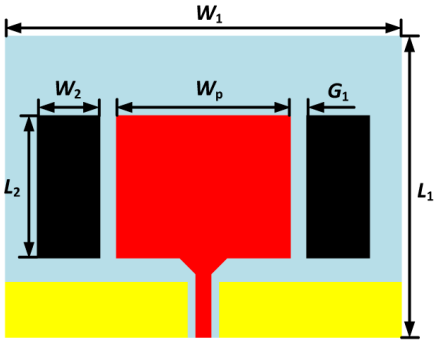
Figure 3.4. Simulated waveform output when fc/data rate is 0.01 and simulated maxi-mum SNR loss (b) versus fc/data rate, and (c) versus code length.

3.3 RF Circuit Design

3.3.1 Antenna

A patch antenna is a popular choice at high frequency due to its low cost, high gain, and small form factor that is compatible with PCB design. They also have relatively narrow bandwidth, which is beneficial for interference resilience, though in some cases the bandwidth is so narrow that lining up the antenna's frequency with the desired frequency band and the MN can be difficult. To slightly ease this constraint, the proposed design employs a conventional patch antenna next to a pair of parasitic patches, as shown in Figure 3.5, which extend the matching bandwidth from 3%

to 5%. The main patch is 9 × 8.4 mm^2 and feeds the following impedance transformer via a grounded coplanar waveguide (GCPW). The simulated antenna gain is 5.5 dB.



Antenna parameters (Unit: mm)

L_1	21
W_1	21
L_2	8.4
W_2	5
W_p	9
G_1	0.3

Figure 3.5. 9 GHz patch antenna layout.

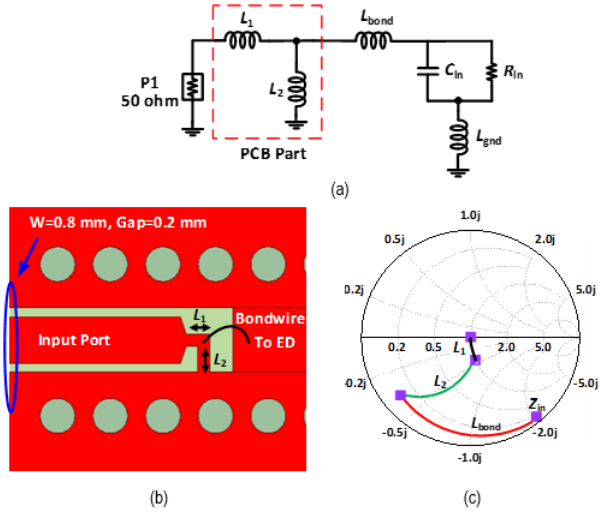


Figure 3.6. (a) Schematic of the 9 GHz transformer, (b) Layout of the transformer, and (c) Matching procedure.

3.3.2 Matching Network

Prior sub-GHz WuRXs utilize discrete components (inductors and/or MEMS resonators) to implement the MNs due to their high Q (>100). However, these high Q passives become inaccessible as the carrier frequency increases. This design instead uses distributed components and a bond wire in the arrangement depicted in Figure 3.6 to form a transformer. The T-shaped

inductor network (L_1, L_2, and L_{bond}) is equivalent to a pair of coupled inductors. No additional capacitance is used to avoid extra loss. The ground inductance is carefully modeled by L_{gnd}, as it can significantly affect performance at 9 GHz. Specifically, L_{gnd} limits the highest operation frequency since it creates a transmission zero at:

$$f_{z,gnd} = \frac{1}{2\pi\sqrt{L_{gnd}C_{in}}}, \quad 3.1$$

where C_{in} is the ED input capacitance. As shown later, C_{in} is estimated to be 115 fF, and thus $f_{z,gnd}$ should be >15 GHz so as to not impair the voltage gain at 9 GHz. This suggests that L_{gnd} should be <0.74 nH. Several approaches were utilized to reduce L_{gnd} to below this value. First, instead of using microstrip line to connect the transformer, a GCPW is used. Thus, the ground is a continuous plane, which reduces L_{gnd}. Second, four ground pads are down-bonded to the ground paddle beneath the chip to minimize the wirebond inductance, though it should be noted that the mutual inductance limits this technique from further improvement. Third, a thin substrate with a via-array is used to connect the top and bottom grounds. Note there is a tradeoff here as too thin of a substrate results in low Q for the distributed inductors, which reduces the voltage gain. In this work, a 20-mil thick Rogers 4003C substrate is used to meet both gain and L_{gnd} requirements. These techniques reduce L_{gnd} from 1 to 0.2 nH.

The transformer voltage gain (A_V) is primarily limited by the effective parallel resistance of the secondary of the transformer. To maximize this resistance, a bond wire inductor is used as the second stage since it has the highest Q (~100) at this frequency. The bond wire length is estimated to be 1.8 mm with an inductance of 1.8 nH. Figure 3.6(b) shows the transformer layout. Inductors L_1 (0.3 nH) and L_2 (0.35 nH) are realized by short stubs that directly connect to the input port and top ground, respectively. The high-Q transformer occupies only 0.02 cm^2 – 300× smaller

than prior work [54]. Figure 3.6(c) shows the impedance matching contour from the high impedance ED to the 50 Ω antenna on a Smith chart.

3.3.3 Envelope Detector

Figure 3.7(a) and (b) depict conventional and the proposed passive ED unit cells and architectures. Cross-coupled self-mixers [47] rectify a differential input signal and thus require a center-tapped transformer, which results in lower Q and thus lower passive gain compared to a single-ended design. Moreover, biasing is implemented using an extra RC network at the RF node that reduces the ED input impedance. On the other hand, a traditional Dickson rectifier operating in sub-V_{t} [29], [31] can rectify a single-ended input signal, but does not have any tunability and only has a single-ended output, which requires a tunable reference circuit for the comparator. To overcome these issues, a tunable passive pseudo-balun ED architecture is proposed, which is a $2N$-stage rectifier with the middle node connected to V_{CM} and the bulk nodes connected to a tunable voltage, V_{bulk}, to set the bandwidth (Figure 3.7b). As such, the baseband AC currents flow in opposite directions relative to ground to form a pseudo-differential output. Compared to the original single-branch N-stage Dickson rectifier, this structure achieves 2× conversion gain and a 1.5 dB sensitivity improvement under the same input signal level without sacrificing output bandwidth. Although the 2^{nd} branch of the N-stage ED could be connected in parallel with the 1^{st} branch without flipping the polarity, this results in the same 1.5 dB improvement in sensitivity, but only half of the conversion gain and is single-ended. V_{bulk} is provided by a diode-connected reference ladder with 4-bit tunability.

To drive a fixed capacitive load from the baseband amplifier, an ED with a large number of stages, N, requires larger transistor widths to maintain the same output bandwidth, and thus has

a larger C_{in}, which limits the achievable transformer gain. As the transistor width increases, the parasitic capacitor from the ED starts to add on to the fixed capacitive load at the output node, which thus requires R_{out} to decrease further. As shown in Figure 3.8(a), larger transformer passive voltage gain, A_{V}, is possible with small N, which has higher R_{in} and lower C_{in}. However, as shown in Figure 3.8(b), since the conversion gain and thus ED scaling factor, k_{ED}, are proportional to N, an ED with large N is more suitable for post-ED stage noise suppression. Moreover, since the passive ED noise power density is $4k_{\mathrm{B}}TR_{\mathrm{out}}$, an ED with a larger N has less total integrated noise, $\sqrt{\overline{v_{\mathrm{n}}^2}}$. To find the optimum N, an objective function was developed to compare designs with different N under the same output bandwidth and operating frequency:

$$SNR_{\mathrm{ED,norm}} = \frac{A_{\mathrm{V}}^2 \cdot k_{\mathrm{ED}}}{\sqrt{\overline{v_{\mathrm{n}}^2}}} \cdot 10^{-9}, \tag{3.2}$$

which is essentially the achievable ED output SNR normalized to its input voltage. An optimum value of N=4 was found for the ED using this equation. On the other hand, the proposed bulk tuning can not only be used to overcome process variation, but can also effectively reduce C_{in} via smaller devices for an equivalent output bandwidth, and therefore maximize the achievable passive voltage gain at a given carrier frequency. By forward biasing the bulk-to-source junction diode (<200 mV), V_{t} is reduced and allows smaller width transistors to be implemented for a given output bandwidth (33.3 Hz in this design). Although the proposed ED could be designed with PMOS devices in a process without a deep N-well, NMOS is adopted in this design to leverage higher mobility and thus lower transistor size for a given output bandwidth. Compared to prior art operating at 5.8 GHz with an active ED that consumed 25.2 μW [59], the RF front-end and passive ED in this work achieves 3 dB better conversion gain with no power consumption and no 1/*f* noise.

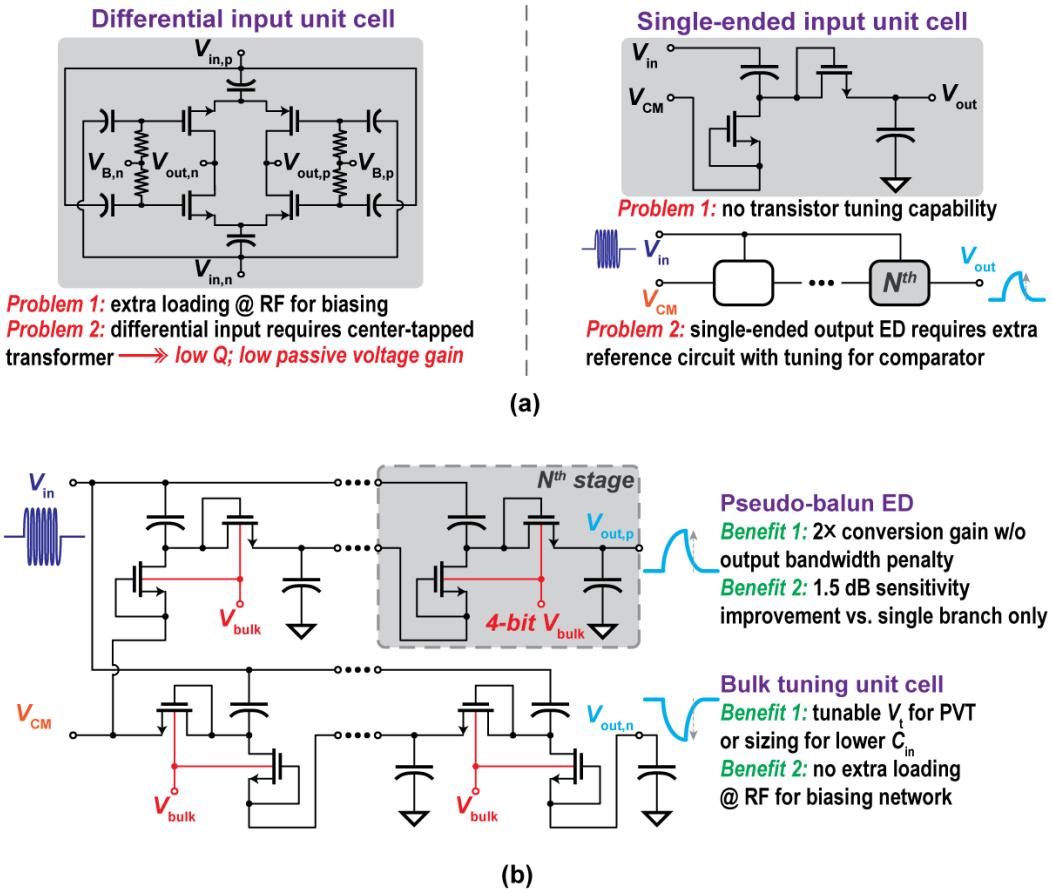


Figure 3.7. (a) Conventional passive ED unit cells and architectures; (b) proposed passive pseudo-balun ED with bulk tuning unit cell.

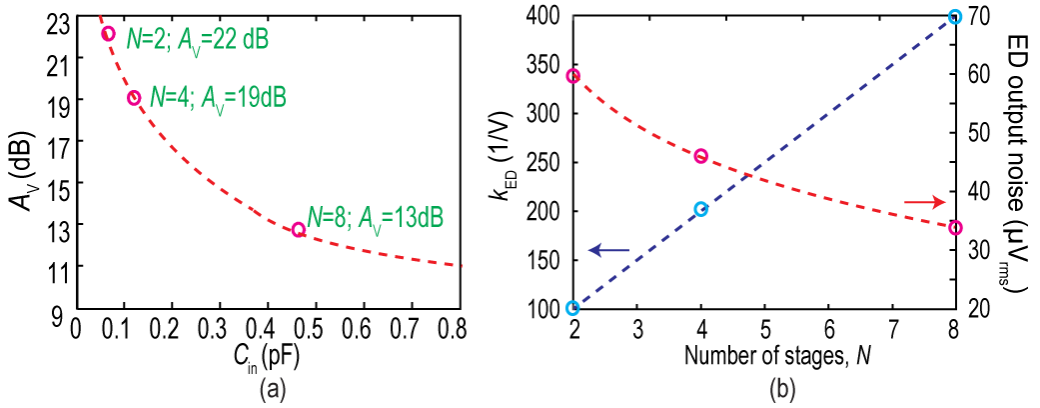


Figure 3.8. Simulated (a) transformer gain vs. Cin, and (b) kED and ED noise vs. N.

3.4 Baseband Circuit Design

3.4.1 Baseband Amplifier

Due to the lack of sufficient RF amplification prior to demodulation by a passive-gain-based ED-first architecture, sensitivity is not typically determined by RF noise, but rather by baseband noise from the ED and BB amplifier [30]. In this work, a BB amplifier with a low (<1 dB) noise figure (NF) is required to maximize the sensitivity. The BB amplifier also must have low input capacitance and high input impedance (>10 GΩ) since the ED output impedance is proportional to its input impedance (>100 MΩ). Fortunately, linearity is generally not an issue in WuRXs that utilize binary modulation (*e.g.*, OOK).

The core BB amplifier is implemented using a single-stage current-reuse inverter-based amplifier with a local CMFB circuit that sets the NMOS transistor source bias by sensing its output CM voltage [Figure 3.9(a)]. Due to the 2× current reuse, the core amplifier is designed to have a 0.4 dB NF with only 3.2 nW of power consumption. To remove the ac-coupling capacitors, a global CMFB around the ED is proposed to properly bias the BB amplifier. This is accomplished by driving the CM node of the pseudo-balun ED, $V_{CM,ED}$, by an auxiliary amplifier. The auxiliary amplifier closes the loop by sensing the tail node voltage from the core amplifier, as shown in Figure 3.9(b). Thus, by adjusting $V_{CM,ED}$, the dc-coupled current-reuse amplifier is biased to the desired operating point and is insensitive to process, voltage, and temperature (PVT) variation.

However, this architecture is sensitive to the dc offsets of the ED and the BB amplifier. Specifically, the pseudo-balun architecture has a systematic offset that can overload the comparator, which would desensitize the WuRX without special design consideration. Figure 3.10 illustrates this issue where the positive branch 8× forward-biased diode-connected NMOS transistors are connected in series with the BB amplifier's input resistance, R_{in}. In contrast, the

negative branch consists of 8× reverse-biased diodes in series with R_{in}. The forward- and reverse-biased diodes have different channel resistances, which results in a non-zero ED offset voltage between $V_{ED,p}$ and $V_{ED,n}$. Unfortunately, the diode resistance is a function of bulk bias voltage, V_{bulk}, and temperature, as shown in Figure 3.10(b) and (c). Based on simulation, the offset voltage varies from 10 to 500 µV, which is significantly larger than the minimum detectable signal at the ED output. Due to the bias voltage and temperature-dependency, the offset is difficult to calibrate out. Furthermore, the core BB amplifier can easily yield >1 mV input-referred offset due to device mismatch, even with large transistors (>50 µm^2) and careful layout. For these reasons, careful considerations are required to enable robust operation over PVT variation.

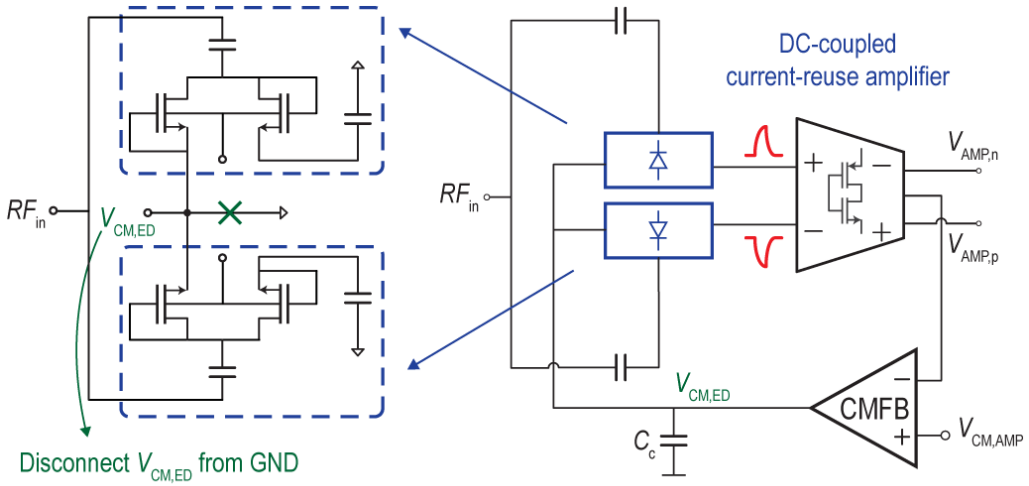


Figure 3.9. Proposed (a) core amplifier and (b) CM-biased ED using global CMFB.

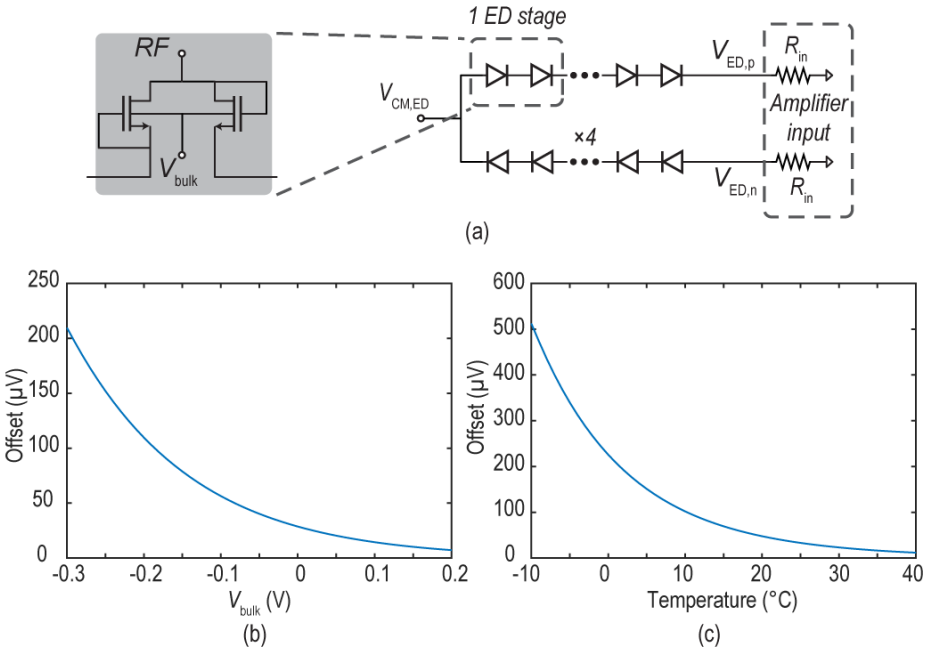


Figure 3.10. (a) Circuit model showing the ED offset issue and simulated offset versus (b) ED bulk bias and (c) temperature.

3.4.2 Autozeroing Network

Rather than degrade the ED input impedance with chopping at the RF input, an output-sampled autozeroing (AZ) network and a replica ED architecture are proposed. Figure 3.11(a) shows the schematic of the proposed scheme. All of the ED bulks are tied together, and the replica ED is matched to the signal path ED through common layout techniques; thus, they should generate the same dc output voltage (*i.e.* $V_{ED,p\text{ or }n} = V_{ED,p\text{ or }n,replica}$). The signal path ED (blue) connects to the RF input via small, on-chip, RF ac-coupling capacitors, whereas the replica ED (purple) doesn't connect to the RF input. Thus, the only signal content exists at $V_{ED,p}$ and $V_{ED,n}$. An on-chip 10 pF capacitor is placed between the outputs of the replica ED to band-limit the noise without affecting the CM loop stability.

The AZ network shown in Figure 3.11 works as follows: During the AZ phase, S_2 and S_3 are closed whereas S_1 and S_4 are open. The replica ED offset, $V_{ED,offset}$, and the amplifier error,

σ_{AMP}, specifically 1/*f* noise and offset, are amplified by gain A and sampled on C_2 with respect to the CM voltage, V_{CM}. During the amplification phase, S_2 and S_3 are open whereas S_1 and S_4 are closed. The ED output and offset along with the amplifier error are amplified and sampled onto C_1 (=C_2) with respect to V_{CM}. The voltage stored on C_2 is in series and thus subtracted, thereby removing the ED offset, amplifier 1/*f* noise, and amplifier offset. Folding of wideband white noise is a typical drawback of AZ since the amplifier has bandwidth that is greater than the sampling frequency, f_s [63]. There are two noise sources in this design that could potentially fold: the ED and the amplifier noise. The ED noise folding is solved by band-limiting it to the data rate and employing 2× oversampling. The amplifier noise folding is inevitable since the signal path is on for only half of the period and the amplifier bandwidth needs to be 2× higher than the equivalent continuous-time amplifier. Consequently, a minimum of 2× noise folding is expected. An explicit sampling capacitor C_1 is added to the amplifier output during the amplification phase to limit the noise bandwidth. In the AZ phase, C_1 is floating and doesn't load the amplifier. With $C_1 = C_2$, the amplifier bandwidth during each phase is the same, both 2× higher than the data rate, and thus the minimum 2× noise folding is achieved. Simulation shows ~7× lower noise by adding C_1 compared to not having it.

Given the low supply voltage (V_{DD} = 0.4 V), the switches in the AZ network require extra attention. The input switches (S_1 and S_2) are driven by a clock booster that generates $2V_{DD}$ to minimize the on-resistance and thus their noise power spectral density. On the other hand, the leakage of the output switches is more important, and thus minimum size transistors with the regular supply voltage are used. Simulation shows all switches contribute <3% of the total noise and switch imperfections (*i.e.* charge injection, clock feedthrough, and leakage) have minimal effect on the amplifier performance across mismatch and PVT variation.

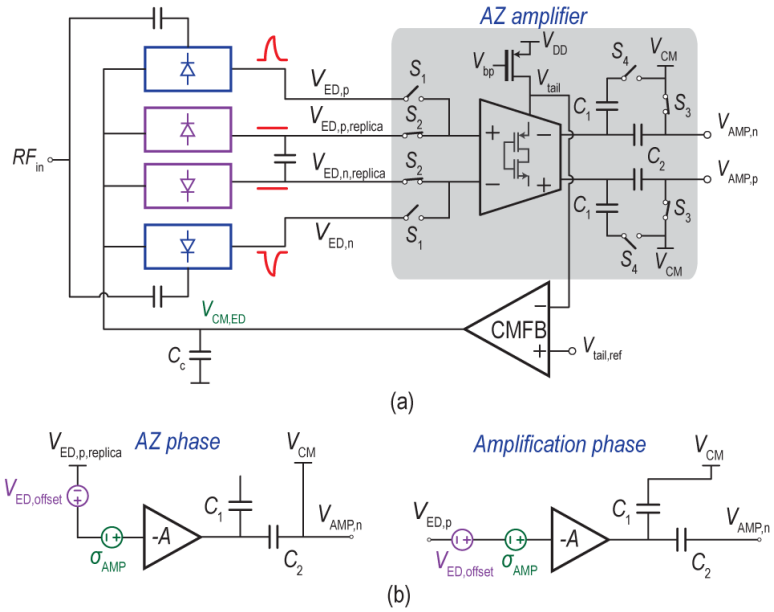


Figure 3.11. Schematic of the proposed (a) replica ED and autozeroing network, and (b) half-circuit model during AZ phase and amplification phase.

The switched-capacitor operation and large input Miller capacitance of the BB amplifier can lead to an unacceptably low input resistance (~2.4 GΩ) that loads the ED. To solve this, neutralization capacitors are connected between the amplifier input and output, thus cancelling the input Miller capacitance. The neutralization capacitors are implemented with half-sized input transistors for matching. Simulation shows the input resistance increases to 28 GΩ, which is >50× the ED output resistance.

3.4.3 Common-Mode Feedback

As a differential, dc-coupled system, the ED and BB amplifier require CMFB to operate correctly. This is accomplished in the proposed design via a global CMFB loop that senses the amplifier tail node, V_{tail}, (shown in Figure 3.9) and compares it to a replica bias circuit, which is implemented the same as the core amplifier, though in this case shorting its input and output and scaling the current by 8× to reduce power consumption [Figure 3.12(a)]. The diode-connected

architecture ensures self-bias and adjust $V_{tail,ref}$ dynamically to accommodate PVT variation. This approach, coupled with the AZ network described above, make dc coupling between the ED and BB amplifier possible.

However, there is a potential start-up issue with this global CMFB loop due to the CM input voltage of the inverter-based core amplifier. Since M_2 works as a source-follower in the global CMFB during normal operation and the CMFB amplifier provides a 180° phase shift at dc, the loop gain is nominally negative. However, there exists an inverting path via M_3 and M_2, which forms a positive feedback loop. During start-up, node A in Figure 3.12(b) stays near ground while node B is charged to V_{DD} quickly through M_1 and M_2. Thus, M_3 is in sub-threshold saturation and M_2 is in triode. The inverting path can overpower the non-inverting path and prevent the amplifier from starting up successfully. To remedy this, a compensation capacitor, C_c, is added between V_{CM} and V_{DD}. This serves two purposes – it sets the dominant pole of the CMFB loop and it pulls up node A to V_{DD} during startup, which drives M_3 into triode and kills the inverting path gain.

Figure 3.13 shows the simulated BB amplifier gain. As expected, a sinc-shaped foldover component appears after enabling the AZ [63]. Fortunately, this is not an issue since the ED output is bandlimited to eliminate the noise aliasing. The total input-referred integrated noise drops from 8.1 to 7.2 μV due to reduced 1/f noise [Figure 3.13(b)]. A 100-point Monte Carlo simulation shows the offset is attenuated by 50× due to the AZ [Figure 3.13(c)]. The residue offset (<500 μV) is due to switch mismatch and amplifier nonlinearity. Lastly, Figure 3.13(d) shows that the circuit starts up properly after V_{CM} and node A are pulled up to V_{DD}.

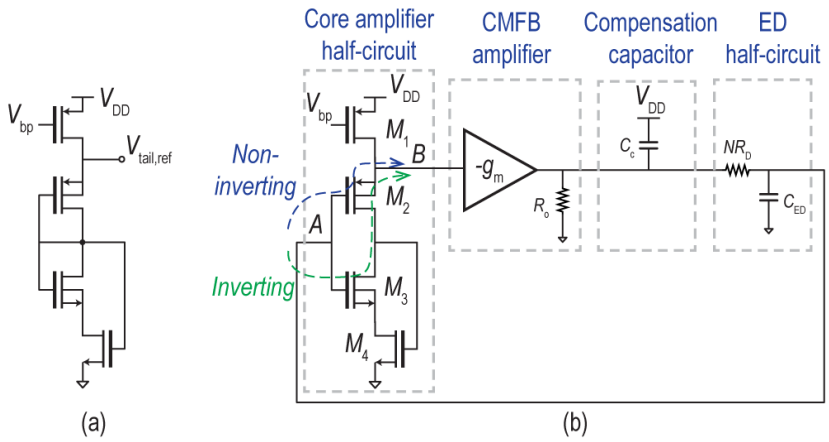


Figure 3.12. Schematic of the (a) replica bias and (b) CMFB loop.

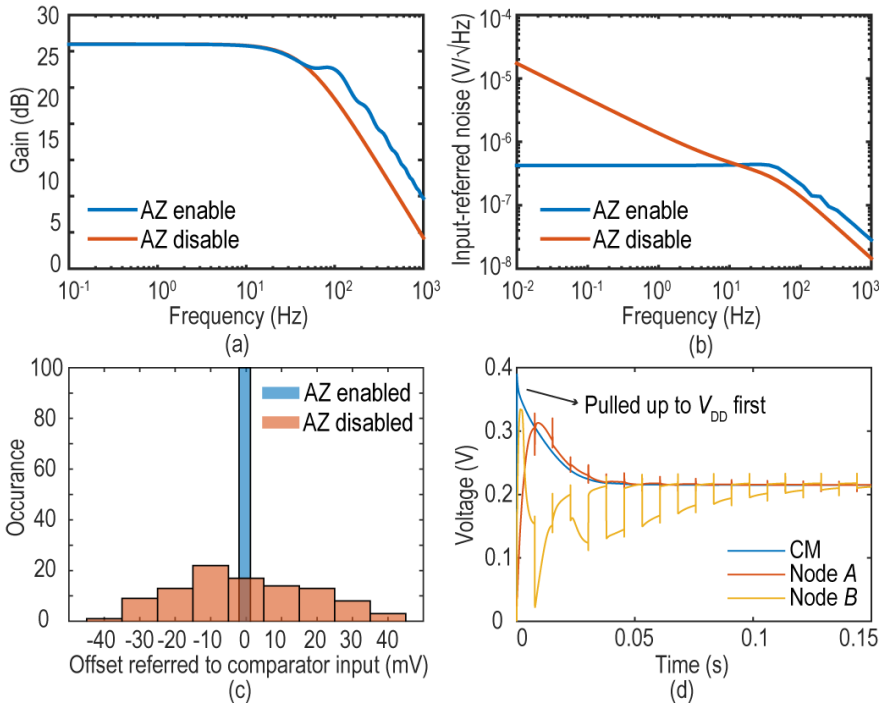


Figure 3.13. Simulated BB amplifier (a) gain, (b) noise PSD, and (c) offset. (d) Startup transient simulation.

3.4.4 Comparator, Correlator, and Oscillator

The sampled output of the BB amplifier is digitized by a comparator, which serves as a 1-bit quantizer. A double-tail dynamic comparator with threshold voltage tuning is implemented

[46]. Since the comparator noise and threshold voltage are attenuated by the BB amplifier gain when referred to the ED output, its noise and tuning step requirements are greatly relaxed.

A self-timed co-clocking scheme is proposed in Figure 3.14 to coordinate the comparator and AZ amplifier. The comparator fires after a half-cycle long amplification phase, then resets the comparator and starts the AZ phase immediately after the comparison is done. This avoids comparator metastability, while ensuring maximum time for both phases, which minimizes settling error. It also reduces the comparator power by ~30% by turning off the comparator early [46].

A 36-b digital correlator implemented with custom digital cells for minimum leakage current processes the incoming data at the comparator output. Prior work has demonstrated that it can effectively overcome transmitter asynchronization with a 2× oversampling rate [2], [6], [7], [16].

The AZ amplifier, comparator and correlator are clocked by a *RC* relaxation oscillator with an on-chip resistor and capacitor. A similar architecture proposed to the one shown in [43] is implemented. It has sub-100 ppm/°C temperature stability and ~1 nW power consumption.

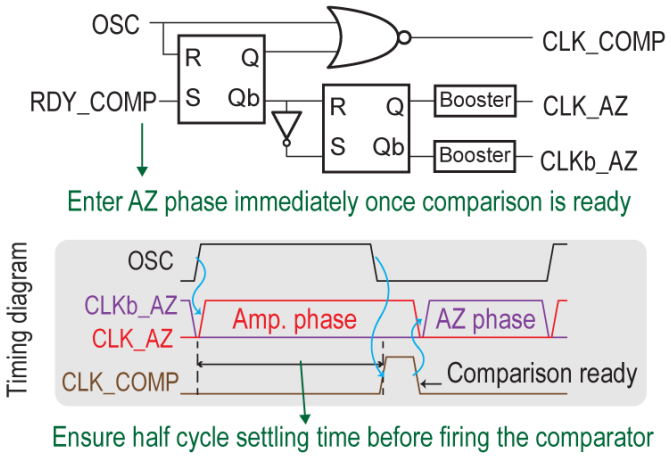


Figure 3.14. Schematic and timing of the AZ and comparator clock generator.

3.5 Measurement Results

The RF die (which contains the ED, CMFB, and BB amplifier) was fabricated in a 65 nm CMOS process to minimize ED parasitics, while the baseband die (comparator and correlator) was fabricated in a 180 nm CMOS process to minimize leakage. The dies were stacked on top of each other during assembly to save area, as shown in Figure 3.15. At room temperature, the system (excluding the temperature compensation blocks) consumes 7.3 nW operating from a 0.4 V supply, with most of the power (4.4 nW) devoted to the BB amplifier for noise reasons. To test the chips across temperature, they were placed within a temperature chamber [Figure 3.16(a)], while the wireless link test was done at room temperature only by separating the horn transmitter 1.73 m (56.3 dB loss) away from the receiver [Figure 3.16(b)].

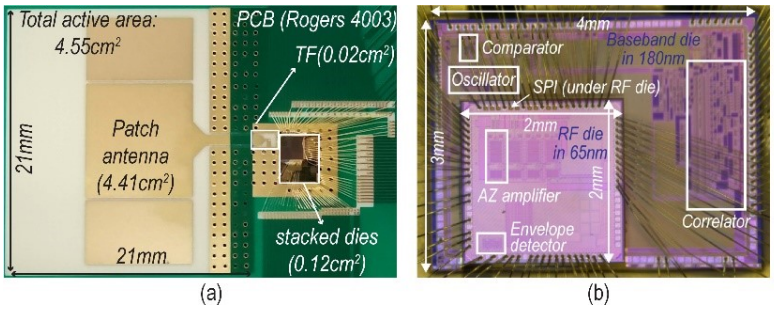


Figure 3.15. Annotated photograph of (a) PCB and (b) stacked die.

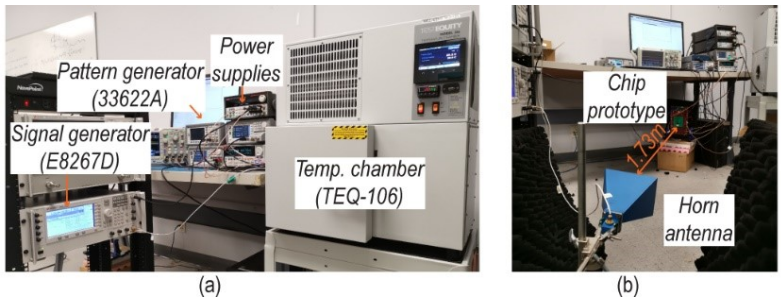


Figure 3.16. Photos of (a) across temperature test setup, and (b) wireless test setup.

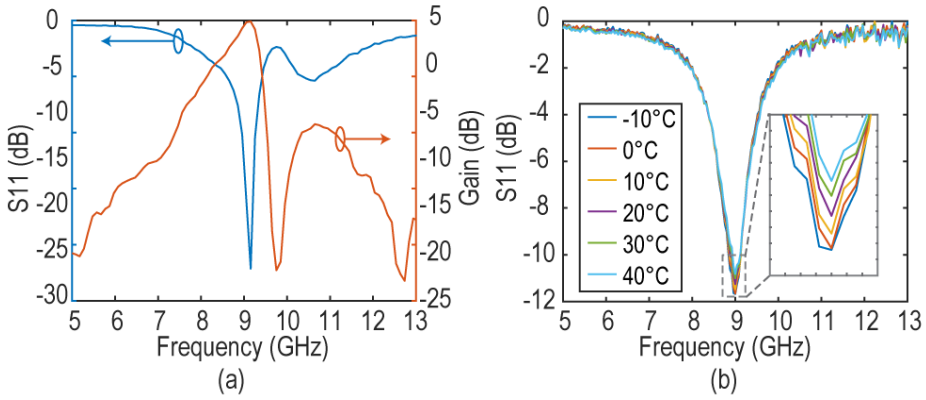


Figure 3.17. Measured (a) antenna S_{11} and gain, and (b) transformer S_{11}.

As shown in Figure 3.17, the patch antenna had a peak gain of 5 dB, and <-10 dB S_{11} between 8.95 and 9.27 GHz, covering the desired 9 GHz band. The gain had a zero at 9.7 GHz, which helps with out-of-band rejection. The MN's S_{11} was characterized over temperature (-10 to 40 °C) with no significant change in center frequency or bandwidth, as shown in Figure 3.17(b). This suggests that both the bond wire inductor Q and the ED input resistance are temperature insensitive. The MN's gain was measured at the BB amplifier output by de-embedding the ED and BB amplifier gain. The MN alone showed a gain of 13.5 dB, which is lower than the 19-dB expected from simulations. This was caused by a lower-than expected ED input resistance due to substrate dielectric losses, as confirmed post-layout extraction simulations using EMX. The gain loss can be remedied by shielding the ED's RF input trace in future work.

The BB amplifier was characterized by applying an external signal at its input and digitizing the output with an external ADC synchronized to the AZ clock. The power spectral density (PSD) was calculated based on a 1-hr long measurement. As shown in Figure 3.18(a), the amplifier PSD was flat down to ~0.02 Hz, owing to the $1/f$ noise reduction of the AZ operation. The PSD from the both the ED and BB amplifier was flat since the passive ED doesn't introduce

1/*f* noise. The tone at 6.6 Hz was due to intermodulation between a 66.6 Hz on-chip clock and 60 Hz interference, which would be reduced in a battery-powered implementation. The CM PSD is shown in Figure 3.18(b), where it can be observed that the CMFB loop bandwidth is ~4 Hz, set by the CMFB amplifier output resistance and C_c.

To illustrate the effectiveness of the offset-cancelling capability, an external DC voltage was applied between the amplifier replica inputs and working inputs to mimic the ED offset. As shown in Figure 3.19(a), the amplifier can tolerate ±13 mV offset, which is much greater than the actual ED offset, based on simulation. After connecting the ED and amplifier, the overall offset was measured across temperature [Figure 3.19(b)]. Since the offset is largely determined by random mismatch, four chips were measured, and the results are consistent.

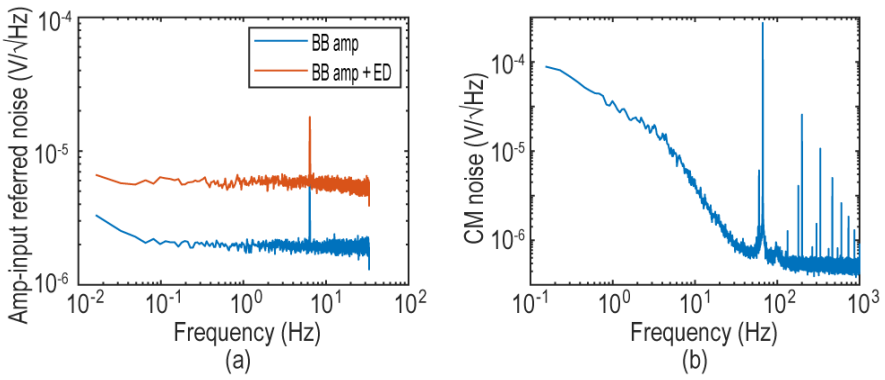


Figure 3.18. Measured noise PSD in (a) differential-mode and (b) common-mode.

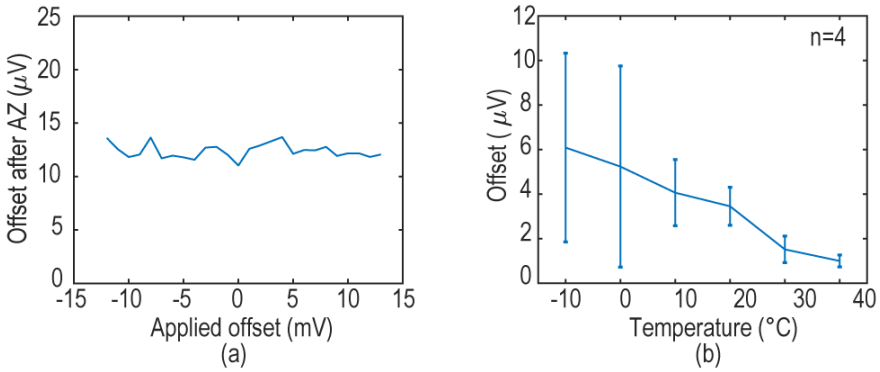


Figure 3.19. Measured AZ amplifier (a) input-referred offset and (b) offset over temperature.

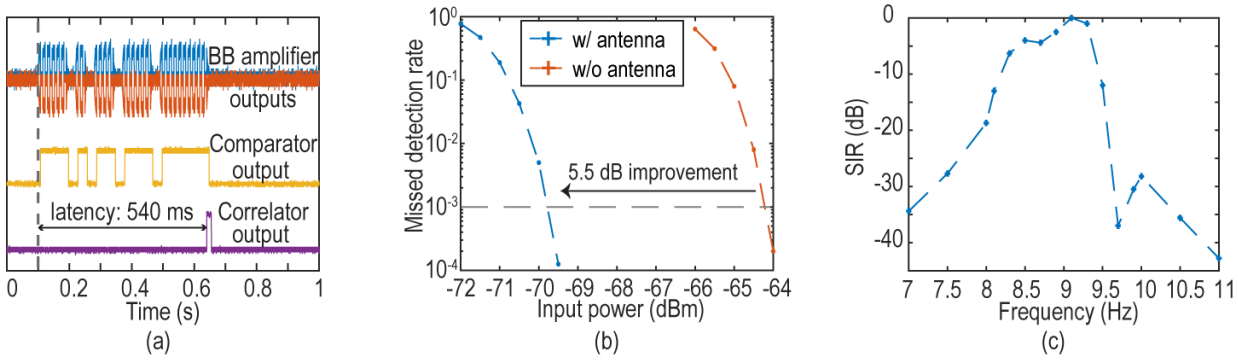


Figure 3.20. Measured (a) transient waveform, (b) MDR curve, and (c) SIR versus frequency.

Figure 3.20(a) shows transient waveforms demonstrating wake-up when the correct code is transmitted. Figure 3.20(b) shows the waterfall curves for the wake-up signature missed detection rate (MDR) with and without the antenna. Operating with the antenna had a 5.5 dB sensitivity improvement compared to without the antenna (-69.5 vs. -64 dBm), which closely matches with the antenna gain measurement result. The worst false alarm rate (FAR) is 0.08/hr. (one in a 12-hour measurement). A modulated signal tone along with a pseudo-random binary sequence (PRBS) modulated at frequency offset Δf to the center frequency were used to test WuRX performance under interference. The input signal power was set to 1 dB higher than the power where MDR =10^{-3} (*i.e.* at -68.5 dBm), and the interferer power was swept until MDR =10^{-3}. The signal-to-interferer ratio (SIR) versus interference frequency is depicted in Figure 3.20(c). The notch at 9.7 GHz was due to the zero in the antenna gain.

Table 2.2 summarizes the system performance and compares it with prior art. The proposed design is the first-reported sub-100 nW WuRX that operates at GHz frequencies. The WuRX requires no off-chip lumped components and occupies only 4.55 cm^2 of area including the antenna.

Figure 3.21 plots the figure-of-merit (FoM) from [46] of the proposed WuRX alongside prior work versus carrier frequency. There is a clear trend of FoM degradation at higher frequencies, largely due to the reduced passive RF gain. While operating at 9 GHz, this work demonstrates an FoM of -116.7 dB and -122.2 dB without and with antenna, respectively, which is higher than prior-art GHz-range WuRXs.

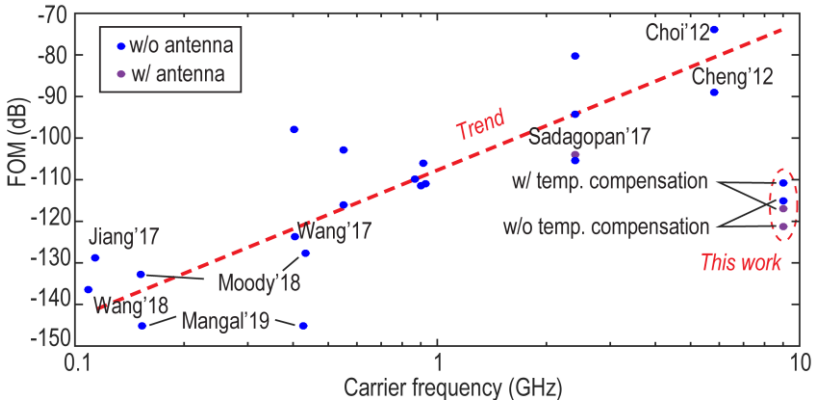


Figure 3.21. Landscape of WuRXs.

Table 3.1. Comparison to state-of-the-art WuRXs

	Wang ESSCIRC'17	[6] JSSC'19	[7] SSCL'18	[5] ISSCC'19	[13] RFIC'17	[16] ISSCC'12	[17] ASSCC'12	**This Work**
	N-ZERO WuRX (<100 nW)				GHz WuRX			**N-ZERO& GHz**
RF frequency (MHz)	405	151.8	109	434.4	2,400	5,800	5,800	**9,000**
Technology	180 nm	130 nm	180 nm	65 nm	65 nm	130 nm	180 nm	**65/180nm**
Power supply (V)	0.4	1/0.6	0.4	0.4	0.8/0.5/0.1	3	1/0.5	**0.4**
Correlator depth (bit)	32	8	36	22	32	32	16	**36**
Clock source	Relax. osc.	Ring osc.	Relax. osc.	Ring osc.	Relax. osc.	No	No	**Relax. osc.**
MN gain (dB)	18.5	27	30.6	23	N/A	3	2	**13.5**
Antenna gain (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**5**
Demodulator	Pseudo-balun CG	Single-ended Dickson	Pseudo-balun Dickson	Single-ended Dickson	Cross-coupled rectifier	Pseudo diff. CG	Pseudo diff. CG	**Pseudo-balun Dickson**
BB Coupling type	DC	AC	AC	AC	DC	DC	AC	**DC**
Wu-latency (ms)	53.3	>80	180	110	12.8	1.14	0.16	**540**
Sensitivity (dBm)	-63.8	-76	-80.5	-79.1	-61.5[c]	-45	-50	**-64/-69.5[c]**
Normalized sensitivity[a] (dB)	-70.2	-81.5	-84.2	-81.0	-71[c]	-59.7	-69	**-65.3/-70.8[c]**
Temperature range	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**-10°C ~ 40°C**
Lumped components	LC MN, capacitors	LC MN, capacitors	LC MN, capacitors	LC MN, resistor	None	LC MN	LC MN	**None**
Total area (cm^2)	>2.4	N/A	>6	N/A	1.875[c]	N/A	N/A	**0.14/4.5[c]**
Power (nW)	4.5	7.6	6.1	0.42	365	30,000	10,000	**7.3**
FoM[b] (dB)	-123.7	-132.7	-136.4	-148	-105.4[c]	-73.2	-89.0	**-116.7/-122.2[c]**

[a.] $P_{SEN,norm}$ (dB)= P_{SEN}+5log(latency). [b.] Sensitivity-power-latency FoM (dB)= $P_{SEN,norm}$−10log(power/1mW). [c.] Including antenna.

3.6 Conclusion

A 7.3 nW power, 9 GHz WuRX was designed for area-constrained, ultra-low power applications. The passive pseudo-balun ED architecture eliminates the 1/*f* noise and improves the sensitivity greatly. By adaptively biasing the ED with a CMFB loop around the baseband amplifier, and autozeroing the baseband amplifier offset, the ac-coupling capacitors were removed. These techniques avoid any off-chip baseband components while achieving narrow baseband bandwidth to minimize noise. Due to the high ED input impedance, this work achieves a state-of-the-art FOM compared to high frequency (>1 GHz) WuRXs.

Chapter 3, in part, is a revision of the material as it appears in Haowei Jiang, Po-Han Peter Wang, Li Gao, Corentin Pochet, Gabriel M. Rebeiz, Drew A. Hall, Patrick P. Mercier, "A 22.3 nW, 4.55 cm^2 Temperature-Robust Wake-up Receiver Achieving a Sensitivity of -69.5 dBm at 9 GHz," in *IEEE Journal of Solid-State Circuits*, and Po-Han Peter Wang, Haowei Jiang, Li Gao, Pinar Sen, Young-Han Kim, Gabriel M. Rebeiz, Patrick P. Mercier, Drew A. Hall, "A 6.1-nW Wake-Up Receiver Achieving −80.5-dBm Sensitivity Via a Passive Pseudo-Balun Envelope Detector," in *IEEE Solid-State Circuits Letters*, May 2018. The dissertation author was the primary investigator and author of these papers.

Chapter 4

Temperature Compensations in WuRXs

4.1 Introduction

Temperature robustness is another design consideration that has been overlooked in prior work. Since achieving such low power levels typically requires low-voltage and/or subthreshold operation, such designs are usually quite sensitive to temperature variation; even a few degrees of temperature variation can adversely affect the performance of several key blocks, leading to unacceptable sensitivity degradation. For example: the exponential I-V curve in sub-threshold region worsens the circuit temperature dependency, and the low supply voltage (<0.5 V) leaves minimal voltage headroom when considering the transistor threshold voltage drift (~2 mV/°C). Unlike conventional "main" radios, which derive frequency references from temperature-stabilized crystals and can support the power overhead of temperature sensing and temperature

compensation of RF and analog circuits, it is not straightforward to compensate nW-level WuRXs without significant power overhead.

Prior-art nW-level WuRXs were not temperature compensated, yet the implemented architectures have obvious places where temperature variation can adversely affect performance. For example, without proper compensation, temperature variation can affect the proposed system performance in the following ways: 1) if the clock frequency deviates from the nominal 2× data rate, it's possible the received sequence could be greater or less than 36 bits, which reduces the ability of the correlator to accurately identify the correct sequence; 2) if the RF or conversion gain drops, the ED and the BB amplifier NFs increase; 3) if the ED or BB amplifier bandwidth drifts too low, this could introduce settling errors and inter-symbol interference, whereas if they drift higher, this leads to excess noise. All these effects lead to sensitivity degradation. It should be noted that the gain of the BB amplifier also depends on the temperature; however, as long as the BB gain doesn't fall too low, there is minimal degradation in SNR from the comparator and thus not compelling reason to compensate it over PVT. On the other hand, signal swing variation with respect to the threshold voltage indeed affects the receiver operating characteristic (ROC) curve, such that the system will tend to have either higher MDR or a degraded FAR. Although, this effect doesn't affect WuRX sensitivity, it still needs to be taken care of to achieve targeted MDR and FAR requirements. Thus, for a WuRX system to operate robustly across temperature variation, the following blocks must be compensated for their temperature dependencies: the relaxation oscillator, the RF/conversion gain, the ED bandwidth, the BB amplifier bandwidth, and the comparator threshold voltage.

4.2 Relaxation Oscillator Temperature Compensation

4.2.1 Generic Relaxation Oscillator

The operation of a comparator-based relaxation oscillator is illustrated in Figure 4.1(a). A bias resistor, R, in conjunction with a beta-multiplier are used to set a reference current, I_{ref}, and a reference voltage, V_{ref} (=RI_{ref}). An integration capacitor, C_{int}, is charged by a mirrored version of I_{ref}, and repeatedly reset by a continuous-time comparator after crossing V_{ref} (Figure 4.1b). Thus, the oscillation period, T_{OSC}, is

$$T_{\mathrm{OSC}} = \tau_{\mathrm{RC}} + \tau_{\mathrm{comp}} + \tau_{\mathrm{buf}} + \tau_{\mathrm{rst}}, \tag{4.1}$$

where τ_{RC} is the time constant formed by R and C_{int}, τ_{comp} is the comparator delay defined as the time taken to assert the comparator output once V_{int} exceeds V_{ref}, τ_{buf} is the digital buffer delay, and τ_{rst} is the reset time that includes discharging the capacitor and resetting the comparator, buffer, and switch. Note that resetting the comparator, is much faster than τ_{comp}. Since the TC of τ_{RC} can be accurately controlled (*e.g.*, TC ≈ 0) using two trimmed resistors to counteract the TCs of each other [66], [67], and both τ_{buf} and τ_{rst} are often negligible for kHz-range oscillators, τ_{comp}, which depends on temperature, becomes significant in the overall temperature stability. Most prior work strived to minimize τ_{comp} by increasing the bandwidth, and therefore the comparator power, to make τ_{comp} a small fraction of the oscillation period (*e.g.*, $\tau_{\mathrm{comp}}/T_{\mathrm{OSC}} < 0.4\%$ in [68]). Other techniques, including feed-forward comparator delay cancellation [66], integrated error feedback [67], and a duty-cycled high-bandwidth comparator [69], have also been used to break this trade-off. However, they require either redundant comparators or complex digital control logic.

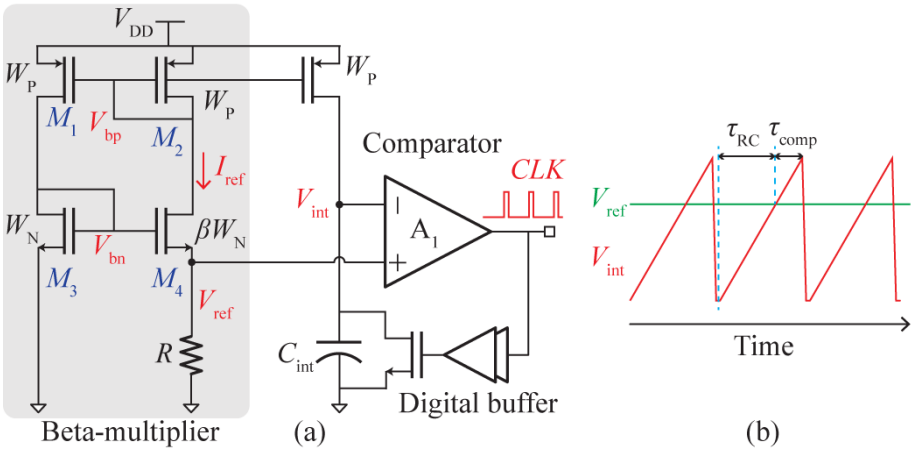


Figure 4.1. (a) Schematic of a typical comparator-based relaxation oscillator, (b) illustration of delay components, where τ_{buf} and τ_{rst} are too trivial to show.

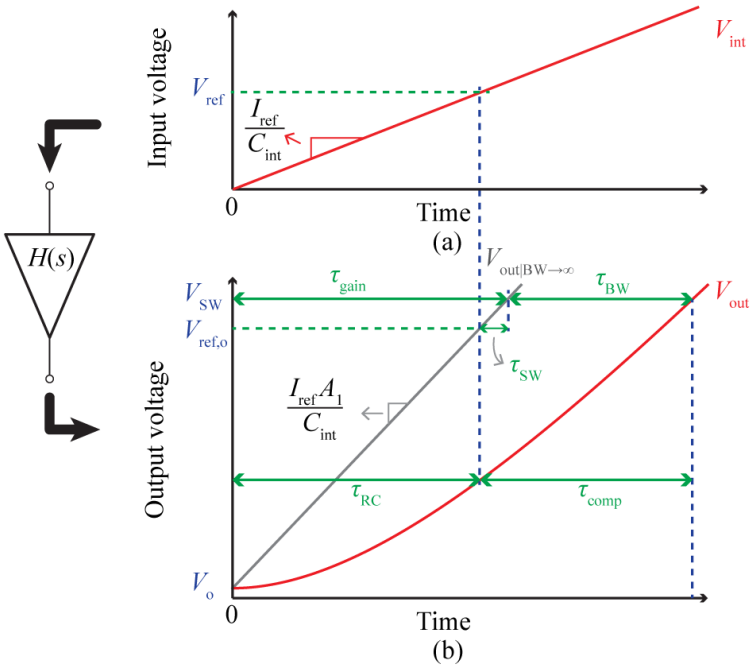


Figure 4.2. Model of the comparator delay following an integrator. and driving a buffer.

4.2.2 Comparator Delay Analysis

4.2.2.1 Comparator Delay Model

The comparator input voltage, V_{int}, is a ramp that can be written as

$$V_{\text{int}}(t) = \frac{I_{\text{ref}}}{C_{\text{int}}} \cdot t \cdot u(t), \tag{4.2}$$

where $u(t)$ is the unit step function, as shown in Figure 4.2(a). The transfer function of the comparator, assuming a single-stage linear, time-invariant continuous-time system, can be written as

$$H(s) = \frac{A_1}{1+s\tau_1}, \tag{4.3}$$

where A_1 and τ_1 are the DC gain and time constant of the comparator, respectively. By converting (4.2) into the s-domain and multiplying by (4.3), the output behavior of the comparator can be expressed as

$$\Delta V_{\text{out}}(s) = \frac{I_{\text{ref}}}{sC_{\text{int}}} H(s), \tag{4.4}$$

where ΔV_{out} is the change in the output voltage. This is graphically illustrated in Figure 4.2 (b) along with an additional curve corresponding to a comparator with infinite bandwidth ($V_{\text{out|BW}\to\infty}$) for comparison. Note that both curves start at a voltage V_{o} and increase until triggering the buffer and resetting the ramp by reaching V_{SW}, which is defined as the switching threshold of the subsequent buffer. Since all of the time constants are annotated on the output waveform [Figure 4.2(b)], V_{ref} is also referred to the output as $V_{\text{ref,o}}$ for convenience, where $V_{\text{ref,o}}$ is defined as the voltage that the comparator with infinite bandwidth reaches when the inputs are equal (*i.e.* $V_{\text{int}} = V_{\text{ref}}$). The time constants τ_{RC} and τ_{comp} are annotated on Figure 4.2 (b) based on the definitions provided in Section I, namely that τ_{RC} ends when V_{int} crosses V_{ref} and τ_{comp} starts immediately afterwards and ends when V_{out} crosses V_{SW}.

The infinite bandwidth comparator curve allows one to decouple the effect of finite gain and finite bandwidth, as shown in Figure 4.2 (b), where τ_{gain} is the time taken for $V_{\text{out|BW}\to\infty}$ to

cross V_{SW} and τ_{BW} is the remaining time that V_{out} takes to cross V_{SW}. The sum of $\tau_{gain}$and τ_{BW} is the total delay, τ_{tot}, which is the time V_{out} takes to increase from V_o to V_{SW}. Note, $\tau_{tot} \approx T_{OSC}$ (based on (4.1), just excluding τ_{buf} and τ_{rst}). By substituting $V_{SW} - V_o$ for ΔV_{out} in (2.1), and taking the inverse Laplace transform, one can derive τ_{tot}, and, more importantly τ_{BW}, as

$$\tau_{tot} = \underbrace{\frac{C_{int}(V_{SW}-V_o)}{I_{ref}A_1}}_{\tau_{gain}} + \underbrace{\underbrace{1 - e^{-\frac{\tau_{tot}}{\tau_1}}}_{\kappa}\tau_1}_{\tau_{BW}}, \tag{4.5}$$

where κ is a scaling factor bounded between 0 and 1. When τ_1 is smaller than τ_{tot}, κ exponentially approaches unity as shown in Figure 4.3. Finally, with $\tau_{BW} = \kappa\tau_1$ from (4.5), τ_{comp} can be written as

$$\tau_{comp} = \tau_{BW} + \underbrace{(V_{SW} - V_{ref,o})\frac{C_{int}}{I_{ref}A_1}}_{\tau_{SW}} = \kappa\tau_1 + \tau_{SW}, \tag{4.6}$$

where τ_{SW} is the additional time that V_{out} takes to reach V_{SW} even with an infinite bandwidth comparator. Note, in practice $V_{ref,o} - V_{SW}$ can be either positive or negative. It is also worth pointing out that the underlying assumption of a linear, time-invariant system may not hold for all implementations, especially considering the large input swing; however, to accurately calculate τ_{SW}, A_1 only needs to be constant over a small range, $V_{SW} - V_{ref,o}$, which is easily achieved in practice. This is the motivation for deriving τ_{comp} with respect to τ_{SW} instead of τ_{gain}, which would require A_1 to be linear over the entire range.

The key takeaway from this analysis is that the comparator delay consists of two terms: one relating to the finite bandwidth ($\tau_{BW} = \kappa\tau_1$) and another dependent on the following buffer stage switching threshold (τ_{SW}). Rather than trying to minimize τ_{BW} to lessen its effect on the oscillator's temperature stability, which would require burning additional power, we propose to

compensate it, along with τ_{SW} instead. Section II-B analyzes the temperature dependence of (4.8), and Section III demonstrates a method to compensate (4.8) by linearizing $\kappa\tau_1$ with a PTAT current, while cancelling τ_{SW} with a two-stage comparator.

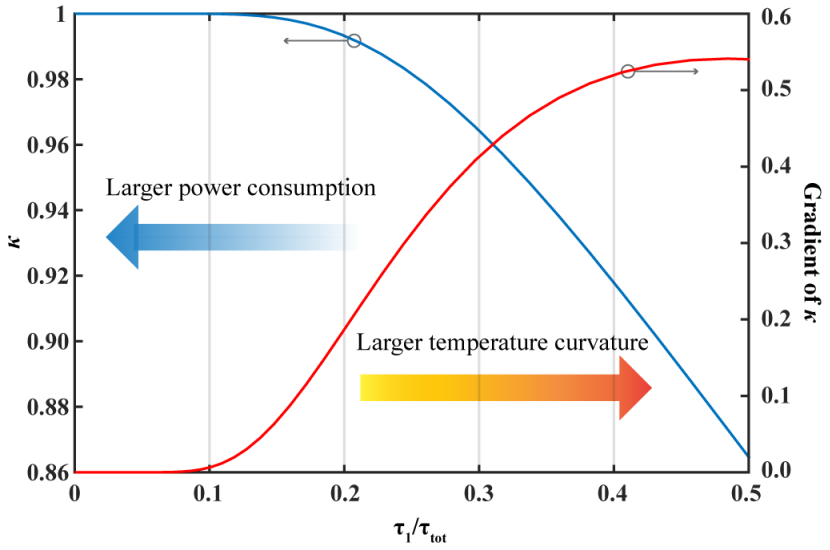


Figure 4.3. Numerical solutions for κ vs. τ_1/τ_{tot}.

4.2.2.2 Temperature Dependence of the Comparator Delay

To analyze the temperature dependence of τ_{comp}, the TC of $\kappa\tau_1$ and τ_{SW} are examined separately to isolate their individual contributions. Assuming operation in subthreshold saturation and neglecting channel length modulation, the current generated by the beta-multiplier in Figure 4.1 is

$$I_{ref} = \frac{\ln(\beta) n k_B T}{qR}, \tag{4.7}$$

where k_B is Boltzmann's constant, n is the subthreshold slope factor (≈1.5 in this process), q is the elementary charge, β is the size ratio between M_4 and M_3, and T is the temperature. Thus, (4.7) is a linear PTAT current. For a comparator biased with I_{ref}, τ_1 is

$$\tau_1 = r_o C_o = \frac{V_A C_o}{I_{ref}},, \quad 4.8$$

where V_A is the Early voltage, which has minimal temperature dependence [70], r_o is the output resistance, and C_o is the load capacitance. Simulation shows C_o, which consists of C_{db} of the transistor and the gate capacitance of the next stage, changes by only 2.2% over the 100°C range. By substituting (4.7) into (4.8) and taking the partial derivative around room temperature (T_0 = 300 K), τ_1 has a CTAT dependence with a 1st order temperature coefficient of

$$\alpha_{\tau 1} = -\frac{1}{T_0}, \quad 4.9$$

Since κ, as shown in Figure 4.3, is dependent on τ_1, it also changes with temperature. If τ_1 is large, κ is PTAT and when multiplied by the CTAT τ_1 results in a negative 2nd order TC. Since κ becomes increasingly sensitive to τ_1 as τ_1 increases (the red curve in Figure 4.3), the 2nd order TC of $\kappa\tau_1$ also becomes significant. Thus, this imposes a design trade-off where decreasing τ_1 requires a more power-hungry comparator, while increasing τ_1 relaxes the comparator bandwidth requirement but leads to larger temperature curvature. By designing τ_1/τ_{tot} to be small, κ approaches unity while the gradient of κ with respect to τ_1 approaches zero. Thus, κ can be approximated as a constant that doesn't affect the temperature dependence. In summary, $\kappa\tau_1$ exhibits a CTAT dependence with slightly larger than first order curvature that, to the first order, can be counteracted by designing a linear PTAT τ_{RC} by trimming R to be PTAT.

The TC of τ_{SW} depends on two factors: $C_{int}/I_{ref}A_1$ and $V_{SW} - V_{ref,o}$. It can be shown that the first term is

$$\frac{C_{int}}{I_{ref}A_1} = \frac{C_{int}}{I_{ref}g_m r_o} = \frac{C_{int}}{\ln(\beta)V_A}R, \quad 4.10$$

where $g_m$is the transconductance. Thus, (4.10) has the same temperature dependence as R. Since V_{SW} and $V_{ref,o}$ are determined by the circuit implementation, they are discussed later in Section

III. However, the trick is that if the circuit is designed to have V_{SW} track $V_{\mathrm{ref,o}}$, then τ_{SW} is zero and the temperature dependence does not matter, as shown in (4.6). In summary, this analysis shows a technique to design a relaxation oscillator by leveraging the CTAT dependence of $\kappa\tau_1$ while cancelling τ_{SW}, which deviates from conventional approaches that minimize the entire $\tau_{\mathrm{comp}}/T_{\mathrm{OSC}}$ by making the comparator have higher bandwidth.

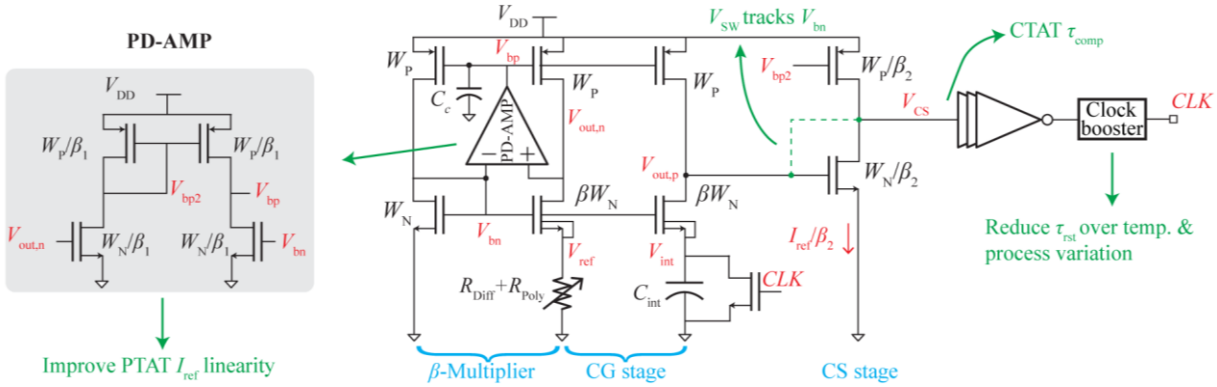


Figure 4.4. Schematic of a relaxation oscillator employing a two-stage comparator, along with PD-AMP in feedback to improve PTAT current temperature linearity.

4.2.3 Relaxation Oscillator Circuit Design

A 1.2 kHz relaxation oscillator has been designed employing a power efficient comparator with a linear temperature-dependent delay from -20°C to 70°C using the previously described analysis.

4.2.2.3 High Linearity PTAT Reference Generator

The beta-multiplier circuit shown in Figure 4.1 is commonly used to generate a PTAT current. To ensure proper operation, each transistor must be in subthreshold saturation ($V_{\mathrm{DSAT}} > 4V_{\mathrm{T}}$). Changes in the transistor threshold voltage, V_{t}, due to temperature and process variation also imposes a limitation on the minimum supply voltage, $V_{\mathrm{DD,min}}$. It can be shown that

$$V_{\mathrm{DD,min}} = \left[V_{\mathrm{DSAT,M2}} + V_{\mathrm{DSAT,M4}} + \ln(\beta)\right]V_T + \Delta V_{\mathrm{bp}}$$
$$= [8 + \ln(\beta)]V_{\mathrm{T}} + \frac{\partial V_{\mathrm{bp}}}{\partial T}\Delta T + \frac{\partial V_{\mathrm{bp}}}{\partial V_{\mathrm{t,P}}}\Delta V_{\mathrm{t,P}}, \quad 4.11$$

where ΔV_{bp} is the change in the drain voltage due to both temperature and process variation, and $\Delta V_{\mathrm{t,P}}$ is the change in threshold voltage due to process variation. Thus, a smaller β factor leads to lower $V_{\mathrm{DD,min}}$ where we choose β=2, resulting in R=47 MΩ and I_{ref} = 0.54 nA at room temperature. Compared to β=3 or 4, this saves 17.5 mV and 30 mV voltage headroom at 70°C, respectively, but more importantly a smaller β also leads to a lower R and thus a smaller area.

The sensitivity of V_{bp} due to temperature and threshold voltage change can be derived from

$$V_{\mathrm{bp}} = V_{\mathrm{DD}} - nV_{\mathrm{T}}\ln\left[\frac{\ln(\beta)n}{(n-1)RK_{\mathrm{P}}V_{\mathrm{T}}}\right] - \left|V_{\mathrm{t,P}}\right|, \quad 4.12$$

where K_{P} is the PMOS transistor transconductance parameter inclusive of the sizing. The 1st order temperature dependence of V_{bp} is

$$\frac{\partial V_{\mathrm{bp}}}{\partial T} \approx -\frac{nk_{\mathrm{B}}}{q} + \frac{\partial\left|V_{\mathrm{t,P}}\right|}{\partial \mathrm{T}} = -0.99\ \mathrm{mV/°}C, \quad 4.13$$

which matches with simulation results (-1.02 mV/°C). Since the total temperature range is 90°C, the drift in V_{bp} due to the temperature change is 92 mV (*i.e.* the 2rd term in Eq. 4.11). Furthermore, V_{bp} changes directly proportionally with the threshold voltage deviation due to process variation (*i.e.* $\partial V_{\mathrm{bp}}/\partial V_{\mathrm{t,P}} = 1$ in Eq. 4.11) accounting for another 45 mV (simulation shows $\Delta V_{\mathrm{t,P}}$ is 45 mV). Adding all of these numbers together, the minimum supply voltage should be >363 mV to ensure proper operation. Therefore, we choose a 0.4 V supply. All transistors were carefully sized to ensure M_1 and M_4 are in saturation at the highest temperature (worst case) and Monte Carlo simulations were conducted to check the circuit operation across process variation.

Without compensation, I_{ref} does not achieve as good of temperature-linearity as indicated by (4.7) due to channel length modulation and drain-induced barrier lowering. Consequently, this non-linear PTAT current would ruin the linearity of the CTAT comparator delay, thereby degrading the temperature stability. To remedy this, a pseudo-differential amplifier (PD-AMP) that forces the PMOS transistors to have the same V_{DS} was inserted into the bias circuit (Figure 4.4). As illustrated in Figure 4.5(a), the linearity of I_{ref} is improved by 25× from -20°C to 70°C in simulation. The feedback also improves the I_{ref} sensitivity to changes in the supply voltage (*i.e.* power supply rejection ratio), as the change modulates V_{DS} of each transistor, and therefore the current. Simulation shows I_{ref} variation reduces from 1% to 0.025% for supply voltages from 0.3 V to 0.6 V [Fig. Figure 4.5(b)]. The PD-AMP is implemented by scaling the original bias circuit by a factor of β_1 to ensure the transistors in PD-AMP have the same headroom as the rest of the bias circuit. Since temperature drift is generally slow, the bandwidth requirement for the PD-AMP is greatly relaxed. Thus, we choose β_1=3 to reduce the power overhead.

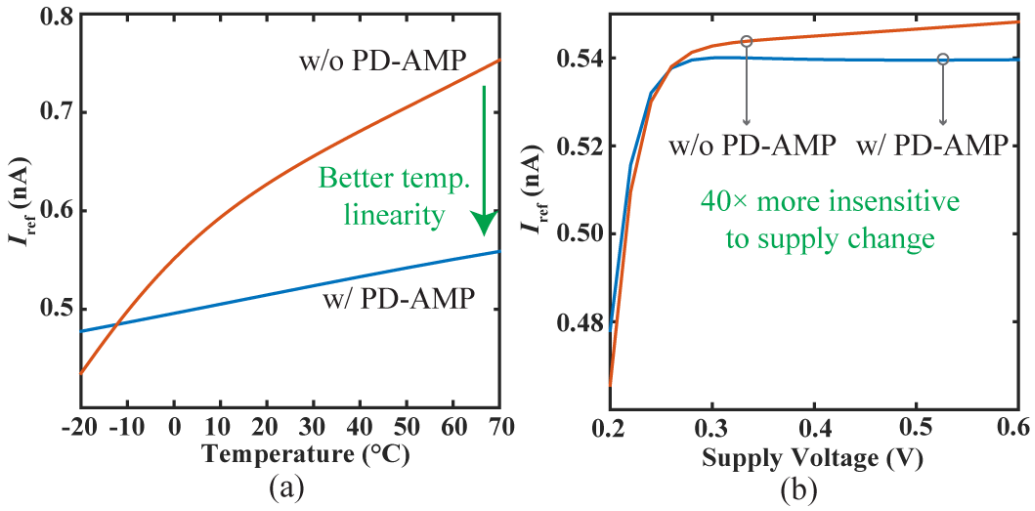


Figure 4.5. Simulations showing (a) reference current vs. temperature, and (b) reference current vs. supply voltage.

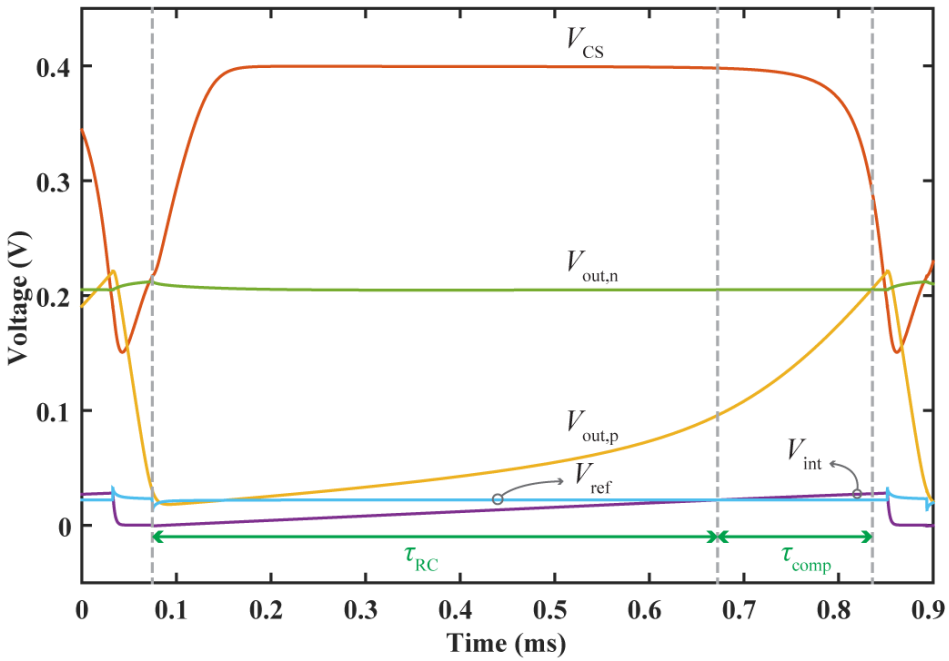


Figure 4.6. Simulated waveforms for one oscillation cycle.

4.2.2.4 Two-Stage τsw-Cancelling Comparator

The 1st stage of the comparator is a common gate (CG) amplifier that reuses part of the reference circuit. This stage doesn't add any power and, as such, has been widely used [70]–[72]; however, it suffers from long and temperature-sensitive delay especially when the bias current is low. Rather than burning additional power to minimize the comparator delay, the technique described in Section II is applied. Since the *R*-branch and the *C*-branch are matched, $V_{\mathrm{out,n}} = V_{\mathrm{out,p}}$ when $V_{\mathrm{int}} = V_{\mathrm{ref}}$ assuming infinite bandwidth. Therefore, $V_{\mathrm{out,n}}$ maps to $V_{\mathrm{ref,o}}$ in the model in Section II and V_{SW} is calculated by shorting the input and output of the buffer stage [73]. If the CG stage feeds into the inverter chain directly, then V_{SW} is the voltage when the inverter input and output is connected. Assuming the n is the same for both PMOS and NMOS transistors, the switching point of the inverter is

$$V_{\mathrm{SW,inv}} \approx \frac{1}{2}\left[V_{\mathrm{DD}} - nV_{\mathrm{T}}\, ln\left(\frac{K_{\mathrm{N}}}{K_{\mathrm{P}}}\right) - \left|V_{\mathrm{t,P}}\right| + V_{\mathrm{t,N}}\right], \quad 4.14$$

Using the same method as in (4.13), it can be shown that $V_{\mathrm{out,n}}$ ($\approx V_{\mathrm{bn}}$) only depends on the threshold voltage of the NMOS transistor, which shows a CTAT temperature dependence. Thus, $V_{\mathrm{SW,inv}}$ will not track $V_{\mathrm{out,n}}$, and $V_{\mathrm{SW,inv}} - V_{\mathrm{out,n}}$ is PTAT due to $-\left|V_{\mathrm{t,P}}\right|$ term in (4.14). Simulations show that $V_{\mathrm{SW,inv}} - V_{\mathrm{out,n}}$ has a strong PTAT temperature dependence (6,500 ppm/°C). When setting *R* to be PTAT, τ_{SW} exhibits a significant positive 2nd order TC due to the cross-multiplying between two PTAT terms with large TCs according to (4.6) and (4.10). Although $\kappa\tau_1$ can be designed to be CTAT to counteract the PTAT *RC* core, therefore minimizing the 1st order TC of T_{OSC}, it is the curvature over temperature that cannot be easily compensated. For example, when designing $\kappa\tau_1/T_{\mathrm{OSC}} = 22\%$, the strong 2nd order TC of τ_{comp} is only scaled by ~22% when adding into T_{OSC}, and consequently the oscillator can achieve, at best, a temperature stability of ~28,800 ppm (2nd order TC is 12.5 ppm/°C^2) over the 90°C range. This simulation is conducted using an ideal resistor with a 1st order TC; as such, the non-linearity from the resistor is isolated while examining the comparator temperature dependence. This is why conventionally designs have added more current to minimize $\kappa\tau_1$, while using a near-zero TC resistor to mitigate the curvature of τ_{SW}. Unfortunately, this is not power efficient and the residue TC (both 1st order and 2nd order) of τ_{SW} potentially limits the overall temperature stability. Furthermore, more current in the CG amplifier means sourcing more current in all three branches of the circuit, which is very inefficient.

To cancel τ_{SW}, a common source (CS) stage is added to the existing CG comparator (Figure 4.4). As shown in Figure 4.6, this CS stage is off during most of a cycle since $V_{\mathrm{out,p}}$ is low. It doesn't turn on until $V_{\mathrm{out,p}}$ approaches $V_{\mathrm{out,n}}$. Thus, it behaves more like a dynamic buffer, rather

than a continuous-time amplifier. The switching voltage, $V_{\mathrm{SW,CS}}$, is approximately $V_{\mathrm{out,n}}$, and as such $V_{\mathrm{SW,CS}} - V_{\mathrm{out,n}}$, and consequently τ_{SW} is cancelled. Since V_{bn} tracks the NMOS V_{t}, τ_{sw} is zero. To ensure good matching, the large devices were used and interdigitated in layout. It should be noted that the PMOS in the CS stage can be biased by either V_{bp} or V_{bp2} from the PD-AMP, which is equal to V_{bp} assuming perfect matching. We used V_{bp2} for layout convenience. With a cancelled τ_{SW}, biasing the CG comparator with I_{ref} results in well-controlled CTAT time constant and thus a CTAT τ_{comp}.

Like a current-starved inverter, the delay of the CS stage is inversely proportional to the bias current scale factor β_2. Through proper sizing, we chose β_2=3 to maintain low power while reducing the temperature stability degradation due to longer τ_{buf} and τ_{rst} [Figure 4.7(a)]. As shown in Figure 4.4, including the CS amplifier, the whole buffer chain has four stages to minimize the overall buffer propagation delay τ_{buf} (10 µs at room temperature) and sharpen the transition edges. The additional CS stage reduces the overall TC curvature by 8× in simulation due to the cancelled τ_{SW} while still maintaining $\kappa\tau_1/T_{\mathrm{OSC}} = \sim 22\%$ [Figure 4.7(b)]. Simulation also shows that the 2nd order curvature flips after adding the CS stage, which is expected because cancelling τ_{SW} removes the positive 2nd order TC of τ_{SW} and manifests the smaller negative 2nd order TC of $\kappa\tau_1$. A 50-point Monte Carlo simulation with process variation and mismatch showed that the TC varied from 33 ppm/°C to 121 ppm/°C over -20°C to 70°C after calibration – a significant improvement over the ~2,000 ppm/°C of the circuit in Figure 4.1(a) for the same I_{ref}.

To illustrate the effectiveness of controlling τ_{comp}, two cases were simulated. As shown in Figure 4.8(a), when R is set to a zero TC, τ_{RC} is constant while τ_{comp} is CTAT, and thus T_{OSC} is CTAT. When R is set with a positive TC, τ_{RC} becomes PTAT while τ_{comp} remains CTAT (but

with a smaller TC), and the overall T_{OSC} is temperature insensitive. The 2nd order TC of τ_{comp} degrades from -7.73 ppm/°C^2 to -15.8 ppm/°C^2 after using the PTAT resistor. As a result, the 2nd order TC of T_{OSC} degrades from -1.76 ppm/°C^2 to -4.27 ppm/°C^2 accordingly. This is as expected, because the non-zero TC of the resistor modulates κ over temperature and creates a 2nd order nonlinearity. Note, C_{int} is ~13 pF, which results in $\tau_{\mathrm{RC}} \approx 610\ \mu\mathrm{s}$ (74% of T_{osc}) at room temperature [Figure 4.8(a)], $\tau_{\mathrm{comp}} \approx 183\ \mu s$ (22% of T_{osc}), and the remaining 4% of T_{OSC} is made up of τ_{buf} and τ_{rst}, which have little impact on the overall temperature stability. In summary, the additional circuits (PD-AMP and CS stage) increase the power by 34%, but improve the temperature stability by 50× compared to the original circuit for the same I_{ref}. Compared to conventional approach by reducing $\tau_{\mathrm{comp}}/T_{\mathrm{OSC}} < 1\%$ with 20× larger I_{ref}, this technique saves ~20× comparator power and ~5× total power.

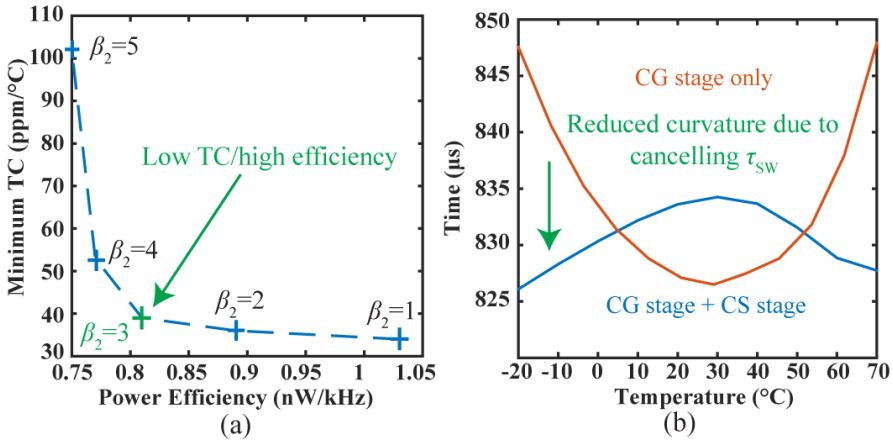


Figure 4.7. Simulation showing (a) TC vs. power efficiency for different sizing ratios, and (b) T_{OSC} vs. temperature showing curvature.

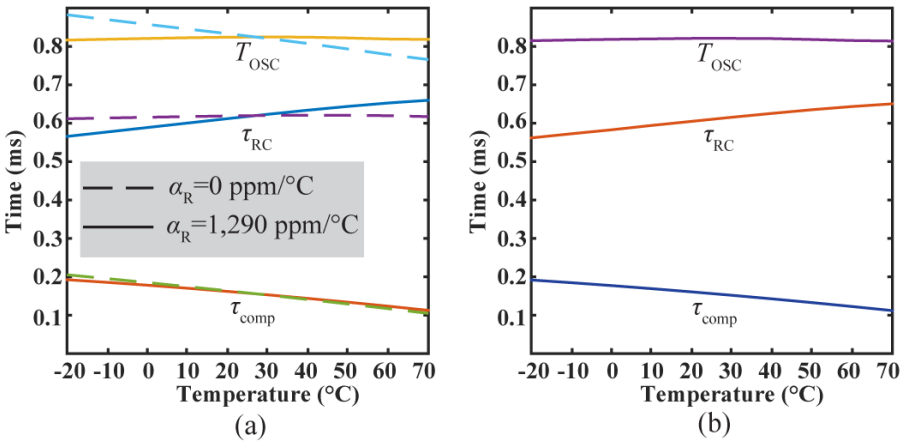


Figure 4.8. Simulated delays with (a) ideal resistors and (b) actual RDAC.

4.2.2.5 Bias Resistor DAC (RDAC) and Clock Booster

To compensate the CTAT comparator delay, the bias resistor must be trimmed, like other relaxation oscillators that are trimmed to yield zero-TC, though in this case to yield a PTAT *RC* core. All modern CMOS technologies have polysilicon resistors (always PTAT) and diffusion resistors (either PTAT or CTAT, depending on grain size and doping concentration [74]), and thus modern processes support PTAT resistors with adjustable TC, α_{R}, via two series PTAT resistors with different TCs (*e.g.*, α_{R1} and α_{R2}).

Based on (4.6), with a CG+CS comparator, the oscillation period is

$$T_{\mathrm{OSC}} \approx C_{\mathrm{int}} R_0 [1 + \alpha_{\mathrm{R}}(T - T_0)] + \kappa\tau_1, \qquad 4.15$$

where R_0 is the resistance of R at room temperature and α_{R} is the compound TC of R. By substituting (4.7) and (4.8) into the 1st order derivative of (4.15), an optimal α_{R} can be calculated as

$$\alpha_{\mathrm{R,opt}} = \frac{V_{\mathrm{A}} C_{\mathrm{CG}}}{\ln(2) n V_{\mathrm{T0}} C_{\mathrm{int}} + V_{\mathrm{A}} C_{\mathrm{CG}}} \cdot \frac{1}{T_0}, \quad 4.16$$

where V_{T0} is the thermal voltage at T_0 and C_{CG} is the output capacitance of the CG stage. The $\alpha_{\mathrm{R,opt}}$ was calculated to be ~1,700 ppm/°C, and simulated to be ~1,290 ppm/°C. The difference comes from the κ variation and 1st order TC from τ_{buf} and τ_{rst}. The nonlinear and time-variant behavior of the comparator also affects the accuracy of calculating $\alpha_{\mathrm{R,opt}}$. To overcome process variation, the resistor is implemented as an RDAC via a series combination of 5b PTAT and CTAT resistors. The frequency can also be tuned by adjusting both resistors and maintaining the same ratio. The oscillator temperature stability was simulated again with the actual RDAC [Figure 4.8(b)]. The 2nd order nonlinearity (3.99 ppm/°C^2) of T_{OSC} is almost the same as the case using an ideal resistor, demonstrating that the 2nd order TC of the actual resistor is not an issue in this design.

Since the $R_{\mathrm{off}}/R_{\mathrm{on}}$ of a MOS switch is small at low supply voltages, a charge pump driven by this oscillator output generates a $-V_{\mathrm{DD}}$ voltage to place the RDAC switches in super-cutoff resulting in >50× larger $R_{\mathrm{off}}/R_{\mathrm{on}}$ that would otherwise limit the operation range to ~50°C. The discharge switch in parallel with C_{int} is driven by a modified clock booster [75] to minimize the discharge time and consequently τ_{rst} over PVT (Figure 4.4). After the capacitor is discharged, the comparator flips and resets the buffer when $V_{\mathrm{out,p}}$ drops below $V_{\mathrm{sw,CG}}$. Thus, there exists a 2nd comparator delay as a part of τ_{rst}. Fortunately, the 2nd comparator delay is very short (8 µs, <1% of T_{OSC}), because firstly the comparator sees a step V_{int} this time, instead of a ramp, and secondly $V_{\mathrm{out,p}}$ only needs to drop a small voltage range to offset the overshoot caused by τ_{buf}. Then the buffer resets (2nd buffer delay) and turns off the switch. Simulation shows τ_{rst} is less than 3% of T_{OSC} with the help of the clock booster.

4.3 Signal Path Temperature Compensation

4.3.1 RF/Conversion Gain

The passive RF gain does not exhibit significant temperature dependence since it is comprised of passive elements that themselves do not have large temperature coefficients (TCs). Thus, no explicit compensation is required. However, the ED *k* factor depends on the sub-threshold slope factor, *n*, and the thermal voltage V_T [51]:

$$k \propto N\left(\frac{1}{n}-\frac{1}{2}\right)\frac{1}{V_T}, \tag{4.17}$$

Simulation shows that the *k* factor changes by 25% from -10 to 40°C, which corresponds to a sensitivity loss of only 1.2 dB. This was deemed to be acceptable, in part because the relatively low loss, and because further compensation would incur a significant power penalty.

4.3.2 ED Temperature-Stabilization via a CTAT Bulk Bias

The ED bandwidth exhibits a strong temperature dependence and must be compensated. The proposed solution is straightforward: since the ED output bandwidth is set by the output impedance of the ED, its bandwidth can be fixed by directly adjusting the output impedance via a bulk-biasing technique. Specifically, for the diode connected transistors of the ED, the diode channel resistance, r_d, is temperature dependent because of the threshold voltage, which is given by:

$$V_t = V_{t,0} + \gamma\left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right) \approx V_{t,0} + \frac{\gamma V_{SB}}{4\emptyset_F}, \tag{4.18}$$

where $V_{t,0}$ is the threshold voltage for zero substrate bias, γ is the body effect parameter, V_{SB} is the source-to-body substrate bias, and $\emptyset_F$ is half surface potential. The approximation is valid, given $|V_{SB}| < |2\emptyset_F| \approx 0.7$ V. To compensate the complementary-to-absolute-temperature (CTAT) $V_{t,0}$, and the proportional-to-absolute-temperature (PTAT) $2\emptyset_F$, V_{SB} needs to be PTAT as well to keep

V_t and r_d constant. Based on simulation for the 65 nm CMOS process, a +10 mV/°C change compensates the threshold voltage change.

To accomplish this, the bulk voltage of the ED's transistors is fed by a CTAT voltage to generate the desired PTAT V_{SB}. Figure 4.9 shows the schematic of the CTAT bulk voltage generator, which consists of a PTAT 3-transistor temperature sensing element and a PTAT to CTAT amplifier. The PTAT element is similar to the work in [76], [77], and generates a 1.2 mV/°C PTAT voltage. The PTAT element is biased between V_{DD} and -V_{DD}, which is generated by an on-chip charge pump [2], to provide a negative output voltage covering 10 to 40°C range. The PTAT voltage is converted to CTAT and the slope is corrected to cover the 500 mV difference in V_{SB} required for -10 to 40 °C. The programmable resistors provide a tunable multiplication ratio to overcome process variation. Note, the multiplication ratio is independent of the TC of the resistors. The entire ED compensation block consumes 11.8 nW at 20 °C.

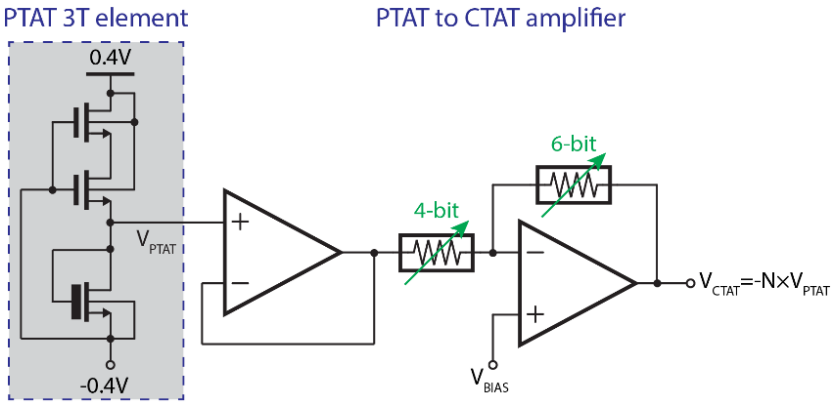


Figure 4.9. Schematic of the ED bulk bias circuit.

4.3.3 BB Amplifier Temperature-Stabilization via a Constant-Current Bias

The BB amplifier's bandwidth also exhibits a strong temperature dependence. As shown previously, the BB amplifier is loaded by 10 pF MIM capacitors, which exhibit almost no

temperature sensitivity. As a result, the temperature dependence of the bandwidth is dominated by the change of the amplifier output resistance

$$BW_{\mathrm{AMP}} \propto 1/r_{\mathrm{AMP}} \propto \lambda I_{\mathrm{AMP}}, \tag{4.19}$$

where r_{AMP} and I_{AMP} are the output resistance and bias current of the BB amplifier, respectively, and λ is the channel length modulation parameter. It has been shown that λ exhibits no significant temperature variation, which means that if the amplifier bias current is constant, so would its bandwidth [65].

A regulated Beta-multiplier is employed to generate a temperature insensitive current. As shown in [65], the bias resistor TC should be ~1/300 (*i.e.* 3,333 ppm/ K) when compensating the system in the vicinity of 300 K. This led to choosing to implement the biasing resistor as a P+ polysilicided resistor with a TC of ~2,880 ppm/K, which is close to the optimal value. The residue TC of the bias current (~500 ppm/K in simulation) corresponds to a 2.5% variation in BW over the -10 to 40 °C temperature range.

4.3.4 Comparator Threshold Dynamic Tuning

Since the BB amplifier is operating in an open-loop way, its dc gain and thus, the BB signal swing and noise amplitude, are sensitive to the PVT variation. To obtain the desired MDR and FAR, the comparator should be set to an optimal value, *e.g.*, 2× the noise standard deviation. An automatic comparator threshold control loop that dynamically tunes the threshold voltage for an optimal value has been widely used for interferer rejection [29], [31]. In fact, this loop also improve the robustness against the temperature variation: when temperature increases, the BB amplifier gain drops, and the comparator tends to generate more zeros than expectation, then the logic adjusts the comparator threshold to be lower to increase the probability of generating zeros. Thus, the

zeros and ones distribution would converge to the expectation, which is programmed based on the desired MDR and FAR values. The block diagram of this logic is shown in Figure 4.10. Since this technique have been demonstrated in prior work and the schedule was tight during the prototype implementation, this logic was not implemented in this work.

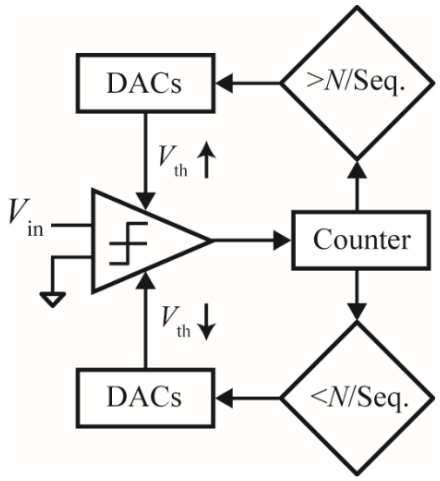


Figure 4.10. Block diagram of the comparator threshold dynamic tuning logic.

4.4 Measurement Results

4.4.1 Relaxation Oscillator Measurement

The proposed oscillator was fabricated in a 0.18µm CMOS SOI process with an active area of 0.2 mm^2 (Figure 4.11). Operating at 0.4 V, the power consumption measured at room temperature was 1.14 nW, 70% of which was static power consumed by the reference generator and comparator, with no significant difference in different chips (n = 5). The frequency of each chip was tuned to be ~1,220 ± 15 Hz. Figure 4.12(a) shows the measured frequency of the same oscillator with different RDAC configurations. The TC of the frequency becomes negative when increasing the PTAT/CTAT resistor ratio, and vice versa. By keeping the ratio fixed, the frequency

can be tuned with a step size of ~30 Hz. The power when calibrated to 1,210 Hz is plotted versus temperature in Figure 4.12 (b). After a 2-point calibration, the measured temperature coefficient varied from 40-155 ppm/°C (n = 5) over the -20°C to 70°C range [Figure 4.13(a)]. Due to the process variation, each chip requires separate calibration, but both the PTAT and CTAT RDAC configuration codes varied less than 6 LSBs across all five chips.

Figure 4.13(b) shows the Allan deviation plot in an uncontrolled room temperature environment. The total measurement duration was 300 s, which means each data point was obtained by >10 times averaging. The short-term uncertainty (jitter) of a relaxation oscillator has been shown to be proportional to the comparator input-referred voltage noise at the switching moment [78]. Thus, the CG comparator with lower bias current inevitably has larger input-referred voltage noise, and therefore larger jitter. This explains why the short-term deviation (*e.g.*, >200 ppm in 0.1 s) is larger than previous works. However, the jitter of such low-power oscillators is typically not an issue in IoT applications because it is used as timer or real-time clock in a wireless network. Thus, long-term stability (Allan deviation floor) is often used to evaluate the noise performance. The oscillator required ~3 s to reach a 58 ppm floor, which is comparable to previous works.

The oscillation frequency generally doesn't change with the supply, since both τ_{RC} and τ_{comp} are independent of supply voltage, to the first order. However, when the comparator is ramping, its V_{DS} changes significantly (Figure 4.6), and therefore the equivalent r_{o} is not constant. When the supply increases, the V_{DS} of CG NMOS transistor also increases, resulting in larger r_{o} and longer τ_{comp}. The measured frequency dropped by 4.3% when the supply was increased from 0.4 V to 0.65 V [Figure 4.13(c)]. Fortunately, this is not a serious issue when operating under a local regulated supply, which is common in IoT nodes. The power did increase by 13× at 0.65 V,

mostly from the body leakage currents of the custom inverters with dynamic threshold-voltage MOSFETs [79], since the static bias current is immune to the supply change due to the PD-AMP. No significant difference was observed from different chips. The temperature stability was examined at different supply voltage without re-calibration. As shown in Figure 4.13(d), the stability is almost unchanged except the center frequency drops when the supply increases. This oscillator achieves state-of-the-art performance with the lowest power consumption (1.14 nW) at the lowest supply voltage (0.4 V) and the best efficiency (0.93 nW/kHz) among kHz-range temperature-compensated relaxation oscillators (Table 4.1).

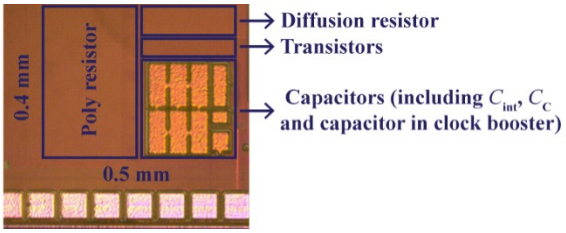


Figure 4.11. Die photo annotated with components.

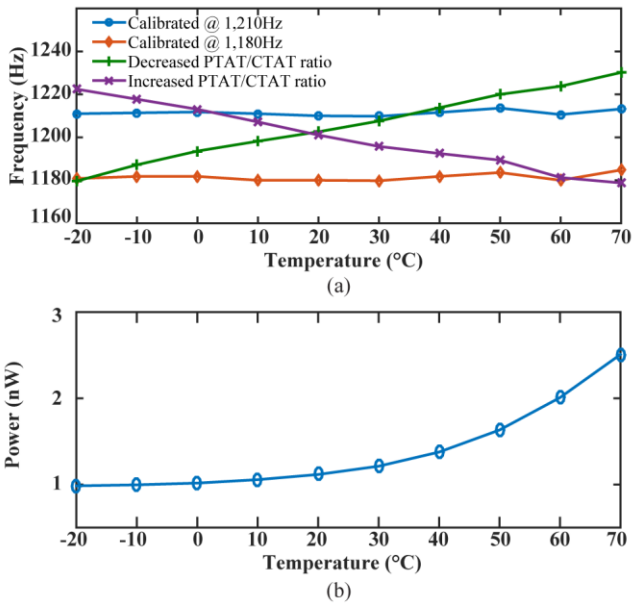


Figure 4.12. Measured (a) temperature sensitivity, and (b) power vs. temperature.

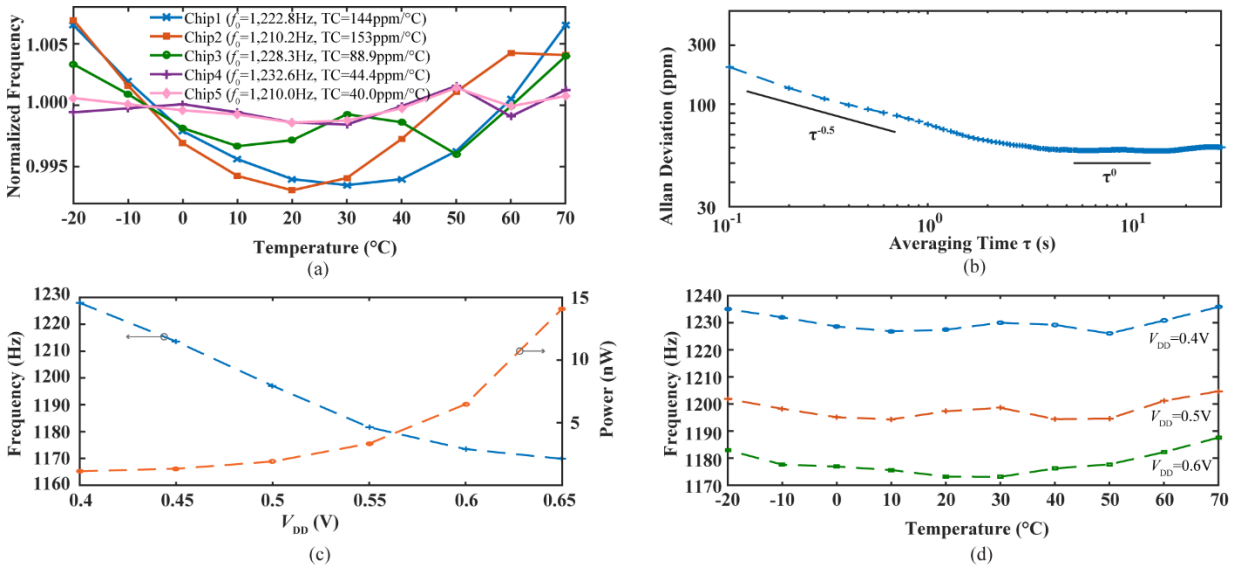


Figure 4.13. Measured (a) temperature sensitivity of 5 chips, (b) Allan deviation, (c) frequency and power vs. supply voltage, and (d) temperature sensitivity at different supply voltages.

Table 4.1. Performance comparison of low power kHz-range integrated oscillator

Parameter	Dai CICC'15	Tokairin VLSI'12	Paidimarri JSSC'16	Denier TCAS'10	Chiang TCAS'14	Jang ISSCC'16	Wang JSSC'16	Griffith ISSCC'14	Shrivastava CICC'12	This Work
Tech. (nm)	180	90	65	350	180	180	250	65	130	180
Freq. (kHz)	122	100	18.5	3.3	28	3	6.4	33	100	1.22
Supply (V)	0.6	0.8	1.0	1.0	1.2	0.85	0.8	1.2	1.1	0.4
Area (mm^2)	0.03	0.12	0.032	0.1	0.16	0.5	1.08	0.015	0.25	0.2
Allan Dev. Floor (ppm)	40	N/A	20	N/A	N/A	63	60	4	N/A	58
Temperature Range (°C)	-20 to 80	-40 to 90	-40 to 90	-20 to 80	-20 to 80	-25 to 85	-20 to 80	-40 to 90	20 to 40	-20 to 70
Calibration?	N/A	N/A	N/A	Multi-point	Yes	N/A	No	Yes	1-point	2-point
TC (ppm/°C)	327	105	38.5	<500	95.5	13.8	148	38.2	5	94
Power (nW)	14.4	280	120	11	40	4.7	75.6	190	150	1.14
Power Efficiency (nW/kHz)	0.12	2.8	6.49	4.0	1.43	1.57	11.8	5.86	1.5	0.93

4.4.2 Signal Path across Temperature Measurement

The RF die (ED, CMFB, and BB amplifier) was fabricated in a 65 nm CMOS process, while the baseband die (temperature compensated bias generators) was fabricated in a 180 nm CMOS process. At room temperature, the temperature compensation blocks consume an additional 15 nW on top of the core WuRX circuit.

The performance of the temperature compensation blocks was characterized from -10 to 40 °C. The ED bulk bias showed a CTAT behavior with -10 mV/°C coefficient [Figure 4.14(a)], and the amplifier bias current was almost temperature-insensitive with only 2.6% change across the temperature range [Figure 4.14 (b)]. The relaxation oscillator frequency dropped from 67.1 Hz to 66.1 Hz, which is stable enough to avoid a missing bit or redundant bit given the 540 ms long sequence.

The overall BB bandwidth and integrated noise of the whole system were both measured across temperature, as shown in Figure 4.15(a). The bandwidth was nearly constant between 0 and 30 °C owing to the bias techniques applied to ED and BB amplifier. The bandwidth dropped at -10 °C since the amplifier PMOS tail transistor was at the edge of saturation, resulting in less current. The bandwidth increased at 40 °C because the amplifier's input transistors were at the edge of saturation, thereby exhibiting lower output impedance. Both could be overcome with a larger supply voltage, at the expense of higher quiescent current. As expected, the integrated noise slightly increased with the temperature [Figure 4.15(a)] since the noise is mostly determined by the ED output integrated noise, which is PTAT given a fixed ED output capacitance. The combined MN gain, ED k factor ($=A_v^2 k$), and amplifier dc gain are plotted in Figure 4.15(b). Across temperature, the gain dropped by 29%, which matches simulation. The amplifier gain dropped by 6 dB because of the open-loop, uncompensated architecture.

Figure 4.16 shows the waterfall curves for the wake-up signature missed detection rate (MDR) over temperature without the antenna. The system configurations (*e.g.*, bias settings and comparator threshold setting) were fixed during the temperature sweep. Since the amplifier gain increases as the temperature decreases, the comparator sees a larger signal and noise amplitude at lower temperature. With a fixed threshold voltage, the worst false alarm rate (FAR) happens at the

low temperature (-10 °C), while the worst MDR occurs at high temperature (40 °C). This explains the shifting of the MDR curves over temperature.

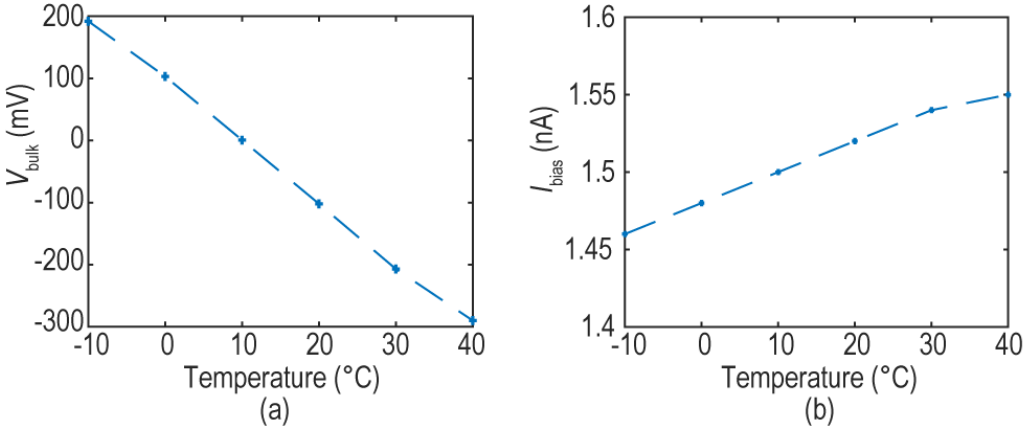


Figure 4.14. Measured (a) ED bulk bias, and (b) BB amplifier current reference.

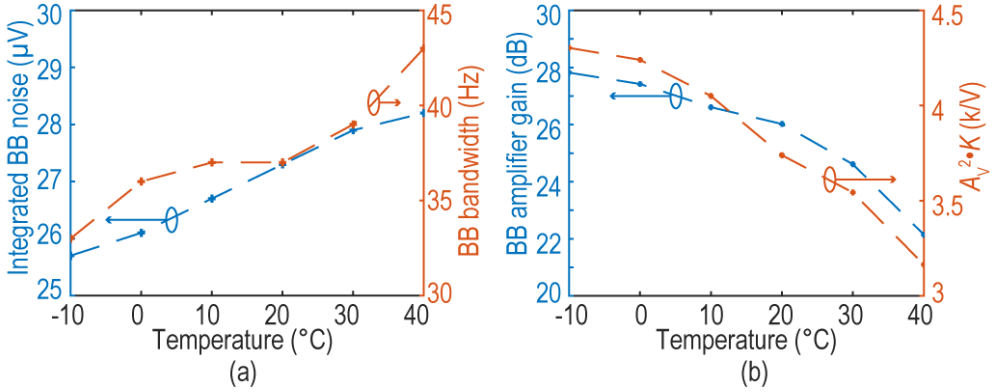


Figure 4.15. Measured (a) BB bandwidth and noise, and (b) BB gain and RF/conversion gain.

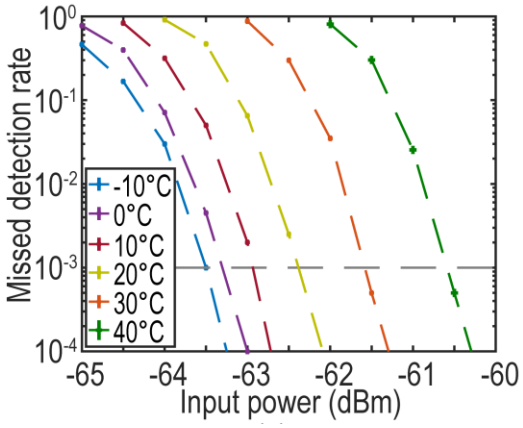


Figure 4.16. Measured MDR curves over temperature.

4.5 Conclusion

For the first time, the temperature stability of the WuRX has been studied. The specifications and behaviors of every block across the temperature is carefully examined. The ED and BB amplifier are compensated in an analog with temperature stabilized bias generation. The Comparator could be compensated digitally for the best robustness. Regarding the local timer, the comparator delay and temperature dependence of a relaxation oscillator based on a ramp response model was analyzed. A two-stage τ_{SW}-cancelling comparator and a technique that utilizes the linear temperature-dependent delay were proposed to implement a relaxation oscillator for low power and low voltage applications. Measurement results validate the proposed technique and demonstrate state-of-the-art performance.

Chapter 4, in part, is based on materials presented in Haowei Jiang, Po-Han Peter Wang, Patrick P. Mercier and Drew A. Hall, "A 0.4-V 0.93-nW/kHz Relaxation Oscillator Exploiting Comparator Temperature-Dependent Delay to Achieve 94-ppm/°C Stability," in *IEEE Journal of Solid-State Circuits*, Oct. 2018, and Haowei Jiang, Po-Han Peter Wang, Li Gao, Corentin Pochet, Gabriel M. Rebeiz, Drew A. Hall, Patrick P. Mercier, "A 22.3 nW, 4.55 cm^2 Temperature-Robust Wake-up Receiver Achieving a Sensitivity of -69.5 dBm at 9 GHz," in *IEEE Journal of Solid-State Circuits*. The dissertation author was the primary investigator and author of these papers.

Chapter 5

A 2-in-1 Temperature and Humidity Sensor

5.1 Introduction

Environmental monitoring plays a key role in industrial automation and human well-being, comfort, and productivity. For example, environmental data is required in applications ranging from micro-climate control, process control systems [80], [81], storage and transportation [82], to climate/weather monitoring [83]. Multiple parameters, such as temperature and humidity, are often collected together [21], [82]–[84]. Wireless connectivity allows many such sensors to operate both independently and in a networked fashion. Taken together, these devices fit with the recent surge in the internet-of-things (IoT) applications that promises to integrate trillions of sensors into one's daily life. However, to achieve such a massive deployment, there are stringent requirements on the sensor's cost, power consumption, and size. As such, there is a strong need to monolithically integrate temperature and humidity sensors.

A key challenge in this vision is to combine the sensors in a compact and power efficient manner as they utilize fundamentally different transduction mechanisms and therefore typically require different analog front-ends (AFEs), as shown in Figure 5.1. For example, CMOS-compatible temperature sensors use resistors [85]–[90], MOSFETs [91]–[93], or bipolar junction transistors (BJTs) [94] as the transducer. On the other hand, most RH sensors are based on a capacitive polymer where a moisture-induced dielectric constant change results in a change in capacitance [18], [21], [80], [81], [95]. Among the various of polymers that exhibit this property, polyimide (PI) is the most popular because it is already used in CMOS foundries. While it is possible to integrate both transducers into a single CMOS chip, prior work has used separate AFEs (*e.g.*, an instrumentation amplifier for the temperature sensor and a charge amplifier for the RH sensor) with only a few works combining the two monolithically [21]. Using separate AFEs and transducer bias circuits doubles the power, area, and complexity [21].

To integrate multiple environmental sensors in an efficient way, this paper presents a resistor-based temperature transducer and a capacitor-based RH transducer combined with a 2-in-1 R&C-to-digital converter (RCDC) front-end that eliminates the need for two distinct AFEs, as shown in Figure 5.1. The RCDC realizes a *R*&*C*-to-time conversion via a frequency-locked loop (FLL). Compared to prior art with open-loop voltage-controlled oscillator (VCO)-based conversion [96], the FLL suppresses the nonlinearity and process, voltage, and temperature (PVT) variation from the VCO to ensure high-linearity conversion. A highly digital time-to-digital converter (TDC) samples the FLL outputs in the phase domain and achieves high dynamic range due to inherent noise-shaping, obviating the need for a conventional voltage domain sigma-delta modulator (SDM) resulting in lower power and area.

The key block within the loop, the *RC*-based time-to-voltage conversion, is realized by an incomplete-settling, switched-capacitor (SC)-based Wheatstone bridge (WhB). Compared to prior work (frequency references [97]–[100] and *C*-sensor [101]) that drive the SC cell with integrators or low-dropout regulators (LDOs), a SC-based WhB that needs no active driver is proposed to improve the noise and power efficiency. Due to the absence of an active driver, incomplete settling is inevitable in the proposed circuit. This work demonstrates that by adding a charge-preserving capacitor and sizing it appropriately, the incomplete-settling SC circuit still exhibits high accuracy (<10 ppm error) and PVT insensitivity at a lower power consumption than prior art. Furthermore, the WhB provides high immunity to supply variation (0.12 °C/V or 0.43 %RH/V) across a wide supply range (1.5 to 2 V), which is needed in battery powered IoT devices. The proposed RH/Temp sensor achieves state-of-the-art RH sensitivity (0.0073 %RH) and high temperature sensitivity (2 mK) while consuming only 15.6 pJ/meas. – 20× lower than commercial RH/Temp sensors [20].

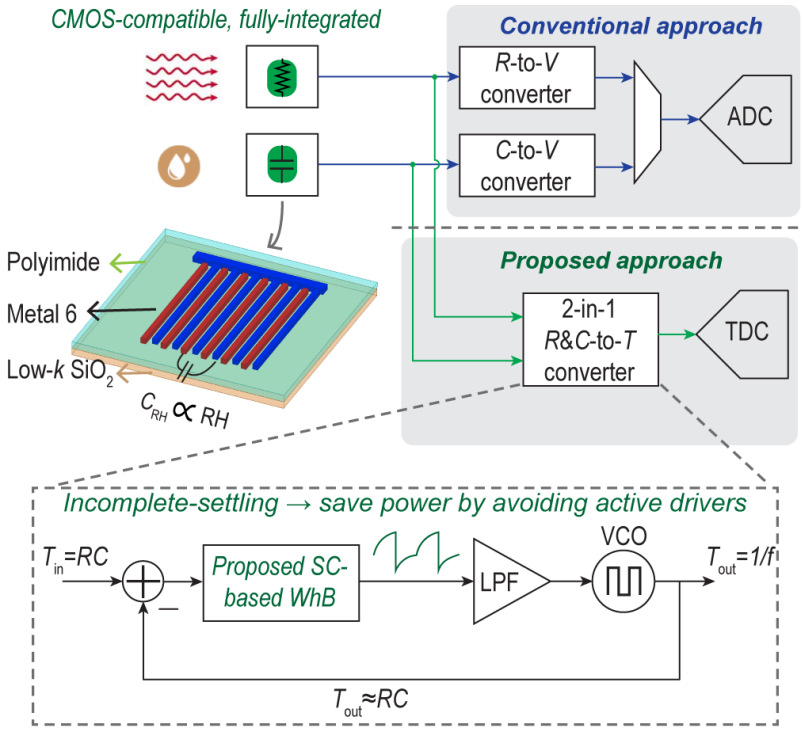


Figure 5.1. Architecture of the 2-in-1 temperature and relative humidity sensor.

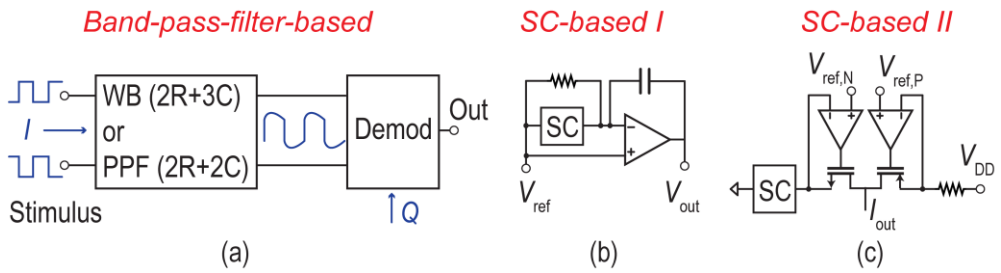


Figure 5.2. Prior work that could be used for R&C sensing, based on (a) a band-pass-filter, (b) a SC integrator, and (c) a SC resistor and LDO.

5.2 Prior *R*- & *C*-Interfaces

Prior resistive interface is either biased in voltage mode or current mode and generates voltage output [17]. The resistive sensor with best resolution and Figure-of-Merit (FoM) uses a WhB-based front-end in the voltage mode [89]. However, the high-performance partly stems from the fact that the WhB requires two resistive transducers with opposite temperature coefficients (TCs), which essentially doubles the transducer sensitivity resulting in a theoretical 6 dB better FoM compared to using a single transducer. Unfortunately, this interface doesn't scale well with technology since a negative TC resistor is not always available (*e.g.*, TSMC 65-nm). Furthermore, it cannot be modified for a *C*-sensor, since the interface only consists of resistors, not capacitors.

A capacitive sensor, more often referred as a capacitance-to-digital converter (CDC), typically combines the capacitive transducer into a charge-redistribution ADC, such as a successive approximation register (SAR) ADC, delta sigma modulator, or a hybrid structure [18], [101]. By referencing the capacitive transducer with respect to a capacitor bank, this architecture features high dynamic range (DR), low power consumption, and fast readout time. However, these popular CDC architectures only consist of capacitors, and don't support resistive-based sensors.

Although not being very popular, there are some *R*- & *C*-sensor interfaces reported in prior temperature sensors [85], [86], [88], [90], frequency references [97]–[100], [102], [103], and CDC [101]. These works can be loosely categorized into band-pass-filter (BPF)-based or SC-based circuits. As shown in Figure 5.2(a), the BPF-based circuit typically requires multiple matched (*e.g.*, poly-phase filter in [90]) or ratioed capacitors (*e.g.*, Wien bridge in [85], [86], [88]). However, duplicating the RH-sensitive film sensor requires large area (>0.2 mm^2) and the mismatch due to process variation is significant [80]. The parasitic capacitance of the floating capacitors and mismatch between them create nonlinear behavior and lowers the Q of BPF, thus reducing the sensitivity and accuracy. Thus, it is less suitable for a *C*-sensor than an *R*-based temperature sensor. The inherent nonlinearity of the BPF and phase-domain readout could also be problematic if not taken care of since: 1) the transducers gain error and offset turn into nonlinearity at the output, which cannot be calibrated out with 2-point trim; 2) the nonlinearity induced AM-PM modulation converts the in-band supply noise to phase noise at the output; 3) the sensitivity is maximal at the BPF center frequency and drops if the excitation frequency is misaligned due to PVT variation; and 4) it requires extensive, high-order linearity calibration. The poly-phase-filter approach has $>V_{DD}$ swing, and the Wien bridge, if operating in voltage-mode (which has the best sensitivity), also has near-rail-to-rail swing complicating the design of a continuous time readout circuit. Even operating the Wien bridge in current mode with an integrator, the amplifier, requiring either a distinct output driving stage to drive a resistive load with large swing or a very large g_m ($\gg 1/R$) for a low-impedance virtual-ground and high driving ability, consumes high power and doesn't scale well into low-power IoT applications [86], [88].

A SC-based method is combined with a charge-balancing SDM for readout as shown in Figure 5.2(b), where the SC circuit is driven by a closed-loop integrator [97], [100], [101]. Like

the phase-domain BPF readout, this method also requires a high-bandwidth, high-output current amplifier to charge and discharge the capacitor during every clock cycle to achieve low settling error (*i.e.* <½ LSB). While it avoids the parasitic capacitance, matching and nonlinearity issues compared the BPF-based method, an accurate, low-impedance voltage reference is required and adds extra power and noise. An alternative SC-based method [Figure 5.2(c)] uses two matched, LDO-based voltage sources with one driving a resistor and the other a SC resistor avoids the parasitic capacitance and capacitors matching issues with only one resistor and one capacitor (not floating) [98], [99]. However, it needs two active voltage sources and two references that add noise and power overhead. Recently, the LDO-based voltage sources have been eliminated by connecting the resistor and capacitor directly in timer designs [102], [103], but the sensitivity and accuracy are either not shown or compromised. Thus, there is a need to propose and analyze a new *R*- & *C*-interface for the RH/Temp application.

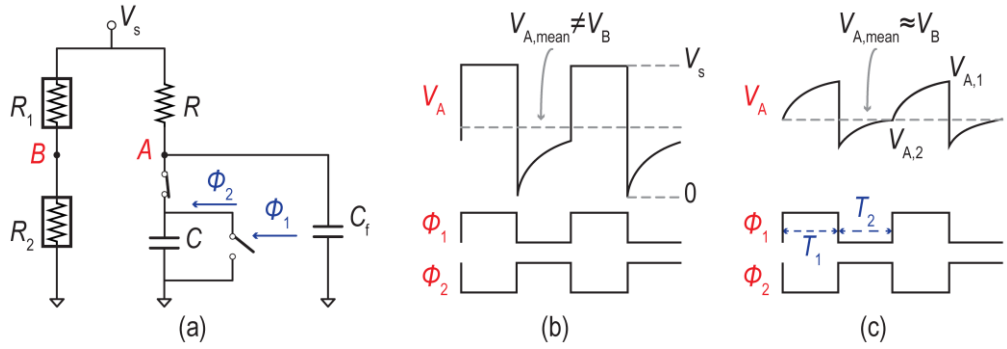


Figure 5.3. (a) Schematic of a SC-based WhB and transient waveforms (not to scale) when (b) $C_f = 0$ and (c) $C_f \gg C$.

5.3 Incomplete-Settling SC-Based WhB

To avoid active drivers, this paper proposes a SC-based WhB for *R*&*C* sensing based on the previous SC method but utilizing incomplete-settling for power savings. The schematic of the

SC-based WhB is shown in Figure 5.3(a). In one branch of the WhB, a capacitor C switched at frequency f_0 is connected to a voltage source V_s via a series resistor R whereas the other branch has two matched resistors in series. A shunt capacitor C_f is placed at node A. It should be noted that, unlike the well-known SC resistor where the charge transfer function is based on complete-settling, V_A doesn't settle completely to V_s due to the large RC time constant. Therefore, the SC resistance equation (*i.e.* $R = 1/f_0C$) doesn't hold. To show this, assume $C_f = 0$ which results in the V_A waveform shown in Figure 5.3(b). When the bridge is balanced (*i.e.* the average output voltage equals zero), the SC should be clocked at

$$f_0 = \frac{(1+e)D}{e}\frac{1}{RC}, \tag{5.1}$$

where e is the base of the natural logarithm and D is the clock duty cycle. With $D = 50\%$, $f_0 = 0.684/RC$. This suggests that due to incomplete settling, the SC should be clocked slower than the fully settled case. Like all incomplete-settling circuits, the settling error depends on the settling time and circuit time constant, therefore D and the parasitic capacitance at node A. As a result, although the error is deterministic, it is sensitive to the clock phase error and the parasitic capacitance, which is evitable when connecting the readout circuit to the WhB output. Due to its susceptibility to phase noise and parasitic capacitance (consequently PVT variation), this SC-based WhB cannot be used directly as the RC sensor front-end when C_f is small.

Instead of building a power-hungry circuit to minimize the settling error, a passive method is proposed by utilizing C_f. Through properly sizing, the settling error can be minimized. It essentially works as a passive integrator where during Φ_2, C extracts charge from C_f through charge sharing, which bypasses the slower path through R. During Φ_1, C dumps the charge to ground completely. Meanwhile, the lost charge of C_f during Φ_2 is supplemented from V_s through R. Ideally, when C_f approaches infinity, node A would stabilize to a near constant voltage, like the

virtual ground of an active integrator. With small enough switch on-resistance, C settles completely to that constant voltage during Φ_2, and its effective resistance is $1/f_0C$. Obviously C_f cannot be sized infinitely large due to the area, bandwidth, and start-up time constraints. To determine the appropriate value for C_f, a time-domain analysis was done in prior work [104]. The waveform at V_A and the two-phase clock are shown in Figure 5.3(b). The voltage at node A at the end of the two clock phases, $V_{A,\Phi 1}$ and $V_{A,\Phi 2}$, is

$$V_{A,\Phi 1} = V_s + \left(V_{A,2} - V_s\right) e^{-\frac{T_1}{RC_f}}, \tag{5.2}$$

$$V_{A,\Phi 2} = V_s + \left(\frac{C_f}{C+C_f} V_{A,1} - V_s\right) e^{-\frac{T_2}{R(C_f+C)}}, \tag{5.3}$$

where T_1 and T_2 are the period of the two phases. During each cycle, the charge Q being transferred is $CV_{A,2}$. Therefore, the node A average voltage is

$$\overline{V_A} = V_s - \frac{RQ}{T_1+T_2} = V_s - RQf_0, \tag{5.4}$$

With D = 50% and negligible deadzone between the two clock phases, substituting (5.2) and (5.3) into (2.1) with $f_0 = 1/RC$,

$$\begin{aligned} &\overline{V_A} = (1+\epsilon)\frac{1}{1+f_0RC} V_s \approx \frac{1}{1+f_0RC} V_s, \\ &\text{where } \epsilon = 1.5\left(1 - \frac{1}{\frac{C_f+C}{C} e^{\frac{C}{C+C_f}} - \frac{C_f}{C} e^{-\frac{C}{C_f}}}\right) - 1. \end{aligned} \tag{5.5}$$

Eqn. (2.1) shows that, on average node A is the output of a voltage divider, between R and a SC resistor whose resistance is approximately $1/f_0C$. ϵ is a parameter that evaluates the approximation error, which depends on the ratio of C_f/C. As the ratio goes to infinity, ϵ approaches zero, which endorses the intuitive explanation above. The calculated ϵ versus the ratio is plotted in Figure 5.4(a), which can be used as a guidance to choose C_f. For instance, C_f should be greater than $60C$ to make the error negligible (<10 ppm). Additionally, large C_f also attenuates the

susceptibility to parasitic capacitance and clock duty cycle. Additionally, this circuit is insensitive to the clock phase error, $V_{A,mean}$ deviates less than 0.3 ppm when the aperture jitter goes up to 100 ppm [Figure 5.4(d)]. The linear curve also suggests that even if there is a small linear phase error over temperature, the induced WhB output error is still linear. Therefore, the proposed approach robustly fixes the incomplete-settling issue in a passive manner. In contrast, without C_f power hungry active drivers are required to achieve the same result. Adding C_f (=60C) improves the SC accuracy by ~5,200× without a power penalty during steady-state.

Compared to prior *RC*-based front-ends, this technique has several benefits, namely: 1) High linearity due to the passive settling error reduction technique. 2) Inherent supply rejection due to the WhB structure. 3) Insensitivity to the parasitic capacitance at the outputs of and the variation of C_f. Thus, C_f can be implemented with a MOS capacitor to save area. 4) Due to incomplete-settling, the swing at V_A is <10 mV, which relaxes the readout circuit linearity requirement. Switching imperfections (*e.g.*, clock feedthrough) are attenuated by C_f.

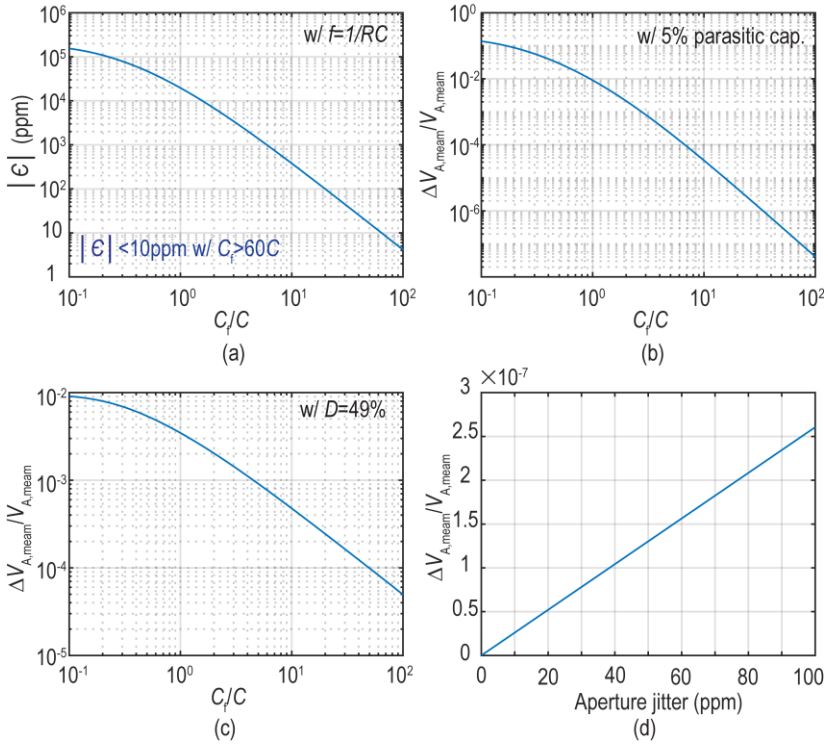


Figure 5.4. Simulated (a) $|\epsilon|$ vs. C_f/C, WhB output change vs. C_f/C (b) with 5% parasitic capacitance, (c) with 49% duty cycle, and (d) with a clock phase error.

5.4 System Design

5.4.1 System Architecture

The preceding analysis shows that if the bridge is balanced (*i.e.* $\overline{V_{AB}} = 0$), the R and C information can be readout from the clock frequency. To that end, a FLL is built around the SC-based WhB to drive the bridge into balance. As shown in Figure 5.5, two SC cells are connected to the bridge via a multiplexer and a silicided poly-resistor is used for temperature sensing. Among the two SC cells, a metal-insulator-metal (MIM) capacitor C is used as a reference and a polyimide film capacitor C_{RH} for humidity sensing. Optimizing for power, sensitivity, and area, a 330 kΩ resistor (at room temperature) and 4 pF capacitors were chosen. This results in a nominal output

frequency of ~758 kHz. C_f is set to be 240~250 pF given the 60× ratio requirement. The WhB is driven directly by the supply (*i.e.* $V_s = V_{DD}$), which is different from prior low-power timer work that implemented a separate voltage source [102], [103]. This maximizes the sensitivity and linearity while avoiding an additional noise source, as explained later.

V_{AB} is amplified and filtered to attenuate the ripple by an active lowpass filter (LPF). The LPF is chopped to remove temperature-dependent offset and the amplifier's 1/*f* noise. A VCO converts the LPF output voltage V_{VCO} into f_o, with a nominal period of t_0. Since it is a linear signal transfer function from the RH/Temp to t_0, t_0 instead of f_0 is taken as the output of the FLL. A 2-phase non-overlapping clock generator closes the loop by feeding back the frequency to the SC cells in the WhB. The FLL outputs during the temperature and RH measurement modes are

$$\begin{aligned} t_{\mathrm{Temp}} &= RC \\ t_{\mathrm{RH}} &= RC_{\mathrm{RH}}, \end{aligned} \tag{5.6}$$

By correlating the results from two modes, the temperature effect in the RH measurement is cancelled.

The 9-b VCO outputs are digitized by a TDC. By doing digitization continuously in the phase domain, the TDC achieves 1st-order noise shaping [105]. The TDC is clocked by an external frequency reference, f_s. Thus, the RH/Temp information (*i.e.* *R* and C_{RH}) are digitized with respect to *C* and f_s.

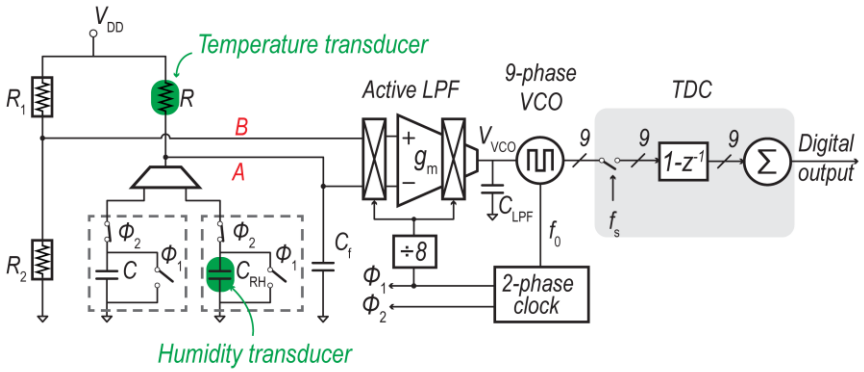


Figure 5.5. System schematic of the RH/Temp sensor using RCDC.

5.4.2 Dynamic Analysis

Since Despite the settling error described earlier, the finite loop gain of the FLL also affects the accuracy and linearity. Furthermore, the FLL dynamics require careful analysis to ensure stability over PVT variation. Thus, a small-signal model of the FLL needs to be derived.

Assuming C_f is large enough, the SC cell can be treated as a clock period-controlled resistor. Thus, the small-signal transfer function of the period-to-voltage conversion, $H_{WhB}(s)$, is derived by taking derivative of the large-signal relation within the SC-based WhB (assuming it is balanced):

$$H_{\mathrm{WhB}}(s) = \frac{\partial\left(\frac{V_{\mathrm{DD}}}{1+CR/t_0}\right)}{\partial t_0}\frac{1}{1+s\frac{RC_{\mathrm{f}}}{2}} = \frac{V_{\mathrm{DD}}}{4t_0}\frac{1}{1+s\frac{RC_{\mathrm{f}}}{2}}. \tag{5.7}$$

Eqn. (2.1) indicates that the balanced SC-based WhB has a dc gain of $K_{WhB}=V_{DD}/4t_0$ and a pole at $\omega_{WhB} = -2/RC_f$. Similarly, the R- and C-to-voltage transfer functions are

$$\begin{aligned} H_{\mathrm{WhB,R2V}}(s) &= Ct_0^2 H_{\mathrm{WhB}}(s), \\ H_{\mathrm{WhB,C2V}}(s) &= Rt_0^2 H_{\mathrm{WhB}}(s). \end{aligned} \tag{5.8}$$

The 1st-order active LPF can be modelled by

$$H_{\mathrm{LPF}}(s) = -\frac{A}{1+\frac{s}{\omega_{\mathrm{LPF}}}}, \tag{5.9}$$

where A and ω_{LPF} are the active LPF dc gain and pole, respectively. The VCO gain is K_{VCO}, defined in Hz/V. Since the oscillation period is taken as the VCO output, the small-signal VCO voltage to period gain is

$$H_{\mathrm{VCO}}(s) = -\frac{t_0}{f_0}K_{\mathrm{VCO}}, \tag{5.10}$$

Assuming the FLL is operating in the temperature mode (*i.e.* R is the input), its block diagram is obtained by substituting the transfer functions derived above [Figure 5.6(a)]. The loop gain is

$$L(s) = \frac{AK_{\mathrm{VCO}}V_{\mathrm{DD}}}{4f_0}\frac{1}{\left(1+\frac{s}{\omega_{\mathrm{LPF}}}\right)\left(1+\frac{s}{\omega_{\mathrm{WhB}}}\right)}, \tag{5.11}$$

This analysis shows that the FLL is a 2$^{\mathrm{rd}}$-order system. By choosing ω_{LPF} as the dominant pole, the active LPF requires lower bandwidth and thus has lower power consumption and lower integrated noise from the transducers and LPF, at the expense of higher area. Alternatively, pushing ω_{LPF} to the non-dominant pole allows higher FLL bandwidth and has smaller area, but requires higher power to extend the active LPF bandwidth and suffers from worse linearity due to higher ripple at V_{VCO}. Since this work is targeting IoT applications, the former is adopted. The gain error is inversely proportional to $L(s{=}0)$, thus higher supply voltage, LPF dc gain and VCO gain result in lower error. This justifies the design choice of using an active LPF with high dc gain and biasing the WhB directly from V_{DD} to maximize the loop gain.

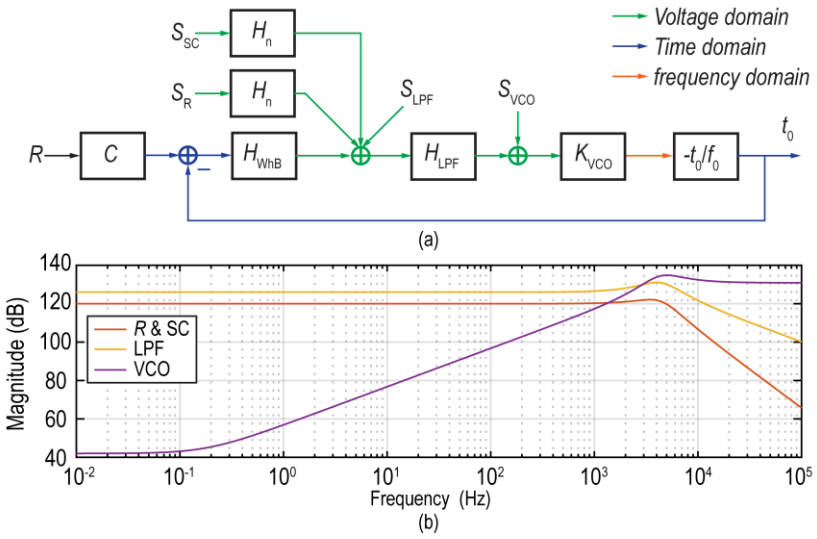


Figure 5.6. (a) FLL block diagram and (b) NTFs of different blocks.

5.4.3 Sensitivity Analysis

Aside from the SC settling and loop gain errors, the noise from each block affects the sensitivity and thus the inaccuracy. To quantify this, the signal transfer function (STF) and noise transfer function (NTF) from each block needs to be analyzed. As derived from the block diagram [Figure 5.6(a)], the STFs are

$$\begin{aligned} STF_{\text{Temp}} &= \alpha t_0 \frac{L(s)}{1+L(s)} \approx \alpha t_0, \\ STF_{\text{RH}} &= \beta t_0 \frac{L(s)}{1+L(s)} \approx \beta t_0, \end{aligned} \tag{5.12}$$

where α and β are the resistor's temperature coefficient (TC) and the capacitor's RH coefficient, respectively.

The noise from the R or SC can be modelled as a voltage noise source in series with a noiseless R or SC. When the WhB is balanced, the noise power spectra density (PSD) from R and SC are equal, $S_{\text{R,SC}} = 4k_{\text{B}}TR$ where k_{B} is Boltzmann's constant, and T is the absolute temperature.

Both noise sources pass through the same transfer function, $H_n(s)$, and sum at the WhB output where

$$H_n(s) = \frac{1}{2\left(1+\frac{s}{\omega_{WhB}}\right)}. \quad 5.13$$

The noise from the reference branch can be made negligible if the reference branch output's bandwidth is limited.

The input-referred active LPF and VCO noise PSDs are S_{LPF} and S_{VCO}, respectively. With that, the NTFs are derived as follows:

$$\begin{aligned} NTF_R = NTF_{SC} &= \frac{2t_0}{V_{DD}} \frac{L(S)}{1+L(s)}, \\ NTF_{LPF} &= \frac{H_{LPF}(s)K_{VCO}}{1+L(s)}, \\ NTF_{VCO} &= \frac{K_{VCO}}{1+L(s)}. \end{aligned} \quad 5.14$$

Bode plots of each NTF is shown in Figure 5.6(b). NTF_R and NTF_{SC} roll off at 40 dB/dec, while NTF_{LPF} rolls off by 20 dB/dec. The noise from the VCO is attenuated by the LPF gain within the open-loop bandwidth and increases by 20 dB/dec afterwards. It should be noted that all noise sources are uncorrelated.

If the noise from the WhB is dominant, by substituting the noise PSD from R and SC resistor in to (5.14), and then input-referring it with (5.12), the PSD (normalized to temperature input) can be obtained. Since the TDC output is decimated by a sinc filter of length T_{conv}, the rms temperature noise (*i.e.* the temperature sensitivity ΔT) is

$$\Delta T \approx \sqrt{2\frac{S_R}{2T_{conv}}\left|\frac{NTF_R}{STF}\right|^2} = \frac{4}{\alpha V_{DD}}\sqrt{\frac{k_B T R}{T_{conv}}}. \quad 5.15$$

Similarly, the RH sensitivity, ΔRH, is

$$\Delta RH \approx \frac{4}{\beta V_{\mathrm{DD}}} \sqrt{\frac{k_B T R}{T_{\mathrm{conv}}}}. \quad 5.16$$

Upon reaching steady-state, the WhB's power consumption is (neglecting the power consumption on the reference branch)

$$P_{\mathrm{WHB}} = \frac{V_{\mathrm{DD}}^2}{2R}. \quad 5.17$$

Substituting (5.15) and (5.17) into the temperature sensor FoM equation, the WhB front-end FoM is

$$\mathrm{FoM}_{\mathrm{WHB}} = \frac{8kT}{\alpha^2}, \quad 5.18$$

In practice, the LPF, VCO, and TDC also contribute noise that degrades the sensitivity while consuming a non-negligible power consumption. So, the sensitivity, power, and following FoM will be worse than above predictions. Nevertheless, a few observations can be made from the above analysis. Namely,

1) Both the sensitivity and FoM are inversely proportional to the transduction coefficient (*i.e.* TC and RH coefficient). Thus, the transducers should be carefully selected to maximize the performance.

2) Increasing the supply voltage linearly improves the sensitivity. The WhB power consumption is proportional to V_{DD}^2, while the power consumption of most other analog blocks (*e.g.*, the amplifier) with static current bias is proportional to V_{DD}. This suggests that even though the FoM of the WhB alone doesn't improve as V_{DD} increases, the overall FoM does when the power of the other analog blocks is considered.

3) Making the WhB full-differential doubles the signal and the sensitivity increases by 3 dB at the cost of doubling WhB power consumption. Although (5.18) doesn't improve, the 2×

signal swing reduces the NTFs allowing 4× lower power consumption from the LPF and VCO provided they are noise limited. The fully differential architecture also cancels switch imperfections. A pseudo-differential WhB is adopted in this design since matching two RH transducers is difficult. If designing a temperature only sensor, a fully-differential SC-WhB is preferred.

5.5 Circuit Implementation

5.5.1 SC Front-End

As shown in the previous analysis, a resistor with high α is preferred. Apart from that, other physical parameters that affect the resistor nonideality should be considered. For example, the 2nd-order TC, voltage dependence, and stress sensitivity affect the sensor nonlinearity, which cannot be corrected by a simple 1st-order trim. 1/*f* noise leads to excess noise and worse sensitivity compared to (5.15) and (5.16). The sheet resistance determines the required area. In this work, a silicided P-type polysilicon resistor is chosen due to its high α (~3,000 ppm/°C), high linearity, and low 1/*f* noise corner (<1 Hz).

The RH transducer is implemented with a metal finger capacitor coated with a PI film (PI-2545). The relative dielectric constant, $\varepsilon_{\mathrm{PI}}$, at ~35 %RH is 3.4. The transducer geometry, to the 1st-order, doesn't affect β, but affects the area, coating difficulty, and response time. For an N finger interdigitated capacitor with finger length L, gap width W, and metal thickness H, the total capacitance can be modeled as

$$C = \varepsilon_{\mathrm{PI}}\varepsilon_0(N-1)\frac{LH}{W}, \tag{5.19}$$

where ε_0 is the vacuum permittivity. To minimize the area, H should be maximized, while W should be minimized. Thus, the geometry parameters are chosen as following: N = 80, H = 40 μm, L = 220 μm, W = 2.5 μm. This geometry results in a capacitance of ~4 pF. The top-metal capacitor is designed to have an opening without passivation to allow for post-processing. The transducer is shielded by overlaying metal layers beneath it. This protects the CMOS die from over etching and reduces the parasitic capacitance associated with the top plate, which connects to the switches. As for the reference capacitor, a MIM capacitor with ~10 ppm/˚C is used. Both MIM capacitor and silicided polysilicon resistor are not exposed to the air in the standard CMOS process, thus showing no humidity dependency.

The reference branch is implemented by 4 diode-connected PMOS transistors in series. The static current is only ~50 nA at room temperature. The transistors are laid in a common-centroid way and have the bulk tied to the source to mitigate mismatch and body effect. It should be noted, even if there is mismatch between the transistors as long as the mismatch is constant over temperature (*i.e.* R_1/R_2 is constant), it only shows up as a gain error, which can be easily removed by a 1st-order trim. A 20 pF MOS capacitor decouples to reference output to limit its noise bandwidth to <10 Hz.

The switches in the multiplexer require extra attention. While the switch should have low on-resistance to not affect the accuracy of R; it should also have good isolation between the two SC cells. To achieve this, the multiplexer switches are implemented with NMOS low-leakage switches (*i.e.* using a unity-gain buffer to drive the intermedia node of two series switches and the body of the switch when the switch is off [106]). The unity-gain buffer doesn't require high bandwidth to cover f_0, since the ripple at f_0 is <5 mV. The residual leakage is negligible, even if there is 5 mV residue offset due to the low bandwidth. The two switches in the multiplexer share

one unity-gain buffer in a time-multiplexed fashion to further minimize the power consumption. Additionally, the SC cell is designed to stay in Φ1 when it is not selected (Figure 5.7), such that the un-selected capacitor (either MIM or PI-film) is shorted to ground to further reduce the crosstalk. In simulation, the crosstalk is negligible (< 5 ppm error when the unselected capacitor changes by 20%).

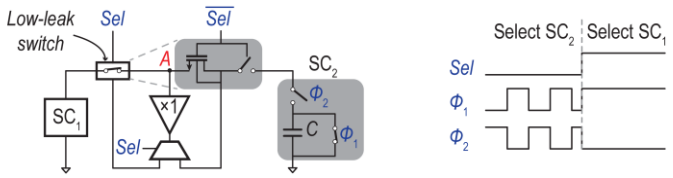


Figure 5.7. Schematic and timing of the high isolation multiplexer scheme.

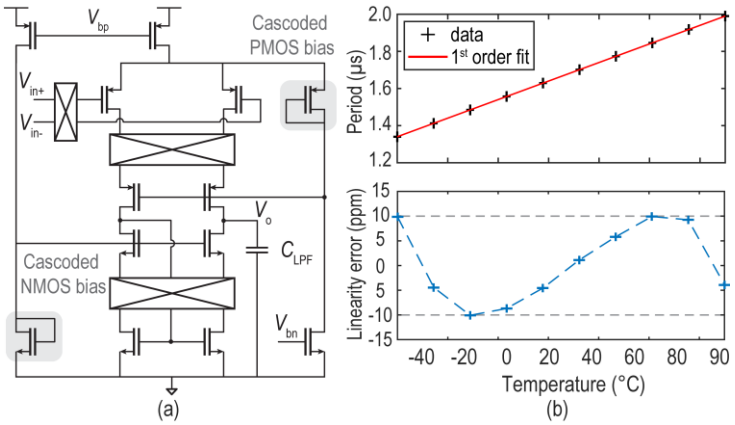


Figure 5.8. (a) Schematic of the active filter (b) simulated FLL transfer curve and linearity error.

5.5.2 Chopper-Stabilized Active Filter

As analyzed in Section 5.4, the active LPF needs to have high enough dc gain to achieve high system linearity and low gain error, and low ω_{LPF} to maintain the FLL stability. Compared to prior work with phase-domain SDM readout, the active LPF has low voltage swing at both the input and output, which relaxes the linearity requirement. Thus, instead of using a closed-loop filter, an open-loop g_m-C architecture is used.

The minimum dc gain requirement can be obtained from (5.11) where assuming the system undergoes 30% supply variation (a typical value for a battery), and the normalized VCO gain (K_{VCO}/f_0) varies between 3~5, the dc gain should be >79 dB to achieve <±10 ppm nonlinearity error. Thus, a telescopic architecture is adopted in the g_m cell [Figure 5.8(a)]. Compared to a two-stage or folded-cascode architecture, it has better noise efficiency. The input pair is implemented with PMOS transistors for two reasons: 1) PMOS transistors have a lower 1/*f* noise corner in this process and 2) PMOS transistors have 100 mV higher threshold voltage than the NMOS such that the input pair is always in subthreshold, which has the optimal noise efficiency, across PVT variation. By choosing a 1.5 V minimum supply voltage, the PMOS input pair is biased in subthreshold saturation while the NMOS load is biased in above-threshold saturation with high overdrive voltage, such that the transistors thermal noise is attenuated. This also gives ~0.4 V minimum output voltage swing, which covers the expected VCO tuning range and the VCO nominal frequency drift due to PVT variation. The dc gain is nominally 84 dB and <79 dB across PVT variation. With such high gain, the FLL transfer curve is simulated with transistor-level circuits and ideal resistors at 1.5 V supply, and the nonlinearity error is <±10 ppm from -40℃ to 85℃ [Figure 5.8(b)]. C_{LPF} is designed to be 3.5 nF to maintain FLL stability and attenuate the switching ripple to ~20 μV. It is implemented with stacked MOS capacitors, MIM capacitors and costumed metal-oxide-metal capacitors (metal-2 to metal-5) to maximize the unit capacitance to ~12 fF•μm^2. A 6 nF capacitor bank is implemented on chip, and only 3.5 nF is connected during the measurement, which occupies 0.29 mm^2 area.

The g_m cell is chopped to remove its 1/*f* noise and offset, which is temperature-dependent and introduces nonlinearity. The up-modulation chopper is placed at the input, and the down-modulation choppers are placed at the cascode nodes, which have ~100× lower impedance and

higher bandwidth than the output nodes. Thus, the down-modulated signal settles faster and creates less settling error. The up-modulated 1/*f* noise and offset are filtered by C_{LPF}. The chopper clock is the FLL output divided down by 8. By setting the chopping clock synchronized to the SC clock and therefore the signal, the spurious tones due to the intermodulation between chopping and SC operation are avoided. The divider ratio is chosen to be 8 such that the nominal chopper frequency (94 kHz) is slightly higher than the simulated g_m cell 1/*f* noise corner frequency (~60 kHz). The clock division down also relaxes the g_m cell bandwidth requirement accordingly, which enables an 8× power savings. As shown in Figure 5.9, the chopper reduces the integrated noise by 26 dB. The simulated noise PSD is 0.3 nV/$\sqrt{\text{Hz}}$, corresponding to 0.19 mK/$\sqrt{\text{Hz}}$, 5 dB lower than the WhB noise PSD. The noise-efficiency factor is 2.4 with a 4 µA bias current, only slightly higher than the theoretical limit for a common-source differential amplifier [107].

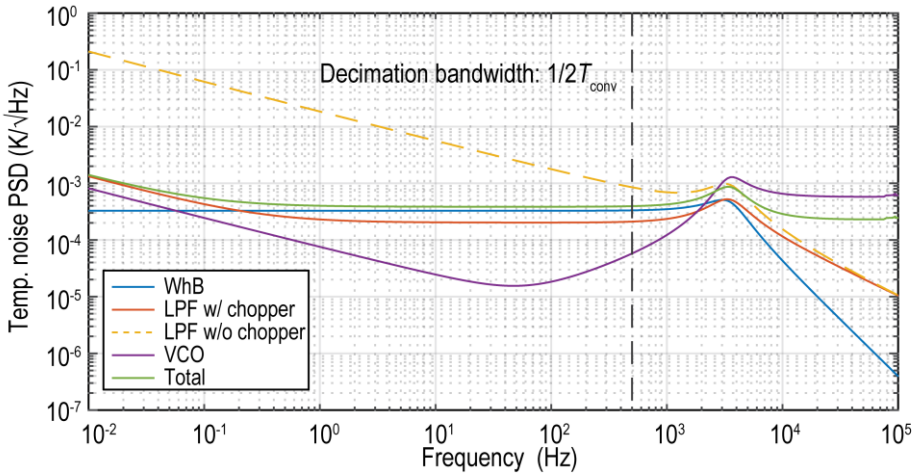


Figure 5.9. Simulated FLL noise PSD referred to the temperature input.

5.5.3 VCO & TDC

As illustrated in Figure 5.10(a), the VCO is implemented with a 9-stage g_m-current-controlled oscillator (g_m-CCO) architecture for good linearity [108]. The g_m of the VCO is

implemented with an NMOS transistor. Since the LPF uses PMOS input pair and tail current source, its output, V_{VCO}, is insensitive to the supply variation. Thus, compared to a VCO with PMOS-g_m, the V_{GS} of the NMOS transistor is also insensitive to the supply variation. Simulation shows >30 dB better supply-rejection comparing to a VCO with a PMOS-g_m. The delay cell is designed to be differential rather than single-end for better supply-rejection and symmetric slewing. A cross-coupled pair is added at each delay cell output to sharpen the transition edge, which improves the VCO 1/*f* noise performance and mitigates the following D-flip-flop metastability (in the TDC) [Figure 5.10(b)].

Since the VCO noise is shaped by the active LPF, the VCO has relaxed thermal noise requirement and is designed for low power consumption (1.2 μW nominally). However, the VCO 1/*f* noise cannot be overlooked. The NMOS g_m cell is sized large (W/L = 80/60) to attenuate the g_m cell 1/*f* noise, and the stage number is set to be 9 to attenuate the delay cell 1/*f* noise. As shown in Figure 5.9, the VCO noise is mostly 1/*f* noise with a -10 dB/dec slope. Since it is attenuated by the loop gain, it contributes least to the overall FLL noise.

The VCO delay cell output phase is sampled and sliced by a D flip-flop. The $1\text{-}z^{-1}$ operation is realized by feeding the sampled phase with respect to a delayed version of it into an XOR gate. The 1st D-flip-flop is implemented with a double-tail cross-coupled latch [Figure 5.10(c)] since the VCO doesn't have rail-to-rail swing, while the 2nd D-flip-flop is implemented with static logic. All 9 XOR gate outputs sum together and generate a 4-bit output, which represents the total transition phases during one sampling period. To avoid missing a transition phase, the sampling frequency, f_s, should be at least twice as f_0. Thus, f_s is chosen to be 2 MHz. The overall system is designed to be thermal noise limited, instead of TDC quantization noise. According to [96], the signal-to-

quantization noise ratio (SQNR) is calculated to be 116 dB, and the quantization noise to be 0.46 mK (referred to temperature), lower than the input-referred thermal noise of the FLL.

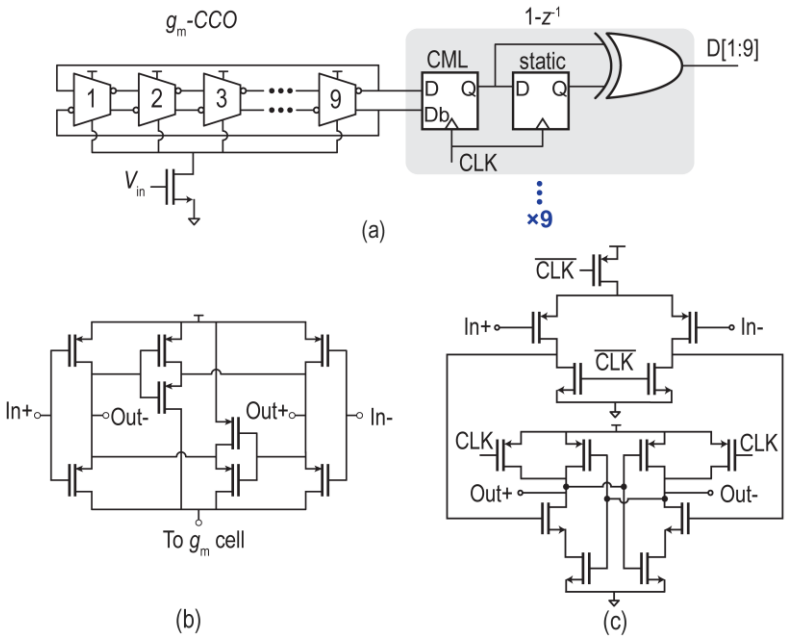


Figure 5.10. Schematic of (a) the VCO and TDC, (b) delay cell, and (c) double-tail latch.

5.6 Measurement

The RH/Temp sensor was fabricated in a standard 180 nm CMOS process [Figure 5.11(a)] and mounted on a FR4 printed circuit board (PCB) directly. The sensor occupies 0.72 mm^2 area, among which the transducers take 0.21 mm^2, and the LPF takes 0.29 mm^2. The decimation filter, a 13b counter, was implemented in a FPGA for versatility. It would consume 0.4 μW power and 0.002 mm^2 if implemented in the same technology.

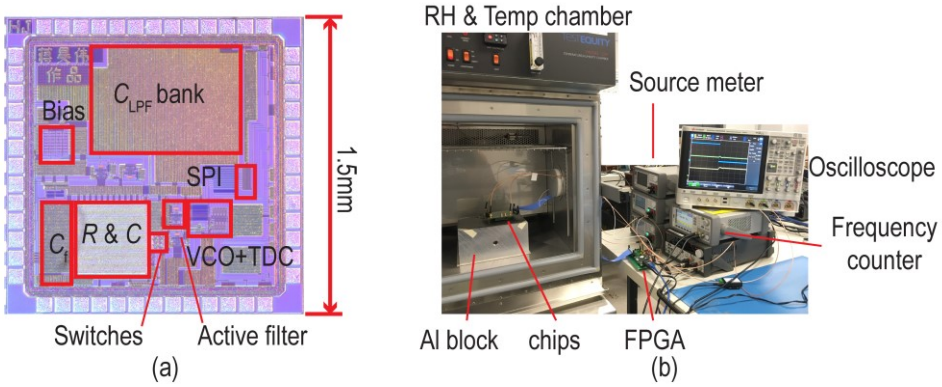


Figure 5.11. Photograph of (a) annotated die and (b) measurement setup.

5.6.1 PI-Coating & Measurement Setup

The chips were wirebonded on PCBs and encapsulated with epoxy, which had an opening above the RH transducer. PI-2545 was drop-casted and spin-coated on the sensors at 2000 rpm for 60 sec. The spin-coating process prevented the PI layer from being too thick, which would slow down the response time. The chips were then cured at 250℃ for 5 hours. Note, all post-process procedures could be done more easily on the entire wafer rather than on a single chip in large-volume production.

The measurement setup is shown in Figure 5.11(b). An environmental chamber (TEQ-123H) was used for RH/Temp control. To filter out the background temperature noise generated by the chamber, the sensors were mounted on a10 kg aluminum block via a thermal conductive pad. The FPGA and other off-the-shelf testing circuits were placed outside the chamber since they cannot tolerate the large RH/Temp range.

5.6.2 Measurement Results

The circuit consumed 15.6 µW from a 1.5 V supply at room temperature, where the analog block (active filter and the bias circuits) consumed 7.9 µW, the SC-WhB 3.4 µW, and digital block (VCO/TDC) 4.2 µW. The power breakdown over temperature is shown in Figure 5.12(a) where the digital power slightly decreased at higher temperature since the FLL output frequency is CTAT; while the analog block power increases with temperature due to the PTAT constant-g_m current reference. The mode switching feature is verified in Figure 5.12(b). Since C_f holds the charge such that V_A doesn't drop during the mode switching, the FLL re-settles quickly, in just 0.6 ms.

The FLL period jitter, the deviation between each period time from the nominal period time, was measured with a frequency counter (Keysight 53230A). Since oversampling would be applied to the FLL, the period jitter after averaging is of-interest. For example, when the nominal frequency is at 741 kHz, 741 periods in row were averaged into one sample to obtain 1 ms averaging. The histogram shows a standard deviation of 8 ps, corresponding to 5.9 ppm, with 1 ms averaging applied to 10^6 period samples [Figure 5.13(a)]. The period jitter is plotted vs. the averaging time in Figure 5.13(b). From 0.1 ms to 10 ms (2 decades), the jitter reduced by 10× since the design is white noise limited. The maximum averaging time was limited by the equipment's memory depth.

The TDC was characterized by fixing the temperature and humidity, thus the FLL generated a fixed output frequency, which served as a dc input for the TDC. The TDC output bitstream PSD was estimated by doing 2^{17}-point fast-Fourier-transform (FFT) and 10× averaging [Figure 5.14(a)]. Since the FLL noise dominates at the low frequency, the FLL bandwidth could

be directly observed from the PSD to be ~2 kHz, slightly lower than simulation, likely due to process variation. The system resolution was characterized by measuring the output noise at room temperature, then normalized to both temperature and RH inputs [Figure 5.14(b)]. 104 dB SNR, or 6 ppm resolution, was achieved with a 1 ms conversion time. This was slightly larger than the FLL jitter with the same averaging time, which verified that the excess noise added by the TDC was much lower than the FLL. By referring to the temperature and RH inputs with α and β, 2 mK and 0.0073 %RH resolution was obtained, respectively. The resolution improved by 10× when T_{conv} increases by 100×, since the thermal noise was dominating, until environmental drift worsened it after ~0.3 s.

The time-domain responses are plotted against commercial probes in Figure 5.15. The temperature mode responded faster than the commercial probe, probably because the commercial Pt-100 probe had better contact with the aluminum block, thus a stronger filtering effect. Each temperature step took about 14 ks to settle, which ensured the measurement accuracy. It can also be observed that this work showed better noise performance than the commercial probe with 10 mK resolution. While in the RH mode, this work showed nearly the same step response as the commercial sensor, which validated the proposed post-processing method. This work showed the same fluctuation as the commercial one since the environmental chamber dominated the background RH noise to be 0.5 %RH.

The transfer curves in both modes were measured on multiple chips (n=10) as shown in Figure 5.16(a,c). The temperature transfer curve showed an average α of 2984 ppm/K and a 6.5% spread on the nominal period. The RH transfer curve showed an average β of 860 ppm/%RH and a 19% spread, larger than the temperature mode due to the additional post-processing. The sensors were calibrated against high accuracy commercial probes: ±0.05℃ inaccuracy Pt-100 sensor and

2 %RH inaccuracy capacitive polymer sensor. After a 1st-order calibration, the remaining errors are shown in Figure 5.16(b,d): the 3σ error is 0.55℃ over the -40 to 85℃ range (industrial standard), and 2.2 %RH over 10 to 95 %RH (limited by equipment). Varying the supply from 1.5 to 2 V at room temperature, the sensor output changes by 0.018%, corresponding a 0.12 °C/V or 0.43 %RH/V supply sensitivity.

To compare the performance of the 2-in-1 RH/Temp sensor with prior temperature sensors, and RH sensors, a slightly modified temperature sensor resolution FoM is used to make a fair comparison regardless of the transducer type. Instead of referring the resolution to absolute temperature, resolution referred to the baseline signal (*i.e.* 1/SNR) is used in the FoM definition

$$\mathrm{FoM_{sen}} = \frac{Power \cdot T_{\mathrm{conv}}}{SNR} = \mathrm{FoM_{Temp}}\alpha^2, \tag{5.20}$$

whose unit is J•ppm^2. It should be noted that this can also be obtained by removing the transducer parameter (*i.e.* α), from the existing temperature sensor FoM, $\mathrm{FoM_{Temp}}$. For completeness, the FoMs referring to both K and %RH are also reported (Table 5.1). This work demonstrated state-of-the-art FoM compared to the prior RH sensor and compound sensor and comparable (19% worse) FoM compared to the state-of-the-art temperature only sensor. It should be noted, this architecture would show better efficiency by designing the WhB to be fully-differential, which relaxes the readout circuit noise requirement. This work also tolerates the widest supply range without an additional regulator. Compared to prior compound sensors, this work occupies the smallest die area.

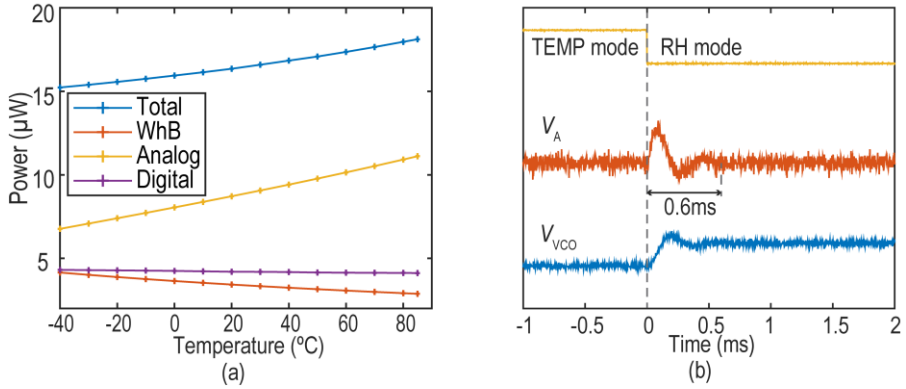


Figure 5.12. Measured (a) power vs. temperature, and (b) waveforms during mode switching.

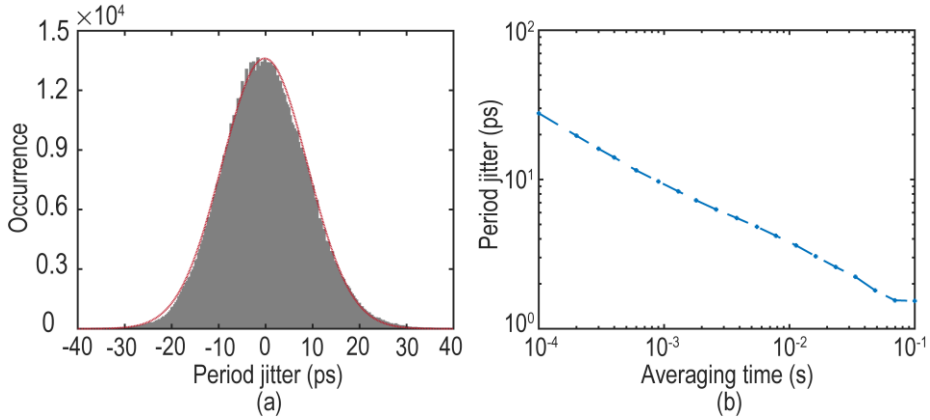


Figure 5.13. Measured (a) FLL jitter histogram with 1 ms averaging, and (b) jitter vs. averaging time.

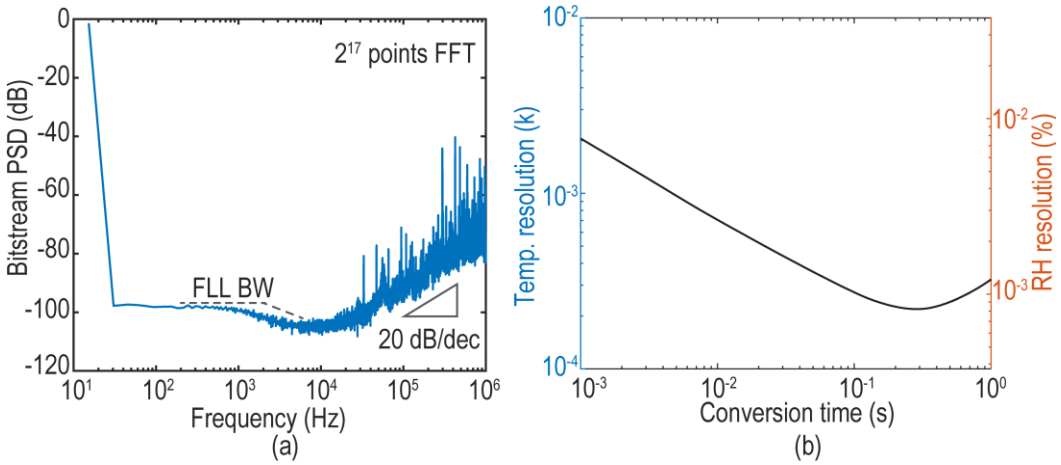


Figure 5.14. Measured (a) resolutions vs. T_{conv}, and (b) TDC PSD.

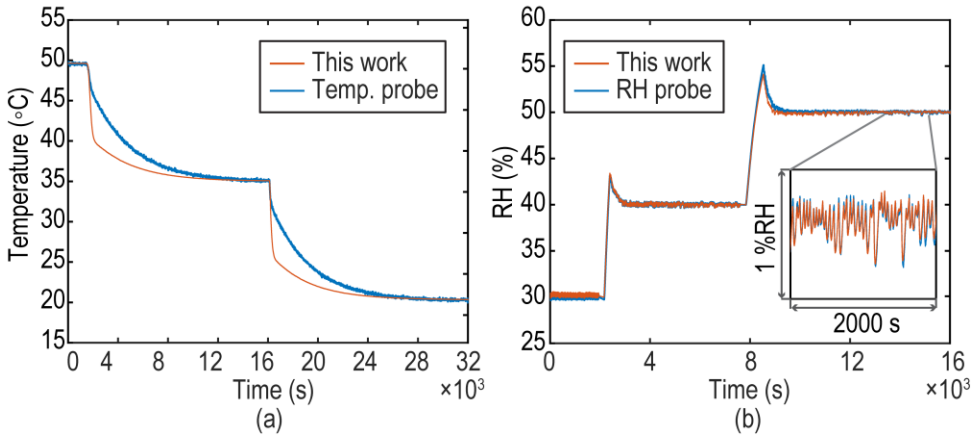


Figure 5.15. Measured step response when (a) temp. changed and (b) RH changed.

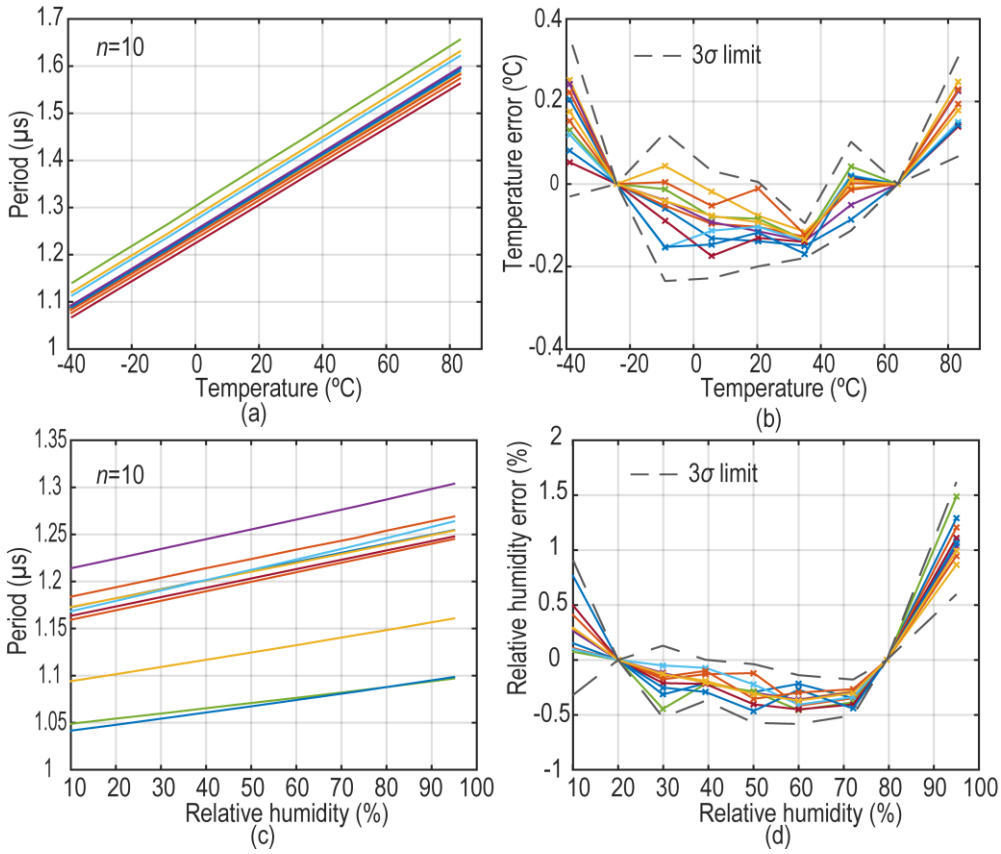


Figure 5.16. Measured (a) temperature transfer curve, (b) temperature error, (c) RH transfer curve, and (d) RH error.

5.7 Conclusion

This chapter presents a fully integrated temperature and humidity sensor consisting of a unified *R&C*-to-*T* converter. Using a FLL with an incomplete-settling, SC-based WhB and a TDC, it avoids high power consumption needed to actively drive the SC compared to prior art and maintains <10 ppm tolerance. Combined with a chopper-stabilized LPF, this system achieves a state-of-the-art RH FoM without degrading the temperature FoM and has low energy (15.6 nJ/meas.) suitable for IoT applications.

Chapter 5, in part, contains materials from Haowei Jiang, Chih-Cheng Huang, Matthew Chan and Drew A. Hall, "A 2-in-1 Temperature and Humidity Sensor Achieving 62 fJ·K^2 and 0.83 pJ·(%RH)^2," in *IEEE Custom Integrated Circuits Conference*, Austin, TX, USA, 2019, and its journal version that has been submitted for publication. The dissertation author was the primary investigator and author of these papers.

Table 5.1. Performance comparison of environmental sensors

	Parameter	Park	Pan	Pan	Choi	Angevare	Mordakhay	Tan	Cirmirakis	Park	Yang	Maruyama	This Work
System	Tech. (nm)	180	180	180	65	180	65	160	600	180	350	180	**180**
	Sensor type	Temp	Temp	Temp	Temp	Temp	Temp	RH	RH	RH/pres./acc	*C*	RH & Temp	**RH & Temp**
	FE type	*RC*	*RC*	*R*	*RC*	*RC*	*RC*	*RC*	*C*	*C*	*RC*	*C*	***RC***
	Active area (mm^2)	0.09	0.72	0.25	0.007	0.007	0.01	0.28	2	1.28	0.35	4.5	**0.72**
	Supply (V)	1.7/1	1.6~2	1.6~2	0.85~1.05	1.8	1.2	1.2	5	1.1	3.3	1.55	**1.5~2**
	Conversion time (ms)	32	10	5	1	0.333	0.08	0.8	NA	0.85	10.5	20	**1**
	Power (μW)	31	180	94	68	1600	12.8	10.3	890	2.96	759	3875	**15.6**
	FOM_{sen} (μJ·ppm^2)	14.7	0.46	0.66	2.08	71000	45.1	1319	NA	21.4	55.1	258	**0.55**
Temp.	Temp. range (°C)	-40~85	-40~85	-55~125	-40~85	-35~125	-40~110	25 only	27~35	40 only	20~70	-20~85	**-40~85**
	3σ error (K) [trim points]	0.12 [3]	0.1[2] [2]	0.12[2] [2]	0.7[2] [2]	0.35[2] [2]	1.4 [2]	-	-	-	-	0.6 [NA]	**0.55 [2]**
	α (ppm/°C)	1356[2]	3000[2]	4400	2200	3000[2]	1465	-	-	-	-	NA	**2984**
	Resolution (mK)	2.8	0.16	0.26	2.5	120	150	-	-	-	-	15	**2**
	FOM_{Temp} (fJ·K^2)	8,000	49	32	430	7.6E6	2.1E4	-	-	-	-	-	**62**
RH	RH range (%)	-	-	-	-			30~95	15~85	30~90	-	0~100	**10~95**
	3σ error (%) [trim points]	-	-	-	-			1.6[4] [2]	NA	3.3[4] [2]	-	4 [NA]	**2.2 [2]**
	β (ppm/%RH)							1750	730	1842	-	316[6]	**860**
	Resolution (%RH)	-	-	-	-			0.05	NA	0.04	2.63[5]	0.0057	**0.0073**
	FOM[1](pJ·%RH^2)	-	-	-	-			20.7	NA	6.3	-	2518	**0.83**

[1] Energy / conversion × (RH resol.)^2 [2] Used high order nonlinearity correction [3] Read from measurement plots
[4] Peak-to-peak error [5] Relative resolution (ppm), calculated from ENOB [6] Calculated from Table III

Chapter 6

Summary

6.1 Summary of Dissertation

This dissertation describes the breakthroughs made to the receivers and sensors that integrate wireless connections into everything by achieving nano-watt power consumption and millimeter area occupation. The following is a summary of the key points and results presented in the dissertation.

Chapter 2 describes a 0.4 V 113.5 MHz OOK-modulated WuRX that achieves -69 dBm sensitivity consuming only 4.5 nW in a 0.18 μm SOI CMOS process. The WuRx was designed for emerging event-driven low-average-throughput applications to reduce system power. While conventional direct envelope detection architectures can achieve low power at moderate sensitivities, this design breaks the conventional trade-off to achieve ultra-low power with high sensitivity by: 1) reducing the baseband signal bandwidth to 300 Hz; 2) modulating OOK signal

with a custom designed 16-bit code sequence to get 4 dB coding gain; 3) employing an off-chip high-Q transformer/filter with 25 dB passive voltage gain enabled by an ED with high input impedance; 4) achieving higher conversion gain using an active-L biased ED; 5) digitizing the ED output via a regenerative comparator with kickback elimination; 6) decoding the received OOK signal using a high-Vt subthreshold digital baseband correlator, operating with 2× oversampling to overcome phase asynchronization, where the clock is generated by a 1.1 nW relaxation oscillator. This work was published in IEEE International Solid-State Circuits Conference and IEEE Journal of Solid-State Circuits.

Chapter 3 presents an improved WuRX with significant innovations on the sensitivity, compactness, and robustness. A 7.3 nW power, 9 GHz WuRX was designed for area-constrained, ultra-low power applications. The passive pseudo-balun ED architecture eliminates the $1/f$ noise and improves the sensitivity greatly. By adaptively biasing the ED with a CMFB loop around the baseband amplifier, and autozeroing the baseband amplifier offset, the ac-coupling capacitors were removed. These techniques avoid any off-chip baseband components while achieving narrow baseband bandwidth to minimize noise. Due to the high ED input impedance, this work achieves a state-of-the-art FOM compared to high frequency (>1 GHz) WuRXs. This work was published in IEEE Solid-State Circuits Letter and IEEE Journal of Solid-State Circuits.

Chapter 4 presents the design techniques towards the WuRXs temperature compensation, which has been overlooked in prior work and for the first time being introduced. The specifications and behaviors of every block across the temperature is carefully examined. The ED and BB amplifier are compensated in an analog with temperature stabilized bias generation. The comparator could be compensated digitally for the best robustness. Regarding the local timer, the comparator delay and temperature dependence of a relaxation oscillator based on a ramp response

model was analyzed. A two-stage τ_{SW}-cancelling comparator and a technique that utilizes the linear temperature-dependent delay were proposed to implement a relaxation oscillator for low power and low voltage applications. Measurement results validate the proposed technique and demonstrate state-of-the-art performance. This work was published in IEEE Journal of Solid-State Circuits.

The following chapter, Chapter 5, presents the development of a fully integrated temperature and humidity sensor consisting of a unified *R*&*C*-to-*T* converter. Using a FLL with an incomplete-settling, SC-based WhB and a TDC, it avoids high power consumption needed to actively drive the SC compared to prior art and maintains <10 ppm tolerance. Combined with a chopper-stabilized LPF, this system achieves a state-of-the-art RH FoM without degrading the temperature FoM and has low energy (15.6 nJ/meas.) suitable for IoT applications.

6.2 Areas for Future Work

Both WuRX project and environmental sensor project presented in this dissertation can be further expanded upon in a few ways.

Regarding the WuRX, it can be improved in the following directions: 1) designed to be standard (*e.g.*, WiFi, Bluetooth Low Energy, or NB-ToT) compliant, such that it could be merged seamlessly into the existing wireless networks at the lowest cost. 2) Better sensitivity could be achieved with duty-cycled active amplification at RF or higher-*Q* transformer filter implemented by microelectromechanical systems (MEMS) device. 3) Exploiting multibit ADC, higher oversampling ratio, and stronger digital matched filter could potentially improves the PVT robustness and interferer rejection.

While better power efficiency and smaller area is achievable in the environmental sensor by utilizing the following approaches: 1) implementing the FLL in a mostly digital way, which dramatically reduces area and power. 2) Further saving area and power with more sophisticated digital calibration (*e.g.*, higher order polynomial fit) that relaxes the linearity requirement of the analog design. 3) The same architecture could be used in other sensing applications, such as displacement or acceleration sensors (capacitive mode), biosensors (resistive mode), and even expanded for large-array usage.

Finally, methods to improve the overall IoT node system should also be studied. For example, a methodology to integrate more sensor front-ends into one efficiently, or a protocol for lower energy and lower latency data transmissions. A possible work-around would be to combine my work with low power data-driven transmitter [14] and use that to demonstrate the effectiveness of implementing the next-generation IoT network.

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