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Switching Schemes for Hybrid Switched-Capacitor DC-DC Power Converters

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Switching Schemes for Hybrid Switched-Capacitor DC-DC Power Converters

By

Margaret Elizabeth Blackwell

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requirements for the degree of

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Associate Professor Robert C. N. Pilawa-Podgurski, Chair
Assistant Professor Jessica Boles
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Switching Schemes for Hybrid Switched-Capacitor DC-DC Power Converters

Abstract

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by

Margaret Elizabeth Blackwell

Doctor of Philosophy in Engineering – Electrical Engineering and Computer Sciences

University of California, Berkeley

Associate Professor Robert C. N. Pilawa-Podgurski, Chair

Power converter topologies are continually evolving and improving especially as new applications such as space exploration mature, and new power architectures emerge. One such evolutionary branch of power converters is hybrid switched-capacitor (SC) converters which leverage capacitors as highly energy-dense components, high figure-of-merit switching devices, and small magnetics to realize high-performance power electronics. To fully exploit the benefits of this relatively new class of power converters requires investigation into control schemes. Whether using conventional switching control strategies or developing novel arrangements, this work explores the theoretical and practical intricacies of applying various switching schemes to hybrid SC converters.

Due to the reliance on capacitors for energy processing, SC converters typically suffer from charge-sharing losses when capacitors are charged/discharged into other capacitors or sources. However, adding a small inductance to the circuit and incorporating clever switching patterns can reduce or eliminate these losses. Furthermore, with an increase in the number of switching devices over traditional converters, losses associated with those switches may also increase. This work examines soft-switching techniques and how application to hybrid SC converters differs from previous works.

Finally, a hybrid SC converter is designed and tested for low-voltage automotive powertrain applications. In an industry that has strict regulations, this work seeks to demonstrate these new topologies can meet the required specifications and can do so with high performance as well. Switching techniques for mitigation of electromagnetic interference are evaluated against regulated limits and against efficiency performance.

Theory, analysis, and experimental results are expounded upon for several switching control strategies of hybrid SC converters addressing challenges of high-efficiency, low-noise, and high-density for applications to data center power delivery, space technology, and automotive powertrains.

To Devin

for your incessant love and support

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Chapter 1

Introduction

1.1 Introduction

With the diversification of the power grid, including new forms of energy production (e.g., renewable energy sources) and advanced loads (e.g., electric vehicles and power-demanding data centers), advancements in power electronics are urgent. Estimates show that by 2030, almost 80% of electricity could flow through power electronics [3], either on the side of power generation or consumption. Data centers used almost 2% of all electricity in the United States in 2014 [4] and the demand is continually increasing with further developments in machine learning, data processing, and digital commerce/communication, especially as teleconferencing fully integrated into the workday. Moreover, aviation accounted for almost 2% of *global* emissions [5] and is expected to triple by 2050 [6]. With increased adoption of hybrid electric aircraft and electric drivetrain, forecasts expect that electricity will account for almost 45% of total transportation consumption in 2050 [5]. In additional to transportation within our atmosphere, space operations – lunar micro-grids, extraterrestrial robotics, and satellites – have also been expanding.

The feasibility of the transition to more electric transportation and of keeping up with the demand for data centers and space exploration requires small (volume or mass), reliable, and efficient power converters. One potential solution to these challenges is to utilize new circuit topologies that can allow for reduced component sizing and reduced specific component losses, such as those associated with magnetic components or switching devices. However, conventional switching strategies may not apply to these new circuit topologies or new switching schemes may need to be implemented to achieve further performance benefits over conventional solutions.

Recently hybrid switched-capacitor (hybrid SC) converters have demonstrated improvements over more conventional topologies due to their use of capacitors as the primary energy transfer elements [7–12]. Hybrid SC converters leverage the superior energy density of capacitors over magnetics [13] to achieve the high power density and efficiency needed in applications such as data center power delivery [14–18] and electric transportation [19–23].

Moreover, to mitigate the hard-charging capacitor losses present in pure switched capacitor (SC) converters, some small inductance is introduced to enable soft-charging of the flying capacitors [24, 25].

Due to their multi-level nature, hybrid SC converters can have lower switch blocking voltages and lower dv/dt at the switch nodes, allowing for the use of lower-voltage-rated, higher figure-of-merit (FOM) switches and smaller magnetic components [25]. However, though these topologies can use lower-voltage-rated switches, they often have a larger number of switching elements and, therefore, more switching instances, which may be hard-switched transitions, emphasizing the need for soft-switching techniques. Moreover, for harsh environments such as automotive or space applications, not only are component rating more constrictive, but additional converter characteristics – such as electromagnetic interference – are regulated, potentially requiring additional components or new switching schemes.

1.2 Organization of Thesis

This thesis explores the implementation of varied control techniques in three domains (Fig. 1.1):

- Line cycle (ms scale)
- Switching period (μs scale)
- Sub-switching period (ns scale)

Heavy emphasis is placed on analytically describing circuit operation at sub-switching periods, specifically for split-phase and zero-voltage switching.

The remainder of this thesis is organized as follows:

Chapter 2 discusses the history and circuit topology evolution of a specific family of (hybrid) switched-capacitor (SC) converters — Dickson-based converters. The merits of Dickson-based power converters as a test-bed for exploring various switching schemes are discussed. Among resonant SC converters, the Dickson converter has some of the lowest switch stress making it a good choice for applications which require more stringent component ratings and for applications that require more complicated switching strategies that might impose additional stress on the switching devices.

To understand the various switching strategies which can further improve the performance of hybrid SC converters, first an analytical framework is presented in Chapter 3. A general method for analyzing ReSC converters based on peak energy requirements serves as a basis for investigating strategies to overcome challenges presented by hybrid SC topologies as well as to demonstrate hybrid SC converters for use in specialized applications. These switching and modulation tactics are discussed in detail in the following chapters.

The use of capacitors as primary energy storage elements in power converters does not come without additional challenges, one of which being capacitor charge-sharing losses. Using switches to connect/disconnect capacitors in various configurations can incur additional losses and generate EMI if there are large capacitor voltage differentials. Chapter 4 discusses

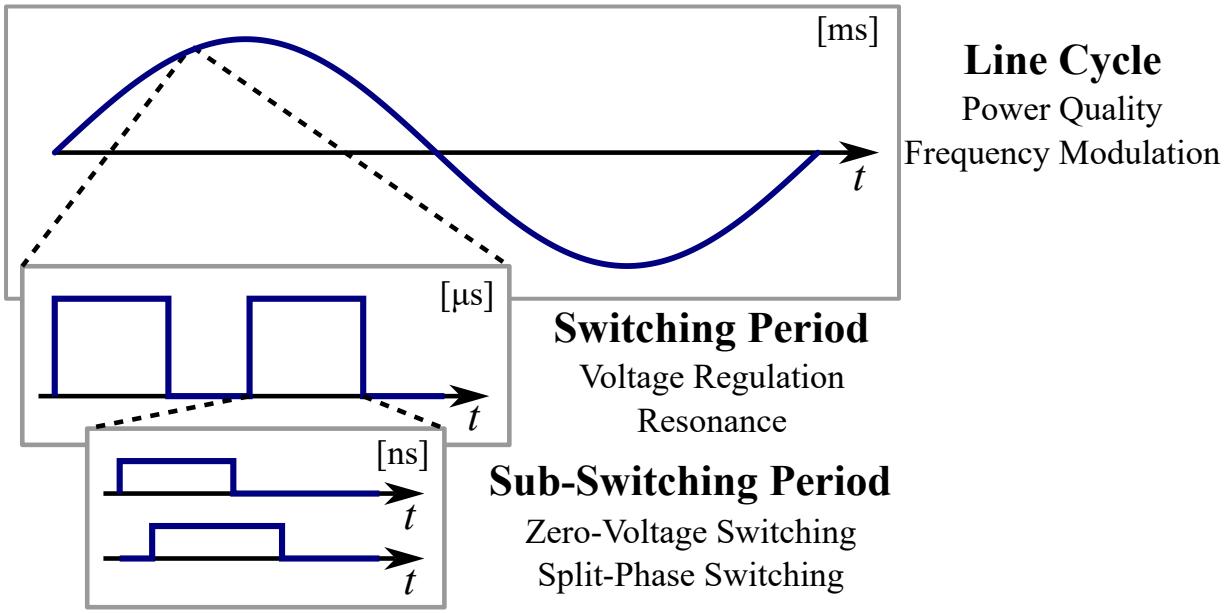


Figure 1.1: Control domains discussed in this thesis.

the theory behind a technique called split-phase switching in which additional switching states are introduced within a switching period to ensure that there are no voltage 'jumps' across any capacitors. Inserting these phases effectively, however, requires inspection of circuit operation and of timing analysis. Moreover, this timing analysis becomes more complicated when additional features are desired in the power converter, such as soft-switching, above-resonant operation, or frequency modulation.

Not only do some hybrid SC converters benefit from implementing split-phase switching, but additionally, techniques such as soft-switching can also improve performance by reducing losses associated with switching devices. Re-configuring a network of capacitors often requires many switching devices. While those devices may be exposed to lower voltage and current stress, they also require more switching transitions than conventional topologies. The nuances that make achieving a specific method of soft-switching — zero-voltage switching (ZVS) — more complicated for hybrid SC converters than conventional topologies are explained in Chapter 5. Additionally, experimental results of a hybrid Dickson converter achieving ZVS on every switch are shown, highlighting the efficiency benefits and validating the presented theoretical work.

Though hybrid SC converters are relatively new in terms of widespread industry/commercial adoption, there have been many demonstrations and validation of the feasibility for their use in data center applications, as one of the highest energy-consuming industries. However, other applications (e.g., automotive or space) which could benefit from the unique characteristics of hybrid SC converters have not yet caught up to data center power delivery, in part due to more constrictive design and testing requirements. Chapter 6 presents theoretical and experimental results of a hybrid SC converter, also a Dickson-derivative topology, designed

specifically for low-voltage automotive powertrain applications requiring voltage regulation. This chapter highlights the inherent benefits hybrid SC converters have for automotive environments, but also investigates areas which have yet to be answered, such as how the EMI noise profile of a hybrid SC converter with many additional switching actions looks compared to the industry-regulated limits. Different switching frequency regimes are compared for efficiency and EMI performance. Furthermore, a conventional frequency modulation strategy is applied this new hybrid SC topology demonstrating EMI reductions without efficiency penalties.

To complete the argument of how hybrid SC converters can and should be used in more application areas, Chapter 7 also briefly discusses the sources of loss in the converter and how hybrid SC topologies can have lower losses compared to conventional solutions.

Finally, this dissertation is closed out in Chapter 8 with a review of this work's contributions to power electronics as well as inviting thought into extensions of the work presented here.

Chapter 2

Dickson Converter Variations

This chapter explores the evolution of a family of pure switched-capacitor converters and hybrid switched-capacitor converters based on the Dickson charge-pump. Both conventional topologies and new topologies are discussed here as an introduction to the specific analyses presented in the following chapters.

2.1 Topology Evolution

Historically, a Cockcroft-Walton voltage multiplier circuit [26] was used in discrete converters to step up low voltages to much higher voltages. The combination of switching devices and capacitors(2.1) used as intermediate voltage 'steps' are the building blocks of any switched-capacitor converter. Each capacitor blocks a fraction of the high-side voltage and therefore each diode also is only subjected to a portion of the high-side voltage – allowing for low-voltage rated parts.

In [27], a charge-pump circuit was proposed for high step-up converters as an improvement over the Cockcroft-Walton multiplier. The Dickson charge-pump, named for the proposer, is shown in Fig. 2.2 and instead of having series-connected capacitors as in the Cockcroft-Walton multiplier, the Dickson charge-pump capacitors are connected in parallel among the diodes. This adjustment in capacitor arrangement allows for easier chip-integration. Fur-

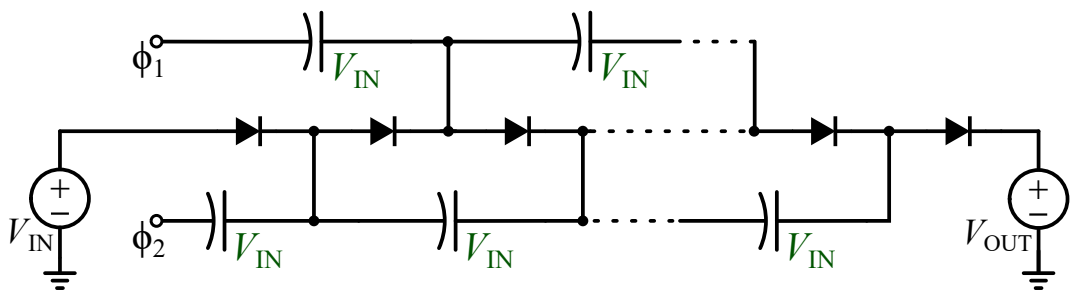


Figure 2.1: Schematic drawing of a Cockcroft-Walton voltage multiplier circuit.

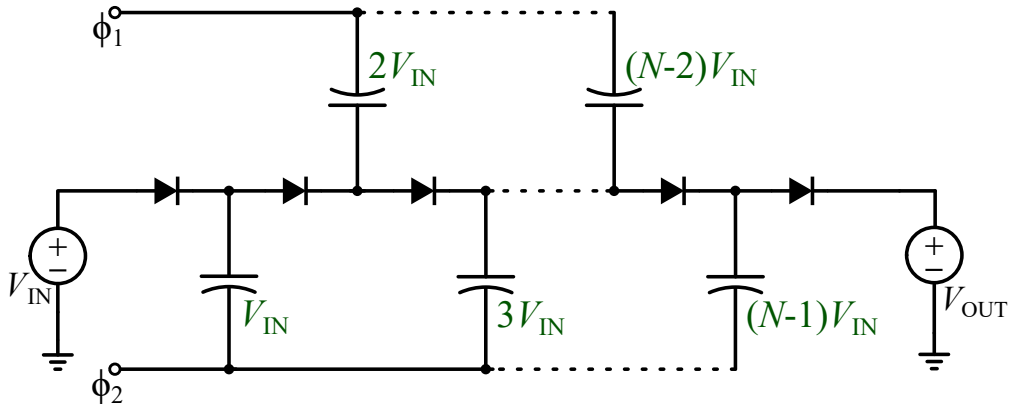


Figure 2.2: Schematic drawing of a Dickson charge-pump circuit.

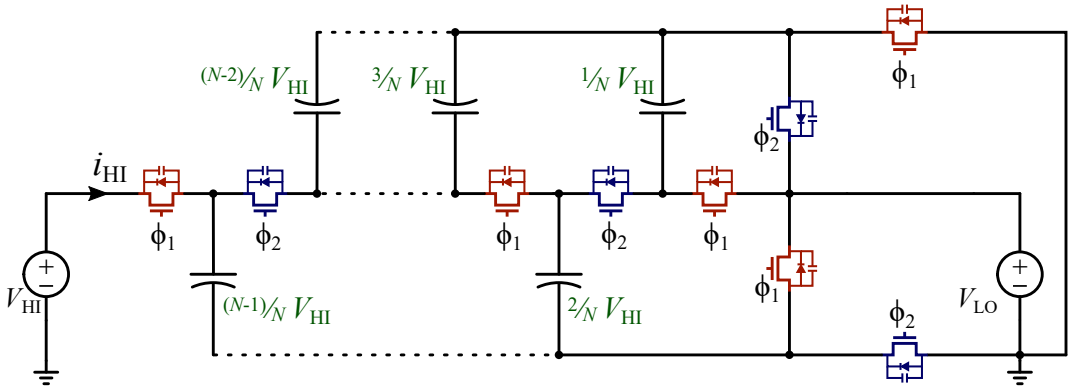


Figure 2.3: Schematic drawing of a pure SC Dickson converter.

thermore, the charge-pump acts similarly to a bootstrapping method, but with the capacitors connected to one of two complementary clock signals to alternately charge the capacitors and discharge them into the load. Despite the capacitors of the Dickson charge-pump needing to block higher voltages than those in the Cockcroft-Walton multiplier, the Dickson charge-pump typically has better performance especially as the conversion ratio increases [27], in part due to the requirement of lower capacitance values.

For step-down applications, the diodes can be replaced with active switching devices as shown in Fig. 2.3. Using two-quandrant devices, such as MOSFETs or GaNFETs, allows power flow from the high-side port to the low-sides port, which is prevented when diodes are used as the switching devices.

As will be described in Chapter 3, one drawback of pure switched-capacitor converters, such as the Cockcroft-Walton multiplier and Dickson charge-pump is the presence of capacitor hard-charging. To mitigate these hard-charging capacitor losses, some small inductance is introduced to enable soft-charging of the flying capacitors [24, 25], forming hybrid switched-capacitor converters. Fig. 2.4 and Fig. 2.5 show hybrid versions of the Cockcroft-Walton multiplier and Dickson charge-pump, respectively. Here, a singular inductance is used to

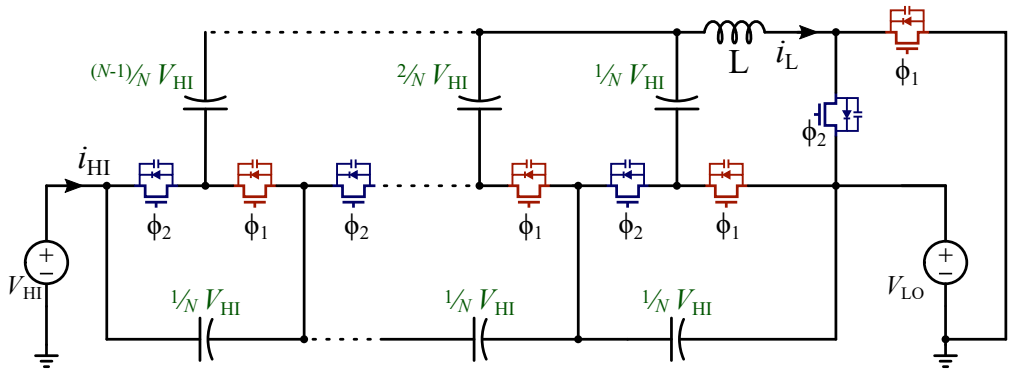


Figure 2.4: Schematic drawing of a hybrid stacked-ladder converter.

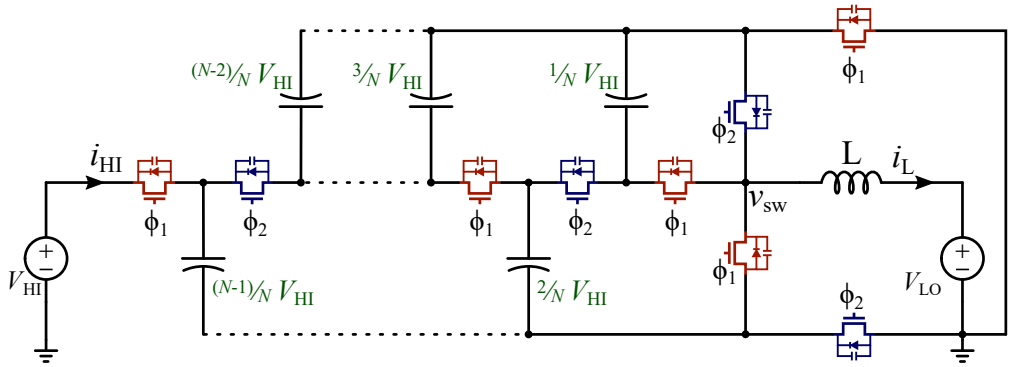


Figure 2.5: Schematic drawing of a hybrid Dickson converter.

facilitate capacitor soft-charging, however, distributed inductors may also be used in other hybrid variations [10, 28, 29] in this family of converters.

Furthermore, interleaving hybrid SC converters have shown strong performance metrics [11, 18, 22, 30] due in part to the reduction of inductor current ripple. Specifically, [11, 22, 30] are derived from Dickson/Cockcroft-Walton circuits with some redundant components eliminated.

As detailed in [12, 31–34], the Dickson converter exhibits minimal total switch stress – defined as the sum across all switching elements of the peak blocking voltage times the rms current through each switch – among hybrid SC converters, making it a practical choice for applications where switching losses are significant and where soft-switching is imperative. The hybrid Dickson converter and the interleaved-input hybrid Dickson converter are used to demonstrate various switching techniques of hybrid SC converters in the following chapters.

2.2 Chapter Summary

This chapter describes the evolution of the Dickson-style hybrid SC converters and introduces two topologies which serve as the basis for the switching analysis and techniques described

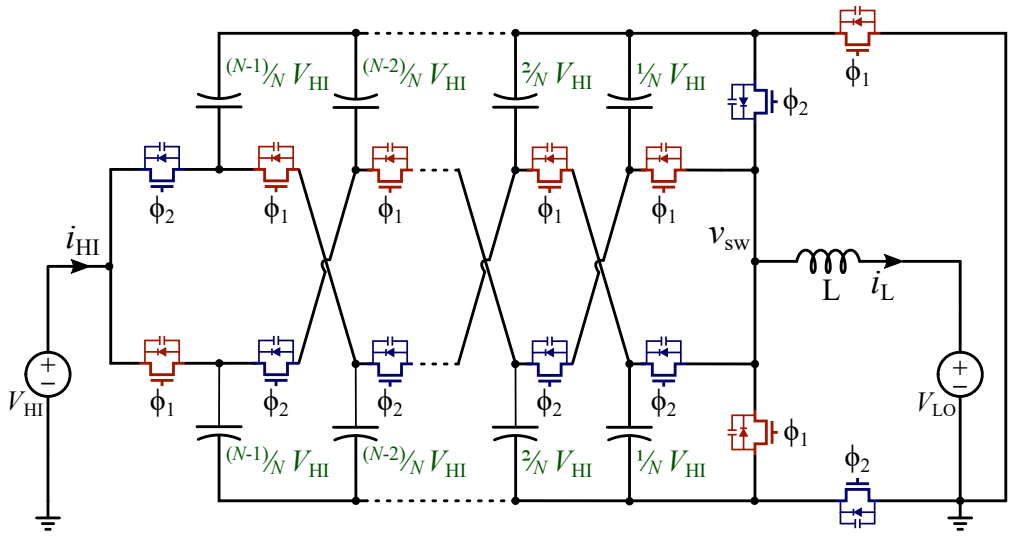


Figure 2.6: Schematic drawing of an interleaved-input hybrid Dickson converter.

in the remainder of this dissertation.

Chapter 3

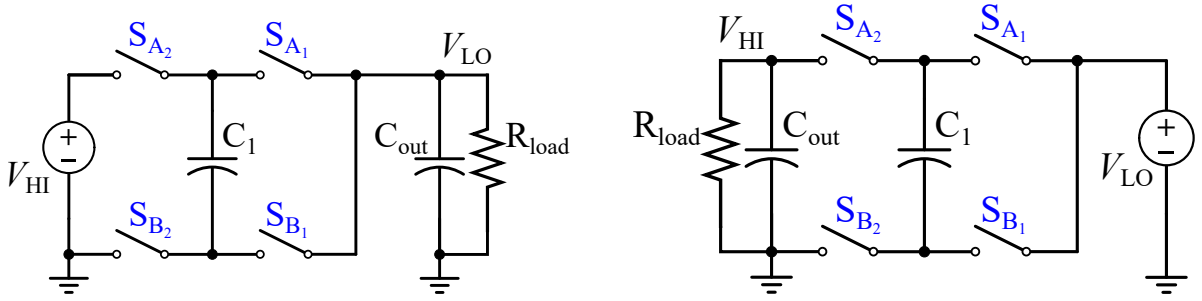
Fundamentals of Hybrid Switched-Capacitor Converters

> Fundamentals are the building blocks of fun.
>
> *Mikhail Baryshnikov*

This chapter highlights the advantages of hybrid switched-capacitor (hybrid SC) converters over conventional pure switched-capacitor (SC) power converters. Then an analytical framework for comparing hybrid SC converters is presented, which will also form the basis of the analysis presented in the following chapters for various switching strategies.

3.1 Modeling of Power Converters

Please note that here and in the remainder of this dissertation, because the presented analysis is (mostly) consistent for both step-up and step-down operation of these power converters (Fig. 3.1), only step-down topologies will be discussed for simplicity. Remarks will be pointed out where step-up operation differs from step-down operation. Furthermore, for simplicity since the analysis here does not account for impacts of terminal capacitance on resonance and converter operation, we model both the high-side and low-side ports as ideal voltage sources, exemplified in the schematic of the conventional Buck converter in Fig. 3.2.



(a) Step-down converter. (b) Step-up converter.

Figure 3.1: Schematic drawings of a step-down and a step-up power converter with consistent analysis presented in the following chapters.

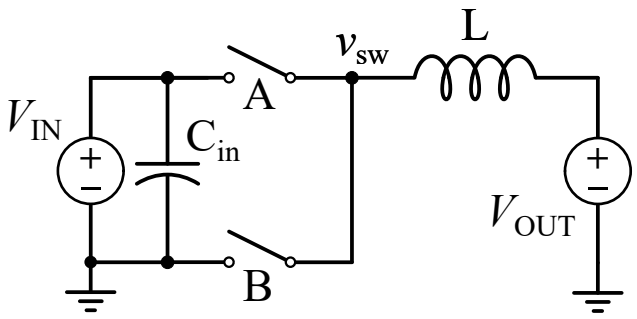


Figure 3.2: Example switched-inductor converter schematic drawing.

3.2 Advantages of Hybrid Switched-Capacitor Converters

Capacitor-based topologies gained traction in both high-conversion-ratio dc-dc and multi-level inverter applications due to various benefits over conventional switched-inductor topologies, such as the Buck converter [35–38]. Moreover, recently, advantages in performance and size (volume and/or mass) of introducing a small inductance into capacitor-based topologies have also been demonstrated [12, 39, 40].

Switched-Inductor and Switched-Capacitor Converters

Compared to conventional switched-inductor topologies, pure switched-capacitor (SC) converters (circuits made of only switches and capacitors) can potentially have higher power densities (i.e., smaller volume/mass for the same processed power) due to the reliance on capacitors as the primary energy storage and processing element, rather than on magnetic elements, such as an inductor, which tend to have lower energy densities [13]. Furthermore, the elimination of the inductor enables easier monolithic integration for low power applications [35–37]. Extending SC converters to high power and high voltage applications

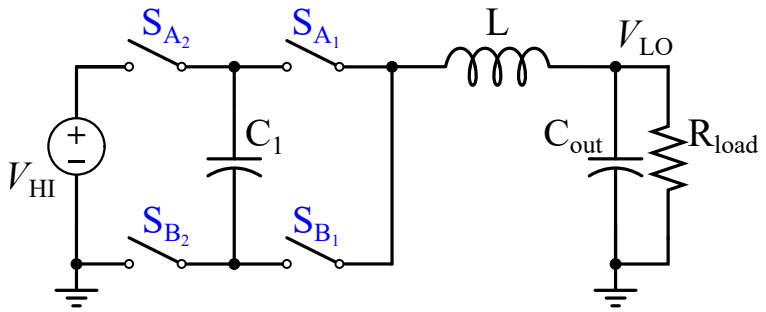


Figure 3.3: Circuit schematic of a 2-to-1 hybrid SC converter with inductor L for soft-charging of capacitor C_1.

does present a few challenges; namely efficiency, voltage regulation, and electromagnetic interference (EMI).

Hybrid Switched-Capacitor Converters

To allay the drawbacks of pure SC converters, a small (compared to conventional switched-inductor topologies) inductance can be inserted into the capacitor charging paths [24, 25, 39–41], creating a 'hybrid' converter which uses both capacitors and inductors for power processing, but still utilizes the capacitors as the primary energy element. An example 2-to-1 'hybrid' converter is illustrated in Fig. 3.3. These hybrid switched-capacitor (hybrid SC) converters can be operated in a resonant-manner to improve efficiency by reducing switching losses, or in a manner similar to that of pulse-width-modulated (PWM) converters to allow for voltage regulation and to reduce conduction losses (from reduced rms currents).

Furthermore, the added inductance helps mitigate the slow-switching limit (SSL) impedance (Fig. 3.4) [32, 42] and associated pulse inrush currents in pure switched capacitor (SC) converters by enabling 'soft-charging' of the flying capacitors [24, 25, 41].

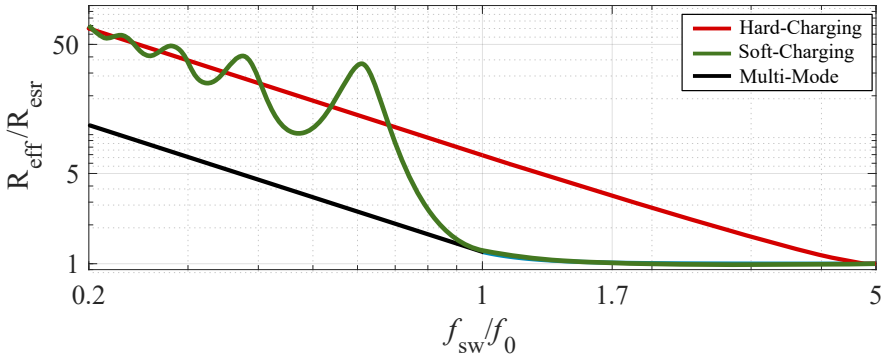


Figure 3.4: Effective output resistance versus frequency of an exemplary pure, resonant, and multi-mode hybrid SC converter [1] in the slow-switching limit frequency range.

Capacitor Soft-charging

The power loss (or output-impedance) in the SSL regime is the result of charging/discharging the capacitors with either a constant voltage source or another capacitor, as illustrated in Fig. 3.5a. This capacitor charge-sharing loss contributes to both lower efficiencies but also to increased EMI, which is a significant concern in several applications such as space and automotive (Chapter 6).

Each switching state of a pure SC converter can be reduced to Fig. 3.5a (or the scenario with one capacitor replaced by a dc voltage source) [1, 43]. For the sake of demonstrating the merits of 'soft-charging', capacitor C_1 is assumed to start fully charged ($V_{1,init} = V_1$) and C_2 fully discharged ($V_{2,init} = 0$); and C_1 and C_2 are assumed to be equal in capacitance.

When the switch closes, because the capacitor voltage cannot change instantaneously, the difference in the initial capacitor voltages is imposed across the series resistor (which may be a combination of switch on-state resistance, trace resistance, and capacitor equivalent series resistance). This voltage differential across a resistive element results in a large instantaneous current through the capacitors, Fig. 3.6, thus producing a noisy transition and termed 'hard-charging'.

The power loss associated with full charge redistribution for the RC circuit in Fig. 3.5a is related to the difference is initial energy, E_{init}, and ending energy, E_{fin}, in the system:

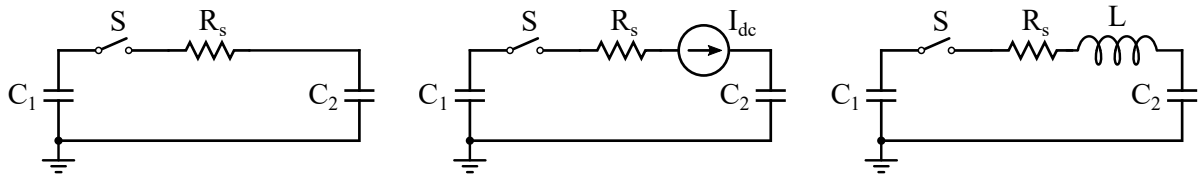
$$P_{\text{loss}} = f_{\text{sw}}(E_{\text{init}} - E_{\text{fin}}) = f_{\text{sw}}\left[\left(\frac{1}{2}C_1V_{1,init}^2 + \frac{1}{2}C_2V_{2,init}^2\right) - \left(\frac{1}{2}C_1V_{1,fin}^2 + \frac{1}{2}C_2V_{2,fin}^2\right)\right] \tag{3.1}$$

$$\rightarrow P_{\text{loss,RC}} = \left(\frac{1}{4}C_1V_1^2\right)f_{\text{sw}} \tag{3.2}$$

This equation is valid only if the on-time duration of the switch is much larger than the time-constant of the circuit, i.e. in the SSL region of operation. Moreover, the capacitor charge-sharing loss does not depend on the value of the series resistance, but rather on the initial difference in voltage across each capacitor. In typical power converter operation, the initial capacitor voltages are dependent on loading conditions, switching frequency, and the capacitance. As load or power are increased, the charge sharing losses can increase proportionally to the *square* of the voltage differential, therefore, limiting the range of allowable voltage ripple based on efficiency [43].

If a current-limiter is placed in series with the capacitors, e.g., Fig. 3.5b, the capacitors charge/discharge linearly, limiting the power loss and generate noise. Furthermore, if instead of a dc current source, an inductor is placed in series with the charging capacitor, a similar benefit is seen. The inductor, which resists instantaneous changes in current charges the capacitor in a resonant manner Fig. 3.5c and Fig. 3.6, again avoiding current spikes. This method of capacitor charging was first termed 'soft-charging' in [24] because the capacitor voltages 'softly' reach equilibrium, without any high dv/dt or di/dt transitions.

Moreover, when soft-charged, capacitor voltage ripple may be greatly increased without incurring large SSL losses. This allows for more effective energy density utilization of the



(a) Hard-charging RC circuit schematic.

(b) Soft-charging RC circuit schematic with an ideal current source.

(c) Soft-charging RLC circuit schematic.

Figure 3.5: Schematic drawings of capacitor charging circuits.

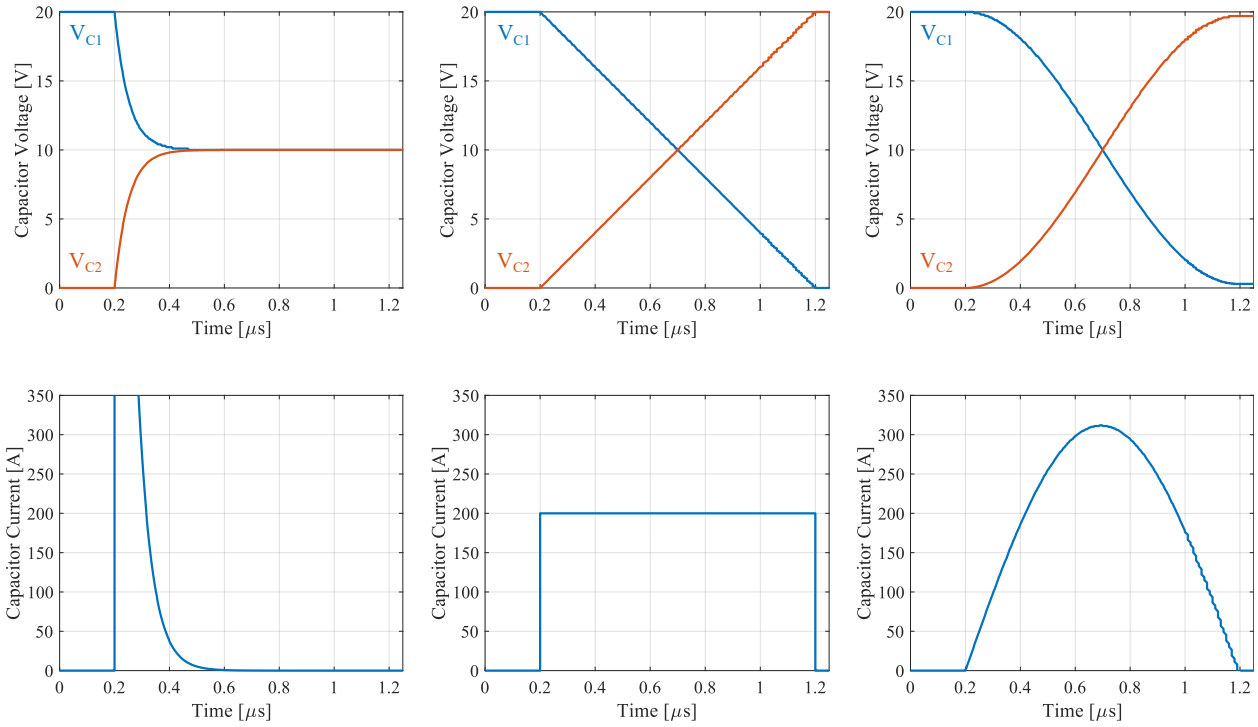


Figure 3.6: Example capacitor charging waveforms corresponding to the circuits in Fig. 3.5.

capacitors which perform most of the voltage conversion [44], while the added magnetics are subjected to reduced volt-seconds. Recent demonstrations [7–12] have considered these benefits and illustrate reductions in overall hybrid SC converter volume as compared with more traditional architectures (e.g. buck/boost).

In addition, it has been shown that resonant converters (those with inductors in series with each capacitor) and soft-charging SC converters (wherein there might only be one lumped inductance) are closely related and it is possible to use similar techniques to analyze and synthesize both types of converters [12, 25, 34].

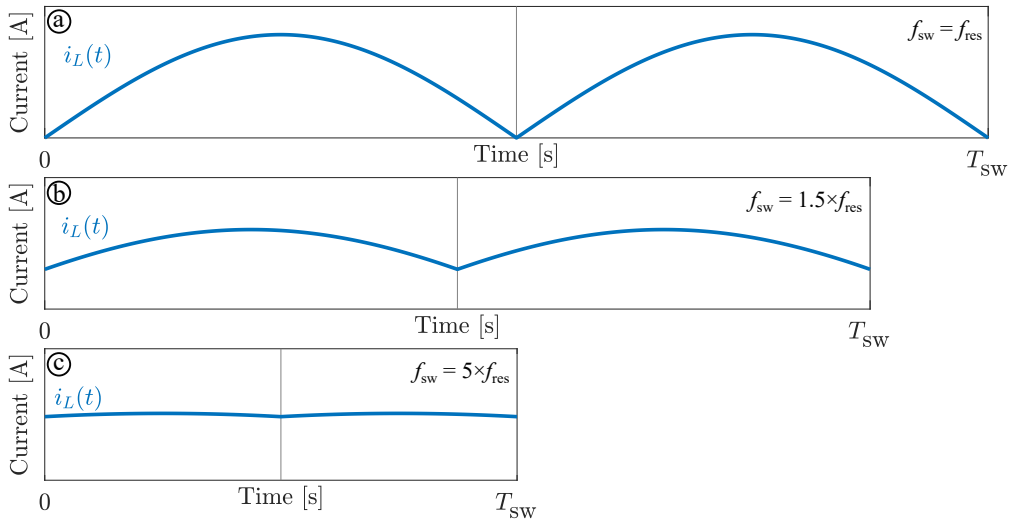


Figure 3.7: Example inductor current waveforms for a hybrid SC converter operating at resonant frequency (a), slightly above resonant frequency (b) and much higher than resonance (c).

Operation Regimes

Hybrid switched-capacitor converters are often operated at the resonant frequency, which depends on the relationship between the effective capacitance and inductance in the conduction path. Because these topologies are made up of different configurations of L-C tanks, when the converter is operated at that resonant point, the inductor current (Fig. 3.7a) is sinusoidal in shape and returns to 0 A at the end of each switching period. Furthermore, some hybrid SC topologies can be operated above resonance (i.e., switching faster than the resonance point). Here, the inductor current does not fully resonate to 0 A, but the shape is still quasi-sinusoidal (Fig. 3.7b-c). Several use-cases and trade-offs for these different operating regimes are discussed in the remainder of this thesis, including impacts on losses, as well as on noise generation.

3.3 General Analysis of Hybrid Switched-Capacitor Converters

Resonant switched capacitor (ReSC) power converters (e.g., Fig. 3.8) are a relatively new class of converter topology. Prior literature has presented analytical methods to calculate both the minimum achievable passive component volume and output impedance for these types of converter; however, these analyses are often limited to ReSC converters operating exactly at resonance (e.g., [12,45]). While this operating point facilitates zero current switching (ZCS) for reduced switching loss, other work in [1, 46–52] has established that operating some ReSC converters above resonance can significantly improve overall converter efficiency

through a reduction in rms currents and associated conduction losses, despite increases in relative switching loss. Although above resonance operation has been demonstrated in practice, a characteristic analysis has been lacking. The framework presented in [12] is not applicable, while a provision (parameter β) in [32] characterizing the ratio of rms to dc inductor current allows the analysis to be extended to above-resonance operation without being explicitly derived.

This work therefore contributes a generalized analytical technique enabling complete characterization of ReSC operation while operating both at and above resonance. No small-ripple approximations are made, resulting in an accurate large-signal solution accounting for both voltage and current ripple on capacitors and inductors, respectively. In addition, the presented analysis is simplified with respect to [12] (which required instantaneous power integrals to be evaluated) and only requires the use of inherent topology characteristics, such as the number of components and phases, and standard charge flow vectors, similar to those described by the analytical method for pure SC converters presented in [42].

While the methodology presented here can be extended and applied to any ReSC converter topology, this work restricts its application to a subset of ReSC converters capable of operating effectively above resonance. Specifically, this work considers fixed-ratio (N:1) ReSC converter topologies with a single inductor placed in series with the low-side port, as is the case for several common example topologies depicted in Fig. 3.8. Termed "direct" in [32, 53], "inductor-at-the-output" in [54], and here as "inductor-at-the-low-side-port" (to accommodate step-up 1:N variants), these structures are capable of operating both at or significantly above their nominal resonant switching frequency. When operated above resonance, the inductor enters a forward continuous conduction mode where the converter exhibits a lower sensitivity to component or timing mismatch, in addition to the aforementioned reduction in rms current.

In contrast, LC-tank type ReSC structures (e.g. [10, 55–59]), termed "indirect" in [53], are constrained to at- or near- resonant operation since they either incur excessive circulating currents when operated above resonance, or hard-charging losses when operated below resonance without the introduction of discontinuous conduction states or dynamic off-time modulation [58, 60, 61].

Consequently, tank-based topologies have a susceptibility to component and timing mismatch and require either active auto-tuning control [62,63], or accurate component tolerance and stability with aging, temperature, and bias — disqualifying Class II multi-layer ceramic capacitors (MLCCs) [64] and soft-saturating magnetics.

Conversely, the switches within tank topologies generally experience favorable constant blocking voltages that are independent of load since voltage ripple is hidden within LC-tank elements [48, 59] — serving to simplify design. Both "direct" and "indirect" topology variations exhibit theoretically identical total passive component volume when operated at resonance, irrespective of inductor count, when inductance is distributed accordingly [12]. However, unless a common core can be used in indirect multi-inductor designs, the magnetics of direct single inductor ReSC designs scale more favorably [65], lending further preference to direct variants. Moreover, the LC tanks within indirect topologies require bi-directional

inductor current, necessitating a 2× increase in flux density ripple, ΔB, as compared to the uni-polar current observed in equivalent direct converters, where much of the spectral power is concentrated at dc, having implications for magnetic losses [66, 67].

Following this reasoning, the subset of ReSC converters evaluated in this work (single inductor "direct" topologies) are simultaneously highly attractive and challenging to fully analyze.

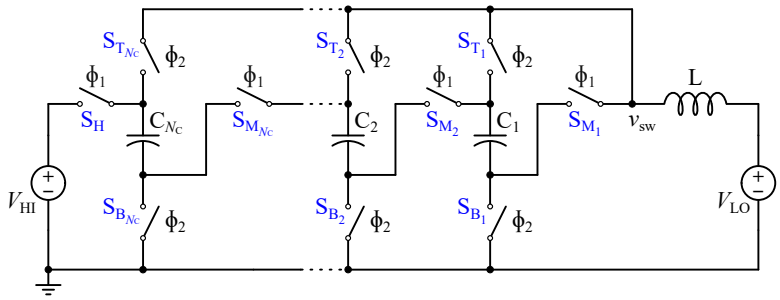
Analytical expressions for peak ratings are derived for both the capacitor voltages and inductor current, aiding the practicing engineer in component selection. These expressions also permit a derivation of the minimum passive component volume, both at- and arbitrarily above- resonance. The general expressions derived herein collapse into the results presented in [12] when constrained to resonant operation, further validating this general approach. In addition, this framework is used to improve the fidelity of calculated switch stress metrics. Prior switch stress computations typically use simplified voltage and current calculations to characterize the switches, such as neglecting the effects of capacitor voltage ripple on switch voltage [12, 42, 51, 68] or neglecting the effects of inductor current ripple on switch current [12, 42].

Here we calculate the precise peak switch voltages and rms currents and demonstrate that prior simplifying assumptions can lead to significant under-sizing of switches for high-ripple designs. Moreover, while minimized passive component volume is emphasized, the presented framework assists with global optimization efforts (e.g., [69]) by providing the large-signal values and waveforms needed for accurate loss estimation.

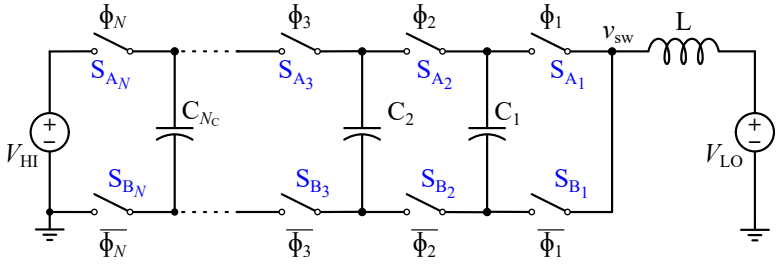
Table 3.1 summarizes, categorizes, and highlights the limitations of several analytical approaches to SC and ReSC analysis presented in the literature. For example when assessing passive volume, [12] addresses both capacitor voltage ripple, Δv_{C}, and inductor current ripple, Δi_L, for both direct and indirect topologies, strictly at resonance. However, the impact of ripple on switch stress is not considered.

3.4 Framework Definition

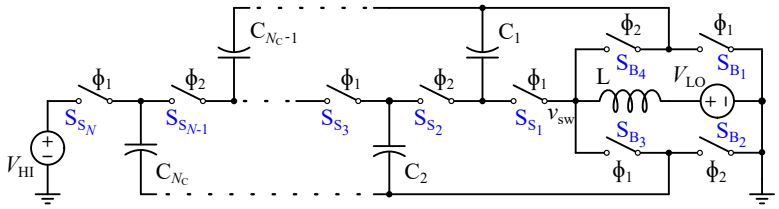
The proposed framework stems from conventional vectorized descriptions of switched capacitor converters in [25, 32, 42, 71] and is derived from fundamental charge-balance and zero volt-second principles. In addition, we assume periodic steady-state operation, with dynamic response beyond the scope of this work. Ideal circuit elements are also assumed, with no ohmic losses or parasitic effects. This assumption is valid for moderate- to heavy-load operation and where ohmic losses have minimal impact on the large-signal dynamics of a converter designed for high efficiency (e.g. $\eta \geq 95\%$). Phase durations are chosen so each phase begins and ends with the same inductor current, implying zero inductor volt-seconds within each phase. This constraint is justified in [34]. Lastly, input and output bypass capacitance is assumed large with respect to the flying capacitors, thus the input and output sources can be considered ideal as is done in many existing models and analyses [9, 25, 32, 42, 48, 72]. Finite input/output bypass capacitors may be included as part of a comprehensive analysis that



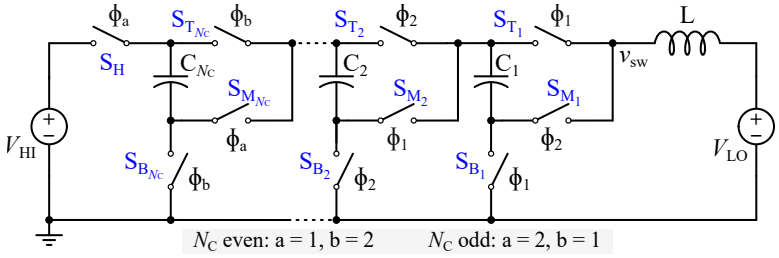
(a) Series-parallel



(b) FCML



(c) Dickson (odd N)



(d) Fibonacci

Figure 3.8: Four common N:1 ReSC converters with "inductor-at-the-output": (a) series-parallel, (b) flying capacitor multilevel (FCML), (c) Dickson (odd N), and (d) Fibonacci. Here N refers to the conversion ratio and N_C refers to the total number of capacitors.

facilitates port voltage ripple constraints [73, 74], however, this adds significant analytical complexity and is omitted here for conciseness. This framework applies not only to two-phase ReSC, but also to multi-phase/multi-resonant converters—more than two phases in a switching period—such as the flying capacitor multi-level (FCML) converter in Fig. 3.8b.

Table 3.1: Survey of Analytical Methods for Switched-Capacitor Converters

	Work	Type	Above Resonance	Analyzes Ripple		Calculates Loss
				Passives	Switches	
Pure SC	Seeman [42]	–	–	Δv_{C}	None	Yes
	McRae [70]	–	–	Δv_{out}	Δv_{out}	Yes
ReSC	Pasternak [32]	Direct	Yes	Δi_L*	Δi_L	Yes
	He [58]	Indirect	–	Δv_{C}, Δv_{out}, Δi_L	None	Yes
	McLaughlin [45]	Both	No	Δi_L*	Δi_L	Yes
	Ye [12]	Both	No	Δv_{C}, Δi_L	None	No
	This Work	Direct	Yes	Δv_{C}, Δi_L	Δv_{C}, Δi_L	No

*provisions for capacitor voltage or inductor current ripple, but does not explicitly define it.

To begin, several topologically-defining vectors are obtained through careful analysis and deduction for each ReSC structure under consideration. These are summarized in Table 3.2 and listed in order of appearance throughout the following sections. General matrices are defined in addition to example values for the odd-N Dickson topology depicted in Fig. 3.8a.

Charge Flow Matrices: $\boldsymbol{a_x}$

As is typical for purely capacitor-based converters [42], periodic steady-state analysis of ReSC structures also begins by assessing charge flow through the converter. To do so, charge flow quantities through all circuit elements are normalized to the amount of charge periodically conducted by the high-side port, q_{HI}, as

$$q_{\mathrm{X},ji} = q_{\mathrm{HI}}\, a_{\mathrm{X},ji} \tag{3.3}$$

where X is the circuit element type (e.g., capacitor, C; inductor, L; or switch, S), j is the phase index, and i is the element index. The charge quantity q_{HI} is itself an operating parameter defined as

$$q_{\mathrm{HI}} = \frac{I_{\mathrm{HI}}}{f_{\mathrm{SW}}} = I_{\mathrm{HI}} T_{\mathrm{SW}} \tag{3.4}$$

Table 3.2: Definition of Characteristic Terms

N	Conversion ratio, N:1 for $N \in \mathbb{N} \geq 2$
N_{C}	Total number of flying capacitors
N_{P}	Total number of phases within a switching period
N_{S}	Total number of switching devices
$a_{X,ji}$	Net charge through the ith element of type X (C, L, or S), during phase j, normalized to high-side charge quantity q_{HI}
v_i	Mid-range dc voltage on ith capacitor, normalized to high-side voltage V_{HI}
c_i	Capacitance of ith capacitor, normalized to arbitrary scaling capacitance C_0
κ_j	Equivalent capacitance seen by the inductor during phase j, normalized to capacitance C_0
$\omega_{0,j}$	Natural angular frequency of the equivalent LC network during phase j
t_j	Time duration of phase j
τ_j	Time duration of phase j normalized to the full switching period T_{sw}

where I_{HI} is the average high-side port current and f_{SW} is the periodic switching frequency (with associated switching period T_{SW}). Subsequently the normalized charge flow matrix, $\boldsymbol{a}_{\boldsymbol{X}}$, is comprised of topologically-dependent entries which are invariant of operating point (i.e., power level, voltage, and switching frequency) whereas q_{HI} scales the charge conducted through all elements in unison, while preserving their relative relationships.

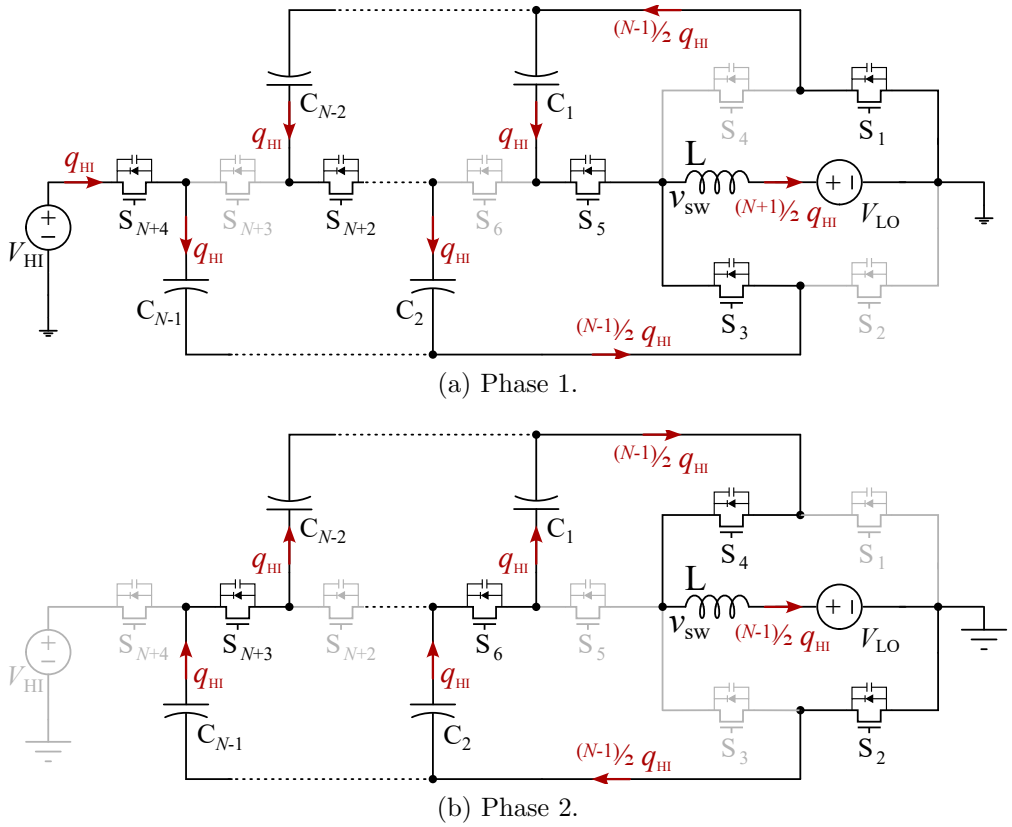
Periodic steady-state requires the capacitors displace zero net charge per full switching period, as described by

$$\sum_{j=1}^{N_{\mathrm{P}}} a_{\mathrm{C},ji} = 0, \tag{3.5}$$

where N_{P} is the number of operating phases. Utilizing this characteristic, values for $\boldsymbol{a}_{\mathrm{C}}$, and subsequently $\boldsymbol{a}_{\mathrm{L}}$ and $\boldsymbol{a}_{\mathrm{S}}$, can then be obtained by inspection.

For example, Fig. 3.9 depicts the periodic steady-state charge flow through an N:1 odd-N Dickson step-down converter operating with two switching phases ($N_{\mathrm{P}} = 2$) and with $N_{\mathrm{C}} = N - 1$ flying capacitors. During phase 1, charge q_{HI} is provided by the high-side source V_{HI}, and is admitted by all even-numbered flying capacitors. In adherence with (3.5), each even-numbered flying capacitor must then release charge q_{HI} during phase 2. The odd-numbered flying capacitors exhibit equal and opposite charge flow of the even-numbered flying capacitors in each phase.

Subsequently, the normalized capacitor charge values, $a_{\mathrm{C},ji}$, for the odd-N Dickson topol-



(a) Phase 1.

(b) Phase 2.

Figure 3.9: Charge flow in a two-phase N:1 odd-N Dickson converter.

ogy are

$$\boldsymbol{a}_{\mathrm{C}_{[N_\mathrm{P}\times N_\mathrm{C}]}} = \begin{bmatrix} \frac{q_{\mathrm{C},11}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},12}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},1N_\mathrm{C}}}{q_\mathrm{HI}} \\ \frac{q_{\mathrm{C},21}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},22}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},2N_\mathrm{C}}}{q_\mathrm{HI}} \end{bmatrix} = \begin{bmatrix} -1 & 1 & \cdots & -1 & 1 & -1 \\ 1 & -1 & \cdots & 1 & -1 & 1 \end{bmatrix} \tag{3.6}$$

where the first row's entries correspond to phase 1 and the second row's entries correspond to phase 2. The charge matrices $\boldsymbol{a}_\mathrm{L}$ and $\boldsymbol{a}_\mathrm{S}$ are similarly determined.

Furthermore, as shown in Fig. 3.9, the charge admitted by V_LO over both phases is equal to $q_\mathrm{LO} = (N_\mathrm{C}/2)\, q_\mathrm{HI} + ((N_\mathrm{C}+2)/2)\, q_\mathrm{HI}$, yielding the converter's voltage conversion ratio:

$$\frac{V_\mathrm{HI}}{V_\mathrm{LO}} = \frac{I_\mathrm{LO}}{I_\mathrm{HI}} = \frac{q_\mathrm{LO} f_\mathrm{sw}}{q_\mathrm{HI} f_\mathrm{sw}} = \frac{((N_\mathrm{C}+2)/2)\, q_\mathrm{HI} + (N_\mathrm{C}/2)\, q_\mathrm{HI}}{q_\mathrm{HI}} = N. \tag{3.7}$$

Moreover, converter power throughput, P_{HI}, may be expressed in terms of the average high-side charge q_{HI} as

$$P_{\text{HI}} = I_{\text{HI}} V_{\text{HI}} = \frac{q_{\text{HI}}}{T_{\text{sw}}} V_{\text{HI}}. \tag{3.8}$$

Mid-Range Flying Capacitor Voltage Vector: $\boldsymbol{v}$

Each flying capacitor's mid-range voltage is defined as the dc value symmetrically centered between the maximum and minimum voltage, as dictated by ripple. This value is distinct from the time-averaged dc voltage which can deviate significantly in multi-phase converters. Here the mid-range voltages can be derived from an assumption of zero average voltage across the inductor (i.e., zero volt-seconds) within each phase. Under this assumption, the inductor may be treated as a short circuit when applying average KVL loops to each phase. Subsequently the absolute mid-range voltages of each flying capacitor, V_{C_i}, may be expressed with respect to the high-side voltage, V_{HI}, as

$$V_{\text{C}_i} = V_{\text{HI}}\, v_i, \tag{3.9}$$

where v_i represents the normalized (to V_{HI}) mid-range voltage. By applying per-phase *average* KVL [34] to the N:1 odd-N Dickson depicted in Fig. 3.10, yields the following:

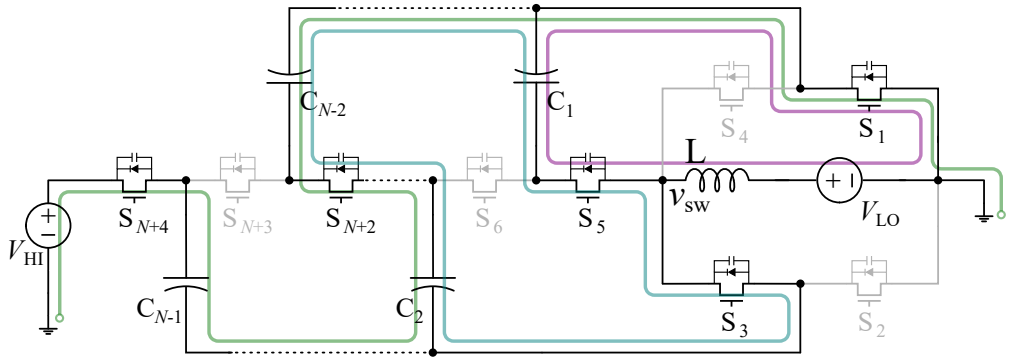
$$\text{Phase 1:} \begin{cases} \langle V_{\text{HI}} \rangle - \langle v_{N\text{-}1} \rangle - \langle v_{N\text{-}2} \rangle + \langle v_{N\text{-}3} \rangle - \langle v_{\text{L}} \rangle - \langle V_{\text{LO}} \rangle = 0 \\ \vdots \\ \langle v_3 \rangle - \langle v_2 \rangle - \langle v_1 \rangle - \langle v_{\text{L}} \rangle - \langle V_{\text{LO}} \rangle = 0 \\ \langle v_1 \rangle - \langle v_{\text{L}} \rangle - \langle V_{\text{LO}} \rangle = 0 \end{cases} \tag{3.10}$$

$$\text{Phase 2:} \begin{cases} \langle v_{N\text{-}1} \rangle - \langle v_{N\text{-}2} \rangle - \langle v_{N\text{-}3} \rangle + \langle v_{N\text{-}4} \rangle - \langle v_{\text{L}} \rangle - \langle V_{\text{LO}} \rangle = 0 \\ \vdots \\ \langle v_2 \rangle - \langle v_1 \rangle - \langle v_{\text{L}} \rangle - \langle V_{\text{LO}} \rangle = 0 \end{cases} \tag{3.11}$$

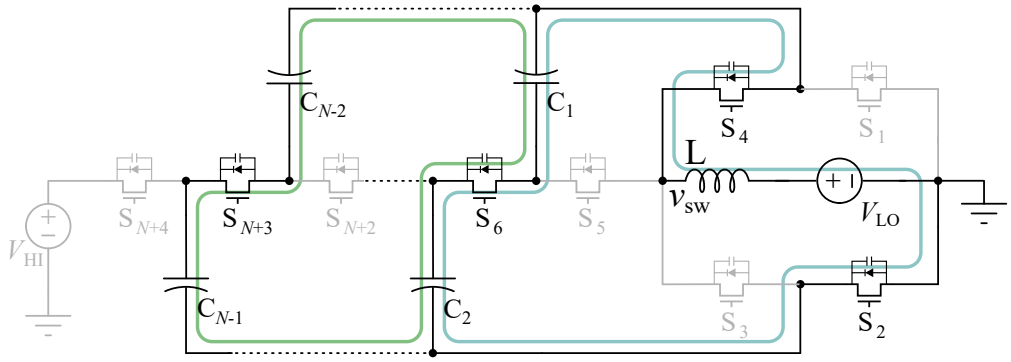
Using the conversion ratio relationship established in (3.7), and assuming that the per-phase average inductor voltage, $\langle v_{\text{L}} \rangle$ is 0 V in periodic steady-state operation [34], the system of equations can be solved. Then, the normalized capacitor voltage vector, $\boldsymbol{v}$, for the two-phase odd-N hybrid SC Dickson converter is defined as

$$\begin{aligned} \boldsymbol{v}_{[1\times N_{\text{C}}]} &= \begin{bmatrix} \dfrac{V_{\text{C}_1}}{V_{\text{HI}}} & \dfrac{V_{\text{C}_2}}{V_{\text{HI}}} & \cdots & \dfrac{V_{\text{C}_{N_{\text{C}}}}}{V_{\text{HI}}} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{1}{N} & \dfrac{2}{N} & \cdots & \dfrac{N_{\text{C}}}{N} \end{bmatrix}. \end{aligned} \tag{3.12}$$

Certain multi-resonant topologies—e.g., the multi-resonant doubler [75] and the cascaded series-parallel [76]—or switching schemes—e.g., split-phase switching [77, 78]—have mid-range voltages dependent on load [71], adding significant analytical complexity. The mid-range voltages for a split-phase hybrid Dickson converter are derived in Chapter 4.



(a) Phase 1.



(b) Phase 2.

Figure 3.10: KVL loops in an N:1 odd-N Dickson converter.

Capacitance Vector: $\boldsymbol{c}$

While some topologies have no strict constraints on capacitance sizing (e.g. FCML converter), others require specific relative sizing to prevent hard-charging and retain simplified clocking schemes, as derived in [25, 30, 71, 79] for example. The absolute capacitance of each flying capacitor, C_i, is normalized to a single capacitance value, C_0, as

$$C_i = C_0 \, c_i \tag{3.13}$$

and by doing so, the required relative capacitor relationships are preserved as the single value C_0 changes—a useful feature for the analytical passive component volume minimization performed in [34].

Considering the exemplar odd-N Dickson topology, all capacitors conduct equal charge in each phase, and each parallel capacitor branch must express identical voltage ripple characteristics, as shown by the equivalent circuits in Fig. 3.11.

Thus, by $Q = CV$ (and to ensure soft-charging behavior) within a phase, each parallel capacitor branch must be equal in effective impedance value. Another system of equations can written and solved for the required capacitor sizing for this converter to ensure soft-

charging with two-phase operation:

$$\boldsymbol{c}_{[1\times N_\mathrm{C}]} = \begin{bmatrix} \frac{C_1}{C_0} & \frac{C_2}{C_0} & \cdots & \frac{C_{N_\mathrm{C}}}{C_0} \end{bmatrix} \tag{3.14}$$

$$= \begin{bmatrix} \frac{N_\mathrm{C}}{N_\mathrm{C}} & \frac{N_\mathrm{C}}{2} & \frac{N_\mathrm{C}}{N_\mathrm{C}-2} & \frac{N_\mathrm{C}}{4} & \cdots & \frac{N_\mathrm{C}}{2} & \frac{N_\mathrm{C}}{N_\mathrm{C}} \end{bmatrix} \tag{3.15}$$

where odd-numbered capacitors have a relative capacitance of $C_i = {}^{N-1}\!/_{N-i}$ and even-numbered capacitors $C_i = {}^{N-1}\!/_{i}$.

The normalized capacitance vector, $\boldsymbol{c}$, is documented in [34] for the series-parallel, Dickson, and Fibonacci, and FCML topologies.

Lumped Equivalent Capacitance Vector; $\boldsymbol{\kappa}$

During each switching phase j, the inductor forms a second-order resonant impedance network with the connected flying capacitors, which have an equivalent lumped capacitance, $C_{\mathrm{e},j}$. This value is then normalized with respect to C_0, yielding $\boldsymbol{\kappa}$:

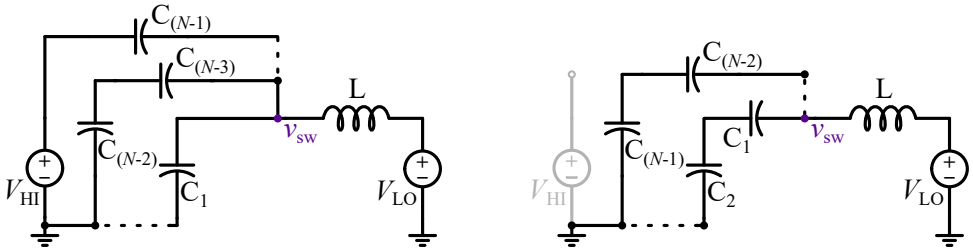
$$C_{\mathrm{e},j} = C_0\,\kappa_j. \tag{3.16}$$

In Phase 1 of the example odd-N Dickson converter (Fig. 3.11), two capacitor branches have a singular capacitor of capacitance $C_i = 1$, where as there are ${}^{(N_\mathrm{C}-3)}\!/_2$ branches with two capacitors in series with capacitance determined by (3.15). However, as mentioned, to maintain voltage matching at phase transitions, the effective capacitance of each branch is equal, and must equal $1 \times C_0$. Therefore, the effective capacitance in Phase 1 as seen at the inductor switch-node is:

$$C_{\mathrm{e},1} = \frac{N_\mathrm{C}+2}{2}\,C_0 \tag{3.17}$$

Moreover, in Phase 2 all capacitor branches comprise two series connected capacitors, again with equivalent impedances. From the relative capacitance sizing defined by (3.14), the effectice capacitance for Phase 2 can also be determined.

$$C_{\mathrm{e},2} == \frac{N_\mathrm{C}^2}{2(N_\mathrm{C}+2)}\,C_0. \tag{3.18}$$



(a) Phase 1. (b) Phase 2.

Figure 3.11: Per-phase equivalent circuits for a two-phase N:1 odd-N Dickson converter.

More generally, the normalized equivalent capacitance vector, $\boldsymbol{\kappa}$, is defined and shown for the odd-N Dickson topology as

$$\boldsymbol{\kappa}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \frac{C_{\mathrm{e},1}}{C_0} \\ \frac{C_{\mathrm{e},2}}{C_0} \end{bmatrix} \tag{3.19}$$

$$= \begin{bmatrix} \frac{N+1}{2} \\ \frac{(N-1)^2}{2(N+1)} \end{bmatrix}. \tag{3.20}$$

This section has obtained fundamental topology-dependent parameters. However, in order to fully characterize the large signal behaviour of a ReSC converter, including passive volume and switch stress both at and above resonance (discussed in [34]), switching-frequency dependencies must also be derived. The following Section 3.5 explores how phase timings and current waveforms depend on switching frequency.

3.5 Phase Timings

A "direct" ReSC converter can be switched at its natural resonant switching frequency, $f_{\mathrm{sw},0}$, to achieve zero current switching (ZCS) at each phase transition. However, dissimilar to "indirect" or LC-tank topologies, the switching frequency of a direct topology may also be increased without incurring increased circulating currents [80]. Subsequently, we define a free parameter, Γ, as the ratio of the actual switching frequency, f_sw, to the natural resonant switching frequency

$$\Gamma = \frac{f_\mathrm{sw}}{f_{\mathrm{sw},0}} = \frac{T_{\mathrm{sw},0}}{T_\mathrm{sw}}. \tag{3.21}$$

Resonant ZCS is obtainable at $\Gamma = 1$ (i.e., at-resonance operation), while for $\Gamma > 1$ (i.e., above-resonance operation) the inductor enters continuous conduction mode (CCM). In practice, values of $\Gamma < 1$ (i.e., below-resonance operation) would only be implemented with a modified discontinuous conduction mode (DCM) or dynamic off-time modulation (DOTM) [53, 60], otherwise SSL losses would reemerge.

The motivation for operation above resonance operation has been explored in [1, 46, 48, 49, 51, 52, 80] as a method for reducing conduction losses and improving overall efficiency due to lower rms currents, smaller capacitor voltage ripple, and lower switch voltage and current stress. However, for several topologies—including the FCML converter and resonant N-phase implementations of Cockcroft-Walton and Dickson converters [81, 82]—the phase durations depend heavily on the relationship between the natural resonant switching frequency and the implemented f_sw. Given that a rigorous proof of the necessary phase timings for above resonance operation has not been demonstrated in the literature, [48, 80] instead relied on closed-loop control to converge on appropriate phase durations.

Therefore, this section expands on an earlier version of this work in [52] to explicitly derive the required relative phase durations for any given switching frequency at or above resonance ($\Gamma \geq 1$). Continuous closed-form expressions are derived for phase-timing durations which minimize the peak, peak-to-peak, and rms inductor current both at resonance and for arbitrary frequencies above resonance. The presented analysis yields a robust method for explicitly determining the phase durations as well as the inductor current waveform used for the switch stress analysis in Chapter 7.

Phase Duration Vector: $\boldsymbol{\tau}$

Each phase duration, t_j, can be defined in terms of the full switching period, T_{sw}, using a normalization parameter, τ_j,

$$t_j = T_{\text{sw}}\,\tau_j \tag{3.22}$$

where T_{sw} defines the sum of all N_{P} phase durations

$$T_{\text{sw}} = \sum_{j=1}^{N_{\text{P}}} t_j. \tag{3.23}$$

The normalized phase duration vector, $\boldsymbol{\tau}$, is deduced from the resonance of the inductor current $i_L(t)$ for each topology and as a function of Γ.

When operating at the resonant switching frequency, $f_{\text{sw},0}$ (i.e., $\Gamma = 1$), each phase is half-wave resonant with $i_{\text{L}}(t)$ starting and ending at 0 A. Thus the phase duration, t_j, equals half the duration of the natural resonant period, $T_{0,j}$, of the lumped LC resonant tank in the jth phase or

$$t_j|_{\Gamma=1} = T_{\text{sw},0} \cdot \tau_j|_{\Gamma=1} = \frac{T_{0,j}}{2} \tag{3.24}$$

as per (3.22).

The natural angular frequency, $\omega_{0,j}$, associated with $T_{0,j}$ can be expressed as

$$\omega_{0,j} = \frac{1}{\sqrt{L \cdot C_0 \kappa_j}} = \frac{2\pi}{T_{0,j}} = \frac{\pi}{t_j|_{\Gamma=1}} \tag{3.25}$$

since parameter κ_j defines the lumped equivalent capacitance.

Calculating the phase durations, t_j, for operation above resonance (i.e., $\Gamma > 1$) requires further analysis. Within each phase j, if the inductor is subjected to zero volt-seconds, then it forms a symmetrically centered sinusoidal segment, as depicted in Fig. 3.12. Continuity in $i_{\text{L}}(t)$ between adjacent phases (including $j = N_{\text{P}}$ and $j = 1$) can be expressed mathematically as

$$I_{\text{pk},j} \cos\left(\omega_{0,j} \frac{t_j}{2}\right) = I_{\text{pk},j+1} \cos\left(\omega_{0,j+1} \frac{-t_{j+1}}{2}\right), \quad \forall j \leq N_{\text{P}} \tag{3.26}$$

where $I_{\text{pk},j}$ is the peak current in phase j.

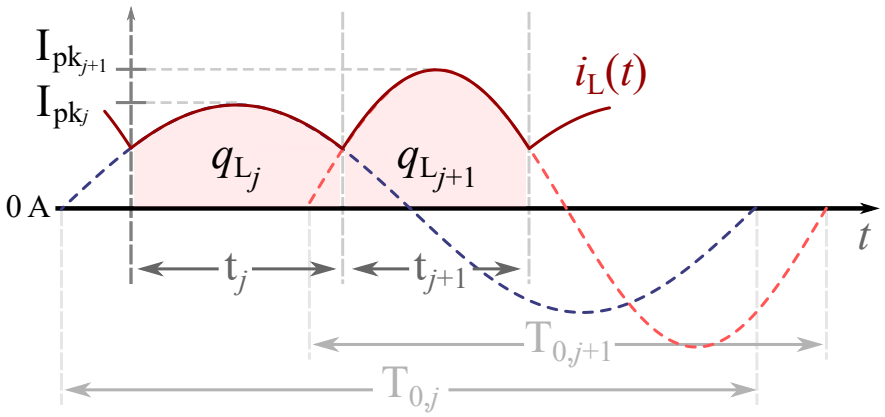


Figure 3.12: Two adjacent phases of the inductor current waveform, $i_L(t)$, operating above resonance. Each phase constitutes a symmetrically centered sinusoidal segment with angular frequency governed by (3.25).

Furthermore during phase j, the inductor conducts charge $q_{\mathrm{L},j}$, where

$$\begin{aligned} q_{\mathrm{L},j} &= \int_{-\frac{t_j}{2}}^{\frac{t_j}{2}} I_{\mathrm{pk},j} \cos(\omega_{0,j}\, t)\, dt \\ &= \frac{2I_{\mathrm{pk},j}}{\omega_{0,j}} \sin\left(\omega_{0,j} \frac{t_j}{2}\right) = q_{\mathrm{HI}}\, a_{\mathrm{L},j}, \quad \forall j \leq N_{\mathrm{P}} \end{aligned} \tag{3.27}$$

which relates to the known normalized charge flow matrix, $\boldsymbol{a}_{\mathrm{L}}$, and can be rearranged with respect to $I_{\mathrm{pk},j}$ as

$$I_{\mathrm{pk},j} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2 \sin\left(\omega_{0,j} \frac{t_j}{2}\right)}, \quad \forall j \leq N_{\mathrm{P}}. \tag{3.28}$$

Combining the phase-to-phase current continuity (3.5) and per-phase charge flow (3.28) yields

$$\frac{a_{\mathrm{L},j}\, \omega_{0,j}}{\tan\left(\omega_{0,j} \frac{t_j}{2}\right)} = \frac{a_{\mathrm{L},j+1}\, \omega_{0,j+1}}{\tan\left(\omega_{0,j+1} \frac{t_{j+1}}{2}\right)}, \quad \forall j \leq N_{\mathrm{P}}. \tag{3.29}$$

Equation (3.29) can be solved using (3.25) and (3.22), to determine appropriate normalized phase durations, τ_j, for each phase. For all two-phase converters, τ_j is notably independent of Γ, as will be demonstrated for the odd-N Dickson converter in Example 1. However, as detailed in [52], phase durations for the FCML converter vary with Γ.

Example: Two-Phase Odd-N Dickson Converter

Consider the two-phase odd-N Dickson topology with arbitrary conversion ratio N in Fig. 3.9 as an example. Substituting the normalized equivalent capacitance vector, κ_j, from (3.20)

into the natural angular frequency, $\omega_{0,j}$, during each phase in (3.25) yields

$$\omega_{0,1} = \sqrt{\frac{2}{N+1}} \cdot \frac{1}{\sqrt{LC_0}} \tag{3.30}$$

and

$$\omega_{0,2} = \sqrt{\frac{2(N+1)}{(N-1)^2}} \cdot \frac{1}{\sqrt{LC_0}} \tag{3.31}$$

with the corresponding relationship between these two frequencies as

$$\omega_{0,1} = \left(\frac{N-1}{N+1}\right)\omega_{0,2}. \tag{3.32}$$

Next, (3.32) and values for normalized inductor charge flow, $a_{\mathrm{L},j}$, (3.34) derived earlier are substituted into the steady-state charge flow and inductor continuity constraint given by (3.29), yielding (3.35)

$$\boldsymbol{a}_{\mathrm{L}_{[N_\mathrm{P}\times 1]}} = \begin{bmatrix} \frac{q_{\mathrm{L},1}}{q_{\mathrm{HI}}} \\ \\ \frac{q_{\mathrm{L},2}}{q_{\mathrm{HI}}} \end{bmatrix} \tag{3.33}$$

$$= \begin{bmatrix} \frac{N_\mathrm{C}}{2} \\ \\ \frac{N_\mathrm{C}+2}{2} \end{bmatrix} \tag{3.34}$$

$$\tan\left(\omega_{0,1}\frac{t_1}{2}\right) = \tan\left(\omega_{0,1}\left(\frac{N+1}{N-1}\right)\cdot\frac{t_2}{2}\right) \tag{3.35}$$

The argument of each tangent is then equated to find a relationship between the two phase time durations

$$t_1 = \frac{N+1}{N-1}\,t_2. \tag{3.36}$$

For this two-phase topology

$$T_\mathrm{sw} = t_1 + t_2, \tag{3.37}$$

and therefore the normalized phase durations, τ_j, become

$$\boldsymbol{\tau}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \frac{t_1}{T_\mathrm{sw}} \\ \\ \frac{t_2}{T_\mathrm{sw}} \end{bmatrix} \tag{3.38}$$

$$= \begin{bmatrix} \frac{N+1}{2N} \\ \\ \frac{N-1}{2N} \end{bmatrix}$$

where $\boldsymbol{\tau}$ only varies with conversion ratio and not Γ.

In addition, substituting (3.32) and (3.36) into (3.5) reveals $I_{\text{pk},1} = I_{\text{pk},2}$—a consistent result for all two-phase converters considered in [34].

3.6 Chapter Summary

This chapter discusses the merits and advantages of hybrid SC converters over conventional switched-inductor and pure SC converters. Furthermore, an analytical framework is established for comparing resonant hybrid SC converters operating at or above resonance. This framework can be extended to evaluate these hybrid SC converters operating as PWM converters. In addition to providing appropriate phase durations for minimized rms currents, this chapter describes a simple method to realize the complete inductor current waveform, allowing not only accurate peak required energies to be calculated, but also more accurate converter losses to be calculated (Chapter 7). The framework presented in this chapter serves as a basis for optimizing hybrid SC converter design based on component peak energy requirements as well as switch stress, which is discussed in Chapter 7.

Chapter 4

Split-Phase Switching

The previous chapters discuss the merits of hybrid switched-capacitor (hybrid SC) converters, there is, however, one caveat: maintaining soft-charging of the flying capacitors and subsequent high passive utilization. For some topologies, capacitor soft-charging can be achieved through component sizing. However, many other topologies, such as the hybrid Dickson-derived circuits require a special switching scheme: split-phase operation. Detailed in [77], split-phase operation describes the introduction of sub-phases within the two main switching phases to ensure soft-charging of the flying capacitors through the output inductor. Without these additional switching states, large current spikes occur at phase transitions due to mismatched loop voltages. These hard-charging events have a negative impact on efficiency, passive utilization, and EMI performance.

4.1 Introduction

The inclusion of a relatively small inductance into an otherwise pure switched-capacitor converter (e.g., pure SC Dickson converter in Fig. 2.3) either at the low-side port of the

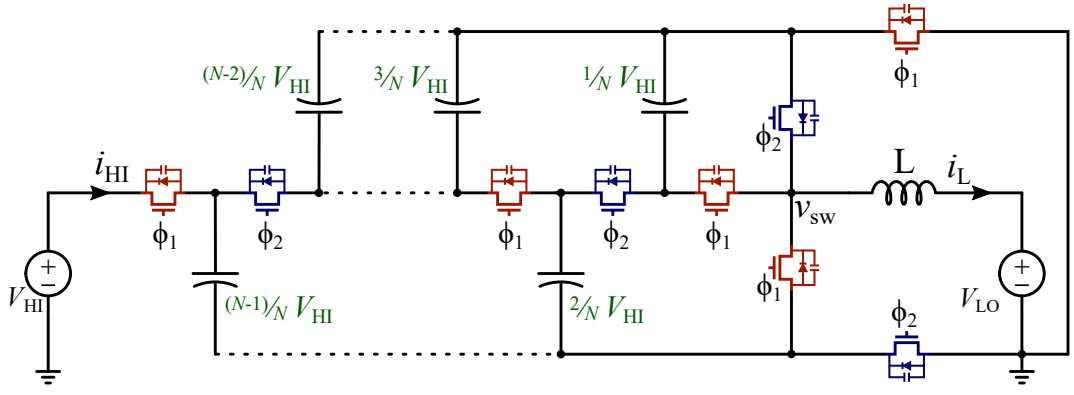


Figure 4.1: Schematic drawing of a hyrbid switched-capacitor Dickson converter.

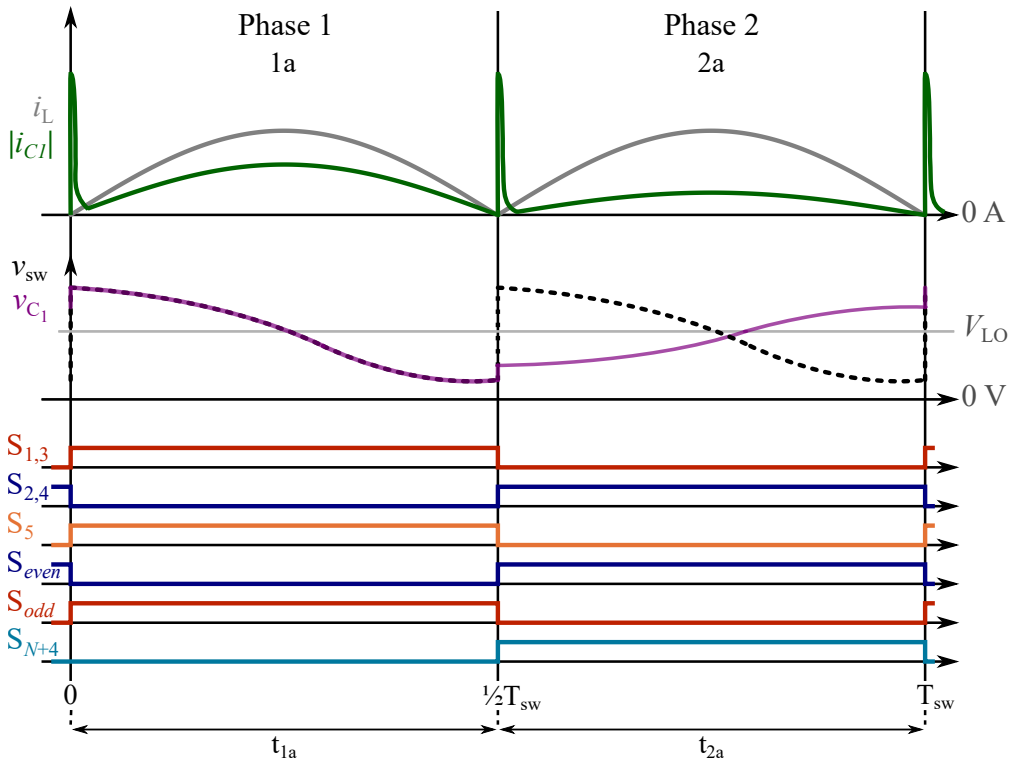


Figure 4.2: Example converter waveforms for a resonant even-N hybrid Dickson converter with two-phase operation. Capacitors C_1 and C_{N-1} are hard-charged, resulting in discontinuous capacitor voltages and high current pulses at phase transitions.

converter (for 'direct' topologies) or distributed in series with the flying capacitors (for 'indirect' topologies) [34, 53] serves to facilitate soft-charging of the flying capacitors [25, 41]. However, even with this modification, some topologies, such as the even-N hybrid Dickson converter, Fig. 4.1, still cannot achieve soft-charging with two-phase operation [77].

Hard-charging transitions incur large current spikes at phase transitions due to mismatched loop voltages and have a negative impact on efficiency, passive utilization, and EMI performance. These large current spikes – resultant from a voltage-mismatch across a capacitor C_1 at phase transitions – are illustrated in Fig. 4.2. To avoid flying capacitor hard-charging, split-phase operation can be utilized, wherein sub-phases are inserted within the primary switching phases to ensure matched loop voltages at phase transitions [25]. When capacitor voltages are consistent across phase transitions, as shown in Fig. 4.8, large dv/dt and di/dt transitions are reduced. However, achieving perfect voltage continuity is non-trivial and requires analysis of phase timings as they relate to each other and to the overall switching frequency.

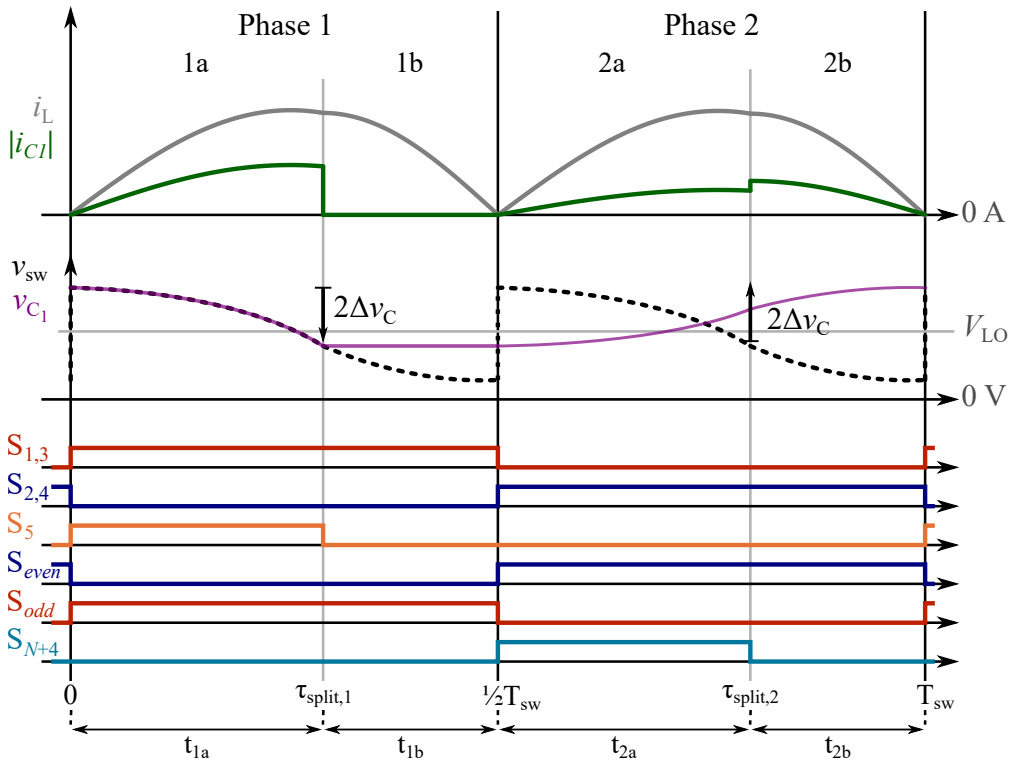


Figure 4.3: Example converter waveforms for a resonant hybrid Dickson converter with split-phase operation. Capacitors C_1 and C_{N-1} are soft-charged, resulting in continuous capacitor voltages and currents at phase transitions.

4.2 Resonant Split-Phase Switching

A methodology for analyzing circuit parameters in typical operation (i.e., no regulation or zero voltage switching phases) of the hybrid Dickson converter is described below based on [34, 83] and serves as the first step in the determination of regulation and ZVS phase timings, which are discussed in later chapters.

The general split-phase analysis analysis presented in this section is valid for step-up and step-down operation both at the resonant switching frequency and operation above resonance, and can also be extended to voltage-regulation of hybrid SC converters, which operate more similarly to pulse-width-modulated converters than to resonant converters. Therefore, we model both the high-side port and the low-side port as voltage sources of voltage V_{HI} and V_{LO}, respectively. Furthermore, we define N as the inherent conversion ratio of the SC network and M as the actualized conversion ratio (accounting for voltage regulation), where $V_{\text{HI}}/V_{\text{LO}} = M$. For the non-regulating case (assuming no losses) $M = N$. We then examine the switching states and charge flow through the circuit to determine important topological and operating parameters.

Even-N Hybrid Dickson Converter

Based on the general analysis presented in Chapter 3, a circuit topology requiring split-phase operation is analyzed here: the hybrid Dickson converter, Fig. 4.4. The analysis in [77] of the hybrid Dickson converter calculated split-phase timing (i.e., when to insert the secondary sub-phase) assuming a constant load current and neglecting any current ripple, which in certain applications may not be a sufficiently-precise approximation. A more thorough method incorporating both the inductor current ripple and capacitor voltage ripple into the split-phase timing calculations is presented in [71] using charge flow analysis to characterize the amount of voltage ripple on the flying capacitors. Furthermore, based on this method, an iteration-based process for determining split-phase timing was presented for a regulating hybrid SC accounting for non-linear inductor current and current ripple [84].

Per-Phase Equivalent Circuits

Fig. 4.5 shows the equivalent circuit configurations of an N:1 hybrid Dickson converter for primary phases — those which are present in conventional two-phase operation — Phase 1a and Phase 2a; and secondary sub-phases — those which are added for capacitor soft-charging — Phase 1b and Phase 2b. During primary phase Phase 1a, only odd-numbered switches in Fig 4.4 are ON: 'bridge' switches S_1 and S_3 in the half-bridges at the low-side port and 'string' switches S_{odd} in the series connected switches. Similarly for Phase 2a, only the even-numbered switches in Fig. 4.4 are ON. The 'b' sub-phases are utilized to satisfy Kirchoff's Voltage Law (KVL) at the transition from Phase 1a to Phase 2a and back to Phase 1a and prevent hard-charging of the flying capacitors. Establishing loop voltages immediately prior to and following a switching transition as continuous values prevents large step changes in voltage across the capacitors at the transition, which would impose large current transients due to capacitor hard-charging. By turning off one of the 'string' switches (S_5 in Phase 1 and S_{N+4} in Phase 2), thereby 'splitting' the primary phase into two sub-phases, the charging

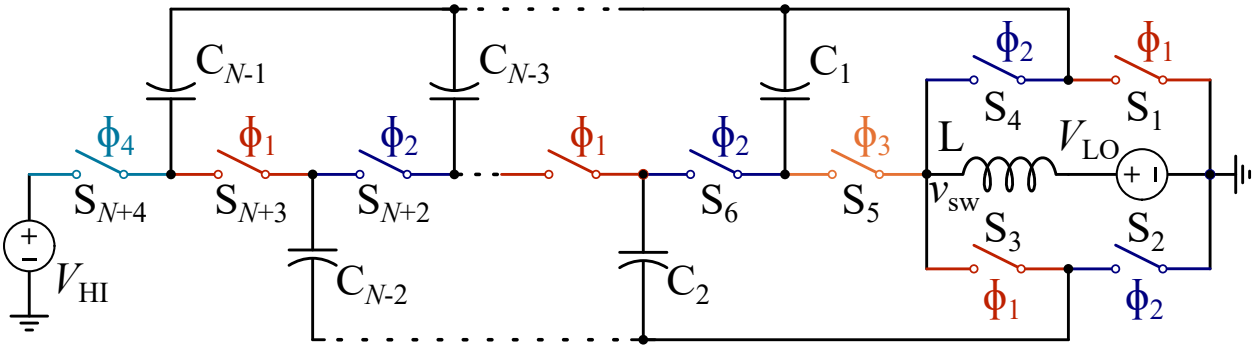
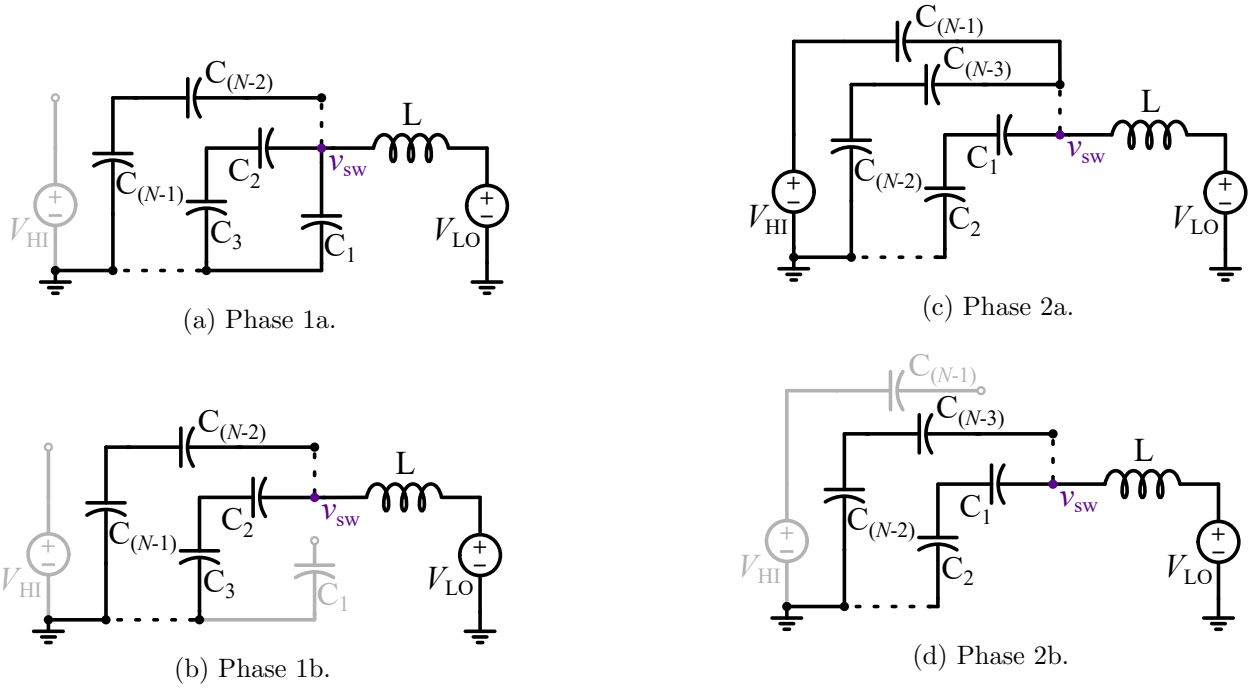


Figure 4.4: Schematic drawing of an even-N Dickson converter with switches labeled with their respective control phases. Switches S_1-S_4 are referred to as 'bridge' switches, S_5, S_{N+4} as 'split-phase' switches, and S_6-S_{N+3} as 'string' switches.



(a) Phase 1a.

(c) Phase 2a.

(b) Phase 1b.

(d) Phase 2b.

Figure 4.5: Equivalent circuits for each sub-phase of an N-to-1 Dickson converter (even N), with split-phase switching as ordered a-d: Phase 1a $\rightarrow$ Phase 1b $\rightarrow$ Phase 2a $\rightarrow$ Phase 2b.

or discharging of capacitor branches connected to the switch-node, v_{sw}, can be interrupted. Due to the difference in effective capacitance of one (or more) of the capacitor branches, the charge rates differ. Therefore, to enforce continuous capacitor voltages at switching transitions, the charge/discharge time of each branch must be controlled differently from conventional two-phase operation.

Determining the correct time at which to turn OFF the 'split-phase' switches, S_5 and S_{N+4}, requires an analysis of the capacitor voltages at phase transitions and therefore the charge-flow within each phase. While the charge-flow analysis for a step-down (N:1) and a step-up (1:N) converter is similar but with charge flowing in opposite directions, we refer here to only a step-down example to simplify the explanations. For an N:1 Dickson converter with number of capacitors: $N_{\text{C}} = N - 1$, the capacitance of each flying capacitor can be defined relative to a normalizing capacitance, C_0. A vector representation of each i-th capacitor, C_i, is given by (4.1) and (4.2).

$$C_i = C_0 \, c_i \tag{4.1}$$

$$\begin{aligned} \boldsymbol{c}_{[1\times N_{\mathrm{C}}]} &= \begin{bmatrix} \frac{C_1}{C_0} & \frac{C_2}{C_0} & \cdots & \frac{C_{N_{\mathrm{C}}}}{C_0} \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \end{aligned} \tag{4.2}$$

During each switching phase, j (where j corresponds to Phase 1, Phase 1a, Phase 2, Phase 2a, etc.), an L-C network is formed consisting of inductor, L, and an effective capacitance, $C_{\mathrm{e},j}$. This equivalent capacitance is formed at the switch-node by series and parallel combinations of flying capacitors. Once split-phase operation is incorporated, there are multiple possible capacitor ratios that can result in soft-charging, however, for the sake of simplicity — though the presented methodology is not contingent on this choice — this analysis assumes each flying capacitor is equal in capacitance, as shown in (4.2). The sub-phase equivalent capacitance, normalized to C_0, seen at the switch-node is defined by (4.3) with per-phase coefficient, κ_j (4.4).

Moreover, with the choice of equal capacitances, $C_i = C_0$, the effective equivalent capacitance at the switch-node is equal for both primary phases Phase 1a and Phase 2a as well as for both secondary 'b' sub-phases, Phase 1b and Phase 2b, (i.e., $C_{\mathrm{e},1a} = C_{\mathrm{e},2a}$ and $C_{\mathrm{e},1b} = C_{\mathrm{e},2b}$).

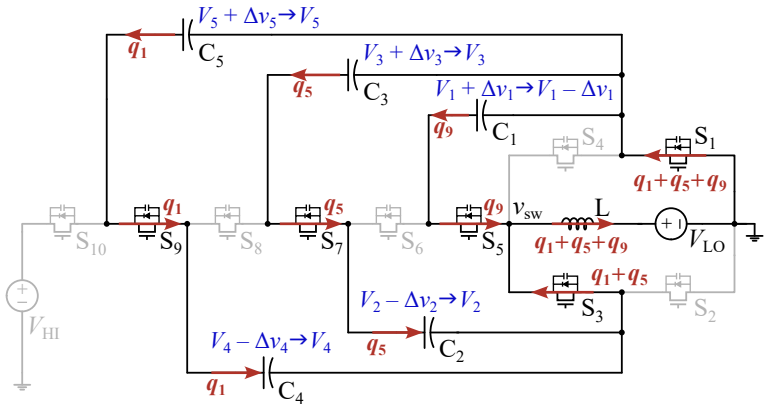
$$C_{\mathrm{e},j} = C_0\,\kappa_j. \tag{4.3}$$

$$\boldsymbol{\kappa}_{[N_{\mathrm{P}}\times 1]} = \begin{bmatrix} \frac{C_{\mathrm{e},1a}}{C_0} \\ \frac{C_{\mathrm{e},1b}}{C_0} \\ \frac{C_{\mathrm{e},2a}}{C_0} \\ \frac{C_{\mathrm{e},2b}}{C_0} \end{bmatrix} = \begin{bmatrix} \frac{N+2}{4} \\ \frac{N-2}{4} \\ \frac{N+2}{4} \\ \frac{N-2}{4} \end{bmatrix} \tag{4.4}$$

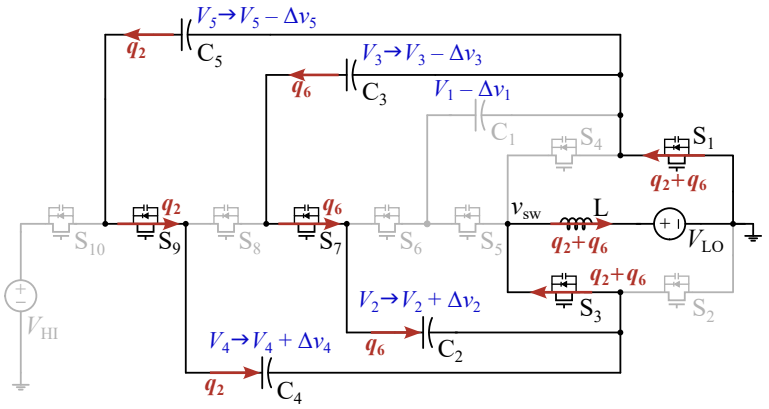
Charge Flow and Voltage Ripple Analysis

The voltage ripple on the flying capacitors, Δv_i, can be defined through charge flow analysis [42]. A normalized charge quantity, q_{HI}, is defined in (4.5) as the total amount of charge provided by the voltage source within a switching period T_{sw}, though a different normalized charge value may be used (e.g., normalizing to the charge through the low-side source). Assuming zero losses, the current I_{HI} supplied by the high-side voltage source, is equal to the low-side current divided by the conversion ratio, M. For this charge flow analysis, we assume that no charge flows through the parasitic output capacitances (C_{oss}) of any of the disabled switches. In general, the value of the flying capacitors is significantly larger than any parasitic device capacitance to justify this assumption. Fig. 4.6 illustrates the charge flow for an example $N = 6$ hybrid Dickson converter.

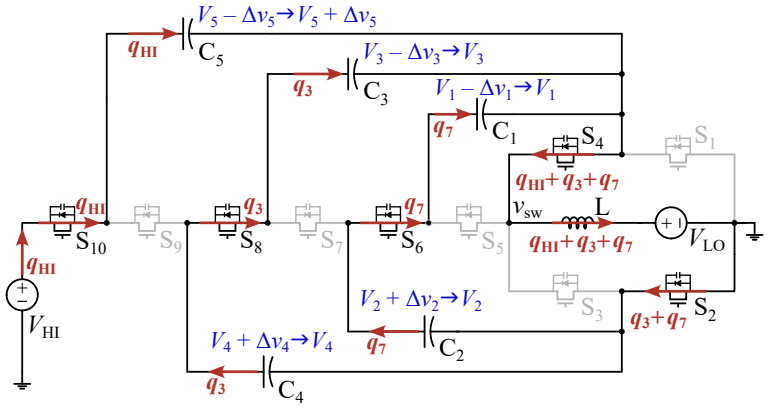
$$q_{\mathrm{HI}} = I_{\mathrm{HI}} \times T_{\mathrm{sw}} = (I_{\mathrm{LO}}/M) \times T_{\mathrm{sw}} \tag{4.5}$$



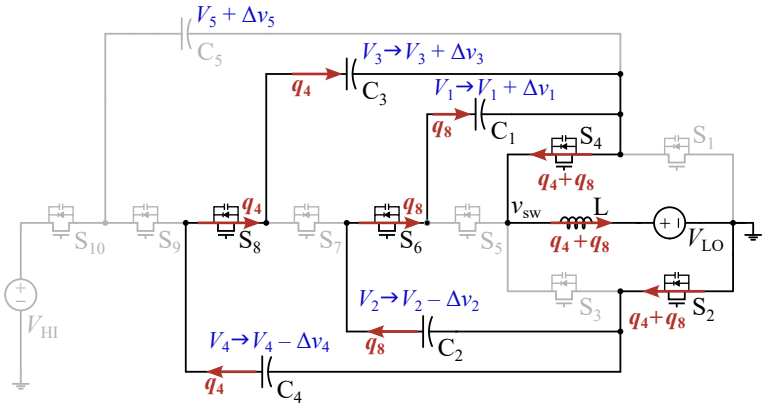
(a) Phase 1a: $t \in [0, t_{\text{split},1})$.



(b) Phase 1b: $t \in [t_{\text{split},1}, T_{\text{sw}}/2)$.



(c) Phase 2a $t \in [T_{\text{sw}}/2, t_{\text{split},2})$.



(d) Phase 2b: $t \in [t_{\text{split},2}, T_{\text{sw}})$.

Figure 4.6: Charge flow during each sub-phase of a 6:1 split-phase hybrid Dickson converter with capacitor voltages labeled for the start of Phases 1a and 1b, at the split-phase transition, and for the end of Phases 1b and 2b.

Because we have chosen to normalize charge quantities to the charge delivered by the high-side voltage supply, it can be easier to begin the charge flow analysis with a phase where the high-side voltage source is connected to the switch network. Therefore, we begin with Phase 2a (Fig. 4.6c), since this is the only circuit configuration in which the high-side source is connected. During this phase, q_{HI} must be flowing from the source and through flying capacitor C_5 (C_{N-1} for the general N:1 example).

To maintain charge balance and ensure steady-state operation, on flying capacitor C_5, the sum total charge quantity into C_5 must be zero. Because C_5 is disconnected in Phase 2b (Fig. 4.6d), no charge flows through it. Therefore the charge quantity that discharges C_5 in the totality of main phase Phase 1 (Phase 1a and Phase 1b together) must be equal to q_{HI}. However, the amount of charge in Phase 1a versus Phase 1b is as-of-yet unknown. Charge quantities q_1 and q_2 are then defined as the charge flowing through C_5 during Phase 1a and Phase 1b, respectively. The charge flowing through capacitors connected in series with C_5 can then be determined. For example, C_4 is charged by q_1 and q_2 during Phase 1a and Phase 1b, respectively. Similar to the definitions of q_1 and q_2, unknown charge quantities q_3 and q_4 are defined for the charge flow in C_4 during Phase 2a and Phase 2b, respectively. The remaining charge quantities flowing through each capacitor and to the low-side port through the inductor can be defined by maintaining charge balance on each capacitor over the entire switching period.

Once each charge quantity is defined, we can solve for the relative magnitudes of the charges and relate the charge flow to capacitor voltage ripple. We know that $q_{\text{HI}} = q_1 + q_2 = q_3 + q_4 = q_5 + q_6 = q_7 + q_8 = q_9$. Assuming each capacitor is equal is value (4.2), all branches which consist of two capacitors in series (i.e., $C_5 - C_4$, and $C_3 - C_2$ branches in Phase 1 and $C_4 - C_3$, and $C_2 - C_1$ branches in Phase 2) have an equal impedance. Another assumption made here and in [71, 83] is that because each corresponding sub-phase (i.e., Phase 1a/Phase 2a and Phase 1b/Phase 2b) has an equivalent impedance network at the switch-node, the converter can be operated with a 50% duty cycle for Phase 1 and Phase 2. Furthermore, if all capacitances equivalent, then the charge flow through a two-capacitor branch is *half* of the charge through a single-capacitor branch because the single capacitor has half of the impedance: $q_{\text{HI}}/2 = q_1 = q_2$, $q_{\text{HI}}/2 = q_3 = q_4$, $q_{\text{HI}}/2 = q_5 = q_6$, and $q_7 = q_8 = q_9/2 = q_{\text{HI}}/2$. This relationship is due to the parallel connection of each branch, therefore each branch has the same voltage imposed across it.

Finally, the relative charge flow through each capacitor C_i can be given by (4.6).

$$\boldsymbol{a}_{\mathrm{C}_{[N_\mathrm{P}\times N_\mathrm{C}]}} = \begin{bmatrix} \frac{q_{\mathrm{C},1a,1}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},1a,2}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},1a,N_\mathrm{C}}}{q_\mathrm{HI}} \\ \frac{q_{\mathrm{C},1b,1}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},1b,2}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},1b,N_\mathrm{C}}}{q_\mathrm{HI}} \\ \frac{q_{\mathrm{C},2a,1}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},2a,2}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},2a,N_\mathrm{C}}}{q_\mathrm{HI}} \\ \frac{q_{\mathrm{C},2b,1}}{q_\mathrm{HI}} & \frac{q_{\mathrm{C},2b,2}}{q_\mathrm{HI}} & \cdots & \frac{q_{\mathrm{C},2b,N_\mathrm{C}}}{q_\mathrm{HI}} \end{bmatrix} \tag{4.6}$$

$$= \begin{bmatrix} -1 & 1/2 & -1/2 & \cdots & 1/2 & -1/2 \\ 0 & 1/2 & -1/2 & \cdots & 1/2 & -1/2 \\ 1/2 & -1/2 & 1/2 & \cdots & -1/2 & 1 \\ 1/2 & -1/2 & 1/2 & \cdots & -1/2 & 0 \end{bmatrix}$$

The peak-to-peak capacitor ripple $2\Delta v_i$ can be defined for each capacitor using $\Delta q = C_i \Delta v_i$. Moreover in this case, because each flying capacitance is equal, and the magnitude of charge through each capacitor is equivalent to q_HI during each overall primary phase, the voltage ripple, Δv_i is given by (4.7) and is equivalent for every flying capacitor.

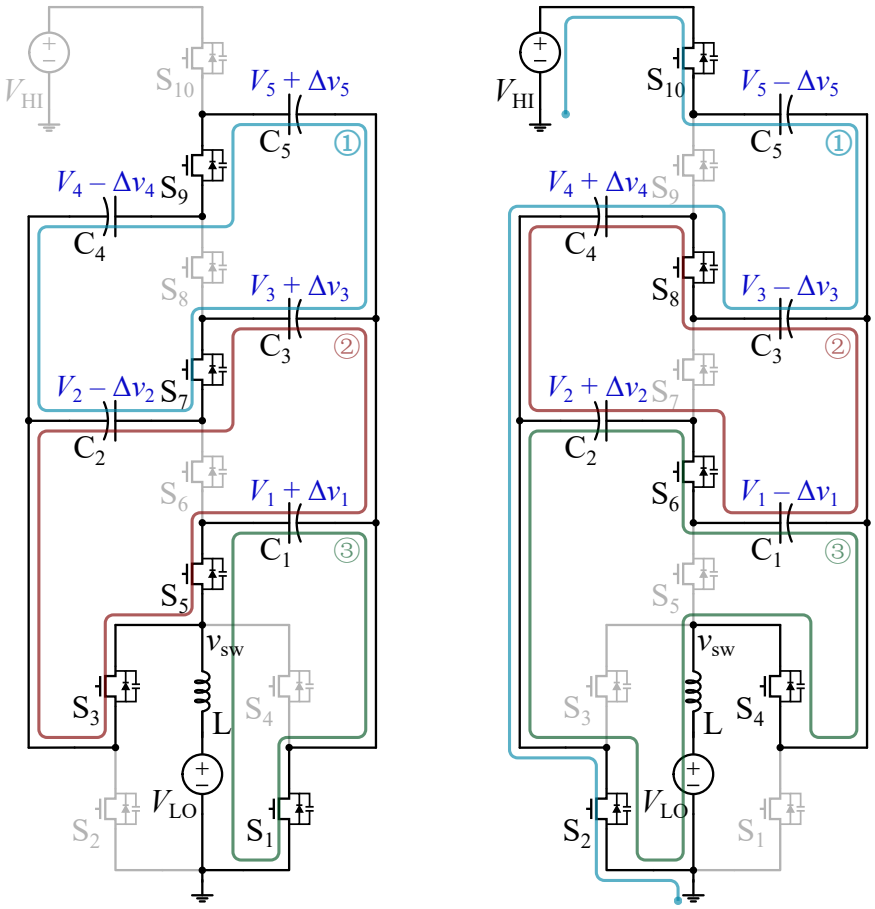
$$\frac{\Delta v_{\mathrm{pp},i}}{2} = \Delta v_i = \frac{q_\mathrm{HI} a_{\mathrm{C},ji}}{2C_i} \tag{4.7}$$

$$\Delta v_i = \frac{q_\mathrm{HI}}{2C_i} := \Delta v_\mathrm{c} \tag{4.8}$$

Capacitor Mid-range Voltages

The nominal DC voltage of the flying capacitors C_i without split-phase operation are derived in [27,77] to be $i \cdot \frac{V_\mathrm{HI}}{N}$ for $i = 1, 2, ...N-1$. However, when split-phase control is used, not every capacitor is charging/discharging over the full cycle and therefore, the nominal voltage on the flying capacitors deviates from the non-split-phase case as a function of load current. A 'mid-range' voltage, V_i, for each capacitor, C_i, can be defined [71] as the mid-point voltage about which the capacitor ripple is centered. This value may be dependent on loading conditions and is distinct from the time-averaged dc voltage which can deviate from the ripple center-point in multi-phase converters, including split-phase converters. Figs. 4.6a and 4.6b, 4.6c and 4.6d show the circuit configurations and capacitor voltages for the beginning and end of each overall phase as well as the capacitor voltages at the time of the 'split'.

Per the charge flow analysis above, odd-numbered capacitors C_1, C_3, and C_5 charge during Phase 2 and discharge during Phase 1. Therefore, during Phase 1, C_{odd} voltages decrease from $V_i + \Delta v_i$ to $V_i - \Delta v_i$, and vice-versa for Phase 2. Even-numbered capacitors C_2, and C_4 ripple similarly but with opposite polarity. These 'start' and 'end' capacitor voltages are labeled in Fig. 4.6. Correct split-phase operation requires that KVL is satisfied when transitioning between the two primary phases resulting in soft-charging of the flying capacitors. Loop



(a) Phase 1. (b) Phase 2.

Figure 4.7: Illustrated KVL loops with capacitor voltages labeled for the beginning of each phase. These KVL relationships are used to determine the mid-range capacitor voltages which satisfy soft-charging conditions.

voltage equations (illustrated in Fig. 4.7) for the start (i.e., at the transition into a phase) of Phase 1 and Phase 2 are given by:

$$\begin{cases} (V_5 + \Delta v_5) - (V_4 - \Delta v_4) - (V_3 + \Delta v_3) + (V_2 - \Delta v_2) = 0 \\ (V_3 + \Delta v_3) - (V_2 - \Delta v_2) - (V_1 + \Delta v_1) = 0 \\ (V_1 + \Delta v_1) = v_{sw} \end{cases} \tag{4.9}$$

and

$$\begin{cases} V_{HI} - (V_5 - \Delta v_5) - (V_4 + \Delta v_4) + (V_3 + \Delta v_3) = 0 \\ (V_4 + \Delta v_4) - (V_3 - \Delta v_3) - (V_2 + \Delta v_2) + (V_1 - \Delta v_1) = 0 \\ (V_2 + \Delta v_2) - (V_1 - \Delta v_1) = v_{sw} \end{cases} \tag{4.10}$$

respectively. Moreover, we see that the charge flow into the inductor during Phase 1 ($q_1 + q_2 + q_5 + q_6 + q_9 = 2q_{\text{HI}}$) and Phase 2 ($q_{\text{HI}} + q_3 + q_4 + q_7 + q_8 = 2q_{\text{HI}}$) is equal. Again. under the assumption that we operate Phase 1 and Phase 2 with equal timing (50%), we can assume that for steady-state operation, the switch-node voltage, v_{sw}, and current, i_{L}, for Phase 1 and 2 operate equivalently, starting and ending at the same values with the same wave-shape. Furthermore, this operating condition results in the lowest rms current value in the inductor [34]. Consequently, v_{sw} is equal at the start (and end) of each total phase.

This set of phase-start KVL equations can be re-written in the form of (4.11) and (4.12). The **A** and **b** matrices for an $N = 6$ Dickson converter are given by (4.13) and (4.14). The corresponding matrices for an $N = 8$ Dickson converter are given in Appendix A. Expanding to any even-N Dickson converter and solving for the mid-range voltages yields (4.15)[1].

$$\mathbf{A}_N \vec{v} = \vec{b}_N \tag{4.11}$$

$$\vec{v} = [V_1, V_2, V_3, ...V_{N-1}]^T \tag{4.12}$$

$$\mathbf{A}_6 = \begin{bmatrix} 0 & 1 & -1 & -1 & 1 \\ -1 & -1 & 1 & 0 & 0 \\ 1 & -1 & -1 & 1 & 0 \\ 0 & 0 & 1 & -1 & -1 \\ -2 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{4.13}$$

$$\mathbf{b}_6 = \begin{bmatrix} 0 \\ -\Delta v_{\text{c}} \\ 0 \\ \Delta v_{\text{c}} - V_{\text{HI}} \\ -\Delta v_{\text{c}} \end{bmatrix} \tag{4.14}$$

$$V_i = \frac{iV_{\text{HI}}}{N} + \Delta v_{\text{c}}\Big(1 - \frac{2i}{N}\Big) \qquad \text{for } i = 1,2,...\text{N-1} \tag{4.15}$$

Split-Phase Timing

Using the mid-range voltages, the switch-node voltage in Fig. 4.8 can be characterized and the duration of each sub-phase can be determined. Eqn. 4.16 describes the switch-node voltage at the times corresponding to $t = 0$, $t = \tau_{\text{split,1}}$, and $t = T_{\text{sw}}/2$ in Figs. 4.6a - 4.6b, respectively, as well as in Fig. 4.8. Generalized equations for the switch-node voltage for an even-N hybrid Dickson with split-phase control are found (4.17) by substituting (4.15) into (4.16).

[1] If the switching sequence is Phase 1b→Phase 1a→Phase 2b→Phase 2a instead of Phase 1a→Phase 1b→Phase 2a→Phase 2b the polarity of the Δv_{c} term is reversed.

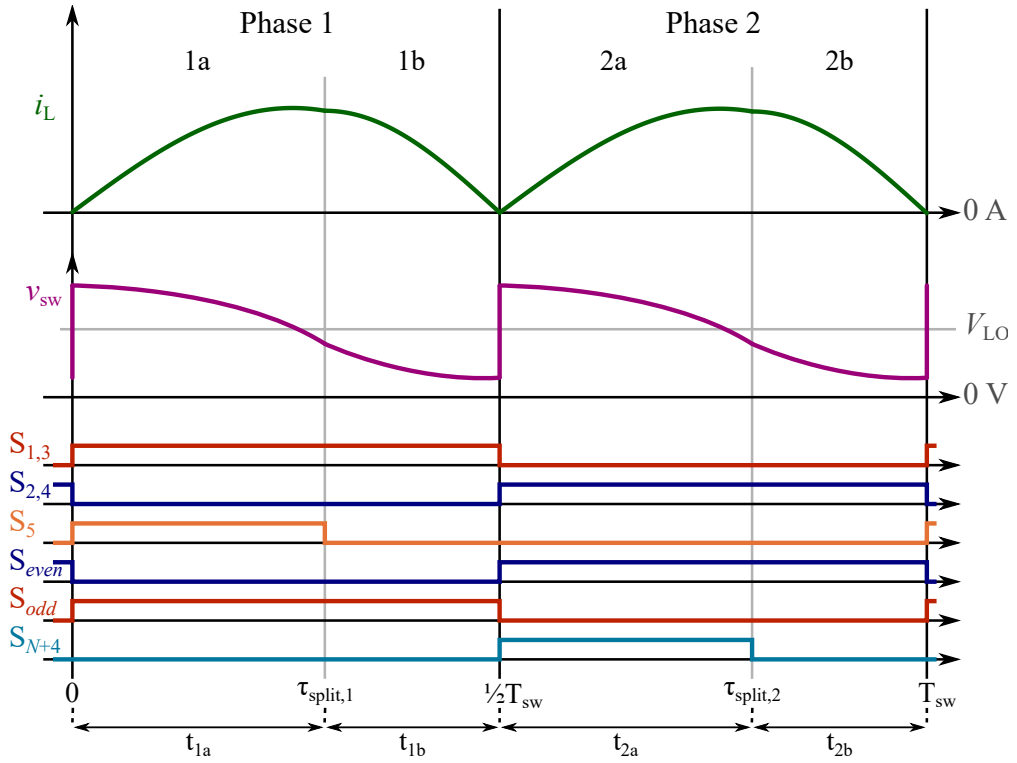


Figure 4.8: Illustrated inductor current and switch-node voltage for an even-N resonant Dickson with split-phase control.

$$\begin{cases} v_{sw}(0) = v_{C_1}(0) \\ v_{sw}(\tau_{split,1}) = v_{C_1}(\tau_{split,1}) \\ v_{sw}(\frac{T_{sw}}{2}) = v_{C_3}(\frac{T_{sw}}{2}) - v_{C_2}(\frac{T_{sw}}{2}) \end{cases} \tag{4.16}$$

$$\begin{cases} v_{sw}(0) = \frac{V_{HI}}{N} + \frac{2\Delta v_c}{N}(N-1) \\ v_{sw}(\tau_{split,1}) = \frac{V_{HI}}{N} - \frac{2\Delta v_c}{N} \\ v_{sw}(\frac{T_{sw}}{2}) = \frac{V_{HI}}{N} - \frac{2\Delta v_c}{N}(N+1) \end{cases} \tag{4.17}$$

When operating *at resonance*, the inductor current begins at 0 A at the start of Phase 1a ($t = 0$) and the switch-node voltage is sinusoidal with a DC offset of value V_{HI}. Using the expressions from (4.17) and shifting by the DC offset, an equation for the sinusoidal shape of the switch-node voltage can be written:

$$v_{sw}(\tau_{split,1}) - \frac{V_{HI}}{N} = \left(v_{sw}(0) - \frac{V_{HI}}{N}\right) cos(\theta_{1a}) \tag{4.18}$$

The duration of this phase configuration, t_{1a}, is determined by (4.19) and the substitution of (4.17) into (4.18). Similarly, duration of Phase 1b is given by (4.20) and (4.21). Assuming

that Phase 1 and 2 operate equivalently, the resonant period for split-phase operation is twice the sum of the time duration of the 'a' and 'b" phases, (4.22).

$$\theta_{1a} = t_{1a}\omega_{1a} \quad \text{where} \quad \omega_{1a} = (\sqrt{LC_{e,1a}})^{-1} \tag{4.19}$$

$$v_{sw}(\tau_{split,1}) - \tfrac{V_{HI}}{N} = \Big(v_{sw}(\tfrac{T_{sw}}{2}) - \tfrac{V_{HI}}{N}\Big) cos(\theta_{1b}) \tag{4.20}$$

$$\theta_{1b} = t_{1b}\omega_{1b} \quad \text{where} \quad \omega_{1b} = (\sqrt{LC_{e,1b}})^{-1} \tag{4.21}$$

$$\begin{aligned} T_{sw} &= 2(t_{1a} + t_{1b}) \\ &= 2\sqrt{\tfrac{LC_0}{4}}\left[\sqrt{N+2}cos^{-1}(\tfrac{-1}{N-1}) + \sqrt{N-2}cos^{-1}(\tfrac{1}{N+1})\right] \end{aligned} \tag{4.22}$$

Mid-range Voltages: $N = 4$ and $N = 8$ Hybrid Dickson Converters

Voltage loop matrices for a 4-to-1 and an 8-to-1 split-phase hybrid Dickson converter are given by (4.23) and (4.24), and (4.25) and (4.26), respectively. To determine the mid-range flying capacitor voltages, (4.11) can be solved using these matrices leading to the result in (4.15).

$$\mathbf{A}_4 = \begin{bmatrix} -1 & -1 & 1 \\ 1 & -1 & -1 \\ -2 & 1 & 0 \end{bmatrix} \tag{4.23}$$

$$\mathbf{b}_4 = \begin{bmatrix} -\Delta v_c \\ \Delta v_c - V_{HI} \\ -\Delta v_c \end{bmatrix} \tag{4.24}$$

$$\mathbf{A}_8 = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 & -1 & 1 \\ 0 & 1 & -1 & -1 & 1 & 0 & 0 \\ -1 & -1 & 1 & 0 & 0 & 0 & 0 \\ 1 & -1 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & -1 \\ -2 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.25}$$

$$\mathbf{b}_8 = \begin{bmatrix} 0 \\ 0 \\ -\Delta v_c \\ 0 \\ 0 \\ \Delta v_c - V_{HI} \\ -\Delta v_c \end{bmatrix} \tag{4.26}$$

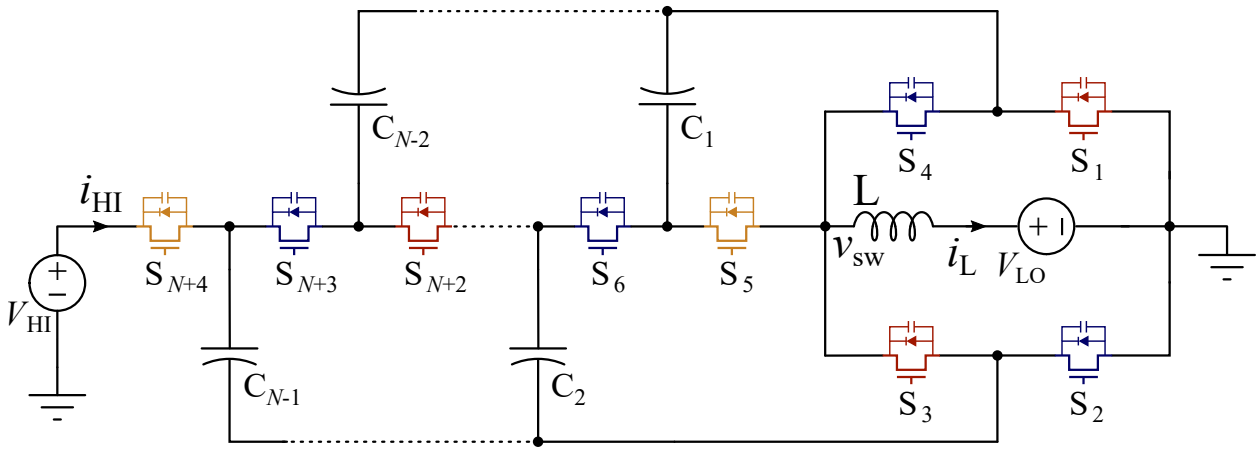


Figure 4.9: Schematic drawing of an odd-N Dickson converter with switches labeled with their respective control phases. Switches S_1-S_4 are referred to as 'bridge' switches, S_5, S_{N+4} as 'split-phase' switches, and S_6-S_{N+3} as 'string' switches.

Odd-N Hybrid Dickson Converter Operation

An odd-N hybrid Dickson converter (Fig. 4.9) can achieve soft-charging of the flying capacitors with standard two-phase operation (no split-phases necessary) by choosing specific capacitance ratios [25]. However, if all capacitors are selected to have equal capacitance such as for the even-N case, a similar analysis to the one presented above can be conducted resulting in the following mid-range voltages. For a split-phase odd-N Dickson converter, only Phase 1 requires split-phase because in Phase 2, each capacitor branch has two series-connected capacitors, whereas in Phase 1 there are two branches with a singular capacitor and $\frac{(N-3)}{2}$ branches with two capacitors in series. Split-phase operation is implemented by disconnecting both single-capacitor branches within Phase 1 to ensure capacitor soft-charging at the transition into Phase 2. Illustrated waveforms are shown in Fig. 4.10 showing the asymmetry between the two phases.

The per-phase equivalent circuits are shown in Fig. 4.11 with effective capacitances given by (4.27). Charge flow analysis (Fig. 4.12) for the odd-N Dickson converter is similar to that for the the odd-N Dickson converter. The KVL equations used for determining the capacitor mid-range voltages are given in (4.28) for an $N = 5$ case. Because the odd-N hybrid Dickson converter does not have two symmetric phases, due to only Phase 1 requiring split-phase operation, equating the switch-node voltage at the start (or end) of each phase as was done for the even-N hybrid Dickson converter is invalid. Instead, the non-split-phase Phase 2 is leveraged to relate capacitor voltages to the low-side voltage. Because Phase 2 does not have a sub-phase, it operates as a typical half-wave resonant circuit, wherein the inductor current and switch-node voltage (and inductor voltage) are purely sinusoidal for the full phase duration. Therefore, a zero-crossing of the inductor voltage occurs at the mid-point of Phase 2. Also at the mid-point of each sub-phase, each connected capacitor is at its mid-range voltage.

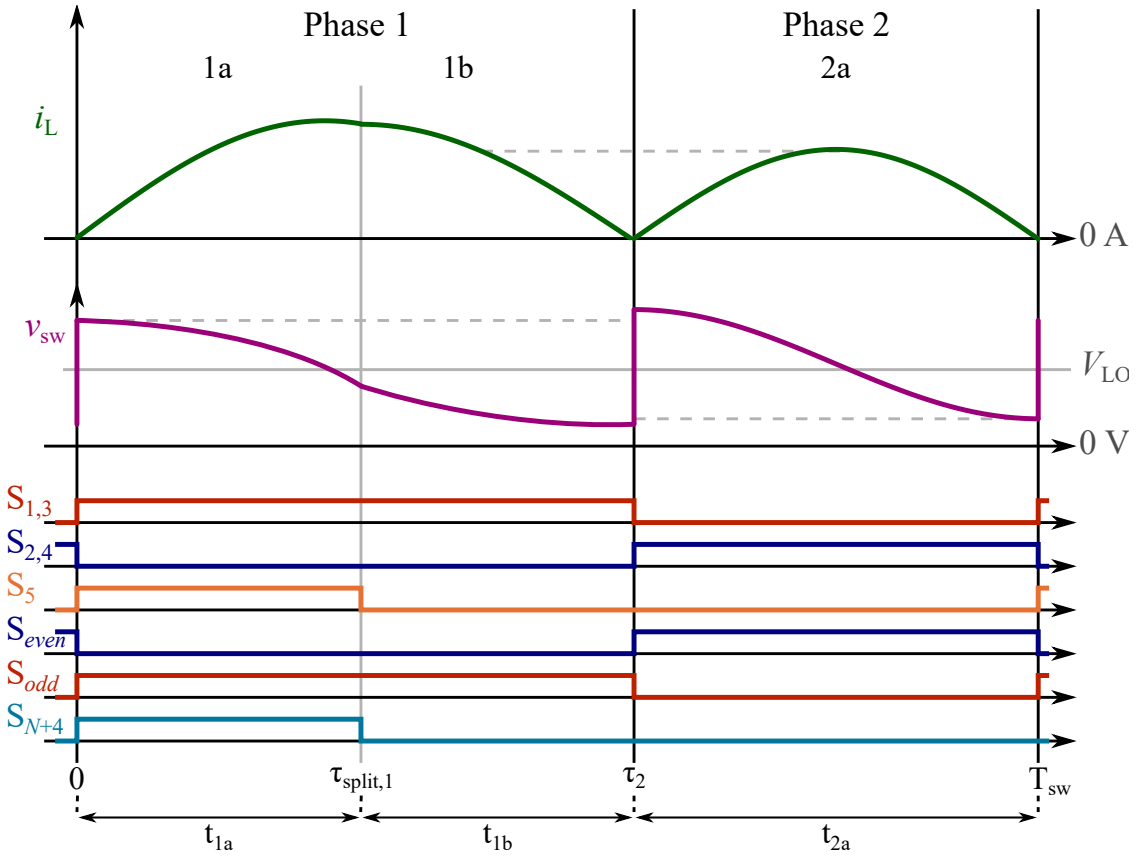
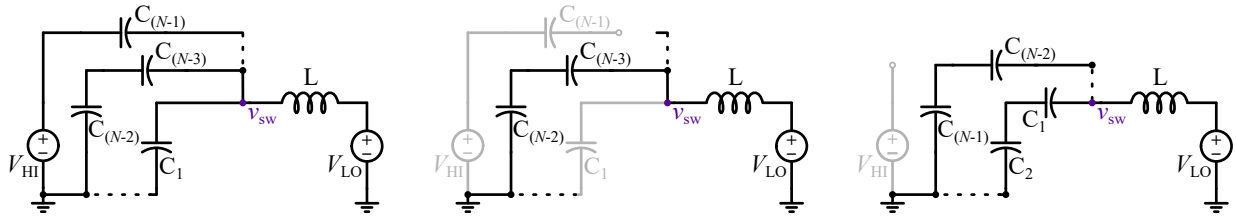


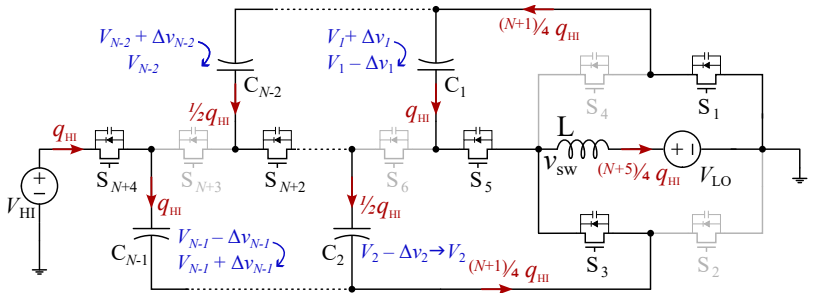
Figure 4.10: Illustrated waveforms for the resonant split-phase odd-N Dickson converter, showing only Phase 1 requiring split-phase operation.



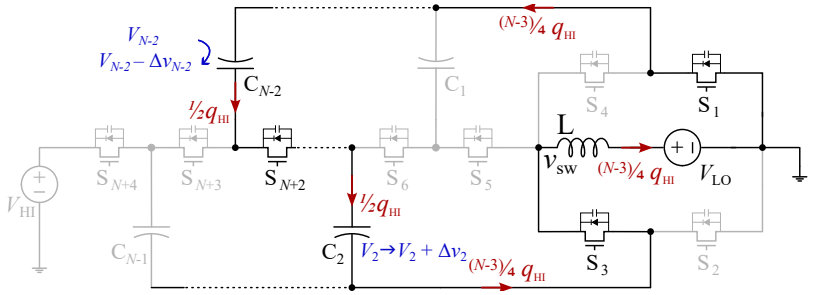
(a) Phase 1a. (b) Phase 1b. (c) Phase 2.

Figure 4.11: Equivalent circuits for each sub-phase of an N-to-1 Dickson converter (odd N), with split-phase switching as ordered a-c: Phase 1a → Phase 1b → Phase 2.

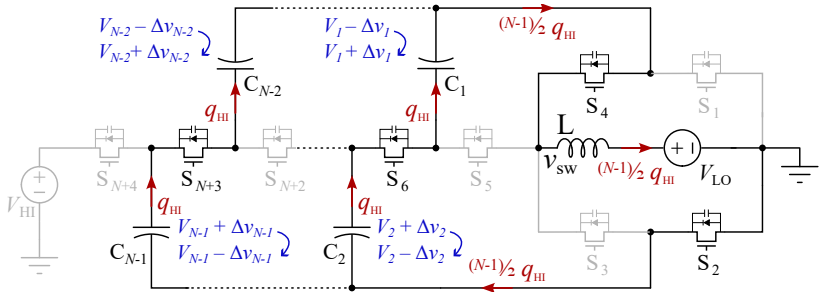
$$\boldsymbol{\kappa}_{[N_P \times 1]} = \begin{bmatrix} \frac{C_{e,1a}}{C_0} \\ \frac{C_{e,1b}}{C_0} \\ \frac{C_{e,2a}}{C_0} \end{bmatrix} = \begin{bmatrix} \frac{N+5}{4} \\ \frac{N-3}{4} \\ \frac{N-1}{4} \end{bmatrix}_{N_{odd}} \tag{4.27}$$



(a) Phase 1a.



(b) Phase 1b.



(c) Phase 2.

Figure 4.12: Charge flow during each sub-phase of a 5:1 split-phase hybrid Dickson converter with capacitor voltages labeled for the start of Phases 1a and 1b, at the split-phase transition, and for the end of Phases 1b and 2.

$$\begin{cases} V_{\text{HI}} - (V_4 - \Delta v_4) - (V_3 + \Delta v_3) + (V_2 - \Delta v_2) = 0 \\ (V_3 + \Delta v_3) - (V_2 - \Delta v_2) - (V_1 + \Delta v_1) = 0 \\ (V_4 + \Delta v_4) - (V_3 - \Delta v_3) - (V_2 + \Delta v_2) + (V_1 - \Delta v_1) = 0 \\ V_2 - V_1 - \frac{V_{\text{HI}}}{N} = 0 \end{cases} \tag{4.28}$$

$$\mathbf{A}_5 = \begin{bmatrix} 0 & 1 & -1 & -1 \\ -1 & -1 & 1 & 0 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 0 & 0 \end{bmatrix} \tag{4.29}$$

$$\mathbf{b}_5 = \begin{bmatrix} \Delta v_\mathrm{c} - V_\mathrm{HI} \\ -\Delta v_\mathrm{c} \\ 0 \\ \\ -\frac{V_\mathrm{HI}}{N} \end{bmatrix} \tag{4.30}$$

A relationship between capacitor mid-range voltages and the low-side voltage can be expressed as a final KVL constraint. The capacitor mid-range voltages for a switching sequence of Phase 1a → Phase 1b → Phase 2a → Phase 1a is given in (4.31). If the order of Phases 1a and 1b is swapped, the Δv_c term in (4.31) is then of negative polarity.

$$V_i = \frac{iV_\mathrm{HI}}{N} - \Delta v_\mathrm{c}\left(\frac{N-2i+(-1)^i}{N+1}\right) \quad \text{for } i = 1,2,...\text{N-1} \tag{4.31}$$

The value of the switch-node voltage at each phase transition is given by (4.32). Following the same procedure as for the even-N hybrid Dickson converter, phase timings for Phase 1a, Phase 1b, and Phase 2 are found by (4.33)-(4.35).

$$\begin{cases} v_\mathrm{sw}(0) = \frac{V_\mathrm{HI}}{N} + \frac{2\Delta v_\mathrm{c}}{N+1}(N-1) \\ v_\mathrm{sw}(\tau_\mathrm{split,1}) = \frac{V_\mathrm{HI}}{N} - \frac{4\Delta v_\mathrm{c}}{N+1} \\ v_\mathrm{sw}(\tau_2^-) = \frac{V_\mathrm{HI}}{N} - \frac{2\Delta v_\mathrm{c}}{N+1}(N+3) \\ v_\mathrm{sw}(\tau_2^+) = \frac{V_\mathrm{HI}}{N} + 2\Delta v_\mathrm{c} \\ v_\mathrm{sw}(T_\mathrm{sw}) = \frac{V_\mathrm{HI}}{N} - 2\Delta v_\mathrm{c} \end{cases} \tag{4.32}$$

$$t_2 = \frac{\pi}{\omega_2} \tag{4.33}$$

$$t_\mathrm{1a} = \frac{1}{\omega_\mathrm{1a}} \cdot cos^{-1}\left(\frac{2}{N-1}\right) \tag{4.34}$$

$$t_\mathrm{1a} = \frac{1}{\omega_\mathrm{1b}} \cdot cos^{-1}\left(\frac{2}{N+3}\right) \tag{4.35}$$

Furthermore, the resonant switching period is defined as (4.36).

$$T_\mathrm{sw} = t_\mathrm{1a} + t_\mathrm{1b} + t_2 = \sqrt{\tfrac{LC_0}{4}}\left(\sqrt{N-5}\,cos^{-1}\left(\frac{2}{N+1}\right) + \sqrt{N-3}\,cos^{-1}\left(\frac{2}{N+3}\right) + \pi\sqrt{N-1}\right) \tag{4.36}$$

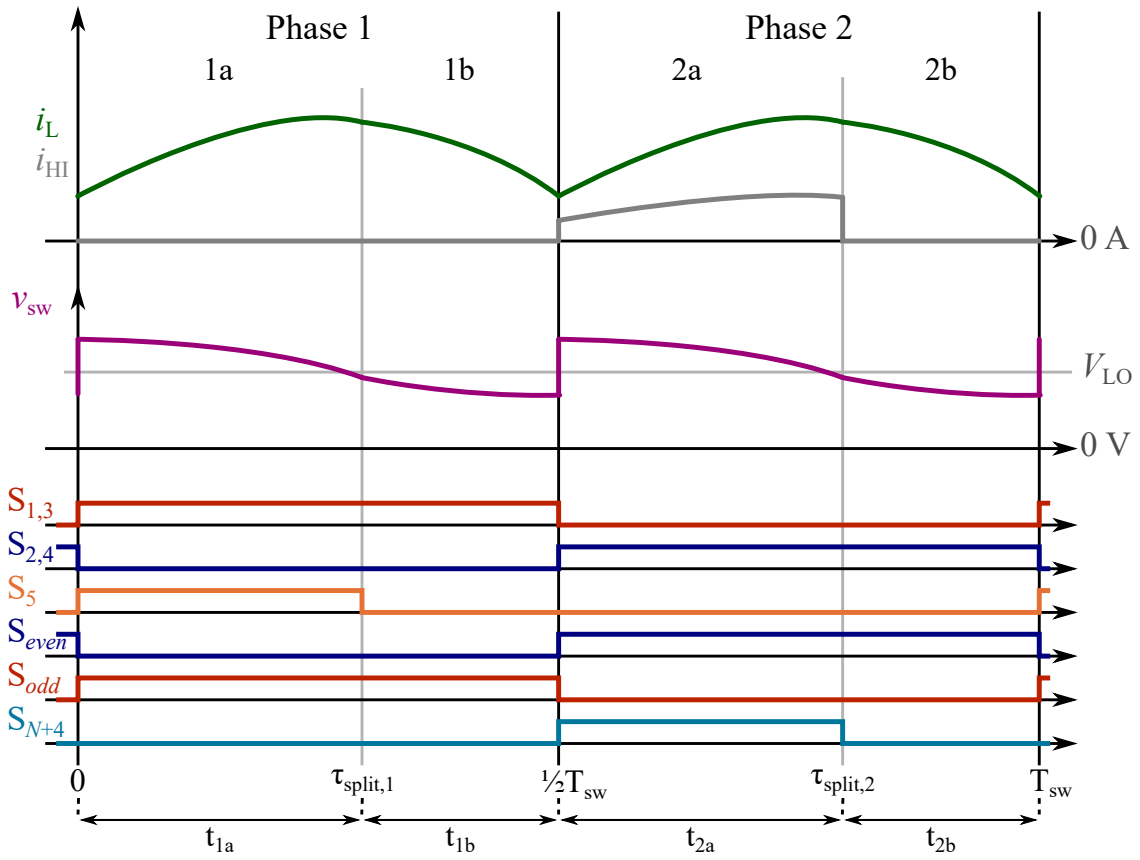


Figure 4.13: Illustrated waveforms for the split-phase even-N Dickson converter, operating at a switching frequency above resonance.

4.3 Above Resonant Split-Phase Switching

Prior work [46,48,52,54] demonstrated that operating some ReSC converters above resonance (i.e., switching faster than the switching frequency which corresponds to ZCS operation) can significantly improve overall converter efficiency through a reduction in rms currents and associated conduction losses, despite increases in relative switching loss. However, for those topologies which require split-phase switching, the phase timings need to be re-evaluated based on the switching frequency and relative current and voltage ripples. Example waveforms for a split-phase even-N Dickson converter operating above resonance (evident by the inductor current, i_L not resonating down to 0 A) are shown in Fig. 4.13.

While the analysis in [77] determines the phase timings based on a small-ripple assumption which correlates to switching much faster than resonant operation, the analysis presented in the prior section of this chapter assumes *at* resonant operation. For the switching frequencies between these two extremes (i.e., $1 < \Gamma < \infty$), determining the split-phase timings requires the use of computer-aided iterative solvers as described in [84].

Table 4.1 lists the time domain expressions that describe the inductor voltage and current

at each phase transition for Phase 1 of an even-N hybrid Dickson converter. Phase 2 for the even-N hybrid Dickson converter is analogous to Phase 1, whereas Phase 2 for the odd-N hybrid Dickson converter is more simplistic since split-phase is not required (Table 4.2). The duration of each phase is dependent on the equivalent L-C product as well as the starting condition. At resonance, we know that the inductor current is 0 A, however when operating above resonance, the initial inductor current is an unknown value. Moreover the inductor voltage at each transition has an analytical expression, but the voltage is dependent on the voltage ripple, which is itself dependent on the switching frequency. Using the expressions in Table 4.1 or 4.2, as well as the relationship between the switching frequency and the voltage ripple (4.37), timings for each phase can be determined. *Note that for odd-N hybrid Dickson converters, $t_{2a} = t_2$ and $t_{2b} = 0$ in (4.37).*

$$\Delta v_{\mathrm{c}} = \frac{I_{\mathrm{HI}}}{2C_0 f_{\mathrm{sw}}} = \frac{I_{\mathrm{HI}}}{2C_0 \Gamma f_{\mathrm{sw},0}} = \frac{I_{\mathrm{HI}}}{2C_0}(t_{1\mathrm{a}} + t_{1\mathrm{b}} + t_{2a} + t_{2b}) \tag{4.37}$$

Table 4.1: Time-Domain Circuit Dynamics Expressions - Phase 1/2 even-N hybrid Dickson Converter

Parameter	Expression	Known Value
$i_{\mathrm{L}}(0)$	$i_{\mathrm{L}}(0)$	
$v_{\mathrm{L}}(0)$	$\frac{2\Delta v_{\mathrm{c}}}{N} \cdot (N-1)$	$= \frac{2\Delta v_{\mathrm{c}}}{N} \cdot (N-1)$
$i_{\mathrm{L}}(\tau_{\mathrm{sp},1})$	$i_{\mathrm{L}}(0)cos(\omega_{1\mathrm{a}} t_{1\mathrm{a}}) + \frac{2\Delta v_{\mathrm{c}} \cdot (N-1)}{N}\sqrt{\frac{C_{\mathrm{e},1\mathrm{a}}}{L}} sin(\omega_{1\mathrm{a}} t_{1\mathrm{a}})$	
$v_{\mathrm{L}}(\tau_{\mathrm{sp},1})$	$\frac{2\Delta v_{\mathrm{c}} \cdot (N-1)}{N} cos(\omega_{1\mathrm{a}} t_{1\mathrm{a}}) - \sqrt{\frac{L}{C_{\mathrm{eq},1\mathrm{a}}}} i_L(0) sin(\omega_{1\mathrm{a}} t_{1\mathrm{a}})$	$= -\frac{2\Delta v_{\mathrm{c}}}{N}$
$i_{\mathrm{L}}(T_{\mathrm{sw}}/2)$	$i_{\mathrm{L}}(\tau_{\mathrm{sp},1}) cos(\omega_{1\mathrm{b}} t_{1\mathrm{b}}) + -(\frac{2\Delta v_{\mathrm{c}}}{N})\sqrt{\frac{C_{\mathrm{e},1\mathrm{b}}}{L}} sin(\omega_{1\mathrm{b}} t_{1\mathrm{b}})$	$= i_{\mathrm{L}}(0)$
$v_{\mathrm{L}}(T_{\mathrm{sw}}/2)$	$-(\frac{2\Delta v_{\mathrm{c}}}{N}) cos(\omega_{1\mathrm{b}} t_{1\mathrm{b}}) - \sqrt{\frac{L}{C_{\mathrm{eq},1\mathrm{b}}}} i_L(\tau_{\mathrm{sp},1}) sin(\omega_{1\mathrm{b}} t_{1\mathrm{b}})$	$= -\frac{2\Delta v_{\mathrm{c}}}{N} \cdot (N+1)$

Table 4.2: Time-Domain Circuit Dynamics Expressions - Phase 1 and 2 odd-N hybrid Dickson Converter

Parameter	Expression	Known Value
$i_{\mathrm{L}}(0)$	$i_{\mathrm{L}}(0)$	
$v_{\mathrm{L}}(0)$	$\frac{2\Delta v_{\mathrm{c}}}{(N+1)} \cdot (N-1)$	$= \frac{2\Delta v_{\mathrm{c}}}{(N+1)} \cdot (N-1)$
$i_{\mathrm{L}}(\tau_{\mathrm{sp},1})$	$i_{\mathrm{L}}(0)cos(\omega_{1\mathrm{a}}t_{1\mathrm{a}}) + \frac{2\Delta v_{\mathrm{c}} \cdot (N-1)}{(N+1)}\sqrt{\frac{C_{\mathrm{e},1\mathrm{a}}}{L}}sin(\omega_{1\mathrm{a}}t_{1\mathrm{a}})$	
$v_{\mathrm{L}}(\tau_{\mathrm{sp},1})$	$\frac{2\Delta v_{\mathrm{c}} \cdot (N-1)}{(N+1)}cos(\omega_{1\mathrm{a}}t_{1\mathrm{a}}) - \sqrt{\frac{L}{C_{\mathrm{eq},1\mathrm{a}}}}i_L(0)sin(\omega_{1\mathrm{a}}t_{1\mathrm{a}})$	$= -\frac{4\Delta v_{\mathrm{c}}}{(N+1)}$
$i_{\mathrm{L}}(\tau_2^-)$	$i_{\mathrm{L}}(\tau_{\mathrm{sp},1})cos(\omega_{1\mathrm{b}}t_{1\mathrm{b}}) + -\frac{4\Delta v_{\mathrm{c}}}{(N+1)}\sqrt{\frac{C_{\mathrm{e},1\mathrm{b}}}{L}}sin(\omega_{1\mathrm{b}}t_{1\mathrm{b}})$	$i_{\mathrm{L}}(0)$
$v_{\mathrm{L}}(\tau_2^-)$	$-\frac{4\Delta v_{\mathrm{c}}}{(N+1)}cos(\omega_{1\mathrm{b}}t_{1\mathrm{b}}) - \sqrt{\frac{L}{C_{\mathrm{eq},1\mathrm{b}}}}i_L(0)sin(\omega_{1\mathrm{b}}t_{1\mathrm{b}})$	$= -\frac{2\Delta v_{\mathrm{c}}}{(N+1)} \cdot (N+3)$
$i_{\mathrm{L}}(\tau_2^+)$	$i_{\mathrm{L}}(0)$	
$v_{\mathrm{L}}(\tau_2^+)$	$2\Delta v_{\mathrm{c}}$	$= 2\Delta v_{\mathrm{c}}$
$i_{\mathrm{L}}(T_{\mathrm{sw}})$	$i_{\mathrm{L}}(0)cos(\omega_2 t_2) + -(2\Delta v_{\mathrm{c}})\sqrt{\frac{C_{\mathrm{e},2}}{L}}sin(\omega_2 t_2)$	$= i_{\mathrm{L}}(0)$
$v_{\mathrm{L}}(T_{\mathrm{sw}})$	$-(2\Delta v_{\mathrm{c}})cos(\omega_2 t_2) - \sqrt{\frac{L}{C_{\mathrm{eq},2}}}i_L(0)sin(\omega_2 t_2)$	$= -2\Delta v_{\mathrm{c}}$

4.4 Chapter Summary

This chapter presents a method for calculating split-phase timings for hybrid switched-capacitor converters accounting for both inductor current ripple and capacitor voltage ripple. Both an even-conversion-ratio and an odd-conversion-ratio hybrid Dickson converter were used as examples for the presented analysis, highlighting many of the nuances that may appear in hybrid SC converter timing. Table 4.3 compares the phase timings for small ripple approximations [77] and the resonant phase timings presented here. This chapter analyzes a particularly important switching scheme for hybrid SC converters and provides a foundation for analysis of further complicated switching schemes.

Table 4.3: Comparison of phase durations for the split-phase hybrid Dickson topology between large ripple and small ripple analysis.

		Small Ripple	Resonant
Even-N	t_{1a}	$\frac{(N+2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N+2} \cdot cos^{-1}\left(\frac{-1}{N-1}\right)\right]$
	t_{1b}	$\frac{(N-2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-2} \cdot cos^{-1}\left(\frac{1}{N+1}\right)\right]$
	t_{2a}	$\frac{(N+2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N+2} \cdot cos^{-1}\left(\frac{-1}{N-1}\right)\right]$
	t_{2b}	$\frac{(N-2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-2} \cdot cos^{-1}\left(\frac{1}{N+1}\right)\right]$
Odd-N	t_{1a}	$\frac{(N+5)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-5} \cdot cos^{-1}\left(\frac{2}{N+1}\right)\right]$
	t_{1b}	$\frac{(N-3)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-3} \cdot cos^{-1}\left(\frac{2}{N+3}\right)\right]$
	t_{2a}	$\frac{(2N-2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-5} \cdot \pi\right]$
	t_{2b}	$0 \cdot T_{sw}$	0

Chapter 5

Soft-Switching Techniques

As power converters continue to push the boundaries of efficiency and power density, topologies such as hybrid switched-capacitor (hybrid SC) converters are gaining traction. However, one limitation to improving power density (by reduction of passive component sizing) is switching loss. Switching faster often leads to reduced current and voltage ripples and therefore to a reduction in required passive component volume, but comes at the cost of potentially increased losses. Two methods for reducing switching losses — resonant operation for achieving zero-current switching (ZCS) and strategic clocking schemes for achieving zero-voltage switching (ZVS) — are common among more conventional topologies. However, there has been little investigation into ZVS operation for hybrid SC converters. Therefore, this chapter presents a generalized analytical approach to determine ZVS operation and timings for hybrid SC topologies. One of the more complex hybrid SC topologies — the split-phase hybrid Dickson converter — is used to highlight the intricacies of implementing ZVS in hybrid SC converters. An experimental 8-to-1 hybrid Dickson converter prototype has been built to demonstrate the efficiency benefits of ZVS operation over ZCS operation and to validate the timing analysis derived here.

5.1 Introduction

Previous works [10, 51, 85] demonstrate high performance step-down hybrid SC converters operating at high-conversion fixed-ratios and with a switching frequency that facilitates zero current switching (ZCS) for reduced voltage-current overlap loss. However, other recent works [54, 86] have shown that zero-voltage switching (ZVS) conditions can provide a greater reduction in switching losses, and therefore a higher efficiency than ZCS operation, particularly at light load. While both soft-switching methods provide efficiency improvements, the conditions for maintaining soft-switching are highly load-dependent. Active control techniques, such as those presented in [63,86–88] detail active tuning of soft-switching conditions. However, prior work demonstrating active ZVS tuning has commonly been demonstrated on topologies where all switch voltages are equal, and several switches are ground-referenced [86].

These characteristics also mean that all switches may be implemented with the same device, so that output capacitance values are similar across all switching elements. For many hybrid SC topologies, not only do the blocking voltages vary for different switches, but also different switching device implementations may be chosen based on voltage and current stresses. Therefore, an analytical description of the soft-switching conditions can be valuable for informing active control techniques for a range of circuit topologies. Rentmeister et al. [89] derive closed-form analytical expressions for ZVS conditions in a flying capacitor multi-level (FCML) converter. However, this work, too, is executed for a very symmetric topology (i.e., one that has many repeated switching-modules), which utilizes the same device for all switches and assumes equal blocking voltage on all switches – neglecting the fact that with greater than two switching cells for the FCML, the switches closest to the inductor and the input source have a lower voltage ripple imposed across the devices [34].

The work presented in this chapter addresses a generalized analytical evaluation of ZVS conditions for any hybrid SC topology, particularly those with less symmetry. Though this work demonstrates the process for a split-phase hybrid Dickson converter – one of the least symmetric hybrid SC topologies, the method is generally extensible.

5.2 Zero-Current Switching

Similar to split-phase operation or voltage regulation phases in certain hybrid SC converters, ZVS operation also requires the introduction of additional phases. Complicating the analysis is the fact that the inductor current is sinusoidal, rather than linear, making closed-form solutions much more difficult to ascertain.

However, other work in [1, 46–49, 51, 52, 54] has established that operating some ReSC converters above resonance can significantly improve overall converter efficiency through a reduction in rms currents and associated conduction losses, despite increases in relative switching loss.

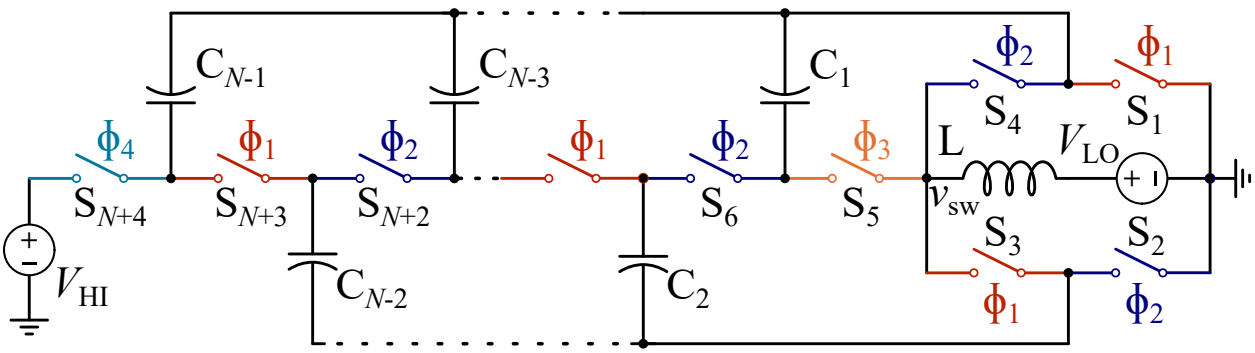


Figure 5.1: Schematic drawing of an even-N Dickson converter with switches labeled with their respective control phases. Switches S_1-S_4 are referred to as 'bridge' switches, S_5, S_{N+4} as 'split-phase' switches, and S_6-S_{N+3} as 'string' switches.

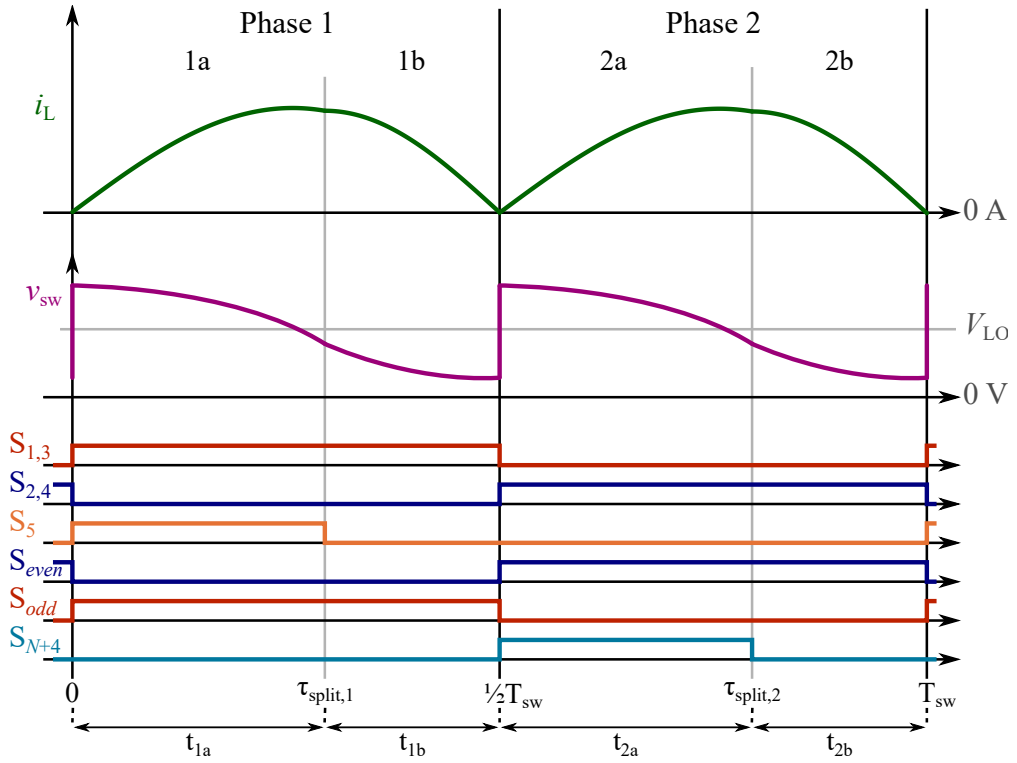


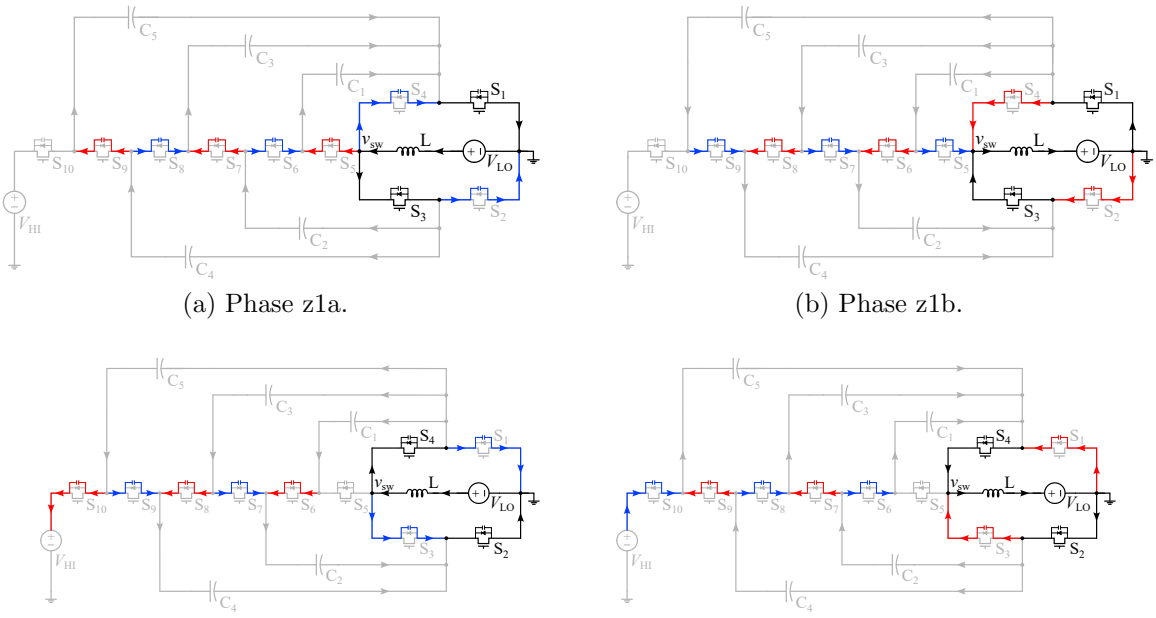
Figure 5.2: Illustrated inductor current and switch-node voltage for an even-N resonant Dickson with split-phase control.

5.3 Zero-Voltage Switching

While increasing switching frequency is a prevalent approach to decreasing passive component sizing and therefore increasing the power density of converter, switching losses also increase with frequency, potentially degrading efficiency. ZVS is one method of reducing these losses by switching a transistor only when the voltage across the device is zero, thereby reducing both overlap losses output capacitance discharge losses [90,91]. ZVS can be realized through resonant operation [92–94] or by using quasi-square-wave (QSW) control, wherein negative inductor current is used to charge/discharge of the switch output capacitances, C_{oss}, thereby achieving ZVS [90, 95–99].

ZVS Circuit Operation

For this analysis of ZVS timing, we assume that the flying capacitance is much larger than the parasitic switch capacitance and therefore does not influence the resonant behavior between the inductor and C_{oss} capacitances [89, 100]. Furthermore, if the flying capacitors are much larger than C_{oss}, then any change in the voltage on the flying capacitors during the ZVS sub-periods is negligible.



(a) Phase z1a.

(b) Phase z1b.

(c) Phase z2a.

(d) Phase z2b.

Figure 5.3: Circuit configurations for ZVS sub-periods showing which C_{oss} capacitances are charging (blue) and discharging (red).

Unlike (multi-level) buck/boost converters which achieve ZVS during switching deadtimes, most hybrid SC topologies require supplementary switching states to achieve ZVS on every switch without additional circuitry. These states, Phase zxa and Phase zxb shown in Fig. 5.4 (where x is either '1' or '2'), can be added between main Phases 1 and 2 to either charge or discharge the necessary parasitic output switch capacitances. (Note: the relative time duration of the ZVS periods to the main phases are exaggerated for visualization purposes.) The ZVS sub-phases differ from typical deadtimes because some switches must remain on to control the current flow to the appropriate switch C_{oss} [50, 86, 101]. Fig. 5.3 shows the circuit configurations for ZVS sub-periods in a 6:1 hybrid Dickson converter.

To determine what supplemental phases are needed to facilitate ZVS turn-on, it is helpful to examine the immediately preceding phase wherein the switch of focus is OFF.

- *Phase z1a:* $t \in [0, \tau_1]$ *and Phase z2a:* $t \in [T_{sw}/2, \tau_3]$

  Before the start of Phase 1, when odd-numbered switches turn on, the C_{oss} capacitances of these switches need to be discharged to 0 V for ZVS operation. To simplify the explanation of the ZVS sub-phases, we first assume that we turn S_1, S_3 on when both the inductor current, i_{L}, and the switch-node voltage, v_{sw}, are zero, therefore enforcing zero-voltage across the drain-source of these switches at the beginning of ZVS sub-phase z1a. At the same time, 'bridge' switches S_2 and S_4 can turn off with zero current due to the inductor current reaching 0 A at the same time that the voltage across S_1 and S_3 reaches 0 V. However, at this point ($t = 0$ in Fig. 5.4) switches S_5

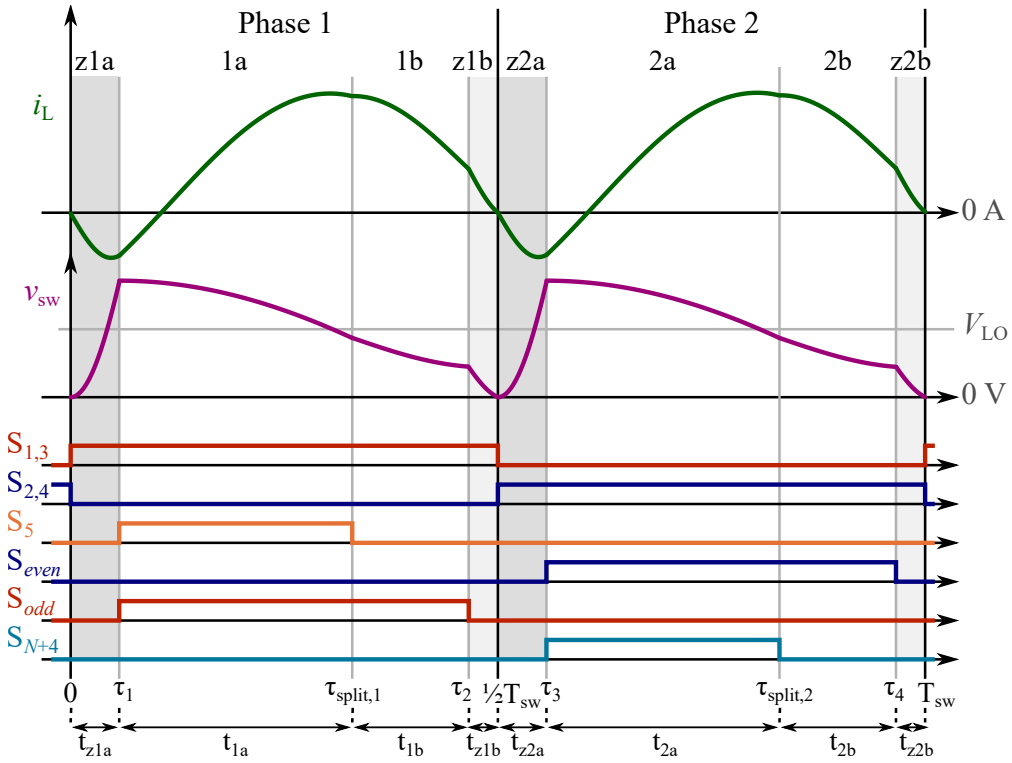


Figure 5.4: Illustrative gate signals, inductor current, and switch-node voltage for a 6:1 resonant Dickson with split-phase control and ZVS.

and S_{odd} do not necessarily have 0 V imposed across their terminals. Therefore, an additional ZVS sub-period, Phase z1a (Fig. 5.3a), is necessary. During this sub-period, only switches S_1 and S_3 are ON (having turned on with ZVS just as Phase 2 ends and Phase 1 begins) and switches S_5, S_7, and S_9 discharge to 0 V for ZVS turn-on at the beginning of Phase 1a. Furthermore, while the C_{oss} capacitances of switches S_5, S_7, and S_9 discharge, current must also flow through the output capacitances of S_2, S_4, and S_6, S_8 and S_{10}, charging these capacitances up from 0 V (since they were just turned off at the end of Phase 2b). Similarly, for Phase 2, we assume switches S_2 and S_4 turn on when i_L and v_{sw} are zero and then Phase z2a can be inserted between Phase 1 and Phase 2 to establish ZVS turn-on of switches S_6, S_8 and S_{10}.

- *Phase z1b: $t \in [\tau_2, T_{sw}/2]$ and Phase z2b: $t \in [\tau_3, T_{sw}]$* Parasitic switch output capacitances of S_1-S_4, S_5, and S_{10} only store $\frac{V_{HI}}{N}$ assuming no flying capacitance ripple,[1] whereas S_6-S_9 capacitances block $2\frac{V_{HI}}{N}$. Therefore if only Phase z1a and Phase z2a are inserted before Phase 1 and Phase 2, respectively, either some switches achieve ZVS while others do not, or some switches have excess body diode conduction because

[1]Switch blocking voltages accounting for capacitor voltage ripple and inductor current ripple are given in Appendix B for any even-N hybrid Dickson converter.

they fully discharge before the other switches. Consequently, additional sub-phases Phase z1b and Phase z2b are inserted between main-phase transitions. At the end of Phase 1b, S_7 and S_9 turn off while S_1 and S_3 remain ON during Phase z1b. The switch-node voltage and the inductor current continue to decrease until they reach zero, at which point, Phase z1b ends with S_1 and S_3 turning off and S_2 and S_4 turning on with ZVS and ZCS. During Phase z1b, switch capacitances of S_2 and S_4 fully discharged to 0 V, whereas S_6 and S_8 only partially discharge to the voltage-level of S_{10}. The remaining discharge of these capacitors occurs in Phase z2a as described above.

Similarly, switches S_1, S_3, S_5, S_7 and S_9 require two ZVS sub-periods, Phase z2b (Fig. 5.3d) and Phase z1a (Fig. 5.3a). In this case, switches S_7 and S_9 are turned off after Phase 1b to discharge the output capacitances of S_1, S_3 fully, and S_7 and S_9 partially in Phase 2zb. Then, switches S_1 and S_3 turn on with ZVS at the same time that S_2, S_4 turn off at zero current. With only S_1, S_3 ON, the output capacitances of switches S_5, S_7, and S_9 discharge during Phase 1za before turning on for Phase 1a. Simultaneously, as switch capacitances are discharging (depicted with red in Fig. 5.3), switches that are off may be charging (depicted with blue) up to values bounded by the flying capacitors.

Table 5.1: Time-Domain Circuit Dynamics Expressions - Phase 1

Parameter	Expression	Known Value
$i_{\mathrm{L}}(0)$	0	$= 0$
$v_{\mathrm{L}}(0)$	$-\left(\frac{V_{\mathrm{HI}}}{N}\right)$	$= -\left(\frac{V_{\mathrm{HI}}}{N}\right)$
$i_{\mathrm{L}}(\tau_1)$	$-\left(\frac{V_{\mathrm{HI}}}{N}\right)\sqrt{\frac{C_{\mathrm{e,z1a}}}{L}}sin(\omega_{\mathrm{z1a}}t_{\mathrm{z1a}})$	
$v_{\mathrm{L}}(\tau_1)$	$-\left(\frac{V_{\mathrm{HI}}}{N}\right)cos(\omega_{\mathrm{z1a}}t_{\mathrm{z1a}})$	$= \frac{2\Delta v_{\mathrm{c}}}{N} \cdot (N-1)$
$i_{\mathrm{L}}(\tau_{\mathrm{split,1}})$	$i_{\mathrm{L}}(\tau_1)cos(\omega_{\mathrm{1a}}t_{\mathrm{1a}}) + \frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}\sqrt{\frac{C_{\mathrm{e,1a}}}{L}}sin(\omega_{\mathrm{1a}}t_{\mathrm{1a}})$	
$v_{\mathrm{L}}(\tau_{\mathrm{split,1}})$	$\frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}cos(\omega_{\mathrm{1a}}t_{\mathrm{1a}}) - \sqrt{\frac{L}{C_{\mathrm{eq,1a}}}}i_L(\tau_1)sin(\omega_{\mathrm{1a}}t_{\mathrm{1a}})$	$= -\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right)$
$i_{\mathrm{L}}(\tau_2)$	$i_{\mathrm{L}}(\tau_{\mathrm{split,1}})cos(\omega_{\mathrm{1b}}t_{\mathrm{1b}}) + \frac{-2\Delta v_{\mathrm{c}}}{N}\sqrt{\frac{C_{\mathrm{e,1b}}}{L}}sin(\omega_{\mathrm{1b}}t_{\mathrm{1b}})$	
$v_{\mathrm{L}}(\tau_2)$	$-\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right)cos(\omega_{\mathrm{1b}}t_{\mathrm{1b}}) - \sqrt{\frac{L}{C_{\mathrm{e,1b}}}}i_{\mathrm{L}}(\tau_{\mathrm{split,1}})sin(\omega_{\mathrm{1b}}t_{\mathrm{1b}})$	$= -\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right) \cdot (N+1)$
$i_{\mathrm{L}}(T_{\mathrm{sw}}/2)$	$i_{\mathrm{L}}(\tau_2)cos(\omega_{\mathrm{z1b}}t_{\mathrm{z1b}}) + \frac{-2\Delta v_{\mathrm{c}}\cdot(N+1)}{N}\sqrt{\frac{C_{\mathrm{e,z1b}}}{L}}sin(\omega_{\mathrm{z1b}}t_{\mathrm{z1b}})$	$= 0 = i_{\mathrm{L}}(0)$
$v_{\mathrm{L}}(\frac{T_{sw}}{2})$	$-\frac{2\Delta v_{\mathrm{c}}\cdot(N+1)}{N}cos(\omega_{\mathrm{z1b}}t_{\mathrm{z1b}}) - \sqrt{\frac{L}{C_{\mathrm{e,z1b}}}}i_{\mathrm{L}}(\tau_2)sin(\omega_{\mathrm{z1b}}t_{\mathrm{z1b}})$	$= -(\frac{V_{\mathrm{HI}}}{N}) = v_{\mathrm{L}}(0)$

Calculating ZVS sub-period timing

During the ZVS sub-periods Phases 1za, 1zb, 2za, and 2zb, the output switch capacitances comprise a resonant LC network with the inductor. Assuming the flying capacitors are much larger than the C_{oss} values, the flying capacitors are treated as DC sources and do not resonate with the inductor during the ZVS sub-periods [89, 100]. Time-domain equations for the voltage across and the current through the inductor are given by (5.1) and (5.2). We assume that Phase 1 and Phase 2 operate symmetrically and therefore only consider Phase 1 for calculating the ZVS sub-period timings. The resonant capacitance is an effective capacitance, $C_{\text{e},j}$ (where j refers to the ZVS sub-periods: z1a, z1b, z2a, and z2b), determined by the switch output capacitances that are participating in the LC network during the specific time period, (5.3) for an even N:1 converter. The resonant frequency is given by (5.4). Here, a linear C_{oss} is assumed and Section 5.4 details the formulation of this linear capacitor.

$$i_{\text{L},j}(t) = i_{\text{L},j}(0)cos(\omega_j t) + \sqrt{\tfrac{C_{\text{e},j}}{L}}\big(v_{\text{sw},j}(0) - \tfrac{V_{\text{HI}}}{N}\big)sin(\omega_j t) \tag{5.1}$$

$$v_{\text{L},j}(t) = \big(v_{\text{sw},j}\big(0) - \tfrac{V_{\text{HI}}}{N}\big)cos(\omega_j t) - \sqrt{\tfrac{L}{C_{\text{e},j}}}i_{\text{L},j}(0)sin(\omega_j t) \tag{5.2}$$

$$C_{\text{e},zx} = (N+1)C_{\text{oss}} \tag{5.3}$$

$$\omega_{zx} = (\sqrt{LC_{\text{e},zx}})^{-1} \tag{5.4}$$

The inductor current and switch-node voltage are illustrated in Fig. 5.5 with known quantities labeled. Equations (given in Table 5.1) for the inductor voltage and current at each phase transition are used to solve for the unknown phase durations: t_{z1a}, t_{z1b}, t_{1a}, and t_{1b}. Due to the addition of the ZVS sub-phases, the initial conditions are no longer the same as the purely resonant split-phase case in Section 4.2, and consequently, the time spent in the 'a' and 'b' phases must be recalculated. One drawback of using this time-domain method to calculate sub-period timings, is that each equation is dependent on Δv_{c}, which is itself dependent on the total switching period (i.e., it is dependent on the sum of all of the sub-period times), creating a circular dependency. Ref. [89] simplified the problem-space of FCML ZVS timings by assuming that ZVS sub-periods can be neglected when calculating T_{sw}, (i.e., $T_{\text{sw}} = 2 \cdot (t_{\text{1a}} + t_{\text{1b}})$ instead of (5.5)). However, because the even-N hybrid Dickson converter requires split-phase switching, either a numerical solver can be used or the timings must be solved iteratively, using the purely resonant split-phase Δv_{c} value as the starting value. Then, all sub-period timings can be calculated based on load current and L-C values.

$$T_{\text{sw}} = 2(t_{\text{z1a}} + t_{\text{z1b}} + t_{\text{1a}} + t_{\text{1b}}) \tag{5.5}$$

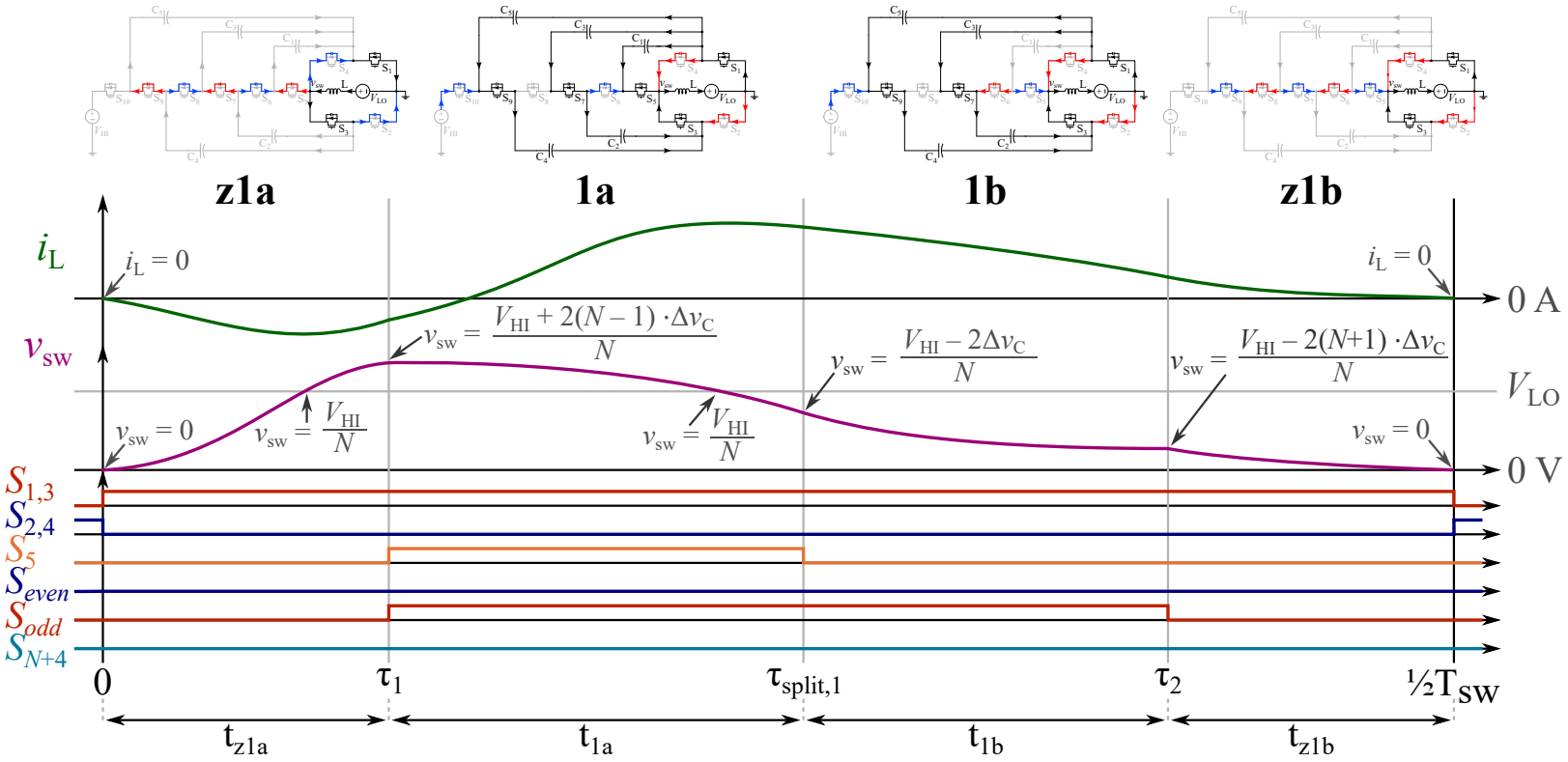


Figure 5.5: Switching states and example waveforms for Phase 1 operation. Phase 2 operates analogously with equivalent inductor current and switch-node voltage waveforms.

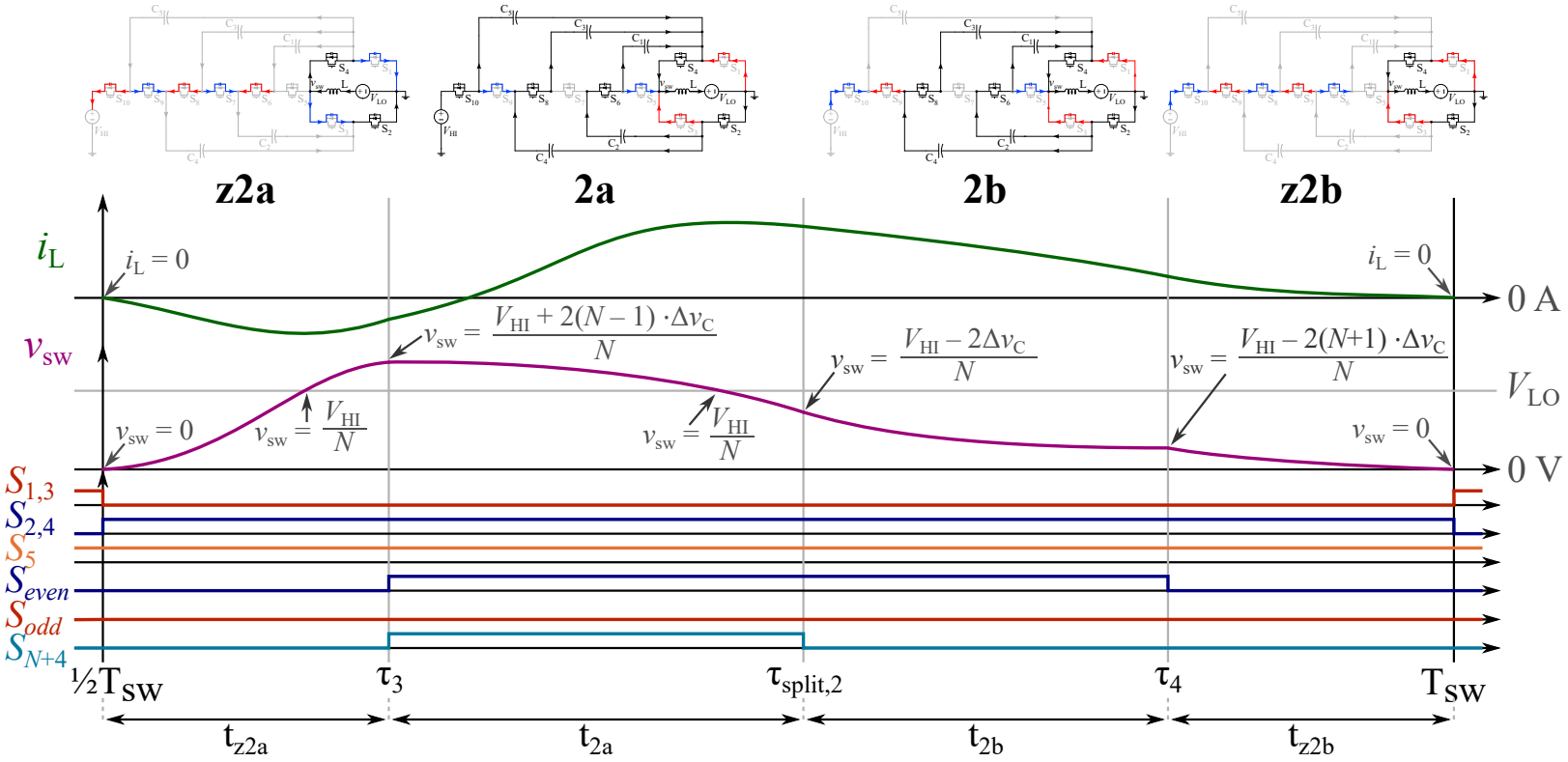


Figure 5.6: Switching states and example waveforms for Phase 2 operation.

5.4 Non-linear $C_{\mathbf{oss}}$ Considerations

As mentioned in Section 5.3, because the switch output capacitance is non-linear, typically a linearized equivalent capacitance is used [102–105] to simplify any analysis. The type of analysis being performed dictates the method of linear equivalence should be used, for example, the capacitance used for switching loss analysis is different than that used for determining the energy required for ZVS. Prior works [102–105] refer to various equivalent capacitances: energy, charge, impedance, ZVS equivalent capacitances in the context of half-bridge switch pairs. Here, and for many hybrid SC converters, the switches are not configured as a typical half-bridge with equal blocking voltages across two equivalent, complementary switches. Moreover, for the 'string' switches which (dis)charge during *two* ZVS sub-phases, the linearized equivalent output capacitance is different between these two phases.

The linearized output capacitances depend on charge and energy analyses. The relationship between the non-linear capacitor's charge and the voltage at which the charge is transferred is given by (5.6) and is illustrated for an example switching device in Fig. 5.8. At a specific blocking voltage (60 V in Fig. 5.8), there is a corresponding charge Q_{oss}. The 'charge-equivalent' linearized capacitance, $C_{Q,\text{eq}}$, is defined as a linear capacitance which stores the same charge as the non-linear capacitor at the specified blocking voltage. The value of $C_{Q,\text{eq}}$ is determined (5.13) by the slope of the line from the origin to the Q_{oss} plot at the specified blocking voltage.

$$Q_{\text{oss}}(V_{\text{ds}}) = \int_0^{V_{\text{ds}}} C_{\text{oss}}(v)\ \mathrm{d}v \tag{5.6}$$

$$C_{Q,\text{eq}} = \frac{Q_{\text{oss}}(V_{\text{ds}})}{V_{\text{ds}}} \tag{5.7}$$

Moreover, an 'energy-equivalent' linearized capacitance, $C_{E,\text{eq}}$, is defined as a linear capacitance which stores the same energy, E_{oss}, as the non-linear capacitor at the specified blocking voltage. The stored energy in the capacitor (5.8) is the area between the Q_{oss}-V_{ds} curve and the Q_{oss} axis at the specified blocking voltage. Using the relationship between stored energy in a linear capacitor (5.9), the value of $C_{E,\text{eq}}$ is determined (5.10) by the slope of the line from the origin to the specified blocking voltage which encompasses an area to the Q_{oss} axis that equals E_{oss}.

$$E_{\text{oss}} = \int_0^{Q_{\text{oss}}(V_{\text{ds}})} v\ \mathrm{d}q = \int_0^{V_{\text{ds}}} v \cdot C_{\text{oss}}(v)\ \mathrm{d}v \tag{5.8}$$

$$E_{\text{c}} = \frac{1}{2} C_{\text{linear}} V_{\text{c}}^2 \tag{5.9}$$

$$C_{E,\text{eq}} = \frac{2 \cdot E_{\text{oss}}}{V_{\text{ds}}^2} \tag{5.10}$$

For evaluating resonant inductor current values in a ZVS transition, [103] defines a linear equivalent capacitance $C_{\mathrm{Z,eq}}$ as the linear capacitance which corresponds to the energy processed by a series impedance during the charge/discharge of a non-linear capacitor through a dc voltage source (Fig. 5.7). The energy processed by the series impedance (5.11) is the difference between the energy supplied by the dc source and the stored energy in the switch output capacitance.

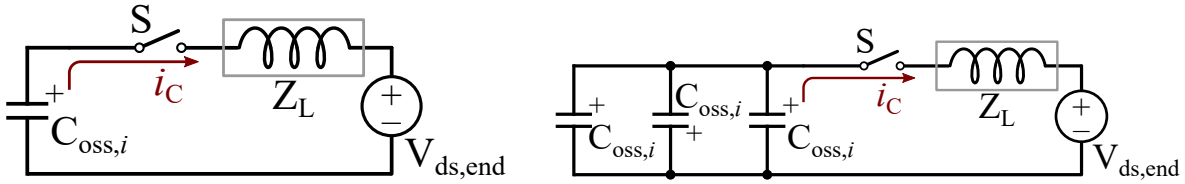
$$E_{\mathrm{Z},ij} = E_{\mathrm{source},ij} - E_{\mathrm{store},ij} \tag{5.11}$$

During a switching transition, a number of switch C_{oss} capacitors may be charging or discharging through a dc voltage source. Here, as stated above we assume that the flying capacitors act as dc voltage sources during the ZVS transitions. Furthermore, an equivalent dc voltage is assumed for each ZVS phase j as the charging/discharging source with a value of $V_{\mathrm{ds},ij}$. This voltage is determined by the blocking voltage of each C_{oss} capacitor at the end (or start) of the ZVS phase for charging (or discharging). The energy supplied by the dc source for capacitor (dis)charging is given by (5.12). The 'supplied' energy from the dc source is negative for a capacitor discharging into the source. The sourced charge can be related to a 'charge-equivalent' linearized capacitance, $C_{Q,\mathrm{eq}}$ (5.13) — defined as a linear capacitance which stores the same charge as the non-linear capacitor at the specified blocking voltage V_x.

$$\begin{aligned} E_{\mathrm{source},ij} &= V_{\mathrm{ds},ij}(\Delta Q_{\mathrm{oss},i}) \\ &= V_{\mathrm{ds},ij}\big(Q_{\mathrm{oss},i}(V_{\mathrm{end},j}) - Q_{\mathrm{oss},i}(V_{\mathrm{start},j})\big) \end{aligned} \tag{5.12}$$

$$C_{Q,\mathrm{eq}}(V_x) = \frac{Q_{\mathrm{oss}}(V_x)}{V_x} = \frac{\int_0^{V_x} C_{\mathrm{oss}}(v)\ \mathrm{d}v}{V_x} \tag{5.13}$$

Moreover, an 'energy-equivalent' linearized capacitance, $C_{E,\mathrm{eq}}$, is defined (5.14) as a linear capacitance which stores the same energy, $E_{\mathrm{oss},ij}$, as the non-linear capacitor at the specified blocking voltage, V_x. The difference in energy stored in each switch output capacitance at the start and end of each switch transition is stored and therefore not processed by the series



(a) Single switch output capacitor. (b) Multiple parallel switch output capacitors.

Figure 5.7: Equivalent circuit diagram for switch C_{oss} capacitor discharging.

impedance. The stored energy can be expressed as (5.15).

$$C_{E,\mathrm{eq}}(V_x) = \frac{2 \cdot E_{\mathrm{oss},ij}}{V_x^2} = \frac{2 \cdot \int_0^{V_x} v \cdot C_{\mathrm{oss}}(v)\ \mathrm{d}v}{V_x^2} \tag{5.14}$$

$$\begin{aligned} E_{\mathrm{store},ij} &= E_{\mathrm{oss},ij}(V_{\mathrm{end},j}) - E_{\mathrm{oss},ij}(V_{\mathrm{start},j}) \\ &= \frac{1}{2}\big(C_{E,\mathrm{eq}}(V_{\mathrm{end},j}) \cdot V_{\mathrm{end},j}^2 - C_{E,\mathrm{eq}}(V_{\mathrm{start},j}) \cdot V_{\mathrm{start},j}^2\big) \end{aligned} \tag{5.15}$$

Using the relationship between voltage and energy for a linear capacitor (5.16), an equivalent capacitance $C_{\mathrm{Z,eq}}$ can be found for each switch during each ZVS phase from (5.11)-(5.16) based on the difference in voltage $\Delta V = V_{\mathrm{end},j} - V_{\mathrm{start},j}$. This capacitance value is used to formulate an effective capacitance at the switch-node during each ZVS phase, $C_{\mathrm{e},zx}$, as a parallel combination of each of the switch C_{oss} capacitances equal to $C_{\mathrm{Z,eq}ij}$.

$$E_{\mathrm{c}} = \frac{1}{2} C_{\mathrm{linear}} V_{\mathrm{c}}^2 \tag{5.16}$$

$$\begin{aligned} C_{Z,\mathrm{eq}}(\Delta V) = 2\Bigg[& \frac{V_{\mathrm{end},j}^2}{(\Delta V)^2} && (5.17) \\ & \times \left(\frac{V_{\mathrm{start},j}}{V_{\mathrm{end},j}} C_{Q,\mathrm{eq}}(V_{\mathrm{end},j}) - \frac{1}{2} C_{E,\mathrm{eq}}(V_{\mathrm{end},j}) \right) && (5.18) \\ & - \frac{V_{\mathrm{start},j}^2}{(\Delta V)^2} \times \left(C_{Q,\mathrm{eq}}(V_{\mathrm{start},j}) - \frac{1}{2} C_{E,\mathrm{eq}}(V_{\mathrm{start},j}) \right) \Bigg] \end{aligned}$$

This impedance-equivalent linearized capacitance can be substituted into the expressions in Table 5.1 to determine the shape of the inductor current during the ZVS transitions. Because each switch output capacitance is linearized based on its individual starting and ending voltages, a total equivalent capacitance seen at the switch-node is formed by a parallel combination of these linearized capacitors for each switch output capacitance that is charging or discharging during the phase being examined.

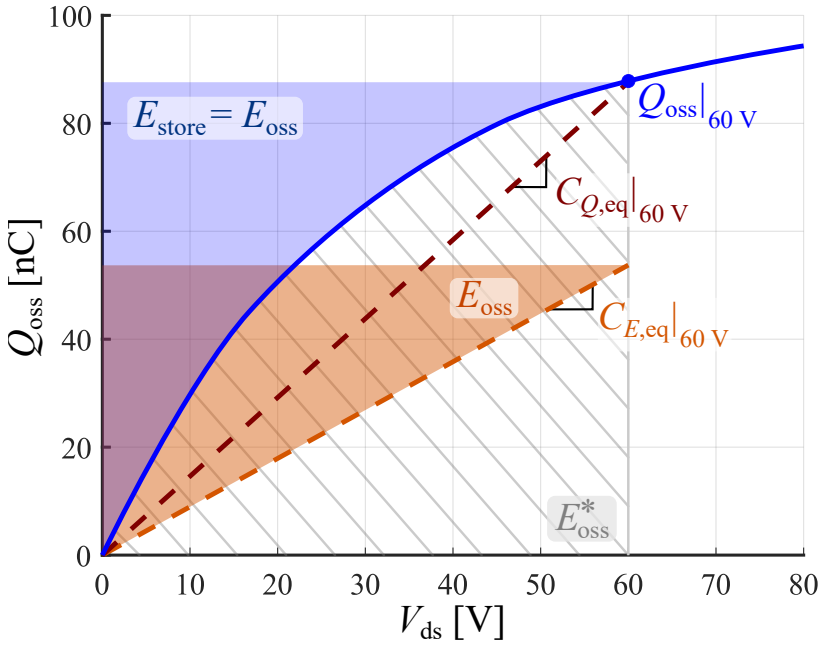


Figure 5.8: Stored charge in the switch output capacitance and as a function of the blocking voltage for an example switch device. Shaded areas corresponding to stored energy, co-energy; as well as linearized capacitances (charge-equivalent ($C_{Q,\text{eq}}$) and energy-equivalent ($C_{E,\text{eq}}$) are notated.

5.5 Experimental Results

One application space in which ZVS may be advantageous, particularly at light load operation, is data center power delivery where switching losses may be more dominant than conduction losses. Therefore, a discrete 8-to-1 hybrid Dickson converter hardware prototype (Fig. 5.9) was constructed to validate the timing analysis presented here. The experimental prototype steps 48 V down to a nominal 6 V utilizing Si MOSFETs. Gate drive power is

Table 5.2: Converter Operating Parameters

Parameter	Value	Units
V_{HI}	48	V
V_{LO}	6	V
$P_{\text{LO},max}$	85	W
f_{res}	114	kHz
L	0.241	μH
C^*_{in}	60	μH
C^*_{fly}	4	μH

* Voltage-de-rated values.

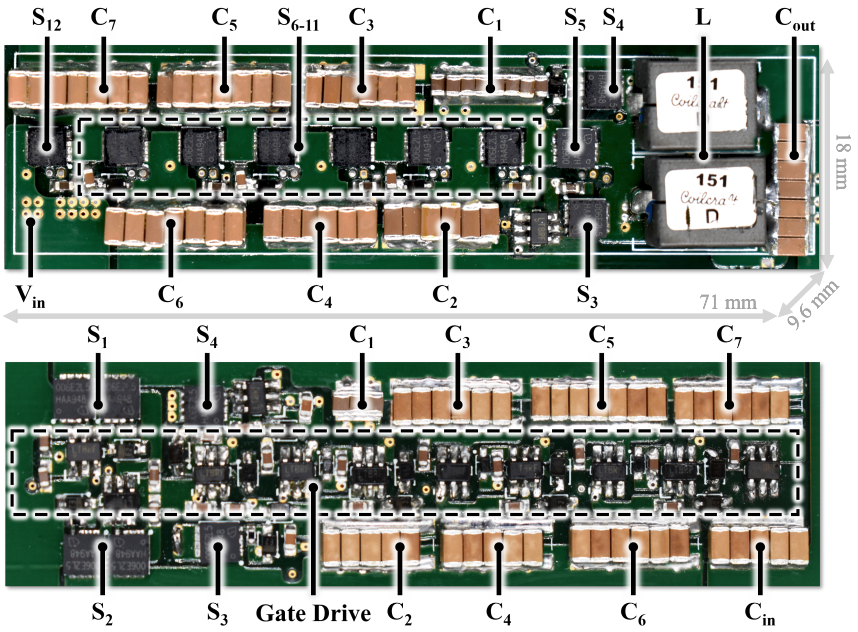


Figure 5.9: Annotated photograph of an 8-to-1 48 V-input hybrid Dickson converter, measuring 71 mm × 18 mm × 9.6 mm.

supplied by both Cascaded Bootstrap (CB) and Gate-Driven Charge Pump (GDCP) methods [106], as shown in Fig. 5.10. Inductor and capacitor values were chosen to balance conduction and switching losses at resonant operation. Table 5.2 defines the operating parameters for this prototype and all components are listed in Table 5.3.

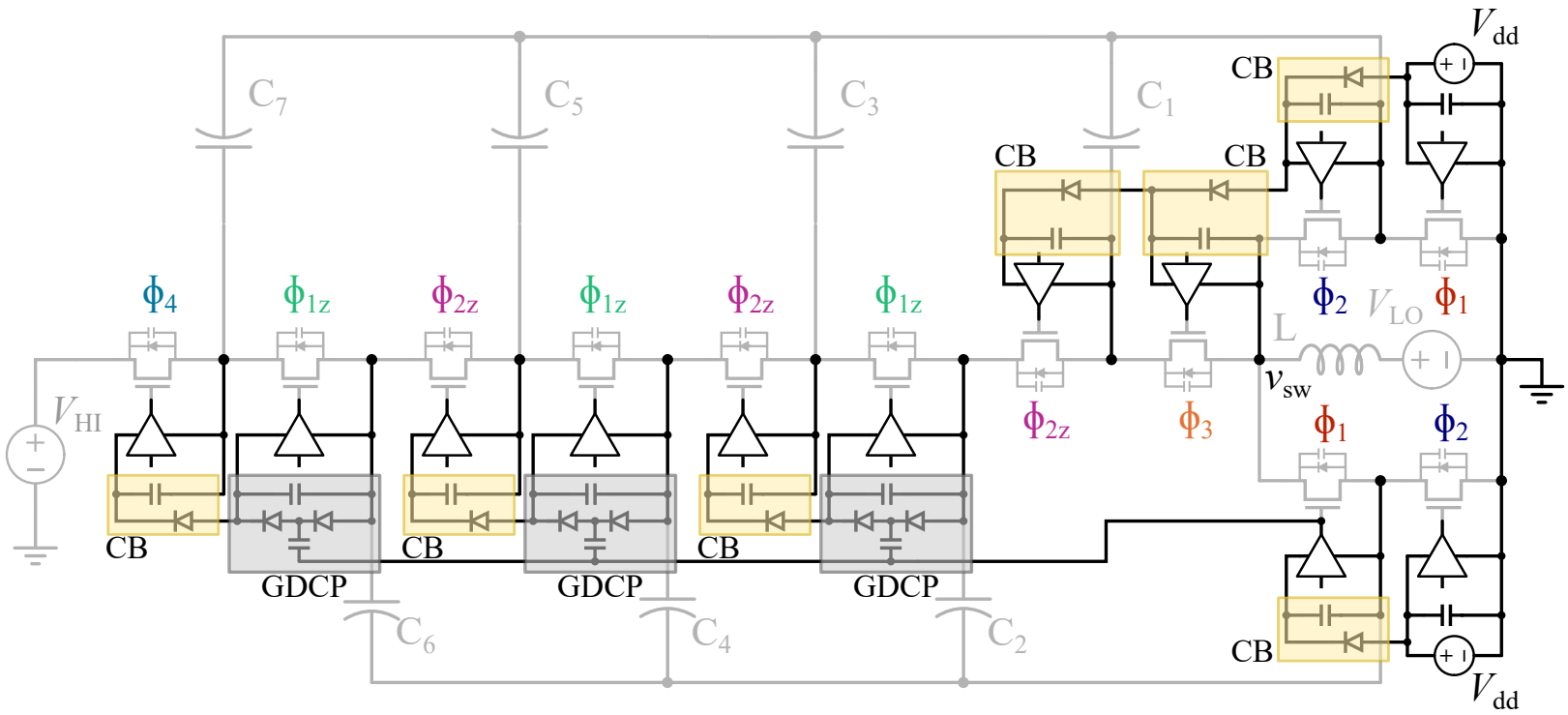


Figure 5.10: Schematic drawing of the gate drive circuitry implemented in the hybrid Dickson converter prototype combining Cascaded Bootstraps (yellow boxes) with Gate-Driven Charge Pumps (grey boxes).

Table 5.3: Component Listing of the Hardware Prototype

Component		Mfr. & Part Number	Parameters
Dickson Power Stage			
Bridge Switches	S_1 - S_4	2x Infineon IQE006NE2LM5	Si MOSFET, 25 V, 0.65 mΩ
String Switches	S_5 - S_{12}	Infineon IQE006NE2LM5	Si MOSFET, 25 V, 0.65 mΩ
Flying Capacitors	$C_1 - C_7$	TDK	∼4 μF de-rated
Inductor	L	Coilcraft SLC1480-231	0.23 μH, 57 A I_{sat}, 0.18 mΩ
Gate Drive			
Gate Driver		Analog Devices Inc. LT4440-5	80 V, high-side driver
Charge Pump Driver		Analog Devices Inc. LT4440-5	80 V, high-side driver
Bootstrap Diodes		Nexperia PMEG6002EJ,115	Schottky, 60 V, 200 mA
Charge Pump Diodes		Diodes Inc. PD3S230L-7	Schottky, 30 V, 2 A
Charge Pump Capacitors		Murata	X5R, 50 V, 2.2 μF
Controller Board			
FPGA		Terasic Inc. P0466	DE10-Lite, Max10 FPGA

Efficiency Measurements

Fig. 5.11 shows efficiency versus load curves measured for ZCS (resonant) operation and ZVS operation. At light load, the efficiency benefit of ZVS over ZCS is evident with a 53% loss-reduction. However, as load increases and conduction losses begin to increase over switching losses, the benefit of ZVS is less apparent. At the maximum load condition of the tested prototype, ZCS operation is *more* efficient than ZVS, this is due to the fact that the conduction losses due to the increase in rms current (owing to the need for negative inductor current) of the ZVS case (Fig. 5.13) outweigh the switching loss reduction from ZVS. An estimated loss breakdown of the ZCS and ZVS cases at 12 A is shown in Fig. 5.12, where ZVS only exhibits a 6% decrease in losses over ZCS operation. Furthermore, the efficiency of using the calculated ZVS times versus fixed ZVS times (i.e., the ZVS times needed to achieve ZVS at a specific load condition is use across all loads) are shown. At light load, these efficiencies are very similar, however at heavy load, they diverge. The calculated ZVS times have a higher efficiency than the fixed-time curve at heavier load due to the loss of full ZVS if the ZVS sub-phase times are improperly set. Moreover, for a simplistic implementation in similar hybrid SC converters, the designer can use fixed ZVS timings to achieve efficiency benefits over ZCS, however, losses may increase more at heavy loads over ZCS than if analytically determined phase timings are used.

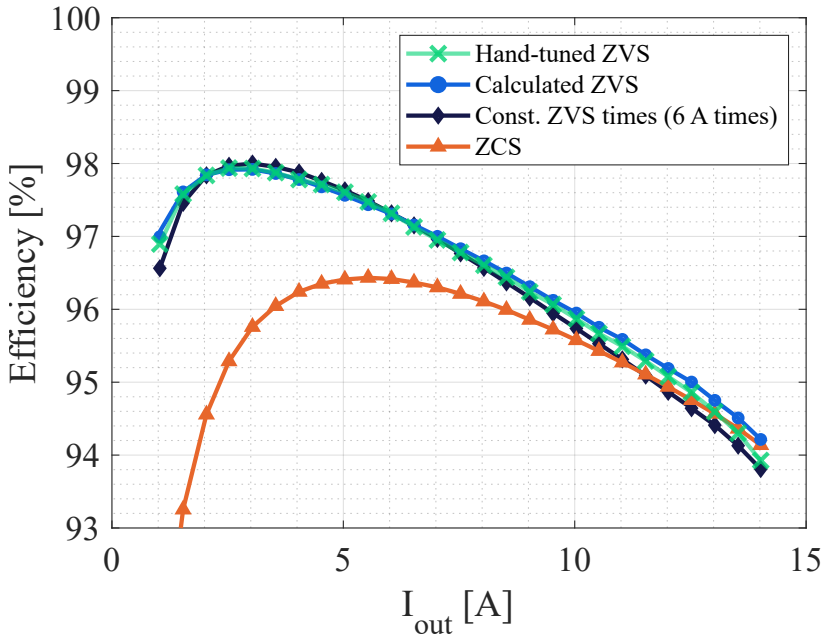
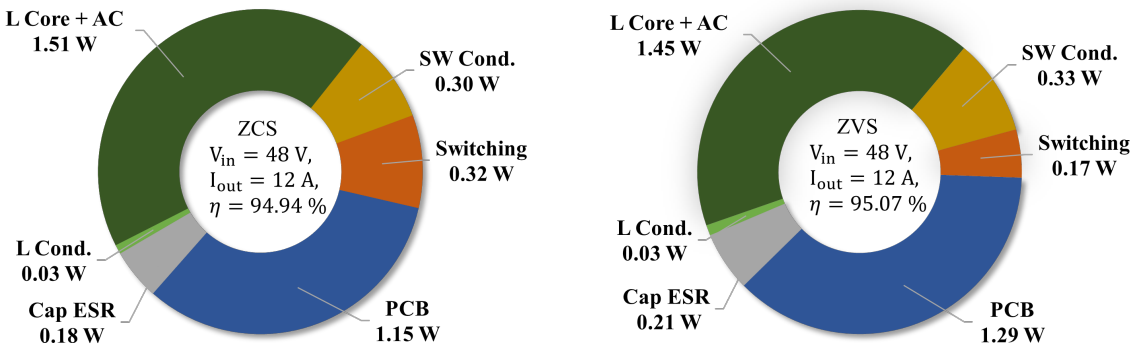


Figure 5.11: Efficiency comparison of various soft-switching timings across a load range for an unregulated 48 V-to-6 V hybrid Dickson converter. ZVS operation has higher efficiency than ZVS operation a lighter load, but as conduction losses begin to dominate with increased load, ZVS operation exhibits lower efficiency.



(a) ZCS. (b) ZVS.

Figure 5.12: Estimated loss breakdown of the 48-to-6 V hybrid Dickson converter at 12 A output current.

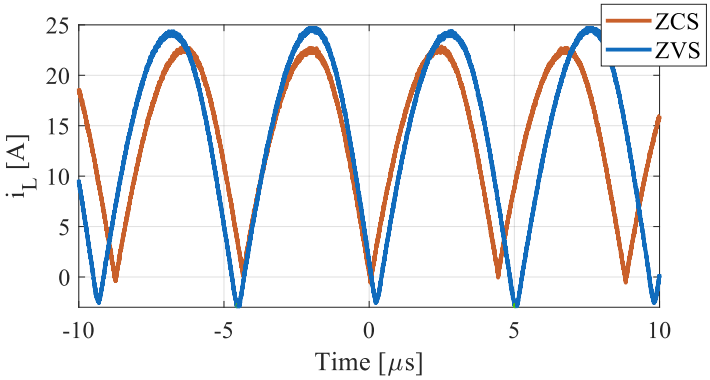


Figure 5.13: Measured inductor current waveforms for ZCS and ZVS operation highlighting the increased peak-to-peak ripple and increased rms of the ZVS case.

Zero-Voltage Switching

Waveforms for switch drain-source and gate-source voltages are shown in Fig. 5.14, demonstrating each drain-source voltage reaching near 0 V before the gate-source begins to turn the switch on. The partial discharge of switches S_6 - S_{11} during phases z1b and z2b can be seen. Because these switches block different voltages than the remaining switches, the lower-blocking-voltage switches achieve ZVS before switches S_6 - S_{11}. Furthermore the absence of ringing on the switch-node voltage, v_{sw}, demonstrates another benefit of soft-switching. Notice that switch drain-source voltages for the 'string' switches is still slightly above 0 V when the device gate-source voltage begins to rise. If deadtime is extended to get ZVS on all switches, there is excessive ringing on the lower voltage switches. However, the drain-source voltage does reach 0 V before the gate-source voltage passes the threshold voltage, thereby still eliminating most of the switching losses.

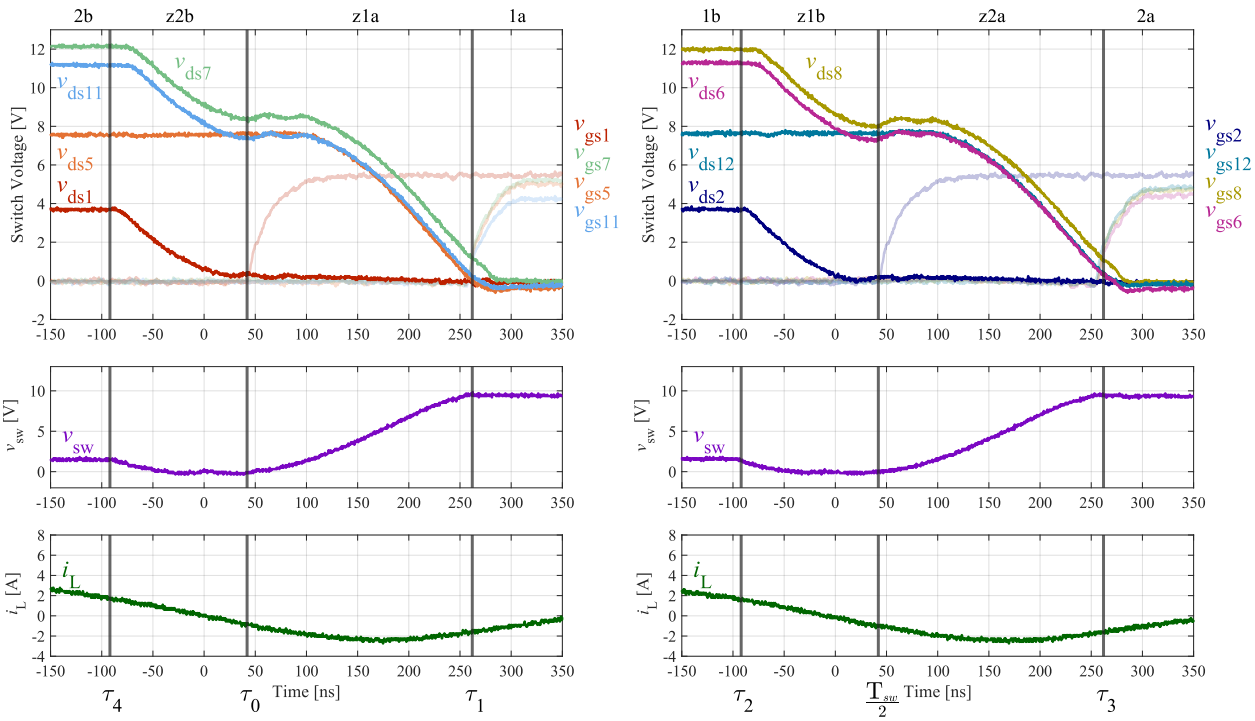
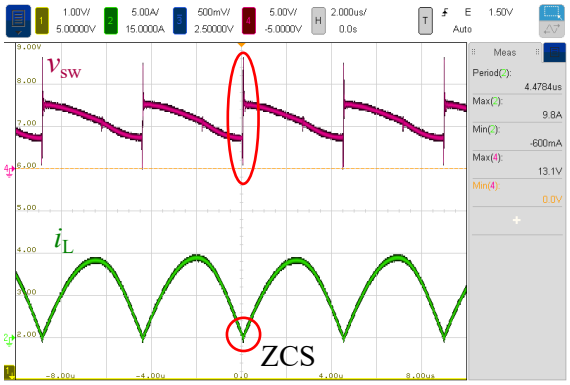
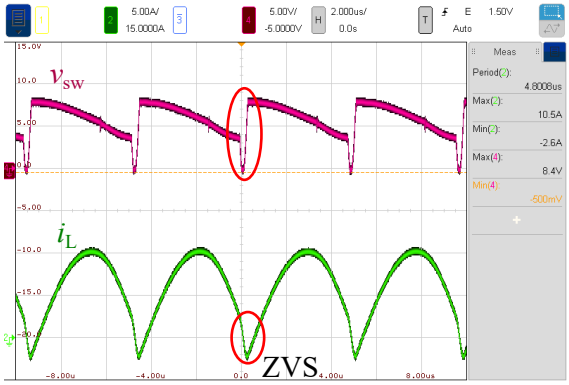


Figure 5.14: Experimental waveforms illustrating switch drain-source and gate-source voltages demonstrating the discharging of switch output capacitance to near 0 V before switch turn-on.

Fig. 5.15 compares the switch-node voltage spikes at phase transitions for ZCS and ZVS operation. Good ZVS operation is characterized by little or no voltage overshoot on the switch-node voltage, however, ZVS oeration also comes at the cost of increased rms inductor current. Switch drain-source voltages for various ZVS sub-phase timings are shown in Fig. 5.16, with too short timings corresponding to steep voltage slopes at phase transitions and too long timings corresponding to increased ringing (and body diode conduction).



(a) ZCS operation at 6 A.

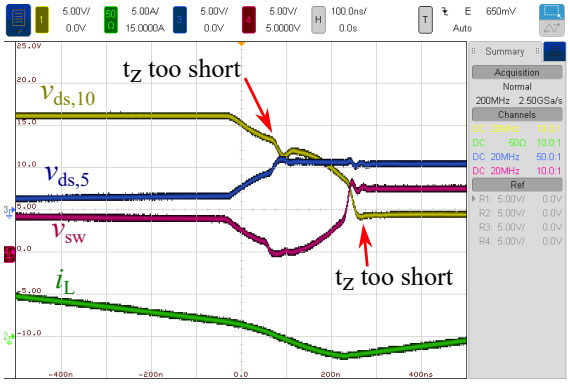


(b) ZVS operation at 6 A.

Figure 5.15: Measured inductor current and switch-node voltage waveforms for ZCS and ZVS operation.

(a) 10 A with t_{z1b} too long and t_{z2a} too short.

(b) 5 A with t_{z1b} too short and t_{z2a} too long.



(c) 5 A with t_{z1b} too short and t_{z2a} too short.

(d) 7 A with t_{z1b} and t_{z2a} optimally timed.

Figure 5.16: Drain-source voltage measurements for switches S_{10} and S_5 exhibiting sub-optimal ZVS phase timings and optimal phase timings for various load currents.

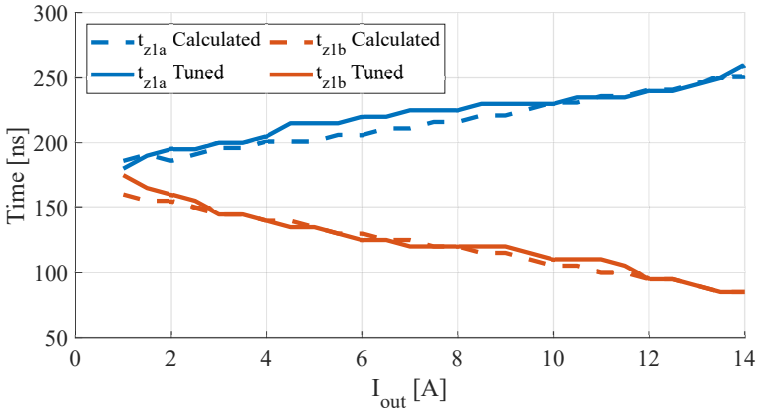
Timing Analysis

Fig. 5.17a shows the calculated ZVS timings as load varies, as well as the hand-tuned timings needed to fully achieve ZVS on every switch. The deviation in calculated and measured is less than 5% in part due to control PWM resolution of the FPGA, as well as due to the fact that output voltage droop and circuit resistances and parasitic inductances/capacitances are not incorporated into the theoretical model.

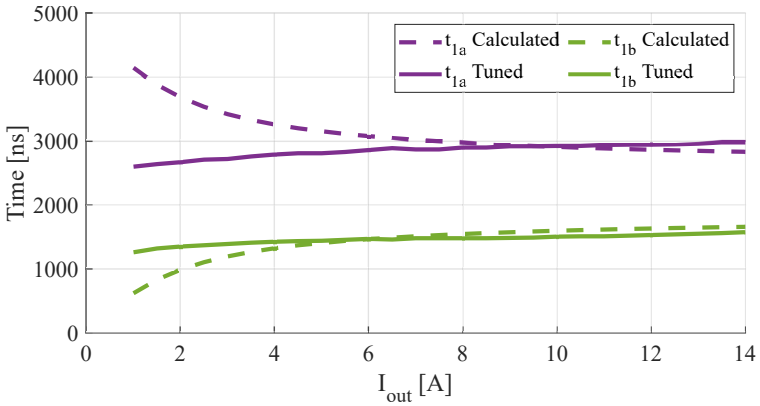
As load increases the voltage ripple on the capacitors increases and the switch-node minimum voltage approaches 0 V. Maintaining the switch-node voltage greater than or equal to 0 V ensures that no switches become excessively reverse-biased, which can lead to increased losses or even to device faults. This reverse-bias condition is described as the 'clamping' voltage in [84] and establishes the the maximum load condition (at a specific switching frequency and capacitance value). As the minimum switch-node voltage decreases, the voltage across even-numbered switch C_{oss} at the end of Phase 1b (and odd-numbered switch C_{oss} at the end of Phase 2b) reduces with load, and therefore the ZVS time required to discharge those capacitors is also reduced. Similarly, the ZVS time t_{z1b} and t_{z2b} increase because the peak switch-node voltage increases as load and voltage ripple increase.

5.6 Chapter Summary

This chapter describes a general analysis of converter operation using the hybrid Dickson converter as an example. The nuances of maintaining soft-charging of the flying capacitors are also described. A method of using sub-phases to achieve ZVS on every switch, and how to determine the time durations of all main phases and ZVS sub-phases is explained and considerations for non-linear switch output capacitance are addressed. Finally, an experimental prototype as well as measured operating waveforms and efficiency to validate the proposed analytical method are presented.



(a) ZVS timing comparison.



(b) Phase 1a and Phase 1b timing comparison.

Figure 5.17: Timing comparison of hand-tuned values to calculated time durations of the 8-to-1 hybrid Dickson converter.

Chapter 6

A Hybrid Switched-Capacitor Converter for Automotive Powertrains

This chapter investigates the challenges of implementing hybrid switched-capacitor (hybrid SC) converters in automotive applications. Several operation and switching techniques are discussed as they relate to both generation and mitigation of electromagnetic interference (EMI), a critical specification for automotive environments. A regulating 48 V-to-5 V Dickson-based dc-dc converter is analyzed, built, and tested to demonstrate the feasibility (and benefits) of using hybrid SC converters for automotive powertrains.

6.1 Background and Motivation

Hybrid switched-capacitor (hybrid SC) converters have achieved high efficiency and power density metrics due to their better utilization of passive components compared to conventional topologies [12, 32]. Particularly, high conversion ratio step-down hybrid SC converters have demonstrated high performance for use in data centers [14, 15, 18, 76], however, these converters are not yet widely explored in other high-energy-consumption industries, such as the automotive industry. Though these hybrid SC topologies boast high performance and passive component utilization, they often have a large number of switching elements and, therefore, more switching instances. However, typically, hybrid SC converters have lower switch blocking-voltages and lower dv/dt at the switch nodes, resulting in reduced electromagnetic interference (EMI). Having lower dv/dt and di/dt transitions than conventional topologies (Fig. 6.2) can improve EMI performance potentially makes them good candidates for use in automotive applications [19–21], where the EMI requirements more stringent. Therefore, further investigation into hybrid SC converter performance within these environmental constraints is necessary.

Moreover, as consumption shifts towards more hybridized and fully electric vehicles

(EVs), internal combustion engine (ICE) vehicles are beginning to adopt 48 V batteries in place of the legacy 12 V battery for partial hybridization of the powertrain, aligning themselves with EVs where 48 V may be used as an intermediary step-down from the high voltage battery [107] (Fig. 6.1). The use of a higher voltage bus decreases I^2R transmission losses and allows for lighter-weight cabling systems to be employed within the vehicle. The more power-hungry subsystems may be powered from a 48 V bus directly, instead of from a 12 V bus, while the lower-voltage subsystems may be driven from a 48 V bus using high-density point-of-load (PoL) converters [20, 96, 108–110]. Following similar trends to data-center power delivery [14, 15, 50, 75, 76, 111], automotive power delivery can eliminate a conversion step by completely removing the 12 V intermediary bus. Table 6.1 compares a few recent 48 V step-down converters either regulated or fixed-ratio as both point-of-load (PoL) and intermediate bus converters (IBCs).

The similarity in power delivery architecture provides an opportunity to apply the advanced power converter designs used in data center applications to automotive power solutions, with a few additional considerations. Firstly, in the automotive powertrain, the 48 V nominal battery voltage can vary between 42 V and 54 V, which the power converter must regulate to the desired output voltage. The power converters themselves must also meet industry EMI requirements so that they do not interfere with any other electrical subsystems. This chapter explores the regulation capabilities and the inherent EMI benefits of a hybrid SC converter, as well as two techniques to mitigate EMI: layout considerations, and Spread-Spectrum Frequency Modulation (SSFM) [112, 113], and analyzes their impacts on the size and efficiency of a hybrid SC converter.

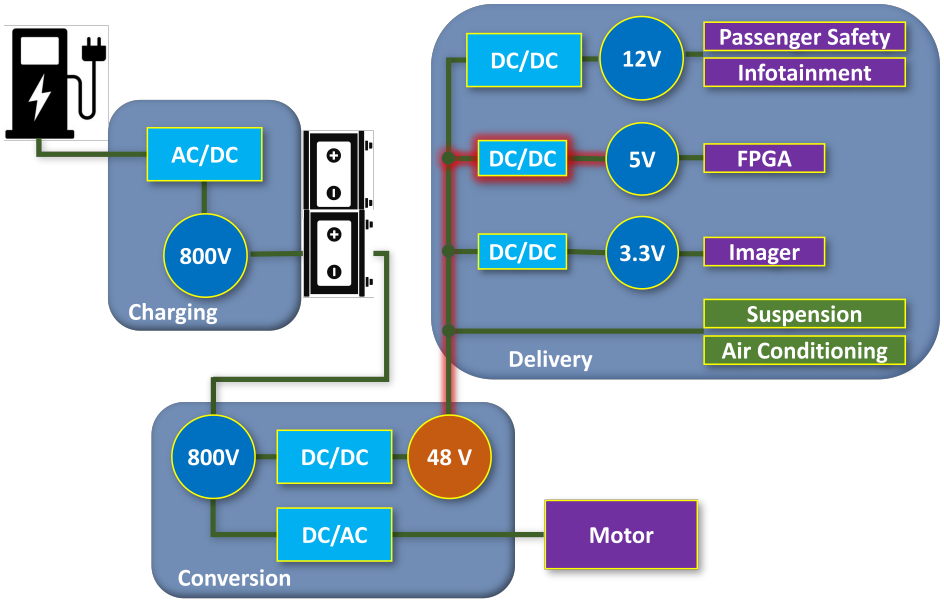


Figure 6.1: Block diagram of a 48 V bus architecture for electric vehicles highlighting the power conversion stage which is the focus of this chapter.

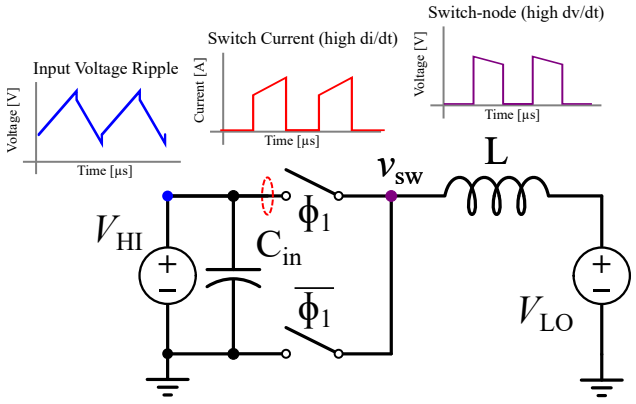


Figure 6.2: Diagram illustrating sources of conducted EMI in a buck converter.

Table 6.1: Survey of 48 V power converters.

Work	Voltage Ratio	Power [W]	Peak Efficiency [%]	Topology	Notes
[114]	48-to-5 V	125	92.0	2-phase Buck	Regulated
[115]	48-to-5 V	100	93.2	Buck	Regulated
[20]	48-to-3.3 V	10	93.0	Hybrid Dickson	IC, regulated
[116]	48-to-3.4 V	450	96.3	Hybrid Ladder	Fixed-ratio
[117]	48-to-6 V	420	98.6	CaSP	Fixed-ratio

Furthermore, automotive applications require components that are rating for vehicle environments. Because of this additional testing, typically automotive components are not only more expensive but can have worse Figures-of-Merit (FOM), such as specific on-state resistance and specific gate charge. Impacts of these component parameters on converter efficiency are discussed in Chapter 7.

This chapter presents a regulating hybrid Dickson switched-capacitor dc-dc power converter [22, 23] with a custom front-end EMI filter to demonstrate the ability of hybrid switched-capacitor converters to meet CISPR 25, Class 5 EMI standards [2], the most stringent class for on-vehicle applications.

6.2 Interleaved-Input, Single-Inductor Dickson Converter

The work presented in this chapter utilizes the interleaved-input, single-inductor Dickson topology (Fig. 6.3) described in [22] to demonstrate efficient, compact, and EMI-compliant DC-DC power conversion in a rugged automotive environment. Even without any additional EMI mitigation, this topology is attractive for automotive off-battery, PoL applications for a number of reasons: interleaved-input, low switch-stress, low dv/dt transitions, and the

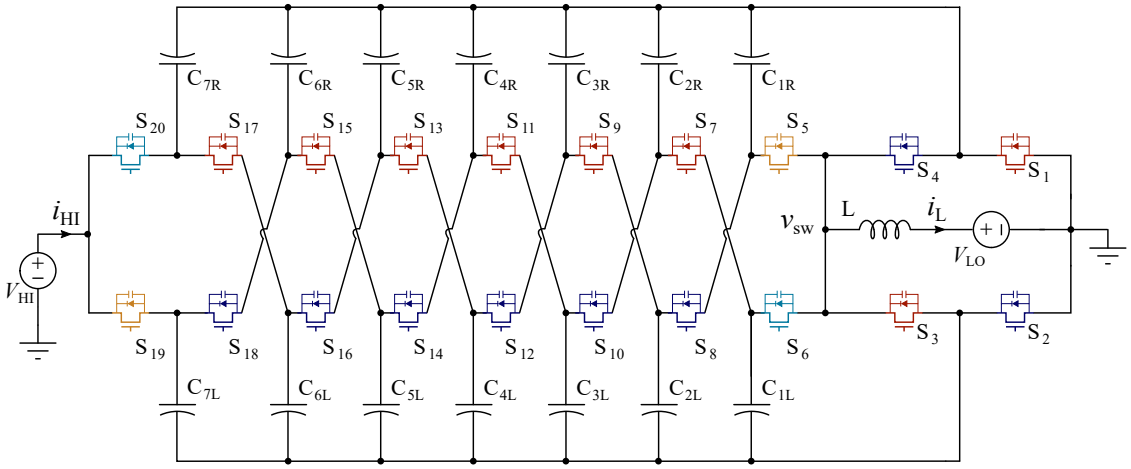


Figure 6.3: Schematic drawing of an 8-to-1 interleaved-input Dickson-variant hybrid switched-capacitor converter.

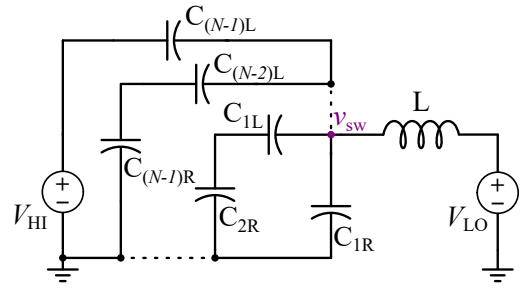
ability to regulate the output voltage, as will be discussed below.

Topology Description

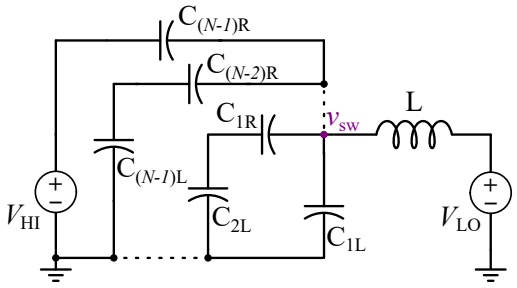
A new hybrid switched-capacitor (SC) topology (Fig. 6.3) evaluated in this work combines several techniques that make this converter especially attractive for off-battery low-voltage automotive converters. As a variation on the hybrid Dickson converter [27,43], this topology – the hybrid interleaved-input, single-inductor Dickson (HISID) converter [22,23,118] – takes a similar approach to reducing current and voltage ripple at the input and output ports – thereby reducing filtering requirements at those ports – as the two-phase interleaved stacked-ladder in [11]. However, in this work, the base topology does not require this bulky capacitor column because it is inherently interleaved with a single inductor on the output instead of two tank-configured inductors in the stacked-ladder topology. While the interleaved stacked-ladder in [11] requires $4N$ switches for an $N:1$ conversion, the proposed topology only requires $2N+4$. Moreover, the HISID converter is capable of continuous forward conduction allowing for regulation through selective phase insertion [77] without incurring increased circulating currents, albeit while sacrificing some zero-current switching (ZCS)/ zero-voltage switching (ZVS) capability.

In the proposed converter, the interleaved nature of the input allows charge to flow from the high-side source during portions of *both* phases (Fig. 6.6), rather than just one phase as is typical with many two-phase converters. Because of this characteristic, the rms value of the input current is reduced compared to the non-interleaved single-inductor Dickson topology [22], thereby reducing the necessary input capacitance. This is very helpful for achieving high power density of the total power conversion system and can help simplify any input filter design.

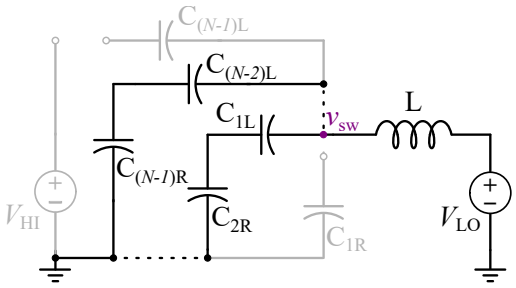
As described in [12, 31, 33], the family of Dickson-style converters, exemplify minimal



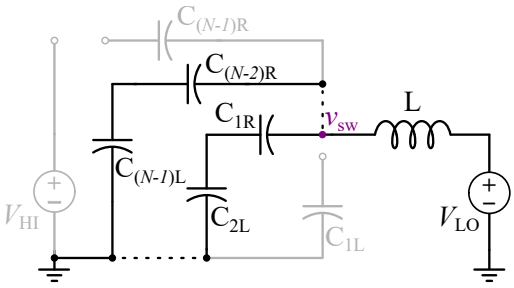
(a) Phase 1a.



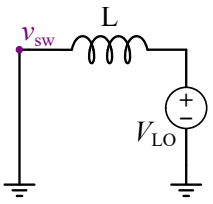
(d) Phase 2a.



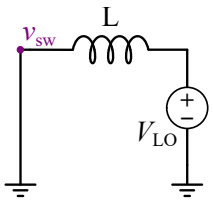
(b) Phase 1b.



(e) Phase 2b.



(c) Phase 1c.



(f) Phase 2c.

Figure 6.4: Equivalent circuits for each sub-phase of a regulating 8-to-1 Dickson converter, with split-phase switching and regulating sequence as ordered a-f: Phase 1a → Phase 1b → Phase 1c → Phase 2a → Phase 2b → Phase 2c.

total switch stress. Furthermore, the inductor at the low-side port of the converter not only allows for resonant and above-resonant operation, but serves as an output EMI filter, as well as facilitating soft-charging of the flying capacitors [41, 77]. While there are many facets of this topology that make it attractive for both EMI and automotive applications, it does require split-phase operation to maintain soft-charging of the flying capacitors, which is an additional control challenge. Split-phase operation refers to the introduction of two sub-phases within the main switching phases and is discussed in more detail in Chapter 4.

Circuit Operation

Exemplar gating signals and corresponding converter operation waveforms for an 8:1 (N=8) interleaved-input, single-inductor Dickson converter are shown in Fig. 6.6 and equivalent circuits for each phase (and sub-phase) in Fig. 6.4. Assuming only two-phase operation is required, all odd-numbered switches ("bridge" switches S_1, S_3 and "string" switches $S_5 - S_{19}$) are turned "ON" during Phase 1 and all even-numbered switches ("bridge" switches S_2, S_4 and "string" switches $S_6 - S_{20}$) are turned "ON" during Phase 2.

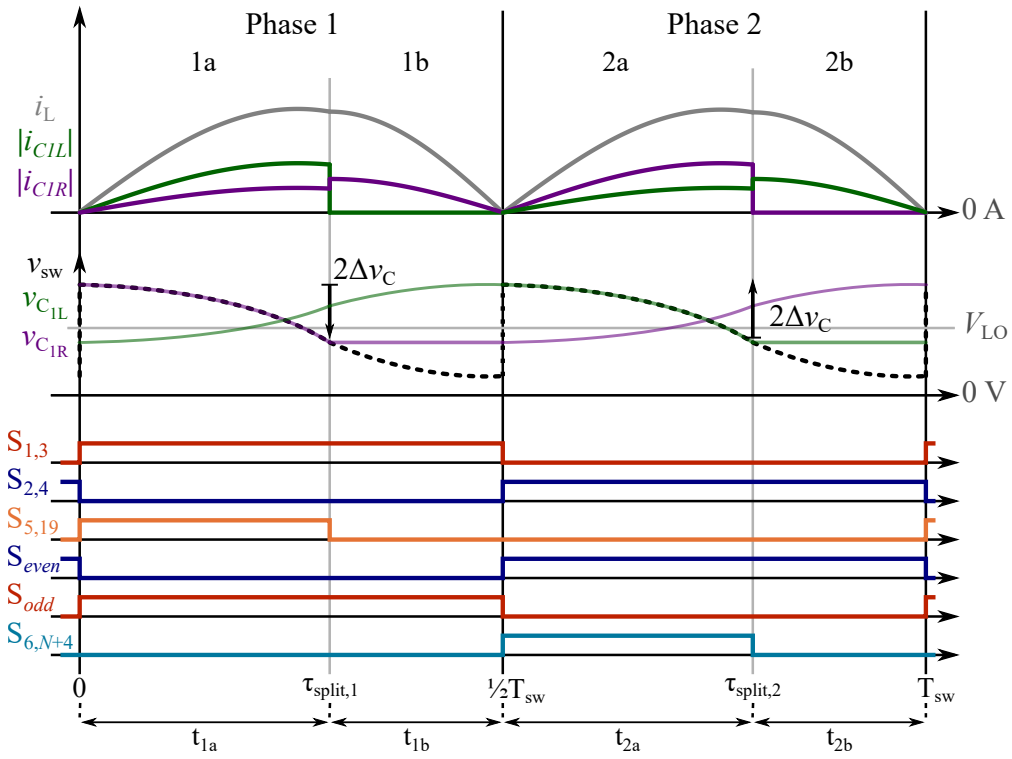


Figure 6.5: Switching scheme and exemplar converter waveforms for split-phase switching of the interleaved-input hybrid Dickson converter operating at the resonant switching frequency.

Due to this topology's interleaved symmetry, sizing flying capacitors such that $C_{xL} = C_{xR}$ for $x = 1 : N - 1$, enforces Phase 1 (Fig. 6.4a) and Phase 2 (Fig. 6.4d) to have equivalent effective capacitance as seen by the inductor. Since the singular inductor at the output is engaged with an identical capacitor network during both phases, Phase 1 and Phase 2 are equivalent, thereby simplifying the analysis of this topology. Furthermore, the converter can operate with a 50% duty cycle for Phases 1 and 2. This implementation imposes a twice-frequency voltage ripple at the switch node and a current through the inductor which has a frequency twice that of the switching frequency.

There is, however, one caveat to maintaining soft-charging of the flying capacitors and subsequent high passive utilization: split-phase operation is required. Detailed in Chapter 4, split-phase operation describes the introduction of sub-phases within the two main switching

phases to ensure soft-charging of the flying capacitors through the output inductor. Without these additional switching states, large current spikes occur at phase transitions due to mismatched loop voltages. These hard-charging events have a negative impact on efficiency, passive utilization, and EMI performance. Example waveforms showing the split-phase and subsequent soft-charging of capacitors $C_{1\mathrm{R}}$ and $C_{1\mathrm{L}}$ in Phases 1 and 2, respectively, are provided in Fig. 6.5

In this work, to satisfy voltage loops at phase transitions, the sub-phases 1b (Fig. 6.4b) and 2b (Fig. 6.4e) are inserted between the transition from Phase 1a to 2a and from 2a to 1a, respectively. Since capacitors $\{C_{1R}, C_{7L}\}$ and $\{C_{1L}, C_{7R}\}$ are not series-connected to other capacitors during Phase 1a and Phase 2a, respectively, these capacitors accrue charge more quickly than the other flying capacitors (assuming all capacitors are equally sized). Switches S_5 and S_{19} (Phase 1b) and Switches S_6 and S_{20} (Phase 2b) turn "OFF" to remove capacitors $\{C_{1R}, C_{7L}\}$ and $\{C_{1L}, C_{7R}\}$ from the circuit before they are reconnected in a different configuration for the following phase. Satisfying the voltage loops requires correct timing of the "b-phase" durations and placement within the primary Phases 1 and 2.

Owing to the requirement for split-phase switching, input switches S_{19} and S_{20} turn "OFF" towards the end of primary Phases 1 and 2, respectively, thereby disconnecting the input source. As such, while the input current is not fully continuous throughout each period, there is still significant improvement over a single-ended topology, where the input current would be zero for the entirety of one phase.

Selection of desired switching frequency is non-trivial, as the converter can be run above resonance to reduce losses. The resonant frequency is set by the value of the passives, and the ratio of f_{sw}/f_{res} can then be tuned for best performance. Considerations for switching losses and conduction losses, as well as the EMI regulatory frequency range [2] and resultant EMI filter size inform the choice of switching frequency and resonant frequency (and thereby the inductor and capacitor values). Tradeoffs of different operating regimes of this Dickson-variant converter topology are explored in detail in [22]– specifically, how the choice of switching frequency impacts efficiency and EMI performance. An advantage of above-resonant operation is the ability to operate in continuous conduction mode (CCM) and regulate the output voltage, a requirement for PoL converters. Additionally, operation of hybrid SC converters above resonance provides immunity to component mismatch, which enables the use of high energy density, Class II ceramic flying capacitors [42, 119].

Output Voltage Regulation

The topology demonstrated in this work achieves a fixed-conversion ratio when operated with 50% duty cycle. However, due to the output configuration (specifically, output inductor, L, and switches $S_1 - S_4$), this Dickson-variant converter can also be viewed as a fixed ratio switched-capacitor network merged with a buck converter at the output. These switches can then be controlled to regulate the output voltage to any value lower than the fixed-conversion ratio output. This chapter focuses on validating the converter for operation with a regulated 5 V output. This voltage level was chosen as the 5 V bus is an important low voltage rail

in an automotive subsystem and supplies downstream loads such as processors, sensors, and in-vehicle networks.

To regulate the output voltage to a level lower than the fixed-ratio output, in this case regulating from 6 V to 5 V, a regulation sub-phase (t_{1c} and t_{2c} in Fig. 6.6) is inserted within each main switching phase, wherein the output inductor is shorted to ground [119, 120]. Phase 1 consists of Phase 1a (Fig. 6.4a), its corresponding split-phase, Phase 1b (Fig. 6.4b), and its regulating sub-phase, Phase 1c (Fig. 6.4c). Similarly, Phase 2 consists of Phase 2a (Fig. 6.4d), Phase 2b (Fig. 6.4e), and Phase 2c (Fig. 6.4f). During the regulating intervals, switches $S_5 - S_{20}$ are off and the current through inductor L freewheels via the four bridge switches, $S_1 - S_4$. The duration of each regulation sub-phase is set according to the required output voltage and the relationship between the switching frequency and resonant frequency.

Because regulating operation requires above-resonance operation and has an additional sub-phase inserted, an iterative solver is required to determine the phase timings which ensure the output voltage regulation as well as capacitor soft-charging. The process for determining these phase duration is similar to the steps described in (Chapter 4) for above-resonant operation, but now with the addition of the regulating phase, wherein the inductor current is linear. Expressions for the time-domain circuit descriptions are provided in Table 6.2 for an even-N regulating hybrid Dickson converter. The HISID has equivalent inductor voltage expressions as the single-ended hybrid Dickson converter, except the equivalent capacitances in each phase are different.

Table 6.2: Time-Domain Circuit Dynamics Expressions - Phase 1 of even-N regulating hybrid converter

Parameter	Expression	Known Value
$i_{\mathrm{L}}(0)$	$i_{\mathrm{L}}(0)$	
$v_{\mathrm{L}}(0)$	$\frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}$	$= \frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}$
$i_{\mathrm{L}}(\tau_{\mathrm{split,1}})$	$i_{\mathrm{L}}(0)cos(\omega_{1\mathrm{a}}t_{1\mathrm{a}}) + \frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}\sqrt{\frac{C_{\mathrm{e,1a}}}{L}}sin(\omega_{1\mathrm{a}}t_{1\mathrm{a}})$	
$v_{\mathrm{L}}(\tau_{\mathrm{split,1}})$	$\frac{2\Delta v_{\mathrm{c}}\cdot(N-1)}{N}cos(\omega_{1\mathrm{a}}t_{1\mathrm{a}}) - \sqrt{\frac{L}{C_{\mathrm{eq,1a}}}}i_L(0)sin(\omega_{1\mathrm{a}}t_{1\mathrm{a}})$	$= -\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right)$
$i_{\mathrm{L}}(\tau_1)$	$i_{\mathrm{L}}(\tau_{\mathrm{split,1}})cos(\omega_{1\mathrm{b}}t_{1\mathrm{b}}) + -\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right)\sqrt{\frac{C_{\mathrm{e,1b}}}{L}}sin(\omega_{1\mathrm{b}}t_{1\mathrm{b}})$	
$v_{\mathrm{L}}(\tau_1)$	$-\left(\frac{2\Delta v_{\mathrm{c}}}{N}\right)cos(\omega_{1\mathrm{b}}t_{1\mathrm{b}}) - \sqrt{\frac{L}{C_{\mathrm{eq,1b}}}}i_L(\tau_{\mathrm{split,1}})sin(\omega_{1\mathrm{b}}t_{1\mathrm{b}})$	$= -\frac{2\Delta v_{\mathrm{c}}\cdot(N+1)}{N}$
$i_{\mathrm{L}}(T_{\mathrm{sw}}/2)$	$i_{\mathrm{L}}(\tau_1) + \frac{-V_{\mathrm{LO}}}{L}\cdot t_{1\mathrm{c}}$	$= i_{\mathrm{L}}(0)$
$v_{\mathrm{L}}(T_{sw}/2)$	$-V_{\mathrm{LO}}$	$= -V_{\mathrm{LO}}$

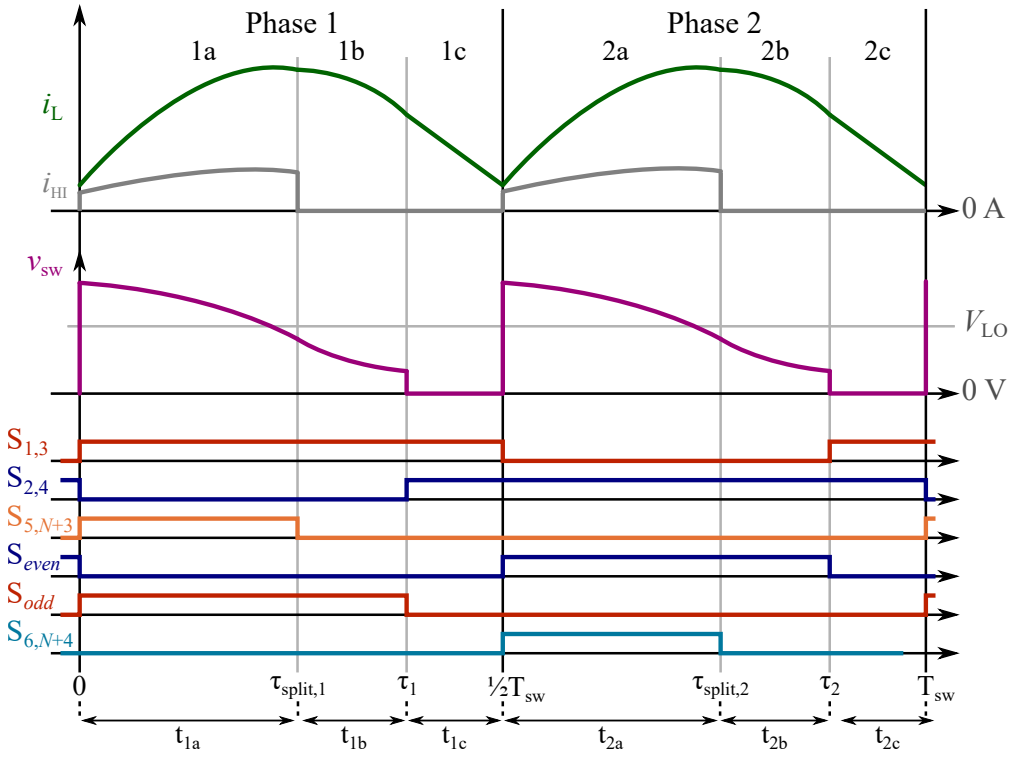


Figure 6.6: Switching scheme and exemplar converter waveforms for output voltage regulation of the interleaved-input hybrid Dickson converter operating at a switching frequency faster than resonance.

6.3 EMI Mitigation Techniques

Automotive power converters are generally placed in close proximity to other in-vehicle electronics, many of which are susceptible to EMI. Thus, the high di/dt and dv/dt associated with the power converter switching transitions (made steeper by the implementation of high-speed, wide-bandgap power transistors such as GaN devices) must be mitigated [121, 122]. In automotive systems, the allowable EMI noise levels are standardized in CISPR 25, with Class 5 limit requirements [2]. The EMI spectrum is measured over the frequency range of 150 kHz to 108 MHz and there are peak, quasi-peak, and average noise limits set within this range. A summary of the specifications for this standard are presented in Table 6.3. Full compliance testing requires peak, quasi-peak, and average detectors, however, both the quasi-peak and average data cannot exceed the peak levels [123]. In this paper, peak EMI data is reported to understand "worst case" noise levels for the converter, and average data is reported to more clearly demonstrate the positive impact of the SSFM technique on noise levels. EMI noise is related to topology as well as PCB design in parasitic elements, copper traces, and ground planes [122, 124, 125].

Both conducted and radiated emissions are regulated, however, this work focuses on re-

ducing the conducted emissions of the converter — in this case, measured in a pre-compliance setup, which provides a good indication of overall EMI performance. Radiated emissions measurements are more difficult to perform and involve the use of a large, fully shielded anechoic chamber, and so were not carried out in this work. While the CISPR 25, Class 5 standard sets limits for the total noise in the system, it can be helpful to split this noise into its sub-components to determine noise origins.

Noise from conducted emissions can be broken down into two different types: common mode (CM) and differential mode (DM), shown in Fig. 6.7. CM refers to noise in which the direction of the "noise currents" on the positive and negative lines of the power converter have the same direction. DM refers to noise in which the direction of the "noise currents" on the positive and negative lines of the power converter have the opposite direction. CM noise increases with increasing parasitic capacitance in the power stage and peak switched output voltage [113,126,127]. On the other hand, DM noise is increased by increasing current through the converter. Higher load current will exacerbate the impact of parasitics in larger current loops throughout the power stage [113].

Here, we measure the EMI at the input side which is connected to the 48 V bus because the bus voltage should be stiff and free of excess injected noise. For applications which utilize a distribution bus, such as the 48 V bus in automotive power trains, it is crucial to shield the bus from noise generated by switching converters. Therefore, for this application, we are primarily interested in the CM and DM noise as seen by the high-side (or 48 V input) source. At the low side port, there are other PoL converters downstream and therefore, noise is of a slightly lower concern than the input port.

There are several ways to reduce conducted EMI in switching power converters. EMI mitigation starts with power converter layout best practices such as strategic component placement, loop area minimization, and effective grounding and shielding techniques. EMI filters are also a common addition to the front-end of a power stage and can be tuned to mitigate problematic noise peaks within the EMI measurement range. Additionally, spread

Table 6.3: Conducted Noise Limits for CISPR 25, Class 5 EMI Standards [2]

Band	Frequency (MHz)	Limit (dBμV)	
		Peak	Average
LW	0.15-0.3	70	50
MW	0.53-1.8	54	34
SW	5.9-6.2	53	33
FM	76-108	38	18
TV	41-88	34	24
CB	26-28	44	24
VHF I	30-54	44	24
VHF II	68-87	38	18

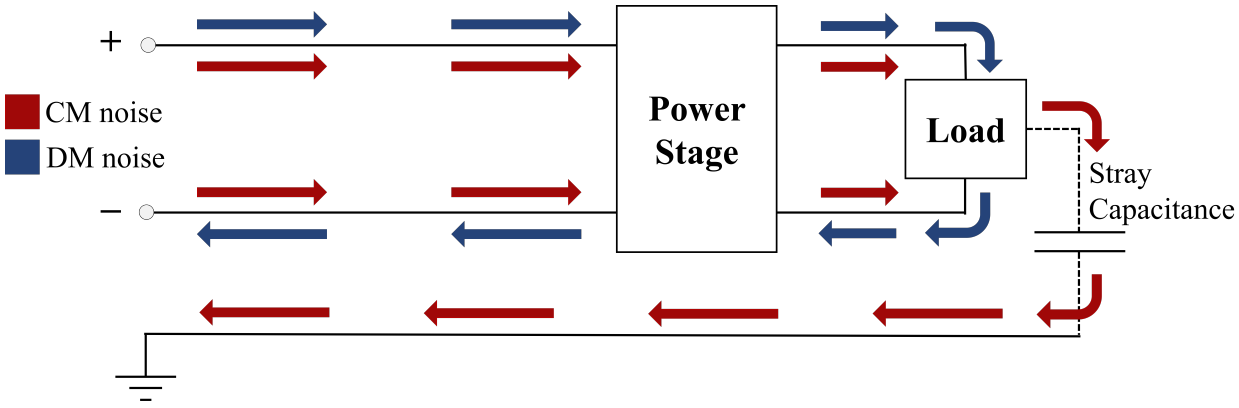


Figure 6.7: Common Mode and Differential Mode noise paths through the system.

spectrum frequency modulation (SSFM) is a well-known control technique that involves using a variable switching frequency to spread the noise peaks across a range of frequencies to reduce conducted EMI [112]. Different SSFM schemes and their specific impacts on converter EMI are explored in more detail in [22] In this work, the Dickson converter layout is designed to minimize potential sources of noise and an SSFM scheme is implemented to further spread out the noise peaks and reduce filter size. To address any additional noise that is still above regulatory limits, a passive front-end EMI filter is built into the prototype.

Spread-Spectrum Frequency Modulation (SSFM)

Because EMI filters add to overall passive component volume and loss, spread spectrum, or "dithering", frequency techniques can also be used to further reduce conducted EMI that is generated by fixed-frequency switching schemes. Spread-spectrum frequency modulation (SSFM) is a control technique that uses a variable switching frequency to reduce conducted EMI [112, 128–130]. To implement this, the converter's periodic switching frequency can be modulated, or dithered, and therefore spread out the original energy of each harmonic about a specified frequency band. This provides a wider spectrum with lower peak amplitudes. There are a variety of periodic and random SSFM methods that can be used to achieve this goal [112, 128–131], several of which are compared in this chapter.

The fundamental parameters for the frequency modulation profiles are:

f_c	Center frequency, or nominal frequency about which the switching frequency is dithered.
Δf_c	Step size of frequency dithering.
$T_m = \frac{1}{f_m}$	Period/frequency of modulation profile.
A_m	Maximum deviation of switching frequency from center frequency, f_c.

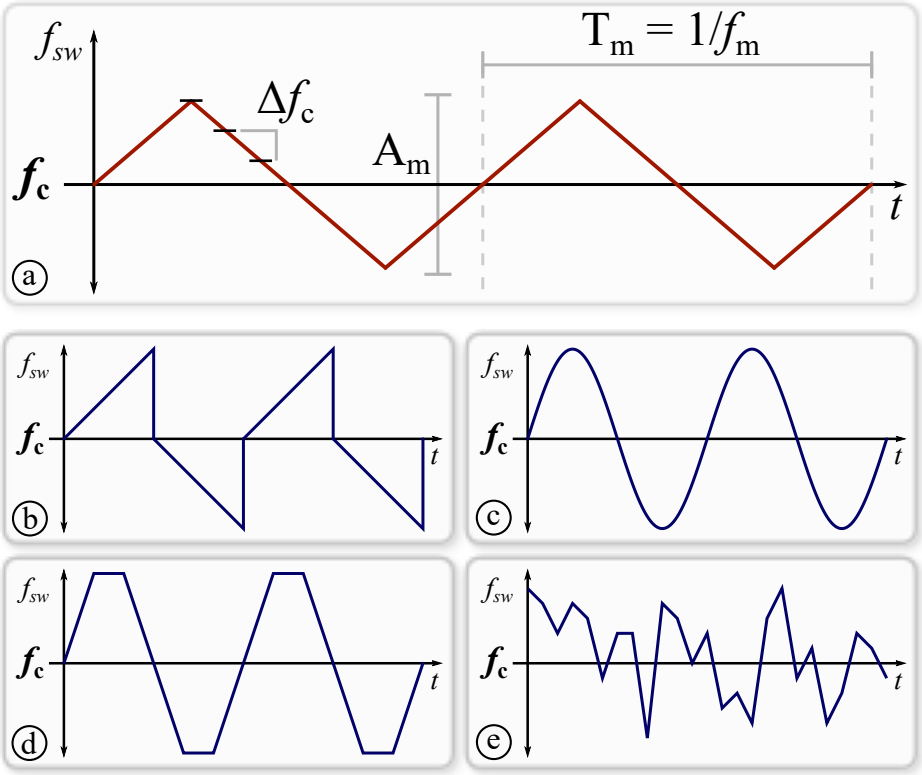


Figure 6.8: Modulated switching frequency over time and key parameters for various SSFM schemes: a) triangular, b) right-triangular, c) sinusoidal, d) trapezoidal, and e) pseudo-random.

Five modulation schemes – right-triangular, triangular, trapezoidal, sinusoidal, pseudo-random – tested in this work (with the execption of pseudo-random) are shown in Fig. 6.8. The EMI effects of changing parameters Δf_c, f_m, and A_m are presented in Section 6.4.

Moreover, implementing SSFM can have impacts on efficiency. Fig. 6.9 plots the effective output resistance of an example SC converter operating in discontinuous conduction mode (DCM) for $f_{sw}/f_0 < 1$ and continuous conduction mode (CCM) for $f_{sw}/f_0 > 1$. Hard-charging and split-phase operation are also shown [1]. Because this work focuses on at- and above-resonant operation, the simplified output resistance plot of Fig. 6.9 is a good reference in analyzing the impacts of SSFM on this work's converter operation.

Except for the pseudo-random scheme, each of these modulation profiles follows a periodic pattern. Ramping the switching frequency up and down avoids noise spiking at any specific frequency and its harmonics [112], but because the switching frequency is being manipulated periodically, one drawback of these methods is that both the input and output voltages can acquire a periodic ripple at the modulation frequency. Therefore, the modulation frequency should be chosen to be sufficiently slow (e.g., 100 times slower than the switching frequency) to avoid too much overlap with the fundamental frequency and its harmonics. Moreover, a

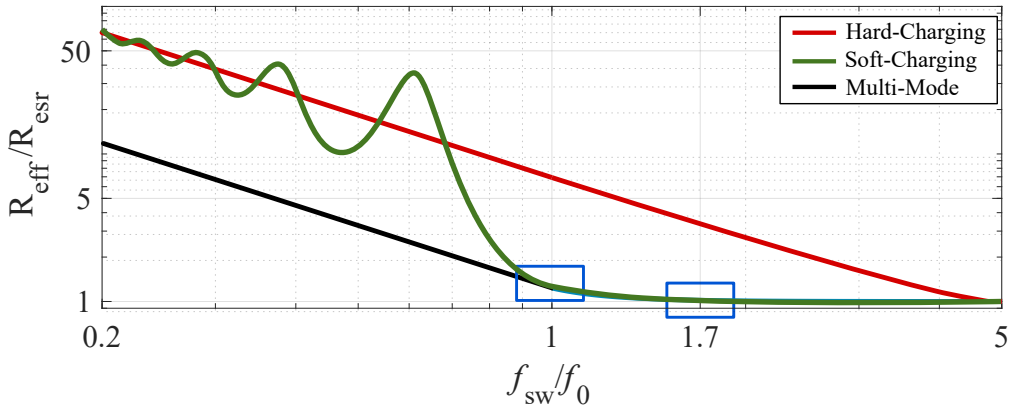


Figure 6.9: Effective output resistance versus frequency of an exemplary pure, resonant, and multi-mode hybrid SC converter [1] with regions of frequency dithering highlighted.

pseudo-random scheme can help overcome the challenges presented by periodic SSFM.

As a final note, the EMI benefits from SSFM may not outweigh the negative impacts on efficiency when operating near resonance, but may be significant for above-resonant operation of the converter [22]. As the switching frequency becomes greater than the resonant frequency, the effective output resistance, R_{eff}, approaches its limit, R_{esr}, which is the effective series resistance of the power components, and represents the lowest possible output resistance [119]. Consequently, operating with a center frequency sufficiently above resonance and with a relatively small dithering band, the losses for the converter remain relatively constant across the SSFM frequency range. In this work, the above-resonance switching frequency of the converter prototype is chosen to keep the fundamental switching harmonic below 150 kHz, the lowest end of the EMI regulatory frequency range [2].

Layout Considerations

Switching converter layout and component placement can have a significant impact on converter noise, and prior work has shown that EMI performance can be improved by minimizing commutation loop parasitic inductance [132]. Typically, power converter topologies which comprise half-bridge modules (e.g., FCML [133] and Series-Capacitor Buck [134]) have relatively simple commutation loops that are easier to minimize in layout. However, for hybrid SC topologies, which have not only more switches, but more complex circuit connections, optimization of commutation loops becomes more complex. In a hybrid SC converter, *each* switch of Phase 1 forms a commutation loop with *each* switch of Phase 2. For example, the 8-to-1 HISID converter has $10 \times 10 = 100$ commutation loops formed. Topologies such as the Dickson converter have many commutation loops overall, but also many loops per switch. It is most effective to layout the switch network in such a way as to create a single very small commutation loop per switch, rather than only slightly minimizing multiple loops per switch. Generally, there is a trade-off between power stage size, PCB loss, and commutation

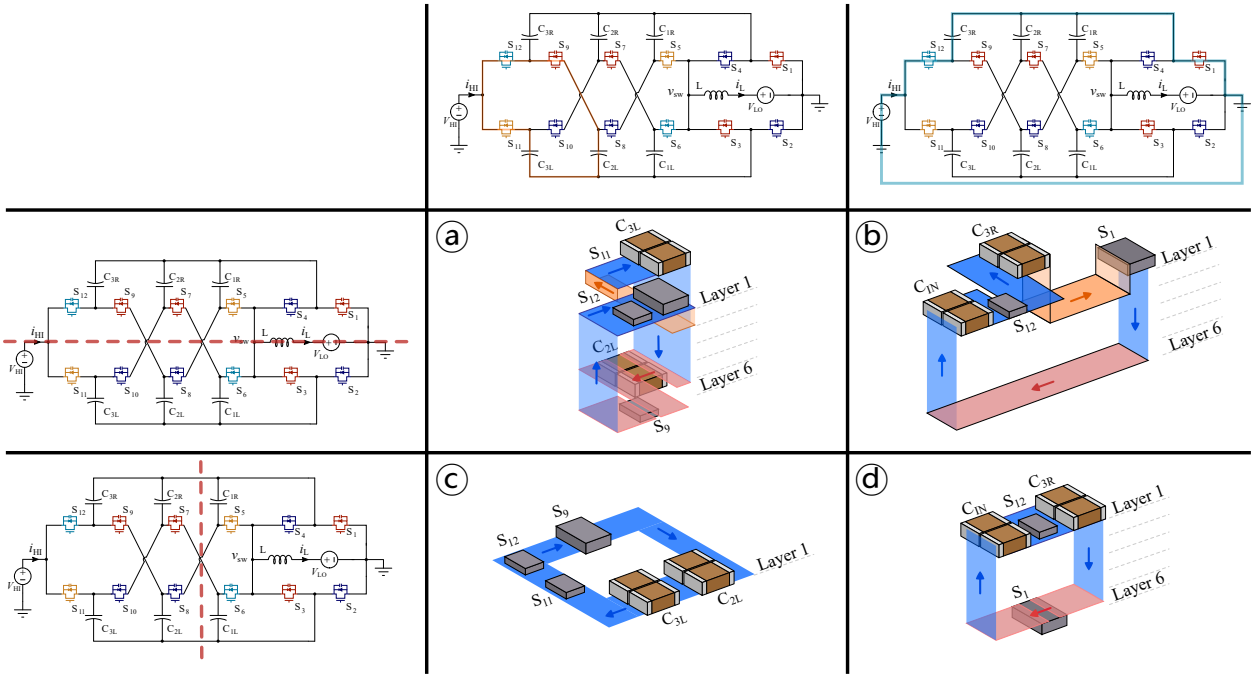


Figure 6.10: Commutation loop comparison for different layout configurations of the HISID converter.

loop size in layout design. And for the HISID converter, minimizing commutation loops may also reduce PCB loss in addition to reduced switching noise and switching loss.

The layout configuration for the HISID converter shown in the second row of Fig. 6.10, wherein the converter is wrapped back on itself (aptly coined as the 'hamburger' fold) is more advantageous than the configuration folded down the 'spine' of the converter ('hotdog' fold) for many reasons. Firstly, it reduces the loss associated with PCB trace resistance. As an example, the PCB trace resistance of S_{12}, C_{3R}, and S_1 through the ground return path is significantly reduced with this layout (Fig. 6.10d) because switch S_{12} is placed directly on top of S_1 (i.e., one switch on the top side and one on the bottom) rather than on the other end of the board (Fig. 6.10b). Finally, the commutation loop inductance is also reduced using the new layout configuration due to the reduced loop area. The comparison between the two different layouts is shown in Fig. 6.10.

6.4 Experimental Prototype

An 8-to-1 discrete hardware prototype was constructed to verify operation as well as to explore efficiency and EMI trade-offs of the proposed interleaved-input single-inductor Dickson converter (Fig. 6.11). The experimental prototype, measuring 24 mm x 97 mm x 9.6 mm, utilizes mixed switch technologies (both Si and GaN) to optimize for on-state resistance ($R_{\mathrm{DS_{on}}}$), drain-to-source voltage (V_{DS}), and gate charge (Q_{G}). The results of these trade-offs are different for automotive-rated switching devices versus commercial-rated parts. Though the blocking voltage of the switches is only $\sim 6\,\mathrm{V}$ or $\sim 12\,\mathrm{V}$, automotive parts at the 40 V rating were chosen due to lower $R_{\mathrm{DS_{on}}}$ and Q_{G}. Furthermore, Si was chosen for most of the switches because at low voltages, Si devices have better FOMs than GaN devices to this date. The input switches $S_{19} - S_{20}$ were selected for a higher-voltage rating ($> 80\,\mathrm{V}$) to account for start-up transients at input voltages up to ∼60 V. Furthermore, physically larger Si devices for switches $S_1 - S_4$ were chosen to minimize $R_{\mathrm{DS_{on}}}$ with only a small power density penalty. These 'bridge' switches conduct the full output current when ON and therefore loss reduction was prioritized over component area. Both Cascaded Bootstrap and Gate-Driven Charge Pump methods [106] are used for bootstrapping in the gate drive power circuit. Furthermore, all components (Table 6.4) on the board are automotive-qualified so as to adhere to the Automotive Electronics Council (AEC) standards. Inductor and capacitor values were chosen to give a resonant switching frequency of 81 kHz, a frequency whose fundamental is

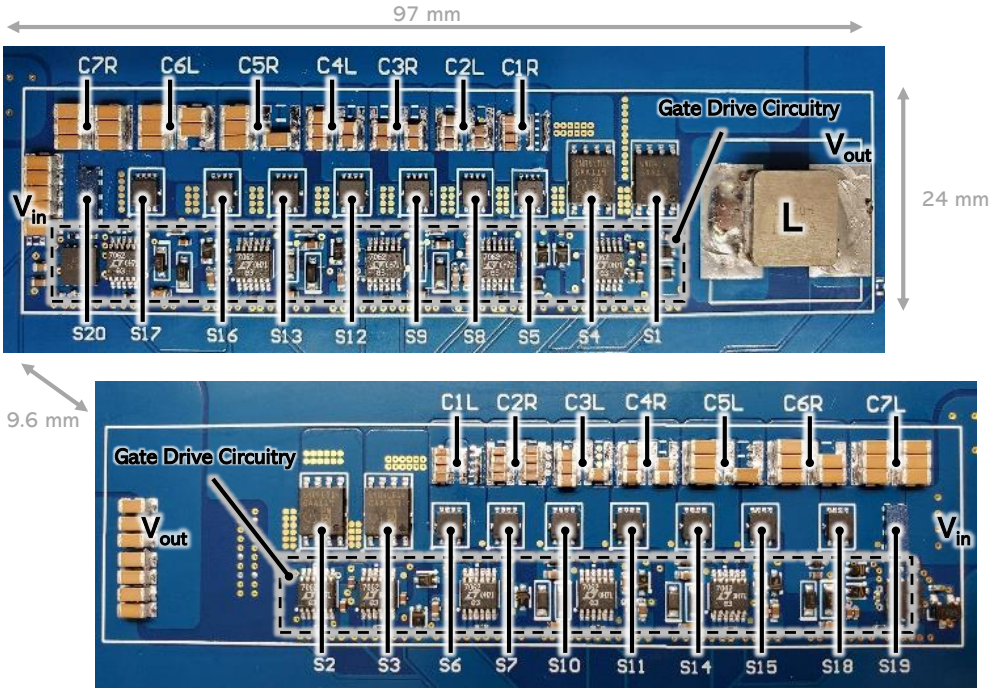


Figure 6.11: Image of prototype board with key components labeled.

Table 6.4: Component Listing of the Hardware Prototype

Component	Mfr. & Part Number	Parameters
Dickson Power Stage		
Start-up Switches S_{19} - S_{20}	EPC EPC2206	GaN, 80 V, 2.5 mΩ
String Switches S_5 - S_{18}	ON Semi NVTFS002-N04CL	Si, 40 V, 3.5 mΩ
Bridge Switches S_1 - S_4	Infineon IAUC100-N04S6L014	Si, 40 V, 1.4 mΩ
Flying Capacitors C_{1x}, C_{2x}	Murata GRT188R61H225KE13	X5R, 50 V, 2.2 μF (x5, x6)
C_{3x}, C_{4x}	TDK CGA4J3X5R1H475K125AB	X5R, 50 V, 4.7 μF (x3, x4)
C_{5x}, C_{6x}, C_{7x}	TDK CGA5L3X5R1H685K160AB	X5R, 50 V, 6.8 μF (x4, x5, x6)
Inductor L	Vishay Dale IHLP4040DZERR19MA1	0.19 μH, 90 A I_{sat}
Gate Drive		
GaN Driver	TI LM5113QDPRRQ1	90 V, high and low-side
LDO	Microchip MCP1792T-5002H	5.0 V, 100 mA
Si Gate Driver	Analog Devices Inc. LTC7062IMSE	Dual high-side driver
Charge Pump Driver	Analog Devices Inc. LTC7062IMSE	Dual high-side driver
Bootstrap Diodes	Nexperia PMEG6002EJ,115	Schottky, 60 V, 200 mA
Charge Pump Diodes	Diodes Inc. PD3S230L-7	Schottky, 30 V, 2 A
Charge Pump Capacitors	Murata GRT188R61H225ME13D	X5R, 50 V, 2.2 μF
Controller Board		
FPGA	Terasic Inc. P0466	DE10-Lite, Max10 FPGA

Table 6.5: Converter Operating Parameters

Parameter	Value	Units
V_{in}	48	V
V_{out}	6	V
$P_{out,max}$	120	W
f_{sw}	50-200	kHz
f_{res}	81	kHz

below the lowest relevant EMI frequency band. Table 6.5 defines the operating parameters for this prototype.

Both inductor current, i_L, and switch-node voltage, v_{sw}, waveforms are shown in Fig. 6.12 for at-resonant and above-resonant (fixed-ratio and regulating) operation of the hardware prototype at the conditions listed in Table 5.2. These two modes of operation correspond to the two regions highlighted in 6.9. As discussed above in Section 6.2, operating the hybrid SC converter above resonance comes with reduced rms currents compared to resonant operation. This is beneficial when the converter needs to be pushed to higher load currents, a regime where conduction loss dominates [22]. Output voltage regulation (implemented as discussed in Section 6.2) exhibits higher rms currents compared to operating at a fixed-conversion ratio, incurring more conduction losses in the switches and magnetics. Furthermore, switches $S_1 - S_4$ conduct for a longer amount of time (depicted in Fig. 6.6), again resulting in increased

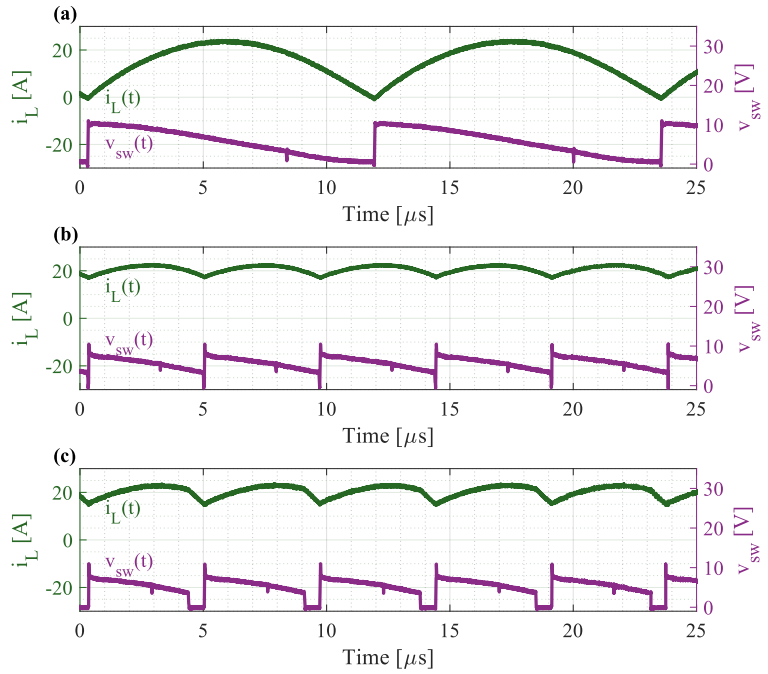


Figure 6.12: (a) Resonant, (b) above resonant, and (c) regulating inductor current, i_L, and switch-node voltage, v_{sw}, measured waveforms for the 8-to-1 discrete hardware prototype.

losses. Higher di/dt transitions in the regulating case also contribute to higher core loss in the inductor [120].

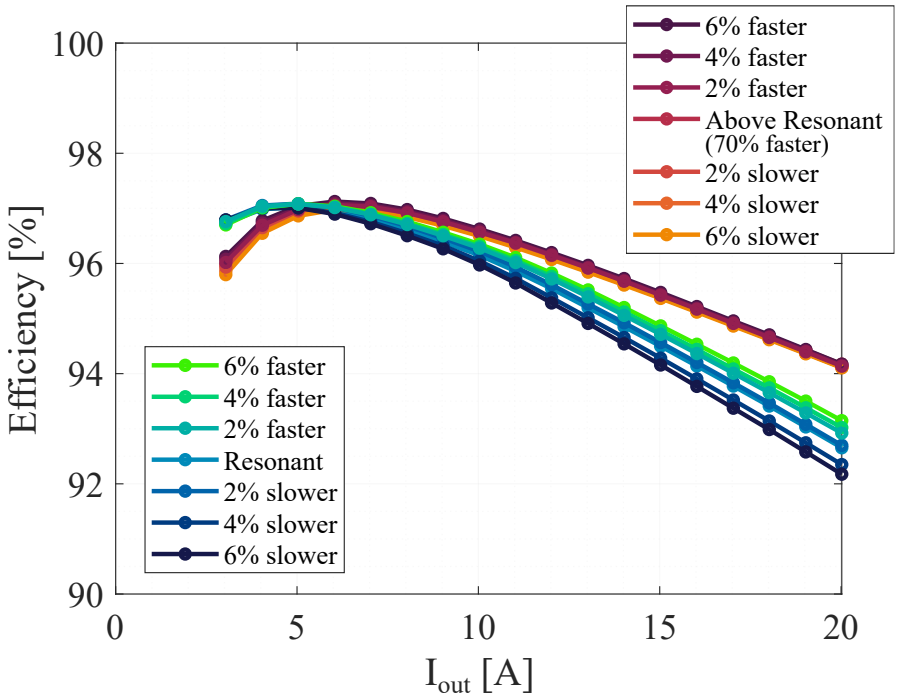


Figure 6.13: Static efficiency plots for frequency bands near resonant and above-resonance operation at 48 V input and un-regulated 6 V output.

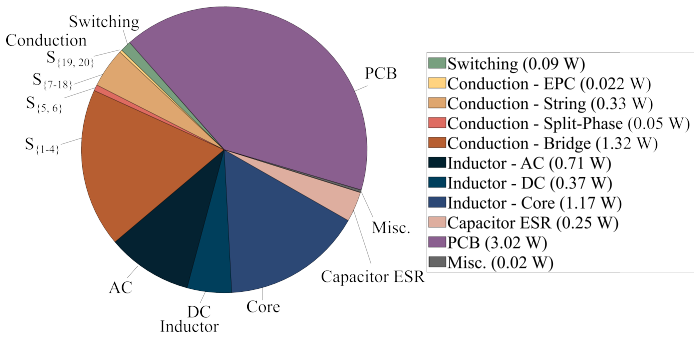
Efficiency Measurements

As discussed above, the mode of operation can impact the efficiency of the converter, especially when comparing resonant (i.e. ZCS) operation with above-resonant operation (i.e. faster switching). Efficiency curves for a range of frequencies around resonance and faster than resonance are presented to compare switching frequency effects on power loss. Additionally, efficiencies were recorded for various switching frequencies with and without utilizing SSFM schemes to demonstrate how SSFM impacts (or does not impact) efficiency.

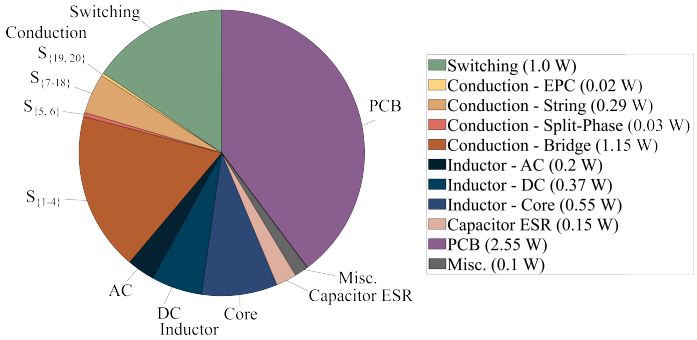
Fig. 6.13 depicts static (meaning no SSFM is employed) efficiency curves for several switching frequencies around resonance and around the frequency 70% faster than resonance. The spread of efficiency lines for resonant and above-resonant operation agree with behavior estimations in Fig. 6.9: for a frequency spectrum around the resonant frequency, the efficiency varies with frequency. However, for operation above resonance, the converter losses are relatively constant with changes in frequency.

Moreover, as expected, resonant operation and its lower switching losses yield better light load efficiency, while the reduced RMS currents of above-resonant operation yields higher efficiency at heavy load, where conduction losses dominate.

Figures 6.14a and 6.14b show the detailed loss breakdowns for at- and above-resonance operation, respectively for a load condition of 20 A. For both modes of operation, the "bridge" switch conduction, PCB, and switching losses are the top contributors to overall loss. How-



(a) At-resonance (81 kHz and 20 A, 113 W, and 93.89% efficient).



(b) Above-resonance (143 kHz and 20 A, 113 W, and 94.62% efficient).

Figure 6.14: Power loss breakdown for hardware prototype for at and above resonance operation.

ever, as expected, the conduction losses are larger for the at-resonant case, due to larger RMS currents, whereas switching losses are a significantly larger portion of the losses when switching faster.

In the loss breakdown of each operation mode, a segment for "measured excess" loss is included. This loss is the discrepancy between the estimated losses and the measured losses. One of the most likely reasons for this disparity is from differences in actual RMS currents and ideal RMS currents. In the actual hardware prototype, because this work only uses open-loop control, the phases may not be perfectly balanced across the load range. Having unequal phase currents leads to sub-optimal current waveshapes, thereby making the RMS currents worse than what theoretical calculations predict. Furthermore, resonant operation has a larger deviation from calculated to measured, potentially due to not achieving full ZVS at this loading condition, incurring more switching loss than expected. To maintain ZVS across a load range, deadtimes need to be dynamically adjusted. Including measured excess losses, resonant (81 kHz) operation at 20 A load has a total of 7.36 W of loss, and 6.42 W for the above-resonance (143 kHz) case.

Furthermore, efficiency versus load curves (Fig. 6.15) were taken for converter operation

at various switching frequencies without SSFM as well as operation utilizing different SSFM schemes, as described in Table 6.6. For higher frequency SSFM modulation, a center frequency, f_c, of 70-75 % faster than resonance was selected. For this circuit implementation, 75% faster than resonance corresponds to 143 kHz. This frequency was chosen so that the fundamental frequency component is kept below the lowest frequency band of CISPR 25 regulations, Table 6.3.

Here, the peak efficiency is 97.27% for resonant operation at 5 A, whereas, the peak efficiency is about 97.16% for all of the 143 kHz operation modes at a load of 6 A. For operation only slightly faster than resonance, 100 kHz (about 20% faster than resonance), the peak efficiency at 5 A for SSFM Mode 5 is 97.35%. At light loads, the at-resonance efficiency exceeds above-resonance efficiency, whereas, at heavy loads, the efficiency for the above-resonance case exceeds that of the resonant case. This trend results due to conduction loss dominating over switching loss at heavy load, and so the gains seen by resonant-ZCS do not outweigh the reduction in RMS currents seen at higher switching frequencies.

Looking at the three different SSFM schemes represented in Fig. 6.15, the peak efficiency of the 100 kHz case with sinusoidal SSFM exceeds that of both the 143 kHz cases with SSFM. Among the three different efficiency curves for 143 kHz presented here, it can be seen that employing SSFM at frequencies much faster than resonance does not affect the efficiency significantly as all three curves for 143 kHz are practically indistinguishable, regardless of the spread-spectrum modulation scheme. However, the efficiency for 143 kHz operation differs from that of 100 kHz operation even though both of these frequencies are higher than resonance. The difference between these two center frequencies and why the losses are different is because 100 kHz (at only 20% faster than resonance) falls much closer to the elbow of the output impedance versus frequency plot in Fig. 6.9. This means that the output impedance and therefore losses are slightly more correlated with changes in frequency. From

Table 6.6: Definition of Converter Modes of Operation

Mode 1	81 kHz, Resonant
Mode 2	143 kHz, no SSFM
Mode 3	143 kHz, triangular SSFM, $\Delta f_c = 3.24$ kHz, $f_m = 1.43$ kHz, and $A_m = 16.19$ kHz
Mode 4	143 kHz, sinusoidal SSFM with long T_m, $f_m = 446.88$ Hz, and $A_m = 4.78$ kHz
Mode 5	100 kHz (or 143 kHz), sinusoidal SSFM with short T_m, $f_m = 625$ Hz (or 893.75 Hz), and $A_m = 35.5$ kHz (or 7.50 kHz)
Mode 6	143 kHz, right triangle SSFM, $\Delta f_c = 752.5$ Hz, $f_m = 1.43$ kHz, and $A_m = 2.26$ kHz

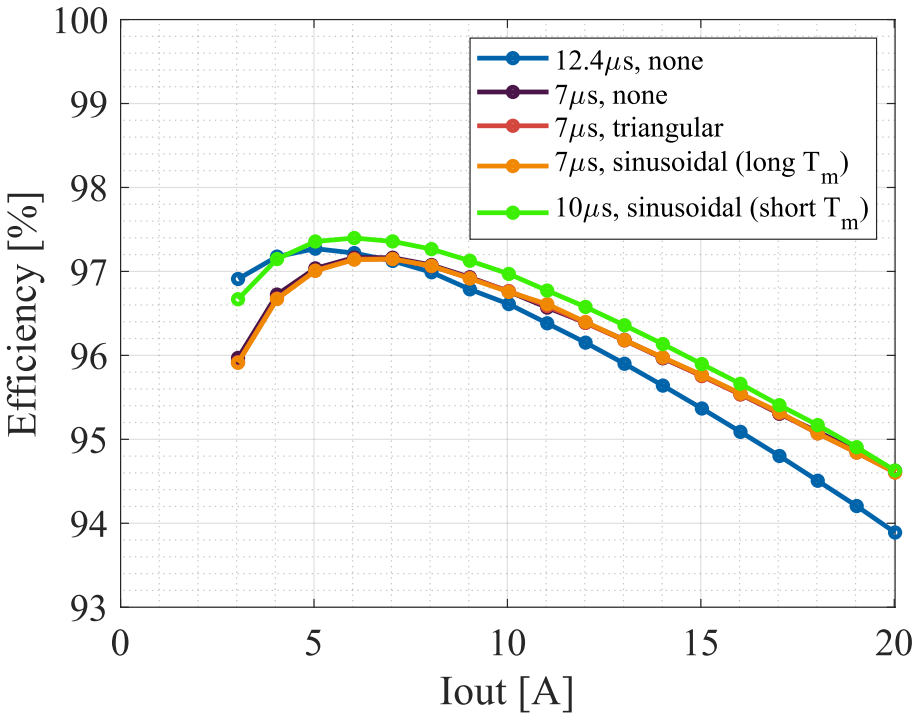


Figure 6.15: Efficiency plots for 48 V input, resonant and above-resonance operation with and without SSFM.

looking at the efficiency data for these several modes of operation, we can see the efficiency trends of operation at and above resonance, as well as the negligible impact of employing SSFM schemes on efficiency. The next section explores effects these different operational modes have on EMI performance.

EMI Measurements

In addition to low power loss, another key requirement for automotive converters is EMI emissions below standardized values. Here, we measure the EMI at the input side which is connected to the 48 V bus because the bus voltage should be stiff and without excess noise injected. At the low side port, there are other PoL converters downstream and therefore, noise is of a slightly lower concern than the input port. The measurement setup is described for the pre-compliance testbed and results for the various switching schemes - at-resonant, above-resonant, and SSFM operation – are presented and compared.

EMI Measurement Setup

Accurate measurements of EMI – conducted emissions and radiated emissions– is a difficult task. For diagnostic testing and EMI pre-compliance checking, a conducted emissions test

bench was assembled in lab, Fig. 6.16. Closely following the setup layout in the CISPR 25 standard [2], a ground plane was setup as a base for the test equipment. The input voltage supply was set up behind the ground shield to prevent any noise from the switching supply coupling into the measurements of the EMI generated from the device under test (DUT). The input voltage supply positive and return leads were connected through large filtering capacitors to 5 μH high voltage line impedance stabilization networks (LISNs) (*Solar Electronics Company 21702-5-TS-50-N*).

The LISNs present a known and precise impedance to the input of the DUT port where the noise measurement is being made. Inserting a known impedance seen at the measurement port is crucial since the output impedance of the power supply is rarely known [135]. The measurement outputs of the LISNs are connected to the spectrum analyzer [136]. Here, an *Tektronix RSA306b* was used. For aggregate EMI measurements, the spectrum analyzer is connected to one of either the positive or negative/return measurement leads from the LISNs and the other lead is terminated with 50 Ω. For insight into noise sources and informing filter design, the conducted noise measurements can also be split into common mode (CM) and differential mode (DM) noise using various methods [135, 137, 138]. The aggregate noise measurement is a vector sum of the DM and CM noise, but additional circuitry is required to decompose these two sources into their respective contributions. Here, a packaged CM/DM splitter, *Tekbox LISN Mate TBLM1* [139], was used to separate the two modes of noise. Similarly to aggregate measurements, the port that is not being measured is terminated with 50 Ω.

The output power ports of the LISNs connect to the positive and negative terminals of the DUT. If an electronic load is used, it is best to setup the load behind or under the ground shield; additionally the cables connecting the output of the DUT to the load should also be shielded.

For the low power supply needed for gate drive power and logic (either FPGA or microcontroller) power, a low voltage power supply is used. The gate drive supply is connected through another LISN to ensure there is no coupling of noise from the power supply into the EMI measurements of the DUT. Ideally, the logic supply would also be connected through a dedicated EMI filter but that is not always practical. The FPGA/microcontroller (if not part of the DUT design, like in this work) should be shielded.

Care should be taken to assemble a measurement test bench which has the lowest noise floor possible, though for practical pre-compliance measurements there may still be some environmental noise.

SSFM EMI Measurements and Comparisons

Figures 6.17-6.18 serve to make a comparison of spread-spectrum versus non-SSFM EMI performance at an input voltage of 48 V, an (unregulated) output voltage of 6 V, and a load current of 20 A. These noise measurements were taken in a laboratory, pre-compliance semi-shielded environment using the *Tektronix RSA306b*. A comparison between Mode 1 and Mode 2, as well as between Mode 1 and Mode 3, from Table 6.6 are presented. Both

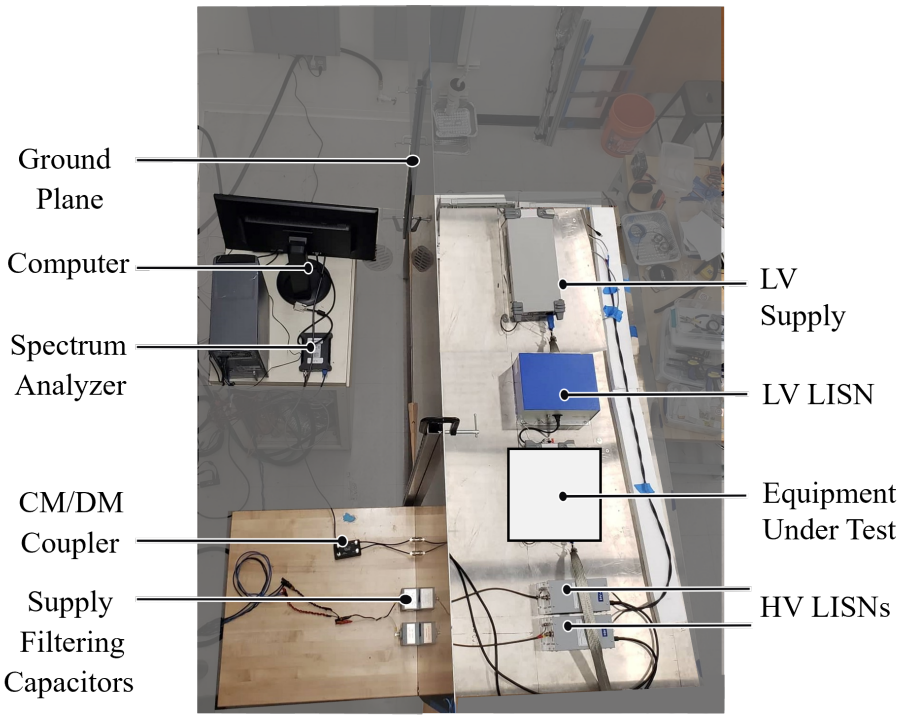
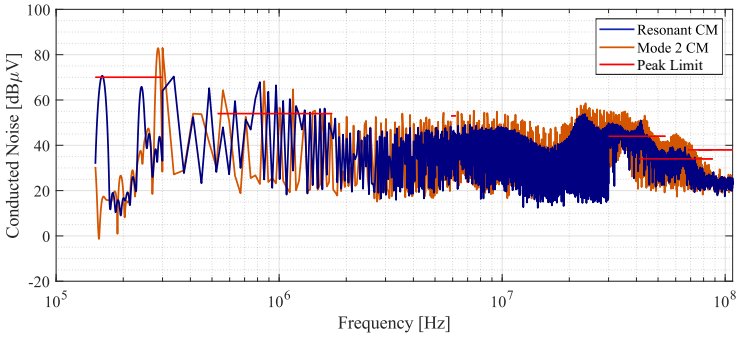


Figure 6.16: In-lab pre-compliance conducted EMI measurement setup.

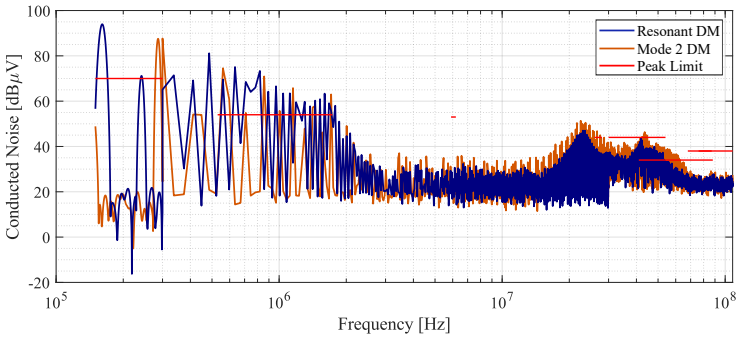
Common Mode (CM) and Differential Mode (DM) noise is shown for each case. It should be noted that in this work, we are interested in analyzing the raw EMI emissions from the converter, so no dedicated EMI filter was employed in these measurements. In Figs. 6.17 and 6.18, the blue trace corresponds to resonant operation with no SSFM employed and acts as a reference within each of the plots to compare the EMI performance of each SSFM mode.

The horizontal lines on the plots denote the CISPR 25, Class 5 standard conducted emissions limits [2] (Table 6.3). It can be seen that the peaks occur around 162 kHz and 286 kHz for at resonance and above resonance, respectively. These frequencies are consistent with twice the switching frequency (i.e. the frequency of the inductor current and switch-node voltage).

First, a comparison of resonant and above-resonant EMI performance is presented in Fig. 6.17 without the use of SSFM. For both CM and DM, the noise profiles are similar. However, the location and magnitude of peaks differ. Due to the soft-switching capability of the resonant operating mode, much of the switching noise can be eliminated, reducing the conducted noise from the converter. For CM noise, the resonant case shows noise levels only slightly above the required limits for the lowest pertinent frequency range. Comparatively, the above-resonant operating mode, while having better efficiency at this voltage and loading condition, has higher CM noise peaks (particularly at the lower frequency bands) without employing any SSFM than does the resonant case. Similar to the CM measurements, DM noise for the resonant case shows lower levels than the above-resonant case for a majority



(a) Common mode (CM) conducted emissions.



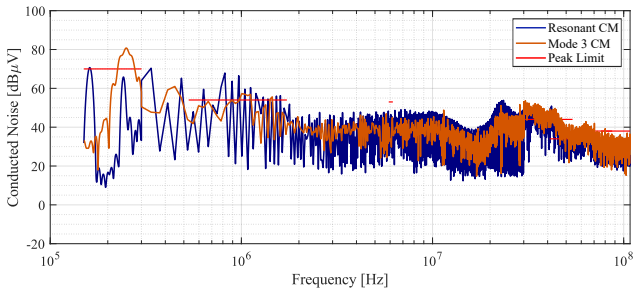
(b) Differential mode (DM) conducted emissions.

Figure 6.17: Conducted emissions for 81 kHz (blue) and 143 kHz (green) with no SSFM, Modes 1 and 2, respectively, at an input voltage of 48 V, an (unregulated) output voltage of 6 V, and a load current of 20 A.

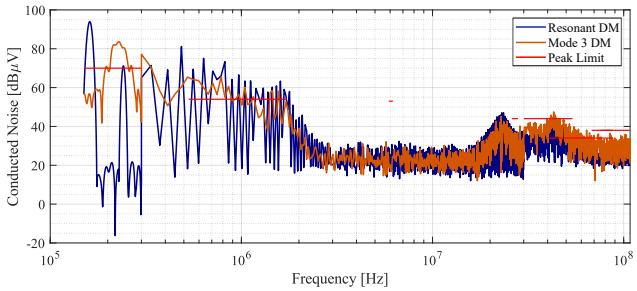
of the frequency bands. Despite generally lower peaks, resonant operation has higher noise levels in the LW band than the above-resonant case. These noise measurements in conjunction with the efficiency data discussed above indicate that there is a clear efficiency and EMI tradeoff between operating at and above resonance.

For the sinusoidal modulation schemes, two cases are presented: EMI performance for a slower, Fig. 6.19, or faster,Fig. 6.20, modulation frequency, f_m. For Common Mode noise, Modes 4 and 5 have a generally lower noise profile than the resonant case, though the peaks are very similar in magnitude and only slightly lower than Mode 2, the no-SSFM case in Fig. 6.17. At the LW and MW frequency bands, the peak-to-limit percentage has about a 10% reduction when the modulation frequency is increased (Mode 5). Furthermore, the noise profile for CM noise with the faster modulation frequency, is narrower, which will help with filter design.

Mode 6 is presented in Fig. 6.21 and is a right-triangle variation on Mode 3, whereby the switching frequency is modulated up, before returning to center for a time, and then modulated lower before returning to center. At the lower frequency range, the CM, Mode



(a) Common mode (CM) conducted emissions.



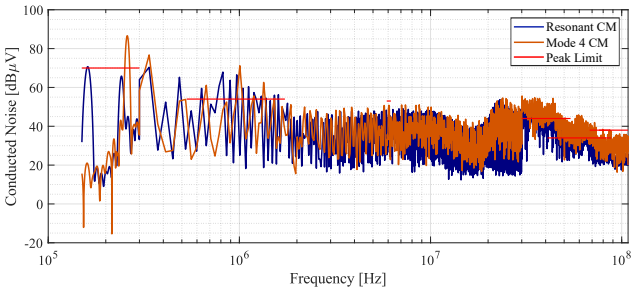
(b) Differential mode (DM) conducted emissions.

Figure 6.18: Conducted emissions for 81 kHz (blue) with no SSFM and 143 kHz (green) with triangle SSFM, Modes 1 and 3, respectively, at an input voltage of 48 V, an (unregulated) output voltage of 6 V, and a load current of 20 A.

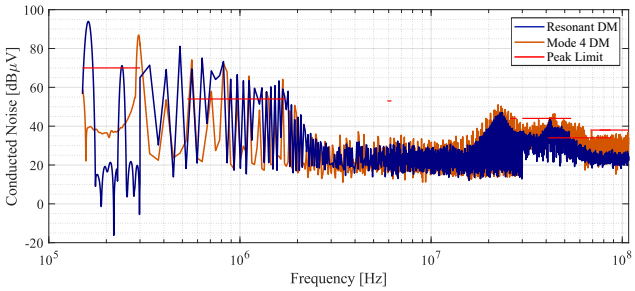
6 SSFM case peaks at 17% above the LW limit while the CM, Mode 3 case peaks at 15% above the limit. For this same frequency range, the DM noise peaks are slightly worse for both Modes 3 and 6, however, the DM, Mode 6 SSFM case peaks differ more strongly, at 23% above the LW limit, from the DM, Mode 3 case peak, at 19% above the limit. Because Mode 6 has a smaller step size of frequency dithering and a smaller maximum deviation from the center frequency, we expect that the SSFM impact will be less pronounced than Mode 3.

For the prototype in this work, the Common Mode peaks are generally lower than the Differential Mode peaks. Due to the switched-capacitor nature of the interleaved-input, single inductor hybrid Dickson topology, the converter has low voltage swing on the switch-node and throughout the circuit, leading to lower Common Mode noise. On the contrary, Differential Mode noise is heavily dependent on the current through the converter. Having several current paths and many capacitor branches, as this topology has, can correlate to larger current loops. Furthermore, the impact of larger current loops will be exacerbated at increasing load and with higher current ripple.

Owing to the requirement of split-phase switching, which results in the input voltage being disconnected from the circuit within each phase, the current ripple at the input source



(a) Common mode (CM) conducted emissions.



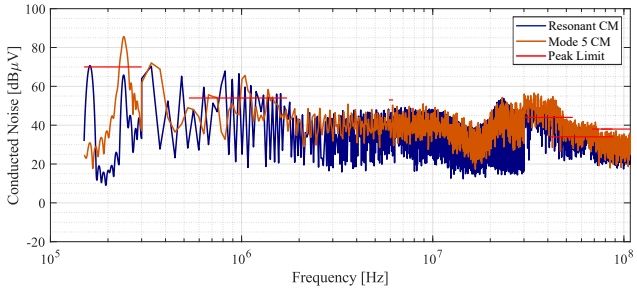
(b) Differential mode (DM) conducted emissions.

Figure 6.19: Conducted emissions for 81 kHz (blue) with no SSFM and 143 kHz (green) with sinusoidal SSFM, Modes 1 and 4, respectively, at 48 V in, and a 20 A load.

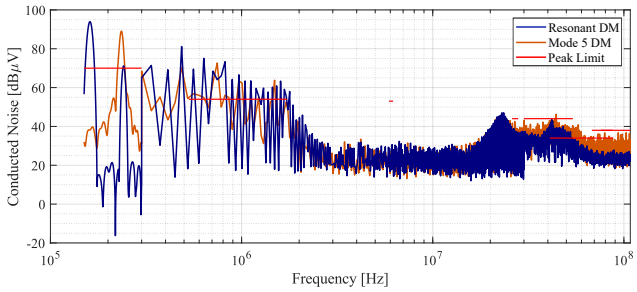
is non-zero. This leads to greater DM noise. Despite the impossibility of eliminating the input current ripple, clever circuit configuration (e.g. the implementation of an interleaved-input in this work) serves to reduce this source of DM noise as compared to a single-ended topology.

As showcased in the previous section, one advantage of operating above resonance is the invariability of efficiency with changing switching frequency. To take advantage of this feature, we can implement SSFM to potentially improve the EMI performance of this converter when it is operating above resonance. This is in an effort to make above-resonance noise levels more comparable to resonant noise levels. Fig. 6.18 and Table 6.7 show conducted emissions plots and related peak-to-limit data, respectively, for Mode 3 (Table 6.6). For both the CM and DM cases, the noise level profile in the middle range of frequencies is noticeably smaller with triangle SSFM employed versus resonant operation with no SSFM. Additionally, the peaks are more spread out indicating the conversion of a narrower and taller peak into a wider and shorter one, the key premise of SSFM. In addition to providing lower losses at heavier loads, operating above resonance allows for the implementation of SSFM without a significant impact on efficiency, but with a clear benefit for EMI performance.

While only comparisons between Modes 1, 2 and 3 are discussed in detail here, Table 6.7 contains peak-to-limit percentages for each remaining SSFM mode outlined in Table 6.6. Even though there is no definitive 'best' modulation scheme, for this prototype at this



(a) Common mode (CM) conducted emissions.



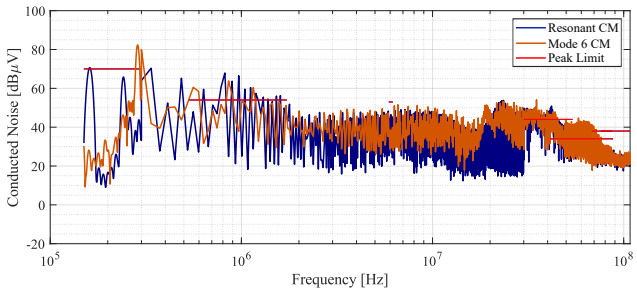
(b) Differential mode (DM) conducted emissions.

Figure 6.20: Conducted emissions for 81 kHz (blue) with no SSFM and 143 kHz (green) with sinusoidal SSFM, Modes 1 and 5, respectively, at 48 V in, and a 20 A load.

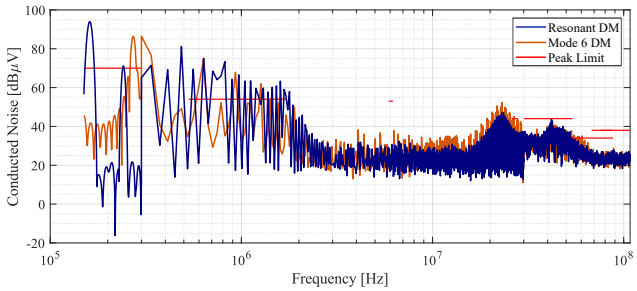
loading condition, the overall trend suggests that the more effective SSFM methods for reducing conducted emissions have a shorter modulation period, T_m, larger frequency step size, Δf_c, and larger maximum frequency deviation, A_m. Moreover, though several schemes for frequency dithering to spread the noise spectrum are presented here, these are only a small subset of the many schemes possible to help reduce conducted EMI.

Aside from implementing SSFM, strategic frequency placement, as well as an EMI filter can be used for EMI mitigation. When it comes to improving EMI at resonant operation, we can choose inductor and capacitor values that correspond to a lower resonant frequency such that not only is the fundamental component below 150 kHz (the lower end of the LW Band), but that the $2\text{x}f_{res}$ peak is as well. Another option for frequency manipulation would be to have the lower harmonics (fundamental or second) occur between the LW and MW frequency bands, avoiding the CISPR limits.

Furthermore, passive EMI filters can be designed to target peaks at specific frequencies, and therefore reduce conducted noise even further. For this topology, because the power inductor is directly connected to the output, it acts as a filter to the low-side port. However, to filter noise at the high-side port, a discrete EMI filter can be placed at the front end [23] of the power converter. For this additional filter, passive components are selected to filter out specific frequency harmonics: where the noise peaks are occurring. Typically, the different



(a) Common mode (CM) conducted emissions.



(b) Differential mode (DM) conducted emissions.

Figure 6.21: Conducted emissions for 81 kHz (blue) with no SSFM and 143 kHz (green) with right triangle SSFM, Modes 1 and 6, respectively, at 48 V in, and a 20 A load.

conducted noise peaks appear at harmonics of the switching frequency. However, due to the requirement of split-phase switching (having switching transitions within a phase), the positioning of the peaks is more complicated than a simple multiple of the switching frequency. In this instance, having preliminary EMI measurements as presented here informs the design of the EMI filter. Furthermore, realizing the impact SSFM has on the location of the peaks is also necessary for a multi-faceted approach to mitigating and filtering out conducted emissions.

Table 6.7: CM and DM Noise Peaks for Various Modes of Operation

Mode	Band	Peak-to-Limit %	
		CM	DM
Mode 1	LW	0.86	34.2
	MW	25.7	38.9
	VHF I	15.6	-2.95
Mode 2	LW	17.1	25.3
‘	MW	26.5	38.0
	VHF I	27.0	5.41
Mode 3	LW	15.2	19.2
	MW	6.10	21.2
	VHF I	21.9	7.93
Mode 4	LW	23.7	23.8
	MW	31.8	37.3
	VHF I	26.4	5.41
Mode 5	LW	11.7	25.7
(143kHz)	MW	21.2	34.8
	VHF I	28.6	5.50
Mode 6	LW	17.6	23.3
	MW	18.2	38.2
	VHF I	22.9	-7.43

6.5 Chapter Summary

The development of a 48 V distribution bus in both EVs and ICE vehicles opens opportunities for adapting advancements in high-efficiency, high-power-density data center power conversion techniques to automotive applications. However, in-vehicle power electronics also require robust component selection and qualification for industry EMI standards. Furthermore, there are trade-offs between achieving these performance standards, which are informed by the analysis of at resonant and above-resonant operation presented here. This chapter discusses the theory and construction of an 8-to-1 hybrid Dickson switched-capacitor converter for automotive systems, as well as the phase timing analysis for a split-phase regulating hybrid SC converter. The topology testing focuses on achieving low EMI and high efficiency by utilizing an interleaved input, as well as frequency modulation techniques. In this work, the efficiency benefits of operating at resonance for light load, but above resonance (for reduced RMS currents and conduction losses) at heavier load were demonstrated. Additionally, several spread-spectrum frequency modulation schemes were compared for both efficiency and EMI performance. Dithering the frequency around a point higher than the resonant frequency has little impact on the efficiency, however, the benefits of SSFM on conducted EMI are evident. Specifically, triangular modulation, greatly flattens out the peak

noise for both CM and DM EMI, which will reduce the amount of filtering required to meet CISPR 25, Class 5 requirements.

Chapter 7

Loss Analysis of Hybrid Switched-Capacitor Converters

Effective design of power converters requires an analysis of loss components. Prior chapters discuss the advantages of hybrid switched-capacitor (hybrid SC) converters from a circuit and component sizing angle, but that argument is incomplete without investigating the sources of power loss. This chapter will briefly discuss methods of calculating losses for several converter components, from high-level scaling laws to intricate mathematical expressions to computer-aided simulations.

7.1 Switching Devices

First-order optimization of power converter design typically aims to minimize total passive component volume of capacitors and inductors while assuming in practice these elements comprise the large majority of a converter's overall volume. However, this minimization may

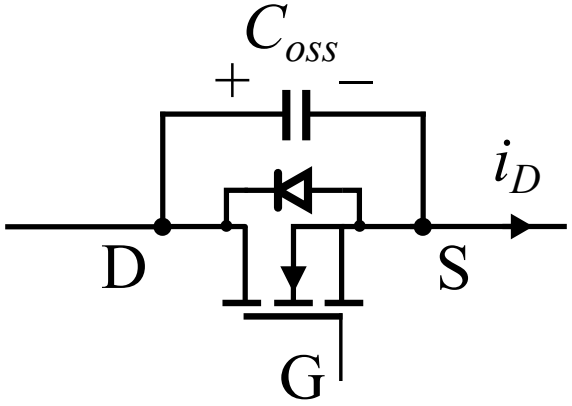


Figure 7.1: Circuit diagram of an N-channel MOSFET with parasitic output capacitance, C_{oss}, and body diode.

incur increased voltage and current ripple, which would subsequently be imposed on the adjacent switching devices. This in turn may lead to increased switch stress, resulting in volume/loss increases within the active devices. An example MOSFET with parasitic output capacitance, C_{oss}, and body diode is depicted in Fig. 7.1 and will be referred to throughout the discussion on loss mechanisms in switching devices for power converters.

Conduction and Switching Loss

Losses associated with switching devices, in this case, specifically FETs, can be broken down into conduction losses, switching losses, and gate driving losses. A general expression of conduction losses of a component x with resistance, R_x, is given by (7.1). Here, the rms current through the component, $i_{\text{rms},x}$ is used instead a dc current to capture frequency- and ripple-dependent losses.

$$P_{\text{cond},x} = i_{\text{rms},x}^2 R_x \tag{7.1}$$

Switching losses arise from various aspects of the device. Each of which is touched on here. Gating losses, or the loss associated with charging and discharging the gate capacitance (effectively the input capacitance C_{iss}) depend on component parameters, gate drive voltage, and switching frequency:

$$P_{\text{gate,S}} = \frac{1}{2} f_{\text{sw}} C_{\text{iss}} V_{\text{drv}}^2. \tag{7.2}$$

Silicon MOSFETs also experience reverse-recovery losses, whereas GaNFETs do not due to the construction of the semiconductor device. These losses (7.3) are a function of the body diode reverse recovery charge and the drain-source voltage when the switch turns on (and the body diode transitions to no longer conducting).

$$P_{\text{qrr}} = Q_{\text{rr}} V_{\text{ds,on}} \tag{7.3}$$

Furthermore, two potentially significant sources of switching losses, particularly at high voltages are overlap losses (7.4) and output capacitance losses (7.5). Overlap loss, depicted by the shaded region in Fig. 7.2 for a turn-on transition relate not only to the voltage across and current through the device at a state transition, but also to the rise and fall time of the gate-source voltage, which are dependent on gate charge and drive strength. Similarly, output capacitance losses are a function of the stored charge on the switch C_{oss} and the blocking voltage. The relationship of a linear output capacitance to the charging losses is given in (7.5) and a discussion of how these losses change when accounting for the non-linearity of the C_{oss} is presented later in this chapter.

$$P_{\text{ovlp}} = \frac{1}{2} f_{\text{sw}} \left(V_{\text{ds,on}} I_{\text{d,on}} t_{\text{on}} + V_{\text{ds,off}} I_{\text{d,off}} t_{\text{off}} \right) \tag{7.4}$$

$$P_{\text{coss}} = f_{\text{sw}} C_{\text{oss}} V_{\text{ds}}^2 \tag{7.5}$$

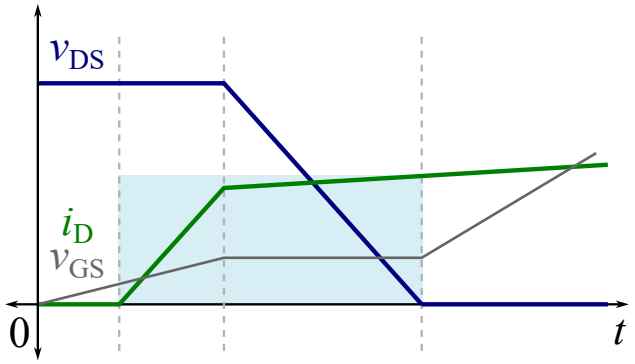


Figure 7.2: Example switch gate-source voltage, drain-source voltage and drain-source current during a turn-on transition. Overlap losses are shown by the highlighted region with the volt-amp product is nonzero.

V-A Metric

One conventional metric *comparing* topologies or operating conditions, rather than computing numerical loss estimates for a specific design, is the switch volt-amp (VA) product [12, 32, 34, 42, 140]. This metric assumes linear device scaling and commonly serves as a proxy for total switching device area and/or loss in a given converter when summed across all switching devices. That is, a lower VA rating translates to a smaller and/or more efficient power converter. However, the assumption of linear device scaling does not accurately capture the trends in on-state resistance, output capacitance, and gate charge as voltage ratings scale.

In this work, we propose a VA metric that takes into account the full effect of the inductor current and capacitor voltage ripples, improving upon calculations presented in past literature by providing a metric with greatly increased fidelity. Furthermore, device scaling laws are also incorporated into the VA rating to more accurately capture the trade-off in switching loss and conduction loss for devices rated for different voltages. To compute a converter's VA rating, the rms current of each switch is multiplied by its corresponding peak voltage, before summing across all elements:

$$\mathrm{VA}_{\mathrm{tot}} = \sum_{i=1}^{N_{\mathrm{S}}} V_{\mathrm{ds,max},i} \cdot I_{\mathrm{rms},i}. \tag{7.6}$$

However, integrating device scaling laws into this metric requires some re-formulation [32, 33, 141–143]. As discussed in the previous section of this chapter, switch losses can be split into conduction and switching-related losses (7.7), where $E_{\mathrm{sw,S}}$ is the energy corresponding to total switching losses [32, 33]. To map performance parameters to scaling parameters (7.8), the on-state resistance and the switching energy can be expressed as 'area-specific' terms: $R_{\mathrm{on,S}} = {}^{\hat{R}_{\mathrm{on,S}}}/_{A_{\mathrm{die}}}$ and $E_{\mathrm{sw,S}} = \hat{E}_{\mathrm{sw,S}} A_{\mathrm{die}}$.

$$P_{\mathrm{S}} = P_{\mathrm{cond,S}} + P_{\mathrm{sw,S}} = i^2_{\mathrm{rms,S}} R_{\mathrm{on,S}} + f_{\mathrm{sw}} E_{\mathrm{sw,S}} \tag{7.7}$$

$$P_{\mathrm{S}} = i_{\mathrm{rms,S}}^2 \frac{\hat{R}_{\mathrm{on,S}}}{A_{\mathrm{die}}} + f_{\mathrm{sw}} \hat{E}_{\mathrm{sw,S}} A_{\mathrm{die}} \tag{7.8}$$

Moreover, the switch losses are minimized (with respect to die area — the scaling term) when conduction and switching losses are balanced (i.e., equal). For a simple example, in a scenario where the gate charge, reverse recovery, and overlap losses are negligible compared to output capacitance losses (e.g., high voltage resonant operation), the minimized switch loss reduces to:

$$P_{\mathrm{S,min}} = 2 V_{\mathrm{ds,max}} i_{\mathrm{rms,S}} \sqrt{f_{\mathrm{sw}} \hat{R}_{\mathrm{S}} \hat{C}_{\mathrm{oss}}}. \tag{7.9}$$

Through data collection of available switching devices, the scaling trends of the area-specific parameters versus rated blocking voltage can be determined. This analysis assumes that there are devices available for a continuous range of blocking voltages and that the switches are operated *at* that rating (further discussion on relaxing this assumption is presented later in this chapter). In [143], the specific on-resistance and specific output capacitance are power fit to a (small) data set. With each parameter taking the form $\hat{R}_{\mathrm{on,S}} = \kappa_{\mathrm{R}} V_{\mathrm{ds,max}}^{\alpha_{\mathrm{R}}}$ and $\hat{C}_{\mathrm{oss,S}} = \kappa_{\mathrm{C}} V_{\mathrm{ds,max}}^{\alpha_{\mathrm{C}}}$, the minimum switch loss for the simplified example reduces to:

$$P_{\mathrm{S,min}} = 2 \left(V_{\mathrm{ds,max}}^{1+\frac{\alpha_{\mathrm{R}}+\alpha_{\mathrm{C}}}{2}} \right) \left(i_{\mathrm{rms,S}} \right) \sqrt{f_{\mathrm{sw}} \kappa_{\mathrm{R}} \kappa_{\mathrm{C}}}. \tag{7.10}$$

The form of 7.10 is reminiscent of the conventional VA product and from this expression a new switch stress metric can be formulated (7.11). Furthermore, for design space optimization, such as that discussed in [12, 34], the switch stress metric can be normalized to a form of the high-side power, however, now the voltage term has a more complex exponent to account for the scaling terms in the switch stress metric.

$$\mathrm{VA}_{\mathrm{tot}} = \sum_{i=1}^{N_{\mathrm{S}}} \left(V_{\mathrm{ds,max}}^{1+\frac{\alpha_{\mathrm{R}}+\alpha_{\mathrm{C}}}{2}} \right)_i \left(i_{\mathrm{rms,S}} \right)_i \rightarrow M_{\mathrm{VA}} = \sum_{i=1}^{N_{\mathrm{S}}} \frac{\left(V_{\mathrm{ds,max}}^{1+\frac{\alpha_{\mathrm{R}}+\alpha_{\mathrm{C}}}{2}} \right)_i \left(i_{\mathrm{rms,S}} \right)_i}{\left(V_{\mathrm{HI}}^{1+\frac{\alpha_{\mathrm{R}}+\alpha_{\mathrm{C}}}{2}} \right) \left(I_{\mathrm{HI}} \right)} \tag{7.11}$$

$$\tag{7.12}$$

7.2 Current and Voltage Analysis

Whether calculating a numeric loss estimate to evaluate a specific design/device, or using a scaling metric to compare topologies/power levels, etc., an analysis of the currents through and the voltages across various components is necessary. Here, closed-form expressions for rms currents and peak blocking voltages are derived for ReSC converters, and suggestions are made for determining these parameters for more complex topologies, such as the split-phase ZVS Dickson converter from Chapter 5.

Current Stress

Rather than using average current for the total VA rating, as in [12, 42], here we calculate the rms current through each component—for both at- and above-resonance operation of resonant switched-capacitor (ReSC) converters —using the inductor current waveform derived in Chapter 3. Utilizing rms current is similar to the analysis performed in [51, 68] and captures conduction losses, thermal requirements, and the effects of operating frequency on current ripple. The process is detailed for an analysis of the switches, but the concept can be applied to the remainder of the circuit.

The normalized charge flow, $a_{\mathrm{S},ji}$, through the ith switching device is obtained using the procedure described in Chapter 3 and are reported here for the example two-phase odd-N Dickson converter (7.14) based on the switch numbering in Fig. 3.9.

$$\boldsymbol{a}_{S[1-4]} = \begin{bmatrix} \frac{N_\mathrm{C}}{2} & 0 & \frac{N_\mathrm{C}}{2} & 0 \\ 0 & \frac{N_\mathrm{C}}{2} & 0 & \frac{N_\mathrm{C}}{2} \end{bmatrix} \tag{7.13}$$

$$\boldsymbol{a}_{S[5-N_\mathrm{S}]} = \begin{bmatrix} 1 & 0 & 1 & \cdots & 0 & 1 \\ 0 & 1 & 0 & \cdots & 1 & 0 \end{bmatrix} \tag{7.14}$$

In phase j, the ratio of the peak current through switch S_i relative to the peak inductor current, as defined in (3.28), is equivalent to the ratio of respective charge flow, or

$$\frac{I_{\mathrm{pk},\mathrm{S}_i,j}}{I_{\mathrm{pk},j}} = \frac{a_{\mathrm{S},ji}}{a_{\mathrm{L},j}}. \tag{7.15}$$

For each switch, S_i, the total rms current in a switching period is constructed from a squared sum of per-phase rms currents as

$$\begin{aligned} I_{\mathrm{rms},\mathrm{S}_i} &= \sqrt{\frac{1}{T_\mathrm{sw}} \int_0^{T_\mathrm{sw}} i_{\mathrm{S}_i}^2(t)\ dt} \\ &= \sqrt{\frac{1}{T_\mathrm{sw}} \sum_{j=1}^{N_\mathrm{P}} \int_{-\frac{t_j}{2}}^{\frac{t_j}{2}} \left(I_{\mathrm{pk},\mathrm{S}_i,j} \cos(\omega_{0,j}\, t)\right)^2\ dt} \\ &= \frac{I_\mathrm{HI}}{2} \sqrt{\frac{\pi}{\Gamma} \sum_{j=1}^{N_\mathrm{P}} \frac{a_{\mathrm{S},ji}^2}{\tau_j|_{\Gamma=1}} \cdot \left(\frac{\frac{\pi}{\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}} + \sin\left(\frac{\pi}{\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}{1 - \cos\left(\frac{\pi}{\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)} \right)} \end{aligned} \tag{7.16}$$

where (3.22) and (3.25) are substituted for t_j and $\omega_{0,j}$, respectively, and q_HI is substituted for the high-side input current, I_HI, using (3.4). A similar analytical expression for the inductor

current rms may be derived as

$$I_{\text{rms,L}} = \frac{I_{\text{HI}}}{2}\sqrt{\frac{\pi}{\Gamma}\sum_{j=1}^{N_{\text{P}}}\frac{a_{\text{L},j}^2}{\tau_j|_{\Gamma=1}}\cdot\left(\frac{\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}+\sin\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}{1-\cos\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}\right)}. \tag{7.17}$$

Interestingly, both the switch and inductor rms currents are independent of both C_0 and f_{sw}, varying only with Γ and I_{HI}. For all two-phase converters, the normalized phase durations are invariant to Γ (i.e., $\tau_j = \tau_j|_{\Gamma=1}$) leading to further simplification of (7.16) and (7.17). In all cases an increase in Γ results in reduced rms currents, as expected.

The rms current expressions derived here are applicable to two-phase and multi-phase ReSC converters, with the exception of converters that require more complex switching schemes, such as split-phase switching. Split-phase converters exhibit more complex inductor current waveforms as discussed in Chapter 4 and analytically determining an rms current through the inductors or switches is tedious; instead, either a numerical/symbolic computation software, such as MATLAB, or a circuit simulation software, such as LTspice, can be used to estimate these values.

Voltage Stress

An analysis of blocking voltage requirements for each switch is necessary in the formulation of the VA metric. Prior work in [12, 42, 51, 68], only calculated switch voltage stresses based on the mid-range capacitor voltages, thereby neglecting the effects of capacitor voltage ripple. In this analysis, the peak voltage indicates switch stress, and more fairly characterizes the performance of switches under the large ripple conditions typical in converters designed for minimized passive volume.

When a switch is disabled, its blocking voltage, $V_{\text{ds},i}$, is dictated by proximal flying capacitors. In every phase, large-signal KVL is applied to obtain expressions for the voltage imposed upon each switch, inclusive of flying capacitor voltage ripple. However the phase and time of occurrence for the peak blocking voltage in each switch is not immediately obvious by inspection. For the ReSC topologies presented in this work, the maximum (or minimum) of V_{ds} in each phase occurs either at its beginning, j_{start}, or end, j_{end}. Therefore the instantaneous blocking voltage immediately before and after each phase transition must be investigated, after which the maximum value is recognized.

Using the two-phase odd-N Dickson converter in Fig. 3.9 as an example, at the start of phase 1 switch S_6 experiences a blocking voltage of

$$V_{\text{ds},N+2}\Big|_{(j=1)_{\text{start}}} = \left(V_{\text{HI}}v_{N-2}+\frac{1}{2}\Delta v_{\text{pp},N-2}\right)-\left(V_{\text{HI}}v_{N-3}-\frac{1}{2}\Delta v_{\text{pp},N-3}\right) \tag{7.18}$$

whereas at the end of phase 1 switch S_6 experiences

$$V_{\text{ds},N+2}\Big|_{(j=1)_{\text{start}}} = \left(V_{\text{HI}}v_{N-2}-\frac{1}{2}\Delta v_{\text{pp},N-2}\right)-\left(V_{\text{HI}}v_{N-3}+\frac{1}{2}\Delta v_{\text{pp},N-3}\right) \tag{7.19}$$

Table 7.1: Two-Phase Odd-N Dickson Maximum Switch Voltage Stress

	$V_{\mathbf{ds,max},i}$	
	Dickson	
S_{B_i}	$\frac{1}{N}V_{\mathrm{HI}} + \frac{1}{2}\frac{q_{\mathrm{HI}}}{C_0}$	$i \in \{1 \leq \mathbb{N} \leq 4\}$
S_{S_i}	$\frac{2}{N}V_{\mathrm{HI}} + \frac{1}{N-1}\frac{q_{\mathrm{HI}}}{C_0}$	$i \in \{2 \leq \mathbb{N} \leq N-1\}$
	$\frac{1}{N}V_{\mathrm{HI}} + \frac{1}{2}\frac{q_{\mathrm{HI}}}{C_0}$	$i \in \{1, N\}$

where v_{N-2} and v_{N-3} are the normalized mid-range voltage of capacitor C_{N-2} and C_{N-3}, respectively. Voltage ripples $\Delta v_{\mathrm{pp},i}$ are defined by (4.7). In this case (7.18) clearly expresses the peak blocking voltage condition in phase 1. Continuing the analysis for every phase shows (7.18) is also the maximum switch voltage stress, $V_{\mathrm{ds,max,B_5}}$, for switch B_5 over the entire switching period.

This search is expanded to all switches, where phases in which a switch is turned on may be ignored since these switches will have 0 V across them. Table 7.1 documents the generalized result for peak voltage stress on each switching element for the two-phase odd-N Dickson topology. Switch stress for odd-N and even-N split-phase Dickson converters is included in Appendix A.

Non-linear $C_{\mathbf{oss}}$

The linearization of the output capacitance and the *method* of linearization is especially critical in the analysis of converters such as hybrid SC converters in which switches block differing voltages. As discussed in Chapter 5, there are various linear-equivalent capacitances that can be defined. For modeling inductor currents for ZVS operation in Chapter 5, the 'impedance-equivalent' capacitance was used. An energy-method for evaluating equivalent output capacitances is used for loss analysis [102, 103, 144]. Fig. 5.8 is reproduced here for easier reference.

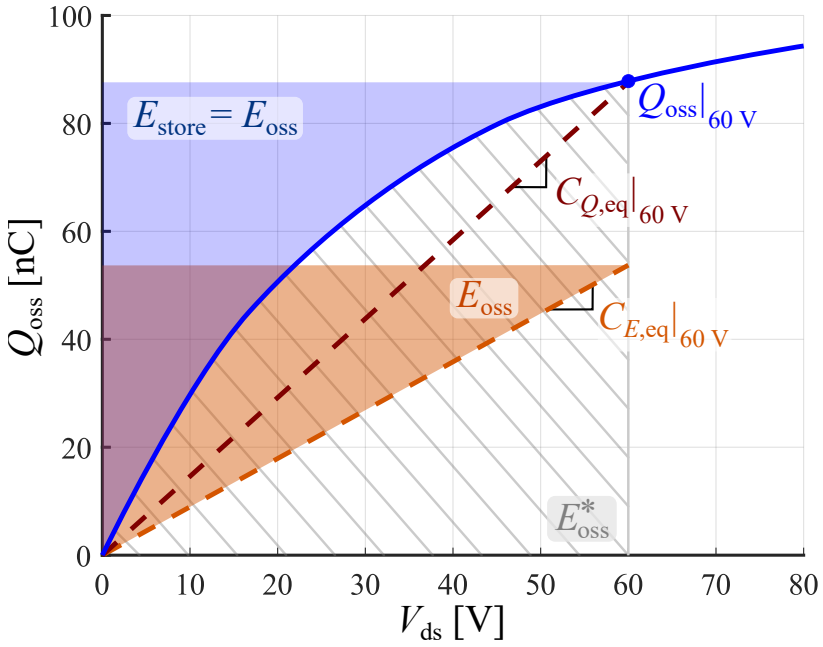


Figure 7.3: Stored charge in the switch output capacitance as a function of the blocking voltage for an example switch device. Shaded areas corresponding to stored energy, co-energy; as well as linearized capacitances (charge-equivalent ($C_{Q,\text{eq}}$) and energy-equivalent ($C_{E,\text{eq}}$) are notated.

Switching Loss

Prior works generally discuss output capacitance switching losses in terms of a half-bridge configuration () and assumes two equivalent devices that block the same peak voltage. From these assumptions the loss analysis is greatly simplified, but loses its generality. Particularly for hybrid SC converters, where there are many switches blocking different voltage changing state during the same transition, a more general analysis of C_{oss} losses is necessary.

During a specific switching transition an energy balance (7.20) can be performed to determine the lost energy. The initial energy stored on any switch output capacitances plus any energy drawn from the dc source (as the charging voltage source) must equal the stored

energy at the end of the transition plus the loss. For the example of a hybrid switched capacitor converter, the energy present in the system at the start of the switching transition (at time t_0), is given by (7.21) and is equal to any energy in the inductor, $E_{\mathrm{L}} = {}^1\!/_2 Li(t_0)^2$ plus the sum of energy stored on OFF switching device output capacitances, E_{oss}. The stored energy in a non-linear capacitor is the area (shaded in blue in Fig 7.3) between the Q_{oss} curve and the Q_{oss} axis (7.22).

$$E_{\mathrm{loss}} = E_{\mathrm{final}} - E_{\mathrm{init}} + E_{\mathrm{src}} \tag{7.20}$$

$$E_{\mathrm{init}} = E_{\mathrm{L}}\big|_{t_0} + \sum_{i=1}^{N_{\mathrm{S}}} E_{\mathrm{Coss},i}\big|_{t_0} \tag{7.21}$$

$$E_{\mathrm{oss},i} = \int_0^{Q_{\mathrm{oss},i}} v \ \mathrm{d}q = \int_0^{v_{ds},i} v \cdot C_{\mathrm{oss},i}(v) \ \mathrm{d}v \tag{7.22}$$

Similarly, the energy present in the system at the end of the switching transition (at time t_1), is given by (7.23) as the sum of inductor and switch output capacitance energies.

$$E_{\mathrm{fin}} = E_{\mathrm{L}}\big|_{t_1} + \sum_{i=1}^{N_{\mathrm{S}}} E_{\mathrm{Coss},i}\big|_{t_1} \tag{7.23}$$

Finally, the energy provided by the dc charging voltage source E_{src} is equal to the sum of the energy required to charge up all 'charging' switch output capacitances. As mentioned in Chapters 3 and 5, when charging a capacitor through a dc source (whether the capacitor is linear or non-linear) from voltage v_0 to v_1, the required energy is (7.24).

$$E_{\mathrm{src}} = V_{\mathrm{dc}} \Delta q_{\mathrm{oss}} = V_{\mathrm{dc}} \cdot (Q_{\mathrm{oss}}\big|_{\mathrm{v_0}}^{\mathrm{v_1}}) \tag{7.24}$$

Furthermore, the energy required for capacitor charging can be related to the stored energy and the 'co-energy' of the output capacitance [102]. The 'co-energy' E^*_{oss} can be visualized as the area under the Q_{oss}-V_{ds} and is expressed in (7.25). This energy represents the energy lost through capacitor charging from v_0 at t_0 to v_1 at t_1.

$$E^*_{\mathrm{oss}} = \int_{v_0}^{v_1} Q_{\mathrm{oss}}(v) \ \mathrm{d}v \tag{7.25}$$

For a switching transition, the total loss is the sum of the discharged stored energy from the switches that are turning on plus the sum of the co-energy from the switches that are turning off (i.e., charging up output capacitances). The final loss expression is given by (7.26).

$$P_{\mathrm{loss,Coss}} = E_{\mathrm{loss}} f_{\mathrm{sw}} = \left[\sum_{i=1}^{N_{\mathrm{S,dis}}} \left(E_{\mathrm{Coss},i}\big|_{t_0} - E_{\mathrm{Coss},i}\big|_{t_1} \right) + \sum_{i=1}^{N_{\mathrm{S,chrg}}} E^*_{\mathrm{Coss},i}\big|_{t_0 \to t_1} \right] f_{\mathrm{sw}} \tag{7.26}$$

This energy loss can also be used to determine the required inductor energy for ZVS. If an exactly soft-switching transition is assumed, $E_{\text{loss}} = 0$ and the initial inductor energy can be determined, for a transition where the inductor current ends at zero.

Switch-Stress Metric

The switch-stress metric and scaling laws presented in Section 7.1 assume that there is a physical device that is rated for exactly the peak drain-source voltage imposed on that switch, however, for discrete switching devices, we know that there is not a continuous voltage rating of available devices. Furthermore, switches that have different (but similar) conduction and voltage stress may be implemented with the same switch selection for several reasons, such as: simplified layout, component procurement, and simplified gate drive solutions. Because the switch-stress metric presented here accounts for switching losses through the inclusion of the scaling of C_{oss}, a more accurate model of the switching losses should factor in the non-linearity of switch output capacitance. Utilizing a device at a voltage lower than its rated voltage typically results in a higher output capacitance. To account for the discrepancy in operating voltage and rated device voltage, [143] introduces a device utilization factor: β defined as $\beta = {}^{V_{\text{ds}}}/_{V_{\text{r}}}$, where $V_{\text{ds,max}}$ is the operating peak drain-source voltage and V_r is the device rated voltage, as shown in Fig. 7.4.

Appendix A of [143] outlines the scaling of the non-linear C_{oss} based on semiconductor

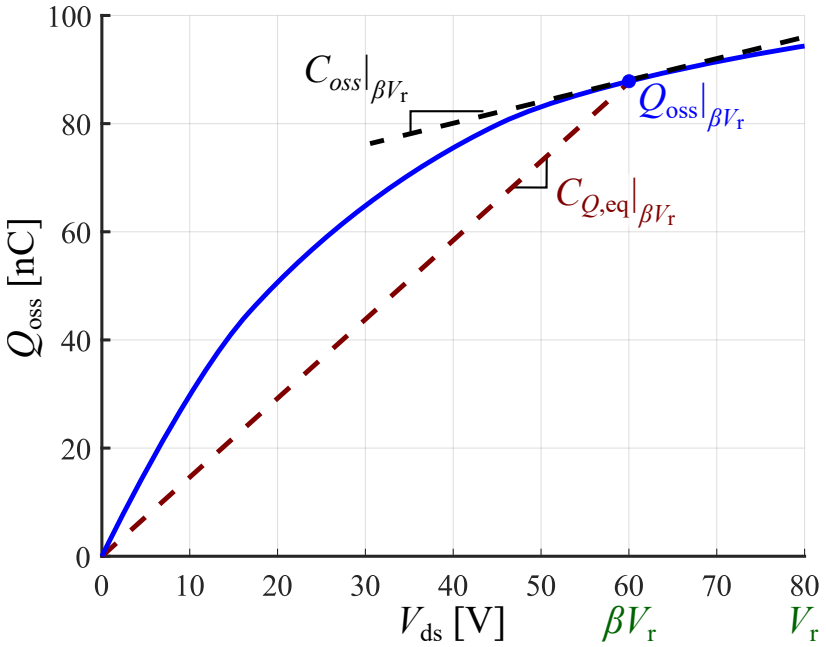


Figure 7.4: Stored charge in the switch output capacitance as a function of the blocking voltage for an example switch device rated at V_{r}. The output capacitance at the operating voltage, βV_{r}, and the linearized charge-equivalent capacitance ($C_{Q,\text{eq}}$) are notated.

device physics. Here, only the incorporation of the utilization factor into the switch-stress FOM is presented. One drawback of accounting for this utilization metric is that now the switch loss metric is quantized based on available technologies. Therefore, inclusion of the rated voltage versus the peak blocking voltage may actually complicate any topology comparison and precludes a closed-form analytical model.

$$C_{\text{oss}}(V_{ds,max}) = \sqrt{\frac{V_{\text{ds,max}}}{V_{\text{r}}}}\kappa_{\text{C}} V_{\text{ds,max}}^{\alpha_{\text{C}}} \times A_{\text{die}} = \frac{1}{\sqrt{\beta}}\kappa_{\text{C}} V_{\text{r}}^{\alpha_{\text{C}}} \times A_{\text{die}} \tag{7.27}$$

$$\text{VA}_{\text{tot}} = \sum_{i=1}^{N_{\text{S}}} \frac{V_{\text{ds,max}}^{3/4}\left(V_{\text{r}}^{\frac{2(\alpha_{\text{R}}+\alpha_{\text{C}})+1}{4}}\right)_i \left(i_{\text{rms,S}}\right)_i}{\left(V_{\text{HI}}^{1+\frac{\alpha_{\text{R}}+\alpha_{\text{C}}}{2}}\right)\left(I_{\text{HI}}\right)} \tag{7.28}$$

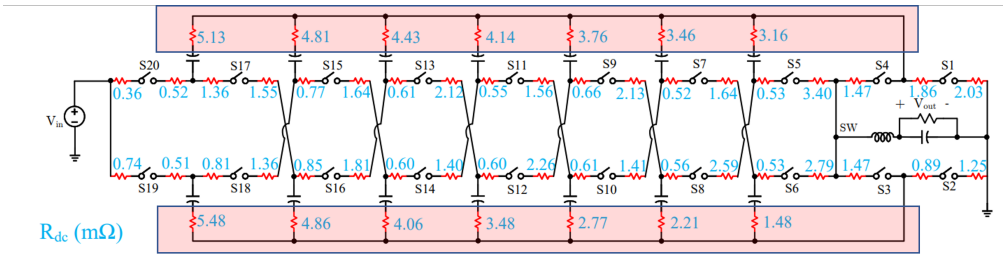
7.3 Capacitors

Recent works [145–147] explore methods of more accurately characterizing and describing losses of multi-layer ceramic capacitors (MLCCs) under large bias conditions, i.e., how they are used in hybrid SC converters with a sizeable voltage ripple on top of a dc voltage. However, for first order loss approximations, (7.1) can be used based on the calculated or simulated rms current through a capacitor. Frequency-dependent equivalent series-resistance (ESR) values for small bias conditions are reported on component data sheets and can be used to calculate an effective resistance of a combination of series/parallel capacitors for each flying capacitor. Furthermore, Class II MLCCs while having extremely high energy densities (making them attractive for use in power dense capacitor-based converters), also experience significant capacitance reduction with increased voltage bias. For resonant converters this can pose a problem in maintaining balanced ZCS or ZVS operation, necessitating active control techniques [63, 86].

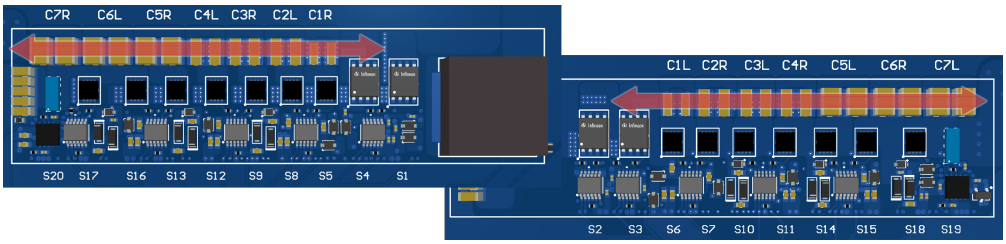
7.4 Printed Circuit Board

As loads continue to increase, demanding larger current handling capabilities of power converters, and as switching frequencies increase to reduce passive component sizing, the design and layout of printed circuit boards (PCBs) becomes crucial to high performance power converters.

The automotive power converter in Chapter 6, nearly 40% of total losses were attributed to PCB trace resistances. For the work presented here, the circuit is laid out folded in half down the 'string' of switches (termed a 'hotdog' fold) with half of the switches on the top side and half on the bottom side (Fig. 7.5). Using ANSYS SIWave, the PCB trace resistances for this layout were estimated. Because the current along the nodes highlighted in red, travels



(a) Simulated PCB trace resistances.

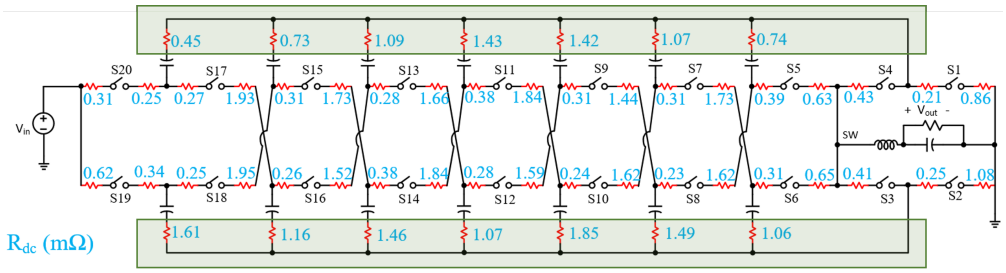


(b) Rendering of the converter layout.

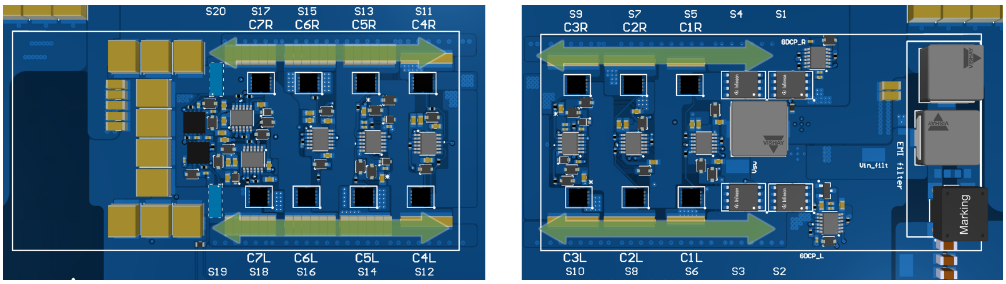
Figure 7.5: Layout diagrams for a laterally symmetric HISID converter, highlighting high impedance paths.

the full length of the power stage, conduction losses are a sizeable portion of the overall converter losses, especially at heavy loads where conduction losses dominate over other loss sources. The DC trace resistance for the 'hamburger' fold is reduced by 77% compared to the 'hotdog' fold in Fig. 6.10.

A re-design of the HISID converter to fold the converter along the vertical axis (in Fig. 7.6), reduces the dc trace resistance by over 75%. Folding the converter at the 'midpoint' of the power path ('hamburger' fold) reduces the path length of the common capacitor nodes by about half compared to the laterally symmetric fold. With the resistance estimates from simulation, the PCB conduction losses can be calculated with (7.1).



(a) Simulated PCB trace resistances.



(b) Rendering of the converter layout.

Figure 7.6: Layout diagrams for a vertically symmetric HISID converter, highlighting reduced impedance paths.

7.5 Magnetics

Modeling of magnetics losses is a complex problem space. Conduction losses are generally of the form (7.1), with the dc resistance, but there are also complex ac winding losses stemming from eddy currents/proximity effects [148, 149]. Furthermore, accurate modeling of core losses typically relies on Steinmetz equations (7.29) or modified Steinmetz equations (e.g., iGSE (7.30)) and Steinmetz parameters [150–152].

$$P_{\text{core}} = k f^{\alpha} \Delta B^{\beta} \tag{7.29}$$

$$P_{\text{core}} = \frac{1}{T} \int_0^T k \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (B_{\text{pp}})^{\beta-\alpha} \mathrm{d}t \tag{7.30}$$

For commercial off-the-shelf magnetics, manufacturers may or may not provide access to full Steinmetz parameter data sets, making modeling these magnetics losses difficult. However, most manufacturers provide an online loss estimation tool to give a first order approximation, though these tools generally assume triangular currents.

7.6 Chapter Summary

This chapter briefly discusses the various loss mechanisms within a power converter. For conduction losses an analytical method for determining rms currents is presented. Additionally, a metric for evaluation of switch stress is provided including accommodations for device scaling trends. While there is still much work to be done in the modeling of power converter losses, a first-order approximation may be sufficient for topology comparisons and relative device evaluations.

Chapter 8

Conclusion

This final chapter discusses some potential extensions of the work presented in the thesis as well as other tangential questions or applications for further work. Additionally a brief review of the presented material closes out this dissertation.

8.1 Future Work

Initial and brief thoughts regarding future research paths of switching techniques are included here to serve as inspiration for prospective works.

Switch Device Scaling

Building off of the switch-stress metric presented in Chapter 7, further survey data is required to more accurately capture the ever-improving switch technologies. The scaling law coefficients extracted by [143] rely on a small data-set of switching devices. An expansion of the component survey in [13] can encompass switching devices and the associated on-state resistance, gate charge, output capacitance, and device area to better track scaling trends. Using scaling laws for device comparison on different operating conditions is particularly of interest as technologies such as GaNFETs are improving not only in high-voltage devices, but also in low-voltage ranges, becoming more competitive with Si MOSFETs.

Switch Reliability

In the same area of component characterization, an analysis of switch reliability on switches achieving ZVS could further bolster the merits of soft-switching techniques. Also, potentially, better FOM devices could be operated at higher voltages without risk of failure if softly switched.

Comparison of Isolated Topologies to Hybrid SC Topologies

Because hybrid SC converters are still an emerging area of power electronics, there are still many unanswered questions regarding the comparison of these converters to more established topologies and transformer-based topologies, such as the LLC converter. Expansion of the topology comparison based on the analysis in Chapter 3 and presented fully in [34] to include transformer analysis can serve as a starting point. However, one challenge is the difference in sizing philosophies of capacitors/inductors versus transformers. Because capacitors and inductors store energy, sizing these components depends on the peak energy storage requirements, but transformers ideally do not store any energy. Therefore, potentially a different methodology than the one presented for capacitors and inductors is required for sizing transformers. Furthermore, high performance transformers are typically custom designs, complicating a potential derivation of scaling laws or general trends in power density, turns ratio, etc.

A more complete comparison of topologies might also require consideration of losses, however, loss modeling tends to be complex and not provide a closed-form relationship between optimal operating parameters.

Knowing at which conversion ratio transformer-based topologies become more attractive than capacitor-based topologies (for a specific design space) opens further research avenues.

Merged SC with Isolated Topology

Having a topology comparison framework including both isolated and non-isolated topologies allows further expansion to merged topologies which utilize both a switched-capacitor (or hybrid SC) stage and a transformer stage [153–155]. In a merged topology, there will be a trade-off in the conversion ratio of the (hybrid) SC stage and the transformer conversion ratio. Furthermore investigation into the operation of these merged topologies will be necessary, especially in switching strategies and modulation techniques which might present different challenges in a merged topology than in a more conventional solution.

8.2 Conclusion

Hybrid switched-capacitor converters have shown initial promise in applications requiring high power density and high efficiency, however, investigations into more complex operation has been lacking. Specifically for applications which could benefit from soft-switching, or those which require EMI mitigation or voltage regulation, this work explores both conventional and novel switching techniques applied to hybrid SC converters. A general analysis of these converters to determine both passive component and switching device sizing is presented. This analytical framework is useful not only for evaluating sizing requirements of a specific design, but also for comparing a set of topologies. A detailed derivation is provided for operational phase timings that ensure soft-charging of flying capacitors in a range of operating conditions. Furthermore, a derivation of zero-voltage switching conditions is de-

scribed, including practical considerations, such as the non-linear output capacitance of the switching devices. This dissertation presented both theoretical discussions and experimental validation of various switching control schemes for hybrid switched-capacitor converters using example hybrid Dickson converters, however, the analysis is applicable to many hybrid SC converters. Moreover, to demonstrate the capability of these more power-dense converters to perform in constrained environments, such as automotive applications, a hybrid SC converter is designed using automotive-rating components and several methods for mitigating EMI are presented and validated. This dissertation presents analysis and validation of complex switching schemes demonstrated on a relatively new branch of power converters, which utilize energy-dense capacitors and better figure-of-merit switching devices to achieve high performance.

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Appendix A

Switch Voltages: Split-Phase Hybrid Dickson Converter

With the flying capacitor voltage at the beginning and end of Phases 1/2 a/b, as well as knowing when switches need to be discharge for ZVS, the voltage stored on each switch output capacitance is given in Table A.3 for an even N:1 converter. For all even-N:1 hybrid Dickson converters, S_1-S_6 are common with S_1-S_4 as the 'bridge' switches, S_5 as the inner split-phase switch, and S_6 as the first main-phase 'string' switch. Furthermore, the switches S_{N+3} (the last main-phase 'string' switch), and S_{N+4} (the outer split-phase switch) are common for all even-N hybrid Dickson converters. As the conversion ratio increases above 4:1, a number of S_{odd}, and S_{even} switches are added. It is shown that the split-phase switches S_5 and S_{N+4} not only discharge/charge during the ZVS sub-periods, but also charge during the main 'a' and 'b' phases when they are OFF, depicted in Fig. 4.6. he maximum blocking voltage of each switch can now be determined based on the preceding analysis. The maximum drain-source voltages of each switch for an even-N hybrid Dickson converter are given in Table A.1 (odd-N in Table A.2. Of note are switches S_6 and S_{N+3} which exhibit maximum blocking voltage at the split-phase times, $\tau_{\text{split},1}$ and $\tau_{\text{split},2}$ respectively, rather than at Phase 1 and Phase 2 transitions (at $T_{\text{sw}}/2$ and T_{sw}) where all other switches encounter their maximum blocking voltage. These switches are 'string' switches that are connected between one 'string' switch and one 'split-phase' switch. If the simpler case of an $N = 4$ split-phase Dickson converter was analyzed and higher-order converter voltage stresses extrapolated from the $N = 4$ case, this notable condition would be missed. With increased capacitor utilization (larger voltage ripple conditions), the difference in blocking voltage of switches S_6 and S_{N+3}, and other 'string' switches S_7–S_{N+2} also increases and care should be taken in the sizing of these switches to ensure that no switch voltage ratings are violated. Switch voltages at each phase transition for an even-N hybrid Dickson converter are given in Table A.3.

Table A.1: Maximum Switch Voltage Stress (even-$N \geq 6$)

$V_{\mathbf{ds,max},i}$	
$\frac{1}{N}V_{\text{HI}} + \frac{N-1}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \leq \mathbb{N} \leq 4\}$
$\frac{1}{N}V_{\text{HI}} + \frac{N-1}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{5, N+4\}$
$\frac{2}{N}V_{\text{HI}} + \frac{N-4}{2N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{6, N+3\}$
$\frac{2}{N}V_{\text{HI}} + \frac{2}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{7 \leq \mathbb{N} \leq N+2\}$

Table A.2: Maximum Switch Voltage Stress (split-phase odd-N Dickson)

$V_{\mathbf{ds,max},i}$	
$\frac{1}{N}V_{\text{HI}} + \frac{N-1}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \leq \mathbb{N} \leq 4\}$
$\frac{1}{N}V_{\text{HI}} + \frac{N-1}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{5, N+4\}$
$\frac{2}{N}V_{\text{HI}} + \frac{N-4}{2N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{6, N+3\}$
$\frac{2}{N}V_{\text{HI}} + \frac{2}{N}\frac{q_{\text{HI}}}{C_0}$	$i \in \{7 \leq \mathbb{N} \leq N+2\}$

Table A.3: Switch Voltages for a ZVS Split-Phase Even-N Dickson Converter

time	$v_{\mathrm{ds}_{1,3}}$	$v_{\mathrm{ds}_{2,4}}$	v_{ds_5}	v_{ds_6}	$v_{\mathrm{ds}_{odd}}$	$v_{\mathrm{ds}_{even}}$	$v_{\mathrm{ds}_{N+3}}$	$v_{\mathrm{ds}_{N+4}}$
$t=0$	0	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$
$t=\tau_1$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$
ΔV_{z1a}	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$	0
$t=\tau_1$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$
$t=\tau_{\mathrm{sp},1}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}+(N-4)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+(N-2)\Delta v_c}{N}$
ΔV_{1a}	0	$-(2\Delta v_c)$	0	Δv_c	0	0	0	Δv_c
$t=\tau_{\mathrm{sp},1}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}+(N-4)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+(N-2)\Delta v_c}{N}$
$t=\tau_2$	0	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$2\Delta v_c$	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$
ΔV_{1b}	0	$-(2\Delta v_c)$	$2\Delta v_c$	$-(\Delta v_c)$	0	0	0	Δv_c
$t=\tau_2$	0	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$2\Delta v_c$	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$
$t=\frac{T_{sw}}{2}$	0	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$
ΔV_{z1b}	0	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	0
$t=\frac{T_{sw}}{2}$	0	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$
$t=\tau_3$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0
ΔV_{z2a}	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	0	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}\right)$
$t=\tau_3$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0
$t=\tau_{\mathrm{sp},2}$	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+(N-2)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}+(N-4)\Delta v_c}{N}$	0
ΔV_{2a}	$-(2\Delta v_c)$	0	Δv_c	0	0	0	Δv_c	0
$t=\tau_{\mathrm{sp},2}$	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+(N-2)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-5\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}+(N-4)\Delta v_c}{N}$	0
$t=\tau_4$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	$2\Delta v_c$
ΔV_{2b}	$-(2\Delta v_c)$	0	Δv_c	0	0	0	$-(\Delta v_c)$	$2\Delta v_c$
$t=\tau_4$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	0	$\frac{2V_{\mathrm{HI}}-4\Delta v_c}{N}$	$2\Delta v_c$
$t=T_{\mathrm{sw}}$	0	0	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}+2(N-1)\Delta v_c}{N}$	$\frac{V_{\mathrm{HI}}-2\Delta v_c}{N}$
ΔV_{z2b}	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	0	0	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$	$-\left(\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}\right)$	$\frac{V_{\mathrm{HI}}-2(N+1)\Delta v_c}{N}$