UNIVERSITY OF CALIFORNIA, SAN DIEGO

High Power, Linear CMOS Power Amplifier for WLAN Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor William Trogler

2013

The dissertation of Ali Afsahi is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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2013

DEDICATION

To my parents, Ziba and Abbas
my wife, Ghazaleh, and my daughter Bahar.

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PUBLICATIONS

A. Afsahi, A. Behzad, V. Magoon and L. E. Larson, "Fully Integrated Dual-Band Power Amplifiers with on-chip Baluns in 65nm CMOS for an 802.11n MIMO WLAN SoC", *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 365-368, June 2009.

A. Afsahi, A. Behzad and L. E. Larson, "A 65nm CMOS 2.4GHz 31.5dBm Power Amplifier with a Distributed-LC Power-Combining Network and Improved Linearization for WLAN Applications", *ISSCC Digest of Technical papers*, pp. 452-453, February 2010.

A. Afsahi, A. Behzad, V. Magoon and L.E. Larson, "Linearized Dual-Band Power Amplifiers With Integrated Baluns in 65 nm CMOS for a 2x2 802.11n MIMO WLAN SoC", *IEEE Journal of Solid State Circuits*, vol. 45, no. 5, pp. 955-966, May 2010

A. Afsahi, and L.E. Larson, "An Integrated 33.5dBm Linear 2.4GHz Power Amplifier in 65nm CMOS for WLAN Applications", *IEEE Custom Integrated Circuits Conference*, pp. 611-614, September 2010

A. Afsahi and L. E. Larson, "Monolithic Power-Combining Techniques for Watt-Level 2.4-GHz CMOS Power Amplifiers for WLAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1247-1260, March 2013.

ABSTRACT OF THE DISSERTATION

High Power, Linear CMOS Power Amplifier for WLAN Applications

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Professor Lawrence Larson, Chair
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The advancement of CMOS technology has enabled a high level of integration in modern, low cost, small form-factor and low power wireless devices. While power amplifiers (PAs) are key components in wireless transceivers, their realization and integration in standard CMOS technology has shown several challenges. The modern wireless standards such as WLAN and LTE, utilize higher order modulation schemes in order to increase the data rate and efficiently use the limited available spectrum and also provide a robust link in a fading environment. These modulations possess a very high peak-to-average ratio (PAR) and require a very linear power amplifier to preserve the integrity of the signal.

In this dissertation several linearization and power combining techniques

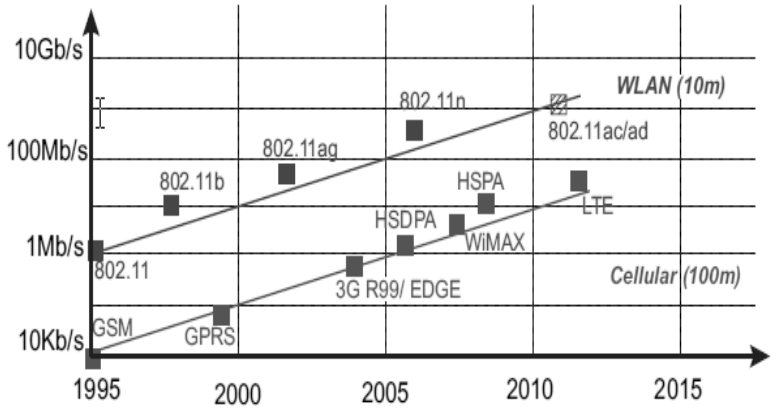
have been proposed to address the challenges of designing a high power and linear PA in CMOS for WLAN applications. To demonstrate these techniques in silicon, three chips have been designed and fabricated in 65nm standard CMOS. In the first chip, a fully integrated dual-band power amplifiers with on-chip baluns for 802.11n MIMO WLAN applications are implemented. With a 3.3v supply, the PAs produce a saturated output power of 28.3dBm and 26.7dBm with peak drain efficiency of 35.3% and 25.3% for the 2.4GHz and 5GHz bands, respectively. By utilizing multiple fully self-contained linearization algorithms, an EVM of -25dB is achieved at 22.4dBm for the 2.4GHz band and 20.5dBm for the 5GHz band while transmitting 54Mbs OFDM. In the next two designs, two monolithic power combining schemes for CMOS power amplifiers, distributed-LC and current-mode transformer-based, are compared. Fully integrated 2.4GHz power amplifiers (PAs) using these techniques were fabricated. From a 3.3 V supply, the distributed-LC combined PA produces a saturated power of 31.5dBm with peak PAE of 25%. The current-mode transformer based PA combiner produces 33.5dBm saturated power with 37.6% peak PAE. With gm-linearization and digital pre-distortion, these PAs transmit 25.5dBm and 26.4dBm with -25dB EVM for a 54Mb/s OFDM signal respectively.

Chapter 1

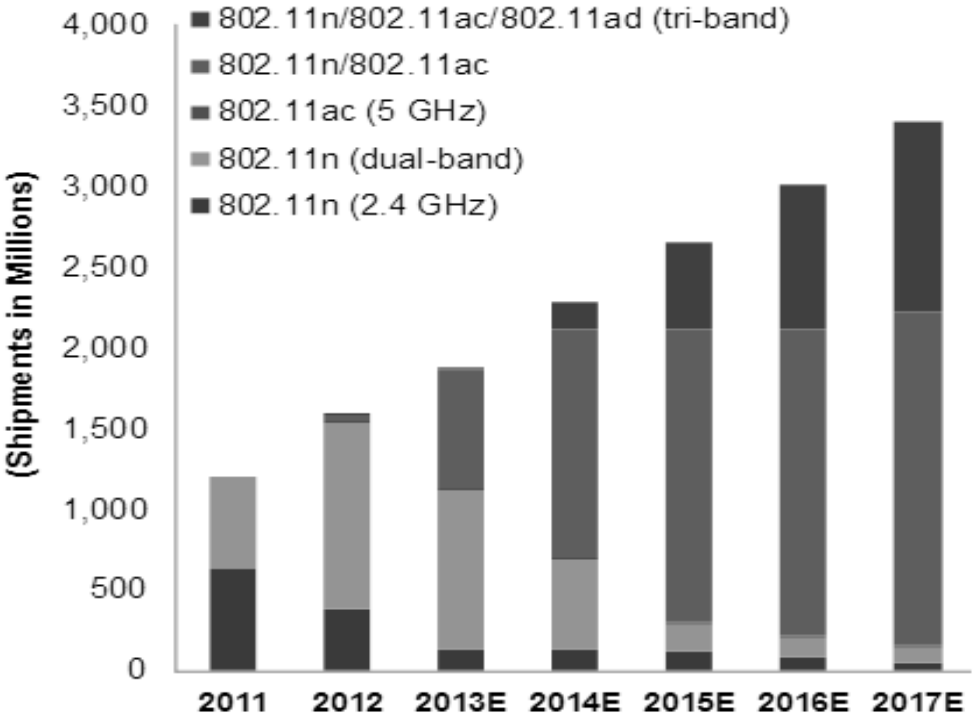
Introduction

Consumer demand for WiFi-enabled products has increased over the last several years, and analyst reports conclude that the sales momentum is expected to continue for the next several years. From laptops to cell phones to television sets, our desire to share broadband information is making wireless connectivity a must-have feature for a range of devices. Figure 1.1 (a) shows the increasing demand for high data rate wireless communication and (b) shows the number of WiFi SoC (System on Chip) chips that have been sold in the last few years.

In order to keep the cost down and have smaller form-factor especially for embedded applications, the transceiver has been integrated with the baseband physical layer (PHY) and media access control (MAC) as an SoC solution in a pure CMOS process [3–9]. One of the main contributors to the cost and size of the solution is the external power amplifiers (PA). Most commercial PAs are not implemented in CMOS but are instead implemented in more expensive technologies like GaAs or SiGe. The focus of this research is on designing a fully integrated, reliable and efficient CMOS power amplifier for Wireless Local Area Network (WLAN) applications, while meeting the stringent requirements of the WLAN standards. In addition, several power combining techniques have been explored to boost the output power efficiently for watt-level applications. It should be noted that these techniques can be applied to other technologies such as GaAs, SiGe or SOI and other wireless standards like Long Term Evolution (LTE) or Worldwide Interoperability for Microwave Access (WiMAX). This introductory chapter will provide



(a)



(b)

Figure 1.1: (a) Growth of high data rate wireless communication [1]. (b) WLAN chipset volume growth chart [2].

some background for this research. First, we will go over the motivations and challenges of designing CMOS integrated PAs. Next, the key requirements of the

WLAN standard will be discussed. We will conclude this chapter with the focus and organization of this dissertation.

1.1 Motivation and Challenges

Figure 1.2 shows a high-level block diagram representing the most common current WiFi solutions [3]. In order to achieve a low cost and compact solution, the transceiver has been highly integrated with the baseband PHY and MAC as an SoC solution, preferably in a pure CMOS process.

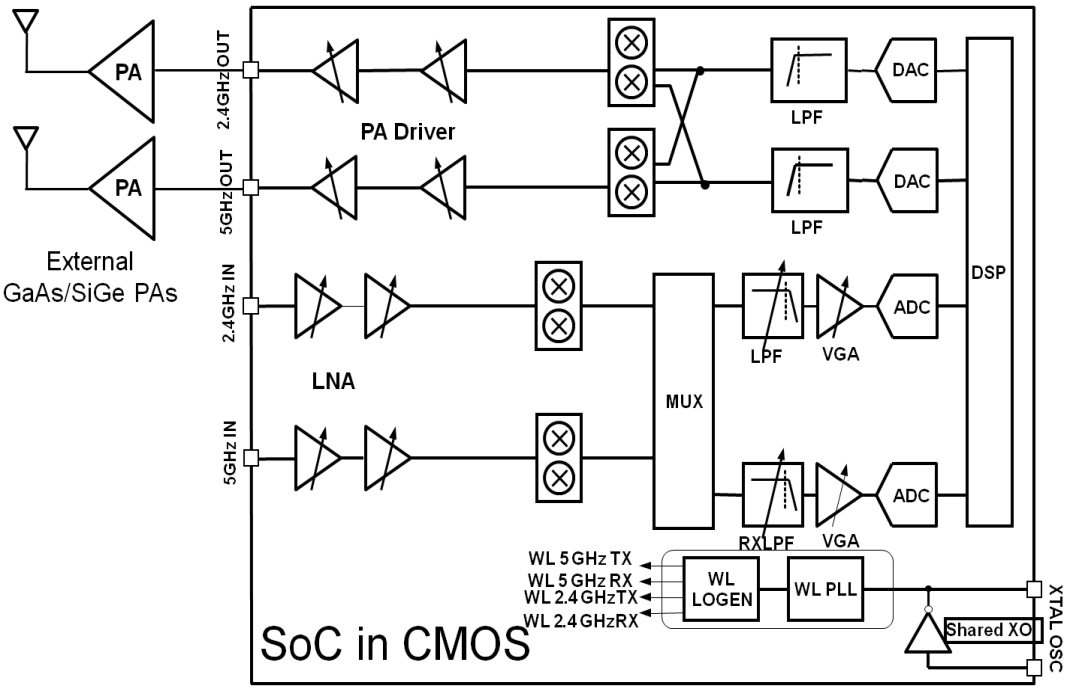


Figure 1.2: High level block diagram of a recent WLAN SoC.

One of the main contributors to the cost and size of the solution is the external power amplifiers (PAs). The PAs are often implemented as a stand-alone module in expensive processes like GaAs or SiGe. For example, in a dual-band 2x2 solution, four PAs are needed to cover both the 2.4-2.5 GHz and 4.9-5.9 GHz bands, which increases the cost and form-factor of the solution significantly. The primary reasons for using these processes are higher output power, better linearity, higher efficiency and better reliability. Recently, there has been a significant amount of

effort to implement the PA in CMOS [**?**, 10–19]. However, the low supply voltage, lossy substrate, lower quality factor passives and lower breakdown voltage make the design of a linear, high power and reliable PA quite challenging in CMOS technology. The integration of these PAs in an SoC poses additional challenges that must be addressed. These include the need for integration in an RF-unfriendly package (higher ground impedance, larger package inductance, higher loss, etc.), and pulling issues of the voltage controlled oscillator (VCO) with the phased lock loop (PLL) integrated on the same substrate. Another challenge, which is even more problematic when integrating PAs in multi-input multi-output (MIMO) systems, is the issue of thermal dissipation. The lower inherent power-added efficiency of CMOS PAs, the simultaneous operation of multiple PAs, and the thermal limitations of the package could all cause the die temperature to rise substantially.

Driven by the need for higher data-rates, WLAN standards utilize higher order modulation schemes and orthogonal frequency division multiplexing coding (OFDM) in order to efficiently use the limited available spectrum and also provide a robust link in a fading environment. OFDM modulation possesses a very high peak-to-average ratio (PAR) and requires a very linear power amplifier to preserve the integrity of the signal. For example, an EVM (error vector magnitude) of -28 dB is required for the higher modulation and coding schemes of the standard. This level of EVM and linearity can be achieved by backing off the average OFDM power from the saturation power, at the expense of lower transmit power and severely degraded efficiency. In general, CMOS PAs exhibit inferior inherent linearity compared to GaAs and SiGe PAs [20]. In addition, deep-submicron CMOS PAs exhibit much larger AM-PM distortion due to the highly nonlinear device capacitance and output resistance. This would require the system to back-off even further from the saturated power of the PA, resulting in even lower transmit power and lower efficiency.

1.2 WLAN Standard and Transmitter System Requirements

A WLAN system (Fig. 1.3) consists of a network hardware backbone, along with several detached components such as PCs, laptops, tablets, TVs, cell phones, printers, etc. as clients [21]. These clients then can access local area network resources remotely using radio-frequency (RF) technology.

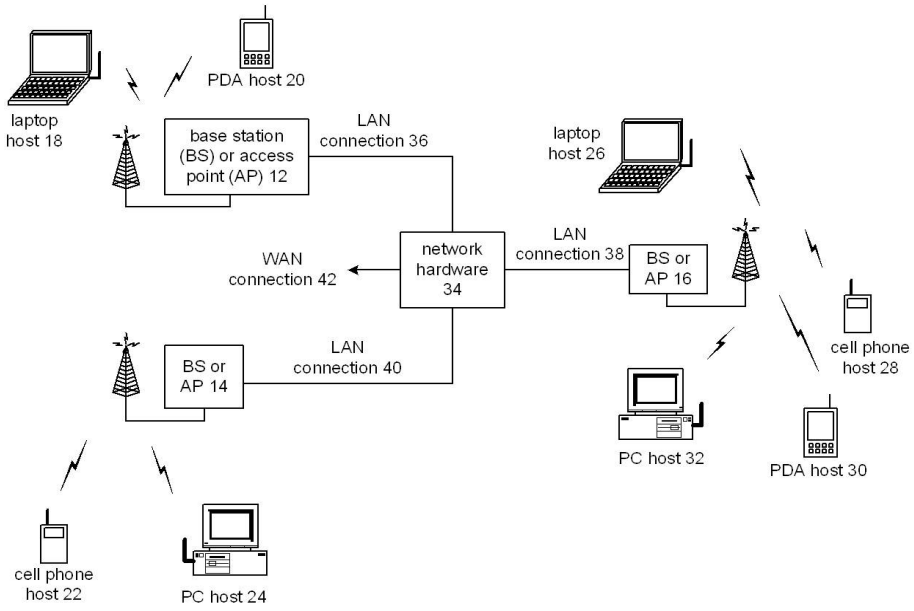


Figure 1.3: Example of WLAN network.

IEEE 802.11 is a specific standard that defines the PHY and MAC layers of a WLAN. Since the time it was approved in 1997, several extensions have been added such as

- 802.11b Operates at the 2.40GHz ISM band and supports data rates of 5.5 and 11 Mbps using complementary code keying (CCK) techniques.

- 802.11a Operates at the 5-GHz band and allows for data rates of 6-54Mbps using OFDM technique.

- 802.11g Operates at the 2.4GHz ISM band and supports data rates from 1 to 54Mbps and is backward compatible with the 802.11b standard.

- 802.11n Operates at 2.4GHz and 5GHz bands and allows for multichannel

and higher data rates. 802.11n can achieve up to 600 Mbps by adoption of (MIMO) techniques as well as the use of wider band channels in combination with space-time signal processing, space-time coding (STC) and space division multiplexing (SDM) [22, 23].

- 802.11ac Operates at 5GHz band enables a maximum single link throughput of at least 500Mbps. This is accomplished by wider RF bandwidth (up to 160MHz), more MIMO spatial streams (up to 8), multi-user MIMO and high-density modulation (up to 256 QAM).

1.2.1 Transmitter Error Vector Magnitude

One of the system requirements specified by 802.11 is transmitter EVM, which is a single scalar number indicating the quality of the modulated signal. To calculate EVM, one needs to compare the real symbols with their ideal symbols on the constellation diagram and calculate the error vectors as shown in Fig. 1.4. For a given symbol, EVM is defined as

$$EVM = \sqrt{\frac{\sum_{i=1}^{M} |Z(i) - R(i)|^2}{\sum_{i=1}^{M} |R(i)|^2}} \tag{1.1}$$

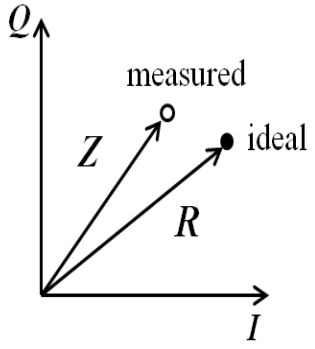


Figure 1.4: Ideal and measured constellation point.

where Z is the measured signal, R is ideal signal, M is the order of the constellation and i is the measurement index. Any systemic error would simply shift the actual constellation points as compared to ideal ones and can be corrected in the

receiver. However, any nonsystematic imperfections, such as random noise, can create an uncertain region in the constellation points about the ideal constellation points. The EVM can be expressed in percentage (maximum 100% and minimum 0%) or decibels as 20Log (EVM). EVM is a function of variety of impairments in transceivers such as phase noise, filter shapes and bandwidth, quadrature imbalances, nonlinearities and memory effect. In a high performance transmitter the last two impairments are mainly dominated by the PA performance. The reason that EVM is commonly used as a metric of the quality of the transmitter is that it is impacted by many such impairments. For the 802.11a and 802.11g, at 54Mbps, the required EVM is -25dB and for 802.11n with higher data rate the required EVM is -28dB.

1.2.2 Transmitter Spectral Mask

The 802.11 standard requires transmitter to meet a certain spectral mask for each modulation type. A linear system can be modeled as

$$y(t) = ax(t) \tag{1.2}$$

Where a is constant. If a sinusoid signal with frequency f_1 is applied as $x(t)$ the output spectrum will only have components at f_1. On the other hand, a nonlinear system can generate frequencies in the output spectrum that did not exist in the input signal. As an example, let's assume that a nonlinear system can be modeled as

$$y(t) = ax^2(t) \tag{1.3}$$

If a sinusoid of frequency f_1 is applied as the input, the output spectrum will have components at f_1 and $2f_1$ and DC. In this system, if two sinusoids with frequencies of f_1 and f_2 are applied at the input, new tones at $2f_1$, $2f_2$, f_1-f_2 and f_2+f_1 will be present at the output. All the modulations used by 802.11 standard have relatively high peak-to-average-ratio (PAR). When a modulated signal with bandwidth W is passed through a linear system, the output will be a signal with the same bandwidth. In contrast, when a non-constant-envelope signal is passed through a nonlinear system the bandwidth of the output signal will be expanded.

If we assume there is more than a single CW tone present at the input of a nonlinear system, the intermodulation (IM) terms will be generated at the output and specifically, the odd-ordered intermodulation terms (IM3, IM5, etc.) are the ones causing spectral regrowth. IM terms can generate spectral components that show up very close to the frequencies of the input. For example, for the case where there are only two CW input tones at frequencies f_1 and f_2, the IM3 components fall at $2f_1$-f_2 and $2f_2$-f_1, which will fall fairly close in frequency to the main signal and will be very difficult to filter. These unwanted spectral components, created by passing of a non-constant-envelope modulated signal through a nonlinear system, are referred to as spectral regrowth. Spectral regrowth can cause several problems in a system. In some platforms, like a cell phone where we have multiple wireless transceivers, the spectral regrowth of one transmitter can cause desensitization of the receiver of a different system in the same platform. For example, the transmitter of a WLAN system operating at 2.4GHz can desensitize the receiver of a wireless WCDMA (2110MHz-2170MHz) or LTE (2300MHz-2400MHz) cellular receiver. In a full-duplex system, a transmitter can generate enough out-of-band energy due to spectral regrowth to saturate its own receiver. Another problem caused by spectral regrowth is to create interference with adjacent channels.

These are the primary reasons why public standards define a spectral mask for system transmitters. In a well-designed transmitter, the spectral regrowth is typically caused by the most nonlinear block of the transmitter, which is usually the power amplifier. However, many other factors can cause spectral mask violations such as baseband/digital noise due to insufficient analog or digital filtering and phase noise of the RF phase-locked loop (PLL). Figure 1.5 shows the spectral mask requirements for 802.11a [21]. The modulated signal for 802.11a is constructed of 52 subcarriers with modulated data around each of these subcarriers, and possesses a very high PAR. As this signal is passed through a nonlinear system, these subcarriers can create intermodulation components and cause spectral regrowth. The standard requires that the spectrum of the transmitted signal be more than 20, 28 and 40 dBc below the peak of the modulated signal at offset frequencies of 11, 20 and 30 MHz away from the center of the band respectively.

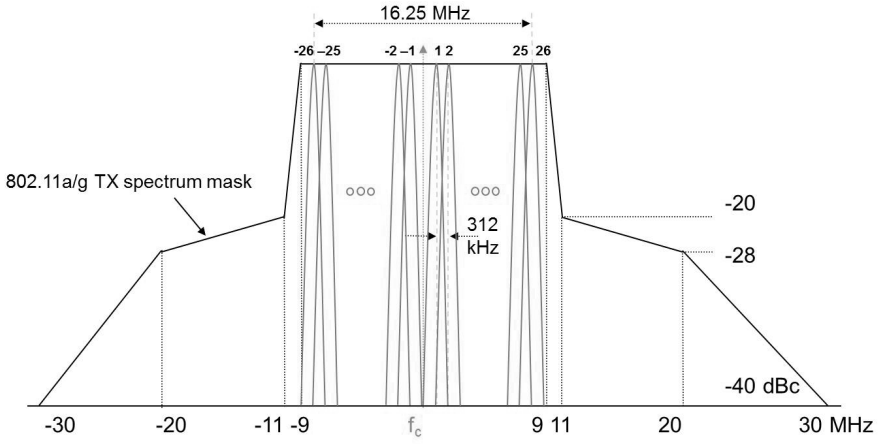


Figure 1.5: 802.11a spectral mask.

1.3 Dissertation Organization

Chapter 2 of this thesis describes important specifications of a power amplifier, introduces some of the common classes of PA operation, and introduces some of the techniques to improve these specifications. In Chapter 3, different types of matching networks for power amplifier, along with their advantages and limitations, are presented. Chapter 4 goes over the details of the architecture and circuit designs as well as measurement results of a linearized dual-band fully integrated CMOS PA for WLAN applications. Different power combiner techniques are discussed and compared in Chapter 5. As a case study, the details of the design and measurements results of two fully integrated CMOS power amplifiers, using two of the proposed combiners, are presented. Chapter 6 concludes the thesis and discusses future directions in the field of high-power, linear and efficient CMOS PA for wireless applications.

Chapter 2

Power Amplifiers: Fundamentals and Limitations

Power amplifiers are used to amplify the signals delivered to the antenna to the desired level, without compromising signal integrity, so that receiver can recover the information transmitted by transmitter. Power amplifiers are classified in different classes according to their circuit configuration. There is a trade-off between linearity and efficiency in these classes and depending on the modulation scheme one needs to select the proper class of operation to meet the standard requirements. In this chapter, the operation mode of different PA classes and their limitation in terms of efficiency and linearity will be discussed. Several linearization and efficiency enhancement techniques will be presented. Finally the chapter will conclude with a summary.

2.1 Fundamentals of Transistor Power Amplifiers

2.1.1 Efficiency of Power Amplifiers

PAs are the most power-hungry block in transceivers and therefore efficiency is a crucial parameter for power amplifiers. There are three definitions that are commonly used in the literature, drain (collector) efficiency, the power added efficiency and the overall efficiency. The drain efficiency (η_{drain}) is defined as

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.1}$$

where P_{DC} is the power drawn from the DC power supply and P_{out} is the average RF power delivered to the load. The drain efficiency ignores the power delivered by the input signal. In some cases, the PA may have a relatively low power gain and requires large RF input power. In this case, the power added efficiency and the overall efficiency provide a more accurate metric of the PA performance. The power added efficiency (PAE) is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.2}$$

where P_{in} is the input power.

2.1.2 Power Output Capability

The power output capability, P_C, is used to compare different types of power amplifier designs. It is a performance metric that measures the amount of the power that one PA can deliver when its transistor is operating under the maximum current (I_{max}) and voltage (V_{max}) reliability limits. Power output capability is defined by

$$P_C = \frac{P_{out}}{I_{max} V_{max}} \tag{2.3}$$

Power output capability is thus a parameter that calculates how well a power amplifier utilizes the device technology to deliver the required output power. A high P_C PA can deliver the required power with a smaller number of devices.

2.1.3 Amplifier Linearity

As discussed in the previous chapter, PA linearity is one of the key requirements on wireless transmitters, especially for the systems that employ complex modulation with amplitude variation like WLAN and LTE. PA nonlinearity causes spectral regrowth and adjacent channel interference. Wireless standards specify a spectral mask to limit the out-of-band leakage. In addition to the spectral mask, PA nonlinearity can degrade the quality of the in-band signal, which is quantified

by the EVM specification based on the modulation type to guarantee an acceptable bit error rate in the receiver.

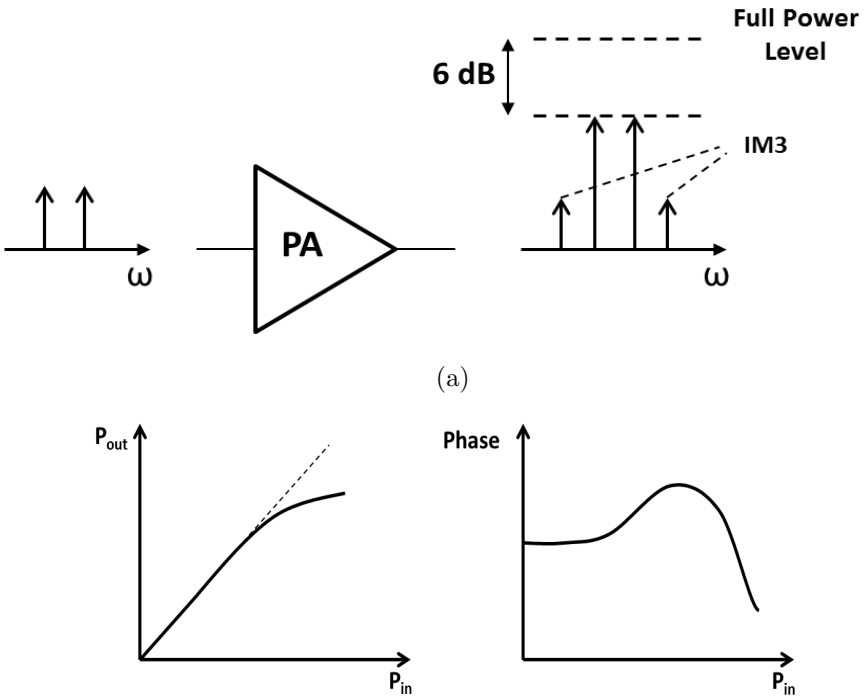


Figure 2.1: (a) PA third order intermodulation. (b) PA AM-AM and AM-PM distortions.

In order to characterize PA nonlinearity, one can use the actual modulated signal to simulate the circuit, and simulate ACPR and EVM, but this would be a very time consuming simulation, especially during the design optimization phase. Instead, PA characterization begins with two general tests of nonlinearity based on CW tones: an intermodulation test and amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) response tests. In the first method, two sinusoidal tones are employed, and the amplitude of each tone is chosen such that it is 6dB below the full power, thus generating the maximum output voltage swing when the two tones add in-phase. The resulting intermodulation terms can provide some indication of ACPR as well as EVM (Fig. 2.1 (a)). In the second method (AM-AM and AM-PM tests), a single tone is applied to the input and its amplitude is

gradually increased and the output amplitude and phase relative to the input are measured. In a perfectly linear system, the output amplitude is a scaled version of the input amplitude and the output phase is shifted from the input phase by a fixed amount. However, in a nonlinear system, there will be some compression in output amplitude and some variation in the output phase as the input amplitude increases (Fig. 2.1 (b)).

In nano-scale CMOS technology, even the linear class PAs such as class-A or AB, show gain compression and phase distortion at large back-off from the maximum output swing due to low device output impedance and variable junction capacitors. As the result, a large back-off from the maximum output voltage is required to meet linearity requirements. This often results in very poor efficiency in cases where a modulated signal with high peak-to-average ratio is used.

2.2 Power Amplifier Classes

2.2.1 Class A, AB, B and C

Class A, AB, B and C amplifiers utilize similar circuit configuration and are distinguished by biasing conditions. Figure 2.2 shows the simplified circuit model of these power amplifiers.

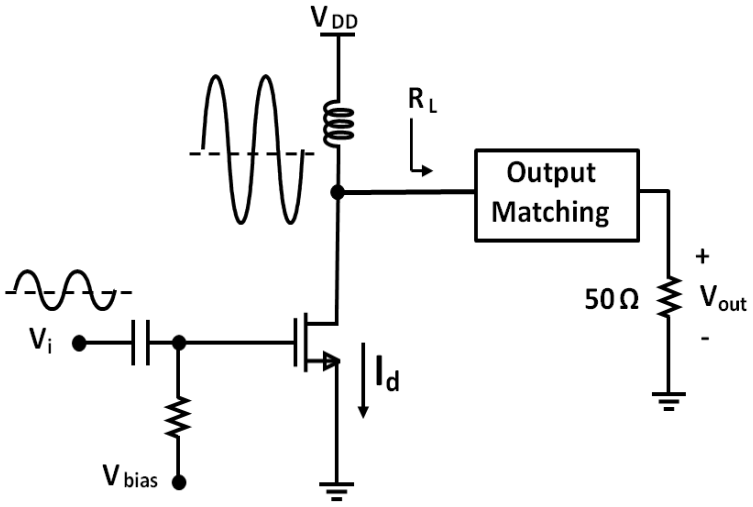


Figure 2.2: Simplified circuit model of a class A, AB, B or C PA.

The active device acts as a transconductor (g_m), which converts the input voltage to current and directs it to the load. The portion of the input signal cycle where the active device is on and conducts the current is known as the *conduction angle* and it defines the class of operation. In a class-A PA, the active device is always conducting current (*conduction angle* = 360°). Class-A amplifiers are typically more linear and less complex than other types, but are very inefficient. The drain efficiency of the PA can be calculated from

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} = \frac{i_d^2 R_L}{2 V_{DD} I_D} \tag{2.4}$$

where i_d is the drain current amplitude, V_{DD} is the supply voltage, I_D is the PA DC current and R_L is the load impedance. At max power, i_d=I_D and V_{DD}=$R_L i_d$ therefore the maximum drain efficiency is only 50% [24]. However, in practice the actual efficiency will be even lower due to device and layout parasitics and finite knee voltage of the active device, which reduces the maximum signal swing.

The DC power dissipation is independent of the signal level and is always fixed, which means at best case 50% of the power will be dissipated in active device. There have been extensive efforts to reduce the power dissipation in the transistor, which have been the base for development of different classes of power amplifiers.

The instantaneous power dissipation in the transistor is the product of its drain current and voltage. One way to minimize this loss is to reduce the conduction angle such that the device only draws current when the drain voltage is at its minimum. The PA classes are based on the *conduction angle*: Class-AB (180°<*conduction angle* <360°), Class-B (*conduction angle* = 180°) and Class-C (*conduction angle* <180°). The Maximum drain efficiency as a function of α (half of the conduction angle) can be calculated from [25]

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \frac{\alpha - sin(\alpha)cos(\alpha)}{sin(\alpha) - \alpha cos(\alpha)} \tag{2.5}$$

and is shown in Fig. 2.3. Note that efficiency increases monotonically with the decrease in conduction angle. The peak theoretical efficiency is 50% at Class-A, 78.5% at Class-B and approaching 100% as α approaches zero. Unfortunately, the

apparent high efficiency at the Class-C bias is also at the expense of a diminishing deliverable output power. It can be shown that [24]

$$P_{out} \propto \frac{2\alpha - sin(2\alpha)}{1 - cos(\alpha)} \tag{2.6}$$

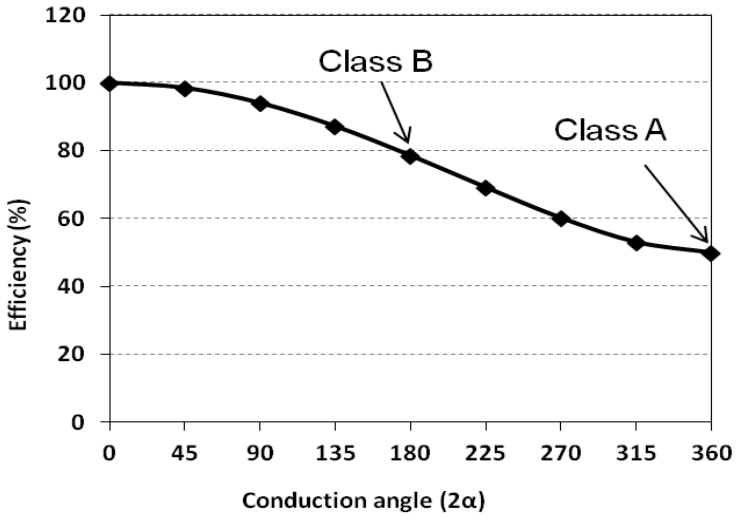


Figure 2.3: PA efficiency as a function of conduction angle.

Class A and reduced conduction angle PAs use a simple resonant load which resonates at the fundamental frequency. Although the efficiency improves by reducing conduction angle, the power capacity and gain will drop severely.

There are some derivative PA topologies, which improve efficiency while maintaining the power capacity by using a multiple-resonator output filter. This filter controls the harmonic content of the drain voltage and/or current, by shaping their waveforms to reduce the power dissipated in the active device. These PAs are named class-F amplifiers and have their own sub-categories: class F1, F2 and F3 [24, 26]. The class A amplifier and its derivatives (AB, B, C and F) are called *linear* amplifiers because they linearly amplify the fundamental component and can preserve both phase and amplitude information.

2.2.2 Switching Power Amplifiers

From the discussion in the previous section, drain voltage and/or drain current shaping is an effective way to enhance amplifier efficiency. The natural way

to do this is to design an amplifier that reduces the transistor's output voltage and current overlapping time. One way to do this is to employ the active device as a switch, driving it with a sufficiently large input signal so that it either is on (high current/low voltage) or off (low voltage/high current) and ideally eliminate power loss in the transistor and achieve 100% efficiency. Figure 2.4 shows a generalized schematic of a switching PA. In practice, given that we need a large output transistor, there will be some transition going from *on to off* modes and vice versa, which creates overlap between current and voltage of the transistors and increases the power loss in the active device. There are different types of switching-mode PAs (class D, class E, class F2, etc), which deal with the finite voltage and current transition time by proper load design.

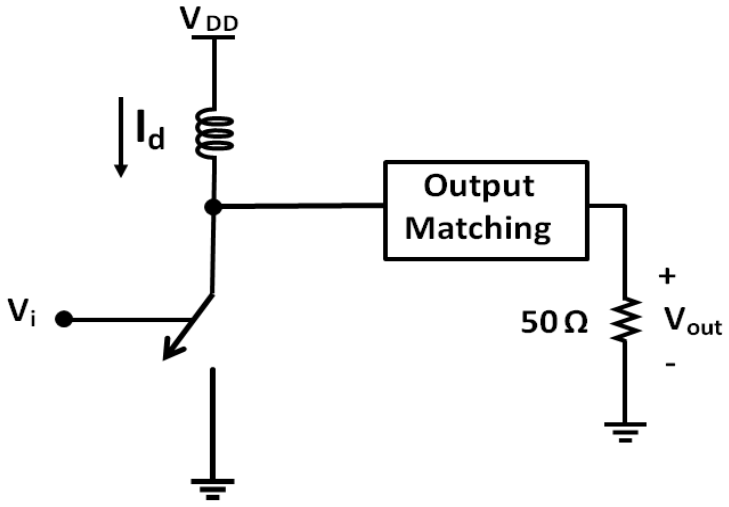


Figure 2.4: Generalized schematic of a switching-mode PA.

A class-D amplifier is composed of a voltage controlled switch and a filtering tank as the load. This can be realized in either single-ended or differential fashion. Figure 2.5 shows one possible implementation, using an n-type differential pair as a switch and a transformer to convert the differential drain signal into the single-ended output.

It can be shown that if the R_{ON} of transistors is finite, the efficiency of the

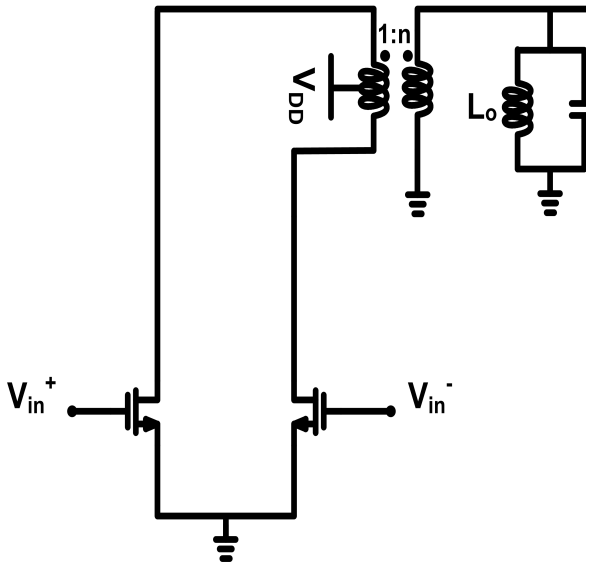


Figure 2.5: Class D PA.

class-D PA can be calculated from [27]

$$\eta = \frac{1}{1 + n^2 R_{ON}/R_L} \leq 100\% \tag{2.7}$$

where n is the transformer turn ratio. Also, the effect of a finite switching time of the device on the overall efficiency can be shown to be [27]

$$\eta_{practical} = \eta_{ideal} \frac{sin\varphi_s}{\varphi_s} \tag{2.8}$$

where φ_s is the angle of the RF cycle taken for the device to switch.

Figure 2.6 shows a circuit schematic of a typical class-E PA. It consists of an RF choke which provides constant DC current and has infinite impedance at RF, a grounded capacitor C2 which can include the drain parasitic capacitance and a series network C_1 and L_1. The value of C_1, C_2 and L_1 are chosen to satisfy two class-E switching conditions: 1) Voltage across the switch reaches zero at the end of the off state 2) The first derivative of the voltage across the switch is zero when the switch turns on (i.e. dV_x/dt=0). These conditions ensure to minimize the overlap between voltage and current of transistor and therefore the power dissipation in switch. Another property of class-E PAs is the large peak voltage across switch in off state (approximately $3.56V_{DD}$-$2.56V_S$ where V_S is the minimum voltage across switch), which raises the reliability risk of the class-E PA [28].

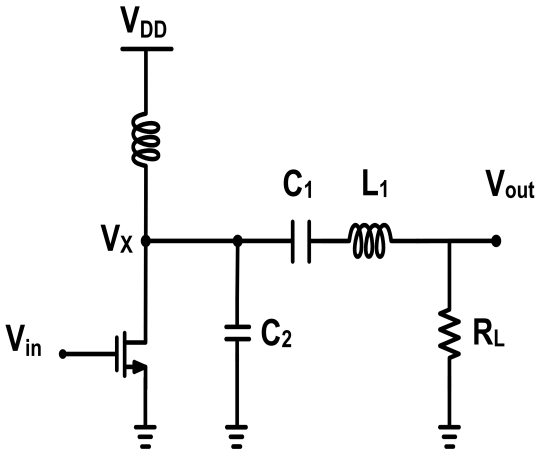


Figure 2.6: Class E PA.

The idea of harmonic shaping described in Section 2.2.1, can be applied in switching PAs as well, which is the basis of the class-F family. Figure 2.7 shows an ideal class-F PA which is constructed with an infinite number of series odd harmonic terminations and a parallel resonator at fundamental frequency. The addition of harmonics, at the correct level, to the fundamental causes a flattening of the drain voltage waveform. The drain voltage waveform becomes approximately a square-wave which results in improved efficiency. If we assume R_{ON} is the on resistance of the switch during the on mode and all the tanks have infinite Q, the drain efficiency of class-F PA can be calculated from [26]

$$\eta = \frac{1}{1 + 2R_{ON}/R_L} \tag{2.9}$$

Switching-mode PAs are inherently non-linear, which makes them unsuitable for more advanced wireless standards that use complex modulation schemes wih both amplitude and phase information and require linear amplification.

2.3 Linearization Techniques

There has been significant effort on linearization techniques to improve the PA linearity and as a result better efficiency and higher output power. In this section, we briefly present three techniques: feedback, feedforward and predistortion.

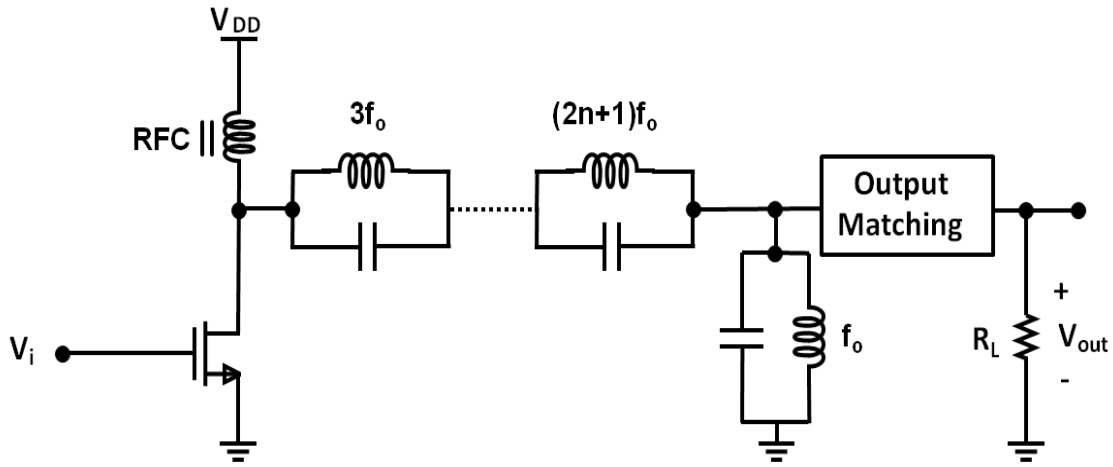


Figure 2.7: Class F PA.

2.3.1 Feedback Linearization

In this technique, an attenuated version of the PA output is compared with the input to create an error which is proportional to the PA nonlinearity. As a result of negative feedback, the loop attempts to minimize the error and makes PA output a replica of PA input. Depending on the frequency of the feedback signal, feedback linearization techniques can be classified into two groups: RF feedback and low-frequency feedback. Figure 2.8 shows the general scheme of RF feedback amplifiers. In practice, adjusting amplitude and phase of the feedback signal accurately at RF is very difficult and increases the risk of instability [29].

Figure 2.9 shows an example of low-frequency feedback known as Cartesian feedback (only one of the quadrature mixers is shown) and first proposed by Petovic in 1983 [30]. In this technique, the sampled RF output signal is downconverted to a baseband signal, which is subtracted from the quadrature input signal to obtain an error signal proportional to the nonlinearity of the transmitter. The feedback loop tries to make the output of the PA a replica of BB_{in}, but at a different carrier frequency. Since the total phase shift through the mixer and the PA is significant, the phase Φ is added to LO signal to synchronize downconversion and upconversion paths and to ensure stability. Cartesian feedback has a practical issue and that is

the choice of the stabilizing LO phase shift, Φ. The loop stability is affected by the loop delay as well as by the characteristics of the nonlinear PA. Also, the required phase shift varies with process and temperature.

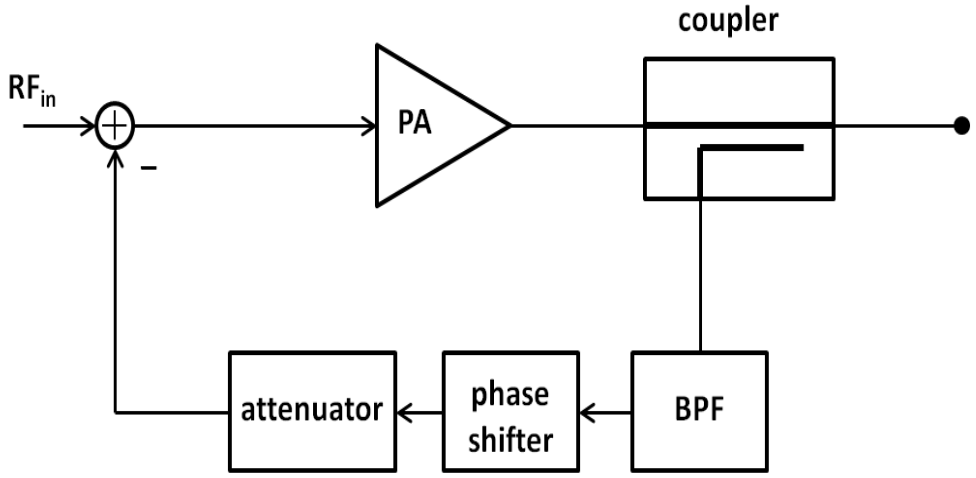


Figure 2.8: RF feedback.

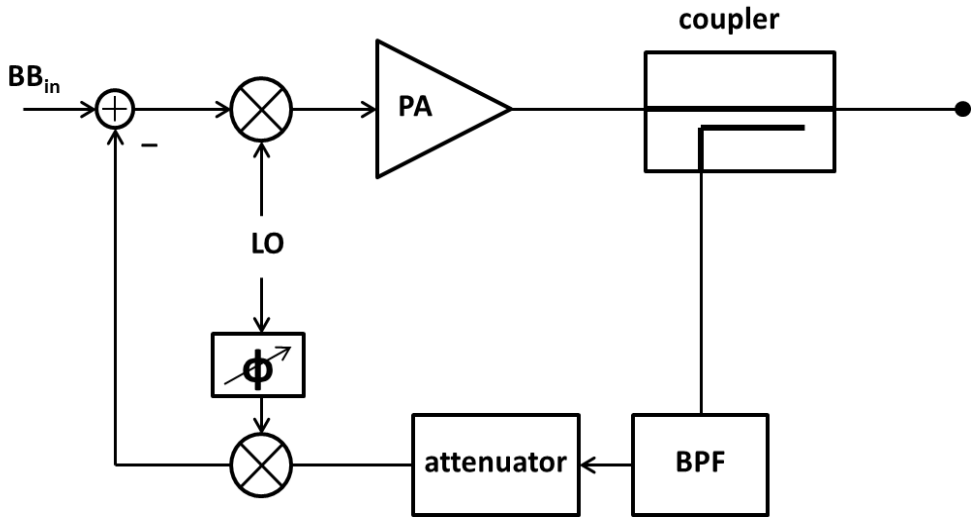


Figure 2.9: Cartesian feedback (only one of the two quadrature paths is shown).

2.3.2 Feedforward

The feedforward technique was introduced in 1928 [31–33]. The feedforward technique has drawn more attention, especially in the wideband and multi-carrier

systems given the limitations of conditional stability and loop bandwidth in the feedback system. Figure 2.10 shows the simplified implementation of a feedforward system. The RF input signal is split into two paths: a main RF path and a signal cancellation path. The distortion generated by the main power amplifier is sampled and fed into a subtractor together with the delayed RF signal. By adjusting the attenuator, the distortion signal of the main amplifier is generated at the output of the subtractor. The residual distortion products are then linearly amplified by an error amplifier, and then combined with the distorted RF signal in the main RF path. Ideally, an amplified RF signal without distortion will be generated at the output of the injector coupler.

There are several practical considerations in the implementation of feedforward systems. The error amplifier must be highly linear, which results in a some depredation of the total efficiency of the feedforward system. Besides, the phase and amplitude imbalances between the main RF path and the signal cancellation path will dramatically degrade the linearization performance. For instance, a 25dB distortion suppression requires either an amplitude error of 0.5dB or less or a phase error of 3.5 degree or less [24]. As a result, extra control must be employed to synchronize both the gain and phase.

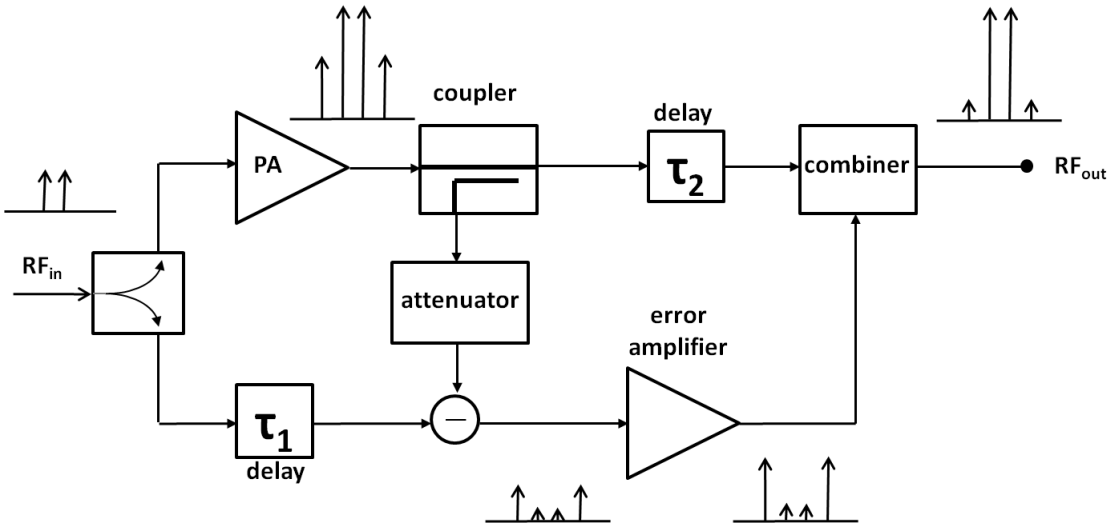


Figure 2.10: Feedforward Power Amplifier.

2.3.3 Pre-distortion

If the PA nonlinearity is known, it is possible to predistort the input signal to the PA in a way that -after passing through the PA- it cancels the PA nonlinearity and the resulting output resembles the ideal waveform. For example, if the PA can be modeled as $y = f(x)$, a predistorter with a characteristic of $y = G.f^{-1}(x)$ can be used to produce a linear cascaded transfer function (Fig. 2.11). Predistortion systems can be categorized into two groups: analog and digital predistortion. Most of the analog schemes try to cancel the third-order nonlinearity.

There are a number of limitations in this predistortion technique. First, it works only for a limited order of nonlinearities. Second, its power gain is negative at all times, which degrades the efficiency of the power amplifier. Third, its effective linearization range is rather limited. Consequently, it is not commonly used in the high-power amplifier linearization.

Predistortion can be implemented in the digital domain to allow for more accurate cancellation. Figure 2.12 shows a simplified implementation of digital predistortion in baseband. PA nonlinearity varies with process, temperature and load impedance and therefore having a periodic calibration using feedback is necessary. As shown in Fig. 2.12, a linearly attenuated version of the PA output is downconverted, digitized and fed back to the digital processor. Using this loop, the system can characterize PA nonlinearity, for example AM-AM and AM-PM distortions, and adjust the predistortion function. There are different digital predistortion algorithms presented which each has its own advantages and disadvantages [29].

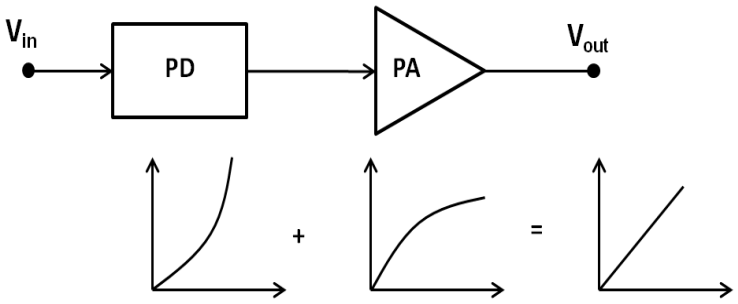


Figure 2.11: Pre-distortion concept.

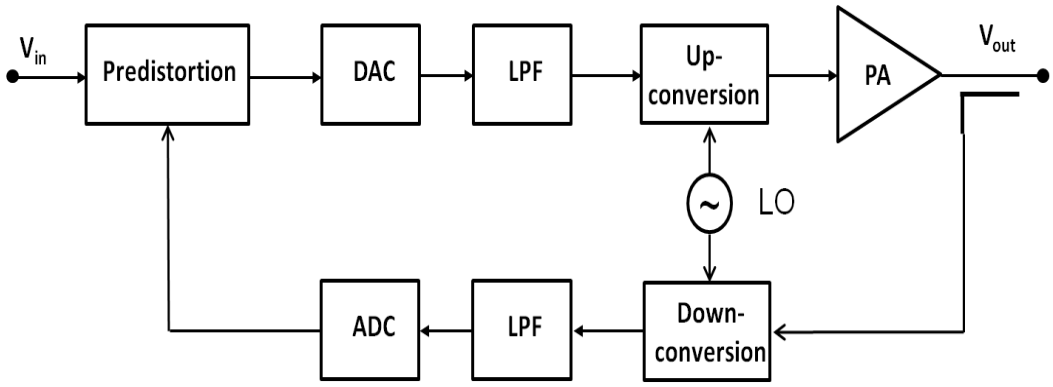


Figure 2.12: Digital baseband pre-distortion.

2.4 Efficiency Enhancement Techniques

PAs are the most power hungry block in wireless transceivers which can directly impact the operation time of the battery in mobile devices. As it is discussed in previous sections, linear PAs are more suitable for more advanced modulation schemes where there is both phase and amplitude information; however these PAs suffer from low efficiency especially at back-off from their peak power. On the other hand, the switching PAs are theoretically more efficient, but they are very nonlinear and can only pass phase information. There have been many of efforts to improve the average efficiency of PAs while meeting the linearity requirements. Here we briefly review the most common techniques.

2.4.1 Dynamic Biasing

As we saw in previous section, the efficiency of a linear amplifier drops as the input signal gets smaller. This reduces the average efficiency of the PA in the presence of a modulated signal with a large PAR. In the dynamic biasing technique, the DC bias voltage (current) of the amplifier varies as a function of the input amplitude. When the amplitude gets smaller, the DC bias voltage drops to lower the DC current of the PA and hence increases the average efficiency. Although the efficiency is improved, the power gain of these amplifiers drops at the same time. Also, varying the bias as a function of signal amplitude can cause extra distortion, which needs to be corrected [34, 35].

2.4.2 Doherty Amplifier

Originally proposed in 1936 [36], the Doherty amplifier consists of a main amplifier and a peak amplifier (Fig. 2.13). By adjusting the phase and amplitude, the output power from both devices can be combined. At low input powers, only the main amplifier is active and at high input powers, where the main amplifier starts to compress, the peak amplifier starts contributing to the output power. This technique extends the linear range by approximately 6dB. The impedance seen by main amplifier can be calculated from [29]

$$Z_{main} = Z_O(\frac{Z_O}{R_L} - \frac{|I_{peak}|}{|I_{main}|}) \tag{2.10}$$

where Z_0 is the characteristic impedance of the transmission line. As can be seen, as the peak amplifier begins to amplify, the load impedance seen by the main PA falls to accommodate more current swing while maintaining maximum voltage swing at the drain. The efficiency of the Doherty amplifier can reach 79% at full power [29]. Figure 2.14 shows the fundamental amplitudes of voltage and current of main and peak amplifiers. The Doherty PA has its own challenges when it comes to full integration. The two transmission lines, especially the one at the output, introduce considerable loss and degrade overall efficiency. Also, the peak amplifier can create distortion due to turning on and off at the presence of large PAR signal.

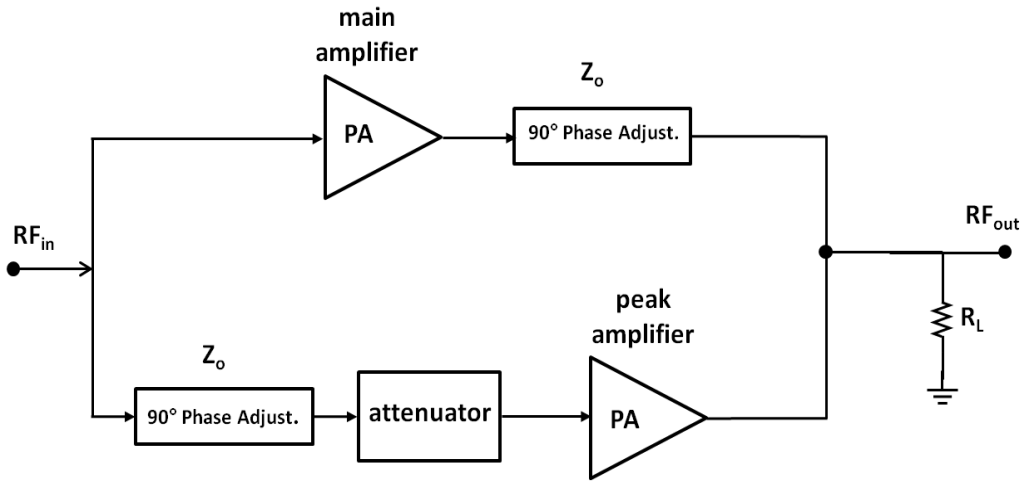


Figure 2.13: Doherty amplifier.

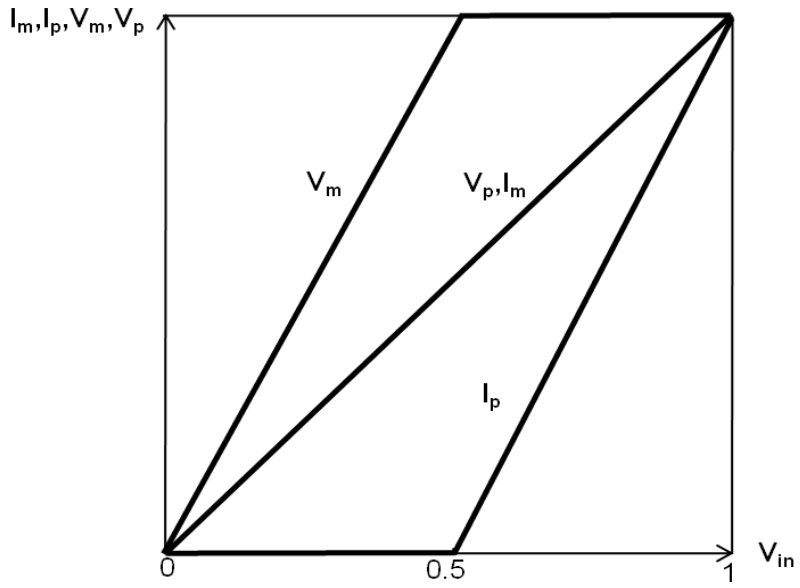


Figure 2.14: Doherty PA: fundamental current and voltage amplitudes.

2.4.3 LINC Amplifier

LINC (Linear Amplification using Nonlinear Components) amplifiers, also known as Outphasing amplifiers, were first proposed in 1935 [37]. The general idea is that a band-pass variable-envelope signal

$$S(t) = A(t)cos(\omega t + \phi(t)) \tag{2.11}$$

can be constructed by adding two constant-envelope phase-modulated waveforms

$$S_1(t) = \cos(\omega t + \phi(t) + \cos^{-1} A(t)) \tag{2.12}$$

and

$$S_1(t) = \cos(\omega t + \phi(t) - \cos^{-1} A(t)) \tag{2.13}$$

To amplify the main signal, these two constant envelope signals can be amplified using high efficient, nonlinear PAs and the resulting output signals are then recombined through a passive combiner into the final output signal. Since each amplifier operates in high efficiency constant amplitude mode, the LINC amplifiers achieve a high overall efficiency.

LINC PAs suffers from several issues. One is the gain and phase imbalances between the two amplifiers. The typical tolerance for most applications is approximately 0.1-0.5dB in gain matching or 0.4-2 degree in phase matching [29]. This is very stringent and impractical to achieve. Although some advanced calibration algorithms [38, 39] have been presented to minimize the gain and phase mismatches, still more work need to be done to use LINC PAs reliably and efficiently in mobile applications.

The second issue is the need for much wider signal bandwidth for each path. Since S_1 and S_2 experience large phase excursion, these two signals have a large bandwidth. The third issue is the loss at the output while combining the two outputs. This has direct impact on overall efficiency. In addition to these issues, cross-talking between the two PAs can result in spectral regrowth. In recent years there have been some researches to overcome these issues [40, 41].

2.4.4 Envelope Elimination and Restoration

First proposed in 1952 by Kahn [42], envelope elimination and restoration (EER) (also known as polar modulation) is a technique to provide a highly efficient and linear power amplifier. As shown in Fig. 2.15, in this technique the limiter before the switching-mode PA eliminates the envelope and creates a constant-envelope signal, which has only the phase information. This signal will be amplified using a high efficiency switching-mode amplifier. The amplitude information will be restored using a linear amplitude modulator on the supply path of the power amplifier.

EER must deal with a number of issues. First, the delay mismatch between envelope and phase paths corrupts the signal. For example, as shown in [43], a delay mismatch of 40ns in an EDGE system, allows only 5dB margin in the spectrum mask. The problem of delay mismatch is a serious one, especially for wide bandwidth signals, because the envelope and phase paths operate at completely different frequencies. The second issue relates to efficiency and linearity of the envelope path. Also, the bandwidth of EER systems is limited by the envelope modulator and is thus more challenging for wideband applications [43].

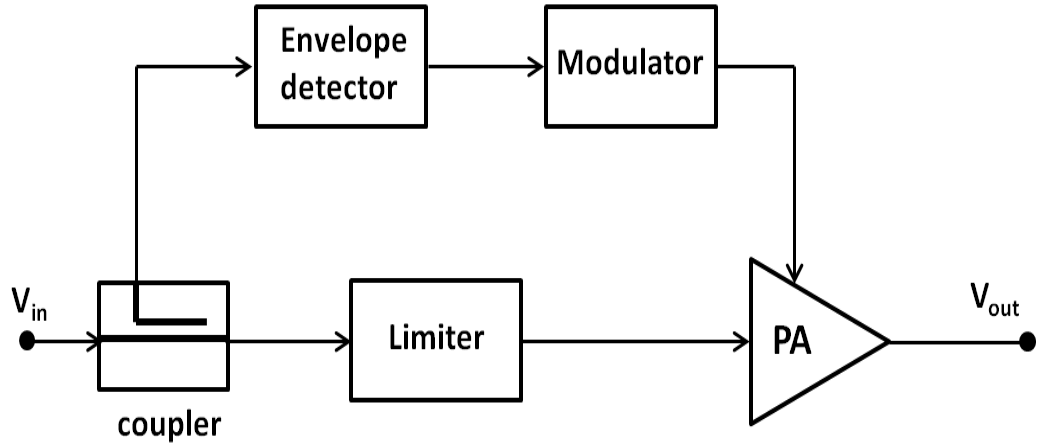


Figure 2.15: Envelope elimination and restoration.

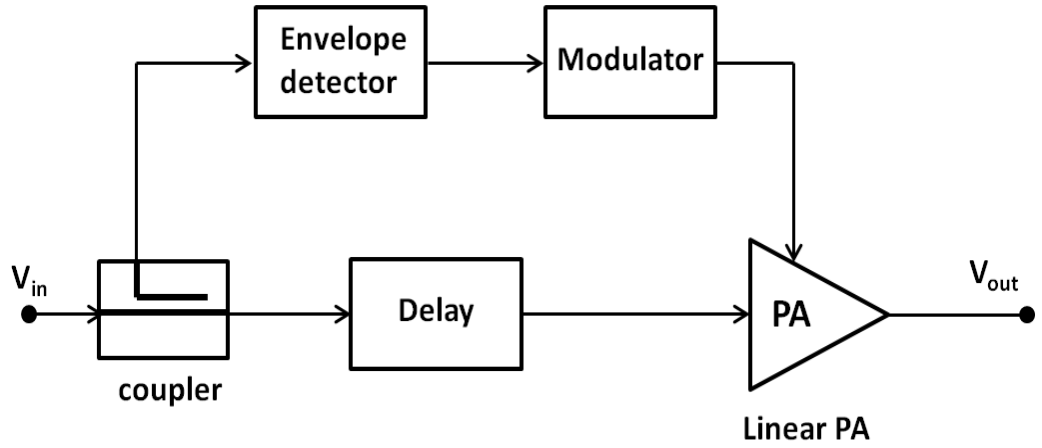


Figure 2.16: Envelope tracking.

2.4.5 Envelope Tracking

Envelope tracking (ET) architecture is similar to the EER except that RF path preserves both amplitude and phase information. Figure 2.16 shows the high level block diagram of ET-PA. In this technique the supply of PA dynamically varies as a function of envelope. Since the dc power consumption is reduced at low powers, the average efficiency is improved. The key challenges in ET architecture are the delay mismatch between signal and envelope paths and the efficiency and bandwidth of the supply modulator especially for wideband signals such as WLAN signal. There has been some progress in recent years to address these issues [44,45].

2.5 Summary

In this chapter we briefly discussed the fundamentals of power amplifiers. Recent wireless standards utilize more advanced modulation schemes with larger PAR to achieve higher data rate and require a very linear PA. A PA is the most power hungry block in transmitter and its efficiency becomes very important in mobile applications. In the traditional PA architectures, linearity and efficiency go in opposite directions. In other words, the more linear PA like class A and class AB the less efficient it is. Several techniques to improve linearity and efficiency have been briefly discussed.

Chapter 3

Matching Network for Power Amplifier Design

Figure 2.2 shows a simplified schematic of a class-AB CMOS power amplifier using a cascode structure. Typically, the thick gate oxide transistor is used as a cascode device to increase the reliability of the PA and to enable the use of a higher supply voltage. A low-loss high impedance transformation ratio matching network is necessary to deliver a large ac power efficiently into a 50Ω load. For example, in Fig. 2.2, to deliver 2W power to a 50Ω antenna from a 3.3V supply requires a transformation of the 50Ω load to approximately 2.2Ω at the drain of the cascode transistor. In this chapter, we will review some common impedance transformation networks suitable for integration in silicon.

3.1 LC Matching Network

Figure 3.1 shows the traditional LC matching network with a simplified narrow-band inductor model where

$$Q_{ind} = \frac{\omega L_P}{R_{LS}} \tag{3.1}$$

The Q_{ind} of the inductor can be modeled by an equivalent parallel resistor R_P through the well-known equivalence

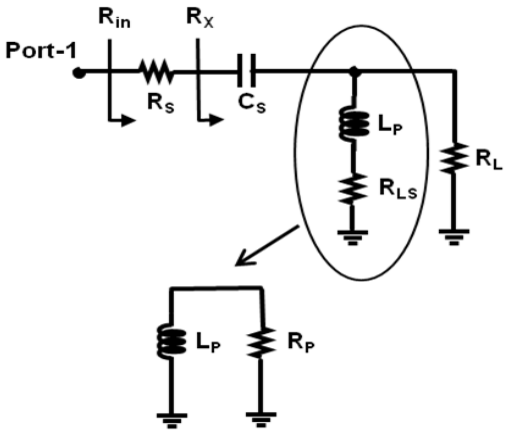


Figure 3.1: Lossy LC matching network.

$$R_P = \frac{(\omega L_P)^2}{R_{LS}} = \omega L_P.Q_{ind} \tag{3.2}$$

Also, any series resistor at port-1, such as layout parasitic resistance, is modeled as R_s. For narrow-band applications, the impedance transformation ratio r at resonance can be calculated from

$$r = \frac{R_L}{R_{in}} = \frac{R_L}{R_s + \frac{R_L||R_P}{1+Q^2_{loaded}}} \tag{3.3}$$

where the loaded quality factor Q_{loaded} is

$$Q_{loaded} = \frac{R_L||R_P}{\omega L_P} \tag{3.4}$$

From 3.2-3.4, ωL_P can be derived in terms of the transformation ratio r, load resistance R_L, inductor quality factor Q_{ind} and layout parasitic R_s, i.e.,

$$\omega L_P = R_L \frac{(2R_L - 2rR_s - rR_L) + \sqrt{(2R_L - 2rR_s - rR_L)^2 - 4(1+Q^2_{ind})(rR_s - R_L)(rR_s + rR_L - R_L)}}{2Q_{ind}(rR_s + rR_L - R_L)} \tag{3.5}$$

Since Q_{ind} itself depends on ω and L_P, 3.2 needs to be solved iteratively to derive a practical inductance value. The power transfer efficiency η of this network is the ratio of the RF power delivered to the load to the RF power delivered to the input of the matching network and can be computed from

$$\eta = \frac{R_L \omega^2 L_P^2 Q_{ind}^2}{(R_s + R_L)\omega^2 L_P^2 Q_{ind}^2 + R_L(2R_s + R_L)\omega L_P Q_{ind} + R_s R_L^2(1 + Q_{ind}^2)} \tag{3.6}$$

Another key parameter is the power enhancement ratio E [46], defined as the ratio of the RF power delivered to the load with the impedance transformation network in place (P_{trans}) to the power delivered to the load without the impedance transformation network (P_{direct}), for a given ac voltage swing at the drain, i.e.

$$E = \frac{P_{trans}}{P_{direct}} = \frac{P_{direct}.r.\eta}{P_{direct}} = r.\eta \tag{3.7}$$

Maximizing this figure of merit achieves the highest possible saturated output power at a given power supply voltage, though not necessarily the highest efficiency. The quantity E depends on both the impedance transformation ratio and the efficiency, and efficiency usually decreases as r increases. For the case where R_s is negligible, η can be calculated for a given E and inductor Q_{ind} [46]

$$\eta = 1 - \frac{\sqrt{E-1}}{Q_{ind}} \tag{3.8}$$

and furthermore the inductance reactance can be computed [46]:

$$\omega L_P = (\frac{1}{\sqrt{E-1}} - \frac{1}{Q_{ind}})R_L \tag{3.9}$$

From 3.9, the upper limit of E can be calculated from

$$E_{max} = 1 + Q_{ind}^2 \tag{3.10}$$

which confirms the difficulty of achieving a high E in silicon technology due to lossy inductors. It should be noted that as we approach this E upper limit, the inductor value and efficiency both approach zero. Figure 3.2 shows the required inductance as a function of E for several values of Q_{ind} and a 50Ω load at 2.45GHz, assuming negligible R_s.

Figure 3.3 plots η for several different values of Q_{ind} at 2.45GHz. These two plots illustrate the tradeoffs between amplifier efficiency and saturated power for a given technology. For example, to deliver 2W of RF power to 50Ω from a

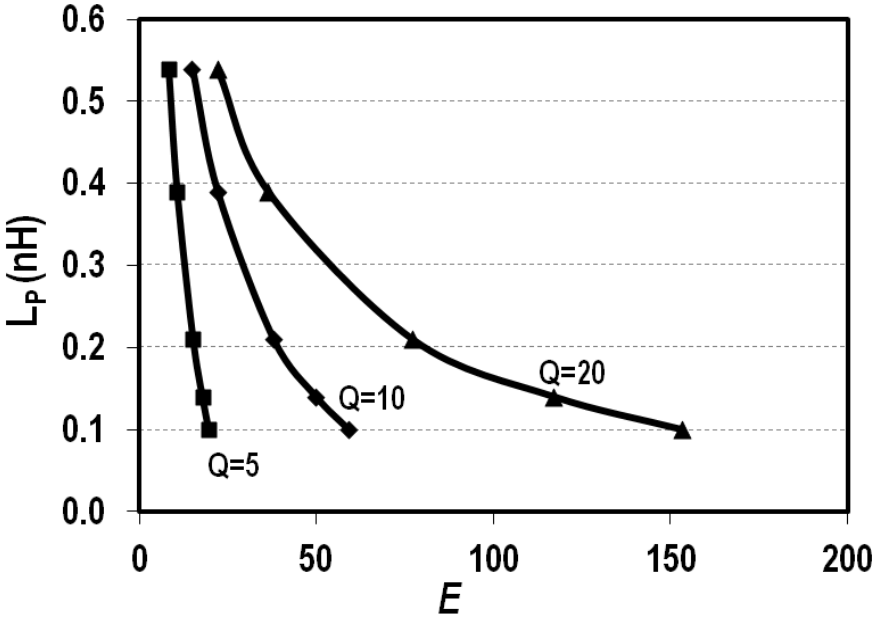


Figure 3.2: Required inductance as a function of E for different Q_{ind} at f_{rf}=2.45GHz and R_s=0.

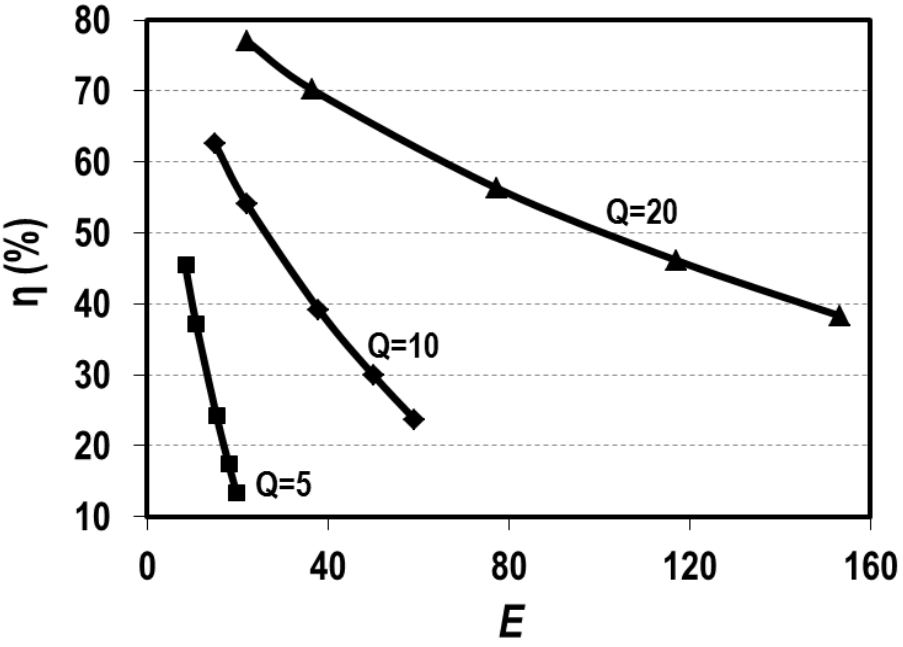


Figure 3.3: Matching network efficiency as a function of E for different Q_{ind} at f_{rf}=2.45GHz and R_s=0.

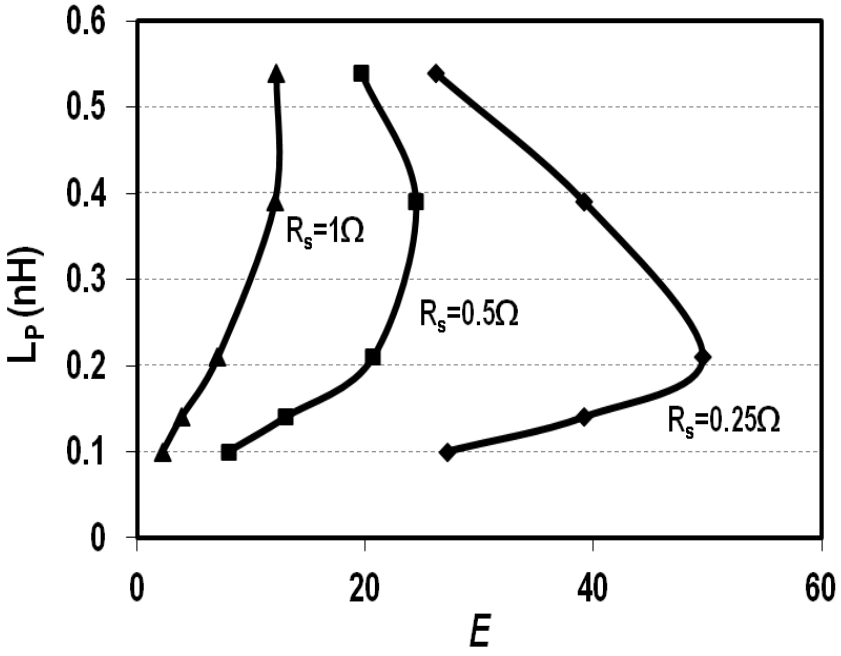


Figure 3.4: Required inductance as a function of E for different R_s and Q_{ind}=∞ at f_{rf}=2.45GHz.

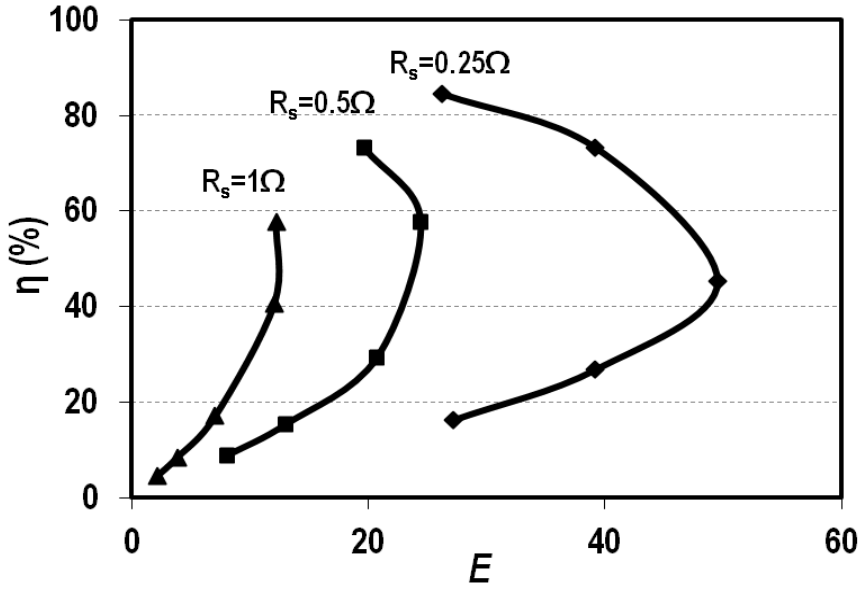


Figure 3.5: Matching network efficiency as a function of E for different R_s and Q_{ind}=∞ at f_{rf}=2.45GHz.

3.3V supply, an E of approximately 23 is required. The resulting inductance value is 370pH and, with a Q_{ind} of ten, the matching network alone will have a power efficiency η of only 53%.

Next, we examine the impact of the series resistance R_s on the performance of the LC matching network. If we assume $R_s \ll R_L$ and the inductor is lossless (Q_{ind}=∞), from 3.2, 3.6 and 3.7 the passive network efficiency η and inductor reactance can be calculated as a function of E, R_s and R_L:

$$\eta \simeq \frac{1+\sqrt{1-\frac{4R_s}{R_L}E}}{2} \qquad \frac{R_L}{2r} \geq R_s \tag{3.11}$$

$$\omega L_P \simeq \sqrt{\frac{R_L^2 - 2R_sR_LE}{E}} \tag{3.12}$$

and the maximum achievable E is

$$E_{max} = \frac{R_L}{4R_s} \tag{3.13}$$

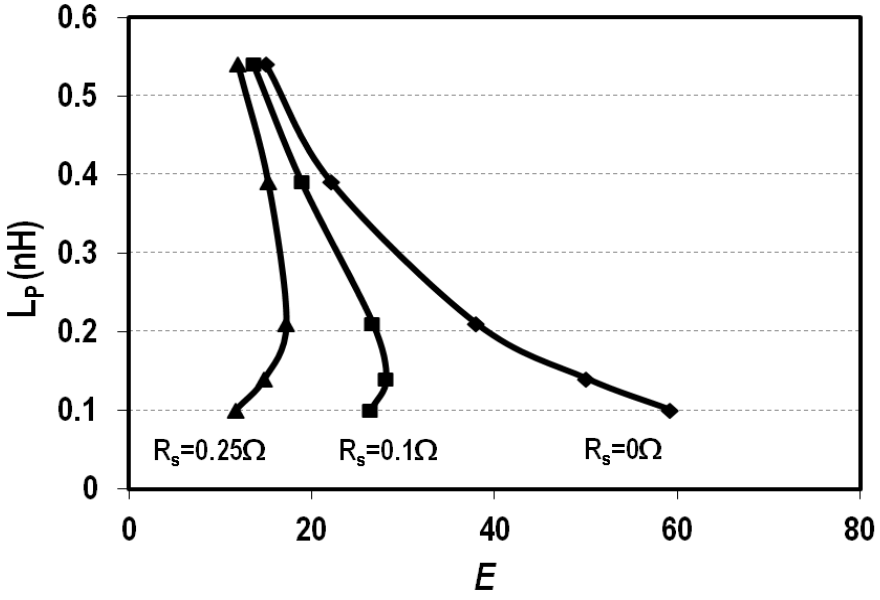


Figure 3.6: Required inductance as a function of E for different R_s and Q_{ind}=10 at f_{rf}=2.45GHz.

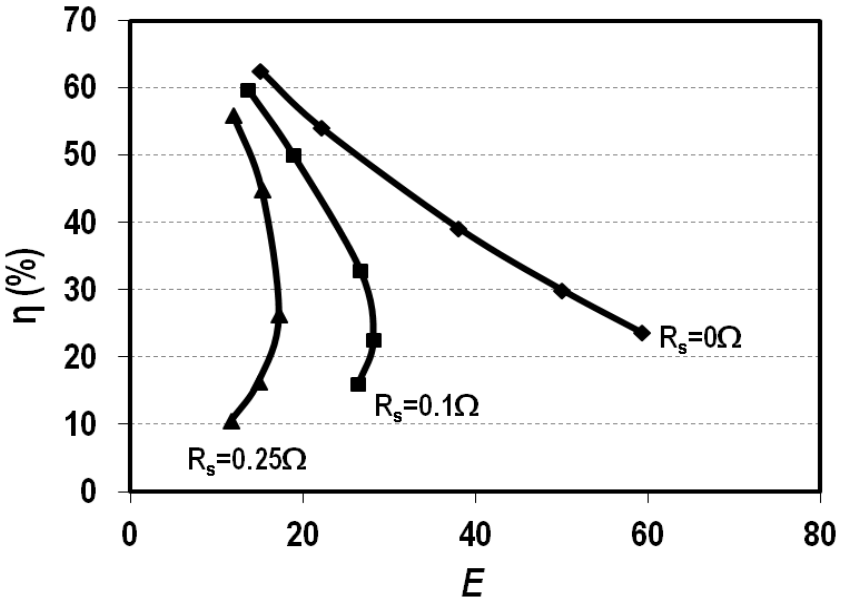


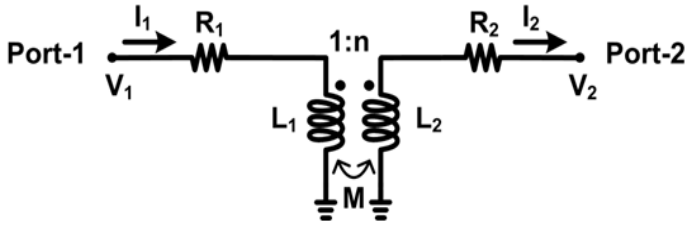
Figure 3.7: Matching network efficiency as a function of E for different R_s and Q_{ind}=10 at f_{rf}=2.45GHz.

For example, 0.5Ω layout parasitic resistance at port-1 can limit the maximum E to 25; if we include the loss of the inductor due to finite quality factor then the maximum achievable E will be even lower. Figures 3.4 and 3.5 show the required inductor and efficiency η as a function of E for different values of R_s respectively. Figures 3.6 and 3.7 show the same parameters as Fig. 3.4 and 3.5 for Q_{ind}=10. It can be seen that for an E of approximately 23 with a 100mΩ parasitic resistance at port-1 and an inductor Q_{ind} of ten, an inductance value of 290pH is required and the matching network will have a maximum power efficiency of only 42%. For R_s>160mΩ and Q_{ind}=10, an E of 23 is not even achievable.

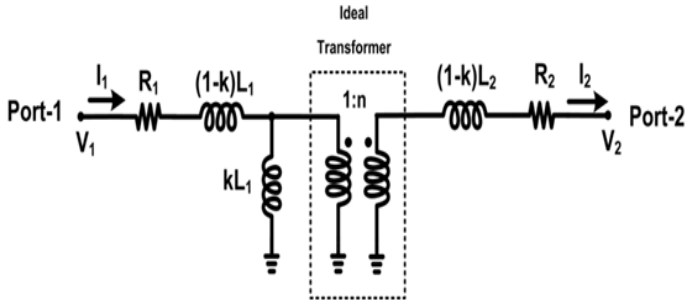
3.2 Transformer-Based Matching Network

Another very common impedance transformation technique is the use of magnetically coupled transformers (Fig. 3.8 (a)). Figure 3.8 (b) shows the simplified model of the transformer of Fig. 3.8 (a), where series resistors R_1 and R_2 model the finite quality factors of the primary and secondary inductances respectively [47]. In order to optimize the performance, some of the transformer's residual

inductance is resonated and a series capacitor can be added at the secondary port. A shunt capacitor may also be necessary on the primary side of the transformer to adjust the input reactance to be tuned at the desired frequency as shown in 3.9. In LC matching, the network presents a real impedance at the desired frequency and an inductor connecting the drain of the device to the dc supply is used to tune the device parasitic capacitor at the desired frequency. The circuit of 3.9 can be used to derive the efficiency η and optimum values of C_L, L_1 and L_2 for maximum efficiency [46]. The η is



(a)



(b)

Figure 3.8: (a) Transformer model, (b) Transformer T-model.

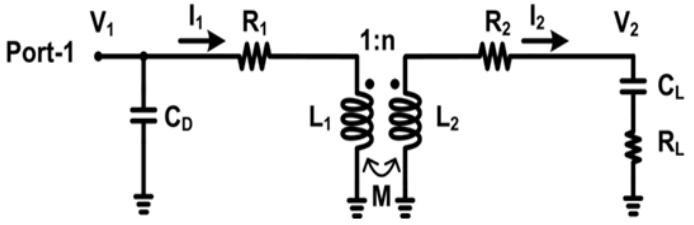


Figure 3.9: Transformer model with tuning.

$$\eta = \frac{R_L/n^2}{(\frac{\omega L_1/Q_2+R_L/n^2}{\omega k L_1})^2.\frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} + R_L/n^2} \tag{3.14}$$

assuming $L_1 \approx L_2/n^2$ and $1/\omega C_L$=ωL_2. The quantities Q_1 and Q_2 are the quality factors of the primary and secondary inductors respectively and n is the transformer turn ratio. Now we can find the optimum value of L_1 by differentiating 3.14 with respect to L_1

$$\omega L_{1-opt} = \frac{R_L}{n^2\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2}.k^2}} \tag{3.15}$$

and

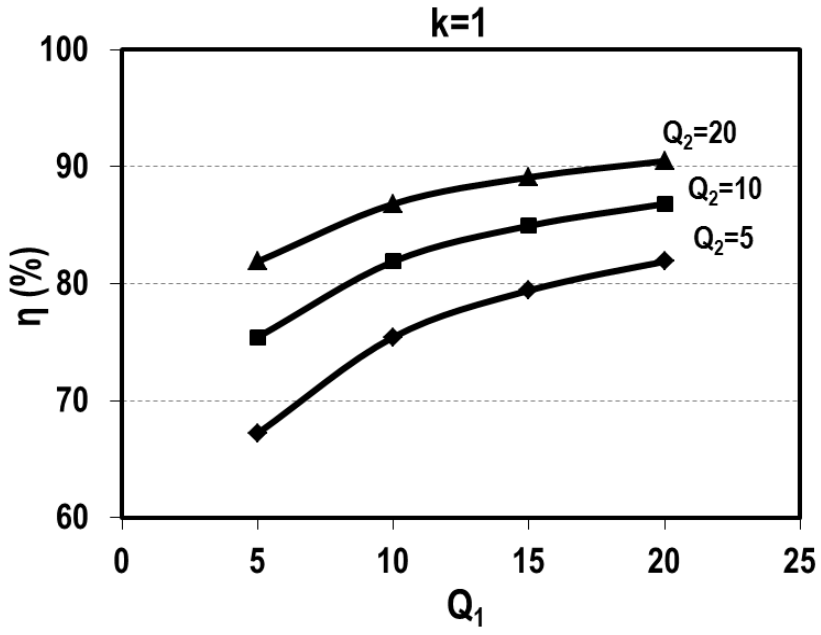
$$\eta_{max} = \frac{1}{1 + \frac{2}{Q_1 Q_2 k^2} + 2\sqrt{\frac{1}{Q_1 Q_2 k^2}(1 + \frac{1}{Q_1 Q_2 k^2})}} \tag{3.16}$$

The turn ratio n for a given E can be calculated from [46]

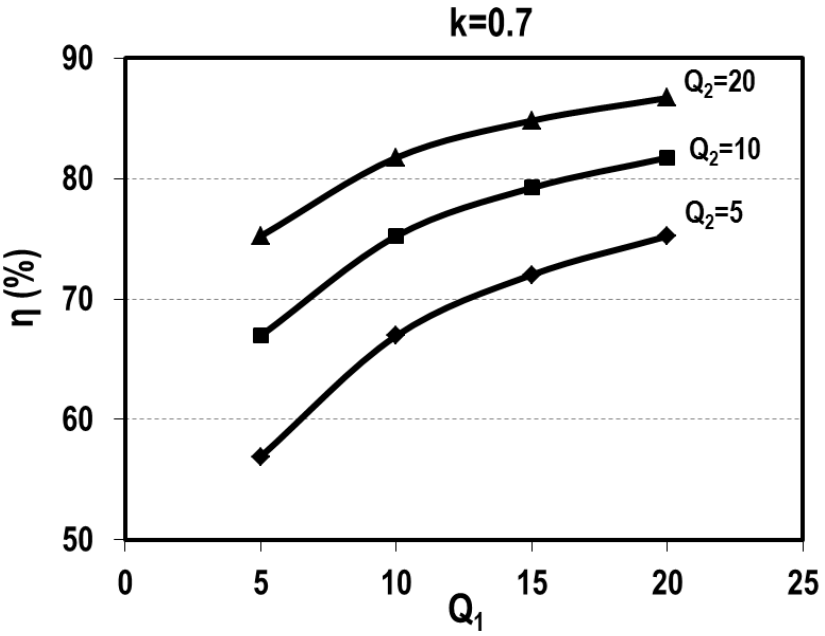
$$n \approx \sqrt{\frac{E(\frac{Q_1}{k^2} + Q_2)}{\eta Q_1}} \tag{3.17}$$

Figure 3.10 plots the calculated efficiency η as a function of the quality factor of the primary and secondary inductors. For example, using 3.15-3.17 it can be calculated that for an E of 23 with primary and secondary inductor quality factor of ten and k of 0.7, the transformer primary should have an inductance of 50pH to achieve the highest efficiency at 2.45GHz. In this case, n should be approximately ten and the maximum efficiency is 75%. These numbers confirm that achieving such a large E would be very challenging using a single transformer, since it would require a very small primary inductance and large turn ratio.

Using the previous analysis, we can compare the performance of an LC matching network and a transformer. In a transformer, efficiency is not a function of E unlike an LC matching network and hence does not drop for larger output power, as can be observed from 3.8 and 3.16. Of course this is valid for a range of E which results in practical inductance value and quality factor. It can be shown that for an E above 15, the transformer provides a higher efficiency than LC network



(a)



(b)

Figure 3.10: Transformer efficiency versus inductor Q, (a) k=1 case (b) k=0.7 case.

for a given inductance quality factor [46]. The disadvantage of a transformer-based matching network is that it requires a low primary inductance to achieve the highest efficiency. For instance, for an E of 23 at 2.45GHz, the necessary primary inductance for maximum efficiency is only 50pH with a transformer, but an inductance of 370pH is required in an LC matching network assuming the same quality factor of ten. Figures 3.11 and 3.12 show the primary inductance value and turn ratio of transformer as a function of E respectively.

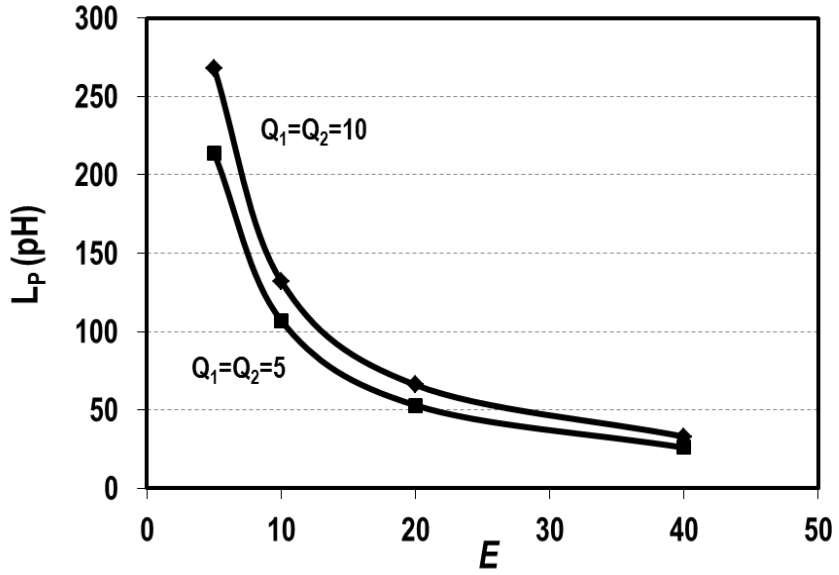


Figure 3.11: Transformer primary inductance as a function of E.

As a summary, for large E, the inductance values will be impractically small, the loss of network will be high and the loss of the network will be very sensitive to parasitic resistance on the low impedance side. In addition to these issues, there is one more practical issue on designing a PA with a large E, which is the design of the driver stage. In Fig. 2.2, where the saturated power is limited by supply voltage, we can assume that approximately

$$P_{sat} \propto i_{out} \propto g_m \propto W \tag{3.18}$$

where gm and W are the transconductance and width of the PA input device, respectively. Therefore

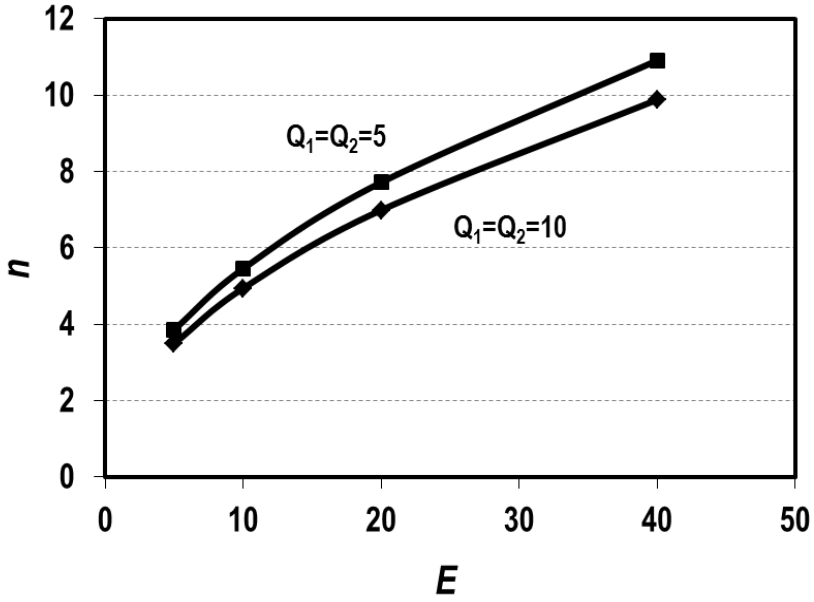


Figure 3.12: Transformer turn ratio as a function of E.

$$C_{gs} \propto W \propto P_{sat} \tag{3.19}$$

where C_{gs} is the gate capacitance of the input device, which is driven by the driver amplifier stage . In order to maximize the gain and efficiency of the driver, an inductor is used to tune out the C_{gs} at the frequency of operation. As a result

$$L_{driver}C_{gs}\omega_o^2 = 1 \Rightarrow L_{driver} \propto \frac{1}{C_{gs}} \propto \frac{1}{P_{sat}} \tag{3.20}$$

$$\begin{aligned} Driver\ gain \propto g_{m-driver}R_{L-driver} &= g_{m-driver}\omega_o L_{driver}Q_{driver} \\ \Rightarrow Driver\ gain \propto \frac{Q_{driver}}{C_{gs}} &\propto \frac{Q_{driver}}{P_{gs}} \end{aligned} \tag{3.21}$$

Equations 3.20 shows that for larger E (higher Psat) we need a smaller load inductor for the driver, which causes lower driver gain (3.21) and at some point make the driver inefficient and impractical to design. One well-known solution to achieve large E efficiently is to combine the output power of multiple smaller PAs, where each PA is presented with higher impedance, which can then have a

more efficient, higher gain driver. In this approach, a low-loss power combining network is needed. In Chapter 5, we will describe and analyze four different power combiner architectures suitable for an integrated PA in CMOS.

3.3 Summary

In this chapter two of the commonly used matching networks, *LC* and transformer based matching networks, were analyzed. The key parameters of the matching network such as component values and efficiency as a function of power enhancement ratio as well as inductor quality factor were derived. In both cases, designing a matching network for large power enhancement ratio results in a large power loss in the network and impractical component values. Chapter 3 is in full a reprint of the material as it appears in the IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 3, pp. 1247-1260, March 2013. The dissertation author is the primary investigator and author of this paper. Professor Lawrence Larson supervised the research which forms the basis for this paper.

Chapter 4

A Linearized Dual-Band CMOS Power Amplifier for a 2x2 802.11n MIMO WLAN SoC

This chapter introduces a fully integrated 2x2 dual-band CMOS PAs with on-chip baluns in a 65nm digital CMOS process integrated in a MIMO SoC solution, utilizing various linearization schemes to achieve the requirements of 802.11n, while transmitting at high power levels and achieving high power added efficiencies.

4.1 Architecture and Circuit Implementation

A block diagram of each of the transmitter slices is shown in Fig. 4.1. All the signals are implemented differentially except the PA output, which is single-ended. The quadrature signals from the DACs are applied to the programmable bandwidth and gain low-pass filters (LPF). The output of the LPFs are then up-converted by quadrature, Gilbert style mixers to the desired RF band. The up-conversion mixers are designed for high linearity and low LO feed-through over a wide gain control range [48]. In order to provide enough RF gain to amplify the signal at the mixer output to the level which is required by the system at the antenna, a three-stage power amplifier is used. In the first two stages, the RF variable gain amplifier (RFVGA) and PA Driver provide voltage gain while the

final stage (PA) delivers the desired output power to the 50 Ω antenna.

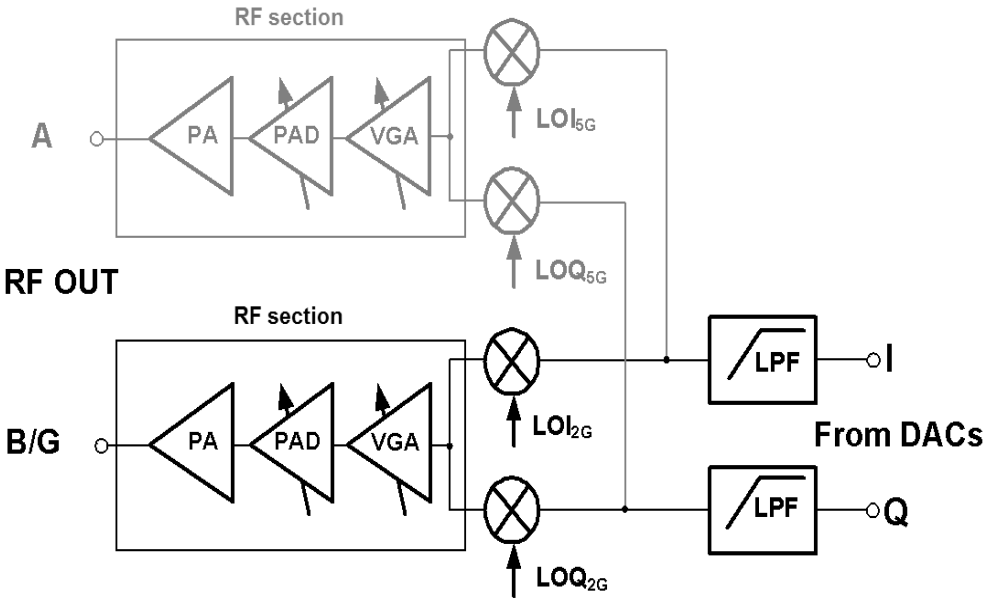


Figure 4.1: Block diagram of each transmit slice.

A pseudo differential cascode amplifier is used for the RFVGA and PA Driver (Fig. 4.2). The loads of the RFVGA and PA Driver are differential inductors, which tune out the total capacitance at the output. Thin gate (core) transistor devices are used due to their higher transconductance. The RFVGA and PA Driver use 1.2v and 3.3v supplies respectively. The cascode devices in the RFVGA are thin gate devices and the ones in the PA Driver are thick gate devices to improve the reliability. Transistors M1-M4 are also made of multiple parallel branches, which can be independently turned on or off by system control to provide enough gain control range and also reduce power consumption for lower RF output powers. In this design since the total parasitic capacitance at the load is dominated by the input capacitance of the following stage, turning on or off some branches has minimum impact on the tuning. In addition, any change in nonlinearity characterization of the transmit chain due to turning on or off the branches can be addressed by the linearization techniques discussed in next section. To cover the entire frequency band, a bank of differential switched-capacitors is used to resonate the RFVGA and PA Driver load at each frequency.

Based on the system requirement, the RF section has to provide at least

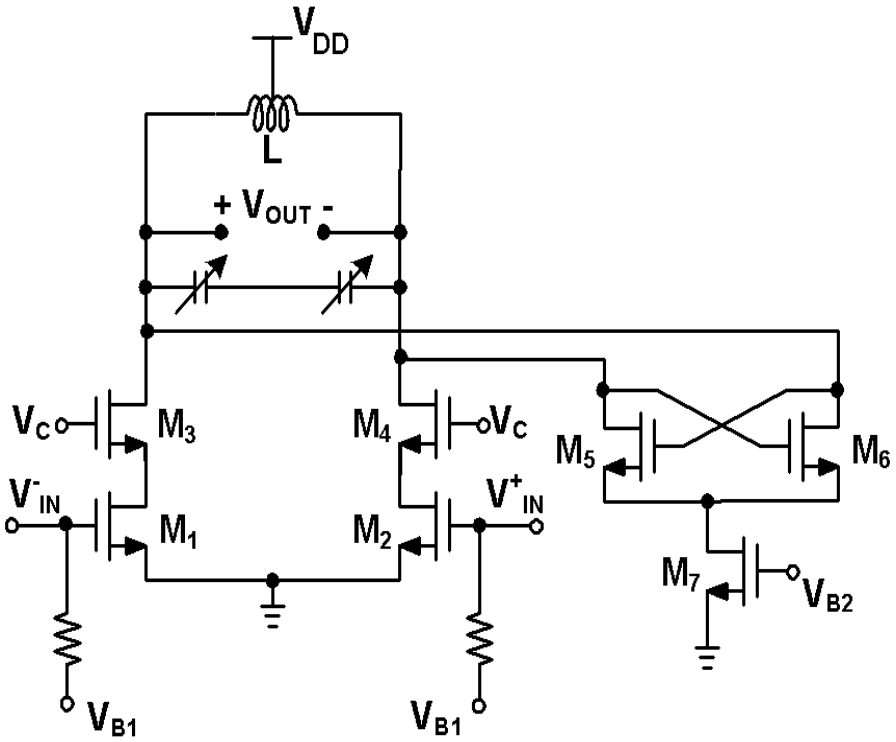


Figure 4.2: Simplified RFVGA and PA Driver schematics.

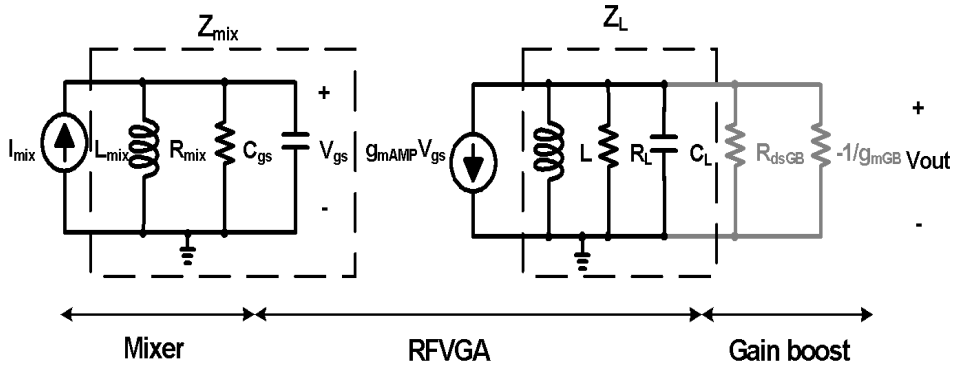


Figure 4.3: Small signal model of the mixer and RFVGA.

30dB gain. Due to low Q inductors and layout parasitics, achieving this gain from three stages at 5GHz is very challenging. Therefore, gain-boost circuitry is utilized at the output of the Mixer, RFVGA and PA Driver to increase the gain of each stage as necessary [49]. The gain boost consists of shunt cross-coupled devices at the output, which boost the effective Q of the tank by providing single-ended negative resistance $(-1/g_{mGB})||R_{dsGB}$ at the resonant frequency, where g_{mGB} and

R_{dsGB} are the transconductance and output resistance of the cross-coupled devices, respectively. Figure 4.3 shows the small-signal model of the RFVGA and the mixer. Capacitor C_L is the total capacitor at the RFVGA output, which includes the input capacitor of the next stage (PA Driver) and the gain boost circuit. The transfer function of transimpedance ($V_{out}(s)/I_{mix}(s)$)) is

$$R_o(s) = \frac{V_{out}(s))}{Imix(s)} \cong Z_{mix}(s) g_{mAMP} Z_L(s) \tag{4.1}$$

where g_{mAMP} is the transconductance of the RFVGA input device in saturation region and $Z_{mix}(s)$ and $Z_L(s)$ are the impedance of the parallel RLC tank at the mixer and RFVGA outputs, respectively and have the form of

$$Z_{mix}(s) = \frac{sR_{mix}\frac{\omega_0}{Q_{mix}}}{s^2 + s\frac{\omega_0}{Q_{mix}} + \omega_0^2} \tag{4.2}$$

$$Z_L(s) = \frac{sR_L\frac{\omega_0}{Q_L}}{s^2 + s\frac{\omega_0}{Q_L} + \omega_0^2} \tag{4.3}$$

where ω_0 is the resonant frequency and $Q = R/\omega_0 L$ is the quality factor of the tank. At resonance, R_o reduces to

$$R_o(\omega_0) = R_{MIX} g_{mAMP} R_L \tag{4.4}$$

By turning on the gain boost circuitry ($M_5 - M_6$ in Fig. 4.2), and assuming that the total capacitance at the output is dominated by the input capacitance of the next stage (PA Driver), the new real part of the RFVGA tank impedance would be

$$R_{Lnew} = R_L || R_{dsGB} || \frac{-1}{g_{mGB}} = \frac{R_L R_{dsGB}}{R_L + R_{dsGB} - g_{mGB} R_L R_{dsGB}} \tag{4.5}$$

and the new Q_L can be calculated from

$$Q_{Lnew} = \frac{R_{Lnew}}{R_L} Q_L \tag{4.6}$$

In order to calculate g_m, the drain current (i_D) of MOS transistor in saturation region without channel-length modulation can be estimated as [50]

$$i_D = \frac{\mu_0}{1 + \theta(v_{GS} - V_T)} C_{ox}{}' \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS}) \tag{4.7}$$

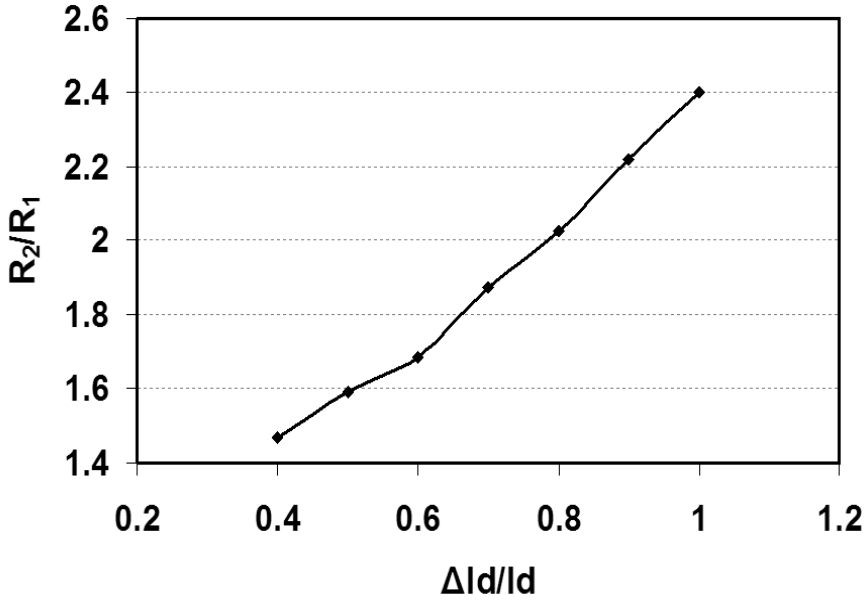


Figure 4.4: Simulated small signal gain benefit from gain boost circuit.

By using Taylor series around bias point (V_{GS})

$$i_D = I_D + a_1 v_{gs} + a_2 v_{gs}^2 + \cdots \tag{4.8}$$

where the gate voltage is the sum of the incremental and DC voltages, i.e. $v_{GS} = V_{GS} + v_{gs}$

$$I_D = \frac{\mu_0}{1 + \theta V_{eff}} C_{ox}{}' \frac{W}{L} V_{eff}^2 (1 + \lambda V_{DS}) \tag{4.9}$$

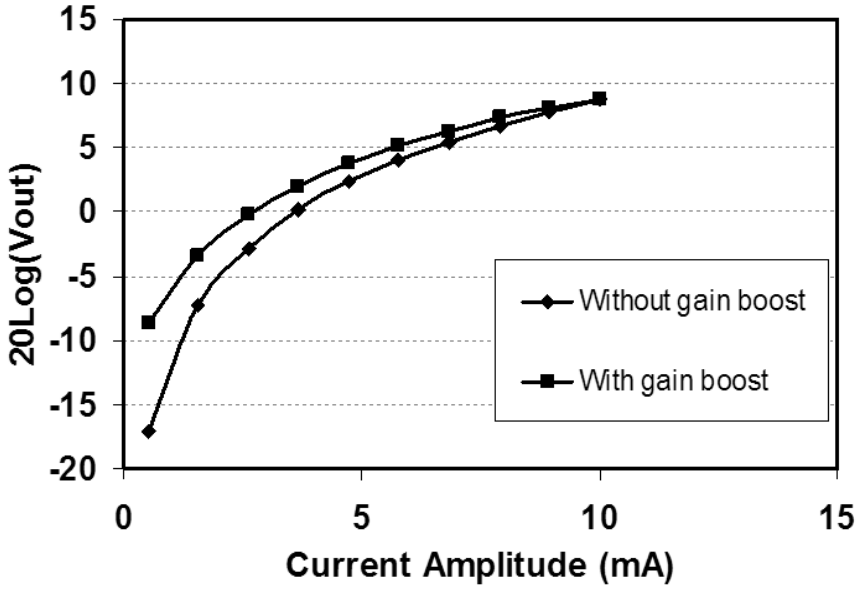
and

$$a_1 = \frac{\mu C_{ox}{}' W}{L} \frac{2V_{eff} + \theta V_{eff}^2}{(1 + \theta V_{eff})^2} (1 + \lambda V_{DS}) \tag{4.10}$$

$$a_2 = \frac{\mu C_{ox}{}' W}{L} \frac{1}{(1 + \theta V_{eff})^3} (1 + \lambda V_{DS}) \tag{4.11}$$

where $V_{eff} = V_{GS} - V_T$. Therefore, at the bias point

$$g_m = a_1 = \frac{\mu C_{ox}{}' W}{L} \frac{2V_{eff} + \theta V_{eff}^2}{(1 + \theta V_{eff})^2} (1 + \lambda V_{DS}) \tag{4.12}$$



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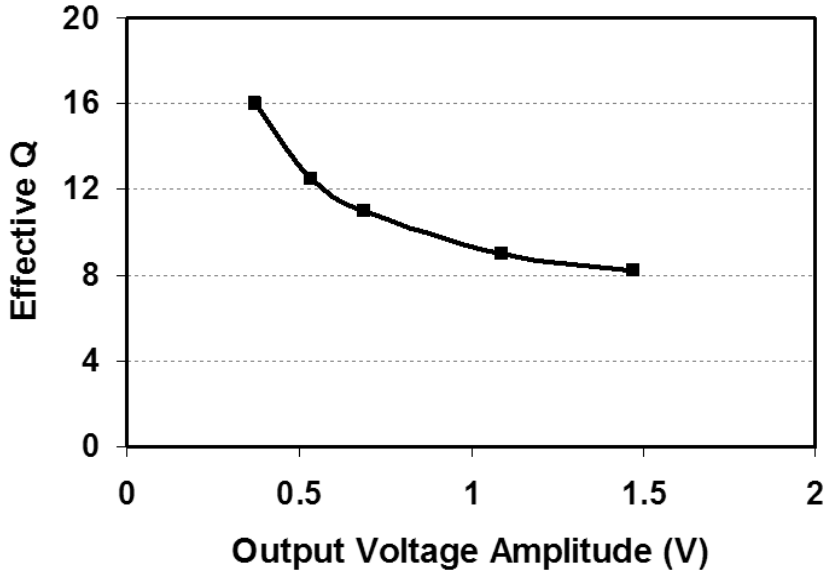


(b)

Figure 4.5: (a) Simulated output voltage with and without gain boost. (b) Simulated overall effective Q as function of output voltage amplitude.

To find g_m as a function of bias current I_D, V_{eff} can be written as a function of I_D using

$$V_{eff} = \frac{\theta I_D + \sqrt{\theta^2 I_D^2 + 4\frac{\mu_0 C_{ox}{}' W}{L}(1+\lambda V_{DS})I_D}}{2\frac{\mu_0 C_{ox}{}' W}{L}(1+\lambda V_{DS})} \tag{4.13}$$

The gain boost increases the overall transimpedance of the amplifier by increasing the output impedance, at the expense of higher current consumption. To show that the gain boost circuit could improve power efficiency, let us consider additional bias current Δi_D in the main amplifier. The transimpedance would then be $R_1(\omega_0) = R_{mix} g_{mAMP}[i_D + \Delta i_D] R_L$. On the other hand, if this additional current is used in the gain boost circuit, the new transimpedance would be

$$R_2(\omega_0) = R_{mix} g_{mAMP}[i_D] \frac{R_L R_{dsGB}}{R_L + R_{dsGB} - g_{mGB}[\Delta i_D](R_L R_{dsGB})} \tag{4.14}$$

and therefore, the gain improvement in using the negative transconductance cell is

$$\frac{R_2}{R_1}(\omega_0) = \frac{g_{mAMP}[i_D]}{g_{mAMP[i_D+\Delta i_D]}} \frac{R_{dsGB}}{R_L + R_{dsGB} - g_{mGB}[\Delta i_D](R_L R_{dsGB})} \tag{4.15}$$

Figure 4.4 shows the benefit from the gain boost circuit, compared to increasing the current in the main amplifier. In practice, $M_5 - M_7$ consists of multiple branches and can be turned on and off as necessary to boost the gain under process-voltage-temperature (PVT) conditions.

Figure 4.5(a) plots the output voltage with gain boost enabled and disabled as a function of current amplitude injecting to the output by $M_1 - M_2$. The overall effective Q_L is plotted in Fig. 4.5(b). At a low output amplitude, the gain boost increases the gain by approximately 8dB, but this boost drops as the signal swing increases. The reason is that the boost is limited by the tail current source. When the output voltage increases, the large-signal transconductance decreases.

Figure 4.6 shows the simulated nonlinearity of the gain boost circuit under large signal conditions as a function of the output swing. In Fig. 4.7 the simulated amplitude and phase distortion of the entire RF section of the 5GHz transmitter at 5.5GHz, with and without gain boost, is plotted. As one can see from (4.8), the

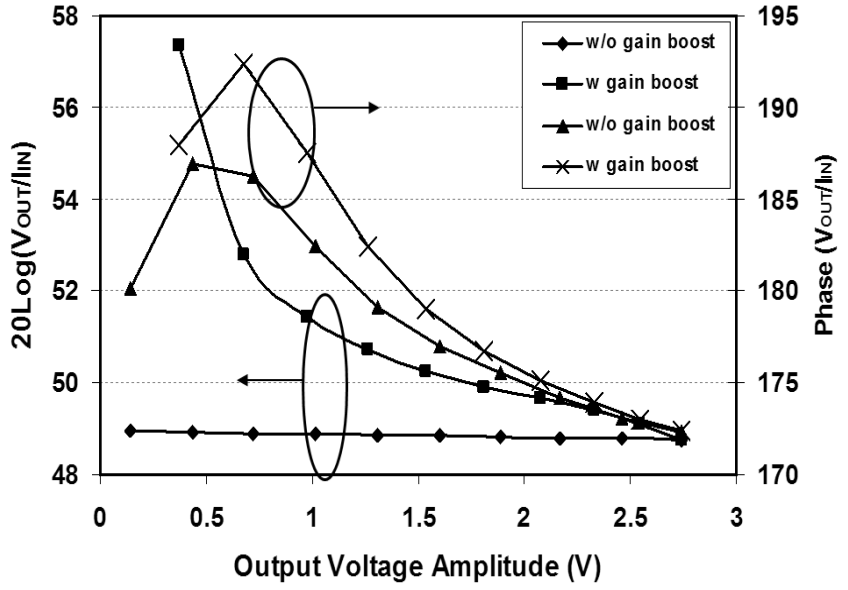


Figure 4.6: Simulated magnitude and phase of the transimpedance (V_{out}/I_{in}) as a function of output voltage amplitude.

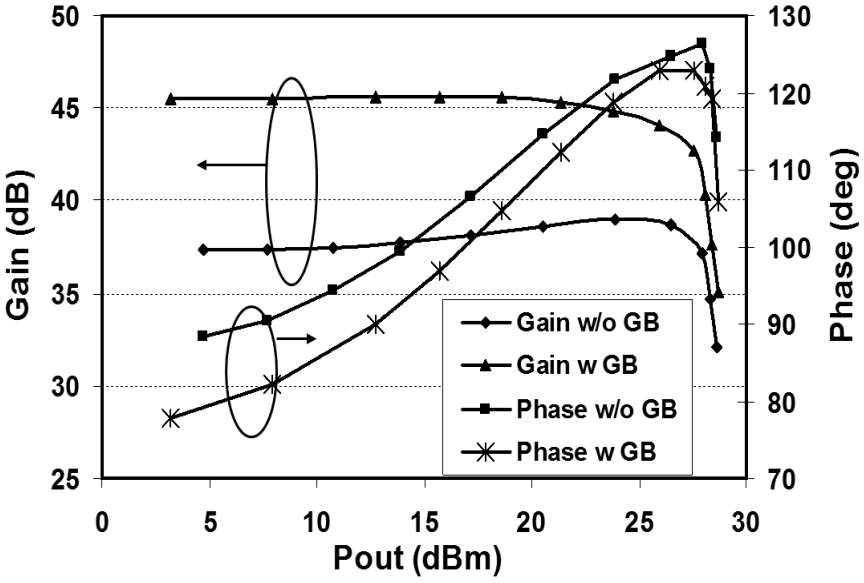


Figure 4.7: Simulated AM-AM and AM-PM of 5GHz TX at 5.5GHz with and without gain boost.

overall gain is a nonlinear function of g_{mGB}, and g_{mGB} itself is very nonlinear in short-channel transistors; and as a result, the gain boost block can be quite nonlinear. The additional nonlinearity is addressed, along with the overall linearization technique, in the next Section.

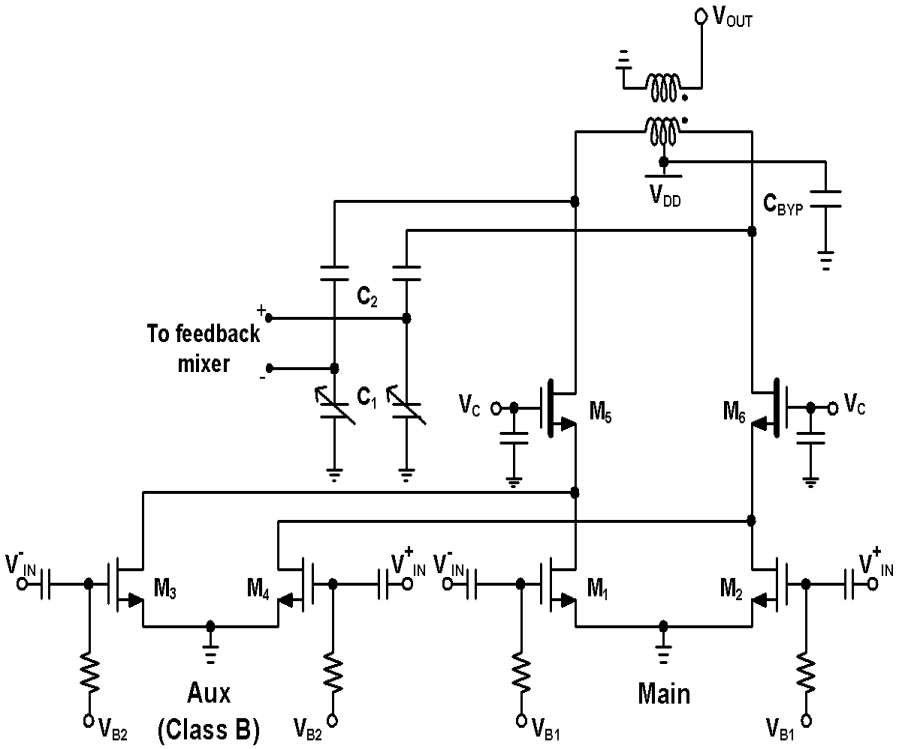


Figure 4.8: Power amplifier (PA) schematic.

Figure 4.8 shows the simplified schematic of the PA. It has the same cascode structure as the PA Driver but with a transformer as the load. The transformer converts the 50 Ω load to the desired impedance at the PA output while the primary inductance of the transformer (PA side) is designed to tune out the total parasitic capacitor at the PA output. It is implemented in top metal to reduce the resistive loss and improve the current handling. Simulations show 1dB and 1.3dB loss, respectively for the 2.4GHz and 5GHz transformers. The layout of the 2.4GHz balun is shown in Fig. 4.9. To enhance the reliability of the PA, the thick-oxide devices are used as the cascode. The cascode gate bias is set to ensure that the V_{ds} of the transconductance device is in the proper and reliable range. To reduce the even harmonic distortion and also the chance of common-mode oscillation, the

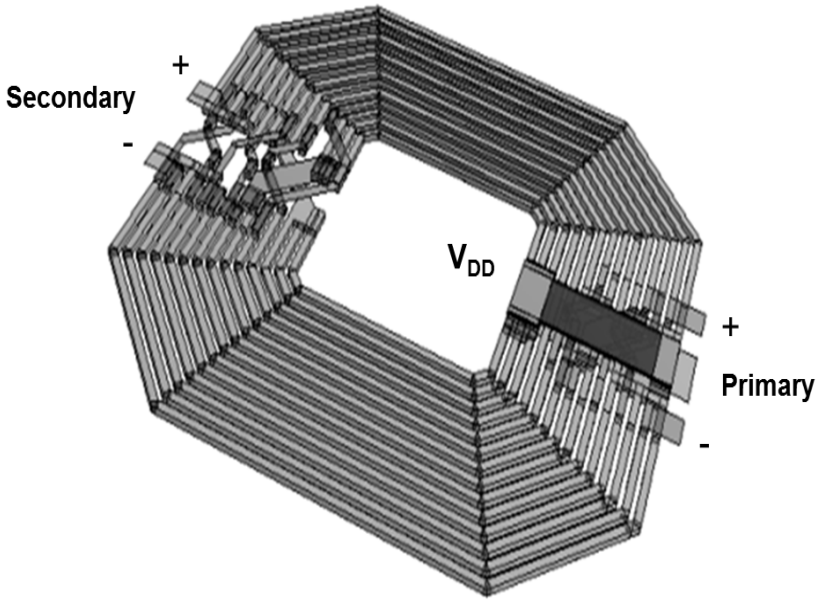


Figure 4.9: 2.4GHz balun layout with 1.6:1 turn ratio

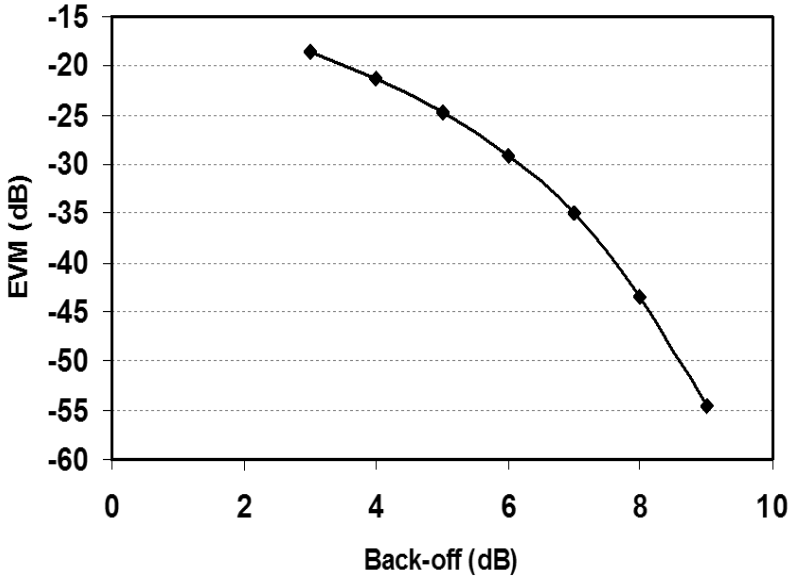


Figure 4.10: Simulated EVM vs. back-off from Psat for an ideal PA with hard clip AM-AM and no AM-PM.

center tap of the transformer is bypassed to the PA ground. Load-pull simulations are used to determine the optimum size for the PA devices and also the optimum

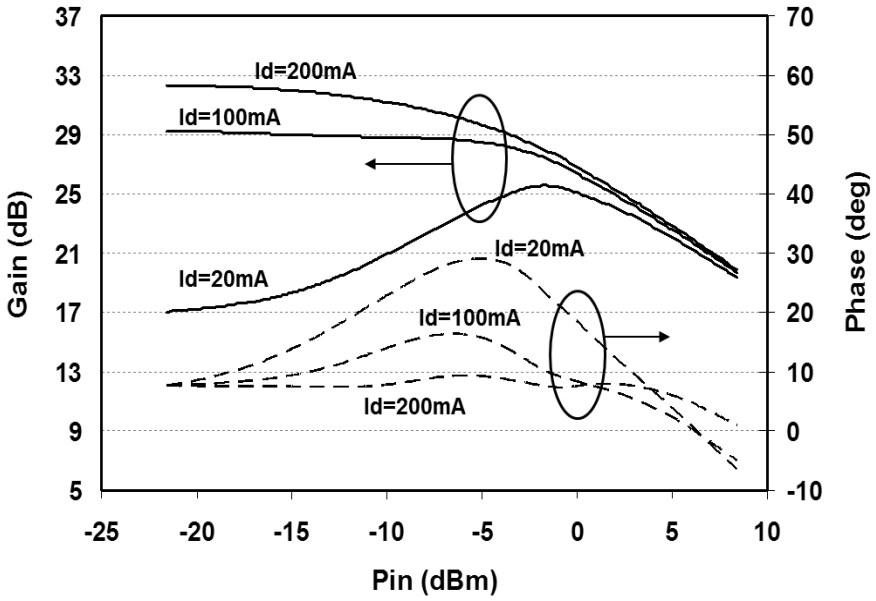
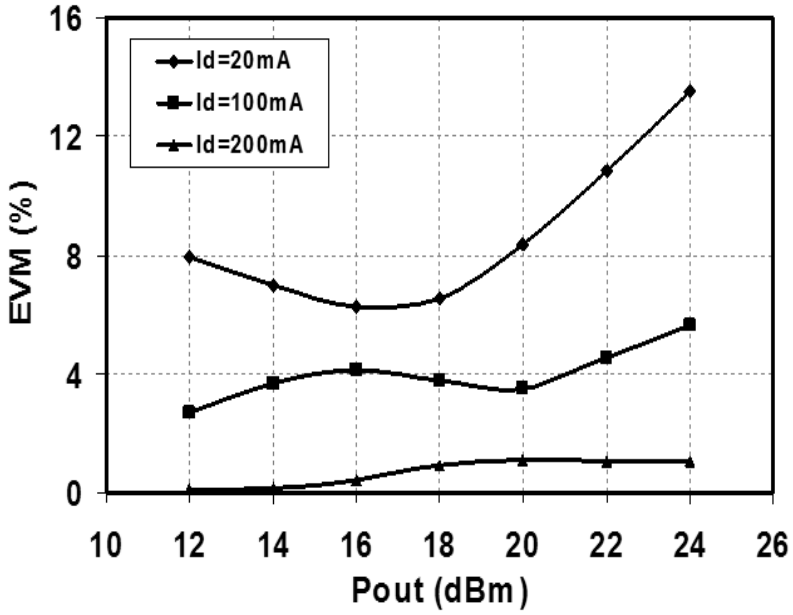


Figure 4.11: Measured AM-AM and AM-PM of 2.4GHz PA and PA Driver for different bias currents of the PA.

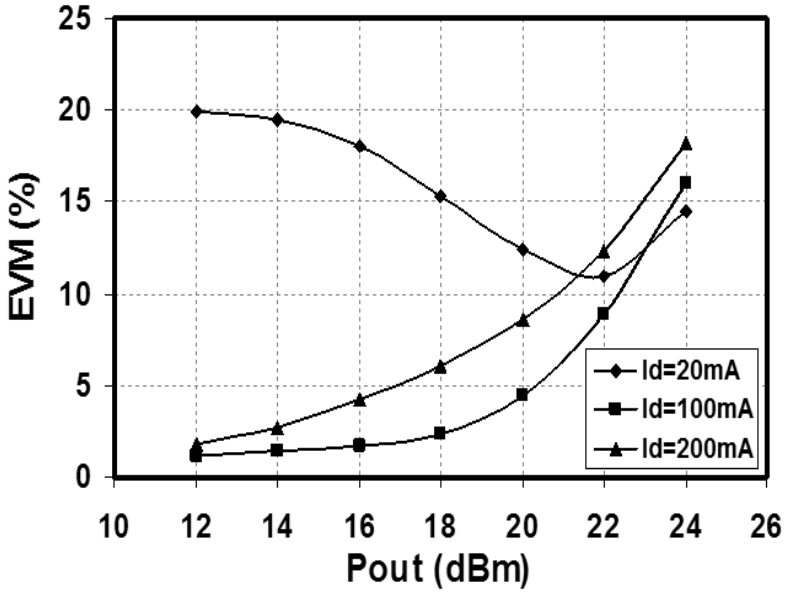
impedance to be presented by the transformer at the cascode drains. To reduce the substrate coupling between PA and PA Driver and the rest of the chip, Deep-N well isolations are used to enclose the PA and PA Driver.

4.2 Linearization Techniques

The 802.11n standard requires at least -28dB EVM for the highest order modulation and coding rate. Due to the large PAR (12dB) of an OFDM signal, this level of EVM and linearity can be achieved by backing off the average OFDM power from the saturated power, at the expense of lower transmit power and severely degraded efficiency. The back-off is a function of the AM-AM and AM-PM characteristics of the transmitter. Figure 4.10 shows the simulated EVM vs. back-off for an ideal PA with a hard clip AM-AM and no AM-PM distortion. A 5dB and 5.5dB back-off from saturation is needed to meet the -25dB and -28dB EVM specifications. In order to see the impact of the AM-AM and AM-PM distortion on EVM, the AM-AM and AM-PM of the 2.4GHz PA and PA Driver are measured



(a)



(b)

Figure 4.12: (a) EVM as a result of having only AM-AM (b) EVM as a result of having only AM-PM. (c) EVM when having both AM-AM and AM-PM.

and applied to an OFDM signal in simulation. Figure 4.11 shows the measured AM-AM and AM-PM for three different gate biases of the PA input transistors. By reducing the gate bias, there is more phase distortion and more gain peaking. Figure 4.12(a) shows the simulated EVM vs. output power for the case where only phase distortion (from Fig. 4.11) exists. The results suggest that to meet the 5% EVM specification, a phase error of less than 10 degrees is required. Figure 4.12 (b) and (c) show the EVM for the case where there is only amplitude distortion, and the case where both amplitude and phase distortions are present. If we consider the other transmitter impairments, such as phase noise, supply noise, I/Q imbalance etc. the linearity requirement is even stricter to achieve a -28dB EVM. Compared to GaAs HBT and SiGe HBT PAs, deep-submicron CMOS PAs exhibit much worse linearity, especially in the 5GHz band. Figure 4.13 shows the measured AM-AM and AM-PM distortion of the 5GHz PA and PA Driver at 5.5GHz.

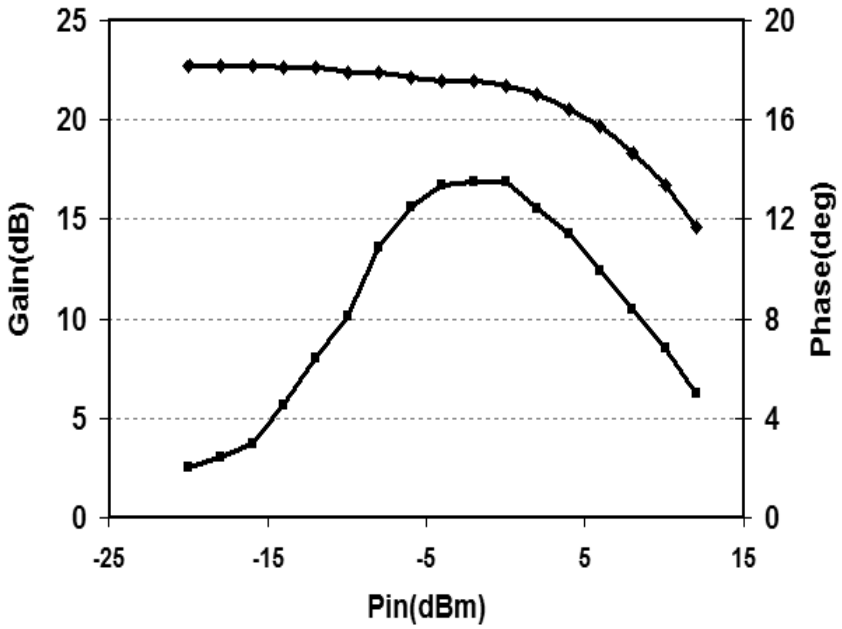


Figure 4.13: Measured AM-AM and AM-PM of 5GHz PA and PA Driver.

A number of linearization techniques have been proposed to improve the performance of integrated CMOS PAs [51–53]. For instance, [52] proposes a technique where the nonlinearity of a class-AB NMOS based PA due to the nonlinear

gate capacitor is compensated by an inverse nonlinearity introduced by a PMOS transistor in parallel with the input device. This technique is not very robust across the PVT and also reduces the gain of the amplifier due to extra parasitic capacitance at the PA input, which could make the design of the PA driver very difficult, particularly in the 5GHz band. Reference [53] proposes a technique using a varactor as part of a tuned circuit to introduce a phase shift that counteracts the AM-PM distortion of the PA. This technique requires a complex calibration scheme, as well as an accurate control signal and is very sensitive to the delay between signal and the control path. Due to these limitations, we therefore propose the use of two linearization schemes. First, the input device of the PA is divided to two separate devices, and each is biased independently (Fig. 4.8) [7]. The main device is biased closer to the class A region (which has a compressive nonlinearity), while the auxiliary device is biased closer to the class B region (which has an expansive nonlinearity); the combination linearizes the effective g_m over a wider range of the input voltage. Figure 4.14 shows the simulated g_m of the main and auxiliary stages, as well as the effective g_m, which is a more linear function of the input voltage. The effectiveness of this technique on overall PA linearity is shown in Fig. 4.15. The 2.4GHz PA is simulated and measured for two cases. In the first case, both the main and auxiliary amplifiers are biased close to the class A region and a P1dB of 21.7dBm is achieved. In the second case, the bias of the auxiliary pair is reduced to maximize the linearity of the overall g_m and as a result the P1dB is increased to 26.6dBm at the expense of lower small-signal gain due to lower overall effective g_m.

In addition, digital pre-distortion is used to achieve the final necessary linearity performance. In order to capture the AM-AM and AM-PM distortion of the transmit chain and correct them in the baseband, an attenuated version of the output of the PA using a capacitive divider C_2 and C_1 (Fig. 4.8) is down-converted through a single Gilbert cell mixer and, after proper filtering and amplification, is digitized and processed in the baseband DSP (Fig. 4.16). This feedback path was designed to ensure that it does not add significant distortion to the attenuated signal, while maintaining an acceptable SNR. To find the proper pre-distortion

function, a complex test signal is applied at the I and Q baseband ports. The pre-distortion function is then calculated by analyzing the AM-AM and AM-PM characteristics of the received signal. The SoC has the capability to utilize a variety of calibration signals, as well as algorithms for on-line or off-line calibration.

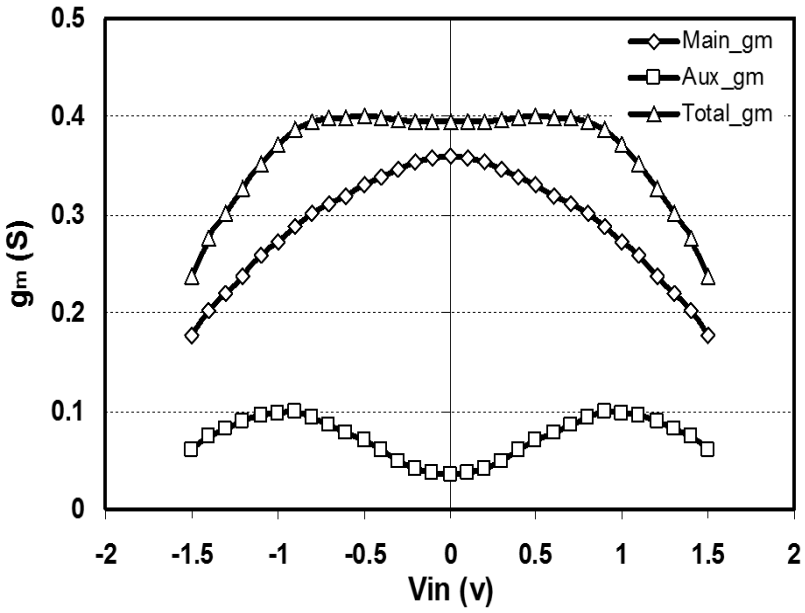


Figure 4.14: Simulated g_m for main and auxiliary devices and the overall g_m.

4.3 Measurements

The chip is fabricated in a 65nm standard CMOS technology. The die photo of the TX section is shown in Fig. 4.17. The size of each RF stage is shown in Table 4.1 shows the measured gain and efficiency of the PA for a CW signal. The 2.4GHz (5GHz) PA achieves 28.3dBm (26.7dBm) saturated power (including the on-chip balun loss) with 35.3% (25.3%) peak drain efficiency. At the saturation point, the 2.4GHz (5GHz) RFVGA and PA Driver are consuming 12mA (20mA) and 30mA (40mA) respectively.

By using the g_m-linearization technique, a P1dB of 26dBm and 23.5dBm is achieved for 2.4GHz and 5GHz bands respectively. As shown in Fig. 4.14, there are two humps in the gm of the auxiliary devices, corresponding to the gate bias

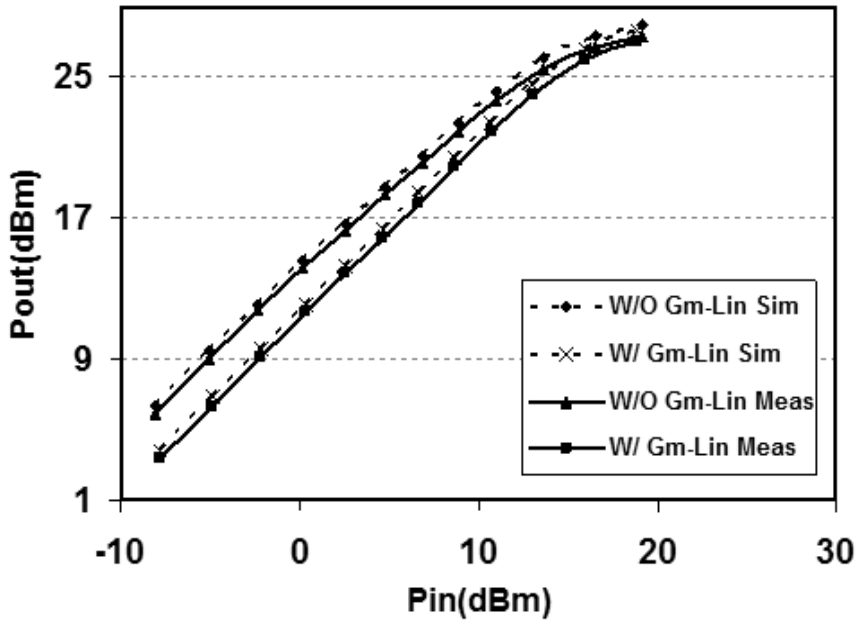


Figure 4.15: 2.4GHz simulated and measured AM-AM with and without using g_m-linearization technique.

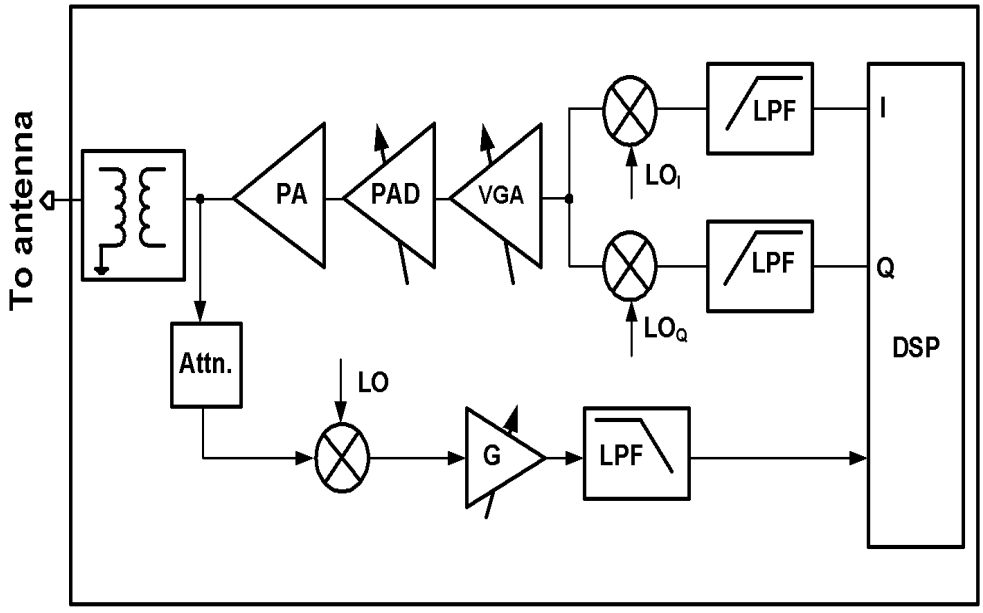


Figure 4.16: Block diagram of transmitter including the pre-distortion feedback path.

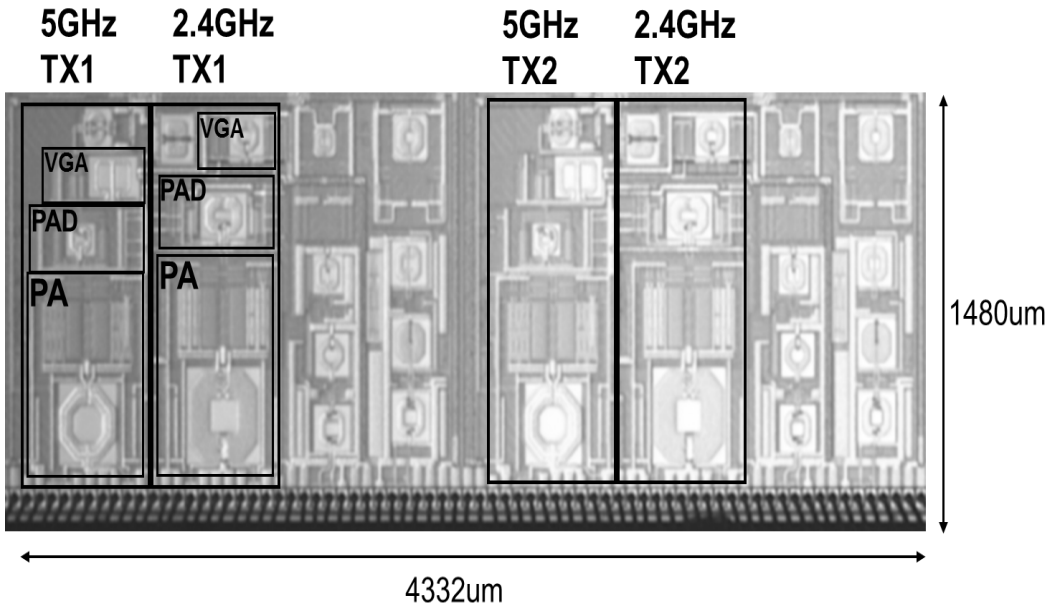


Figure 4.17: Die photo.

Table 4.1: Die size for each block

	$RFVGA$	PAD	PA
2.4GHz	$0.074mm^2$	$0.132mm^2$	$0.31mm^2$
5GHz	$0.085mm^2$	$0.092mm^2$	$0.27mm^2$

of the auxiliary devices. As a result, depending on the location of these humps and also the absolute value of the main and auxiliary gm, there could be some peaking in the gain (Fig. 4.18). Any residual AM-AM and AM-PM nonlinearity is subsequently corrected by the closed-loop pre-distortion algorithm. The TX RF section has more than 32dB and 40dB gain for 5GHz-6GHz and 2.4GHz bands respectively. In Fig. 4.19 the saturated power of the 5GHz PA is plotted across the entire band, which shows less than 0.5dB variation from 4.9GHz to 5.9GHz.

Figure 4.20 (a) and (b) show the measured EVM as a function of output power for a 54Mb/s OFDM signal for the entire TX chain (each core) for the 5-6GHz band and the 2.4GHz band. A -25dB (-28dB) EVM is achieved at 22.4dBm (21.2dBm) and 20.5dBm (19.5dBm) with a drain efficiency of 23.2% (19%) and 17.1% (14.1%) for 2.442GHz and 5.5GHz channels, respectively, using the described

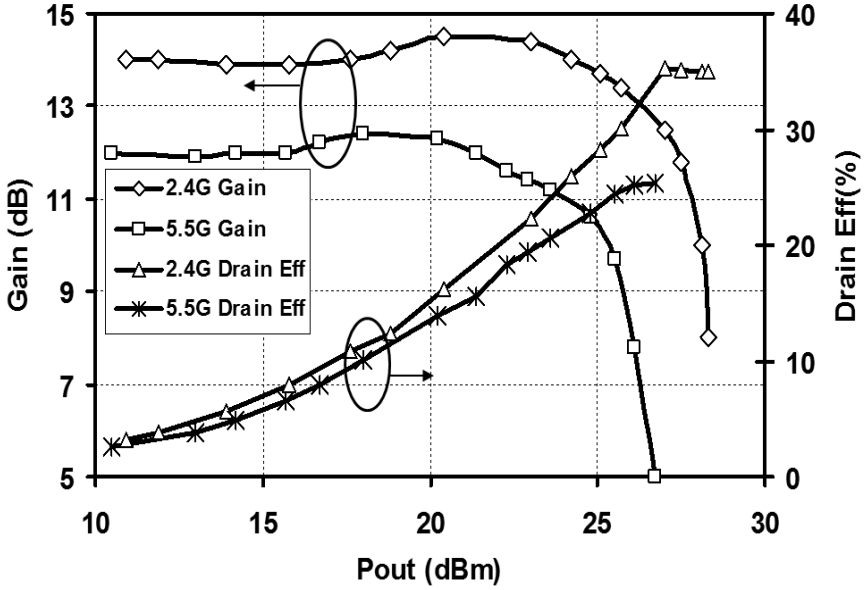


Figure 4.18: Measured CW gain and drain efficiency of the 2.4GHz and 5GHz PAs.

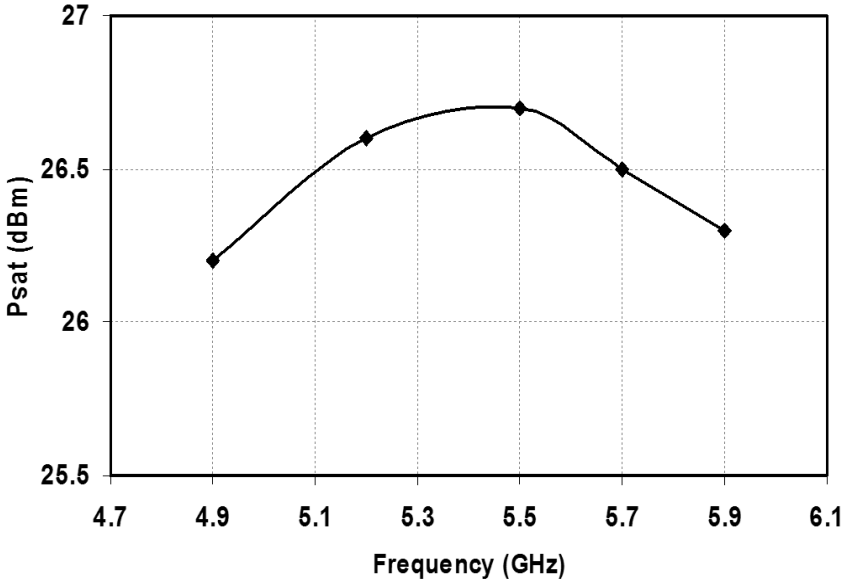
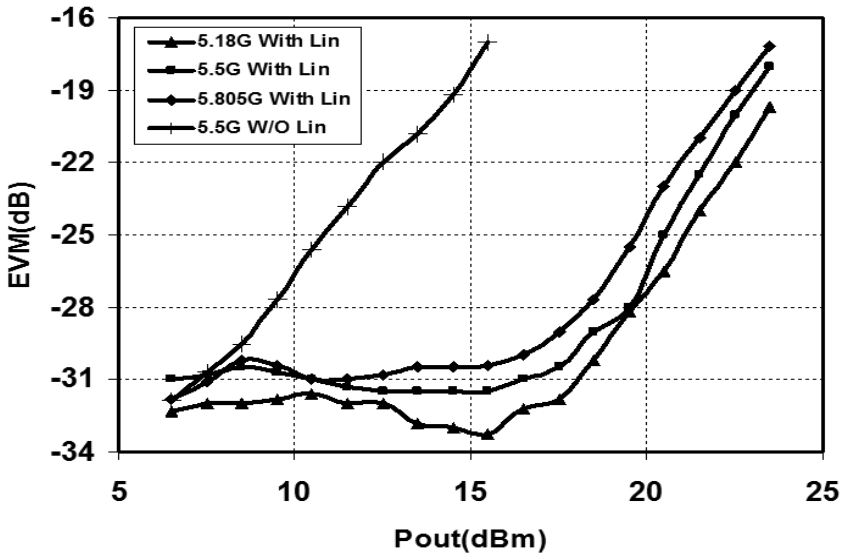
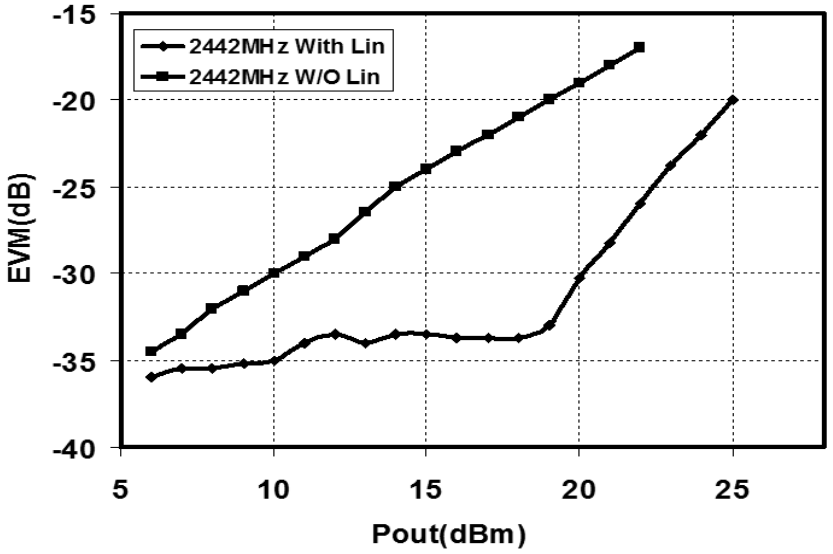


Figure 4.19: Measured saturated power across 5GHz band.

linearization scheme. Fig. 4.20 (b) also displays channel 2.442GHz with all linearization techniques disabled. It is clear that for a -25dB EVM, 8.4dB higher



(a)



(b)

Figure 4.20: (a) Measured EVM as a function of output power for 5GHz band with and without linearization. (b) Measured EVM as a function of output power for 2.4GHz band with and without linearization.

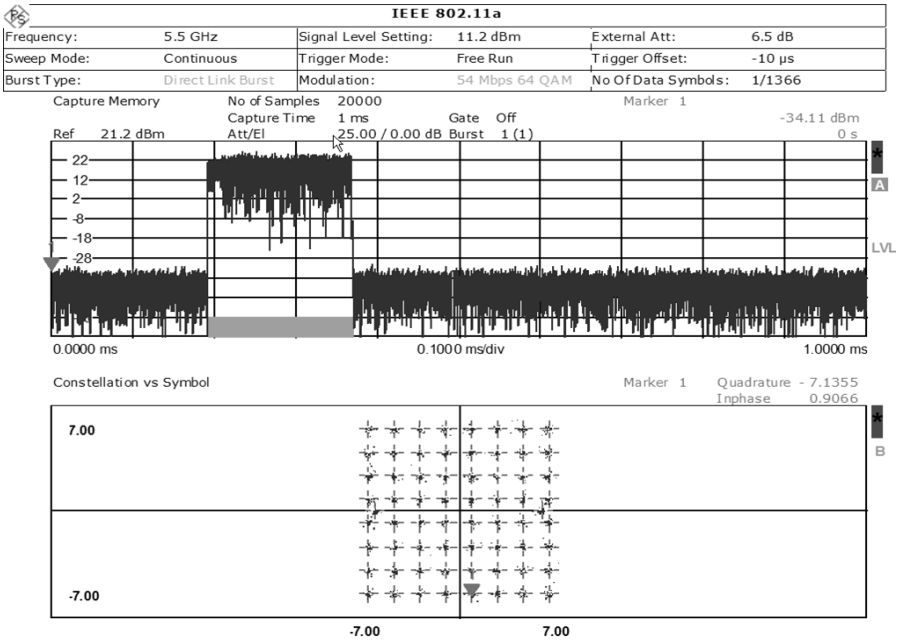


Figure 4.21: Measured 5G TX constellation diagram (Po=19dBm at 5500MHz).

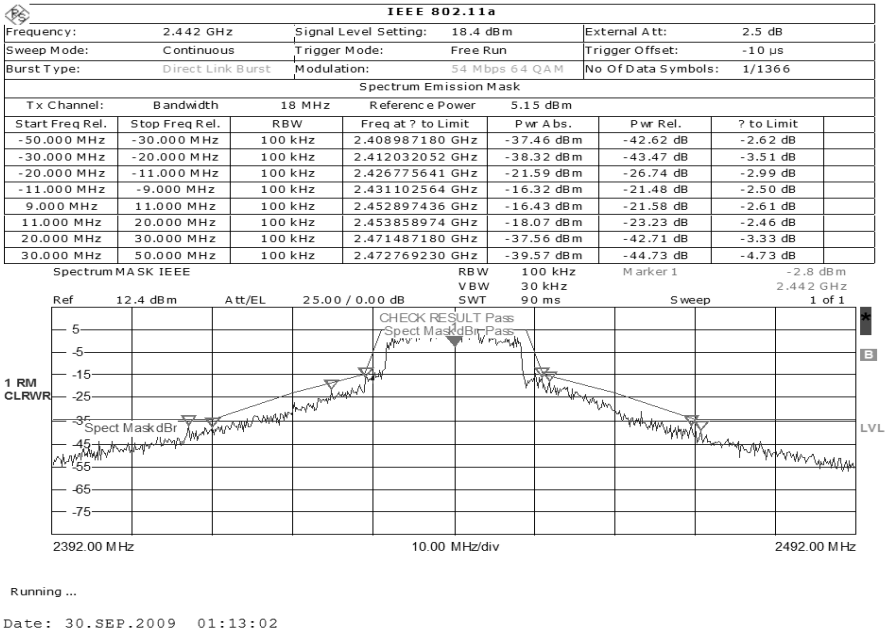


Figure 4.22: Measured 802.11g spectral mask for 22dBm Pout at 2442MHz.

power with 3.7 times higher efficiency is achieved with linearization. The constellation diagram at 19dBm TX power in the legacy 802.11a mode is shown in Fig. 4.21. Figure 4.22 shows the 802.11g spectral mask for 22dBm on channel 2.442GHz.

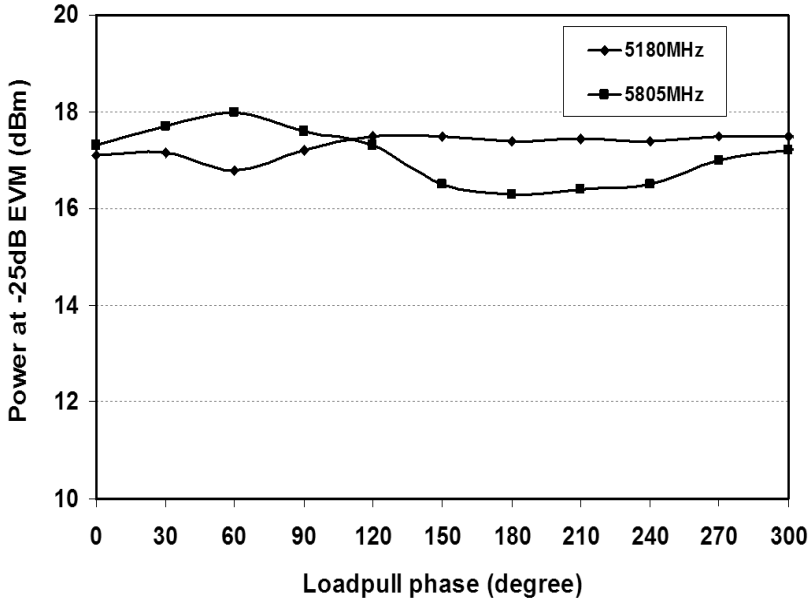


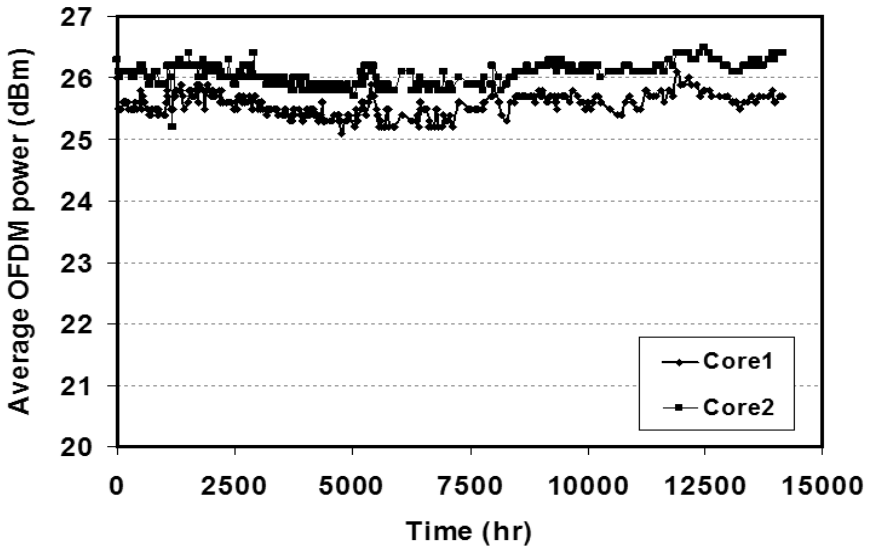
Figure 4.23: Measured performance under 3:1 VSWR for channels 5180MHz and 5805MHz.

The performance of the TX is examined under 3:1 VSWR condition at the antenna with 2.5dB board loss. Figure 4.23 shows the max linear power (-28dB EVM) for channels 5180MHz and 5805MHz after applying all the linearization techniques with less than 2 dB variation across all the angles. Table II summarizes the performance of the dual-band PA presented in this chater and shows the comparison with other state-of-the-art MIMO PAs.

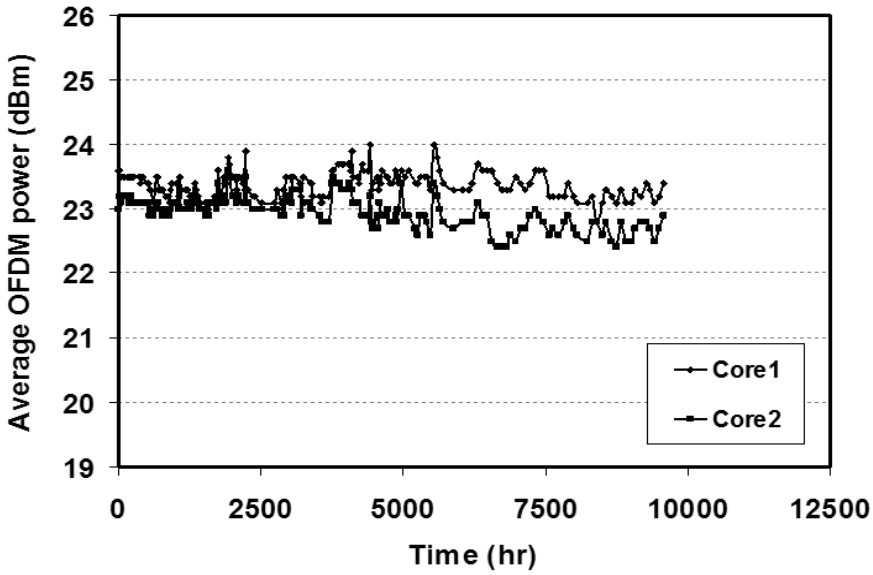
4.4 Reliability

There are a variety of degradation mechanisms that must be considered in the design of the CMOS power amplifier.

These mechanisms can coexist during the PA operation [54–56]. There are three key MOS aging phenomena that can result in transistor failure, Negative Bias Temperature Instability (NBTI) which is dominant in PMOS, Hot Carrier Injection (HCI) which can happen in both NMOS and PMOS and Time Dependant Dielectric Breakdown (TDDB), which is a failure mechanism due to catastrophic



(a)



(b)

Figure 4.24: Measured output power degradation over time at 3.6v supply and 27C (a) Channel 2442MHz, (b) Channel 5500MHz.

failure of the transistor gate dielectric resulting in a hard failure of the transistors. NBTI is a strong function of Vgb bias, and becomes worse at higher temperature.

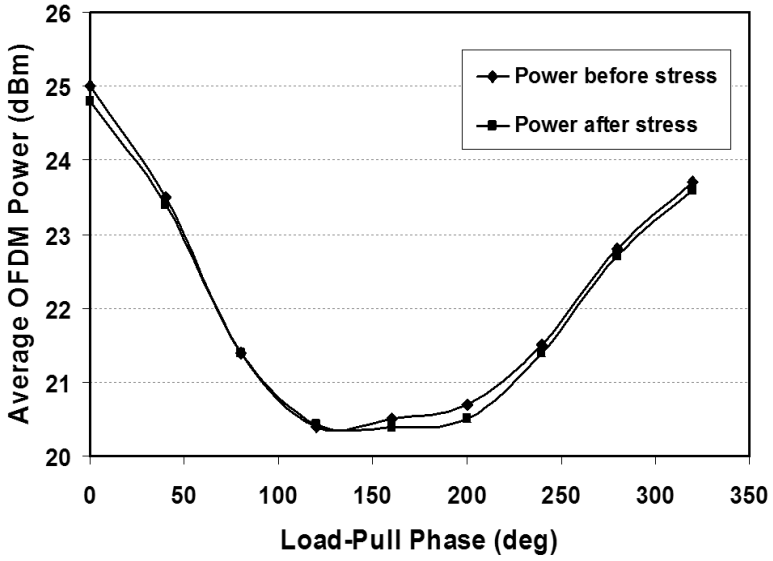


Figure 4.25: Measured output power degradation under 10:1 VSWR for different load-pull phases for channel 2442MHz.

The most important effect of NBTI is a threshold voltage (V_t) shift, which can progress until the transistor is destroyed. In HCI, the degradation is a function of the V_{gs} and V_{ds} stress combination and the most prominent effects are g_m, R_ds and V_t shifts. HCI damages are more severe at the drain side, resulting in asymmetrical device characteristics after stress. HCI usually gets worse at lower temperatures. TDDB usually happens when the gate oxide is overdriven beyond TDDB specifications, and it is worse at higher temperature, and the failures show up as a sudden fatality.

There are also some other MOS aging mechanisms such as Positive Bias Temperature Instability (PBTI), which is seldom an issue in low voltage applications, Non-Conducting Stress (NCS) which is important when $V_{gs} = 0$ and $V_{ds} > 0$ and Stress Induced Leakage Current (SILC) which has more impact on flash memories and MOS 1/f noise [57, 58].

In this design, the bias voltages of each transistor are selected to make sure all the devices are in a reliable region with general foundry guidelines being considered. Also, the transmit aging effect is simulated at its operating point with

an OFDM source. In order to obtain an assessment of the transmit performance degradation over time in a real application, a high average power 64-QAM OFDM signal with more than 90% duty cycle is transmitted using the on-chip baseband generator. The output power is monitored for an extreme condition for a long period of time for hundreds of parts while transmitting on both cores at the same time.

Figure 4.24 (a) shows the output power at 2.442GHz, 3.6v supply and room temperature while transmitting 25.5dBm 54Mbps OFDM signal at both cores simultaneously. In this experiment, the power control loop is disabled. The PAs exhibit less than 0.5dB degradation over this time period. In a real application, the power control loop would easily compensate for any such reduction of power.

Table 4.2: Performance Comparison

	ref[8]	ref[15]	This work
Psat (2.4GHz)	$25dBm$	$NoData$	$28.3dBm$
Psat(5.5GHz)	$23.5dBm$	$25dBm$	$26.7dBm$
Power @ -25dB (-28dB)			
EVM (2.4G)	$17(15.5)dBm$	$8.5(17.5)dBm$	$22.4(21.2)dBm$
Power @ -25dB (-28dB)			
EVM (5.5GHz)	$16(14.5)dBm$	$18.3(17)dBm$	$20.5(19.5)dBm$
Max Eff (2.4GHz)	50%	$NoData$	35.3%
Max Eff (5.5GHz)	30%	$NoData$	25.3%
Linearization	DPD	No	DPD and Offset-Gm
On chip balun	No	N/A	Yes
Supply	$3.3V$	$3.3V$	$3.3V$
Technology	90nm CMOS	SiGe HBT	65nm CMOS

Figure 4.24 (b) shows the output power of 5GHz PA with the same supply and temperature conditions as 2GHz PA while transmitting 23.5dBm OFDM signal at 5.5GHz. The reliability of the PAs are also tested at -40C and 75C for typical process corner as well as fast and slow corners and less than a 0.5dB degradation in output power is observed.

To test the ruggedness of the PA under VSWR condition, the output power is monitored for 10:1 VSWR condition. First the power for each phase is measured. Then PA is left for one hour at each phase while transmitting a large OFDM

signal continuously. After one hour, the output power for each phase re-measured. Figure 4.25 shows that there is no significant degradation in output power under 10:1 VSWR conditions.

4.5 Summary

A fully integrated, 2x2 dual band draft 802.11n power amplifier has been implemented in a standard 65nm CMOS process. A low-loss on chip balun is used to convert the differential output to single-ended, while providing an optimum load to the PA. Multiple linearization schemes are used to linearize the PA, to transmit a higher output power and obtain a higher efficiency while satisfying the standard specifications for both 2.3GHz and 5GHz bands. The reliability of the PAs are evaluated with accelerated aging tests under extreme conditions, with no failures observed. Chapter 4 is in full a reprint of the material as it appears in IEEE Journal of Solid State Circuits, vol. 45, no. 5, pp. 955-966, May 2010. The dissertation author is the primary investigator and author of this paper. Professor Lawrence Larson supervised the research which forms the basis for this paper.

Chapter 5

Power Combining Techniques

As was discussed in Chapter 3, there are several practical issues to design a high E PA in CMOS processes. Power combining is an attractive solution to some of these problems and there has been a significant amount of effort on the development of on-chip power combiners. In this section, we will compare four candidates for integration.

5.1 Wilkinson Power Combiner

One commonly used combiner in micro-strip circuits is the Wilkinson divider/combiner [59]. A lumped-element equivalent circuit can be used in lower frequency applications using the quarter-wave transmission line LC equivalent network [60].

Figure 5.1 shows an N-way lumped-element Wilkinson power combiner. The necessary value of the capacitance, inductance and resistance can be calculated from

$$L = \frac{\sqrt{NR_L R_{in}}}{\omega},\ C = \frac{1}{\omega\sqrt{NR_L R_{in}}},\ R = R_{in} \tag{5.1}$$

The total efficiency of the combiner is equal to the efficiency of one of the branches shown in Fig. 5.2. The power dissipated in the inductor is

$$P_{loss} = \frac{\omega L}{Q_{ind}} |i_1|^2 \tag{5.2}$$

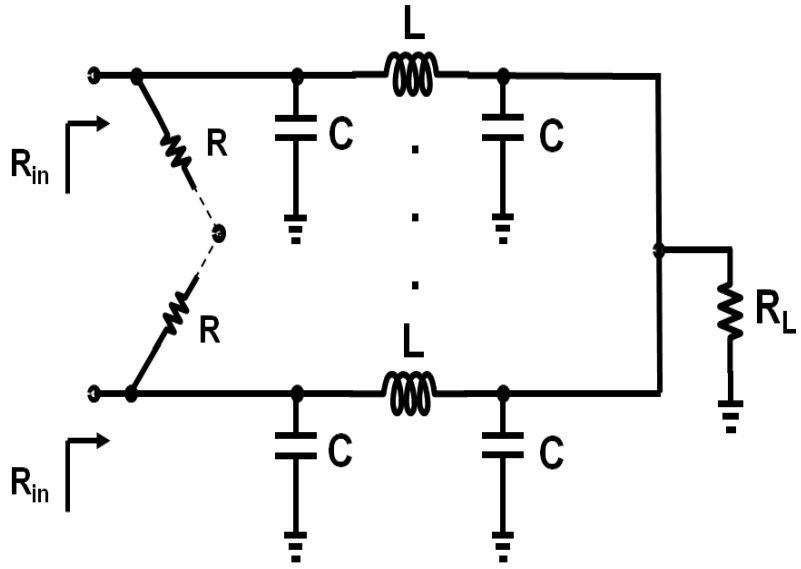


Figure 5.1: N-way lumped-element equivalent model of Wilkinson power combiner.

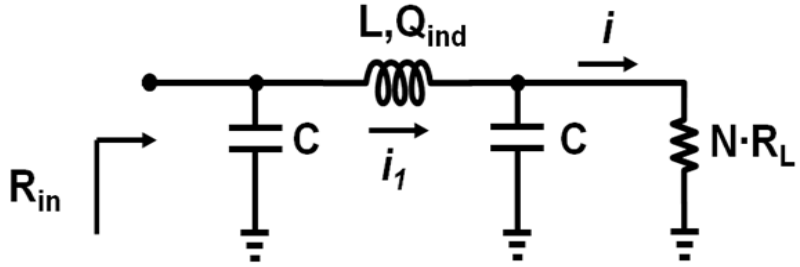


Figure 5.2: Equivalent model of a single branch of the Wilkinson combiner.

and the output power is

$$P_{lout} = NR_L |i|^2 \tag{5.3}$$

where

$$i = \frac{1}{1 + jNR_L C\omega} i_1 \tag{5.4}$$

and

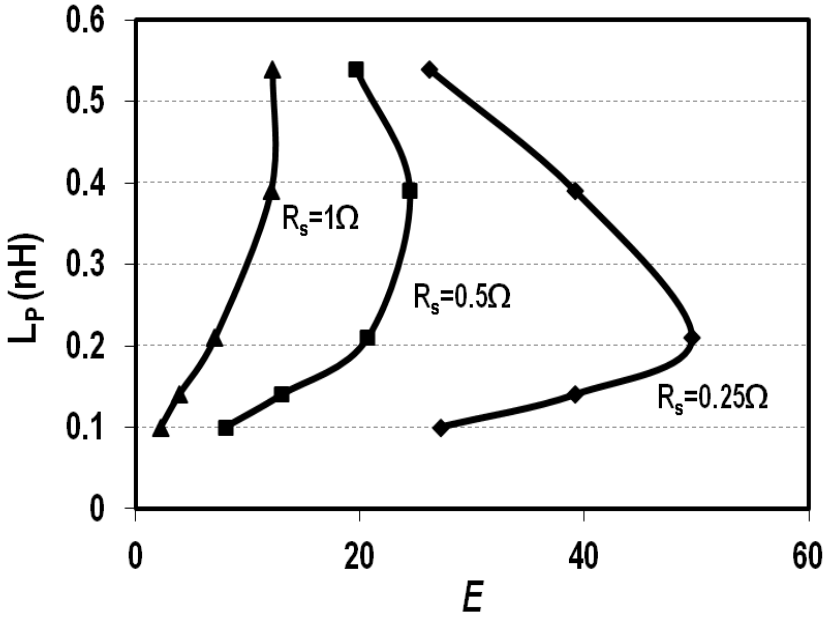


Figure 5.3: Loss of 2-way Wilkinson power combiner for 100 Ω to 50 Ω transformation at 2.45 GHz as a function of inductor Q.

$$|i| = \frac{1}{\sqrt{1+rN}}\,|i_1| \tag{5.5}$$

from 5.1. Therefore η can be calculated from

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}} = \frac{Q_{ind}}{Q_{ind}+\sqrt{\frac{1}{Nr}}+\sqrt{Nr}} \tag{5.6}$$

where Q_{ind} is the quality factor of each inductor and r is the impedance transformation ratio from the load to the output of each branch when the inductor is ideal. Figure 5.3 compares the loss of a 2-way combiner when $r = 2$, calculated from 5.6 with simulation results, and the agreement is excellent.

5.2 Distributed-LC Power Combiner

In this technique [18], the power transistor is divided into N equivalent sections and a distributed high-pass LC network is used to provide N times larger impedance at the drain of each transistor, as shown in Fig. 5.4(a). The distributed

impedance transformation ratio r is defined as the ratio of the load impedance to the impedance provided to one of the PAs. The impedance seen by each PA is

$$Z_{in} = \frac{NL_{dist}^2\omega^2 R_L}{R_L^2 + L_{dist}^2\omega^2} + j.(\frac{NL_{dist}\omega R_L^2}{R_L^2 + L_{dist}^2\zeta\omega^2} - \frac{1}{C_{dist}\omega}) \tag{5.7}$$

At resonance

$$\frac{1}{C_{dist}\omega} = \frac{NL_{dist}\omega R_L^2}{R_L^2 + L_{dist}^2\omega^2} \tag{5.8}$$

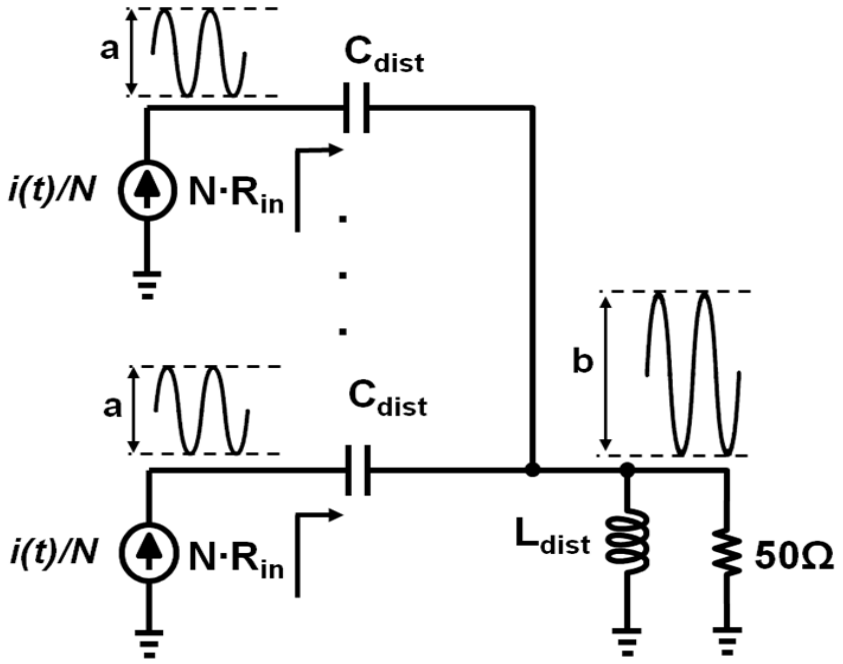
and

$$Real[Z_{in}] = R_{in} = \frac{NL_{dist}^2\omega^2 R_L}{R_L^2 + L_{dist}^2\omega^2} \tag{5.9}$$

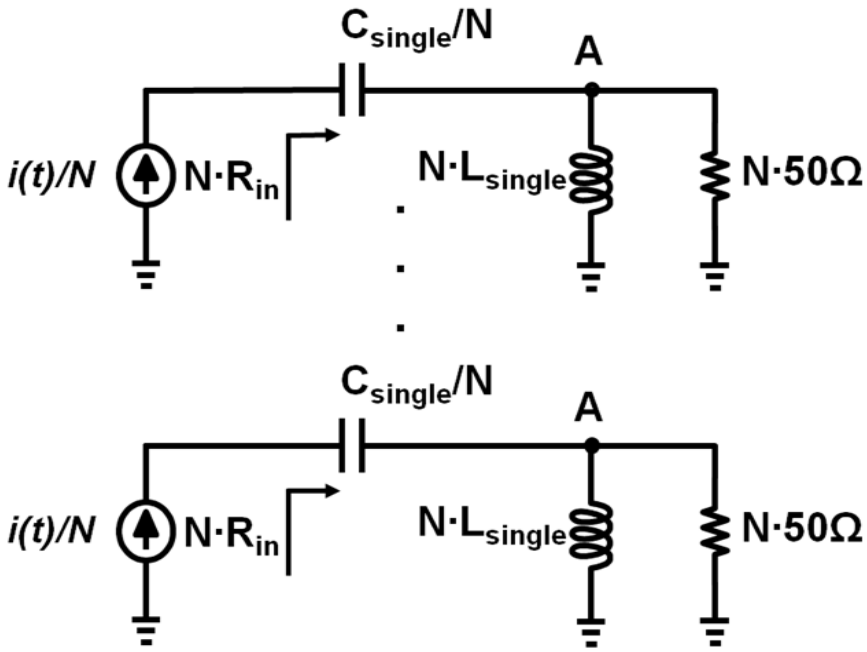
In order to achieve $1/N^{th}$ the transformation ratio compared to a single stage-design, the value of capacitance and inductance can be calculated from

$$r_{dist} = \frac{r_{single}}{N} \Rightarrow L_{dist} = L_{single}, C_{dist} = \frac{C_{single}}{N} \tag{5.10}$$

where L_{single} and C_{single} are the inductance and capacitance values of the single-stage matching network. As one can see, the same inductance is used as the single-stage LC network for a given output power, and therefore the efficiency of the distributed LC combiner in the absence of parasitic resistance R_s is the same as the single-stage LC network, since the power dissipated in the inductor is the same in each case. However, since each PA is presented with N times higher impedance, it requires an N times smaller device, which makes the design of the individual PA driver more efficient. This is also the case in other power combining approaches. In addition, the efficiency of the distributed LC network is less sensitive to R_s (any parasitic resistance) in series with each capacitor due to the higher impedance provided to each PA. In order to demonstrate this, we model the combiner in Fig. 5.4(a) by N parallel LC networks (Fig. 5.4(b)) which are connected together at node A. The efficiency of entire combiner is equal to efficiency of each LC branch. In the presence of R_s (assuming infinite Q for inductor), the efficiency can be found from



(a)



(b)

Figure 5.4: Single stage and distributed-LC matching network.

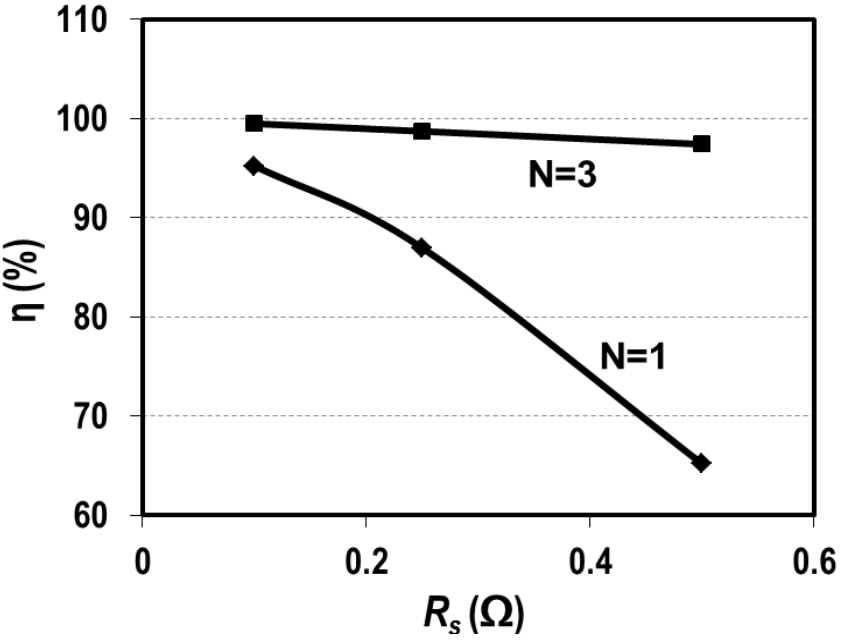


Figure 5.5: Efficiency of the single stage vs distributed-LC network as a function of Rs.

$$\eta \cong 1 - \frac{r_{single}}{N^2} \cdot \frac{R_s}{R_L} = \frac{1 + \sqrt{1 - \frac{4R_s}{N^2 R_L} E_{dist}}}{2} \tag{5.11}$$

and $E_{dist-max}$ is equal to

$$E_{dist-max} = \frac{N^2 R_L}{4R_s} \tag{5.12}$$

As one can see, the efficiency for a given E is less sensitive to R_s compared to single-stage LC network (3.11). Figure 5.5 compares the efficiency of a distributed LC network with three sections (N=3) with a single-stage LC network, for different R_s values assuming an ideal inductor and $E = 23$ at 2.45 GHz. For example, for the case of $R_s = 0.5\ \Omega$, the efficiency of distributed LC network is 97% compared to 65% for a single-stage design.

In order to see the impact of the mismatch between the capacitors on the combiner performance, we assume each PA operates at saturated power, which corresponds to the maximum voltage swing at the drain of each transistor. Therefore, we can approximate each PA by a voltage source V_{pa}. In a single-stage LC

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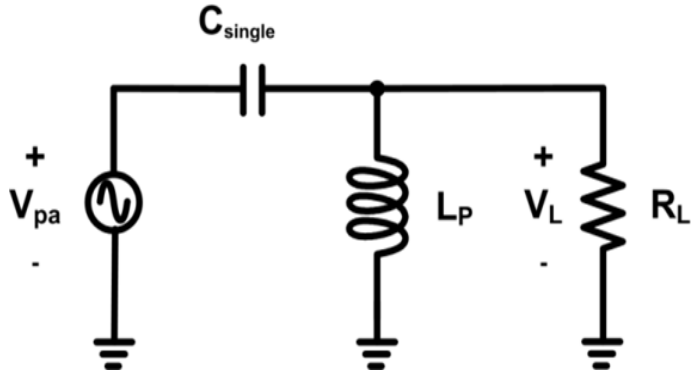
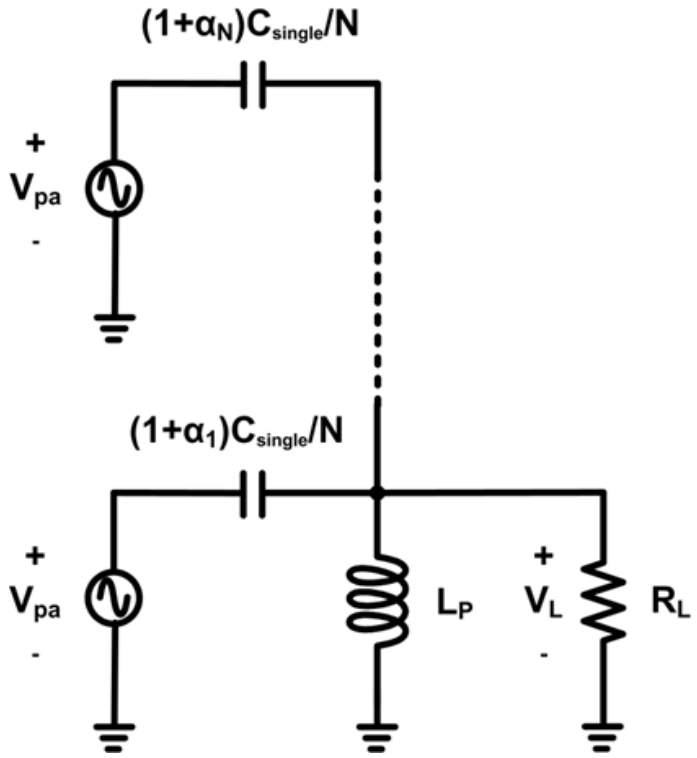


(a)



(b)

Figure 5.6: (a) Single stage LC matching network. (b) Distributed-LC matching network with capacitor mismatch.

network (Fig. 5.6(a)) the load voltage can be calculated from

$$V_L = \frac{jR_L C_{single}\omega}{1 + j\frac{R_L}{Q_L^2} C_{single}\omega} \cdot V_{pa} \tag{5.13}$$

where Q_L is the inductor loaded quality factor. In a distributed LC combiner, the voltage across the load will be determined by (5.13) if there is no mismatch between capacitors. However, if there is a mismatch between capacitors (Fig. 5.6(b)) the load voltage is

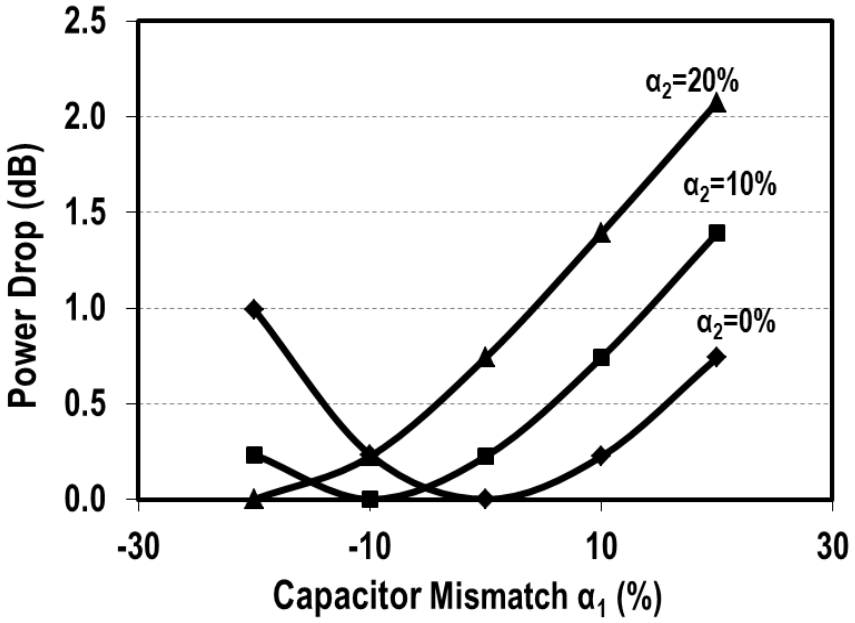


Figure 5.7: Calculated drop in peak power due to capacitor mismatch in distributed-LC network with two branches and E=22.7 at 2.45 GHz.

$$V_L = \frac{jR_L C_{single}\omega(1+\frac{1}{N}\sum_{i=1}^{N}\alpha_i)}{1+jR_L C_{single}\omega(\frac{1}{Q_L^2}+\frac{1}{N}\sum_{i=1}^{N}\alpha_i)} \cdot V_{pa} \tag{5.14}$$

where α_i is the mismatch coefficient for capacitor i and is defined as

$$\alpha_i = \frac{NC_{dist-i} - C_{single}}{C_{single}} \tag{5.15}$$

The drop in maximum power due to this mismatch can be calculated from

$$P_{sat-max} - P_{sat} = 20log\left|\frac{(1+j\frac{R_L}{Q_L^2}C_{single}\omega)(1+\frac{1}{N}\sum_{i=1}^{N}\alpha_i)}{1+jR_L C_{single}\omega(\frac{1}{Q_L^2}+\frac{1}{N}\sum_{i=1}^{N}\alpha_i)}\right| \tag{5.16}$$

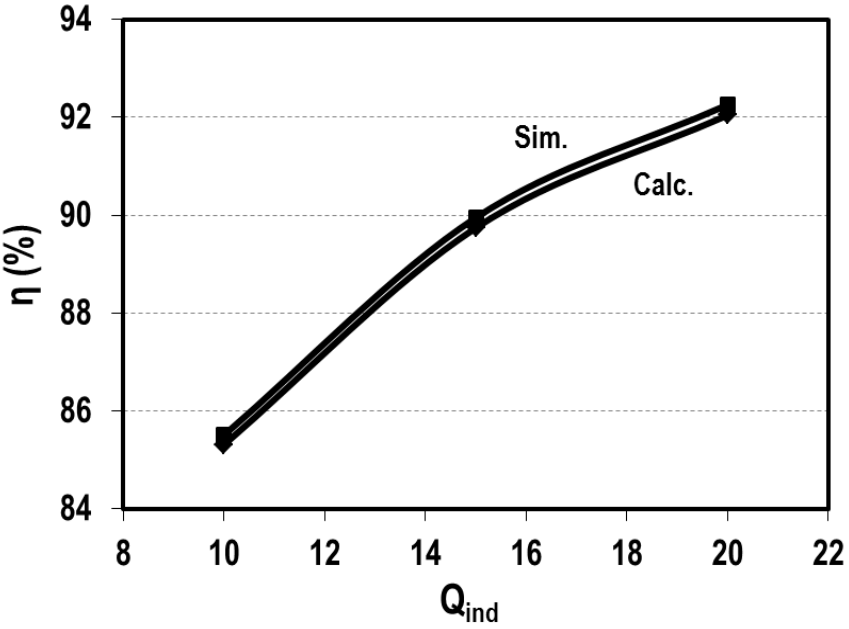


Figure 5.8: Loss of 2-way distributed-LC combiner while r=2 at 2.45 GHz as a function of inductor Q.

Figure 5.7 shows the power drop due to mismatch between capacitors in an LC distributed network with two branches and E=23 at 2.45 GHz. For this case the drop in Psat will be less that 1 dB if the capacitor values are in the range of +/-10% of nominal value.

Compared to the Wilkinson power combiner, the distributed-LC combiner requires only one inductor which results in significant area saving. The efficiency of the N-way distributed-LC combiner when $R_s = 0$ can be calculated from

$$\eta = \frac{Q_{ind}}{Q_{ind} + \sqrt{Nr - 1}} \tag{5.17}$$

where Q_{ind} is the quality factor of the inductor and r is the impedance transformation ratio from the load to the output of each branch when the inductor is ideal. Figure 5.8 compares the loss of the 2-way distributed-LC combiner while r=2 with simulation, which confirms the accuracy of (5.17). Figure 5.9 compares the loss of N-way Wilkinson and N-way distributed-LC power combiners as a function of Nr and inductor quality factor which shows distributed-LC power combiner has lower loss.

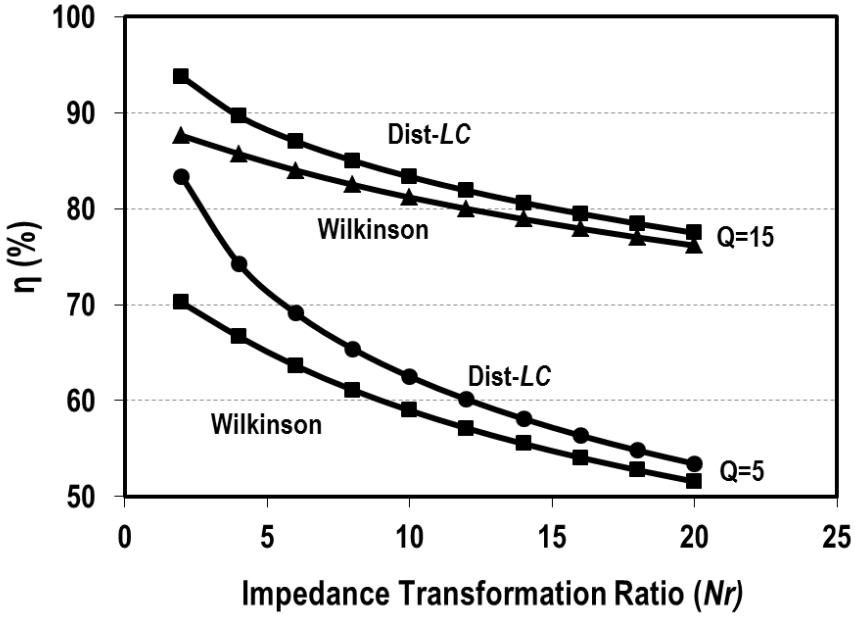
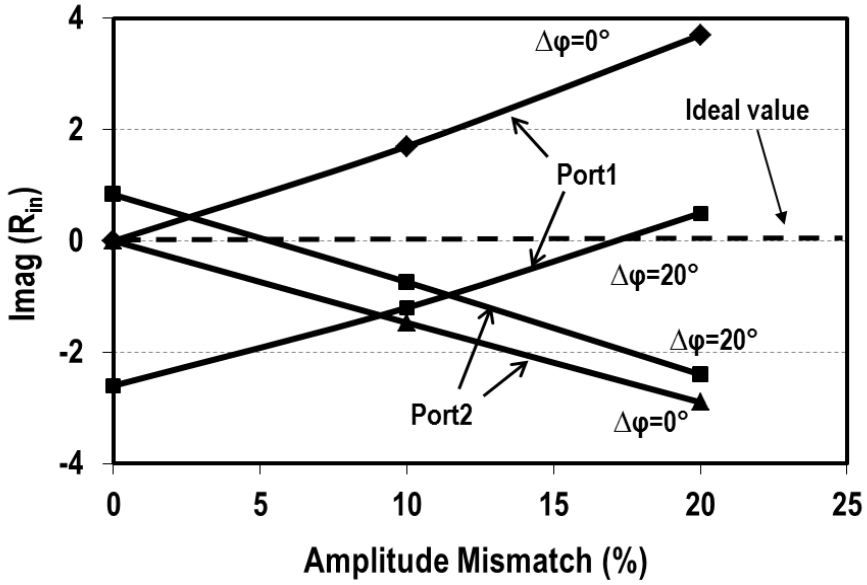


Figure 5.9: Calculated combining network efficiency of N-way Wilkinson and N-way distributed-LC power combiners as a function of Nr and inductor quality factor.

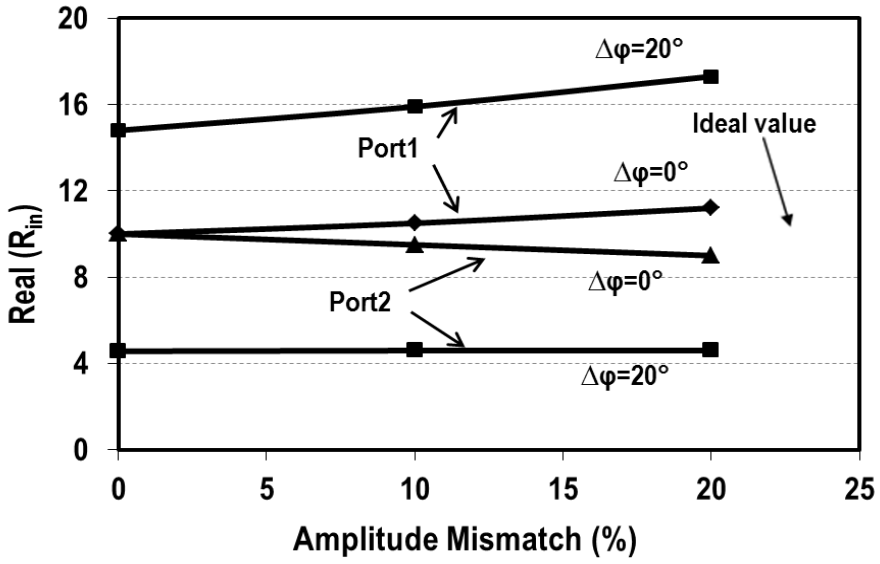
One of the main advantages of Wilkinson combiner compared to distributed-LC combiner is its robustness to the mismatch between power amplifiers. In order to show this, a two-way Wilkinson and distributed-LC combiners are simulated at 2.45 GHz while transforming 50 Ω to 10 Ω at the output of each PA. The impedance presented to each PA in the Wilkinson combiner remains at 10 Ω when there is a mismatch; however it changes in the LC combiner. Figure 5.10 shows the impedance that each PA sees when there is a mismatch between amplitude and phase of the current generated by one of the PA relative to the other one. Figure 5.11 plots the simulated output power drop due to mismatch, which is very similar in both combiners.

5.3 Voltage-mode Transformer-Based Combiner

This approach has been demonstrated utilizing slab inductors, a figure 8 structure and symmetric two-way power combining [10, 46, 61, 62]. The details



(a)



(b)

Figure 5.10: Single stage and distributed-LC matching network.

of this type of combiner have been discussed in the referred papers and we just highlight some of the key features as a reference. In all cases, the secondary coils of N transformers are connected in series and their primaries are driven by separate

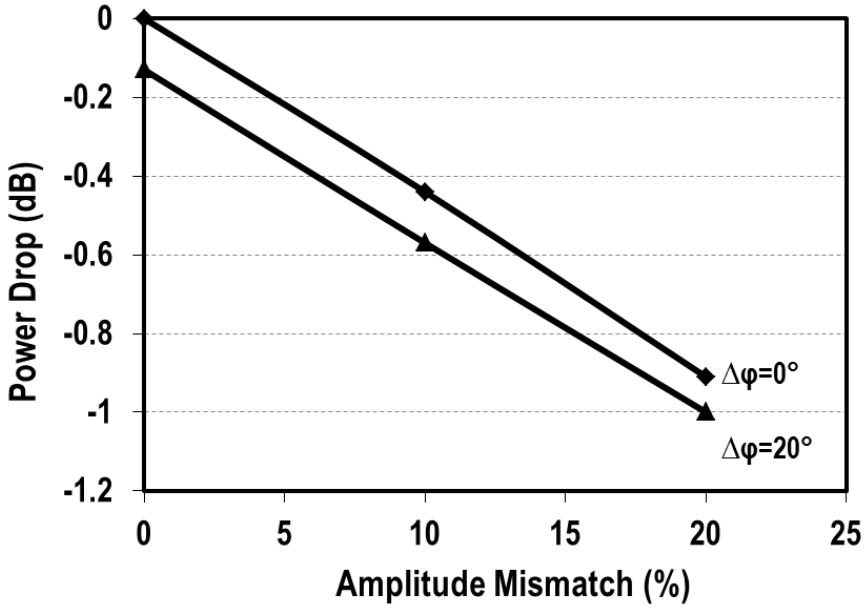


Figure 5.11: Output power drop due to mismatch between the amplitudes and phases of the PAs in 2-way *LC* and 2-way Wilkinson combiners.

amplifiers as shown in Fig. 5.12.

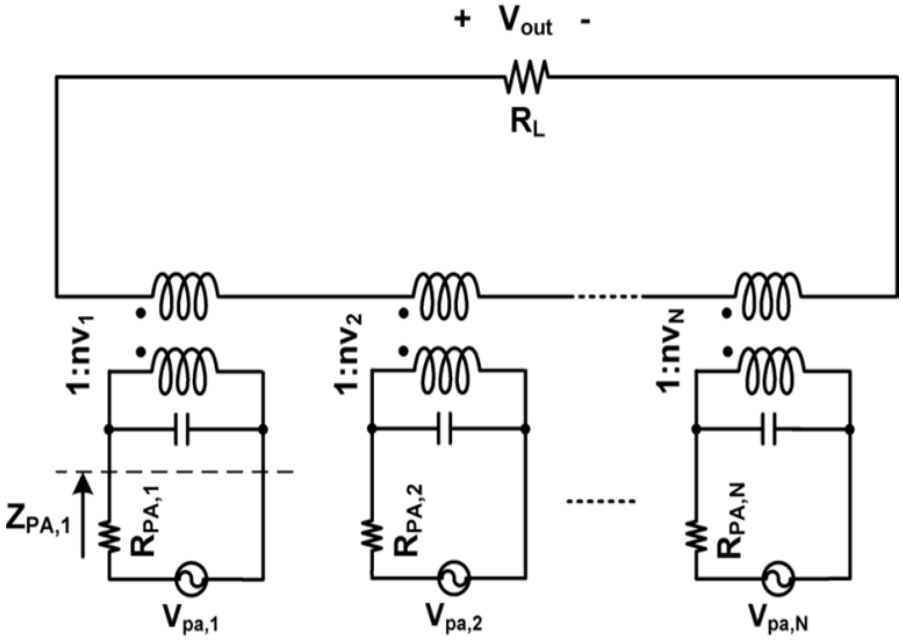


Figure 5.12: Voltage-mode transformer-based power combiner.

The AC voltages add on the secondary side, generating higher output power.

To simplify the equations it is assumed that transformers are lossless and their effective primary inductances are tuned with the capacitance load at the primary at the operating frequency. Therefore, the impedance seen by each PA can be written as [20]

$$Z_{nv,j} = \frac{(R_L + \sum_{i=1}^{N} nv_i^2 \cdot R_{PA,i}) \cdot V_{pa,j}}{nv_j \cdot \sum_{i=1}^{N} nv_i \cdot V_{pa,i}} - R_{PA,j} \tag{5.18}$$

where R_L is the load impedance, nv_i is the turn ratio of the transformer i and $V_{pa,i}$ and $R_{PA,i}$ are the Thevenin equivalent voltage source and output impedance of PA i. It can be seen that the impedance that each PA sees is a function of output impedance and output voltage of all the PAs. If we assume all the power amplifiers have the same output impedance and output voltage and all transformers have the same turn ratio nv, 5.18 simplifies to a resistive value of

$$R_{nv} = \frac{R_L}{N \cdot nv^2} \tag{5.19}$$

and the total power delivered to load equals to

$$P_{out} = N^2 \cdot nv^2 \frac{V_{pa}^2}{2R_L} \tag{5.20}$$

assuming $R_{nv} >> R_{PA}$. The impedance transformation ratio is defined as

$$r = \frac{R_L}{R_{nv}} = N \cdot nv^2 \tag{5.21}$$

5.21 shows that the output power can be increased by increasing N or nv.

5.4 Current-mode Transformer-Based Combiner

In this approach [63], the secondary coils are connected in parallel and their primaries are driven by separate amplifiers as shown in Fig. 5.13. The secondary currents sum in the load impedance to generate high output power.

To find the admittance Y_{nc} seen by each PA, assume that each amplifier is modeled with its Norton equivalent current source $I_{pa,i}$ and output admittance $G_{PA,i}$ and the turn ratio of transformer i is 1:n_{ci} . Then, the primary voltage in transformer i, when only considering current source $I_{pa,i}$, can be obtained as

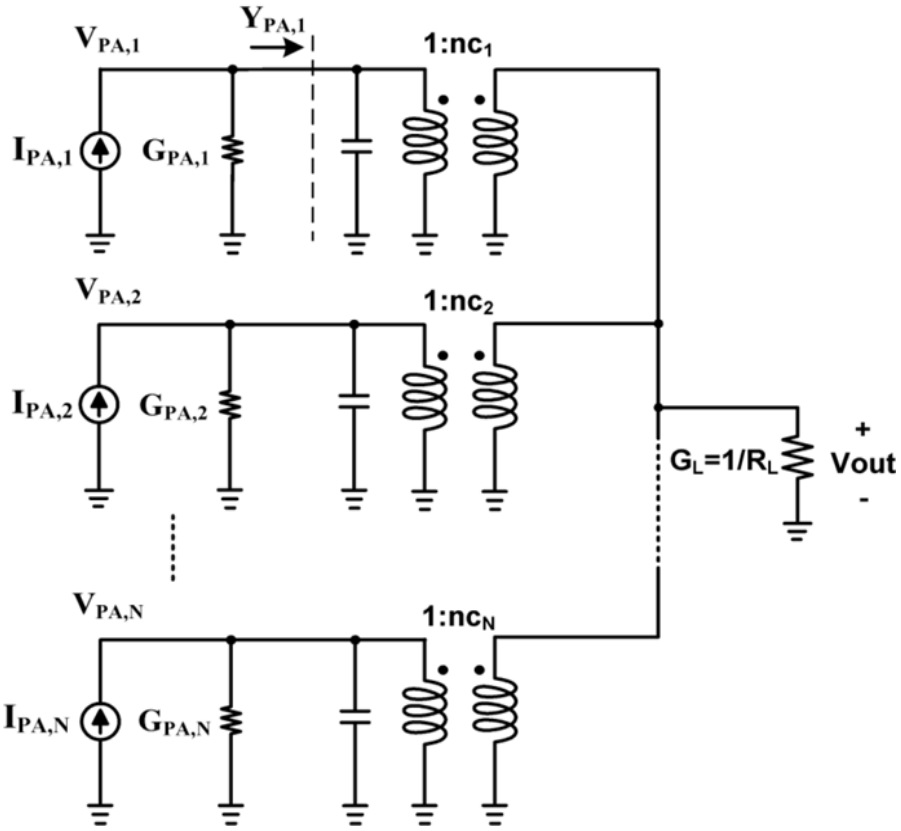


Figure 5.13: Current-mode transformer-based power combiner.

$$V_{PA,i,i} = \frac{i_{PA,i}}{nc_i^2 \cdot (G_L + \sum_{j=1}^{N} \frac{G_{PA,j}}{nc_j^2})} \tag{5.22}$$

Similarly, the primary voltage in transformer i when only considering current source $I_{pa,k}$ can be written as

$$V_{PA,i,k} = \frac{i_{PA,k}}{nc_i nc_k \cdot (G_L + \sum_{j=1}^{N} \frac{G_{PA,j}}{nc_j^2})} \tag{5.23}$$

The total primary voltage of transformer i, according to superposition theorem, can be found from

$$V_{PA,i} = \frac{1}{nc_i \cdot (G_L + \sum_{j=1}^{N} \frac{G_{PA,j}}{nc_j^2})} \cdot \sum_{j=1}^{N} \frac{i_{PA,j}}{nc_j} \tag{5.24}$$

Since $V_{PA,i}$ can also be written as

$$V_{PA,i} = \frac{i_{PA,i}}{G_{PA,i} + Y_{PA,i}} \tag{5.25}$$

the transformed load admittance, $Y_{PA,i}$, seen by amplifier i can be written as

$$Y_{PA,i} = \frac{i_{PA,i}}{V_{PA,i}} - G_{PA,i} = \frac{nc_i \cdot (G_L + \sum_{j=1}^{N} \frac{G_{PA,j}}{nc_j^2}) \cdot i_{PA,i}}{\sum_{j=1}^{N} \frac{i_{PA,j}}{nc_j}} - G_{PA,i} \tag{5.26}$$

Here also for simplicity it is assumed that transformers are lossless and their effective primary inductances are tuned with the capacitance load at the primary at the operation frequency. When all power amplifiers and transformers are identical, 5.26 simplifies to a value of

$$G_{nc} = \frac{G_L \cdot nc^2}{N} \tag{5.27}$$

where nc is the turn ratio of each transformer. The impedance transformation ratio is defined as

$$r = \frac{R_L}{R_{nc}} = \frac{nc^2}{N} \tag{5.28}$$

In order to achieve the same transformation ratio as the one in voltage-mode transformer based combiner,nc must be N times larger than nv. Using the above analysis, we can see for large E it is more efficient and practical to use a power combiner than a single matching network. In addition, based on the analysis in chapter 4, a transformer can provide better efficiency than an LC network for larger output power.

5.5 Watt-level 2.4GHz CMOS PA for WLAN application

To demonstrate these techniques, two PAs have been fabricated in standard 65-nm CMOS using distributed LC matching and current-mode transformer-based combiner networks. The details of the PA core design is explained in 4. Each chip has been packaged in 40-pin QFN package. Figures 5.14 and 5.15 show the two die photographs.

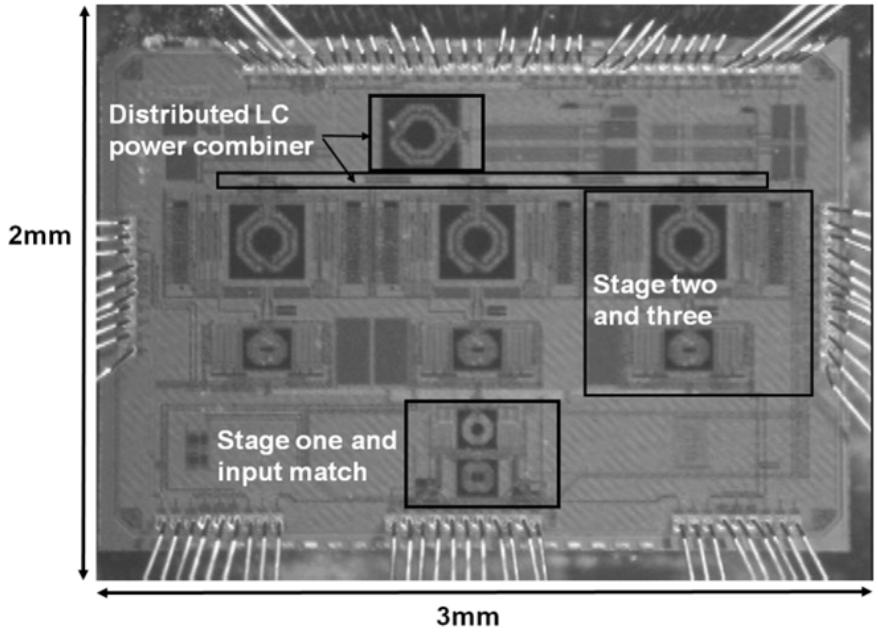


Figure 5.14: Die photo of the PA with distributed-LC combiner.

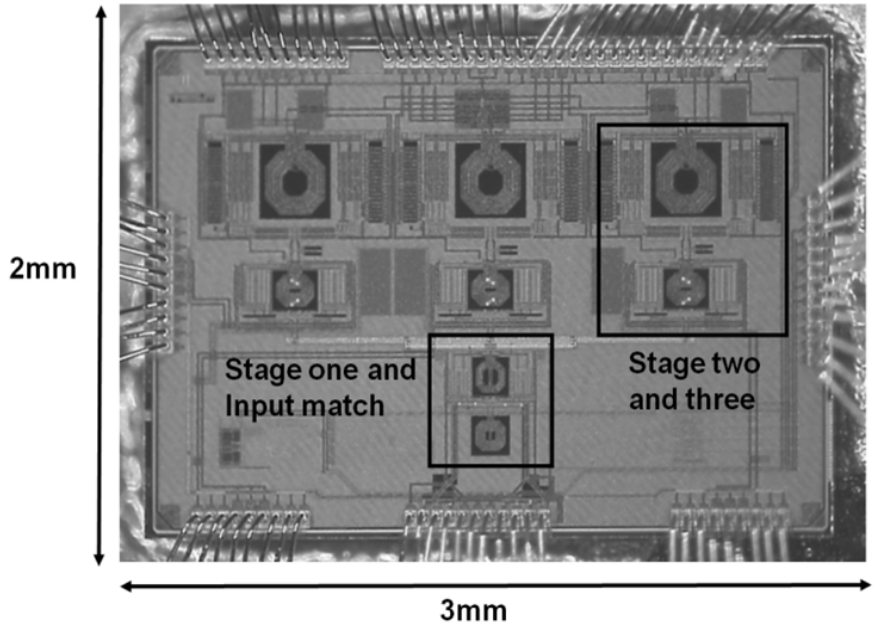


Figure 5.15: Die photograph of the PA with current-mode transformer based combiner.

Figures 5.16 and 5.17 show the high-level block diagrams of each PA. Each one has three differential stages with its corresponding power combiner. The first

stage is a 1.2 V pseudo-differential cascode amplifier with an inductive load tuned to 2.45 GHz. The second stage is a 3.3 V cascode amplifier with a thick oxide cascode device to improve the reliability. Its output is transformer-coupled to the input of the final stage to increase the common-mode stability. Figure 5.18 shows the simplified schematic of the final stage. It also utilizes a cascode structure with an inductor as the load for the distributed-LC combiner and a transformer for the current- mode transformer based combiner. The cascode gate bias is carefully set to make sure the Vds of the gm-stage is in the proper and reliable range. To improve the linearity of the PA, an auxiliary stage is used. The main and auxiliary devices are biased with an offset level to linearize the effective transconductance over a wide range of input voltages [10]. By utilizing this analog gm-linearization scheme, the P1dB of the transmitter is enhanced to be closer to Psat. In order to improve the linearity further, an open-loop digital pre-distortion technique is used.

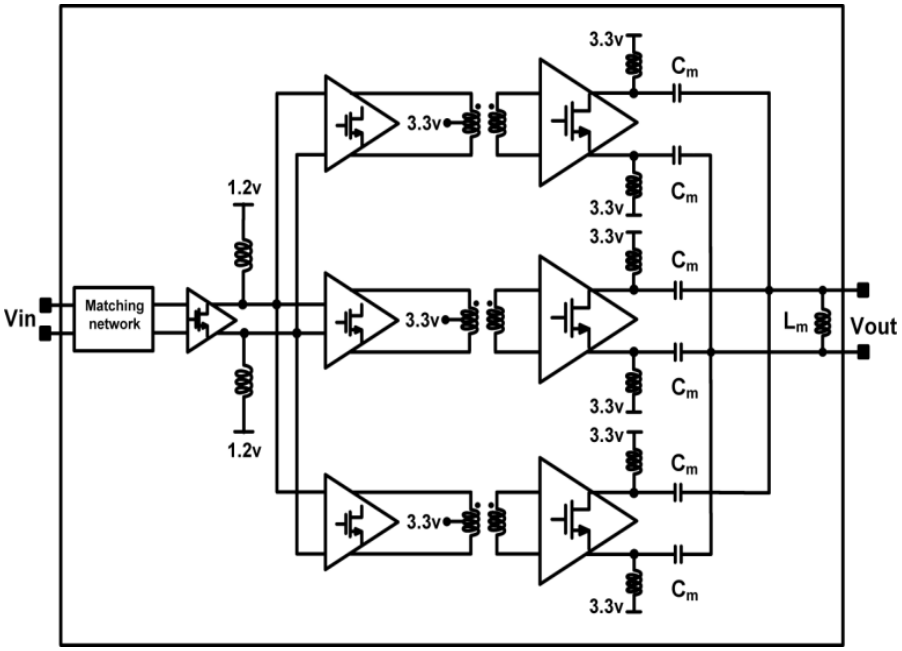


Figure 5.16: High-level block diagram of PA with distributed-LC combiner.

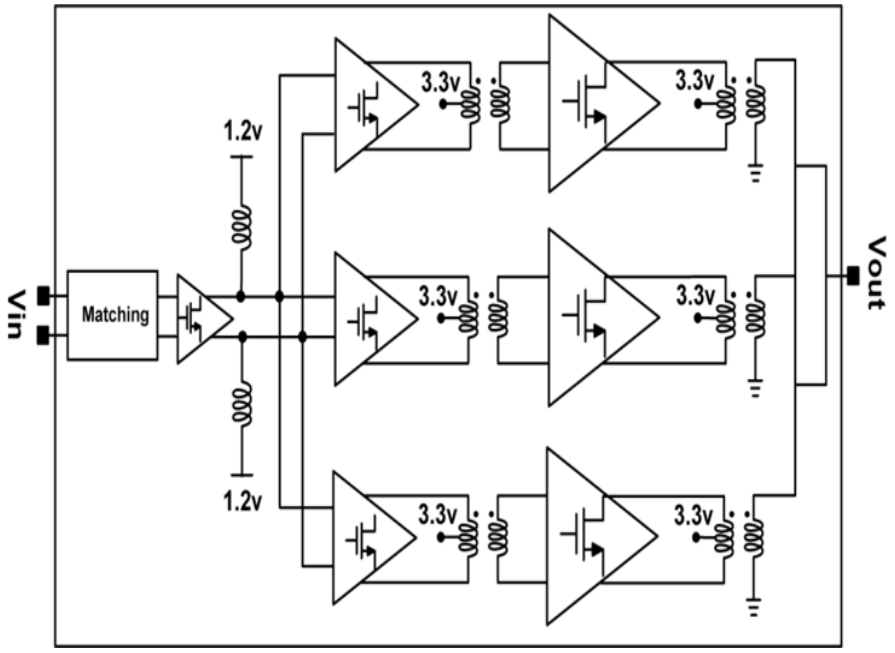


Figure 5.17: High-level block diagram of PA with current-mode transformer based combiner.

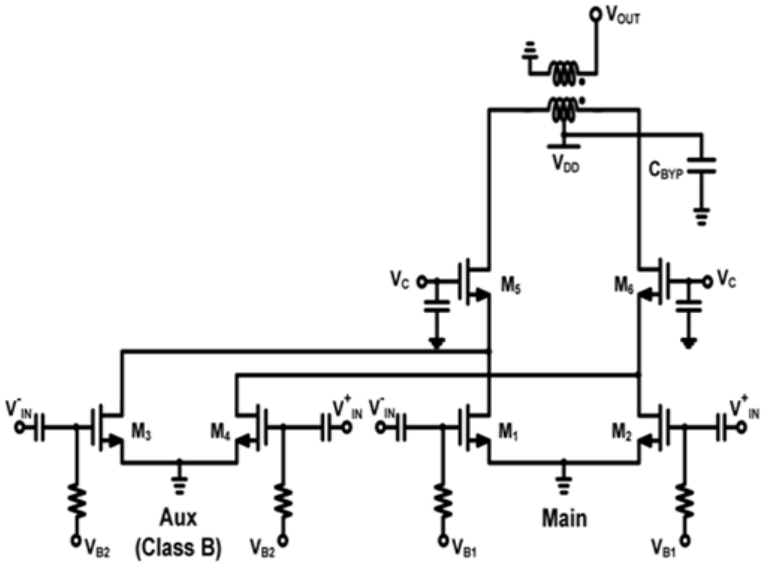


Figure 5.18: Simplified schematic of output stage.

5.5.1 Measurements

Figure 5.19 shows the measured S-parameters for the PA with distributed *LC* combiner. The PA achieves 32 dB small-signal gain at 2.45 GHz and better

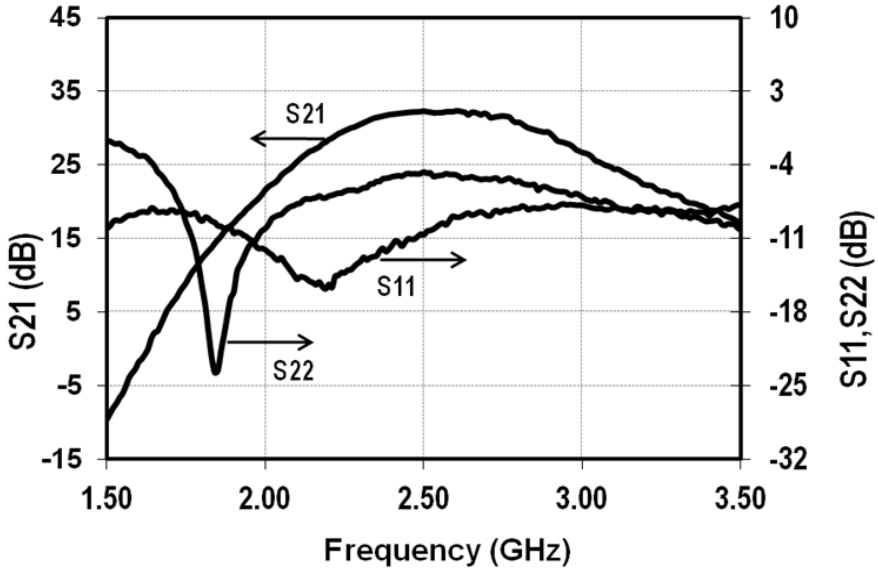


Figure 5.19: Measured S-parameters of PA with distributed-LC combiner.

than -8 dB input match from 1.5- GHz to 3.5 GHz. The BW of S21 is limited by the tuned tank at the output of first and second stages. In order to make the center frequency programmable, a bank of switched-capacitor networks is added to the output of first and second stages and the center frequency can be programmed by digital section of SoC. The simulated and measured output power and PAE vs. input power for a 2.45 GHz single tone are plotted in Fig. 5.20. At a supply of 3.3 V, the measured Psat is 31.5 dBm with peak PAE of 25%. The AM-AM and AM-PM distortions are shown in Fig. 5.21. By using the g_m-linearization technique, a P1dB of 27.5 dBm is achieved.

The phase distortion at P1dB point is approximately 2 degrees and the overall phase distortion is more than 10 degrees at Psat. This degree of amplitude and phase distortion can severely degrade the EVM at high average powers. To improve the linearity of the PA even further, an open-loop digital pre-distortion (DPD) technique is used. Figure 5.22 shows the measured EVM results, for a 64-QAM OFDM signal, with and without DPD. Without DPD the measured average power for -25 dB (-28 dB) EVM is 21.3 dBm (18-dBm) with 8.5% (5%) PAE and after applying DPD, an output power of 25.5 dBm (24.5 dBm) with 16% (14%) PAE and -25 dB (-28 dB) EVM is achieved. The output spectrum meets 802.11g

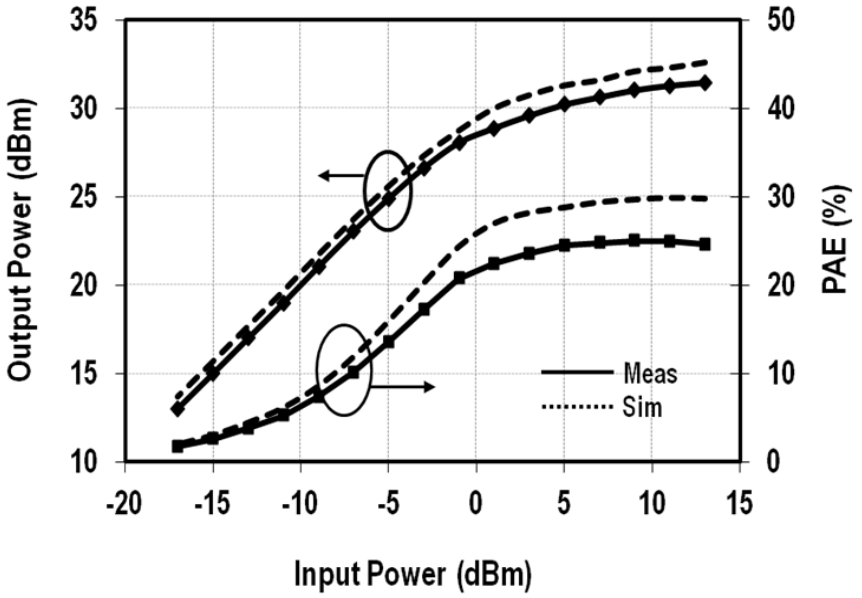


Figure 5.20: Simulated and measured output power and PAE of PA with distributed-LC combiner.

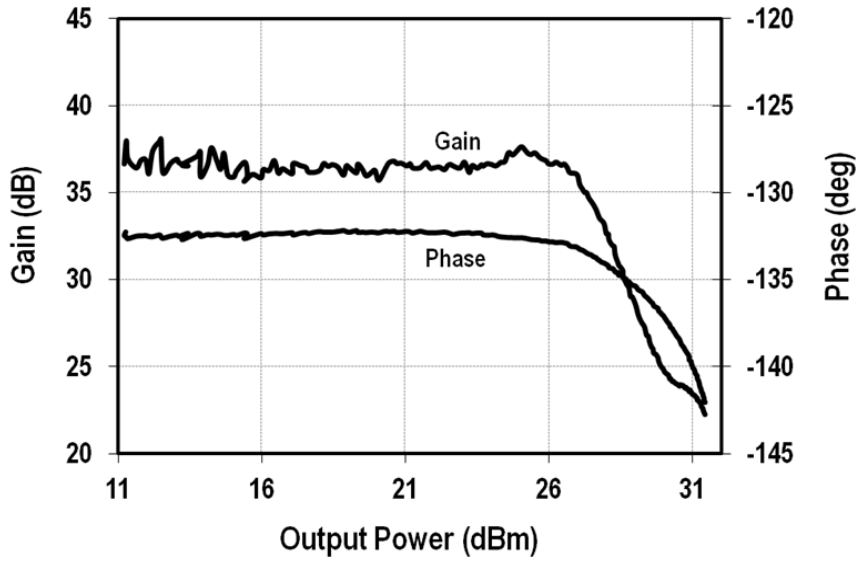


Figure 5.21: Measured AM-AM and AM-PM distortions of PA with distributed-LC combiner.

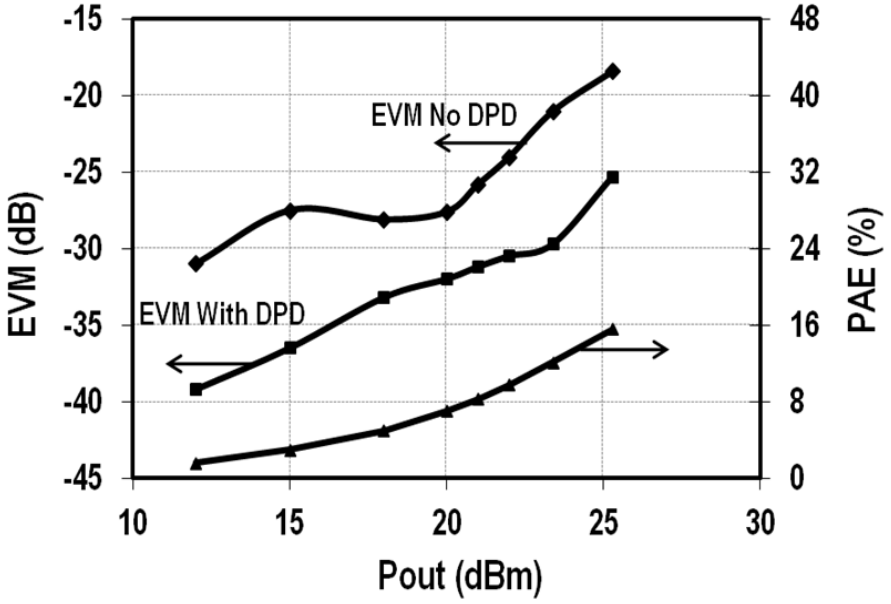


Figure 5.22: Measured EVM for a 64-QAM OFDM signal, with and without DPD of PA with distributed-LC combiner.

mask at 26 dBm output power.

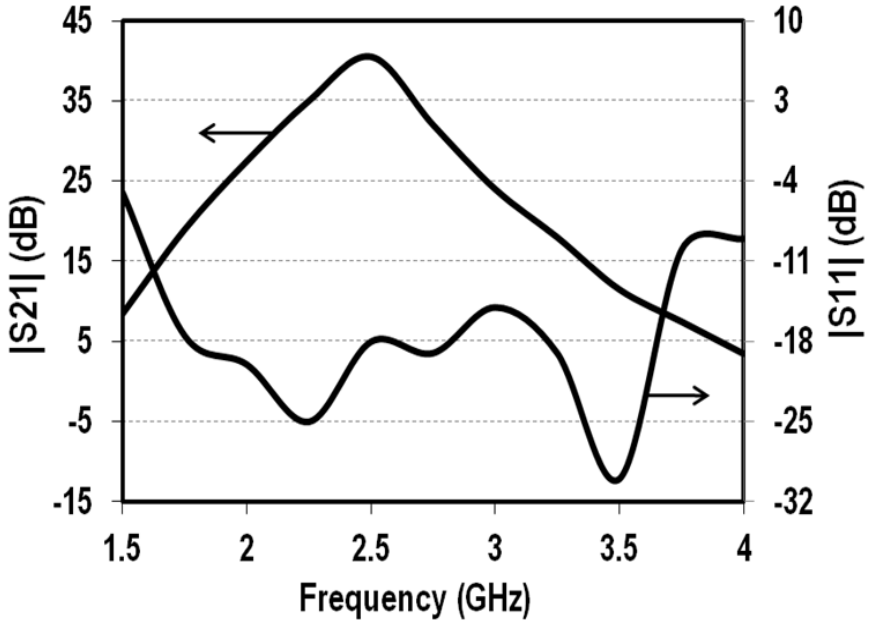


Figure 5.23: Measured S-parameters of PA with current-mode transformer based combiner.

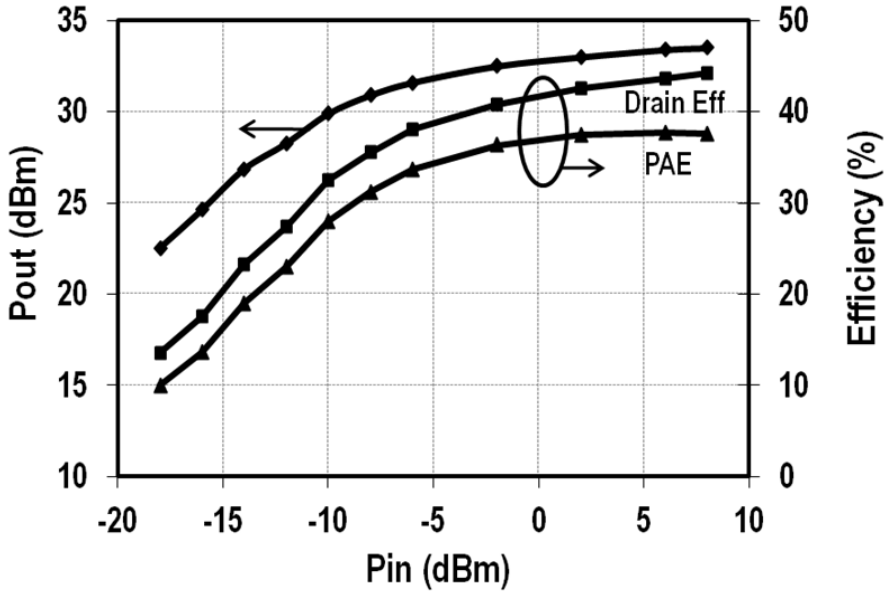


Figure 5.24: Measured output power, PAE and Drain efficiency of PA with current-mode transformer based combiner.

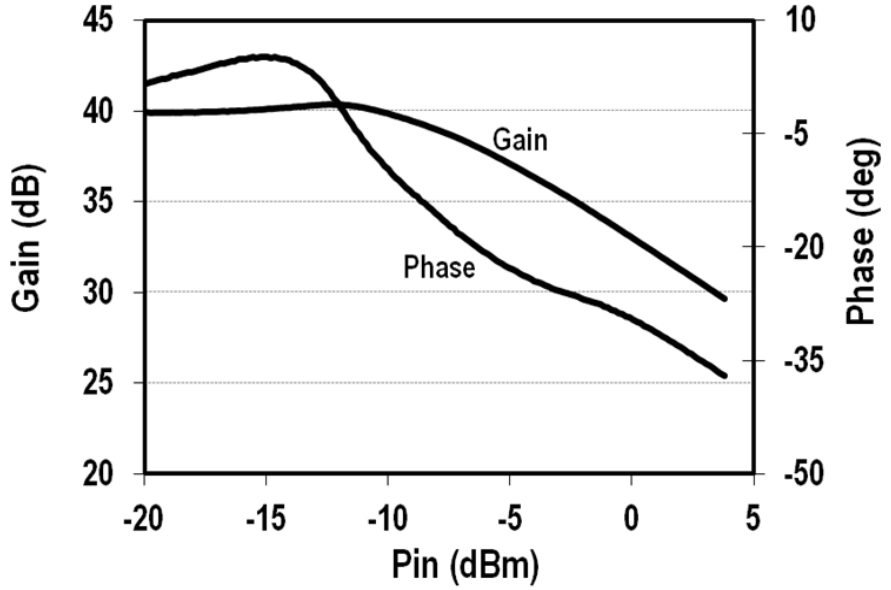


Figure 5.25: Measured AM-AM and AM-PM distortion of PA with current-mode transformer based combiner.

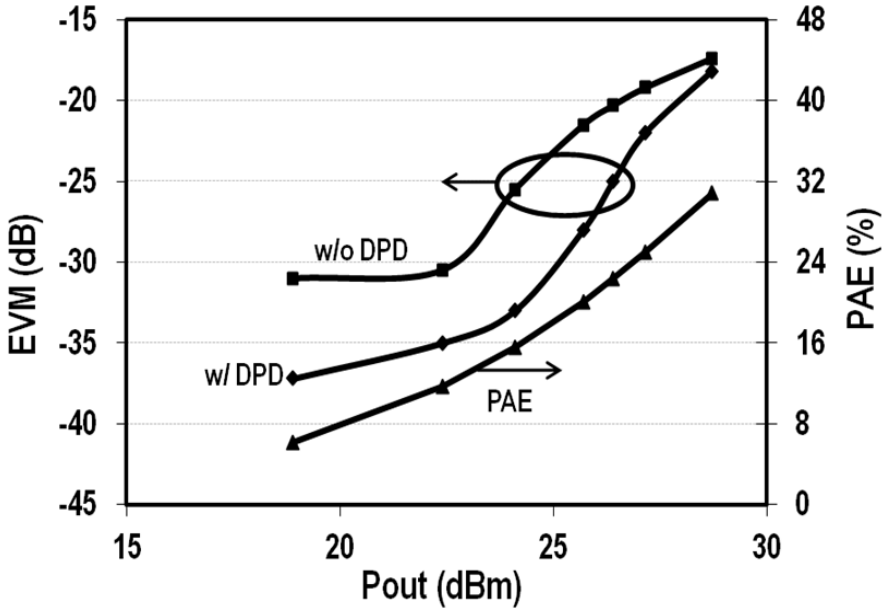


Figure 5.26: Measured EVM and PAE for an OFDM 54 Mb/s signal of PA with current-mode transformer based combiner.

Figure 5.23 shows the measured S-parameters for the PA with the current-mode transformer based combiner. The PA achieves 40 dB small-signal gain at 2.45 GHz and better than -10dB input match from 1.7 GHz to 3.7 GHz. Figure 5.24 shows the measured output power, PAE and drain efficiency for a 2.45 GHz single tone. At a supply of 3.3 V the measured Psat is 33.5 dBm with a peak PAE and drain efficiency of 37.6% and 44.2% respectively. The measurements show that the PA can deliver more than 30 dBm saturated power from 1.6 GHz to 3.6 GHz. The measured AM-AM and AM-PM distortion are plotted in Fig. 5.25. By using the gm-linearization technique, a P1dB of 30.5 dBm is achieved. The phase distortion at P1dB is approximately 14 degrees, which can be mostly compensated by digital pre-distortion. One can reduce the phase distortion by reducing the offset voltage between the main and auxiliary devices at the input of the final stage, at the expense of lower P1dB.

The measured EVM for a 54 Mb/s OFDM signal with and without digital pre-distortion (DPD) is shown in Fig. 5.26. Without DPD, the measured average power for -25 dB EVM is 23.9 dBm with 14% PAE and after applying DPD, an

output power of 26.4 dBm with 22% PAE and -25 dB EVM is achieved. The output spectrum meets the 802.11g mask at 27 dBm output power. Table I summarizes the performance of these two PAs which shows the current-mode transformer combiner PA has better performance for this power and frequency ranges which agrees with the analysis in Chapter 4.

Table 5.1: Performance Summary

	Dist LC	Current mode transf.	Ref[12]
Psat	$31.5dBm$	$33.5dBm$	$30.1dBm$
Small Signal Gain	$32dB$	$40dB$	$28dB$
Peak PAE	25%	37.6%	33%
Power at -25 dB EVM	$25.5dBm$	$26.4dBm$	$22.7dBm$
PAE at -25 dB EVM	16%	22%	12.4%
Power at -28 dB EVM	$24.5dBm$	$25.7dBm$	N/A
PAE at -28 dB EVM	14%	20%	N/A
Max Eff (5.5GHz)	30%	$NoData$	25.3%
Supply	$3.3V$	$3.3V$	$3.3V$
Technology	$65nCMOS$	$65nCMOS$	$90nCMOS$

5.6 Summary

In this chapter several power combining schemes were demonstrated. It is shown that due to lossy passive components in silicon, achieving a high power enhancement ratio from a single stage LC matching network or single transformer is challenging. However, distributed combiners have the potential of achieving high E in silicon. Two fully integrated linear power amplifiers using these combiners were fabricated in a 65-nm CMOS process and saturated powers of 31.5dBm and 33.5dBm were achieved. The measurement results show that the current-mode transformer based combiner PA had the best performance in the frequency and power ranges of interest. Chapter 5 is in full a reprint of the material as it appears in the IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 3, pp. 1247-1260, March 2013. The dissertation author is the primary investigator and author of this paper. Professor Lawrence Larson supervised the research which forms the basis for this paper.

Chapter 6

Conclusion

Explosive growth in WiFi-enabled products, as well as cost pressure from consumers, has forced manufactures to lower the cost and form factor of their solutions. One of the most effective way to provide such a solution is a high level of integration. Due to its VLSI capabilities, CMOS technology has shown to be a suitable process to integrate almost an entire system (Memory, DSP, analog, RF etc.) in a single chip. One of the few building blocks that has not yet been integrated is the power amplifier. Most commercial power amplifiers are fabricated in more expensive technologies like GaAs or SiGe due to their higher breakdown voltage, better linearity and higher efficiency.

Modern transmitters for wireless communications, including WiFi transmitters, employ spectrally efficient digital modulations such as OFDM with high peak-to-average ratio and require a very linear power amplifier. Deep-submicron CMOS technology exhibits much more nonlinearity comparing to other process like GaAs and SiGe, which makes designing high power and linear PAs in this process more challenging. In this dissertation several techniques have been proposed to design a high power, linear and reliable CMOS PA for WLAN applications.

This dissertation started with a summary of key transmitter system requirements of WLAN standard, and continued with a chapter on the fundamentals and limitations of power amplifiers. The output matching network is one of the key sections of a power amplifier that can have direct impact on the performance of the PA, such as efficiency and maximum output power. In Chapter 3, two commonly

used matching networks, LC-matching network and transformer-based matching network, are discussed and their advantages and disadvantages are compared. It is shown that for a practical range of power enhancement ratio (E), a transformer-based matching network exhibits higher efficiency.

In Chapter 4, a fully integrated, 2x2 dual band 802.11n power amplifier implemented in a standard 65nm CMOS process was presented. A low-loss on-chip balun is used to convert the differential output to single-ended, while providing an optimum load to the PA. Multiple linearization schemes (digital pre-distortion and g_m-linearization) are used to linearize the PA, to transmit a higher output power and obtain a higher efficiency while satisfying the standard specifications for both 2.4GHz and 5GHz bands. In addition, a gain boost technique has been used to increase the linear gain especially for 5GHz band. The reliability of the PAs are evaluated with accelerated aging tests under extreme conditions, with no failures observed.

In Chapter 3, we showed that for a large E, if one wants to use a single stage matching network, the inductance value will be impractically small, the loss of the network will be high, the loss of the network will be very sensitive to parasitics on the low impedance side and designing the PA driver will be very challenging. Power combining techniques are suggested as one practical solution. Chapter 5 discusses multiple traditional power combining techniques such as Wilkinson combiners and voltage-mode transformer-based combiners and proposes two new power combining schemes, distributed-LC and current-mode transformer-based combiners. Two fully integrated linear PAs using these combiners were fabricated in a 65-nm CMOS process and saturated powers of 31.5 and 33.5 dBm were achieved. The measurement results show that the current-mode transformer-based combiner PA had the best performance in the frequency and power ranges of interest.

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