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A 16-Channel Wireless Neural Interfacing SoC
With RF-powered Energy-Replenishing Adiabatic Stimulation

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Abstract

This paper presents a fully-integrated 16-channel wireless neural interfacing SoC that employs an adiabatic stimulator powered directly from a 190-MHz on-chip antenna to eliminate bulky external components while simultaneously avoiding rectifier and regulator losses. Using a charge replenishing architecture, the stimulator outputs up to 145-µA, while achieving a 63.1% charge replenishing ratio and a stimulation efficiency factor of 6.0. Analog front-ends (AFEs) and telemetry circuitry are also included.

Introduction

Neural sensing and actuating platforms require tightly integrated low-power recording and stimulation ICs to achieve high spatiotemporal resolution in tight anatomic environments. Most recent neural interfacing devices, however, still rely on bulky external components such as antennas, capacitors, or inductors for system functionality and/or efficiency improvements [1], potentially limiting their utility when ultra-miniaturized integration is required.

To overcome this challenge, this paper presents a neural interfacing SoC that incorporates all functionality on a chip: an on-chip antenna, efficient adiabatic stimulation drivers, AFEs, an ADC, and wireless power and data telemetry. A block diagram of the proposed SoC is shown in Fig. 1. As a 3x3mm^2 planar microsystem with 16 on-chip quad-segmented electrodes, the chip can be used for cortical applications, much like µECoG arrays [1], as most of the curvilinear features of the cortex have small radii of curvature, enabling tight cortical contact.

RF-powered Adiabatic Stimulation

Adiabatic stimulators are desirable in energy-constrained systems, yet have not been demonstrated with both high efficiency and full integration, as most prior art relies on bulky external components such as capacitors [2,3] or inductors [4], or alternatively cascade several power converters, each with substantial loss mechanisms, in order to synthesize the required waveforms [5]. In contrast, the stimulator in [6] relies on comparison at the RF frequency so that it is limited to applications with low frequency (< 10 MHz) RF input. In this work, power for adiabatic charging is synthesized directly from an on-chip LC tank resonating at 190 MHz. Importantly, the proposed adiabatic stimulator recycles the charged stored on the electrode capacitance and delivers it back to V_{DD} in order to further increase energy savings as shown in Fig. 2.

The core blocks of the adiabatic stimulator are shown in Fig. 3. In the stimulation current controller (Fig. 3 (a) and (b)), a single current source is used for both positive and negative phases. The positive side current is controlled by an amplifier to maintain the common-mode voltage of the stimulating electrodes and the entire chip to be same, even during stimulation. For the energy replenishment phase, the charged electrodes serve as a power source to provide current back to the system power supply until the voltage rail decreases to V_{DD} (=0.8 V). Any residual charge on the electrodes is then cancelled out by shorting.

The adiabatic supply voltage generator shown in Fig. 3 (c) is powered by an LC tank resonating at 190MHz, and produces stimulation power supplies V_{DD-STM} and V_{SS-STM} according to the stimulation electrode voltages V_{STM-U} and V_{STM-L}. The switches in each rectifier unit fold or unfold its own stage according to V_{STM-U} and V_{STM-L}. Floating bulk devices provided in the employed SOI process are utilized as necessary. This direct RF-to-stimulation-supply converter can produce wider voltage rails, measured up to 9 times V_{DD} for increasing the maximum deliverable charge per stimulation phase. The generated stimulation pulses are relayed to electrodes through a high-voltage tolerant switch matrix.

Measurement Results

Fig. 4 (a) shows measured 120-µA differential tri-phasic stimulation waveforms and the corresponding currents through RC-modeled electrodes (15nF+900Ω in series). V_{DD-STM} and V_{SS-STM} follow V_{STM-U} and V_{STM-L} closely, and can reach up to -3.3 V and + 3.9 V.

The supply current from the stimulator V_{DD} is shown in Fig. 4 (b). The negative current indicates energy is being replenished back to V_{DD}. As the computed cumulative charge shows, more than 63% of charge is returned. As shown in Fig. 4 (c), the rectified V_{DD} increases during the energy-replenishing phase. The stimulator was further validated across several representative electrode types: 250x250 µm^2 Pt electrodes [7] in Fig. 4 (d) and purely resistive electrodes of 50 kΩ in Fig. 4 (e).

The proposed stimulator has two distinct advantages. First, the adiabatic stimulation supplies are directly generated from RF while conventional approaches require cascade power conditioning circuits, large external passives, or both, leading to lower overall efficiency. Second, it replenishes energy from the charged electrodes, resulting in more energy-efficient operation. For benchmarking the stimulator performance, a stimulation efficiency factor (SEF, Fig. 5) is employed which compares the proposed stimulator to an ideal stimulator operating with current sources from constant voltage rails set at the min/max of the required stimulation voltage compliance. The proposed adiabatic stimulator achieves a measured SEF of 5 excluding replenished energy, and SEF of 6 with estimated replenished energy, which is more than 3 times better than prior art.

The SoC also features neural recording capabilities that include a variable-gain AFE and a time-multiplexed SAR ADC. A schematic of the front-end, along with measured results are shown in Fig. 6. A unity gain buffer is used to average the common mode and drive the reference of the second stage of each channel.

The chip was fabricated in a 0.18-µm CMOS SOI process, and a die photo is shown in Fig. 7. Table I summarizes and compares with other state-of-the-art adiabatic stimulators. The chip operation was further validated for stimulation and recording under in vivo (mice cortical surface) physiological conditions, of which characterization will be presented elsewhere.

References

[1] R. Muller *et al.*, *ISSCC Dig. Tech. Papers*, pp. 412-413, 2014.

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[3] H-M. Lee et al., *ISSCC Dig. Tech. Papers*, pp. 414-415, 2014.

[4] S.K. Arfin and R. Sarpeshkar, *IEEE TBioCAS*, **6**(1), Feb. 2012.

[5] D. Yeager *et al.*, *Dig. Symp. VLSI Circuits*, 2014.

[6] Çilingiroğlu and İpek, *IEEE TBioCAS*, **6**(4), Aug. 2013.

[7] Franks *et al.*, *IEEE TBME*, **52**(7), Jul. 2005.

Fig. 1. Concept of fully integrated silicon neural interface microsystem with embedded electrodes and RF inductive power and data telemetry. Block diagram with functional components.
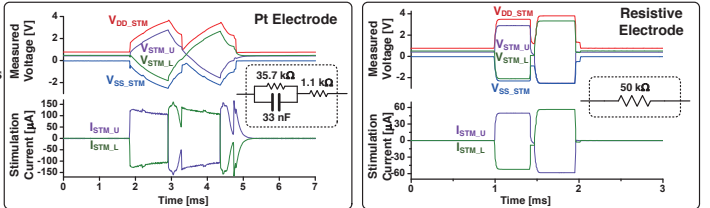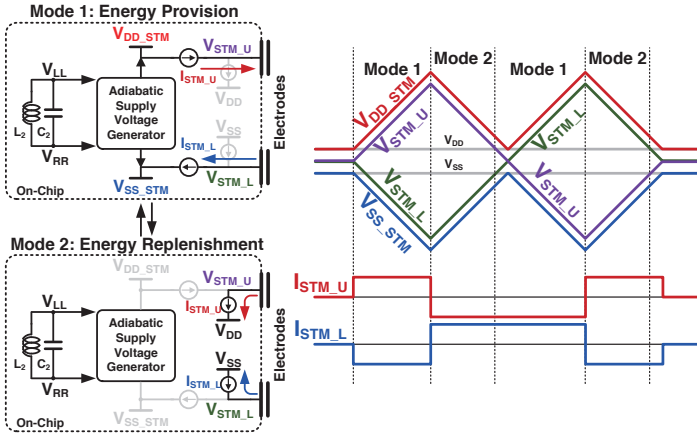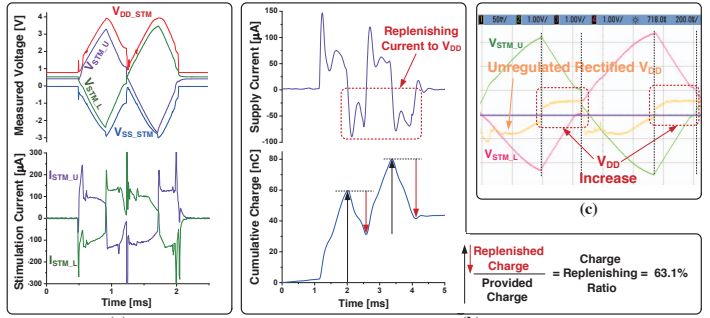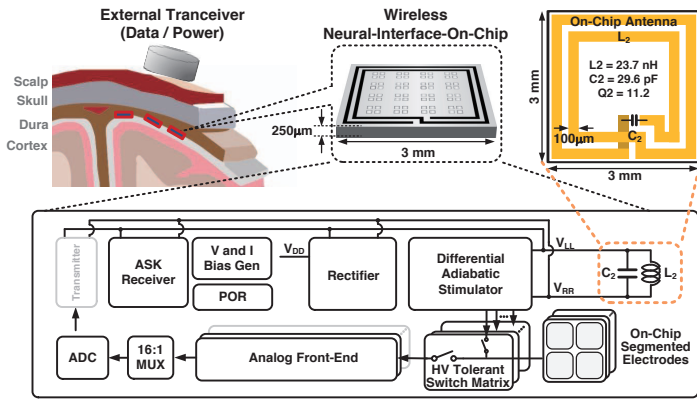

Fig. 2. Principle and operation of energy-replenishing differential stimulator.

Fig. 3. Stimulation circuits. (a) Current controller circuit. (b) Simplified diagram, and principle of energy replenishment. (c) RF-powered adiabatic voltage supply generator circuit.

Fig. 4. (a) Measured stimulation waveforms. (b) Supply current and accumulated charge. (c) Change of unregulated rectified V_{DD} during stimulation. Measured waveforms with (d) 250×250 μm^2 Pt electrode and (e) resistive electrode models.

Fig. 5. Energy delivery, loss, and replenishment for different stimulator topologies. Stimulation Efficiency Factor (SEF) as a proposed figure of merit.

$$SEF = \frac{E_{STIM\_Ideal\_Current\_Source}}{E_{STIM}}$$

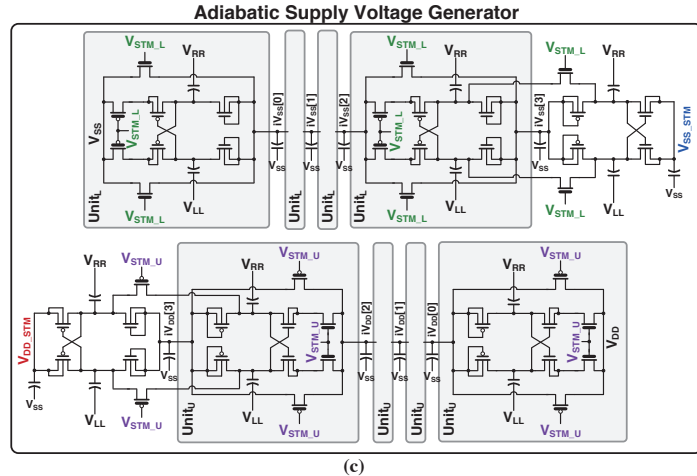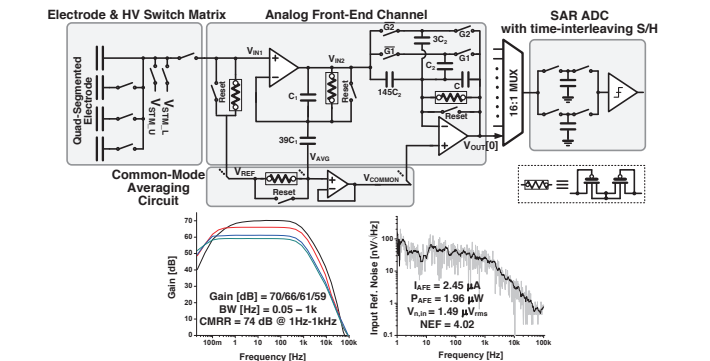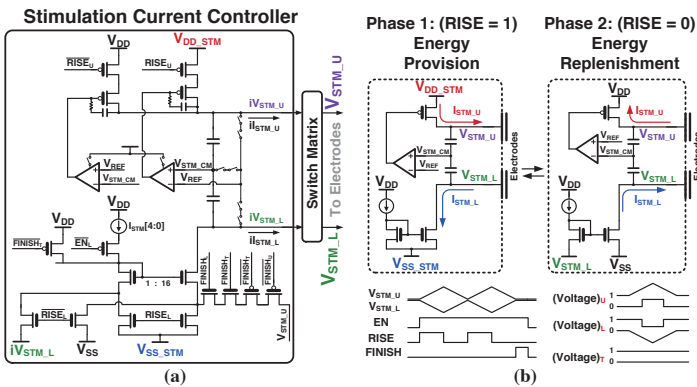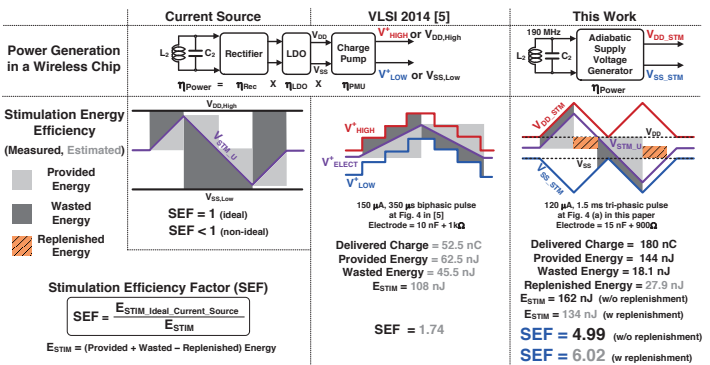$E_{STIM} = $ (Provided + Wasted − Replenished) Energy

Fig. 6. AFEs and time-interleaved S/H multiplexed SAR ADC. Simplified circuit diagram, and AFE characterization.

Fig. 7. Chip micrograph.

Table I: Comparison with state-of-the-art adiabatic stimulators

	This Work	TBioCAS 2011 Kelly [2]	TBioCAS 2012 Arfin [4]	TBioCAS 2013 Çilingiroğlu [6]	VLSI 2014 Yeager [5]
Technology [μm]	0.18 SOI	1.5	0.35	0.18	0.065
Source of Stimulation Power	190 MHz On-Chip LC	125 kHz External LC	V_{DD}	5 MHz External LC	V_{DD}
Supply Voltage [V]	0.8	±1.75	3.3	N/A	1
Stimulation Supply Voltage Range [V]	-3.3 ~ +3.9 (9 V_{DD})	±1.75 (1 V_{DD})	1 V_{DD}	N/A	0 ~ 8.7 (8.7 V_{DD})
Max. Current [μA]	145	400	450	140	>500
Wireless Power Transfer	Yes	Yes	No	Yes	No
External Components	None	LC tank, Capacitors, Electrodes	Inductor, Electrodes	LC tank, Electrodes	Electrodes
Charge Replenishing Ratio	63.1%	N/A	N/A	N/A	N/A
SEF	4.99 (w/o replenishment) 6.02[†] (w/ replenishment)	2.13 ~ 2.94[‡]	N/A	N/A	1.74[‡]
Electrode Model	4nF+250Ω, 15nF+900Ω, 50kΩ, Pt (35nF/33nF+1.1kΩ)	980nF+1.15kΩ	930nF+1kΩ	5.5nF/6kΩ+4kΩ	10nF+1kΩ

[†]Estimated, [‡]Estimated based on the reported figures and numbers