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Development of FlexTrate^{TM} and Demonstration of Flexible Heterogeneously Integrated Low Form-factor Wireless Multi-channel Surface Electromyography (sEMG) Device

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy

in Electrical and Computer Engineering

by

Arsalan Alam

2021

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2021

ABSTRACT OF THE DISSERTATION

Development of FlexTrate^{TM} and Demonstration of Flexible Heterogeneously Integrated Low Form-factor Wireless Multi-channel Surface Electromyography (sEMG) Device

by

Arsalan Alam

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2021

Professor Subramanian Srikantes Iyer, Chair

Leading-edge implantable applications such as neural implanted prosthetics and next-generation Internet of Things (IoT) devices require the integration of high performance and low power logic, memory and sensors at high interconnect density which is not possible using conventional printed flexible electronics. As flexible applications mature, there will be a demand that they are "smart," which will require leading edge CMOS and RF electronics, advanced sensors, and power management. There is a need to develop a robust and flexible electronics packaging platform that will enable the unrestricted integration of high-performance, state-of-the-art components (processors, memories, sensors, data transmitters and receivers, power sources etc.) on biocompatible, flexible substrates with the ability to miniaturize, interconnect at high density with acceptable reliability, and scale-up in manufacturing at economical and cost-effective price points.

Considering all the above requirements, in this work, the development of a highly flexible and reliable heterogeneous integration platform with fine interconnect pitch (≤ 40 µm) called FlexTrate^{TM} is investigated. The fabrication and assembly processes necessary for such a platform are developed. FlexTrate^{TM} is based on a die-first flexible Fan-Out Wafer-Level Packaging (FOWLP) approach where Polydimethylsiloxane (PDMS) is used as a molding compound to embed the heterogeneous dies and integrate them with mechanically robust vertically corrugated interconnects at 20-40 µm pad pitches without the use of solder. FlexTrate^{TM} is demonstrated to be bendable to 1 mm bending radius for thousands of bending cycles with minimal degradation in the system's electrical performance. The benefits to system performance and flexibility of FlexTrate^{TM}-style integration are highlighted through three demonstrations: 200 dies integrated at 40 µm pad pitches, a foldable display, and a wearable biosensing system in the form of wireless multi-channel surface electromyography (sEMG) system. The sEMG system can be attached to the skin to record quality muscle signals through dry electrodes and can transmit data to a computer or smartphone via Bluetooth Low Energy (BLE). The ability to acquire muscle signals through our device in a mobile setting is critical for the study of many muscular physiological phenomena and disorders.

The dissertation of Arsalan Alam is approved.

Sam Emaminejad

Dwight Christopher Streit

Michael Selvan Joseph

Subramanian Srikantes Iyer, Committee Chair

University of California, Los Angeles

2021

DEDICATION

To my family…

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VITA

2007-2011	Bachelor of Technology in Electronics Engineering,
	Aligarh Muslim University
2013-2015	Master of Technology in Electronics Engineering,
	Indian Institute of Technology, Roorkee

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1. Introduction

1.1 Conventional flexible electronics

In the past decades, work in flexible devices may be divided into three categories: (1) organic semiconductors that are deposited on flexible substrates in sheet-level processing or roll-to-roll processing [1-3]; (2) Thin-Film Transistor (TFT) fabrication on flexible substrates [4, 5]; and (3) so-called transfer technologies that allow the integration of an extremely thin, single crystal, inorganic semiconductor layer on flexible substrates, such as Silicon-On-Insulator (SOI) and III–V semiconductors on Si [6, 7]. Although the performance of the organic semiconductors has improved significantly recently [8, 9], the performance of inorganic single crystal semiconductors represented by Si and III-V compounds has not been achieved by organic semiconductors.

On the other hand, Flexible Hybrid Electronics (FHE) combine the flexibility of flexible substrates with the performance of single crystal inorganic semiconductor devices to create a new category of electronics [10, 11]. Traditional rigid/flex packages enable the integration of thick Si dies on flexible substrates [12, 13]. These technologies are not based on Wafer-Level Packaging (WLP), and the flexibility is limited by their rigid substrates or large packaged chips. More recently, to enhance the flexibility of the rigid single crystal semiconductors, ultra-thin dies are mounted on flexible substrates [14, 15]. This is because such thinned dies can be more flexible and can conform to curved profiles. However, ultra-thin dies are very sensitive to applied stresses [14] by which both the performance degradation and property deviation would be induced due to die thinning process and bending to small bending radii. Lee et al. have reported that the retention time of

thinned DRAM (Dynamic Random-Access Memory) having planar capacitors is shortened when the die thickness is less than 50 μm [16].

While recent progress in the field of flexible electronics has been impressive, it is still not easy to integrate high-performance electronics which require fine pad and interconnect pitches of < 100 μm while retaining the flexibility of the overall system.

1.2 Objective of this work

Leading-edge implantable applications such as neural implanted prosthetics and next-generation Internet of Things (IoT) devices require the integration of high performance and low power logic, memory and sensors at high interconnect density which is not possible using conventional printed flexible electronics. As flexible applications mature, there will be a demand that they are "smart," which will require leading edge CMOS and RF electronics, advanced sensors, and power management. There is a need to develop a robust and flexible electronics packaging platform that will enable the unrestricted integration of high-performance, state-of-the-art components (processors, memories, sensors, data transmitters and receivers, power sources etc.) on biocompatible, flexible substrates with the ability to miniaturize, interconnect at high density with acceptable reliability, and scale-up in manufacturing at economical and cost-effective price points. Considering all the above requirements, in this work, the development of a highly flexible and reliable heterogeneous integration platform with fine interconnect pitch (≤ 40 μm) called FlexTrate™ is investigated. The fabrication and assembly processes necessary for such a platform are developed. The benefits to system performance and flexibility of FlexTrate™-style integration are highlighted through three demonstrations: 200 dies integrated at 40 μm pad pitches, a foldable

display, and a wearable biosensing system in the form of wireless multi-channel surface electromyography (sEMG) system [17-26].

1.3. FlexTrate^{TM} technology

A new approach of making flexible systems is demonstrated called "FlexTrate^{TM}" that is based on die-first flexible Fan-Out Wafer-Level Packaging (FOWLP) technique. FlexTrate^{TM} allows solderless heterogeneous integration of bare dies at ≤ 40 μm pad pitches not achievable using conventional flexible technologies. FlexTrate^{TM} is bendable to 1 mm bending radius for over thousands of bending cycles. Through FlexTrate^{TM}, we can target next generation wearable and implantable applications that require high-performance flexible systems, such as multi-channel sEMG system, optogenetics for neural implants, and so on.

1.3.1 Technology description

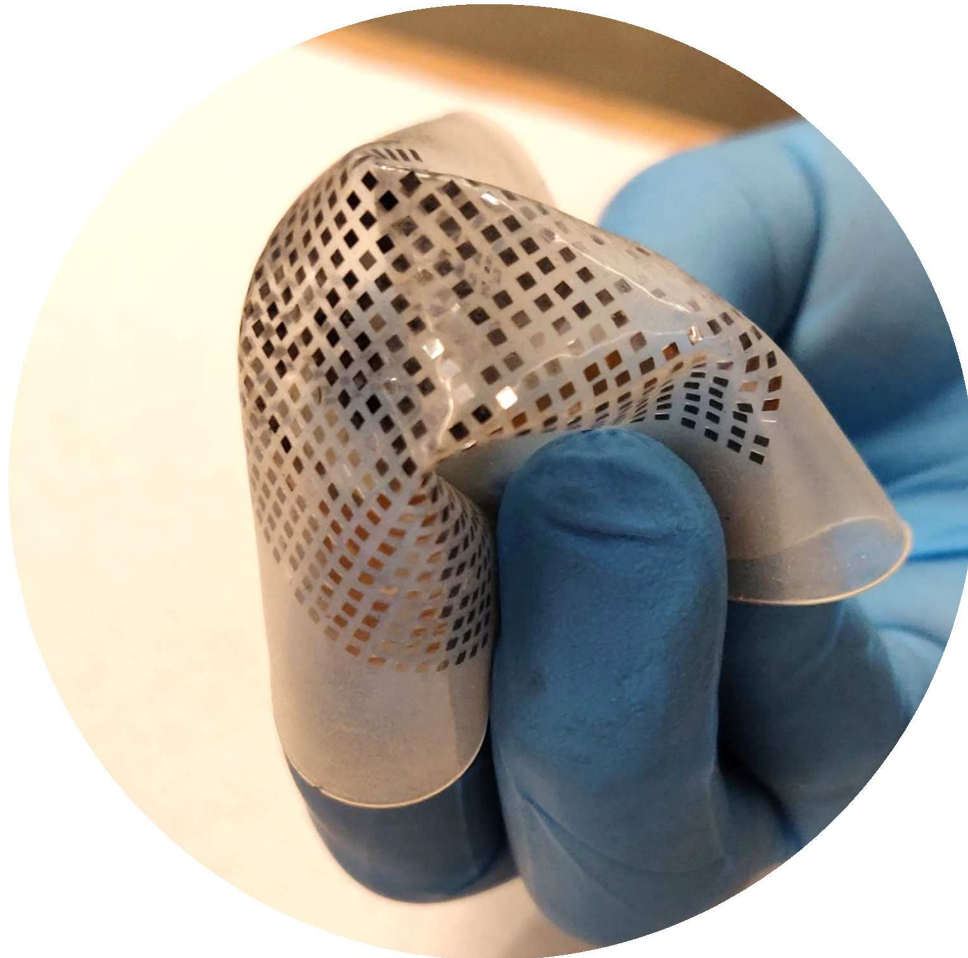


Figure 1. 1. Image of the flexible FlexTrate^{TM} platform with embedded Si dies.

In the FlexTrate^{TM} approach, the rigid dies are embedded in a flexible polymeric substrate that is fabricated at the wafer level using an advanced die-first FOWLP technology, as shown in Fig. 1.1. FOWLP has become a mainstream packaging technology because of its numerous advantages over conventional packaging techniques such as Wafer-Level Chip-Scale Packaging (WLCSP) and Flip-Chip Ball Grid Array packaging (FCBGA) [27, 28]. FOWLP allows heterogeneous integration and provides good electrical and thermal performances, high density of I/Os, compatibility with 3D integration, low package profile, and low cost. It also eliminates the need for wafer bumping, reflow for flip chip, underfill and flux cleaning. FOWLP is expected to reduce

package sizes, shorten inter-chip wirings by eliminating laminates, and integrate dies in rigid Epoxy Mold Compounds (EMCs) [29, 30]. Several Redistribution Layer (RDL)-first approaches with and without wafer-level processing have been reported for rigid [31] and flexible [32, 33] device system integration. Compared to RDL-first FOWLP with die/flip-chip bonding processes, die-first FOWLP is more cost-effective [34]. If the die shift issues in die-first FOWLP are mitigated, the production yield would be further increased, leading to drastic cost reduction. The most significant advantage of the die-first FOWLP is that wire bonding, printable wiring, and solder bumping are not required for connecting the neighboring dies, and there are no additional packaging processes due to the embedded structure [35, 36]. In our embodiment of this approach, the high flexibility is achieved by the unique structure of FlexTrate™, consisting of the hard and soft segments analogous to how a bicycle chain is flexible despite rigid chain components. The dies themselves do not bend, whereas the polymer regions between the dies are bent, similar to the joints in a bicycle chain. Heterogeneous dies are embedded in a flexible substrate and electrically connected with high-density interconnects formed via wafer-level processing. Similar structures using rigid device islands interconnected with horseshoe wirings have been developed for stretchable electronics [32, 33, 37], but the fabrication concept of these systems is considerably different from FlexTrate™ which is based on scalable WLP using embedded Si dies that are assembled in a face-down configuration. Landesberger et al. [38] have presented a similar approach to our FOWLP-based FlexTrate™, although they employ ultra-thin Si dies having equalized die thicknesses, which are bonded in a face-up configuration. Due to the advanced die-first FOWLP approach, the FlexTrate™ process enables scalable integration of heterogeneous dies of various thicknesses and much tighter interconnect formation than conventional rigid/flex packages. In addition, fine-pitch interconnects can be formed at the wafer level. Presently, inkjet

printing can draw very fine wirings in parallel, but the wire thicknesses are limited [39]. FlexTrate™ with inorganic single crystal semiconductor dies can realize highly integrated flexible device systems without using low-performance organic semiconductors, ultra-thin devices/dies, or colloid/paste based wirings.

1.4 Comparison with conventional technologies

FlexTrate™ leverages the advantages of the die first FOWLP technique to flexible electronics. The integration of small bare dies increases the flexibility of the FlexTrate™ platform. Here we discuss the advantages and limitations of FlexTrate™ over conventional technologies.

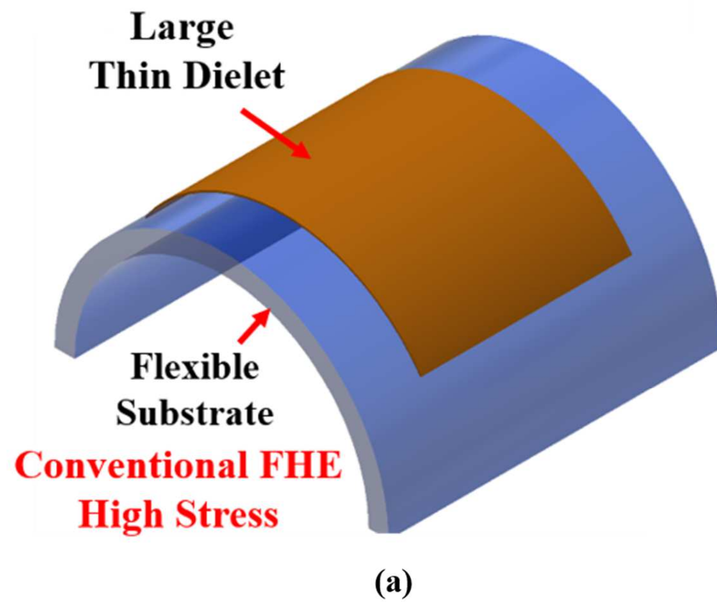
1.4.1 Advantages

Some of the key merits of the FlexTrate™ technology, and a comparison to the approaches used in rigid FOWLP, conventional FHE, and flexible PCB, are listed below.

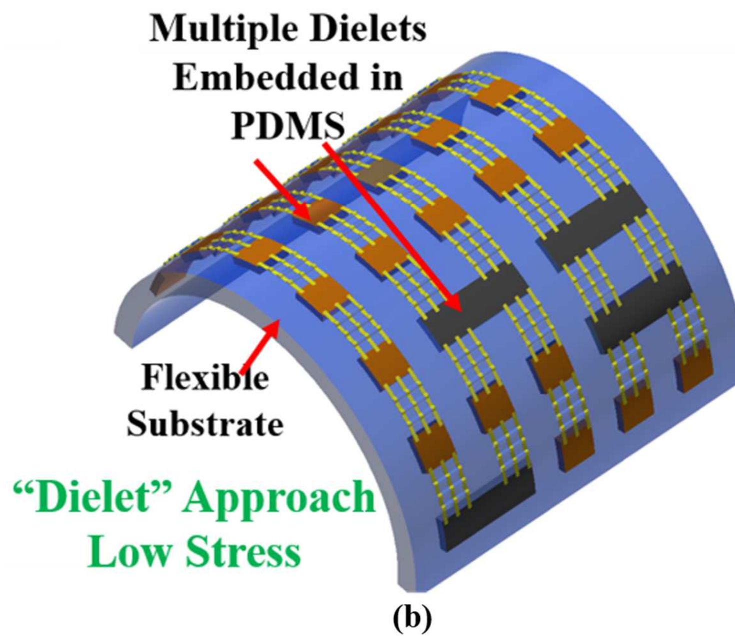
Properties	Epoxy Mold Compound (EMC)	PDMS (MDX4-4210)	Advantage
Elongation at break	< 1 %	500 %	Flexibility
Curing T	> 150 °C	25 °C- 80 °C	Low die shift
Glass transition T (T_g)	165 °C	-120 °C	Room T cure
Young's modulus	22 GPa	0.5 MPa	Low thermo-mechanical stress
Biocompatibility	No	Yes	Implantable

Table 1. 1. Properties of biocompatible PDMS used in FlexTrate™ and non-biocompatible rigid epoxy used in conventional FOWLP.

- Rigid FOWLP integration has four major challenges: (1) the high glass transition temperature (T_g) of rigid molding compound used in wafer reconstitution, (2) the coefficient of thermal expansion (CTE) mismatch with respect to Si dies, (3) high drag forces from the mold reflow during mold compression process, and (4) mold shrinkage during the curing process [38]. These process challenges cause substrate warpage, poor die co-planarity with respect to the molding compound (die pop-up), and, most importantly, die shift from the original placement position [29, 40, 41]. The state-of-the-art die shifts are of the order of 10-20 μm [40]. These large die shifts result in large overlay tolerances for the interconnects that are used to connect the dies, which in turn limits the finest interconnect pitch to ~3X the worst-case die shift (i.e., 40-80 μm). To overcome the above mentioned FOWLP challenges, a biocompatible molding compound is chosen, namely PDMS based "Silastic MDX4-4210", which has significantly improved thermo-mechanical properties compared to rigid epoxy-based molding compounds, as shown in Table 1.1 Although PDMS has significantly higher CTE mismatch with respect to both Si and Cu (300 vs. 3 and 17 ppm/K, respectively) when compared to rigid molding compounds (7.5 ppm/K), the die shift is reduced because of two main reasons: (1) since the T_g of PDMS is -120 □, it can be cured at room temperature, minimizing cure shrinkage after curing; (2) PDMS exhibits four orders of magnitude lower Young's modulus as compared to rigid molding compounds, and the drag force during mold compression and flow is, therefore, not large enough to cause significant die shift. As such, die co-planarity and die tilt of < 1 μm and maximum die shift of < 8 μm across a 100 mm wafer have been demonstrated on FlexTrate^{TM}.



(a)



(b)

Figure 1. 2. (a) Schematic of a large, thin die bonded on a flexible substrate in the conventional FHE approach, where the die undergoes high stress upon bending to small bending radii, (b) schematic of the "dielet" approach in FlexTrate^{TM}, showing multiple dies connected at fine interconnect pitch.

	Conventional FHE	FlexTrate™
Die thickness	Thin (< 50 µm)	100-300 µm
Interconnect	Printed	Electroplated Cu
Interconnect pad pitch	Coarse (> 100 µm)	Fine (≤ 40µm)
Die bonding	High T	Embedded, Room T.

Table 1. 2. Advantages of FlexTrate™ over conventional FHE.

- To enhance the flexibility of conventional FHE, ultra-thin dies, typically less than 20 µm, are mounted on flexible substrates [11] because such thinned dies can conform to curved surfaces. However, there are three major drawbacks to this approach. First, ultra-thin dies are susceptible to the stress-induced device variation and circuit performance degradation. For example, Lee et al. have reported that the retention time of thinned DRAM having planar capacitors is reduced when the die thickness is 50 µm or less by more than 50% [16]. Second, the potential manufacturability of products is dependent on achieving high yield after two processes: (1) wafer thinning from bulk inorganic substrates and (2) handling of ultra-thin dies using flip-chip techniques [42, 43]. Third, and most importantly, the printed interconnects on flexible substrates have coarse pitches, typically in the range of hundreds of microns, which limits the integration of high-performance logic/memory dies requiring high number of I/Os. In addition, either wire bonding/ball bumping is typically used to create connections to communicate with other integrated chips, which does not allow for a high number of I/Os needed for high-performance logic and memory dies [44], and also limits the flexibility of the entire assembly [45]. On the other hand,

FlexTrate™ has various benefits in terms of enabling heterogeneous integration, form factor reduction, and overall higher performance. Fig. 1.2 shows the schematic of conventional FHE approach and the FlexTrate™ approach. The advantages of FlexTrate™ vs. conventional FHE techniques are summarized in Table 1.2.

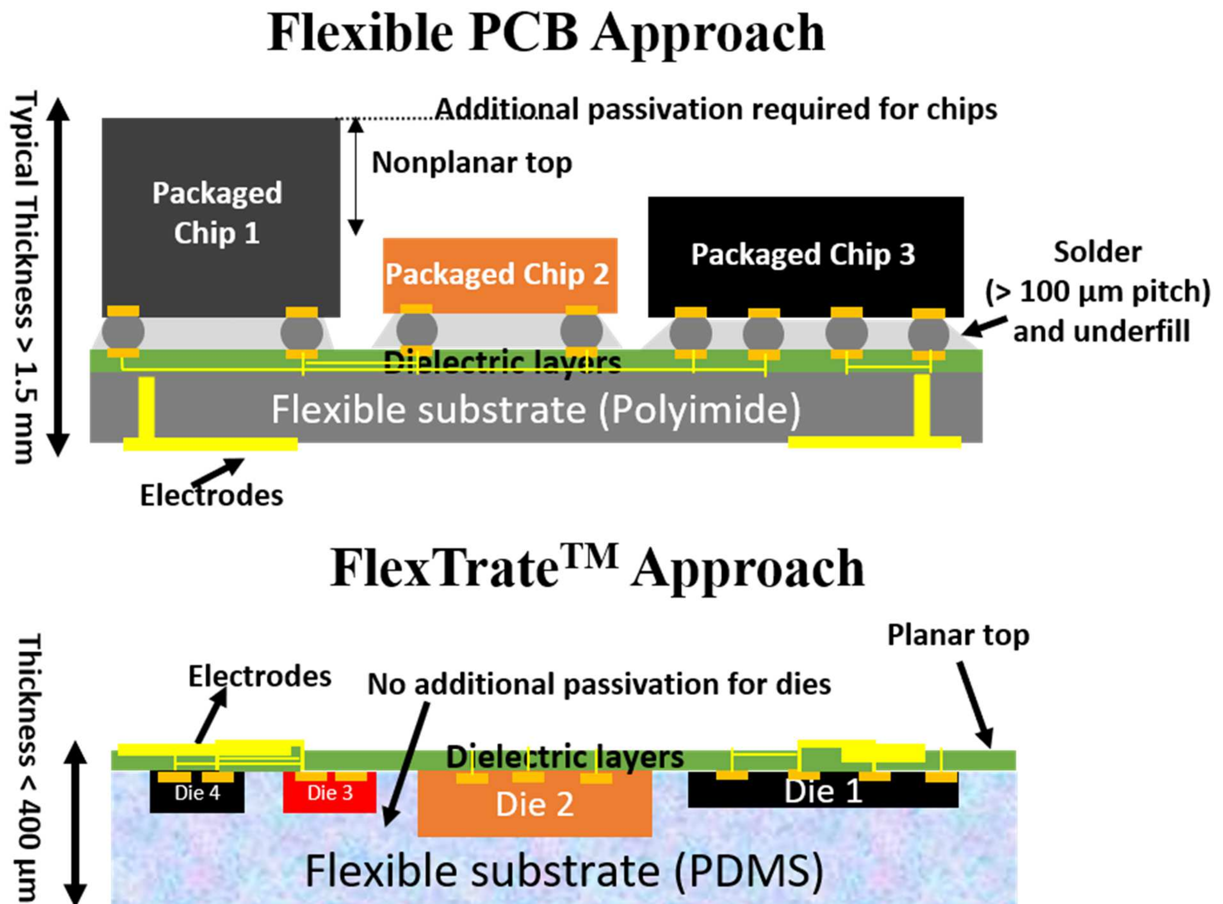


Figure 1. 3. Schematic showing comparison of "flexible PCB" approach to "FlexTrate™" approach for making flexible devices.

	Flexible PCB Approach	FlexTrate^{TM} Approach
Integration	Chip-last	Die-first
Solder/paste	Required	Not required
Underfill	Required	Not required
Minimum pad pitch	~ 100 µm	~ 40 µm
Bare die integration	Limited	Yes
Additional chip passivation	Required	Not required
Flexibility	Lower	Higher

Table 1. 3. Comparison of FlexTrate^{TM} approach over flexible PCB approach.

- The current flexible PCB approach to make flexible electronics involves bulky, packaged chips bonded to a flexible substrate using stiff solder or anisotropic conductive paste (ACP) joints. Fig. 1.3 shows a schematic of the "flexible PCB" approach compared to the FlexTrateTM approach. The comparison of FlexTrate^{TM} approach vs. flexible PCB approach are summarized in Table 1.3. FlexTrate^{TM} enables solderless heterogeneous integration of bare dies at 20-40 µm pad pitches not achievable using conventional PCB technology.
- FlexTrate^{TM} allows integration of high-performance bare dies that require pad pitches of ~ 40 µm. The integration of 200 dies connected in daisy chains at 40 µm pad pitch has been demonstrated on FlexTrate^{TM}. Integration of bare dies vs. packaged chips helps to significantly reduce the volume of the electronic components, which are rigid in nature.

This reduction in volume allows for an overall smaller form factor and provides more flexibility to the system.

- The novel engineered vertically corrugated structures for interconnects on FlexTrate^{TM} reduce the buckling amplitude of the interconnects by 5X when compared to the planar interconnects. Moreover, the vertically corrugated interconnects are much more flexible than planar interconnects and can be reliably bent to 1 mm bending radius for over thousands of bending cycles with minimal performance degradation.

1.4.2 Limitations and challenges

Every technology comes with several challenges and certain limitations. Some of the major challenges and limitations of the FlexTrate^{TM} technology are listed below. Although this list is not exhaustive, it presents an overview of the different types of challenges and the strategies to overcome them. A conceptual model of the overall system on the FlexTrate^{TM} is illustrated in Fig. 1.4 and shows some of the key enablers in realizing a flexible system on FlexTrate^{TM}.

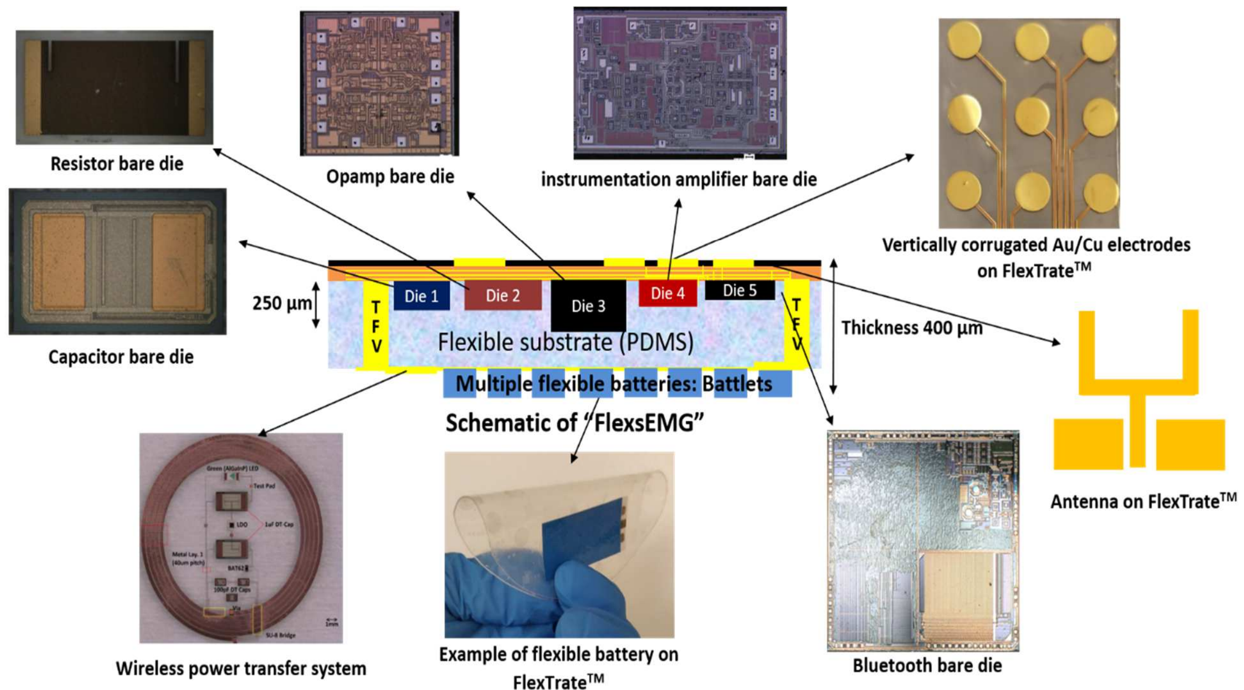


Figure 1. 4. Schematic representing an overview of the FlexTrate^{TM} technology. Some of the key enablers are highlighted, including system integration, heterogeneous integrated dies, sensors, electrodes, wireless power delivery, wireless communication, Through FlexTrate^{TM} Vias (TFVs), external connectors, and passive dies.

- FlexTrate^{TM} is based on the die-first FOWLP approach. As a result, once the dies are embedded in the substrate they cannot be removed or reused. This can be expensive during the process development phase if the yield of the RDL build-up is low. Moreover, the typical challenges of die-first FOWLP, such as die-tilt, die pop-up, and die shift are also seen in FlexTrate^{TM}. However, by using PDMS as a substrate, which has favorable thermo-mechanical properties, as shown in Table 1.1, there is reduction of die-tilt and die pop-up to $\leq$ 1 µm and die shift of $<$ 8 µm across a 100 mm wafer, which is the lowest die shift value in literature as of this writing [24, 29].

- The vertically corrugated structure to make interconnects are about 5 μm in height. This leads to increased non-planarity for the 2nd metallization layer. The non-planarity can be reduced by having a thick (≥ 10 μm) dielectric layer for 2nd layer RDL.
- Direct metallization on PDMS is not feasible due to the high CTE and Young's modulus mismatch between the metal and PDMS substrate. This drawback is overcome by depositing buffer layers on PDMS to allow reliable metallization on FlexTrate™. However, the dielectric deposition increases process complexity. Direct printing of interconnects on PDMS may be a potential alternative solution to reduce process complexity.
- The FlexTrate™ process is expensive process because it uses conventional cleanroom processes to make the RDL, such as metal deposition, lithography, dry etching, etc. The cost can be reduced by switching to printing techniques, such as screen printing, roll-to-roll printing, or inkjet printing.
- The current alignment strategy to achieve high die placement accuracy of ± 1 μm requires the alignment marks to be made on the thermal release adhesive of the 1st handler. This increases process complexity and cost since the adhesive is not reusable. Alternative approaches, such as patterning alignment marks on the reusable 1st handler, without compromising on the ± 1 μm die placement accuracy need to be explored.
- It is difficult to acquire the required bare dies to complete a system on FlexTrate™. This is mainly because of limited supply-chain for bare dies. Collaboration with companies like i3 Microsystems, which specialize in de-packaging commercially available chips help us to get access to bare dies.

- Currently, masks are used to define patterns for the RDL development on FlexTrate^{TM}. Making masks is an expensive process, particularly when multiple mask designs are needed during the process development phase. Approaches such as maskless lithography through direct write laser tools to make patterns on FlexTrate^{TM} can be explored.
- The overall thickness of FlexTrate^{TM} is defined by the thickest die. Increased FlexTrate^{TM} thickness reduces the overall flexibility of the platform. The use of bare dies with ≤ 300 μm thickness can help to keep the overall FlexTrate^{TM} as thin as possible.
- Currently, the vertically corrugated interconnects on FlexTrate^{TM} are not stretchable. There are many wearable and implantable applications that require the stretchability of the system. Printable stretchable interconnects can be integrated into FlexTrate^{TM} to allow for the overall stretchability of FlexTrate^{TM}.

1.5 Scope of this work

There are several key enablers for successful assembly of a highly flexible and reliable system on FlexTrate^{TM}, including the substrate technology, fine-pitch interconnect process, power delivery, die-die communication, wireless communication, heat extraction, and novel system integration approach through FOWLP. Addressing all the issues would require considerable time and human resources beyond this dissertation's scope. Therefore, this dissertation focuses on certain fundamental aspects of the FlexTrate^{TM} technology. These include development of the fabrication techniques for the FlexTrate^{TM} platform, development of the alignment mark strategy, the die embedding process in the flexible substrate based on FOWLP while reducing die-tilt, die pop-up, and die shift, development of vertically corrugated fine-pitch (≤ 40 μm) flexible interconnects, system passivation, high system flexibility, wireless communication, and finally, demonstration of

a fully integrated wearable application in the form of a wireless multi-channel low form factor, flexible sEMG system on the FlexTrate™ platform. This work is a first step in demonstrating the technological advancement and the performance advantages of the FlexTrate™ technology.

1.6 Organization of this dissertation

The remainder of this thesis is organized as follows:

Chapter 2 illustrates the process flow of FlexTrate™, including the fabrication of vertically corrugated interconnects and two metallization layers on FlexTrate™.

Chapter 3 describes the die integration on FlexTrate™. The 200 dies integrated at 40 μm pad pitches and a foldable display with 42 LEDs are shown along with their bendability results.

Chapter 4 details the development and testing of a multi-channel sEMG system on FlexTrate™ along with the initial manufacturing process of FlexTrate™ at i3 Microsystems.

Chapter 5 presents the summary and outlook of this work.

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2. FlexTrate™ Fabrication

In this chapter, the fabrication process of the FlexTrate™ is described, and the results of fabricated FlexTrate™ samples are presented.

2.1 Fabrication process flow

S. No	Steps	Measurement	Method Used	Process details
1	Glass handler (1st handler)	4” diameter, 500 µm thick	-	-
2	Adhesive A (3195M, Nitto REVALPHA™) on glass handler	Single side thermal release @ 120 □	Thermal release on top side	Manual placement
3	Parylene-C deposition	~0.5 µm	CVD	
4	Fluoropolymer (3M™ Novec™ 1700)	~0.2 µm	Spin Coating	(i) 5 s, 1000 rpm (ii) 30 s, 4000 rpm (iii) Stop
5	Au Deposition	~50 nm	E-beam deposition	
6	SU-8 2000.5	~0.5 µm	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 4000 rpm

				(iii) Stop
7	Pattern SU-8 2000.5		Lithography-	Prebake @ 80 □ for 120 s, energy dose @ 80 mJ/cm^2, post bake for 180 s, develop for 60 s, triple rinse with IPA
8	Etch Au		Cl_2 dry etch	Cl_2 :30 sccm, Ar: 10 sccm, RF power: 500 W
9	Etch fluoropolymer and Parylene-C		O_2 RIE	O_2:100 sccm, DC power 300 W for 120 s
10	Place dies		Pick-and-place tool	Placement force: ~5 N/mm^2 die area
11	Place Teflon ring	~150 µm greater than die thickness	-	Manual placement
12	Dispense Silastic MDX4-4210 PDMS	~3.7 g for 500 µm thickness	Manual dispense	10:1 ratio by mass of PDMS: curing agent mixed by THINKY™, ARE-310 @ 2200 rpm for 120 s
13	Adhesive B (3195V, Nitto REVALPHA™)	Single side thermal release @ 180 □	Thermal release on top side	Manual placement

	on Si handler (2nd handler)	4” diameter, 500 μm thick handler		
14	Place 2nd handler over PDMS	-	Adhesive B’s thermal release side on PDMS	-
15	Compression mold and curing of PDMS		Compression molding	
16	Release 1st handler		Thermal release	120 □ for 180 s
17	Surface treatment for adhesion		O_2 RIE	O_2:100 sccm, DC power 100 W for 180 s
18	Adhesion promoter (AP-3000)		Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 3000 rpm (iii) Stop
19	Parylene-C deposition	~1 μm	CVD	
20	Surface treatment for adhesion		O_2 RIE	O_2:100 sccm, DC power 100 W for 50 s
21	SU-8 2001	~1 μm	Spin coating	(i) 5 s, 1000 rpm

				(ii) 30 s, 3000 rpm (iii) Stop
22	Blanket expose SU-8 2001	-	Lithography	Prebake @ 95 ℃ for 120 s, energy dose @ 120 mJ/cm^2, Post bake for 180 s, develop for 60 s, triple rinse with IPA
23	SU-8 2005	~5 µm	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 3000 rpm (iii) Stop
24	Corrugation on SU-8 2005		Lithography	Prebake @ 95 ℃ for 180 s, energy dose @ 90 mJ/cm^2, post bake for 240 s, develop for 180 s, triple rinse with IPA
25	Photoresist AZ P4620	~7 µm	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 4000 rpm (iii) Stop
26	Pattern resist for vias		Lithography	Prebake @ 110 ℃ for 80 s, Energy dose @ 650 mJ/cm^2, develop for 180 s in MIF AZ 300 Developer

27	Etch vias to die pads	~2.5 µm	O_2 RIE	O_2:100 sccm, DC power 300 W for 180 s
28	Remove resist		Rinse in Acetone+IPA+DI water	
29	Surface treatment for adhesion		O_2 RIE	O_2:100 sccm, DC power 100 W for 60 s
30	Sputter Ti/Cu	Ti/Cu-50 nm/500 nm	RF sputtering	Power: 350 W
31	Photoresist AZ P4620	~7 µm	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 4000 rpm (iii) Stop
32	Pattern resist		Lithography	Prebake @ 110 □ for 80 s, Energy dose @ 650 mJ/cm^2, develop for 180 s in MIF AZ 300 Developer
33	Plating interconnects (Technic, Inc plating bath)	~5 µm	Cu electroplating	

34	Remove resist		Rinse in Acetone+IPA+DI water	
35	Etch Cu seed layer with	~500 nm	Wet etching	APS-100 Cu Etchant
36	Etch Ti seed layer	~50 nm	Wet etching	BOE 6:1
37	Surface treatment for adhesion		O_2 RIE	O_2:100 sccm, DC power 100 W for 60 s
38	Adhesion promoter	AP-3000	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 3000 rpm (iii) Stop
39	Parylene-C deposition	~2 µm	CVD	
40	Photoresist AZ P4620	~7 µm	Spin coating	(i) 5 s, 1000 rpm (ii) 30 s, 4000 rpm (iii) Stop
41	Pattern resist		Lithography	Prebake @ 110 ℃ for 80 s, Energy dose @ 650 mJ/cm^2, develop for 180 s in MIF AZ 300 Developer

42	Etch vias to pads	~2 μm	O_2 RIE	O_2:100 sccm, DC power 300 W for 180 s
43	Remove Resist		Rinse in Acetone+IPA+DI water	
44	Release 2nd handler		Thermal release	180 □ for 120 s

Table 2. 1. Process steps for FlexTrate™ fabrication.

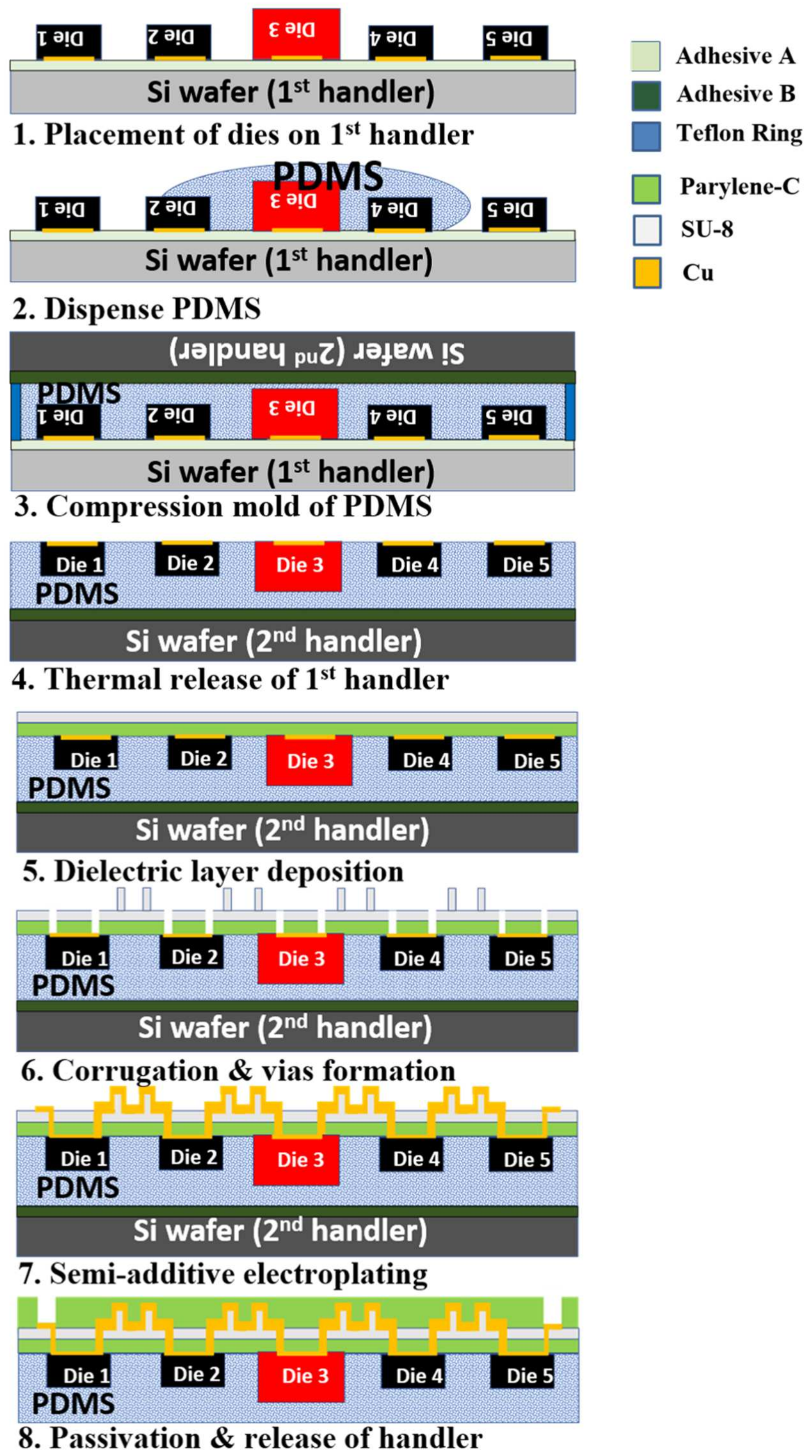


Figure 2. 1. Schematic of major steps in the fabrication of FlexTrate^{TM}.

The process steps for fine-pitch interconnects on FlexTrate™ are detailed in Table 2.1 A schematic of the major process steps is shown in Fig. 2.1 and described below:

Step 1: A thermally removable adhesive A is placed over a glass wafer (1st handler). Then, ~ 0.5 µm thick Parylene-C is deposited over the adhesive A via Chemical Vapor Deposition (CVD). This is followed by spin coating a fluoropolymer over the Parylene-C. The deposition of Parylene-C and the fluoropolymer help in the transfer of Au alignment marks from adhesive A to the PDMS substrate in the later steps. Next, Au is deposited by e-beam evaporation over the fluoropolymer. Photoresist SU-8 2000.5 is spun over the Au layer and is lithographically patterned for use as a soft mask to make alignment marks. The Au is then dry etched to form the alignment marks. The exposed SU-8, fluoropolymer, and Parylene-C are etched away by O_2 plasma. A pick-and-place tool is used to place the dies, face down, on the adhesive with high alignment accuracy (± 1 µm).

Step 2: A circular Teflon ring having an outer diameter of 100 mm and an inner diameter of 90 mm, is placed at the outer boundary of adhesive A. The Teflon ring determines the thickness of the cured PDMS. Then, PDMS is mixed with the curing agent in a ratio of 10:1 by mass and manually dispensed over adhesive A with dies (face down) placed on it.

Step 3: Another thermally removable adhesive B, having a higher release temperature than adhesive A, is placed over a Si wafer (2nd handler). Adhesive B is placed over the uncured PDMS and the assembly is placed under vacuum to degas the PDMS._After degassing, the PDMS is compression molded and allowed to cure for 24 hrs. at 25 □.

Step 4: The 1st handler is removed by heating the system to the release temperature of adhesive A. The PDMS surface is then treated with O_2 plasma to make it hydrophilic, and an adhesion promoter is spin-coated over its surface.

Step 5: Parylene-C is deposited over the PDMS surface. The Parylene-C surface is also treated with O_2 plasma to make it hydrophilic. Next, SU-8 2001 is deposited by spin-coating and blanket exposed. The deposited Parylene-C and SU-8 2001 act as stress buffer layers by reducing the difference of Young's modulus and CTE mismatch between PDMS and metal interconnects, enabling crack- free metallization on FlexTrate^{TM} in further steps. Moreover, they also reduce the surface non-planarity between the top of the dies and the substrate.

Step 6: To make corrugations on the top surface, SU-8 2005 is spin-coated and lithographically patterned. To etch the contact holes, PR AZ P4620 is spin-coated and lithographically patterned. With PR AZ P4620 acting as a soft mask, the vias are dry-etched through the SU-8 2001 and Parylene-C layers to contact the die pads. After making the vias, the photoresist is removed, and the surface is treated with O_2 plasma to make it hydrophilic to improve adhesion for the metal seed layer.

Step 7: A thin blanket seed layers of Ti/Cu of thicknesses 50 nm/500 nm are sputtered over the top hydrophilic surface of FlexTrate^{TM}, where the sputtered metal layer also contacts the pads on the dies. AZ P4620 photoresist is spin-coated and lithographically patterned. A semi-additive process of Cu electroplating is used to obtain ~ 5 μm thick Cu interconnects that run over the top layer of the FlexTrate^{TM} and contact the underlying dies through the vias to form fine-pitch interconnects. After electroplating the interconnects, the photoresist is removed, followed by the removal of the Ti/Cu seed layers by wet etching.

Step 8: The surface of FlexTrate^{TM} is made hydrophilic by O_2 plasma treatment and Parylene-C is deposited via CVD to passivate FlexTrate^{TM}. The passivation is patterned via O_2 plasma dry etching using AZ P4620 as a soft mask. Finally, the 2nd handler is removed by heating the assembly to the release temperature of adhesive B, and the fabrication of FlexTrate^{TM} is complete.

2.2 Alignment marks strategy

2.2.1 Alignment marks on the adhesive of 1st handler

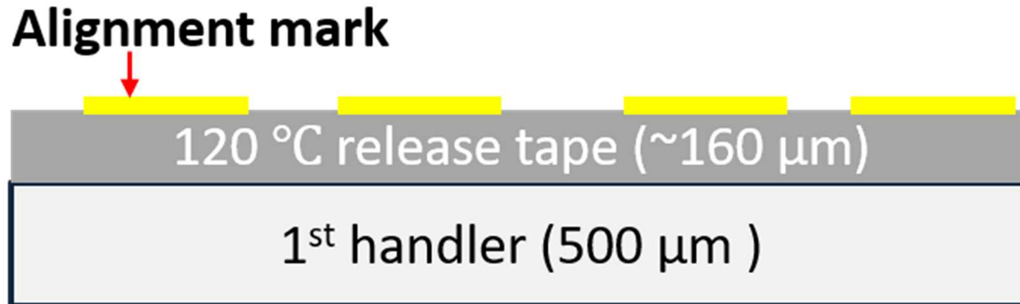


Figure 2. 2. Alignment marks fabricated on adhesive A of the 1st handler.

In this approach, the alignment marks are fabricated on the adhesive of the 1st handler (glass) as shown in Fig. 2.2. The process steps used to make the alignment marks on the adhesive of the 1st handler are shown in steps 2-9 in Table 2.1. Due to multiple processing steps to make alignment marks on the adhesive, including dry etching, this approach is quite expensive. Moreover, alignment marks need to be made each time a new FlexTrate™ sample is fabricated, as the thermal release adhesive A cannot be reused, leading to increased process complexity and cost. The pick-and-place tool used to place dies can recognize the alignment marks with high accuracy as the alignment marks are in direct line of sight of the tool's IR camera. Die placement accuracy of ± 1 µm was achieved using this alignment strategy, the details of which are in section 3.1.

2.2.2 Alignment marks on the 1st handler

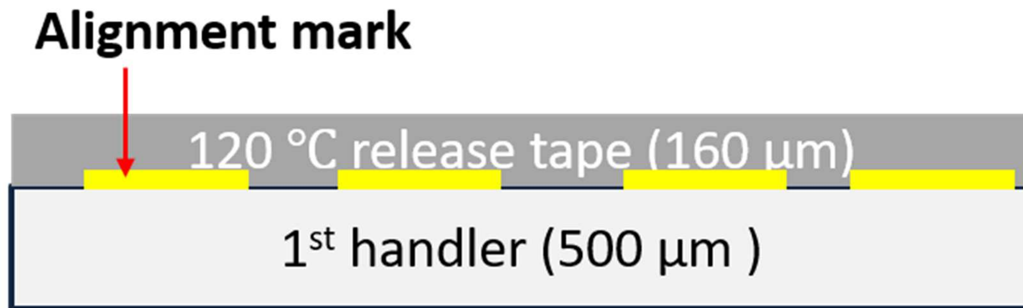


Figure 2. 3. Alignment marks fabricated on the 1st handler.

In this alignment mark strategy, the alignment marks are fabricated on the 1st handler before placing the thermal release adhesive on the 1st handler, as shown in Fig. 2.3. The standard lift-off process is used to make the alignment marks of Ti/Au (20/200 nm). Au is used due to the high contrast for the pick-and-place tool to recognize the alignment marks through the adhesive. The pick-and-place tool used to place dies recognizes the alignment marks with reduced accuracy as compared to the previous alignment strategy as the alignment marks are not in the direct line of sight of the tool's camera. Die placement accuracy of ± 10 µm was achieved using this alignment strategy. This strategy can be used for integrating systems that do not need high alignment tolerance. With this approach, the 1st handler with alignment marks can be re-used multiple times when fabricating multiple copies of the same system on FlexTrate™, leading to reduced process complexity and cost.

2.3 Vertically corrugated interconnects

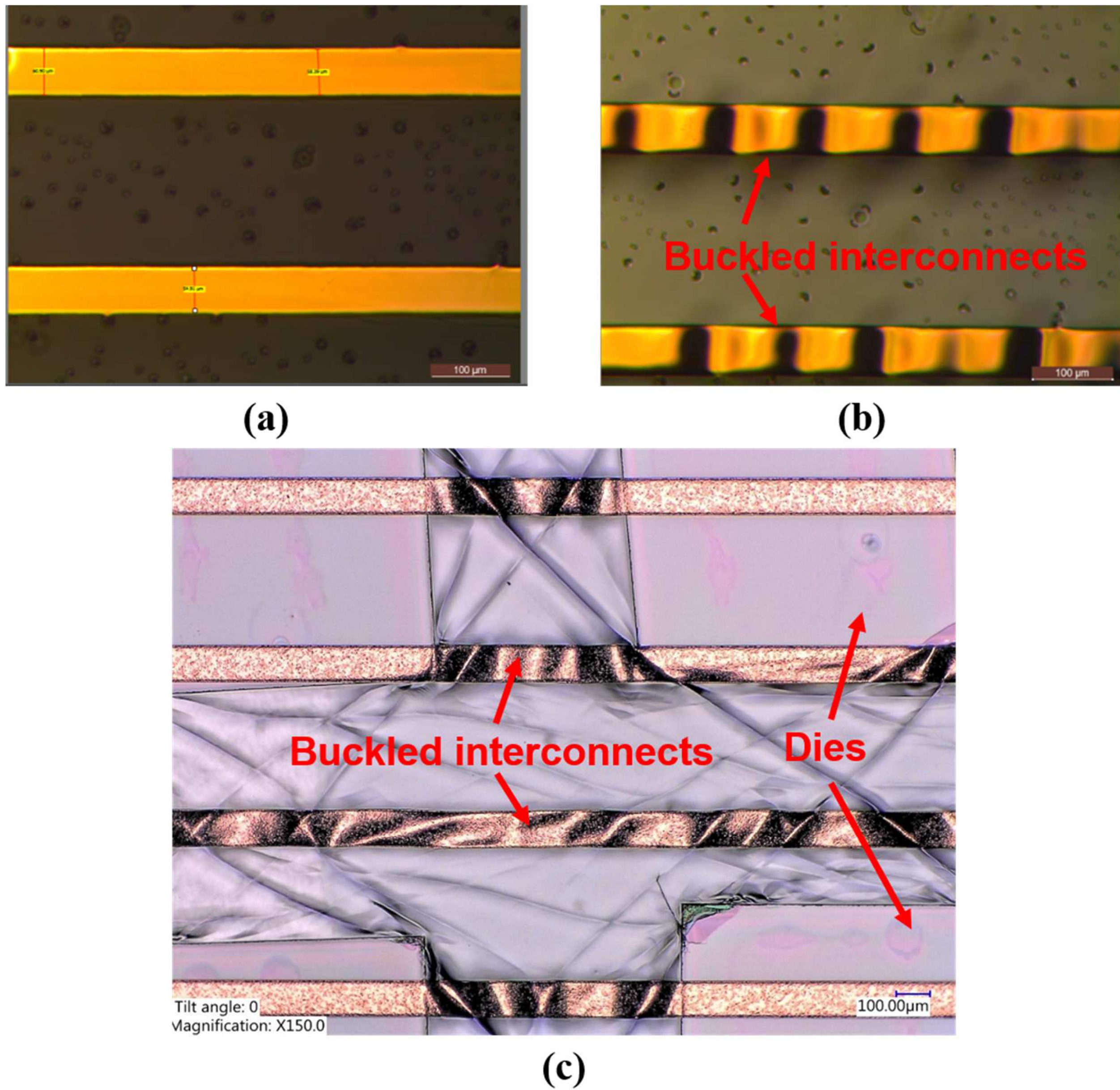


Figure 2. 4. Planar Cu interconnects (a) before and (b) after the thermal release of the 2nd handler. (c) Planar 100 µm width Cu interconnect running over dies after thermal release from the 2nd handler.

Formation of reliable fine-pitch interconnects on elastomeric substrates is challenging because of the thermo-elastic wrinkling/buckling phenomenon arising due to compressive stress induced by shrinkage of a pre-strained substrate after release. This happens in the case of FlexTrate^{TM} after the final thermal release step at 180 □ when the substrate is cooled down to room temperature (Step 8 in Fig. 2.1 [1-5]. This can potentially cause catastrophic failure due to buckle-induced delamination of deposited thin metal films [6, 7]. The buckling of interconnects on FlexTrate^{TM} is shown in Fig. 2.4. To reduce the buckling of interconnects, novel engineered vertically corrugated interconnects were fabricated on FlexTrate^{TM}.

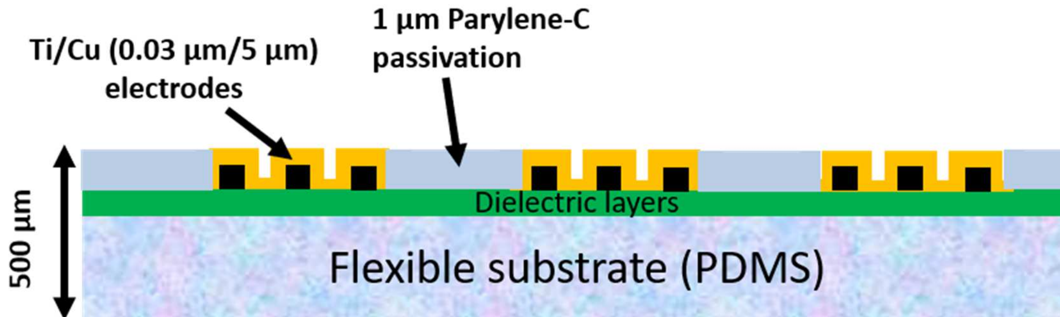


Figure 2. 5. Cross-sectional schematic of the vertically corrugated interconnects fabricated on FlexTrate^{TM}.

Beam mechanics dictates that the critical stress needed to induce buckling in a beam is inversely proportional to the square of the length of the beam [8]. Hence, linear reduction in the beam length results in a quadratic increase in the critical stress value required to induce buckling. This inspired the concept of "vertically corrugated" interconnects, where an intentional and controlled "segmentation" of the interconnects is used to counteract buckling due to the high compressive stress [1]. Fig. 2.5 shows the cross-sectional schematic of vertically corrugated interconnects formed on FlexTrate^{TM}. Fig. 2.6 (a) shows the 100 µm width corrugated interconnects fabricated on FlexTrate^{TM}. The amplitude of buckle waves of planar and "corrugated" interconnects was

measured to be 15 and 3 μm, respectively, and showed more than 5X reduction for "corrugated" interconnects as compared to the planar interconnect, as shown in Figs. 2.6 (b) and (c).

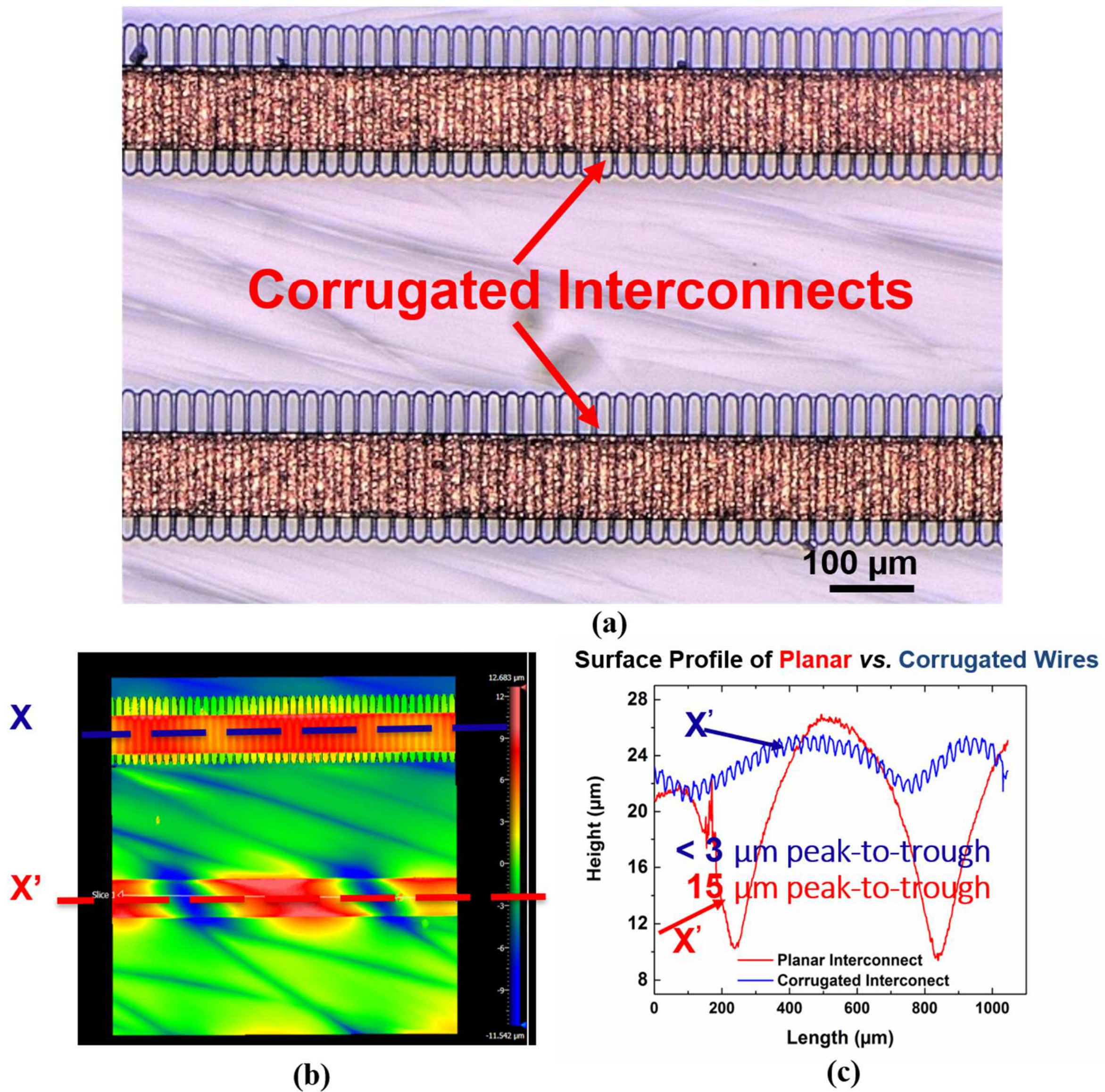


Figure 2. 6. (a) Image showing corrugated 100 μm with lines on FlexTrate^{TM}. (b) Surface profile demonstrating the buckling of planar and corrugated interconnects. (c) Plot of the surface height along lines X and X' shown in (b).

2.3.1 Bending reliability test

Resistance values for both planar and corrugated interconnects were reported after bending at different bending radii as shown in Fig. 2.7. Corrugated interconnects show less than 0.4 % increase in average measured resistance per line width, which confirmed the reliability of the fabricated corrugated interconnects. The Von Mises stress profile was also studied in both planar and corrugated Cu interconnects under mechanical bending at 1 mm bending radius at the point of highest stress, for Cu interconnect length of 15 mm, width of 100 μm, and thickness of 4 μm. Results showed that while the stresses depend on the exact location on the corrugation, the overall stress was shown to reduce on top of the corrugated structure compared to planar interconnects, and showed similar values to planar structure on the bottom of the corrugations [2].

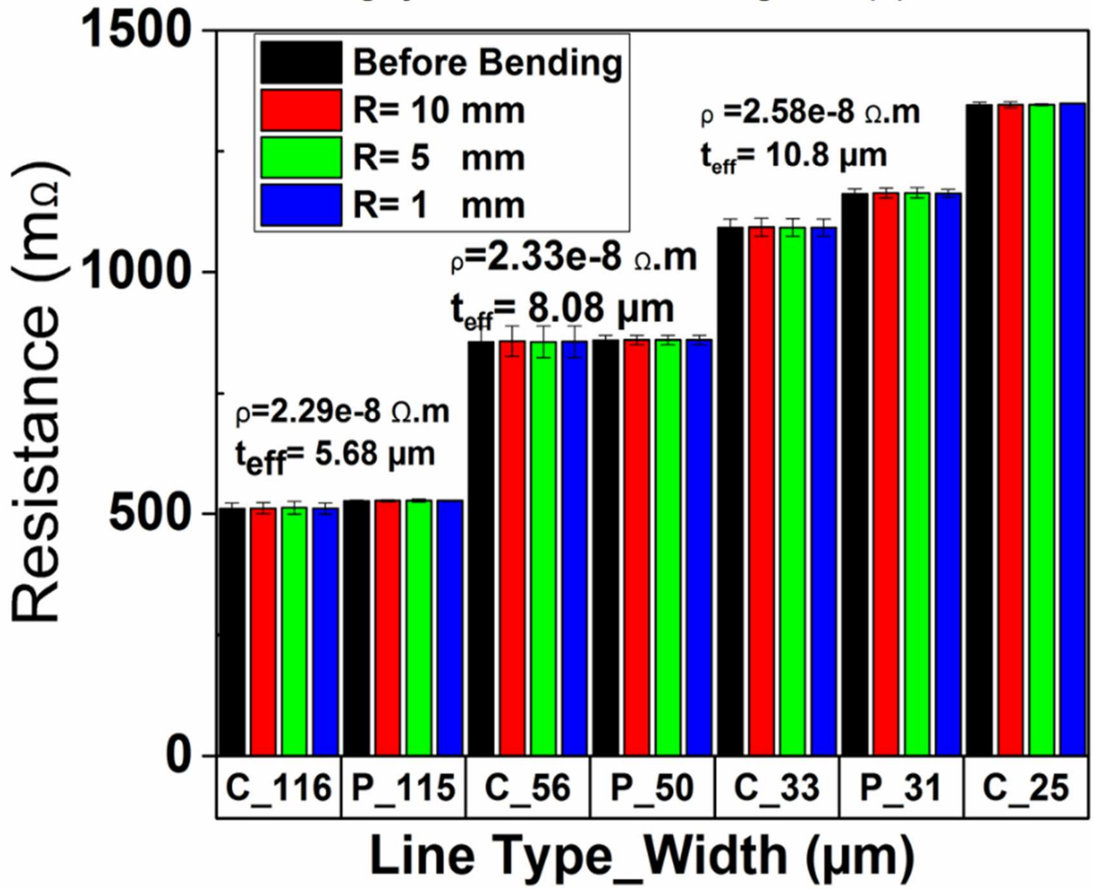


Figure 2. 7. Metal interconnect reliability before and after bending for 1000 cycles at R=10, 5, and 1 mm for planar and corrugated interconnects.

2.4 Demonstration of two metallization layers

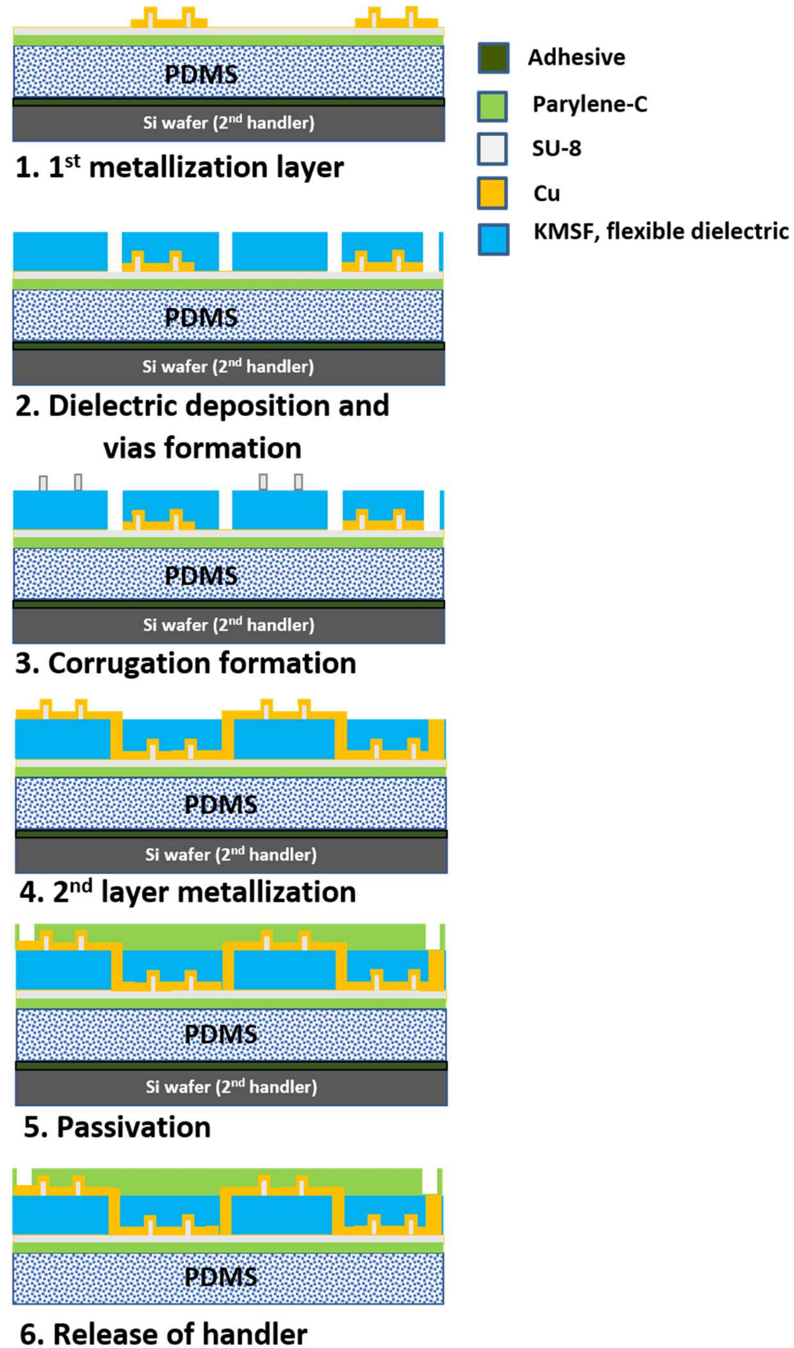
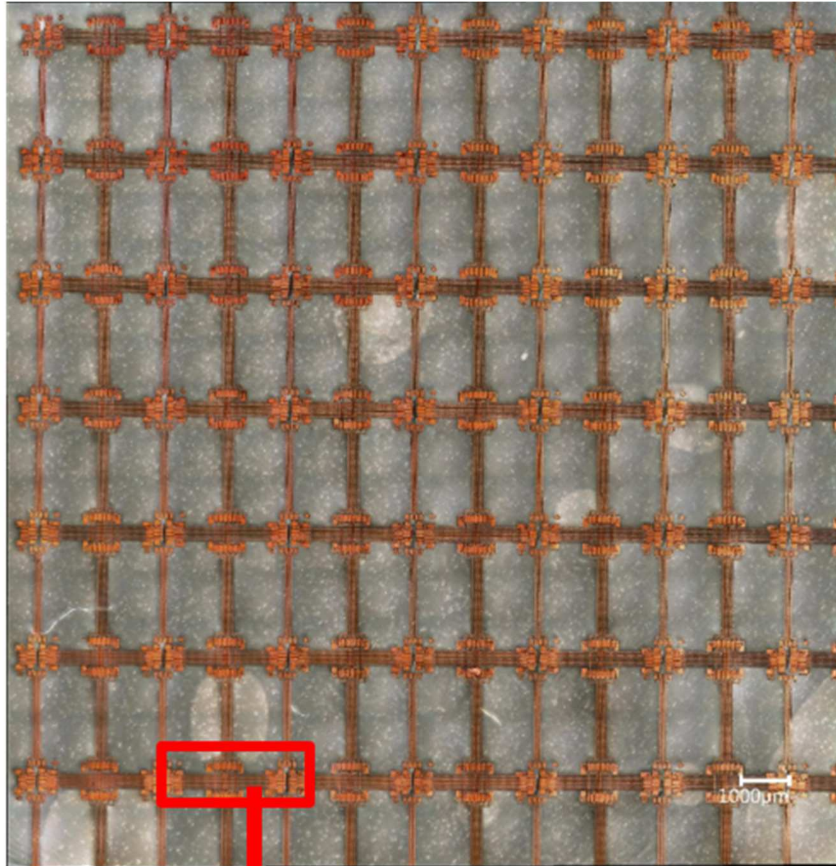
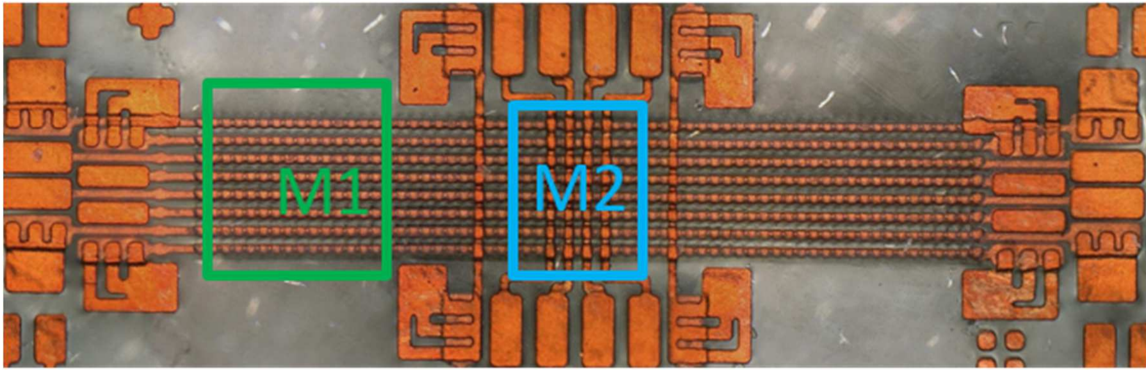


Figure 2. 8. The process flow for fabricating two metallization layers on FlexTrate^{TM}. (Figure not drawn to scale)



(a)



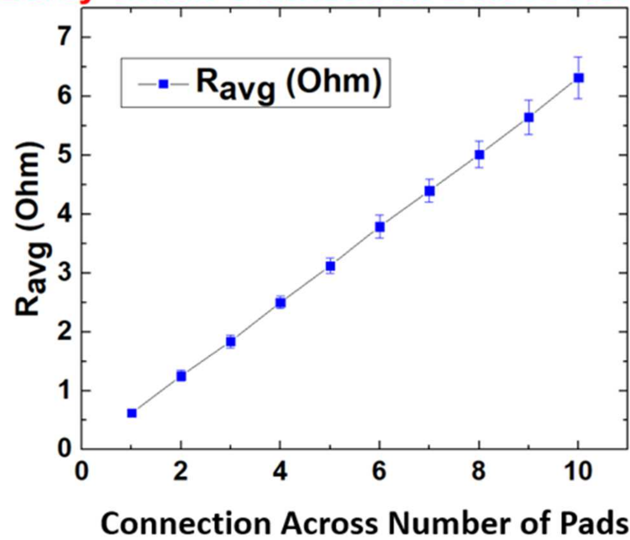
(b)

Figure 2. 9. (a) Image of the fabricated sample with two metallization layers, and (b) a magnified image with fine interconnect pitches of 40 μm, where M2 is running over M1 layer.

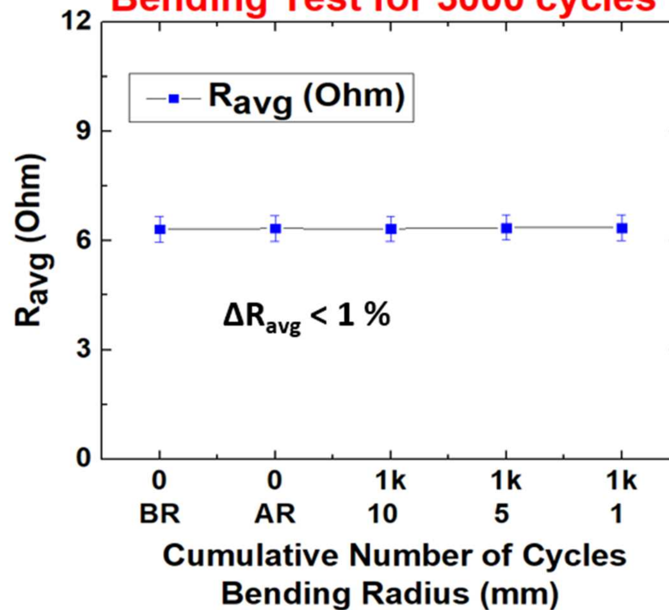
The process flow for fabricating one metal layer with vertically corrugated interconnects and dies on FlexTrate™ has been previously demonstrated [3]. The vertically corrugated interconnects help mitigate the buckling of metal wires on elastomeric substrates and are more reliable than planar interconnects [2]. The process flow for two metallization layers on FlexTrate™ connected in a daisy chain pattern is shown in Fig. 2.8. Here KMSF 1000 was used as the interlayer dielectric material between the 1st and 2nd metallization layers. The fabricated sample and a magnified image with fine interconnect pitches of 40 μm are shown in Fig. 2.9 (a) and (b), respectively [4].

2.4.1 Bending reliability test

The resistance of daisy chain connections from pad one to up to pad ten was measured via 4-point probe Before Release (BR) from the 2nd handler, and the average resistance (R_{avg}) was plotted and shown in Fig. 2.10 (a). As expected, the R_{avg} increases linearly with the number of pad connections, demonstrating good alignment between the M1 and M2 metal layers. The end-to-end resistance from pad one to pad ten was similarly measured BR and After Release (AR) from the 2nd handler. The sample was then bent to 10 mm, 5 mm, and 1 mm bending radius for 1000 cycles each for a cumulative 3000 bending cycles, and the end-to-end resistance was measured at each bending radius. Fig. 2.10 (b) shows that $\Delta R_{avg} < 1$ %, attesting to the reliability of the metal interconnects even under extreme bending conditions. The favorable mechanical properties of KMSF 1000, such as low Young's Modulus and high elongation, allow such extreme flexibility.



(a)



(b)

Figure 2. 10. (a). Plot of R_{avg} vs. connections across the number of pads. (b) Plot of the end-to-end R_{avg} for Before Release (BR) and After Release (AR) of the sample from the 2nd handler and following 1000 bending cycles at each bending radius [4].

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3. Die Integration on FlexTrate™

3.1 Die shift evaluation

Die shift is a serious problem in current die-first FOWLP using rigid EMCs. Sharma et al. [1] have previous reported the average die shift is beyond 40 μm and maximum die shift is nearly 80 μm. These large die shifts are mainly due to the thermal cure shrinkage of the molding compound, low adhesion strength between temporary adhesives and dies, and CTE mismatch between EMCs, handler, and dies. The EMCs including silica fillers have relatively low CTE that is one order magnitude lower than typical epoxies. However, the die shift cannot be eliminated, and thus must be compensated. One approach to do this is by pre-shifting the die before molding, such that the dies are deliberately misplaced during the pick-and-place process to account for the drift [1]. Die shifts are predicted based on die size and location on the wafer, and placed appropriately to compensate for the die shift, but this prediction is not perfect. In modern processes, lithography tools are dedicated to FOWLP applications, and for instance, steppers can accurately compensate for the large die shift in a die-by-die alignment mode [2]. Although the allowable values for die shift depend on lithographic requirements, large die shift reduces wafer-level packaging density and production yield/throughput for patterning.

The thermomechanical characteristics of the biocompatible PDMS (Silastic MDX4-4210) and a rigid EMC including silica fillers typically used in FOWLP [3] are summarized in Table 1.1 for comparison. The elongation at break of the PDMS is quite high, compared to the EMC. The T_g of PDMS is much lower than room temperature, which means thermal stress accumulated with Young's modulus and CTE mismatch in the temperature regions ranging from room temperature

to T_g is negligible [4]. By applying the Stoney's equation [5-7] with the following PDMS/EMC/Si parameters: Young's modulus (MPa): 0.5/22000/190000, CTE (ppm/K): 300/7.5/2.6, PDMS/EMC curing temperature (□): 80/125, and 0.272 for Si Poisson ratio, the total warpage of a 300-mm-diameter Si wafer with a PDMS or EMC of 500 μm thickness are 1.8 μm and 2.4 mm, respectively. The large difference is due to the low Young's modulus of the PDMS. Although the Stoney's equation can well assume the film thickness to be less than 1/20 of the substrate thickness and is a better approximation for smaller substrates [6, 7], the lower Young's modulus for PDMS allows the use of this approximation even for thicker PDMS films.

To evaluate die shift, template matching was deployed as the primary mechanism to assess real die positions in the sample [8]. Template matching is an image processing technique to match an image to a template image. An automated upright optical microscope (Nanotronics, nSpec®) was utilized for the acquisition. The acquisition was defined by the XY area of stage space, the optical conditions, resolution, and auto-focus with which the images were acquired. Global alignments were defined for the sample, to indicate the global sample axes and origin reference before rastering for images. A reference template was supplied, depicting a single instance of the die to which all other instances in the sample were compared with. Template matching was performed automatically to determine real die positions. The input template was matched to each image in the acquisition, and a normalized cross-correlation was used to determine similarity between the template and the image. A similarity score was calculated for each pixel in each image. Locations whose similarity scores were higher than the specified selection criteria were registered as possible dies. On samples where die rotational positions were expected to vary, the template was rotated before matching and rerun through a range of angles to see which produced the highest score for

each die. This approach allowed for the assignment of multiple, independent die rotational positions within the same field of view.

3.1.1 Results

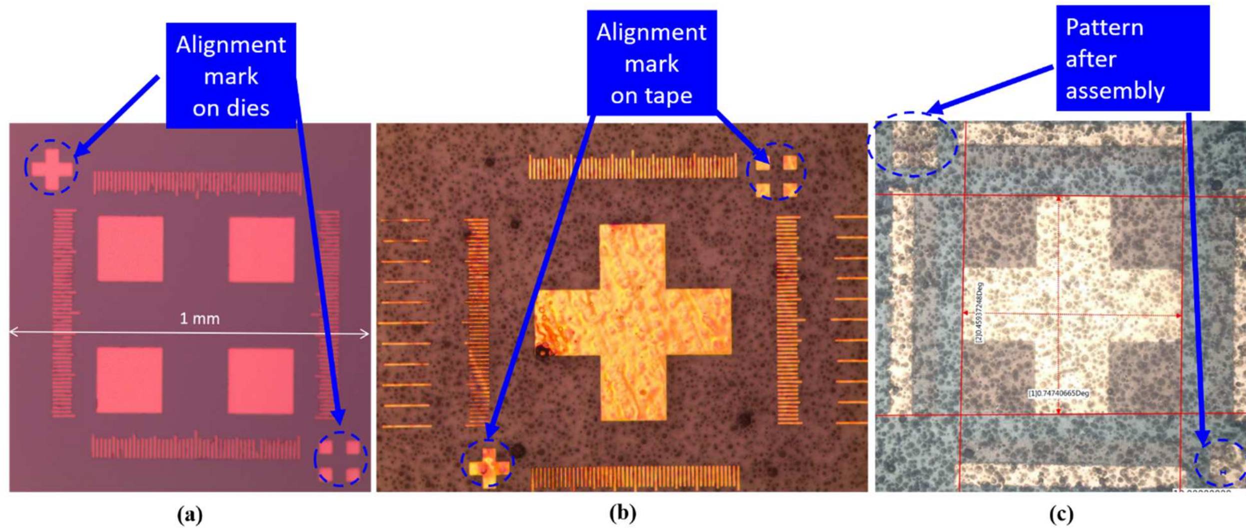

Figure 3. 1. Alignment fiducial marks on (a) die (b) tape, (c) the final assembly of die placed on the tape, which are imaged through the backside of a glass substrate laminated with a thermal release tape.

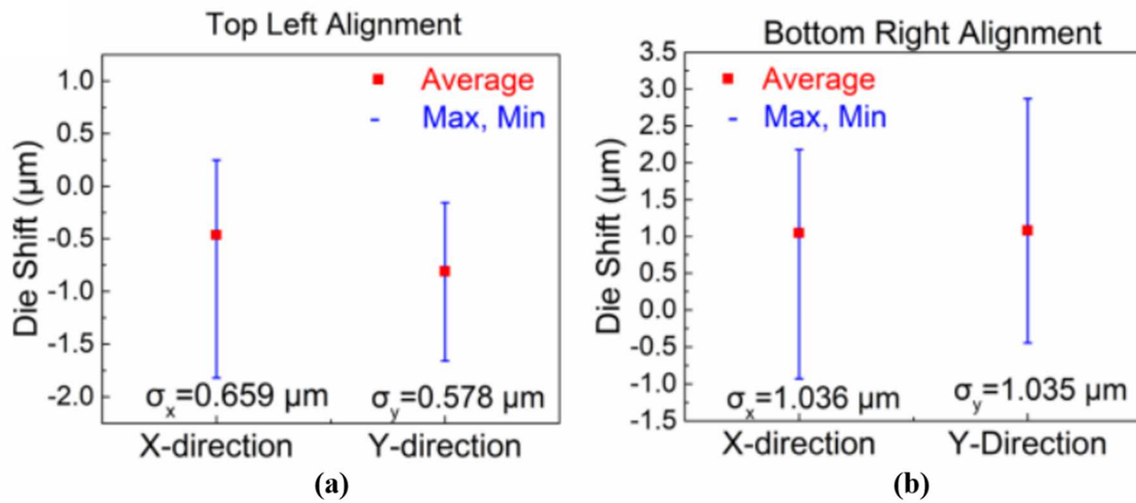

Figure 3. 2. Die placement accuracy measurements provided as the misalignment average, standard deviation, and min-max values for (a) top left alignment fiducial, and (b) bottom right alignment fiducial marks.

The die shift was evaluated before and after PDMS curing using Vernier scale patterns on the temporary adhesive laminated on the 1st handler. The dies, having the corresponding Vernier patterns, were aligned, and placed using a pick-and-place tool on the adhesive tape. An alignment strategy that uses two alignment fiducials was used, as shown in Fig. 3.1 (a) and (b), on both the integrated dies and the adhesive tape on the 1st handler. The flip-chip assembled die on the adhesive is shown in Fig. 3.1 (c). The placement accuracy of an array of 25 dies is shown in Fig. 3.2 (a) and (b) for alignment accuracy in both the x and y directions. The average misplacement was measured to be < 1 μm. The high placement accuracy helps reduce the aggregate die shift measured after wafer reconstruction.

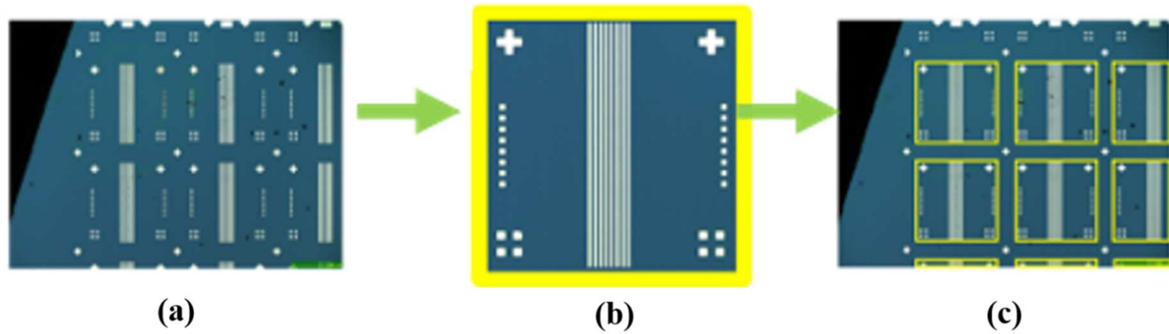

Figure 3. 3. (a) Die positions across control sample utilizing (b) die template to find instances and assign real die positions in (c) control sample.

Fig. 3.3 illustrates the acquisition and analysis workflow. In the expected die locations, real translational and rotational positions were associated with die indices, names, and dimensions. In this workflow, template matching can be expected to supply real die positions within repeatability corresponding to the equivalent physical dimensions of the pixel used for acquisition on the imaging system, provided that the pixel size is larger than the stage XY encoder resolution of the system, which in this case was 50 nm. To demonstrate accuracy and repeatability of die position assessment, trials were repeated on a control sample consisting of a 100 mm Si/SiO2 wafer patterned with Ti/Cu alignment marks by lift-off. Here, actual die positions were matched within a ± 1 µm tolerance. Acquisition was run with white light brightfield and a pixel size of 0.90 µm. Table 3.1 reports the detected pitch X and pitch Y, defined as the distance from each die to its nearest neighbor in each dimension. For five trials and 2462 dies in the sample range, imaging time per die took an average of 0.04 s. Using standard statistical quality assurance methods to project a normal distribution of measurement outcomes from the average range of trials, a projected equipment variation (EV) of 0.19 µm, representing 95 percent of outcomes, was

computed, which satisfies recognized manufacturing quality assurance of more than an order of magnitude smaller than the nominal tolerance of ± 1 µm [9].

Mean average (µm)	**1099.94**
Mean range (µm)	**0.08**
Projected Equipment Variation (EV) (95%) (µm)	**0.19**
Nominal value +/- tolerance (µm)	**1100 ± 1**
Error (Mean average) (%)	**0.0055**

Table 3. 1. X and Y pitch accuracy based on 5 independent measurements of the sample.

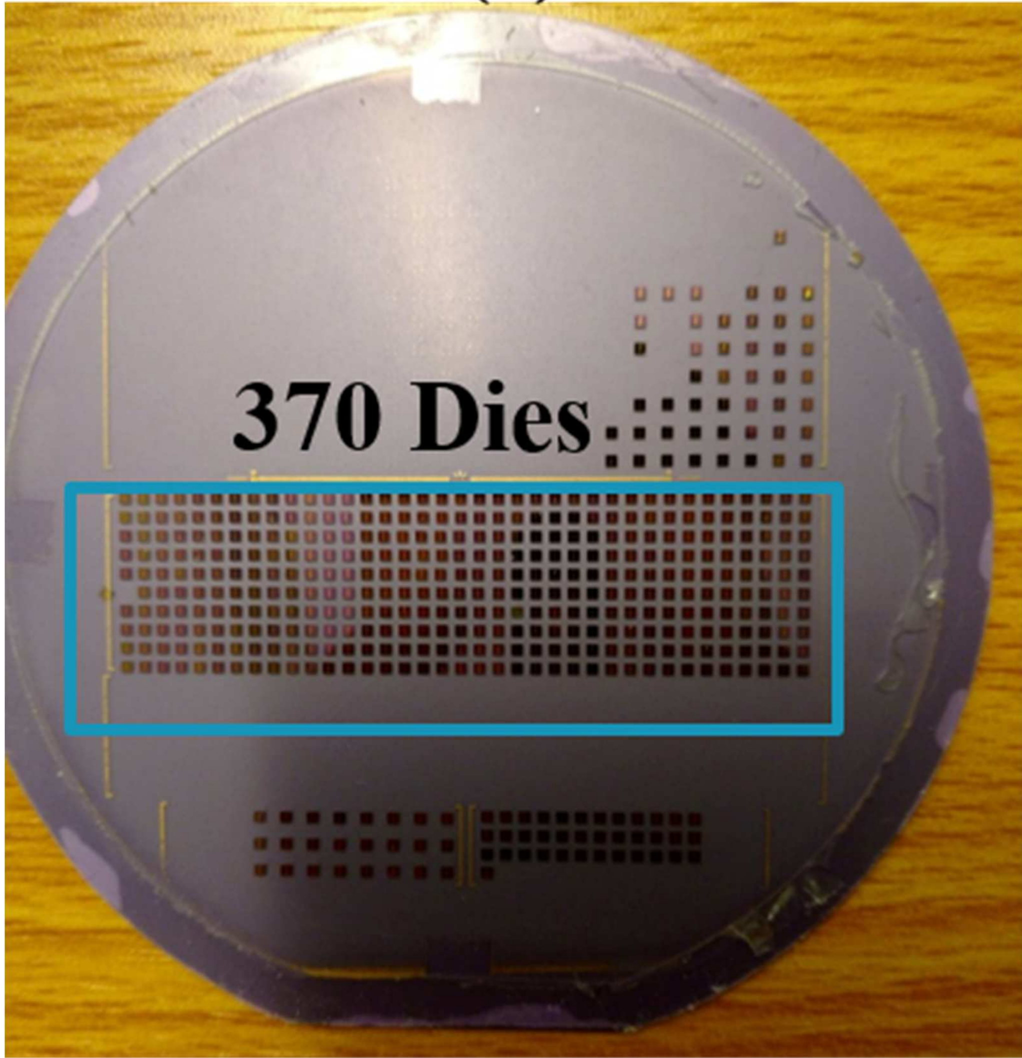

Figure 3. 4. Image of the 100 mm sample fabricated through FOWLP with 370 dies placed to evaluate die shift on 2nd handler.

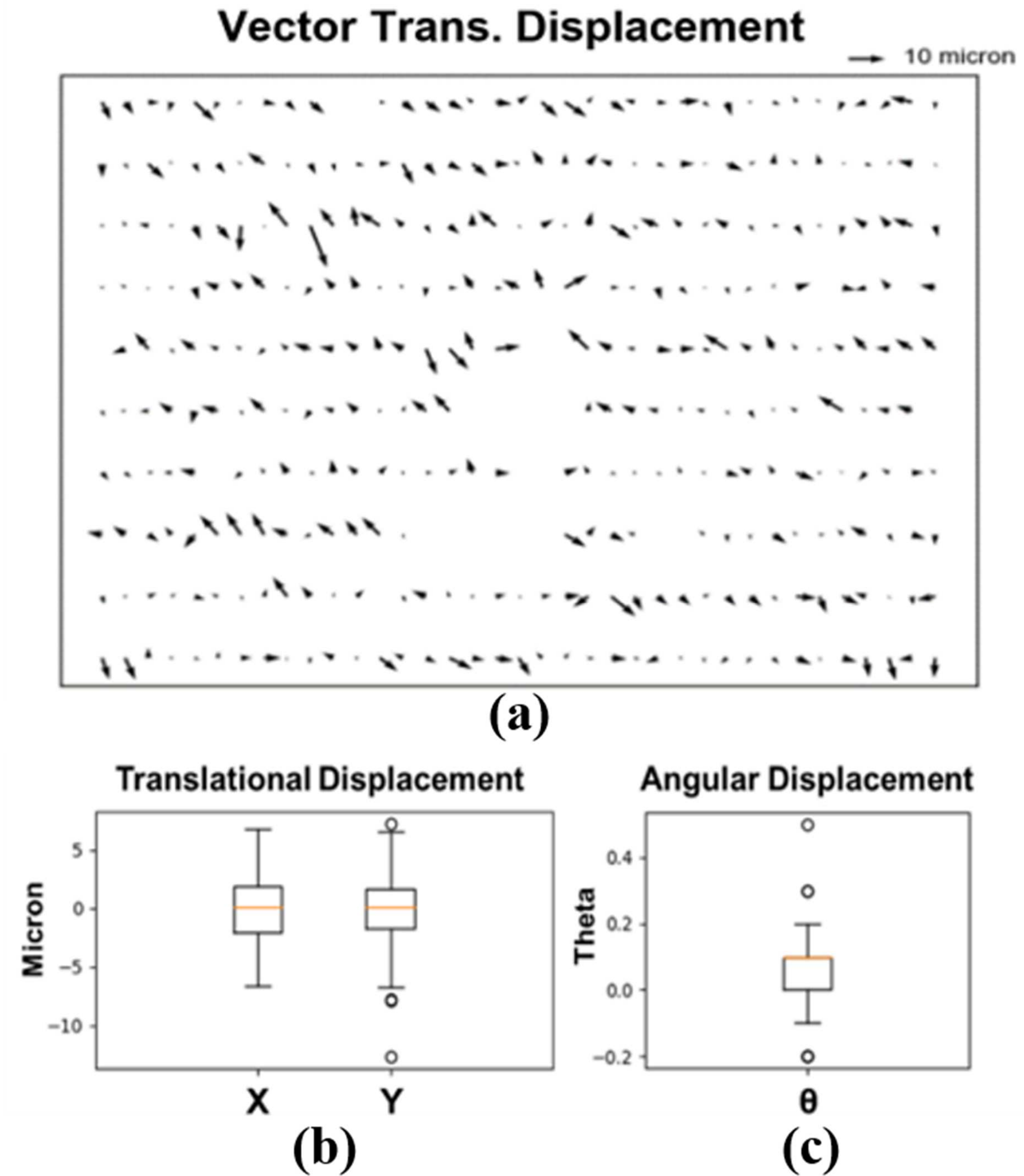

Figure 3. 5. (a) Vector plot showing magnitude and direction of significant displacements from nominal positions on FOWLP sample. Spread of (b) translational and (c) rotational displacements from nominal positions of dies.

With the validation on a control sample, the same method was used on a FlexTrate™ sample as shown in Fig. 3.4, where die translational and rotational positions were prone to vary from nominal positions due to die shift. The actual pitch was used as a guide to determine nominal translational positions, whereas the nominal die rotational positions were taken to be orthogonal to the global sample axis. Fig. 3.5 gives a vector plot indicating the magnitude and direction of die XY deviations with respect to the nominal positions and the spread of die translational and rotational positions in their discrepancies from nominal. The die shift values reported were significantly less than the die µshift expectations for conventional rigid FOWLP [1, 10-13]. The low curing temperature (~25 □) of PDMS based FOWLP process reduces die shift affects more than the rigid epoxy molding compound of similar size, thus enabling fine-pitch interconnects on FlexTrate™ without resorting to die pre-shift techniques [10-13].

3.2 Integration of 200 dies at 40 µm pad pitch

After the positive results of making flexible and reliable vertically corrugated interconnects and demonstration of maximum die shift of < 8 µm on FlexTrate™, we demonstrate the integration of multiple dies connected in daisy chains at 40 µm pad pitch on FlexTrate™ platform and test its flexibility.

The 40 µm pitch interconnects form a daisy chain connection to the underlying dies, which have 8×20 µm Au lines with corresponding 40 µm wire pitch and 20 µm pad size as shown in Fig. 3.6 (a). After dies were transferred to the 2nd handler, the deposited stress buffer layer acted as a low-k dielectric, which we used for forming the first RDL. Vias were etched through the stress buffer layers, as shown in Fig. 3.6 (b). The via diameter was measured to be ~18 µm over the 20 µm pad

size. Masked lithography was used with alignment marks on the dies for corrugations patterning, via etching, Cu interconnect plating and line passivation, as shown in Fig. 3.6 (c).

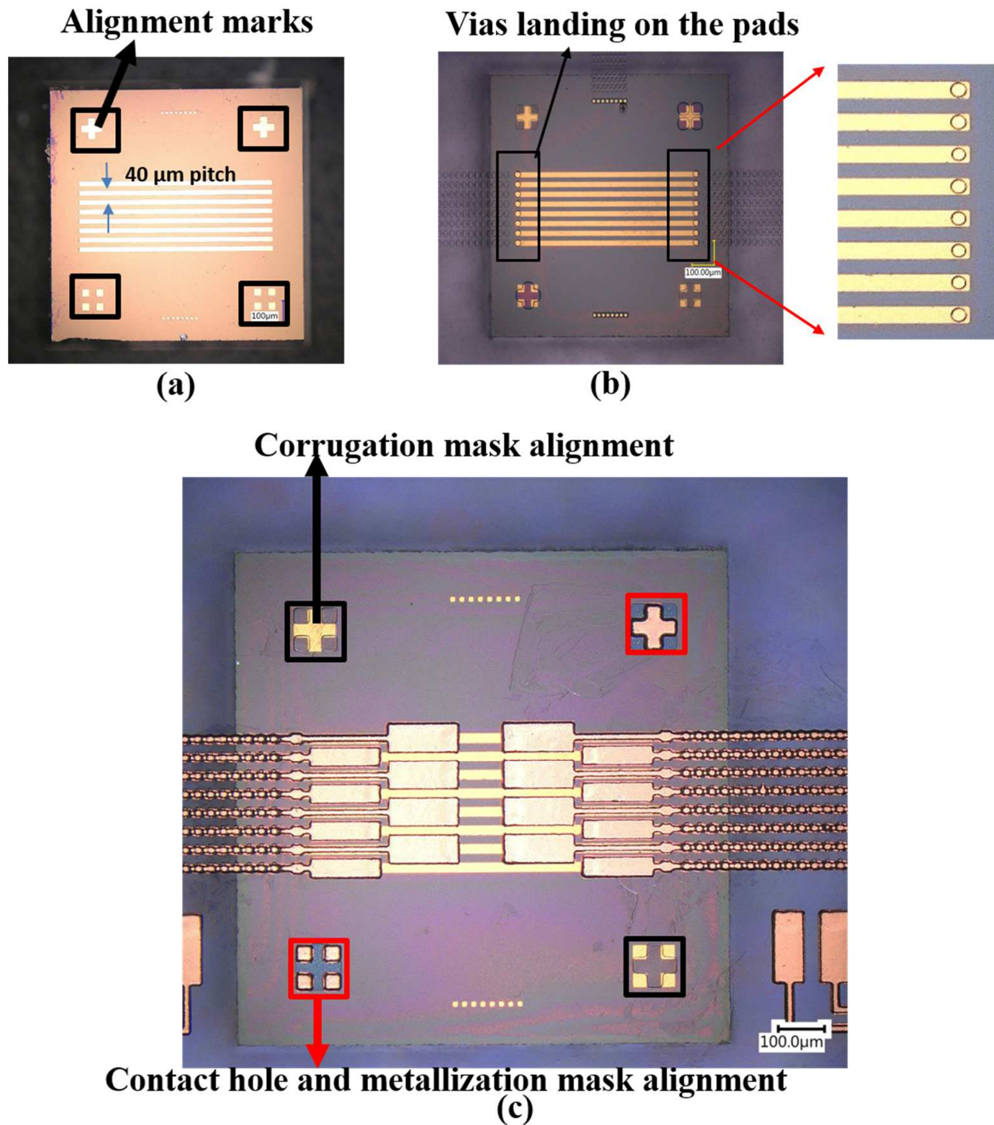

Figure 3. 6. (a) Fabricated 1 mm x 1 mm x 0.2 mm die with 8×20 µm Au lines at 40 µm pitch. Alignment marks for local fine alignment are shown in the black boxes (b) Contact vias etched through the buffer layers to contact the underlying 40 µm pitch lines on the dies. (c) Alignment mark design to obtain fine alignment using separate alignment marks for corrugations, via etching, and interconnect formation.

The placement accuracy of ± 1 µm was achieved while placing the dies on the 1st handler using a pick-and-place tool. A 10 × 20 array of 1 mm^2 dies were integrated at 1.8 mm die pitch with vertically corrugated Cu interconnects (~5 µm thickness) at 40 µm interconnect pitch, connected in daisy chains, as shown in Fig. 3.7 (a). The 200 dies were integrated over a 35 mm × 18 mm area. Magnified images of a Si die with pads and corrugated interconnects at 40 µm pitch are shown in Figs. 3.7 (b) and (c), respectively. The alignment marks near the corners of the die, (Fig. 3.7 (b)) were used for fine alignment during the different stages of the fabrication process.

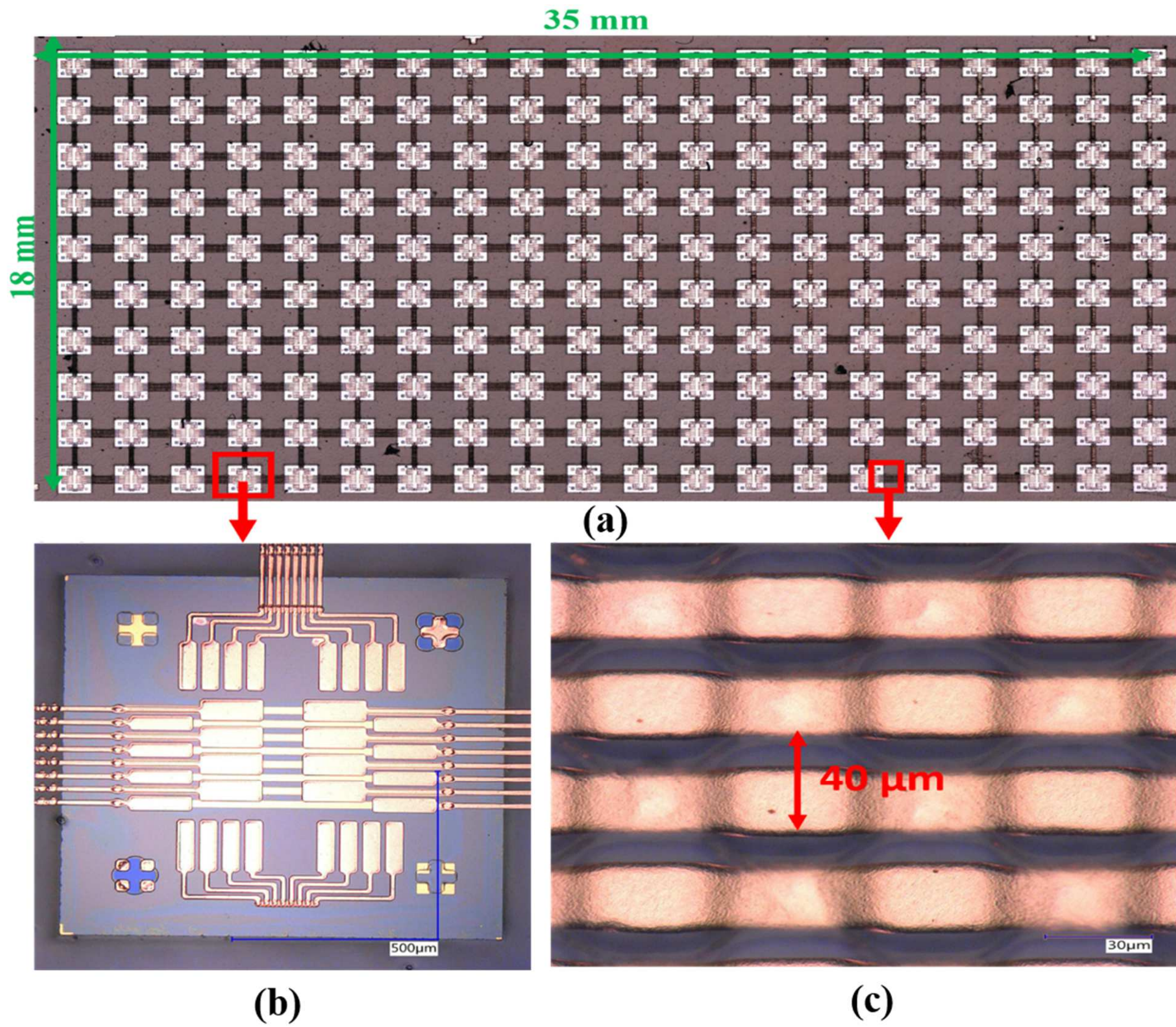

Figure 3. 7. (a) Image of 10×20 array of daisy chain connected dies on FlexTrate^{TM}. Magnified images of (b) a die with pads, and (c) corrugated interconnects with 40 µm pitch.

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3.2.1 Bending reliability test

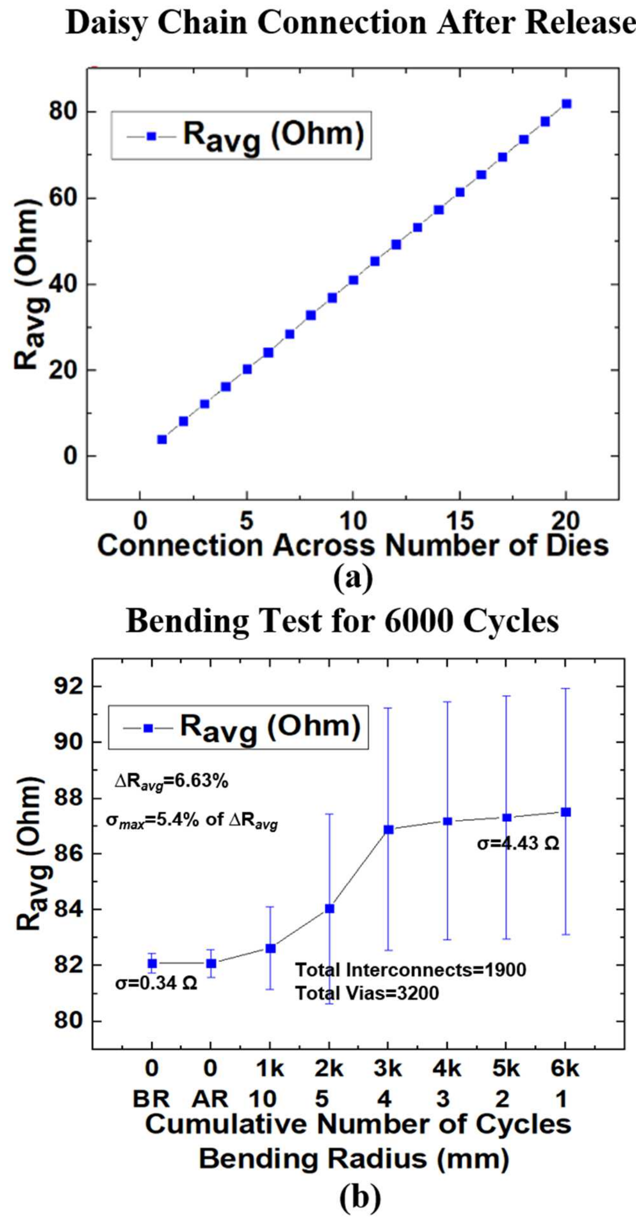

Figure 3. 8. Mechanical reliability plot for 10×20 dies connected at 40 μm interconnect pitch on FlexTrate™ in a daisy chain demonstrating (a) R_{avg} (Ω) vs. connections across number of dies, and (b) R_{avg} (Ω) for different bending conditions. The increase in resistance is due to the microcracks generation and propagation in the interconnects upon the cyclic bending.

The 10 x 20 array of dies has total of 1520 interconnects and 3200 vias. The resistance was measured using a four-point probe across the 20 dies for each of the 10 rows and the average resistance (R_{avg}) was plotted, as shown in Fig. 3.8 (a). R_{avg} linearly increased with the number of dies as expected, with maximum standard deviation (σ_{max}) = 0.23 Ω. The linear increase in resistance signifies that good alignment was achieved for connecting the 40 µm pitch metal lines on the dies with 40 µm pitch corrugated interconnects on FlexTrate™ over the 35 mm ×18 mm area. The end-to-end resistances were measured across 20 dies for a total of 80 connections BR and AR of FlexTrate™, as well as after cyclic bending at 10, 5, 4-, 3-, 2-, and 1-mm bending radii for 1000 cycles each. The plot of R_{avg} with standard deviation (σ) is shown in Fig. 3.8 (b), with $\Delta R_{avg} < 7$ % and $\sigma_{max} < 5.5$ % of R_{avg}, and no failure of interconnects. The increase is resistance is due to the microcracks generation and propagation in the interconnects upon the cyclic bending [14, 15]. Moreover, these results demonstrate the mechanical reliability of FlexTrate™ under repeated bending to small bending radii.

3.3 Foldable display

After the promising result demonstrating the integration of 200 dummy Si dies connected at 40 µm pad pitches in daisy chains, and the cyclic bending study demonstrating its reliability, we demonstrate the integration of off-the-shelf active components on our FlexTrate™ platform. For this, we integrated commercially available LEDs on the FlexTrate™ platform in the form of a 7-segment foldable display and tested its flexibility.

3.3.1 LED solder removal

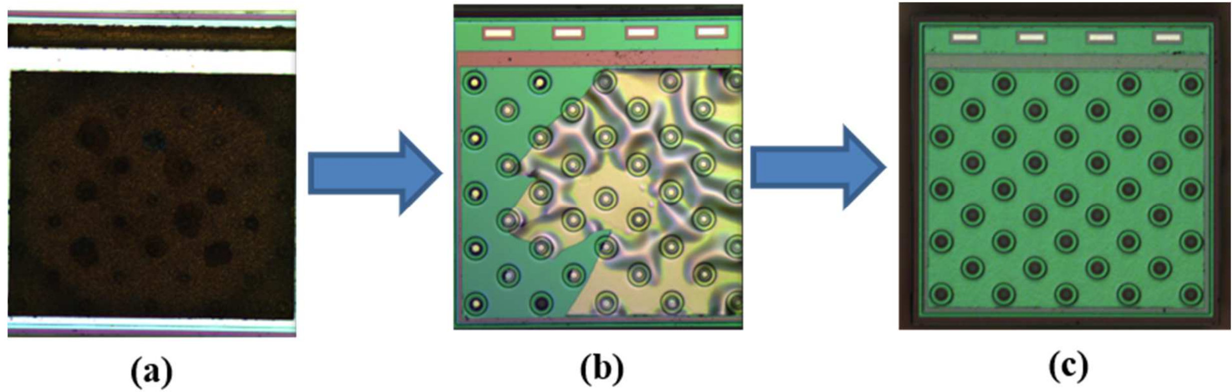

Figure 3. 9. Image of the actual LED pads with (a) solder, (b) LED dipped in aqua-regia for 120 s where the solder was partly removed, and (c) LED dipped in aqua-regia for 300 s where the solder was completely removed. After the removal of the solder, the LED dies were integrated into the FlexTrate™.

The commercially available LEDs (DA 1000, Cree Inc.) had solder termination which needed to be removed to allow for direct metallization on the metal pads of the LEDs through the FlexTrate™ process. For this, the LEDs were dipped in aqua-regia for 300 s. Fig. 3.9 shows the solder removal from the LED with help of aqua-regia.

3.3.2 Design and integration

The design of the 7-segment display with 42 commercially available, 335 µm thick, 1 mm^2, InGaN blue/green LEDs on the 1st handler is shown in Fig. 3.10. The LEDs in each segment were placed using 3 mm placement pitch to allow for higher flexibility. Moreover, 200 µm thick, 1 mm^2 Si dies with alignment marks were used to help in alignment during the fabrication process. The fabricated FlexTrate™ sample of the 7-segment foldable display over a 37 mm × 52 mm area is shown in Fig. 3.11 (a). Each segment of the 7-segment display had 6 LEDs connected in parallel using

corrugated Cu interconnects at 40 µm pitch, as shown in Fig. 3.10 (b) and (c) respectively. A 2.54 mm pitch connector was soldered to the pads to externally connect the 7-segment display to a microcontroller. The LEDs were powered using a power supply under current compliance of 200 mA. A display of "UCLA CHIPS" as an example, where each letter was displayed one at a time on the foldable display, is shown in Fig. 3.11 (d). Furthermore, the complete folding of the display integrated with green LEDs, is shown in Fig. 3.12.

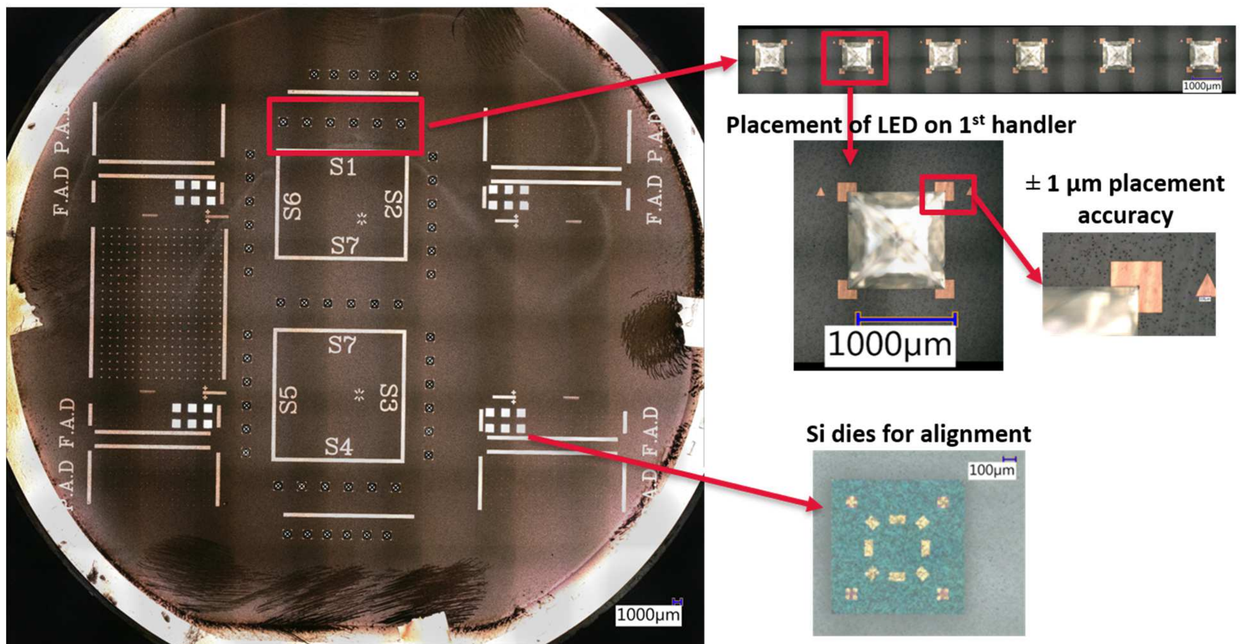

Figure 3. 10. (a). Placement of dies on 1st handler for the 7-segment display.

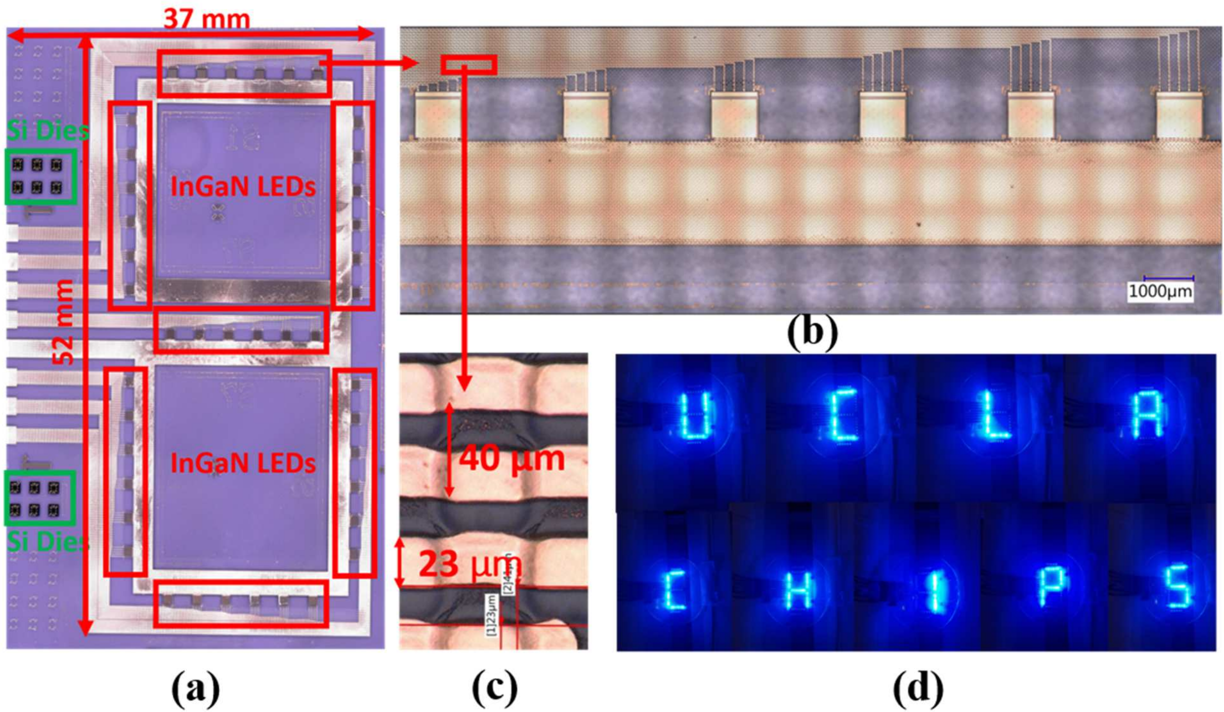

Figure 3. 11. (a) Foldable display with 42 LEDs on FlexTrate™ in the form of 7-segment display along with embedded Si dies for accurate alignment purposes demonstrating a truly heterogeneous integration, (b) magnified image of a segment of the 7-segment display consisting of six LEDs, (c) magnified image of 40 μm pitch corrugated interconnects, and (d) programming of the 7-segment display to show "UCLA CHIPS" as an example, where each letter was displayed one at a time on the foldable display.

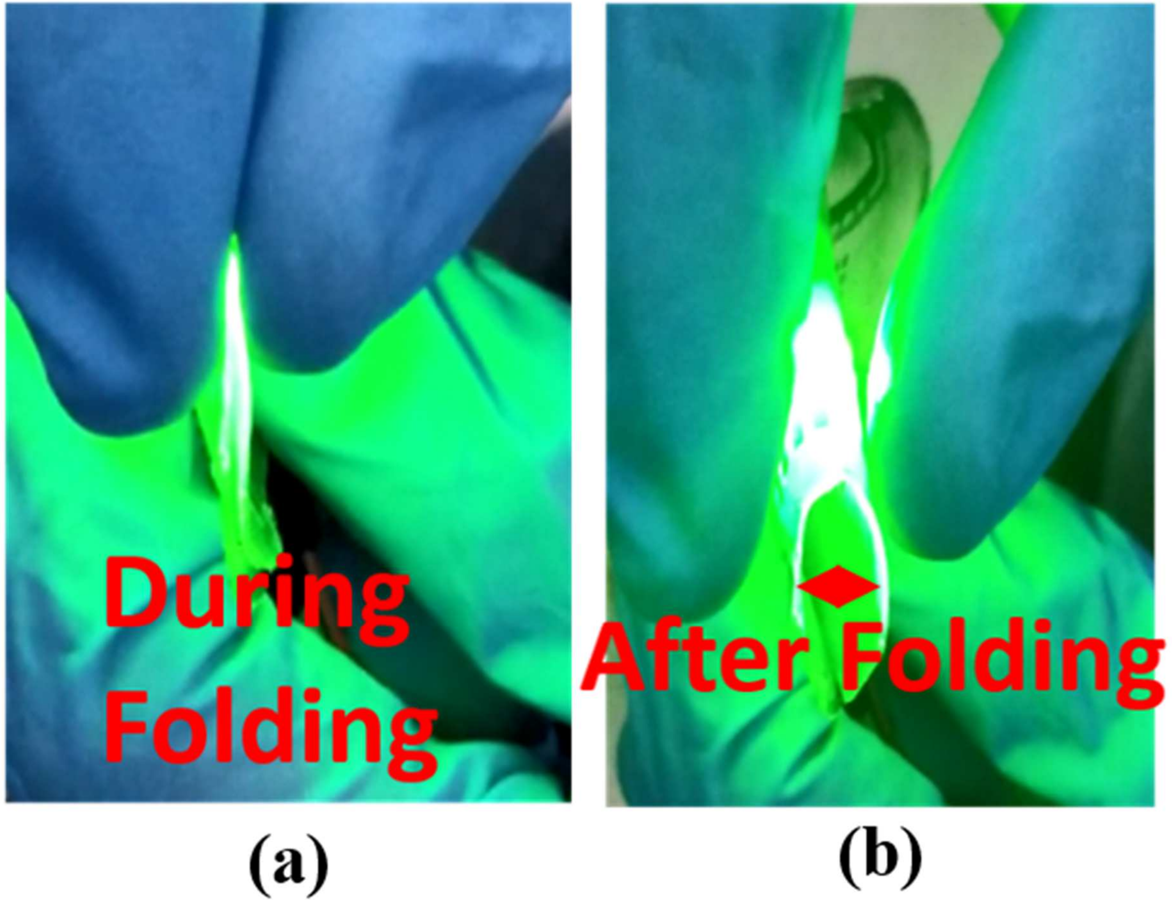

Figure 3. 12. Image of the foldable display (a) during folding (bending radius = 0 mm) and (b) after folding (bending radius > 0 mm). The green LEDs remain illuminated throughout the folding process.

3.3.3 Bending reliability test

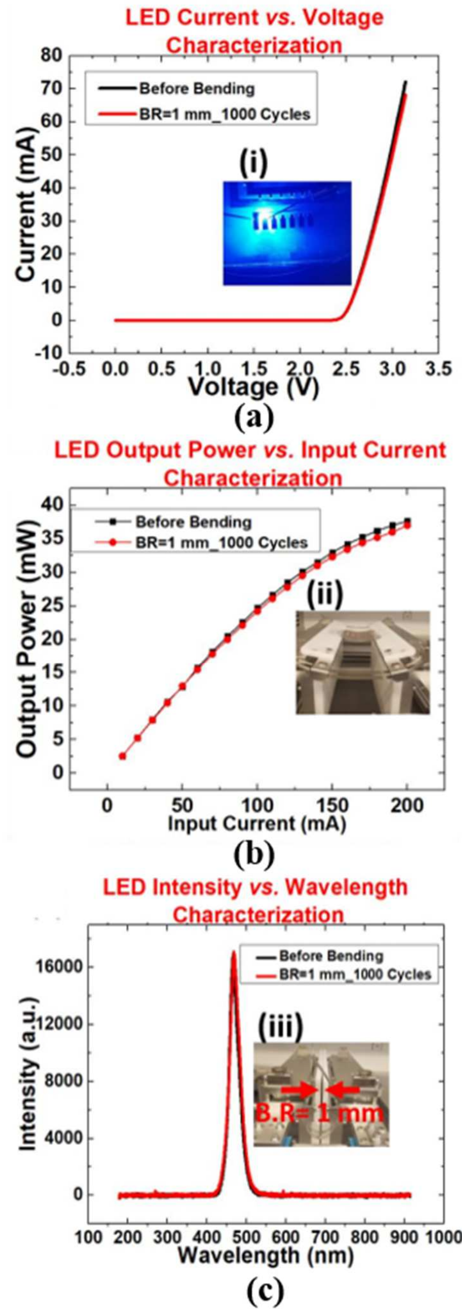

Figure 3. 13. Plots of the characterization of blue LEDs embedded in the fabricated foldable display before and after bending to 1 mm bending radius for 1000 bending cycles, for (a) current (mA) vs. voltage (V), (b) output power (mW) vs. input current (mA), and (c) intensity (a.u.) vs. wavelength (nm) at 100 mA.

The current (mA) vs. voltage (V), output power (mW) vs. input current (mA), and intensity (a.u.) vs. wavelength (nm) at 100mA were measured for the blue LEDs integrated on FlexTrate^{TM} before and after bending at 1 mm bending radius for 1000 bending cycles, as shown in Fig. 3.13 (a), (b), and (c), respectively. The output power of the LEDs was measured using lenses to collimate the light to a photodiode power sensor (S120VC). The spectra from the LEDs were measured using a spectrometer (Ocean Optics USB4000) which covers the range of 200 - 1100 nm. The measurement was done through free space and the photodiode, which has a detector wavelength range of 200–1100 nm, was set to measure the specific wavelength acquired from the spectrometer. The current vs. voltage characterization demonstrated that the resistance of the interconnects connecting the LEDs does not experience any significant change upon bending. The output power vs. input current and intensity (a.u.) vs. wavelength characterizations demonstrated that the PDMS has similar transparency before and after bending. Post bending, the LEDs exhibit similar characteristics, and interconnects, pads, and dies do not delaminate, demonstrating that the package is very reliable even under cyclic bending at extreme bending radii. Such a system can be scaled up to manufacture high density, full-colored, highly flexible displays in the future.

3.3.4 Thermal dissipation analysis

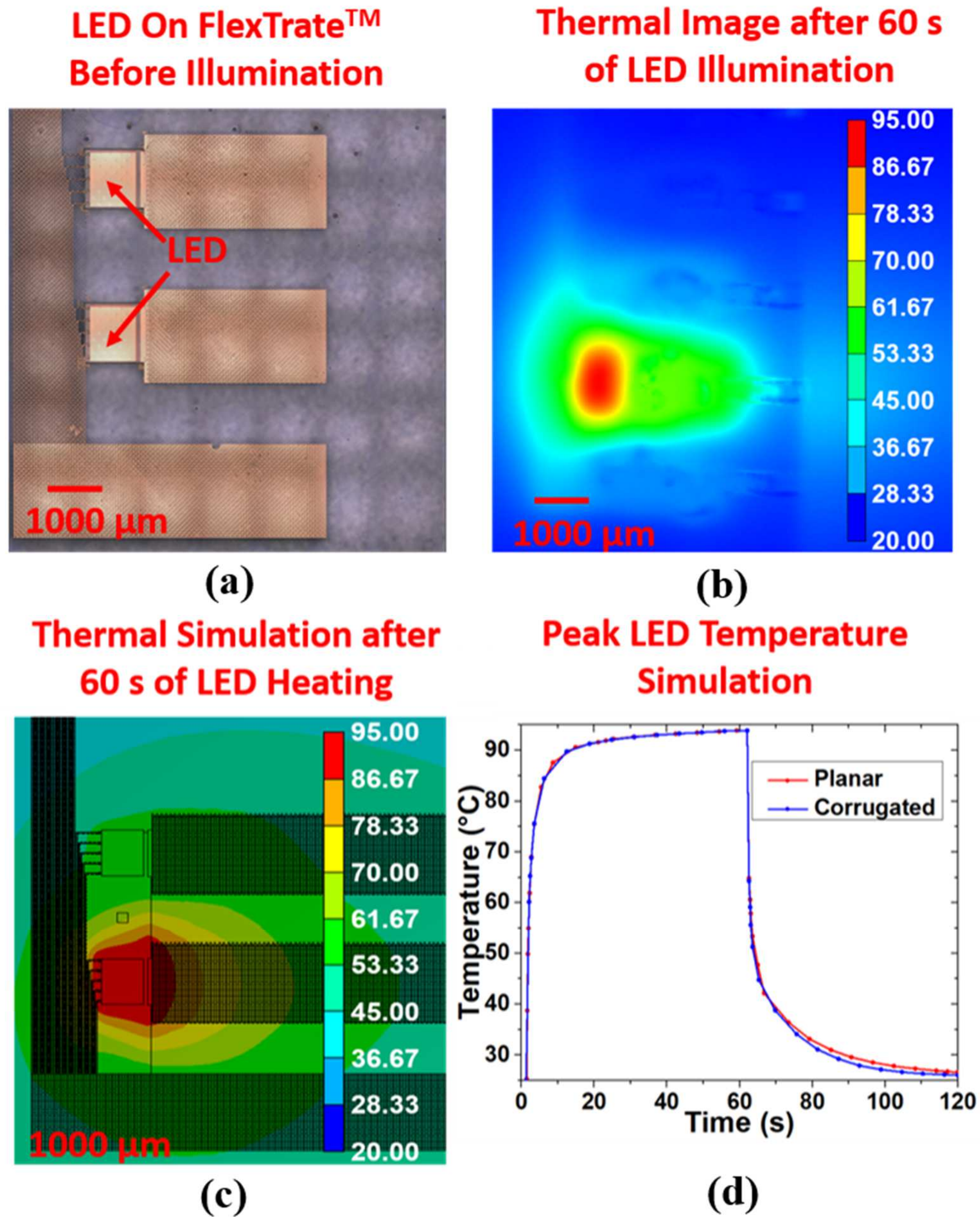

Figure 3. 14. (a) Optical image of the sample under test. Thermal image after 60 s of illumination of a single LED at 100 mA during (b) experiment and (c) simulations, which demonstrate the heat spreading along corrugated interconnects, and (d) simulations evaluating peak temperature of LED over time for planar vs. corrugated interconnects, where the LED reaches ambient temperature in 114 s with planar interconnects vs. 100 s with corrugated interconnects.

The dissipation of heat was analyzed through the foldable display on FlexTrate^{TM}. The image of the sample with LEDs before illumination is shown in Fig. 3.14 (a). One LED was illuminated by passing 100 mA current for 60 s to reach near-steady state temperature. The current supply was then removed, and the sample was allowed to cool under ambient conditions for 60 s. For Finite Element Analysis (FEA), a model based on the experimental setup was used. A convection coefficient of 20 W/m^2 was applied to the outward-exposed faces of the model. To analyze how heat propagated through FlexTrate^{TM} and dissipated under ambient conditions, the temperature of the center LED was set to the peak measured temperature of the first 60 s of the experiment as an isothermal constraint. The temperature constraint was then removed, at which point heat conduction and convection were the only two mechanisms for heat transfer in the model. The thermal profile and peak temperature of the model were observed for an additional 60 s under this condition. Figs. 3.14 (b) and (c) show the surface thermal profile after 60 s of illumination of the LED for experiment and simulation, respectively. The thermal image was taken using a FLIR A655sc high resolution infrared camera. The surface temperature distribution from the simulation results was similar to the experimental results. The simulation was performed again under identical conditions with planar interconnects replacing corrugated interconnects. Fig. 3.14 (d) shows the simulated peak temperature in the LED comparing the heat dissipation through planar vs. corrugated interconnects. Based on the experimental and simulated data, it was observed that the Cu pads and interconnects act as heat spreaders. Heat dissipation occurred primarily through the Cu. In addition, the use of corrugated Cu interconnects increased the surface-to-volume ratio allowing for 12.3 % faster cooling of the LED to ambient temperature compared to planar interconnects.

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4. Multi-channel FlexsEMG System

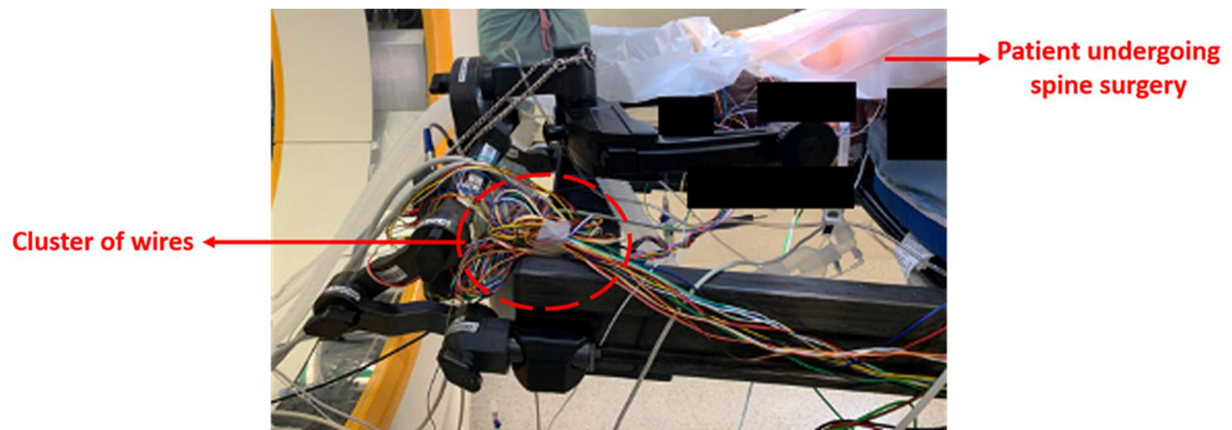

Figure 4. 1. A typical wiring harness during an IONM requisition during spine surgery. The FlexsEMG system will remove the cluster of wires. (Picture courtesy: Dr. Luke Macyszyn)

After successfully demonstrating 200 dies integrated at 40 µm pad pitches and a foldable display, we demonstrate a fully integrated multi-channel wireless sEMG system on FlexTrate^{TM} called "FlexsEMG".

Complex neurological surgery involves surgical incisions near the brainstem, spinal cord, cortex, and neuromuscular junctions with a substantial chance of nerve injury during surgery. Intra-Operative Neurological Monitoring (IONM) utilizes cranial as well as peripheral biopotentials in combination with Motor Evoked Potentials (MEP) measured using wired sEMG sensors to provide real-time, outcome-sensitive injury monitoring to surgeons [1]. This allows them to avoid nerve injury and subsequent post-surgical disability. However, existing IONM systems are bulky, expensive, and have a cluster of wires (Fig. 4.1), making surgery more difficult and requiring extensive manual monitoring [2]. Further, the need to readjust sensor positions when the patient is moved, adds additional time and cost to surgeries. This increases the probability of blood loss, sepsis, contamination, and complications due to surgeon fatigue. Thus, there is a need to develop

a flexible, sterilizable and reusable wireless sEMG device for IONM which can replace current systems and improve patient outcomes by reducing the duration and complexity of surgery. Additionally, this device may be used for ambulatory post-operative therapeutics and rehabilitation as well.

4.1 Introduction to sEMG

Locomotor function of the human body is driven through coordinated engagement of the neuromuscular control mechanism. It consists of the central nervous system and the skeletal muscular system. Action potential is the ionic current that drives the muscular activation. The degree and intensity of muscle contraction is a function of recruitment of motor units. A motor unit consists of motor neurons and the muscle fibers they are directly synapsed to via the neuromuscular junction. Motor neurons interact with skeletal muscles at the neuromuscular junction through which the muscle activation is generated [3-8]. Intensity of muscle activation and generation of strength at the joint is modulated through the recruitment of motor units [3-6]. The electromyograph records the muscle level spread of motor endplate potential during muscle activation [5-7].

For the last three decades, sEMG has been used in various domains ranging from medical research and injury rehabilitation to sports science and human machine interfaces. Romaniszyn et al. concluded that sEMG can be used to accurately identify the innervation zones of the Gracilis muscles [8]. SEMG has been used successfully in clinical gait analysis where it has been utilized for both, functional diagnosis as well as analysis of therapeutic outcomes [9-11]. Numerous conditions, including but not limited to, stroke, cerebral palsy, and ligament injuries require the use of sEMG in the treatment procedures [9]. Although a single channel can record accurate

recordings from the target muscle, by using multiple channels the spatial accuracy can be increased and a larger topographical muscle area can be covered in order to understand the spread of EMG activity throughout muscle groups [8, 12]. This has allowed multi-channel sEMG to be used in fields like gesture recognition and fatigue analysis [7, 13]. Using modern machine learning and deep learning methods on the acquired signals, sEMG can be used to develop fully functional real-time controllable prosthetics. Moreover, since there is no constraint on the muscles that can be analyzed for this purpose, even disabled people with amputations can be used to train the models for higher accuracy and usability [14]. One major application of multi-channel sEMG is the calculation of Muscle Fiber Conduction Velocity (MFCV) [15-17]. This is possible when these channels are placed in a linear array along the path of the action potential in the muscles. MFCV refers to the speed of an action potential as it travels through muscle fibers. With constant exertion in muscles, the firing rate of motor neurons changes which directly affects the action potential trends in the muscle. Multi-channel sEMG can capture these changes over time and hence is widely used in fatigue detection studies [15, 18].

4.2 Vertically corrugated electrode design

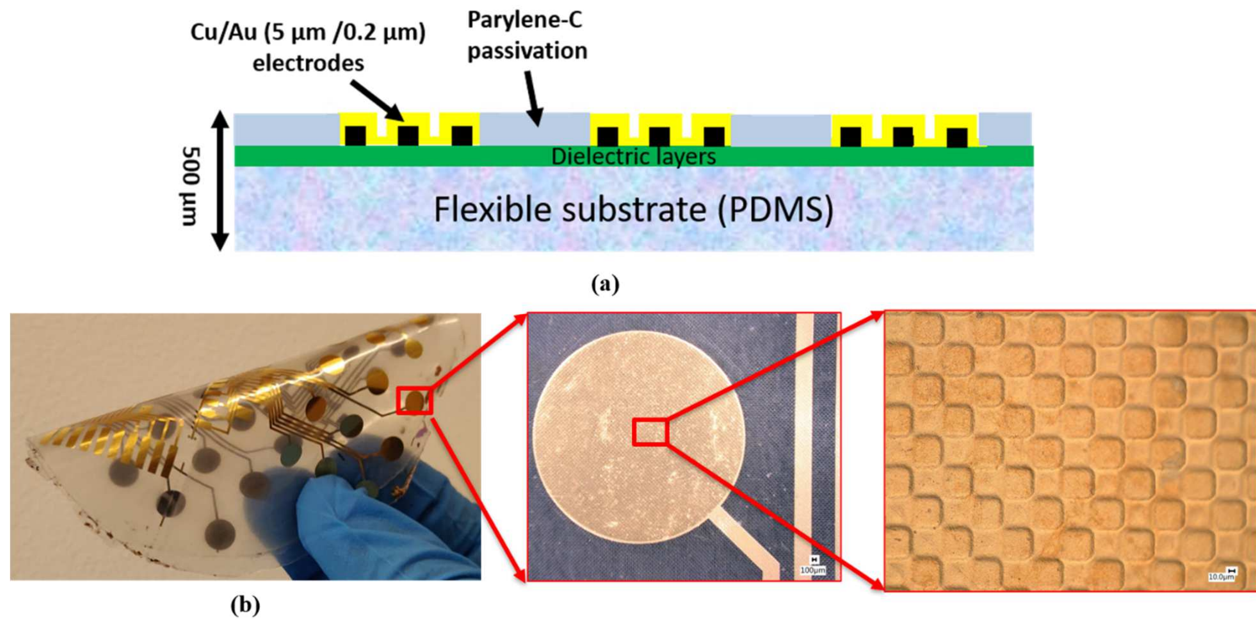

Figure 4. 2. (a) The schematic of the fabricated sEMG electrodes on FlexTrate^{TM}. The images show (b) bent vertically corrugated gold capped copper sEMG electrodes on FlexTrate^{TM}.

Using the standard FlexTrate^{TM} process flow, the sEMG electrodes were fabricated in 3x3 arrays using 40 nm/5000 nm Ti/Cu capped with 20 nm/200 nm of Ti/Au for biocompatibility. The schematic of the electrodes on FlexTrate^{TM} is shown in Fig. 4.2 (a). Flexibility of the FlexTrate^{TM} platform allows the electrodes to conform intimately to the skin. The versatility of the platform is demonstrated in Fig. 4.2 (b), where it is bent in forms that competing platforms may find difficult to replicate [19, 20].

Selection of the electrode size, shape, material, and inter- electrode distance is critical for obtaining high signal-to-noise (SNR) ratio and reducing measurement artifacts such as DC potential and environment noise [21]. Moreover, for large high density (HD)-sEMG electrode arrays, and smaller electrode sizes, amplifiers must deal with relatively high electrode impedances.

FlexTrate^{TM} allows integration of low impedance electroplated electrodes, rather than printed conductive inks, with integrated CMOS based multi-channel amplifier die(s), and low resistance interconnects at fine pitches, unmatched by today's printing techniques [22]. The FlexTrate^{TM} electrodes in each array have diameters of 4 mm, 5 mm, and 6 mm [23].

4.2.1 Electrode configuration

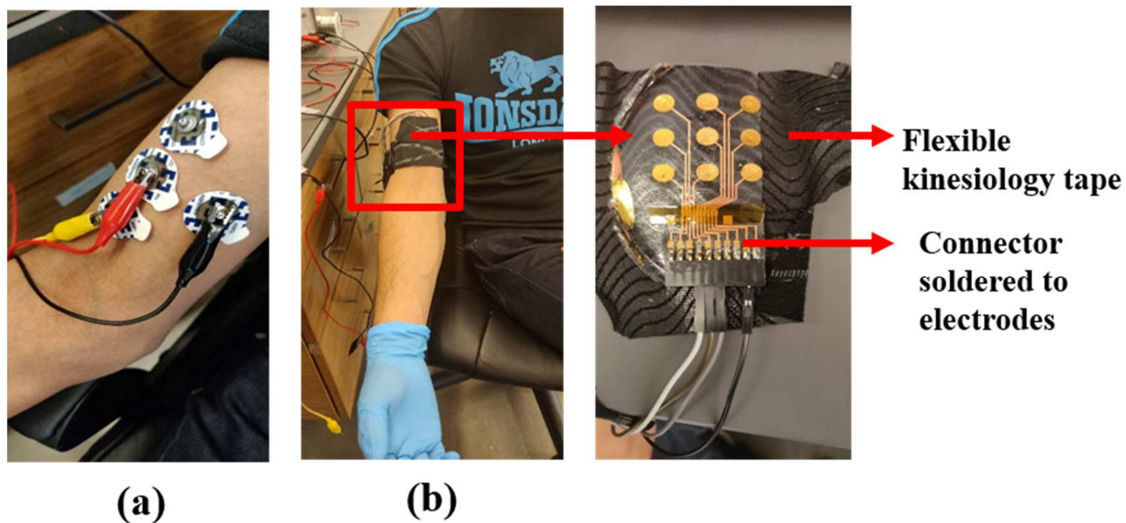

Figure 4. 3. Image of the attachment of (a) Ag/AgCl electrodes and (b) FlexTrate^{TM} electrodes on the bicep muscles.

In this study, 3 electrodes were used to record one-channel sEMG signal, where 2 electrodes were connected in a bipolar configuration and the 3rd electrode was the reference. Commercially available biocompatible conductive gel was applied on the electrodes for ease of contact to the biological surfaces. A high-pass filter with cut-off frequency at 5 Hz was used to remove the low-frequency noise, movement artifacts, and DC potentials, and a low pass filter with cut-off frequency at 500 Hz was used to remove the high-frequency noise, as sEMG signals have a frequency range between 5-500 Hz [24]. The instrumentation amplifier (INA129) was integrated

with a 100 Ω resistor to function as a differential amplifier with gain of 500 and 0.1 μF capacitors, 3.3 kΩ, 330 kΩ resistors, and Op-amp (LM324) together function as sEMG signal filters. The performance of commercial gel-based Ag/AgCl electrodes, which consist of a dry electrode component (Ø = 7 mm) and a layer of conductive gel and adhesive (Ø = 24 mm), was compared to the performance of the FlexTrate™ electrodes by recording the muscle-flexing activity.

The Ag/AgCl electrodes were attached to the biceps of the subject as shown in Fig. 4.3 (a). Alligator clips were used to connect the Ag/AgCl electrodes to the circuitry on the breadboard. To attach the FlexTrate™ electrodes on the bicep muscles of the subject, an external flexible kinesiology tape was used, as shown in Fig. 4.3 (b). A connector was soldered to the electrodes on FlexTrate™ and jumper wires were used to connect the FlexTrate™ electrode array to the circuitry on the breadboard, as shown in Fig. 4.3 (b).

4.2.2 Muscle signal

The muscle signal captured by the Ag/AgCl electrodes and 4 mm, 5 mm, and 6 mm diameter FlexTrate™ electrodes is shown in Fig. 4.4 (a), (b), (c), and (d), respectively. For the FlexTrate™ electrodes, the amplitude of the muscle signal increased with the increase in electrode diameter, which is in agreement with literature [25]. Moreover, the 6 mm diameter FlexTrate™ electrodes were able to capture similar muscle signals compared to the commercial Ag/AgCl electrodes.

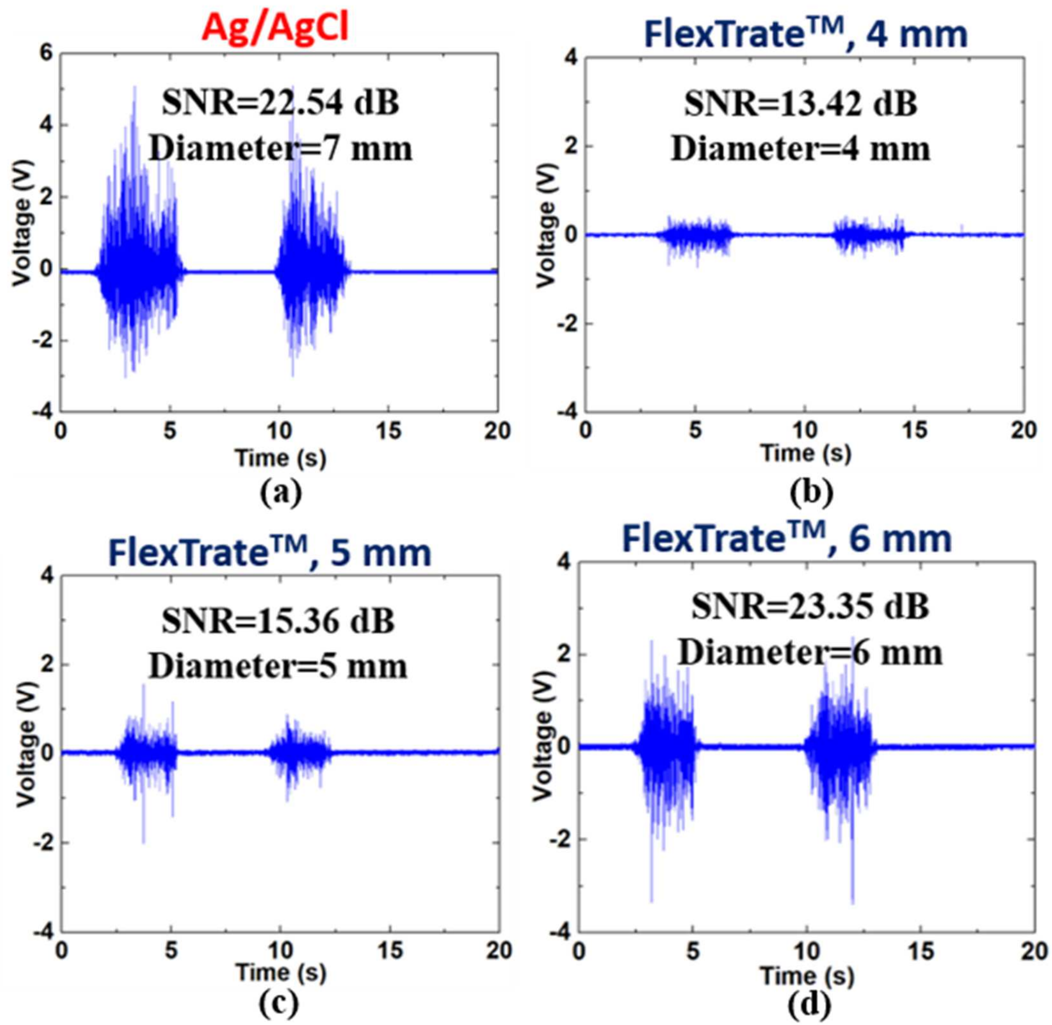

Figure 4. 4. The SNR of (a) standard Ag/AgCl electrodes and FlexTrate™ electrodes of diameter (b) 4 mm, (c) 5 mm, and (d) 6 mm.

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4.2.3 Spatial resolution

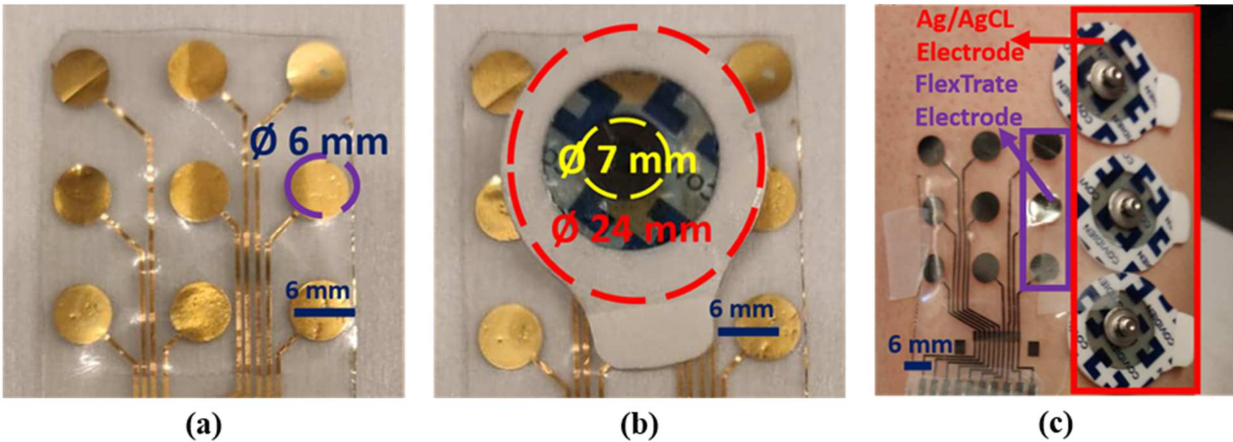


Figure 4. 5. (a) Image of a fabricated 3x3 array of electrodes on FlexTrate^{TM} with 6 mm diameter and 12 mm inter-electrode distance. (b) The image shows a size comparison of our electrode array with a commercially available Ag/AgCl electrode. (c) Image shows ~5X reduction in size for 3 FlexTrate^{TM} electrodes compared to 3 Ag/AgCl electrodes.

Spatial information of the muscle activation is an important part of the study related to muscular activity. Hence the electrodes were designed in an array configuration which increases the number of recording positions to gain spatial information concerning the distribution of EMG activity over a muscle, or the timing relationships between different muscle firing events. For HD-sEMG arrays, literature suggests that only certain array geometries and recording configurations can yield useful spatial and temporal information about the muscle unit action potential (MUAP), peak identification, and the MFCV [26]. To reliably record muscle activation signals, a 3x3 array of 6 mm diameter electrodes and 12 mm inter-electrode distance was designed. Fig. 4.5 (a) shows a fabricated electrode array architecture on FlexTrate^{TM} and Fig. 4.5 (b) shows a size comparison of the FlexTrate^{TM} electrode array with a commercially available Ag/AgCl electrode. One FlexTrate^{TM} electrode had 6 mm diameter compared to 24 mm diameter of Ag/AgCl electrode. Fig. 4.5 (c) compares the area of 3 FlexTrate^{TM} electrodes with 3 Ag/AgCl electrodes, where it

was clearly observed that FlexTrate^{TM} electrodes provide > 5X reduction in area. Owing to the reduced size, the FlexTrate^{TM} electrodes can be used for making HD-sEMG electrode arrays.

4.2.4 Post-processing

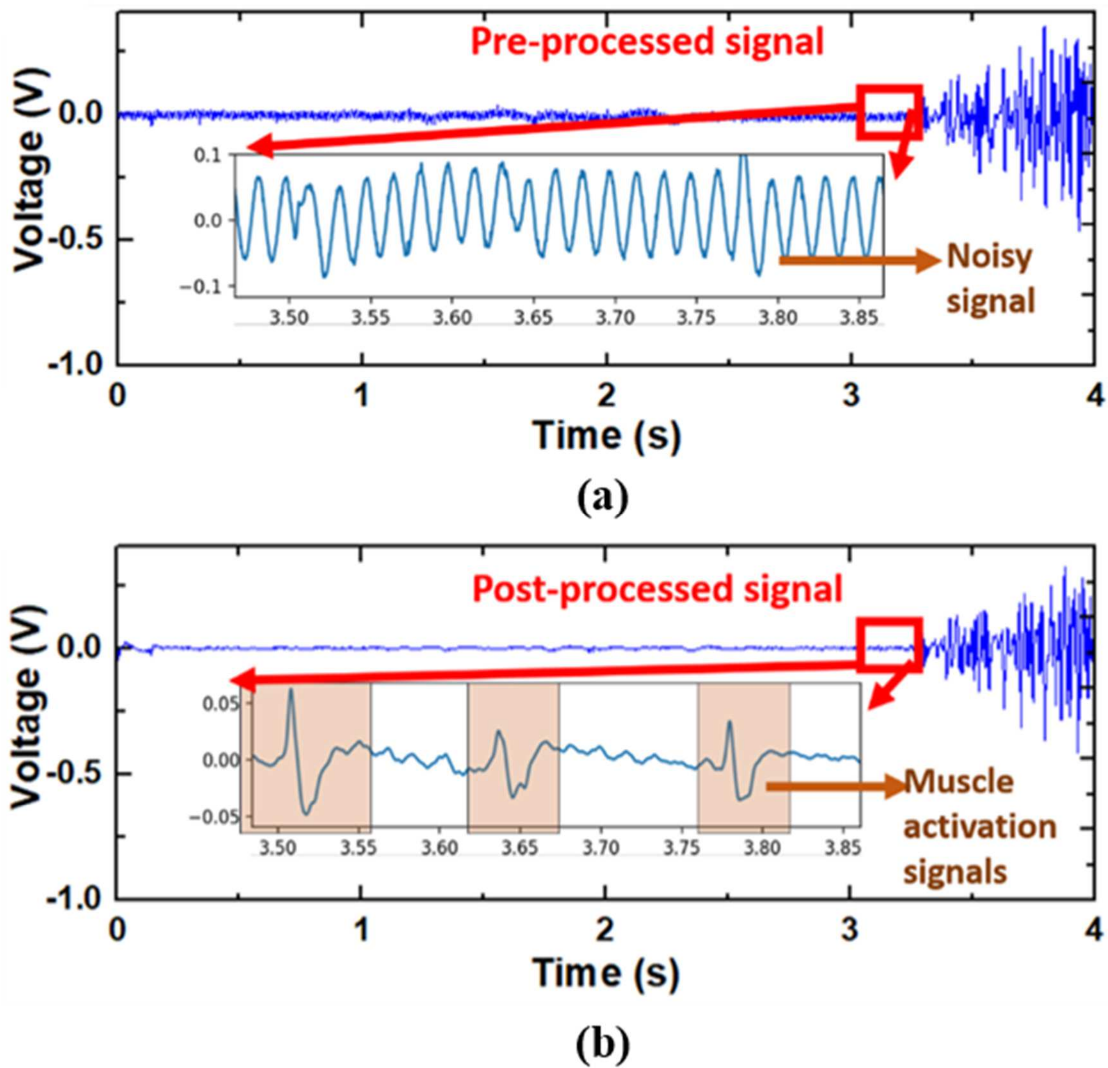


Figure 4. 6. The pre- and post-processed signals received wirelessly are shown in (a) and (b), respectively. The inset of the pre-processed signal is noisy, whereas the inset of the post-processed signal shows the signature of muscle activation.

The muscle components of interest were relaxed for the first 3 s of recording to establish a baseline and then flexed for 5 s under a static load of 4.5 kg. The sEMG signal was sent over Bluetooth at 4 kHz sampling rate. The ISP1807 was used as the Bluetooth module. It uses Bluetooth Low Energy (BLE) which is a low powered Bluetooth for IoT applications. To improve the sEMG signal, the received signal was post-processed, first by signal smoothing using a mean filter of width 2.5 ms followed by Butterworth bandpass filter of 9th order to remove frequencies below 5 Hz and above 500 Hz, and a 60 Hz notch filter with quality factor Q=30 to remove the capacitively coupled ac supply noise. The pre- and post-processed signals received wirelessly are shown in Fig. 4.6 (a) and (b), respectively. The inset of Fig. 4.6 (a) shows a noisy baseline; however, the muscle activation can be clearly seen in the inset of Fig. 4.6 (b). The baseline noise and oscillations are observed to be suppressed by post-processing. The post-processing protocol filtered the raw signal to accentuate the signature of the muscle activation. This indicated that the FlexTrate™ electrodes coupled with standard post-processing borrowed from literature were capable of recording biologically meaningful signals.

4.2.5 Reliability

To test the reliability of the sEMG electrodes fabricated on FlexTrate™ bending, temperature-humidity, thermal-cycling, and saline immersion tests were performed on them. During the bending test, the electrodes were bent for 1000 bending cycles at each bending radius from 10 mm down to 0.5 mm. For temperature-humidity, thermal-cycling, and saline-immersion tests, the samples were kept at 85 □/85 % Relative Humidity (RH) for > 500 hours, -40 □ to 125 □ for 30 cycles, and in Phosphate Buffered Saline (PBS) solution at room temperature for > 200 hours, respectively. The results for these tests are shown in Fig. 4.7. The change in average resistance

post bending, temperature-humidity, thermal-cycling, and saline-immersion tests were measured to be 2.1 %, 2.47 %, 3.1 %, and 3.88 %, respectively.

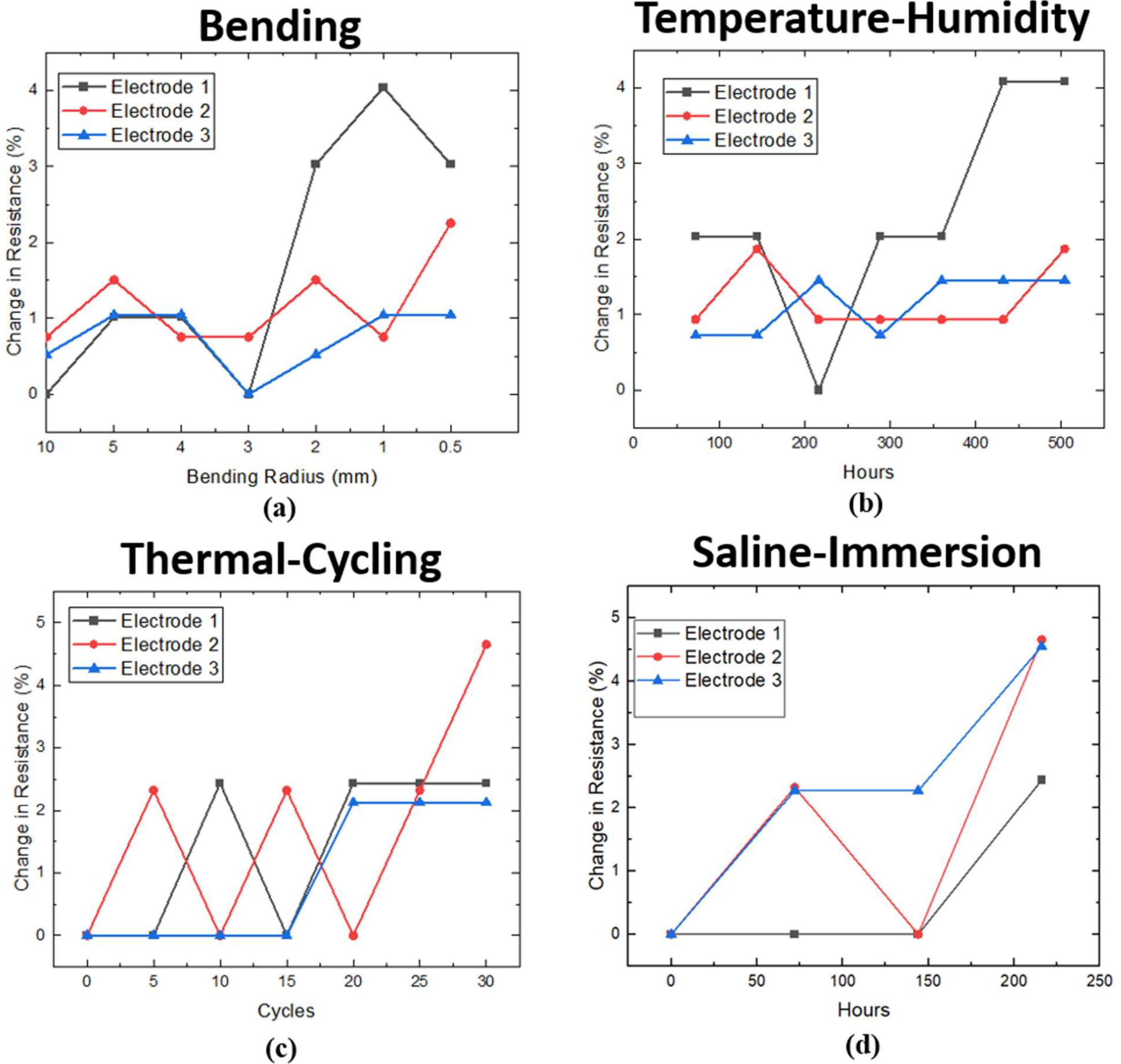


Figure 4. 7. Results of reliability tests on sEMG electrodes on FlexTrate^{TM} including (a) bending, (b) temperature-humidity, (c) thermal-cycling, and (d) saline-immersion tests.

4.3 FlexsEMG system: One-channel

4.3.1 Fabrication

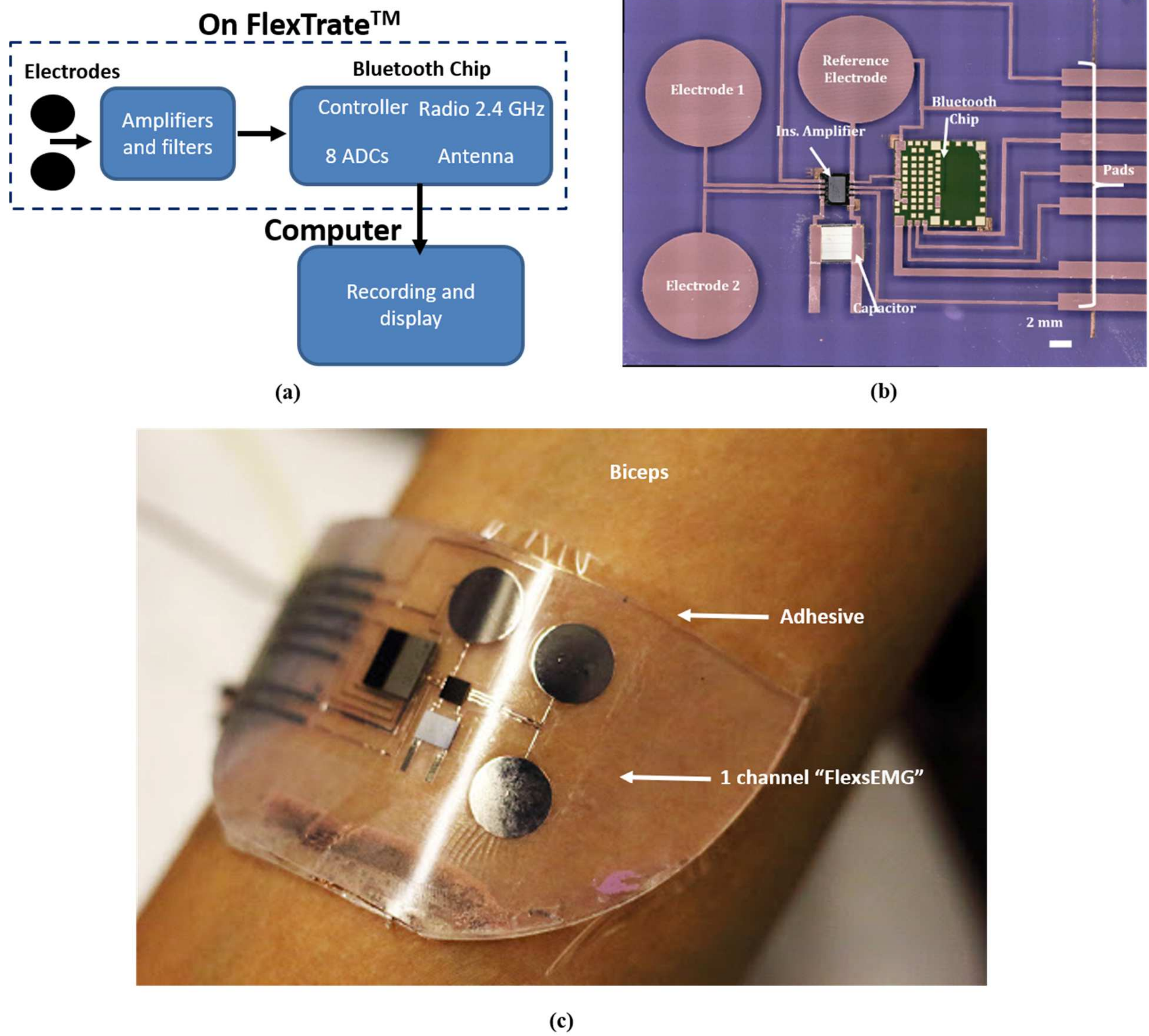


Figure 4. 8. (a) Simplified block diagram of the one-channel FlexsEMG system, (b) magnified image of integrated electronics in the FlexsEMG system, and (c) image of the one-channel FlexsEMG system attached to the bicep muscle of a subject.

After testing the flexible, Au capped copper electrodes on FlexTrate^{TM}, we integrate a simple bipolar configuration one-channel sEMG system on FlexTrate^{TM} and test the system. For this, INA 333 with 3.3 μF bare die capacitor was used as the instrumentation amplifier. ISP 1807 was used as the Bluetooth module. The amplified and filtered sEMG signal from the instrumentation amplifier was fed to the ADC of the ISP 1807 Bluetooth chip that digitized the signal and sent it wirelessly to a computer over Bluetooth communication. A simplified block diagram of the electronics is shown in Fig. 4.8 (a). The image of the one-channel sEMG system on FlexTrate^{TM} post fabrication is shown in Fig. 4.8 (b). The overall thickness of the one-channel FlexsEMG system is 2 mm in order to reliably integrate the 1 mm thick ISP 1807. An adhesive tape was used to secure the sEMG module firmly on the muscles as shown in Fig. 4.8 (c). The muscles were flexed, and the signals were recorded from the FlexsEMG as well as Ag/AgCl electrodes for comparison.

4.3.2 Recording of muscle signals

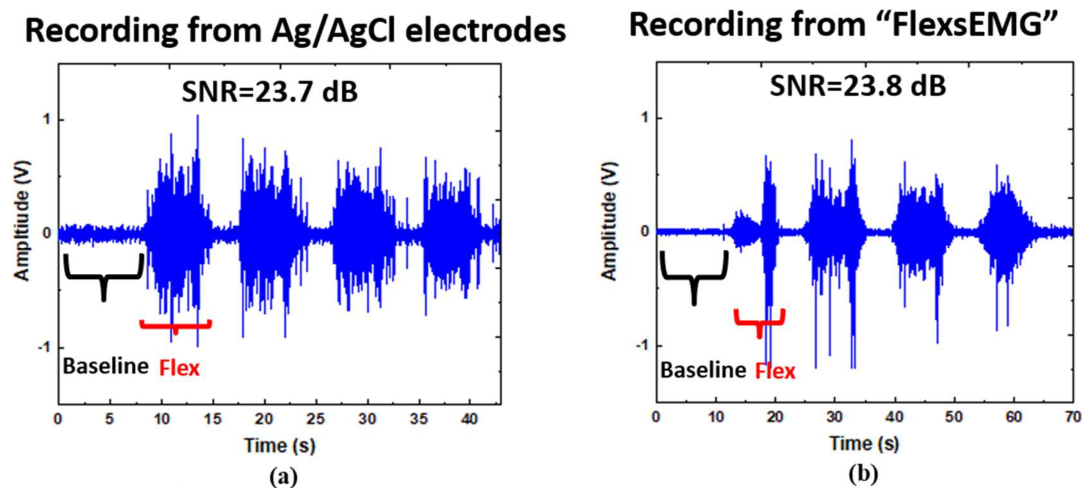


Figure 4. 9. sEMG signals captured by (a) Ag/AgCl electrodes and (b) one-channel FlexsEMG patch.

The sEMG signals acquired by the one-channel FlexsEMG were compared to the gold standard Ag/AgCl electrodes. The electronic circuitry for the Ag/AgCl electrodes were on the breadboard. The sEMG signals from the physiological motions where the subject rested the arm for baseline signal and then held a 4.5 kg weight to flex the bicep muscles and repeated this cycle 4 times were well captured by both Ag/AgCl electrodes and the FlexsEMG patch, as shown in Fig. 4.9 (a) and (b), respectively. The SNRs evaluated from the EMG signals captured during muscle activation from the Ag/AgCl (23.7 dB) system and the FlexsEMG patch (23.7 dB) were similar.

4.4 FlexsEMG system: Multi-channel

After successfully integrating the Au capped vertically corrugated copper electrodes along with the amplifier and Bluetooth module on the FlexTrate^{TM} platform, we integrate a multi-channel FlexsEMG system, which includes a heterogeneous solderless integration of a compact packaged BLE chip (EYSHSNZWZ, size: 8.5 mm x 3.25 mm x 0.85 mm) with integrated antenna, an sEMG front-end die (RHD 2216) that supports processing of 16 sEMG bipolar channels, Si capacitor dies of 10 nF and 100 nF, twenty circular electrodes (Ø = 6 mm) with 6 mm spacing and a 10 mm x 10 mm reference electrode on FlexTrate^{TM} across a compact (75 mm x 45 mm x 1 mm) device size. The FlexsEMG of 1 mm thickness was needed to integrate the BLE chip of 0.85 mm thickness.

4.4.1 Fabrication

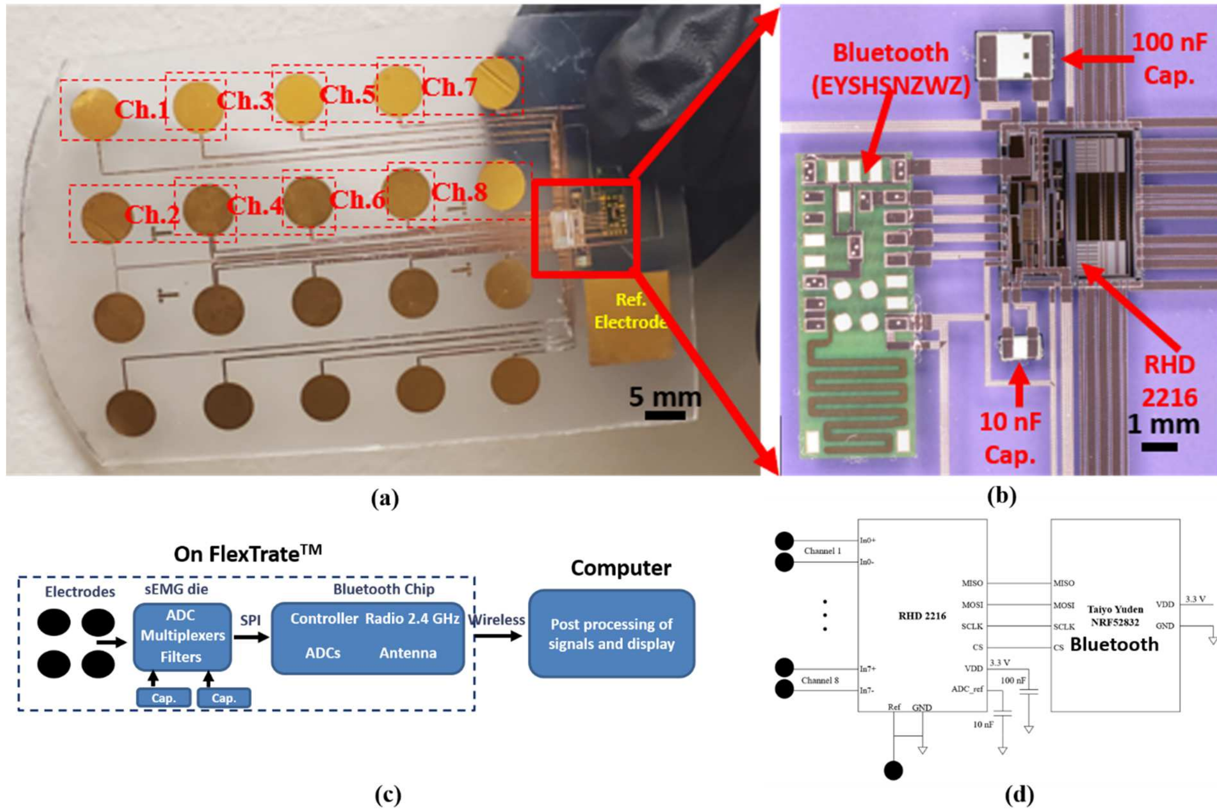


Figure 4. 10. (a) Fabricated FlexsEMG system, (b) magnified image of integrated electronics, (c) simplified block diagram of the system, and (d) circuit diagram of the system.

The standard process flow for FlexTrate™ fabrication was followed to demonstrate the multi-channel FlexsEMG system [27, 28]. Figs. 4.10 (a) and (b) show the fabricated FlexsEMG system and a high magnification image of the integrated electronics, respectively. There were multiple extra electrodes for redundancy (Fig. 4.10 (a)). The sEMG front-end die (size: 4.8 mm x 4.1 mm x 0.2 mm) was integrated instead of its packaged version (size: 8 mm x 8 mm x 0.85 mm) as there was the benefit of ~14X reduction in volume. A simplified block diagram and the circuit diagram of the system are shown in Figs. 4.10 (c) and (d), respectively. The FlexsEMG electrodes were

made of 5 μm electroplated Cu to provide reduced impedance and were capped with 20 nm/200 nm Ti/Au to ensure biocompatibility of the electrodes. The electrodes were engineered to have vertical corrugations that increase their surface area and flexibility. These electrodes contacted the skin directly without the use of messy gels that sometimes produce allergic reactions and degrade over time. Figs. 4.11 (a) and (b) show the FlexsEMG bent to a small bending radius and rolled on itself, respectively. A 70 mAh rechargeable battery was connected to the FlexsEMG system with the help of double-side Cu tape with conductive adhesive and the FlexsEMG system was attached to a subject's bicep muscle with the use of a waterproof adhesive (Tegaderm™), as shown in Fig. 4.12 (a) and (b), respectively. The overall FlexsEMG system weighed just 4.9 g.

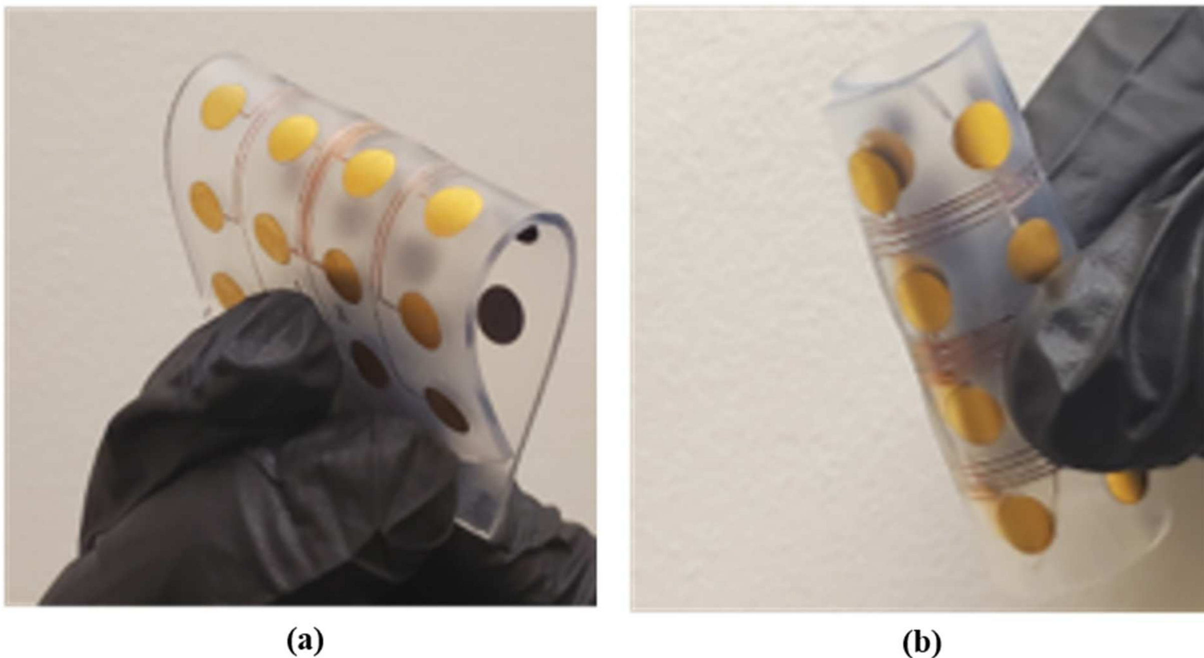
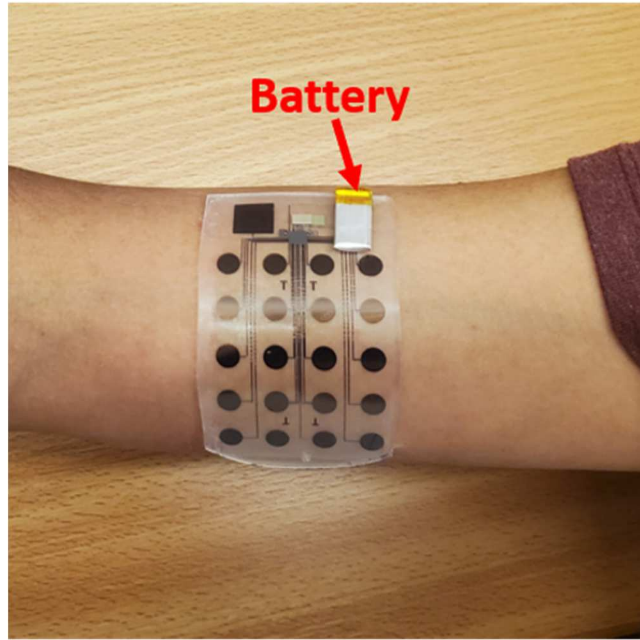


Figure 4. 11. Image of the FlexsEMG system being (a) bent and (b) rolled.



(a)

(b)

Figure 4. 12. FlexsEMG with the battery placed on the biceps (a) before and (b) after applying skin adhesive.

4.4.2 Results

Figure 4. 13. Subject holding a 4.5 kg load.

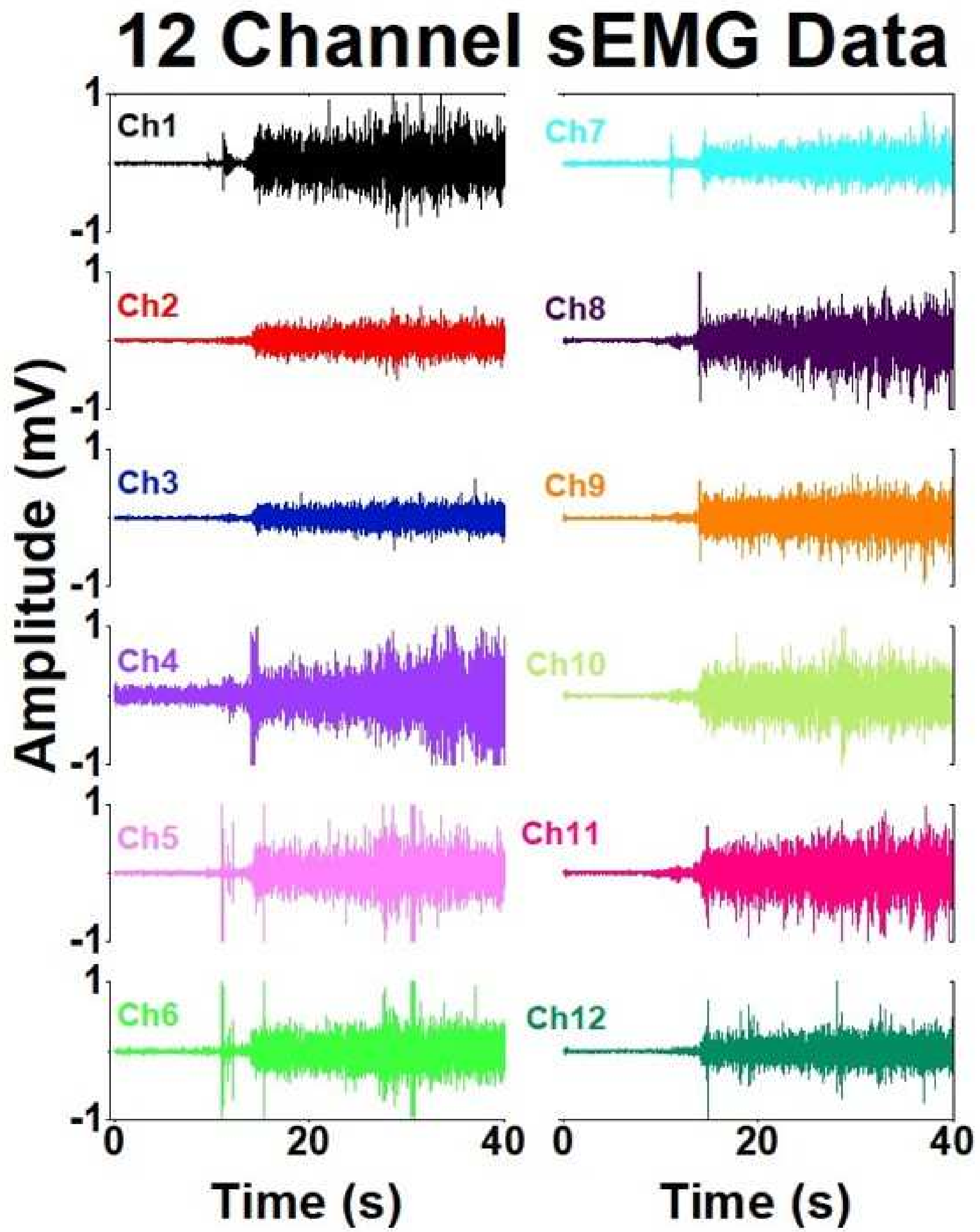


Figure 4. 14. The voltage vs. time recording of 12 bipolar channels from the FlexsEMG system.

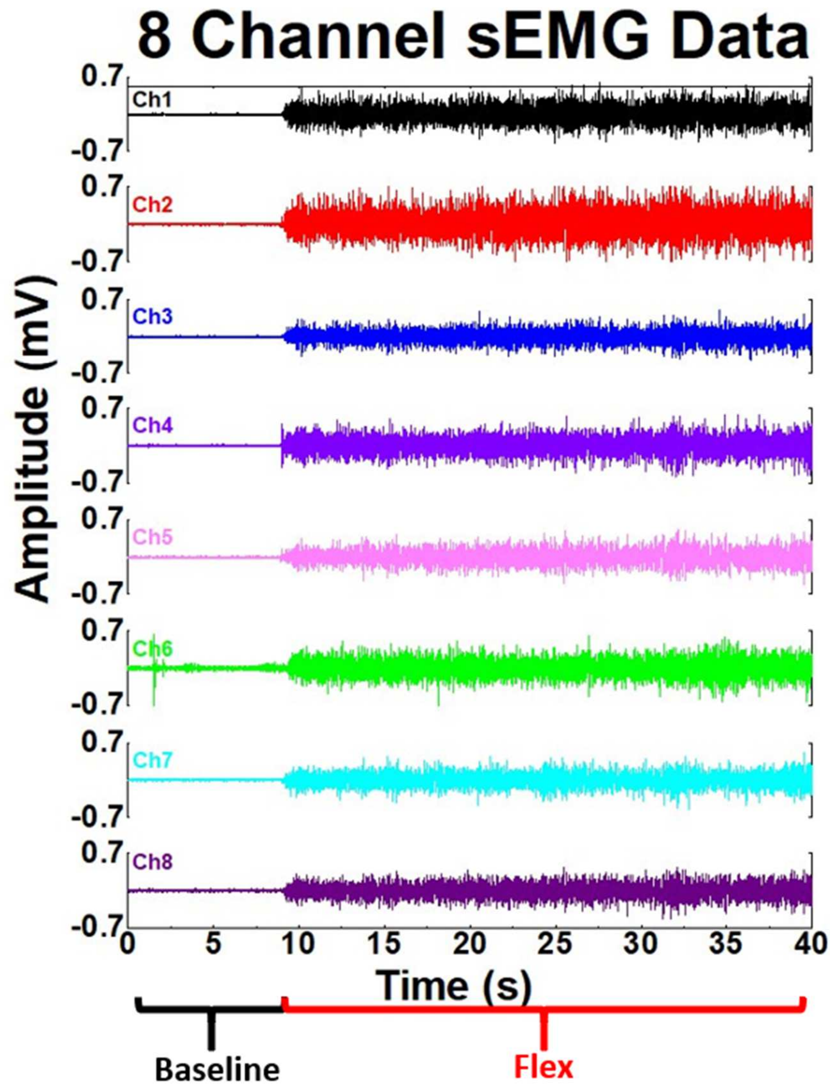


Figure 4. 15. The voltage vs. time recording of 8-bipolar channels from the FlexsEMG system.

The seated subject had the bicep muscles relaxed for 10 s and then held a 4.5 kg load for 30 s as shown in Fig. 4.13. The motor activation at the biceps brachii muscles was recorded before and during the hold using the FlexsEMG. The sEMG front-end die was programmed to record from 12 channels with each channel passing through a 5-100 Hz 1st order high and 3rd order low Butterworth filter at a 500 samples/s sampling rate, where each sample was of 16 bits. The sEMG signals received from the FlexsEMG were further passed through an 8th order 60 Hz notch filter to

remove the 60 Hz supply noise. The sEMG signals recorded are shown in Fig. 4.14 with average SNR of 22 dB during the flexed period. These low sampling sEMG signals can be used for applications of gesture recognition [13]. The sEMG signals were then recorded from just the 8 channels at higher sampling of 900 samples/s and each channel was passed through 5-300 Hz filter on the FlexsEMG system followed by a 60 Hz notch filter off the FlexsEMG. The subject repeated the experiment and the sEMG signals were recorded, as shown in Fig. 4.15 with average SNR of 23.2 dB during the loaded period. The sEMG signal strength, mean frequency (MNF), and MFCV were further analyzed.

4.4.2.1 Muscle signals over time

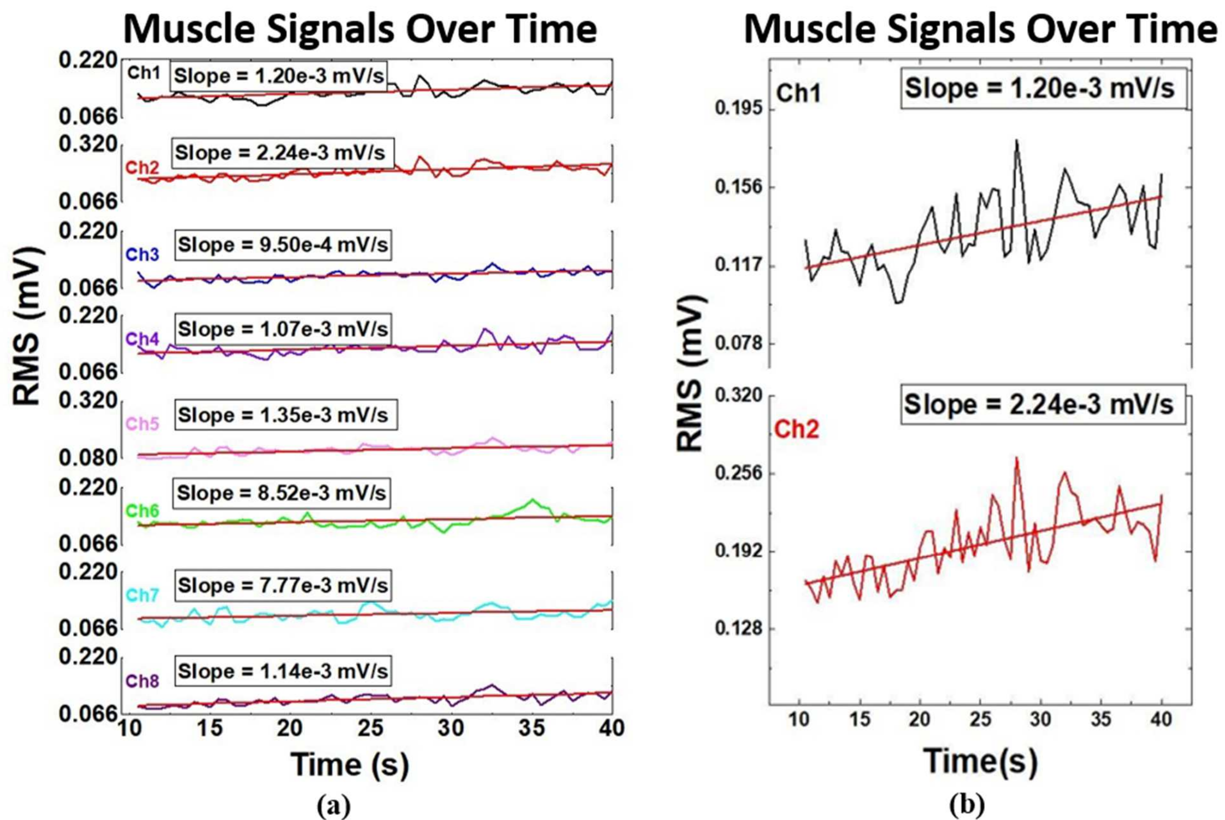


Figure 4. 16. sEMG signal over time plot of the (a) 8 recorded sEMG channels and (b) magnified plots of Ch. 1 and Ch. 2 while the subject held a load.

The RMS of the sEMG signal is a widely used time-domain feature to analyze the sEMG signals. The RMS of the sEMG signal was calculated at 500 ms epochs throughout the contraction ((Figs. 4.16 (a) and (b)). The RMS of each sEMG channel had an upward trend from the start-to-end of the contraction with an average slope of 1.2e-3 mV/s. In the case of isometric contractions, the amplitude of the EMG signals has been shown to increase with time along with an increase in the signal period [7]. This upward trend is caused by the need for higher muscle fiber recruitment in order to maintain a constant force over a period of time.

4.4.2.2 Mean frequency (MNF)

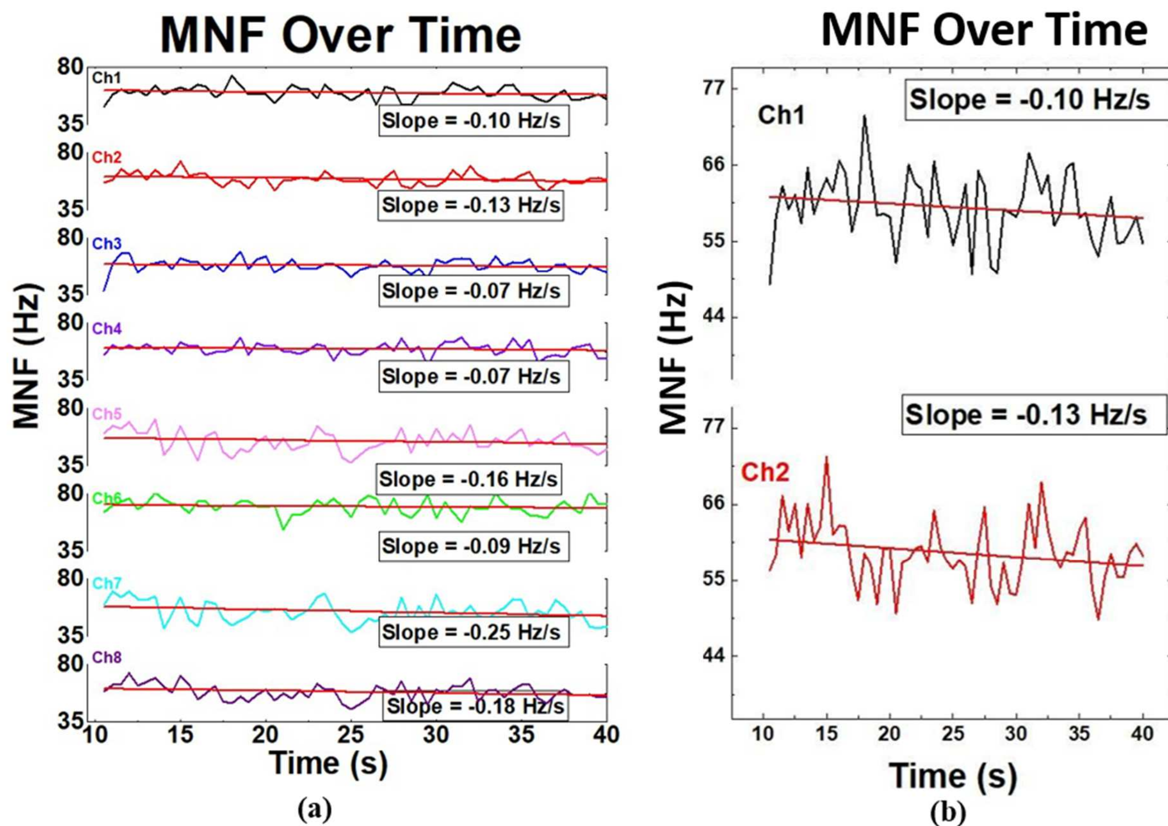


Figure 4. 17. MNF vs. time plot of the 8 sEMG channels and (b) magnified plots of Ch. 1 and Ch. while the subject held a load.

While time-domain analysis shows how the amplitude of sEMG signal changes over time, the frequency domain transforms the signal into multiple bands of frequencies. The height of each band showcases how much signal lies in that particular frequency range. This transformation is done using a Short Time Fourier transform (STFT). During a fixed load isometric contraction, it has been shown that the myoelectric power spectrum distribution changes over time [7]. With constant exertion, a decrease in the power of the high-frequency region is observed alongside an increase in power of the low-frequency region [7].

The MNF was calculated at the same 500 ms epochs (Figs. 4.17 (a) and (b)). In all 8 sEMG channels, a downward trend was identified in the MNF throughout the flexed period, thus indicating a shift to lower frequency values over time. The MNF varied with the linear fit slopes ranging from -0.25 Hz/s to -0.066 Hz/s, with an average slope of -0.13 Hz/s.

4.4.2.3 Muscle fiber conduction velocity (MFCV)

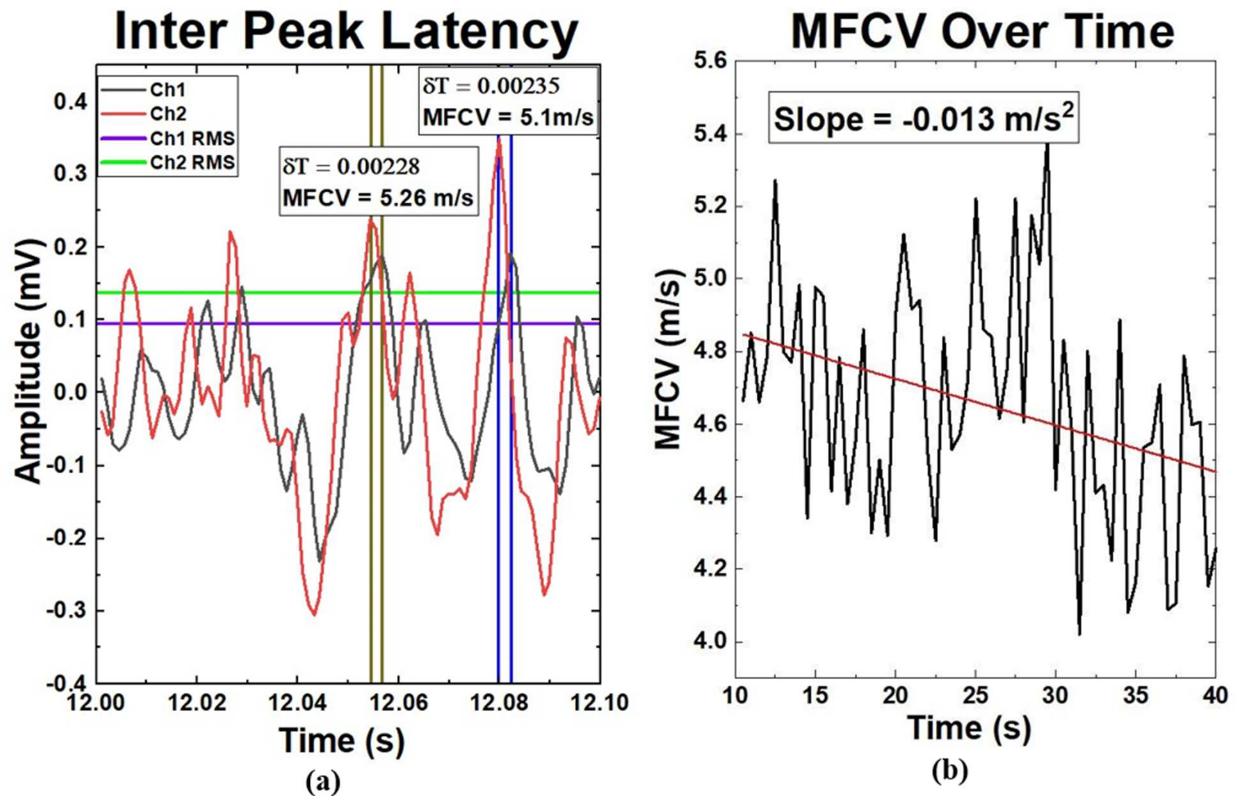


Figure 4. 18. (a) Amplitude vs. time plot for two sEMG channels for evaluating MFCV by Interpeak Latency Method and (b) change in MFCV vs. time while the subject held a load. MFCV was calculated at 500 ms intervals.

MFCV refers to the speed of an action potential as it travels through muscle fibers [15]. In the case of sEMG, this speed is the time delay between signals of two linearly positioned electrodes, divided by the inter-electrode distance. As stated earlier, multi-channel sEMG is needed for calculating MFCV. In fatigue studies, a reduction in the myoelectric power is often seen as a sign of diminishing conduction velocity, often associated with a higher power for lower frequency and a shift to lower powers for higher-frequency signals in the frequency domain [7]. The Interpeak Latency Method was used to evaluate the MFCV from channels 1 and 2 [12]. Fig. 4.18 (a) shows

an example of sEMG signals of channel 1 and channel 2 over 100 ms used to evaluate the MFCV. For each 500 ms block, a mean of the MFCV was calculated, as shown in Fig. 4.18 (b). The calculated MFCV ranges from 4.02 m/s to 5.4 m/s with a mean of 4.66 m/s and agrees with the values in the literature [12]. Over the course of the contraction, the MFCV decreased with the slope of -0.013 m/s^2.

4.4.3 Comparison with other systems

Most of the common sEMG systems today have a rigid and bulky hub that contains the battery and the electronics for processing of the signals, wirelessly communicating the signals to an external receiver for further post processing and analysis. The systems that allow multi-channel sEMG acquisition become much bulkier in size to accommodate for larger number of electrodes. Such large and rigid systems are not comfortable nor practical to wear over a long time. A few wearable wireless sEMG systems such as the MC10 Biostamp and Skintronics from Kim et. al. have demonstrated fully flexible sEMG systems [19, 20]. However, both these approaches use bulky packaged chips and non-flexible solder or anisotropic conductive paste (ACP) to make connection between the packaged chips and the PCBs that limits their overall flexibility. Moreover, such systems are single-channel systems that limit the detailed analysis of the muscles and do not allow for evaluation of MFCV. We have demonstrated a wearable wireless multi-channel sEMG system that is also flexible. Our multi-channel FlexsEMG system provided spatial filtering by measuring a single muscle activity or a group of muscle activities from multiple electrodes placed over the area of interest. It also allowed the evaluation of MFCV. Table 4.1 compares some of the sEMG systems to our FlexsEMG system.

	MC10 BioStampRC [19]	Y-S Kim et al. [20]	This work "FlexsEMG"
Fabrication Tech.	Modular PCB	Flexible PCB	Flexible FOWLP
Channels	Single	Single	Multi-channel (Up to 16)
Area (mm^2)	66 x 34	~50 x 30	74 x 45
Area per channel (mm^2) (Normalized to FlexsEMG)	2244 (10.8X)	1500 (7.2X)	208.125 (1)
Solder/ACP free	No	No	Yes
Interconnect pitch (μm)	> 100	> 100	≤ 40
Electrodes	Ø = 10 mm (wet)	10 mm x 10 mm (dry)	Ø = 6 mm (dry)
Additional hardware	IMU, memory, power management	IMU, memory, power management	To be added

Table 4. 1. Comparison of sEMG system with our FlexsEMG system.

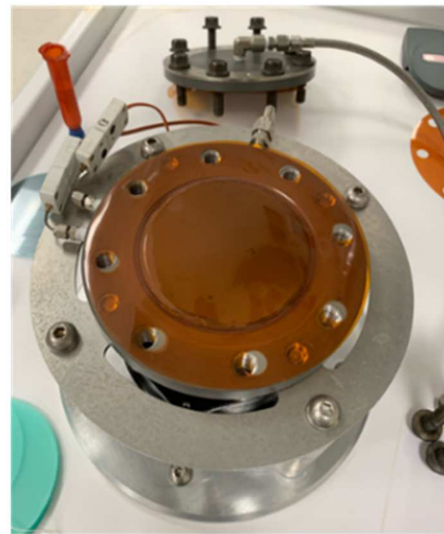
4.5 Manufacturing with i3 Microsystems

4.5.1 Fabrication of FlexTrate^{TM}

Towards the manufacturing process, we partnered with i3 Microsystems for the manufacturing of the FlexsEMG system. i3 Microsystems has established the PDMS molding process using an onsite lamination system, as shown in Fig. 4.19 (a) and (b). They have been able to optimize the steps of placing thermal release tape on 1st handler, picking and placing dies on the 1st handler, use 0.5 mm thick and 100 mm diameter stainless-steel ring to provide thickness to the FlexTrate^{TM} sample, dispense PDMS on the 1st handler, place the 2nd handler with another thermal release

adhesive and compression mold the system in the laminator tool to allow curing of PDMS at 40 □ for 4 hours. The lamination station can process 3 samples at once. Post curing, they heat the system to release the 1st handler, and have the dies integrated on the 2nd handler. The samples were then sent to UCLA to complete the build-up process. Fig. 4.20 (a) shows the process flow of FlexTrate^{TM} and highlights the collaborative work done by i3 Microsystems and UCLA.

(a)



(b)

Figure 4. 19. Image of (a) the complete laminator system and (b) individual laminator unit developed at i3 Microsystems for compression molding PDMS as part of FlexTrate^{TM} manufacturing.

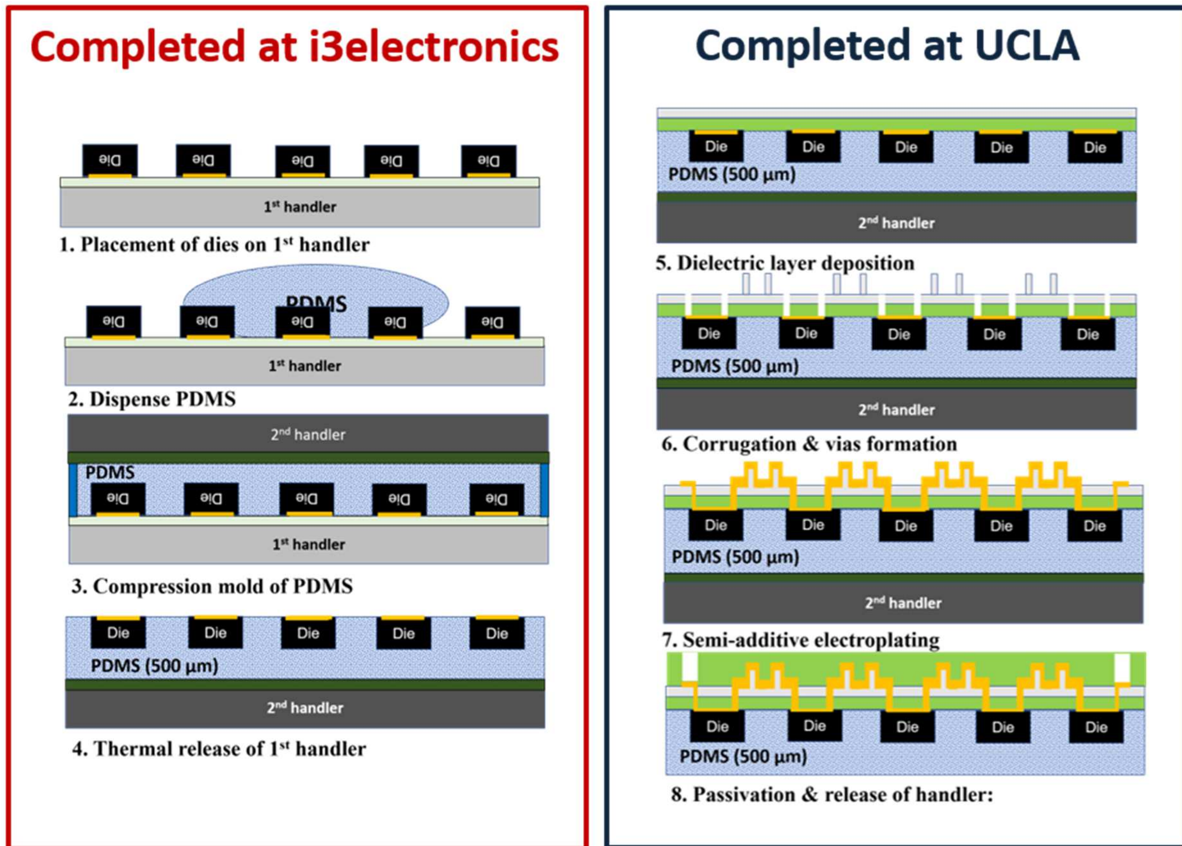


Figure 4. 20. The process flow of FlexTrate^{TM} and highlighting the collaborative work done by i3 Microsystems and UCLA.

4.5.2 Results

The 1 mm^2 Si dies placed by i3 Microsystems were fabricated and provided by UCLA. The Si dies were placed in 5 x 5 array at 1.8 mm pitch.

4.5.2.1 Die shift

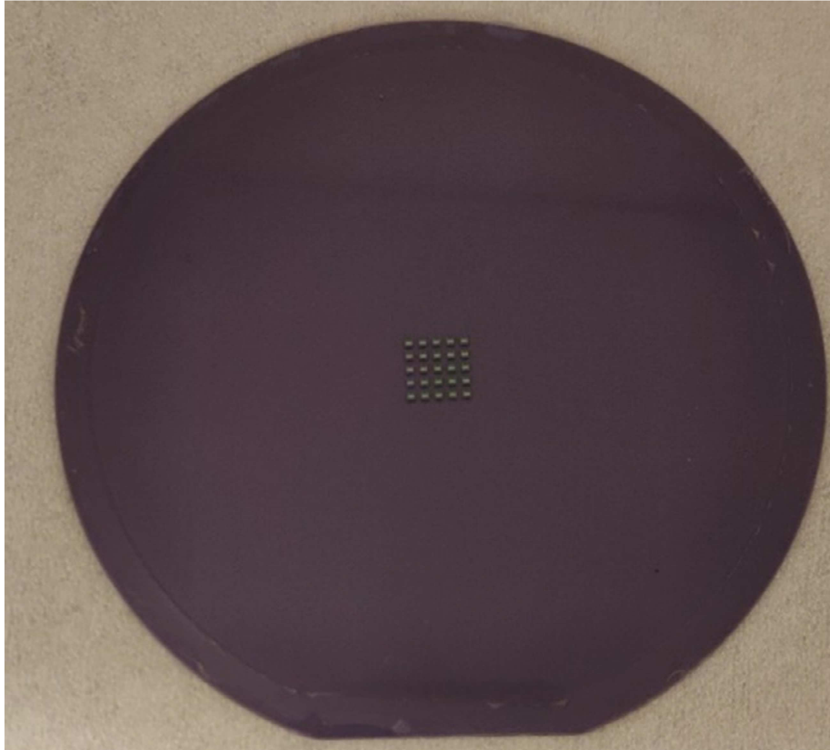


Figure 4. 21. The image of the sample with 5 x 5 array of dies received by UCLA.

Row/Column number	1	2	3	4	5
1	0.869828	1.2018	0.913105	0.593718	0.454178
2	0.683474	1.215936	**2.335732**	0.633921	0.34994
3	0.292252	0.721539	0	0.467189	0.665562
4	**2.853674**	0.803334	1.437668	0.925263	0.297406
5	1.874216	0.794284	0.549118	1.125307	1.412129

Table 4. 2. Die shift analysis on the FlexTrate^{TM} sample fabricated by i3 Microsystems, post release of the 1st handler.

The image of the sample with 5 x 5 array of dies received by UCLA is shown in Fig. 4.21. The die shift analysis on the sample after release of the 1st handler was done at UCLA, with the help of the

Nanotronics tool (nSpec®). The maximum die shift was measured to be < 3 µm, as shown in Table 4.2, which were satisfactory to demonstrate 40 µm pad pitch integration on the FlexTrate^{TM} sample.

4.5.2.2 Interconnections at 40 µm pad pitch

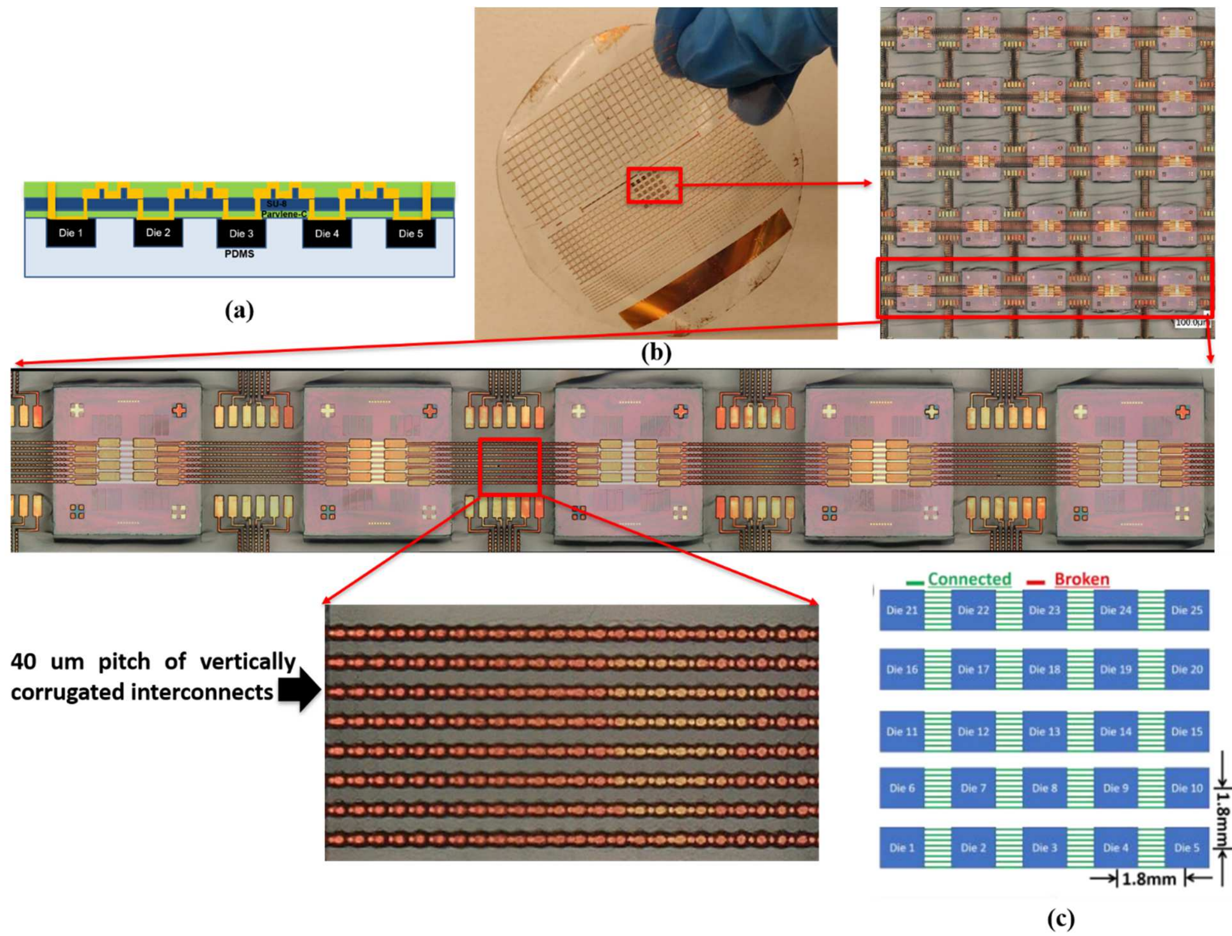


Figure 4. 22. (a) Schematic of the FlexTrate^{TM} sample. (b) Image of FlexTrate^{TM} sample after release of 2nd handler. (c) Schematic of the electrical connections post-testing.

The schematic of the daisy chain connection across the dies is shown in Fig. 4.22 (a). The sample post metallization to demonstrate 40 µm pad pitch integration across 5 x 5 array of Si dies and post

release of the 2nd handler is shown in Fig. 4.22 (b). All the daisy chain connections across the dies were connected, as shown in the schematic in Fig. 4.22 (c).

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5. Conclusion

5.1 Summary

1. A flexible FOWLP platform called FlexTrate™ was demonstrated for heterogeneous integration of high-performance dies in a flexible and biocompatible elastomeric package. FlexTrate™ was demonstrated to be bendable to 1 mm bending radius for thousands of bending cycles with minimal degradation in the system's electrical performance.
2. FlexTrate™ with two metallization layers at 40 µm interconnect pitches was shown to be bendable to 1 mm bending radius for over 3000 bending cycles, demonstrating its extreme flexibility.
3. A 10 × 20 array of 1 mm^2 dies and a foldable display with 42 InGaN LED dies were integrated on the FlexTrate™. Both the systems had fine pitch (40 µm) corrugated interconnects and were successfully bent down to 1 mm bending radius for over 1000 bending cycles.
4. The 6 mm diameter electrodes on FlexTrate™ capture as good SNR as Ag/AgCl electrodes. The electrodes passed multiple reliability tests with no significant change in resistance, such as a bending test of 0.5 mm bending radius for over 1000 bending cycles, a temperature-humidity test (85 □/85%RH) for > 500 hours, a thermal-cycling (-40 □-125 □) test for > 30 cycles, and a saline-immersion test in PBS at room temperature for > 200 hours.
5. A fully flexible 12-bipolar channel solderless sEMG system using flexible FOWLP was demonstrated. The system can be attached to the skin to record quality sEMG signals through dry electrodes and transmit data via Bluetooth. The ability to acquire these signals

through FlexsEMG in a mobile setting is critical for the study of many muscular physiological phenomena and disorders.

6. Initial promising results of manufacturing of FlexTrate™ with i3 Microsystems were demonstrated. Towards the manufacturing process of FlexTrate™, i3 Microsystems has established the PDMS molding process using an onsite lamination system, and have been able to optimize several steps: placing the thermal release tape on the 1st handler, picking and placing dies on the 1st handler, using 0.5 mm thick and 100 mm diameter stainless-steel rings to define the thickness of the FlexTrate™ sample, dispensing PDMS on the 1st handler, placing the 2nd handler with another thermal release adhesive, compression molding the assembly in the laminator tool in which PDMS is cured at 40 □ for 4 hours, and releasing the 1st handler post cure. The RDL build-up process was completed at UCLA to demonstrate 40 μm pad pitch integration across a 5 x 5 array of Si dies. The work towards complete manufacturing of FlexTrate™ by i3 Microsystems at their facilities is on-going.
7. The FlexTrate™ platform could potentially enable next generation heterogeneous, flexible/implantable, high-performance systems, such as multi-channel sEMG system, optogenetics for neural implants, and so on.

5.2 Outlook

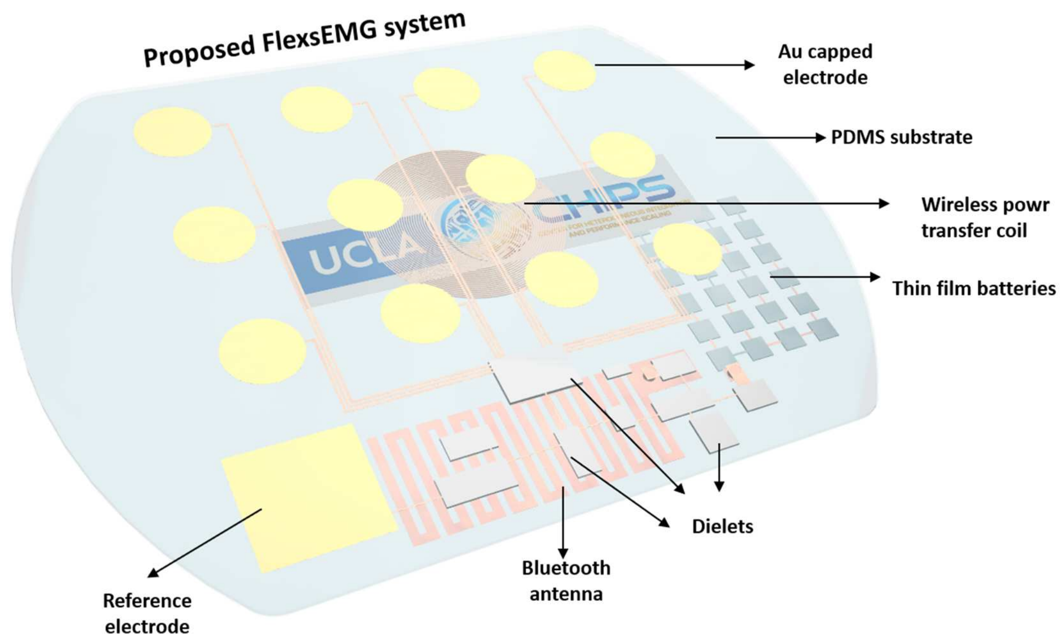

Figure 5. 1. Schematic of the proposed two-sided (3D) integrated FlexsEMG system.

A fully flexible multi-bipolar channel solderless sEMG system called "FlexsEMG" has been demonstrated. Our group has received the Institutional Review Board (IRB) approval to test our FlexsEMG device on human subjects but have not yet been able to fabricate a sufficient number of units to do reasonable field studies to establish user comfort and reliability. In addition, we will be incorporating several enhancements based on initial user feedback. The schematic of the proposed FlexsEMG system is shown in Fig. 5.1. It is a two-sided (3D) integrated system and will include the following:

1. Front-end sEMG data processing system that supports amplification, programmable high- and low-pass filtering, and digitization of sEMG signals from up to 12 bipolar channels.
2. Up to twenty gold-capped vertically corrugated flexible dry high-performance high-density electrodes.

3. Bluetooth Low Energy (BLE) system and antenna for wirelessly transmitting the sEMG signals.
4. Rechargeable ultra-thin power sources, power management system, and wireless charging capabilities.
5. An Inertial measurement unit (IMU) with accelerometers, gyroscopes, and magnetometers.
6. Additional integrated memory for data storage – this has the potential to reduce power significantly
7. Ergonomic reusable adhesives for ease of attachment
8. An edge-based AI accelerator as well as a suite of AI/ML algorithms will be developed for biomarker discovery, gesture recognition, power optimization and therapeutic enhancement in both clinical and non-clinical settings.

Moreover, all the CMOS ICs will be integrated in bare die form and will be provided by our industry partner, i3 Microsystems. The integration of bare dies instead of packaged chips enables an overall smaller area and much more physical flexibility to the fabricated device. Also, the removal of wires along with the capability to reprogram the band pass filters in our FlexsEMG system will help to manage the motion artifacts, potential cross talk, and ambient electrical noise.